INTEGRATED MEMS MICROSENSORS

by

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Dedicated To

My loving mother Ramanamma Chitteboyina, my father Moulali Chitteboyina, and in memory of my Late grandmother Panga Subbamma.

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ABSTRACT

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Many Micro-Electro-Mechanical Systems (MEMS) products have been commercialized at a fraction of the cost and size of conventional devices. Low cost, small sizes and multi-function are the ultimate objectives of commodity MEMS devices. An intelligent micro-system requires that the processing circuitry, sensors, and actuators be integrated on the same chip. Integrated MEMS can improve performance of the overall product in several applications. In this work integrated MEMS devices are investigated through semiconducting Yttrium Barium Copper Oxide (YBaCuO) microbolometer arrays on complementary metal oxide semiconductor (CMOS) substrates, a novel tunable infrared microspectrometer, and a novel device-level packaging technique for MEMS resonators.

YBaCuO microbolometers are integrated with CMOS readout circuits using CTIA (Capacitive Transimpedance Amplifier) design technique in AMI 1.5μm double-poly-double-metal n-well 2.5V CMOS technology. The thermal isolation of the self-supporting micromachined YBaCuO microbolometers is varied by designing two different electrode arm geometries. The first geometry is designed to obtain a relatively fast 200 Hz frame rate while maintaining moderate detectivity. The second arm geometry is designed to achieve a traditional 30 Hz frame rate with high detectivity microbolometers. The design of a novel tunable, microspectrometer, based upon Bragg diffraction grating structure, capable of operating in the infrared region (1 μm to 10 μm) of the optical spectrum is also presented. The tunability of the microspectrometer is achieved by changing the position of the perfect conductor placed below the dielectric waveguide grating structure. Many MEMS devices require expensive vacuum packaging. MEMS resonator is one example where the Q-factor of the resonator depends upon the pressure of the vacuum; such a device, therefore, serves as a good test-bed for "growing your own package". At present, the packaging cost of these MEMS resonators is 70-80% of the total cost of the final MEMS product. A ground-breaking device-level packaging technique for these MEMS resonators that would satisfy all the standards set by International Technology Roadmap for Semiconductors (ITRS) 2005 and cut down the cost of the overall MEMS product drastically has also been presented.

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CHAPTER 1

INTRODUCTION

1.1 Introduction to Micro-Electro-Mechanical Systems

Since the invention of the monolithic integrated circuit (IC), most electronic and optoelectronic integrated circuits have been fabricated on semiconductor and glass substrates. The constraint to monitor and control many of the complex processes that are involved in the real world has led to the need of intelligent micro-systems called micro-electro-mechanical systems (MEMS). Micro-Electro-Mechanical Systems (MEMS) technology can be viewed as a fabrication technology for manufacturing micro and nanoscale devices. The history of MEMS is reliant on a broad range of novel micromachining processes developed by the IC industry, which has primarily changed the world economy and the way our society lives. In the year 1959, physicist Richard Feynman gave a famous talk[1] entitled, “There's plenty of room at the bottom” at an American Physical Society meeting at Caltech, describing nanotechnology as an important field for the future. In this talk, he explained in detail on the benefits to be gained by making things small. These benefits included higher spatial resolution, higher operating speeds, and the ability to batch-fabricate things.

The majority of the MEMS fabrication techniques can be categorized into surface micromachining and bulk micromachining. Surface micromachining[2] performs additions and subtractions of thin films made of materials such as silicon dioxide, silicon nitride,

polysilicon, aluminum, gold by photolithography, thin-film deposition techniques, plasma etching and wet etching. Bulk micromachining[3] mostly reshapes the silicon substrate with different crystal orientations underlying the thin-film structures. Deep reactive ion etching and wet anisotropic silicon etching are among the most commonly used bulk micromachining tools to create high aspect ratio structures.

A few key milestones in the development of IC micromachining and MEMS technologies are cited as follows. The planar batch-fabrication process was invented in the year 1960. The resonant gate transistor, produced by Nathenson at Westinghouse in the year 1967, was the first batch-fabricated MEMS device[4]. The first micromachined accelerometer was developed at Stanford University in the year 1979. The commercialization of MEMS started in the year 1980s by several automotive companies. Microhinges were developed at the University of California, Berkeley in the year 1991 by Pister et. al.[5] making it possible to build large structures out of the plane of the substrate, giving MEMS significant access to three-dimension. In the past few decades, while employing batch-fabricating techniques and the economies of scale successfully exploited by the IC industry, the MEMS market is growing dramatically with predicted values in the $27 Billion by the year 2007[6]. Beyond 2007, growth is expected to continue as new applications and products are developed and global market penetration continues.

MEMS usually consist of released mechanical structures that are anchored, suspended and set into motion by mechanical, thermal, acoustical or photonic energy sources. MEMS devices are very small, in the order of microns. This offers many advantages. First, a lot of structures can be packed in one small area, reducing the overall cost. Second, smaller devices consume less power because they have very little inertia

and the losses are negligible. Last, but not the least, MEMS uses fully developed and readily available fabrication methods for patterning, depositing, and etching layers in the IC industry. This means that the existing equipment and fabrication techniques can be used for MEMS fabrication, making possible the mass production of MEMS chips.

A majority of MEMS research is to develop complex systems integrated with IC, sensors and actuators. Research on the field of micromachined sensors and actuators in the engineering world can be traced back as early as the 1980's. Kurt Petersen published the first impressive review of application of silicon as mechanical material, more than the electronic material in 1982[3]. Almost at the same time, R. T. Howe proposed techniques to fabricate microbeams from polycrystalline silicon films using technology developed from building microelectronic devices for the integrated circuits. It was in the year 1984 that Roger Howe and Richard Muller published their work demonstrating a resonant vapor sensor fabricated using an integrated polysilicon process. It was the first prototype polysilicon MEMS device, a chemical vapor sensor which was a fully integrated microelectromechanical system[7]. Since then, MEMS technology has found applications on building various types of sensors and actuators.

MEMS market is growing dramatically with commercially successful MEMS devices and systems including microsensors, microactuators, micromirrors, microrelays, and microsystems. One particular topic of great interest to this dissertation is integrated MEMS microsensors. A microsensor is commonly used to describe a miniature device that converts a non-electrical quantity, such as pressure, temperature, or gas concentration, into an electrical signal. Small size, multi-function and low cost is the ultimate goals of commodity MEMS microsensors.

In the most integrated of systems, it includes entire analog and digital circuit systems for stabilizing, controlling and reading out the information content of the MEMS device. The requirement of separate signal-conditioning circuitry, which in turn requires multi-chip assembly, makes the packaging of MEMS devices complicated and expensive. In the case of an array of devices, on-chip multiplexing circuitry can control the entire array through only a handful of bond pads. An intelligent micro-system requires that the processing circuitry, sensors, and actuators be integrated on the same chip. MEMS have been developed for use in many sensing applications over the past few decades.

Clearly integrated MEMS can improve performance in several sensor applications. This dissertation's focus is on three aspects of integration of MEMS microsensors. The fabrication of complementary metal-oxide-semiconductor (CMOS) compatible semiconducting Yttrium Barium Copper Oxide (YBaCuO) microbolometer arrays, a novel tunable infrared microspectrometer, and a novel device-level vacuum-packaging technique for MEMS resonator is presented in this dissertation. In the case of CMOS compatible semiconducting YBaCuO microbolometer arrays, the microbolometers are the MEMS microsensors sensing the infrared radiation and producing an output signal corresponding to the incident radiation. In the case of a tunable infrared microspectrometer, the infrared detector is the microsensor which senses the power radiated from the dielectric waveguide grating structure. In the case of vacuum-packaged MEMS resonator, the resonator is the microsensor since its quality factor Q depends on the pressure in the vacuum-cavity.

1.2 Semiconducting YBaCuO uncooled focal plane arrays

Infrared focal plane arrays (IRFPA's) are needed for a variety of defense applications such as missile targeting, night vision, surveillance, and security; as well as in biomedical instrumentation. Older-generation IRFPA devices require cryogenic cooling to improve sensitivity and signal-to-noise, which in turn limits the portability and increases the cost of cameras made from these devices. Microbolometric IR sensors have been introduced more recently to reduce the need for cooling. In these devices, the absorption of IR radiation causes a rise in the temperature of a microscopic resistor. The rise in the temperature produces a corresponding change in the resistor's value which can be detected electrically. Uncooled infrared detectors have fascinated considerable attention in recent years because of its high quality imaging with reduced cost, weight, and system size than compared to cooled infrared detectors. Recently uncooled infrared detectors have emerged to replace cryogenically cooled infrared detectors in a number of applications in addition to motivating the development of new applications[8,9]. In reference [8], the focal plane array and the electronics within the camera were designed as an integrated unit to meet a broad range of end user applications by providing features such as non- uniformity, correction, autogain and level, NTSC, PAL video and digital outputs. These features made possible economical digital IR imagery for quantitative as well as qualitative medical applications. A few years ago, Mitsubishi Inc produced a semiconducting Yttrium Barium Copper Oxide (YBaCuO) infrared focal plane array utilizing an amorphous-Si sacrificial layer[10], a thin metal film absorber, and encapsulated the detector with silicon nitride. The Mitsubishi work demonstrates the basic feasibility of YBaCuO IR focal plane arrays. The YBaCuO thermometers fabricated by Mitsubishi

displayed significantly higher resistivity (90 Ω-cm) than the YBaCuO thermometers fabricated (5-20 Ω-cm) by P. C. Shan et al[11]. The use of low resistivity YBaCuO makes the interface with the readout circuit easier. Also, wet etching of amorphous silicon can result in hydrostatic stiction problems. DRS Infrared Technologies have reported uncooled 15-60 Hz frame rate infrared cameras[12] with Vanadium Oxide (VO_x) as the detector material.

This dissertation investigates the integration of self-supporting, low resistivity, low thermal mass, sacrificial polyimide based YBaCuO infrared sensors (microbolometers) with a capacitive transimpedance amplifier (CTIA) readout circuit based on a constant voltage (CV)[13,14,15] technique. The importance of this research is that it would provide a great potential for imaging at a fast frame rate (200 Hz) or with greater sensitivity. The method of fabricating self-supporting semiconducting YBaCuO microbolometers on CTIA CMOS readout circuit is novel. The microbolometers were patterned entirely by liftoff over a topologically rough substrate avoiding any damage that could have caused to the underlying circuits due to the use of acids.

1.3 Tunable Infrared Microspectrometer based on Bragg grating

At present, one-dimensional and two-dimensional optical filters operate at a fixed wavelength. One-dimensional optical filters or gratings have seen applications as transmission filters or spectrometers[16], as grating coupled quantum well infrared detectors to diffract the incident radiation away from normal incidence[17,18], surface emitters for laser diodes[19], and as a dielectric antenna similar to surface emitting lasers[20]. In reference [16], a new soft X-ray spectrometer covering the photon energy range of 50–500 eV was developed. It employs a free-standing transmission grating coupled to a

microchannel-plate detector. Its simplicity of operation makes the device attractive for applications such as the study of soft X-ray emission from laser-produced plasmas. The theory of the grating-coupled quantum-well infrared detector, based on the modal expansion method is presented[17] with numerical simulation results. Numerical simulations show that quantum efficiencies integrated with respect to wavelength may be obtained in a detector equipped with a crossed grating of square symmetry, and a waveguide. In reference [19], a circular-polarized (CP) reconfigurable grating antenna for low-cost millimeter-wave beam steering is presented. Using inertia-less mechanical movement, the grating design can be reconfigured along the surface of a dielectric image line, allowing a directive CP beam to steer across a wide range of angles. The results published are inherently scalable to higher millimeter-wave frequencies and have numerous uses in emerging millimeter-wave satellite communications applications and other related systems for mobile communications and radar. Two-dimensional optical filters or 2-D photonic band gap crystals have seen applications as filters[21] and antenna[22].

A substantial amount of research has been done towards the development of integrated optical circuits. Recently, laboratory-on-a-chip applications have been developed. One key component of laboratory-on-a-chip applications is an optical spectrometer that may be used for spectral analysis (composition and structure) in application such as gas monitoring. Several researchers have developed micromachined, optical spectral filters[23,24,25,26,27,28] that are capable of operating in the visible and near-infrared portion of the optical spectrum. The spectral filters generally utilize coupled filters, interferometry, or dispersion to separate radiation into its spectral components. In addition to the work mentioned above[23], a research group at Delft University of

Technology (Netherlands) has investigated several different spectral filter configurations including: A 16-channel Fabry-Perot Etalon spectrometer that utilized 16 different resonant cavity thicknesses formed by multiple lithography processes and pnp phototransistor detectors. The 16-channels covered the spectral range of 370 to 480 nm. A bulk-micromachined cavity spectral filter was investigated, that utilized a grating and propagation through the cavity to disperse the radiation and project it onto the detector array[22]. An infrared spectral filter that utilizes a diffraction grating to disperse the radiation and project it onto a thermopile detector array is mentioned[22], which serves as a good review of this groups' work.

Most of the one-dimensional and two-dimensional optical spectral filters fabricated to date are fixed in their spectral response and cannot be tuned. A literature survey reveals that most of the micromachined spectral filters have targeted the visible and near IR portion of the spectrum, utilizing photodiode or phototransistor optical detectors. In this dissertation, an innovative technique of tuning a highly efficient infrared microspectrometer based on Bragg diffraction grating structure that is capable of operating in the mid-infrared portion of the optical spectrum is presented. This novel invention is different from present technology in a way that it provides a method for electronically adjusting the center wavelength of the filter.

1.4 Vacuum-packaged RF MEMS resonator

MEMS on-wafer packaging has been recognized as the most promising technology for cost reduction of the overall MEMS product. In today's scenario, half of the MEMS market is microsensors and actuators. The packaging cost is 70 - 80% of the

total cost of a MEMS product. Packaging of MEMS devices is a big challenge in the present competitive integrated circuit industry.

Various low temperature monolithic thin-film packaging techniques have been demonstrated[29,30,31,32,33]. Low temperature is one of the preferences in the packaging process, especially in RF MEMS packaging where metal (e.g., gold or aluminum) is frequently used to build the devices and thus cannot withstand any high temperature processes. Also, if MEMS devices are to be integrated with CMOS circuits, low temperature packaging of the MEMS devices is highly desired to accommodate the thermal budget constraints of microelectronic components. An RF resonator was sealed by a PECVD film[29] following release of the sacrificial layer through the 0.25 µm vias in the cavity ceiling. The maximum processing temperature was 400 °C, allowing the integration of MEMS processes with the Bi-CMOS processes. Evaporated or sputtered thin films, which can be deposited at room temperature in vacuum equipment, are the candidates of sealing films in low temperature hermetic packaging. Mei et al.[30] demonstrated a vacuum microdiode device encapsulated inside a silicon nitride cavity sealed by evaporating silicon dioxide and aluminum. These devices are fabricated with an on-chip vacuum cavity through directional material sealing techniques initiated at vacuum pressure of $\sim 2\times10^{-6}$ T. Bartek et al.[31] used evaporated aluminum sealing as well as LPCVD polysilicon sealing to package a diode device in a silicon nitride membrane cavity. Stark et al.[32] developed a thin-film electroplated metal package featuring low process temperature (< 250 ^{o}C). An innovative approach[33] was demonstrated to obtain a sealed cavity with certain pressure of N_2 gas inside, an environment desired for a RF switch to achieve fast settling time during operation. A liquid encapsulant, with

appropriate surface tension value to ensure no wick into the cavity through the release hole, was applied over a released cavity by spin coating in a dry N_2 atmosphere. The liquid encapsulant was then cured at 250 °C to form a sealed shell over the switch.

None of the existing or developing, MEMS packaging technologies meet the specific standards set by International Technology Roadmap for Semiconductors (ITRS) 2005. This dissertation presents a ground breaking device-level packaging technique that would satisfy all the standards set by ITRS 2005, cutting down the cost of the overall MEMS products drastically, and hence getting access to consumer electronic goods at a much cheaper price. The novelty of the invention lies in the fact that the devices will be self-packaged (vacuum-packaged). The integrity of the packaging will be verified using the packaged device (sensor in this case) itself. The packaged device is the MEMS resonator.

My contribution to this dissertation can be summarized as follows:

- Design and fabrication of self-supporting semiconducting YBaCuO microbolometer arrays on Capacitive Transimpedance Amplifier (CTIA) CMOS readout circuit.
- Design of a Bragg grating based tunable infrared microspectrometer capable of operating in the mid-infrared region of the optical spectrum.
- Design, fabrication, and characterization of MEMS resonators.
- Design of two device-level packaging techniques for MEMS resonators.

CHAPTER 2

SEMICONDUCTING YBaCuO UNCOOLED FOCAL PLANE ARRAYS

2.1 Introduction

Infrared (IR) imaging technology has been developed for various applications including medical examination, astronomy, missile guidance, and other strategic equipment. The integration of commercial and military IR imaging systems is very challenging. This concept has led to the increasing research and development efforts in applying the commercial CMOS technologies for the design of IR imaging systems.

Since infrared radiation was detected, various infrared detectors have been developed to convert incident radiation into electrical signals. Sensors that detect infrared radiation are generally classified into two types, photon detectors and thermal detectors. Photon detectors operate using the photovoltaic effect or photoconductivity. Most infrared photon detectors are based upon HgCdTe devices or silicon Schottky barrier diodes. Photon detectors have really short time response; however they have to be embedded with a cryogenic cooling system which increases the overall cost. In contrast, thermal detectors operate by utilizing the heat generated by the absorption of the photon flux to change the temperature. The change in the temperature is associated with a change in measurable electrical property of the material such as electrical resistance (microbolometer) or spontaneous electrical polarization (pyroelectric detector). Thermal

detectors do not require expensive cryogenic cooling and hence they are called uncooled infrared detectors.

Recently uncooled infrared detectors have emerged to replace cryogenically cooled infrared detectors in a number of applications in addition to motivating the development of new applications[8,9]. Uncooled infrared detectors are becoming very attractive in a large number of applications such as night vision for security and policing, search and rescue, military, thermal imagery for firefighters (ability to see through smoke), industrial nondestructive test and inspection, radiometry and spectroscopy applications in space sciences and medicine. Thermal detectors can operate over a large optical bandwidth, extending from the ultraviolet to microwave frequencies, limited only by the ability to absorb the incident radiation[34,35].

2.1.1 Foundation

Our research group has pioneered the semiconducting phase of $YBa_2Cu_3O_{6+x}$ (Yttrium Barium Copper Oxide) thin films for uncooled infrared detection applications[11]. For $0.3 \le x \le 0.5$, $YBa_2Cu_3O_{6+x}$ behaves as a semiconductor. Semiconducting YBaCuO has high temperature coefficient of resistance (TCR), typically greater than -3%K^{-1} at 290K, relatively low 1/f noise[36], and the ease of fabrication by rf magnetron sputtering at room temperature from single, composite, commercially available targets.

A figure of merit for detector performance, voltage responsivity, R_v, is defined as the amount of signal produced per unit radiation flux falling on the detector. For a bolometer the voltage responsivity is given by:

$$R_V = \frac{\eta\beta R I_b}{G_{eff}\left(1+\omega^2\tau_{th}^2\right)^{1/2}} \qquad (1)$$

where I_b is the bias current, R is the bolometer resistance, η is the absorption coefficient, G_{eff} is the effective thermal conductance to the substrate, ω is the radiation modulation frequency, τ_{th} is the thermal response time, defined by C_{th}/G_{eff} where C_{th} is the thermal capacitance, and β is the thermal coefficient of resistance given by $\frac{1}{R}\frac{dR}{dT}$.

The specific detectivity is an important figure of merit which normalizes the performance of the detector with respect to the detector area A_d and the noise per unit bandwidth. In case of a current biased detector, detectivity is expressed as:

$$D^* = \frac{R_V \sqrt{A_d \Delta f}}{\Delta V_n} \qquad (2)$$

where Δf is the electrical bandwidth and ΔV_n is the total noise voltage measured over Δf. Being area and noise normalized, the detectivity is more useful in comparing different detectors. The total noise in the detector is given as ΔV_n:

$$\Delta V_n = \sqrt{V_{1/f}^{\ 2} + V_J^{\ 2} + V_{TF}^{\ 2} + V_{BG}^{\ 2}} \qquad (3)$$

For small $\Delta f << f$,

$$V_{1/f} = \sqrt{\frac{\alpha_H V_{dc}^2 \Delta f}{Nf}} \qquad (4)$$

$V_{1/f}$ is the flicker noise or 1/f noise; α_H is the Hooge parameter, V_{dc} is the dc bias voltage across the detector, N is the number of fluctuations in the sample, f is the electrical frequency.

$$V_J = \sqrt{4kTR\Delta f} \qquad (5)$$

V_J is the Johnson noise; k is the Boltzmann's constant, T is the bolometer temperature (K).

$$V_{TF} = \frac{R_V \sqrt{4kT^2 G_{th} \Delta f}}{\eta} \qquad (6)$$

V_{TF} is the temperature fluctuation noise;

G_{th} is the thermal conductance of the detector (WK^{-1})

$$V_{BG} = \frac{R_V \sqrt{4kT^2 G_{rad} \Delta f}}{\eta} \qquad (7)$$

V_{BG} is the background noise;

where $G_{rad} \cong 8\varepsilon A_d \sigma T_o^{\ 3}$ is the radiative conductance of the material, T_o is the temperature of the heat sink (K), σ is the Stefan-Boltzmann's constant ($5.67x10^{-12}$ $W/(cm^2K^4)$) and ε is the detector emissivity (assumed equal to absorptivity at all wavelengths).

The first generation YBaCuO microbolometers were fabricated with YBaCuO infrared sensitive element deposited on top of SiO_2 or Si_3N_4 bridge structure[37]. The optimum speed and detectivity characteristics were not realized due to the large thermal mass of the detector. The second generation microbolometers were developed with the YBaCuO infrared material being self-supported[38]. The self-supporting microbolometers exhibit low thermal mass that results in a reduced thermal time constant. The third generation YBaCuO microbolometers[39] were built with titanium electrode arms and optimized cavity depth for maximum infrared absorption by using an aluminum reflecting layer. The research presented in this chapter will build on these results and

improve the self-supporting microbolometer performance. The small thermal conductance achieved by suspending the microbolometer using micromachining techniques allows the bolometer to integrate the radiant energy and produce large response. However, the decrease in thermal conductance slows the detector response time by producing a corresponding increase in the thermal time constant. Thus, there is a trade off between the response speed and responsivity.

This chapter investigates the integration of self-supporting YBaCuO infrared sensors (microbolometers) with a capacitive transimpedance amplifier (CTIA) readout circuit based on a constant voltage (CV)[13,14,15] technique. The readout circuit was designed utilizing AMI 1.5μm double-poly-double-metal n-well 2.5V low noise analog CMOS process available through the MOSIS foundry. A unit-cell, 4x4 array, and 32x32 array readout circuits were designed to investigate integration issues associated with YBaCuO microbolometers. The simulation results and data rates were normalized to a traditional 640x480 focal plane array where 30 Hz and 200 Hz frame rates are desired.

2.1.2 Motivation

The primary motivation behind this research is to help in the performance of uncooled infrared cameras by the higher frame rate of 200 Hz for faster thermal imaging in commercial, military and biomedical applications or with improvements in microbolometers sensitivity. Current uncooled infrared cameras typically operate at 15-60 Hz frame rates and have detectivity in the 10^8 cmHz$^{1/2}$/W range. The research will also exhibit the ability to fabricate two-dimensional, sacrificial polyimide-based, self-supporting uncooled YBaCuO microbolometric arrays.

2.1.3 Approach

The approach to achieve the discussed motives is described below.

2.1.3.1 Readout circuit design

The first task is to design the readout circuit that includes multiplexing circuitry to address the microbolometer array, transimpedance amplifiers to integrate the current flowing through the microbolometer and preamplifier. Nominally the readout would be a 32x32 pixel array with a 65 µm pitch to maintain relatively low foundry cost.

2.1.3.2 Microbolometer design

The next task is to design microbolometers to interface with the readout circuit. The electrode arm mask will be varied to achieve two different goals in detector design. One design will utilize a moderately low thermal conductance and low thermal mass of the self-supporting geometry to obtain a relatively fast thermal detector (200 Hz). The second electrode microbolometer design will be aimed at maximizing the detectivity while maintaining the traditional (30 Hz) frame rate.

2.1.3.3 Integration of microbolometers with readout circuit

Next, the readout circuit die received from the MOSIS foundry would serve as the substrates for the fabrication of two-dimensional microbolometer arrays using a polyimide sacrificial layer at the NanoFab Center in the University of Texas at Arlington.

2.1.3.4 Microbolometer fabrication process compatibility

Verify CMOS-compatibility of the microbolometer fabrication process.

2.2 Readout circuit design

The readout circuit was designed utilizing AMI 1.5 µm low noise analog CMOS process that is available through the MOSIS foundry. The simulations and the layout

were done using Virtuoso tool from Cadence Design Systems. The building blocks for the readout circuit are discussed as follows.

2.2.1 Operational amplifier design

The operational amplifier designed[40] has two gain stages and a unity-gain output stage as shown in Figure 2.1a. The first gain stage is a differential-input single-ended output stage. The second gain stage is a common-source stage. The output buffer is normally present only when resistive loads need to be driven. Compensation circuit is included to ensure stability when the op-amp is used with feedback. It is usually a capacitor and often called the Miller capacitance since its effective capacitive load on the first stage is larger than its physical value. The overall dc gain is largely unaffected by the choice of having n-channel or p-channel input stages. But for a given power dissipation, having a p-channel input-pair maximizes the slew rate. Having a p-channel input stage implies that the second stage has an n-channel input drive transistor. This configuration maximizes the transconductance of the drive transistor of the second stage, which is critical when high-frequency operation is important. An n-channel source follower is preferable because this will have less voltage drop. C_c is used as the compensation capacitor. It is called dominant-pole compensation. The transistor M16 (shown in Figure 2.1b) operates as a resistor since no dc bias current flows through it and is used for lead compensation. The schematic and layout of the op-amp was done using AMI 1.5 μm double-poly-double-metal n-well 2.5V CMOS technology as shown in Figures 2.1b and 2.1c respectively. The complete amplifier consists of the individual stages discussed above, in addition to current-mirror biasing circuitry.

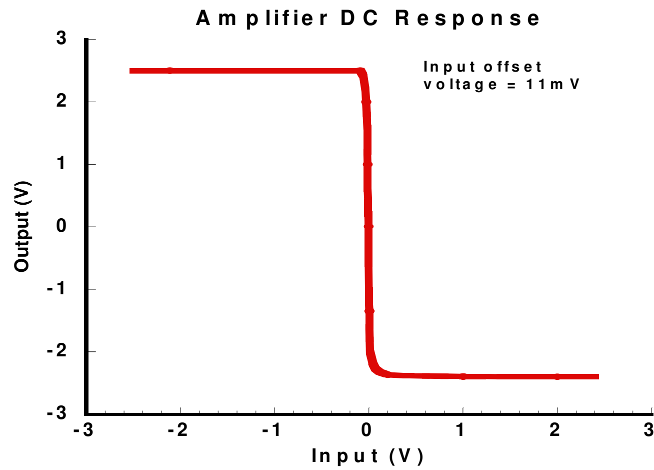
a)

b)

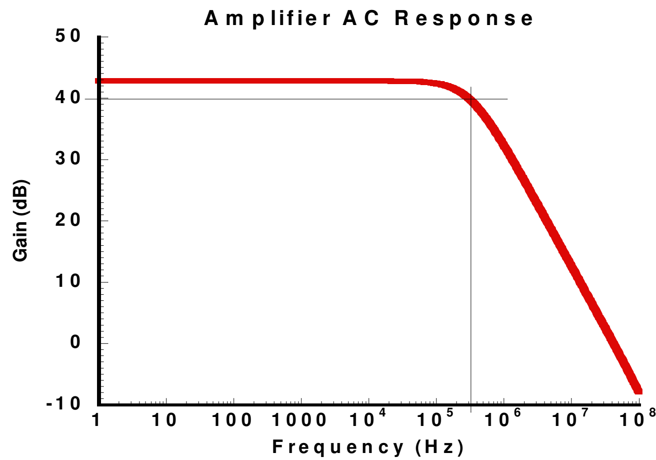
c)

Figure 2.1 a) Block diagram b) Schematic and c) Layout of two-stage CMOS operational amplifier.

The AC and DC response of the operational amplifier was simulated using SPECTRE tool from Cadence as shown in Figure 2.2 below. The performance parameters of the op-amp are summarized in Table 2.1.



a)



b)

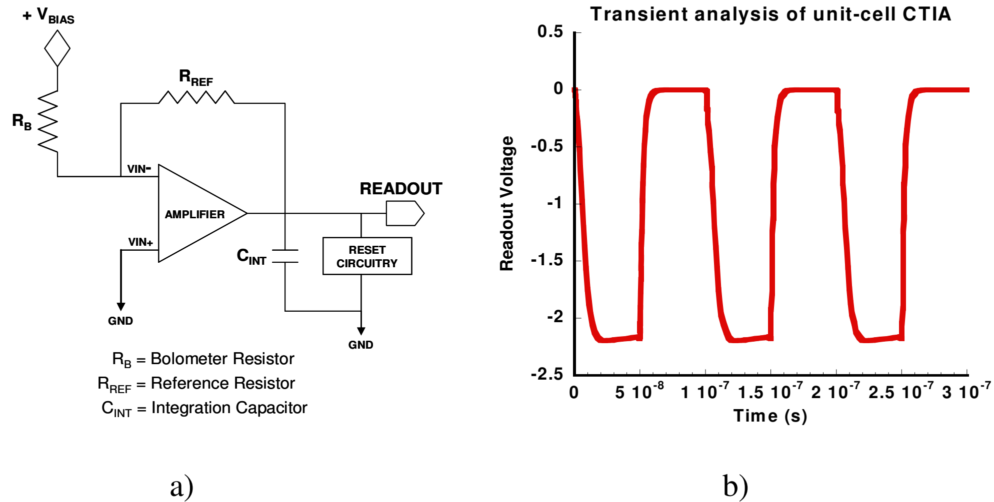
Figure 2.2 a) DC and b) AC response of operational amplifier.

Table 2.1 Performance parameters of CMOS operational amplifier

Low Frequency Gain	**42.85 dB**
Unity-gain Frequency	**37.8 MHz**
3-dB Frequency	**325 KHz**
Amplifiers' Response Time	**4.3 ns**

2.2.2 Unit-cell CTIA 1 pixel design

In CTIA 1 readout technique as shown in Figure 2.3a, each pixel has a bolometer R_B coupled by direct injection via CMOS switch addressed by the clock signal. Pulse biasing is employed to reduce the overall power dissipation and reduce the substrate thermal sensitivity[10]. The microbolometer is pulsed voltage biased. The useful current from the bolometer is integrated in a CTIA fashion. Before pixel integration, a common reference resistor R_{REF} is used to divert the background current and for temperature compensation. A reset transistor in the capacitive feedback loop is used to discharge the capacitor C_{INT}. The advantages of CTIA technique include low read noise[41], high uniformity, and reduced substrate thermal sensitivity fluctuation.



a) b)

Figure 2.3 a) Schematic and b) Simulated transient response of a unit-cell CTIA pixel.

The transient response of a CTIA unit-cell was simulated using SPECTRE tool from Cadence with V_{BIAS} = 2.5V, R_B = 1 MΩ, R_{REF} = 1.01 MΩ, C_{INT} = 1.0 pF and 10 MHz clock signal. As shown in Figure 2.3b, the output readout voltage is -2.2V and the pixel is reset to 0V using the reset circuitry after reading the output voltage.

2.2.3 Focal plane array design

The topology for 4x4 CTIA array readout circuit is shown in Figure 2.4 below. There are 16 infrared pixels which are pulsed voltage biased on a row-by-row basis using row multiplexer followed by 4 CTIA amplifiers. The CTIA amplifiers integrate the current from the infrared pixels. The column multiplexer circuitry sets the sequence of the voltages to be readout serially. A source follower is used for the final readout voltages in order to drive the load with negligible loss of signal level. An extra circuitry is included in the logic block to drive the integration signals and reset signals since there is only one master clock signal for the entire circuitry to readout row and column data. After resetting all the pixels in a given row, the next row pixels are selected and readout in a timely fashion.

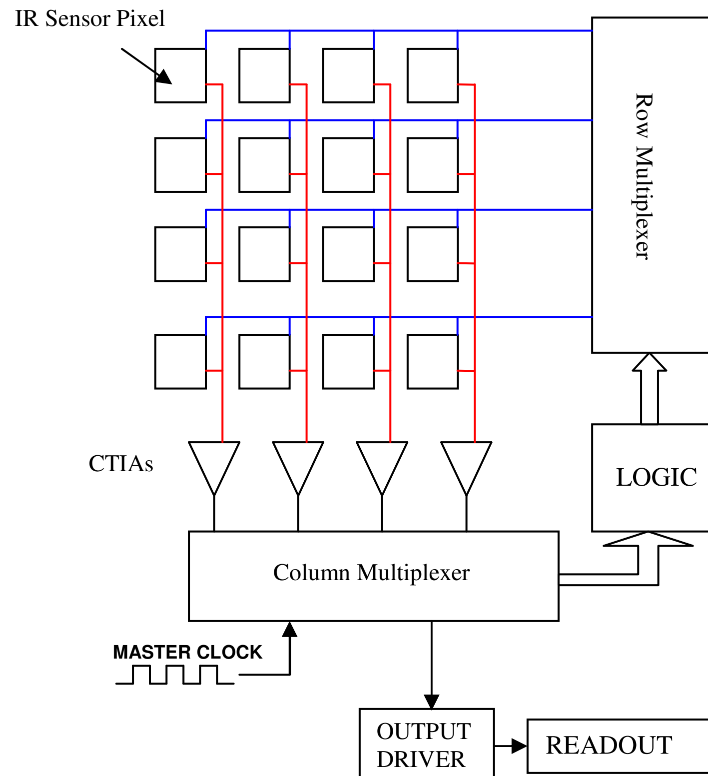


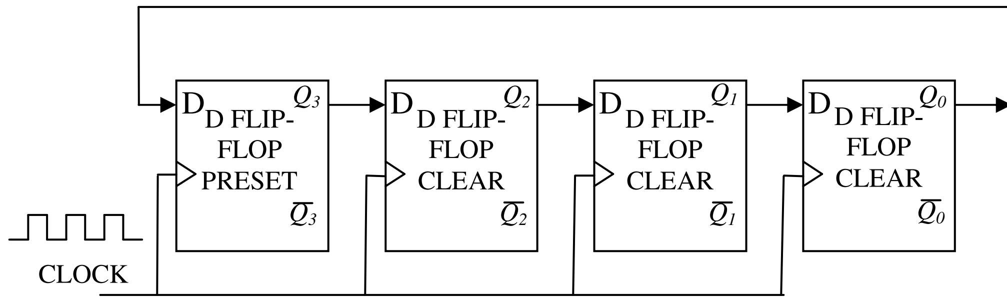
Figure 2.4 Readout circuit topology.

2.2.4 Timing circuitry design

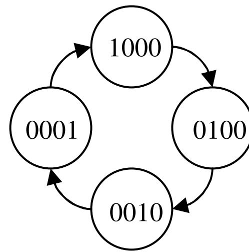
The timing circuitry for 4x4 and 32x32 CTIA focal plane arrays (FPAs) is designed using shift-registers. A shift-register is a group of flip-flops arranged such that the binary numbers stored in the flip-flops are shifted from one flip-flop to the next for every clock pulse. The shift-register is implemented using master/slave delay flip-flops (D flip-flop) in a ring counter fashion. The data shifts from left to right and back around from Q_0 to Q_3 as shown in Figure 2.5a. In most instances a single 1 is in the register, and it is made to circulate around as long as clock pulses are applied as shown in Figure 2.5b.

To operate properly, a ring counter must start with only one flip-flop in the 1 state and all others in the 0 state. In order to implement the above condition, one D flip-flop with preset input (connected to 1 state), all the other D flip-flops with clear inputs (connected to 0 state) are used. With the above condition, as soon as we turn on the power, Q_3=1 Q_2=0 Q_1=0 Q_0=0.

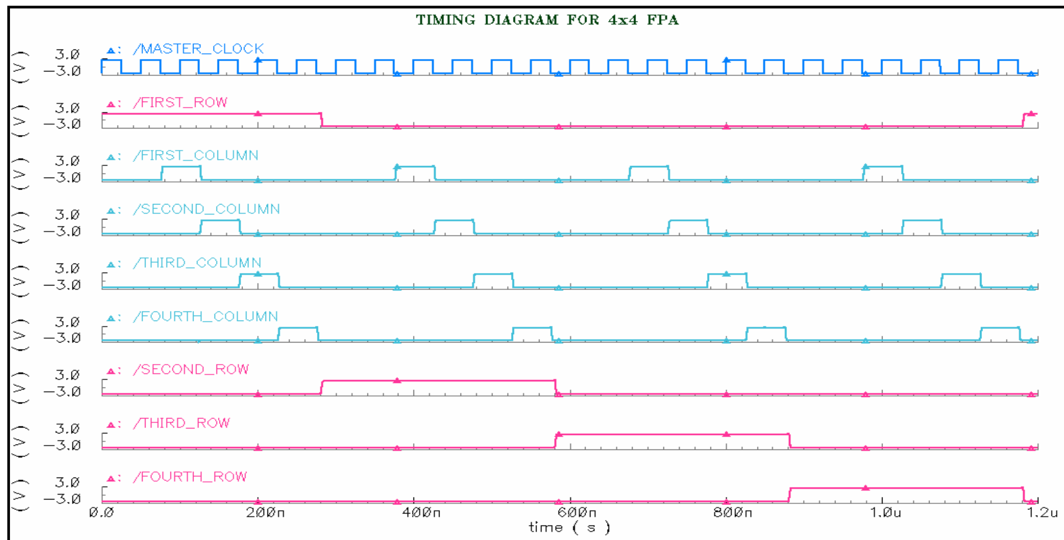
The building blocks used for the overall timing circuitry was designed with static CMOS logic using minimum sized transistors (W= 4.5 µm and L=1.5 µm). The building blocks used are CMOS switch, inverter, 2-input NAND gate, 3-input NAND gate, D flip-flop-clear, D flip-flop-preset, 4-bit ring counter and 6-bit ring counter. The CMOS switch was used to select an infrared pixel on the FPA. It connects the microbolometer to the readout-circuit on the substrate. The inverter was used in the D flip-flop circuitry to get the CLKBAR signal. The 2-input NAND gate was used as a slave in the D flip-flop. The 3-input NAND gate was used as a master in the D flip-flop. The D flip-flop-preset was used to give Q=1 QBAR=0 at the start of the ring counter. The D flip-flop-clear was used to give Q=0 QBAR=1 at the start of the ring counter.



a)



b)



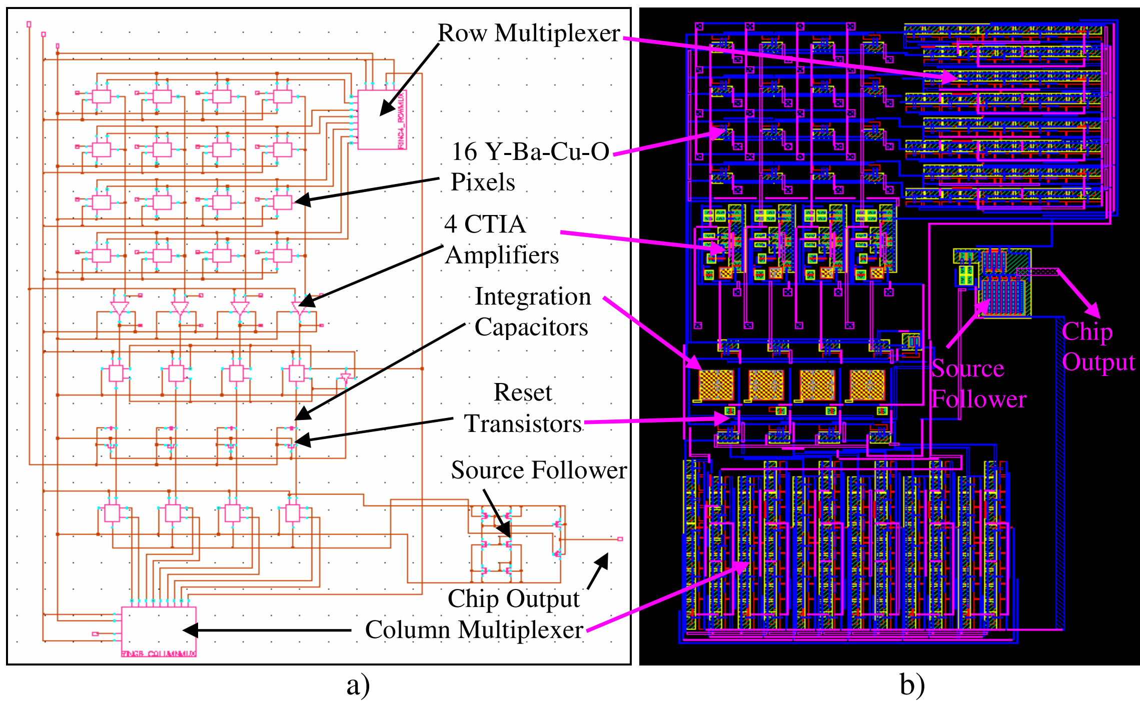
c)

Figure 2.5 a) Schematic and b) State-diagram of a 4-bit ring counter c) Timing diagram for a 4x4 CTIA focal plane array.

The technique shown in Figure 2.5c is used since there is only one master clock signal available that drives the entire timing circuitry of the readout circuit.

2.2.5 4x4 CTIA 1 focal plane array

The simulation for 4x4 CTIA 1 focal plane array was done with the schematic and layout as shown in Figures 2.6a and 2.6b respectively. The readout voltages shown in Figure 2.6c are -0.29V, -0.39V, -0.44V, -0.47V for 1.1MΩ, 1.2MΩ, 1.3MΩ, 1.4MΩ bolometer and 1MΩ reference resistors respectively.



a) b)

c)

Figure 2.6 a) Schematic b) Layout c) Transient analysis of a 4x4 CTIA FPA.

2.2.6 Frame rate analysis of 640x480 CTIA 1 focal plane array

Simulating the transient analysis of a 4x4 CTIA 1 FPA using a 100 MHz clock signal, we can see from Figure 2.7 that the readout time for 16 pixels is 238 ns. We also see that the first two pixels for a particular row are not fully integrated hence, we are not reading out the saturated voltages. But for the last two pixels we are reading out the saturated voltages. A very good solution for the above situation would be to have different integration times for the two groups of pixels. This is possible by adding extra delay logic at the output of the circuit that generates the clock pulse for integration.

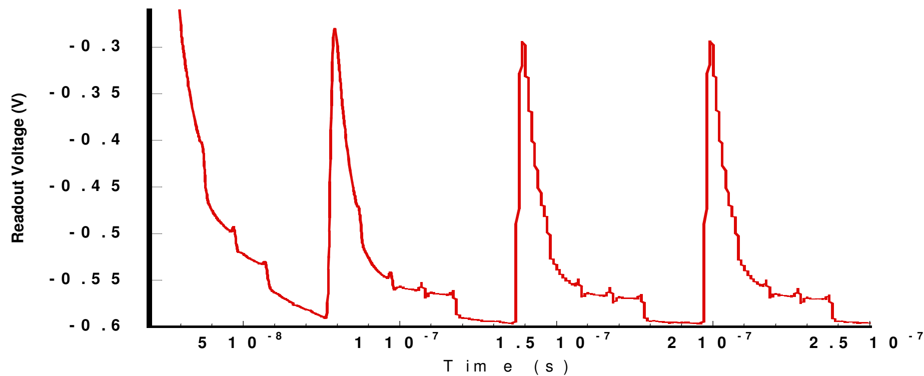


Figure 2.7 Simulated transient analysis of a 4x4 CTIA 1 array (100 MHz clock signal).

If we extrapolate the same timing scheme for a 640x480 array then, the readout time for 307200 pixels is 4.5696 ms which translates to a frame rate of 218 Hz. This fast frame rate achieved could be used in building infrared cameras for medical imaging applications such as monitoring respiration and heart rate.

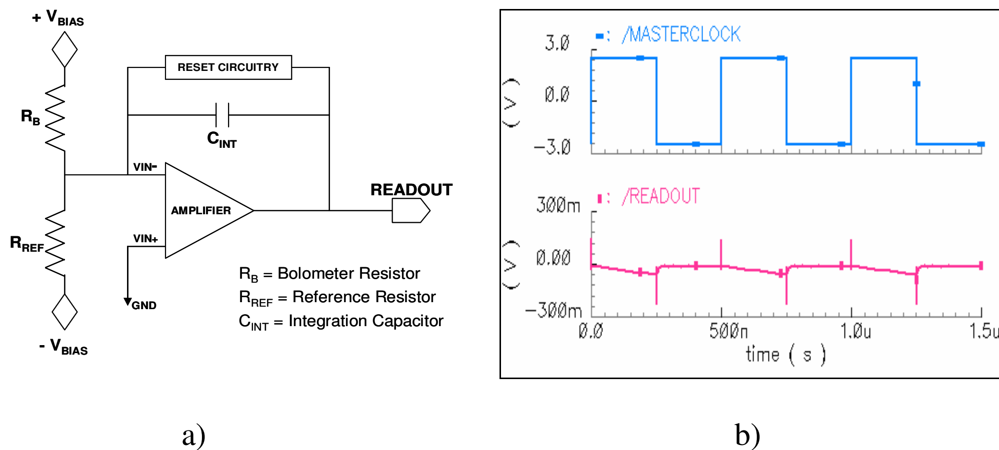
The overall power dissipation calculated using HSPICE tool for a 640x480 CTIA array is 612 mW. Most of the power dissipation in the readout circuit is due to the amplifier as shown in Table 2.2. The digital circuitry contributes to the power only during switching since they are designed using static CMOS logic.

Table 2.2 Readout circuit power dissipation

CELL	POWER DISSIPATION
Inverter	0.162 µW
Amplifier	0.912 mW
CMOS Switch	3.97 nW
Row multiplexing circuitry	13.49 µW
Column multiplexing circuitry	0.175 mW

2.2.7 Unit-cell CTIA 2 pixel design

Two other CTIA configurations namely CTIA 2 and 3 were also designed and analyzed. In CTIA 2 pixel design, each infrared pixel has a bolometer R_B and a reference resistor R_{REF} coupled via CMOS switch as shown in Figure 2.8a. Before integration current most of the dark current is diverted by the use of reference resistance R_{REF}. The useful current from the bolometer is integrated by the integration capacitor in feedback to the op-amp in a CTIA technique and the readout output voltage is -80 mV as shown in Figure 2.8b. If we use CTIA 2 design to implement a FPA, the bolometers would be still biased by CMOS switches in the ON state in order to avoid temperature rise within the integration time in spite of the column not being addressed by the column multiplexer.

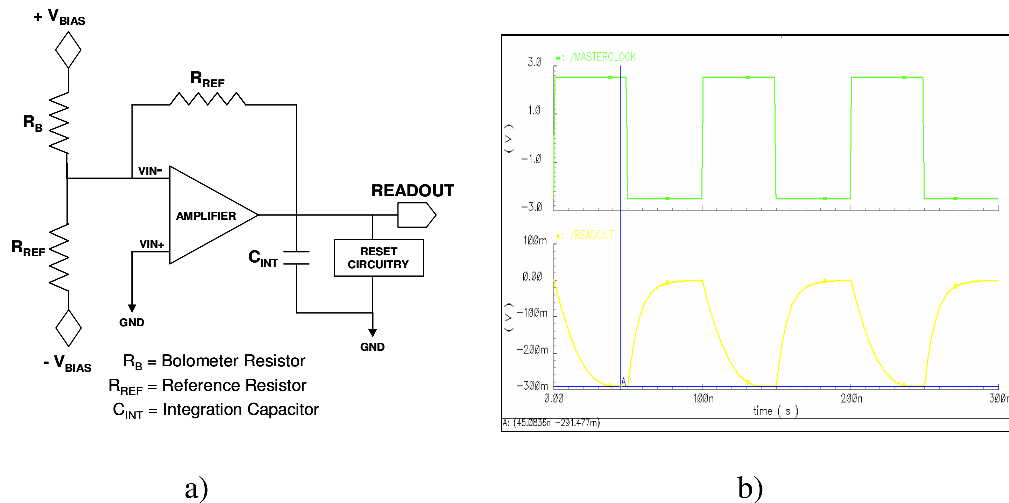


a) b)

Figure 2.8 a) Schematic and b) Simulated transient response of a unit-cell CTIA 2 pixel.

2.2.8 Unit-cell CTIA 3 pixel design

The schematic of CTIA 3 configuration as shown in Figure 2.9a is similar to that of CTIA 1 except that the bolometer R_B and reference resistor R_{REF} are coupled via CMOS switch addressed by the clock signal. Before integration most of the dark current is diverted by the use of reference resistance R_{REF}. The useful current from the bolometer is integrated in a CTIA technique and the readout output voltage is -0.29 V as shown in Figure 2.9b.



a) b)

Figure 2.9 a) Schematic and b) Simulated transient response of a unit-cell CTIA 3 pixel.

CTIA 1 design was chosen to be laid out on the full-chip to realize a 32x32 FPA because of the following reasons:

a) The area of CTIA 1 is the least compared to the other two CTIA designs.

b) The output noise voltage which is 5.48×10^{-9} V/Hz$^{1/2}$ is less compared to the other two CTIA designs.

c) Having a reference resistor R_{REF} in feedback to the op-amp gives a better control on the output readout voltage.

2.2.9 Full-chip readout DIE

Three CTIA unit-cells, three 4x4 CTIA arrays, 32x32 CTIA array with 65x65 μm^2 cell size, test PMOS transistors, NMOS transistors, inverters and CTIA amplifiers were laid-out on the readout die as shown in Figure 2.10. 100x90 μm^2 bond pads were designed to facilitate wire bonding. A source follower is designed using PMOS transistors of W/L ratio 400. This source follower is used in all the three configurations. Such high W/L ratio is kept to drive the capacitance due to the bond pad and the oscilloscope. Also, the source follower is used for the final readout voltages in order to drive the load with negligible loss of signal level

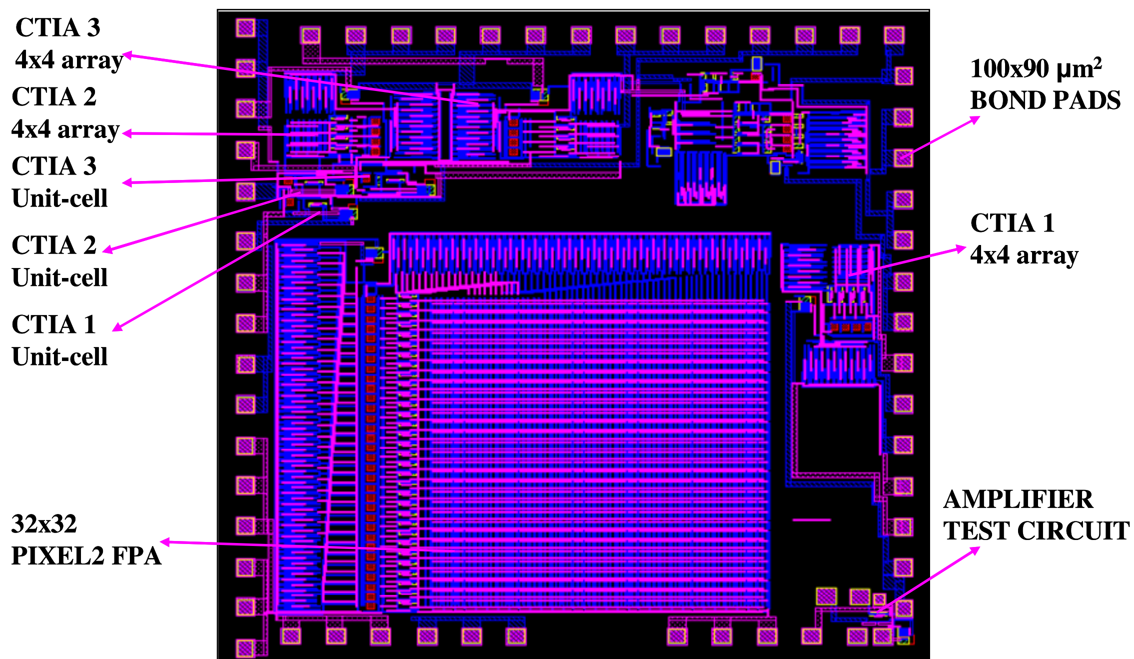


Figure 2.10 4500x4500 μm^2 CMOS readout DIE.

2.3 Microbolometer design

Microbolometers were designed to interface with the CTIA readout circuit. The YBaCuO microbolometers were designed[42] with two different electrode arm geometries to provide thermal isolation from the substrate. This was achieved by changing only one mask, which was used to pattern the sacrificial polyimide.

2.3.1 30 Hz Frame rate design

Figure 2.11 shows the microbolometer design to achieve 30 Hz frame rate. The electrode arm geometry was aimed at maximizing the detectivity (~ 10^9 cmHz$^{1/2}$/W) while maintaining a 5 msec thermal time constant which translates to the traditional 30 Hz frame rate. The length and thickness of the titanium electrode arm designed in this case is 55 µm and 1000 A^o respectively as shown in Appendix A. The YBaCuO pixel size is 35x35 µm^2.

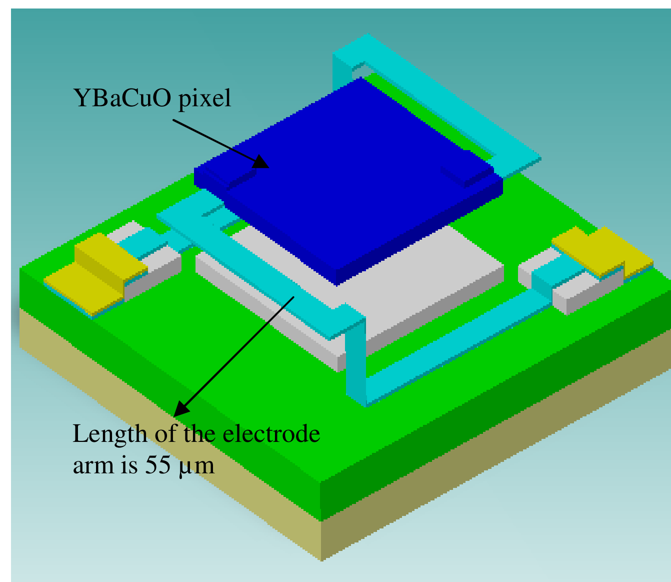


Figure 2.11 30 Hz frame rate microbolometer design.

2.3.2 200 Hz Frame rate design

Figure 2.12 shows the microbolometer design to achieve 200 Hz frame rate. The electrode arm geometry was designed to achieve moderately low thermal conductance and low thermal mass of the self-supporting geometry to obtain a relatively fast thermal detector (200 Hz frame rate) , thermal time constant less than 1 msec, while maintaining a detectivity (~ 10^8 $cmHz^{1/2}/W$). The length and thickness of the electrode arm designed in this case is 24 µm and 2000 A° respectively as shown in Appendix B. The YBaCuO pixel size is 35x35 μm^2.

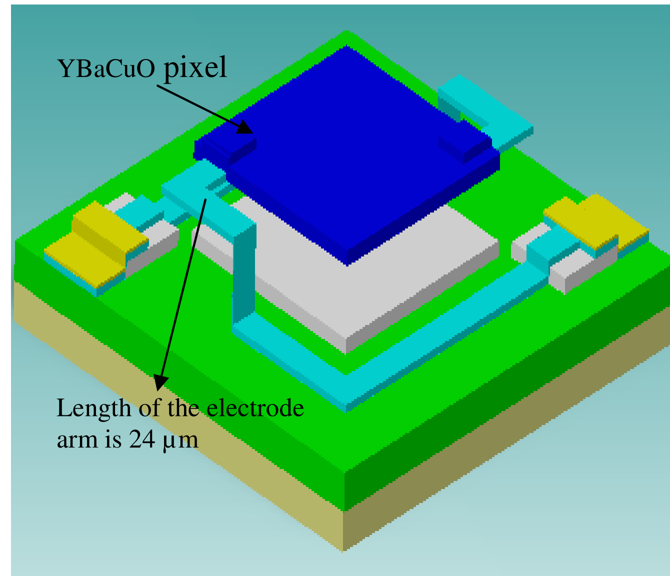


Figure 2.12 200 Hz frame rate microbolometer design.

2.4 Integration of microbolometers with readout circuit

The MOSIS foundry service was used to fabricate the readout circuits, providing the circuits as unplanarized die. The CMOS compatible YBaCuO microbolometer fabrication process presented could also be used to fabricate YBaCuO microbolometer on full silicon wafers. Self-supporting YBaCuO microbolometers were fabricated on the CMOS die with CTIA readout circuitry to form focal plane arrays using a surface

micromachining technique. The CMOS readout circuit was fabricated with 8x8 μm^2 glass cuts to facilitate the electrical connection between the readout circuitry, the YBaCuO reference resistors, and the YBaCuO microbolometers.

2.4.1 Microbolometer fabrication

The microbolometer fabrication process starts with bonding the CMOS readout die on a silicon carrier wafer (Figure 2.13) using polyimide PI2555 from HD Microsystems. The microbolometer fabrication steps involved the deposition of the aluminum mirror, PI2737 polyimide sacrificial layer spin-coating and curing, titanium deposition, gold deposition, YBaCuO deposition and finally polyimide ashing to obtain the suspended bridge structure.

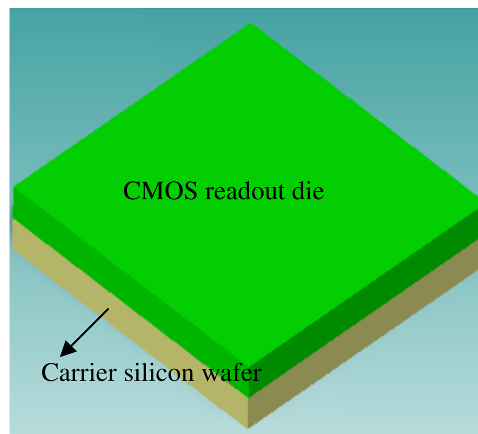


Figure 2.13 CMOS readout die bonded to carrier silicon wafer.

At first, the aluminum (Al) mirror was deposited by thermal evaporation to obtain 400 nm of thickness and patterned by liftoff to form an optically resonant cavity with the suspended YBaCuO microbolometer. The cavity height was designed to be 2 µm, at approximately λ/4 wavelength, to increase absorption in the 8-14 µm atmospheric transmission window. Aluminum was also patterned to partially fill the glass cuts in the

readout die and help with the electrical connection between the readout circuit and the microbolometers as shown in Figure 2.14.

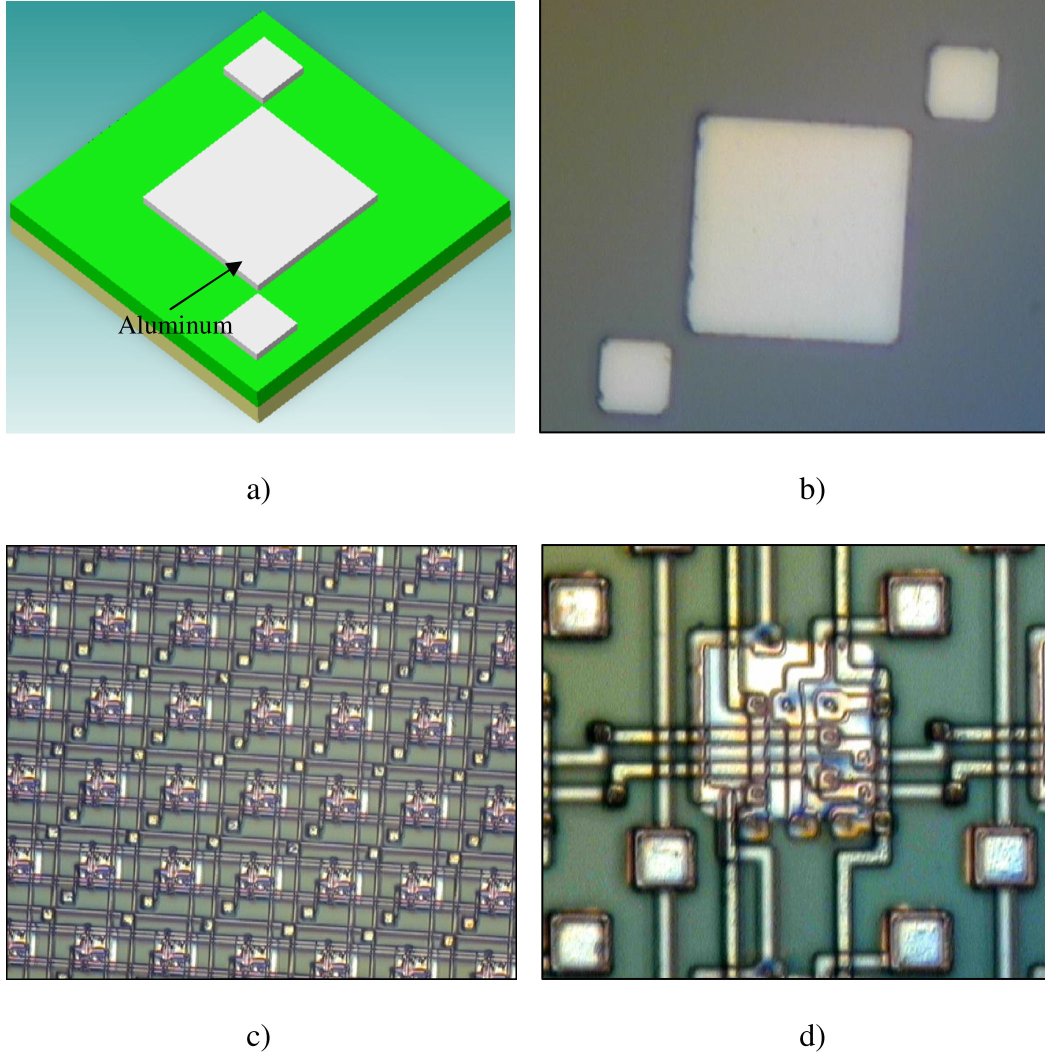


Figure 2.14 Aluminum patterning a) CoventorWare model; optical picture of b) aluminum pixel on the substrate c) aluminum pixels on 32x32 CTIA array d) magnified optical picture of c).

Next, the sacrificial polyimide PI 2737 (from HD Microsystems) was spin coated and patterned using negative lithography (Figure 2.15). The polyimide was cured at 275

^{0}C for 4 hours. The polyimide thickness, around 2 µm, formed the mesa bridge between the YBaCuO pixel and aluminum mirror.

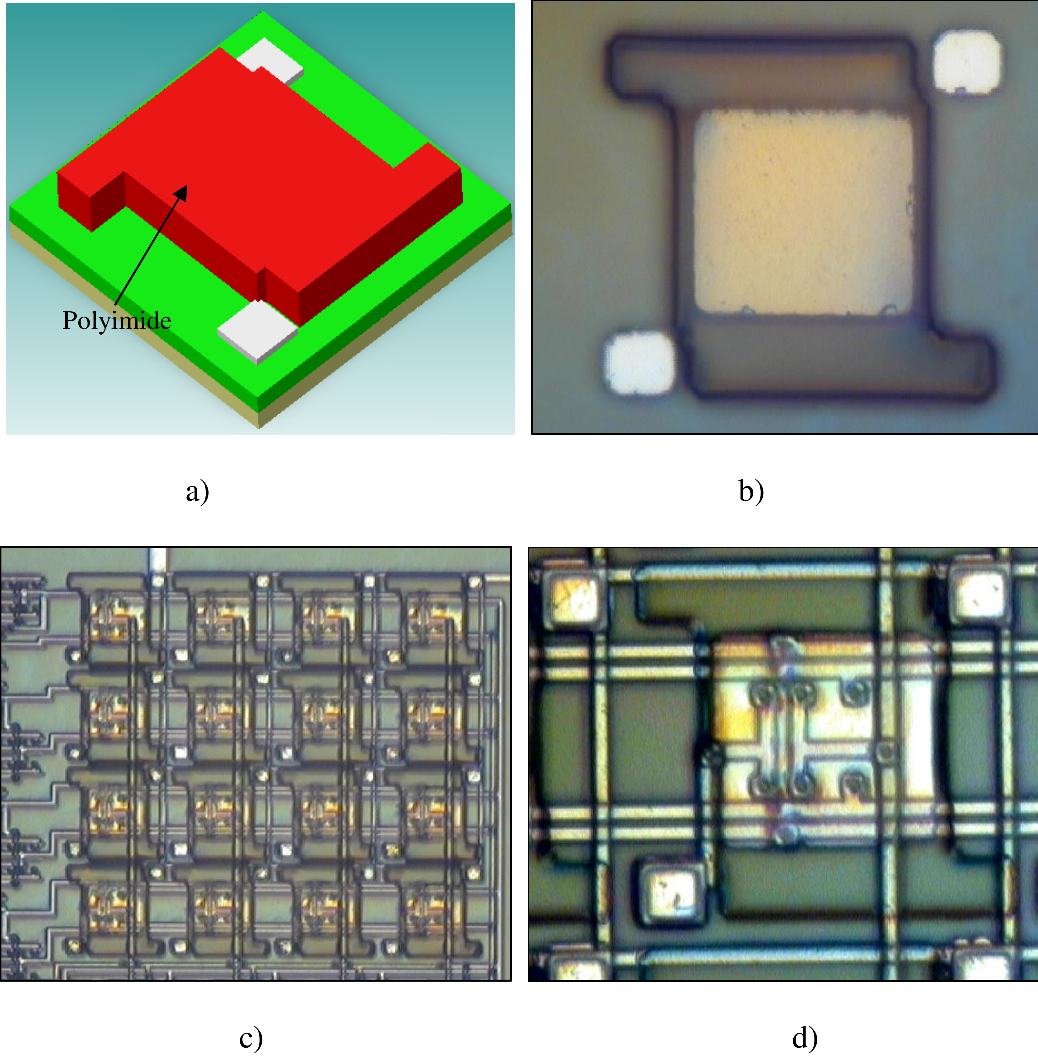


Figure 2.15 PI2737 patterning a) CoventorWare model; optical picture of b) polyimide pattern after curing to form test microbolometer c) polyimide pattern after curing to form 4x4 array of microbolometers d) magnified picture of c).

The 100-nm-thick or 200-nm-thick titanium (Ti) was deposited by rf magnetron sputtering at 150W in pure argon environment at 10 mTorr pressure and patterned by liftoff to form electrode arms that support the YBaCuO thermometer above the substrate.

The Ti electrode arms hold the YBaCuO thermometer above the substrate to achieve thermal isolation. The low thermal conductance of the electrode arms minimizes the heat transfer from the YBaCuO thermometer to the substrate and results in higher responsivity. Ti has low thermal conductivity compared to gold and aluminum. Nickel chromium also has a low thermal conductivity and could be used too. The 55 μm electrode arm geometry was investigated (Figure 2.16) by selecting the sacrificial polyimide pattern.

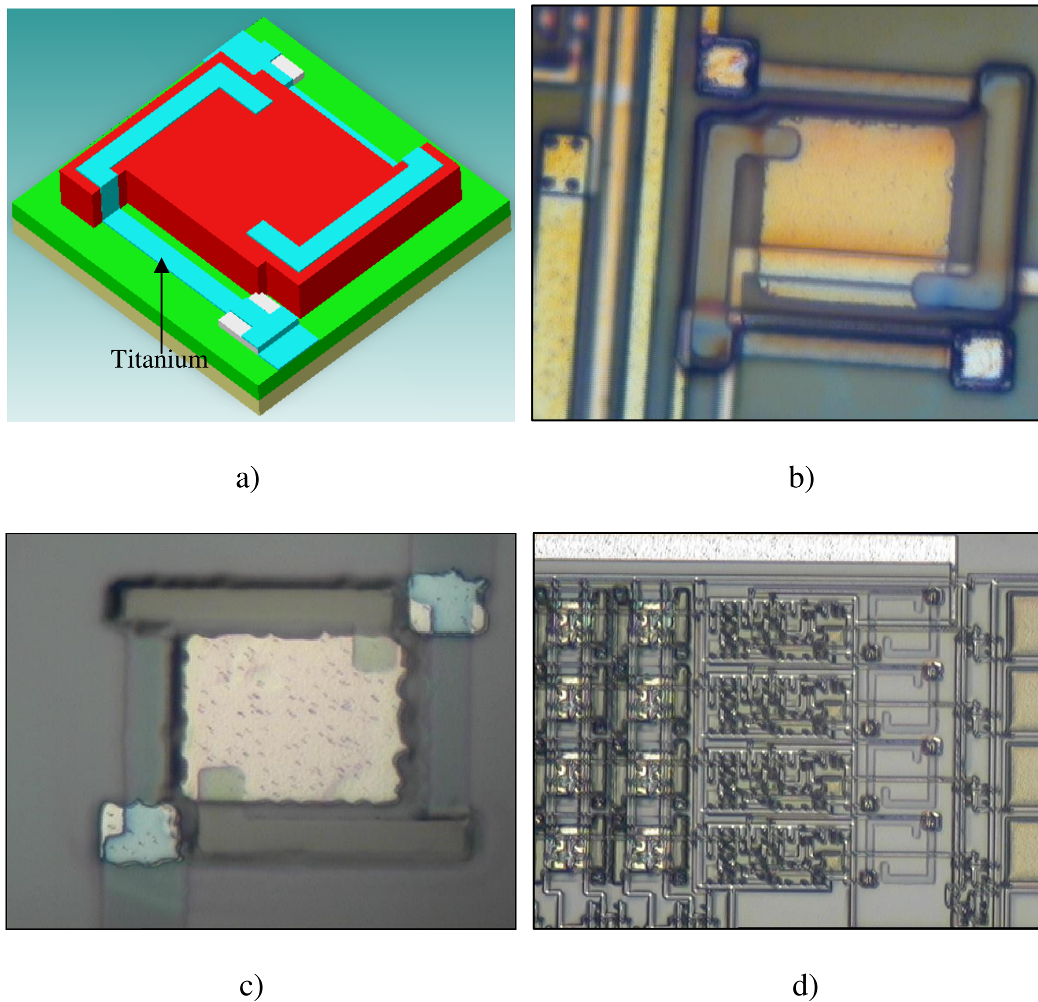


Figure 2.16 Titanium patterning a) CoventorWare model; optical picture of b) 55 μm titanium arm c) titanium arms to form a test microbolometer d) titanium arms to form four reference resistors.

Next, a 70-nm-thick gold (Au) film was sputtered at 100 W, 10 mT pressure and patterned by liftoff to form an ohmic contact between Ti arms and the microbolometer (Figure 2.17). Au forms a good electrical contact with semiconducting YBaCuO.

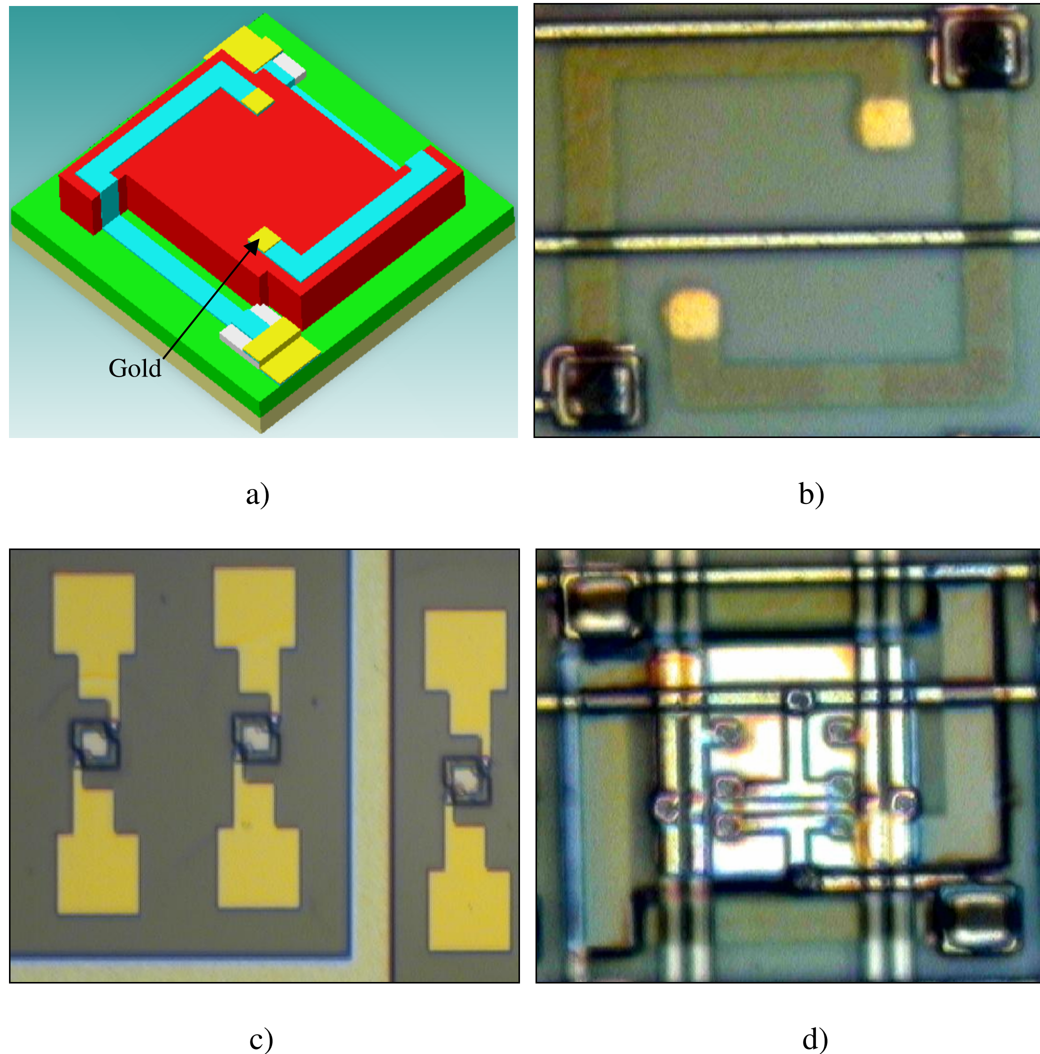
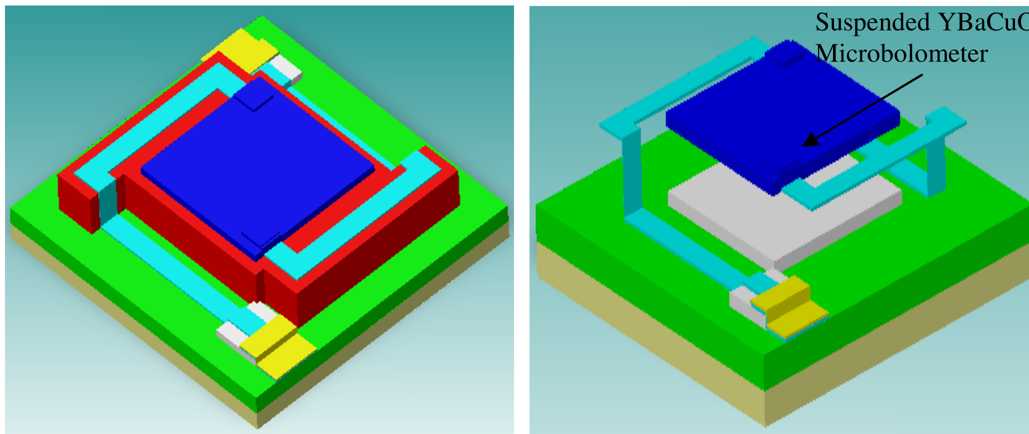


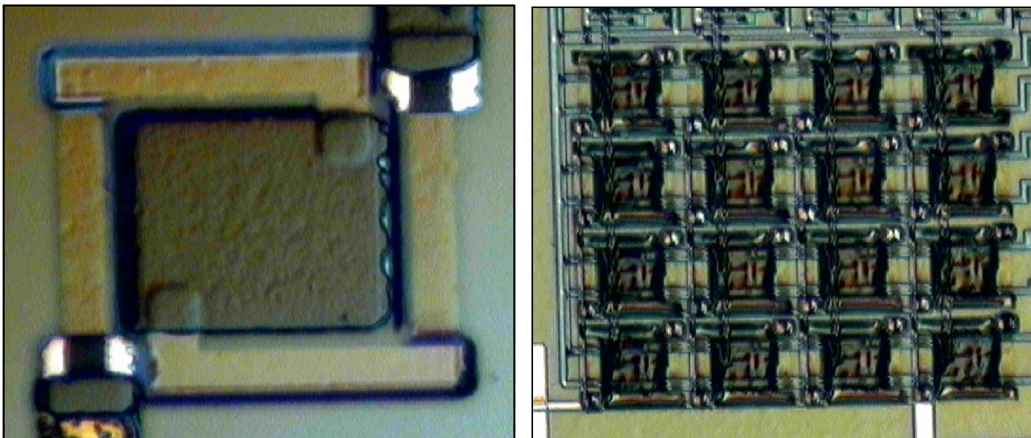
Figure 2.17 Gold patterning a) CoventorWare model b) optical picture of 5x5 μm^2 gold contacts on reference resistor on the substrate c) gold bondpads to facilitate wire bonding d) 5x5 μm^2 gold contacts on 4x4 CTIA array.

Then the 400-nm-thick YBaCuO was deposited by rf magnetron sputtering at 75W in pure argon environment at 10 mTorr pressure. The YBaCuO thermometer was patterned by liftoff. Finally, the sacrificial polyimide layer was removed by ashing in

oxygen plasma for approximately 10 hours at 100W plasma in a pure oxygen environment at 120 mTorr pressure. The removal of the PI2737 sacrificial polyimide layer created an approximately 2 µm microcavity (Figure 2.18) between the YBaCuO microbolometer and the aluminum mirror. After ashing the sacrificial polyimide, the self-supporting YBaCuO pixel is suspended by titanium arms providing thermal isolation from the substrate. This completed the microbolometer fabrication process.



a) b)



c) d)

Figure 2.18 YBaCuO patterning and ashing a) CoventorWare model after YBaCuO patterning b) CoventorWare model of suspended microbolometer c) optical picture of fully suspended test microbolometer d) optical picture of fully suspended 4x4 array of microbolometers.

2.5 Scanning Electron Microscope (SEM) micrographs of fabricated microbolometers

Figure 2.19a shows the rise in the titanium arm and the suspended test microbolometer. Figure 2.19b shows the reference resistor fabricated on the substrate for temperature compensation. Figures 2.19c and 2.19d show the suspended microbolometers fabricated on the readout circuit.

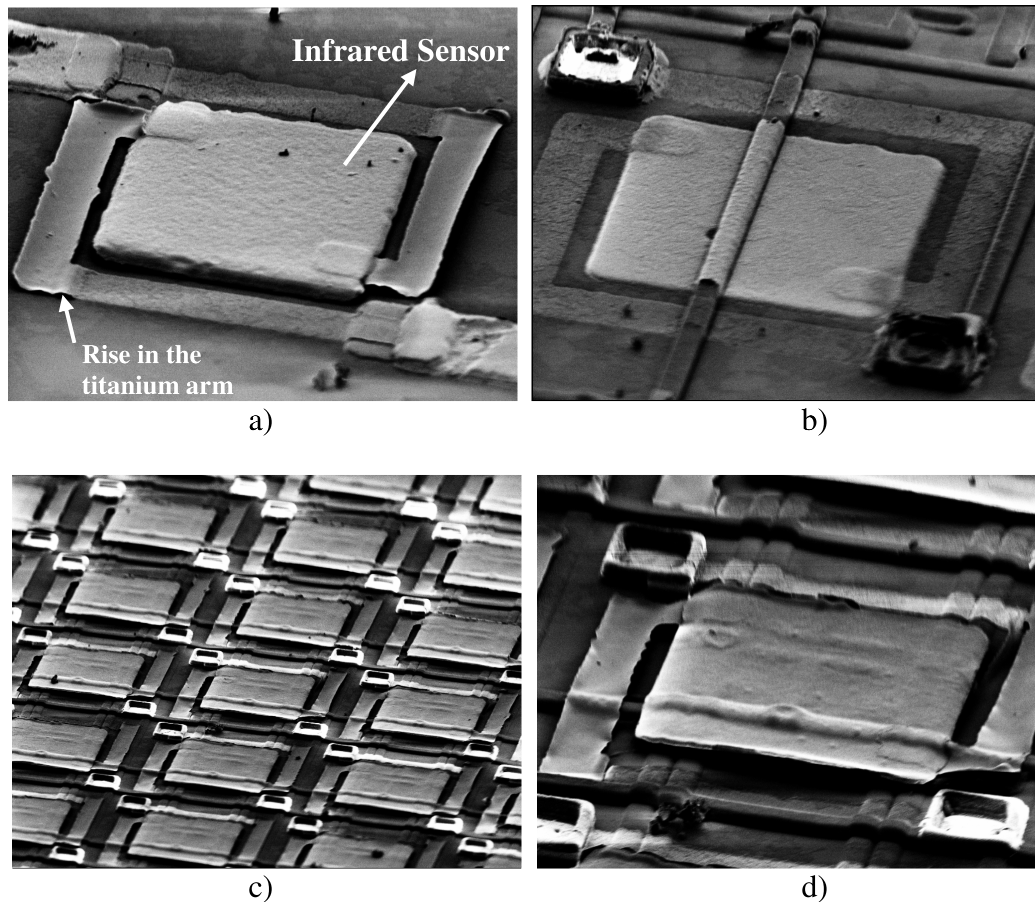


Figure 2.19 SEM micrographs of a) 55 µm electrode arm length test microbolometer b) YBaCuO reference resistor on the substrate c) fully suspended array of microbolometers d) magnified picture of c).

2.6 Microbolometer fabrication process compatibility

To verify that the YBaCuO microbolometer fabrication process is CMOS compatible, test circuits were incorporated into the die and characterized before and after

microbolometer fabrication. The test circuits included NMOS, PMOS transistors, CMOS inverter, and CTIA amplifier circuits.

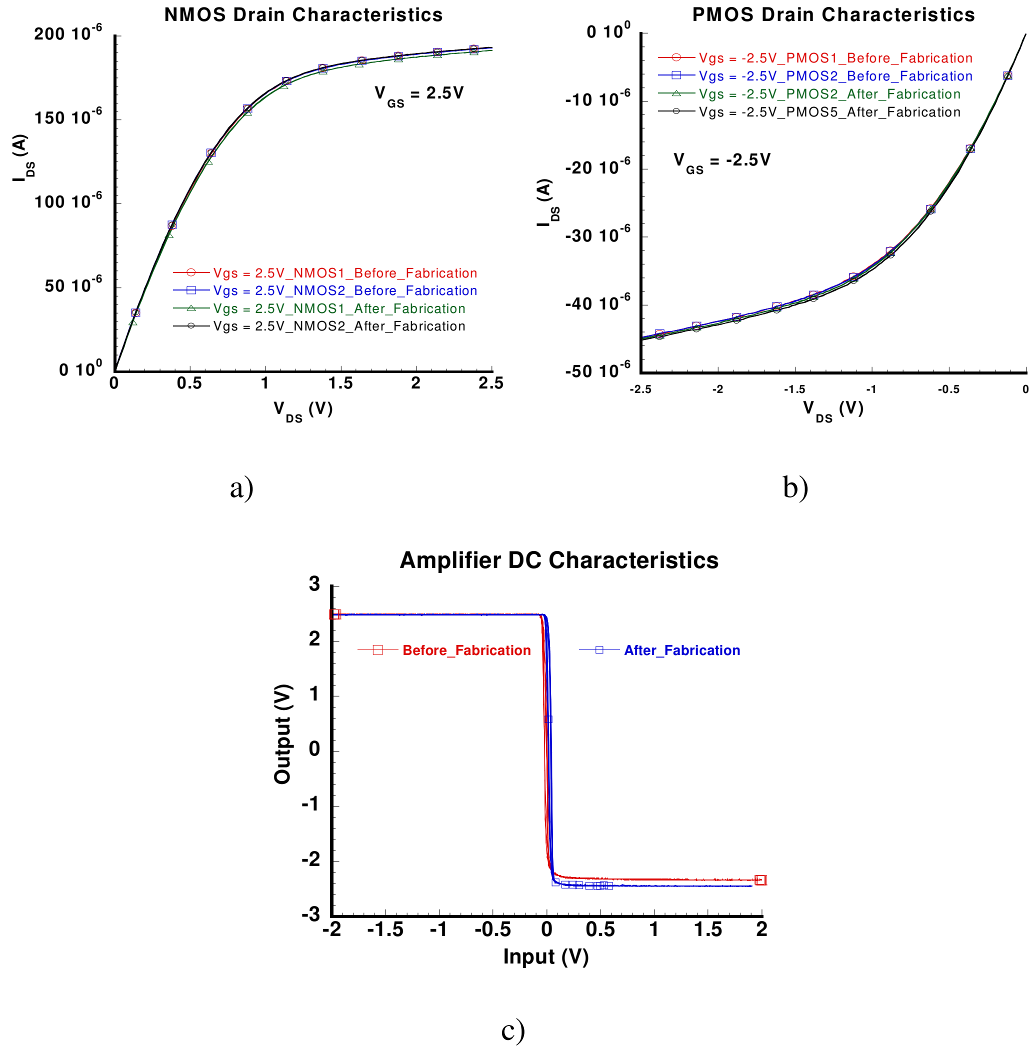


Figure 2.20 Measured a) NMOS b) PMOS drain characteristics and c) Amplifier DC characteristics.

Presented in Figure 2.20a and Figure 2.20b is the drain-to-source current I_{DS} versus drain-to-source voltage V_{DS} characteristics of two NMOS and two PMOS transistors measured before and after fabrication. The results showed minimal variation

from transistor to transistor and no visible difference before and after fabrication, indicating no change in the threshold voltage or drain saturation current.

In Figure 2.20c, the DC transfer characteristics of the CTIA amplifier is shown. This represents a more complicated circuit comprised of several transistors. The CTIA amplifier showed minimal difference before and after fabrication.

2.7 Novelty

The method of fabricating self-supporting semiconducting YBaCuO microbolometers on CTIA CMOS readout circuit is novel. The microbolometers were patterned entirely by liftoff over a topologically rough substrate. The purpose of this invention is that YBaCuO microbolometers must be integrated with CMOS readout circuits to be commercially viable.

2.8 Summary

The CTIA readout circuit is designed and analyzed using AMI 1.5μm double-poly-double-metal n-well 2.5V CMOS technology. The CTIA readout technique has low power dissipation, high uniformity and reduced substrate thermal sensitivity fluctuation. A frame rate of 218 Hz can be achieved for a 640x480 array using the CTIA readout design, which is crucial for medical imaging applications such as monitoring respiration and heart rate. A CMOS compatible fabrication process for YBaCuO microbolometer is presented. The fabrication process enables the thermal path of the electrode arms to be selected by varying the sacrificial polyimide mask pattern. Self-supporting YBaCuO microbolometer pixel focal plane arrays are designed, fabricated and integrated for the first time with the CTIA CMOS readout circuitry.

CHAPTER 3

TUNABLE INFRARED MICROSPECTROMETER BASED ON BRAGG GRATING

3.1 Introduction

The utilization of MEMS fabrication techniques has revolutionized the miniaturization of several macroscopic devices. During the past two decades, the world has seen a tremendous growth in optical communication systems. A substantial amount of research has been done towards the development of integrated optical circuits. Recently, laboratory-on-a-chip applications have been developed. One key component of laboratory-on-a-chip applications is an optical spectrometer that may be used for spectral analysis (composition and structure) in application such as gas monitoring.

Several researchers have developed micromachined, optical spectral filters[23,24,25,26,27,28] that are capable of operating in the visible and near-infrared portion of the optical spectrum. The spectral filters generally utilize coupled filters, interferometry, or dispersion to separate radiation into its spectral components. Most of the spectral filters fabricated to date are fixed in their spectral response and cannot be tuned. In addition to the work mentioned above, a research group at Delft University of Technology (Netherlands) has investigated several different spectral filter configurations including: A 16-channel Fabry-Perot Etalon spectrometer that utilized 16 different resonant cavity thicknesses formed by multiple lithography processes and pnp phototransistor detectors[23]. The 16-channels covered the spectral range of 370 to 480 nm.

A bulk-micromachined cavity spectral filter was investigated, that utilized a grating and propagation through the cavity to disperse the radiation and project it onto the detector array[22]. An infrared spectral filter that utilizes a diffraction grating to disperse the radiation and project it onto a thermopile detector array is mentioned in reference [22], which serves as a good review of this groups' work. Elsewhere, a diffraction grating microspectrometer utilizing silicon photodiodes has been fabricated using the LIGA process[24]. The use of slab-waveguide transmission gratings which produced a dispersion of 1 rad/μm with an efficiency of 60%[27].

Waveguide gratings are widely used for coupling light into and out of the waveguides for many years, already[43,44,45,46,47]. In this work, a tunable grating microspectrometer is investigated using the finite difference time domain method. A grating period Λ, approximately equal to an integral multiple of half the propagating wavelength in the guide (Bragg condition), etched into the surface of a uniform waveguide, creates a coupling between the propagating wave and an identical contradirectional wave. The theoretical analysis of waveguide gratings is based on coupled mode theory and Bloch wave analysis[43,44,45,46,47].

Integrated optical waveguides with embedded grating structures using the above phenomenon have several impending applications in optical communication systems[48]. Some of the grating devices which have already been established include thin-film optical filters, distributed feedback lasers (DFB), and distributed Bragg reflector lasers (DBR)[49].

In this work, a tunable, highly efficient infrared microspectrometer based on Bragg diffraction grating structure that is capable of operating in the mid-infrared (1 μm

to 10 µm) portion of the optical spectrum is presented. The microspectrometer presented is designed to detect approximately a 3 µm free space wavelength.

3.2 Grating design

A waveguide grating will diffract light into and out of the substrate as shown in Figure 3.1. In Figure 3.1, w is the groove width, Λ is the grating period, d is the groove depth, h is the waveguide thickness, ε_1 is the permittivity of aluminum oxide at 2.75 µm, and ε_2 is the permittivity of free space.

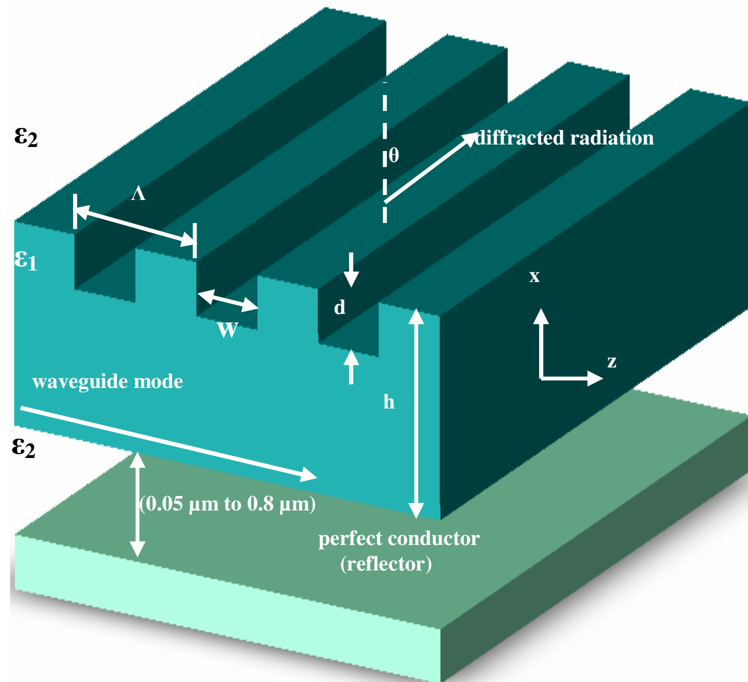


Figure 3.1 Rectangular grating etched into the surface of aluminum oxide (Al_2O_3) slab waveguide.

The design of simple rectangular grating started with the calculation of radiation losses, due to refractive index perturbations, by the volume current method (VCM)[50]. The simulations were done using OptiFDTD tool from Optiwave Systems. OptiFDTD, a

powerful, highly integrated, and user friendly CAD environment is based on the finite-difference time-domain (FDTD) algorithm with second-order numerical accuracy.

The designed parameters for 3 μm microspectrometer are grating period Λ=2.3 μm, grating depth d=1.1 μm, waveguide height h=1.5 μm and N=10, the number of grating sections.

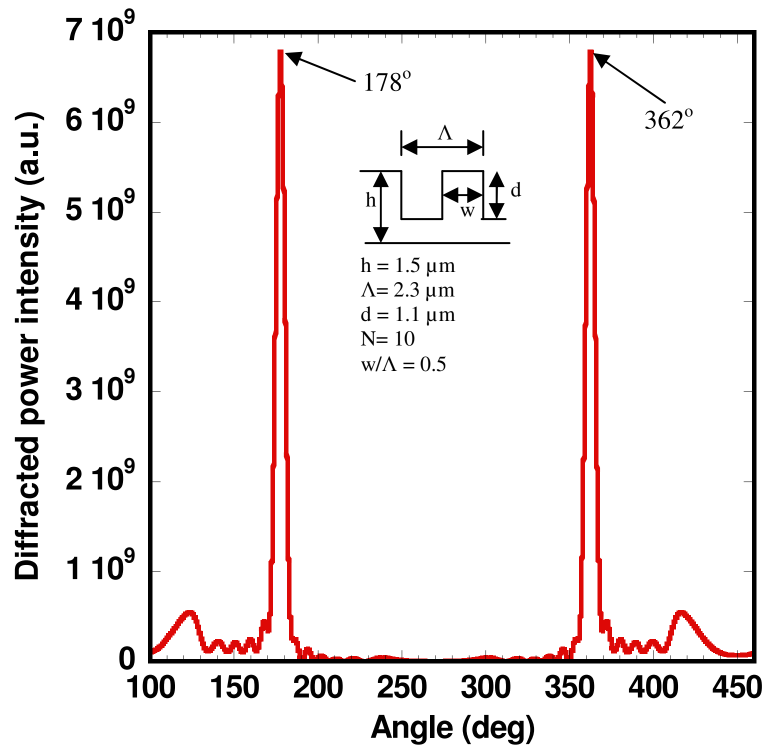


Figure 3.2 Simulated diffracted radiation from a rectangular grating designed to detect 3 μm wavelength.

From Figure 3.2, the radiation symmetrically peaks into and out of the substrate at 178° and 362° respectively. This result concurs with published results[51], obtained using Bloch wave and coupled mode analysis, when translated from 0.88 μm to 3 μm free space wavelength.

3.3 Absorptivity of the microspectrometer

A planewave is launched normal to the grating structure. The power is absorbed by a perfect detector placed in the waveguide. In this case, the absorptivity is a ratio of the output power (Watts) to the input power (Watts). Hence the unit of absorptivity in this work is mentioned as dimensionless. The absorptivity calculated is the ratio of absorbed power to the incident power. The calculation shows 28% absorptivity by the grating without the reflector below the grating with a corresponding maximum wavelength of 2.75 µm as shown in Figure 3.3. The groove depth "d" was optimized to achieve maximum absorptivity.

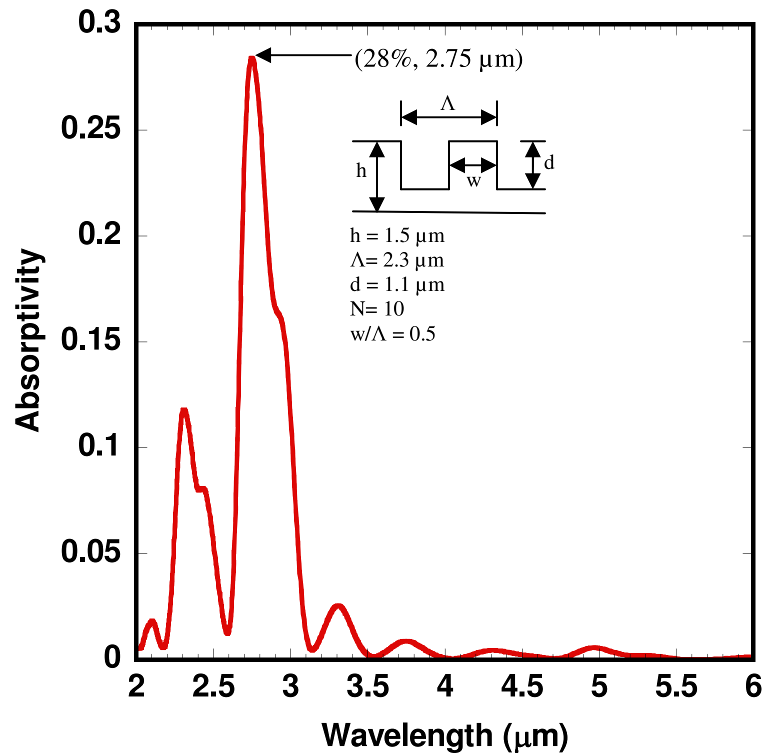


Figure 3.3 Simulated absorptivity versus wavelength for the spectrometer without reflector at normal incidence.

3.4 Tuning the microspectrometer

A perfect conductor of 0.4 μm thickness is placed 0.8 μm below the rectangular grating structure to reflect the power lost due to leakage and to tune the propagation constant of the grated dielectric waveguide and thereby the Bragg condition. From Figure 3.4 we can see that the calculated absorptivity has increased from 28% to 43% with the same design parameters.

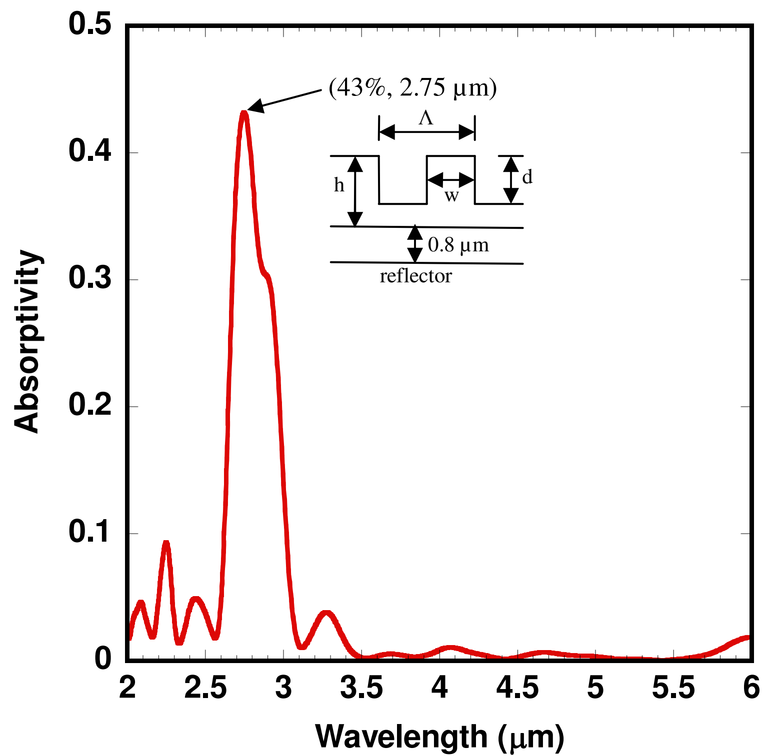


Figure 3.4 Simulated absorptivity versus wavelength for the spectrometer with reflector at normal incidence.

3.5 Tunability of the microspectrometer

The tunability of the spectrometer is achieved by changing the position of the perfect conductor placed below the rectangular grating structure. The perfect conductor can be realized in practice by a thin film reflector formed by a metal or dielectric mirror.

The reflector is micromachined so that is movable and can change its position with respect to the grated dielectric waveguide by electrostatic or thermal actuation as is common in microelectromechanical devices. The reflector perturbed the evanescent wave below the grated dielectric waveguide, thereby changing its propagation constant. The absorptivity decreased as we changed the position of the perfect conductor away from the grating structure as shown in Figure 3.5. The position of the perfect conductor was nominally changed from 0.05 to 0.8 μm below the grated waveguide in the simulations.

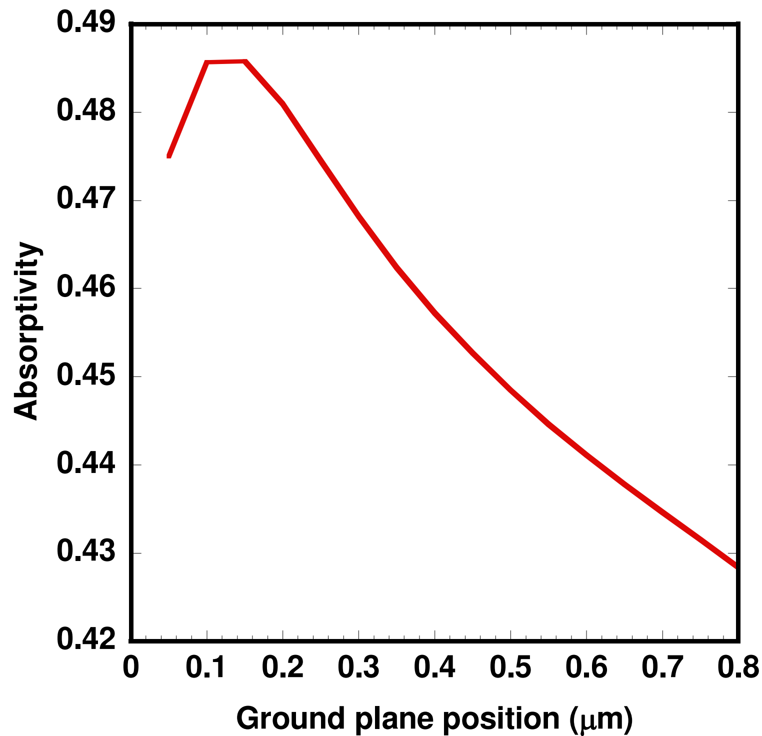


Figure 3.5 Simulated absorptivity versus reflector position.

A tunability of approximately 10% is shown in Figure 3.6, for a 2.75 μm microspectrometer with the perfect conductor position varied from 0.05 μm to 0.8 μm. In practice, the reflector position could be varied from being in contact with the grated waveguide to a position far away. As the position of the reflector below the grated

waveguide is changed a simultaneous change in the center frequency of the absorption occurs.

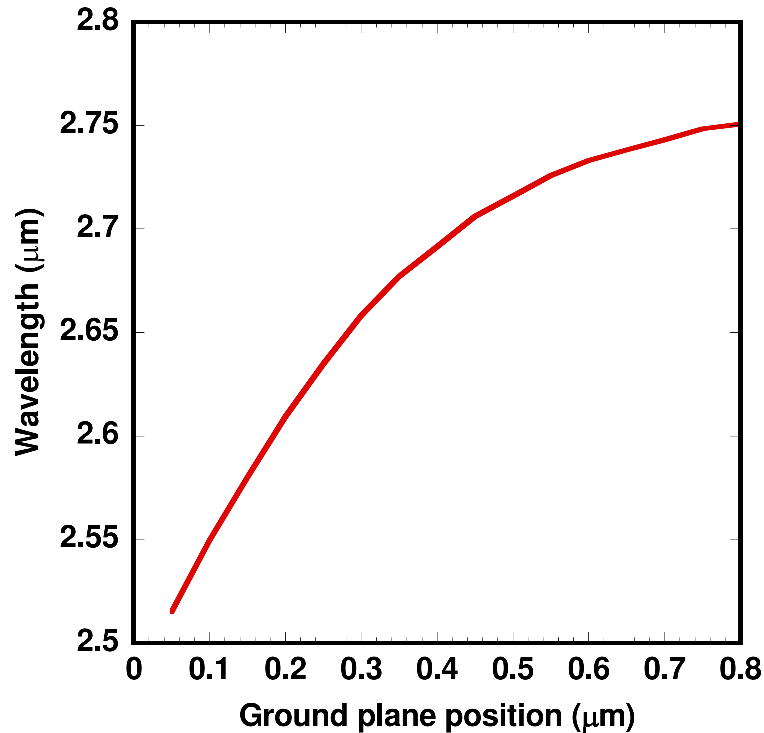


Figure 3.6 Simulated center wavelength versus reflector position.

3.6 Novelty of the microspectrometer

At present, one-dimensional and two-dimensional optical filters operate at a fixed wavelength. The novelty of the tunable microspectrometer designed is the method of tuning the optical filter by electronically adjusting the center wavelength of the filter. An electrostatically actuated moveable mirror is utilized above or below the optical filter to change the propagation constant and thereby tune the filter. Other tunable filters are based on a Fabry-Perot resonator where a moveable mirror is used to tune a resonant cavity.

3.7 Summary

The coupled mode theory and Bloch wave analysis was verified for scattered radiation from diffraction gratings on the surface of waveguide structures. A 2.75 μm tunable microspectrometer was designed with 10% tunability and an absorptivity of 45%. The design parameters, grating period Λ and groove depth d, were adapted to span wavelengths in the mid-infrared region of the optical spectrum.

CHAPTER 4

VACUUM-PACKAGED RF MEMS RESONATOR

4.1 Introduction

Microelectromechanical systems (MEMS) facilitate the integration of integrated electronics with sensors and actuators. MEMS packaging is very challenging because the packaging should not only protect the device from the outside world, provide proper interfacing with other circuitry, but also not hinder with the abilities of the enclosed device. Some of the major issues encountered while selecting a packaging type for MEMS devices are thermal budget, mechanical strength, size, and cost. These issues limit the choice of the packaging materials. This chapter investigates a ground-breaking, device-level, high pay-off packaging technique for MEMS devices. To clarify the motivation of this chapter, first it is necessary to have a brief review of packaging in the broad scope, and then followed by a more narrow focus of packaging for MEMS.

4.2 Packaging

The function of a package is to integrate all of the components required for an application specific system that minimizes the size, cost, and complexity. The package provides the interface between the components and the overall system. The following subsections give a brief picture of the main functions of the package; mechanical support, protection from the environment, and the connection of signals to other system components.

4.2.1 Mechanical support

Due to the very nature of silicon devices being a mechanical structure (at least at the chip level), the requirement to support and protect the device from thermal and mechanical shock, vibration, high acceleration, particles, and other physical damage during storage and operation of the part becomes critical.

4.2.2 Protection from environment

Many elements in the environment can cause corrosion or physical damage to the metal lines of the other components in the package. Moisture penetration can be a major concern for electronics due to the interaction between the moisture and materials in the device. For example, aluminum lines can corrode quickly in the presence of moisture, whereas gold lines degrade slowly in moisture. Also, junctions of dissimilar metals can corrode in the presence of moisture.

4.2.3 Electrical connection to other system components

Because the package is the primary interface between the device and the system, it must be capable of transferring DC power and in some designs, RF signals. In addition, the package may be required to distribute the power and signals to other components inside the package. The drive to reduce costs and system size by integrating more MEMS and other components into a single package increases the distribution problems as the number of interconnects within the package increases.

4.3 MEMS packaging

Although MEMS products have steadily gained a share in the commercial markets, packaging of MEMS devices is usually developed case-by-case and still remains as a significant roadblock in today's commercialization path. Due to the sensitive and

fragile nature of the moving devices, the packaging cost often amounts to a major portion as much as 70-80% of the cost of the MEMS product. One promising approach presented in this dissertation to cut down the cost of the whole packaging process drastically is the device-level packaging technique. In this technique, packaging of all the MEMS devices on one wafer is done at the same time rather than on an individual die, because it simplifies subsequent packaging procedure. After packaging the devices inside a sealed cavity on the wafer, the tools and protocols for microelectronics packaging can be used, cutting down the cost of the whole packaging process. In general, the device-level packaging approach falls into two categories: hybrid wafer bonding packaging and monolithic thin-film packaging.

4.3.1 Hybrid wafer bonding packaging

In a hybrid wafer bonding packaging process as shown in Figure 4.1a[52], a separate substrate is bonded to the MEMS wafer to cap the MEMS components using a wide variety of bonding techniques, either in a form of direct surface bonding or using an intermediate layer.

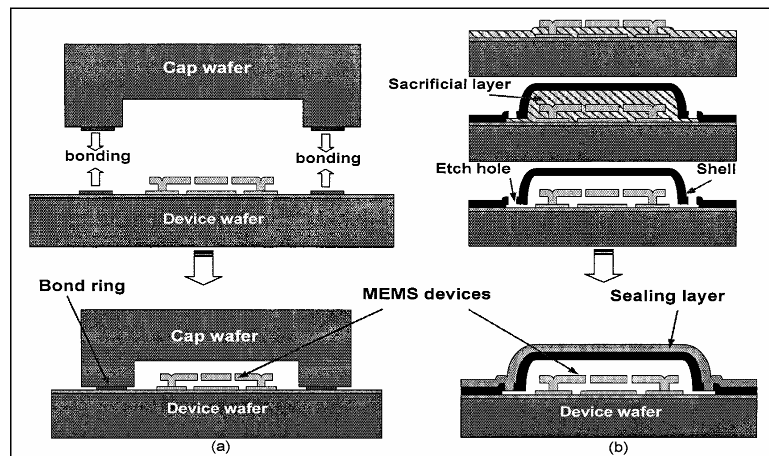


Figure 4.1 a) Hybrid by wafer to wafer bonding b) Monolithic by thin-film encapsulation.

Hybrid packaging has been intensively studied and is now the mainstream approach adopted in the industry. For example, in Motorola's MEMS pressure sensor and accelerometer, the device is capped at the wafer level using a silicon top cap wafer that is bonded to the sensor wafer using low-temperature glass frit bonding. Texas Instrument's Digital Micromirror Device (DMD)[53] device wafer is bonded to the carrier wafer by adhesive bonding.

4.3.2 Monolithic thin-film packaging

While wafer bonding has been proven and being widely used in industry, monolithic thin-film packaging has long been considered as a potentially more cost-effective technology. In monolithic thin-film packaging, the packaging process is carried out on the same wafer where the MEMS device is fabricated by adding extra steps to the surface micromachining process used to construct the device. As shown in Figure 4.1b, a sacrificial layer is deposited on top of an unreleased device and then covered by a thin-film encapsulation layer. The device is released after the sacrificial layer is removed through trench cuts opened in the encapsulation layer. The package sealing is achieved by depositing thin films on top of the encapsulation layer in an appropriate pressure condition. Monolithic thin-film packaging has several advantages over hybrid packaging:

1) It employs the surface-micromachining batch fabrication processes, avoiding the need for aligning two wafers and the challenges of bonding on processed surfaces.

2) It eliminates the seal ring, allowing much smaller volume cavities, therefore increasing the number of available die per wafer.

(3) Having much lower topography, thin-film encapsulation allows for post-encapsulation processes for additional MEMS or IC steps.

The earliest report to monolithically create microcavities by surface micromachining was by Guckel[54]. In their work, an absolute pressure sensor was developed by building pressure sensing elements on top of a polysilicon cavity sealed in vacuum, obtained after the 0_2 trapped inside the cavity was consumed by the polysilicon wall through oxidation. Carlos et al.[55] used LPCVD low stress silicon nitride to seal a silicon nitride cavity, inside which was a micro-incandescent light source.

Low temperature is one of the preferences in the packaging process, especially in RF MEMS packaging where metal (e.g., gold or aluminum) is frequently used to build the devices and thus can't withstand any high temperature processes. If CMOS circuits are pre-fabricated on the wafer, low temperature packaging of the MEMS devices is highly desired to accommodate the thermal budget constraints of microelectronic components. Various low temperature monolithic thin-film packaging techniques have been demonstrated. In reference [29], an RF resonator was sealed by a PECVD film following release of the sacrificial layer through the 0.25 μm vias in the cavity ceiling. The maximum processing temperature was 400 °C. Evaporated or sputtered thin films, which can be deposited at room temperature in a vacuum environment, are the candidates of sealing films in low temperature hermetic packaging. Mei et al.[30] demonstrated a vacuum microdiode device encapsulated inside a silicon nitride cavity sealed by evaporating silicon dioxide and aluminum. These devices are fabricated with an on-chip vacuum cavity through directional material sealing techniques initiated at vacuum pressure of ~2×10^{-6} T. Similarly, Bartek et al.[31] used evaporated aluminum sealing as well as LPCVD polysilicon sealing to package a diode device in a silicon nitride membrane cavity. Stark et al.[32] developed a thin-film electroplated metal package

featuring low process temperature (< 250 ^{o}C). An innovative approach[33] was demonstrated to obtain a sealed cavity with certain pressure of N_2 gas inside, an environment desired for an RF switch to achieve fast settling time during operation. A liquid encapsulant, with appropriate surface tension value to ensure no wick into the cavity through the release hole, was applied over a released cavity by spin coating in a dry N_2 atmosphere. The liquid encapsulant was then cured at 250 °C to form a sealed shell over the switch.

4.4 MEMS resonator packaging

4.4.1 Foundation

As a model, MEMS resonators were self-packaged and the reason for using a resonator is that the resonator's responsivity is a function of the pressure in the package. Such a device will enable us to build and test the integrity of vacuum-sealed packages using the packaged device (sensor) itself. Many MEMS require expensive vacuum packaging. To demonstrate why vacuum packaging is important, a generic style of micromachined double ended tuning fork (DETF) resonator is shown in Figure 4.2[56].

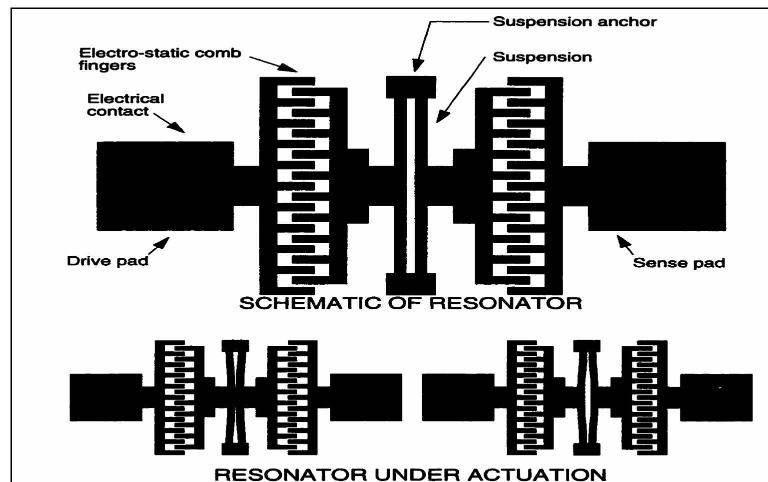


Figure 4.2 Double ended tuning fork (DETF) resonator.

The natural frequency is governed by the mass of the shuttle, the stiffness of the suspension, and the level of internal and viscous damping. The latter parameter is primarily influenced by the pressure level of the gas surrounding the resonator. More significantly, reducing viscous damping increases the quality factor of vibration. Higher quality factors correspond to a reduced bandwidth at the natural frequency which causes the resonator to resonate at a narrower frequency range. Therefore, since resonators are designed to operate at a specific frequency and in some cases over a narrow range of frequencies, many resonators are operated in a vacuum environment[57]. Another advantage is that the ratio of resonator signal amplitude to the noise caused by the motion of the surrounding gas molecules (Brownian noise) is increased. Our research group has successfully packaged infrared detectors on conventional silicon wafers using aluminum oxide (Al_2O_3)[58] and silicon nitride (Si_3N_4)[59] as the encapsulated layer. The characterization of these detectors showed similar results in air and vacuum indicating the integrity of the vacuum cavity.

4.4.2 Motivation

At present, approximately half of the MEMS market is microsensors. With the increase in their demand, there is a major anxiety on the choice of packaging and the mounting technologies associated with it. The average packaging cost is 70 - 80% of the total cost of a MEMS product. The primary motive behind this research is to cut down the cost of MEMS packaging.

4.4.3 Approach

The approach to achieve self-packaged MEMS resonators is to first fabricate vacuum-cavity packages without resonators to identify any processing issues prior to the

integration of the MEMS device and to test the survival of the packages to over-molding process. The next step is to fabricate and characterize MEMS resonators. The last task is to vacuum-package the MEMS resonators.

4.5 Vacuum-cavity packages

The fabrication of vacuum-cavity packages without resonators has commenced as a pipe-cleaning lot to identify any processing issues prior to the integration of the MEMS device in the package. Vacuum-cavity packages were designed that can package resonators ranging from 2 MHz to 100 MHz frequencies.

4.5.1 Fabrication

Figures 4.3a-4.3d show the CoventorWare models and the fabricated packages at different stages of fabrication. The left column describes the process flow and the right column describes the optical pictures of the fabricated vacuum-packages. The fabrication process flow starts with a deposition of 6000 A^o silicon dioxide insulation layer followed by spin coating 4.0 µm polyimide sacrificial layer. The polyimide (Figure 4.3a) is then cured at 275 ^oC for 4 hours to get a thickness of 2.5 µm. Next, 0.8 µm thick aluminum oxide layer is deposited by rf sputtering. Trench cuts are made (Figure 4.3b) in the aluminum oxide layer by etching the aluminum oxide using hydrofluoric acid (HF) to facilitate the removal of sacrificial layer. The sacrificial layer is removed (Figure 4.3c) using an oxygen-based plasma asher and the cavity is sealed by depositing 3.5 µm thick aluminum oxide sealing layer (Figure 4.3d) by rf sputtering at 10 mTorr pressure. Since the deposition is done at an extremely low pressure environment (10 mTorr), the packages are vacuum-packaged.

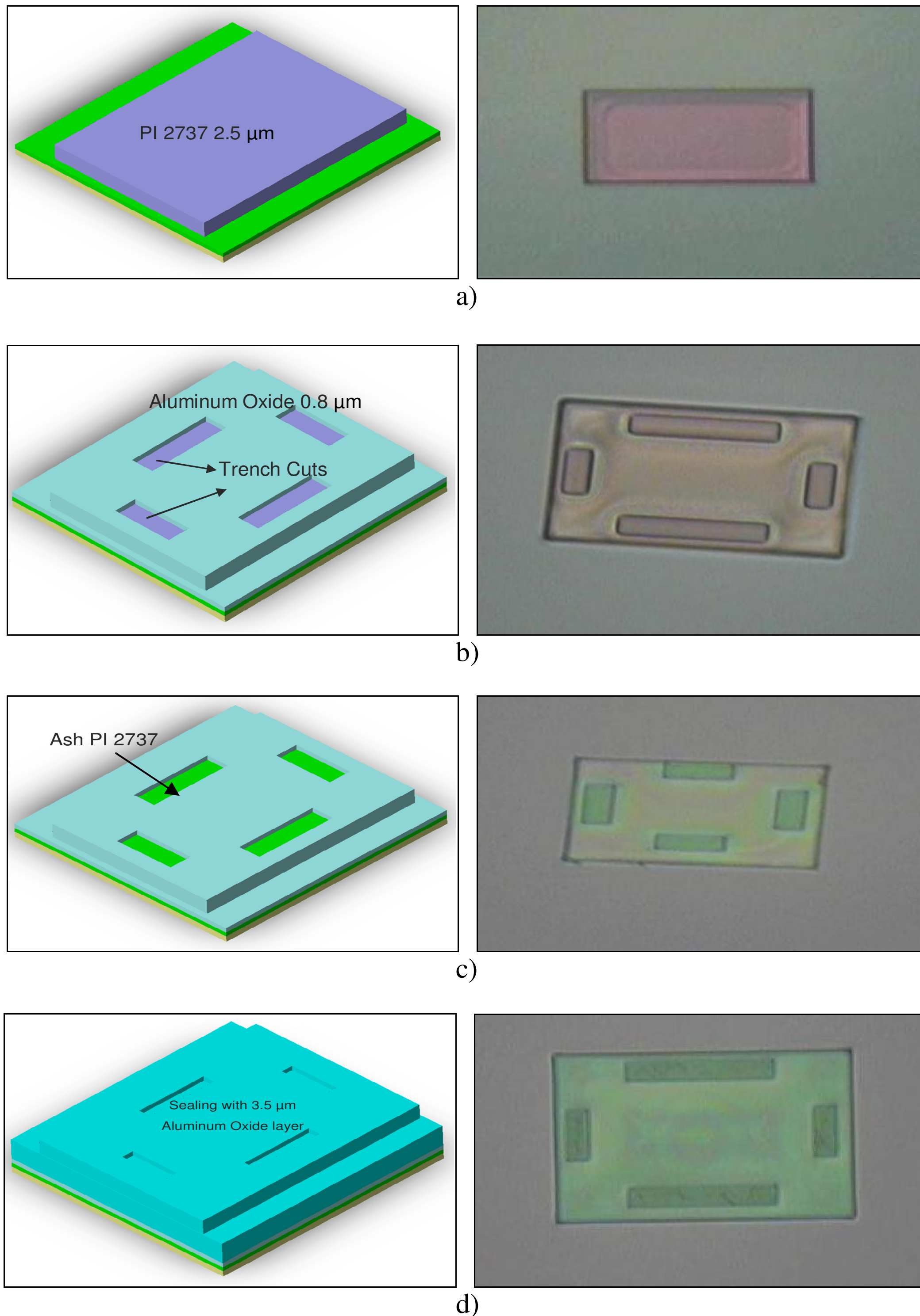


Figure 4.3 CoventorWare model and optical pictures of fabricated vacuum-cavity packages a) Poyimide after curing on top of silicon dioxide on a clean wafer b) Aluminum oxide deposition followed by trench-cut openings c) Ash polyimide sacrificial layer d) Seal the cavity with aluminum oxide layer.

Figure 4.4a shows the SEM micrograph of vacuum-cavity package that would package a 2 MHz resonator. A focused-ion-beam (FIB) was cut into the package to show the presence of a vacuum-cavity. From Figure 4.4b, we can see the presence of a vacuum-cavity in the package.

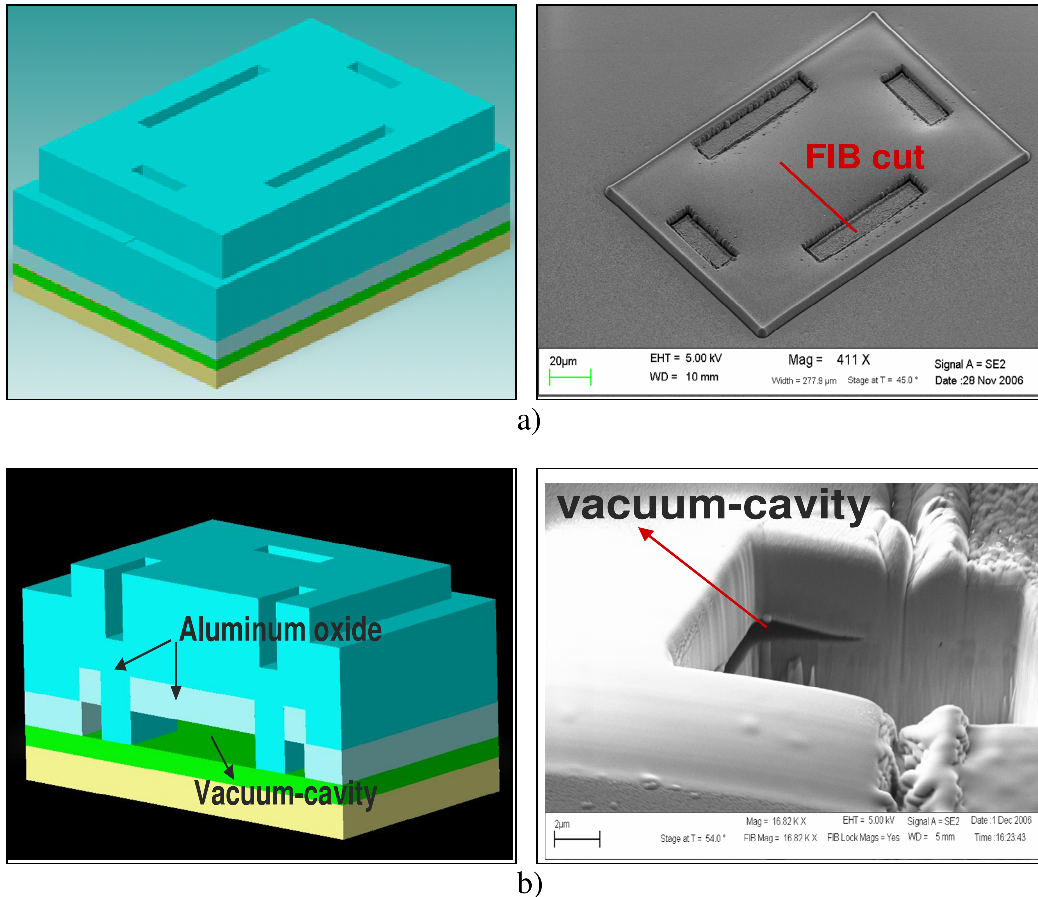
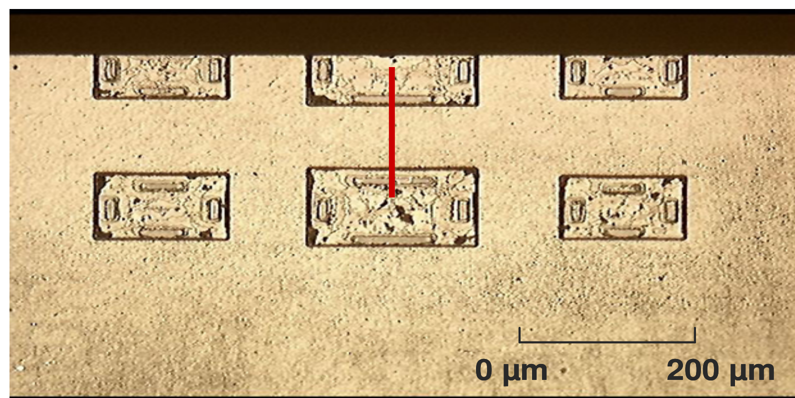


Figure 4.4 CoventorWare model and SEM picture of a) vacuum-cavity package without the resonator b) focused ion beam (FIB) cut into the vacuum-package to show the presence of a vacuum-cavity.

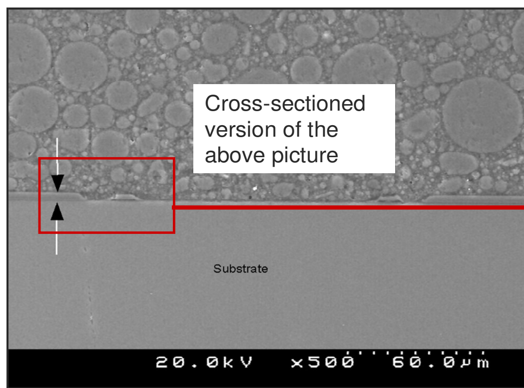
4.5.2 Over-molding vacuum-cavity packages

The fabricated vacuum-cavity packages were sent to Freescale Semiconductor for over-molding process. The over-molding process was done at Freescale Semiconductor using the appropriate mold material. These packages would package 2, 5, 10, 15, 20, 25

MHz resonators. Figure 4.5a shows six different vacuum-cavity packages after the over-molding process. An FIB cut was made in these packages and Figure 4.5b shows the cross-section of a cut made in the center of the packages as shown by red line in Figure 4.5a. Figure 4.5c shows the magnified image of 4.5b and we can see that the packages are still intact and have survived the over-molding process. Also, no major processing issues were encountered during the vacuum-cavity package fabrication process.



a)



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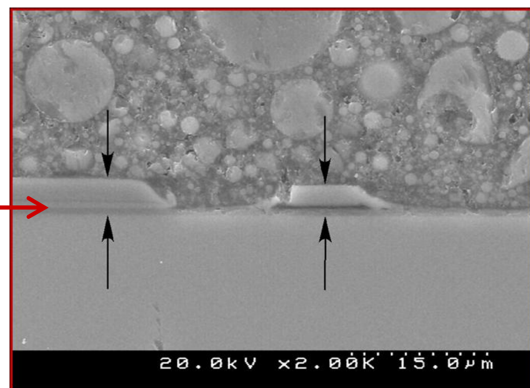


c)

Figure 4.5 a) Vacuum-cavity packages after the over-molding process b) Cross-sectioned version of 4.5a c) Magnified image of 4.5b.

The technique of fabricating the vacuum-cavity packages without the resonators gives a strong foundation to foresee any upcoming issues or challenges in the fabrication of vacuum-cavity packages with the resonators.

4.6 RF MEMS resonator

4.6.1 Design

The complete integration of analog functions such as filters, mixers, reference oscillators, and duplexers is crucial for reduced system form factor, higher performance, improved functionality, and reduced cost. These functions generally require the use of resonators and are currently implemented either by using expensive and large discrete parts, through on-chip integration using low-Q (quality factor) LC circuits that require large areas of expensive silicon, or through active CMOS-circuits which often have low-Q and high power consumption. Integrated MEMS resonators have the potential to integrate all of the above functions without the drawback of existing solutions and decrease in size with increasing frequency; have high-Q (quality factor), low power consumption, and the potential for co-integration with CMOS backend process flows.

The fixed-fixed resonator beam design was done by Freescale Semiconductor Inc. and modifications were made in the design to fit according to the compatibility of the equipment in the clean room at UTA.

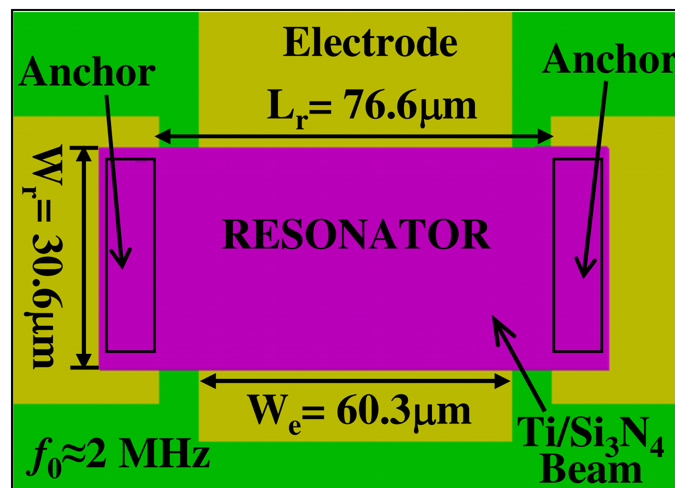
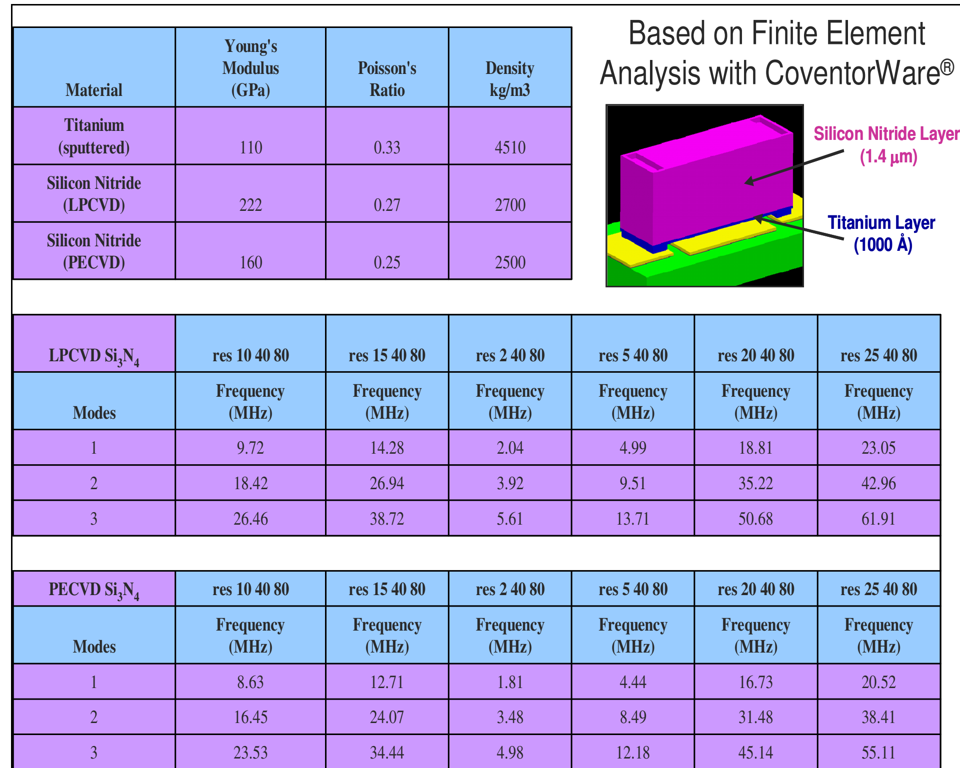


Figure 4.6 Top view of a 2 MHz MEMS Resonator design.

The fundamental mode resonator frequency for this design is given by the following equation[60].

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{K_r}{m_r}} = 1.03\sqrt{\frac{E}{\rho}}\frac{h}{L_r^2}$$

where K_r is the beam stiffness, m_r is the mass of the beam, E is the Young's modulus, ρ is the beam material density, h and L_r are the thickness and length of the beam. Resonators in the frequency range 2 MHz – 100 MHz were designed.



Material	Young's Modulus (GPa)	Poisson's Ratio	Density kg/m3
Titanium (sputtered)	110	0.33	4510
Silicon Nitride (LPCVD)	222	0.27	2700
Silicon Nitride (PECVD)	160	0.25	2500

LPCVD Si_3N_4	res 10 40 80	res 15 40 80	res 2 40 80	res 5 40 80	res 20 40 80	res 25 40 80
Modes	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
1	9.72	14.28	2.04	4.99	18.81	23.05
2	18.42	26.94	3.92	9.51	35.22	42.96
3	26.46	38.72	5.61	13.71	50.68	61.91

PECVD Si_3N_4	res 10 40 80	res 15 40 80	res 2 40 80	res 5 40 80	res 20 40 80	res 25 40 80
Modes	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
1	8.63	12.71	1.81	4.44	16.73	20.52
2	16.45	24.07	3.48	8.49	31.48	38.41
3	23.53	34.44	4.98	12.18	45.14	55.11

Figure 4.7 Resonant frequency simulation results.

Figure 4.7 shows the resonant frequency simulation results CoventorWare. The material properties used in the design are as shown in the top table in Figure 4.7. The next two tables in Figure 4.7 show the resonators' fabrication with the beam material comprising of Low-Pressure Chemical Vapor Deposition (LPCVD) and Plasma

Enhanced Chemical Vapor Deposition (PECVD) silicon nitride and titanium. The designed values and the simulated values match proving the integrity of the design.

4.6.2 Fabrication

The methodology used to fabricate the fixed-fixed resonators using polyimide PI2737 as a sacrificial release layer is outlined in the following paragraph and is illustrated in Figure 4.8.

The fabrication of MEMS resonator is based on a surface micromachining technique[61,62]. The process flow, as shown in Figures 4.8a-4.8d starts with deposition of silicon dioxide using wet oxidation process on a clean silicon wafer serving as an insulating layer between the metal conductor and the silicon substrate. Next, a bi-layer 670 A^o thick titanium/gold thin film (Figure 4.8a) is deposited by rf sputtering and patterned using standard lift-off technique to form the electrode, anchor and conductors. Next, photo-definable polyimide PI2737 from HD Microsystems was used as the sacrificial layer. The polyimide PI2737 was diluted with thinner T-9039 and kept overnight to mix properly. The resultant polyimide can be used to form sacrificial layer of thickness 1000 A^o to 5000 A^o. The 3100 A^o thick sacrificial layer was spin coated, cured at 275 ^oC for two hours thirty minutes to define the critical air-gap height 1700 A^o (Figure 4.8b) between the resonator beam and the drive electrode. The resonator beam 2.2 µm thick, consisting of titanium metal layer and low stress aluminum oxide layer was then deposited by rf sputtering and patterned using lift-off technique (Figure 4.8c). Finally, sacrificial layer was removed using an oxygen-based plasma asher to form fully suspended resonators (Figure 4.8d).

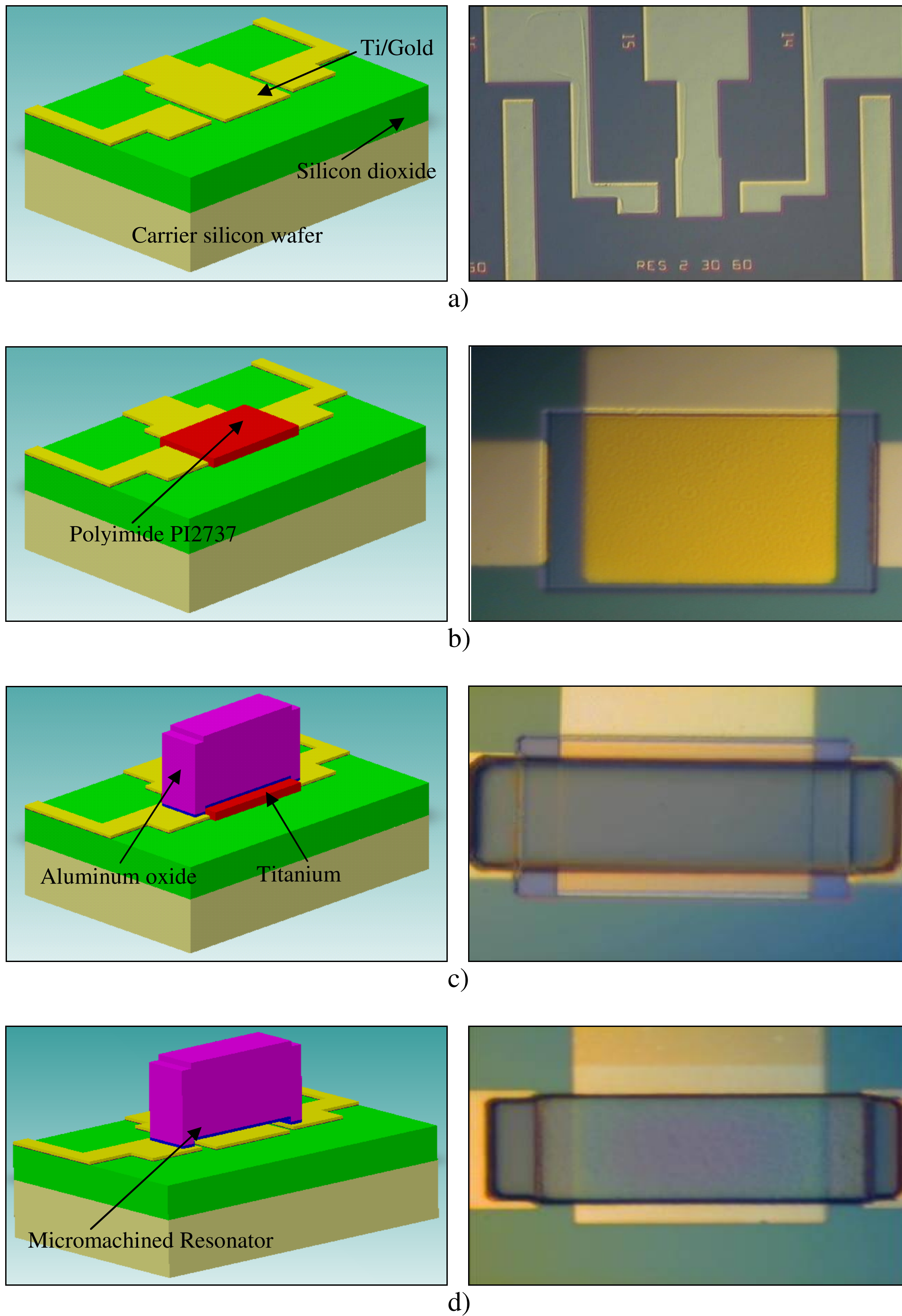
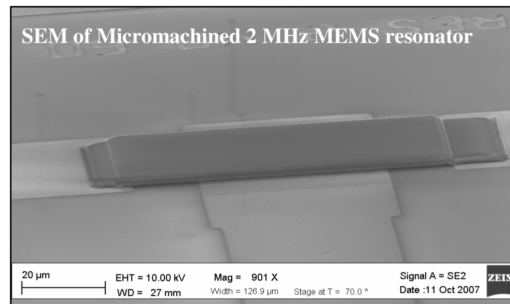


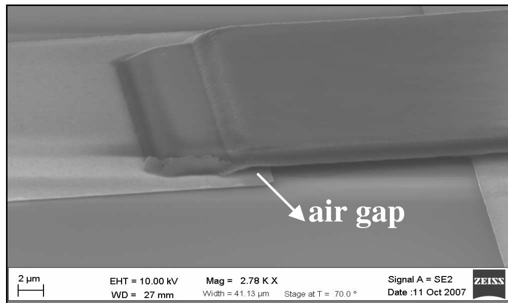
Figure 4.8 CoventorWare model and fabricated optical pictures of a) Titanium and gold metal layer b) sacrificial layer c) titanium/aluminum oxide layer to form the resonator beam d) Ash the sacrificial layer to release the resonator.

4.6.3 SEM of fabricated devices

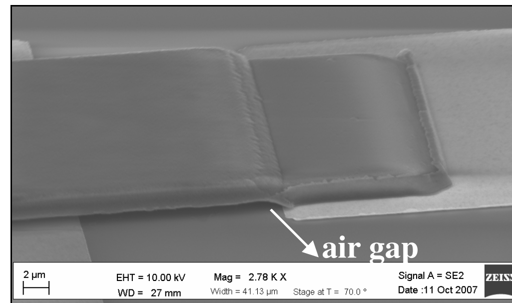
Scanning electron microscopy (SEM) analyses was done to verify release of the bridge structures. Figure 4.9a shows the SEM of a 2 MHz resonator. From Figures 4.9b and 4.9c, we can clearly see that the device is fully released. Also, it is evident from the SEM micrographs of 5 MHz resonator (Figure 4.9d) and 10 MHz resonator (Figure 4.9e) that the devices are fully released.



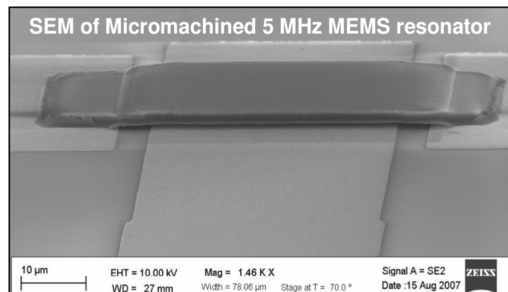
a)



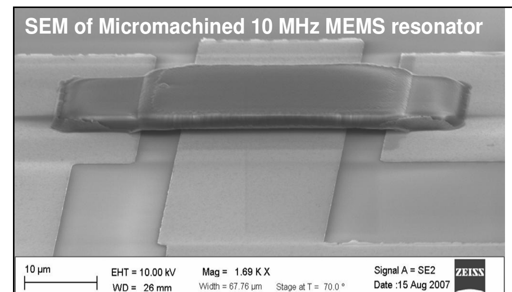
b)



c)



d)

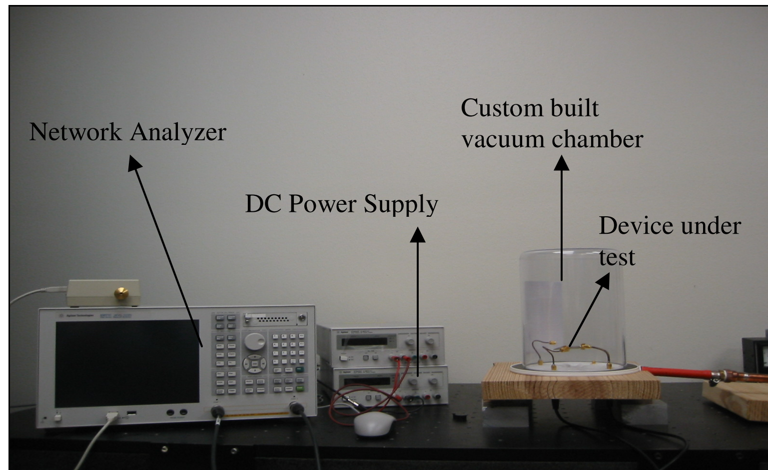


e)

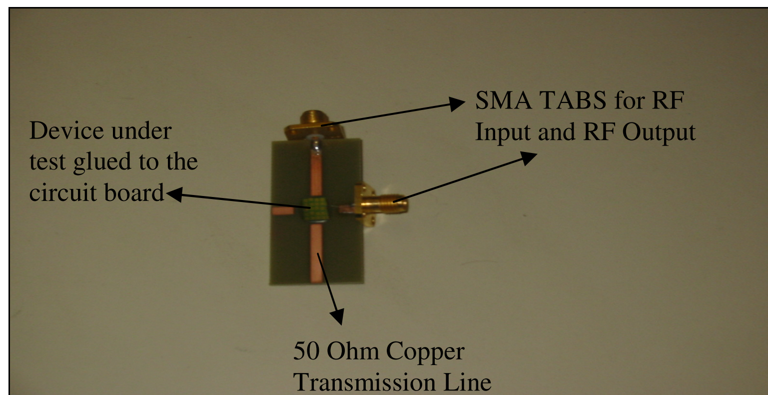
Figure 4.9 SEM of a) Micromachined 2 MHz resonator b) Magnified image at the left anchor c) Magnified image at the right anchor d) 5 MHz resonator e) 10 MHz resonator.

4.6.4 Characterization

DC characterization of the released devices was performed using an Agilent E3620A DC power supply for beam breakdown, V_{bd} (electrical breakdown or mechanical pull-down). The pull-down voltages measured for a 2MHz and a 5 MHz resonator were 51V and 58V respectively. RF resonance measurements were performed in a custom-built vacuum chamber as shown in Figure 4.10a. The device under test was glued and to a 50 Ω copper transmission line circuit board as shown in Figure 4.10b. The resonator was wire-bonded using WEST BOND bonding equipment.



a)



b)

Figure 4.10 a) RF characterization experimental setup b) Device under test glued to the circuit board.

Both input and output RF signals were provided and measured using an Agilent E5071C Series Network Analyzer. The DC bias was provided by the DC power supply. Figure 4.11 shows the measured RF response S_{21} of 2 MHz resonator of length 76.59 µm, width 30.64 µm, and electrode width 45.23 µm at a vacuum level of 30 mTorr. The measured RF response showed resonant frequency of 2.1265 MHz with a Q factor (~ 50).

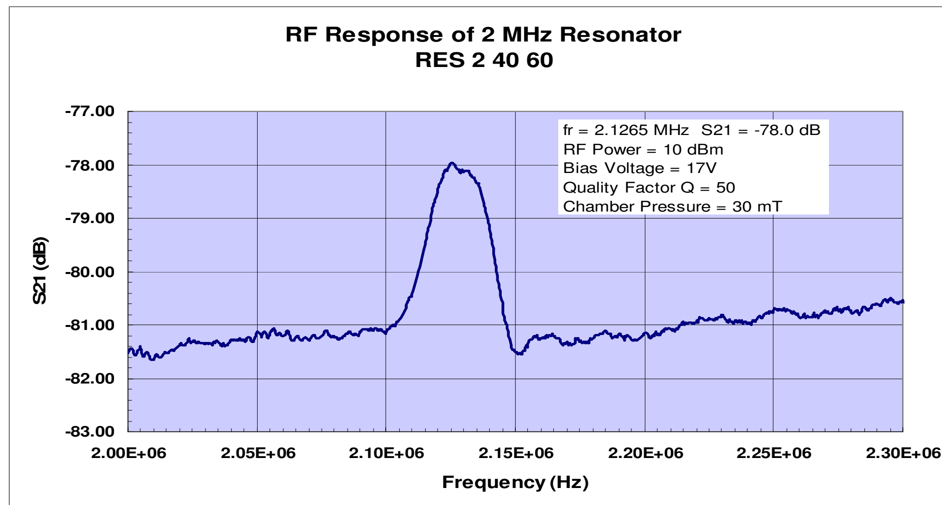


Figure 4.11 Measured S_{21} of 2 MHz resonator.

Figure 4.12 shows the measured RF response S_{21} of a 2 MHz resonator at the same vacuum level of 30 mTorr but at different bias voltages.

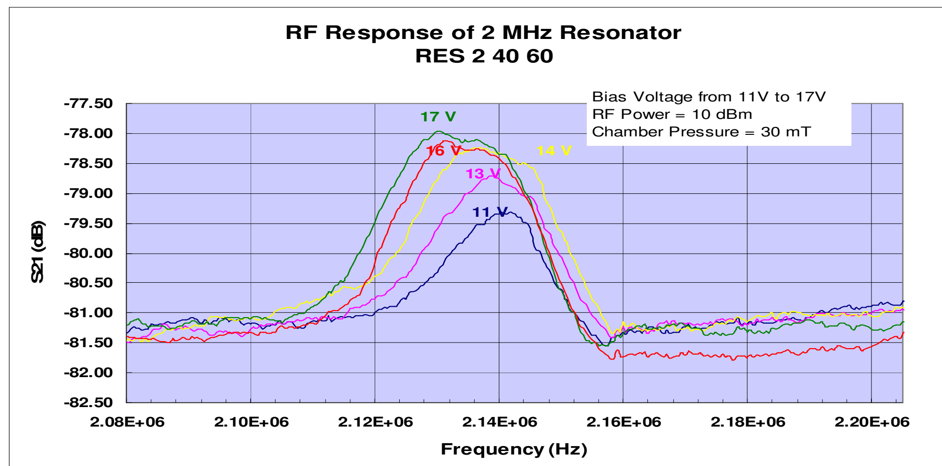


Figure 4.12 Measured S_{21} of 2 MHz resonator at different bias voltages.

Frequency tuning as a function of bias voltage has been measured and is shown in Figure 4.13. The frequency decrease with increasing bias voltage is due to the "spring softening" of the device, i.e. a decrease in the overall spring constant K_r of the device caused by a restoring force equal to but opposite in direction to the force derived from the electrostatic field provided by the bias voltage. DC-voltage tunability of MEM resonator frequency is important in order to compensate for manufacturing variations and ambient/operating temperature changes.

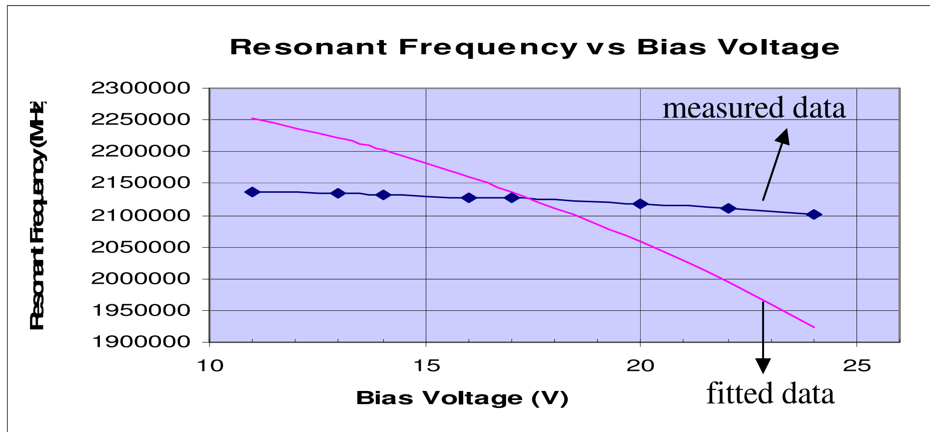


Figure 4.13 Measured resonance frequency versus bias voltage.

The theoretical expression[63] for the resonant frequency is given by

$$f_r = \frac{1}{2\pi}\sqrt{\frac{K_r}{m_r}} \qquad (1)$$

where K_r and m_r are the spring constant and mass of the resonator.

$K_r = 16EW_r(\frac{h}{L_r})^3 - \frac{C_o V_{dr}^{\ 2}}{d^2}$ and $m_r = 0.38\rho h L_r W_r$ where h, L_r, W_r, E, and ρ are the resonator height, length, width, Young's modulus, and beam material density, C_o is the resonator static capacitance, V_{dr} is the drive voltage, and d is the air-gap between the resonator beam and the drive electrode.

The curve in Figure 4.13 was fitted to the theoretical expression for resonant frequency given by equation (1) and the resonator beam material properties (E and ρ) were extracted using solver tool in Microsoft Excel. The goal of the optimization technique used in this method was to minimize the error between the calculated resonant frequency and the measured resonant frequency. The values for the material properties were chosen based on the minimum error obtained by the solver tool. The density, Young's modulus E[65] of resonator beam comprising of Al_2O_3 and Ti is 10540 kg/m^3 and 383 GPa respectively. The density and Young's modulus of the composite beam obtained by solver tool is 10641 kg/m^3 and 387 GPa which matches very well with the published data.

Figure 4.14 shows S_{21} of a 2 MHz resonator at different chamber pressures. We can see that S_{21} does not change much from 50 mT to 500 mT but it decreases at 1 Atm. pressure. If we have a better way of controlling from 500 mT to 1 Atm. pressure, a relationship between the Q factor and pressure variation could have been established. But this definitely proves that the resonator needs vacuum-packaging for proper operation.

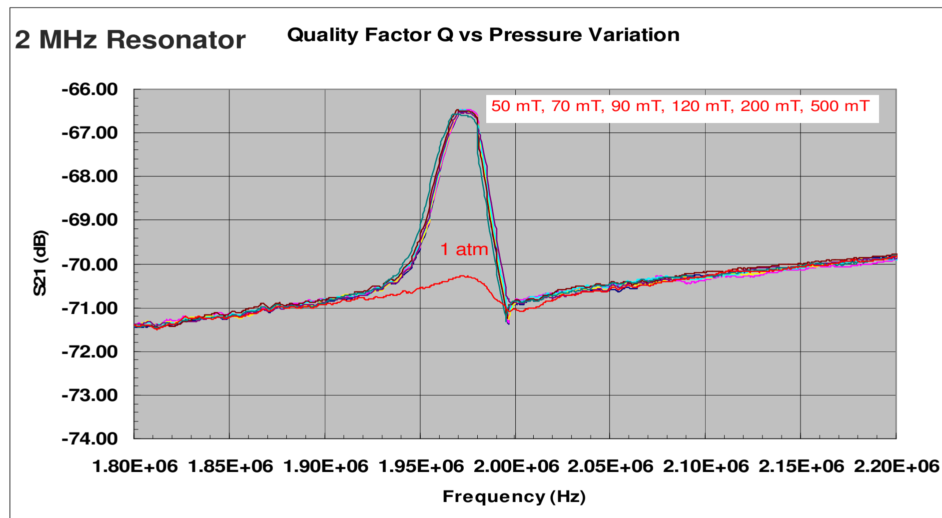


Figure 4.14 Measured resonance frequency at various pressures.

4.7 Vacuum-packaged RF MEMS resonator

This section details the design, and fabrication of packaged MEMS resonators using two different "self-packaging" approaches namely canopy and well structure.

4.7.1 Canopy structure

In this approach[64], a second sacrificial layer is used to define the vacuum-cavity to enclose the resonator followed by aluminum oxide encapsulation layer. Trench cuts are made in the encapsulation layer to remove both the sacrificial layers followed by deposition of a thick sealing layer at a low pressure (10 mTorr).

4.7.1.1 Fabrication

The fabrication process flow for the canopy structure, as shown in Figures 4.15a to 4.15f starts with the resonator not released (Figure 4.15a). This is done to protect the resonator from further processing steps. Next, spin coat 4.5 µm polyimide sacrificial layer and cure it at 275 ^{o}C for four hours to form a thickness of 2.5 µm (Figure 4.15b), followed by deposition of rf sputtered 0.83 µm aluminum oxide layer. Trench cuts (Figure 4.15c) are made in the aluminum oxide layer using lift-off technique to facilitate the removal of sacrificial layers 1 and 2. From Figure 4.15d, we can see that the second sacrificial layer is completely removed using an oxygen-based plasma asher. Currently ashing of the first sacrificial layer is going on since there are still traces of the first sacrificial layer as is evident from Figure 4.15d. Then, the cavity is sealed by depositing 3.5 µm rf sputtered Al_2O_3 sealing layer (Figure 4.15e). Since the deposition is done at 10 mTorr, the resonator is vacuum-packaged. Finally, bond pads are opened on the die to form the electrical leads for characterizing the self-packaged resonators (Figure 4.15f).

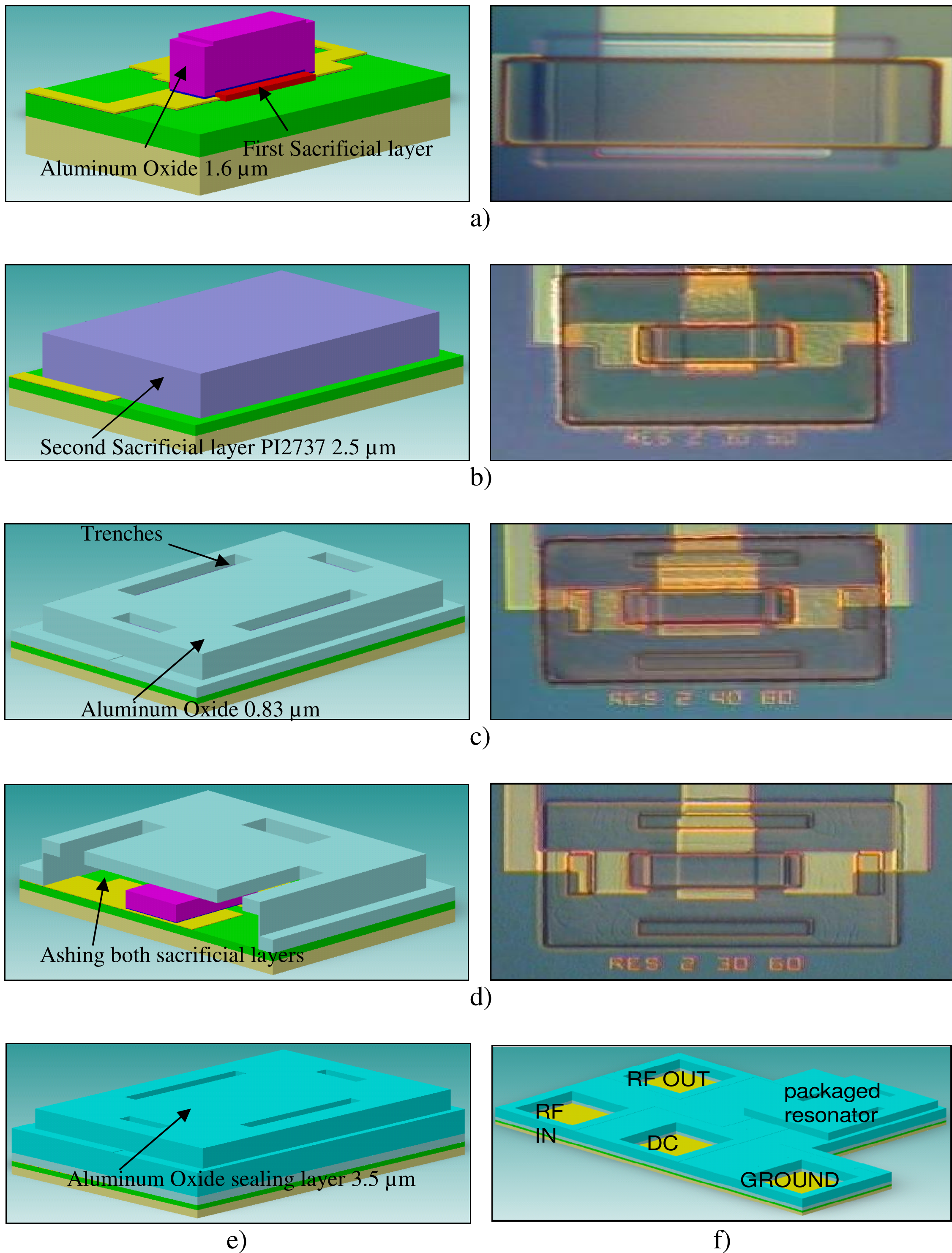


Figure 4.15 CoventorWare model and fabricated optical pictures of a) unreleased resonator b) spin coat second sacrificial layer c) deposit encapsulation layer d) ash first and second sacrificial layers e) deposit sealing layer at 10 mTorr pressure f) open bond pads.

4.7.1.2 Loading analysis

The mechanical strength of the canopy structure was simulated by CoventorWare. Pressure was applied on top of the package (Figure 4.16a). Figure 4.16b shows the lateral dimensions of a 2 MHz packaged resonator. The deflection (Figure 4.16c), maximum misses stress (Figure 4.16d) induced was simulated. The yield strength of Al_2O_3 sealing layer is 15.4 GPa[65]. From Figure 4.16d, the canopy structure packaging technique can withstand up to 103 Atm. pressure, making it an efficient packaging technique.

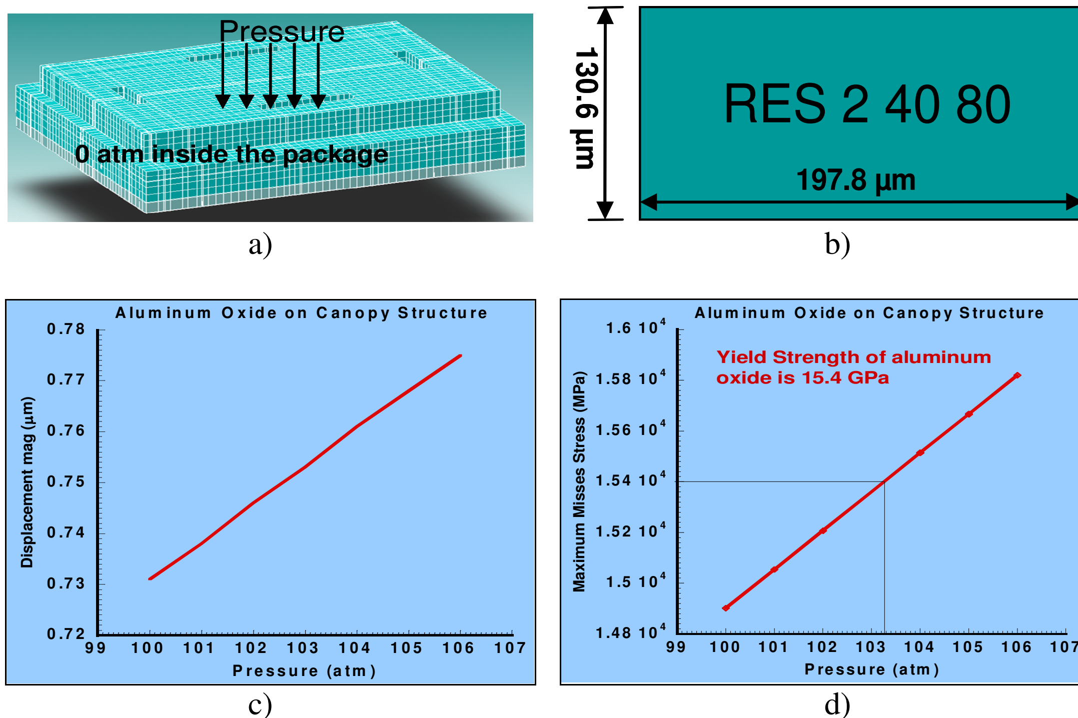


Figure 4.16 a) Meshed model of 2 MHz resonator built in CoventorWare b) Lateral dimensions of a 2 MHz resonator c) Simulated displacement versus pressure d) Simulated misses stress versus pressure.

4.7.2 Well structure

This technique[66] is different than the canopy structure in a way that a much thinner sealing layer would be sufficient to seal the vacuum-cavity and package the resonator. Also, this approach is used keeping silicon nitride sealing layer in mind.

4.7.2.1 Fabrication process flow

The fabrication process flow (Figures 4.17a to 4.17f) starts with the unreleased resonator and a well formation around it (Figure 4.17a). Next, spin coat 2.5 μm polyimide sacrificial layer (Figure 4.17b) followed by deposition of 1 μm silicon nitride layer (Figure 4.17c). Trench cuts are made in the silicon nitride layer to facilitate the removal of sacrificial layers 1 and 2 (Figure 4.17d). The cavity is then sealed by depositing 2 μm silicon nitride sealing layer (Figure 4.17e). Since the deposition is done at 10 mTorr, the resonator is vacuum-packaged. Finally, bond pads are opened on the die for characterizing the self-packaged resonators (Figure 4.17f).

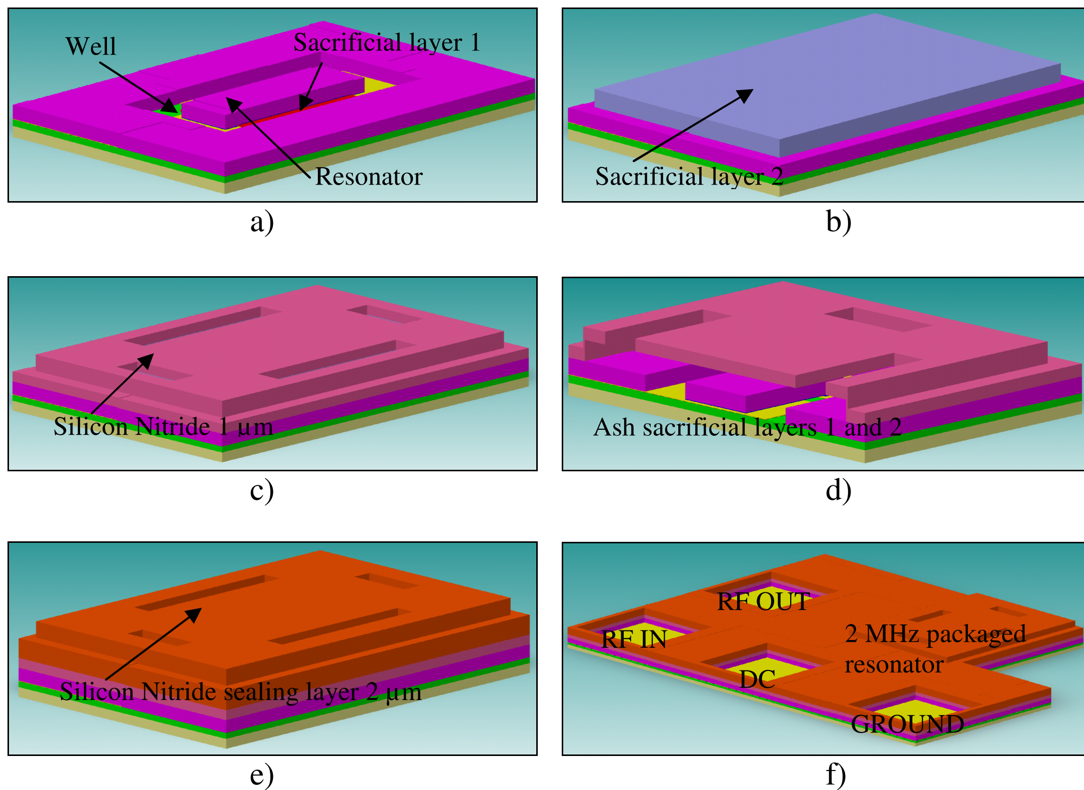


Figure 4.17 CoventorWare models of a) Well formation around the unreleased resonator b) spin coat second sacrificial layer c) deposit encapsulation layer d) Ash the first and second sacrificial layers to release the resonator e) deposit the sealing layer at 10 mTorr pressure f) open bond pads for electrical characterization.

4.7.2.2 Loading analysis

The mechanical strength of the vacuum cavity for well structure was also simulated using CoventorWare. Pressure is applied on top of the vacuum cavity (Figure 4.18a). Figure 4.18b shows the lateral dimensions of a 2 MHz packaged resonator. The deflection (Figure 4.18c), maximum misses stress (Figure 4.18d) induced was simulated. The yield strength of silicon nitride varies from 140 MPa to 2.4 GPa depending on the deposition process[65]. From Figure 4.18d, the well structure packaging technique can withstand up to 5 Atm. pressure, making it an efficient packaging technique.

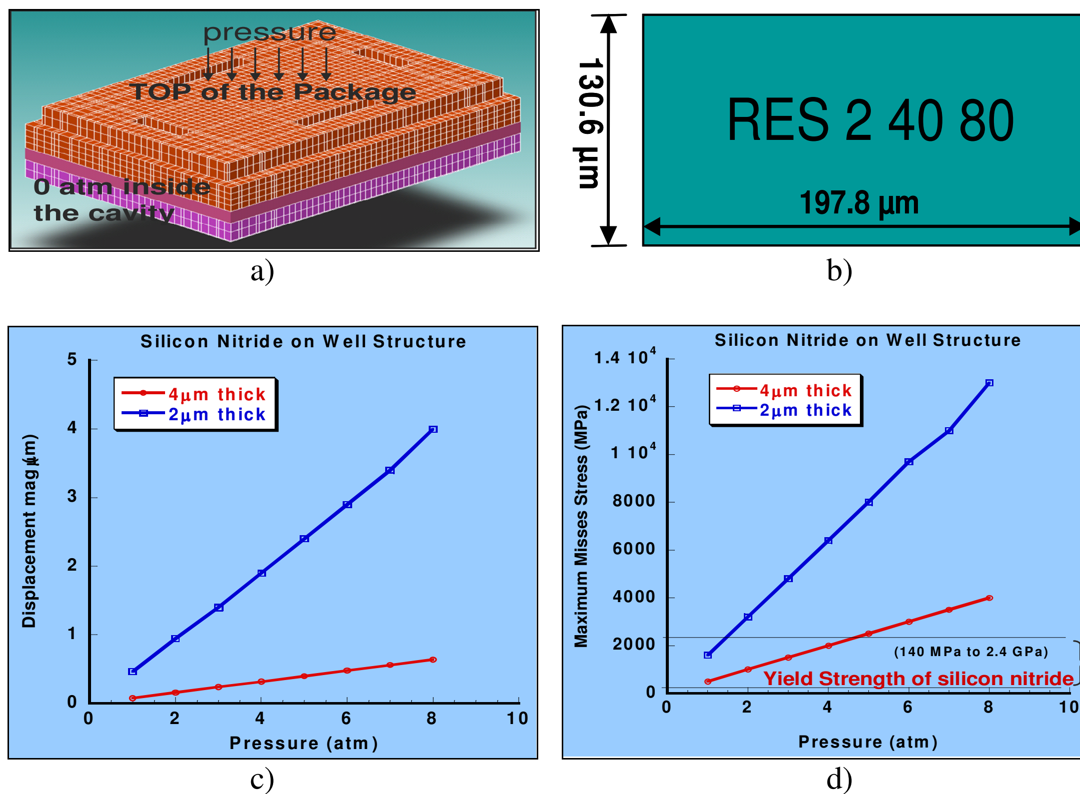


Figure 4.18 a) Meshed model of 2 MHz resonator built in CoventorWare b) Lateral dimensions of a 2 MHz resonator c) Simulated displacement versus pressure d) Simulated misses stress versus pressure.

4.8 Novelty

The novelty of the invention lies in the fact that the devices were self-packaged (vacuum-packaged). The integrity of the packaging would be verified using the packaged device (sensor in this case) itself. The packaged device is the MEMS resonator.

4.9 Summary

A novel device-level packaging technique for MEMS resonators was presented. Vacuum-cavity packages without MEMS resonators were successfully fabricated. No major processing issues were observed in the fabrication of vacuum-cavity packages prior to the integration of MEMS device in the package. MEMS resonators have been designed and successfully fabricated based on a surface micromachining technique. The RF response of 2 MHz resonators showed a quality factor Q~50 and a resonant frequency of 2.1265 MHz at 30 mTorr pressure. Two different self-packaging approaches namely canopy and well structures have been designed. The canopy and well self-packaging structures can withstand up to 103 Atm. and 5 Atm. of pressure respectively based on Finite Element Analysis with CoventorWare®. The pressure tolerances can be further increased by building the packages with thicker sealing layers. Packaging of MEMS resonators based on canopy technique is currently on-going and no major fabrication challenges have been faced so far. The second sacrificial layer was removed successfully thus forming a cavity around the resonator. Once the resonator is released completely by removing the first sacrificial layer, the cavity will be sealed by aluminum oxide sealing layer to form vacuum-packaged RF MEMS resonator.

CHAPTER 5

CONCLUSIONS

This dissertation has developed and demonstrated integrated MEMS microsensors that can improve performance in several sensor applications from a cost, size, and multifunction perspective. This dissertation has also introduced many areas for further studies.

Chapter 1 introduced the background of this work. Chapter 2 described the design and fabrication of semiconducting YBaCuO uncooled focal plane arrays. The CTIA readout circuit was designed and analyzed using AMI 1.5µm double-poly-double-metal n-well 2.5V CMOS technology. It was demonstrated through CADENCE simulations that a frame rate of 218 Hz can be achieved for a 640x480 array using the CTIA readout low-power design, which is crucial for medical imaging applications such as monitoring respiration and heart rate. Microbolometers were designed to interface with the CTIA readout circuit. The YBaCuO microbolometers were designed with two different electrode arm geometries to provide thermal isolation from the substrate. This was achieved by changing only one mask, which was used to pattern the sacrificial polyimide. The first electrode arm geometry was aimed at maximizing the detectivity (~ 10^9 $cmHz^{1/2}/W$) while maintaining a 5 msec thermal time constant which translates to the

traditional 30 Hz frame rate. The second electrode arm geometry was designed to achieve moderately low thermal conductance and low thermal mass of the self-supporting geometry to obtain a relatively fast thermal detector (200 Hz frame rate), thermal time constant less than 1 msec, while maintaining a detectivity (~ 10^8 cmHz$^{1/2}$/W). Self-supporting YBaCuO microbolometer pixel focal plane arrays (4x4, 32x32) were designed, fabricated and integrated for the first time with the CTIA CMOS readout circuitry. Several test-circuits were tested before and after the fabrication of YBaCuO microbolometers and it was found that the microbolometer fabrication process is CMOS compatible.

In chapter 3, a novel tunable infrared microspectrometer was presented. The coupled mode theory and Bloch wave analysis was verified for scattered radiation from diffraction gratings on the surface of waveguide structures. A 2.75 μm tunable microspectrometer was designed with 10% tunability and an absorptivity of 45%. The design parameters, grating period Λ and groove depth d, were adapted to span wavelengths in the mid-infrared region of the optical spectrum.

In chapter 4, a novel device-level packaging technique for MEMS resonators was presented. Vacuum-cavity packages without MEMS resonators were successfully fabricated and no major processing issues were observed in the fabrication of vacuum-cavity packages prior to the integration of MEMS device in the package. MEMS resonators were designed and successfully fabricated based on a surface micromachining technique. The RF response of 2 MHz resonators showed a quality factor Q~50 and a resonant frequency of 2.1265 MHz at 30 mTorr pressure. The DC-tuning of the resonator was verified by measuring the RF response at different bias voltages. Two different novel

and high payoff self-packaging approaches namely canopy and well structures were designed to package the MEMS resonators. The canopy and well self-packaging structures can withstand up to 103 Atm. and 5 Atm. of pressure respectively based on Finite Element Analysis with CoventorWare® simulations. It was also shown that the pressure tolerances can be further increased by building the packages with thicker sealing layers. Packaging of MEMS resonators based on canopy technique is currently on-going. The second sacrificial polyimide layer was removed and at present the first sacrificial layer is being removed. Once both the sacrificial layers have been removed completely, the package would be sealed and bond pads would be opened to characterize the resonators and test the integrity of vacuum in the package.

APPENDIX A

MICROBOLOMETER DESIGN TO ACHIEVE 30 HZ FRAME RATE

Microbolometer Design to achieve thermal time constant < 5 msec and Detectivity of 10^9 cmHz$^{1/2}$/W

$I_b := 1.5 \cdot 10^{-6}$	A	Bias current		
$R_b := 1 \cdot 10^{6}$	Ω	Microbolometer resistance	$\Delta f := 1$	Hz
$\beta := 0.032$	K^{-1}	Temperature coefficient of resistance		
$\eta := 0.6$		Efficiency		
$\sigma := 5.67 \cdot 10^{-12}$	$\frac{W}{cm^2 \cdot K^4}$	Stefan Boltzmann's constant		
$P_i := I_b^{\,2} \cdot R_b$		The heating power		
$k := 1.38 \cdot 10^{-23}$	$\frac{J}{K}$	Boltzmann's constant		
$T := 300$	K			

C_{th} Calculations

$c_{YBCO} := 2.65$	$\frac{J}{K \cdot cm^3}$	specific heat for YBCO
$c_{Au} := 2.47$	$\frac{J}{K \cdot cm^3}$	specific heat for gold
$c_{Ti} := 2.34$	$\frac{J}{K \cdot cm^3}$	specific heat for titanium

C_{th} for YBCO

$W_{YBCO} := 35 \cdot 10^{-4}$	cm	Length, Width and Thickness of YBCO
$L_{YBCO} := 35 \cdot 10^{-4}$	cm	
$T_{YBCO} := 0.4 \cdot 10^{-4}$	cm	

$A := W_{YBCO} \cdot L_{YBCO}$ Area of the Microbolometer

$C_{YBCO} := W_{YBCO} \cdot L_{YBCO} \cdot T_{YBCO} \cdot c_{YBCO}$ Thermal Capacitance of YBCO

C_{th} for Ti

$W_{Ti} := 5 \cdot 10^{-4}$	cm	Length, Width and Thickness of Titanium
$L_{Ti} := 55 \cdot 10^{-4}$	cm	

$T_{Ti} := 0.1 \cdot 10^{-4}$ cm

$C_{Ti} := W_{Ti} \cdot L_{Ti} \cdot T_{Ti} \cdot c_{Ti}$ Thermal Capacitance of Titanium

C_{th} for Au

Length, Width and Thickness of gold

$W_{Au} := 5 \cdot 10^{-4}$ cm

$L_{Au} := 5 \cdot 10^{-4}$ cm

$T_{Au} := 0.07 \cdot 10^{-4}$ cm

$C_{Au} := W_{Au} \cdot L_{Au} \cdot T_{Au} \cdot c_{Au}$ Thermal Capacitance of gold

Total C_{th}

$C_{th} := C_{YBCO} + 2 \cdot C_{Au} + 2 \cdot \frac{C_{Ti}}{3}$ Total Thermal Capacitance of the Microbolometer

G_{th} Calculation

$K_{Ti} := 0.219$ $\frac{W}{cm \cdot K}$

$G_{Ti} := \frac{(K_{Ti} \cdot W_{Ti} \cdot T_{Ti})}{L_{Ti}}$ $\frac{W}{K}$ The electrode arm thermal conductance

$G_{th} := 2 \cdot G_{Ti}$ $\frac{W}{K}$ The factor of 2 is present since there are two electrode arms

$G_{rad} := 8 \cdot \eta \cdot A \cdot \sigma \cdot T^3$ The radiative conductance

$G_{eff} := G_{th} + G_{rad} - \beta \cdot P_j$ $G_{eff} = 3.352 \times 10^{-7}$

$\tau_{th} := \frac{C_{th}}{G_{eff}}$ $\tau_{th} = 4.028 \times 10^{-3}$ seconds Thermal time constant

$f := 1, 10 .. 2000$

Responsivity Calculation

$$R_V(f) := \frac{(\eta \cdot \beta \cdot I_b \cdot R_b)}{G_{eff} \cdot \sqrt{1 + 4 \cdot \pi^2 \cdot f^2 \cdot \tau_{th}^2}}$$

Detectivity Calculation

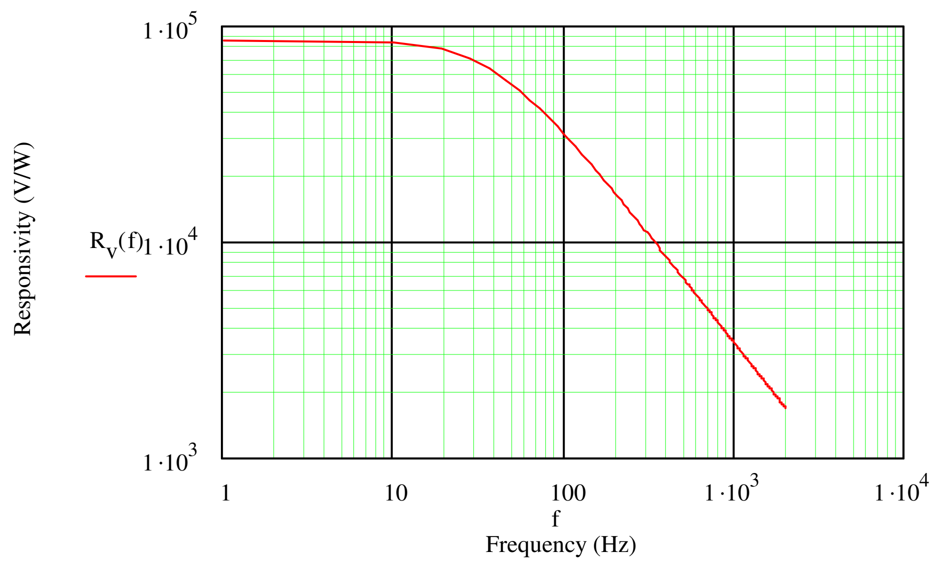
$V_n := \sqrt{4 \cdot k \cdot T \cdot R_b \cdot \Delta f}$ Johnson Noise

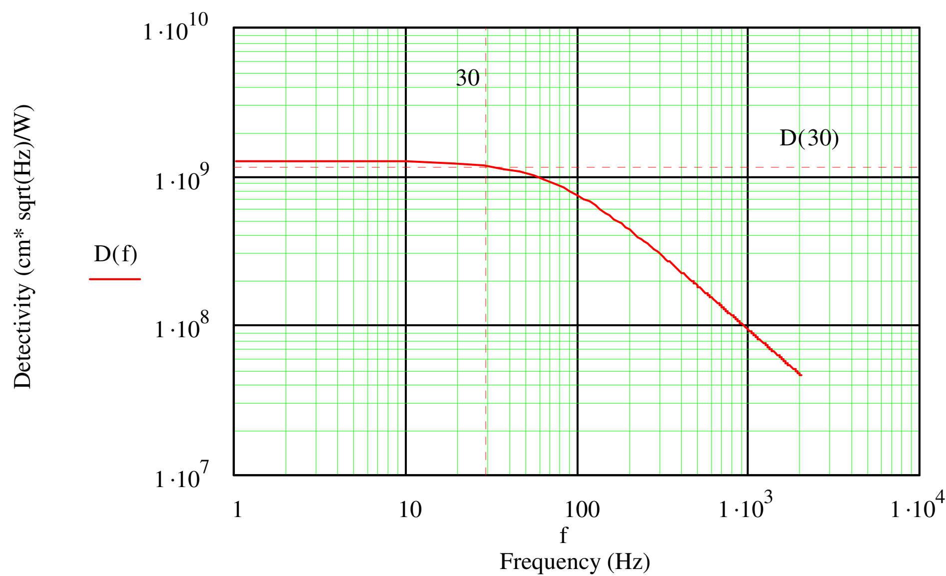
$V_{tf}(f) := R_V(f) \cdot \frac{\sqrt{4 \cdot k \cdot T^2 \cdot \Delta f \cdot G_{th}}}{\eta}$ Thermal Fluctuation Noise

$$V_{bg}(f) := R_V(f) \cdot \frac{\sqrt{4 \cdot k \cdot T^2 \cdot \Delta f \cdot G_{rad}}}{\eta}$$

Background Noise

$$D(f) := R_V(f) \cdot \frac{\sqrt{\Delta f \cdot A}}{\sqrt{V_n^{\,2} + V_{tf}(f)^2 + V_{bg}(f)^2}}$$





$D(1) = 1.248 \times 10^9$ $\quad D(30) = 1.157 \times 10^9$

Detectivity at 30 Hz

APPENDIX B

MICROBOLOMETER DESIGN TO ACHIEVE 200 HZ FRAME RATE

Microbolometer Design to achieve thermal time constant < 1 msec and Detectivity of 10^8 cmHz$^{1/2}$/W

$I_b := 1.5 \cdot 10^{-6}$ A — Bias current

$R_b := 1 \cdot 10^{6}$ Ω — Microbolometer resistance — $\Delta f := 1$ Hz

$A := \left(35 \cdot 10^{-4}\right)^2$ cm^2 — Area of the Microbolometer

$\beta := 0.032$ K^{-1} — Temperature coefficient of resistance

$\eta := 0.3$ — Efficiency

$\sigma := 5.67 \cdot 10^{-12}$ $\frac{W}{cm^2 \cdot K^4}$ — Stefan Boltzmann's constant

$P_i := I_b{}^2 \cdot R_b$ — The heating power

$k := 1.38 \cdot 10^{-23}$ $\frac{J}{K}$ — Boltzmann's constant

$T := 300$ K

C_{th} Calculations

$c_{YBCO} := 2.65$ $\frac{J}{K \cdot cm^3}$ — specific heat for YBCO

$c_{Au} := 2.47$ $\frac{J}{K \cdot cm^3}$ — specific heat for gold

$c_{Ti} := 2.34$ $\frac{J}{K \cdot cm^3}$ — specific heat for titanium

C_{th} for YBCO

$W_{YBCO} := 35 \cdot 10^{-4}$ cm — Length, Width and Thickness of YBCO

$L_{YBCO} := 35 \cdot 10^{-4}$ cm

$T_{YBCO} := 0.4 \cdot 10^{-4}$ cm

$C_{YBCO} := W_{YBCO} \cdot L_{YBCO} \cdot T_{YBCO} \cdot c_{YBCO}$ — Thermal Capacitance of YBCO

C_{th} for Ti

$W_{Ti} := 5 \cdot 10^{-4}$ cm — Length, Width and Thickness of Titanium

$L_{Ti} := 24 \cdot 10^{-4}$ cm

$T_{Ti} := 0.2 \cdot 10^{-4}$ cm

$C_{Ti} := W_{Ti} \cdot L_{Ti} \cdot T_{Ti} \cdot c_{Ti}$ Thermal Capacitance of Titanium

C_{th} for Au

$W_{Au} := 5 \cdot 10^{-4}$ cm Length, Width and Thickness of gold

$L_{Au} := 5 \cdot 10^{-4}$ cm

$T_{Au} := 0.07 \cdot 10^{-4}$ cm

$C_{Au} := W_{Au} \cdot L_{Au} \cdot T_{Au} \cdot c_{Au}$ Thermal Capacitance of gold

Total C_{th}

$C_{th} := C_{YBCO} + 2 \cdot C_{Au} + 2 \cdot \frac{C_{Ti}}{3}$ Total Thermal Capacitance of the Microbolometer

G_{th} Calculation

$K_{Ti} := 0.219$ $\frac{W}{cm \cdot K}$

$G_{Ti} := \frac{(K_{Ti} \cdot W_{Ti} \cdot T_{Ti})}{L_{Ti}}$ $\frac{W}{K}$ The electrode arm thermal conductance

The factor of 2 is present since there are two electrode arms

$G_{th} := 2 \cdot G_{Ti}$

$G_{th} = 1.825 \times 10^{-6}$ $\frac{W}{K}$

$G_{rad} := 8 \cdot \eta \cdot A \cdot \sigma \cdot T^3$ The radiative conductance

$G_{eff} := G_{th} + G_{rad} + \beta \cdot P_i$ $G_{eff} = 1.902 \times 10^{-6}$

$\tau_{th} := \frac{C_{th}}{G_{eff}}$ $\tau_{th} = 7.071 \times 10^{-4}$ seconds Thermal time constant

$f := 1, 10 .. 2000$

Responsivity Calculation

$$R_V(f) := \frac{(\eta \cdot \beta \cdot I_b \cdot R_b)}{G_{eff} \cdot \sqrt{1 + 4 \cdot \pi^2 \cdot f^2 \cdot \tau_{th}^2}}$$

Detectivity Calculation

$V_n := \sqrt{4 \cdot k \cdot T \cdot R_b \cdot \Delta f}$ Johnson Noise

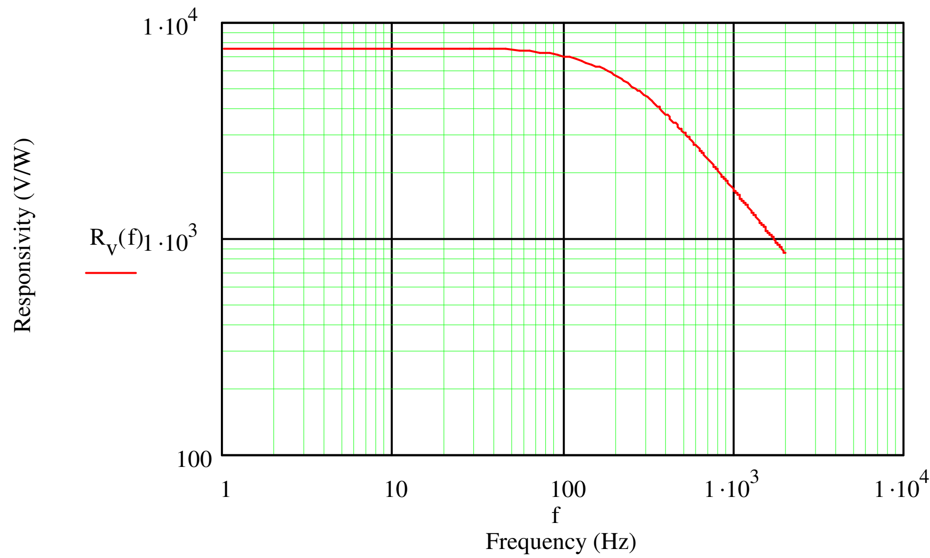
$$V_{tf}(f) := R_V(f)\cdot\frac{\sqrt{4\cdot k\cdot T^2\cdot\Delta f\cdot G_{th}}}{\eta}$$

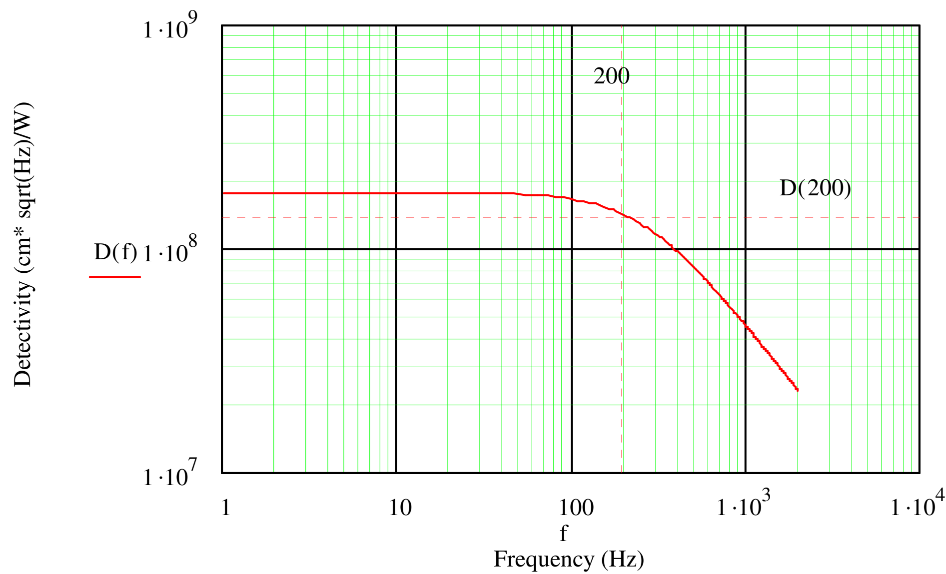
Thermal Fluctuation Noise

$$V_{bg}(f) := R_V(f)\cdot\frac{\sqrt{4\cdot k\cdot T^2\cdot\Delta f\cdot G_{rad}}}{\eta}$$

Background Noise

$$D(f) := R_V(f)\cdot\frac{\sqrt{\Delta f\cdot A}}{\sqrt{V_n{}^2 + V_{tf}(f)^2 + V_{bg}(f)^2}}$$





$D(1) = 1.773\times 10^8$ $D(200) = 1.408\times 10^8$ **Detectivity at 200 Hz**

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