DESIGN OF A SIGNAL GENERATOR USING CURRENT FEEDBACK OPERATIONAL AMPLIFIERS

by

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ABSTRACT

DESIGN OF A SIGNAL GENERATOR USING CURRENT FEEDBACK OPERATIONAL AMPLIFIERS

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Sinusoidal, triangular and rectangular waveforms are generated using current feedback operational amplifiers. A signal generator using a Current Feedback Operational Amplifier (CFOA) was designed, simulated and fabricated. The simulated frequency of oscillation for the sinusoidal wave is 13.13 MHz to 23.94 MHz, for the triangular and the rectangular wave are 6.78 MHz to 59.5 MHz in simulation. The current feedback operational amplifier can achieve higher oscillation frequency than a voltage feedback operational amplifier.

Two different types of current feedback operational amplifiers were designed. These are the double buffer current feedback operational amplifier and the double buffer current booster current feedback operational amplifier. A macro-model for the double buffer CFOA is developed as well. Although the voltage feedback amplifier has many advantages, the current feedback amplifier can operate at higher frequencies. Three test chips for the current feedback operational amplifier were designed. UTA246V, UTA246W are the double buffer CFOA and UTA246X is double buffer current booster CFOA. A triangular and rectangular wave generator was built using the UTA246W CFOA. The frequency of oscillation was found 2.8 MHz.

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CHAPTER 1

INTRODUCTION

In today's electronic systems, various forms of signals are necessary, such as sinusoidal, square, triangular, pulse, waves. Computer and control systems need clock pulses. In communication systems, there are a variety of waveforms needed for modulation waveforms. Triangular waves are used for scanning an electron beam on a CRT screen, in precise time measurements, and in time modulation. The sine wave is the most fundamental waveform. In a mathematical sense, any other waveform can be expressed as the Fourier combination of basic sine waves. Sine waves are used extensively in test, reference, and carrier signals. Despite its simplicity, the generation of a pure sine wave is challenging. Sinusoidal, triangular and rectangular waveforms are generated using current feedback operational amplifiers.

1.1 Organization

Chapter 2 focuses on bipolar junction transistor characterization. It presents the modes of operation for a BJT, I-V characteristics, transistor current gain, β, and transition frequency, f_T.

Chapter 3 focuses on current feedback operation amplifiers. It presents the applications, the advantages, and the disadvantages of the current feedback operational amplifier. Input offset voltage, input bias current, common mode input range, output

voltage swing, common mode rejection ratio, and power supply rejection ratio of the CFOA discussed in this chapter. Finally a proposed CFOA schematic diagram and the simulation results for the CFOA presented here.

Chapter 4 presents the macro-model for the current feedback operational amplifier. It also presents the macro-model parameter extraction process from the full CFOA model.

Chapter 5 presents the slew rate for the current feedback operational amplifier. It also presents the slew rate improvement technique for the CFOA. It presents the critical resistance for the CFOA, gain bandwidth product and the slew rate relationship for the VFOA, gain bandwidth product for the CFOA in the non-inverting gain configuration. Finally presents the trade off between the slew rate, the quiescent current, and bandwidth for the CFOA.

Chapter 6 presents the CFOA parameters with temperature. These parameters are the input offset current (I_{OS}), input offset voltage (V_{OS}), common mode input range (CMIR), common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), open loop transimpedance, slew rate, quiescent current, bandwidth, and output swing.

Chapter 7 presents the sinusoidal wave generator using a current feedback operational amplifier. It presents the condition of oscillation, challenges for practical oscillator design.

Chapter 8 presents the triangular and rectangular wave generators using current feedback operational amplifiers. It presents the multivibrators and integrators.

Chapter 9 presents the CFOA layout and measurement. Three CFOAs have been fabricated by National Semiconductor, Inc. Test circuits and results for measuring the CMRR, CMIR, PSRR, slew rate, input offset current, input offset voltage of the CFOA presented in this chapter.

In chapter 10, a summery of the results and the future work presented.

CHAPTER 2

BIPOLAR JUNCTION TRANSISTOR

Bipolar junction transistors are used in designing the current feedback operational amplifiers and the signal generator. So it is necessary to discuss the characteristics of the BJT. The BJT offers higher power handling and greater bandwidth than typical MOS devices.

2.1 Modes of Operation for a BJT

The four possible regions of operation for an NPN transistor is shown in Figure 2.1. In the forward active region, the base-emitter junction is forward biased and the

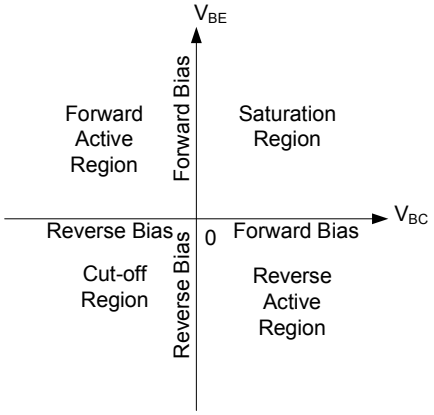


Figure 2.1 Modes of operation for an NPN transistor

base-collector junction is reverse biased. In the reverse active region, the base-emitter junction is reverse biased and base-collector junction is forward biased. In the cut-off region, both base-emitter and base-collector region is reverse biased. In the saturation region, both base-emitter and base-collector regions are forward biased.

In analog electronic circuits, transistors are usually biased in the forward active region. In this region, the transistor gain, β, is high. The saturation region of a bipolar transistor is usually avoided because the transistor gain, β, in this region is very low. In the reverse active region, the collector injects electrons into the base region [1]. Here the injection efficiency is poor because the collector is more lightly doped than the emitter. In the cut-off region, the transistor is off. Hence there is no collector current, because there is no charge in the base region.

2.2 I-V Characteristics

The I_C versus V_{CE} characteristic for an ideal common emitter NPN transistor is shown in Figure 2.2. In the active region, where I_B is fixed, I_C is constant when V_{CE}

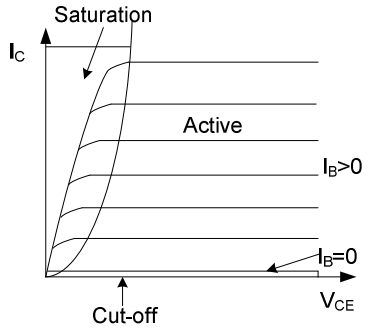


Figure 2.2 I_C-V_{CE} characteristic for an ideal NPN transistor

changes. Because any further increase of the reverse bias, the base-collector junction voltages change and the base-emitter junction voltage is fixed which is controlled by I_B [2]. In active region, the current gain, $\beta=I_C/I_B$ is very large. For a real transistor, I_C is not constant but has a slight positive slope. If I_C plot is extrapolated back onto the V_{CE} axis, it meets into a point. This point is called Early voltage. The Early voltage is

$$V_A = \frac{I_C}{\frac{\partial I_C}{\partial V_{CE}}} \tag{2.1}$$

The real NPN transistor I_C-V_{CE} characteristic is shown in Figure 2.3.

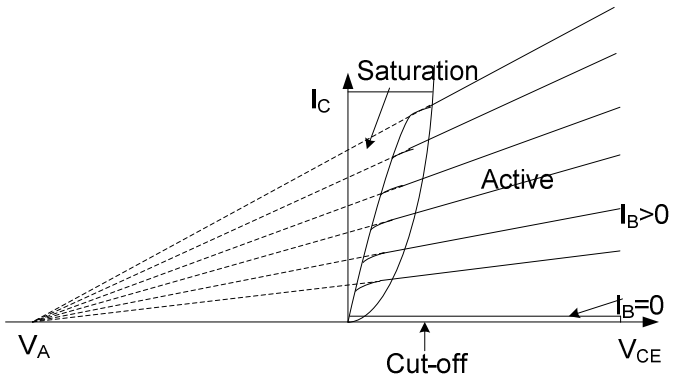


Figure 2.3 Real NPN transistor I_C-V_{CE} characteristic

2.3 Space-Charge Recombination Current

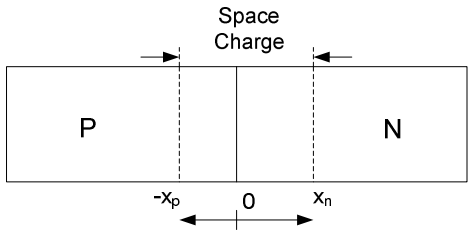


Figure 2.4 P-N junction diode

The p-n junction diode is shown in Figure 2.4. The space-charge recombination current for a forward biased p-n junction diode can be calculated from the continuity equation. The continuity equation for the hole current density $J_p(x)$ is

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\frac{\partial J_P}{\partial x} + G_P - R_P \tag{2.2}$$

Here G_P and R_P are the generation and recombination rates. At steady state with no external generation $\partial p/\partial t = 0$ and $G_P = 0$. The continuity equation can be rewritten as

$$-\frac{dJ_P}{dx} = qR_P \tag{2.3}$$

Integrating equation (2.3) for the depletion region of the p-n junction, gives

$$-\left[J_P(x_n) - J_P(-x_p)\right] = q\int_{-x_p}^{x_n} R_P dx \tag{2.4}$$

Since, $J_P(x_n) = 0$, the equation for the space-charge recombination current density is

$$J_{scr} = q\int_{-x_p}^{x_n} R_P dx \tag{2.5}$$

The recombination rate in equation (2.5) will vary with position. The usual assumption made to find the closed form solution of the integral is to use the maximum recombination rate. The maximum recombination rate for $V_a > 3kT/q$ is

$$R_P(\max) = \frac{n_i}{2\tau_p}\exp\left(\frac{qV_a}{2kT}\right) \tag{2.6}$$

Here V_a is the external voltage applied to the p-n junction. Substituting R_P into equation (2.5)

$$J_{scr} = \frac{n_i}{2\tau_p}\exp\left(\frac{qV_a}{2kT}\right)\left[x_n + x_p\right] \tag{2.7}$$

The space charge recombination current is

$$I_{scr} = J_{scr}A \tag{2.8}$$

$$I_{scr} = \left[x_n + x_p\right]\frac{n_i A}{2\tau_p}\exp\left(\frac{qV_a}{2kT}\right) \tag{2.9}$$

$I_{s-scr} = \left[x_n + x_p\right]\frac{n_i A}{2\tau_p}$ is called the saturation space-charge recombination density. Thus the space charge recombination current for a forward biased p-n junction diode is

$$I_{scr} = Is_{scr} \exp\left(\frac{qV_a}{2kT}\right) \tag{2.10}$$

2.4 Transistor Current Gain, β

The transistor current gain, β, changes with changing collector current. The variation of β with collector current can be divided into three regions. In the low current region, β increases as I_C increases. In the mid current region, β is approximately constant. In the high current region, β decreases as I_C increases. The behavior of β vs I_C can be explained by plotting base current I_B and collector current I_C on a log scale vs V_{BE}. An example plot is shown in Figure 2.5.

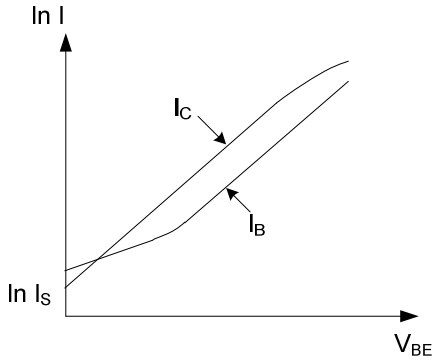


Figure 2.5 I_C and I_B versus V_{BE} for a BJT

In the mid current region, both I_B and I_C follow the Shockley model equation. The Shockley model for I_B and I_C is

$$I_B \approx \frac{I_S}{\beta_{FM}} \exp\frac{V_{BE}}{V_T} \tag{2.11}$$

$$I_C = I_S \exp\frac{V_{BE}}{V_T} \tag{2.12}$$

The value, β_{FM}, is the maximum value of β, and I_S is the transistor saturation current. At low current levels, the collector current I_C is

$$I_C = I_S \exp\frac{V_{BE}}{V_T} \tag{2.13}$$

The base current I_B is

$$I_B \propto I_S \exp\frac{V_{BE}}{2V_T} \tag{2.14}$$

I_B is proportional to $\exp(V_{BE}/2V_T)$ due to the space charge recombination current and/or surface recombination current [1]. At high current level, I_B follows the same behavior given in 2.11. But β decreases because I_C decreases. I_C decreases because of a high injection level. The collector current I_C becomes

$$I_C \approx I_{SH} \exp\frac{V_{BE}}{2V_T} \tag{2.15}$$

At a high current level, β also decreases because of the Kirk effect. This effect occurs when the minority carrier concentration in the collector region becomes comparable to the donor-atom doping density [3, 4].

The value for β increases as temperature increases. The emitter region is highly doped which causes the emitter junction efficiency, γ, to increase with temperature [3, 5]. A typical β versus I_C plot is shown in Figure 2.6.

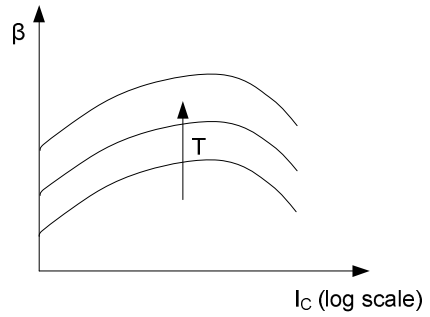


Figure 2.6 Typical β versus I_C plot for a BJT

2.5 Transition Frequency, f_T

The small signal equivalent circuit for the BJT transistor is shown in Figure 2.7.

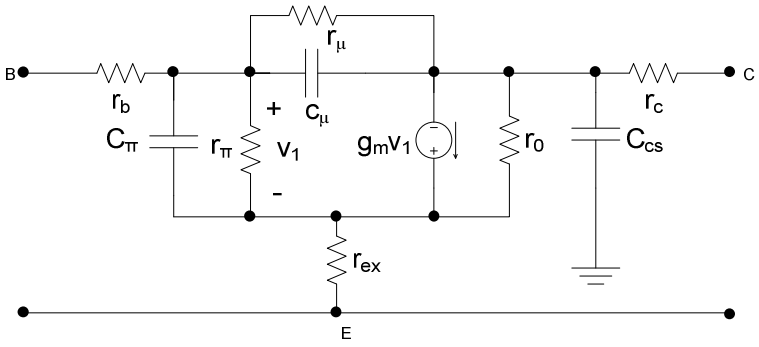


Figure 2.7 Small signal equivalent circuit for a BJT

The capacitive elements in the transistor equivalent circuit control the high frequency gain. The frequency where the magnitude of the short circuit common emitter current gain falls to unity is called the transition frequency or f_T. This is the maximum frequency where the transistor can be used as an amplifier [3].

The value of f_T can be found by using the small signal equivalent circuit of the transistor. A small signal current i_{in} is applied to the base and i_0 is found when the collector is grounded. Since r_μ is very large and the r_{ex} value is small, r_μ and r_{ex} can be neglected. The resultant circuit is shown in Figure 2.8.

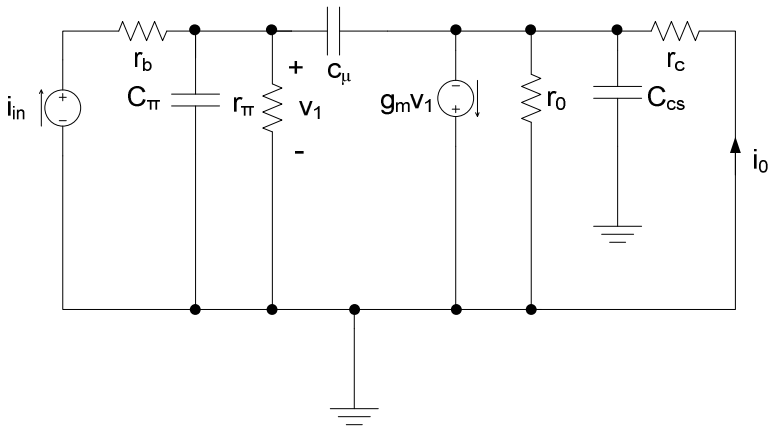


Figure 2.8 Small signal equivalent circuit of BJT for calculating f_T

If r_c is very small, then

$$v_1 \approx \frac{r_\pi}{1 + r_\pi\left(C_\pi + C_\mu\right)s} i_{in} \tag{2.16}$$

Here the current through C_μ is negligible.

$$i_0 = g_m v_1 \tag{2.17}$$

From equation (2.16) and (2.17),

$$i_0 \approx \frac{g_m r_\pi}{1 + r_\pi\left(C_\pi + C_\mu\right)s} i_{in} \tag{2.18}$$

Using $\beta_0 = g_m r_\pi$, equation (2.18) becomes

$$i_0 = \frac{\beta_0}{1 + \dfrac{\beta_0\left(C_\pi + C_\mu\right)s}{g_m}} i_{in} \tag{2.19}$$

Small signal high frequency current gain can be written as

$$\beta(j\omega) = \frac{i_0}{i_{in}} \tag{2.20}$$

So equation (2.19) becomes

$$\beta(j\omega) = \frac{\beta_0}{1 + \frac{\beta_0(C_\pi + C_\mu)j\omega}{g_m}} \tag{2.21}$$

But at high frequency, the imaginary part dominates. So

$$\beta(j\omega) \approx \frac{g_m}{(C_\pi + C_\mu)j\omega} \tag{2.22}$$

The transition frequency, f_T, can be found when $|\beta(j\omega)|=1$. Thus

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)} \tag{2.23}$$

and

$$\tau_T = \frac{1}{2\pi f_T} \tag{2.24}$$

From equations (2.23) and (2.24)

$$\tau_T = \frac{C_\pi}{g_m} + \frac{C_\mu}{g_m} \tag{2.25}$$

The base emitter capacitance is given by

$$C_\pi = C_b + C_{je} \tag{2.26}$$

where C_b = the base-charging capacitance and C_{je} = the emitter base depletion layer capacitance. Thus equation (2.25) becomes

$$\tau_T = \frac{C_b}{g_m} + \frac{C_{je}}{g_m} + \frac{C_\mu}{g_m} \tag{2.27}$$

The base transit time is

$$\tau_T = \frac{C_b}{g_m} \tag{2.28}$$

Equation (2.27) becomes

$$\tau_T = \tau_F + \frac{C_{je}}{g_m} + \frac{C_\mu}{g_m} \tag{2.29}$$

So that f_T is dependent on g_m. Since g_m depends on I_C, f_T depends on I_C. At low values of I_C, C_{je} and C_μ dominate and f_T falls as I_C decreases. At high frequencies f_T decreases because τ_F increases which is caused by high-level injection and Kirk effect [3]. A typical f_T curve for a bipolar junction transistor is shown in Figure 2.9.

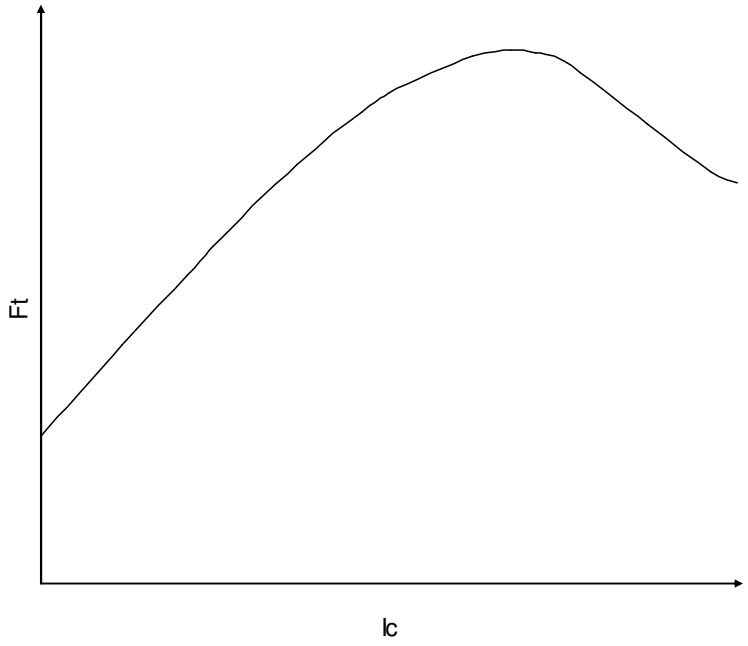
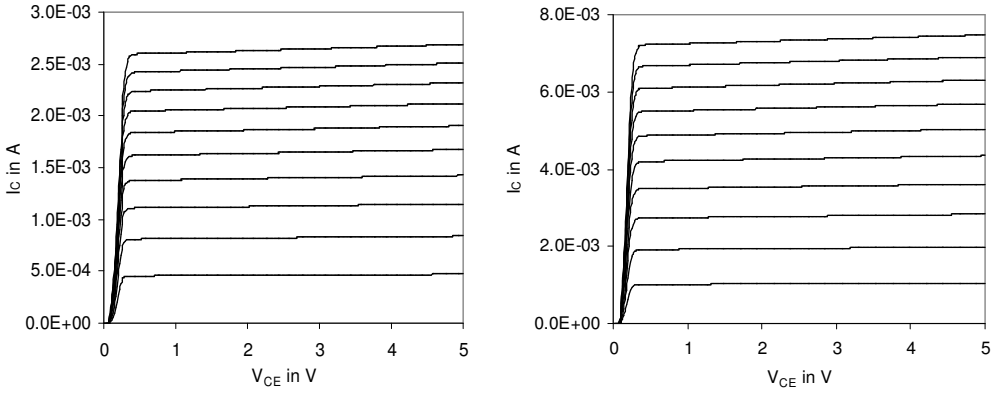


Figure 2.9 f_T versus I_C for BJT

2.6 Simulation Results

The NPN and PNP transistor model parameters used in this analysis are given in Appendix A. All transistors need to be biased in the forward active region. Transistors also need to be biased in the region where f_T is high and the β value is almost constant if I_C changes.

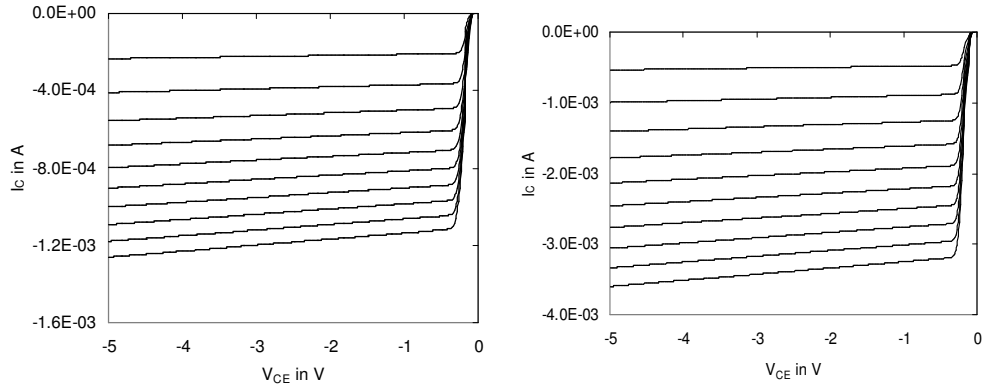
The I_C versus V_{CE} plots for an NPN transistor is shown in Figure 2.10. The I_C versus V_{CE} plots for the PNP transistor is shown in Figure 2.11. For single transistor, I_B changes from 5 uA to 50 uA and for 6 transistors in parallel, I_B changes from 10 uA to 100 uA for both NPN and PNP transistor.



(a) (b)

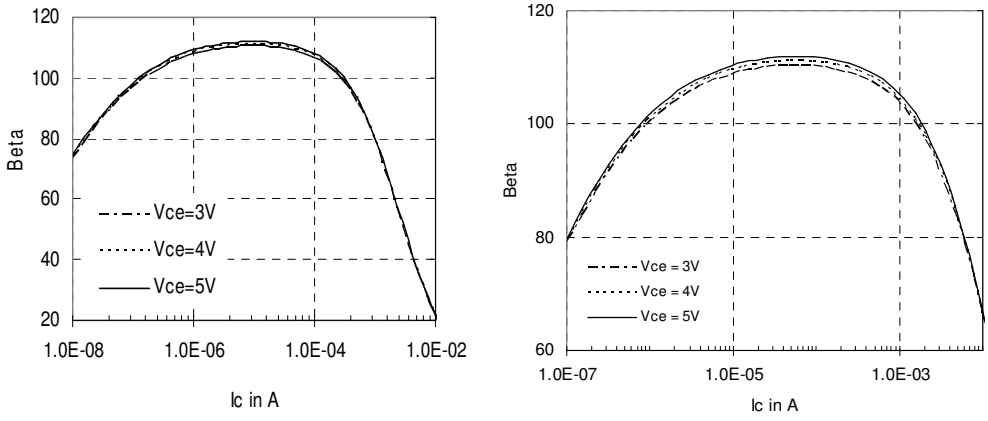
Figure 2.10 NPN transistor I_C versus V_{CE} (a) single transistor (b) 6 transistors in parallel

NPN and PNP transistor β versus I_C are shown in Figure 2.12 and Figure 2.13. Here the collector-emitter voltage changes from 3V to 5V.



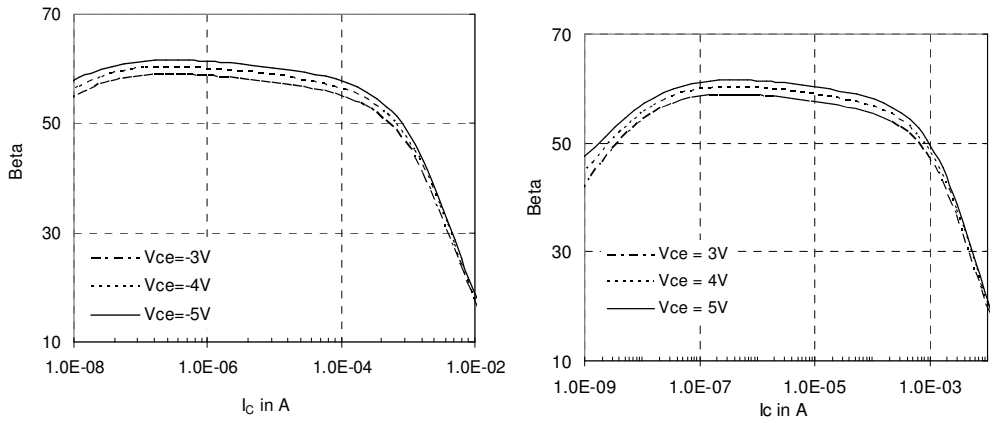
(a) (b)

Figure 2.11 PNP transistor I_C versus V_{CE} (a) single transistor (b) 6 transistors in parallel



(a) (b)

Figure 2.12 NPN transistor β versus I_C (a) single transistor (b) 6 transistors in parallel



(a) (b)

Figure 2.13 PNP transistor β versus I_C (a) single transistor (b) 6 transistors in parallel

The NPN and PNP transistor β versus I_C variation with changing temperature are shown in Figure 2.14 and Figure 2.15. Here temperature changes from -60°C to 120°C with 30ºC increment and collector-emitter voltage is 3V.

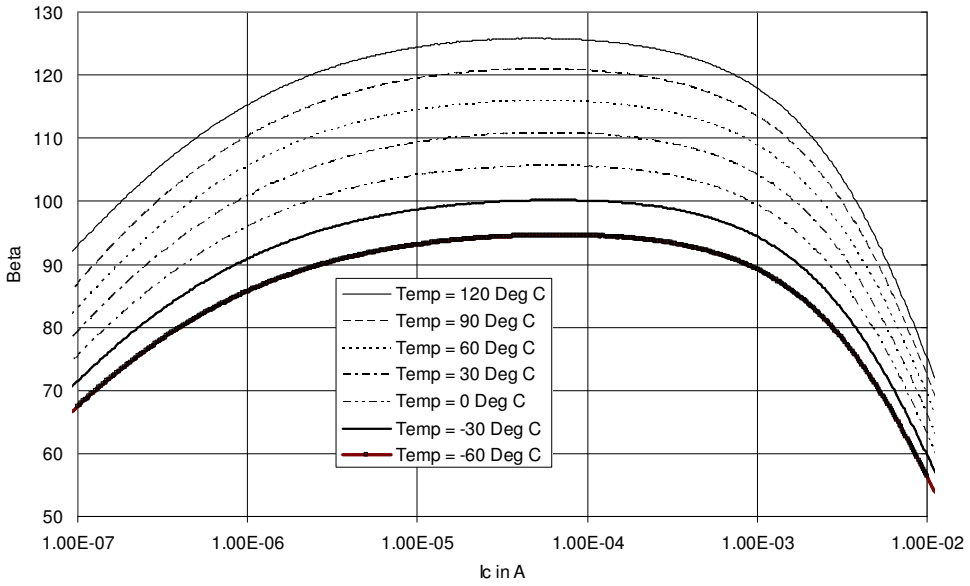


Figure 2.14 NPN transistor β versus I_C with temperature for 6 transistors in parallel

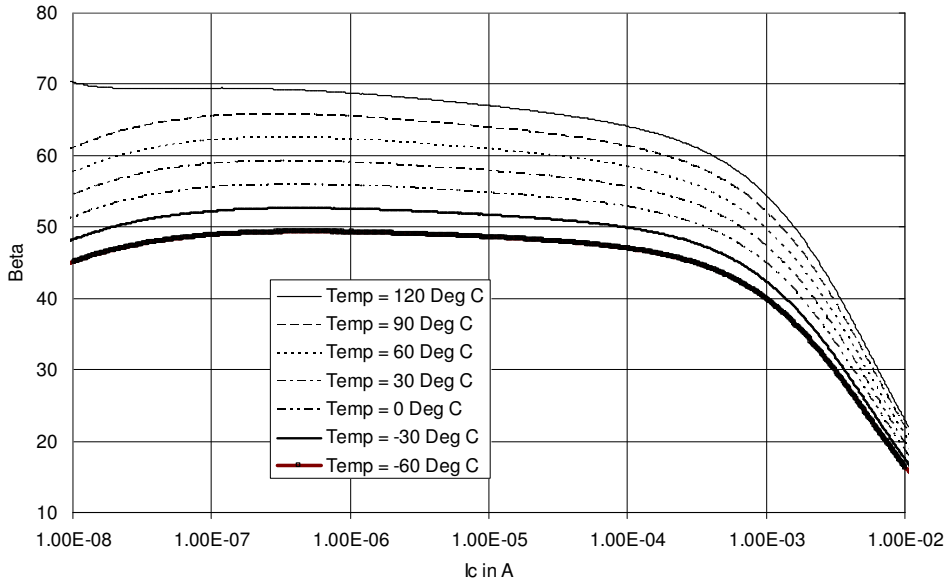


Figure 2.15 PNP transistor β versus I_C with temperature for 6 transistors in parallel

The NPN and PNP transistor f_T versus I_C are shown in Figure 2.16 and Figure 2.17.

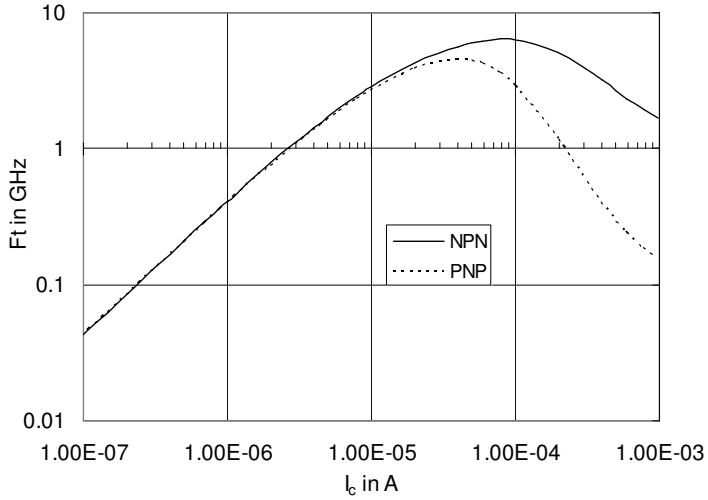


Figure 2.16 f_T versus I_C for single transistor

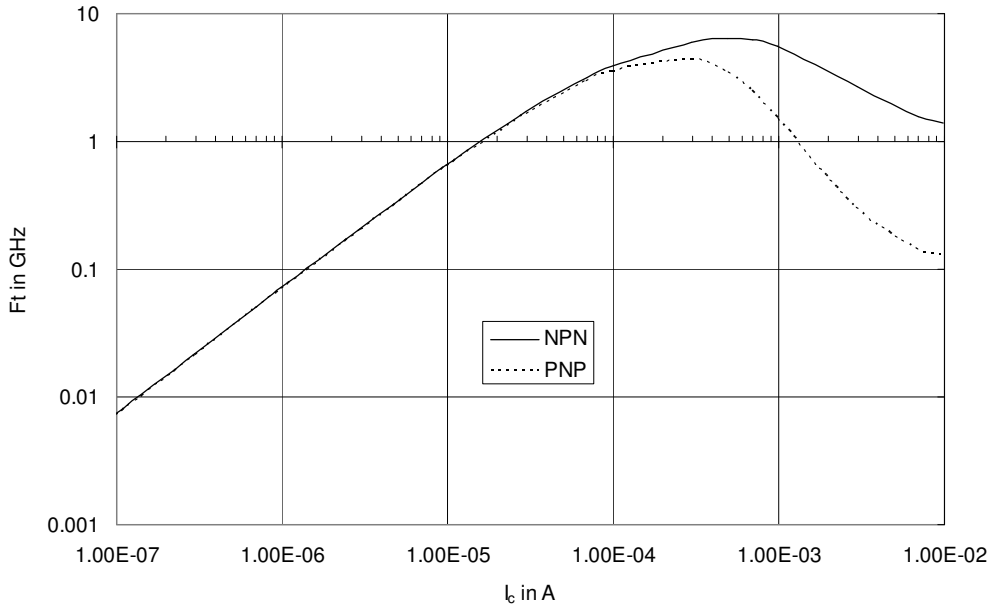


Figure 2.17 f_T versus I_C for 6 transistors in parallel

2.7 Summary

The modes of operation for a bipolar junction transistor were discussed in this chapter. All transistors need to be biased in the forward active region. The I_C versus V_{CE} characteristics of a BJT were discussed and simulated for NPN and PNP transistors. The various regions of a transistor current gain, β, were discussed in this chapter in detail. The analytical expression for f_T was developed. From the SPICE model, the simulation response for β and f_T for NPN and PNP transistors were given. The simulation was done using the Cadence Spectra simulator. The simulation result of the NPN and PNP transistors current gain, β, versus I_C with changing temperature were also given.

CHAPTER 3

THE CURRENT FEEDBACK OPERATIONAL AMPLIFIER

The operational amplifier was originally designed to perform mathematical operations by using voltage as an analogue of another quantity [6]. Op-amps were originally developed in the vacuum tube [7] era. At that time they consumed lots of space and energy. Later operational amplifiers were made smaller by implementing discrete transistors. Now they are implemented as monolithic integrated circuits (ICs). These are highly efficient and cost effective. In the late 1960s, the first integrated op-amp became widely available, which was created by Bob Widlar [8]. It was rapidly superseded by the 741.

Op-amp circuits are the basis for the electronic analog computer. They do basic mathematical operations such as addition, subtraction, integration, differentiation, and so on. Today an operational amplifier is a versatile circuit element with many applications. Op-amps usually have parameters within tightly specified limits, with standardized packaging and power supply requirements. With only a few external components, op-amp circuits can perform a wide variety of analog signal processing tasks.

Analog Design has historically been dominated by voltage mode signal processing [9]. Voltage feedback amplifier architecture has several attractive features.

These are the differential long-tail pair, high-impedance input stage, which is very good at rejecting common mode signals [10]. However the voltage feedback amplifier has some limitations. The gain bandwidth product is a constant and slew rate is low compared to the current feedback operational amplifier. Slew rate is limited to a maximum value which is determined by the ratio of the input stage bias current to the dominant pole compensation capacitor [11].

Recently, the current feedback operational amplifier has become more popular and is widely being used in the electronics and telecommunications industries. It offers some very good features over the voltage feedback operation amplifier. The two great features in the CFOA are slew rate and bandwidth. Although the CFOA is better than the VFOA in slew rate and bandwidth, the CFOA has some disadvantages. These are the input offset voltage (V_{OS}), input offset current (I_{OS}), common mode input range (CMIR), common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and open loop gain. VFOAs are generally used for precision and general purpose applications. CFOAs are used in high frequency applications especially over 100MHz.

3.1 Applications for Current Feedback Operational Amplifiers

There are lots of applications for the CFOA circuit. Included in them are arbitrary waveform driver, high-resolution and high-sampling rate analog to digital converter (ADC) drivers, high-resolution and high-sampling rate digital to analog converter (DAC) output buffers, IF amplification for wireless communications applications, broadcast video and HDTV line drivers, PC and workstation video boards, facsimile and imaging systems, DSL line driver, medical imaging, high-resolution

video, high speed signal processing, pulse amplifiers, ADC/DAC gain amplifiers, monitor preamplifiers, low cost precision IF amplifiers, and active filters [12 – 16] .

3.2 Advantages and Disadvantages of the Current Feedback Operational Amplifier

The advantages of the current feedback operational amplifier over the voltage feedback operational amplifier are

- Slew rate (SR) – slew rate for CFOA is high compared to VFOA.
- Bandwidth – bandwidth for CFOA is high compared to VFOA.

The disadvantages of current feedback operational amplifiers are

- Input offset voltage (V_{OS}) - V_{OS} for a CFOA is high compared to a VFOA.
- Input offset current (I_{OS}) - I_{OS} for a CFOA is high compared to a VFOA.
- Common mode input range (CMIR) - CMIR for a CFOA is low compared to a VFOA.
- Common mode rejection ratio (CMRR) - CMRR for a CFOA is low compared to a VFOA.
- Power supply rejection ratio (PSRR) - PSRR for a CFOA is low compared to a VFOA.
- Open loop gain - open loop gain for a CFOA is low compared to a VFOA.

Typical value of those parameters for the VFOA (LM741) [17] and the CFOA (LT1497) [18] is given in Table 3.1. These values are determined at T = 27°C and V_{CC} = V_{EE} = 15 V.

Table 3.1 Typical Parameter Values for the VFOA and the CFOA

Parameters	LM741	LT1497	Unit
V_{OS}	±1.0	±3	mV
I_{OS}	±20n	±7μ	A
CMIR	±13		V
CMRR	90	62	dB
PSRR	96	76	dB
SR	0.5	900	V/μS

3.3 Input Offset Voltage

The input offset voltage is defined as the input voltage needed to set the output voltage to zero.

$$V_{os} = V_{id}\Big|_{V_0=0} \tag{3.1}$$

Input offset voltages for the CFOA are generally worse than that of the voltage feedback operational amplifier. It suffers mismatch and Early voltage effects much more in the CFOA than that of the VFOA.

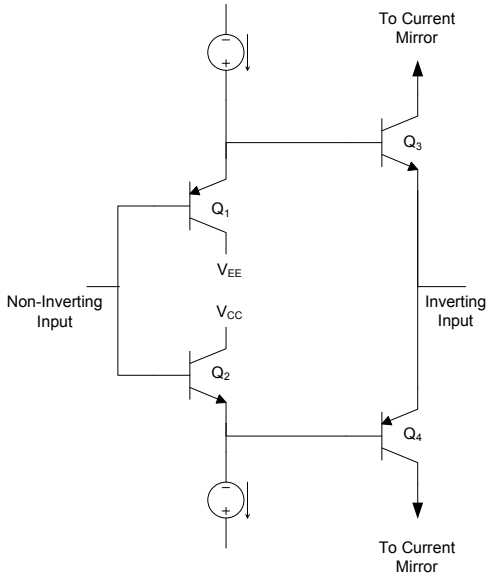


Figure 3.1 CFOA input stage

Figure 3.1 shows a simple CFOA input stage. This CFOA has very high noninverting input impedance and low inverting input impedance. Also the offset voltage is very high. It depends on the V_{BE} mismatches between the NPN and PNP transistors. It is possible to control V_{BE} matching between the NPN and PNP transistors in a bipolar process [19], but it is very difficult.

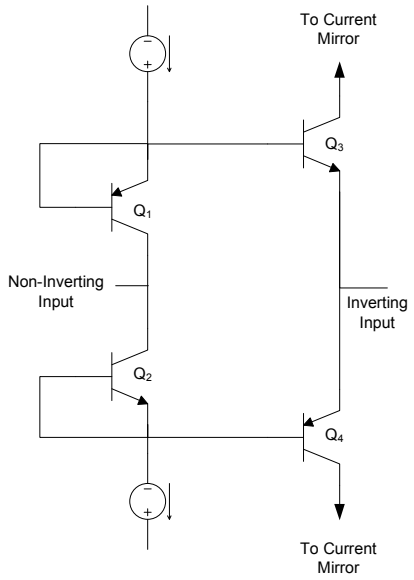


Figure 3.2 Another type CFOA input stage

Figure 3.2 shows the input stage of another type of CFOA. This input stage has two diodes and two transistors. It allows matching NPN transistors with NPN, and PNP transistors with PNP. Thus, the V_{OS} is relatively low. But V_{OS} is still not comparable to that of a VFOA. This is because of the mismatch caused by the Early voltage. This input stage has relatively low noninverting input impedances and a high noninverting

input bias current. This noninverting input current is a collector current. But in Figure 3.1, the noninverting input current is a base current.

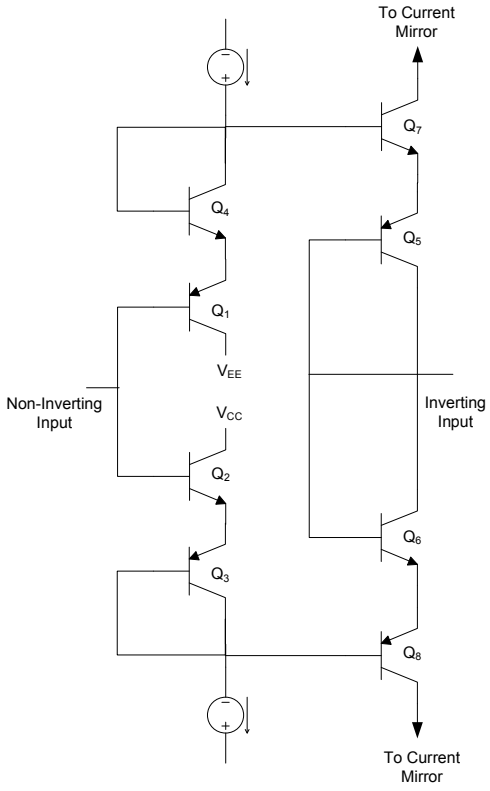


Figure 3.3 Eight transistor CFOA input stage

Another eight transistor input stage for the CFOA is shown in Figure 3.3. It has high non-inverting input impedance and low non-inverting input bias current. It matches transistor types, i.e. NPN with NPN, and PNP with PNP. But this input stage still suffers from mismatches in the Early voltage. Analyzing the lower part of the circuit,

$$V_{OS} = V_{BEQ2} + V_{BEQ3} - V_{BEQ8} - V_{BEQ6} \tag{3.2}$$

NPN transistor pair Q_1, Q_6 and PNP transistor pair Q_3, Q_8 have different V_{CE} voltages. For this configuration, the common mode input range is low. The input stage

transistors can be cascoded to improve V_{OS}, but this can result in common mode input range limitations [20].

3.4 Input Bias Current

The input bias current is defined as the current drawn from the positive and negative inputs terminals to bias the input stage of the amplifier.

$$I_B = \frac{I_p + I_n}{2} \tag{3.3}$$

The input bias currents are well matched in the VFOA. But in the CFOA, the input bias currents are not matched. The inverting input bias current is a result of a mismatch between the upper and lower current mirrors. This current difference flows directly out of the inverting input terminals. The non-inverting and inverting input bias currents are uncorrelated.

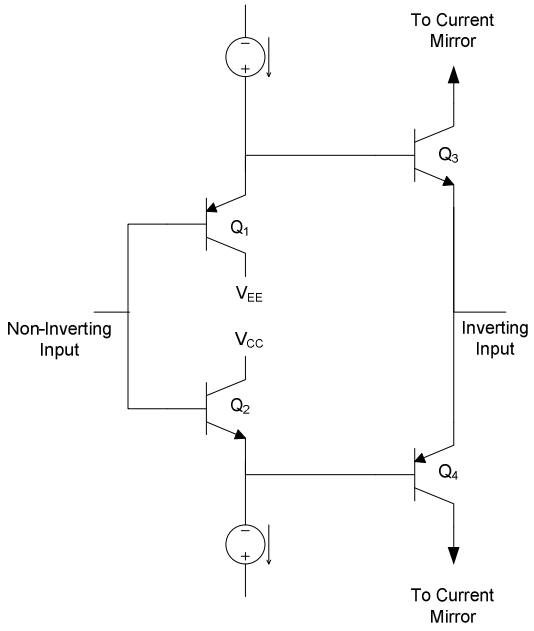


Figure 3.4 CFOA input stage for input bias current

3.5 Common Mode Input Range

The common mode input range (CMIR) is defined as the input common mode voltages for which the amplifier operates properly. For most operational amplifiers, CMIR is specified with

$$-V_{EE} + \Delta V_{EE} \le V_{ic}(CMIR) \le V_{cc} - \Delta V_{cc} \tag{3.4}$$

The common mode input range for the CFOA is worse than that of the VFOA. In the VFOA, CMIR can be rail-to-rail, i.e. from V_{CC} to V_{EE}. The best CFOA CMIR can be within two diodes of either supply voltages. Cascoding the input stage for improving V_{OS} generally makes CMIR worse.

The circuit diagram for finding CMIR is shown in Figure 3.5. Here all resistance values are the same. V_0 is plotted as a function of V_{in}. At a certain value of V_{in}, V_0 reaches either the positive or negative rail. So the CMIR is between $\pm$½V_{in}.

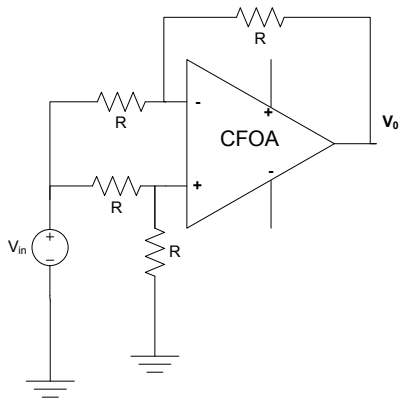


Figure 3.5 CMIR simulation circuit

3.6 Output Voltage Swing

Output voltage swing is the maximum output voltage for which the output voltage is undistorted.

$$V_{o(\min)} \le V_o \le V_{o(\max)} \tag{3.5}$$

Where $V_{o(max)}$ and $V_{o(min)}$ are the output voltages just before reaching a predetermined level of distortion. The output voltage swing for the CFOA can be found from the CFOA V_0 versus I_{in} curve. A typical V_0 versus I_{in} curve for the CFOA is shown in figure 3.6.

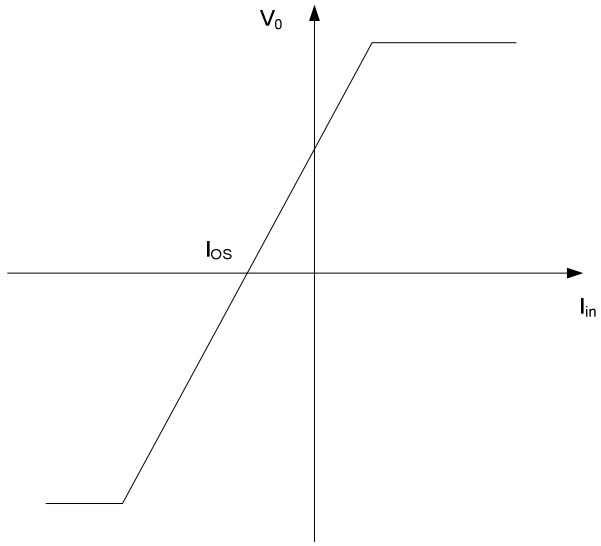


Figure 3.6 Typical V_0 versus I_{in} curve for the CFOA

3.7 Output Short Circuit Current

Output short circuit current is the amount of output current that the amplifier can source or sink when the output is grounded.

$$I_{o(\min)} \le I_o \le I_{0(\max)} \tag{3.6}$$

Where $I_{o(min)}$ is the maximum sinking current and the $I_{o(max)}$ is the maximum sourcing current.

3.8 Power Dissipation

Power dissipation is the amount of power consumed by the amplifier during stand-by operation.

$$P_{diss} = V_{CC} I_{CC} + V_{EE} I_{EE} \tag{3.7}$$

Where V_{CC} is the positive power supply and V_{EE} is the negative power supply. I_{CC} is the current drawn from the positive power supply and I_{EE} is the current sink to the negative power supply.

3.9 Common Mode Rejection Ratio

The common mode rejection ratio (CMRR) is a measure of how well the amplifier can reject common mode input signals from the output voltage. For the VFOA, CMRR is generally good and over 100 dB. If the change in the input bias current is small, then the CMRR is defined by

$$CMRR = \frac{A_{dm}}{A_{cm}} \tag{3.8}$$

Where A_{dm} is the differential mode gain and A_{cm} is the common mode gain. From equation (3.8), CMRR is derived

$$CMRR = \left(\frac{\Delta V_{os}}{\Delta V_{cm}} \right)^{-1} \tag{3.9}$$

Input stages have almost identical voltages across both input devices. CMRR is caused by the mismatches in the input devices.

CMRR for the CFOA is worse than that of the VFOA. The input stage of the CFOA is the main factor determining the CMRR performance. The output impedance of the input stage is one of the reasons for lower CMRR [21]. The change in noninverting input current, I_{bn}, and inverting input current, I_{bi}, is not small and they are uncorrelated. Early voltage errors are modulated directly by the change of common mode voltage.

CMRR for the CFOA can be increased by bootstrapping the entire input stage which is described in [22]. The conventional CFOA can be described as a core current conveyor, type CCII+, with the Z-node connected to the output voltage buffer.

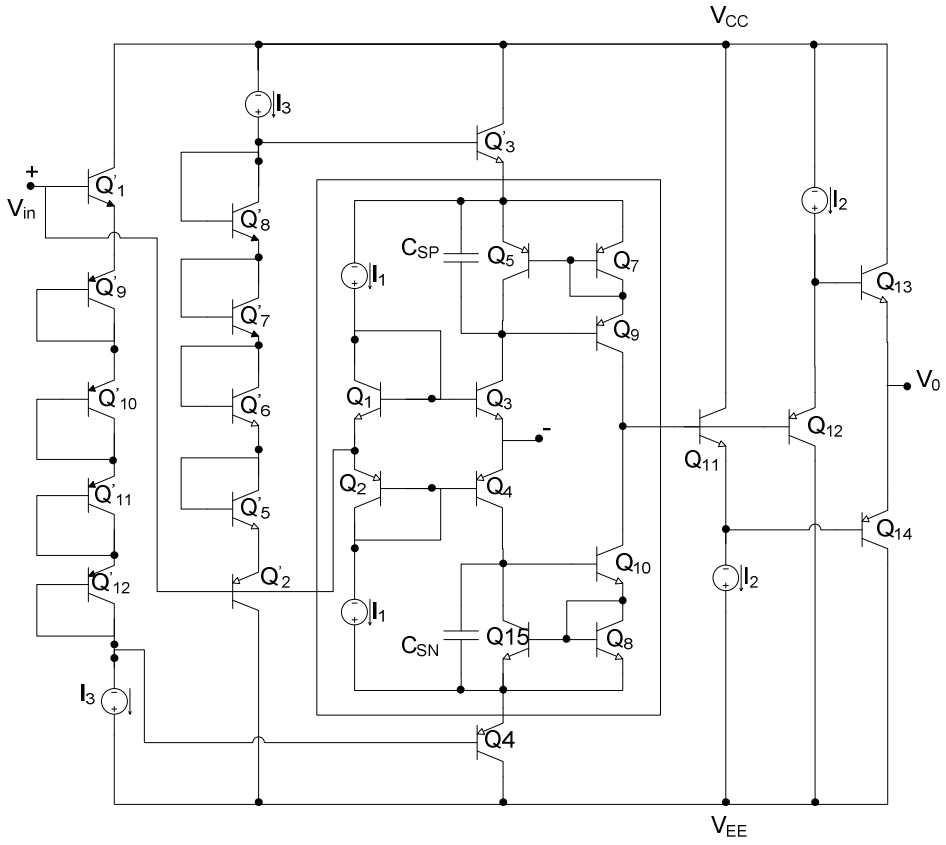


Figure 3.7 High CMRR current-feedback operational amplifier

Here the input transistor pair Q_1/Q_3 and Q_2/Q_4 are NPN and PNP respectively. So the matching between Q_1 and Q_3 and Q_2 and Q_4 are better than that of a conventional CFOA. The composite voltage followers Q_1'/Q_4' and Q_2'/Q_3' apply the noninverting input voltage to the emitters of Q_5 and Q_6, effectively floating or bootstrapping the input stage. Diode connected transistors Q_5' to Q_{12}' provides appropriate dc biasing. The signal voltage difference between the collector and base of both Q_3 and Q_4 is almost equal to zero. So the influence of the Early voltage effect from Q_3 and Q_4 is almost entirely eliminated, yielding a significant improvement in both CMRR and PSRR. Also the input referred offset voltage is improved. A further improvement can be made by cascoding the two transistors Q_3 and Q_4. Cascoding Q_3 and Q_4 into Q_{3a}/Q_{3b} and Q_{4a}/Q_{4b} increases the effective r_{ce}. So there is an additional increase of CMRR. The Slew rates for those CFOAs are significantly lower. Generally a tradeoff exists between slew rate and CMRR in most CFOA circuits [23].

3.10 Power Supply Rejection Ratio

The power supply rejection ratio (PSRR) is defined as the product of the ratio of the change in supply voltage to the change in the output voltage of the op amp caused by the change in the power supply and the open loop gain of the op amp [24]. So

$$PSRR = \frac{\Delta V_{CC}}{\Delta V_0} A_V(s) = \frac{\left.\frac{V_0}{V_{in}}\right|_{V_{cc}=0}}{\left.\frac{V_0}{V_{cc}}\right|_{V_{in}=0}} \tag{3.10}$$

where V_{cc} is the small signal voltage in the positive power supply. Thus

$$PSRR = \frac{A_V\big|_{V\,cc=0}}{A_{cc}\big|_{V\,in=0}} \tag{3.11}$$

Where $A_V = V_0/V_{in}$ and $A_{cc} = V_0/V_{cc}$. PSRR can be found by calculating A_V and A_{cc} and combining the results. But it is easier to use the unity gain-configuration of an op amp to make this measurement. An ideal op amp has an infinite PSRR.

PSRR is a measure of how well the amplifier can reject any signal applied to the power supply terminals from the output voltage. PSRR is very good for a VFOA. If it is assumed the change in input bias current is small then PSRR is defined by

$$PSRR = \left(\frac{\Delta V_{os}}{\Delta V_{ps}}\right)^{-1} \tag{3.12}$$

Where V_{os} is the input offset voltage and V_{ps} is the power supply. PSRR are caused by the mismatches in the input devices.

PSRR is worse in the CFOA. The change in I_{bn} and I_{bi} is not small and they are uncorrelated. Early voltage errors are modulated directly by the change of supply voltage.

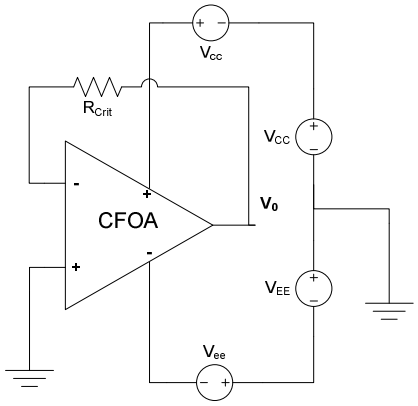


Figure 3.8 CFOA configured for simulation or measurement of PSRR

Figure 3.8 shows the circuit for direct simulation or measurement of PSRR as a function of frequency. Here a small sinusoidal voltage V_{cc} /V_{ee} is applied in series with the power supply V_{CC}/V_{EE} to measure or simulate $PSRR^{+}$/$PSRR^{-}$.

$$\frac{\Delta V_0}{V_{cc}} \cong \frac{1}{PSRR^{+}} \tag{3.13}$$

And

$$\frac{\Delta V_0}{V_{ee}} \cong \frac{1}{PSRR^{-}} \tag{3.14}$$

3.11 Proposed CFOA Schematic Diagram

The schematic diagram for a CFOA is shown in Figure 3.9. The schematic diagram shows the inverting input terminal, non-inverting input terminal, high Z terminal, and the output terminal.

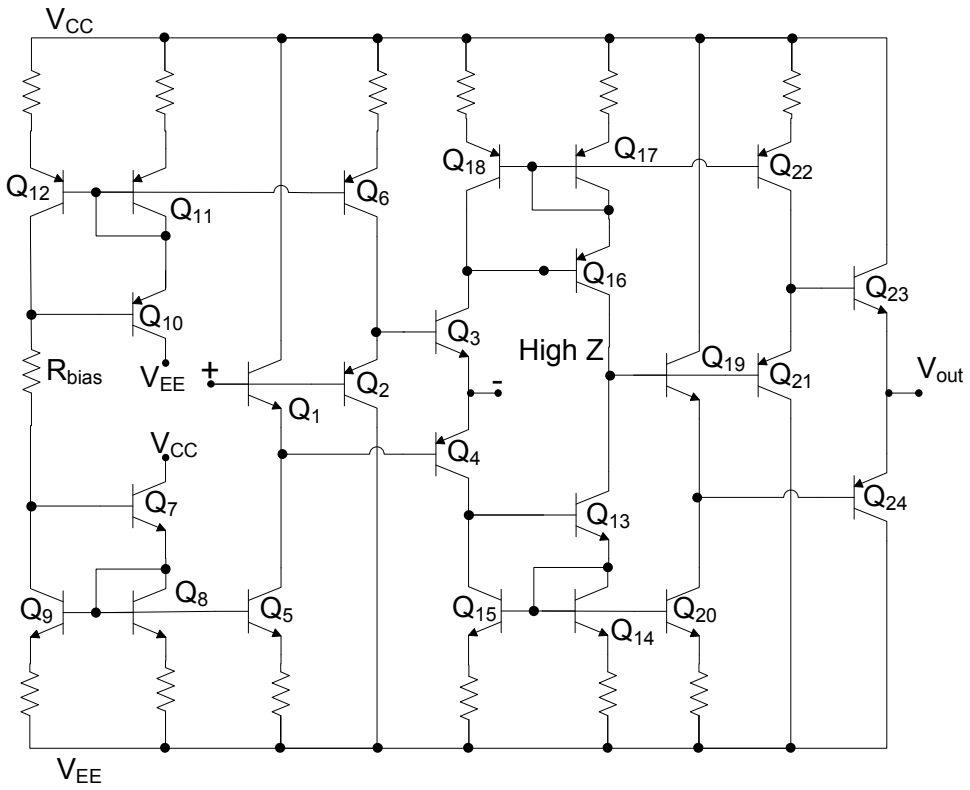


Figure 3.9 Complete schematic diagram of the CFOA

3.12 Simulation Results

The V_0 versus I_{in} curve for the CFOA is shown in Figure 3.10. The supply voltage is ± 5 V. Here the maximum output voltage swing is ± 3.85 V. The input offset current is -7.73 uA.

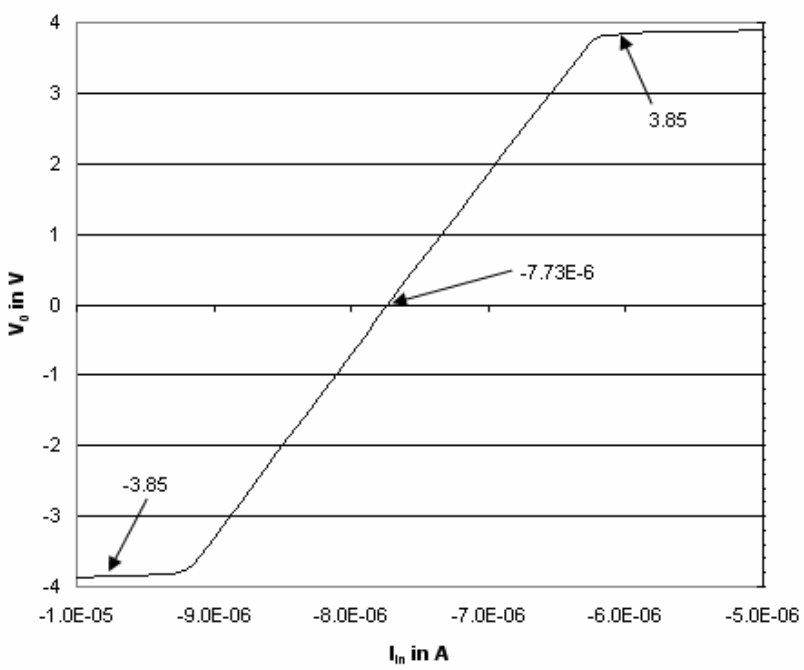


Figure 3.10 Current transfer curve

The input offset voltage is 24.87 mV.

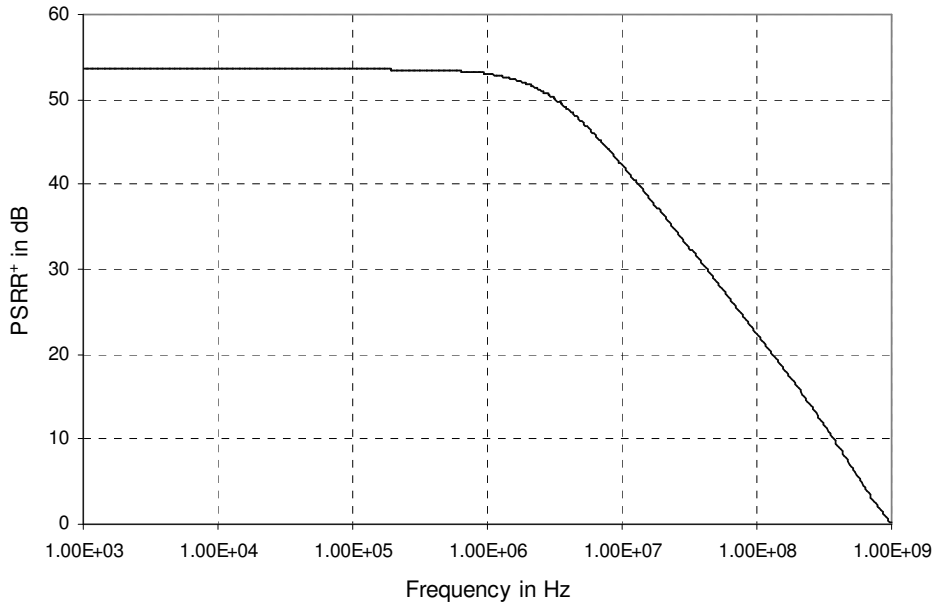


Figure 3.11 Positive PSRR

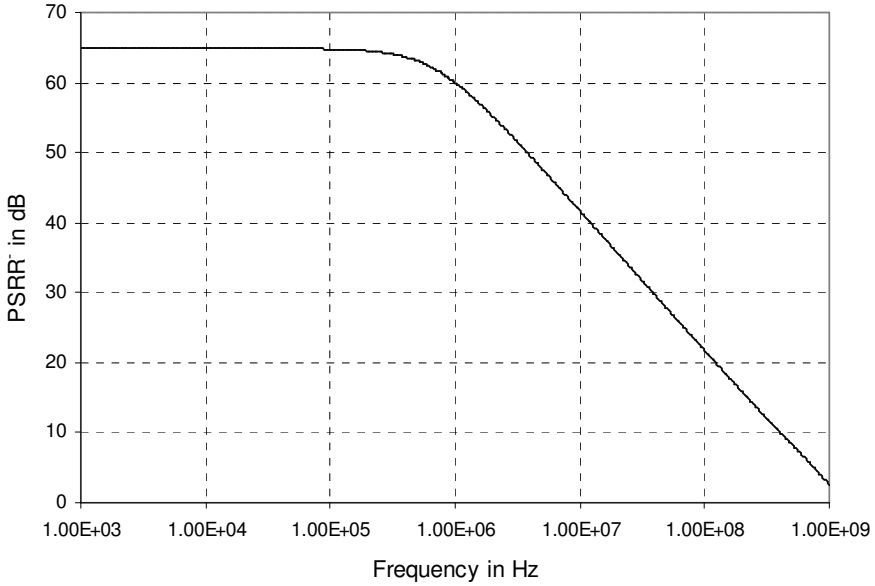


Figure 3.12 Negative PSRR

Figure 3.11 shows the positive PSRR and Figure 3.12 shows the negative PSRR for the CFOA. The positive PSRR is 53.54 dB and the negative PSRR is 64.87 dB. Here the feedback resistance used for the PSRR simulation is 1 kΩ.

Figure 3.13 shows the simulation result for the CMIR. The circuit used for the CMIR simulation is shown in Figure 3.5. Here the value for R is 2 kΩ. Thus, the positive CMIR is 3.065 V, and the negative CMIR is -3.12 V.

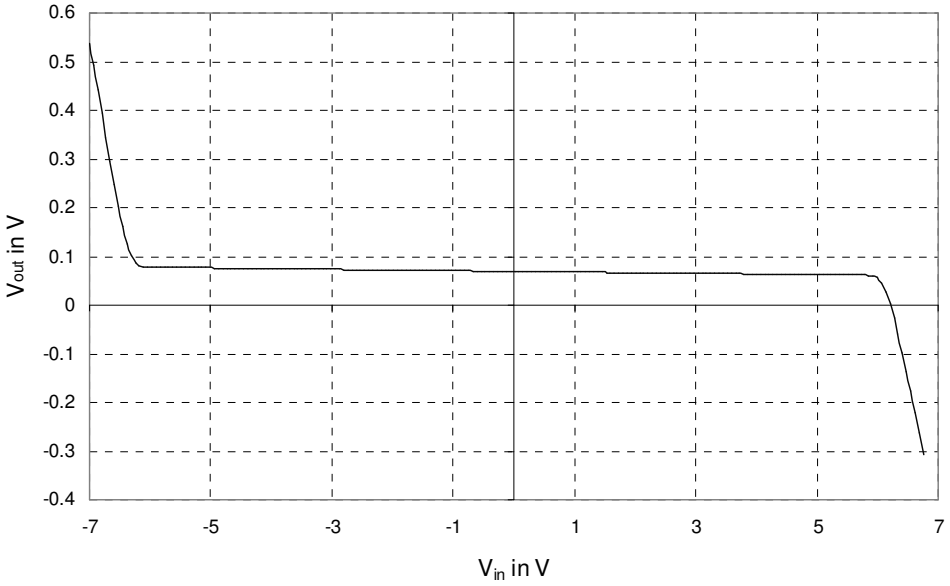


Figure 3.13 CMIR

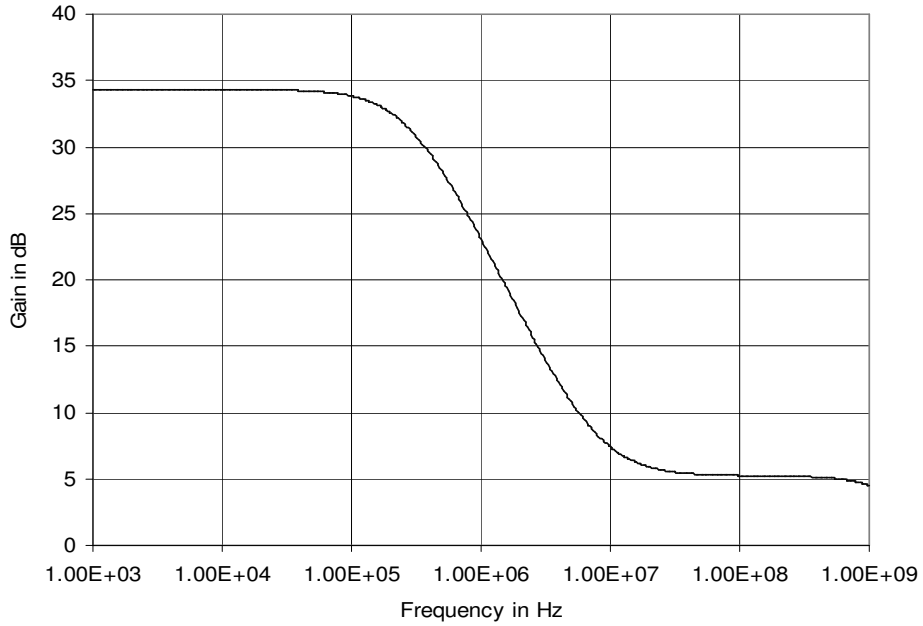


Figure 3.14 Common mode gain

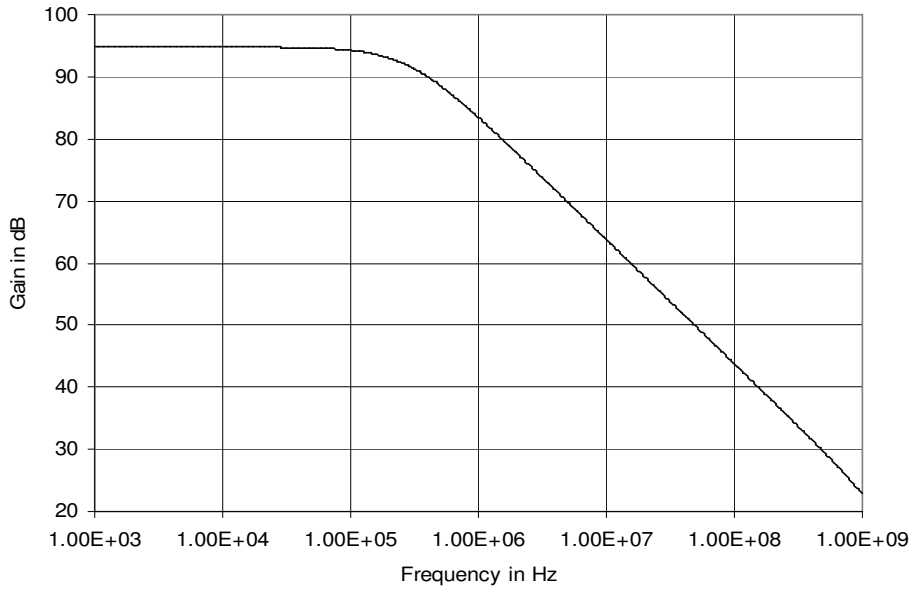


Figure 3.15 Differential mode gain

Figure 3.14 shows the simulation result for the common mode gain, and Figure 3.15 shows the simulation result for the differential mode gain. Here the common mode gain is 34.47 dB, and the differential mode gain is 94.92 dB. Thus, the CMRR is 60.45 dB.

3.13 Summary

CFOA DC parameters, such as input offset voltage (V_{OS}), input offset current (I_{OS}), common mode input range (CMIR), common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and maximum output voltage swing were shown to be dramatically different for the CFOA and VFOA. In simulation, the maximum output voltage swing for the CFOA was found ± 3.85 V, the input offset current was -7.73 uA, the input offset voltage was 24.87 mV, the positive PSRR was 53.54 dB, the

negative PSRR was 64.87 dB, the positive CMIR was 3.065 V, the negative CMIR was -3.12 V, and the CMRR was 60.45 dB.

CHAPTER 4

MACRO-MODEL FOR THE CURRENT FEEDBACK OPERATIONAL AMPLIFIER

The macro-model is a model that simulates the circuit operation that is close to the actual circuit without modeling every component of the circuit. Simulation of a large circuit with a macro-model is faster. The CFOA macro-model is used to make analytical predictions for a sine wave oscillator, and waveform generator. It is used to predict the frequency of oscillation for the waveforms. The techniques for finding the values of the macro-model parameters are discussed in the following sections.

4.1 CFOA Single Pole Macro-model

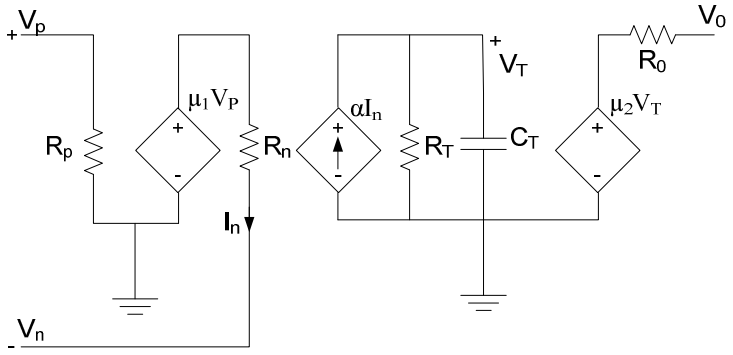


Figure 4.1 CFOA single pole macro-model

The CFOA single pole macro-model is shown in Figure 4.1 [25]. Here R_p is the input resistance for the non-inverting input terminal, R_n is the output load resistance of the input buffer, μ_1 is the coefficient for the input buffer, α is the coefficient for the

current mirror, R_T is the low frequency transimpedance, C_T is the internal capacitance for the transimpedance, R_0 is the output buffer output load resistance, and μ_2 is the coefficient for the output buffer. The typical range for the macro-model parameters are shown in Table 4.1 [25].

Table 4.1 Typical Range for Macro-model Parameter

R_p	100 KΩ to 1 MΩ
R_n	10 Ω to 100 Ω
R_0	5 Ω to 50 Ω
μ_1	≥ 1
μ_2	≤ 1
α	≤ 1
R_T	100 KΩ to 100 MΩ
$\omega_1 = \frac{1}{R_T C_T}$	10 KHz to 300 KHz

4.2 Macro-model Parameter Extraction

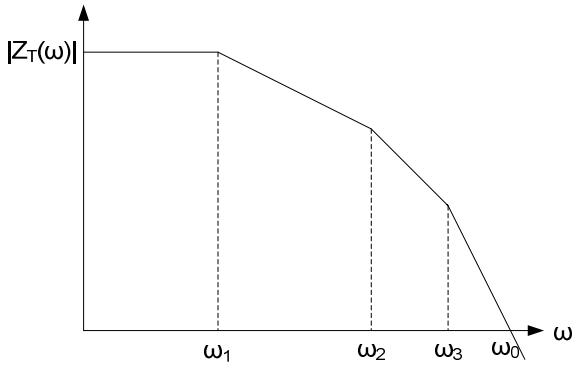


Figure 4.2 Typical open loop transimpedance for CFOA

Macro-model parameter R_T and C_T can be found from the open loop transimpedance plot. A typical open loop transimpedance plot is shown in Figure 4.2. Here R_T is the low frequency open loop transimpedance. C_T can be found from equation (4.1).

$$\omega_1 = \frac{1}{R_T C_T} \tag{4.1}$$

where ω_1 is -3dB angular frequency of the open loop transimpedance. From equation (4.1), C_T is

$$C_T = \frac{1}{\omega_1 R_T} \tag{4.2}$$

The macro-model resistance, R_0, can be found by connecting a load resistance, R_L, from the CFOA output to ground which is shown in Fig. 4.3(a) [24]. The voltage drop across R_L at a certain value of I_{in} can be used to calculate R_0. If no load is connected at the output terminal, the output voltage for the CFOA is V_{01}. From Figure 4.1,

$$V_{O1} = \mu_2 V_T \tag{4.3}$$

If load resistance R_L is connected to the output terminal then the output voltage is V_{02}. From Figure 4.1,

$$V_{O2} = \frac{R_L}{R_L + R_O} \mu_2 V_T \tag{4.4}$$

From equation (4.3) and (4.4),

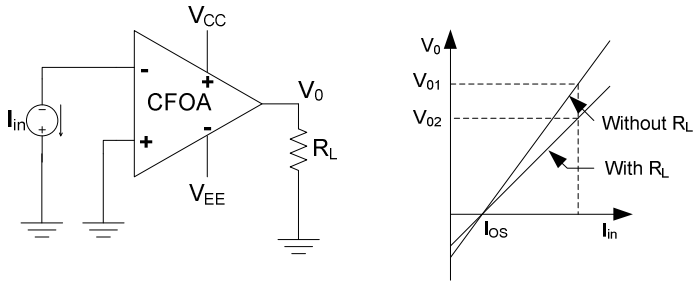
$$\frac{V_{O1}}{V_{O2}} = \left(1 + \frac{R_O}{R_L}\right) \tag{4.5}$$

Thus, R_O is

$$R_O = R_L \left(\frac{V_{O1}}{V_{O2}} - 1\right) \tag{4.6}$$

Here V_{01} is the output voltage without output resistance R_L and V_{02} is the output voltage with output resistance R_L for the same current input I_{in}.

Another way to find R_0 is to vary R_L until $V_{02}=V_{01}/2$. Under this condition, R_L is equal to R_{out}.



(a) (b)

Figure 4.3 (a) CFOA with load resistance R_L and (b) CFOA output voltage vs I_{in}

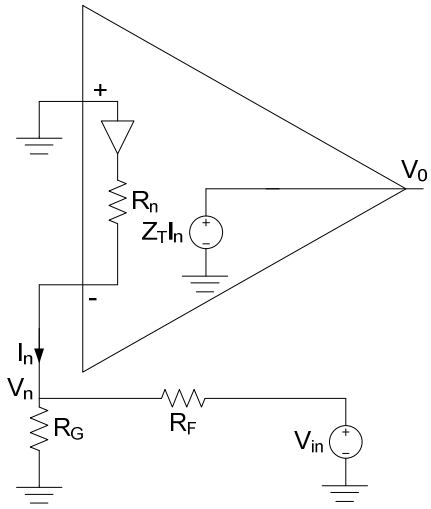


Figure 4.4 CFOA configured for finding macro-model resistance R_n

The macro-model resistance R_n can be found from Figure 4.4 [26]. Here

$$I_n = \frac{V_n}{R_G} + \frac{V_n - V_{in}}{R_F} \tag{4.7}$$

$$V_n = -I_n R_n \tag{4.8}$$

$$I_n = \frac{V_0}{Z_T} \tag{4.9}$$

where Z_T is the open loop transimpedance of the CFOA. From equations (4.7), (4.8), and (4.9)

$$\frac{V_0}{Z_T} + \frac{V_0 R_n}{Z_T R_G} + \frac{V_0 R_n}{Z_T R_F} + \frac{V_{in}}{R_F} = 0 \tag{4.10}$$

Let A_v be the voltage gain.

$$A_V = \frac{V_0}{V_{in}} \tag{4.11}$$

Equation (4.10) becomes

$$\frac{A_V}{Z_T} + \frac{A_V R_n}{Z_T R_G} + \frac{A_V R_n}{Z_T R_F} + \frac{1}{R_F} = 0 \tag{4.12}$$

$$\frac{A_V R_n}{Z_T}\left(\frac{R_F + R_G}{R_F R_G}\right) = \frac{-Z_T - A_V R_F}{R_F Z_T} \tag{4.13}$$

$$\mathrm{R_n} = \frac{-Z_T - A_V R_F}{\mathrm{A_V}\left(1 + \dfrac{\mathrm{R_F}}{\mathrm{R_G}}\right)} \tag{4.14}$$

4.3 Simulation Results for the Macro-model Parameter Extraction

Fig. 4.5 shows the open loop transimpedance for the full model CFOA. The low frequency transimpedance is 2.59 MΩ and the first pole is at the frequency of 280 KHz. Thus, R_T is 2.59 MΩ and C_T is 0.219 pF.

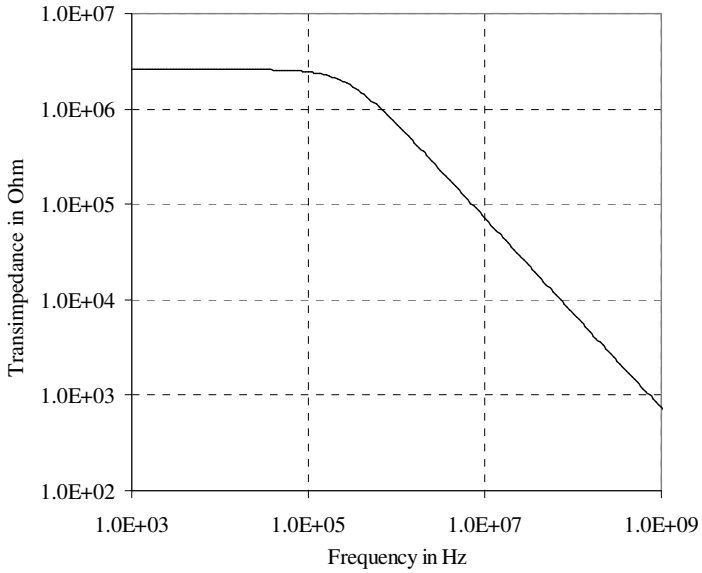


Figure 4.5 Open loop transimpedance for CFOA

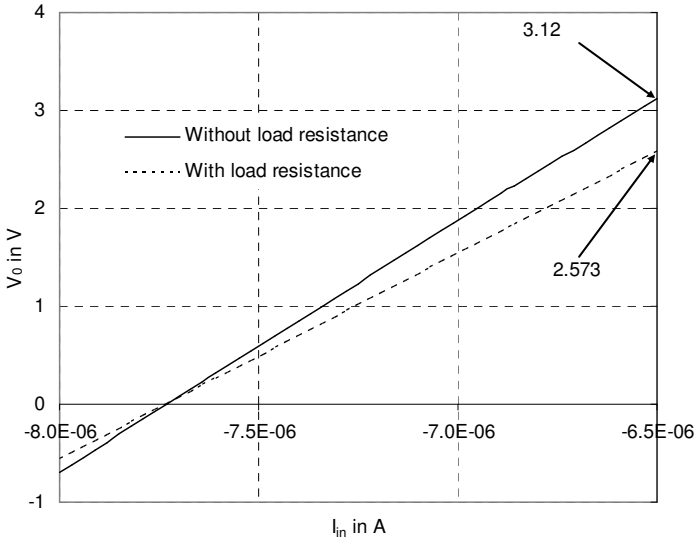


Figure 4.6 CFOA output voltage and without load resistance for changing I_{in}

Figure 4.6 shows the CFOA output with a load resistance of 2 kΩ and without load resistance as a function of I_{in}. When I_{in} = -6.5 uA, the output voltage is 3.12 V

when no load is connected, and 2.573 V when the 2 kΩ load is connected. So, the macro-model output resistance R_0 is 425 Ω.

Figure 4.7 shows the output voltage for the figure 4.4 configuration. Here the input voltage is 1 mV. The output voltage at low frequency is 1.24 V giving a gain of 1240. Here R_F and R_G are both 2 kΩ. Thus, using equation (4.4), R_n is 44.35 Ω.

The assumptions made in the macro-model are as follows

$\mu_1 = 1$

$\mu_2 = 1$

$\alpha = 1$

$R_p = \infty$

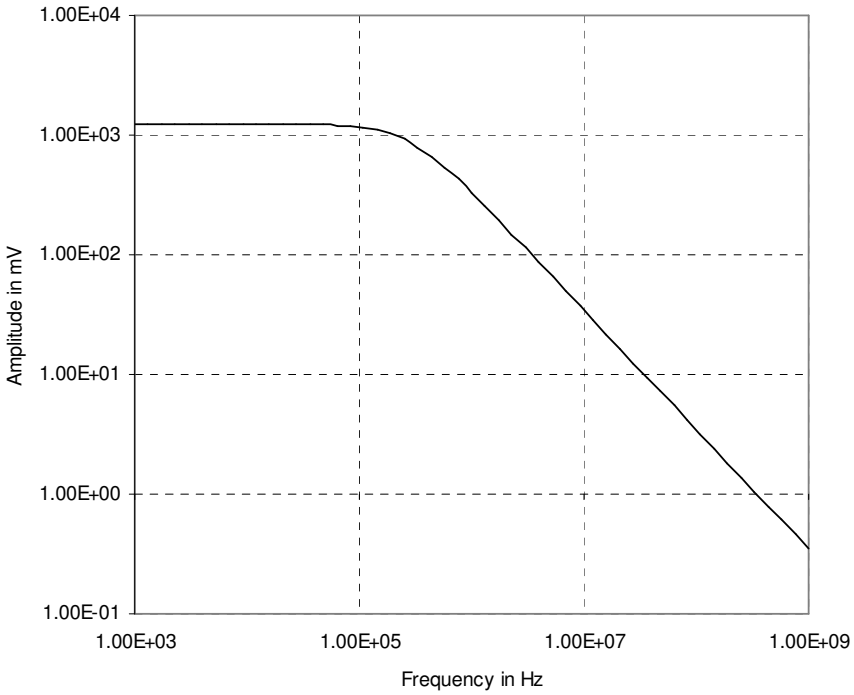


Figure 4.7 CFOA output voltage for the figure 4.4 configuration

4.4 CFOA Macro-model

The extracted CFOA macro-model is shown in Figure 4.8. Here V_P is the positive input terminal, V_n is the negative input terminal, and V_0 is the output terminal.

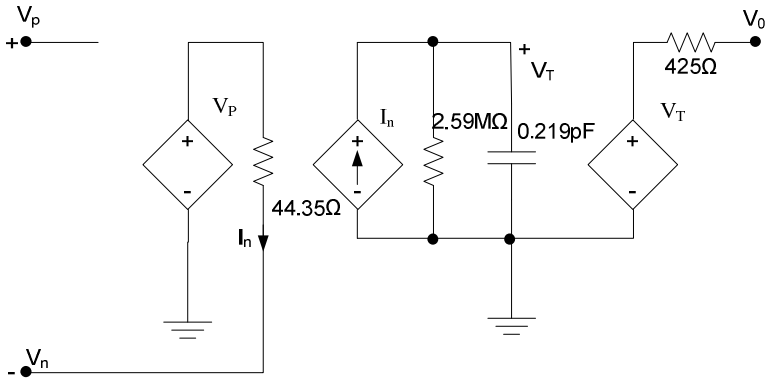


Figure 4.8 CFOA macro-model

4.5 Summary

The output resistance of the input buffer, R_n, was found to be 44.35 Ω. The output resistance of the output buffer, R_0, was found to be 425 Ω. The low frequency transimpedance, R_T, was found to be 2.59 MΩ, and the internal capacitance, C_T, was found to be 0.219 pF.

CHAPTER 5

SLEW RATE, BANDWIDTH, AND POWER DISSIPATION FOR CURRENT FEEDBACK AND VOLTAGE FEEDBACK OPERATIONAL AMPLIFIERS

5.1 Slew Rate

Slew-rate (SR) for an amplifier is defined by how quickly the output can track a step input, i.e. the maximum rate of change of output of an amplifier. Figure 5.1 shows an input waveform and its corresponding output waveform.

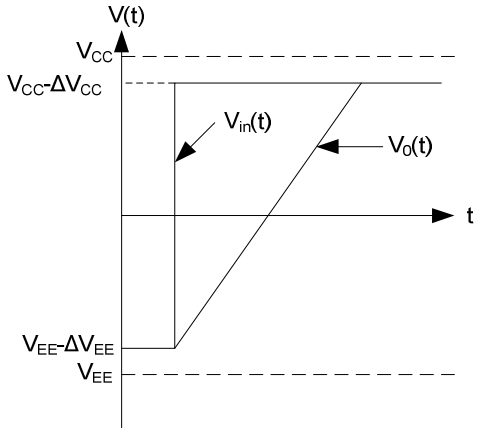


Figure 5.1 Input and output waveform for slew-rate calculation

So the slew-rate is

$$SR = \max\left(\left|\frac{dv_0(t)}{dt}\right|\right) \tag{5.1}$$

where $v_0(t)$ is the output produced by the amplifier as a function of time. The SR describes the degradation effect of an amplifier to the high frequency response at its

near maximum rated output voltage. The higher the value of the SR, the better the amplifier operates for high speed applications. The unit of SR is V/μSec.

The slew-rate for a CFOA is much higher than that of a VFOA. The slew-rate for the VFOA depends on the compensation capacitor and the tail current of the input differential pair. Thus the SR for the VFOA is [25]

$$SR \approx \frac{I_{EE}}{C_C^{'}} = \frac{I_{EE}}{C_C + C_{\mu 5}} \tag{5.2}$$

The VFOA circuit with tail current I_{EE} and compensation capacitor $C_C^{'}$ is shown in Figure 5.2.

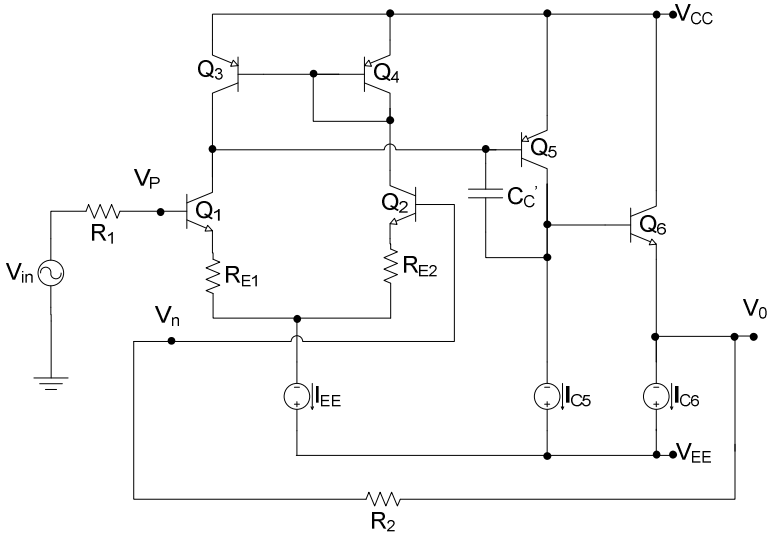


Figure 5.2 Simplified schematic diagram of a VFOA

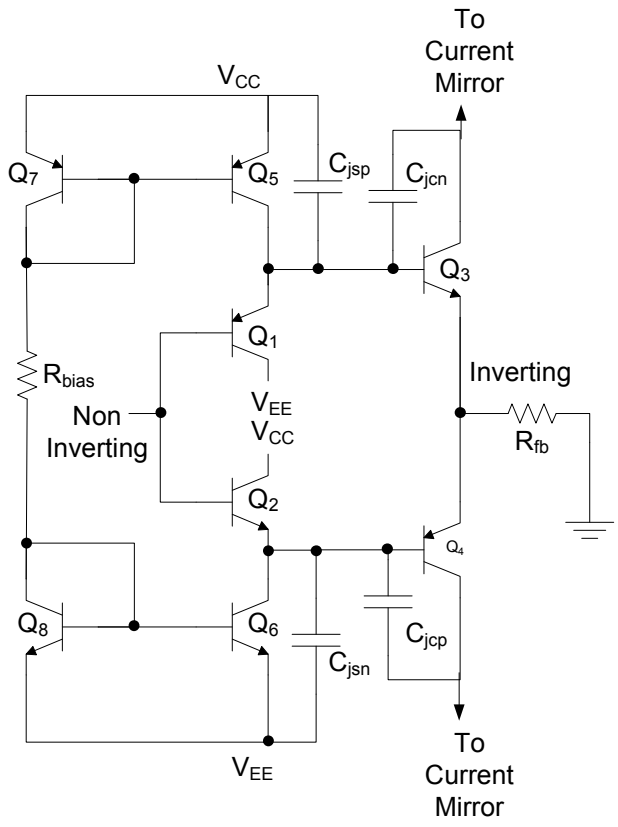


Figure 5.3 CFOA input stage

The slew-rate calculation is more complex for the CFOA. The input stage of the CFOA is shown in Figure 5.3. In [27], the author describes the SR for the CFOA. If a positive voltage is applied to the noninverting terminal of Figure 5.3 then the inverting terminal voltage also increases by the same magnitude. Transistor, Q_3 will source an error current into the R_{fb} resistor. This current is mirrored to the high impedance node which is shown in Figure 3.9. The voltage at the output node of Figure 3.9 is equal to the error current multiplied by the equivalent impedance of the high impedance node. The slew rate depends on the ability of Q_5 and Q_6 to charge or discharge the high impedance node internal capacitor. The slew rate is also limited by the parasitic

capacitance of the transistors. The base current demand of Q_3 and Q_4 worsens the problem. At the positive input step, Q_6 charges the transistor internal capacitance, C_{jsn}, and C_{jcp}. At the negative input step, Q_5 charges the transistor internal capacitance, C_{jsp}, and C_{jcn}.

A current booster circuit can be used to reduce the effect of the parasitic capacitor. Figure 5.4 shows the current booster circuit for improved slew rate.

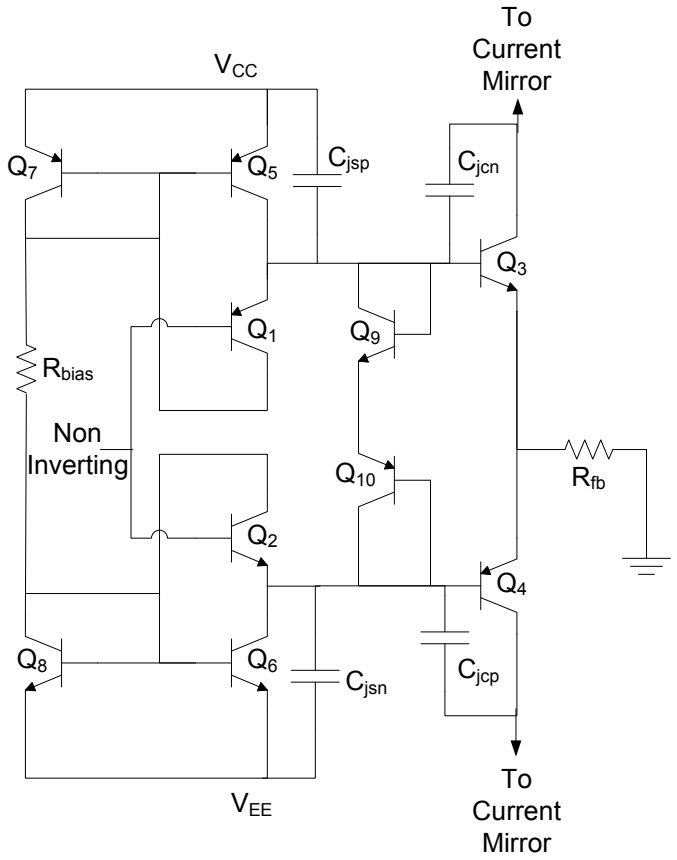


Figure 5.4 Current booster circuit for improved slew rate

For the positive input voltage, Q_1 begins to slew due to the transistor internal capacitance, C_{jsp}, and C_{jcn}. Q_2 sources more current to charge the transistor internal

capacitance, C_{jsn}, and C_{jcp}. This extra current is recirculated through Q_7, which increases the bias current for Q_1. Similarly, for the negative input voltage, Q_1 sinks more current to charge the transistor internal capacitance, C_{jsp}, and C_{jcn}, which is recirculated through Q_8 and increases the bias current for Q_2. Thus it increases the slew rate. The double buffer current booster CFOA is shown in Figure 5.5.

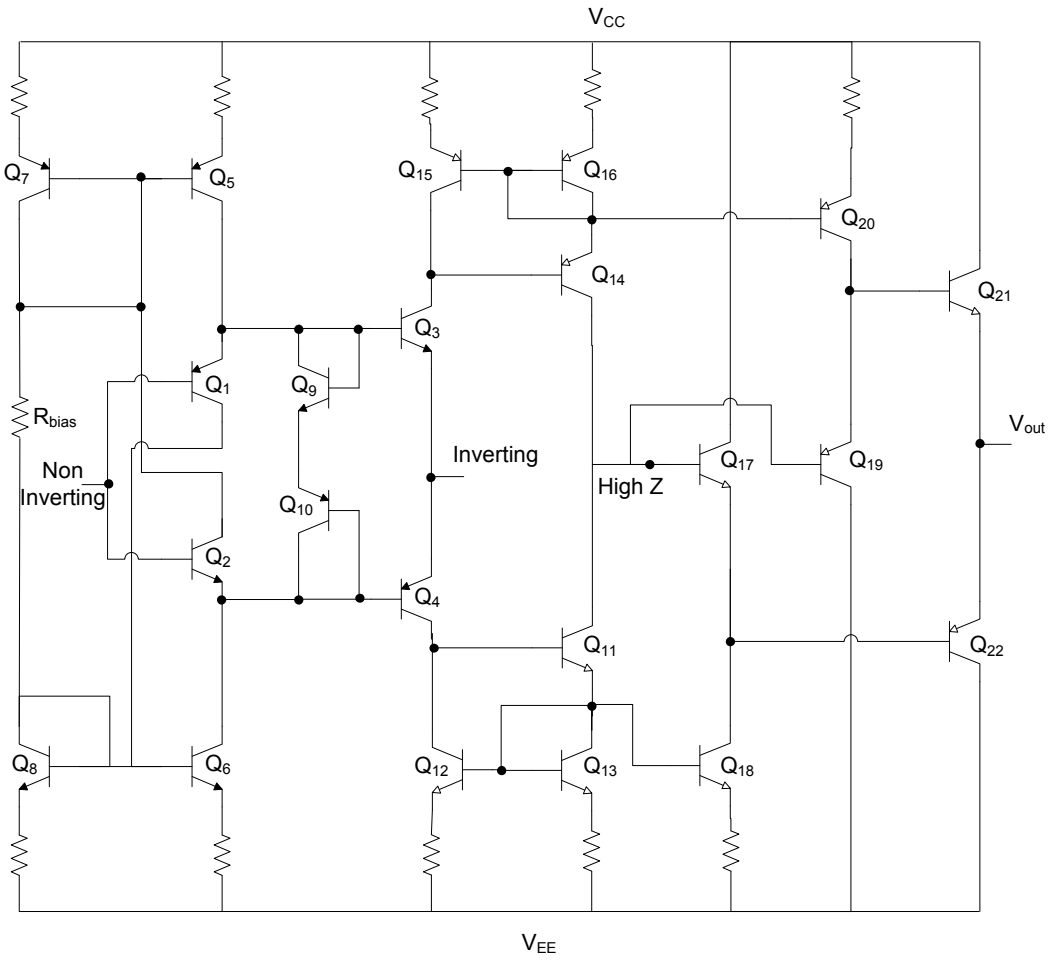


Figure 5.5 Double buffer current booster CFOA

The configuration for measuring and simulation of slew rate for the CFOA is shown in Figure 5.6. If the input step is sufficiently small (<0.5V), the output should not

slew [24]. If the input step magnitude is large, the CFOA will slew. The slew rate can be determined from the slope of the output waveform during the rise and fall of the waveform. The CFOA should be configured in the unity gain configuration with a feedback resistance greater than the critical resistance of the CFOA.

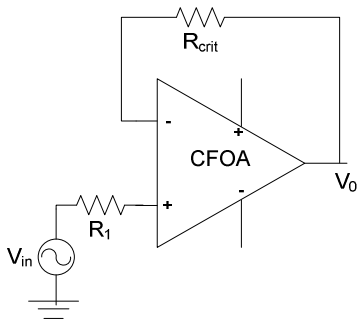


Figure 5.6 SR simulation circuit

5.2 Critical Resistance

Figure 5.7 shows a CFOA configured as a voltage follower. In the voltage follower configuration, the CFOA needs to use with feedback resistance. With zero feedback resistance, the output voltage phase crosses 180º before amplitude goes down to zero dB. The minimum value of feedback resistance needed to maintain stable operation is called the critical resistance. Critical resistance can be found from the transimpedance plot. A typical transimpedance plot for the CFOA is shown in Figure 5.8. If the magnitude and phase for transimpedance are plotted in the same graph then at a certain frequency the phase exceeds 180º. At 180º phase shift, the value of the transimpedance is the critical resistance.

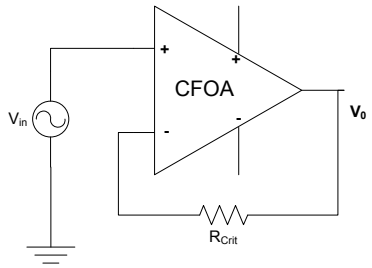


Figure 5.7 CFOA configured as a voltage follower

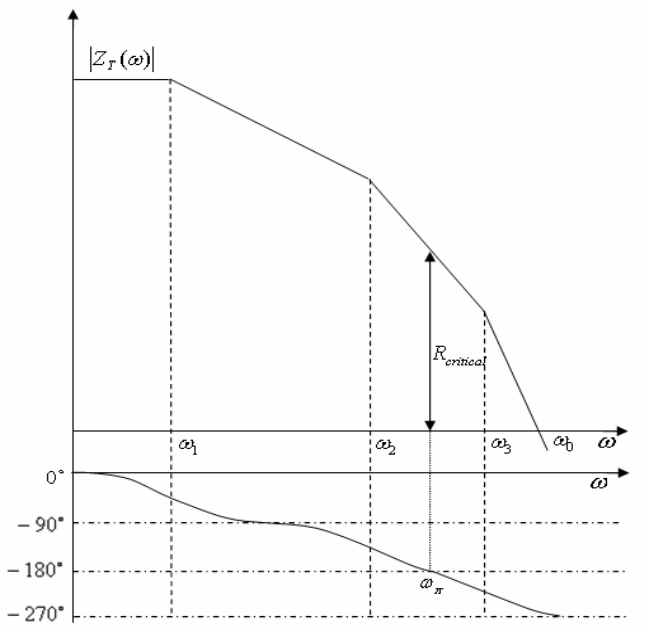


Figure 5.8 Typical transimpedance plot

5.3. Gain Bandwidth Product and the Slew Rate Relationship for VFOA

The DC gain of a VFOA is

$$G_{vdm}(0) = Z_T(0) g_{meffdm} \tag{5.3}$$

where $Z_T(s)$ is the transimpedance function of the class A driver and g_{meffdm} is the effective differential mode transconductance of the driver devices Q_1 and Q_2 of the VFOA which is shown in Figure 5.2.

Here, the -3 dB bandwidth is the frequency at which the magnitude of the voltage gain is 1/√2 times the DC value. The bandwidth of the VFOA is [25]

$$BW = \frac{1}{Z_T(0)\left(C_C + C_{\mu 5}\right)} \tag{5.4}$$

The gain bandwidth product is defined as the product of the DC gain and the -3 dB bandwidth. Thus the gain bandwidth product of the VFOA is [25]

$$GBW = \frac{g_{meffdm}}{C_C + C_{\mu 5}} \tag{5.5}$$

The magnitude and phase response for a typical VFOA is shown in figure 5.9.

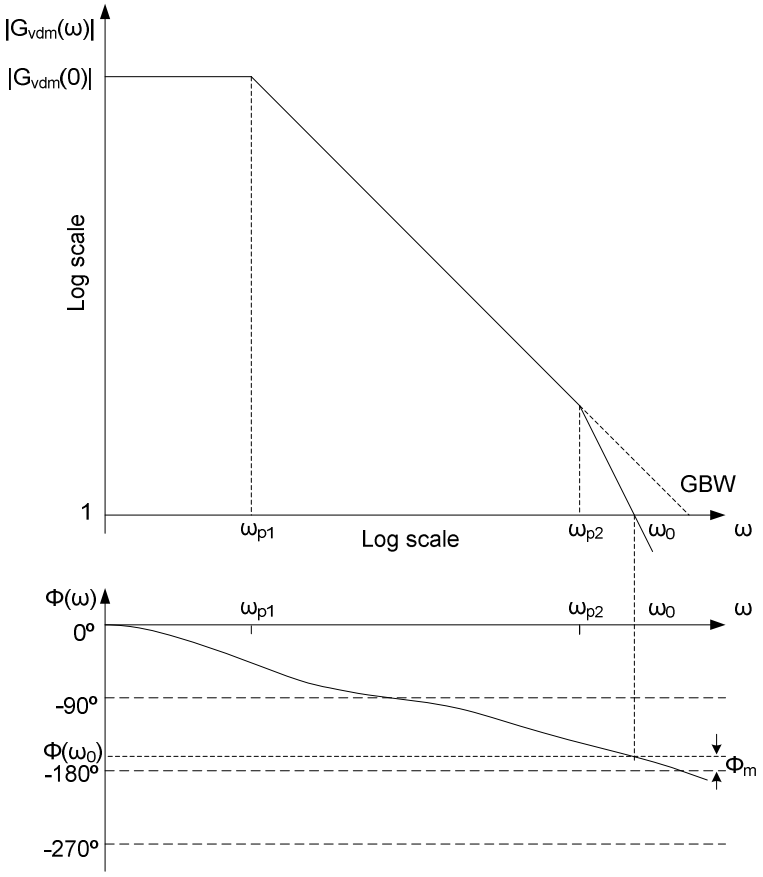


Figure 5.9 Magnitude and phase response of VFOA

From equation (5.2) and (5.5), it is clear that slew rate and gain bandwidth product is related. Thus for this VFOA,

$$SR = \frac{I_{EE} GBW}{g_{meffdm}} \tag{5.6}$$

5.4 Gain Bandwidth Product for the CFOA in the Non-inverting Gain Configuration

The block diagram for the CFOA in the non-inverting gain configuration is shown in Figure 5.10. The CFOA is replaced by the macro-model discussed in section 4.1 and the resulting figure is shown in Figure 5.11.

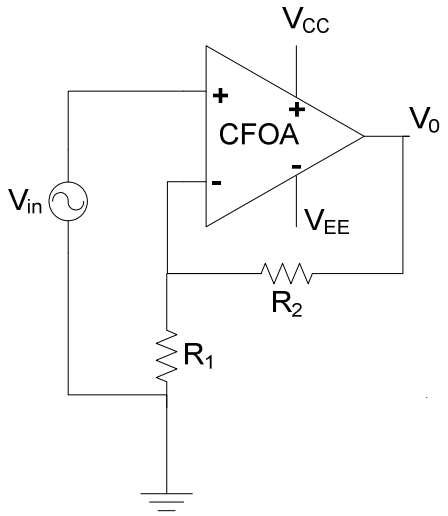


Figure 5.10 CFOA in non-inverting gain configuration

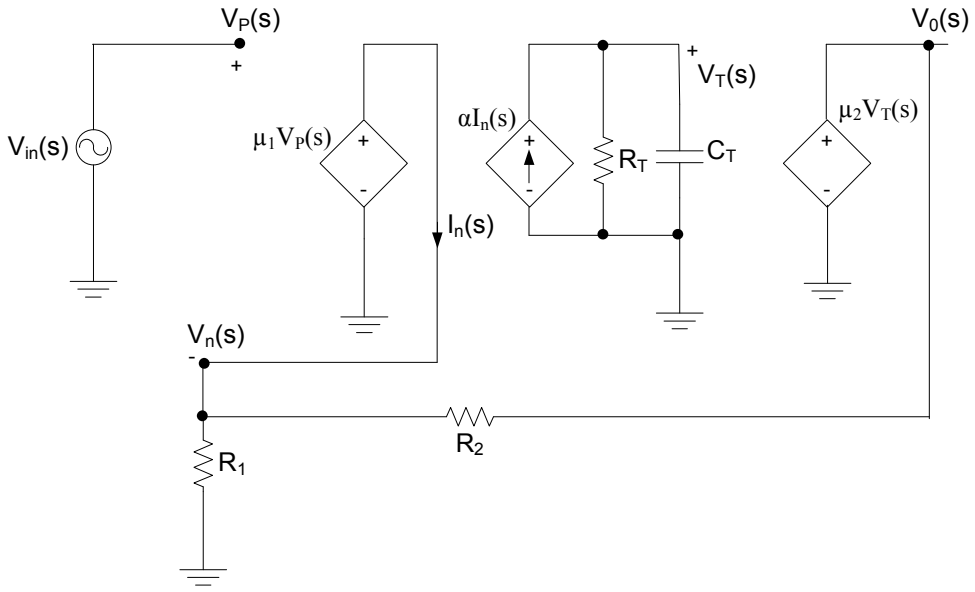


Figure 5.11 The CFOA in non-inverting gain configuration where the CFOA is replaced with its macro-model

Here, μ_1 is the coefficient for the input buffer, α is the coefficient for the current mirror, and μ_2 is the coefficient for the output buffer. The typical value for those parameters is one. Here, R_n is the output resistance of the input buffer, and R_0 is the output resistance for output buffer. The typical value for those parameters is less than 100 Ω. Here the assumption made for the macro-model is

$$\mu_1 = \mu_2 = \alpha = 1 \tag{5.7}$$

and

$$R_n = R_{out} = 0 \tag{5.8}$$

So,

$$V_n(s) = \mu_1 V_1(s) = \mu_1 V_p(s) = \mu_1 V_{in}(s) = V_{in}(s) \tag{5.9}$$

The node equation at node V_n of Figure 5.11 is

$$I_n(s) = \frac{V_n(s)}{R_1} + \frac{V_n(s) - V_0(s)}{R_2} \tag{5.10}$$

Since $\mu_2 = 1$

$$V_0(s) = \mu_2 V_T(s) = V_T(s) \tag{5.11}$$

and

$$V_T(s) = \alpha(s) Z_T(s) I_n(s) = Z_T(s) I_n(s) \tag{5.12}$$

Combining equations (5.9), (5.10), (5.11), and (5.12), the non-inverting voltage gain becomes,

$$G_{VNI}(s) = \frac{V_0(s)}{V_{in}(s)} = \left(1 + \frac{R_2}{R_1}\right)\left[\frac{\frac{Z_T(s)}{R_2}}{1 + \frac{Z_T(s)}{R_2}}\right] = \left(1 + \frac{R_2}{R_1}\right)\left[\frac{T(s)}{1 + T(s)}\right] \tag{5.13}$$

The open loop gain is

$$T(s) = \frac{Z_T(s)}{R_2} = \frac{\frac{R_T}{R_2}}{1 + \frac{s}{\omega_{ol}}} \tag{5.14}$$

and the open loop pole is

$$\omega_{ol} = \frac{1}{R_T C_T} \tag{5.15}$$

So, the open loop transimpedance is

$$Z_T(s) = \frac{R_T}{1 + \frac{s}{\omega_{ol}}} \tag{5.16}$$

The open loop gain bandwidth product is

$$GBW_{ol} = T(0)\omega_{ol} = \left(\frac{R_T}{R_2}\right)\frac{1}{R_T C_T} = \frac{1}{R_2 C_T} \tag{5.17}$$

The closed loop gain at low frequencies is

$$G_{VNI}(0) = \left(1+\frac{R_2}{R_1}\right)\left(\frac{T(0)}{1+T(0)}\right) \tag{5.18}$$

$$G_{VNI}(0) = \left(1+\frac{R_2}{R_1}\right)\left(\frac{\frac{R_T}{R_2}}{1+\frac{R_T}{R_2}}\right) \tag{5.19}$$

Since $\frac{R_T}{R_2}$>>1,

$$G_{VNI}(0) \cong \left(1+\frac{R_2}{R_1}\right) \tag{5.20}$$

The closed loop bandwidth is

$$\omega_{ANI} = \left(1+\frac{R_T}{R_2}\right)\omega_{ol} \cong \frac{R_T}{R_2}\omega_{ol} = \frac{1}{R_2 C_T} \tag{5.21}$$

The closed loop gain bandwidth product is

$$GBW_{cl} = G_{VNI}(0)\omega_{ANI} = \left(1+\frac{R_2}{R_1}\right)\frac{R_T}{R_2}\omega_{ol} = \left(1+\frac{R_2}{R_1}\right)\frac{1}{R_2 C_T} = \left(1+\frac{R_2}{R_1}\right)GBW_{ol} \tag{5.22}$$

The closed loop gain bandwidth product is $(1+R_2/R_1)$ times greater than the open loop gain bandwidth product.

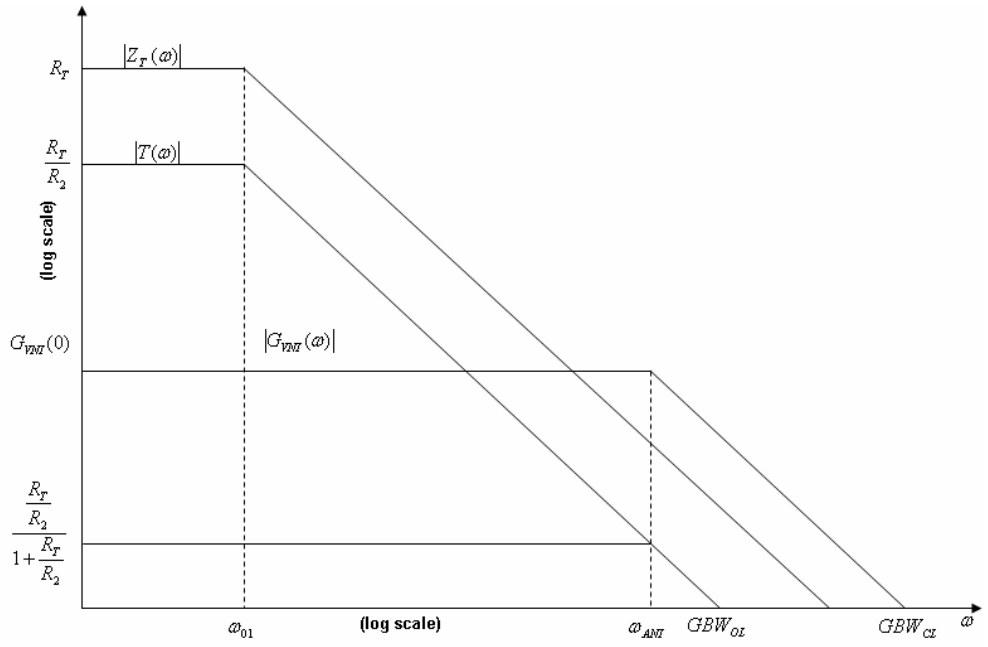


Figure 5.12 CFOA Bode plot

5.5 Simulation Results

Figure 5.13 shows the simulation result for the critical resistance for the double buffer current feedback operational amplifier which is shown in Figure 3.9. Here the solid line is the amplitude plot and the dotted line is the phase plot. It shows that at the frequency of 2.05 GHz, the phase shift is 180° between input and output. At that frequency, the magnitude of the transimpedance plot is 323 Ω. Thus, the critical resistance for the CFOA is 323 Ω.

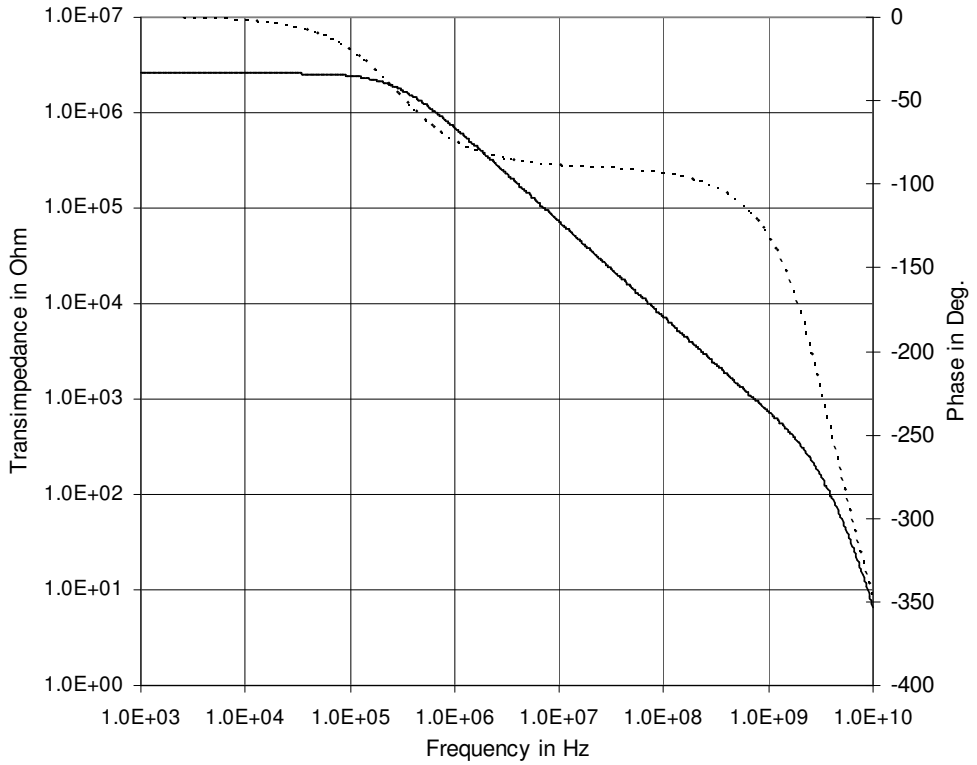


Figure 5.13 Critical resistance for double buffer CFOA

Figure 5.14 shows the double buffer CFOA slew rate simulation. Here the feedback resistance is 1.5 kΩ. The positive slew rate is 3405 V/uS, and the negative slew rate is 2192 V/uS.

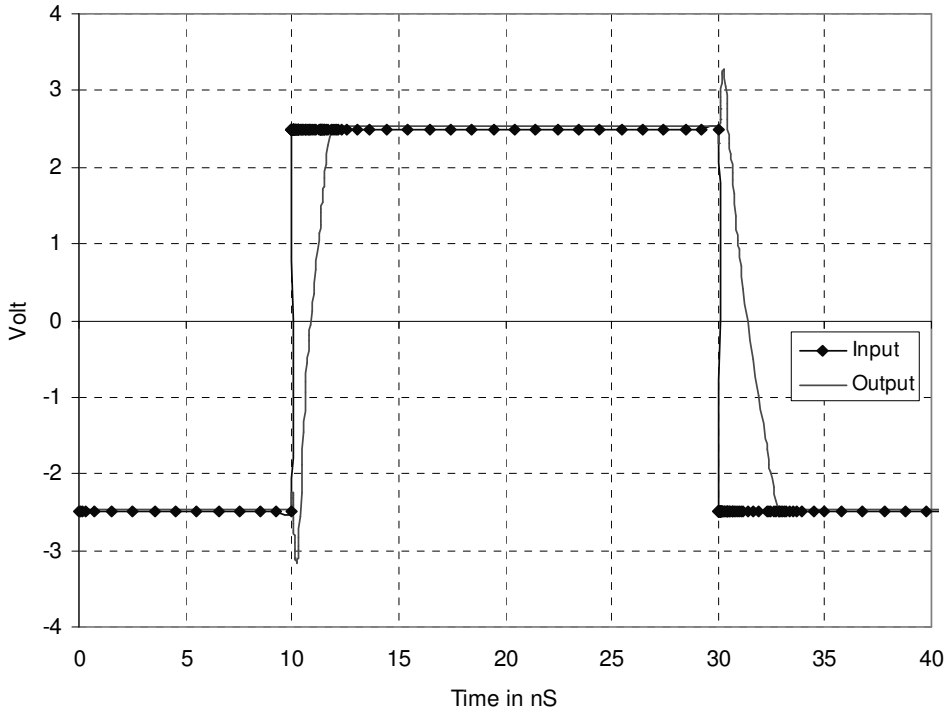


Figure 5.14 Double buffer CFOA slew rate simulation

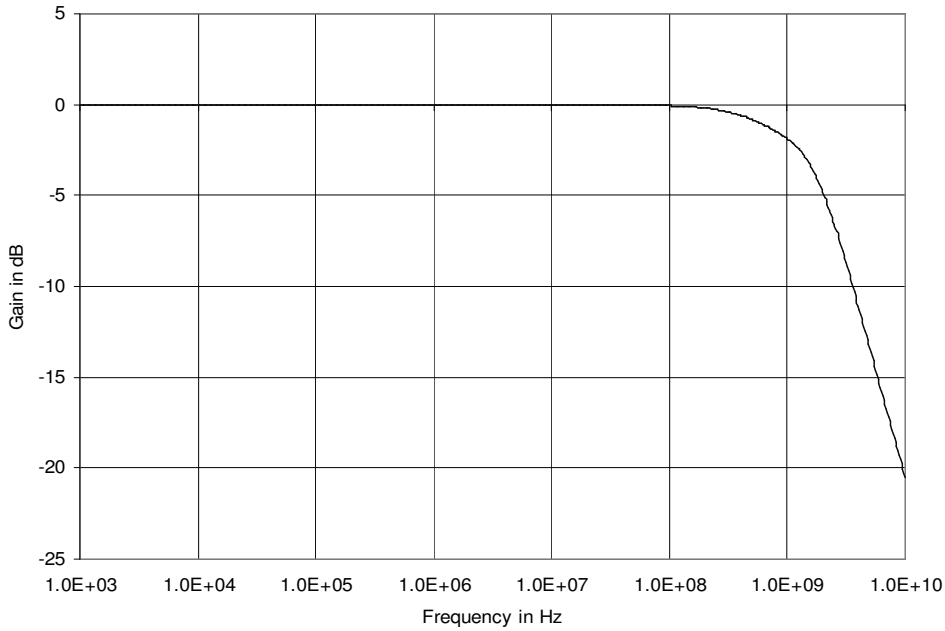


Figure 5.15 Double buffer CFOA bandwidth simulation

Figure 5.15 shows the double buffer CFOA bandwidth simulation. The feedback resistance is 1.5 kΩ. Here, -3 dB bandwidth is 1.457 GHz for the gain of one configuration.

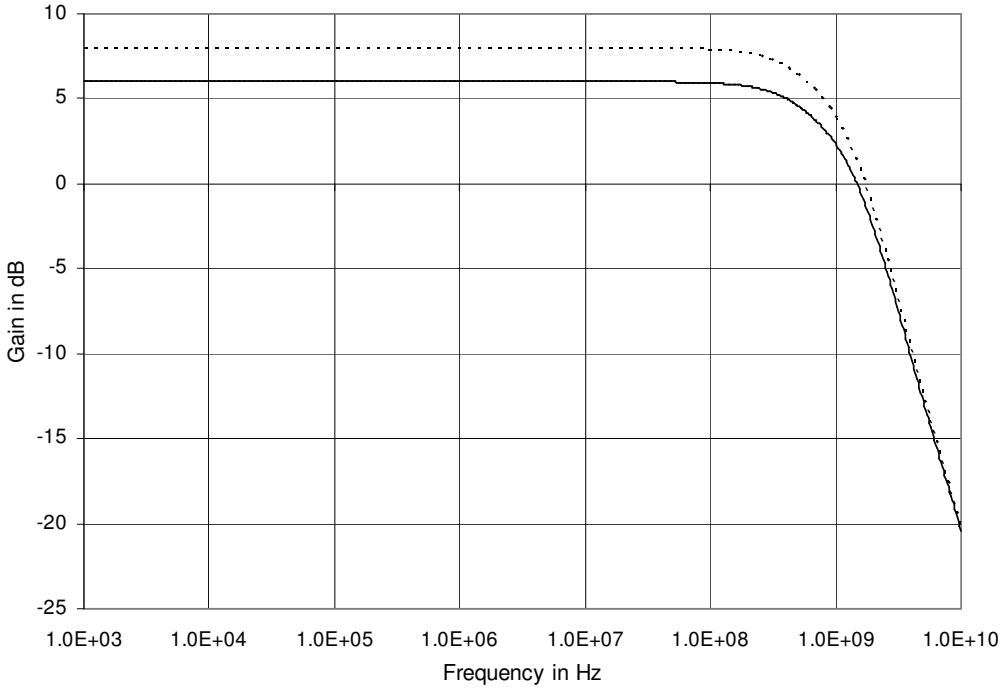


Figure 5.16 Double buffer CFOA bandwidth simulation for various gain configurations

Figure 5.16 shows the Bode plot for the double buffer CFOA in the non-inverting gain configuration. The CFOA configuration is shown in Figure 5.10. The dotted line shows the Bode plot for R_1 = 1 kΩ, R_2 = 1.5 kΩ. The low frequency gain is 7.943 dB, and the -3 dB bandwidth is 783 MHz. So, the gain bandwidth product is 1954 MHz. The solid line shows the Bode plot for R_1 = 1.5 kΩ, R_2 = 1.5 kΩ. The low frequency gain is 6.005 dB, and the -3 dB bandwidth is 842.8 MHz. The gain

bandwidth product is 1683 MHz. So, the gain bandwidth product is variable for the CFOA. This is one of the advantages of the CFOA over the VFOA.

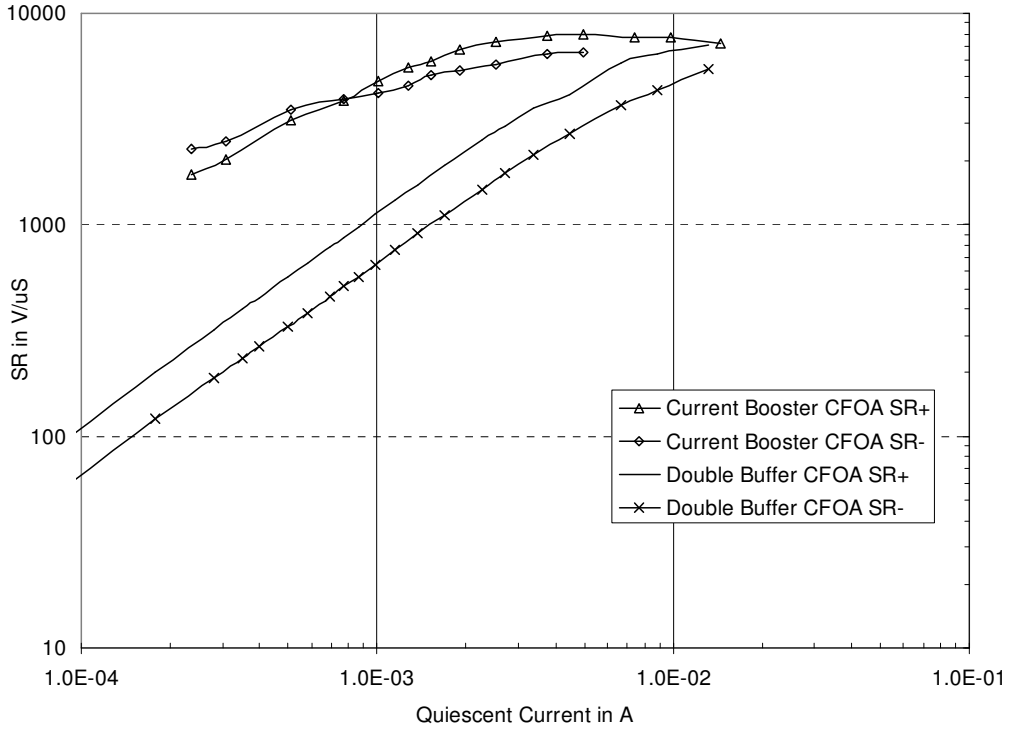


Figure 5.17 Slew rate versus quiescent current for CFOA

Figure 5.17 shows the slew rate versus the quiescent current for the double buffer CFOA and the double buffer current booster CFOA. The schematic diagram for the double buffer CFOA is shown in Figure 3.9. The schematic diagram for the double buffer current booster CFOA is shown in Figure 5.5. The feedback resistance used for the slew rate simulation is 1.5 kΩ. It shows that at lower quiescent current, the slew rate is low. The current booster increases the slew rate at low quiescent current. But, at high quiescent current, the current booster does little for the slew rate.

Figure 5.18 shows the -3 dB bandwidth versus quiescent current for the double buffer CFOA and the double buffer current booster CFOA. For the double buffer CFOA, the maximum -3 dB bandwidth is 1.893 GHz for one gain configuration. The quiescent current for maximum bandwidth is 6.64 mA. For the double buffer current booster CFOA, the maximum -3 dB bandwidth is 1.831 GHz for one gain configuration. The quiescent current for maximum bandwidth is 4.98 mA.

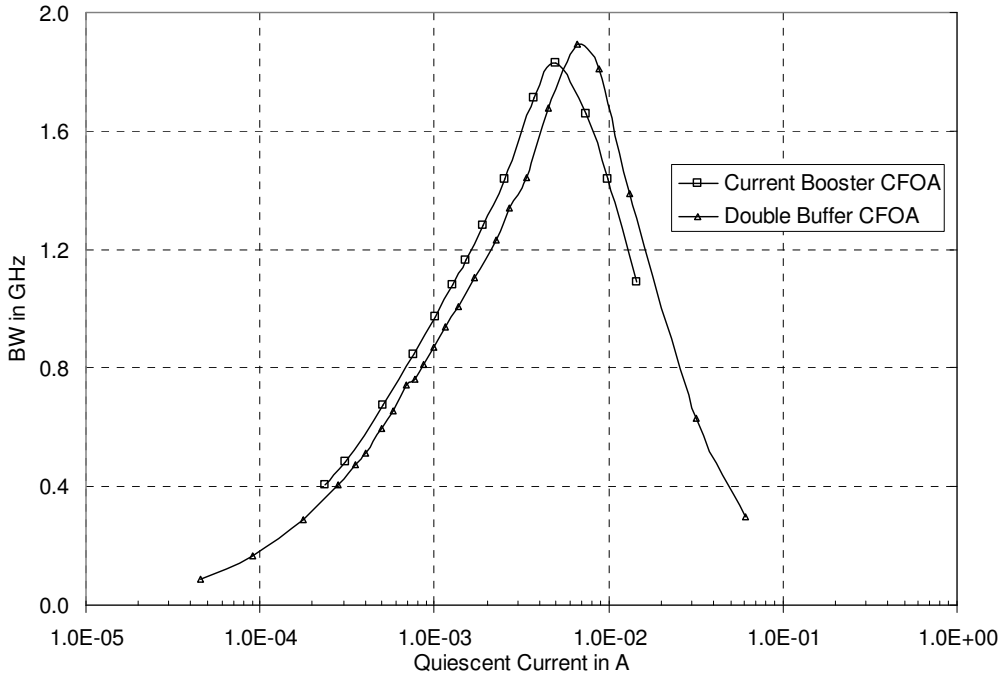


Figure 5.18 Bandwidth versus quiescent current for CFOA

Figure 5.19 shows the bandwidth/power dissipation versus quiescent current for the double buffer CFOA and the double buffer current booster CFOA. Power dissipation is defined in section 3.8. For 45.3 uA quiescent current, the bandwidth/power dissipation is 1.99×10^{11} Hz/W, and for 61.3 mA quiescent current, the bandwidth/power dissipation is 0.49×10^{9} Hz/W for the double buffer CFOA. For 235

uA quiescent current, the bandwidth/power dissipation is 1.72×10^{11} Hz/W, and for 14.5 mA quiescent current, the bandwidth/power dissipation is 7.52×10^{9} Hz/W for the double buffer current booster CFOA. That means for low quiescent current, bandwidth/power dissipation is high, and for high quiescent current bandwidth/power dissipation is low.

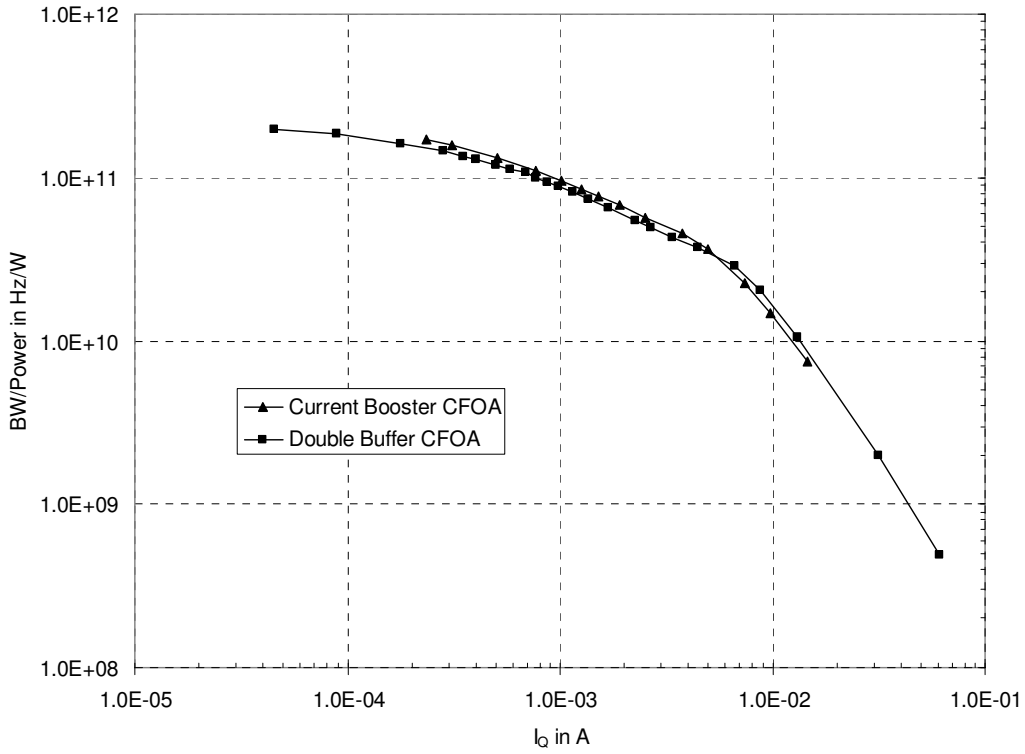


Figure 5.19 Bandwidth/power dissipation versus quiescent current for CFOA

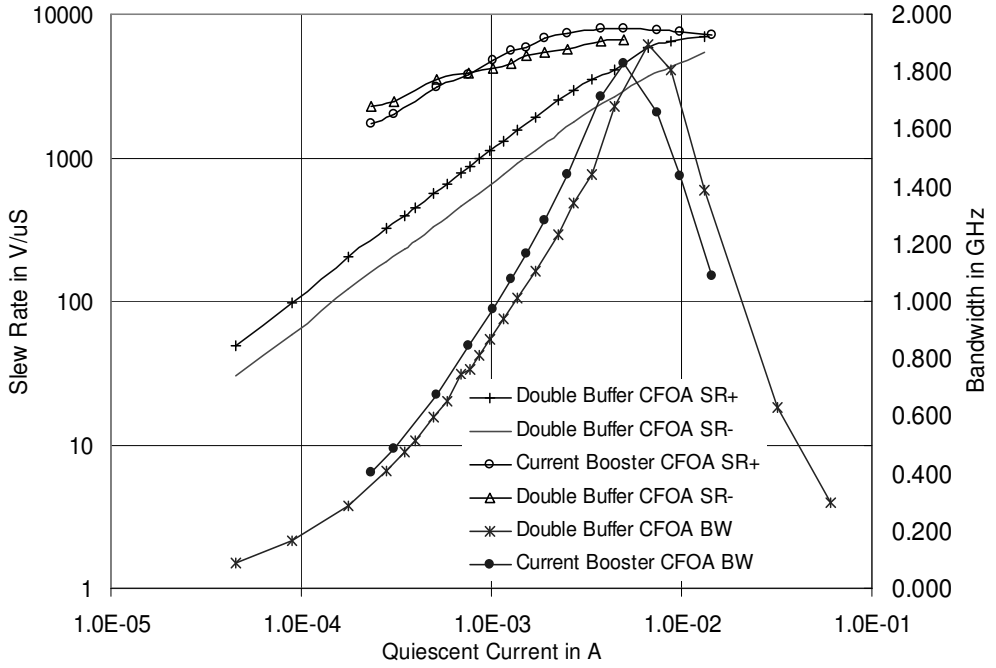


Figure 5.20 Slew rate and bandwidth versus quiescent current for CFOA

Figure 5.20 shows the slew rate and bandwidth versus quiescent current for the double buffer CFOA and the double buffer current booster CFOA.

5.6 Summary

The critical resistance for the double buffer CFOA was found to be 325 Ω. The gain bandwidth product for the CFOA is variable. It was proved mathematically and by simulation. For 2.0 gain configuration, the gain bandwidth product is 1683 MHz, and for 2.5 gain configuration, the gain bandwidth product is 1953 MHz. There is a relationship between slew rate, quiescent current and bandwidth for the CFOA. For 0.3 mA quiescent current, the positive slew rate is 340 V/μS, and the negative slew rate is 200 V/μS for the double buffer CFOA. For the same quiescent current, the positive slew rate is 2000 V/μS, and the negative slew rate is 2400 V/μS for the double buffer current

booster CFOA. For 4.0 mA quiescent current, the positive slew rate is 3850 V/μS, and the negative slew rate is 2400 V/μS for the double buffer CFOA. For same quiescent current, the positive slew rate is 7900 V/μS, and the negative slew rate is 6500 V/μS for the double buffer current booster CFOA. For lower quiescent current, the slew rate is lower, and for higher quiescent current the slew rate is higher. Bandwidth also varies with quiescent current. For the double buffer CFOA, the maximum -3dB bandwidth is 1.893 GHz for one gain configuration. The quiescent current for maximum bandwidth is 6.64 mA. For the double buffer current booster CFOA, the maximum -3dB bandwidth is 1.831 GHz for one gain configuration. The quiescent current for maximum bandwidth is 4.98 mA. Bandwidth/power dissipation versus quiescent current for both types of CFOAs were plotted. For the double buffer CFOA, the bandwidth/power dissipation is 1.99×10^{11} Hz/W for 45.3 μA quiescent current and 4.9×10^{8} Hz/W for 61.3 mA quiescent current. For the double buffer current booster CFOA, the bandwidth/power dissipation is 1.72×10^{11} Hz/W for 235 μA quiescent current and 7.52×10^{9} Hz/W for 14.5 mA quiescent current.

CHAPTER 6

TEMPERATURE DEPENDENCE OF THE CURRENT FEEDBACK OPERATIONAL AMPLIFIER

6.1 CFOA Parameter with Temperature

Current feedback operational amplifier parameters changes with temperature. These parameters are the input offset current (I_{OS}), input offset voltage (V_{OS}), common mode input range (CMIR), common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), open loop transimpedance, slew rate, quiescent current, bandwidth, and output swing. All simulation results are for the full model double buffer CFOA.

The current transfer curve is defined by the output voltage change as a function of input current. The CFOA current transfer curve with temperature is shown in Figure 6.1. It is seen that at higher temperatures the current transfer curve shifts to the right. The power supply for the CFOA is ± 5 V. Maximum output voltages increase if temperature increases. The reason for this is that the transistor beta increases as temperature increases.

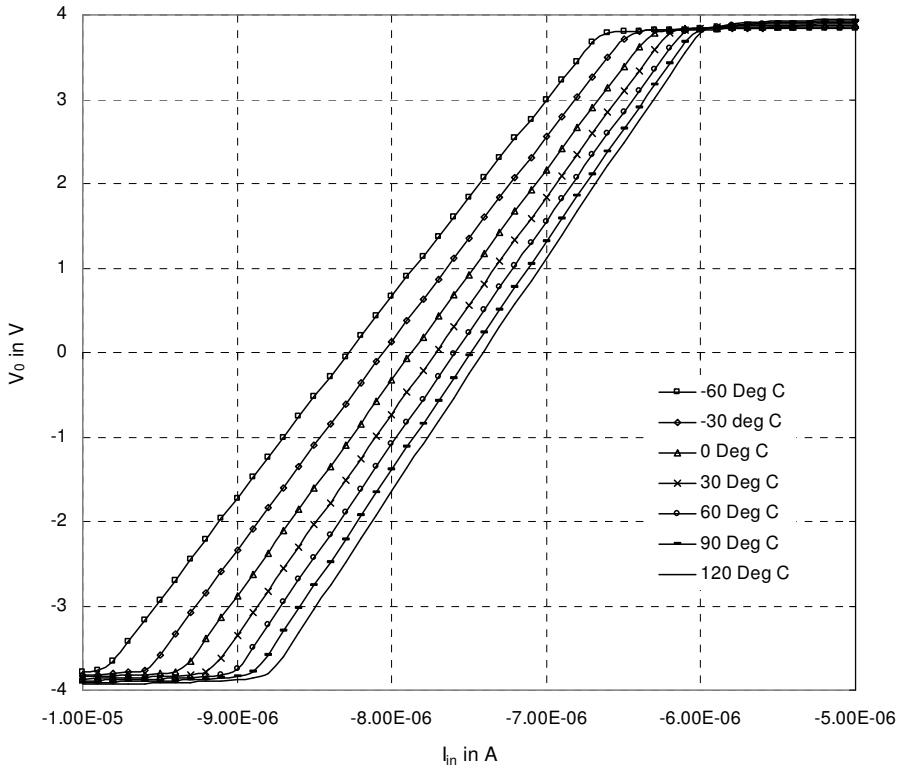


Figure 6.1 CFOA current transfer curve with temperature

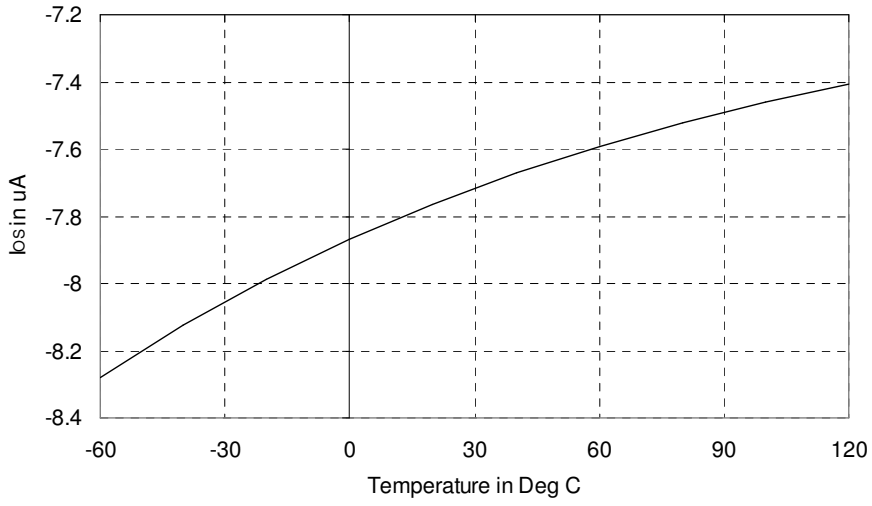


Figure 6.2 Input offset current versus temperature

Figure 6.2 shows the input offset current versus temperature. If temperature increases, the input offset current decreases. The reason for this is that the transistor beta increases as temperature increases.

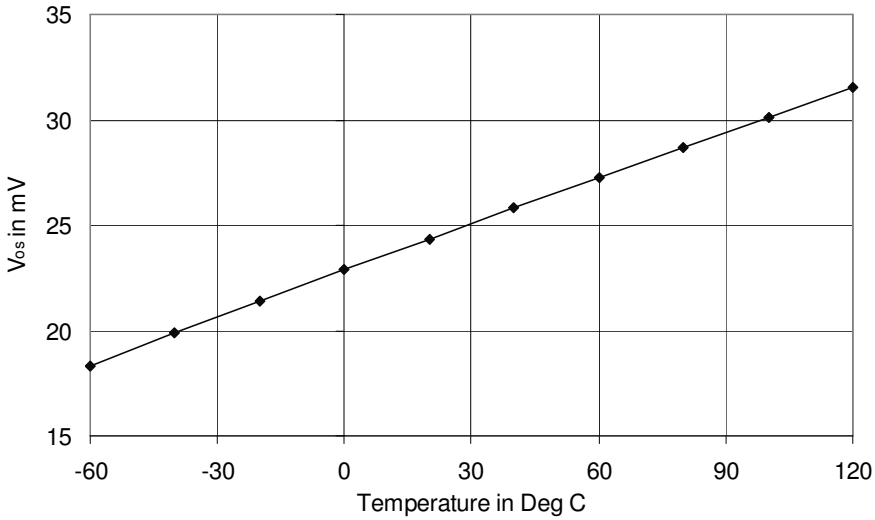


Figure 6.3 Input offset voltage versus temperature

Figure 6.3 shows the input offset voltage versus temperature. If temperature increases, the input offset voltage increases.

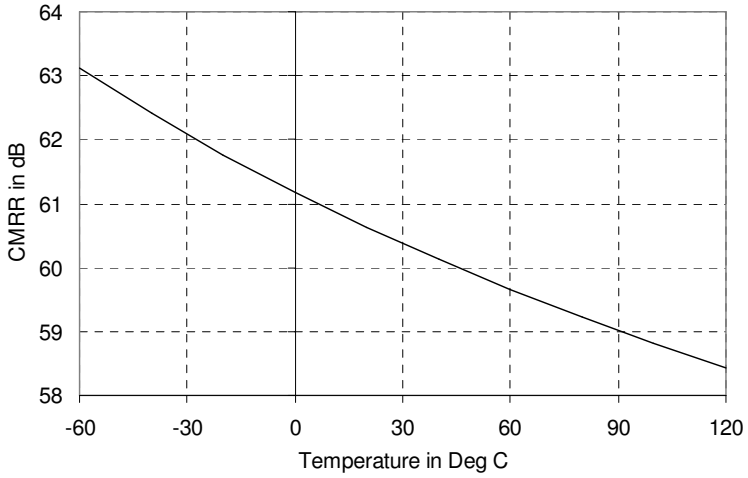


Figure 6.4 Common mode rejection ratio versus temperature

Figure 6.4 shows the common mode rejection ratio versus temperature. If temperature increases, the common mode rejection ratio decreases.

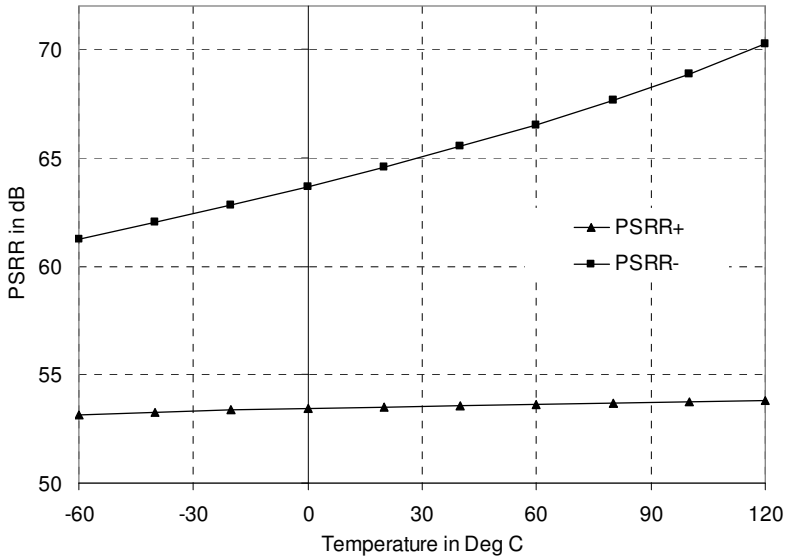


Figure 6.5 Power supply rejection ratio versus temperature

Figure 6.5 shows the power supply rejection ratio versus temperature. If temperature increases, the power supply rejection ratio (PSRR) increases. But the $PSRR^+$ (at positive supply) increases faster than the $PSRR^-$ (at the negative supply).

Figure 6.6 shows the open loop transimpedance versus temperature. If temperature increases, the open loop transimpedance increases.

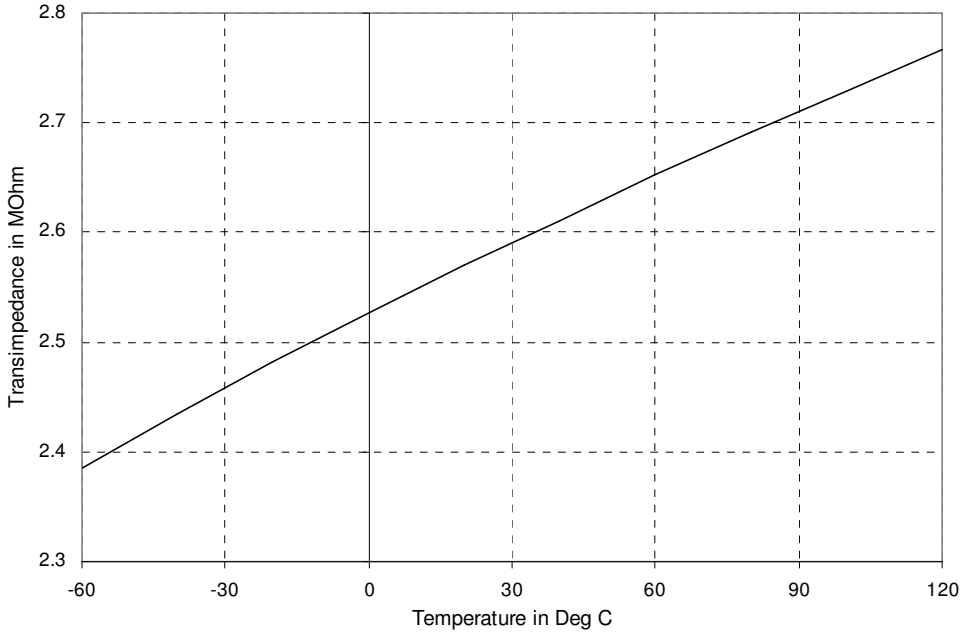


Figure 6.6 Open loop transimpedance versus temperature

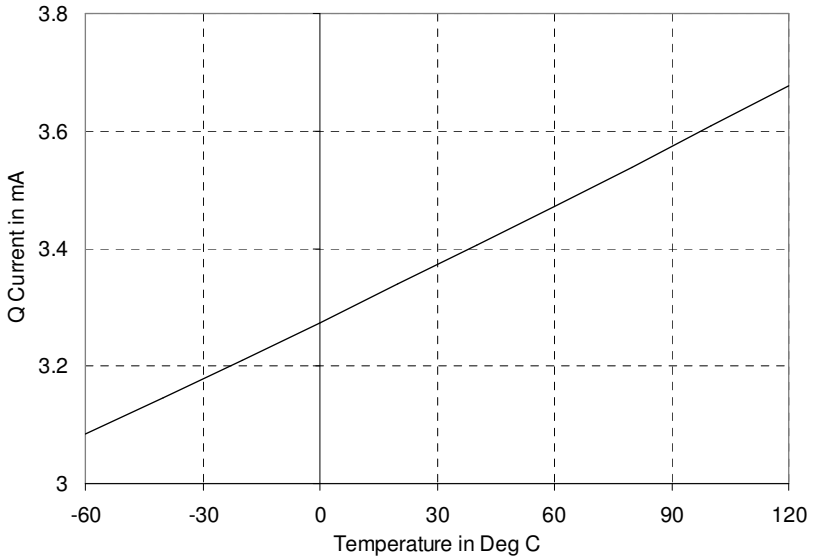


Figure 6.7 Quiescent versus temperature

Figure 6.7 shows the quiescent current versus temperature. If temperature increases, the quiescent current increases.

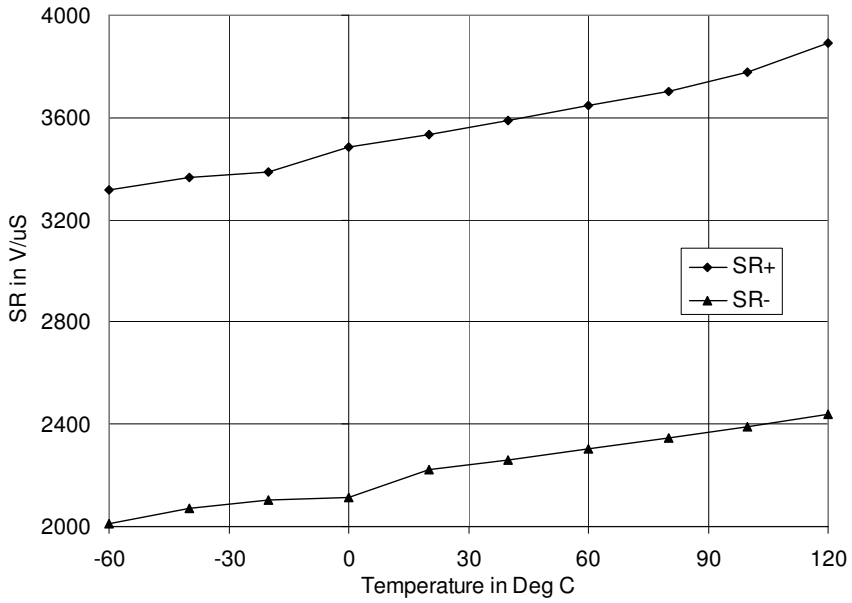


Figure 6.8 Slew rate versus temperature

Figure 6.8 shows the slew rate versus temperature. Here the slew rate increases if temperature increases. The positive slew rate for the CFOA input stage of figure 5.3 is given by [28]

$$SR^{+} \approx \frac{I_{C5} - \dfrac{|V_{in}|}{\beta_{npn} R_{fb}}}{C_{jsp} + C_{jcn}} \tag{6.1}$$

The negative slew rate for the CFOA input stage of figure 5.3 is given by [28]

$$SR^{-} \approx \frac{I_{C6} - \dfrac{|V_{in}|}{\beta_{pnp} R_{fb}}}{C_{jsn} + C_{jcp}} \tag{6.2}$$

Since the transistor beta increases with temperature, the SR^{+} and SR^{-} also increase with temperature.

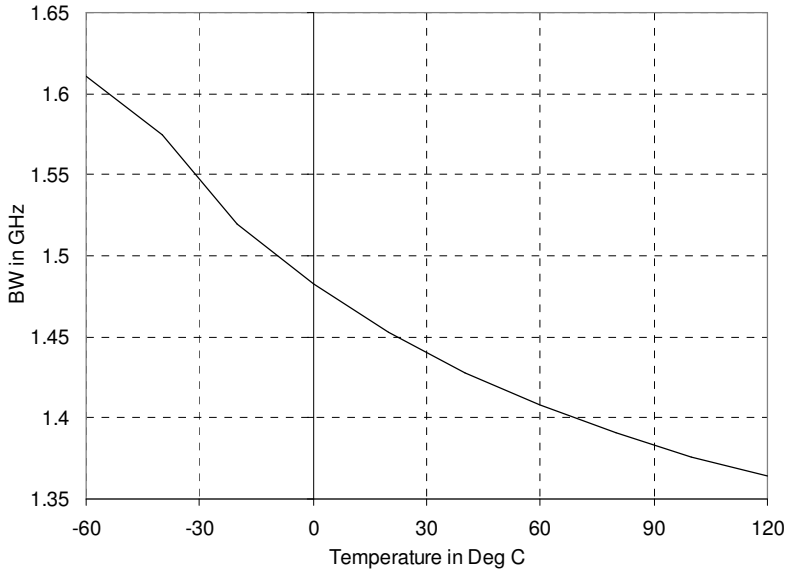


Figure 6.9 Bandwidth versus temperature

Figure 6.9 shows the -3 dB bandwidth versus temperature. If temperature increases, the bandwidth decreases.

This is all summarize in Table 6.1.

Table 6.1 Summary of the CFOA Parameters with Temperature

Parameter	Increase/decrease with temperature
Input offset current	Decrease
Input offset voltage	Increase
Common mode rejection ratio	Decrease
Power supply rejection ratio	Increase
Transimpedance	Increase
Quiescent current	Increase
Slew rate	Increase
Bandwidth	Decrease

CHAPTER 7

SINUSOIDAL WAVE GENERATOR USING A CURRENT FEEDBACK OPERATIONAL AMPLIFIER

The purity of a sinusoidal wave is measured by its total harmonic distortion [29]. A pure sine wave has only the fundamental, and all other harmonics are zero, making the Total Harmonic Distortion (THD) = 0%. For a pure triangular wave, the THD is approximately 12%. The objective of the sine wave generator is to achieve a THD as low as possible.

7.1 Condition of Oscillation

An oscillator produces a periodic voltage waveform that has to be sustained indefinitely without any input signal. The block diagram for a sinusoidal oscillator is shown in Figure 7.1 [30]. It consists of an amplifier and a feedback network.

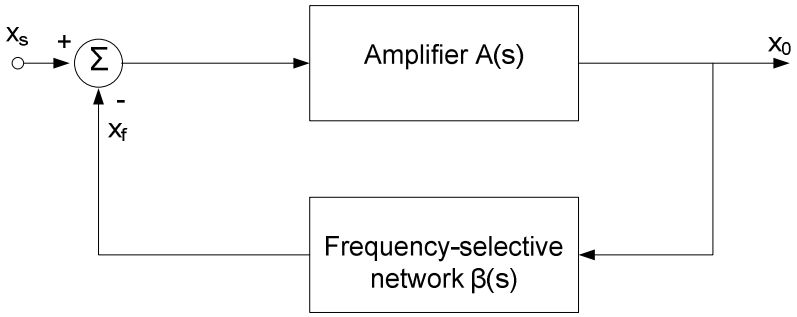


Figure 7.1 The basic structure of a sinusoidal oscillator

For an actual oscillator circuit, there is no input signal. The circuit amplifies its own noise component at the frequency of f_0. The closed loop gain with its feedback network is given by

$$A_f(s) = \frac{A(s)}{1 + A(s)\beta(s)} \tag{7.1}$$

The loop gain for this circuit is

$$L(s) = A(s)\beta(s) \tag{7.2}$$

The characteristic equation is

$$1 + L(s) = 0 \tag{7.3}$$

For the oscillation to begin, a loop gain of -1 or smaller is necessary [31]. If a negative feedback circuit has a loop gain that satisfies two conditions:

$$\left|L(f_0)\right| \geq 1 \tag{7.4}$$

$$\angle L(f_0) = 180^\circ \tag{7.5}$$

then the circuit can oscillate at f_0. These conditions are called the "Barkhausen criteria". The Barkhausen criterion guarantees sustained oscillations in the mathematical sense. In order to ensure oscillation in the presence of temperature and process variations, it is required to choose a loop gain magnitude greater than 1.

7.2 Design of Practical Oscillators

The steady state operating conditions of an oscillator cannot be accurately predicted by simple mathematical techniques. The design of practical oscillators is more art than an exact science [32]. Due to the nonlinearity of the circuits, the linear methods used in analysis of amplifiers in principle do not apply to oscillators. However, linear

analysis is useful in predicting many aspects of the oscillator. In an oscillator, the output of the circuit must be fed back to the input with a gain slightly greater than unity and with a phase shift of 180°. Approximate prediction of the oscillation frequency can be made by using the small signal analysis of the circuit. The magnitude of the loop gain at the oscillation frequency should be $1.3>|A(s)\beta(s)|>1.00$ [32] to ensure the generation of the oscillation with minimum harmonic distortion. The transient time to steady state operation is shorter for higher loop gain at the frequency of oscillation [32].

The frequency dependency of the reactive components complicates the oscillator design. At a higher frequency, an inductor may act as a capacitor due to the stray capacitance between the windings of the inductor. The parasitic effects in the reactive component may cause the circuit to oscillate at different frequencies than those predicted by linear small signal analysis.

7.3 Sinusoidal Oscillators Using Current Feedback Operational Amplifiers

Recently, a variety of sinusoidal oscillators have been proposed using current feedback operational amplifiers. In [33], the author proposed sinusoidal oscillator using a CFOA. Five passive components and one CFOA are required to build an oscillator. With the combination of five external components, five different oscillators can be produced. Frequency of oscillation was shown from 0.2 MHz to 0.65 MHz with a function of one passive component.

In [34], the author proposed a sinusoidal oscillator using a CFOA. Four to six passive components and one CFOA are required to build an oscillator. With the combination of four to six external components, eight different oscillators can be

produced. Frequency of oscillation was shown from 0.7 MHz to 1.1 MHz as a function of one passive component.

In [35], the author proposed sinusoidal oscillator using two CFOAs. Seven passive components and two CFOAs are required to build an oscillator. The frequency of oscillation was shown from 5 MHz to 50 MHz as a function of one passive component. In [36-44], the authors proposed various sinusoidal oscillators using current feedback operational amplifiers.

7.4 Proposed Sinusoidal Oscillator Using a CFOA

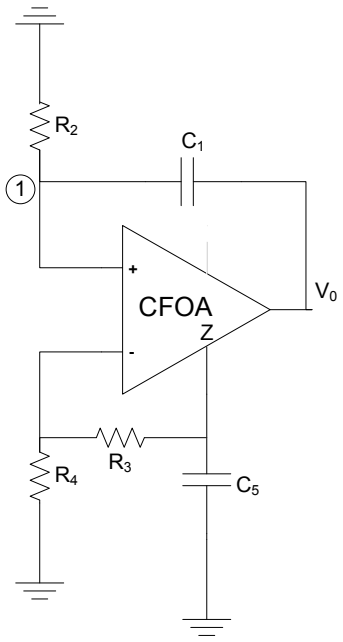


Figure 7.2 Sinusoidal oscillator using CFOA

The sinusoidal oscillator circuit is shown in Figure 7. 2 [45]. There are two ways to find the frequency of oscillation of this circuit. The first way is to find the loop gain. To find the loop gain, the loop is broken at the CFOA positive input terminal and an input voltage V_1 is applied. Then the return voltage that appears at node 1 is found.

The loop gain is equated to unity to find ω_0. The second approach is to analyze the circuit and eliminate all current and voltage variables. Then generate a Nodal-Admittance Matrix (NAM). The determinant of the NAM is set to zero. The resulting equation can be used to predict the frequency of oscillation and condition of oscillation. The full CFOA used in this research is shown in Figure 3.9. A macro-model for this amplifier is shown in Figure 4.1. Replacing the CFOA by its macro-model in Figure 7.2, the circuit becomes that shown in Figure 7.3.

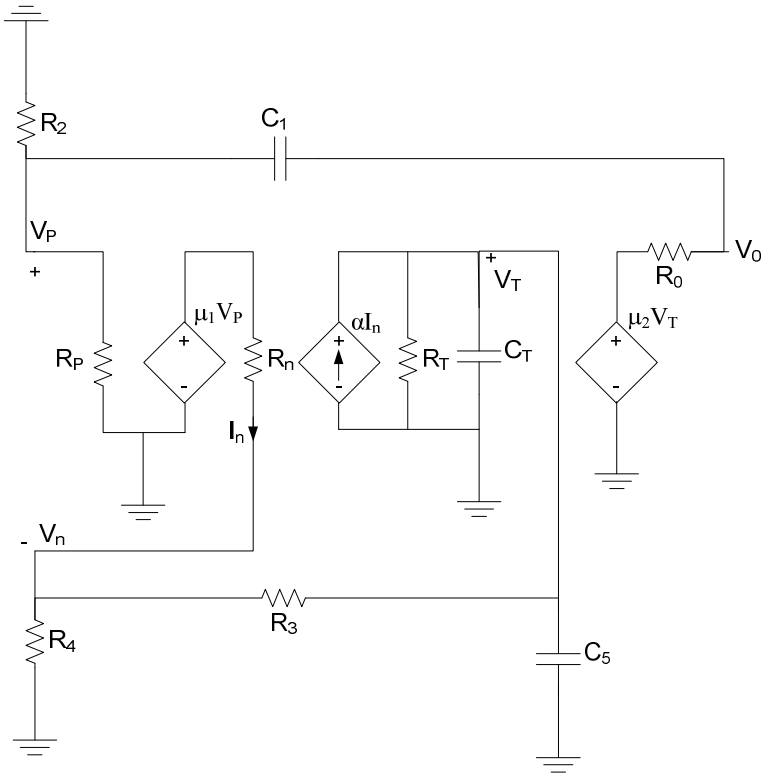


Figure 7.3 Sinusoidal oscillator

Rearranging Figure 7. 3, the circuit becomes that shown in Figure 7.4.

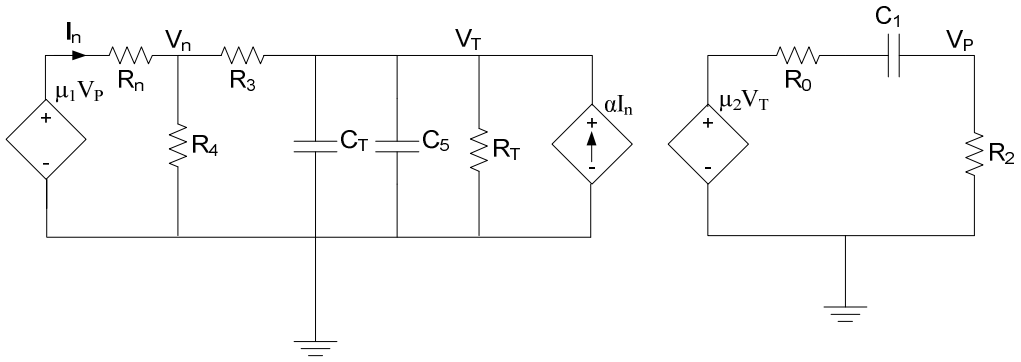


Figure 7.4 Simplified diagram of Figure 7.3

Figure 7.5 is the same circuit as with the voltage source replaced by a current source.

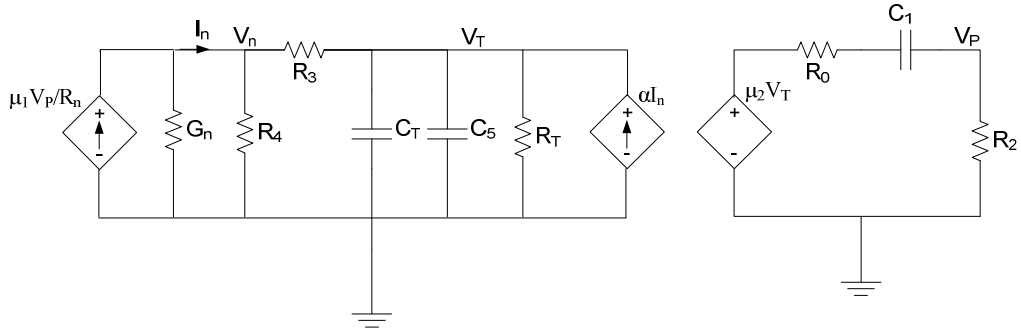


Figure 7.5 Modified diagram of Figure 7.4

$$I_n = \frac{\mu_1 V_P - V_n}{R_n} = G_n\left(\mu_1 V_P - V_n\right) \tag{7.6}$$

The node equation at node V_n is

$$\mu_1 G_n V_P = V_n\left(G_n + G_4\right) + \left(V_n - V_T\right)G_3 \tag{7.7}$$

$$\mu_1 G_n V_P = V_n\left(G_n + G_3 + G_4\right) - V_T G_3 \tag{7.8}$$

The node equation at node V_T is

$$\alpha I_n = V_T s\left(C_5 + C_T\right) + V_T G_T + G_3\left(V_T - V_n\right) \tag{7.9}$$

$$\alpha I_n = V_T\left[G_3 + G_T + s\left(C_5 + C_T\right)\right] - V_n G_3 \tag{7.10}$$

Writing in matrix form for equations (7.8) and (7.10)

$$\begin{bmatrix} G_n + G_3 + G_4 & -G_3 \\ -G_3 & G_3 + G_T + s\left(C_5 + C_T\right) \end{bmatrix} \begin{bmatrix} V_n \\ V_T \end{bmatrix} = \begin{bmatrix} \mu_1 G_n V_P \\ \alpha I_n \end{bmatrix} \tag{7.11}$$

For the right hand loop,

$$V_P = \mu_2 V_T \frac{sC_1G_0}{sC_1G_0 + sC_1G_2 + G_0G_2} \tag{7.12}$$

Putting V_P in equation (7.6)

$$I_n = \frac{sC_1\mu_1\mu_2G_0G_nV_T}{sC_1G_0 + sC_1G_2 + G_0G_2} - G_nV_n \tag{7.13}$$

Multiplying equation (7.12) by $\mu_1 G_n$, the equation becomes

$$\mu_1 G_n V_P = \mu_1\mu_2 V_T \frac{sC_1G_0G_n}{sC_1G_0 + sC_1G_2 + G_0G_2} \tag{7.14}$$

Multiplying equation (7.13) by α, the equation becomes

$$\alpha I_n = \frac{sC_1\alpha\mu_1\mu_2G_0G_nV_T}{sC_1G_0 + sC_1G_2 + G_0G_2} - \alpha G_nV_n \tag{7.15}$$

In matrix form equations (7.14) and (7.15) become

$$\begin{bmatrix} \mu_1 G_n V_P \\ \alpha I_n \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{sC_1\mu_1\mu_2G_0G_n}{sC_1G_0 + sC_1G_2 + G_0G_2} \\ -\alpha G_n & \dfrac{sC_1\alpha\mu_1\mu_2G_0G_n}{sC_1G_0 + sC_1G_2 + G_0G_2} \end{bmatrix} \begin{bmatrix} V_n \\ V_T \end{bmatrix} \tag{7.16}$$

From equation (7.11) and (7.16), the nodal-admittance matrix becomes

$$\left[Y_n(s)\right] = \begin{bmatrix} G_n + G_3 + G_4 & -\left(G_3 + \dfrac{sC_1\mu_1\mu_2G_0G_n}{sC_1G_0 + sC_1G_2 + G_0G_2}\right) \\ -\left(G_3 - \alpha G_n\right) & G_3 + G_T + s\left(C_5 + C_T\right) - \dfrac{sC_1\alpha\mu_1\mu_2G_0G_n}{sC_1G_0 + sC_1G_2 + G_0G_2} \end{bmatrix} \tag{7.17}$$

μ_1 is the coefficient for the input buffer, α is the coefficient for the current mirror, and μ_2 is the coefficient for the output buffer. The typical value for those parameters is one. If $\alpha = 1$, $\mu_1 = 1$, $\mu_2 = 1$ in equation (7.17), the nodal-admittance matrix becomes

$$[Y_n(s)] = \begin{bmatrix} G_n + G_3 + G_4 & -\left(G_3 + \dfrac{sC_1G_0G_n}{sC_1G_0 + sC_1G_2 + G_0G_2}\right) \\ -(G_3 - G_n) & G_3 + G_T + s(C_5 + C_T) - \dfrac{sC_1G_0G_n}{sC_1G_0 + sC_1G_2 + G_0G_2} \end{bmatrix} \tag{7.18}$$

The determinant of the NAM is

$$\begin{aligned} Det[Y_n(s)] = (G_n + G_3 + G_4)\{G_3 + G_T + s(C_5 + C_T) \\ - \frac{sC_1G_0G_n}{sC_1G_0 + sC_1G_2 + G_0G_2}\} \\ - (G_3 - G_n)\left(G_3 + \frac{sC_1G_0G_n}{sC_1G_0 + sC_1G_2 + G_0G_2}\right) \end{aligned} \tag{7.19}$$

$$\Delta(s) = \frac{N(s)}{D(s)} \tag{7.20}$$

Here

$$D(s) = (sC_1G_0 + sC_1G_2 + G_0G_2) \tag{7.21}$$

and

$$\begin{aligned} N(s) = (G_n + G_3 + G_4)[\{G_3 + G_T + s(C_5 + C_T)\}(sC_1G_0 + sC_1G_2 + G_0G_2) \\ - sC_1G_0G_n] - (G_3 - G_n)(sC_1G_0G_3 + sC_1G_2G_3 + G_0G_2G_3 + sC_1G_0G_n) \end{aligned} \tag{7.22}$$

$$\begin{aligned} N(s) = (G_n + G_3 + G_4)[s(C_1G_0 + C_1G_2)(G_3 + G_T) + s(C_5 + C_T)G_0G_2 \\ - sC_1G_0G_n + s^2(C_5 + C_T)(C_1G_0 + C_1G_2) + G_0G_2(G_3 + G_T)] \\ - (G_3 - G_n)[s(C_1G_0G_3 + C_1G_2G_3 + C_1G_0G_n) + G_0G_2G_3] \end{aligned} \tag{7.23}$$

$$\begin{aligned} N(s) &= s^2(C_5+C_T)(C_1G_0+C_1G_2)(G_n+G_3+G_4) \\ &+ s(G_n+G_3+G_4)\left[(C_1G_0+C_1G_2)(G_3+G_T)+(C_5+C_T)G_0G_2-C_1G_0G_n\right] \\ &+ s(G_n-G_3)(C_1G_0G_3+C_1G_2G_3+C_1G_0G_n) \\ &+ G_0G_2(G_n+G_3+G_4)(G_3+G_T)+G_0G_2G_3(G_n-G_3) \end{aligned} \tag{7.24}$$

$$\begin{aligned} N(s) &= s^2C_1(C_5+C_T)(G_0+G_2)(G_n+G_3+G_4) \\ &+ s(G_n+G_3+G_4)\left[C_1\{(G_0+G_2)(G_3+G_T)-G_0G_n\}+(C_5+C_T)G_0G_2\right] \\ &+ sC_1(G_n-G_3)(G_0G_3+G_2G_3+G_0G_n) \\ &+ G_0G_2\left[G_T(G_n+G_3+G_4)+G_3(2G_n+G_4)\right] \end{aligned} \tag{7.25}$$

If s = jω, N(s) becomes

$$\begin{aligned} N(\omega) &= -\omega^2C_1(C_5+C_T)(G_0+G_2)(G_n+G_3+G_4) \\ &+ j\omega(G_n+G_3+G_4)\left[C_1\{(G_0+G_2)(G_3+G_T)-G_0G_n\}+(C_5+C_T)G_0G_2\right] \\ &+ j\omega C_1(G_n-G_3)(G_0G_3+G_2G_3+G_0G_n) \\ &+ G_0G_2\left[G_T(G_n+G_3+G_4)+G_3(2G_n+G_4)\right] \end{aligned} \tag{7.26}$$

For oscillation to start, N(s) has to be zero. Thus, the real part is zero and imaginary part is zero. For the real part to be zero,

$$\begin{aligned} &-\omega^2C_1(C_5+C_T)(G_0+G_2)(G_n+G_3+G_4) \\ &+G_0G_2\left[G_T(G_n+G_3+G_4)+G_3(2G_n+G_4)\right]=0 \end{aligned} \tag{7.27}$$

Putting $\omega = 2\pi f_0$ in equation (7.27), the frequency of oscillation becomes

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{G_0G_2\left[G_T(G_n+G_3+G_4)+G_3(2G_n+G_4)\right]}{C_1(C_5+C_T)(G_0+G_2)(G_n+G_3+G_4)}} \tag{7.28}$$

The imaginary part of equation (7.26) is also zero,

$$\begin{aligned} &j\omega(G_n+G_3+G_4)\left[C_1\{(G_0+G_2)(G_3+G_T)-G_0G_n\}+(C_5+C_T)G_0G_2\right] \\ &+j\omega C_1(G_n-G_3)(G_0G_3+G_2G_3+G_0G_n)=0 \end{aligned} \tag{7.29}$$

The condition of oscillation becomes

$$\begin{aligned}&(G_n+G_3+G_4)[C_1\{(G_0+G_2)(G_3+G_T)-G_0G_n\}+(C_5+C_T)G_0G_2]\\&+C_1(G_n-G_3)(G_0G_3+G_2G_3+G_0G_n)=0\end{aligned} \tag{7.30}$$

7.5 Simulation Results

The calculated and simulated frequency of oscillation as a function of C_1 is shown in Figure 7.6. Here R_2, R_3, R_4, and C_5 values are kept constant. These values are R_2 = 5 kΩ, R_3 = 3 kΩ, R_4 = 800 Ω, and C_5 = 5 pF. The frequency of oscillation is 23.93 MHz by calculation and 23.94 MHz by simulation when C_1 is 1 pF. The frequency of oscillation is 13.82 MHz by calculation and 13.13 MHz by simulation when C_1 is 3 pF. The maximum difference between calculation and simulation is 5% over range for C_1 of 1 to 3 pF.

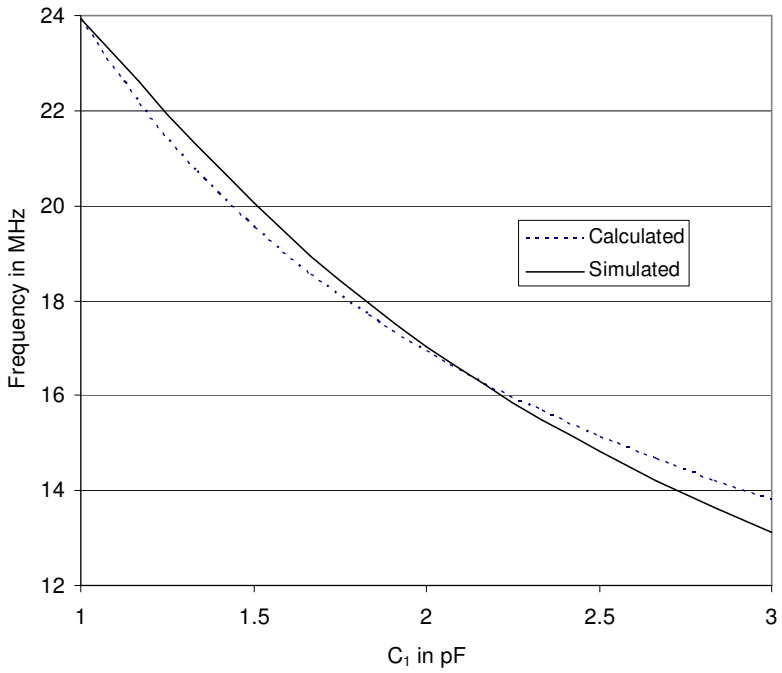


Figure 7.6 Frequency of oscillation versus C_1 for sinusoidal waveform

The calculated and simulated frequency of oscillation as a function of R_2 is shown in Figure 7.7. Here C_1, R_3, R_4, and C_5 values are kept constant. These values are C_1 = 2 pF, R_3 = 3 kΩ, R_4 = 800 Ω, and C_5 = 5 pF. The frequency of oscillation is 23.04 MHz by calculation and 24.57 MHz by simulation when R_2 is 2.5 kΩ. The frequency of oscillation is 16.92 MHz by calculation and 17.04 MHz by simulation when R_2 is 5 kΩ. The maximum difference between calculation and simulation is 6.6% over range for R_2 of 2.5 to 5 kΩ.

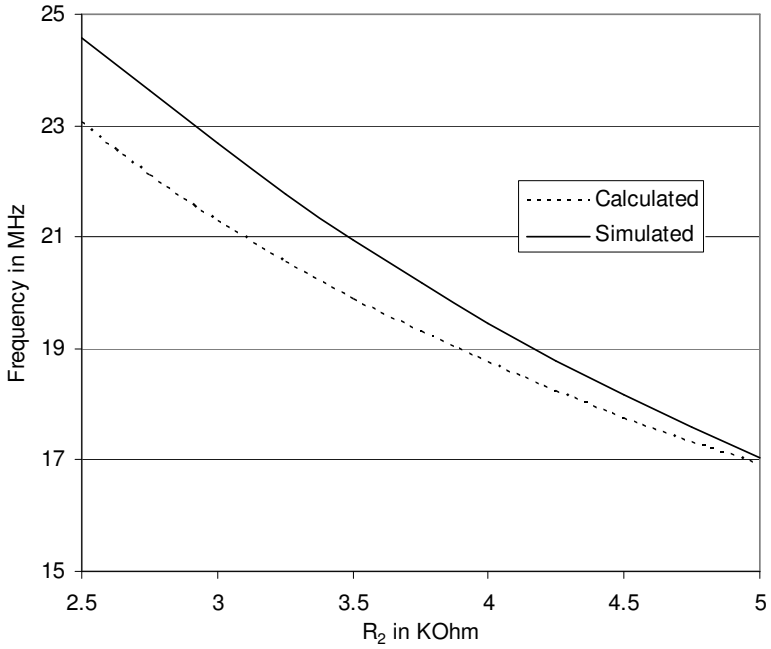


Figure 7.7 Frequency of oscillation versus R_2 for sinusoidal waveform

The calculated and simulated frequency of oscillation as a function of R_3 is shown in Figure 7.8. Here C_1, R_2, R_4, and C_5 values are kept constant. These values are C_1 = 2 pF, R_2 = 5 kΩ, R_4 = 800 Ω, and C_5 = 5 pF. The frequency of oscillation is 28.91

MHz by calculation and 24.7 MHz by simulation when R_3 is 1 kΩ. The frequency of oscillation is 13.15 MHz by calculation and 13.91 MHz by simulation when R_3 is 5 kΩ. The maximum difference between calculation and simulation is 5.8% over range for R_1 of 1 to 5 kΩ.

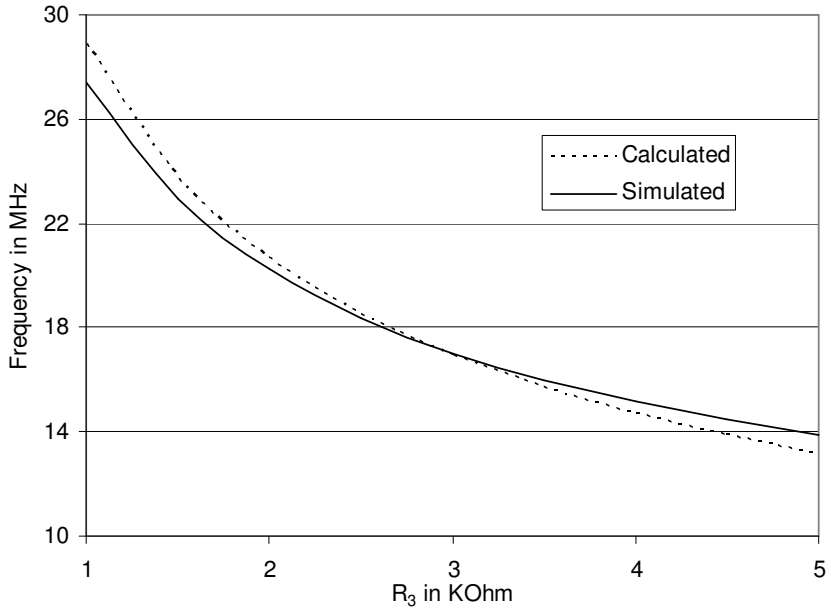


Figure 7.8 Frequency of oscillation versus R_3 for sinusoidal waveform

The calculated and simulated frequency of oscillation as a function of R_4 is shown in Figure 7.9. Here C_1, R_2, R_3, and C_5 values are kept constant. These values are C_1 = 2 pF, R_2 = 5 kΩ, R_3 = 3 kΩ, and C_5 = 5 pF. The frequency of oscillation is 16.89 MHz by calculation and 16.74 MHz by simulation when R_4 is 700 Ω. The frequency of oscillation is 17.02 MHz by calculation and 17.43 MHz by simulation when R_4 is 1.1 kΩ. The maximum difference between calculation and simulation is 2.4% over range for R_4 of 0.7 to 1.1 kΩ.

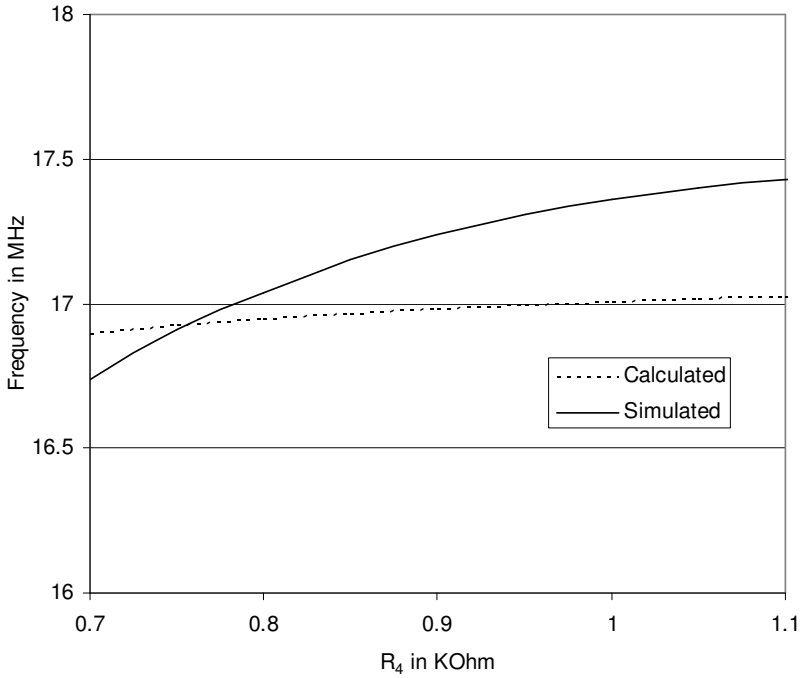


Figure 7.9 Frequency of oscillation versus R_4 for sinusoidal waveform

The calculated and simulated frequency of oscillation as a function of C_5 is shown in Figure 7.10. Here C_1, R_2, R_3, and R_4 values are kept constant. These values are C_1 = 2 pF, R_2 = 5 kΩ, R_3 = 3 kΩ, and R_4 = 800 Ω. The frequency of oscillation is 16.92 MHz by calculation and 17.04 MHz by simulation when C_5 is 5 pF. The frequency of oscillation is 12.09 MHz by calculation and 12.67 MHz by simulation when C_5 is 10 pF. The maximum difference between calculation and simulation is 4.8% over range for C_5 of 5 to 10 pF.

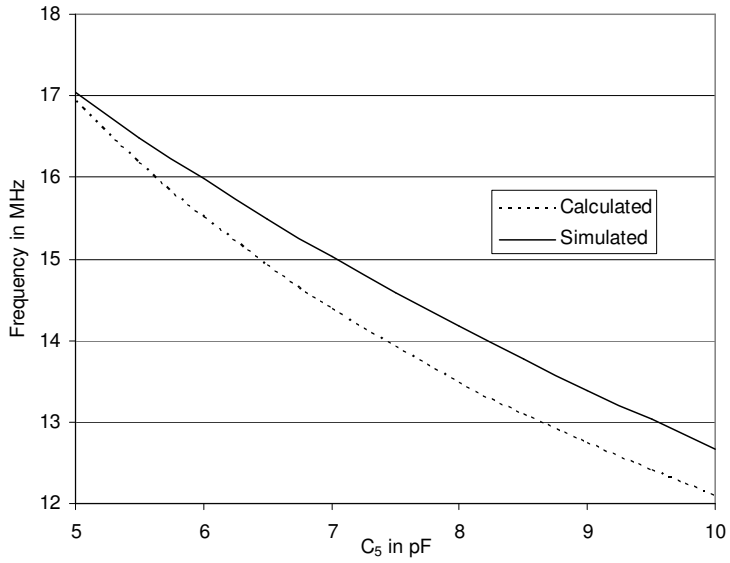


Figure 7.10 Frequency of oscillation versus C_5 for sinusoidal waveform

The simulated sinusoidal waveform is shown in Figure 7.11. Here C_1 = 1 pF, R_2 = 5 kΩ, R_3 = 3 kΩ, R_4 = 800 Ω, and C_5 = 5 pF. The simulated frequency of oscillation for the full model is 23.94 MHz.

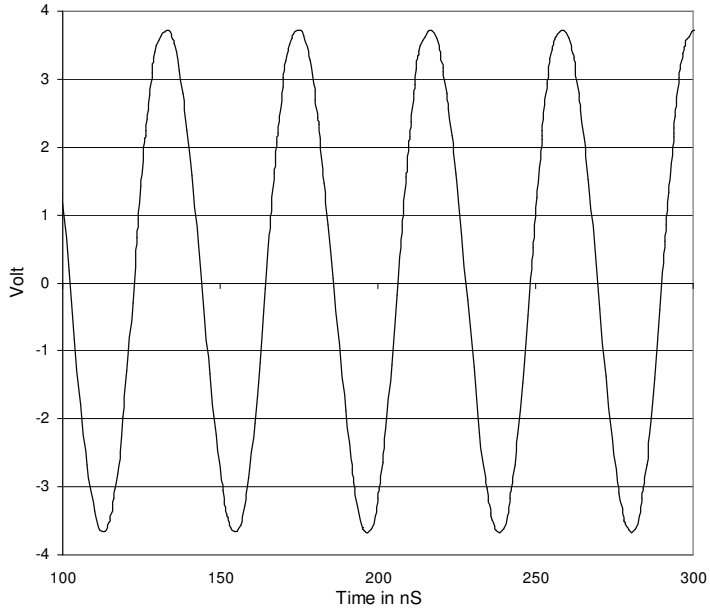


Figure 7.11 Simulated sinusoidal waveform

Figure 7.12 shows the harmonic components of a sinusoidal waveform. The difference between the fundamental and second harmonic which is the highest among higher harmonics, is 26.8 dB.

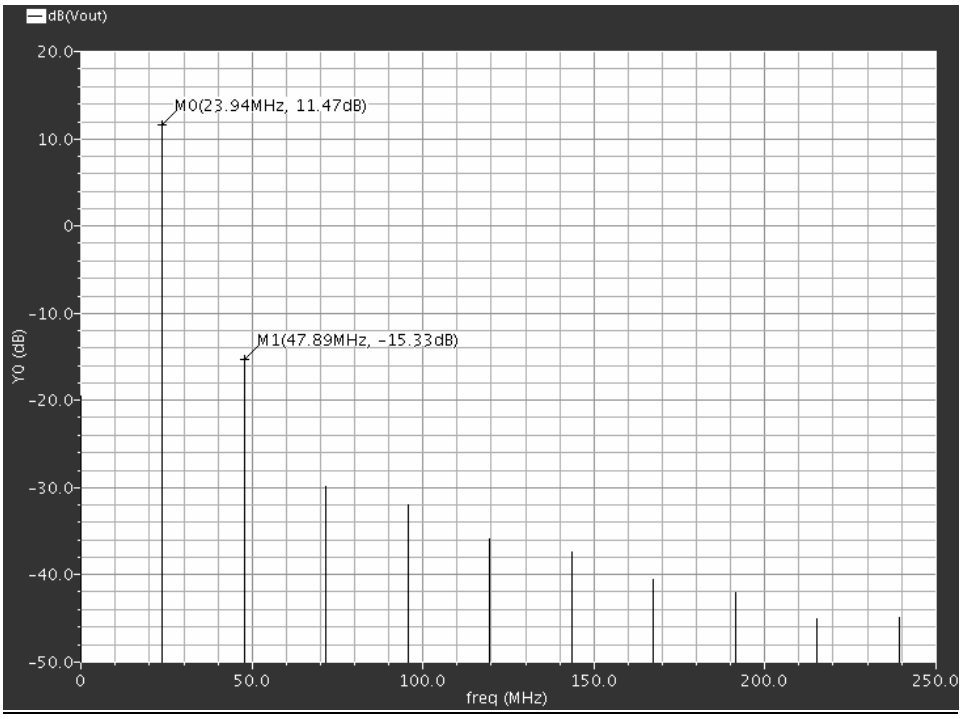


Figure 7.12 Harmonic components of sinusoidal waveform

7.6 Summary

A pure sine wave has only the fundamental and all other harmonics are zero, so, the THD = 0%. For oscillation to start, the loop gain has to be one or greater than one, and the phase shift is 180°. These conditions are necessary but not sufficient. A sinusoidal oscillator using a current feedback operational amplifier was developed. The equations for the frequency of oscillation and the condition of oscillation were derived. The reason for using a CFOA is that it gets higher frequency of oscillation compared to the voltage feedback operational amplifier. The simulated sinusoidal waveform and its

harmonic components were shown. Finally, the calculated and simulated frequency of oscillation of the proposed sinusoidal oscillator as a function of C_1, R_2, R_3, R_4, and C_5 were compared one variable at a time was varied and the other variables were held constant. The maximum deviation from the calculated frequency of oscillation to the simulated frequency of oscillation was 6.6%.

Table 7.1 Sinusoidal Oscillator Summary Table

Variable	Range	Calculated frequency range in MHz	Simulated frequency range in MHz	% of Maximum error between calculation and simulation
C_1	1 pF to 3 pF	13.82 - 23.93	13.13 - 23.94	5%
R_2	2.5 kΩ to 5 kΩ	16.92 - 23.04	17.04 - 24.57	6.6%
R_3	1 kΩ to 5 kΩ	13.14 - 28.90	13.91 - 27.40	5.8%
R_4	0.7 kΩ to 1.1 kΩ	16.89 - 17.02	16.74 - 17.43	2.4%
C_5	5 pF to 10 pF	12.09 - 16.92	12.67 - 17.04	4.8%

CHAPTER 8

TRIANGULAR AND RECTANGULAR WAVE GENERATOR USING CURRENT FEEDBACK OPERATIONAL AMPLIFIERS

8.1 Multivibrators

Multivibrators are often used to generate triangular, square, or pulse waves. There are three types of Multivibrators: bistable, monostable and astable. A bistable multivibrator has two stable states. Circuits can stay in either stable state indefinitely. External commands are necessary to change the circuit from one state to the other state. An astable multivibrator toggles periodically from one state to another state without any external command. The timing is set by a suitable circuit usually a capacitor or quartz crystal [29]. A monostable multivibrator has only one stable state. A trigger signal is necessary to force output to the other unstable state. After the circuit stays in the unstable state for a fixed time, the circuit returns to the stable state. A delay is set by a suitable circuit.

8.1.1 Bistable Multivibrators

One of the simplest bistable multivibrators is the comparator [46]. A bistable multivibrator can be made by connecting an amplifier in the positive feedback configuration. In this case the loop gain is greater than unity. The circuit with the positive feedback configuration is shown in Figure 8.1 [30].

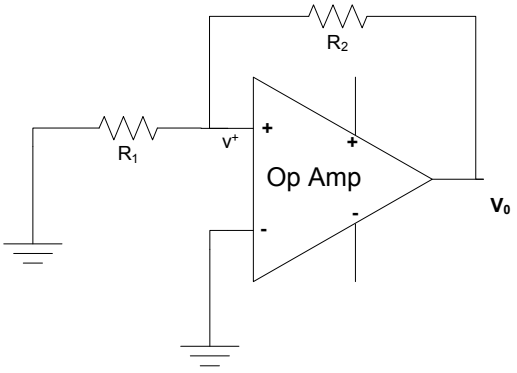


Figure 8.1 A positive feedback loop capable of bistable operation

The operation of this circuit is explained below. This circuit has no external excitation. Assume a small electrical noise causes the positive input terminal to increase v^+ voltage. This signal is amplified by the amplifier. Let the open loop gain of the amplifier be A, which is a very large number. Thus the output voltage, V_0, would be much greater than v^+. The voltage divider will feed $V_0R_1/(R_1+R_2)$ to the positive input terminal of the amplifier. This voltage is amplified by the amplifier again. This regenerative process continues until the op amp saturates and the output voltage reaches the positive rail. Let the positive rail voltage be V_{sat}^+. At this time the voltage at the positive input terminal is $V_{sat}^+R_1/(R_1+R_2)$. This is positive and keeps the op amp at positive saturation. This is one of the stable states for this circuit. A negative rail output voltage can be explained by similar ways. Let the negative rail voltage be V_{sat}^-. This is the other stable state. This circuit has two stable states. This circuit can exist at one of the two states indefinitely, but can not stay at the $V_0 = 0$ state. Any disturbance, such as noise can cause the circuit to switch to any of the two stable states. The $V_0 = 0$ state is called the metastable state [30].

8.1.2 Transfer Characteristics of a Bistable Circuit

For this circuit, there are two terminals connected to the ground. Either of the two terminals can serve as an input terminal. Figure 8.2 shows a bistable circuit where the input voltage, V_{in}, is connected to the negative input terminal. To derive the V_0 to V_{in} transfer characteristic, let V_0 be at one of the two possible levels, say V_{sat}^+.

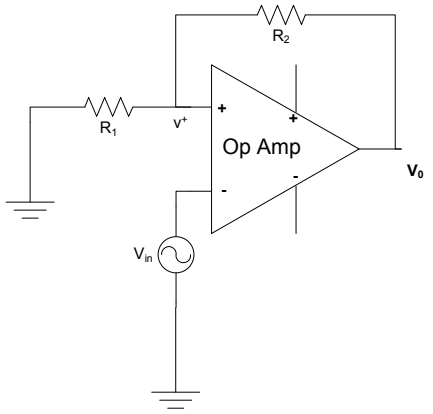


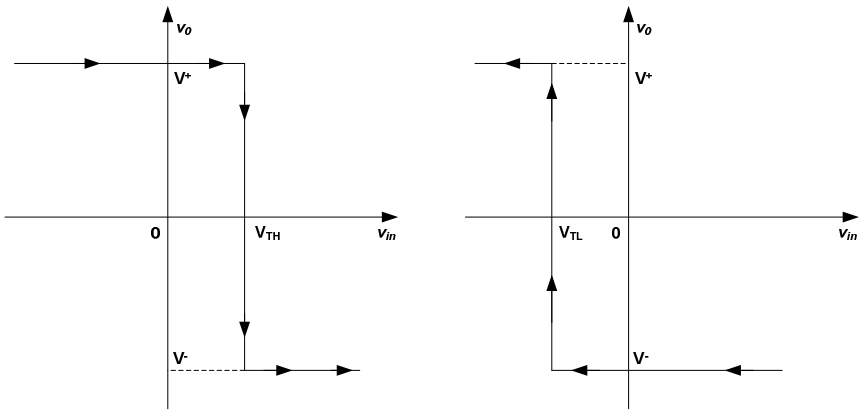
Figure 8.2 A bistable circuit where input voltage V_{in} is connected in negative input terminal

Thus the voltage at the positive input terminal of the Op Amp is

$$v^+ = \frac{R_1}{R_1 + R_2} V_{sat}^+ \tag{8.1}$$

Let, V_{in} increase from zero voltage. V_0 will stay constant at V_{sat}^+ until $V_{in} = v^+$. As V_{in} begins to increase v^+, a net negative value develops between the two input terminals of the op amp. This voltage is amplified by the amplifier. Thus V_0 goes negative. The voltage divider will feed $V_0R_1/(R_1+R_2)$ voltage to the positive input terminal of the Op Amp. Here V_0 is negative. So, v^+ goes to negative. This increases the net negative voltage at the input terminal of the op amp. The net negative input amplified by the op

amp again and this process will continue until the V_0 reaches the negative rail. If this voltage is V_{sat}^-, then any further increase of V_{in} has no effect on V_0. Figure 8.3 (a) shows the input-output characteristics for increasing V_{in}.



(a) (b)

Figure 8.3 (a) $V_{in} - V_0$ characteristics for increasing V_{in}, (b) $V_{in} - V_0$ characteristics for decreasing V_{in}

Now consider V_{in} is decreasing. The positive input terminal voltage of the op amp is

$$v^+ = \frac{R_1}{R_1 + R_2} V_{sat}^- \tag{8.2}$$

The output for the op amp will stay at negative saturation until V_{in} is equal to V_{sat}^- .$R_1/(R_1+R_2)$. If V_{in} goes below this value, a net positive voltage appears between the op amp input terminals. This voltage is amplified by the amplifier. Thus V_0 goes positive. The voltage divider will feed back $V_0R_1/(R_1+R_2)$ to the positive input terminal of the Op Amp. Here V_0 is positive. So, v^+ goes to a positive value. This increases the net positive voltage at the input terminal of the op amp. The input terminal voltage will be amplified

by the op amp again, and this process will continue until V_0 reaches the positive rail. Any further increase of V_{in} has no effect on V_0. Figure 8.3 (b) shows the input output characteristics for decreasing V_{in}. The complete $V_{in} - V_0$ characteristic for the circuit is shown in Figure 8.4.

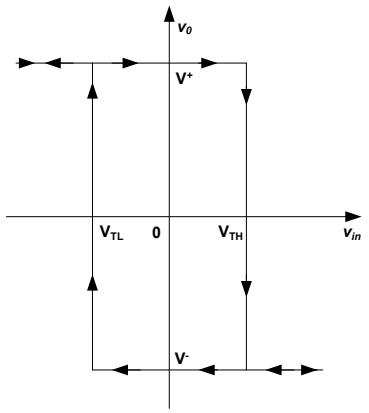
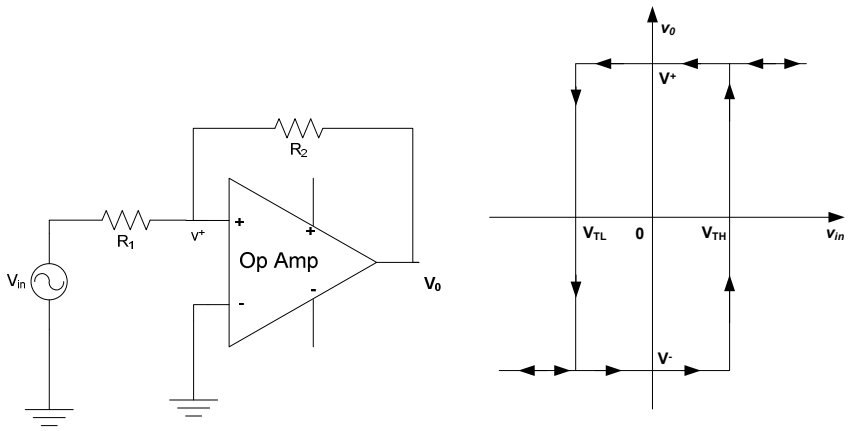


Figure 8.4 Complete $V_{in} - V_0$ characteristic

The circuit changes states at different values of V_{in} for increasing or decreasing V_{in}. It is said that the circuit has hysteresis [30]. The width of the hysteresis is the difference between the high threshold (V_{TH}) and the low threshold (V_{TL}). The bistable circuit changes from the positive state to the negative state for increasing V_{in}. The circuit is an inverting bistable circuit. This bistable circuit is also known as a Schmitt trigger [30].

A noninverting bistable circuit and its transfer characteristics are shown in Figure 8.5. The circuit operation can be explained in similar ways as above.



(a) (b)

Figure 8.5 (a) Noninverting bistable circuit, (b) $V_{in} - V_0$ characteristic for noninverting bistable circuit

Some applications for bistable circuits are comparator, digital memory system, and square wave generator.

8.2 Integrator

Integrators are commonly used in signal generators. An integrator can be made by putting a capacitor in the feedback path and a resistor at the inverting input of an op amp. This circuit performs the mathematical operation of integration. The integrator circuit is shown in Figure 8.6. [46]. Assuming that the op amp is operating in the linear region.

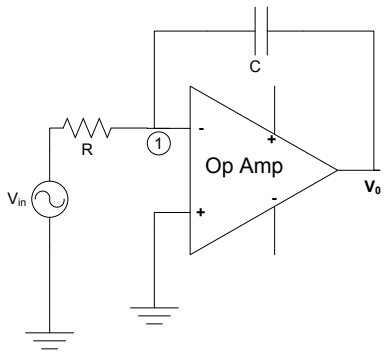


Figure 8.6 Integrator

Nodal analysis at node 1 gives,

$$0 = \frac{V_{in} - V_1}{R} + C\frac{d}{dt}(V_0 - V_1) \tag{8.3}$$

Since $V_1 = 0$ the virtual ground, equation (8.3) becomes

$$0 = \frac{V_{in} - V_1}{R} + C\frac{dV_0}{dt} \tag{8.4}$$

Solving for V_0 from equation (8.4)

$$V_0 = -\frac{1}{RC}\int V_{in}dt \tag{8.5}$$

This equation shows the output voltage of the circuit is a product of the integration of the inverting input signal and the reciprocal of the RC time constant. There is a negative sign at the output voltage. Thus, this circuit is said to be an inverting integrator. This is also known as a Miller integrator.

The operation of the integrator circuit can be described in the frequency domain. Here $Z_1(s) = R$ and $Z_2(s) = 1/sC$. So the transfer function is

$$H(s) = \frac{V_0(s)}{V_{in}(s)} = -\frac{Z_2(s)}{Z_1(s)} = -\frac{1}{sCR} \tag{8.6}$$

This transfer function has a pole at the origin. Let s = jω,

Equation (8.6) can be rewritten as

$$H(j\omega) = -\frac{1}{j\omega/\omega_0} = \frac{1}{\omega/\omega_0}\angle +90^\circ \tag{8.7}$$

where $\omega_0 = \frac{1}{RC}$. The Bode plot for this circuit is shown in Figure 8.7.

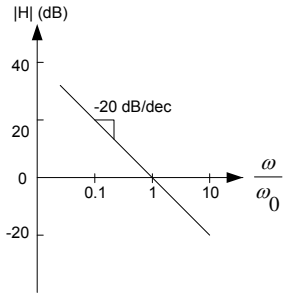


Figure 8.7 Magnitude Bode plot for integrator

It is a straight line with a slope of -20 dB/dec, where $\omega = \omega_0$ is the unity gain frequency. The circuit introduces a 90° phase lead between V_{in} and V_0. This integrator has extremely high gain at low frequencies. So the circuit is seldom used alone, because it tends to saturate [29]. The integrator is usually placed inside a control loop to keep the circuit in the linear region.

8.3 Generation of Triangular and Rectangular Waveform

The schematic diagram for the generation of triangular and rectangular waveforms is shown in Figure 8.8 [30]. Here an integrator and a bistable circuit are used. The integrator charges or discharges a capacitor in a linear way. Thus, the integrator produces a triangular waveform. Because the inverter is inverting, a bistable circuit is necessary which is stable in both positive and negative polarity. A non-inverting type of

bistable circuit is necessary. The output of the integrator is a triangular wave and the output of the bistable circuit is a rectangular wave.

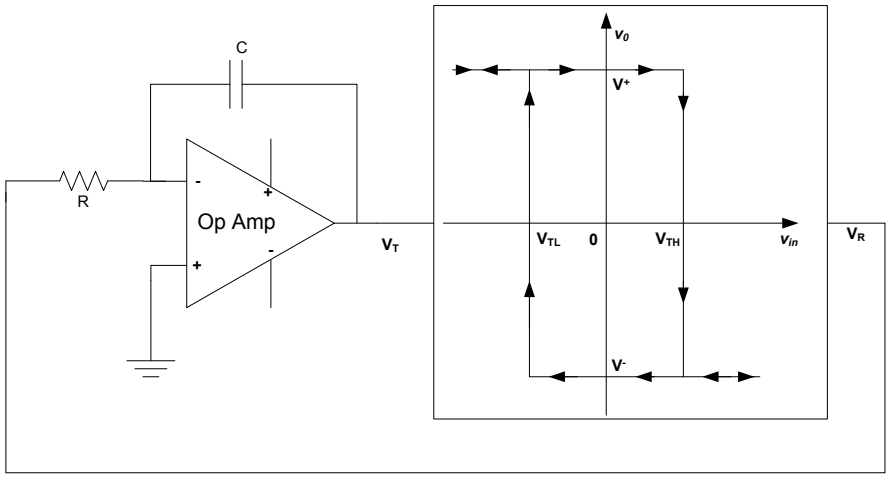


Figure 8.8 General schematic diagram for generating triangular and rectangular wave

Let the output of the bistable circuit be V_{sat}^+. A current equal to V_{sat}^+/R will flow into the resistor R and through capacitor C. So the output of the integrator will decrease linearly at a slope of $-V_{sat}^+/RC$. This decrease will continue until the output of the integrator reaches the lower threshold, V_{TL}, of the bistable circuit. At this point the bistable circuit will change its state and the output of the bistable circuit will become V_{sat}^-. Now current flowing through R and C will change direction. The magnitude of the current is $|V_{sat}^-|/R$. So the integrator output will start to increase linearly at a slope of $|V_{sat}^-|/RC$. This process will continue until the output of the integrator reaches the higher threshold, V_{TH}, of the bistable circuit. At this point the bistable circuit will change its

state and the output of the bistable circuit will become V_{sat}^{+}. The current into the integrator changes its direction and this process continues.

8.4 Integrator Circuit with Current Feedback Operational Amplifier

The integrator realization with the CFOA is shown in Figure 8.9. The transfer

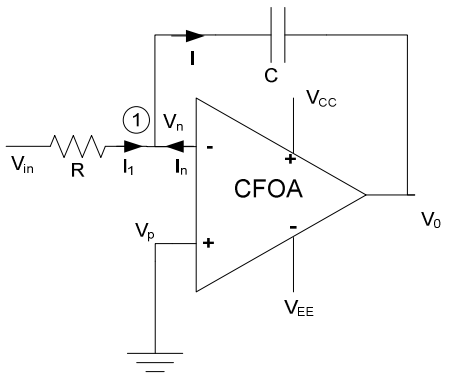


Figure 8.9 CFOA integrator

function for this circuit is to be found. Here the positive terminal for the CFOA is grounded. Thus

$$V_n = V_p = 0 \tag{8.8}$$

Here I_n is the input current for inverting input terminal of the CFOA. Using node analysis at node 1,

$$I_n + \frac{V_{in} - V_n}{R} = sC\left(V_n - V_0\right) \tag{8.9}$$

$$I_n = V_n\left(sC + \frac{1}{R}\right) - sCV_0 - \frac{V_{in}}{R} \tag{8.10}$$

Using the CFOA macro-model of Figure 4.1, V_0 is

$$V_0 = Z_T I_n \tag{8.11}$$

By combining equation (8.10) and (8.11), the resultant equation is

$$V_0 = Z_T V_n\left(sC + \frac{1}{R}\right) - sZ_T C V_0 - \frac{V_{in} Z_T}{R} \tag{8.12}$$

$$V_0\left(1 + sZ_T C\right) = -\frac{V_{in} Z_T}{R} \tag{8.13}$$

Thus the transfer function is

$$H(s) = \frac{V_0}{V_{in}} = -\frac{\frac{Z_T}{R}}{\left(1 + sZ_T C\right)} \tag{8.14}$$

The calculated transfer function and simulated full model CFOA integrator transfer function is shown in Figure 8.10. Here the two plots match at low frequencies with slightly increasing error at high frequencies.

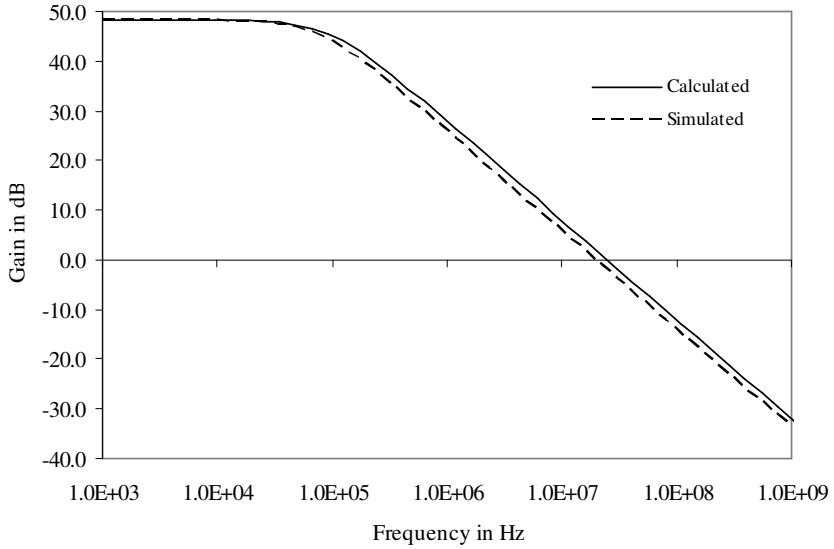


Figure 8.10 Transfer function for CFOA integrator

8.5 Triangular and Rectangular Wave Generator Using Two CFOAs

The triangular and rectangular wave generator circuit is shown in Fig. 8.11. The triangular wave can be generated by alternately charging and discharging a capacitor with a constant current. For this circuit, current drive for the capacitor C_1 is provided by the $CFOA_1$. In the second circuit, $CFOA_2$, is configured as a Schmitt trigger. Here, the diode clamp is used to stabilize the Schmitt trigger output level at $\pm nV_{D(on)}$, where n is the number of diodes and $V_{D(on)}$ is the forward voltage drop for each diode. Without the diode clamp the Schmitt trigger output would be at the ± of the maximum output voltage of the CFOA.

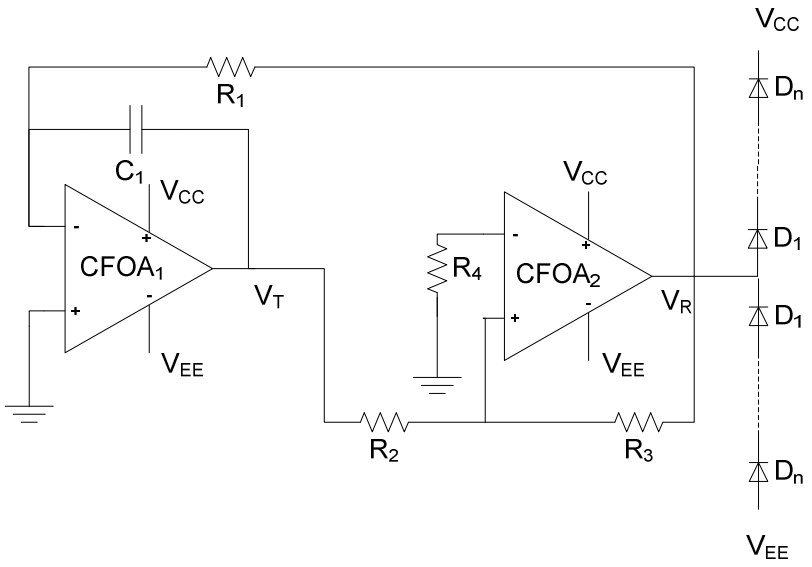


Figure 8.11 Triangular and rectangular wave generator

The frequency of oscillation of this circuit can be found by the following process. The integrator with capacitor in the feedback path and resistor in the inverting input terminal with branch currents are shown in the Figure 8.9. The upward ramping

voltage for the integrator is shown in Figure 8.12. The time required to charge the capacitor by a voltage ΔV is Δt.

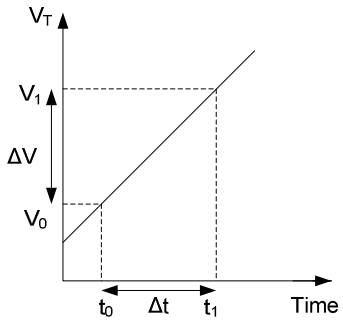


Figure 8.12 Upward ramping voltage for the integrator

So

$$C_1 \Delta V = I \Delta t \tag{8.15}$$

Rearranging equation (8.15) for Δt,

$$\Delta t = \frac{C_1}{I} \Delta V \tag{8.16}$$

The currents at node 1 of Figure 8.9 is,

$$I = I_1 + I_n \tag{8.17}$$

Using the macro-model for the CFOA in the integrator,

$$I_n = -\frac{V_T}{Z_T} \tag{8.18}$$

Here Z_T is the open loop transimpedance for the CFOA.

$$I = \frac{V_R}{R_1} - \frac{V_T}{Z_T} \tag{8.19}$$

The Schmitt Trigger circuit is shown if Figure 8.13.

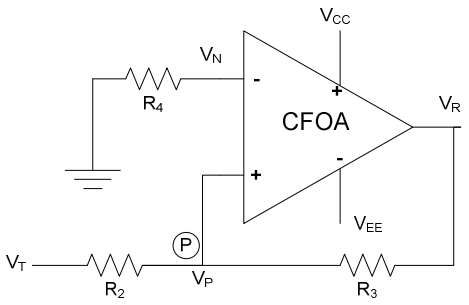


Figure 8.13 Schmitt trigger

Using the node equation at node P,

$$\frac{V_T - V_P}{R_2} = \frac{V_P - V_R}{R_3} \tag{8.20}$$

Rearranging equation (8.20) for V_T

$$V_T = V_P\left(1 + \frac{R_2}{R_3}\right) - V_R\frac{R_2}{R_3} \tag{8.21}$$

A sample triangular waveform is shown in Figure 8.14.

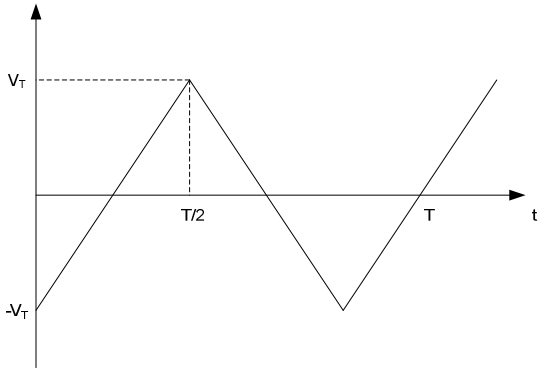


Figure 8.14 Triangular waveform

The time taken to ramp from $-V_T$ to V_T is T/2. So

$$\Delta t = \frac{T}{2} \tag{8.22}$$

Here ΔV is the voltage swing for the triangular waveform. Thus

$$\Delta V = 2V_T \tag{8.23}$$

From equation (8.16) and (8.21),

$$\frac{T}{2} = \frac{C_1}{I}\Delta V \tag{8.24}$$

$$\frac{T}{2} = \frac{C_1}{I}2V_T \tag{8.25}$$

$$T = \frac{4C_1}{I}V_T \tag{8.26}$$

$$T = \frac{4C_1\left[V_P\left(1+\frac{R_2}{R_3}\right)-V_R\frac{R_2}{R_3}\right]}{\frac{V_R}{R_1}-\frac{V_T}{Z_T}} \tag{8.27}$$

The period of the triangular, V_T, or rectangular, V_R, waveform is

$$T = \frac{4C_1\left[V_P\left(1+\frac{R_2}{R_3}\right)-V_R\frac{R_2}{R_3}\right]}{\frac{V_R}{R_1}-\frac{V_P}{Z_T}\left(1+\frac{R_2}{R_3}\right)+V_R\frac{R_2}{R_3Z_T}} \tag{8.28}$$

The frequency of oscillation for the triangular and rectangular waveform is

$$f_0 = \frac{\frac{V_R}{R_1}-\frac{V_P}{Z_T}\left(1+\frac{R_2}{R_3}\right)+V_R\frac{R_2}{R_3Z_T}}{4C_1\left[V_P\left(1+\frac{R_2}{R_3}\right)-V_R\frac{R_2}{R_3}\right]} \tag{8.29}$$

For the Schmitt trigger,

$$V_P = V_N \tag{8.30}$$

Thus the frequency of oscillation for the triangular and rectangular waveform becomes

$$f_0 = \frac{\frac{V_R}{R_1} - \frac{V_N}{Z_T}\left(1 + \frac{R_2}{R_3}\right) + V_R \frac{R_2}{R_3 Z_T}}{4C_1\left[V_N\left(1 + \frac{R_2}{R_3}\right) - V_R \frac{R_2}{R_3}\right]} \tag{8.31}$$

8.6 Simulation Results

The frequency of oscillation for the triangular and rectangular waveform is given in equation (8.31).

Here

V_R = Peak voltage of the square waveform

V_N = Peak voltage at the negative input terminal of the $CFOA_2$

Z_T = Open loop transimpedance of the $CFOA_1$

But the open loop transimpedance of the $CFOA_1$ varies when the frequency changes by 50 KHz. To verify equation (8.31), it is easier to calculate the open loop transimpedance and match this with the simulated open loop transimpedance of the CFOA. Rearranging equation (8.31), the resultant equation is

$$\frac{V_R}{R_1} + V_R \frac{R_2}{R_3 Z_T} - \frac{V_N}{Z_T}\left(1 + \frac{R_2}{R_3}\right) = 4C_1 f_0\left[V_N\left(1 + \frac{R_2}{R_3}\right) - V_R \frac{R_2}{R_3}\right] \tag{8.32}$$

$$\frac{1}{Z_T}\left[V_R \frac{R_2}{R_3} - V_N\left(1 + \frac{R_2}{R_3}\right)\right] = 4C_1 f_0\left[V_N\left(1 + \frac{R_2}{R_3}\right) - V_R \frac{R_2}{R_3}\right] - \frac{V_R}{R_1} \tag{8.33}$$

$$Z_T = \frac{V_N\left(1+\frac{R_2}{R_3}\right) - V_R\frac{R_2}{R_3}}{\frac{V_R}{R_1} - 4C_1 f_0\left[V_N\left(1+\frac{R_2}{R_3}\right) - V_R\frac{R_2}{R_3}\right]} \tag{8.34}$$

Figure 8.15 shows the calculated and simulated open loop transimpedance as a function of R_1. Here R_2 is 1.1 kΩ, R_3 is 3 kΩ and C_1 is 600 fF. The values of R_2, R_3, and C_1 are chosen so that the output voltage is stable. In this case, no diode clamp was used at the rectangular waveform output. Figure 8.15 also shows the frequency of oscillation versus R_1. The frequency of oscillation was found to be 6.78 MHz to 59.5 MHz. For R_1 = 100 kΩ, the frequency of oscillation is 6.78 MHz and for R_1 = 6 kΩ, the frequency of oscillation is 59.5 MHz.

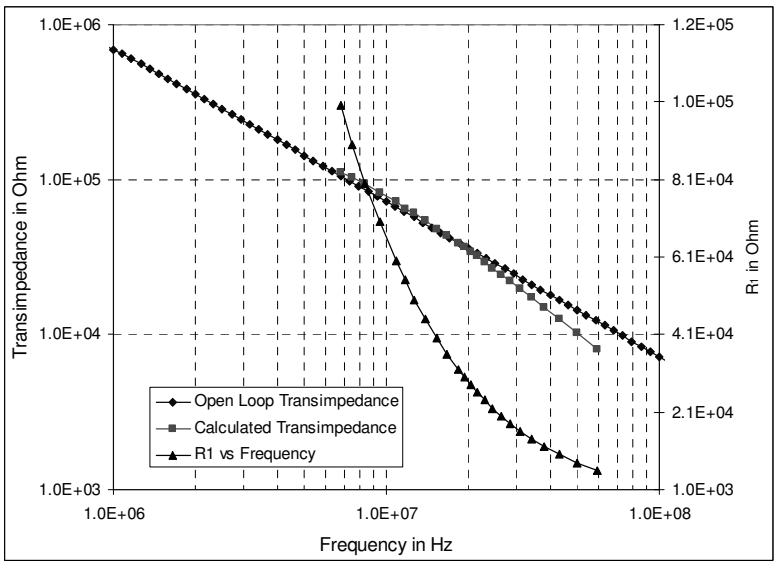


Figure 8.15 Transimpedance and R_1 versus frequency of oscillation for triangular and rectangular wave

Figure 8.16 shows the calculated and simulated open loop transimpedance as a function of R_1. Here R_2 is 1.1 kΩ, R_3 is 3 kΩ and C_1 is 600 fF. In this case, the diode clamp was used at the rectangular waveform output.

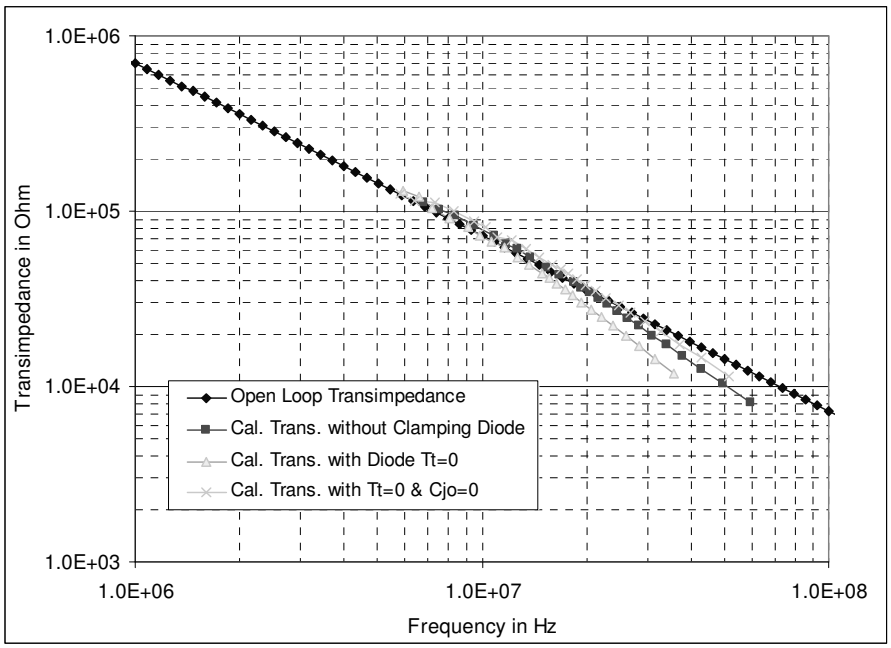


Figure 8.16 Calculated and simulated transimpedance with changing R_1 versus frequency of oscillation for triangular and rectangular wave

Figure 8.17 shows the calculated and simulated open loop transimpedance as a function of R_2. Here R_1 is 22 kΩ, R_3 is 3 kΩ and C_1 is 600 fF. In this case, no diode clamp was used at the rectangular waveform output. Figure 17 also shows the frequency of oscillation versus R_2. The frequency of oscillation was found to be 12.9 MHz to 37.7 MHz. For R_2 = 2.6 kΩ, the frequency of oscillation is 12.9 MHz and for R_2 = 500 Ω, the frequency of oscillation is 37.7 MHz.

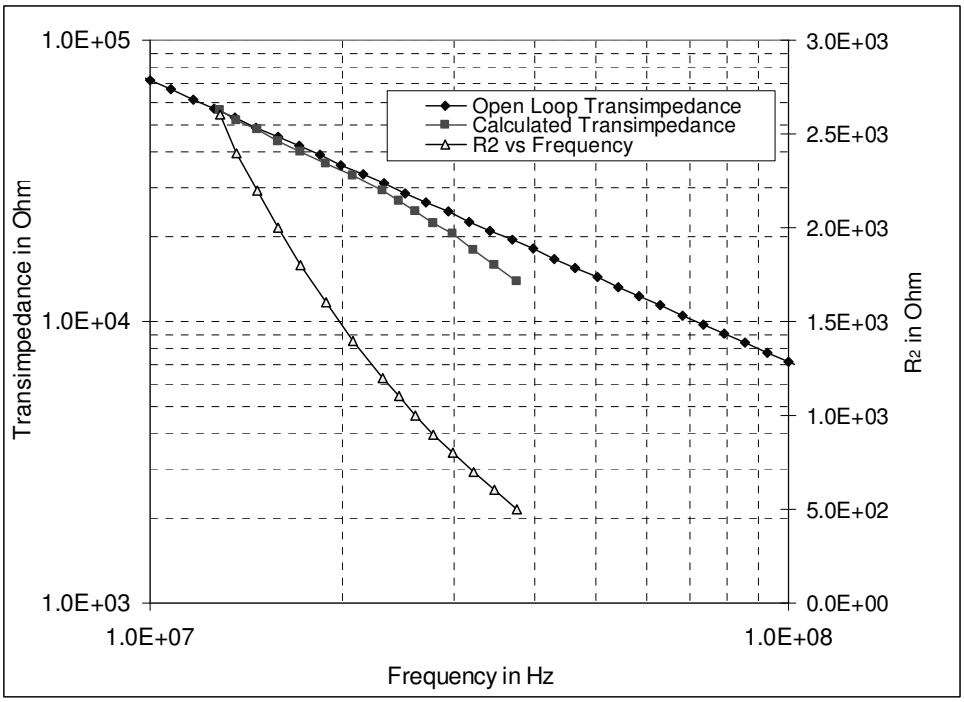


Figure 8.17 Transimpedance and R_2 versus frequency of oscillation for triangular and rectangular wave

Figure 8.18 shows the calculated and simulated open loop transimpedance as a function of R_2. Here R_1 is 22 kΩ, R_3 is 3 kΩ and C_1 is 600 fF. In this case, the diode clamp was used at the rectangular waveform output.

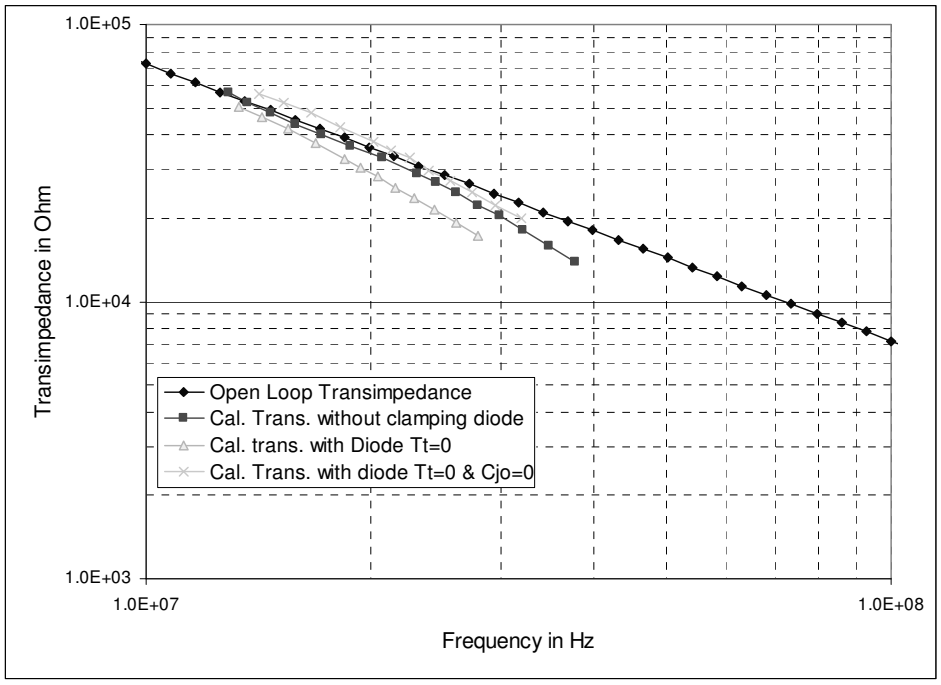


Figure 8.18 Calculated and simulated transimpedance with changing R_2 versus frequency of oscillation for triangular and rectangular wave

Figure 8.19 shows the calculated and simulated open loop transimpedance as a function of R_3. Here R_1 is 22 kΩ, R_2 is 1.1 kΩ and C_1 is 600 fF. In this case, no diode clamp was used at the rectangular waveform output. Figure 19 also shows the frequency of oscillation versus R_3. The frequency of oscillation was found to be 14.8 MHz to 24.5 MHz. For R_3 = 1.5 kΩ, the frequency of oscillation is 14.8 MHz and for R_3 = 3 kΩ, the frequency of oscillation is 24.5 MHz.

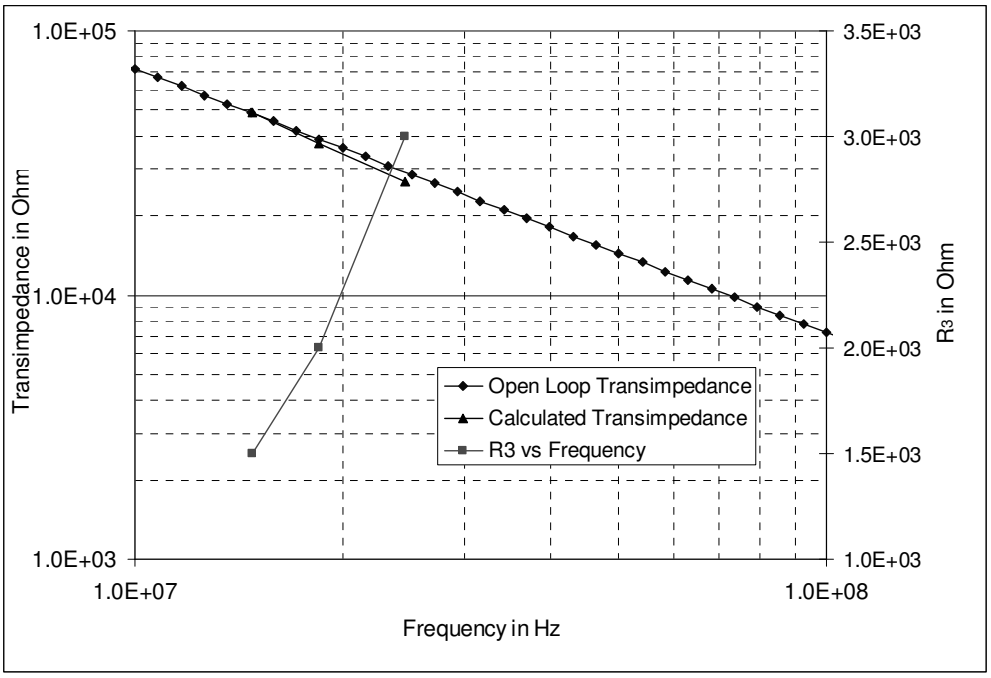


Figure 8.19 Transimpedance and R_3 versus frequency of oscillation for triangular and rectangular wave

Figure 8.20 shows the calculated and simulated open loop transimpedance as a function of R_3. Here R_1 is 22 kΩ, R_2 is 1.1 kΩ and C_1 is 600 fF. In this case, the diode clamp was used at the rectangular waveform output.

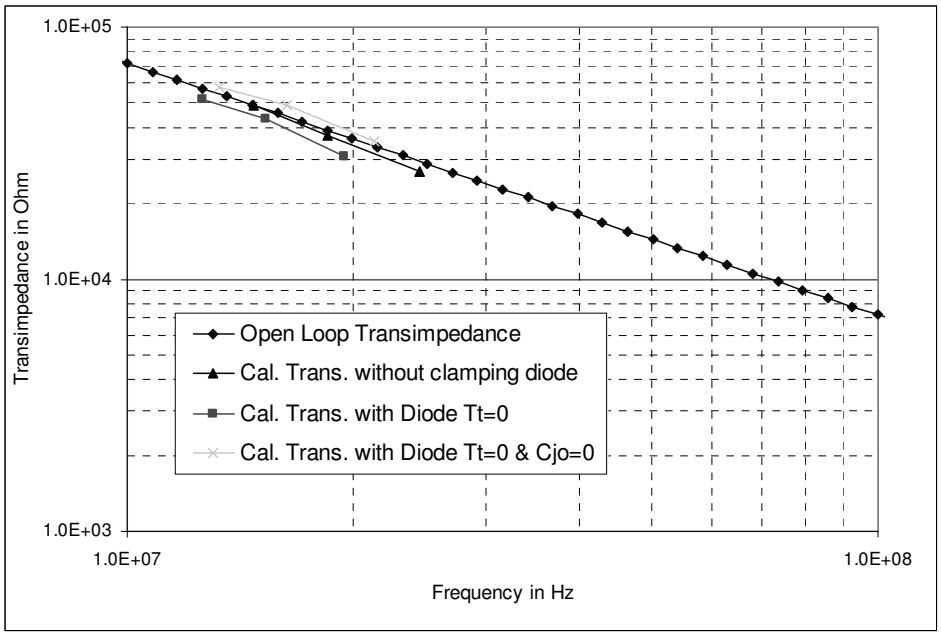


Figure 8.20 Calculated and simulated transimpedance with changing R_3 versus frequency of oscillation for triangular and rectangular wave

Figure 8.21 shows the calculated and simulated open loop transimpedance as a function of C_1. Here R_1 is 22 kΩ, R_2 is 1.1 kΩ, and R_3 is 3 kΩ. In this case, no diode clamp was used at the rectangular waveform output. Figure 21 also shows the frequency of oscillation versus C_1. The frequency of oscillation was found to be 24.5 MHz to 48.7 MHz. For C_1 = 600 fF, the frequency of oscillation is 24.5 MHz and for C_1 = 80 fF, the frequency of oscillation is 48.7 MHz.

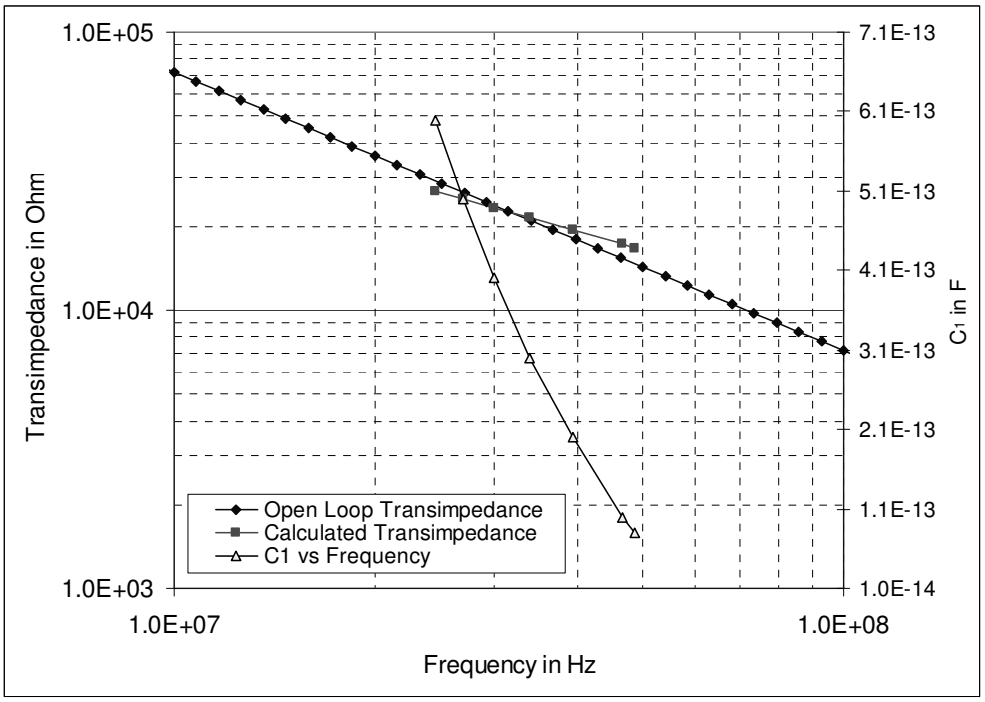


Figure 8.21 Transimpedance and C_1 versus frequency of oscillation for triangular and rectangular wave

Figure 8.22 shows the calculated and simulated open loop transimpedance as a function of C_1. Here R_1 is 22 kΩ, R_2 is 1.1 kΩ, and R_3 is 3 kΩ. In this case, the diode clamp was used at the rectangular waveform output. The triangular and rectangular waveforms are shown in figure 8.23.

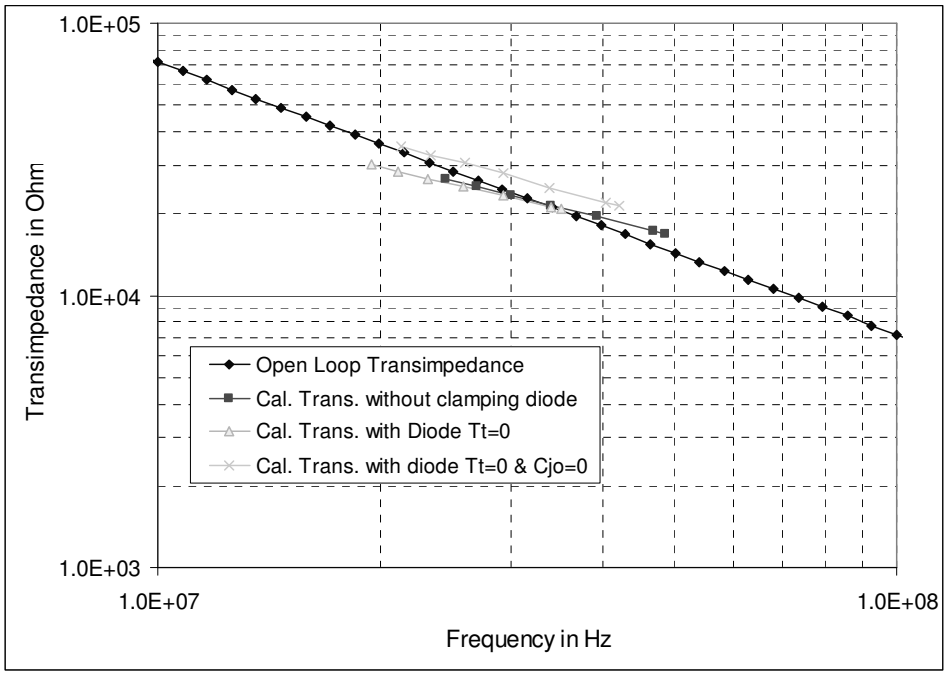


Figure 8.22 Calculated and simulated transimpedance with changing C_1 versus frequency of oscillation for triangular and rectangular wave

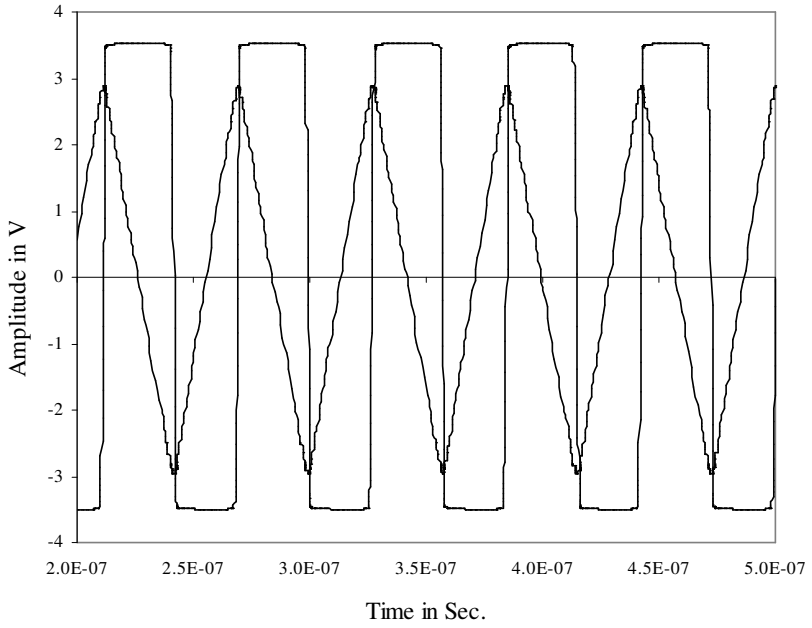


Figure 8.23. Output waveform for triangular and rectangular wave

CHAPTER 9

CURRENT FEEDBACK OPERATIONAL AMPLIFIER LAYOUT AND MEASUREMENTS

The layout and measurement results of three different types of CFOAs are presented in this chapter. All CFOAs were fabricated by National Semiconductor's Bipolar Junction Transistor (BJT) process. The UTA246V, and UTA246W are double buffer current feedback operational amplifiers. The double buffer current feedback operational amplifier is presented in Chapter 3. UTA246X is a double buffer current booster current feedback operational amplifier. The double buffer current booster current feedback operational amplifier is presented in Chapter 5.

9.1 Schematic Diagram and Layout for the UTA246V, UTA246W, and UTA246X

The schematic diagram for the UTA246V is shown in Figure 9.1 and the layout for this circuit is shown in Figure 9.2. The schematic diagram for the UTA246W is shown in Figure 9.3 and the layout for this circuit is shown in Figure 9.4. The schematic diagram for the UTA246X is shown in Figure 9.5 and the layout for this circuit is shown in Figure 9.6.

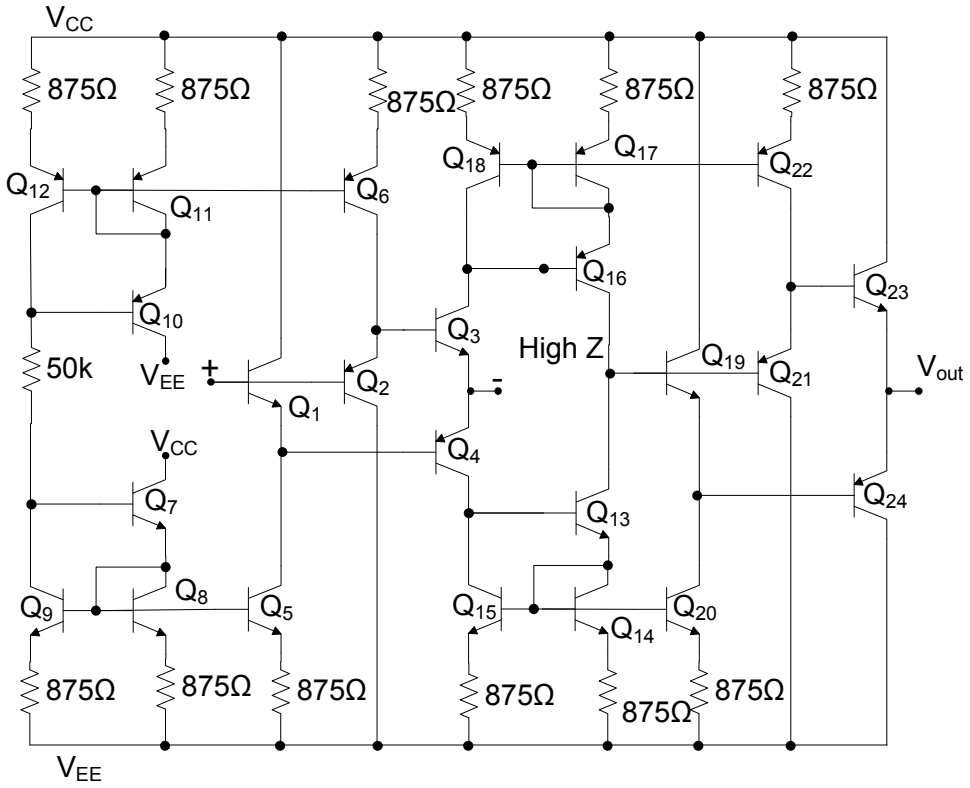


Figure 9.1 Schematic diagram of the CFOA UTA246V

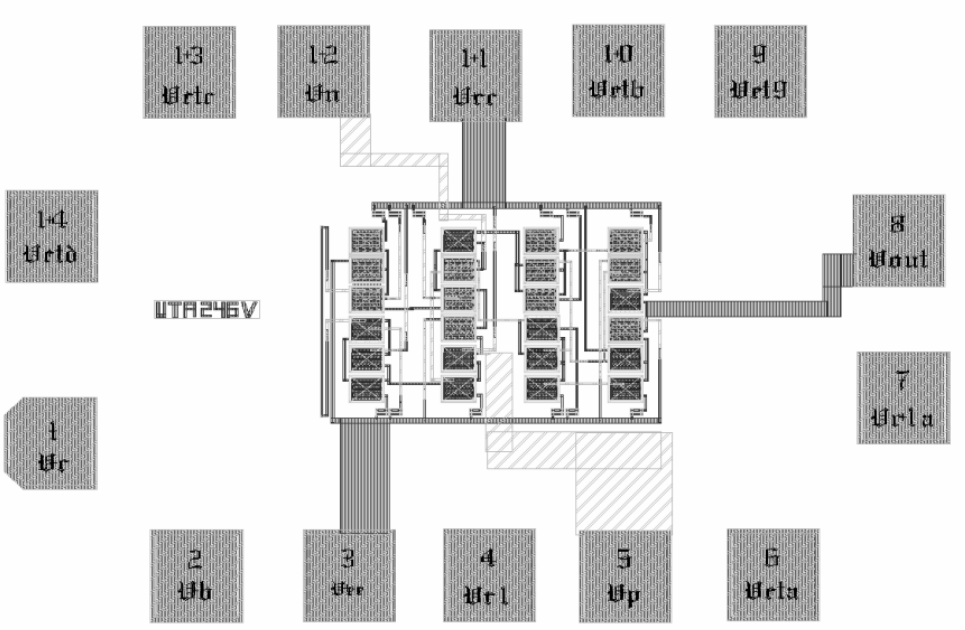


Figure 9.2 Layout of the CFOA UTA246V

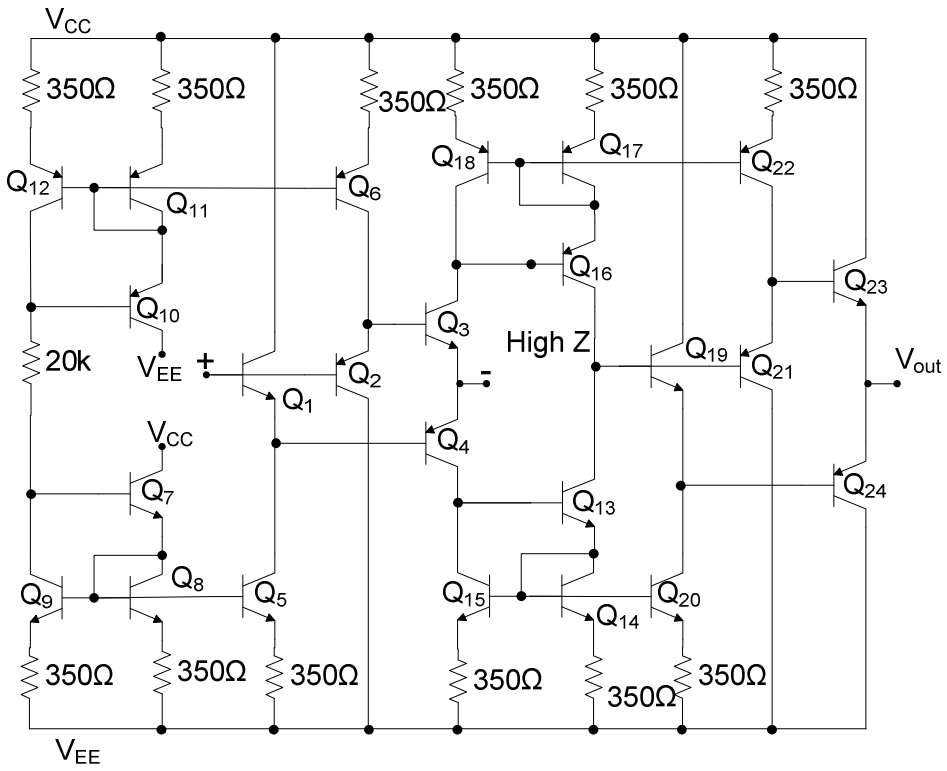


Figure 9.3 Schematic diagram of the CFOA UTA246W

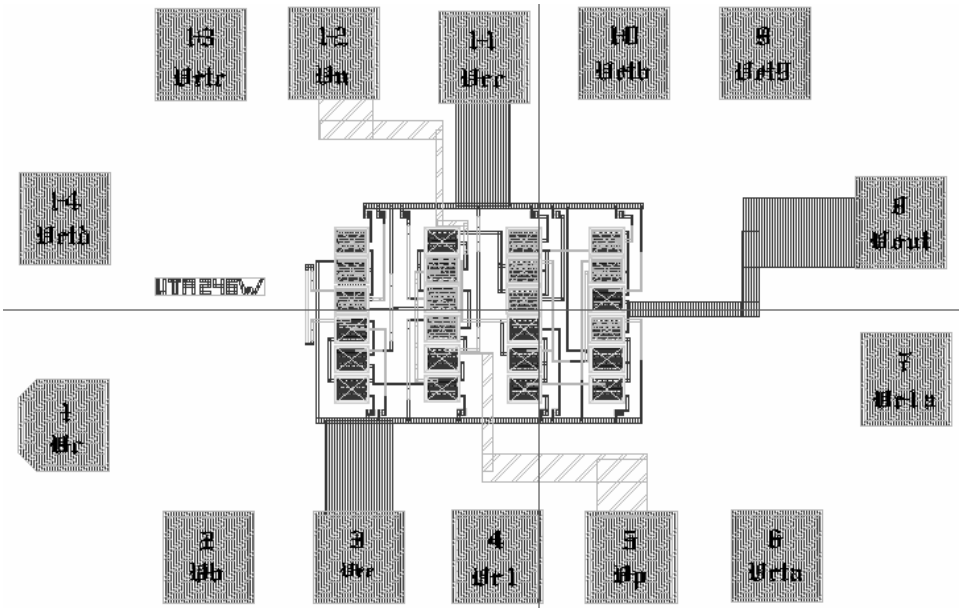


Figure 9.4 Layout of the CFOA UTA246W

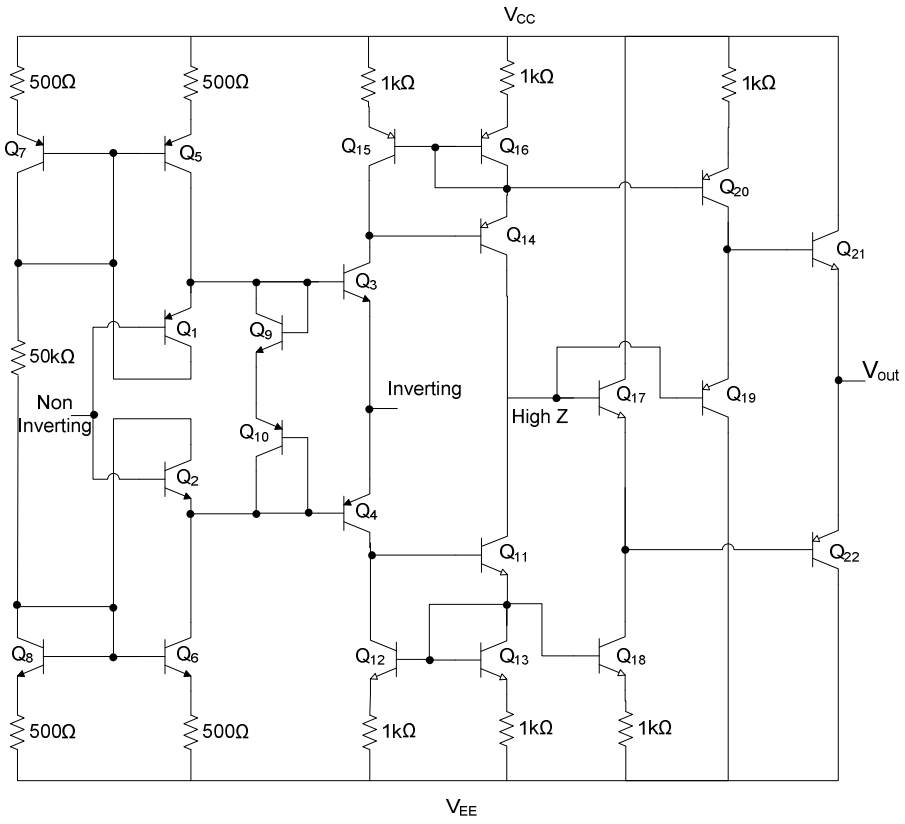


Figure 9.5 Schematic diagram of the CFOA UTA246X

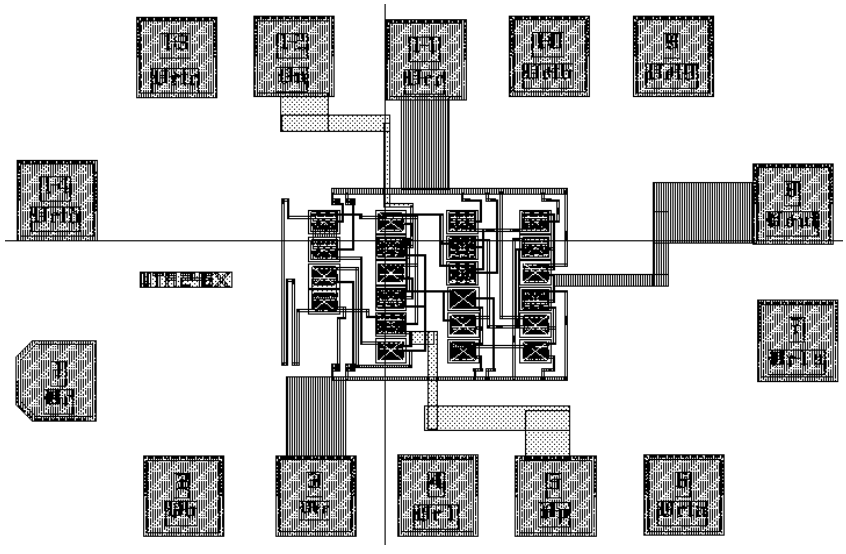


Figure 9.6 Layout of the CFOA UTA246X

9.2 Test Circuit for Measuring the CMRR and PSRR

The test circuit for measuring the CMRR and PSRR is shown in Figure 9.7 [25]. This circuit was developed by Bob Pease of National Semiconductor Corporation [25]. The OP07 is used as a unity gain buffer. The function of OP07 is to reduce the effect of the device under test's (DUT) output resistance on the measurement. The resistor R_5 is

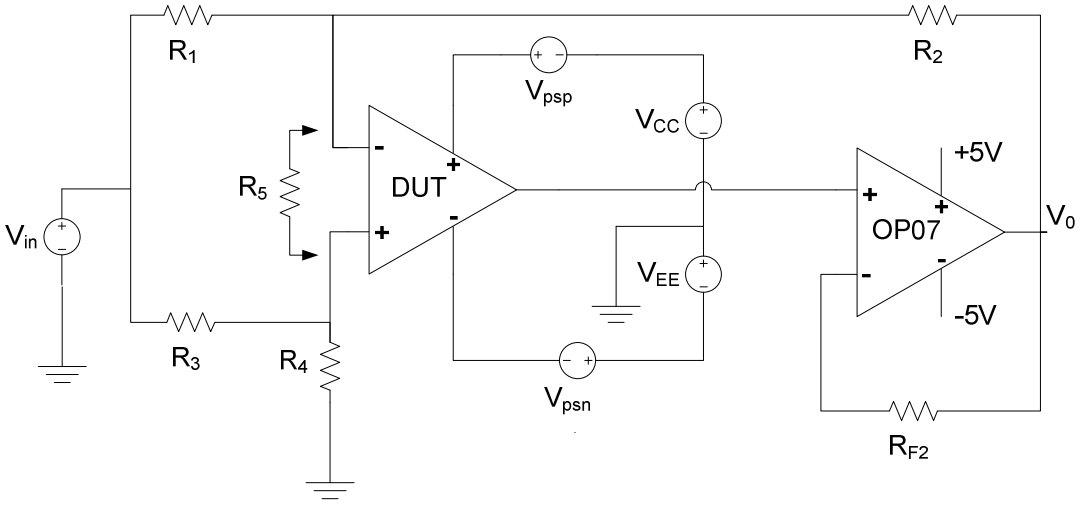


Figure 9.7 Test circuit for measuring the CMRR and PSRR

inserted between the input terminals of the DUT to change the circuit's noise gain. By monitoring the changes in the output voltage caused by changes in the exciting voltages (V_{in}, V_{psp}, V_{psn}), the change in noise gain can be used to compute the rejection ratios. The OP07 is assumed to be an ideal op-amp. The output voltage, V_0, is

$$V_0 = G_{v1}V_{in} - G_{v2}V_{\varepsilon} \tag{9.1}$$

The signal gain is

$$G_{v1} = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right) - \frac{R_2}{R_1} \tag{9.2}$$

The noise gain is

$$G_{v2} = 1 + \frac{R_2}{R_1} + \frac{R_2 + R_4}{R_5} \tag{9.3}$$

The input error voltage, V_ε, contains all non-ideal parameters that affect the op-amp's output voltage when the input is zero. The input error voltage is

$$V_\varepsilon = V_{OS} - \frac{V_{ic}}{CMRR} - \frac{V_{psp}}{PSRR^+} - \frac{V_{psn}}{PSRR^-} \tag{9.4}$$

The voltages V_{psp} and V_{psn} represent the changes in the positive and negative power supply voltages. V_{ic} is the amplifier's common-mode input voltage.

$$V_{ic} = \frac{V_p + V_n}{2} = \left(\frac{R_4}{R_3 + R_4} \right) V_{in} \tag{9.5}$$

9.2.1 Common Mode Rejection Ratio

The steps for measuring the common mode rejection ratio are described below. Set V_{psp} and V_{psn} equal to zero and R_5 to $R_5(1)$.Then vary the DC value of V_{in} from $V_{in}(a)$ to $V_{in}(b)$ and generate the difference. The difference value is

$$\Delta V_{in} = V_{in}(a) - V_{in}(b) \tag{9.6}$$

Measure the corresponding DC values of V_0 at $V_0(a)$ and $V_0(b)$ and generate the difference. The difference value is

$$\Delta V_0[R_5(1)] = V_0(a) - V_0(b) \tag{9.7}$$

Set R_5 to $R_5(2)$. Vary the DC value of V_{in} by the same amount and generate the difference. The difference value is

$$\Delta V_{in} = V_{in}(a) - V_{in}(b) \tag{9.8}$$

Measure the corresponding DC values of V_0 at $V_0(a)$ and $V_0(b)$ and generate the difference. The difference value is

$$\Delta V_0[R_5(2)] = V_0(a) - V_0(b) \tag{9.9}$$

Calculate CMRR from

$$CMRR = \left| \frac{R_4(R_2 + R_4)}{R_3 + R_4} \left[\frac{1}{R_5(1)} - \frac{1}{R_5(2)} \right] \right| \left[\frac{V_{in}(a) - V_{in}(b)}{\Delta V_0[R_5(1)] - \Delta V_0[R_5(2)]} \right] \tag{9.10}$$

9.2.2 Positive Power Supply Rejection Ratio

The steps for measuring the positive power supply rejection ratio are described below. Set V_{in} and V_{psn} equal to zero and R_5 to $R_5(1)$. Then vary the DC value of V_{psp} from $V_{psp}(a)$ to $V_{psp}(b)$ and generate the difference. The difference value is

$$\Delta V_{psp} = V_{psp}(a) - V_{psp}(b) \tag{9.11}$$

Measure the corresponding DC values of V_0 at $V_0(a)$ and $V_0(b)$ and generate the difference. The difference value is

$$\Delta V_0[R_5(1)] = V_0(a) - V_0(b) \tag{9.12}$$

Set R_5 to $R_5(2)$. Vary the DC value of V_{psp} by the same amount and generate the difference. The difference value is

$$\Delta V_{psp} = V_{psp}(a) - V_{psp}(b) \tag{9.13}$$

Measure the corresponding DC values of V_0 at $V_0(a)$ and $V_0(b)$ and generate the difference. The difference value is

$$\Delta V_0[R_5(2)] = V_0(a) - V_0(b) \tag{9.14}$$

Calculate $PSRR^+$ from

$$PSRR^{+} = \left| \left(R_2 + R_4\right) \left[\frac{1}{R_5(1)} - \frac{1}{R_5(2)} \right] \right| \left[\frac{V_{psp}(a) - V_{psp}(b)}{\Delta V_0[R_5(1)] - \Delta V_0[R_5(2)]} \right] \tag{9.15}$$

9.2.3 Negative Power Supply Rejection Ratio

The steps for measuring the negative power supply rejection ratio are described below. Set V_{in} and V_{psp} equal to zero and R_5 to $R_5(1)$. Then vary the DC value of V_{psn} from $V_{psn}(a)$ to $V_{psn}(b)$ and generate the difference. The difference value is

$$\Delta V_{psn} = V_{psn}(a) - V_{psn}(b) \tag{9.16}$$

Measure the corresponding DC values of V_0 at $V_0(a)$ and $V_0(b)$ and generate the difference. The difference value is

$$\Delta V_0[R_5(1)] = V_0(a) - V_0(b) \tag{9.17}$$

Set R_5 to $R_5(2)$. Vary the DC value of V_{psn} by the same amount and generate the difference. The difference value is

$$\Delta V_{psn} = V_{psn}(a) - V_{psn}(b) \tag{9.18}$$

Measure the corresponding DC values of V_0 at $V_0(a)$ and $V_0(b)$ and generate the difference. The difference value is

$$\Delta V_0[R_5(2)] = V_0(a) - V_0(b) \tag{9.19}$$

Calculate $PSRR^{-}$ from

$$PSRR^{-} = \left| \left(R_2 + R_4\right) \left[\frac{1}{R_5(1)} - \frac{1}{R_5(2)} \right] \right| \left[\frac{V_{psn}(a) - V_{psn}(b)}{\Delta V_0[R_5(1)] - \Delta V_0[R_5(2)]} \right] \tag{9.20}$$

9.3 Test Circuit for Measuring the Input Offset Voltage and Input Offset Current

The test circuit for measuring the CMRR and PSRR is shown in Figure 9.8 [25]. Here V_{id} and V_{ic} represent the differential-mode and the common-mode input voltages to the DUT. Assume that the OP07s in this circuit are ideal op-amps.

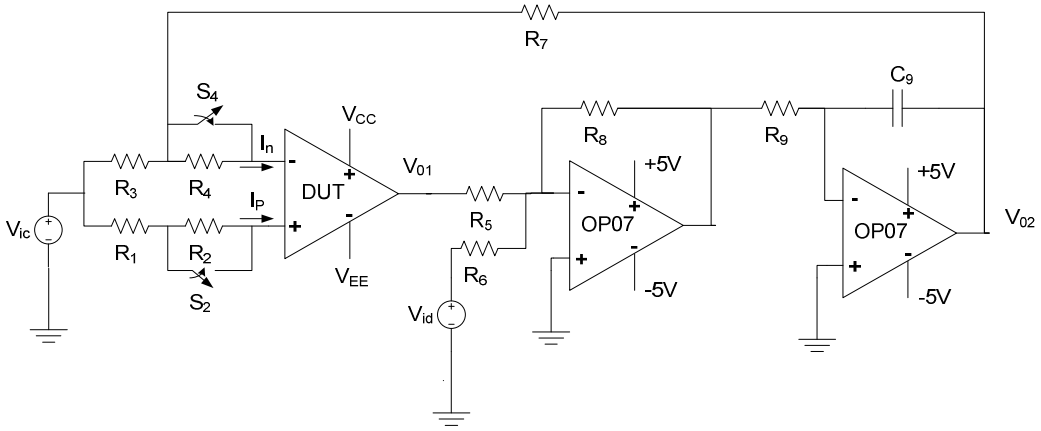


Figure 9.8 Test circuit for measuring the input offset voltage and input offset current

Low frequency, small signal expression for the output voltage V_{02} is

$$V_{id} = \left(\frac{R_6}{R_5}\right)\left(\frac{R_3}{R_3+R_7}\right)G_{vdm}\left(V_{02}-V_{ic}\right)-\left(\frac{R_6}{R_5}\right)G_{vcm}V_{ic} + \left(\frac{R_6}{R_5}\right)G_{vdm}\left(V_{OS}+R_P I_P - R_n I_n\right) \tag{9.21}$$

Where

$$R_P = R_1 + R_2 \tag{9.22}$$

$$R_n = R_4 + \frac{R_3 R_7}{R_3 + R_7} \tag{9.23}$$

9.3.1 Input Offset Voltage V_{OS}

The steps for measuring the input offset voltage are described below. Close switch S_2 and S_4. Then set V_{ic} and V_{id} to zero and measure V_{02} with a DC voltmeter. Calculate V_{OS} from

$$V_{OS} = -\left(\frac{R_3}{R_3 + R_7}\right)V_{02} \tag{9.24}$$

9.3.2 Positive Input Terminal Current I_P

The steps for measuring the positive input terminal current are described below. Open switch S_2 and close switch S_4. Then set V_{ic} and V_{id} to zero and measure V_{02} with a DC voltmeter. Calculate I_P from

$$I_P = -\frac{1}{R_P}\left[\left(\frac{R_3}{R_3 + R_7}\right)V_{02} + V_{OS}\right] \tag{9.25}$$

9.3.3 Negative Input Terminal Current I_n

The steps for measuring the negative input terminal current are described below. Close switch S_2 and open switch S_4. Then set V_{ic} and V_{id} to zero and measure V_{02} with a DC voltmeter. Calculate I_n from

$$I_n = \frac{1}{R_n}\left[\left(\frac{R_3}{R_3 + R_7}\right)V_{02} + V_{OS}\right] \tag{9.26}$$

9.3.4 Input Offset Current

Calculate the input offset current from the positive input terminal current and the negative input terminal current.

$$I_{OS} = I_P - I_n \tag{9.27}$$

9.4 Test Circuit for Measuring the CMIR

The test circuit for measuring the CMIR is shown in Figure 9.9. Here all resistance values are the same. V_0 is plotted as a function of V_{in}. At a certain value of V_{in}, the feedback loop breaks and the V_0 reaches either the positive or negative rail. So the CMIR for this CFOA is $\pm$ ½V_{in}.

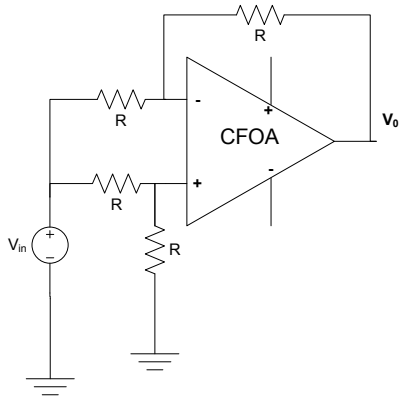


Figure 9.9 CMIR measurement circuit

9.5 Test Circuit for Measuring the Slew Rate

The configuration for measuring the slew rate for the CFOA is shown in Figure 9.10. The slew rate can be determined from the slope of the output waveform during the rise and fall of the waveform. The CFOA should be configured in the unity gain configuration with a feedback resistance greater than the critical resistance of the CFOA. The unity gain configuration places the CFOA in the worst case because its feedback is the largest.

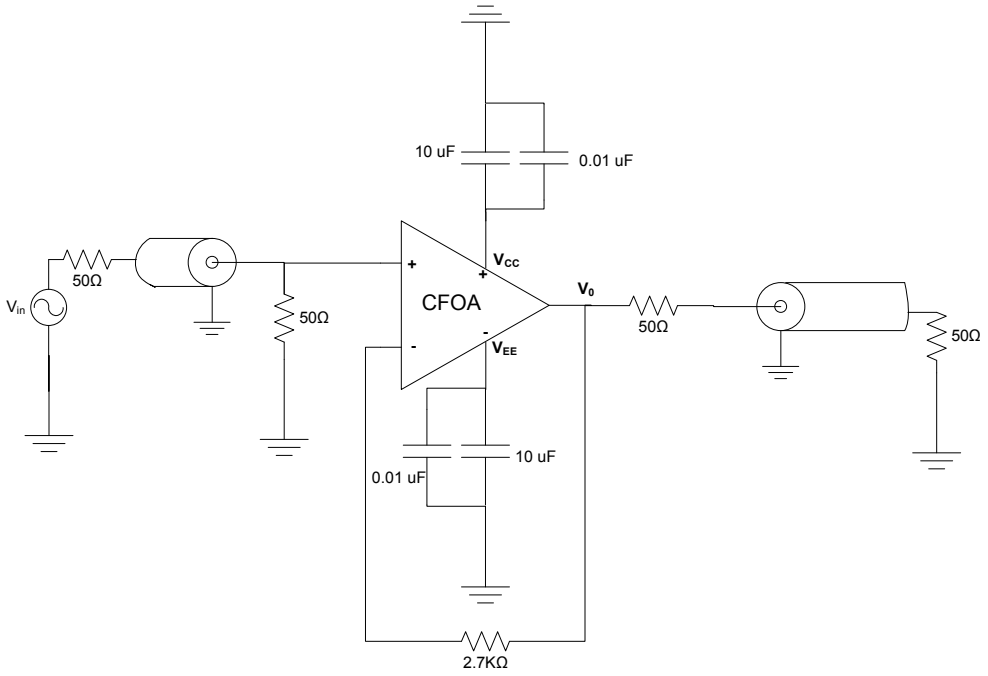


Figure 9.10 SR measurement circuit

9.6 Test Circuit for Generating the Triangular and Rectangular Wave

The triangular and rectangular wave generator circuit is shown in Figure 9.11. Here the power supply voltages are ± 5 V.

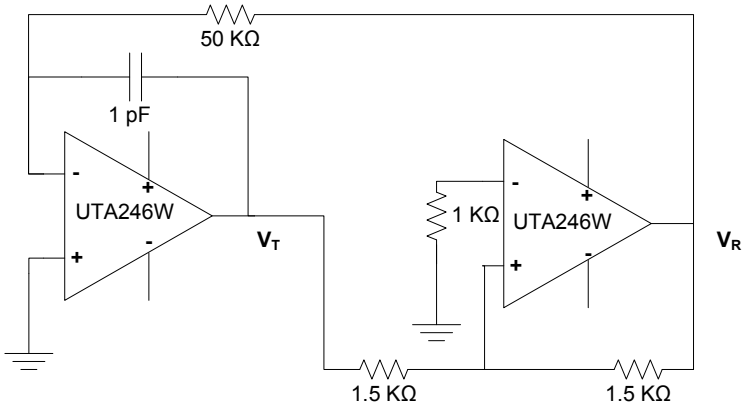


Figure 9.11 The triangular and rectangular wave generator circuit

9.7 Measurement Results

The measurement results for the CFOA UTA246V, UTA246W, and UTA246X is given in table 9.1. Here the supply voltage is ± 5 V.

Table 9.1 Measurement Results for the UTA246V, UTA246W, and UTA246X

Parameter	UTA246V	UTA246W	UTA246X
CMRR	100.95 dB	93.43 dB	76.78 dB
$PSRR^+$	96.67 dB	99.54 dB	60.83 dB
$PSRR^-$	94.82 dB	102.31 dB	69.57 dB
CMIR	3.08 V	3.03 V	3.23 V
Input Offset Current	-3.16 µA	-3.17 µA	-3.12 µA
Input Offset Voltage	7.19 mV	7.20 mV	7.03 mV

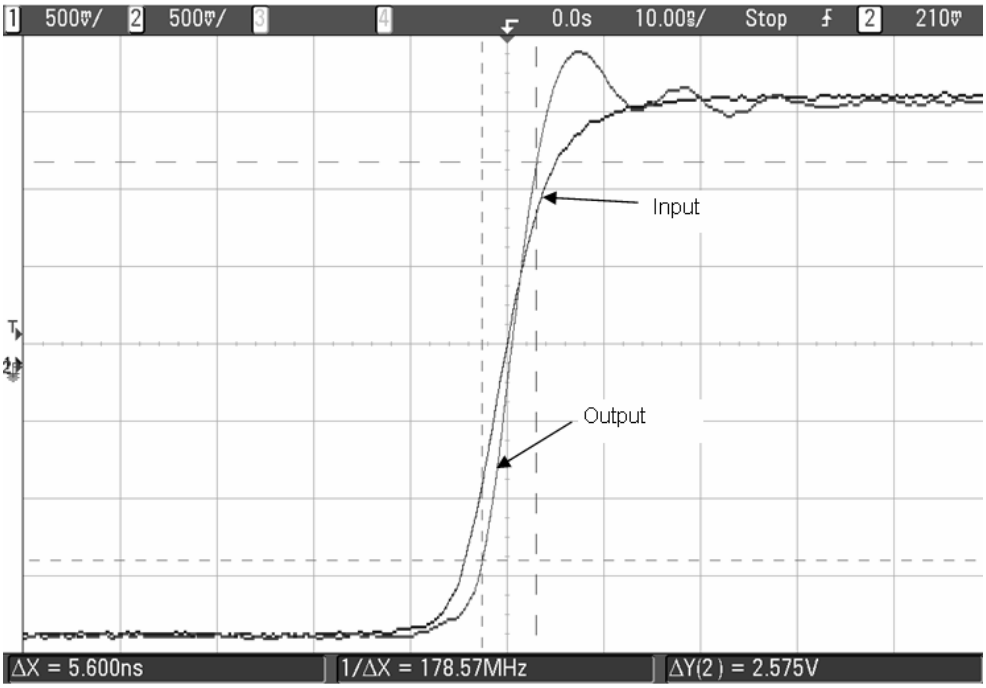


Figure 9.12 Slew rate measurement result for UTA246V

In Figure 9.12, Figure 9.13, and Figure 9.14, the input signal slew rate is 325 V/µS. There is no extra slew for the output signal. So the slew rate for the CFOAs is 325 V/µS or greater.

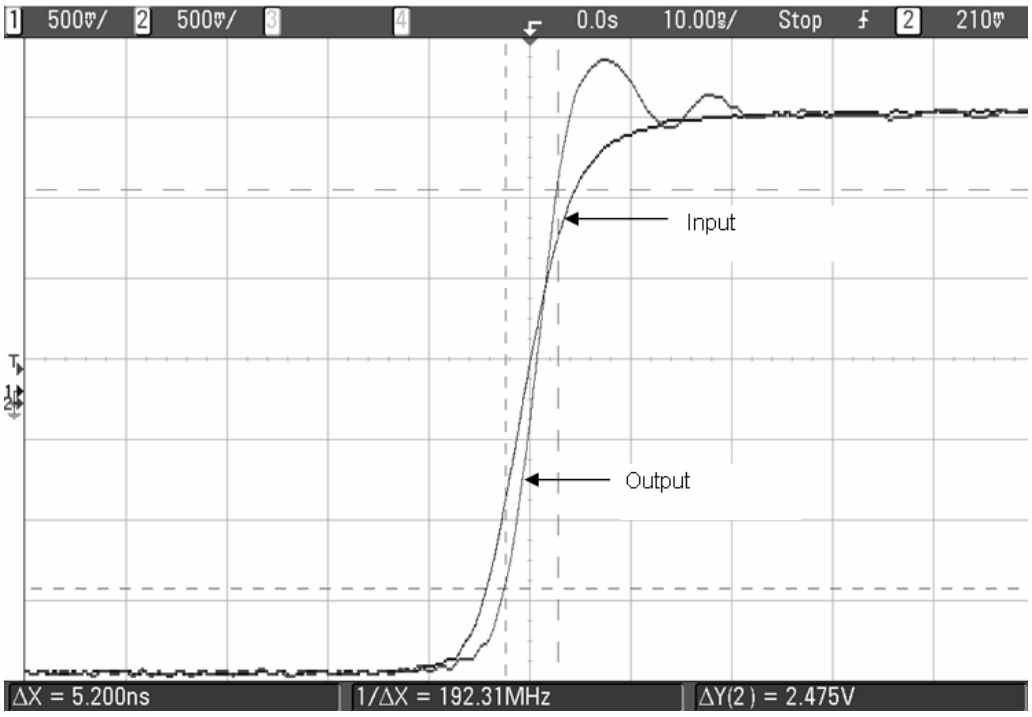


Figure 9.13 Slew rate measurement result for UTA246W

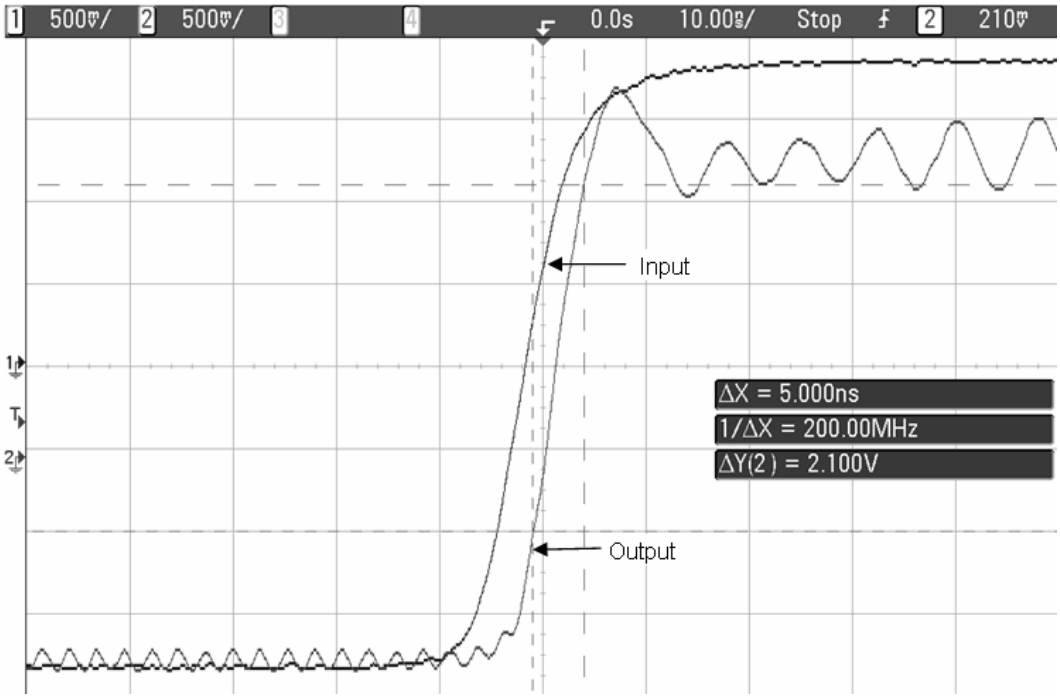


Figure 9.14 Slew rate measurement result for UTA246X

Figure 9.15 Measurement result for triangular and rectangular waveform

The measured frequency of oscillation for the triangular and rectangular waveforms is 2.8 MHz. Smaller values of capacitance would make the frequency of oscillation higher.

CHAPTER 10

CONCLUSIONS AND FUTURE WORK

Current feedback operational amplifier has higher slew rate and higher bandwidth compared to the voltage feedback operational amplifiers. Any signal generator built with current feedback operational amplifiers would expect to operate at higher frequency compared to the voltage feedback operational amplifiers and higher amplitude compared to CMOS technology.

Bipolar junction characterizations were presented in chapter 2. The current feedback operational amplifier and its macro-model were studied extensively in chapter 3 to chapter 6. The maximum simulated output voltage for the double buffer CFOA was found to be ± 3.85 V when biased with ± 5 V power supplies. The simulated input offset voltage was -7.73 μA, the input offset voltage was 24.87 mV, the positive PSRR was 53.54 dB, the negative PSRR was 64.87 dB, the positive CMIR was 3.065 V, the negative CMIR was -3.12 V, and the CMRR was 60.45 dB for the double buffer CFOA.

For 0.3 mA quiescent current, the positive slew rate was 340 V/μS, and the negative slew rate was 200 V/μS for the double buffer CFOA. For the same quiescent current, the positive slew rate was 2000 V/μS, and the negative slew rate was 2400 V/μS for the double buffer current booster CFOA. For 4.0 mA quiescent current, the positive slew rate was 3850 V/μS, and the negative slew rate was 2400 V/μS for the

double buffer CFOA. For the same quiescent current, the positive slew rate was 7900 V/μS, and the negative slew rate was 6500 V/μS for the double buffer current booster CFOA.

Three test chips for the current feedback operational amplifier were fabricated and tested. UTA246V, UTA246W are the double buffer CFOA and UTA246X is double buffer current booster CFOA. The slew rate for the CFOAs is 325 V/μS or greater.

A sinusoidal oscillator design is presented in chapter 7 and a triangular, rectangular wave generator is presented in chapter 8. The simulated frequency of oscillation for the sinusoidal oscillator was 13.13 MHz to 23.94 MHz. The simulated frequency of oscillation for the triangular and rectangular waveform was 6.78 MHz to 59.5 MHz. One protoboard test circuit was built for measuring the triangular and rectangular waveforms. Here UTA246W was used for the CFOAs, external capacitor and resistors are used. The measured frequency of oscillation for the triangular and rectangular waveform was 2.8 MHz.

10.1 Recommendations for Future Work

Noise and harmonic distortion for the current feedback operational amplifier are not studied in this dissertation work.

The sinusoidal, triangular, and rectangular wave generator can be made tunable. To make the sinusoidal oscillator tunable, it is required to change the C_1, R_2, R_3, R_4, or C_5 as a function of current or voltage. For triangular or rectangular wave, R_1, R_2, R_3, or C_1 needs to be a function of current or voltage. A translinear cell can be used to change the resistance value as a function of current.

APPENDIX A

BIPOLAR TRANSISTOR MODEL FILES [47]

```
.MODEL QINN NPN (
+ IS = 6.060E-18 BF = 130.0 NF = 1.000
+ VAF = 156.0 IKF = 3.04E-3 ISE = 1.260E-15
+ NE = 2.000 BR = 3.000 NR = 1.000
+ VAR = 5.000 IKR = 3.040E-2 ISC = 6.060E-17
+ NC = 1.000 RB = 400.0 IRB = 1.000E-3
+ RBM = 30.0 RE = 15.0 RC = 10
+ CJE = 4.7E-15 VJE = 0.928 MJE = 0.333
+ TF = 1.77E-11 XTF = 10.0 VTF = 2.500
+ ITF = 1.0E-3 PTF = 25.0 CJC = 1.03E-14
+ VJC = 0.732 MJC = 0.250 XCJC = 1.0
+ TR = 1.77E-9 CJS = 5.000E-15 VJS = 0.655
+ MJS = 0.0 XTB = 3.5E-1 EG = 1.126
+ XTI = 4.0 KF = 1.0E-9 AF = 2.0
+ FC = 0.5 TNOM = 27 LATERAL = NO)

.MODEL QINP PNP (
+ IS = 2.6912E-18 BF = 71.5 NF = 1.000
+ VAF = 52.0 IKF = 1.350E-3 ISE = 1.256E-15
+ NE = 2.5 BR = 4.0 NR = 1.0
+ VAR = 3.0 IKR = 1.35E-2 ISC = 2.691E-17
+ NC = 1.00 RB = 177.78 IRB = 4.440E-4
+ RBM = 13.33 RE = 33.75 RC = 22.5
+ CJE = 4.70204E-15 VJE = 0.928 MJE = 0.333
+ TF = 1.990E-11 XTF = 100.0 VTF = 2.50
+ ITF = 1.350E-3 PTF = 30.0 CJC = 1.03119E-14
+ VJC = 0.732 MJC = 0.25 XCJC = 1.0
+ TR = 1.990E-9 CJS = 5.000E-15 VJS = 0.655
+ MJS = 0.0 XTB = 3.0E-1 EG = 1.126
+ XTI = 4.0 KF = 3.43E-10 AF = 2.0
+ FC = 0.5 TNOM = 27 LATERAL = NO)
```

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AKM Sydul Haque was born and brought up in Netrakona, Bangladesh. He received B.S. in Electrical Engineering from Bangladesh University of Engineering and Technology, Dhaka, Bangladesh, in February 1995. After working four years in Bangladesh, he commenced his graduate studies in USA. He obtained his M.S. from the University of Texas at Arlington, Texas, United States in December 2001. Since January 2003, he has been working towards the Ph.D. at the University of Texas at Arlington, Texas, United States. His research interest focuses on Current Feedback Amplifier based Signal Generator. He acquired his Ph.D. degree in August 2008.