DESIGN OF ANALOG CORRELATOR FOR 22-29GHz UWB VEHICULAR RADAR SYSTEM IN IBM 90nm CMOS PROCESS

by

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ABSTRACT

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In this thesis analog correlator is designed for UWB vehicular radar system. Operating frequency of the correlator is 22-29GHz. IBM 90nm CMOS process is used for the design, Simulations are done in CADENCE Spectre and SpectreRF. UWB signal of 22-29GHz is generated in ADS. Gaussian mono-pulse is shaped with band-pass filter to meet FCC mask. Simulations are done by using this signal.

Typical receiver of UWB system consists of LNA, analog correlator and ADC. Analog correlator is the matched filter which is a part of receiver. It is used to detect the incoming RF signal by maximizing signal to noise ratio at its output. Correlator is composed of two blocks namely multiplier and integrator. Multiplication of input RF signal with locally generated template signal is integrated by the capacitor. This correlated signal which is a low frequency signal then converted into digital domain by ADC for further processing.

Proposed architecture gives more gain compared to conventional architecture. Gain is improved from -13.97dB to -2.49dB. New method of improving isolation ratio is suggested and results show the

improvement of isolation ratio by 2dB. Inductive peaking technique is used to enhance the bandwidth of the circuit. Bandwidth improves by 50% by using inductors at series with the load resistance and also in series with source node of current source transistors.Holding time of the circuit is 2.3ns. Simulation results shows that signal can be detected in the presence of noise.

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CHAPTER 1

INTRODUCTION

Ultra-wide band (UWB) systems are becoming more and more popular as they offer unique advantages in communication and measurement systems, imaging systems, vehicular radar systems. UWB systems are defined by Federal Communication Commission (FCC) in spring 2002 through its modified and amended 47CFR Part 15 regulations. UWB characterizes transmission systems which occupies 500MHz of spectrum or has a fractional bandwidth of 20%. Such high bandwidth systems rely on ultra short (nanosecond scale) pulses which can be transmitted directly and are free from sine wave carrier. As a result they do not require IF processing. Large bandwidth and short duration pulses makes UWB system an attractive option for bandwidth-demanding position critical low power applications in wireless communications, networking, radar imagining, and localization systems [1].

Two different technologies are proposed for the UWB systems and they are broadly classified as carrier less and carrier based technologies. Impulse Radio (IR) UWB is carrier less UWB technology while Orthogonal Frequency Division Multiplexing (OFDM) is carrier based UWB technology. IR UWB does not use sinusoidal carrier to shift the signal at higher frequency but it transmits the signal at baseband. It use sub nanosecond wide pulses to generate gigahertz wide signal. It does not require any IF signal and RF front end design is less complex. Because of short duration of pulses it leads to lower multipath fading and provides higher immunity to interference from other radio systems. In case of OFDM technology total spectrum is divided into several bands each having minimum bandwidth of 500MHz. The transmission of data for a given user can occur on different sub-bands in subsequent periods of time [2]. As different carrier frequencies are used for different bands system architecture becomes more complex. As mentioned earlier IR UWB does not use carrier signal hence system architecture is simpler compared to OFDM. Also power consumption of IR UWB systems is lesser than OFDM systems. Because of its simplicity IR UWB is the best candidate for UWB systems.

Figure 1 shows the typical block diagram of IR UWB receiver. Received signal from antenna is fed to Low Noise Amplifier (LNA) which amplifies the signal. Then this amplified signal is fed to analog correlator. Analog Correlator consists of two blocks, multiplier followed by an integrator. Multiplier produces the multiplication of received signal and locally generated template signal. Output of integrator is converted to digital signal by sample and hold circuit and ADC. Analog correlator acts as a matched filter which correlates the received signal with the template signal and maximizes the signal to noise ratio (SNR) at its output.

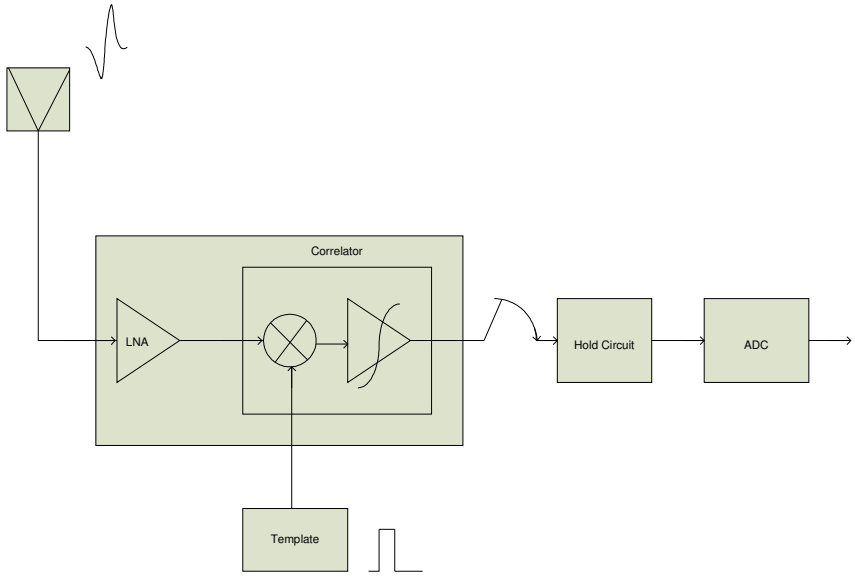


Figure 1.1 Block Diagram of typical UWB receiver

Correlator acts as detector in the UWB receiver. Correlation can be realized in both analog and digital domain. In order to do correlation in digital domain it is first required to convert analog signal to digital signal with ADC. If input signal is high frequency (few GHz) signal then sampling frequency required is double of the maximum frequency in the signal by Nyquist criterion. Thus it is difficult to realize the ADC. The advantage of analog correlator is that it can process the signals in real time and provide a continuous output at a low frequency and thereby remove the need of special ADC requirement in the receiver [3]. Thesis discusses the Design of an Analog correlator for 22-29GHz frequency band for vehicular radar application.

Analog Correlator in [3, 4, 5] are designed for 3.1-10.6GHz communication application. Correlator presented in [4] is designed in SiGe technology while correlator in [4, 5] are designed in CMOS 0.18μm technology. Correlator presented in [6] is designed for 128 MHz DS-CDMA wireless applications in 0.6 μm technology. UWB multipliers presented in [7, 8, 9 and 10] are designed for communication application in CMOS 0.18 μm technology. Proposed analog correlator is designed in CMOS 90nm technology for 22-29 GHz UWB vehicular radar application. Proposed design also suggests ways of improving conversion gain and linearity of the circuit.

CMOS 90nm process is chosen for the design because it has transit frequency (ft) around 120GHz. Power supply voltage required to get high ft is limited to 1.2V this limits maximum transistors that can be stacked on top of each other and kept in saturation. As a results gain suffers. Different architectures and methods can be found out to compensate this problem. The main advantage of CMOS process over other technologies like SiGe is it is cheap to fabricate, consumes less chip area.

This thesis is organized as follows. Chapter 1 provides brief introduction to UWB systems. It discusses the typical IR UWB receiver block diagram and states the function of analog correlator. It provides motivation of the work that is performed and also reason for choosing CMOS technology. In Chapter 2 background material is provided to discuss design of CMOS analog correlator for UWB radar application. It includes basic UWB system overview and a brief discussion on IBM 90nm CMOS process. Chapter also discusses gm/id design methodology used to design the proposed correlator. The purpose of Chapter 3 is to provide broad overview of correlator theory and discuss different types of correlator designed so far. Chapter 4 discusses proposed correlator design with discussion on results obtained from simulation. Chapter 5 provides conclusion and future work.

CHAPTER 2

BACKGROUND

2.1 Basics of UWB Technology

2.1.1 *History of Ultra-Wide Band Technology*

Research on UWB systems is going on for a long time, although they were not referred to as "Ultra-Wideband". In 1901 Marconi carried out spark-gap transmission experiment which is considered as first experiment of impulse radio. Ross and Bennett [11] and Harmuth [12] made pioneering contributions to modern UWB systems. First patent of UWB communication systems was awarded to Ross in 1973. Through 1980's UWB technology was commonly referred to as carrier-free, base band, or impulse communication. United States Department of Defense coined the term "Ultra-Wide Band" for the first time. The United States Department of Defense was using UWB technology for a long time but technological advances prior to 1994 were classified. Even though UWB technology has many attractive features, research in UWB technology was limited to radar systems and mainly for military applications [1]. However in spring 2002 Federal communication commission (FCC) passed a legislation allowing commercial use of UWB capable devices under certain guidelines [13].

2.1.2 *Definition of UWB systems*

Ultra-Wide Band term is frequently used in UWB radars and refers to electromagnetic waveforms that are characterized by an instantaneous fractional energy bandwidth greater than 0.20-0.25

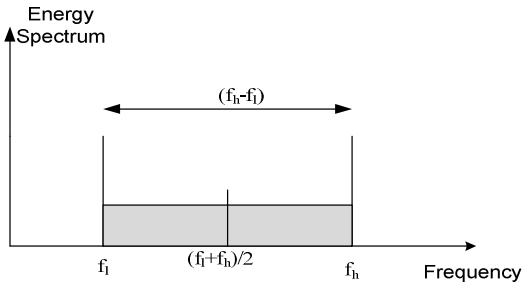


Figure 2.1 Energy Bandwidth [2]

Figure 2.1 illustrate the concept of energy bandwidth. Energy bandwidth of the waveform is defined by frequencies f_L and f_H which contains 90% energy of waveform in that that interval. Thus width, f_H-f_L is defined as energy bandwidth [2].

However FCC defines UWB signal as a signal which has a spectral occupancy of more than 500MHz or has a fractional bandwidth of 20%. Fractional bandwidth is defined as

$$F_{bw} = \frac{Bandwidth(BW)}{CenterFrequency} = \frac{f_v - f_L}{(f_v + f_L)/2} \tag{2.1}$$

Where, f_U and f_L are the upper and lower -10dB emission points, respectively. FCC specifies that a system with the center frequency in excess of 2.5GHz must have a bandwidth of 500MHz, but a system whose center frequency is less than 2.5GHz must have fractional bandwidth (F_{bw}) of at least 20% to be characterized as an UWB system.

2.1.3 *Regulations on UWB systems*

In spring 2002 FCC released a document which established different bands of frequencies to be used for different applications

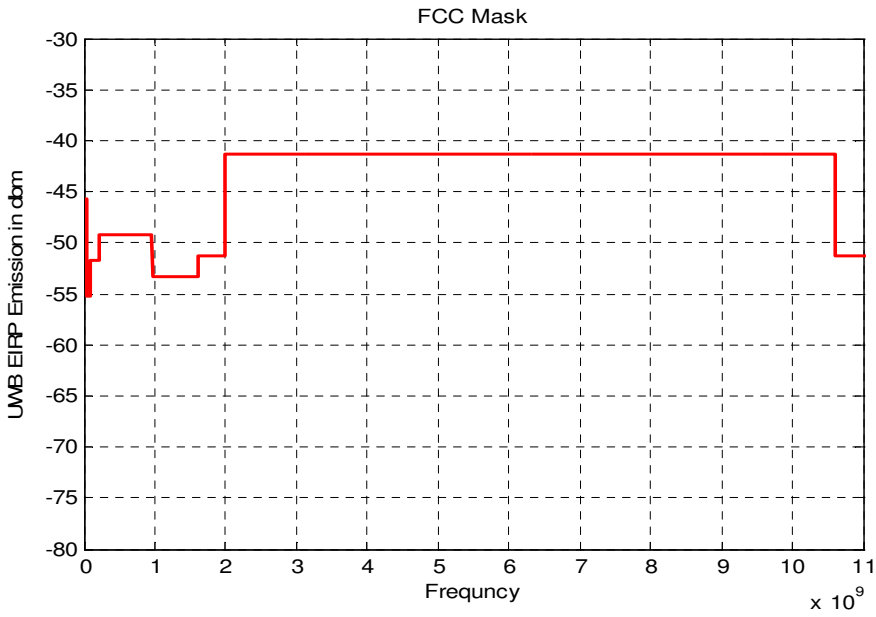


Figure 2.2 Spectral Mask Specified by FCC

FCC specifies 3.1GHz to 10.6GHz band for the communication application. Figure 2.2 shows the spectral emission mask specified by FCC. Transmitted power level allowed in 3.1-10.6GHz in -41.3dBm/MHz .The outdoor transmission limit is lower from 1.6-3.1GHz than the indoor limit because this band is used by some other application as well. Thus, FCC places greater restrictions on transmitted power in this region to avoid interference. Frequency band from 22-29GHz is assigned for vehicular radar application. Transmitted power allowed in this band is -41.3dBm/MHz

2.1.4 Applications of UWB

UWB applications to wireless communications are most widely appreciated. In today's time high speed communication is the need and UWB exactly offers this. One of the main features of UWB is high data rates combined with low power consumption. Low power consumption is possible because of large bandwidth. These qualities of UWB systems can be illustrated by Shannon's Information Capacity theorem. Shannon's theorem states that maximum theoretical channel capacity (C in bits per second) is a function of channel bandwidth (B), signal power(S), and noise power (N) and is given by

$$C = B\log_2\left(1 + S/N\right) \tag{2.2}$$

In case of narrow band systems bandwidth of channel is limited thus in order to data rate, which is data rate, only choice is to increase signal power. But in UWB systems bandwidth available is huge (3.1 -10.6 GHz, 7 GHz of bandwidth) thus we can large data rates and the same time signal power transmitted is less.

FCC also allowed 22-29GHz band for vehicular radar applications. Using UWB systems for vehicular radar applications proves very beneficial. In case of UWB systems pulses with very short durations are sent which increases the radar resolution. It also reduces the multipath fading. There are many other wireless communication, imaging and biomedical applications possible with UWB.

2.1.5 Standardization of UWB systems

UWB systems share the spectrum with many existing wireless systems. This is the main reason for the limitations on the transmitted power of UWB systems. One of the most important standardized systems which share the spectrum UWB systems is global positioning systems (GPS), IEEE 802.11

systems. In order to have good integration of existing communication systems with UWB systems and to have highest level of quality to end user IEEE is developing several standards.

One of the most attractive applications of UWB systems is in wireless personal area network (WPAN). This is one of the most important reasons that most of the recent standardization activity of UWB systems by IEEE occurred in this standard- Standard for wireless personal area network (WPAN-802.15) task group. In 802.15 standards family new task group 802.15.3 is formed to consider an alternative high data rate physical layer (PHY) implementation with UWB technology. Currently group is examining two different proposals of implementing physical layer with UWB. Once it is finalized then UWB systems will provide better performance and capabilities to systems which are currently using Bluetooth technology.

IEEE has established the 802.15.4 study group to define a new physical layer concept. This is intended to be used for low-data rate applications [14].Potential applications are sensors, interactive toys, smart badges, remote controls and home automation.

2.1.6 System Architectures of UWB systems

There are two different types of system architectures which can be employed to efficiently use UWB spectrum. They are namely Impulse type UWB (IR-UWB) and carrier based orthogonal frequency division multiplexing (OFDM). Both of the system architectures have certain advantages and disadvantages over each other. These both system architectures are the two major competing proposals for IEEE 802.15.3 standards. It is already decided that for 802.15.4 standard IR UWB is to be used because of its simplicity and localization capabilities. OFDM Alliance (MBOA) supports a type of OFDM architecture referred to as MB-OFDM (www.multibandofdm.org) while The UWB forum is proposing a form of IR-UWB called Direct Sequence UWB (DS-UWB) (www.uwbforum.org).

2.1.6.1 IR-UWB Systems

In IR UWB systems baseband communication is employed. In this type of UWB systems pulses with very short duration (sub nanosecond) are transmitted. Pulse position modulation (PPM), Pulse Amplitude modulation (PAM) or Phase shift keying (PSK) are used as modulation schemes. It is required that in IR UWB systems each pulse should match exact spectral mask defined by FCC.

There are basically two different types of receivers employed IR-UWB systems namely coherent receiver and non-coherent receivers. Figure 2.2 shows the typical coherent receivers.

In these types of receivers input RF signal is correlated to locally generated pulse. Here it is required that both template and input RF signal should match in time and shape to have maximum output. Thus if template and input RF signal are not aliened then output can't have all the energy of input RF pulse. Also it is required to have shapes of both template and input RF signals to be matched.

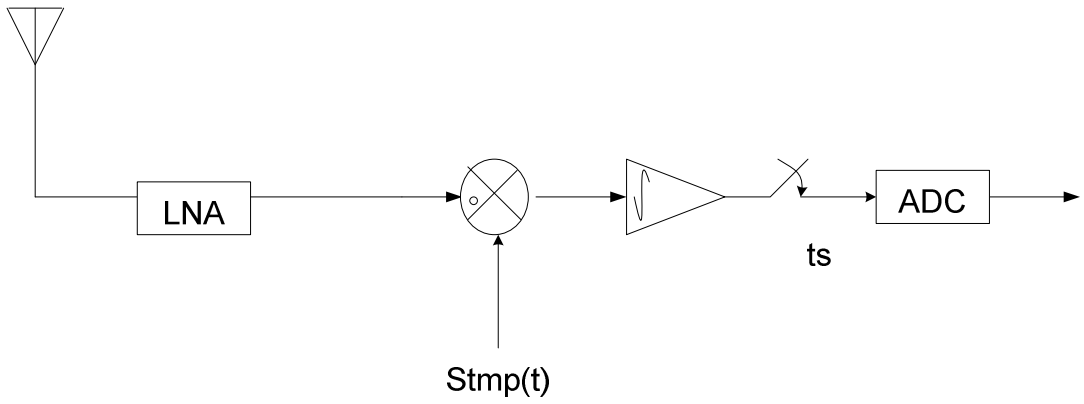


Figure 2.3 Coherent Receiver for IR UWB systems.

Figure 2.3 shows the non-coherent type receiver. In this type of receiver input RF signal is delayed by one period and correlated with the next pulse. Thus transmitter should send dummy pulses before each information pulse. This increase the overhead as far as transmitter is concerned and increases the power requirements. In the receiver the delay cell which is used to delay the dummy pulse becomes critical.

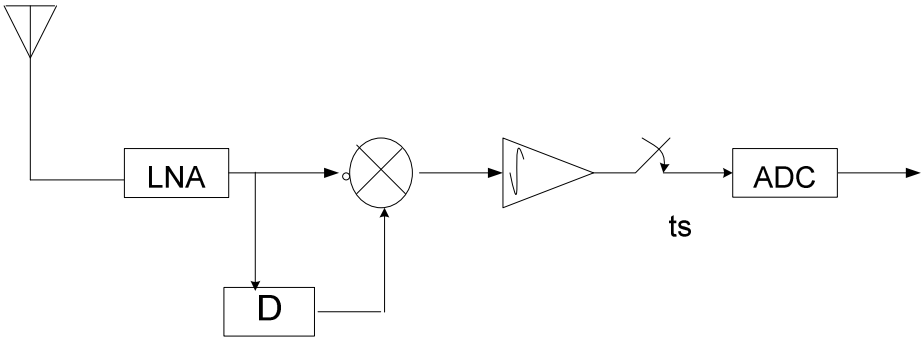


Figure 2.4 Non-Coherent Receivers.

2.1.6.2 MB-OFDM

Recent Wi-Fi products use a technique of wireless communication called as OFDM (orthogonal frequency division multiplexing). As OFDM is the latest architecture trend in Wi-Fi products, in order to take advantage of the design experience OFDM technique have been proposed for realizing UWB systems.

MB-OFDM systems achieves UWB communication by adding together multiple orthogonal bands of communication, i.e. frequency division multiplexing. Total spectrum is divided in different bands and each band is divided into sub-bands (each 528MHz wide to satisfy UWB definition). A time interleaving technique was proposed to specify which sub-band would be active for communication at any given time.

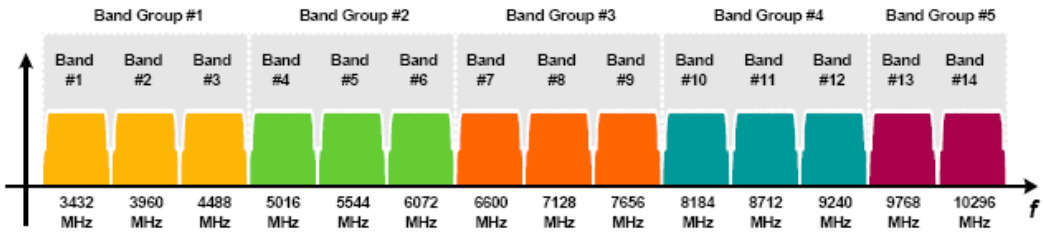


Figure 2.5 Frequency band plan of the MBOA proposal for IEEE 802.15.3a PHY

The PHY layer of proposed MB-OFDM is basically a descendant from 802.11 a/g systems. These systems have potential of achieving high data rates. But they suffer high power consumption and high circuit complexity. Figure 2.6 shows the block diagram of MB-OFDM receiver.

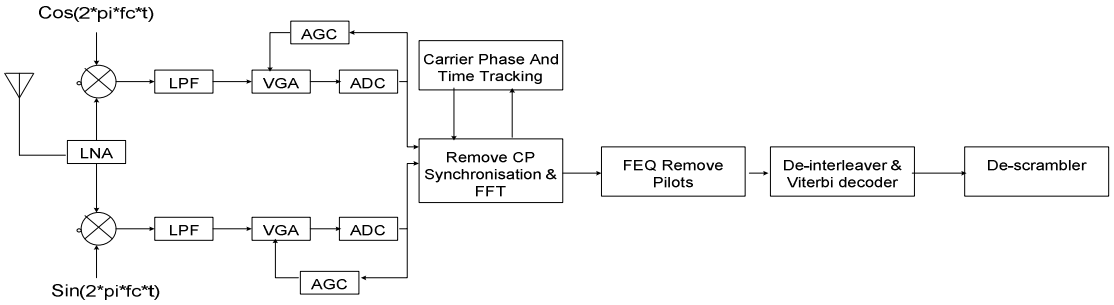


Figure 2.6 Typical UWB MB-OFDM receivers.

From the figure it is evident that this architecture is much more complicated compared to IR-UWB systems and also they consumes more power. This is the reasons this system architecture is not chosen for IEEE 802.15.4 standard.

In this thesis Analog correlator is designed to operate at 22-29GHz frequency for IR-UWB radar applications.

CHAPTER 3

ANALOG CORRELATOR

This chapter reviews the theory of Analog correlator. Analog correlator acts as a detector which detects the incoming RF signal. In order to understand the Analog correlator we will review the UWB receiver block diagram which was discussed in chapter 2.

3.1 Block Diagram of IR UWB Receiver

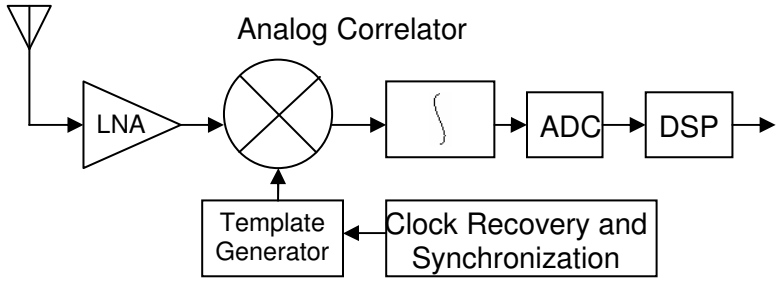


Figure 3.1 Block Diagram of IR UWB Receiver

Figure 3.1 shows the basic block diagram of IR UWB receiver that can be used for vehicular radar applications in 22-29GHz frequency band. Received signal acts as an input to low noise amplifier (LNA). LNA should have wideband matching from 22-29GHz. As it can be seen from the figure Analog Correlator has two inputs, one is for received signal which is amplified by LNA and other input is for locally generated template signal. Clock recovery and synchronization along with sequence generator, synchronizes the template signal to the received signal. Thus multiplier which is the first block of the correlator senses both the inputs at the same time and multiplies the signal. Integrator integrates this signal and produces the input for ADC. Analog correlator acts as a matched filter which through multiplication and integration maximizes the SNR at the output of correlator. Also it can be seen that multiplication of two signals with same frequencies generate two frequency components one low frequency (DC signal) and signal with twice the frequency of individual signal. But integrator is low pass

filter thus low frequency signal is converted to digital domain by the ADC. Once signal is digitized then signal processing can be used on this signal to extract all the information from this signal.

3.1.1 *Types of Correlator*

Analog correlator used in IR UWB receiver correlates the received signal to the locally generated template signal in analog correlator. This function of correlation can also be done in the digital domain. Thus correlator can be classified as Analog correlator or Digital correlator. In order to realize the digital correlator first received signal should be converted to digital domain. In this application the input signal in frequency range of 22-29GHz .In order to convert this signal to digital domain it is required to have sampling frequency of ADC to be at least 58GHz according Nyquist criterion. This poses unrealistic requirements on ADC. But if correlation function is realized in Analog domain then as mentioned earlier multiplier and integrator converts the high frequency signal to low frequency signal. Thus unrealistic requirements on ADC relieved.

3.2 Matched Filter

As explained earlier that analog correlator is a matched filter lets investigate the theory of match filter which followed by the example of signal detection by Analog correlator.

3.2.1 *Definition of Matched Filter*

If s(t) is any waveform, then a filter which is matched to the s(t) is by definition, one with the impulse response

$$h(t) = s(t_m - t) \qquad (3.1)$$

Where t_m is arbitrary constant. Figure 3.2 shows how exactly h(t) looks like.

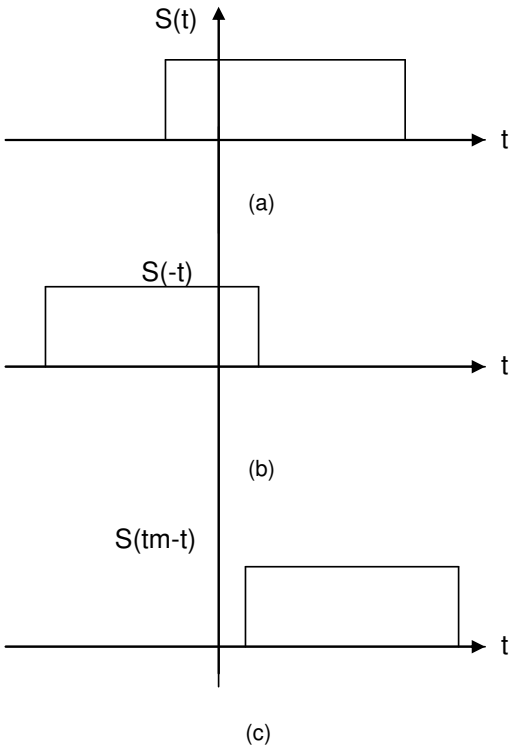


Figure 3.2 (a) shows the signal waveform (b) shows reversed signal in time domain s(-t) and (c) shows signal shifted by constant tm, s(tm-t) [15]

3.2.2 *Need of Match Filters in Radar Receivers*

In case of radar signal which is scattered or reflected by the target contains the information about the target. The reflected signal while coming to the receiver front end get contaminated by the noise in the channel. Also when such signal is received by the front end of receiver it also adds the noise. It is required by the detector to extract the required information form a such a signal which contains noise.

In typical communication systems it is required to detect the signal in noisy environment while is case digital communication systems decision has to be made from received signal if logic 0 or logic 1 is transmitted. Thus the appropriate figure of merit in case of digital systems is probability of error. In case of radars it's not only the decision making about logic 0 or logic 1 but we also need to extract the information about target like the distance, velocity etc.

Before discussing mathematically how to detect the signal consider the following figure.

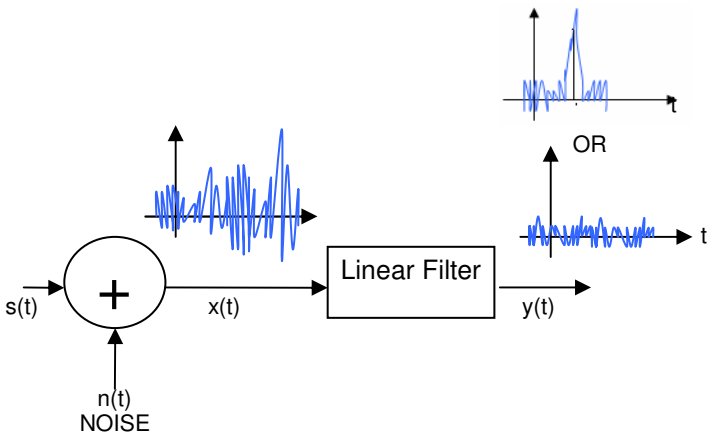


Figure 3.3 Operation of Matched Filter

Let's consider the received signal is r(t). This signal might be a combination of both noise signal n(t) of power density $N_0/2$ watts/cps and signal s(t) which is returned from the target. If there is no signal returned from the target then r(t) will only contain noise signal n(t). Thus by operating on r(t) it is required to find out if the received signal contains information signal s(t) or not. This looks like a filtering function where it is required to filter out information signal from the noise signal. Let's consider linear filter is doing this job. As filter is assumed to be linear its output y(t) can be represented as follows

$$y(t)= y_s(t) + y_n(t) \qquad (3.2)$$

Where $y_s(t)$ is filter out put due to signal and $y_n(t)$ is the filter output due to noise signal. Whenever information signal s(t) is present in r(t) it is required for the filter to increase the instantaneous power of the $y_s(t)$ compared to $y_n(t)$. Thus it is required for the filter to have maximum signal to noise ratio (SNR).

3.2.3 Mathematical Derivation of match filter

Let's assume that signal r(t) received at instants $T=t_0$ contains information signal S(t). Thus it is necessary for the filter to give maximum SNR at $T=t_0$. Let's assume that transfer function of the filter is $G(j2\pi f)$.

Output noise power density at the output of the filter is given by

$$\frac{N_0}{2}\int_{-\infty}^{\infty}\left|G(j2\pi f)\right|^2 df \qquad (3.3)$$

Also if s(t) is the signal then S(j2πf) is the spectrum of the signal. Then output of the filter is given by $S(j2\pi f) * G(j2\pi f)$ and out of the filter at T=t_0 can be found out by inverse Fourier transform

$$y_n(t_0) = \int_{-\infty}^{\infty} S(j2\pi f)G(j2\pi f)e^{j2\Pi ft_0}df \tag{3.4}$$

The signal to noise ratio is given by the ratio of the square of eq 3.3 and eq 3.2. It is required to have maximum value of this ratio.

$$\rho = \frac{2\left[\int_{-\infty}^{\infty} S(j2\pi f)G(j2\pi f)e^{j2\Pi ft_0}df\right]^2}{N_0\int_{-\infty}^{\infty}\left|G(2\pi f)\right|^2 df} \tag{3.5}$$

It can be seen that numerator of the expression 3.4 is real. And indentifying G (j2πf) as f(x) and $S(j2\pi f)e^{j2\pi ft_0}$ as g(x) Schwarz inequality gives

$$\left|\int f(x)g(x)dx\right|^2 \le \int\left|f(x)\right|^2 dx\int\left|g(x)\right|^2 dx \tag{3.6}$$

If $f(x) = K * g(x)$ hence

$$G(j2\pi f) = KS^*(j2\pi f)e^{-j2\Pi ft_0} \tag{3.7}$$

Thus by using expression 3.5 one can obtain

$$\rho \le \frac{2}{N_0}\int_{-\infty}^{\infty}\left|S(j2\pi f)\right|^2 df \tag{3.8}$$

As $\left|S(j2\pi f)\right|^2$ is the energy of the signal 3.7 can be written as

$$\rho \le \frac{2E}{N_0} \tag{3.9}$$

Thus filter with transfer function $G(j2\pi f) = KS^*(j2\pi f)e^{-j2\Pi ft_0}$ maximizes the SNR at T=t_0

Let signal received is given by

$$r(t) = s(t) + n(t) \tag{3.10}$$

Filter impulse response is given by

$$h(t) = S(t_0 - t) = p(t_0 - t) \tag{3.11}$$

output of the filter is the convolution of r(t) and h(t)

$$y(t) = \int_{\infty}^{\infty} r(x)h(t-x)dx \tag{3.12}$$

Where $h(t) = p[t_0 - (t-x)] = p(x + t_0 - t)$ thus substituting $h(t)$ as $p(x + t_0 - t)$

$$y(t) = \int r(x)\, p(x - t_o - t)dx \tag{3.13}$$

at $t=t_0$

$$y(t_0) = \int_{0}^{t_0} r(x)\, p(x) \tag{3.14}$$

Thus matched filter is called as correlator and can be implemented as multiplier and integrator.

3.3 Detection of Signal Using Analog correlator

This second demonstrate how analog correlator detects the incoming signal. Figure 3.4 shows the Correlator part of UWB receiver.

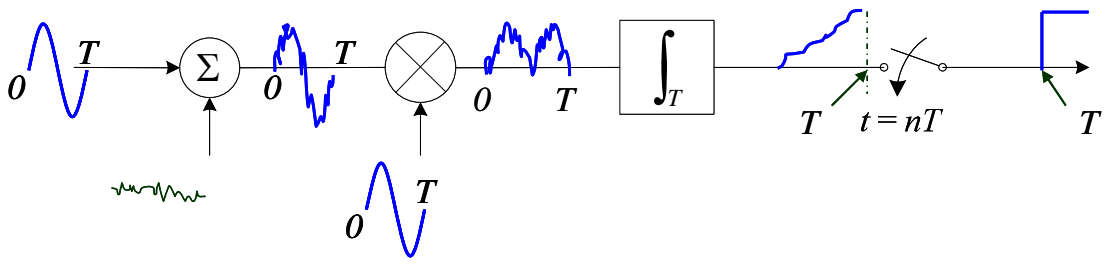


Figure 3.4 Illustration of signal detection using analog correlator

As shown in the figure one of the input of the multiplier is the noisy signal which can be considered as signal coming from target which mixed with noise. Other input to the multiplier is called as template signal which is same as transmitted signal. Multiplier multiplies these two signals. This is signal is integrated over the time period of the signal. At t=T switch is closed that is output of the integrator is sampled at every time period. Thus output received is maximum and without noise.

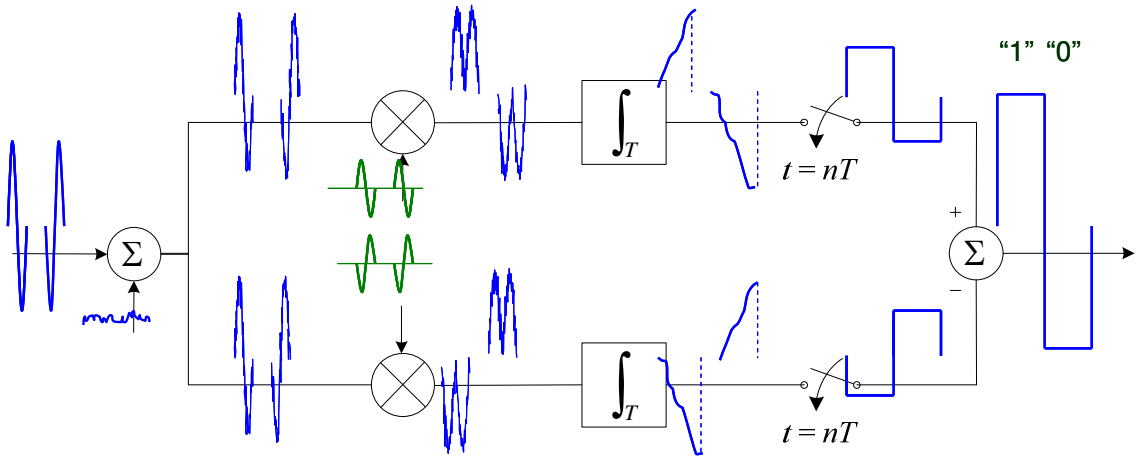


Figure 3.5 Illustration of Signal detection in two dimensional signal spaces.

Figure 3.4 shows how signal detection is done in two dimensional signal spaces. Here it is assumed that BPSK modulation scheme is used to modulate the signal. For logic one signal is transmitted as it is while for transmitting logic 0 signal is transmitted with 180^0 phase shift. In order to detect such a signal two correlator are required. Both the multipliers receive the same signal but the locally generated template signals for both the multipliers have 180^0 phase difference. Rest of the operation is same.

3.4 Circuit level implementation of Analog correlator

Analog correlator is the combination of two blocks of multiplier and integrator. These two blocks can be realized as two different blocks or can be integrated as one block. This section discusses basic idea of analog multiplication and integration.

3.4.1 *Multiplier*

Multiplication of two signals with CMOS can be understood by examining the basic MOSFET current equations. Drain current MOSFET when it operates in linear and saturation region is given by following equations.

$$I_d = K\left[V_{gs} - V_t - \frac{v_{ds}}{2}\right]v_{ds} = K\left[v_{gs}v_{ds} - v_T v_{ds} - \frac{v_{ds}^2}{2}\right]$$

For $v_{gs} > v_T, v_{ds} < v_{gs} - v_T$ (3.15)

$$I_d = \frac{K}{2}\left[v_{gs} - v_T\right]^2 = \frac{K}{2}\left[v_{gs}^2 - 2v_{gs}v_T - v_T^2\right], \quad (3.16)$$

For $v_{gs} > v_T, v_{ds} > v_{gs} - v_T$

Equation 3.15 gives the equation drain current when MOSFET operates in linear region. It can be seen that multiplication can be realized by $v_{gs} * v_{ds}$ term or by v_{ds}^2. Drain current of MOSFET in saturation region is given by equation 3.16. From this equation it is clear that multiplication can be realized by $(v_{gs} - v_T)^2$ or by $v_{gs} * v_T$. But when from the equations it is evident that while having the required product there are many unwanted terms in the equations. In order to have pure multiplication of two signals it is required to cancel out these unwanted terms. There are basic two cancellation methods as described as follows.

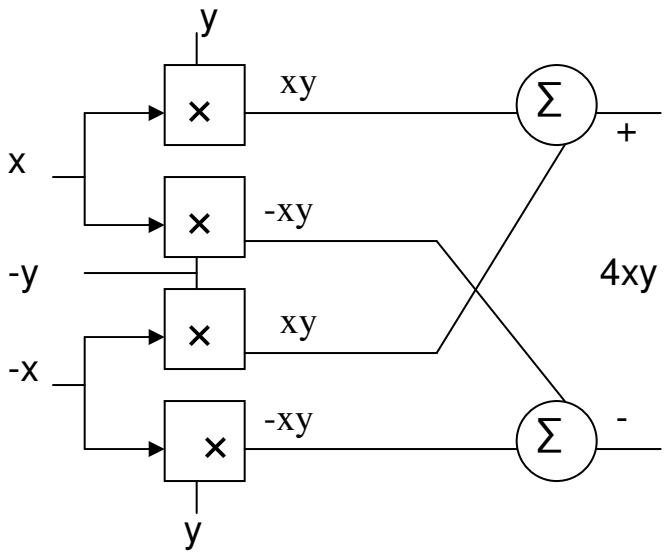


Figure 3.6 First method of cancellation [17]

In this case there are four multipliers and each has two inputs. Each of these is single quadrant multipliers .These type of multipliers are generally implemented by vgs*vds terms. This method multiplies the signal and cancels out the higher order components as follows.

$$\left[(X+x)(Y+y)+(X-x)(Y-y)\right]-\left[(X-x)(Y+y)+(X+x)(Y-y)\right] = 4xy \quad (3.17)$$

Here X and Y are DC components of signals or large signals while x and y are small signals.

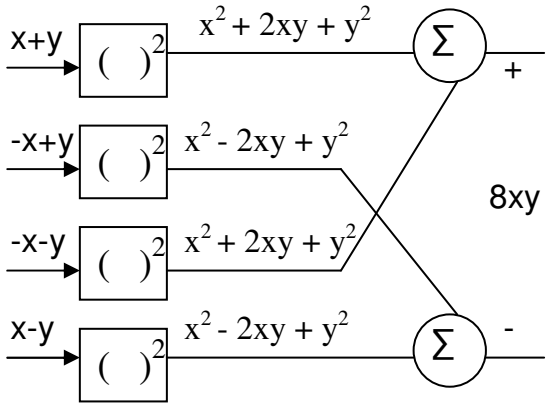


Figure 3.7 Second method of cancellation [17]

In this type of multiplier which works on the principle of square law of MOSFET's Cancellation achieved by this method is given by following equation.

$$\begin{aligned}&\left[\{(X+x)+(Y+y)\}^2+\{(X-x)+(Y-y)\}^2\right]\\&-\left[\{(X-x)+(Y+y)\}^2+\{(X+x)+(Y-y)\}^2\right]=8xy\end{aligned} \tag{3.18}$$

Thus multiplication of two signals using MOSFET is actually composed of two processes, first multiplication and second is the cancellation of unwanted terms in the multiplication.

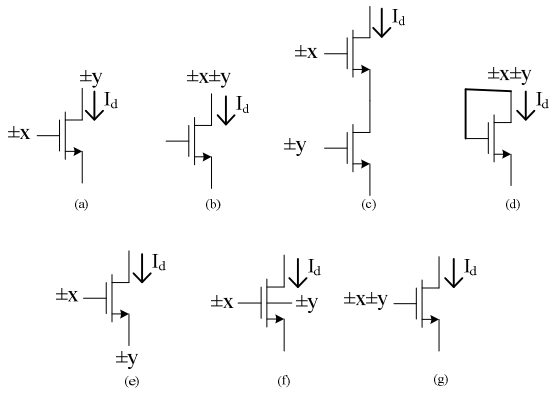


Figure 3.8 Different methods of injecting voltage signals [17]

3.4.2 *Integrator*

Function of integrator is to carry out the integration of the multiplied signal. Integration function can be realized by a typical Gm-C integrator. In this case it adds one more block to the circuit and hence will have more power dissipation and also will consume more chip area. Thus it is advisable to combine both multiplication and integration by a single block. It will be explained in later section how to achieve this function.

3.5 Performance matrix of Analog correlator

Performance criterion of the correlator mainly depends on the performance of the multiplier. There are several parameters which are important in the design of multiplier. They are as follows.

1. Linearity – Analog multiplier is nothing but the combination of transconductance amplifiers arranged in a particular way. The input-output characteristics of typical transconductance amplifier are given by

$$i(t) \approx a_0 + a_1 x(t) + ... + a_n x^n(t) \quad (3.19)$$

This shows typical transconductance amplifier has many non-linear terms. But if input x(t) is small enough then we can neglect the higher order terms and the equation 3.18 can be approximated as

$$i(t) \approx a_0 + a_1 x(t) \quad (3.20)$$

Where a_0 is considered as operating point and a_1 the small signal gain. Thus as long as a1x(t)<<a0 then operating point of the amplifier is not disturbed and we can neglect the higher order terms. In case of analog multiplier we want out given by

Z= Kxy (3.21)

This is achieved by cancelling the higher order terms as explained in the figure 3.5 and 3.6

2. Power Consumption- In today's analog circuit design power consumption is one of the important parameters. But in this application power consumption is not very critical
3. Gain- It is difficult to define the gain of the multiplier. As output is function of both the inputs x and y. Also input and output's are at different frequencies. Thus borrowing the conversion gain

concept from the mixers. Voltage Conversion gain of the mixer is defined as the ratio of rms value of IF voltage to rms value of input RF voltage while power conversion gain of the mixer is given by IF power delivered to load divided by the available RF power from the source.

4. Bandwidth- Bandwidth is yet another important parameter. In this particular application correlator is working at 22-29GHZ this circuit should have input bandwidth of 29GHz to accommodate the incoming signal.
5. Isolation- Again isolation term is not defined for the multiplier but borrowing the definition from the mixers. In case of multiplier input port which receives the signal can be defined as RF port while the other input to which template signal is applied can be defined as LO port and output can be defined as IF port. In this particular application LO to RF isolation is very important. Template signal looks for the input signal. Thus if there is no input RF signal and if RF LO isolation is poor then template signal can get multiplied to itself and multiplication can appear at the output. Also RF –IF isolation is also very important.
6. Noise Figure- Correlator is the second block in the RF front end after LNA. Thus it is required to have low noise figure. Noise figure around 15-20dB is fair enough.

3.6 Different structure of Analog Correlator and UWB multipliers

There are different structures implemented for analog correlator and UWB multipliers. CMOS technology and SiGe technology is used for the implementation. Most of them are designed for 3.1-10.6GHz UWB communication applications. Analog correlator design for 22-29GHz application in 90nm CMOS technology is not done to date. Most of the correlator and multipliers designed use Gilbert cell core as multiplier [3, 4, 5 and 9] .While multipliers designed in [7] uses programmable transconductors as multiplier. Most of the designs are done in 0.18μ or 0.25 μ. Figure 3.9 shows typical block diagram of analog correlator [3].

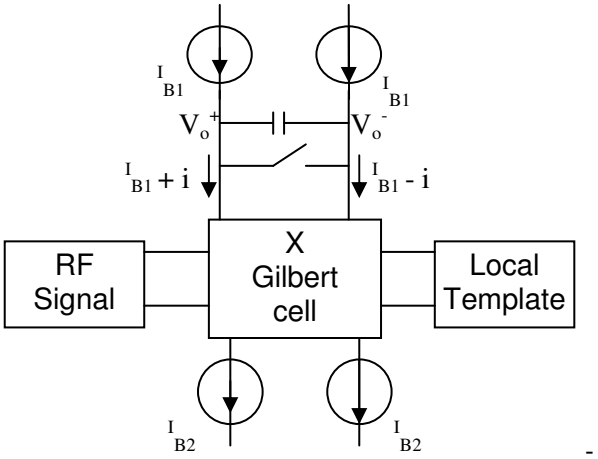


Figure 3.9 Block Diagram of Analog Correlator

It can be seen here that Gilbert cell is used as multiplier which multiplies RF and template signals. Differential current i contains the multiplication of two input signals. This differential current is integrated on the capacitor. Thus function of multiplication and integration is done by a single block. Figure 3.10 shows the circuit of typical Gilbert cell acting as multiplier.

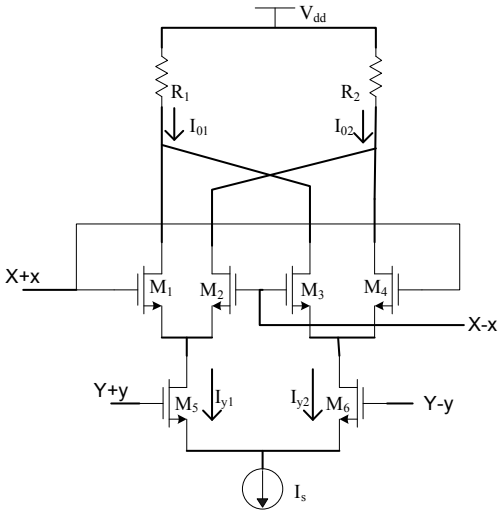


Figure 3.10 Gilbert cell Multiplier

There are three levels of transistors. Uppermost transistors has X+x and X_x as inputs while next two transistors has Y+y and Y-y as inputs. Last transistor acts as a current source. Output current of Gilbert cell cab be given as

$$I_0 = I_{01} - I_{02} = 2\sqrt{2KK_x xy} \tag{3.22}$$

Gilbert cell can also be implemented without using the tail current source as well. Figure 3.11 shows Gilbert cell without tail current source.

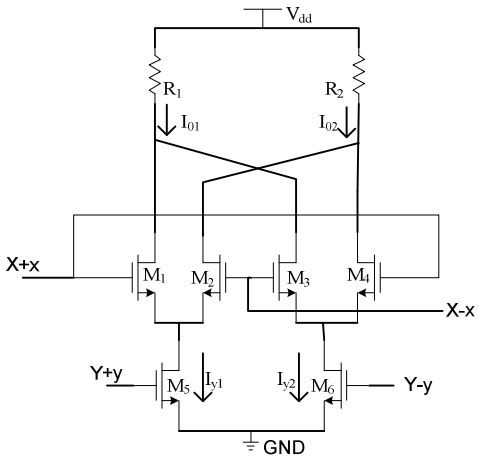


Figure 3.11 Gilbert cell Multiplier without Current Source

This increases the linearity and input range of the circuit. But common mode rejection of the circuit is decreased. There are many ways suggested to increase the gain and bandwidth of the Gilbert cell (9).

As mentioned earlier these are done in 0.18 μ or 0.25μ technologies. These technologies use power supply voltages of 1.8 and 2.5V respectively. With such a supply voltage it is possible to stack 3 or 4 transistors on top of each other to have more gain. But power supply used in 90nm is 1.2 V which makes it difficult to stack more than three transistors (including load) and keep them all in saturation. Thus it is required to find different architectures which can inherently have more gain.

CHAPTER 4

PROPOSED ARCHITECTURE

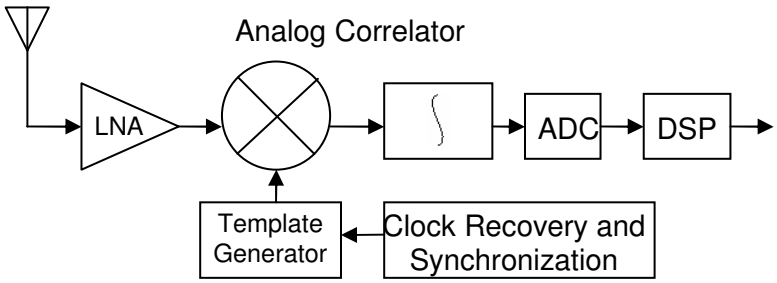


Figure 4.1 Basic structure of UWB radar receiver

Figure 4.1 shows the basic UWB radar receiver structure. This structure is simulated in ADS along with transmitter to obtain the template and RF signals. In this system simulation 22-29 GHz signal generated by shaping Gaussian mono pulse with band pass filter. This is the information signal which is transmitted through the channel. Channel is modeled to have channel delay and the loss. Also 5GHz white noise is added to the main transmitted signal. Such a signal is received by receiving antenna which has a gain of 15dB and amplified by LNA which has gain of 10dB. The signal after LNA has a amplitude of 1mV peak to peak and it is one of the inputs to the correlator. Signal obtained after LNA in system simulation is used for all simulations in the thesis. The other input to the correlator is locally generated template signal which is same as the transmitted signal. Amplitude of this signal can be adjusted.

In Analog correlator structure analog multiplier is very important. Multiplier receives both RF signal from LNA, which is the first block in the RF front end, and it multiplies this signal with the locally generated template signal. Received signal is very weak signal thus multiplier should have enough gain. Also both template and received signal are large bandwidth, in this case 22-29GHz signal. Thus multiplier is a high frequency circuit and should have large bandwidth. As explained in the previous chapter Gilbert cell is the most common multiplier which is employed in many multipliers which are designed for 3.1-

10.6GHz UWB communication application. Here we start with basic architecture which is based on programmable transconductance explained in [10] and [17]. This architecture is chosen as it has more gain compared to Gilbert cell as explained below.

All the simulations are performed in CADENCE Spectre and SpectreRF. Technology used for the simulations is IBM90nm CMOS.

4.1 Basic Architecture

Figure 4.2 shows the basic architecture used in this work.

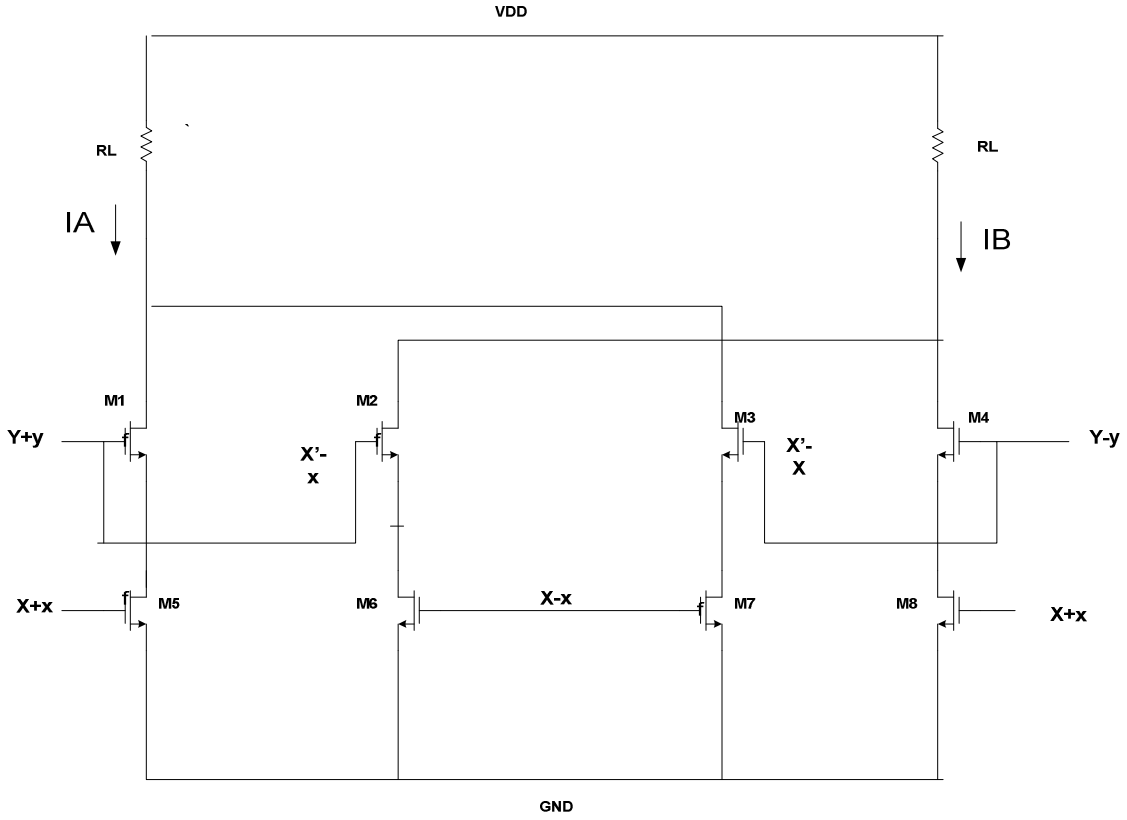


Figure 4.2 Basic architecture

This architecture uses MOS cascade concepts [10]. Architecture can be explained by considering two MOSFET connected in cascade fashion as shown in figure 4.3

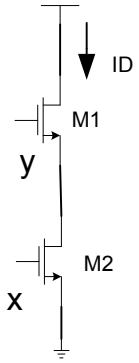


Figure 4.3 MOSFET connected in cascade fashion

If both transistors M1 and M2 are operating is saturation region and lets assume x and y are small signals. Then M2 acts as simple common source amplifier then voltage at the drain of M2 will be 180^0 out of phase with its input and hence it is –x. Now Vgs of M1 is (y+x) and hence the drain current which is given by

$$Id = K(Vgs - Vt)^2 \tag{4.1}$$

Will contain multiplication of x and y. But as it can be seen this multiplication will also have many other terms which are not desired and should be cancelled out. As a result we need to use architecture shown in figure 4.2 which is a four quadrant multiplier. In this figure all transistors are working in saturation region hence saturation region current can be given as

$$Id = K(Vgs - Vt)^2$$

$$K = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right) \tag{4.2}$$

Let's consider current flowing through transistor M1 is Id_1 similarly currents flowing through M2-M9 are Id_2 –Id_8 respectively.

From 4.3 we can write current Id1 as

$$\sqrt{Id_1} = \sqrt{K_1}\left(Vgs_1 - Vt\right) \tag{4.3}$$

Multiplying both the sides by $\sqrt{Id_1}$

$$Id_1 = \sqrt{K_1}\left(Vgs_{1\_} Vt\right)\sqrt{Id_1} \tag{4.4}$$

But $Id_1 = Id_5$ thus $\sqrt{Id_1} = \sqrt{Id_5}$

$$\sqrt{Id_5} = K_5(Vgs_5 - Vt) \tag{4.5}$$

Substituting equation (4.5) in (4.4)

$$\sqrt{Id_1} = \sqrt{K_1 K_5}\left(Vgs_1 - Vt\right)\left(Vgs_5 - Vt\right) \tag{4.6}$$

Let $Vgs_1 = y - V_o$, $Vgs_5 = x$ and $\sqrt{K_1 K_5} = K$, thus

$$Id_1 = K(y - V_o - Vt)(x - Vt) \quad (4.7)$$

Let $-V_o - Vt = a$ and $V_t = b$

$$Id_1 = K(y - a)(x - b) \quad (4.8)$$

Similarly equations for Id_2 ID_3 and Id_4 can be obtained

$$Id_2 = K(y - a)(-x - b) \quad (4.9)$$
$$Id_3 = K(-y - a)(-x - b) \quad (4.10)$$
$$Id_4 = K(-y - a)(x - b) \quad (4.11)$$

Now output current is given by

$$I_A - I_B = (Id_1 + Id_3) - (Id_2 + Id_4) \quad (4.12)$$
$$I_A - I_B = (Id_1 - Id_2) + (Id_3 - Id_4) \quad (4.13)$$

Substituting (4.8) to (4.13) and simplifying we can obtain

$$I_A - I_B = 4 \cdot K \cdot x \cdot y \quad (4.14)$$

(W/L) of M1-M4 are equal and (W/L) of M5-M8 are same thus

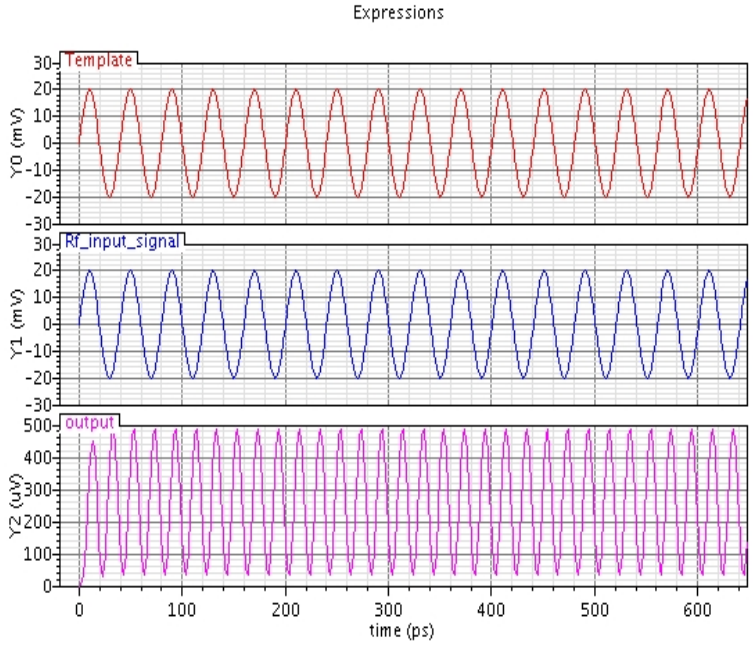
$$K_1 = K_2 = K_3 = K_4 \quad (4.15)$$

$$K_5 = K_6 = K_7 = K_8 \quad (4.16)$$

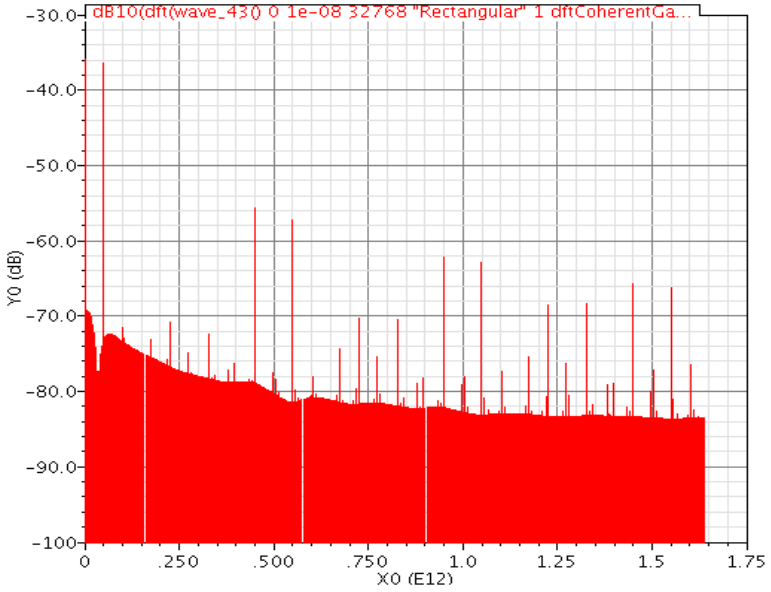
Thus output current can be written as

$$I_A - I_B = 4 \cdot \sqrt{K_1 K_5} \cdot x \cdot y \quad (4.17)$$

It can be seen that differential output current of this current is more than that of Gilbert cell. This circuit is designed for the application and figure 4.4 shows the simulation results. This architecture is first verified by applying sine wave inputs and by taking Fourier transform of the input to verify the output frequencies present in the circuit. Sine waves of 25GHz and 40mV peak to peak voltage are applied to transistors.



(a)

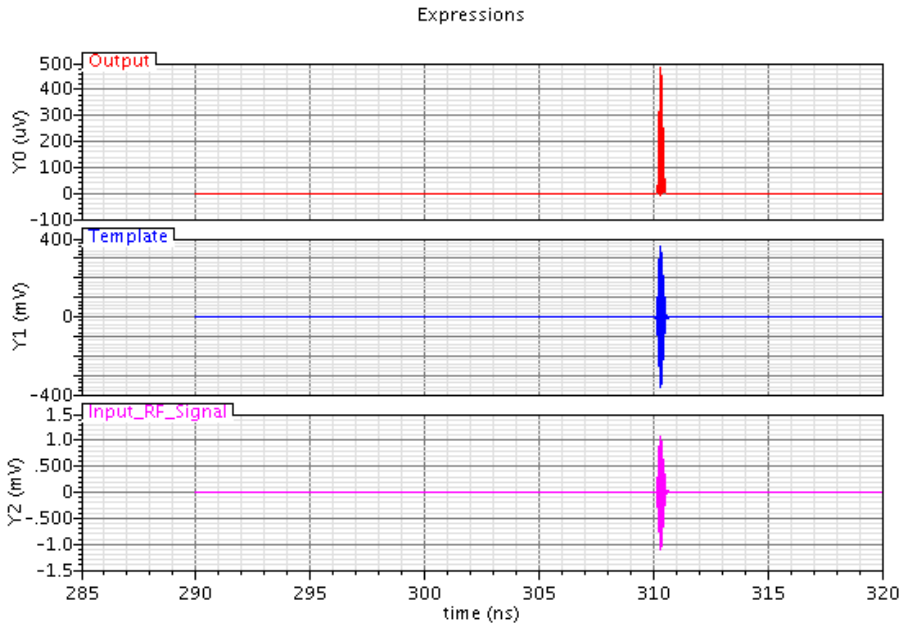


(b)

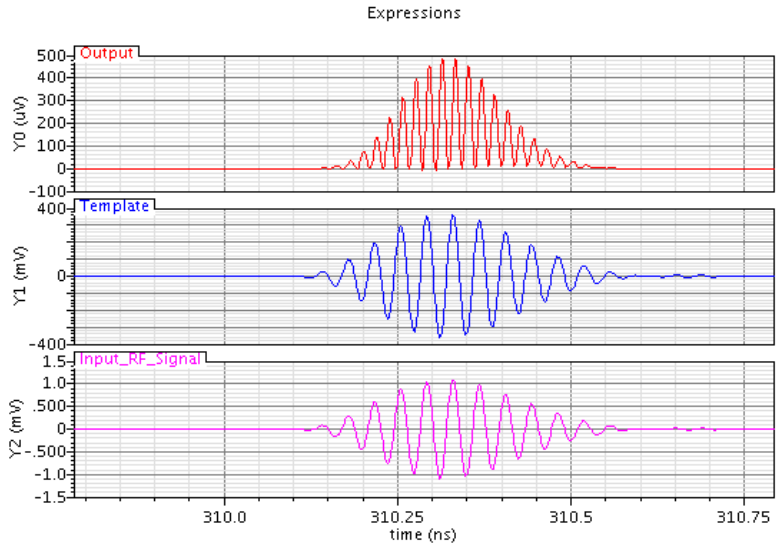
Figure 4.4 (a) Simulation results when template and received signal are both of 25GHz sinusoidal.(b) Fourier transform of the output shown in (a)

Figure 4.4 (a) show the simulation results when the circuit receives both inputs as sine waves. Figure (b) shows FFT of the output signal. In the figure 4.4 (a) Y0 is the one of the sine wave inputs while Y1 is another sine wave input. Y2 is the output of the circuit whose magnitude is about 480μV. Figure 4.4 (b) shows the frequency spectrum of the output signal Y2.By theory multiplication of two frequencies produces sum and difference frequencies. Thus output of the circuit when exited by two signals of 25GHz frequencies should produce difference frequency of (25GHz-25 GHz) which is 0Hz and sum frequency of (25 GHz + 25 GHz) 50GHz. output spectrum shows two peaks at frequency 0Hz and at 50GHz.This verifies the theory and we can say circuit functioning as per theory.

Now Input RF signal is applied to bottom transistors (M5-M9) while template signal is applied to upper transistors (M1-M4). These both signals as explained are generated in ADS system simulations.



(a)



(b)

Figure 4.5(a) Simulation Results for the architecture in fig 4.2 (b) zoomed view

In the figure 4.5 Y0 is the output signal which is about 450μV while Y1 is the template signal whose magnitude is 700mV peak to peak. Y2 is the received RF signal whose magnitude is 2mV peak to peak. It can be seen that output voltage is the multiplication of the template signal and received RF

signal. But the output voltage is around 450μV. Gain of the circuit is defined as the ratio of output signal to input RF signal.

$$Gain = 20\log\left(\frac{OutputVoltage}{InputRFvoltage}\right)$$

In this circuit gain is -13.97dB which is very small. As given by equation 4.17 gain can be increased by increasing (W/L) ratio of upper transistors (M1-M4) or lower transistors (M5-M8). Gain can also be increased by increasing load resistor. If (W/L) ratio of bottom transistors (M5-M8) is increased then total current in the circuit will increase. This will cause more voltage to drop across load resistors. In 90nm CMOS technology supply voltage used is only 1.2V. If large voltage drops across load resistors then it will be difficult to keep transistors (M1-M5) and (M5-M8) in saturation region. If (W/L) ratio of upper transistors (M1-M4) is increased then it will increase the capacitance at the output node and hence will degrade the frequency response. Also increasing the (W/L) ratio of upper transistors (M1-M4) will decrease drain to source voltage of these transistors in order to keep the same current flowing through them. This might take these transistors out of saturation region. Increasing load resistance affects the same way. Increasing load resistance will make more voltage to drop across it as result transistors may not remain in saturation region. Also increasing the resistance affects the frequency response of the circuit. Thus it is required to increase the gain of the circuit without changing operating region of transistors and affecting frequency response.

4.2 External Current Source to increase gain

Most common way of increasing the gain is shown in figure 4.6 and explained in [20] this method is called current injection method.

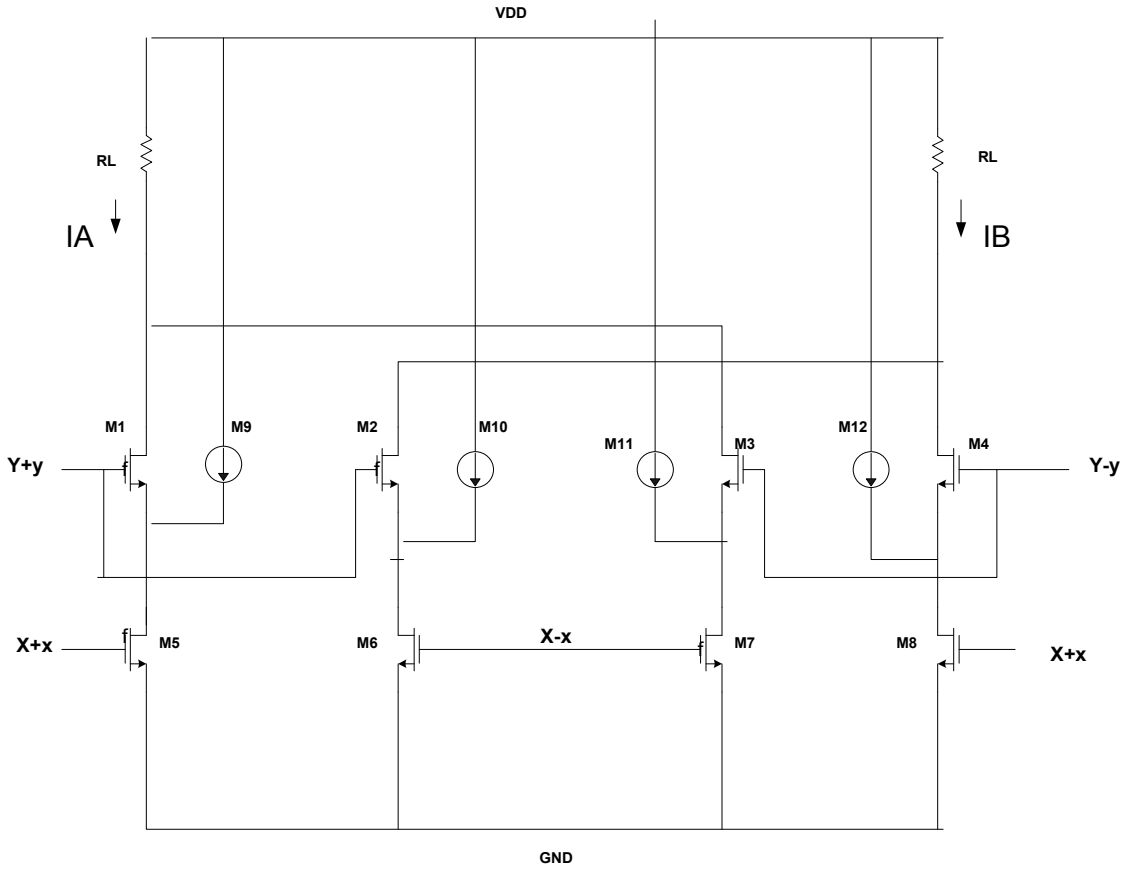


Figure 4.6 Current sources to increase gain

Figure 4.6 shows that current sources (M9-M12) used to increase the gain of the architecture. By adding these current sources current through (M5-M12) can increased without increasing current through transistors (M1-M5) and load resistors. This can be done by increasing (W/L) of bottom transistors. Thus again by observing equation 4.17 by increasing (W/L) ratio of bottom transistors we can increase the gain of the circuit. By doing this operating region of transistors are not changed. These current sources are generally implemented by PMOS transistors. But here they are implemented by NMOS transistors reason for which will be explained shortly.

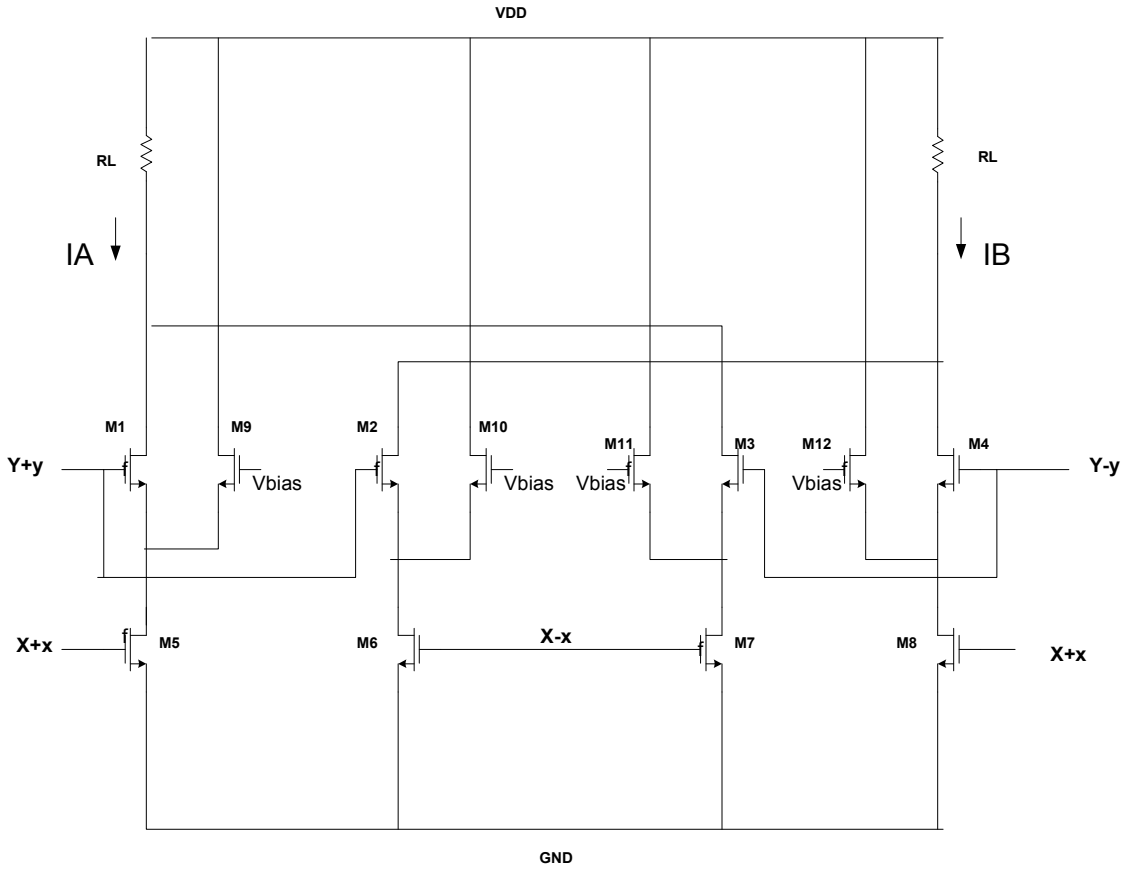
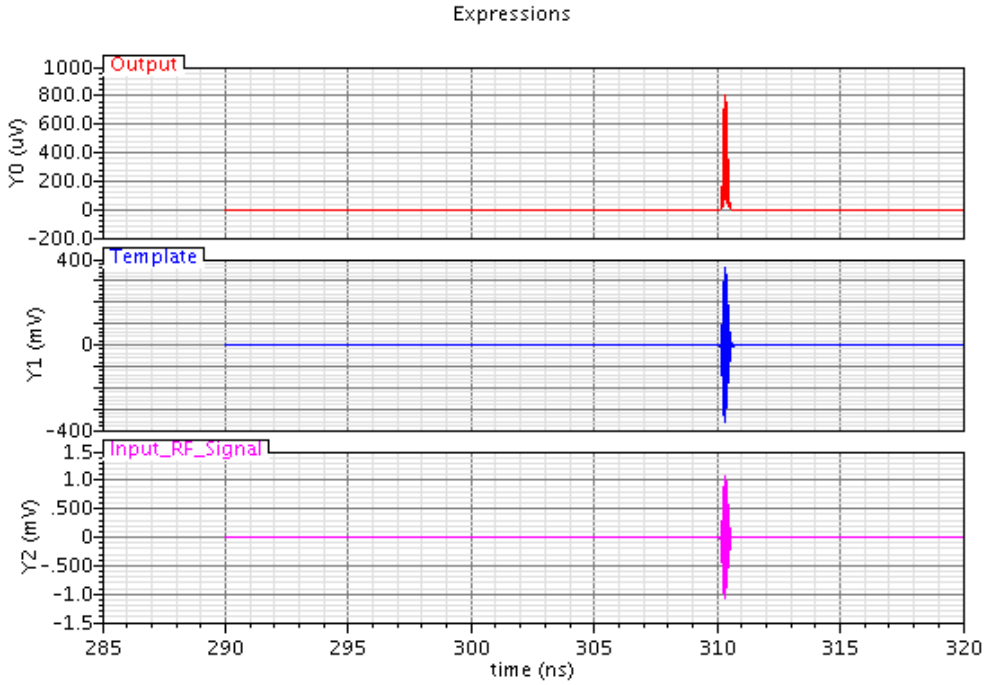
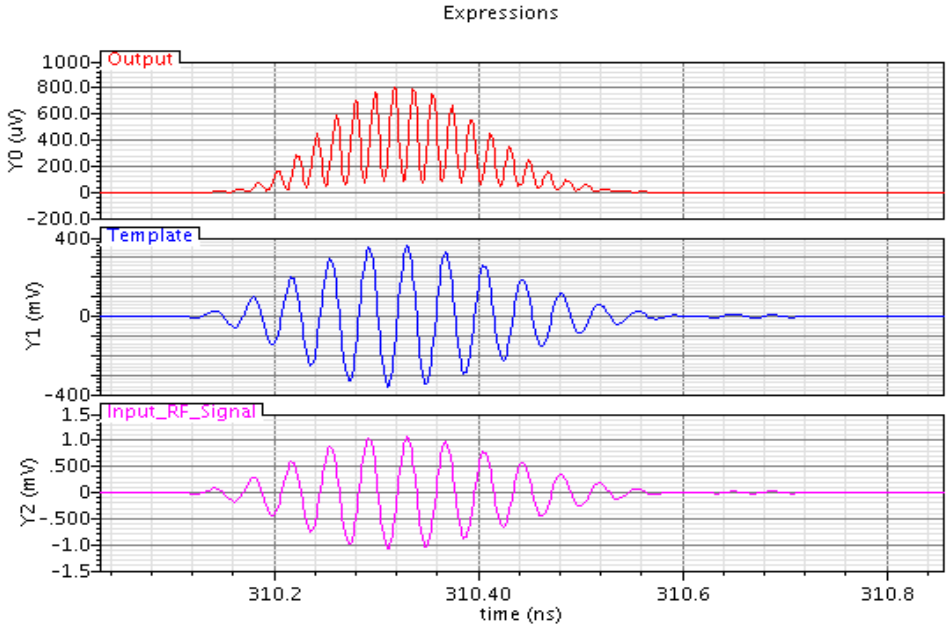


Figure 4.7 Current sources implemented by NMOS transistors

Figure 4.7 shows transistor (M9-M12) act as current sources. Vbias is the DC bias voltage used to bias these current source transistors in saturation region. Figure 4.8 shows the simulation results for the above circuit. Received RF signal is applied to bottom transistors (M5-M8) and template signal is applied to upper transistors (M1-M4) while transistors (M9-M12) are acting as current sources.



(a)



(b)

Figure 4.8 (a) Simulation Results by adding current sources to increases gain (b) zoomed view

In the figure 4.8 Y0 is the output signal which is about 800μV while Y1 is the template signal whose magnitude is 700mV peak to peak. Y2 is the received RF signal whose magnitude is 2mV peak to peak. As output voltage is now 800 μV and hence gain is -7.9dB.Thus gain is increased from -13.97dB to -7.9dB.

4.3 Proposed Architecture

More gain of the multiplier is better because more is the gain lesser will specifications on ADC requirements. Gain of the circuit can be further increased if the small signal voltage is applied to the current source transistors (M9-M12) as shown in figure 4.7.

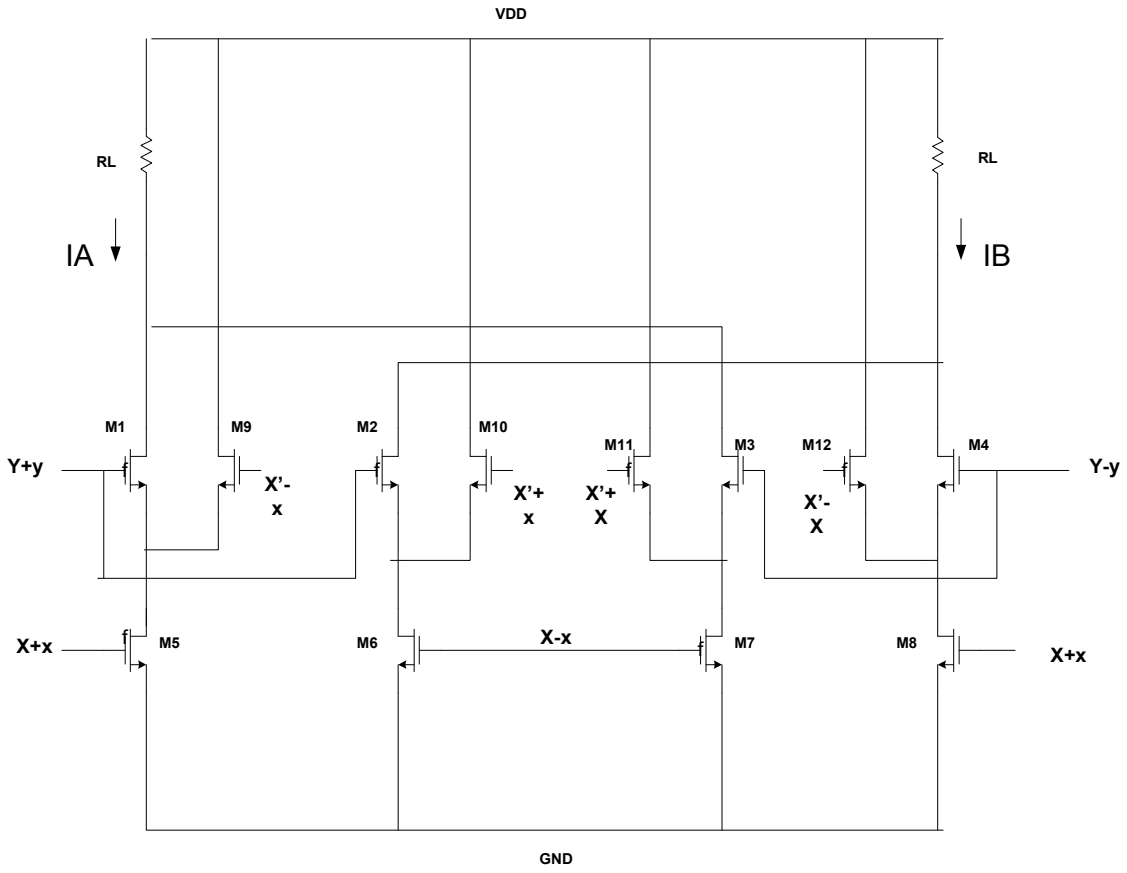


Figure 4.9 Proposed Architecture small signal voltage is applied to current source transistors

As shown in figure 4.9 small signal voltage is applied to current source transistors (M9-M12) in a particular way. If the bottom transistor (M5-M9) X+x as its input where X is large signal DC bias and x is

small signal then current source transistor connected at its drain has $X^{'}$-x as its input. Similarly if bottom transistor (M5-M12) has X-x input then current source transistor has X+x as input. Thus current source transistors (M9-M12) form yet another multiplier with M1-M4.

Most intuitive explanation of this architecture is as follows. Consider one branch of transistor M1-M5 and M9. By superposition theorem let's consider small signal is applied to only M5 which is x then voltage at the drain of M5 is –x as its common source amplifier. Now consider small signal is applied to only M9 and M9 acts as source follower. Then voltage at the drain on M5 is still –x. Thus both M5 and M9 forces current with same polarity through M1.As a result drain current through M1 is now because of two voltages hence more.

Let's investigate how this multiplier which is formed by transistors M1-M4 along with M9-M12 works. As explained above by superposition let's consider small signal is applied to M1-M4 while transistors M5-M8 have only DC biasing voltages. Thus transistors M5-M8 acts as current sources. Transistors (M1-M4) also have small signal voltage. Figure 4.10 shows resultant circuit.

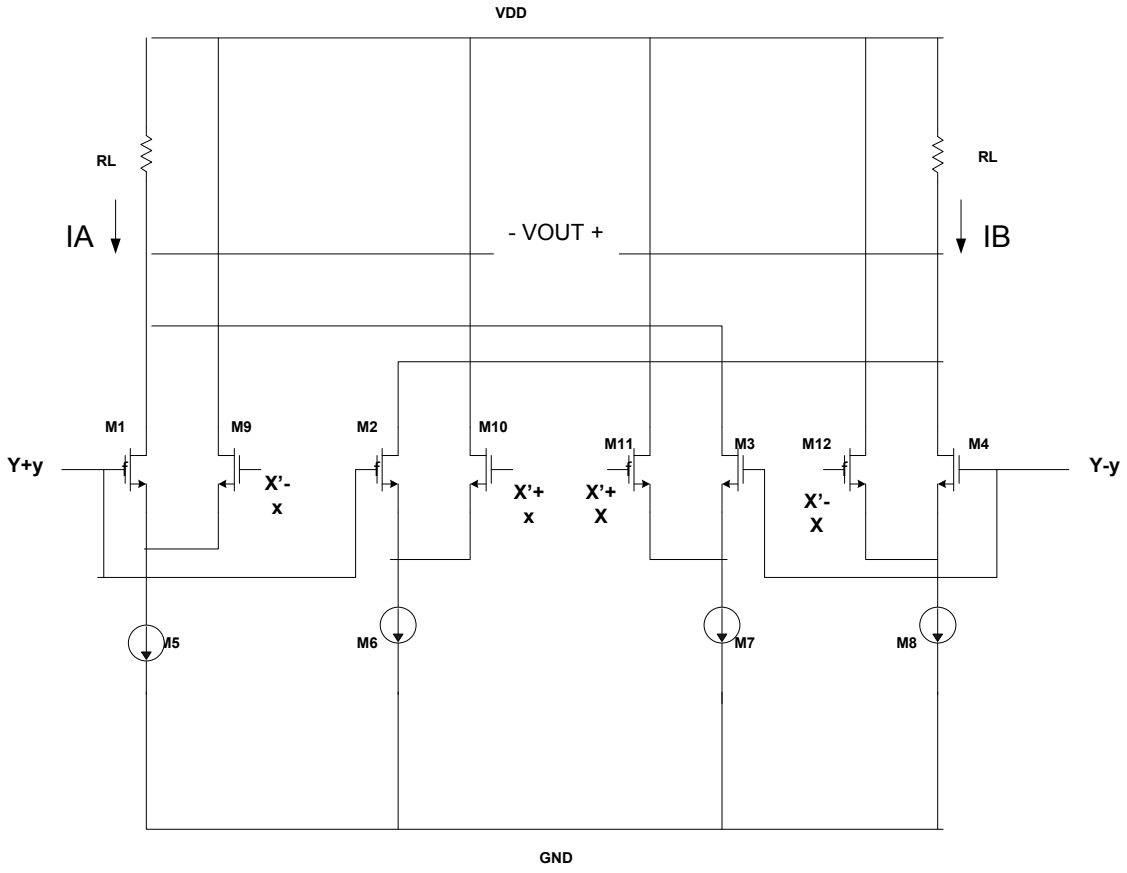


Figure 4.10 Transistors M5-M8 acting as current source.

If transistors M9-M12 have large widths then they acts source followers. Vgs of M9-M12 approaches to V_t .Thus we can assume voltages at the sources of M1-M4 same as that of gates of M9-M12 (by neglecting Vgs of M9-M12 which approaches to V_t). Figure 4.11 shows resulting circuit.

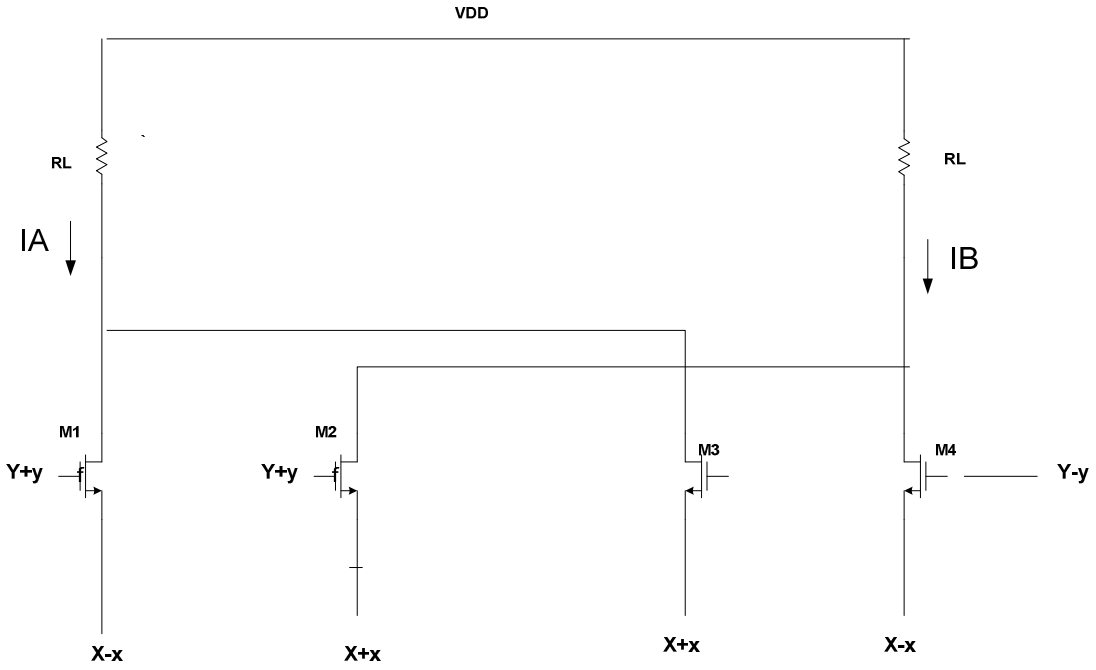


Figure 4.11 M9-M12 acting as sources follower

Let's assume currents flowing through M1-M4 as Id_1-Id_4. Id1 is given by

$$Id_1 = K_1(Vgs_1 - Vt)^2 \tag{4.18}$$

Recognizing Vgs as subtraction of two voltages we get

$$Id_1 = K_1[(Y + y) - (X - x) - Vt]^2 \tag{4.19}$$

Let $Y - X - Vt = Z$ thus Id_1 can be rewritten as

$$Id_1 = K_1[Z + (y + x)]^2 \tag{4.20}$$

Let $K_1 = K_2 = K_3 = K_4 = K$

$$Id_1 = K[Z + (y + x)]^2 \tag{4.21}$$

In similar way we can write equations for Id2- Id4 as

$$Id_2 = K[Z + (y - x)]^2 \tag{4.22}$$

$$Id_3 = K[Z + (-y - x)]^2 \tag{4.23}$$

$$Id_4 = K\left[Z + (-y + x)\right]^2 \tag{4.24}$$

Output current I_A- I_B cab be given as

$$I_A - I_B = \left(I_1 + I_3\right) - \left(I_2 + I_4\right) \tag{4.25}$$

$$I_A - I_B = \left(I_1 - I_2\right) + \left(I_3 - I_4\right) \tag{4.26}$$

Substituting (4.21) through (4.22) in equation (4.26) and simplifying we can get

$$I_A - I_B = 4 \cdot K \cdot x \cdot y \tag{4.27}$$

$$I_A - I_B = 4 \cdot K_1 \cdot x \cdot y \tag{4.28}$$

Thus total output current is the addition of (4.17) and (4.28) is given by

$$I_{out} = 4 \cdot \sqrt{K_1 K_5} \cdot x \cdot y + 4 \cdot K_1 \cdot x \cdot y \tag{4.29}$$

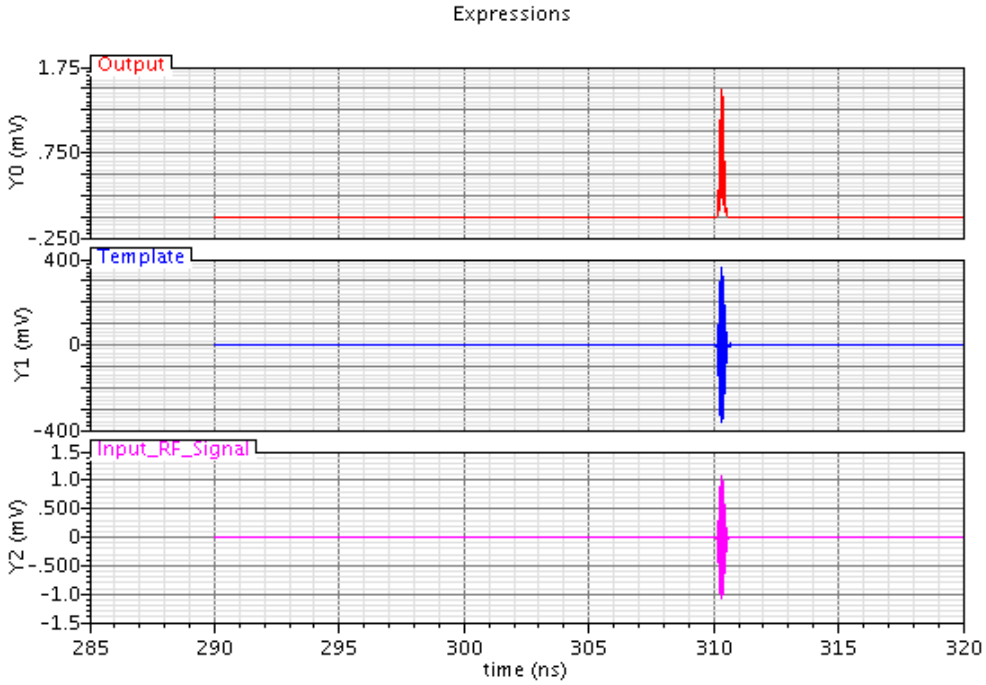
$$I_{out} = 4 \cdot \left(\sqrt{K_1 K_5} + K_1\right) \cdot x \cdot y \tag{4.30}$$

With same values of K it can be proved that Output current is equal to

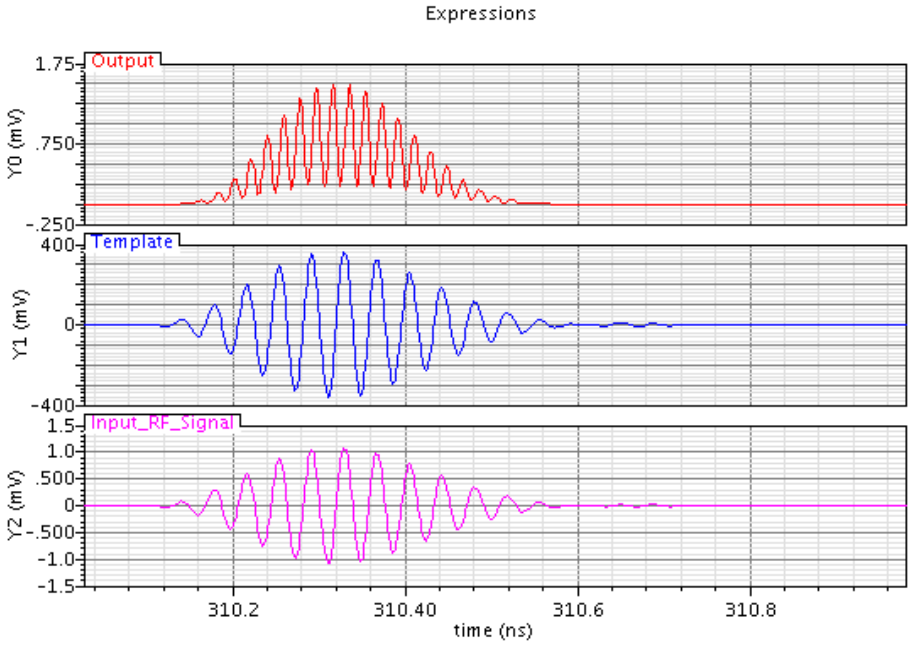
$$Iout = 2\sqrt{2} \cdot K \cdot x \cdot y \tag{4.31}$$

Thus this new architecture gives more gain compared to Gilbert cell and other multipliers described in (9) and (10).

Figure 4.12 shows the simulation results for the same architecture. Received RF signal is applied to transistors (M5-M8) and (M9-M12) as explained while template signal is applied to upper transistors (M1-M4).



(a)



(b)

Figure 4.12 (a) Simulation Results for Proposed Architecture (b) zoomed view

In Figure 4.12 Y0 is the output voltage which is about 1.5mV. Y1 is the template signal of about 700mV and Y2 is the received RF signal of 2mV peak to .Gain of the circuits is found out to be -2.49dB. Table 4.1 shows the output voltages and gains for all the three architectures discussed so far.

Table 4.1 Comparison of Different architectures.

Architecture	Output Voltage	Gain
Basic Architecture	450μV	-13.97dB
Current Injection Architecture	800μV	-7.9dB
New Architecture	1.5mV	-2.49dB

Thus this architecture implements two multipliers in one structure and also offers the benefits of Current injection method.

4.3.1 *Isolation*

As in case of mixers port to port isolation is important in UWB multipliers. Isolation between received RF signal port and template signal port is very important. In this application template signal looks for the received signal. Thus it scans in time. If isolation between these two ports is poor then it might cause what is called self multiplication of template signal. When RF signal is not present then also template can multiply with itself and produces the output. Thus it is important to improve the isolation between these two ports. Section 4.3.1.1 discusses the method of improving isolation ratio.

4.3.1.1 Method to improve isolation between input RF port and template port.

Before investigating the method for improving better isolation it is required to find the reasons for poor isolation.

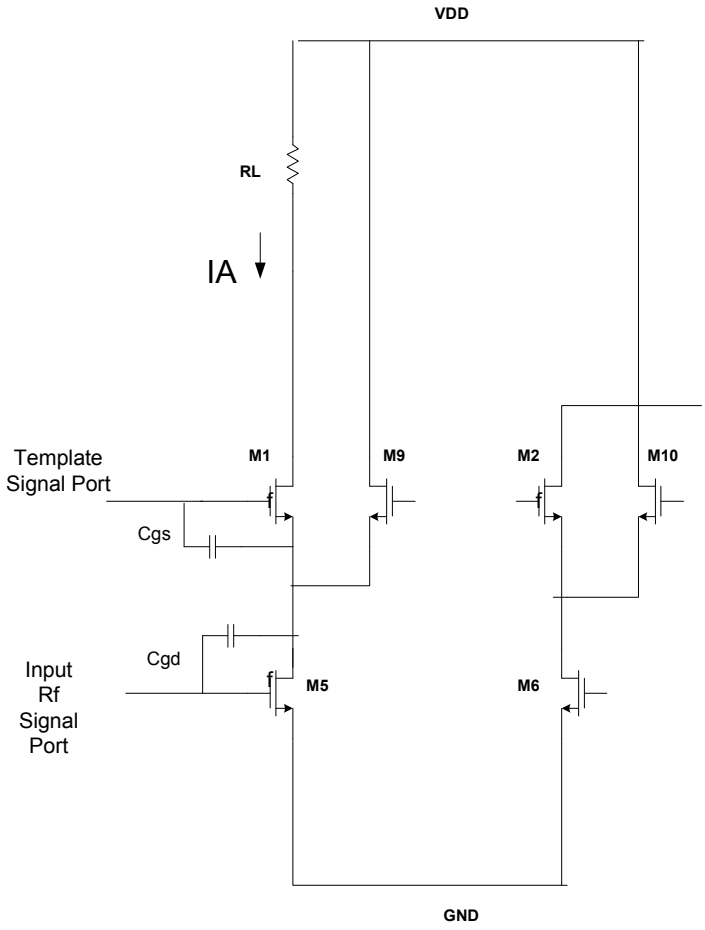


Figure 4.13 Reasons for bad isolation

Consider figure 4.13 which shows partial circuit. It can be seen from the figure that template signal port and input RF signal port are connected by two device capacitances namely Cgs and Cgd. At low frequency there impedance is very high and these two ports are isolated. But as frequency increases then Cgs and Cgd offer low impedance and hence template signal can leaks to RF port and can get self multiplied. Consider figure 4.14 which shows the method to improve isolation between the ports.

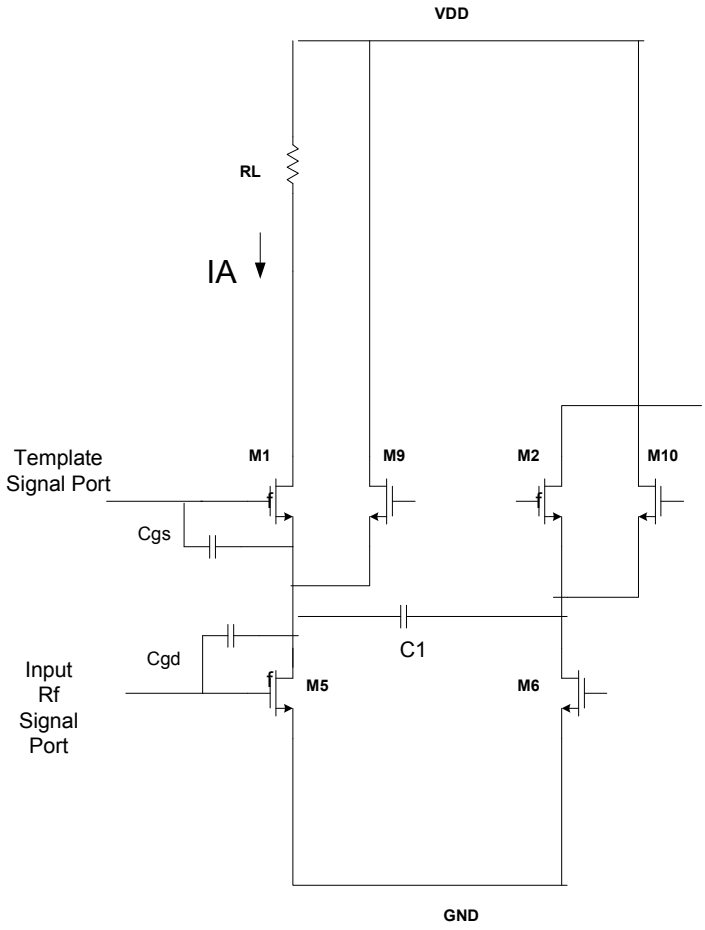


Figure 4.14 Method to improve isolation between the ports

Here external capacitor C1 is connected between the drains of M5 and M6. If we look from the template signal port then parallel combination of Cgd and C1 is in series with Cgs thus it reduces the total input capacitances seen from the template signal port and as a result improves the isolation of the circuit. An increase of this capacitance value improves the isolation as it reduces total input capacitance seen from template signal port. Figure 4.15 shows the complete circuit diagram using new method of improving isolation.

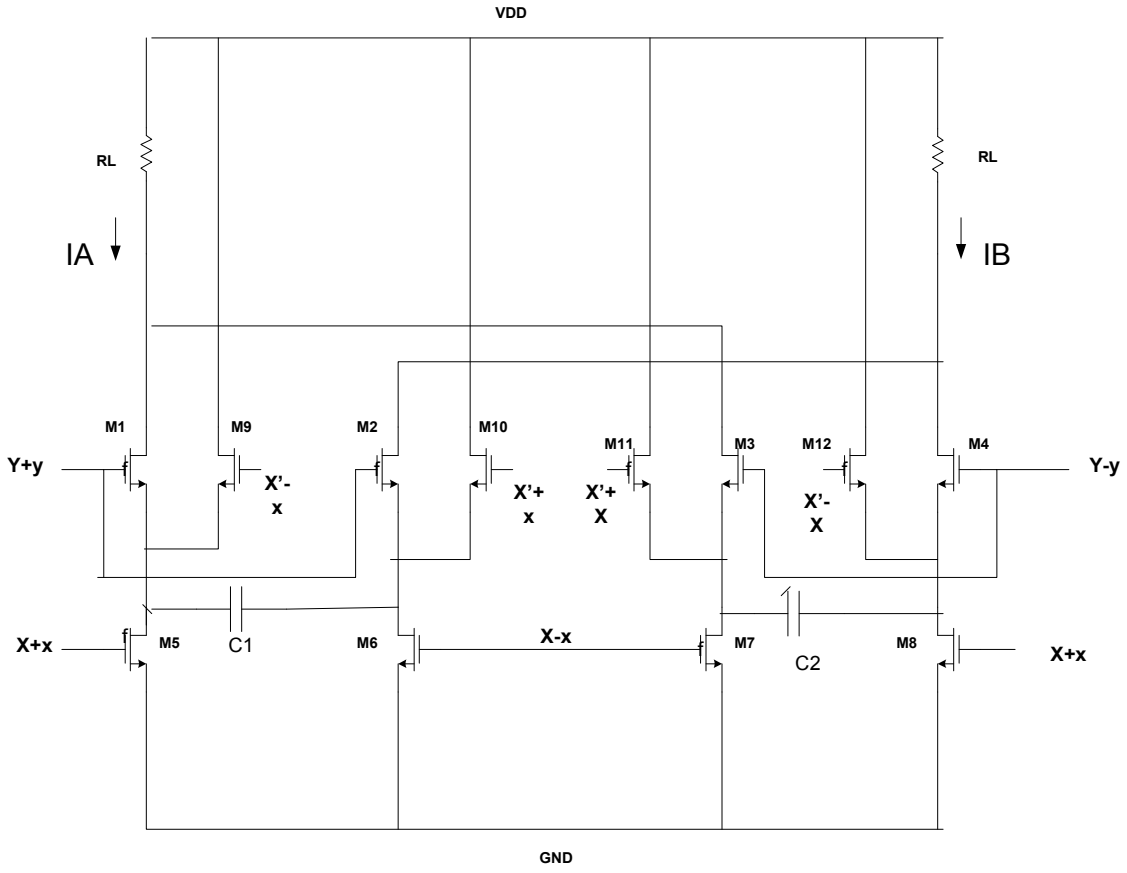
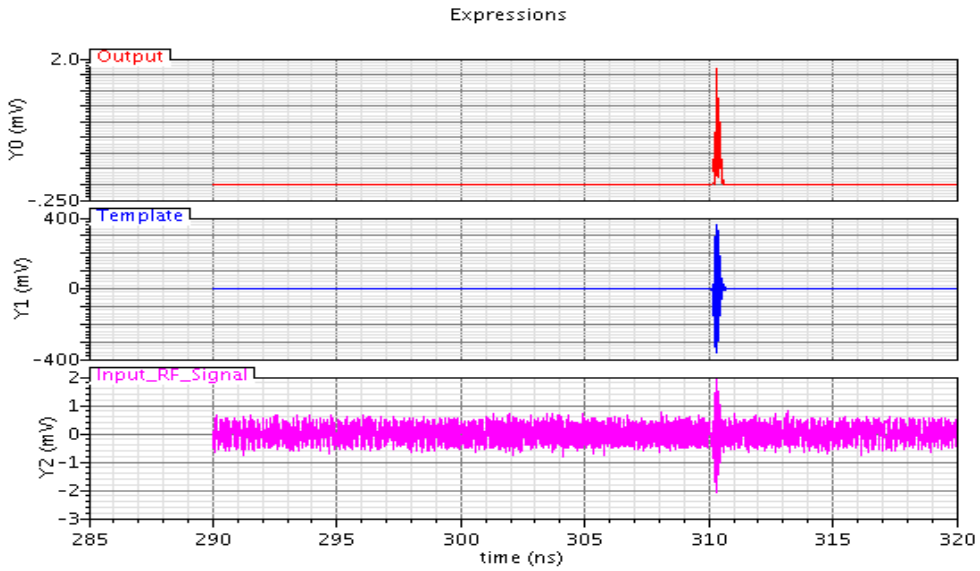


Figure 4.15 Method to improve isolation ratio between Template signal port and input RF port.

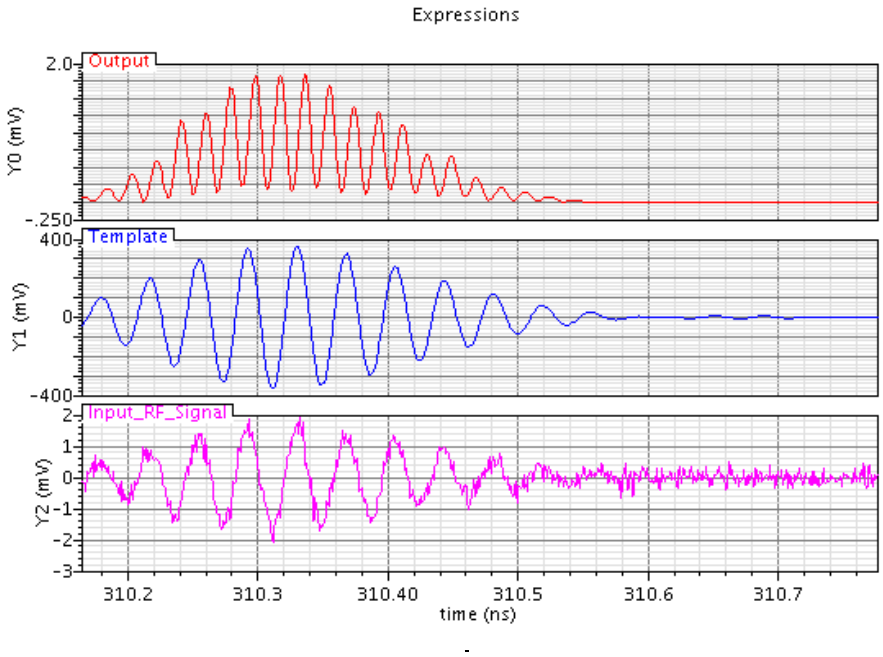
Another important parameter in UWB multiplier is it should detect the signal in the presence of noise. This is because signal received is the signal scattered or reflected back from the object this adds noise to the signal also channel adds noise to the signal. As a result multiplier should detect the signal in the noisy environment. In order to simulate this situation additive Gaussian noise of power KTB is added to the received signal. Here K=Boltzmann constant T=operating temperature and B is the noise bandwidth which is 5GHz. Template signal is applied to upper transistor (M1-M4) while noisy received signal is applied to transistors (M5-M8) and (M9-M12).

Figure 4.16 shows the output of the circuit. In this figure Y0 is the output of the circuit which is about 1.9mV while Y1 is the template signal and Y2 is the noisy received signal. It can be seen that signal

is detected by the multiplier even in the noisy environment. Increase in the magnitude of the output signal is because of noise which is random in nature.



(a)



(b)

Figure 4.16 (a) Detection of the signal in the presence of noise (b) Zoomed view

4.4 Bandwidth

Multiplier should have 29GHz of bandwidth to accommodate the input signal. More bandwidth signifies that circuit has almost constant gain till that point. In this circuit at the output node load resistance and capacitances of two transistors creates a pole and this is the dominant pole in the circuit. At the same time pole at the drain node of M5-M9 is also important as the value of the capacitors at this node large. Bandwidth of the circuit in fig 4.15 is shown in the following figure.

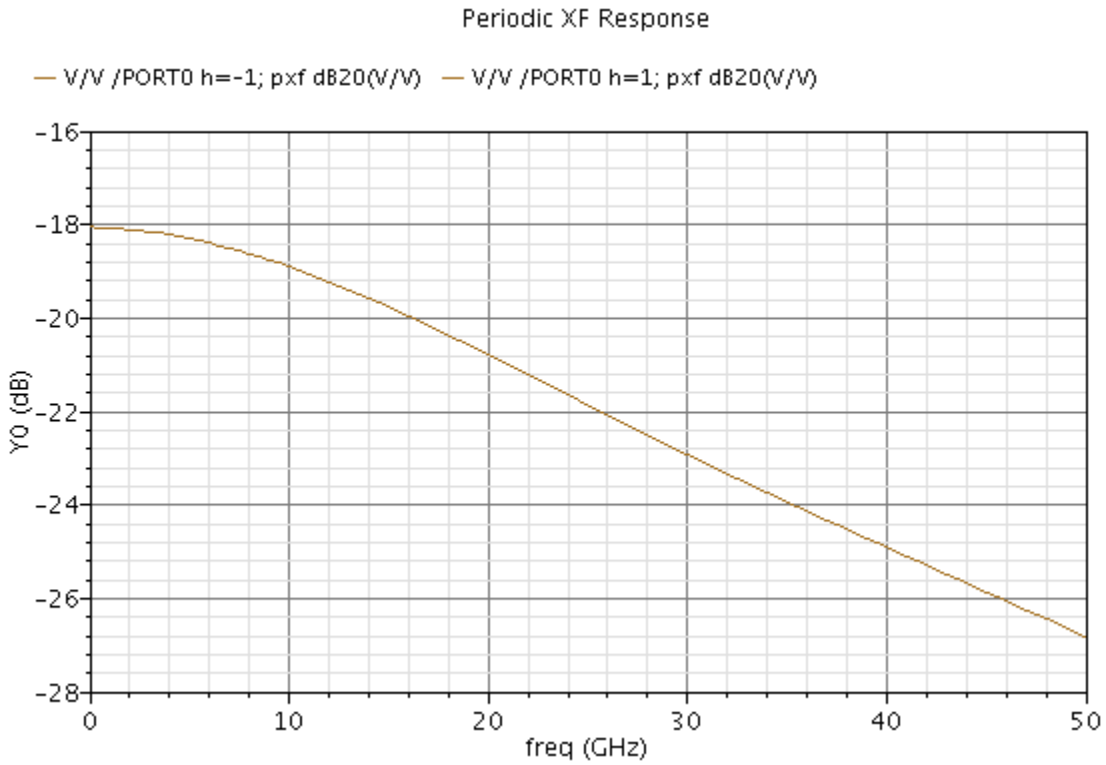


Figure 4.17 Bandwidth of the circuit explained in fig 4.15

It can be seen that bandwidth is 20GHz. One of the most common methods to increase the bandwidth is by inductive peaking.

Figure 4.18 shows simple common source amplifier with inductor in series with the load. [18]

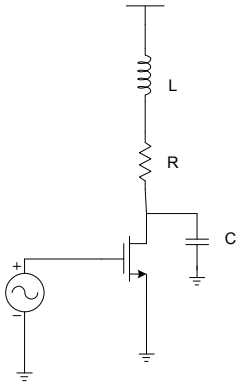


Figure 4.18 Common source amplifier with peaking inductor

By putting inductor at the drain it resonates with capacitive load, which limits the bandwidth, and hence gives greater bandwidth. [19] The transfer function of this circuit can be found out as

$$\frac{V_{out}}{Vin} = -g_m \frac{sL + R}{s^2 LC + sRC + 1} \tag{4.32}$$

This is the transfer function of typical second order system whose resonance frequency is given by $\omega_n = \frac{1}{\sqrt{LC}}$. Also being second order system there is a overshoot at the resonant frequency this depends on the Q of the system which is given by

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{4.33}$$

Thus in this circuit bandwidth extension is achieved by two ways a) by connecting a series inductor with load resistance b) Inductor in series with (M9-M12) to tune the capacitance at the drains of (M1-M5) Figure 4.19 shows the circuit with inductors.

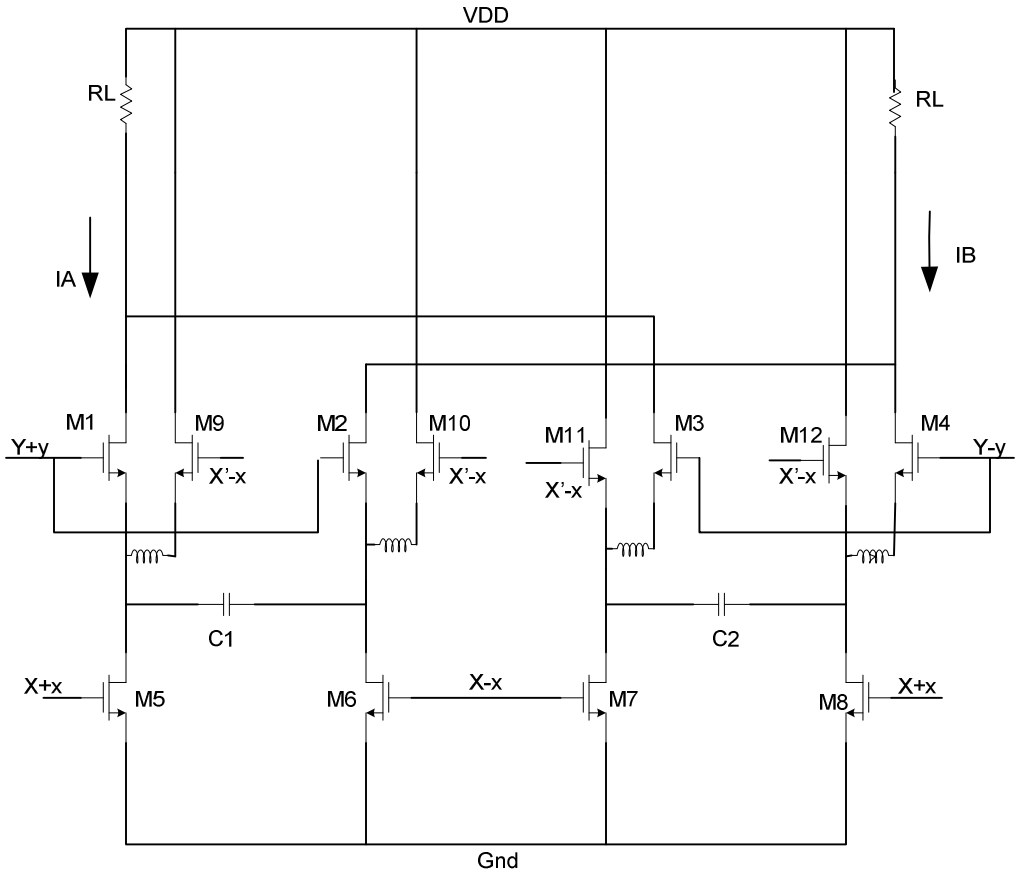


Figure 4.19 Circuit Diagram with inductor

In the figure inductors are connected at the source of (M9-M12) is used to tune the capacitors at drain of (M5-M8).

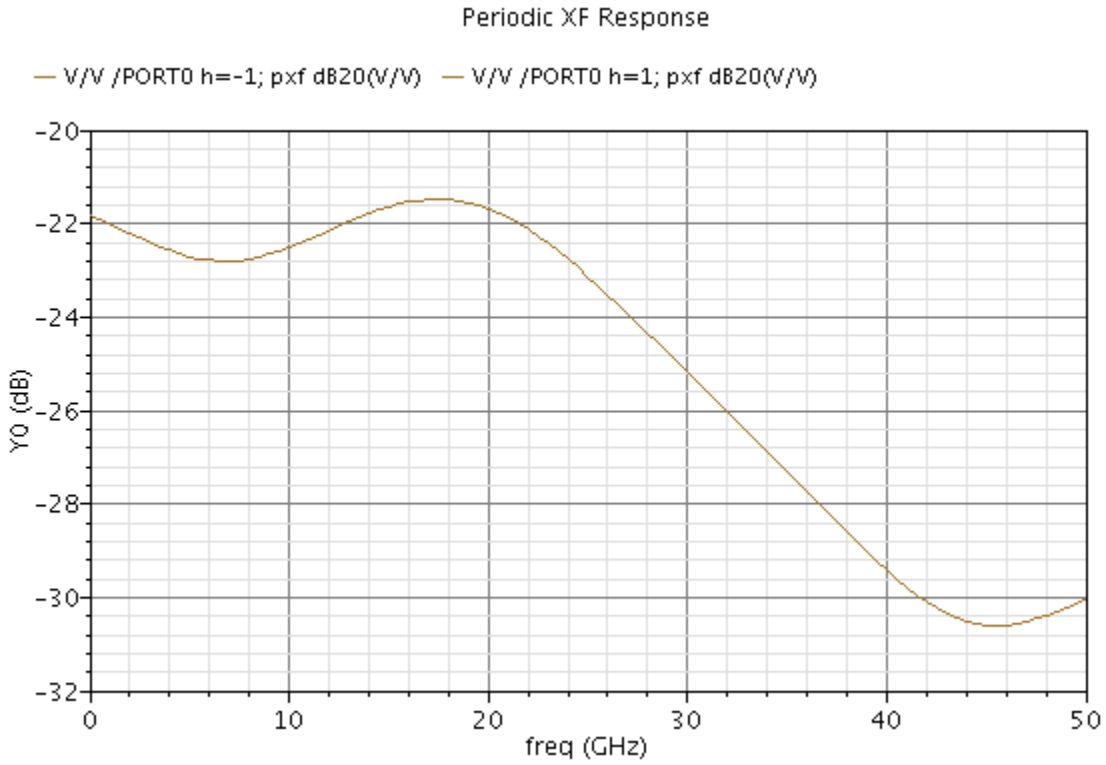
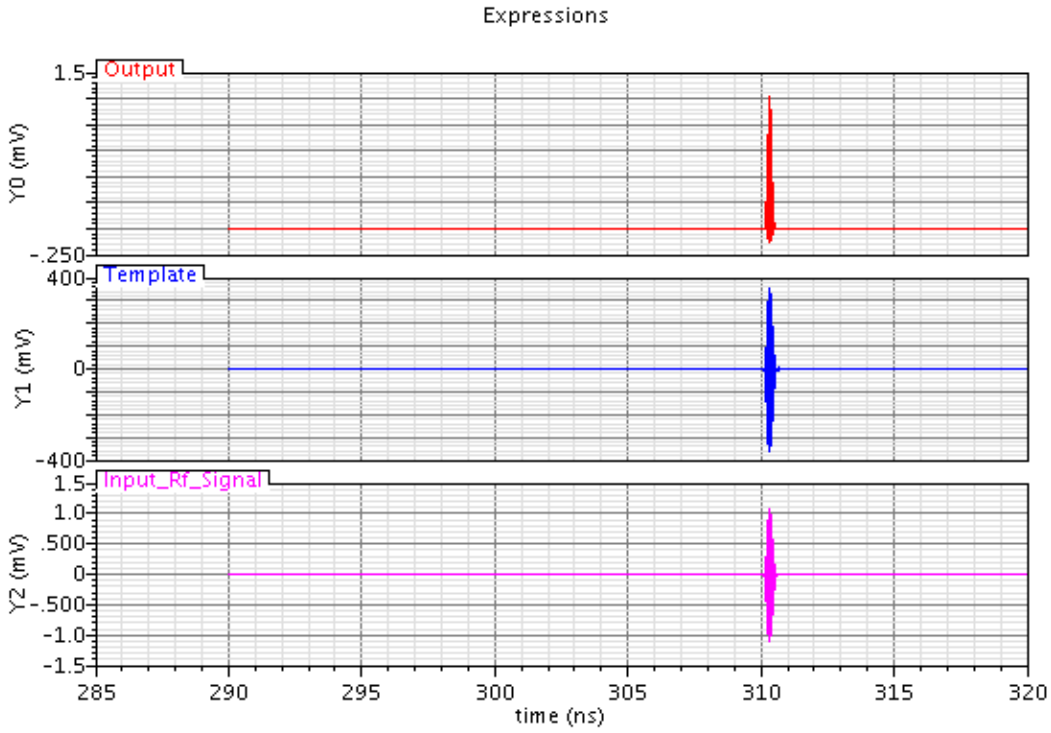


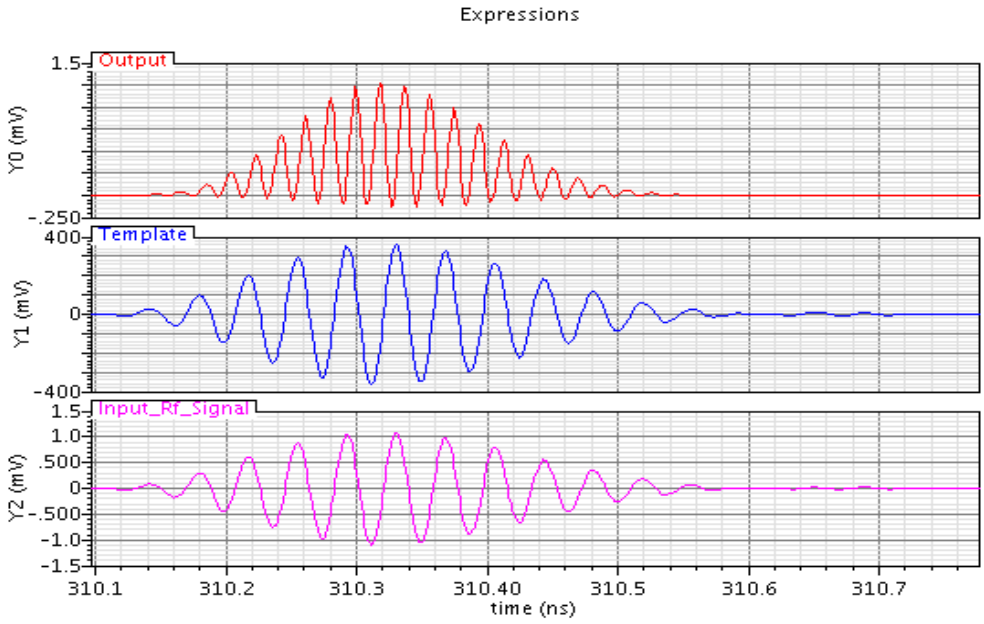
Figure 4.20 Shows the bandwidth of the circuit with inductive peaking.

It can be seen that bandwidth of the circuit is about 30GHz. This is because as explained above Inductor tunes the capacitor at the source node of transistors (M9-M12) and cancels the dominant pole.

Figure 4.20 shows the transient response after connecting the inductors in the circuit. Here template signal is applied to upper transistors (M1-M4) while received RF signal is applied to transistors (M5-M8) and (M9-M12). Y0 is the output of the circuit which is about 1.4mV while Y1 is the template signal and Y2 is the received RF signal. This verifies that even after adding inductors in the circuit its transient response is not adversely affected.



(a)



(b)

Figure 4.21 (a) Output after inductive peaking (b) zoomed view

4.5 Complete Correlator Circuit

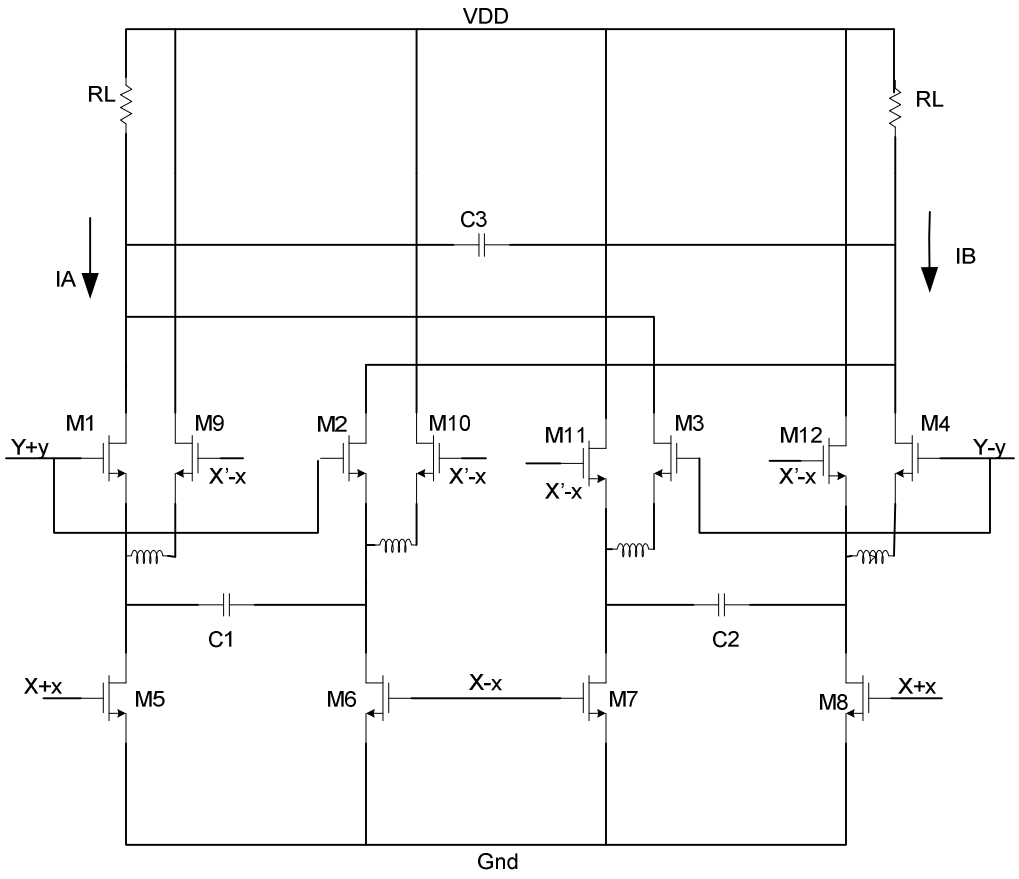
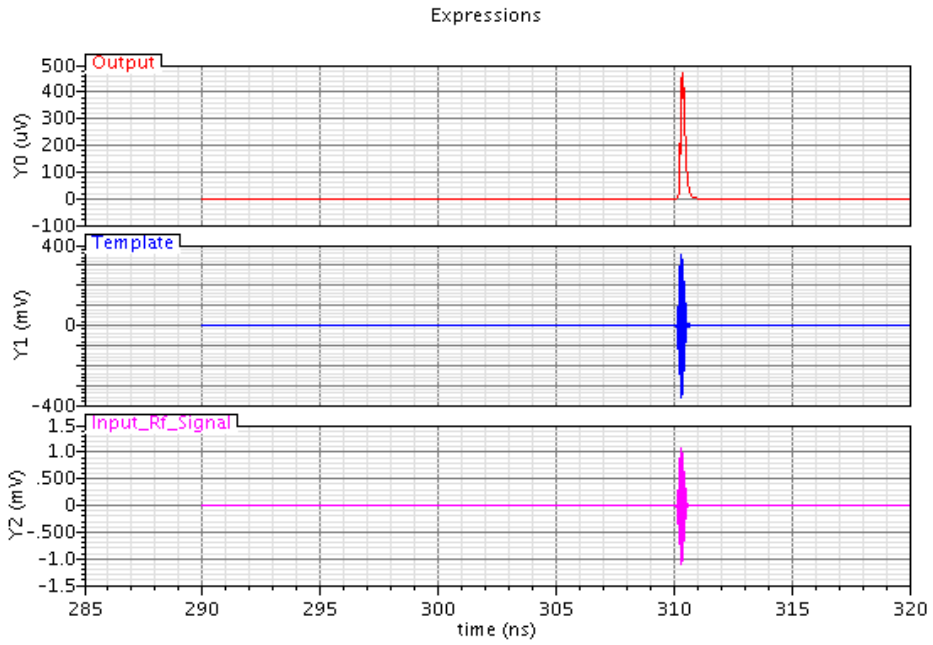
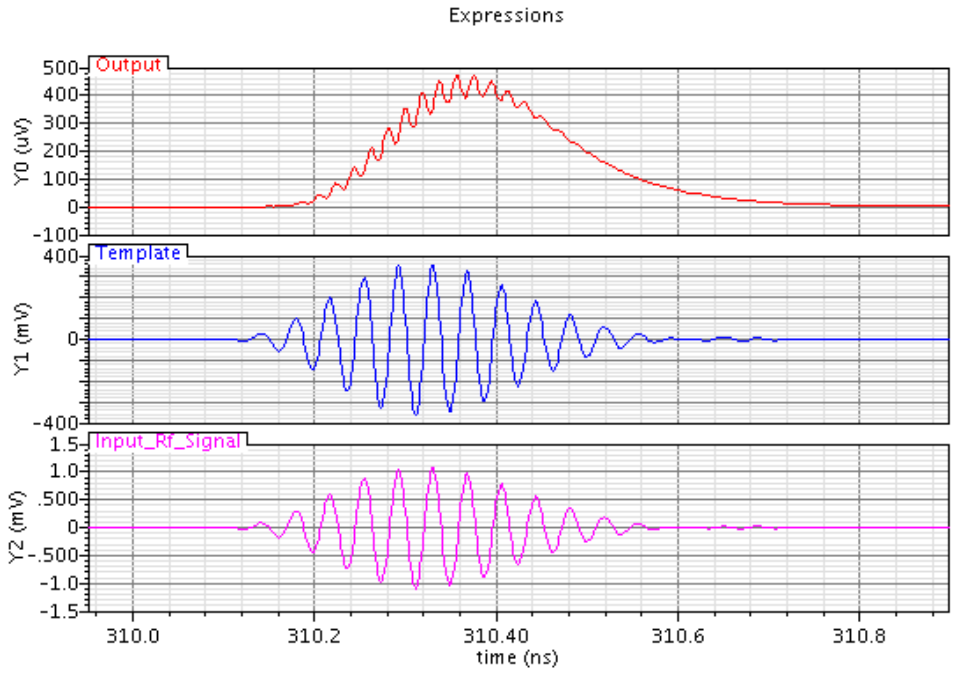


Figure 4.22 Analog Correlator

Figure 4.22 shows the complete diagram of Analog correlator. Differential current (IA-IB) which contains the multiplication of the input is integrated by the capacitor C3. Circuit uses new architecture to have more gain. Capacitors C1 and C2 are used to increase the isolation ratio between template port and input RF port that is between y and x ports. Inductive peaking is used to increase the bandwidth of the circuit.



(a)

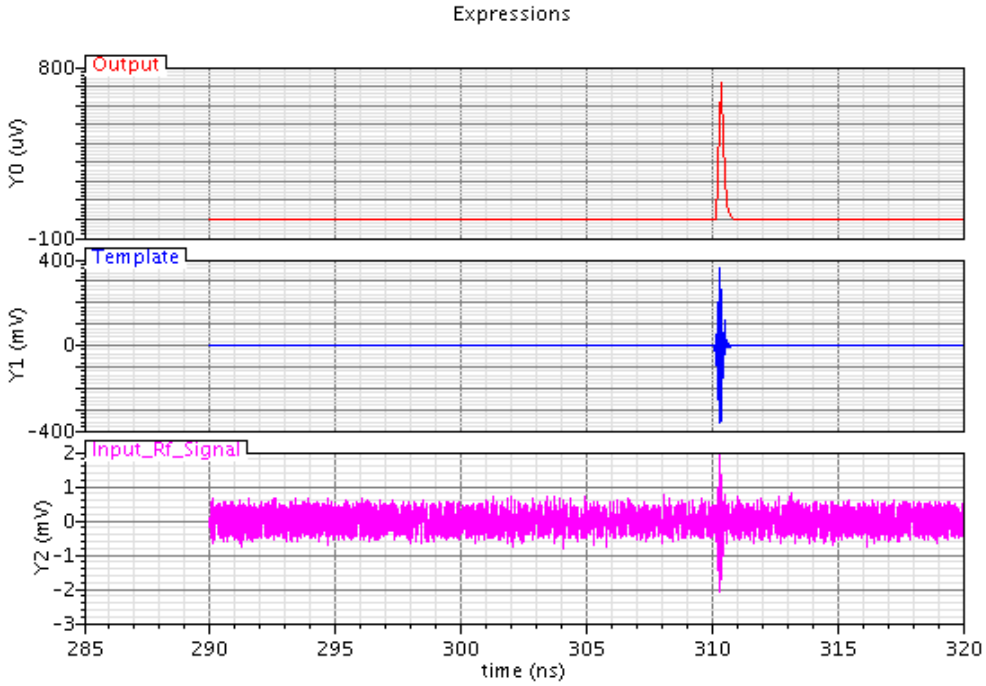


(b)

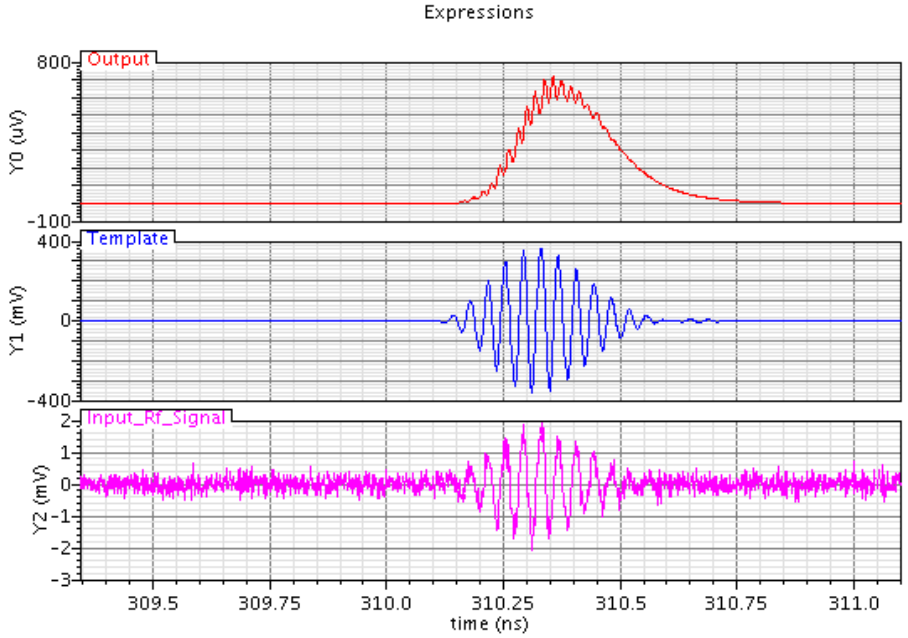
Figure 4.23 (a) Correlated output (b) zoomed view

Figure 4.23 shows the response of the correlator. Template signal is applied to transistors (M1-M4) while received RF signal is applied to transistors (M5-M8) and (M9-M12). Y0 shows the integrated output. Y1 is the template signal and Y2 is the received RF signal. It can be seen that output signal Y0 is the integrated signal. After integration its amplitude is decreased to 450μV. This amplitude depends on the capacitor value.

In figure 4.23 received RF signal applied was noiseless thus it is required to test the performance of the circuit in the presence of noise. In order to simulate this condition again, noise of power KTB is added to the received signal. Here K=Boltzmann constant T=operating temperature and B is the noise bandwidth which is 5GHz. Noisy received signal is applied to the transistors (M5-M8) and (M9-M12). While template signal is applied to transistors (M1-M4) Figure 4.24 shows the simulation results of the circuit in the presence of noise.



(a)



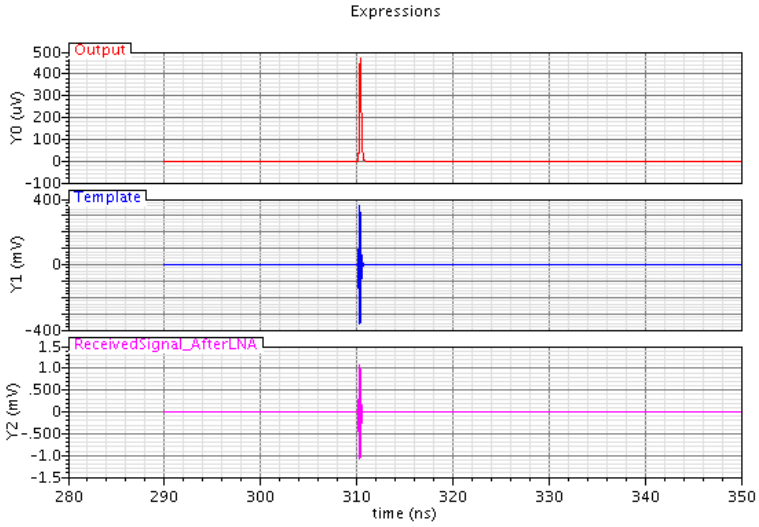
(b)

Figure 4.24 (a) correlated output with noise (b) zoomed view

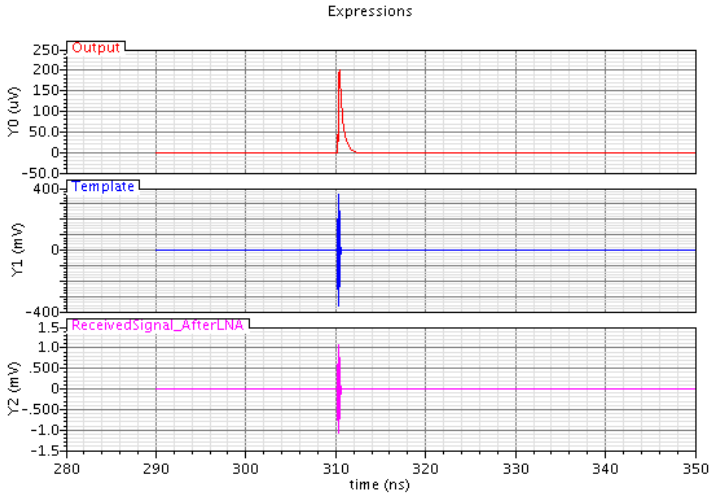
In figure 4.24 Y0 is the correlated output signal while Y1 is the template signal of 700mV peak to peak and Y2 is the received noisy signal. Figure shows that signal can be detected even in the noisy environment. Output Y0 is about 750μV because of noise. Value of capacitor can be changed to change the amplitude and the holding time. Voltage across the capacitor can be given by following relation

$$V_c = \frac{1}{c}\int (IA - IB)dt \tag{4.34}$$

Thus if value of capacitor is increased then voltage across it will decrease.



(a)



(b)

Figure 4.25 (a) value of integrating capacitor is changed to 100fF (b) Value if integrating capacitor is changed to 500fF

Figure 4.25 shows the results when value of capacitor is changed. In figure 4.25 (a) and (b) Y0 is the correlated output, Y1 is the template signal while Y2 is received RF signal after LNA. It can be seen that when value of capacitor is changed to 100fF output voltage is decreased to 400µV and when value of capacitor is changed to 100fF output voltage is decreased to 200µV.This voltage can be increased by the having post amplifiers in the circuit.

Integrating capacitor should hold the output voltage for large time so that ADC can sample this voltage and convert it to the digital domain. One of the main reasons to have more holding time is considering the jitter of ADC clock. Time for which Capacitor should hold the voltage across it should be greater than the jitter of the sampling clock of ADC. Generally ADC clock has jitter of about 400ps. The proposed circuit in this thesis has holding time about 60ps and hence it is required to increase the holding time of the circuit. Holding time of the circuit can be increased by having Gm-C integrator as a next stage in the circuit. Having large capacitor at the output with large output resistance holding time can be increased.

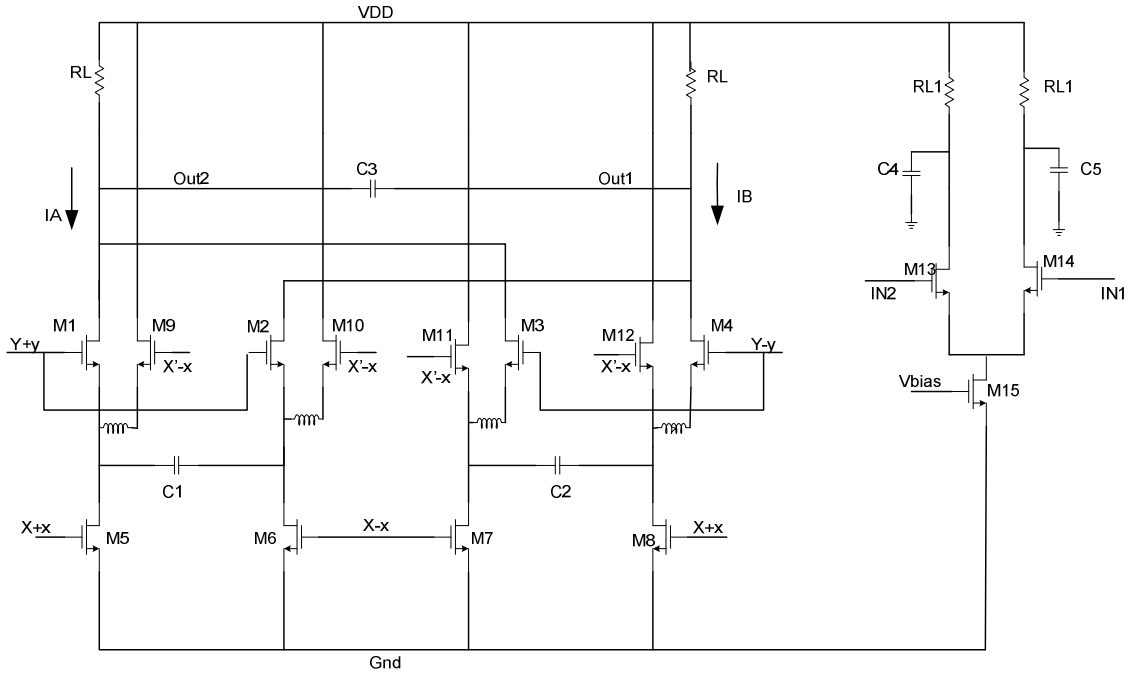


Figure 4.26 Gm-C integrator to increase the holding time of the circuit.

Output of the circuit is given to the Gm-C integrator which a differential amplifier with the large value of capacitor at the output. As the output capacitor and the resistance is large time for which capacitor holds the output voltage is large.

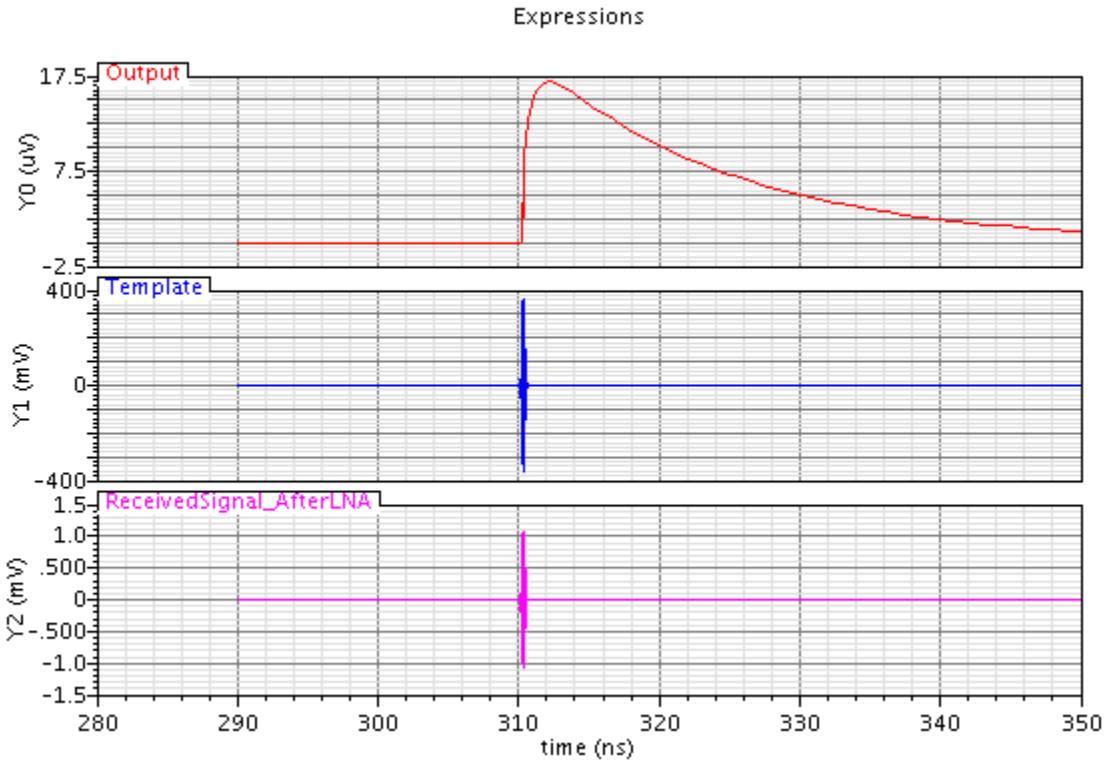


Figure 4.27 Simulation results with Gm-C integrator

In figure 4.27 Y0 is the output voltage, Y1 is the template signal and Y2 is the received RF signal. It can be seen that capacitor holds the voltage for large amount of time as discharging time of the capacitor is increased. The holding time thus obtained is 2.3ns which is much greater than jitter of ADC sampling clock.Holding time constant can be approximated by simple equation

$$\tau = RC \tag{4.35}$$

Voltage across capacitor is given by

$$V_c = \frac{1}{c}\int (IA - IB)dt \tag{4.36}$$

if we want to increase the holding time by increasing the value of capacitor then voltage across capacitor decreases. Thus there is a treadoff between holding time and output voltage.

In correlator we need to dump the voltage across capacitor once it is sampled by ADC. This dumping action can be implemented by two NMOS switches which turn on after holding time, in this case after 2.3nsec

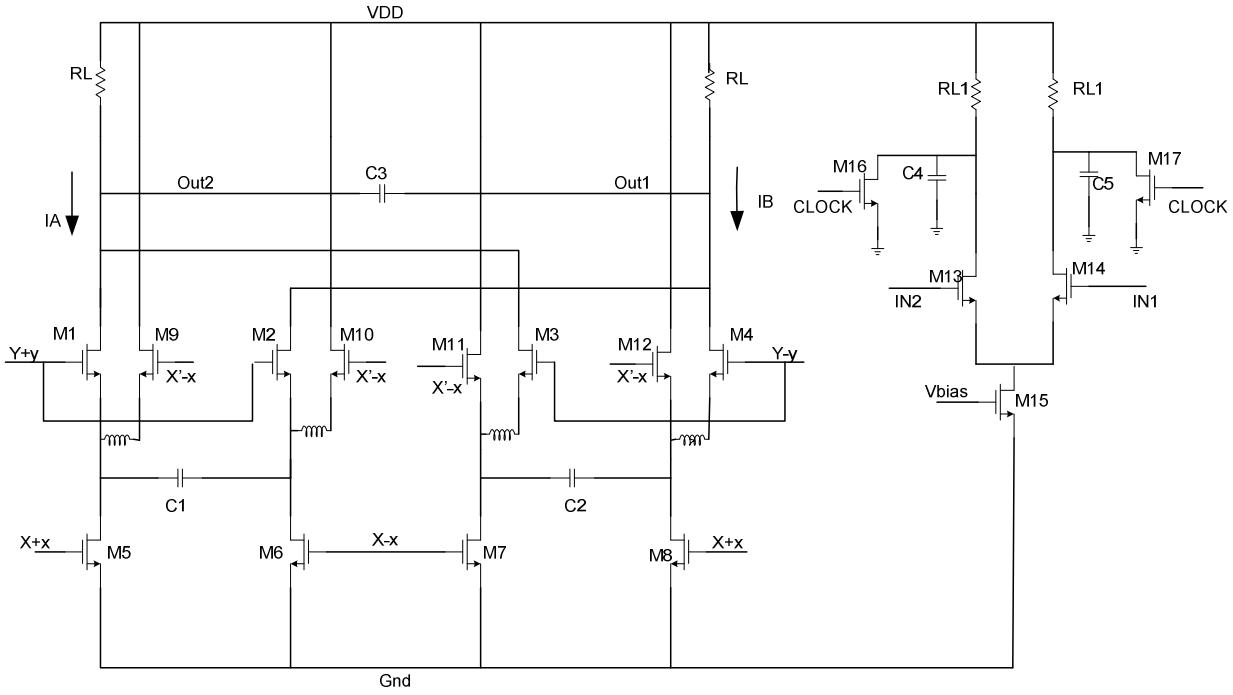


Figure 4.28 Dumping switches implemented

Figure 4.28 shows the implementation of dumping switches. Switches are realized by transistor M16 and M17. Gate voltage of these transistors is high after holding time.

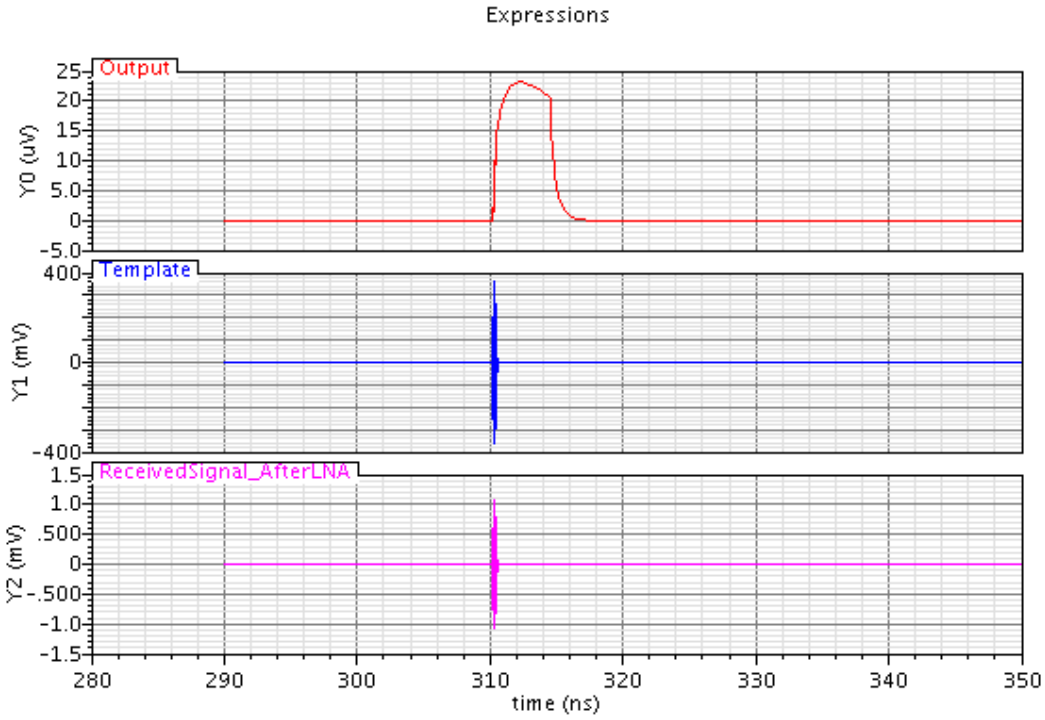


Figure 4.29 Simulation results after implementing dumping switches

In figure 4.29 Y0 is the output voltage Y1 is the template signal while Y2 is the received RF signal after LNA. It can be seen from the figure that voltage across the capacitor is cleared off after holding time that is after it is sampled by ADC. Output voltage thus obtained is of small value but it can be increased by having post amplifiers after Gm-C integrator.

CHAPTER 5

CONCLUSION

In this thesis Analog correlator for UWB vehicular radar system operating at 22-29GHz is designed. Technology used for the designing is IBM 90nm CMOS technology. Analog correlator is made up of two blocks namely multiplier and integrator. New architecture is proposed for the multiplier which is actually two multipliers in one block and gives more gain compared to conventional Gilbert cell multipliers. With the new architecture gain can be increased from -13.97dB to-2.49dB.New method of using capacitors to increase the isolation ratio is suggested. With this method isolation ratio between port at which template signal is applied and port where input RF signal is applied is improved. Improvement of 2dB of isolation ratio is shown in the thesis. This will avoid self multiplication of template signal when there is no RF signal. Also method of inductive peaking at the output node and also at source node current source transistors is suggested. With this method bandwidth of the circuit can be extended from 20GHz to 30GHz thus bandwidth can be extended about 50%.

Integration is achieved by connecting a capacitor between differential nodes of the circuit. Thus differential current which contains multiplication of the input signal is integrated by the capacitor. But the holding time of this correlator is less a nanosecond and to be improved. There are several ways of increasing the holding time. One of the easiest ways to realize integration is by Gm-C integrator which has large output impedance and hence more holding time. Holding time of the circuit is improved to 2.3ns by using Gm-C integrator.Other ways of improving holding time of circuit are suggested in [4].

For future work multiplier design which gives gain more than 0dB is desirable. Also as passive inductors consume lot more chip area thus use of active inductors for peaking is desirable. Thus integration of both blocks multiplier and integrator in single block which gives more gain and holding time is desirable.

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