

THERMAL EFFECTS AND ANALYSIS OF HIGH FREQUENCY DEVICES IN
ANALOG INTEGRATED CIRCUIT
DESIGN

By

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ABSTRACT

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Heterojunction Bipolar Junction Transistors (HBTs) are used in various high frequency applications in modern day technology. These devices produce high trans-conductance which is need for high frequency application. Their gain is significantly larger than complimentary metal-oxide-semiconductor (CMOS) devices which also imply there is high current within the devices. Since HBTs are very compact structure, the thermal heating generated within the devices needs to be characterized. This thesis explores the thermal effects from self heating in the static and time domains of the devices using 3D dimensional simulation and mathematical modeling using heat flow equation.

The study concentrates on the thermal modeling aspects of the heterojunction bipolar transistors using the TCAD 3-dimensional thermal simulation. Die concentration and operational speed of transistors are rapidly increasing because of high market a demand, which can lead to thermal runaway complication and current crowding effect. The susceptibility of transistors to temperature change requires a more sensitive and accurate modeling for the thermal effects of the device. The heat source is the junction between base and lightly doped collector. This heat gets trapped within the device because of the presence of isolation oxide sidewalls and bottom oxide layer. The thermal impedance depends on the position of the heat source, its separation from the sidewalls and bottom oxide, as well as the thickness of

the oxide wall and bottom. The thickness of the wafer also changes the thermal heating effect. The spreading resistance from the heat source to the sidewalls and bottom oxide, to the wafer, and then to ambient temperature has been calculated using the heat flow equation. The results are then compared to TCAD simulation. The mathematical model was within 10% when compared to the 3D TCAD simulation. The model presented in this work is based on an extension of the constant angle heat spreading, resulting in closed form expressions which can be used for practical applications. The electrical analogy developed from the thermal analysis can be used in VBIC, HICUM and MEXTRAM compact models, which are used to model the behavior of HBTs.

Solder bump packaging results to the formation of a thermal equivalent transmission line for the heat flow from the heat source to the ambient temperature at the bumps. This paper analyses the effect of thermal heating when devices are connected using solder bumps. TCAD simulation is performed and mathematical model is developed to support the 3-D simulation result. The thermal impedance depends on the length of line from the heat source to the solder bumps, which is modeled by using electrical transmission line analogy. Closer the solder bump is to the device smaller is be thermal resistance, other tactics are discussed which can reduce the thermal resistance. An infinitely long line results in a static characteristic impedance for the line. The equivalent electrical analogy for the thermal transmission line is modeled which can be implemented in standard device modeling s like HICUM, VBIC or METRAM.

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CHAPTER 1
INTRODUCTION
1.1 Introduction

The semiconductor industry demands advanced and smaller devices for high speed communication, high precision circuits, and faster microprocessors. Emerging markets in high-speed analog and fourth generation wireless base-stations, demands ever-increasing high frequency bandwidth and precision device control to differentiate new products. Applications are in the areas of wireless infrastructures, medical imaging, cable modems, base-station support, lower power and high-speed performance, especially in portable systems. One of the most competitive high speed analog is Silicon Germanium (SiGe) Hetero-junction Bipolar Transistor (HBT) which is now well established into mainstream manufacturing. Many high-speed high-precision analog applications require HBT technologies to be fabricated on thick-film silicon-on-insulator (SOI) substrates due to lower parasitic capacitances and better linearity, though care is needed to mitigate thermal effects on SOI, and high cost of SOI wafers compared to bulk-silicon wafers still limits market applications for lower cost solutions. Designers are faced with great challenges to meet high demands in the technological industry. Die concentration and operational speed of transistors are rapidly increasing because of market demand, leading to thermal runaway complication and current crowding effect. The susceptibility of transistors to temperature change requires a more sensitive and accurate modeling of the thermal effects of the device, as well as heating effects from adjacent devices. The use of SOI wafer in combination with full dielectric isolation (Deep Trench (DT) + Shallow Trench (ST)) is of particular interest since the transistor footprint is minimized, leading to much higher transistor density. However, due to the poor thermal conductivity of SiO₂, the self-heating is much aggravated for a fully dielectric isolated transistor. It is reported that for a SiGe HBT the use of SOI+DT/ST causes the effective thermal resistance to be five times greater compared to

the one using SOI+ST. The proper device design of SiGe HBT on SOI to mitigate self-heating effect has become a critical issue in recent years.

This research is concentrates on the thermal modeling of Hetero-junction Bipolar Junction Transistors (HBT) to ameliorate existing thermal models. Three main reasons for thermal effects in HBT are, 1)self-heating caused by the temperature rise within the structure of a device particularly for deep trench (DT) devices 2) thermal coupling between adjacent transistors on the same chip, 3) package thermal effects which raise the overall temperature of the chip [1]. This paper focuses on self-heating aspects and tries to apply this knowledge to practical device characterizations and circuit designs. Several attempts have been made to improve the simulated models to achieve real world measurement results. In this dissertation, three dimensional (3D) model for HBT has been created using Synopsys Transactions on Computer Aided Design (TCAD) tools, mathematical model has been developed and finally the mathematical model and TCAD simulations were compared to measurement results. Finite element device simulation is used to examine the thermal properties of the different isolation structures in more detail. In particular, the influence of the buried oxide, deep trench sidewalls and the metallization on the heat propagation is studied. Calibration for the devices was done to match the measurement result. Finally, a model for the devices is being proposed future tendency prediction.

HBT are an important building block of high speed IC designs [2]. HBT are manufactured by using trench isolation and silicon-on-insulator (SOI) technologies. Some of the advantages of these transistors are reduced parasitic capacitance, low leakage current, latch-up free and radiation hardened circuitry. A major disadvantage of HBT is the poor thermal conductivity of the dielectric. For this research work, the Texas Instrument HBT have been used to extract real world results. The manufacturing process used for these devices is called CBC8 process.

1.2 Process Integration Of HBT Using The CBC8

CBC8 (Complementary BiCMOS) technology developed at Texas Instruments is for highest-speed precision-analog applications. Key advantages include nearly matched SiGeC PNP/NPN, ideal for push-pull design applications and lower power consumption with increased speed by targeting reduced

parasitic effects with SOI CBiCOMS and complimentary hetero-junction bipolar transistors (HBT) which meet the needs for high gain and low noise applications. This section covers the basic technology flows involved in CBC8 process. Figure.1 provides a block diagram flow of the key process modules for CBC8.

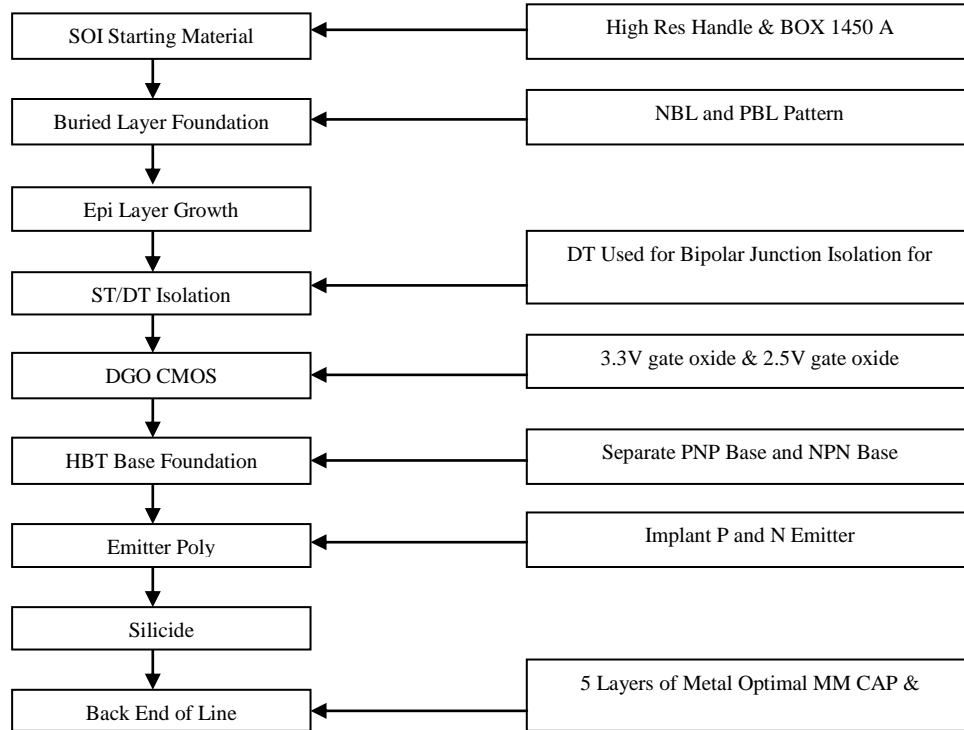


Figure 1.1 Block Diagram process flow of CBC8 [1]

The technology begins with high resistive silicon-on-insulator (SOI) 200mm bonded wafer. N-type and P-Type buried-layers (NBL and PBL) are next patterned and implanted to form the HBT collector NBL and PBL. Implants and anneals were optimized for zero defects in active buried layer regions. Next is to grow an epi-layer to minimize defects, up-diffusion, and auto-doping effects. Shallow trenches (STI) and deep trenches (DT) are next patterned and filled with oxide to define bipolar isolation regions and Complementary Metal Oxide Semiconductor (CMOS) junction isolation regions. *Chemical-mechanical planarization (CMP)* is used to improve the planarity of composite and STI regions. HBT collector sinker implants are patterned and optimized for minimization of collector resistance linkup and sinker capacitor gate oxide integrity (GOI) robustness. Gate poly-silicon is patterned followed by a deposited protection layer. Bipolar open regions are formed followed by reduced pressure low

temperature Reduced-pressure chemical-vapor-depositions (RPCVD) nonselective epi base growth. This in-situ doped epi process sequence is repeated for both PNP base and NPN base formation. At this step, special care was given for SiGe-Base band-gap optimization to give better beta, Early voltage (V_A), and unity gain and maximum oscillation frequency (f_T/f_{max}) HBT performance compared to silicon only CBiCMOS platforms on SOI. Next Emitter/base dielectric is formed, Emitter-window are defined with photo and etch followed by single poly emitter deposition with no interfacial emitter oxide IFO formed. $N+$ and $P+$ emitter poly implant and emitter poly etch complete the emitter sequence. Lithography defined final patterning of devices bases completes the process followed by silicidation. Standard back-end-of the line processing follows with 5 layers of metal and optional inductor and oxide Metal Insulator Metal (MIM) capacitor RF/analog ideal for linear applications Figure 1.2 shows a Scanning Electron Microscope (SEM) cross-section of a SiGe hetero-junction bipolar transistor (HBT) with a single base, emitter, and collector contact layout (BEC) configuration. Full dielectric isolation can be seen with vertical DT intercepting the BOX and STI regions used to separate composite contact regions.

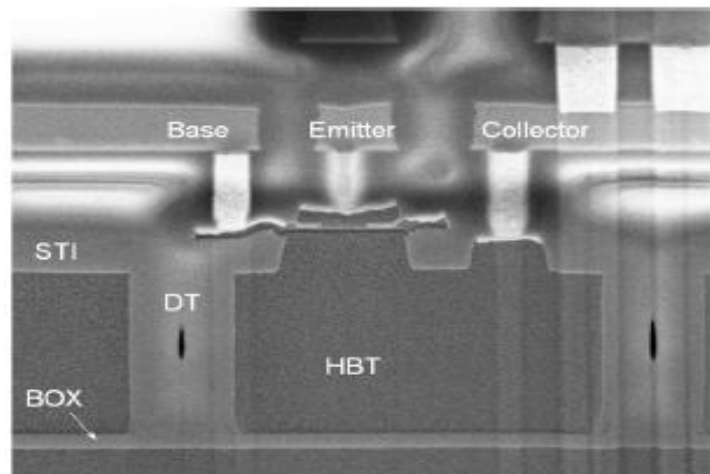


Figure 1.2 Cross section of a complement [1].

Figure 1.3 shows the top and cross sectional views of the HBT. The DT and the buried oxide act as a thermal-isolated blanket, while the heat dissipation through the top metal wiring is known to be very limited. The tub area enclosed within DT determine the silicon volume for heat dissipation hence the

thermal resistance of the transistor. The space between DT and composite, which is defined by the arrows in Figure 1.3, is thus a critical design parameter.

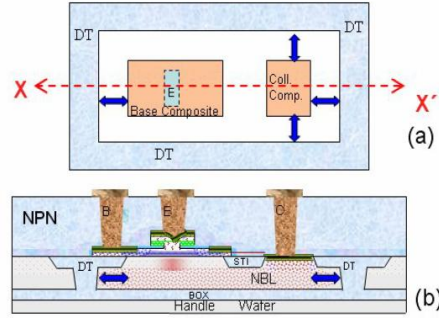


Figure 1.3 (a)Top view of the layout for a NPN HBT (b) Cross sectional view of the NPN transistor in X' direction.[2]

For high performance, SiGe HBTs are often biased in very high current densities and voltages, which can become a serious self-heating issue[2]. Thermal resistance R_{th} is an effective measure for gauging device self-heating. At $A_E = 2.5 \mu m^2$, R_{th} is 3500 K/W for the SiGe HBT on SOI, which is nearly twice that of the bulk SiGe HBT (1800 K/W). An increase in thermal resistance degrades the SOA, since internal self-heating can lead to thermal runaway. Flyback loci model given in [2][42] to characterize the SOA.

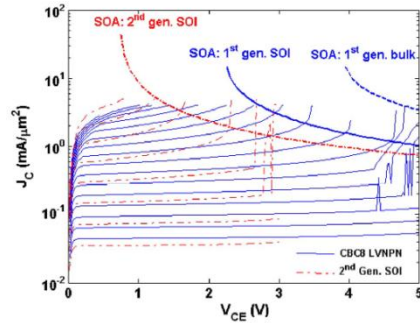


Figure 1.4 Characterization of SOA of three SiGe technologies based on point of thermal runaways.[2][41]

The SOA current density for thermal and electrical stability can be expressed as[2][41]

$$J_{C,SOA,Thermal} \leq \frac{\alpha}{A_E} \cdot \frac{C_{POWER}}{V_{CE}-C_{BIAS}} \quad (1.1)$$

$$J_{C,SOA,Electrical} \leq J_{B,Crit} \cdot \frac{1 - \left(\frac{V_{CB}}{BV_{CB0}}\right)^n}{\left(\frac{V_{CB}}{BV_{CB0}}\right)^n} \quad (1.2)$$

$$\frac{1}{J_{C,SOA,Electrothermal}} = \frac{1}{J_{C,SOAThermal}} + \frac{1}{J_{C,SOA,Electrothermal}} \quad (1.3)$$

where A_E is emitter area, a is a defined failure condition ($a = 2$ in 100% J_c increase), C_{POWER} ($\approx V_T/(\varphi_{BE} \cdot R_{TH})$) is related to power dissipation, and C_{BIAS} ($\approx R_E/(\varphi_{BE} \cdot R_{TH})$) is coefficient associated with voltage drop. R_{TH} is the thermal resistance, φ_{BE} is the temperature coefficient of base-emitter potential voltage, R_E is the emitter resistance and $J_{B,Crit}$ is the critical current breakdown.

Table 1.1 Typical CBiCMOS device characteristics

Device	Parameter	Unit	LV NPN	HV NPN	HV PNP	
SiGe HBT						
	AE	μm ²	0.25x1	0.25x1	0.25x1	
	βDC	300	300	300		
	VA	V	200	250	85	
	fT@1.5V	GHz	57	34	38	
	fmax@1.5V	GHz	95	85	80	
	Nfmin@2GHz	dB	0.7	0.7	0.8	
	BVCEO	V	3	5.2	5.2	
	BVCBO	V	12	19	11	
	1/f noise -Sib@1Hz	A ² /Hz	5.00E-21	6.00E-21	1.50E-20	
CMOS						
			LV NMOS	HV NMOS	LV PMOS	HV PMOS
	W/L		5/0.24	5/0.4	5/0.24	5/0.4
	VDD	V	2.5	3.3	2.5	3.3
	VT	V	0.6	0.7	0.65	0.7
	IDSAT	μA/μm	570	500	290	260
	Off Current <	pA/μm	1	1	1	1
	fT@VDD/2	GHz	28	17	13	8
	fT@VDD	GHz	30	18	17.5	10

1.3 Application Of HBT And Its Advantages Over CMOS

The HBT process uses deep trench technology on a bonded wafer for complete dielectric isolation and optimal high-speed amplifier performance. This process enables designers to make power-efficient and high-speed amplifiers. Complementary bipolar (CB) processes enables class AB output stages with very low quiescent current and high output drive in analog circuits. Also, the CB process allows high-swing complementary common-emitter output stages, commonly known as "rail-to-rail outputs." On some processes for Metal-oxide-Semiconductor Field Effect Transistors (MOSFETs), these output stages can be a challenge to design with well-controlled frequency and time-domain responses because the output transistors vary from quiescent conditions to sinking or sourcing high currents to near saturation of the output transistors. The low collector resistance and reduced quasi-saturation effects make CBC8 process well suited for rail-to-rail output stages.

Rail-to-rail input stages can be designed on a CB process, by using both PNP and NPN input stages. Other circuitry is required to steer current to the appropriate differential pair depending on the common-mode voltage. Both stages usually require a folded-cascode to shift level. A CB process having high-performance Bipolar Junction Transistors (BJTs) of both types will ensure consistent performance stage when either the input stages is active. The HBT process goal was to deliver the highest level of analog performance possible, while minimizing wafer cost and development time. The performance benefits of complementary bipolar analog Integrated Circuits (ICs) can be seen in the analog circuits used in wired broadband applications such as xDSL and cable modems. The most critical analog blocks are the drivers and receivers. Due to differences in device physics, receivers using low base-resistance BJTs have low input noise voltage with a much lower operating current and die area than CMOS designs.

Texas Instruments stated that CB designs yield lower distortion than CMOS due to the higher trans-conductance of BJTs. High gate capacitance of large MOSFET devices have problems with stability and power dissipation. In practice, CB designs are superior in combining low distortion, low power dissipation, and frequency stability. The higher breakdown voltages achieved in high-speed BJTs gives CB line drivers a higher output swing [3].

The minimum channel length of CMOS transistors determines the power-delay product and the IC area. Reducing CMOS channel length is expensive because it is set primarily by lithography. The analogous parameter for bipolar transistors is the vertical dimension of the active base region ("base width"), critical for determining the current gain and the transition frequency. These junction profiles are controlled by implantation and Rapid Thermal Annealing (RTA). Since the minimum feature size for a BJT (usually the emitter stripe width) is less significant than CMOS, a high-performance CB process can be developed with less investment of capital and time. The CBC8 process minimum emitter width is 0.4 micro meter, allowing it to be manufactured at a low cost.

As explained in the introduction, the HBT circuits are greatly influenced by thermal effects and accurate modeling tools are necessary to achieve effective practical design results. The High current model(HICUM) and MEXTRAM model has been used to calculate the thermal effects of transistors. The HICUM is preferred over the Spice Gummel Poon (SGP) model because it is a more accurate model and has a self heating parameter. Using the HICUM model, the thermal parameters can be altered to obtain simulated results which accurately reflect the measurement results.

1.4 Medici Davinci

The TCAD tool used in this dissertation is from Synopsys. Synopsys device simulation tools includes Taurus Medici which is comprised of Medici, Davinci, and TSupreme4. Medici is used of 2D simulation and Davinci is used for 3D simulation. TSupreme4 is for process simulation. Medici predicts the electrical characteristics of arbitrary two-dimensional structures under user specified operating conditions. MEDICI solve Poisson's, Thermal, Current-Continuity and Energy-Balance equations for electron and hole. It is applicable to a broad variety of technologies, ranging from submicron devices to large power structures. Typical device applications include diodes, BJTs, MOSFETs, JFETs, MESFETs, HBTs, HEMTs, IGBTs, CCDs and GTOs. Medici can be used to for the following application:

- Determine I-V characteristics, gain and speed of transistors and diodes.
- Understand internal device operation through potential, field, carrier, carrier temperature
- Ionization rate and current density distributions.

- Analyze and understand breakdown mechanisms.
- Refine device designs to achieve optimal performance.
- Investigate failure mechanisms, such as leakage paths and hot electron effects.
- Study transient radiation effects, such as single event and dose rate upset.

1.5 Conclusion

Several procedures were done to determine the R_{th} and C_{th} . The R_{th} can be calculated from the frequency and static domain measurements. It is essential to perform the time domain measurements for the C_{th} calculation.

In the second chapter the basics of HBT is being covered. Some of its important characteristics are being explained. Finally industry standard model for HBT are being introduced and compared. High Current Model (HICUM) is introduced and compared to other industry model. The HICUM model has a one element thermal network which can be used to model the thermal characteristics of a device.

Chapter three discusses the physics behind heat flow and calculation necessary for a planar heat flow. Then more complicated models from a three dimensional heat flow is being introduced. The mathematical model from the heat flow equation and its correspondence to electrical analogy is being developed and explained. Four different approaches for calculating thermal impedance for a three dimensional heat flow is being discussed.

Chapter four introduces the proposed model for the thermal network in HBT. Simulation and modeling for each layer are done. Different approaches are discussed to calculate the elements in proposed model. Chapter five summaries all the TCAD simulations and device scaling tools. Chapter 6 looks into other areas of research than can be done for thermal analysis of HBT.

CHAPTER 2

HETERO-JUNCTION BIPOLAR JUNCTION TRANSISTOR

2.1 Introduction HBT

This chapter begins with a review of bipolar junction transistor (BJT). The functionality of a HBT is identical to that of a BJT. This chapter reviews BJT properties, functionalities and basic understanding of the device properties. It introduces various modeling tools and provides a comparison. The BJT was invented in 1948 at Bell Telephone Laboratories, New Jersey, USA. It was the first mass produced transistor. BJTs are preferred for high-frequency and analog applications because of their high speed, low noise, and high output power. The term bipolar emphasizes that both electrons and holes are involved in the operation of a BJT. In fact, minority carrier diffusion plays the leading role just as in the PN junction diode. The word junction refers to the fact that PN junctions are critical to the operation of the BJT. BJTs are also simply known as bipolar transistors. HBTs differ from conventional BJTs in their use of hetero-structures, particularly in the base-emitter junction. In a uniform material like in BJT, an electric field exerts the same amount of force on an electron and a hole, producing movements in opposite directions as represented in Figure 2.1a. With optimum modifications in the semiconductor energy gap, the forces on an electron and a hole may differ, and at an extreme, drive the carriers along the same direction as shown in Figure 2.1b. This modification would be the use of different material. The ability

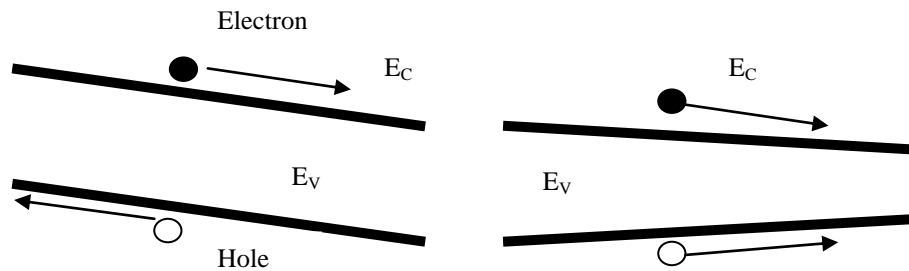


Figure 2.1 (a) An electric field applies the same amount of force but in opposite directions on an electron and a hole (b) Electron and hole can move in the same direction in a hetero-structure.[4]

to change the material composition to independently control and manipulate the movement of carriers

advantageous to the hetero-structures for transistor design [4].

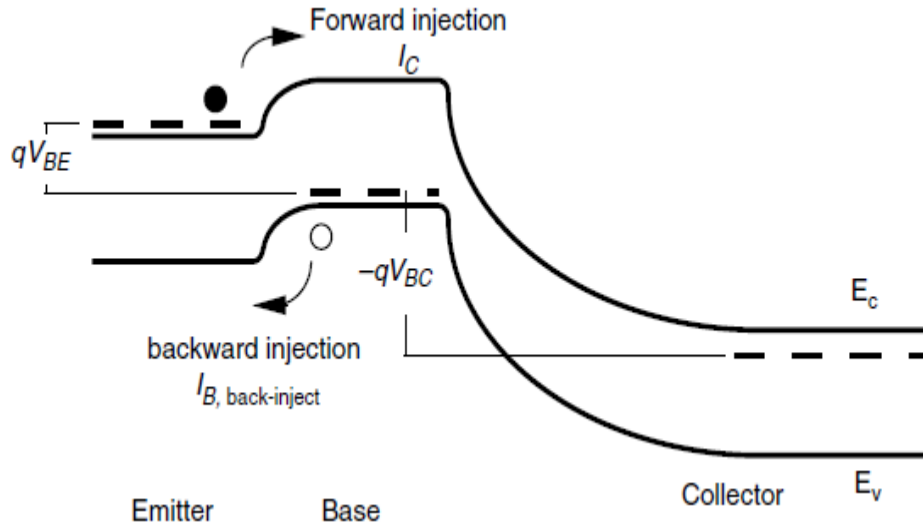


Figure 2.2 Band Diagram of an npn bipolar junction transistor. [5]

Figure 2.2 represents energy the band diagram of an npn BJT. The energy gap is the same throughout the entire transistor structure. The Fermi levels and the depletion regions of the band diagram reflect the BJT design constraint that the doping level is highest in the emitter, and lowest in the collector. The Fermi level in the emitter is above the conduction band, signifying that the emitter is degenerately doped. As shown in Figure 2.2 the two current components are forward injection and backward injection. Forward injection current is because of the flow of electron (Since the transistor considered in this example is an npn device, the minority carriers are electron in base. The opposite would be the case of a pnp). These electrons are emitted at the emitter, cross the base-emitter potential barrier with the help of the voltage between base-emitter (V_{BE}) bias, diffuses through the thin base layer as minority carriers, and then are swept by the large electric field in the reverse-biased base-collector junction. The carriers finally leave the collector as the collector current. Only a few electrons are lost through recombination with the majority holes in the base. Of the three phases of the carrier transport, the diffusion through the base layer is the rate-limiting step. Therefore a quantitative expression of I_C , intimately related to the base layer parameters. The amount of the electron injection from the emitter to the base can be controlled by varying

the V_{BE} . This current flow, however, is independent of V_{BC} , as long as the base-collector junction is reverse biased. The property that the desired signal (I_C) is modified by the input bias (V_{BE}) but unaffected by the output bias (V_{BC}) fulfills the requirement of a sound three-terminal transistor.

The current component caused by the movement of holes are back-injected from the base to the emitter. This current does not get collected at the collector terminal and does not contribute to the desired output signal. When V_{BE} is applied so that the desired electrons are emitted from the emitter to the base, holes are back-injected from the base to the emitter. The bipolar transistor is named because both electrons and holes play significant roles in the device operation. An optimum design of a bipolar transistor maximizes the electron current transfer while minimizing the hole current. The hole current, $I_{B,back-inject}$ is a base current because holes come from the base layer where they are majority carriers. I_C is limited by the diffusion process in the base where the electrons are minority carriers. $I_{B,back-inject}$ is limited by the diffusion in the emitter where the holes are minority carriers. Fick's law states that a diffusion current density across a layer is equal to the diffusion coefficient times the carrier concentration gradient.[5] The carrier concentrations at one end of the base layer and the emitter layer (for the calculation of $I_{B,back-inject}$) are both proportional to $\exp(qV_{BE}/kT)$, and are 0 at the other end which is at the base layer and collect layer.[5]

$$I_C = \frac{q \cdot A_{emit} \cdot D_{n-base} \cdot n_{i-base}^2}{X_{base} \cdot N_{base}} \exp\left(\frac{qV_{BE}}{kT}\right) \quad (2.1)$$

$$I_{B,back-inject} = \frac{q \cdot A_{emit} \cdot D_{n-emitter} \cdot n_{i-emitter}^2}{X_{emit} \cdot N_{emit}} \exp\left(\frac{qV_{BE}}{kT}\right) \quad (2.2)$$

where,

A_{emit}	= Area of the Emitter
D_{n-base} & $D_{n-emitter}$	= Electron diffusion coefficient in the base and emitter layers
N_{base} & $N_{emitter}$	= Doping concentration at the base and emitter layers
X_{base} & $X_{emitter}$	= Thickness of the base and emitter layers
n_{i-base} & $n_{i-emitter}$	= Intrinsic carrier concentration in the base and emitter layers

The collector current, I_C is proportional to emitter area because the collector current results from the carriers injected into the base from the emitter. In the case of the homo-junction BJT, the intrinsic carrier concentration in the base and emitter are equal the ratio of I_C to $I_{B,back-inject}$

$$\frac{I_C}{I_{B,back-inject}} = \frac{D_{n-base} \cdot X_{emit} \cdot N_{emit}}{X_{base} \cdot N_{base} \cdot D_{n-emit}} \text{ (BJT)} \quad (2.3)$$

From equation (2.3) it can be seen that emitter doping needs to be higher than the base doping for the collector current to dominate back injection current. That would also provide high emitter injection efficiency and therefore large current gain. A lightly doped base gives high base resistance, which is undesirable. Low emitter doping reduces emitter junction capacitance, in order to achieve high f_T and f_{max} . The significance of f_T and f_{max} is discussed later in this chapter. A heavily doped emitter can lead to a slight shrinkage of E_g in the emitter since as the donor states merge with conduction band which lowers emitter injection efficiency. Therefore in practice base are highly doped and emitter are lightly doped, with a tradeoff of having higher back injection current in case of BJT.

If transistors are made of materials that allow hetero-junctions to be used, the emitter injection efficiency can be increased without strict requirements on doping. By replacing the homo-junction emitter with a hetero-junction emitter which has a larger energy gap material, which allows for the design freedom of independently optimizing the $I_C / I_{B,back-inject}$ ratio and the doping levels.

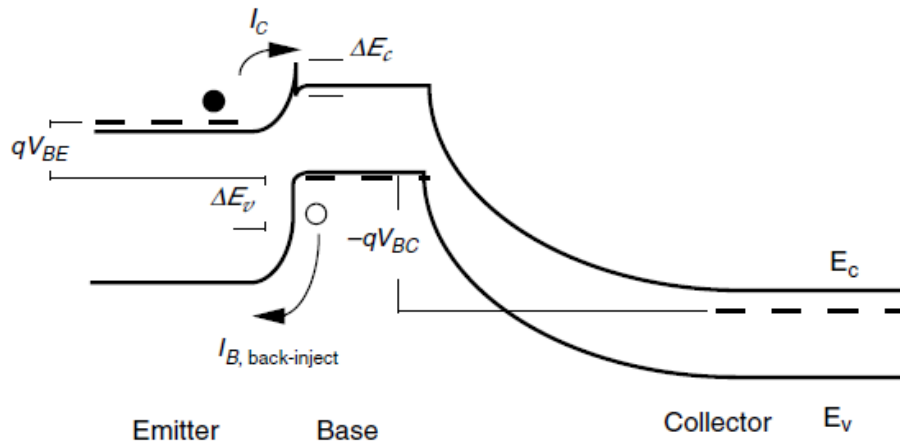


Figure 2.3 Band Diagram of a npn abrupt hetero-junction bipolar transistor.[5]

Figure 2.3 shows that the energy band gap at the emitter base junction is higher when compared to energy band gap at the emitter base junction in Figure 2.2. The energy gap difference in the base-

emitter hetero-junction of an HBT hinders the holes flow from the base because of the larger energy barrier than the electrons have from the emitter. With the same application of V_{BE} , the forces acting on the electrons and holes differ, favoring the electron injection from the emitter into the base to the hole back-injection from the base into the emitter. Figure 2.3 shows that the difference in the electron and hole barriers is ΔE_v , which is the valence band discontinuity. The $I_C/I_{B,back-inject}$ ratio of can be extended to the HBT as:

$$\frac{I_C}{I_{B,back-inject}} = \frac{D_{n-base} \cdot X_{emit} \cdot N_{emit}}{X_{base} \cdot N_{base} \cdot D_{n-emit}} \exp\left(\frac{\Delta E_v}{kT}\right) \text{ (ABRUPT HBT)} \quad (2.4)$$

Thus even if the base doping is higher than emitter doping the exponential factor would increase the $I_C/I_{B,back-inject}$ significantly, to improve HBT performance. The amount of improvement from a homo-junction to a hetero-junction depends on the band alignment properties of the two hetero-materials.

The hetero-junction shown in Figure 2.3 has a spike and notch in the conduction band commonly observed for heterojunctions. It is possible to smooth out such discontinuities in the bands by grading the composition of the ternary or quaternary alloy between the two materials as shown in Figure 2.4. Grading out the conduction band spike improves the electron injection by reducing the barrier that electrons must overcome.

There are some HBT designs, however, that make use of the spike as a "launching ramp" to inject hot electrons into the base. Similarly equation 2.4 can be modified for a graded junction.

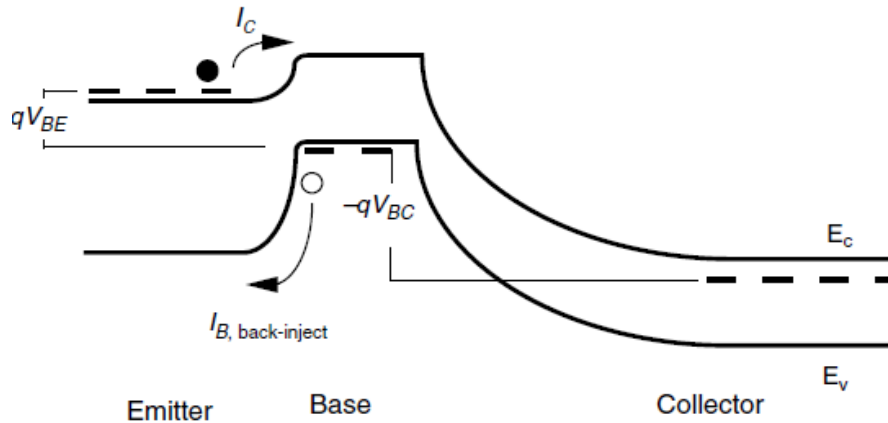


Figure 2.4: Graded Hetero-junction Bipolar Junction Transistor [5]

2.2 Base Current Components In HBT

Both HBTs and BJTs have five dominant base current components. The major difference between the HBT and the BJT is the base back injection current which is smaller in the HBT when compared to the BJT. The other four components are recombination current and are listed below.

- 1) Extrinsic base surface recombination current
- 2) Base contact surface recombination current
- 3) Bulk recombination current in the base
- 4) Space-charge recombination current in the base-emitter junction depletion region.

Depending on the transistor geometrical layout, epitaxial layer design, and the processing details that shape each of the five base current components, the current gain can have various bias and temperature dependencies. Figure 2.5 shows the four base recombination currents.

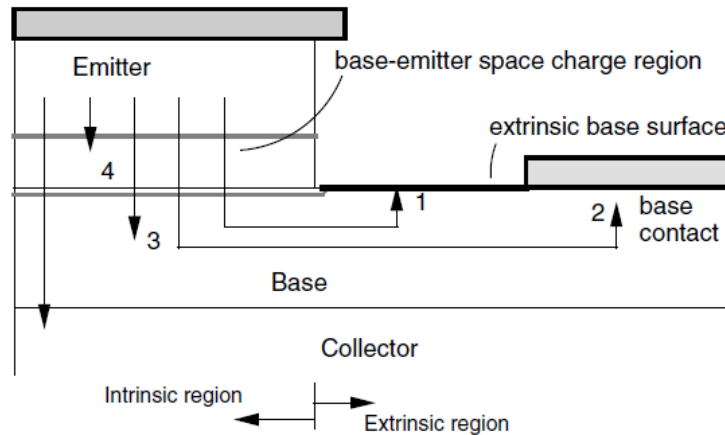


Figure 2.5 Four dominate base current representation [6]

2.3 High Frequency Performance

Current gain is the most important DC parameter characterizing a bipolar transistor. The high frequency properties are generally measured by two figures of merit: f_T , the cutoff frequency, and f_{max} , the maximum oscillation frequency. The cutoff frequency is the frequency at which the magnitude of the AC current gain (small-signal collector current divided by small-signal base current) decreases to unity. The cutoff frequency is also emitter-collector transit time from (2.5):

$$f_T = \frac{1}{2\pi\tau_{ec}} \quad (2.5)$$

The emitter-collector transit time can be broken up into several components. The emitter charging time, is the time required to change the base potential by charging up the junction base-emitter (C_{j-BC}) and base-collector (C_{j-BE}) capacitances through the differential base-emitter junction resistance:

$$\tau_e = \frac{kT}{qI_C} (C_{j-BE} + C_{j-BC}) \quad (2.6)$$

The second component is the base transit time, the time required for the forward-injected charges to diffuse or drift through base. It is given by,

$$\tau_b = \frac{X_{base}^2}{v \cdot D_{n-base}} \quad (2.7)$$

The space-charge transit time, is the time required for the electrons to drift through the depletion region of the base-collector junction. It is given by,

$$\tau_{sc} = \frac{X_{dep}}{2v_{sat}} \quad (2.8)$$

where, X_{dep} =depletion thickness of the base-collector junction

The last term, the collector charging time, is given by

$$\tau_c = (R_E + R_C) \cdot C_{j-BC} \quad (2.9)$$

where R_E and R_C are the device emitter and collector resistances, respectively. The value of this charging time depends greatly on the parasitic resistances. This is the term that degrades the HBT's high frequency performance when the contacts are poorly fabricated. The overall transit time is a sum of the four time constants:

$$\tau_{ec} = \frac{kT}{qI_C} (C_{j-BC} + C_{j-BE}) + \frac{X_{base}^2}{v \cdot D_{n-base}} + \frac{X_{dep}}{2v_{sat}} + (R_E + R_C) \cdot C_{j-BC} \quad (2.10)$$

In most HBTs, R_E and R_C are dominated by the electrode resistances; the epitaxial resistances in the emitter and collector layers are insignificant. The maximum oscillation frequency (f_{max}) is the frequency at which the unilateral power gain is equal to 1. The derivation is [7]:

$$f_{max} = \sqrt{\frac{f_T}{8 \cdot \pi \cdot R_B \cdot C_{j-BC}}} \quad (2.11)$$

The base resistance has three components that are roughly equal in magnitude. They are base electrode resistance ($R_{B,eltd}$); intrinsic base resistance ($R_{B,intrinsic}$); and extrinsic base resistance ($R_{B,extrinsic}$). $R_{B,eltd}$ is intimately related to processing, depending on the contact metal and the alloying recipe used to form the contact. In HBTs the base resistance is significant. As the base current flows horizontally from the base contact to the center of the emitter region, a non-zero voltage is developed, with an increasingly larger magnitude toward the center of the base. The effective base-emitter junction voltage is larger at the edge than at the center. Since the amount of carrier injection depends exponentially on the junction voltage at a given position, most of the injection takes place near the emitter edges, causing emitter crowding. Sometimes this phenomenon of non-uniform current conduction is referred to as the base crowding. Both terms are acceptable, depending on whether the focus is on the crowding of the emitter current or the base current. A figure of merit quantifying the severity of emitter crowding is the effective emitter width (W_{eff}). It is defined as the emitter width that would result at the same current level if current crowding were absent and the emitter current density were uniform at its edge value.

Because of the emitter crowding, all high-frequency III-V HBTs capable of GHz performance have a narrow emitter width (2 μm). The choice of the emitter width is a trade-off between the ease (cost) of device fabrication versus the transistor performance. The W_{eff}/W_E ratio increases with increase in the doping level (since the base resistance decreases). However, an increase in base doping is accompanied by shortened minority lifetime. The large increase in $I_{B,bulk}$ causes the emitter crowding to be more pronounced as N_{base} increases

2.4 Modeling Of HBT

2.4.1 Ebers-Moll Model

The Ebers–Moll model is a way to visualize as well as to mathematically describe both the active and the saturation regions of BJT operation. It is also the basis of BJT SPICE models for circuit simulation. The starting point is the idea that I_C is driven by two forces, V_{BE} and V_{BC} . It is a one-

dimensional BJT model, which focuses on the recombination in the base region.[8] The Ebers-Moll terminal current relations depend on the superposition of two current components: 1) from the emitter junction , 2) from the collector junction. The Ebers-Moll model is based on several assumptions such as low level injection, uniform doping in each region with abrupt junctions, one dimensional current flow, negligible recombination-generation in the space charge regions and negligible electric fields outside of space charge regions.

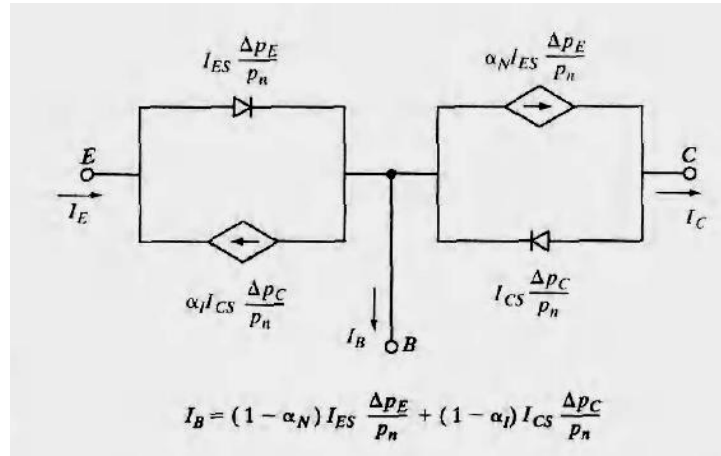


Figure 2.6 Eber-Moll model. [5]

This model contains two diodes and two current sources as indicated in Figure 2.6. The two diodes represent the base emitter and base-collector diodes. The current sources quantify the transport of minority carriers through the base region. I_E is the saturation current of the base-emitter diode and I_C is the saturation current of the base-collector diode. The α_F term is the forward transport factor and the α_R term is the reverse transport factor.

2.4.2 Gummel–Poon Model[9]

The BJT model used in circuit simulators such as SPICE can accurately represent the DC and dynamic currents of the transistor in response to $V_{BE}(t)$ and $V_{CE}(t)$. A typical circuit simulation model or compact model is made of the Ebers–Moll model plus additional enhancements for high-level injection, voltage-dependent capacitances that accurately represent the charge storage in the transistor, and parasitic resistances. This BJT model is known as the Gummel–Poon model(SGP).

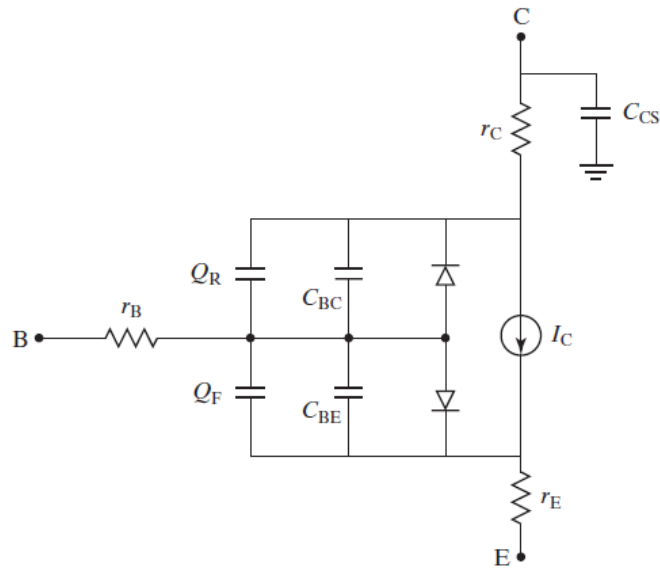


Figure 2.7 Gummel Poon Model[9]

The major improvements in the Gummel-Poon model are the inclusion of the high injection effect, Early effect, terminal series resistance, generation and recombination current sources, auger recombination, band gap narrowing, current crowding, and the Kirk effect.

2.4.3 Introduction To The High Current Model

High Current Model (HICUM) model for the BJT was developed in 1995 to replace the SGP model. HICUM is designed not only to mimic but also to overcome major deficiencies the SGP model lacks. The advantages of HICUM to its predecessor, the SGP model[5] are:

- Correct Early effect based on the junction charges
- Modified Kull model for quasi-saturation valid for high-injection at the collector junction
- Parasitic substrate transistor
- Weak avalanche current included at the base-collector junction
- Self-heating model defined embedded in the model code by a thermal network.
- First-order model of distributed-base for AC and DC emitter current crowding
- Improved single-piecewise junction capacitance model
- Improved complete static temperature mapping

- Inclusion of overlap capacitance
- Improved high-level diffusion capacitance modeling
- Second-order excess phase network consistent with AC->transient
- High-order continuity in equations
- Decoupling of base and collector current
- Improved Heterojunction Bipolar Transistor (HBT) modeling

In Figure 2.8, the thermal circuit is represented by a thermal resistance (R_{th}) and a thermal capacitance (C_{th}) which is incorporated in the HICUM model. The R_{th} and C_{th} results to a 1-pole network (circuit with a single time constant), and does not take into account the different regions of the device that could possibly contribute multiple poles to the thermal network. The thermal network is added to the four terminals transistor (collector, base, emitter and substrate) to model the local temperature rise. In Appendix G a procedure is being described where a fifth terminate of the self heating can be added to the model using Spectra.

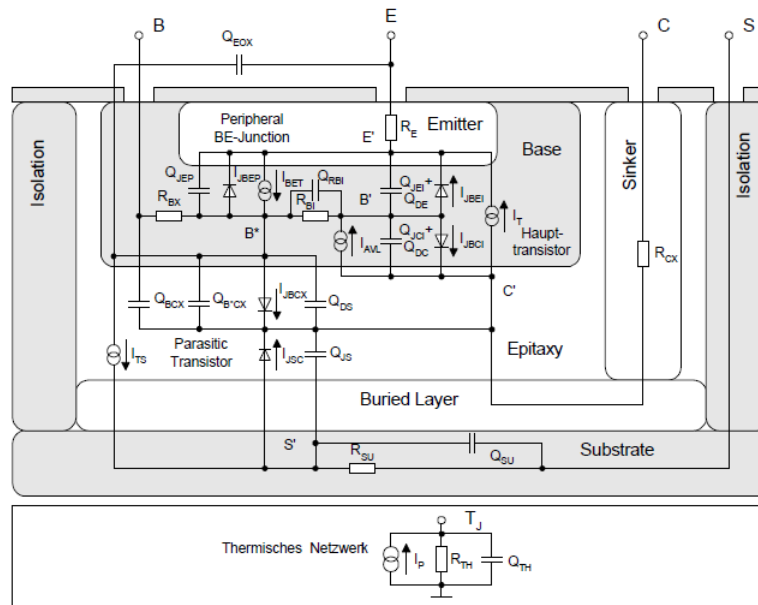


Figure 2.8 The HICUM Model [5,36].

2.4.4 Mextram Model For HBT

Mextram is a compact model for bipolar transistors: it supports the design of bipolar transistor circuits in silicon (Si) and silicon-germanium (SiGe) based process technologies. Mextram is developed and supported at Delft University of Technology. It includes self-heating, allowing device temperature to be dynamically computed. Self-heating calculations use only analytical derivatives, reducing simulation times thus numerical derivatives computation would be required. Modeling of SiGe is now possible, using a dedicated set of experimentally determined parameters which makes the extraction procedure easier.

Mextram has been selected by the Compact Model Council (CMC) as a world standard bipolar transistor compact model for the semiconductor industry. Mextram provides several features that Gummel-Poon model lacks:

- Bias-dependent Early effect
- High injection effects
- Ohmic resistance of the epitaxial layer
- Velocity saturation effects on the resistance of the epitaxial layer
- Hard and quasi saturation (including Kirk effect)
- Split base-collector and base-emitter depletion capacitance
- Substrate effects and parasitic PNP
- Current crowding and conductivity modulation of the base resistance
- First order approximation of distributed high frequency effects in the intrinsic base

(high frequency current crowding and excess-phase shift)

- Recombination in the base (for SiGe transistors)
- Early effect in the case of a graded bandgap (for SiGe transistors)
- Temperature scaling
- Self-Heating

The choice between HICUM and MEXTRAM depends on application. HICUM has a superior performing weak base-collector avalanche, substrate, depletion charge and capacitance models when compared to MEXTRAM. MEXTRAM performs faster and better current model which makes it ideal for HBT modeling. Generally for HBT, MEXTRAM is preferred [36]. [36] explains depends on the device, and its application, the models are chosen. But for thermal network characteristics does not vary from MEXTRAM to HICUM.

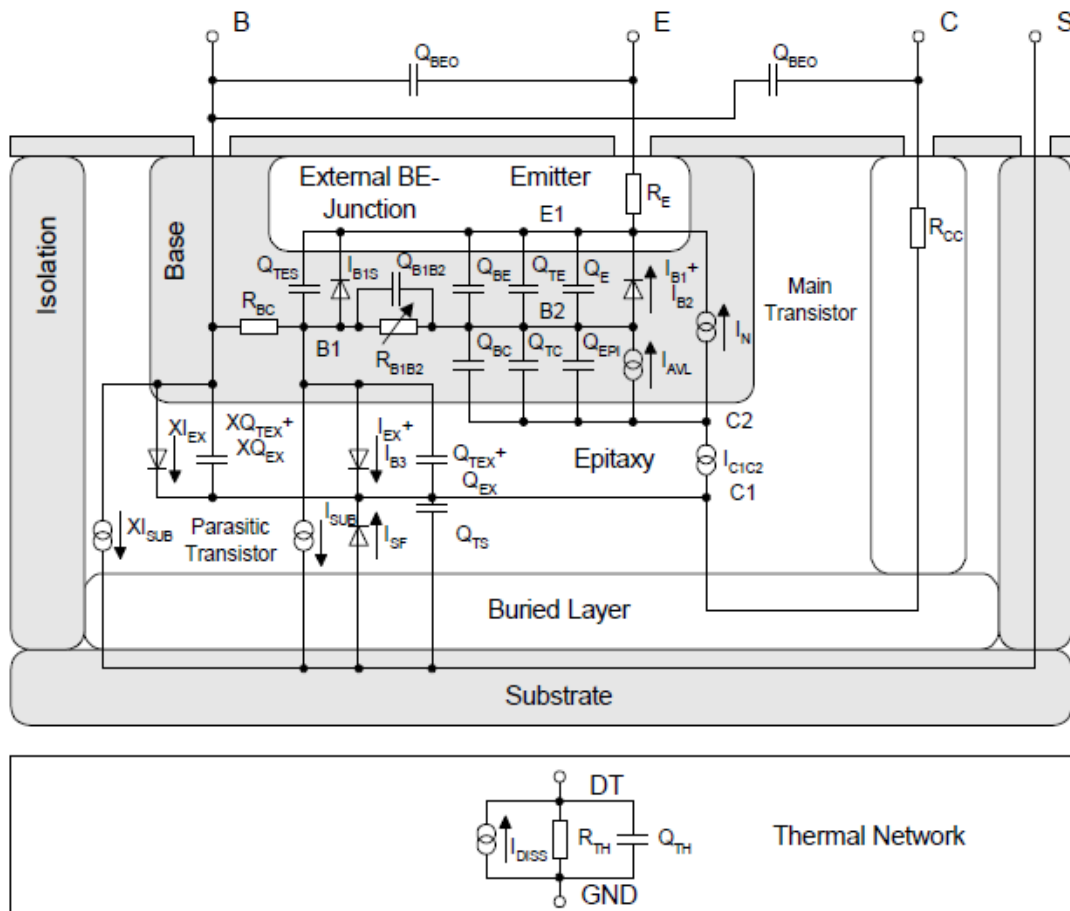


Figure 2.9 MEXTRAM Model Network

CHAPTER 3

HEAT FLOW FUNDAMENTALS AND NUMERICAL ANALYSIS

3.1 Heat Flow In Materials

3.1.1 Introduction

In this chapter, the process of heat flow is being presented. To calculate the spatially-dependent lattice temperature, the heat flow equation is [11]:

$$\rho \cdot c \cdot \frac{\partial T}{\partial t} = H + \vec{\nabla}(\lambda(T)) \cdot \vec{\nabla}T \quad (3.1)$$

Where ρ = the mass density of the material (g/cm³).

c = the specific heat of the material (J/g-K).

H = the thermal power density generated by the internal heat source (W/cm³)

λ = the thermal conductivity of the material (W/cm-K)

t = time (sec)

The term H in equation 3.1 represents the heat produced because of the transport of electrons, holes and recombination/generation carriers. Therefore, H can be represented as:

$$H = H_n + H_p + H_U \quad (3.2)$$

where, H_n = lattice heating due to electron transport

$$H_n = \frac{3k}{2} \cdot \frac{T_n - T}{\tau_{wn}} \cdot n \quad ,$$

where, T_n is the electron temperature and τ_{wn} is the energy relaxation time constant for electrons and n is

electron concentration. H_p = lattice heating due to hole transport

$$H_p = \frac{3k}{2} \cdot \frac{T_p - T}{\tau_{wp}} \cdot p$$

where, T_p is the hole temperature and τ_{wp} is the energy relaxation time

constant for holes and p is hole concentration. H_U = lattice heating due to carrier recombination/generation and is related to Shockley-Read-Hall recombination rate.

The approximate heat in electrons and holes can also be calculated from the product of their respective current density and ambient electric field vector in carrier transport equation.

3.1.2 Thermal Resistance In One Dimension

The thermal resistance can be calculated from equation (3.1). However even at steady state, the calculation gets complicated, and it is necessary to use the Kirchhoff Transform which gives the non-linear solution in terms of an assumed constant conductivity ($\lambda_o = \lambda(T_o)$). In the steady state $\partial T/\partial t = 0$ in equation (3.1), therefore:

$$H + \vec{\nabla}(\lambda(T) \cdot \vec{\nabla}T) = 0 \quad (3.2)$$

$$\Rightarrow -H = \vec{\nabla}(\lambda(T) \cdot \vec{\nabla}T) \quad (3.3)$$

The thermal heat produced in case of three dimensional heat flow can be calculated from

$$-\iiint H \, dx \, dy \, dz = \iiint \vec{\nabla}(\lambda(T) \cdot \vec{\nabla}T) \, dx \, dy \, dz \quad (3.4)$$

For the case of heat flow in the x dimension, equation (3.4) is considered only for the x dimension.

If the conductivity can be treated as a constant mean it is not dependent on temperature than,

$$-\int H \, dx = \int \vec{\nabla}(\lambda(T) \cdot \vec{\nabla}T) \, dx \quad (3.5)$$

$$\Rightarrow -H = (\lambda(T) \cdot A) \frac{\partial T}{\partial x} \quad (3.6)$$

where A is the area of thermal heat source

$$\Rightarrow -\int_{x_0}^{x_1} \frac{H}{(\lambda(T) \cdot A)} = \int_{x_0}^{x_1} \frac{\partial T}{\partial x} \quad (3.7)$$

$$\Rightarrow T_1 - T_0 = \frac{H}{(\lambda(T) \cdot A)} (x_1 - x_0) \quad (3.8)$$

where T_1 and T_0 are the temperatures at the heat source and the ambient, X_1 and X_0 are the distance between the heat source and the ambient, with heat flowing through in one dimension only.

Thermal resistance is defined as the ratio of the difference in temperatures between two isothermal surfaces and the total heat flow between them. Thermal resistance R_{TH} can be expressed as

$$R_{TH} = \frac{T_J - T_A}{P} \quad (3.9)$$

where T_j is the junction temperature, T_A is the ambient temperature, and P is the heat flow rate. The unit for R_{TH} is K/W.

Comparing equation (3.9) to (3.8) the R_{TH} in a material can be calculated

$$\Rightarrow R_{TH} = \frac{T_1 - T_0}{H} = \frac{1}{(\lambda(T) \cdot A)} (x_1 - x_0) \quad (3.10)$$

3.1.3 Application of Kirchhoff's Transformation.

The Kirchhoff Transform gives the non-linear solution in terms of constant conductivity ($\lambda_o = \lambda(T_o)$). The Kirchhoff Transform states

$$U = P \cdot R_0 = \frac{1}{\lambda_o} \int_{T_0}^{T_1} \lambda(T) dT \quad (3.11)$$

$$\frac{\partial U}{\partial T} = \frac{\lambda(T)}{\lambda_o} \quad (3.12)$$

where R_0 is the linear thermal resistance at the ambient temperature, U is heat generated

Applying equation (3.11) to (3.3) results to

$$-H = \vec{\nabla} \left(\lambda(T) \cdot \frac{\partial T}{\partial U} \vec{\nabla} U \right) \quad (3.13)$$

$$\Rightarrow -H = (\lambda_o \cdot \nabla^2 U) \quad (3.14)$$

$$= \left(\lambda_o \cdot A \cdot \frac{\partial U}{\partial x} \right) \quad (3.15)$$

$$\Rightarrow \frac{-H}{\lambda_o \cdot A} = \frac{\partial U}{\partial x} \quad (3.16)$$

$$\therefore \int dU = - \int_{x_0}^{x_1} \frac{H}{\lambda_o \cdot A} dx \quad (3.17)$$

Hence,

$$U = \frac{H}{\lambda_o \cdot A} (x_0 - x_1) \quad (3.18)$$

If the relationship of (T) in silicon is model as $T = \lambda_o (T/T_o)^n$, using Kirchhoff transformation from

(3.8) and 3.18, rise in Temperature can be calculated [12].

$$T - T_0 = T_0 \cdot \left\{ \left[1 + (n + 1) \frac{P \cdot R_0}{T_0} \right]^{\frac{1}{n+1}} - 1 \right\} \quad (3.19)$$

Substituting equation 3.19 in 3.10 results to a non-linear equation for R_{TH}

$$\Rightarrow R_{TH} = \frac{1}{(\lambda_0 \cdot A)} \cdot (x_1 - x_0) \cdot \left[1 + (n + 1) \frac{P \cdot R_0}{T_0} \right]^{1/(n+1)} \quad (3.20)$$

3.1.4 Thermal Conductivity of Silicon And Silicon Dioxide

Thermal conductivity of Silicon (k_{si}) varies with temperature and is modeled in the program Davinci by the equation below [11]:

$$\lambda = (A.TH.CON + B.TH.CON \cdot T + C.TH.CON \cdot T^2 + D.TH.CON \cdot T^{-E.TH.CON})^{-1} \quad (3.21)$$

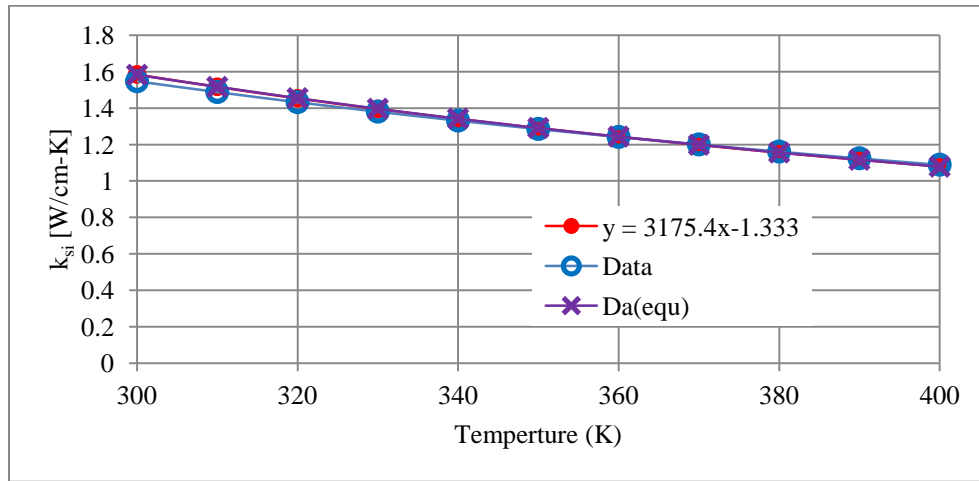


Figure 3.1 Thermal Conductivity of Silicon[13]

Figure 3.1 represent the data measurement for [13] with power model fits. A.TH.CON, B.TH.CON, C.TH.CON, D.TH.CON and E.TH.CON are parameters that were varied in order to fit the data in Davinci. The Da(equ) fit in the Figure 3.1 represents fit for the data by using the equation (3.20). If $(T_o) = \lambda_o (T/T_o)^n$ is considered then $n = -1.333$ as shown in power model fit in Figure 3.1 which is standard for silicon [13]. Applying Kirchhoff Transforms from equation 3.11 results to

$$U = P \cdot R_0 = \int_{T_0}^{T_1} \frac{\lambda(T)}{\lambda_0} dT$$

$$\begin{aligned}
&= \int_{T_0}^{T_1} \lambda_0 \left(\frac{T}{T_0}\right)^n \frac{1}{\lambda_0} dT \\
&= \int_{T_0}^{T_1} \left(\frac{T}{T_0}\right)^n dT \\
&= \frac{1}{n+1} \cdot \frac{1}{(T_0)^n} \cdot (T)^{n+1} \Big|_{T_0}^{T_1} \\
\therefore P \cdot R_0 &= \frac{1}{n+1} \cdot \frac{1}{(T_0)^n} \cdot (T)^{n+1} \Big|_{T_0}^{T_1} \\
&= \frac{1}{n+1} \cdot \frac{1}{(T_0)^n} \cdot (T_1)^{n+1} - \frac{1}{n+1} \cdot \frac{1}{(T_0)^n} \cdot (T_0)^{n+1} \\
&= \frac{T_0}{n+1} \left(\frac{T_1}{T_0}\right)^{n+1} - \frac{T_0}{n+1} \\
P \cdot R_0 &= \frac{T_0}{n+1} \cdot \left(\left(\frac{T_1}{T_0}\right)^{n+1} - 1 \right) \\
\Rightarrow T_0 \cdot \left(\frac{(n+1) \cdot P \cdot R_0}{T_0} + 1 \right)^{\frac{1}{n+1}} &= T_1 \\
\therefore T_1 - T_0 &= T_0 \cdot \left(\frac{(n+1) \cdot P \cdot R_0}{T_0} + 1 \right)^{\frac{1}{n+1}} - T_0 \\
&= T_0 \cdot \left\{ \left(\frac{(n+1) \cdot P \cdot R_0}{T_0} + 1 \right)^{\frac{1}{n+1}} - 1 \right\} \quad (3.22)
\end{aligned}$$

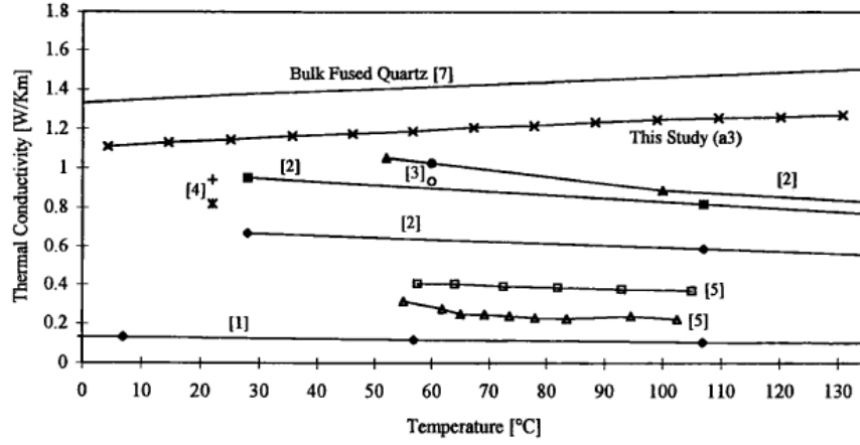


Figure 3.2 Thermal Conductivity of Silicon Dioxide for thickness greater than 300nm [14]

From Figure 3.2 similar conductivity of silicon dioxide can be obtained. Several measured data for silicon is being presented in Figure 3.2 [14]. For thickness greater than 300nm, the data (This Study(a3)) was used. For thickness less than 150nano meter, data in Figure 3.3 was used.

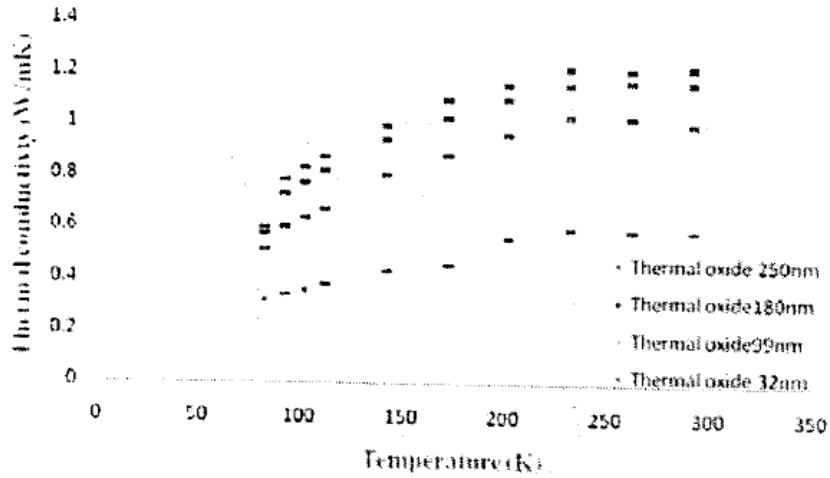


Figure 3.3 Silicon dioxide thermal conductivity for thickness below 300nm[15].

For silicon dioxide, after using Kirchhoff Transformed, the solution can be represented as

$$T - T_0 = \frac{\lambda_0}{\lambda'} \cdot \left\{ \sqrt{1 + 2 \frac{\lambda'}{\lambda_0} P \cdot R_0} - 1 \right\} \quad (3.23)$$

where $\lambda_{SiO_2}(T) = \lambda_0 + \lambda'(T - T_0)$, $\lambda' = d\lambda/dT$

For SiO₂ with thickness greater than 300nano meter,

$$\lambda_0 = 1.14 \times 10^{-2} \text{ W/cm-K}, T_0 = 300 \text{ K and } \lambda' = 1.4 \times 10^{-5} \text{ W/cm-K}^2 \text{ [13]}$$

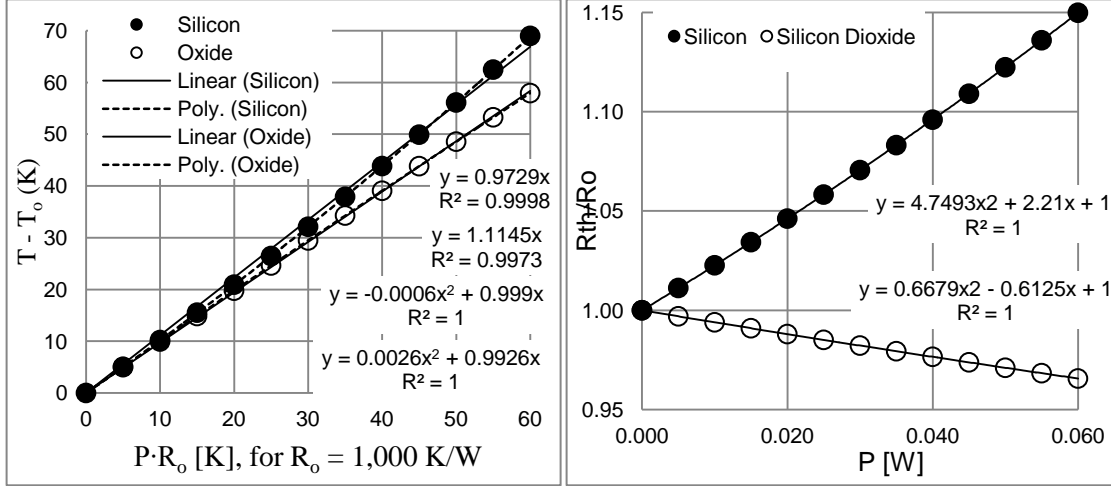


Figure 3.4 (a) Represents rise in temperature vs rise in power for silicon and silicon dioxide.
(b) Rise in R_{TH} vs rise in Power

3.1.5 Thermal Capacitance

Thermal capacitance can be derived from the heat flow equation. Material has the ability to absorb heat energy and release it. Thermal capacity is defined as the amount of thermal energy required to raise the temperature of one mole of material by one Kelvin [16]. This is represented in equation (3.20).

$$C = \frac{dH}{dT} \quad (3.24)$$

where C is the heat capacity. The unit of C is [W-s/mol-K], H is [W-s] and T is [K]. From the heat flow equation in 3.1, the term $\rho \cdot c \cdot \frac{\partial T}{\partial t}$ represents the time varying heat flow dependency. For one dimensional heat flow, the thermal capacitance is:

$$C_{TH} = c_p \cdot \rho \cdot V \quad (3.25)$$

where c_p is the specific heat of the material, ρ is the density of the material, and V is the volume of the material ($V = A \cdot L$). L is the thickness.

3.2 The Electrical And Thermal Analogy

3.2.1 Introduction

Modeling of heat flow in the transistor requires an equivalent thermal analogy to electrical circuit which can be used to develop the thermal network. This can be done by comparing poisson equation to heat flow equation. A direct comparison is done in Table 3.1 between Poisson equations to the heat flow equation. From the comparison the between the electrical and thermal domains are listed in Table 3.2. If thermal conductivity is constant, the temperature in the thermal domain is analogous to voltage in the electrical domain. The rate of heat flow in the thermal domain is analogous to current flow in the electrical domain and ambient temperature in the thermal domain is analogous to ground in the electrical domain. Thus the linear heat-flow solution for a region with R_{th} is analogous to Ohm's law:

$$\Delta T = P \cdot R_{th} \text{ is the analogy to } \Delta V = I \cdot R \quad (3.26)$$

Table 3.1 Poisson Equation vs Heat Equation

POISSON EQUATION	HEAT FLOW EQUATION
$\nabla^2 V = -\frac{\rho}{\epsilon}$ <p>ρ = Charge Density ϵ = Permittivity</p>	$\nabla^2 T = \frac{-g(x, y, z)}{k}, \text{ where } k = \text{constant}$ <p>$\Delta T = T - T_0$ [K] is the temperature rise above local ambient k = Thermal Conductivity [W-cm⁻¹K⁻¹] g = Volumetric Heat Gen. Rate [W cm⁻³]</p>
$\frac{\partial^2 V}{\partial x^2} = R C \frac{\partial V}{\partial t}$	$\frac{\partial^2 T}{\partial x^2} = R C \frac{\partial T}{\partial t}$

From Figure 3.5(a) the analogy between the resistances in the thermal domain and the electrical domain is illustrated by a block of solid whose top and bottom surfaces are maintained at temperatures T_1 and T_2 respectively. The thermal resistance of the solid is given by:

$$R_{TH} = \frac{T_1 - T_2}{P} \quad (3.27)$$

where P is the power flowing from the top surface to the bottom surface. The equivalent electrical network for the block is shown in Figure 3.5 (b). The heat energy stored (H) in the thermal capacitances is calculated as shown below:

$$\begin{aligned}
 H &= (T_1 - T_{ambient}) \cdot \frac{C_{TH}}{2} + (T_2 - T_{ambient}) \cdot \frac{C_{TH}}{2} \\
 &= (T_{avg} - T_{ambient}) \cdot C_{TH}
 \end{aligned}
 \tag{3.28}$$

where $T_{avg}=(T_1+T_2)/2$ is the average temperature of the solid and $T_{ambient}$ is the ambient temperature.

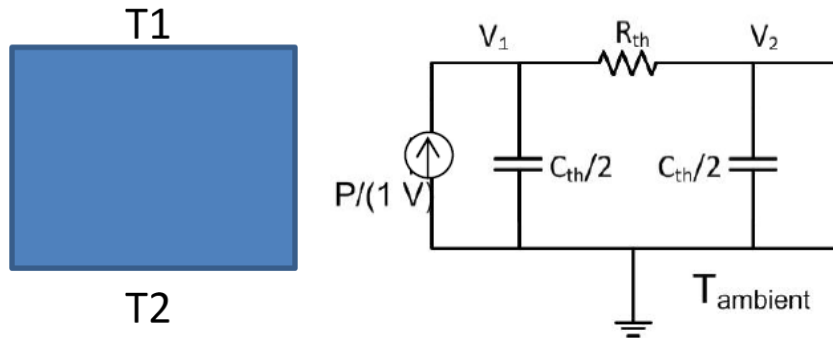


Figure 3.5 (a) A block of where heat flowing from top to bottom (b) the equivalent circuit

Table 3.2 Thermal – Electrical analogy [17]

Thermal		Electrical	
Temperature	T in K	Voltage	V in volt
Heat flow	P in W	Current	I in Amp
Thermal resistance	R_{TH} in K/W	Resistance	R in ohm
Thermal capacitance	C_{TH} in J/K	Capacitance	C in Farad
Thermal flux [4]	Φ_{TH} in W/m ²	Electrical Current Density	J in A/m ²

From the equivalent circuit model in Figure 3.5 (b) the total thermal resistance is represented by R_{TH} [K/W] and the total thermal capacitance is represented by C_{TH} [W/K]. I_{TH} [A] is the power which is consumed by the device divided by 1 volt and dt is the temperature of the device after I_{TH} is applied to the

combination of R_{TH} and C_{TH} . The ambient temperature is represented by tl and t is the temperature at any given instant. So, the device temperature (dt) for the thermal network can be calculated by equation 3.25:

$$dt(t) = tl + I_{TH} \cdot R_{TH} \left(1 - e^{-\frac{t}{\tau}}\right) \quad (3.29)$$

$$\frac{dt(t)-tl}{I_{TH}} = R_{TH} \left(1 - e^{-\frac{t}{\tau}}\right) \quad (3.30)$$

$$Z_{TH}(t) = \frac{T-T_{ambient}}{P(t)} = R_{TH} \left(1 - e^{-\frac{t}{\tau}}\right) \quad (3.31)$$

where τ is the thermal time constant ($\tau = R_{TH} \cdot C_{TH}$) in seconds, $Z_{TH}(t)$ is the thermal step response of the thermal impedance which consists of one thermal resistance and one thermal capacitance [$R_{TH} // C_{TH}$], $T(t)$ is the time dependent temperature at each node [dt], $T_{ambient}$ is the constant temperature at the heat sink [tl], and $P(t)$ is the total power [$I_{TH}(t) \times I[V]$]. The units are for $T(t)$ is [K], $T_{ambient}$ is [K], and $P(t)$ is [W]. It is assumed that $T(t)$ is the time dependent maximum lattice temperature in the device. The usual way to characterize the thermal network is the analysis of the thermal response to a step in the applied power. This thermal response is called the transient thermal impedance [18]. The transient thermal impedance is called the thermal step response in this paper. The thermal step response of the thermal network can be expressed by a multi-pole model as shown in equation (3.28).

$$Z_{TH}(t) = R_{TH1} \left(1 - e^{-\frac{t}{\tau_1}}\right) + R_{TH2} \left(1 - e^{-\frac{t}{\tau_2}}\right) + \dots + R_{THn} \left(1 - e^{-\frac{t}{\tau_n}}\right) \quad (3.32)$$

3.2.2 Distributed Nature Of Heat Flow

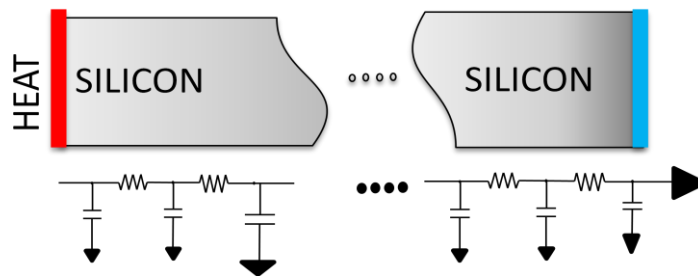


Figure 3.6 Heat flow through silicon modeled as a distributive network.

A silicon structure can be sub-divided into several silicon slab. Heat spreads with a constant angle from the power source[19]. The value of the angle depends on substrate boundaries [12, 20]. Each

section contributes to the total R_{Th} and C_{Th} of the structure. If each section is represented by equal values of R_{th} and C_{th} , the corresponding $C_{Th}/2$ capacitors are aggregated at each node. Note that the “ambient end” (right end) $C_{Th}/2$ is short-circuited. The left end is the heat source. The distributed equivalent circuit analogy simulation is obtained from the following network in Figure 3.7.

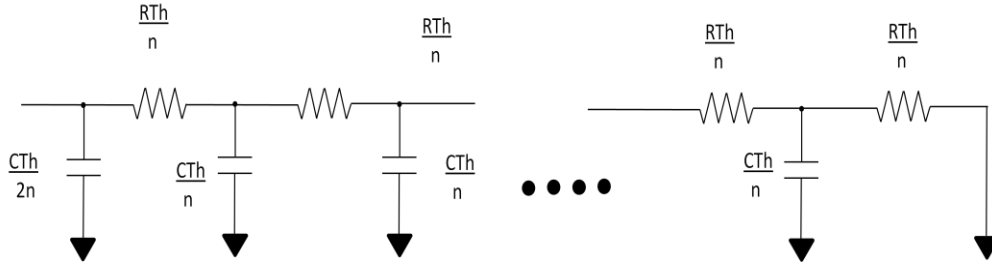


Figure 3.7 The distributive network in silicon.

Considering a silicon structure of size $3.7\mu\text{m} \times 2.5\mu\text{m} \times 10\mu\text{m}$, calculation is done to calculate the total R_{TH} and C_{TH} . Here t is considered as thickness of each slab.

$$R_{TH} = \frac{t}{\lambda \cdot A} = 6989 \text{ ; } C_{TH} = \rho \cdot c \cdot t \cdot A = 18.2 \cdot 10^{-9} \text{ ; } T_{au} = R_{TH} \cdot C_{TH} = 1.26 \cdot 10^{-6}$$

If 10 equally distance sections of the structure is considered, the respective thermal impedance for each section can be considered to be equal to

$$R_{Th} = \frac{R_{TH}}{n} \text{ ; } C_{Th} = \frac{C_{TH}}{n} \quad (3.33)$$

where n equal to 10.

A 3-D Davinci simulation for the silicon structure is compared to the distributive network is compared in Figure 3.8.

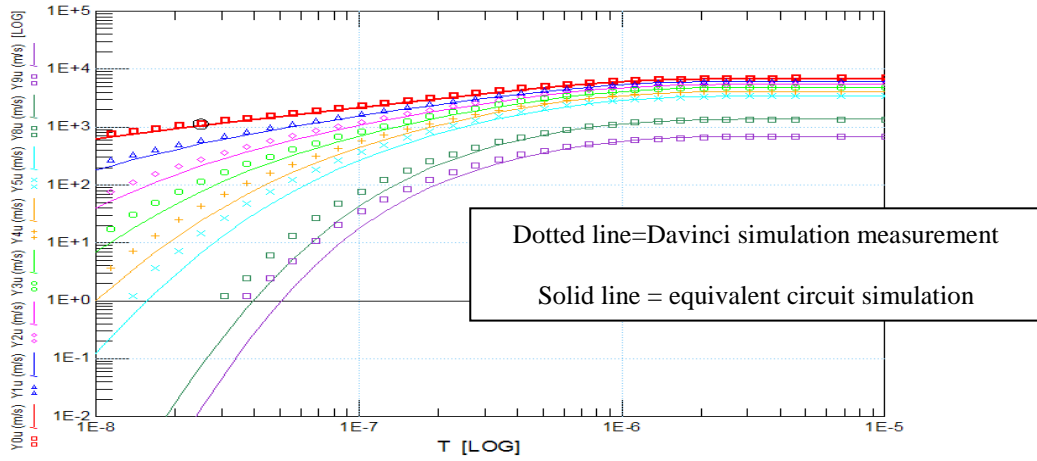


Figure 3.8 Davinci simulation compared to distributive network.

Table 3.3 Comparison between Davinci simulation and mathematical calculation.

	W	L							
	3.8	2.5							
	Si	Si	Si	Si	Si	Si	Si	Si	Si
t(micron)	10	9	8	7.00	6	5	4	2	1
Rth	6,805.22	6,124.70	5,444.18	4,763.65	4,083.13	3,402.61	2,722.09	1,361.04	680.52
Cth	1.87E-10	8.43E-11	7.49E-11	6.56E-11	5.62E-11	4.68E-11	3.75E-11	1.87E-11	9.37E-12
TAUth	1.27E-06	5.16E-07	4.08E-07	3.12E-07	2.29E-07	1.59E-07	1.02E-07	2.55E-08	6.37E-09
Final Davinci Rth results	6881.6	6186.7	5493.0	4800.4	4110.3	3421.4	2733.7	1364.	681.6

Using the equation from 3.28 a simple slab calculation is shown in Table 3.3. The Table also includes the Davinci result as in Figure 3.9 so that a comparison can be established.

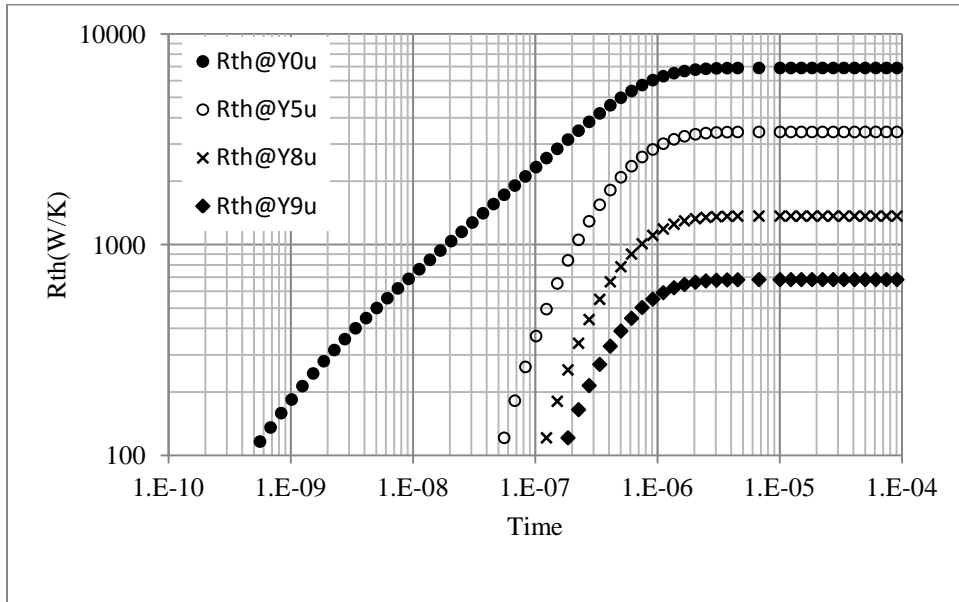


Figure 3.9 Davinci simulation result for a slab.

3.2.3 Steady State Heat Flow

The study of heat flow has been studied by considering the heat flow to be analogous to the flow of charges. It has been shown in Section 3.2.2 that the heat flow is approximately proportional to the temperature gradient and current flow is proportional to the potential gradient. The constant of proportionality K is called the thermal conductivity [21].

$$\vec{h} = K\nabla T \quad (3.34)$$

Equation 3.30 is similar to the relation between electric field E and electrostatic potential Φ given by

$$\vec{E} = -\nabla\Phi \quad (3.35)$$

Therefore steady heat-flow problems and electrostatic problems are the same as in equation (3.34). The heat flow vector \vec{h} corresponds to \vec{E} , and the temperature T corresponds to Φ .

3.2.4 Dynamic Heat Flow

Equation (3.35) reflects the dynamic electrical thermal analogy where the temperature T can be a dependant on time. The voltage equation in a transmission line with R and C elements (one dimensional dependence) is given by

$$\frac{\partial^2 V}{\partial x^2} = R' \cdot C' \cdot \frac{\partial V}{\partial t} \quad (3.36)$$

where R' and C' are the resistance and capacitance per unit length of the transmission line, respectively.

The heat flow equation (heat diffusion equation) in a material is given by

$$\nabla^2 T = R_{th} \cdot C_{th} \cdot \frac{\partial T}{\partial t} \quad (3.37)$$

where R_{th} and C_{th} are the resistance and capacitance per unit volume of the material, respectively.

3.2.5 Thermal Resistance

Solving equation (3.37) with appropriate boundary conditions, we can find out the (lumped) thermal resistance of the material as done in equation 3.31. For derivation purpose, a material of length l and cross-section area S is considered with the ends at temperature T_0 and T_l . The thermal resistance is :

$$R_{th} = \frac{T_0 - T_l}{P} = \frac{l}{kS} \quad (3.38)$$

where R_{th} is the thermal resistance, P is the time rate of heat flow through the material and k is the thermal conductivity of the material. The unit for R_{th} is K/W . R_{th} is compared to the electrical resistance R of a material with conductivity σ , length l and cross-section S which has voltages V_0 and V_l applied at its ends, with current I through it.

$$R = \frac{V_0 - V_l}{I} = \frac{l}{\sigma S} \quad (3.39)$$

3.2.6 Thermal Capacitance

Thermal capacitance is a measure of how much heat energy can be stored and dissipated in a material. The thermal capacitance (lumped model) is given by

$$C_{th} = c_p \rho V \quad (3.40)$$

where c_p is the specific heat at constant pressure, ρ is the density and V is the volume of the material. The unit of thermal capacitance is J/K . Thermal capacity is defined as the amount of thermal energy required to raise the temperature of one mole of material by one Kelvin therefore:

$$C_{th} = \frac{\Delta Q}{\Delta T} \quad (3.41)$$

where Q is charge and T is time. This implies that the change in heat stored in the material per degree Kelvin change in temperature.

3.2.7 Conservation Of Charge And Energy

In the electrical domain, the principle of conservation of charge corresponds to the principle of conservation of energy in the thermal domain. This is listed below

- The electric charge (Q_c) stored in a capacitor is given by integrating the current $i(t)$ through it with respect to time (t) i.e.

$$Q_c = \int i(t) dt \quad (3.42)$$

- The heat energy Q_h stored in a capacitor is given by integrating the power flow through the material with respect to time because, power ($P(t)$) flow in thermal domain corresponds to current in electrical the domain.

$$Q_h = \int P(t) dt \quad (3.43)$$

- The electric energy stored (En) in a capacitor is given by

$$En = \int_0^Q \frac{q}{C} dq = 1/2 \cdot C \cdot V^2 \quad (3.44)$$

The corresponding relation in thermal domain gives a quantity whose dimensions (J. K; joules. kelvin) are not equal to those of energy (J). Therefore, conservation of charge in the electrical domain corresponds to conservation of heat energy in the thermal domain.

3.3Mathematical Calculation for 2D-3D Heat Flow in Silicon

This section discusses several heat flow two dimensional and three dimensional calculations. The calculation of heat flow has been compared with simulation using 3D TCAD and measurements. Three main heat flow techniques are used for the mathematical analysis in this dissertation.

3.3.1 Joy And Schlig[22]

A mathematical model of the three dimensional transient heat flows which takes into account the physical structure of the device and the actual region of power dissipation was presented by Joy and Schlig. This section describes their mathematical model. Their model predicts the time-dependent temperature response to power dissipation as a function of time. Several assumptions are considered

regarding the structure of the device. The effect of all chip boundaries except the one closest to the device is neglected. The top surface of the chip may be considered to be adiabatic. This permits using symmetry in the real medium which is a semi-infinite homogeneous half space for analysis. The region of power dissipation is approximated by a solid rectangular parallelepiped submerged beneath the surface of the semi-infinite medium as shown below.

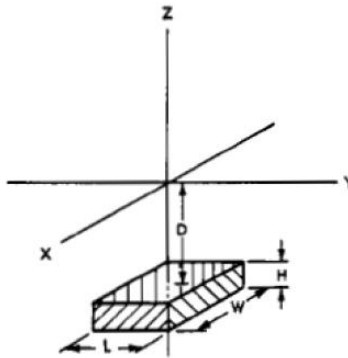


Figure 3.10 Heat source below the surface of semi-infinite medium [22]

In this method the heat dissipation occurs within a specific volume (LWH) at a depth D below the surface of the semi-infinite medium, as shown in Figure 3.10. The mathematical result for a semi-infinite medium with an adiabatic surface can be obtained by using the method of imaging which is done by placing an identical semi-infinite block dissipating the same amount of heat at the same distance D from the adiabatic surface so that there is no effective flow of heat across the surface which is shown in Figure 3.11 .

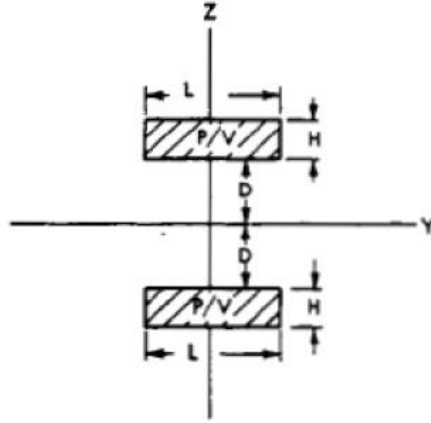


Figure 3.11 Cross-section of heat source and its image[22]

The two heat sources are mirror images of each other, generating the same amount of heat. The temperature response as a function of time is given by

$$T(x, y, z, t) = \frac{P}{8C} \int_0^t \{I_1(u) \cdot I_2(u) \cdot I_3(u)\} du \quad (3.45)$$

where,

$$I_1(u) = \left[\operatorname{erf} \left(\frac{\frac{W}{2} + x}{\sqrt{4 \cdot k \cdot u}} \right) + \operatorname{erf} \left(\frac{\frac{W}{2} - x}{\sqrt{4 \cdot k \cdot u}} \right) \right]$$

$$I_2(u) = \left[\operatorname{erf} \left(\frac{\frac{L}{2} + y}{\sqrt{4 \cdot k \cdot u}} \right) + \operatorname{erf} \left(\frac{\frac{L}{2} - y}{\sqrt{4 \cdot k \cdot u}} \right) \right]$$

$$I_3(u) = \left[\operatorname{erf} \left(\frac{D + H + z}{\sqrt{4 \cdot k \cdot u}} \right) + \operatorname{erf} \left(\frac{-D - z}{\sqrt{4 \cdot k \cdot u}} \right) + \operatorname{erf} \left(\frac{D + H - z}{\sqrt{4 \cdot k \cdot u}} \right) \operatorname{erf} \left(\frac{-D + z}{\sqrt{4 \cdot k \cdot u}} \right) \right]$$

k is the thermal diffusivity, ρ is the density of medium, c_p is the heat capacity, P is total power delivered.

Therefore the thermal resistance (R_{TH}) and capacitance (C_{TH}) are calculated by evaluating equation 3.41

as $t \rightarrow \infty$:

$$C_{TH}(x, y, z, t) = V \cdot \rho \cdot c_p \quad | \quad R_{TH}(x, y, z, t) = \frac{T(x, y, z, t)}{P} \quad (3.46)$$

Although this method leads to a compact form of thermal resistance for thermal sources immersed in a simple homogeneous medium, a rather complicated boundary condition should be dealt with in the presence of additional structures such as oxide trenches. Heat conduction in a wafer is similar to the heat conduction in a semi-infinite solid since the thickness of the wafer is large compared to the thickness of the Si tub and the buried oxide. It is to be noted that the distributed models are more relevant than lumped models for the calculation of wafer thermal impedance.

3.3.2 Rinaldi Method Without Trench Isolation [23, 24]

A mathematical model of the transient temperature response of integrated devices was proposed by N. Rinaldi which takes into account the three-dimensional (3-D) nature of heat flow and the physical structure of the device. Simple analytical relations for the transient thermal impedance and thermal time constants are considered in this model. The calculations have been using Joy and Schlig's. The region where power is dissipated is modeled as a solid rectangular parallelepiped located beneath the surface of a semi-infinite semiconductor substrate, as shown in Figure 3.12 (a). The top surface is assumed adiabatic. The region where power is dissipated is modeled as an infinitely thin rectangle of dimensions $W \times L$ located at a depth D from the surface as shown in Figure 3.12(b). An image source is introduced at a position symmetric with respect to the $z = 0$ plane.

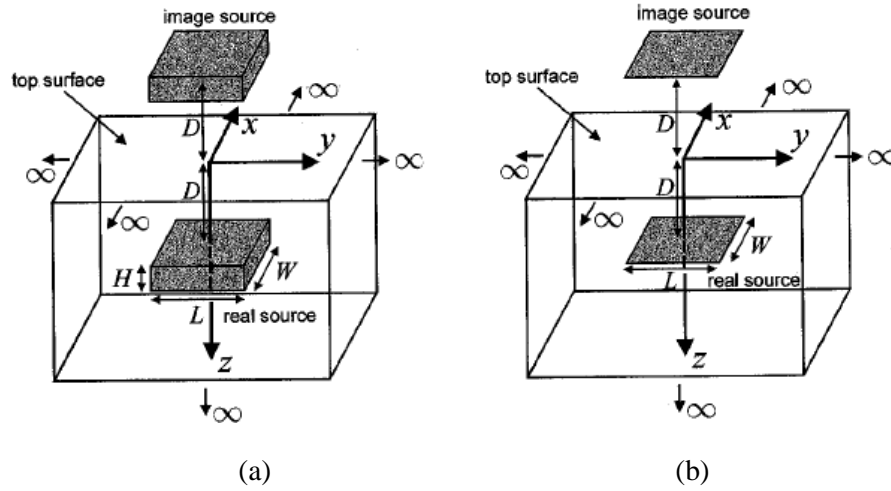


Figure 3.12 (a) Thermal model of an integrated device with a volume heat source (b) Thermal model of an integrated device with a surface heat source [23]

The temperature response at the center of the heat source, assuming that $D = 0$ in Figure 3.12 is given by[23]

$$Tp(t) = \frac{P \cdot \sqrt{\alpha}}{k \cdot W \cdot L \cdot \sqrt{\pi}} \int_0^t \left[\operatorname{erf} \left(\frac{\sqrt{\pi}}{2} \cdot \sqrt{\frac{t_1}{u}} \right) \cdot \operatorname{erf} \left(\frac{\sqrt{\pi}}{2} \cdot \sqrt{\frac{t_2}{u}} \right) \right] \frac{du}{\sqrt{u}} \quad (3.47)$$

where α is the thermal diffusivity in cm^2/s , P is the power dissipated in watts, k is the thermal conductivity of substrate ($\text{W}/\text{cm}\cdot\text{K}$) and $W \cdot L$ is the area of the heat source, $t_1 = W^2/(4\pi\alpha)$ and $t_2 = L^2/(4\pi\alpha)$. Since $L > W$, it is assumed that $t_1 < t_2$ without the loss of generality. The above equation does not have an analytical solution therefore some approximation has been considered to simplify the integrand function. The approximations are:

$$\operatorname{erf}(\vartheta) = \begin{cases} 1 & \text{for } \vartheta \rightarrow \infty \\ 0 & \text{for } \vartheta = 0 \\ \frac{2}{\sqrt{\pi}} \vartheta & \text{for } 0 < \vartheta \leq \frac{\sqrt{\pi}}{2} \\ 1 & \vartheta \geq \frac{\sqrt{\pi}}{2} \end{cases} \quad (3.48)$$

Using the approximations from equation (3.48), equation (3.49) can be simplified to calculate transient thermal impedance.

$$Z_{th}(t) = \frac{Tp(t)}{P} = \frac{\sqrt{\alpha}}{k \cdot W \cdot L \cdot \sqrt{\pi}} \cdot \begin{cases} 2\sqrt{t}, & t \leq t_1 \\ 2\sqrt{t} \left[1 + \ln \sqrt{\frac{t}{t_1}} \right], & t_1 \leq t \leq t_2 \\ 2\sqrt{t} \left[1 + \ln \sqrt{\frac{t}{t_1}} \right] - 2\sqrt{t_1 \cdot \frac{t_2}{t}}, & t_2 \leq t \end{cases} \quad (3.49)$$

where the transient thermal impedance $Z_{th}(t)$ has been defined as the ratio between the peak temperature $Tp(t)$, dissipated power P and α is a constant. The steady-state value of the peak temperature can be easily obtained by letting $t \rightarrow \infty$

$$R_{th} = \frac{Tp(\infty)}{P} = \frac{\sqrt{\alpha}}{k \cdot W \cdot L \cdot \sqrt{\pi}} \cdot 2\sqrt{t} \left[1 + \ln \sqrt{\frac{t}{t_1}} \right] = \frac{1}{k \cdot L \cdot \pi} \left[2 + LN \left(\frac{L}{W} \right) \right] \quad (3.50)$$

The calculation of C_{th} is done from the derivation of rise time and delay for the transient function. A normalized thermal impedance (ζ_{th}) is defined as

$$\zeta_{th} = \frac{Tp(\tau)}{Tp(\infty)} = \begin{cases} \frac{\sqrt{\tau \cdot a}}{2 + \ln(a)}, & \tau \leq \tau_1 = 1/a \\ \frac{1}{2} \cdot \frac{2 + \ln(\tau \cdot a)}{2 + \ln(a)}, & \tau_1 \leq \tau \leq \tau_2 \\ 1 - \frac{\sqrt{\tau \cdot a}}{2 + \ln(a)}, & \tau_2 \leq \tau \end{cases} \quad (3.51)$$

where $\tau = t/t_{th}$, $\tau_1 = t_1/t_{th} = 1/a$ and $\tau_2 = t_2/t_{th} = a$

The normalized delay and rise time can be calculated as

$$\tau_{delay} = \frac{1}{a} \left(\frac{2 + \ln(a)}{10} \right) \quad (3.52)$$

$$\tau_{rise} = \frac{1}{\tau_{delay}} - \tau_{delay} \quad (3.53)$$

3.3.3 N. Rinaldi Method with Trench Isolation[25,26]

All BJT and HBT devices are surrounded by isolation oxide to protect individual devices electrical integrity. The two approaches presented above can be used for wafer because wafers are not bounded by isolation oxide. The buried layer which is the tub of the device several different approach is necessary for calculation of heat flow. Many bipolar processes are based on deep trench isolation (DTI) because for the need of electrically insulating the active devices from neighboring transistors.

Unfortunately, due to the poor thermal conductivity of the trench-filling materials, the heat flow coming

from the active transistor area is mostly confined within the silicon-only region enclosed by trench before spreading into the substrate, thereby leading to lower thermal conduction compared to bulk-silicon transistors of comparable size.

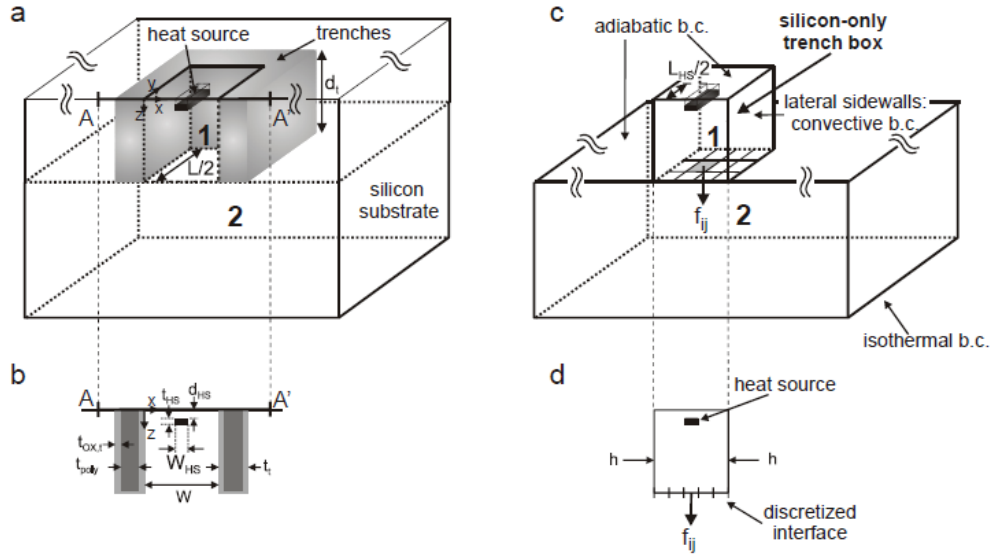


Figure 3.13 (a) Analyzed trench domain and (b) cross-section corresponding to the trench region (c) simplified silicon-only domain partitioned into subdomains 1 and 2 and (d) cross-section of the related trench box.

Table 3.4 Geometrical parameter of the trench isolated structure

Parameter	Description	Parameter	Description
W	Trench box width	t_{poly}	Thickness of the trench poly
L	Trench box length	W_{HS}	Heat source width
t_t	Trench box thickness	L_{HS}	Heat source length
d_t	Trench box depth	t_{HS}	Heat source thickness
$t_{ox,t}$	Trench oxide thickness	d_{HS}	Heat source depth

Figure 3.13 illustrates the box structure with deep trenches. In the case of BJT or HBT the heat source is generally at the depletion of base collector junction. The temperature field expressions under steady state condition can be divided into two sections. Section 1 consists of a silicon only rectangular parallelepiped – coinciding with the trench box – with adiabatic top surface, convective boundary conditions at lateral faces, and bottom surface into $R_1 \times R_2$ elementary rectangles, each of them characterized by a uniform outward-going heat flux f_{ij} . By resorting to the *Effects Superposition Principle*

(ESP), the temperature rise above ambient at an arbitrary point $\vec{r} = (x, y, z)$ can be calculated as the sum of two terms

$$\vartheta_1(\vec{r}) = \vartheta_{1,p}(\vec{r}) + \vartheta_{1,f}(\vec{r}) \quad (3.54)$$

$\vartheta_{1,p}(\vec{r})$ represents the power dissipated by the heat source and describes the simplified case of an adiabatic boundary condition at the bottom surface where heat flux is zero. This can be expressed as a double Fourier series

$$\vartheta_{1,p}(\vec{r}) = \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} X_n(x) Y_m(y) Z_{nm,p}(z) \quad (3.55)$$

where $X_n(x)$, $Y_m(y)$, and $Z_{nm,p}(z)$ are eigenfunctions[27] which depends on the heat transfer coefficient h . The heat transfer coefficient is a function of d_t , t_t and k_{fill} . k_{fill} represents thermal conductivity of the deep trench with polysilicon inside with silicon dioxide conductivity k_{ox} and polysilicon conductivity k_{poly} .

$$k_{fill} = t_t \cdot \left(\frac{2 \cdot t_{ox,t}}{k_{ox}} + \frac{t_{poly}}{k_{poly}} \right)^{-1} \quad (3.56)$$

The term $\vartheta_{1,f}(\vec{r})$ is negative in equation (3.54) represents the term that allows taking into account the nonuniform outward-going flux through the partitioned bottom interface. Such a term is in turn evaluated by ESP as the sum of sub-terms, each obtained by enabling one of the fluxes and keeping the others equal to zero (i.e., by considering all the elementary rectangles adiabatic except for one), and is given by

$$\vartheta_{1,f}(\vec{r}) = \sum_{i=1}^{R_1} \sum_{j=1}^{R_2} \left[\sum_{n=0}^{\infty} \sum_{m=0}^{\infty} X_n(x) Y_m(y) Z_{nm,fiy}(z) \right] \quad (3.57)$$

where the eigenfunctions $Z_{nm,fiy}(z)$ are linearly dependent on the unknown fluxes f_{ij} .

The second section represented as a laterally infinite domain with isothermal bottom surface at ambient temperature and top surface adiabatic everywhere except for the interface with section 1, where a nonuniform inward-going flux is assumed. The temperature increase, denoted as $\vartheta_2(\vec{r})$, can be evaluated using ESP by summing the elementary contributions due to the heat fluxes f_{ij} as

$$\vartheta_2(\vec{r}) = \sum_{i=1}^{R_1} \sum_{j=1}^{R_2} \vartheta_{2,fiy}(\vec{r}) \quad (3.58)$$

The terms $\vartheta_{2,fij}(\vec{r})$ are linearly dependent on the unknown fluxes f_{ij} [24]. The adiabatic condition at the top surface (except for the elementary rectangle R_{ij} , where a non-zero uniform inward-going flux f_{ij} is present) and the isothermal condition at the bottom face are satisfied by resorting to the image method. No boundary conditions are accounted for at the lateral sidewalls. Since the domain is assumed embedded in a silicon wafer, their impact on the temperature distribution can be safely neglected.

The image method for evaluating the temperature field in section 2 is preferred over the Fourier series expansion technique, since the latter requires a noticeable number of terms to achieve a prescribed accuracy for structures with large chip-to source size. Lastly, the temperature continuity is imposed at the centers of all the elementary rectangles R_{ij} ,

$$\vartheta_1(x_i, y_j, d_t) = \vartheta_2(x_i, y_j, d_t) \quad (3.59)$$

Solving the resulting linear system of $R_1 \times R_2$ equations allows determining the fluxes f_{ij} , so that the temperature field can be evaluated in both sections. After having calculated the temperature distribution in section 1, the self heating thermal resistance R_{TH} is calculated. R_{TH} is calculated as the average of the temperature rise above ambient normalized to the dissipated power over the heat source projection on the top surface.

$$R_{TH} = \frac{1}{P_D \cdot W_{HS} \cdot L_{HS}} \cdot \int_{x_1}^{x_2} \int_{y_1}^{y_2} \vartheta_1(x, y, 0) dy dx \quad (3.60)$$

3.3.4 Masana's Method Of Thermal Impedance Estimation [17]

This section describes the thermal impedance calculation proposed by Masana. The time dependent equation of conduction of heat in an isotropic medium is given by

$$\nabla^2 T = \frac{1}{\alpha_p} \cdot \frac{\partial T}{\partial t} \quad (3.61)$$

where T is the temperature, α_p is the thermal diffusivity at constant pressure and ∇^2 is the Laplacian operator. The thermal resistance is defined as a lumped model obtained by the integrating over the distributed volume with certain boundaries. Figure 3.14 shows a block with constant cross-section, S with

constant temperature and heat flux q across it, zero heat flux flowing out of the vertical walls. Equation (3.61) is integrated in one-dimension, and the constant of integration is obtained by applying the boundary conditions. Equation (3.61) can be modified to

$$\frac{dT}{dx} = -\frac{q}{k} \quad (3.62)$$

where k is the thermal conductivity of the medium. The rate of heat input to the volume is $W=qS$ watts. Integrating results to

$$\frac{T_0-T_l}{W} = \frac{l}{kS} = R_{TH} \quad (3.63)$$

where T_0 and T_l are the temperatures at $x=0$ and $x=l$ respectively. Thus the thermal resistance between any two isothermal surfaces can be obtained, by solving equation (3.61) by applying boundary conditions and dividing the temperature difference by the rate of heat flow between the surfaces. The thermal resistance can be calculated by integration along a path of length l with a cross-section S . The relevant characteristic of the medium filling the volume is the thermal conductivity k . Thermal capacity is a magnitude associated with heat storage and accordingly the integration has to be performed for the volume $V=lS$, with the heat capacity c_p is the relevant characteristic of the medium filling that volume. The thermal capacitance is then equal to

$$C_{TH} = V \cdot \rho \cdot c_p \quad (3.64)$$

where ρ is the density of the medium with units kg/m^3 , V is the volume in m^3 , and c_p is the specific heat with units $\text{J}/\text{kg}\cdot\text{K}$.

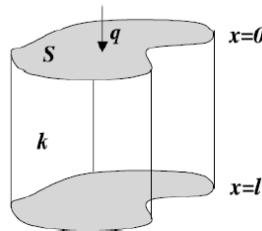


Figure 3.14 Block of material for thermal impedance calculation[17].

Masana proposed a variable angle method (VAM) [28] which is used to calculate the thermal resistance of the volume in Figure 3.15. The heat source, its projection on the next layer boundary and the edges defined by the spreading angles $\alpha_1, \alpha_2, \beta_1$ and β_2 delimit this volume as shown in Figure 3.15. These angles are associated with the source dimensions x and y respectively. In the general case, the spreading is different for each side of the heat source according to its placement with respect to the substrate.

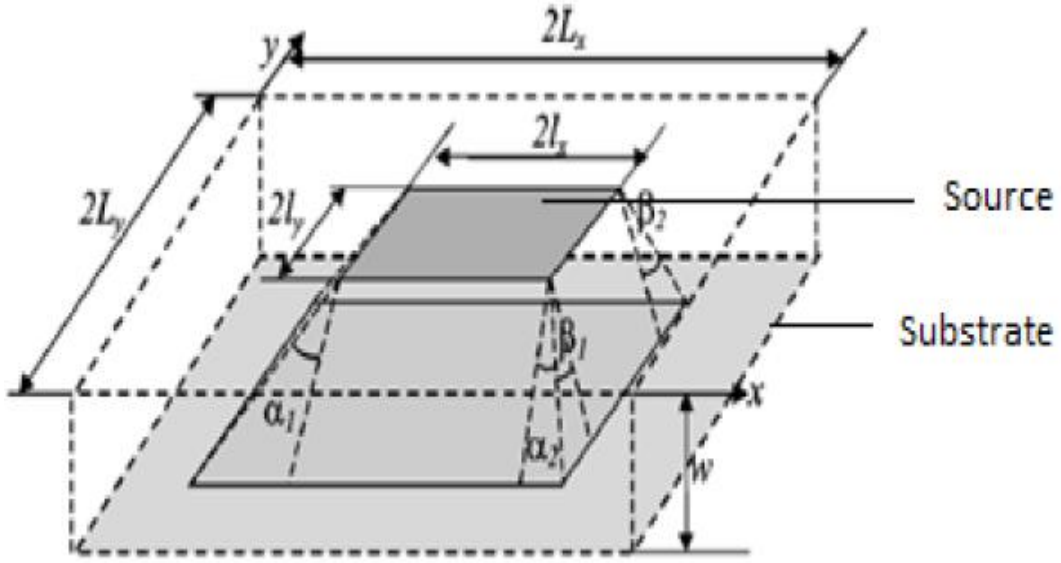


Figure 3.15 Thermal spread model from Masana [17]

Using the angel representation R_{TH} can be calculated and be represented by

$$R_{TH} = \frac{1}{k} \cdot \frac{1}{\gamma_e \tan \alpha - \tan \beta} \cdot \ln \frac{l_x + w \tan \alpha}{l_x + w \tan \beta / \gamma_e} \quad (3.65)$$

where $\gamma_e = l_y / l_x$ and $\gamma_s = L_y / L_x$ are the aspect ratios of the heating element and substrate respectively. The spreading angles are given by

$$(\tan \alpha)_i = \frac{(\tan \alpha_1 + \tan \alpha_2)_i}{2} = \left(1 + \frac{1 - \rho_L}{1 + \rho_L} \cdot \frac{l_{xn}}{\varepsilon_x^2} \right) \cdot \frac{w_n + \left[\frac{\rho_S}{1 + \rho_S} \right] \cdot l_{xn}}{w_n + \left[\frac{1}{1 + \rho_S} \right] \cdot l_{xn}} \Bigg|_i \quad (3.66)$$

$$(\tan \beta)_i = \frac{(\tan \beta_1 + \tan \beta_2)_i}{2} = \left(1 + \frac{1 - \rho_L}{1 + \rho_L} \cdot \frac{l_{xn}}{\varepsilon_y^2} \cdot \frac{\gamma_e}{\gamma_s} \right) \cdot \frac{w_n + \left[\frac{\rho_S}{1 + \rho_S} \right] \cdot l_{xn} \cdot \gamma_e}{w_n + \left[\frac{1}{1 + \rho_S} \right] \cdot l_{xn} \cdot \gamma_e} \Bigg|_i \quad (3.67)$$

where $i = 1, 2$; $l_{xn} = l_x/L_x$, $w_n = w/L_x$ are the normalized dimensions. ϵ_x and ϵ_y are the eccentricity parameters given by $\epsilon_x = \frac{\sqrt{L_{x1} \cdot L_{x2}}}{L_x}$; $\epsilon_y = \frac{\sqrt{L_{y1} \cdot L_{y2}}}{L_y}$. The boundary dependence comes through ρ_S and ρ_L .

$$\rho_S = \frac{k_i}{k_{i+1}}; \rho_L = \frac{k_i}{k_L} \quad (3.68)$$

where k_i and k_{i+1} are the thermal conductivities of the present and next layer respectively, and k_L is the thermal conductivity of side walls.

The thermal capacitance calculation is not straight forward because it is difficult to associate a given volume to the heat flow path due to the distributed nature of the problem.

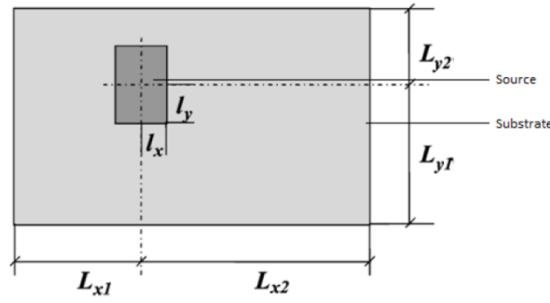


Figure 3.16 Source to substrate offset[28]

The heat flow is confined to this volume and hence their limiting walls are assumed to be adiabatic. Consequently, the same volume considered for the calculation of thermal resistance can also be used for the calculation of thermal capacitance. The volume is given by

$$V = 4 \int_0^w (l_x + z \tan \alpha) \cdot (l_y + z \tan \beta) dz \quad (3.69)$$

Inserting equation 3.69 into 3.63 gives C_{TH} .

3.4 Summary

In an HBT, there are three main regions 1) the tub 2) the bottom oxide and 3) the wafer. Using the methods described above the thermal impedance of each layer can be calculated. The tub consists of deep and shallow trenches in case of BJT and HBT therefore Ranildi estimation with isolation trench is preferred. Masana method also can be used in case of tub. The bottom oxide is very thin and have high resistivity therefore Joy and Schlig's gives a good estimation. For the wafer calculation shows Joy and

Schilig, Masana and Ranaldi methods without trench isolation all give similar results. In Chapter 4, these mathematical calculations are compared to TCAD simulation result.

CHAPTER 4

THERMAL CHARACTERIZATION OF HBT

4.1 Self-Heating Of HBT

This section looks into self heating of a Heterojunction Bipolar junction Transistor (HBT). An HBT has a very compact structure which is because of the presence of isolation oxide surrounding the device, heat gets trapped within the device, which can result to change in the device behavior. This means that is a SOI (Silicon On Insulator) substrate concurrently with lateral trenches, so that the silicon structure becomes an island totally surrounded by insulating materials. Figure 4.1 illustrates an HBT with heat source, H. Because of the presence of the deep trench (DT) and the shallow trench (STI), the overall heat flow changes. It is important to incorporate these variables for the thermal impedance network and calculation.

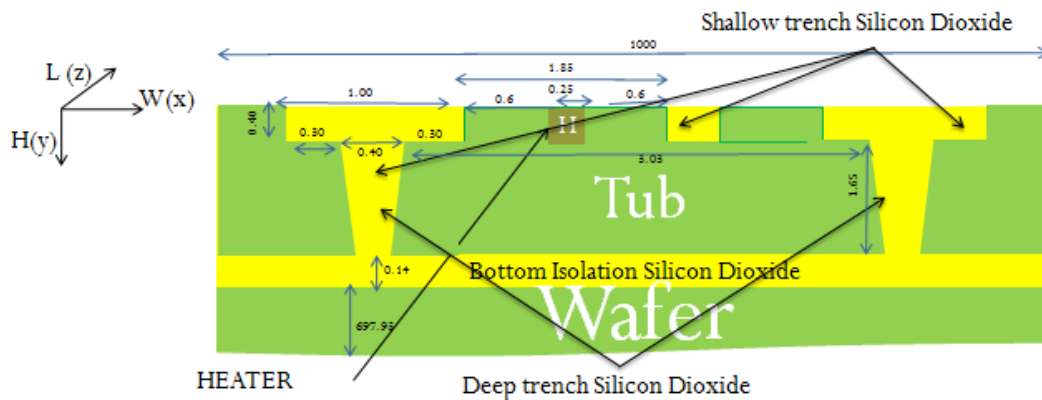


Figure 4.1 An HBT structure (not scaled) [1]

Self-heating is caused by power dissipation in the depletion region between the lightly doped collector and the base region of the device which results in an increase in junction temperature of the device. This is because the electric field is maximum in the region of lightly doped collector and heavy doped collector. Self-heating of a transistor can be characterized by its thermal resistance and thermal

capacitance. Self-heating can be modeled conceptually as illustrated in Figure 4.2. A thermal network is included with the electrical model of the device. The thermal network is driven by the power dissipated within the device. The dissipated power is calculated by adding the individual powers of the non-storage branches of the electrical network.

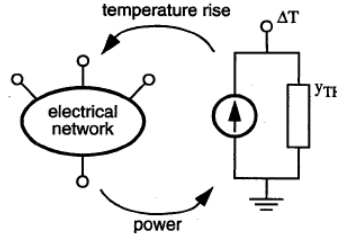


Figure 4.2 Self heating model [29]

The rise in temperature, ΔT , from the thermal network is coupled back to the constitutive elements of the electrical network. In an HBT, heat dissipation occurs mainly in the lightly doped collector-base depletion region that carries the bulk of the injected current. Carriers attain high velocities and give up their energy to the lattice through phonon interactions. The Self-heating effect is included in the High Current Model (HICUM) model for the HBT. At high frequencies, the device thermal response cannot track the electrical variations, so that at high frequency the output conductance $1/r_o$ is equal to the intrinsic electrical value. At low frequencies, the device temperature varies with the electrical variations of the applied signal and the output conductance is different from the intrinsic electrical value. The thermal admittance, Y_{TH} , can be characterized by observing the difference between the measured output conductance and the calculated intrinsic electrical conductance. The small signal admittance parameters including the effects of self-heating are given by [29]

$$y_{11}(j\omega) = g_{\pi} + \frac{g_{bt}(I_b + g_{\pi} \cdot V_b + g_m \cdot V_c)}{y_{TH} - (g_{ct} \cdot V_c + g_{bt} \cdot V_b)} + j\omega(C_{be} + C_{bc}) \quad (4.1)$$

$$y_{12}(j\omega) = \frac{g_{bt}(I_c + g_o \cdot V_c)}{y_{TH} - (g_{ct} \cdot V_c + g_{bt} \cdot V_b)} - j\omega C_{bc} \quad (4.2)$$

$$y_{21}(j\omega) = g_m + \frac{g_{ct}(I_b + g_{\pi} \cdot V_b + g_m \cdot V_c)}{y_{TH} - (g_{ct} \cdot V_c + g_{bt} \cdot V_b)} - j\omega C_{bc} \quad (4.3)$$

$$y_{22}(j\omega) = g_0 + \frac{g_{bt}(I_c + g_c \cdot V_c)}{y_{TH} - (g_{ct} \cdot V_c + g_{bt} \cdot V_b)} + j\omega(C_{cs} + C_{bc}) \quad (4.4)$$

where $g_\pi = \partial I_b / \partial V_b$ is the intrinsic electrical input conductance, $g_o = \partial I_c / \partial V_c$ is the intrinsic electrical output conductance, $g_m = \partial I_c / \partial V_b - g_o$ is the intrinsic electrical trans-conductance, $g_{bt} = \partial I_b / \partial \Delta T$ and $g_{ct} = \partial I_c / \partial \Delta T$ are the thermal trans-conductance [29].

4.2 Thermal Modeling Of HBT

Thermal modeling of an HBT is represented in Figure 4.3. The dissipated power in the thermal network of an HBT can be represented as

$$P_{Total} = I_C \cdot V_{CE} + I_B \cdot V_{BE} \quad (4.5)$$

where I_C is the collector current, V_{CE} is the collector-emitter voltage, I_B is the base current, and V_{BE} is the base-emitter voltage. The local temperature rise, ΔT , from the thermal network is coupled back to the HBT. A series combination of one or more Z_{TH} blocks which consists of one thermal resistance, R_{TH} , and one thermal capacitance, C_{TH} , is normally used as the thermal network. This implies that the response from a step change, $\Delta T(t)$, is the sum of one or more exponential terms with different weights and time constants.

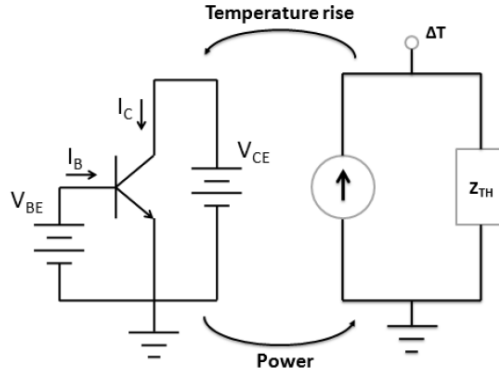


Figure 4.3 Compact thermal model [30]

The most common thermal network (Figure 4.4) is a single parallel combination of a thermal resistance and a thermal capacitance. However, representation of a thermal resistance and a thermal

capacitance as an electrical resistance and an electrical capacitance is not directly applicable, since the temperature is not constant over the substrate.

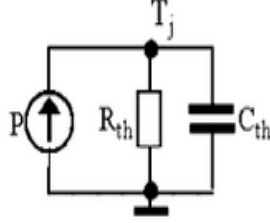


Figure 4.4 Thermal network in HICUM model[8]

4.3 Self Heating In HICUM MODEL

In a HICUM model the thermal effects are modeled by implementing an additional thermal network as shown in Figure 4.4. The thermal network models the interaction between electrical characteristics and the thermal effects. The above thermal sub-circuit with $I_{TH} = P \cdot I \text{ A/W}$ and $Z_{TH} = Z_{TH} \cdot I \text{ Ohm W/K}$ couples the instantaneous power dissipation in the device to the thermal network. Therefore from the equation $\Delta T = R_{TH} \cdot P$, the voltage level of the temperature node dt is numerically equal to the local temperature rise K , which is used to calculate the instantaneous electrical characteristics of the transistor.

$$P = V_{CE} \cdot I_C + V_{BE} \cdot I_B$$

$$I_{th} = \frac{P}{1[V]}$$

$$Z_{th} = \frac{\partial T_j}{\partial P} = R_{th} \cdot \left(1 - e^{-\frac{t}{\tau_{th}}}\right)$$

$$\tau_{th} = R_{th} \cdot C_{th} \quad (4.6)$$

4.4 Proposed Compact Thermal Model For HBT

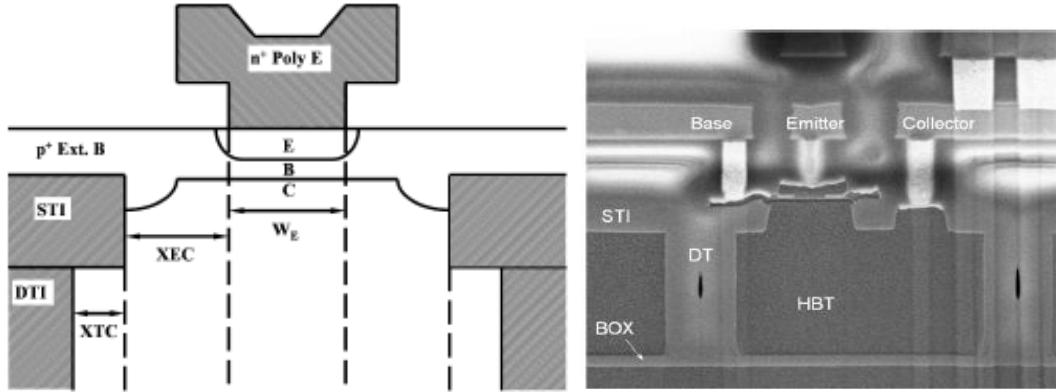


Figure 4.5 (a) Conceptual structure[31] (b) Fabricated cross section diagram of HBT from TI-Silicon Labs[2].

For the HBT represented in Figure 4.5, a thermal compact model is proposed which is represented in Figure 4.6. This model was developed in [12] which represents the possible heat flow paths

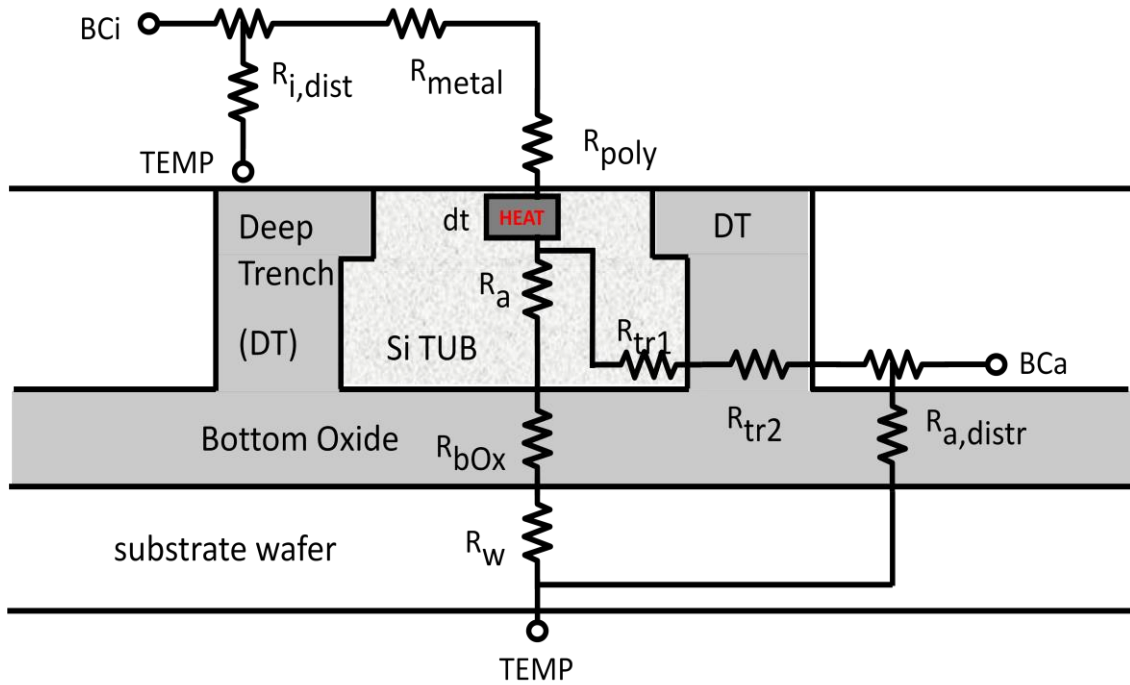


Figure 4.6 Thermal element compact model for HBT. [12]

The thermal element model for the HBT in Figure 4.6 is proposed based on the 3-D Davinci simulations for the actual device structures from Figure 4.5 and mathematical analysis. The power is dissipated at the lightly doped collector to base depletion region as indicated as HEAT in Figure 4.6. Heat can flow through the silicon TUB downwards to the bottom silicon dioxide. This heat flow can be approximated by a spreading resistance model from the heat source to the bottom of the TUB indicated as R_a in Figure 4.6. Heat also flows from the heat source to the inside of the side walls of DT which is modeled by R_{tr1} . There are four side walls in the TUB therefore R_{tr1} can be considered as four parallel combinations of the heat path from the source to the inside side wall of the DT. The interface between the Si tub, the bottom isolation and trench oxide is assumed to be at a uniform temperature. R_{bOx} represents the heat flow from the bottom of the TUB to bottom of the bottom oxide (or the top of the wafer). R_{tr2} models the heat flow through the DTs. The interface temperature between the Si TUB and the isolation oxide depends on the distance between the heat source and a given point. A distributive network can be formed which represents heat path from adjacent heat device and is represented as $R_{a,distr}$. BCa represents adjacent devices. $TEMP$ in the Figure 4.6 represents the ambient temperature. R_{poly} is the heat path model for the poly-silicon of the emitter. R_{metal} represents the thermal heat path because of the via connections to metal connection of the bond wires. The metal connection and the bond wires can be considered as $R_{i,dist}$ which is a distributive network because of metal lines connected to the devices emitter, base and junction. BCi represents internal connection to other devices.

4.5. Heat Source Estimation and Simulation

4.5.1 Heat Source Simulation

Davinci can calculate the lattice temperature using the heat equation. A Davinci module called the Lattice Temperature Advanced Application Module (LT-AAM) can be used to perform non-isothermal electrical analysis by simultaneously solving the electrical and thermal equations. The current flow and recombination of carriers increases the lattice temperature in a device.

The heat is produced in the depletion region of the lightly doped collector to base region. It is important to located the position of the depletion region and its dimension, so that the three dimensional

HEAT source structure can be converted to a planar source for mathematical modeling. In order to verify the accuracy of the Medici simulation structure, the Medici circuit simulation is used to simulate gummel plot which is compared to measurement. The Medici simulation assumes 1 micro meter thickness in the z domain, therefore Medici simulation for gummel would correspond to the 1um device measurement. The comparison of the 1um device measurement to the Medici simulation is being presented in Figure 4.7, which reflects the Medici simulation's accuracy to real device measurement.

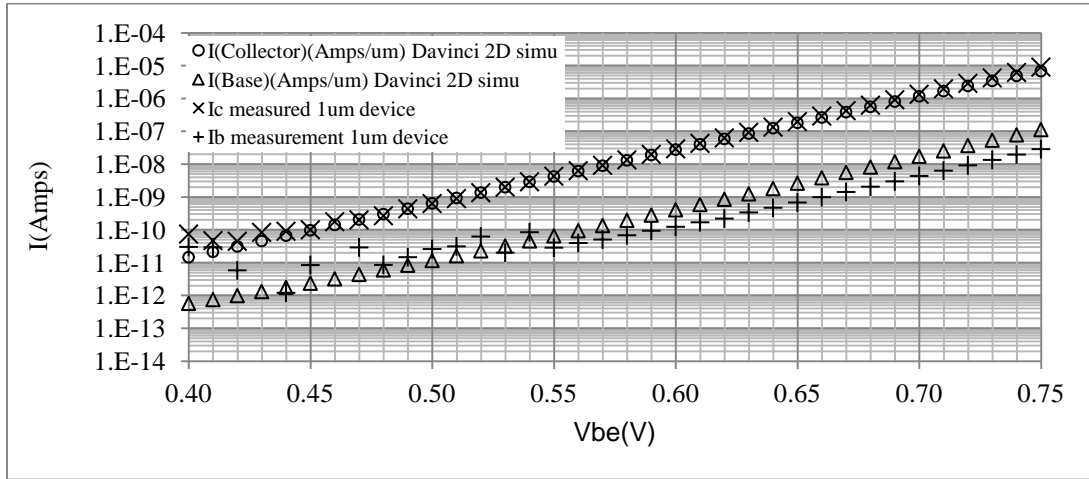


Figure 4.7 Gummel simulation of Medici 2D simulation compared to 1um device measurement.

Then the isotherm simulation of the two dimensional Medici simulation is performed [31]. The location of the hottest point is determined from the isothermal line shown in Figure 4.8. The temperatures along the isothermal lines were extracted from the MEDICI simulation which ranged from 301.255K to 300 in the case where $V_{be}=0.85V$ and $V_{ce}=1.73V$. From Figure 4.8 it is seen that the hottest temperature is 301.255K at the lightly doped collector to the heavy doped collector junction, the bottom of the TUB is 301.052K, the bottom of the oxide is 300.548K. Therefore most heat is trapped because of the presence of bottom oxide. Since the structure is not symmetric, therefore the inside sidewall between are not equal as shown with the right inside sidewall at 301.143K and the left inside sidewall is at 300.875K. Outside the deep trenches (DT) the temperature varies from 300.497K to 300.527K.

Figure 4.8 not only provides the location of the hottest point, but also provides the temperature at the emitter base junction, this is important because current equations are based on the emitter base junction temperature. From measurement it is possible to measure emitter base junction temperature. The true temperature of a device can be evaluated from comparing the junction temperature of the Medici simulation to measurement and then finding the hottest temperature of the device from the simulation that corresponds to that junction temperature. Figure 4.9 shows the temperature profile at each junction.

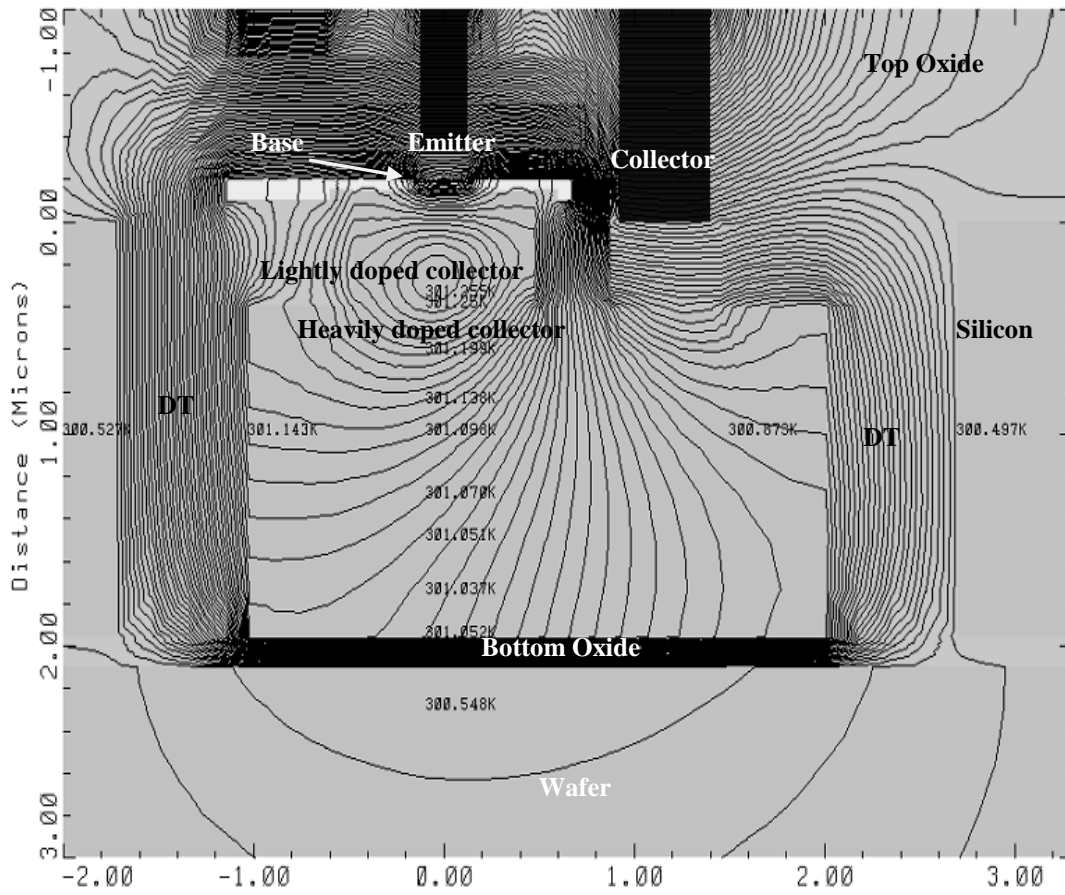


Figure 4.8 Temperature profile for 2-D Medici simulation

The temperature in the simulation is varied by keeping base-emitter voltage (V_{be}) constant at 0.85V and varying the collector-emitter voltage (V_{ce}). The temperature along the Y axis is being recorded with the x-axis at 0.0625um. The bottom of the lightly doped collector to heavy doped collector located at

0.36 μm , bottom of intrinsic base at $-0.15\mu\text{m}$, top of the intrinsic base is at $-0.20\mu\text{m}$, as seen in Figure 4.9. It shown how the temperature varies at hottest point, at the intrinsic base bottom (InBase BOTTOM), intrinsic base top (InBase TOP) and emitter top verse V_{ce} , while V_{be} being constant at 0.85V . It is possible to evaluate the thermal resistance of this two dimensional structure.

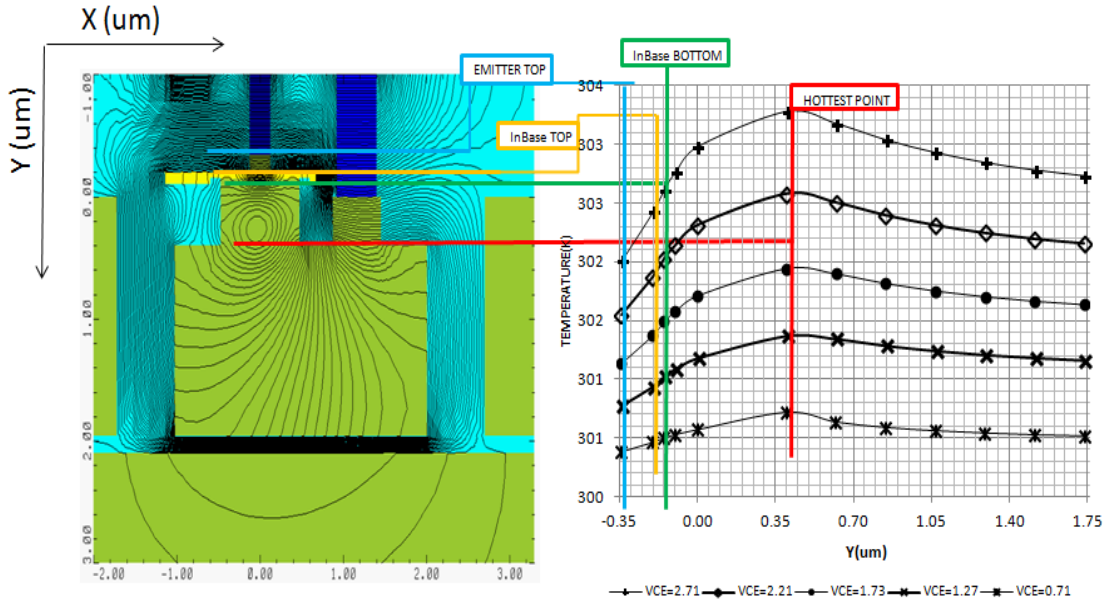


Figure 4.9 Temperature profile at each junctions

4.5.2 Estimation Of R_{th}

The following steps are undertaken to calculate the thermal impedance:

Estimation of R_{th} from a 2D simulation from the Medici simulation

- The isothermal characteristics are being extracted first.
- The heat flow equation is being turned off in the Medici simulation. The increase in lattice temperature in a device due to current flow and recombination of carriers is included self-consistently in the solution of the device equations. Medici solves the lattice heat equation in addition to Poisson's equation and the electron and hole current-continuity equations. The default solves the heat equation in a decoupled manner from the other device equations.

- Keep the device at a constant temp and extract output characteristics of the device (Ic vs Vce). This means that the ambient temperature is varied. Also the thermal conductive of the materials are being set to a constant for all the material and therefore is not the temperature dependent. This is done by putting all the temperature dependent coefficient to zero as in (4.7). It means each mesh point in the simulation should be at constant temperature.

$$\lambda = \frac{1}{(A.TH.CON+B.TH.CON \cdot T+C.TH.CON \cdot T^2+D.TH.CON \cdot T-E.TH.CON)} \quad (4.7)$$

- Repeat the isothermal characteristics for several temperatures and obtain the output characteristics.
- Turn on the heat flow equations, keep the ambient temperature of device at 300K and repeat output characteristics of the device (Ic vs Vce). This can be done by using the LAT.TEMP application module. Appendix C provides the code of such a simulation.
- Intersection of curves between no heat flow equation and with heat flow equation would provides the power for that given temperature. This means for a given voltage and current, the temperature at the emitter base junction can be evaluated. Calculate R_{th} as the ratio of temperature rise to total power.

$$\text{Temperature Rise} = \Delta T = R_{th0} \cdot \text{Power} \quad (4.8)$$

$$\text{Power} = I_c \cdot V_{ce} + I_b \cdot V_{be} \quad (4.9)$$

I_b can be estimated from I_c since the forward beta for the device is around 100. Therefore all the intersection points between x and y, in the Figure 4.10 provide the power and the temperature the device is actually experiencing. The change in temperature to change in power provides the thermal resistance at ambient conditions.

$$R_{th0} = \frac{\partial T}{\partial P} \quad 4.10$$

where, T is the temperature at the junction of the emitter – base, P is the power dissipated in the device.

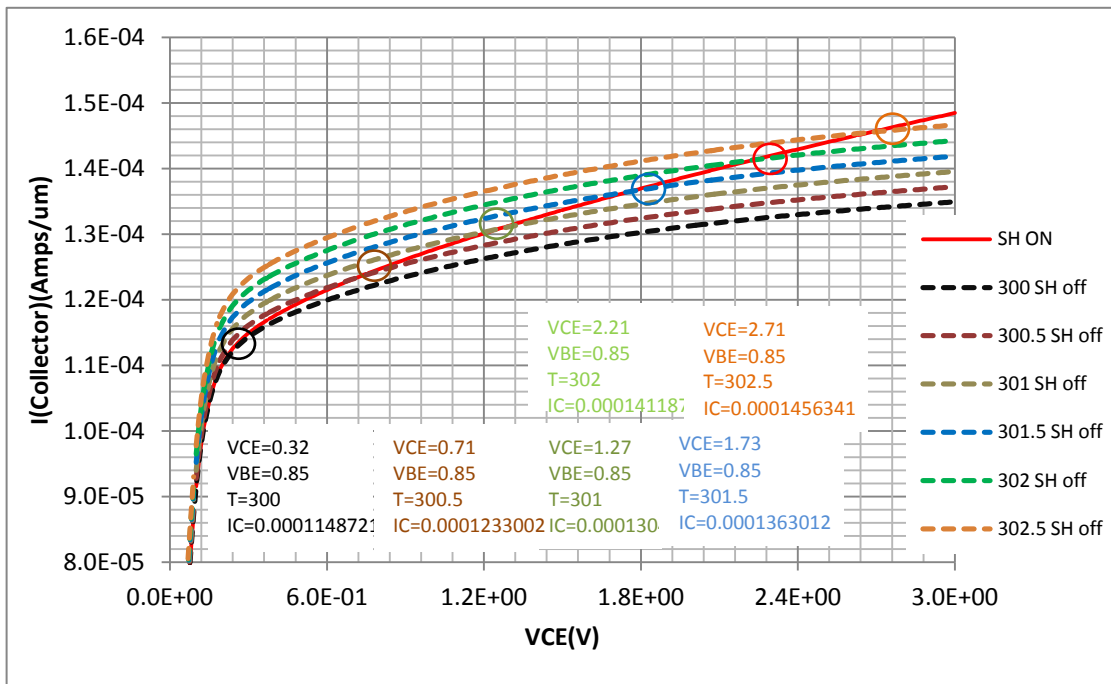


Figure 4.10 Calculation of R_{th0}

- From the 2D SH (SELF HEATING) on simulation, the location and the temperature of the hottest point is determined. Record the temperature at the junction of the intrinsic base to light doped collector and the intrinsic base to the emitter polysilicon. This is shown in Figure 4.10.

From the Figure 4.10 Power vs temperature can be plotted as shown in Figure 4.11.

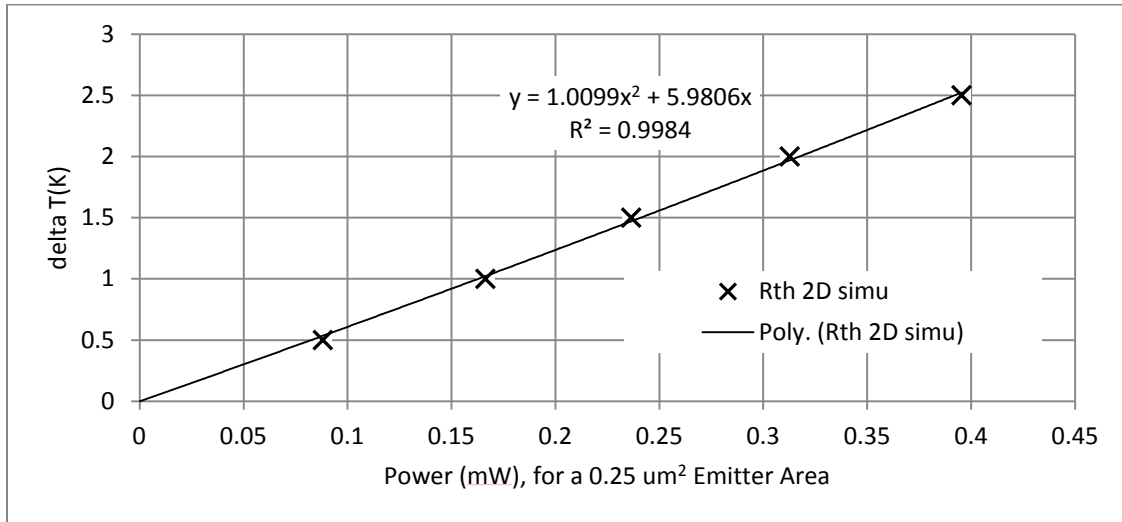


Figure 4.11 Calculation of R_{th}

The total R_{th} is

$$R_{th} = \frac{\partial T}{\partial P} + \frac{\partial T^2}{\partial P^2} \cdot P = R_{th0} + \frac{\partial R}{\partial P} \cdot P \quad (4.11)$$

4.5.3 Estimation Of Effective Heater Size

In this section, the estimation of the effective size of the heat source is discussed. Instead of using an electrical heat source as in the previous section 4.5.2, thermal electrons are used for the estimation of R_{th} . The physical structure and its properties used for the heat source is explained in APPENDIX A. By using a thermal electrode heat source, thermal capacitance can be evaluated which cannot be done using an electrical heat source. The 2D Medici simulation is being repeated using the thermal electrode structure. This is shown in Figure 4.12.

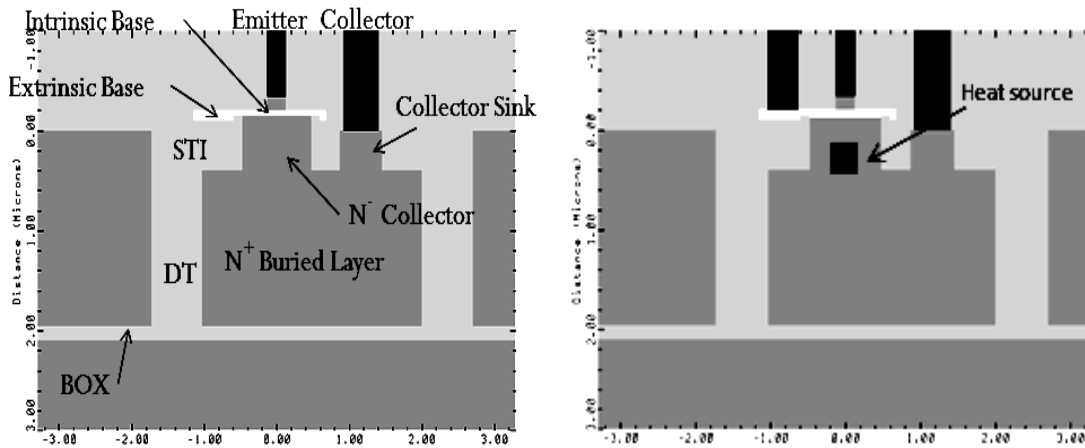


Figure 4.12 Medici 2D simulation using thermal electrode heat source.

From the simulation result in Figure 4.9, the heat source temperature is set to the hottest temperature obtained from previous 2D simulation. Figure 4.9 also shows the temperature at the junction of the intrinsic base to the light doped collector (T_{jlbLc}) and the intrinsic base to the emitter poly-silicon (T_{jibE}). Since the width and the length of the depletion region of a lightly doped collector to base is assumed to be the same width (x um) and length (z um) as the emitter, the only variable is the height of the depletion region (y um). The next step is to determine the height of the depletion region. This is done by varying the height of the heat source until the temperature of T_{jlbLc} and T_{jibE} are the same when the electrical heat source is being used in the simulation. This provides the height of the depletion region. Using this area for the depletion region, perform 3D simulation is performed to determine R_{th} . This procedure is followed in all the device to determine R_{th} .

4.5.4 Modeling Of The Heat Source

In order to model the heat flow with the devices, it is essential to have a planar heat source. All the heat flow models described in chapter 3 use a planar heat source. Therefore the 3 dimensional heat source is converted to a 2 dimension planar heat source. This is done by assuming a spreading angle for the heater as shown in Figure 4.13. This heater spreading angle can be considered for length side as well as width side. The estimation of the angle is described later on this chapter. The bottom of the heater can be considered the new 2 dimensional heat source which is planar in structure.

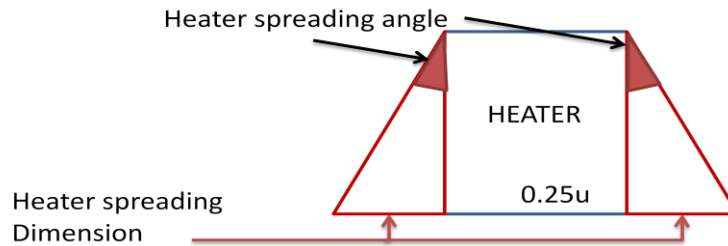


Figure 4.13 Conversion of 3D dimensional heat source to a planar structure.

4.6 R_{th} Determination Using Tapered Structure

4.6.1 Davinci Simulation

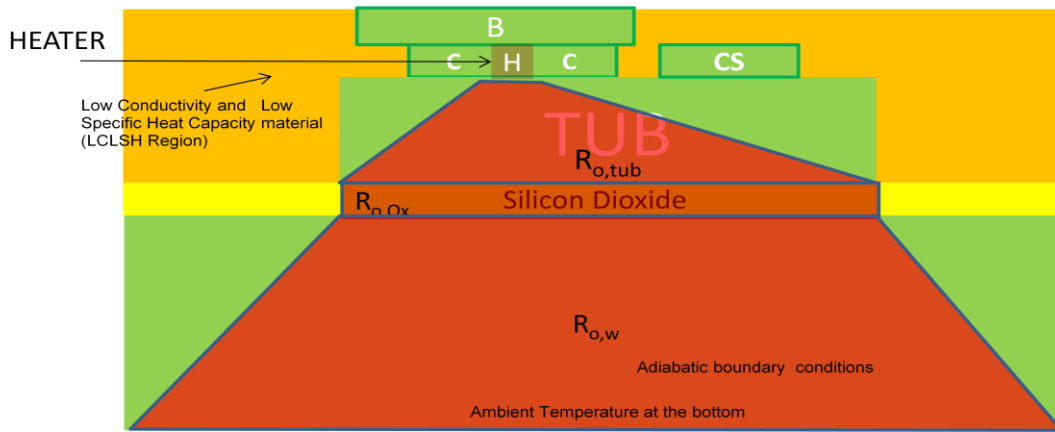


Figure 4.14 3D simulation for device with ambient temperature at the bottom.

In this section of the study, 3D simulation was done forcing the path of the heat flow only through the bottom of the wafer. The spreading resistance in the tub, oxide and wafer can be modeling using this structure in Figure 4.14 with the application of thermal electrode heat source. The 3 dimensional heat source obtained from the previous structure determined from Section 4.5.4, all the devices are simulated the dimension provided by Texas instrument-Silicon Labs. From the 3 dimensional simulation obtained, the spreading resistance of the tub, oxide bottom and wafer can are estimated. The spreading resistance of the silicon tub is calculated by modeling the tub into section of small slab. In this calculation it is being assumed that the thermal resistance increase linearly from bottom slab to the top

and the time constant from each slab remains constant. This assumption is derived from the calculation provided by Masana and Rinaldi.[17,23]

4.6.2 Modeling Of Davinci Simulation

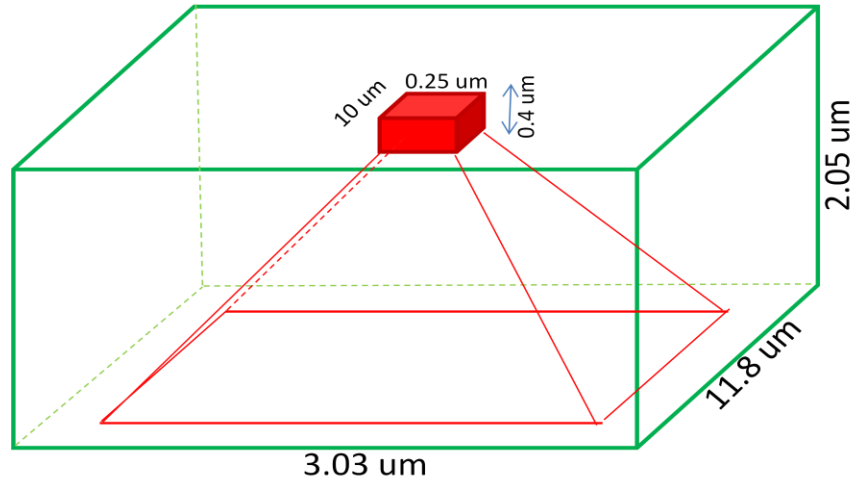


Figure 4.15 Davinci representation of 10 μm device TUB (not scaled)

Three difference approaches have been used to calculate the thermal impedance in the TUB region.

- Constant area ratio
- Constant thermal resistance increase
- Constant increase in length and width

$$R_{th} = \frac{t}{A \cdot kSi} \quad (4.12)$$

The Davinci simulation is then optimized to fit a 35 element Cauer network. A RC Cauer network is a ladder network of R and C where all the capacitance are being reference to ground. The calculation is performed by first calculation the bottom most section of the element by

$$R_{th(\text{bottom of the Tub})} = 10000 \cdot (t/NT) / (kSi \cdot c \cdot \text{Area}_{\text{bottom of the TUB}}) \quad (4.13)$$

NT= total number of elements

Optimized Elements = $c_{(\text{fraction bottom of the area})}$

t = thickness of each section, and

kSi = conductivity of silicon (1.5468K-cm/W)

The thermal resistance of each element is calculated by adding R_p to bottom most thermal resistance.

This is given by :

$$R_{th_i} = R_{th_n} + R_p(NT - N) \quad (4.14)$$

$$C_{th_{n(\text{bottom of the Tub})}} = c \cdot (\text{Area}_{\text{bottom of the TUB}}) \cdot \text{denSi} \cdot C_{pSi} \cdot (t/NT) / 10000^3$$

where N is number of elements in the Cauer network.

After calculation of the bottom most thermal resistance and capacitance, the optimized R_p would give the next area above the bottom most thermal resistance.

$$\text{Area}_i = 10000 \cdot (t/NT) / (kSi \cdot (R_{th_n} + R_p(NT - N))) \quad (4.15)$$

The thermal resistance can be calculated from the area calculation.

$$C_{th_i} = \text{Area}_i \cdot \text{denSi} \cdot C_{pSi} \cdot (t/NT) / 10000^3 \quad (4.16)$$

The next step is to optimized and calculate the Tub bottom area and source area.

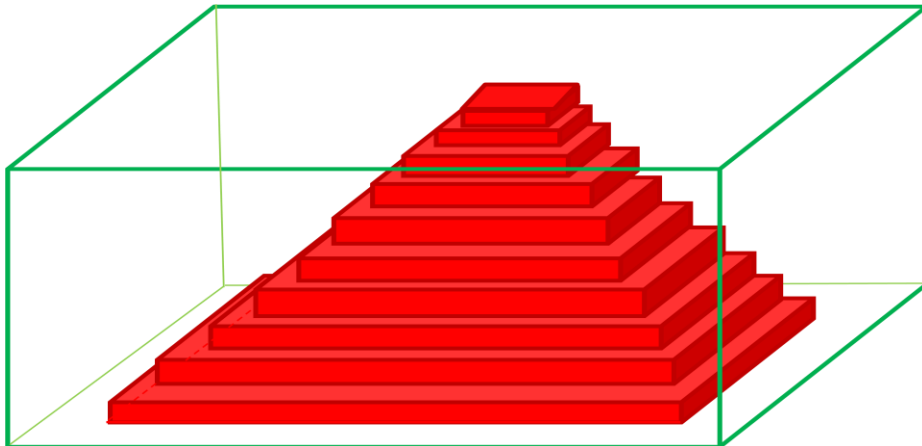


Figure 4.16 The taper representation of Tub heating.

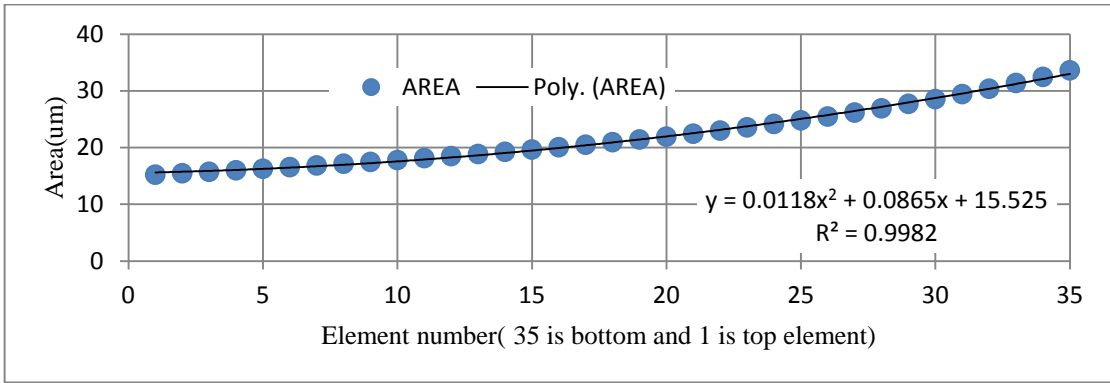


Figure 4.17 Area vs Element number

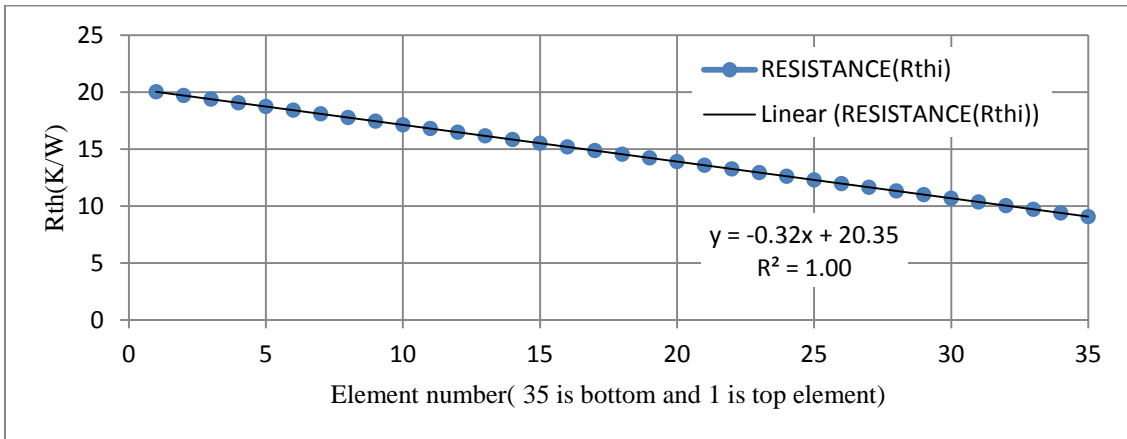


Figure 4.18 Rth vs Element number

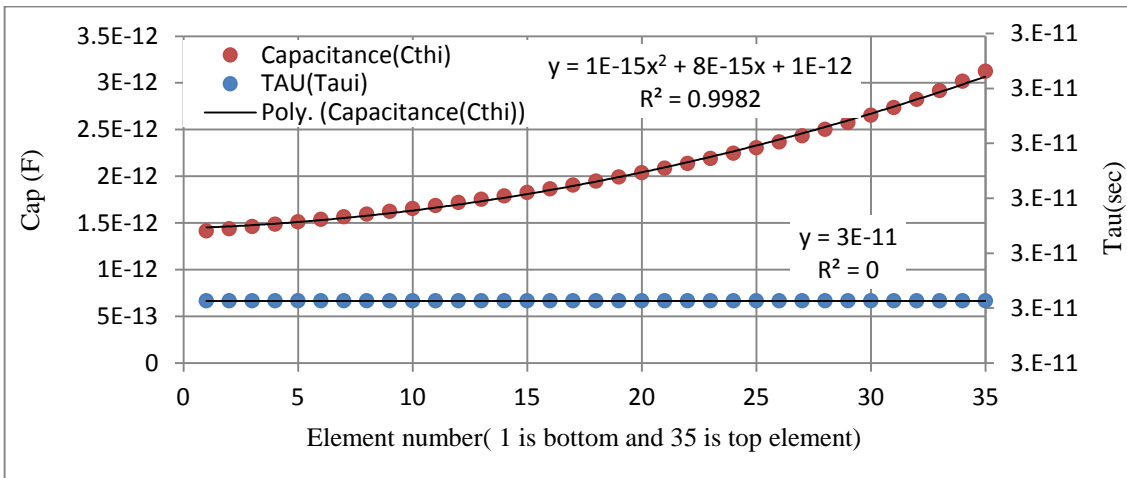


Figure 4.19 Cth and Tau vs element number

After the area of the two dimensional heat source is obtained from the previous calculation, the heater area is compared to the emitter bottom area. The three dimensional heater surface area of the four side walls and the bottom is then transformed a two dimensional area. The angle α is varied until it corresponds to the two dimensional heat area obtained from the 35 element calculation.

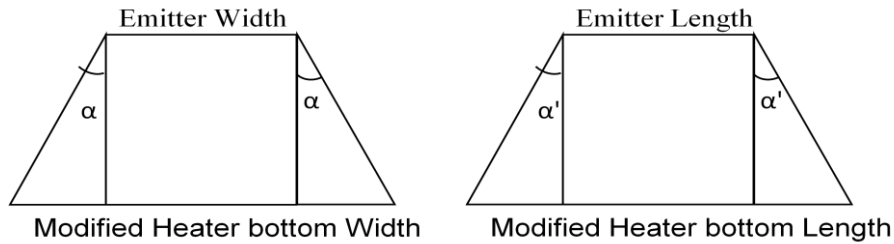


Figure 4.20 Heat source modeling

Heat source area = $(\tan(\alpha) \cdot \text{heater height} \cdot 2 + \text{heater bottom Length}) \cdot (\tan(\alpha) \cdot \text{heater height} \cdot 2 + \text{heater bottom width})$

The value of α is varied till it matches the data from the Davinci simulation. This optimizes α to match with heater area from ICCAP and excel.

If $L_{\text{bottom heater}} > L_{\text{bottom of Tub}}$

Then $L_{\text{bottom heater}} = L_{\text{bottom of Tub}}$

Or $L'_{\text{bottom heater}} = \tan(\alpha) \cdot \text{heater height} \cdot 2 + \text{heater bottom length}$

$W'_{\text{bottom heater}} = (\tan(\alpha) \cdot \text{heater height} \cdot 2 + \text{heater bottom width})$

Optimize α to match with heater area from ICCAP and excel.

After the calculation of the 2 dimensional heater, the spreading angle is calculated.

If $L'_{\text{bottom Tub}} > L_{\text{bottom of Tub}}$

Then $L'_{\text{bottom Tub}} = L_{\text{bottom of Tub}}$

Or $L'_{\text{bottom Tub}} = \tan(\Phi) \cdot \text{Tub height} \cdot 2 + L'_{\text{bottom heater}}$

$W'_{\text{bottom Tub}} = (\tan(\Phi) \cdot \text{Tub height} \cdot 2 + W'_{\text{bottom heater}})$

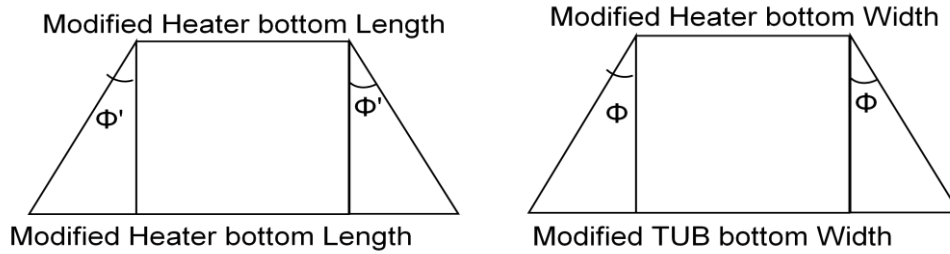


Figure 4.21 Tub modeling

Φ and Φ' can be obtained by optimization to match with bottom area from ICCAP and excel. Example of such an optimization is shown in Figure 4.22.

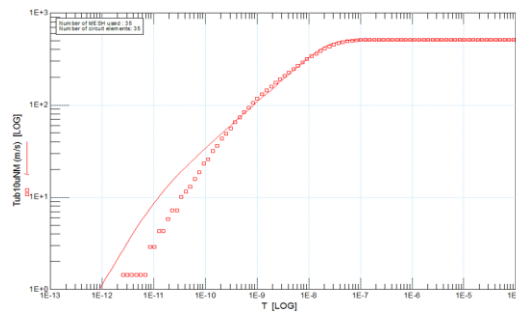


Figure 4.22 Optimization of angle to fit the Davinci model.

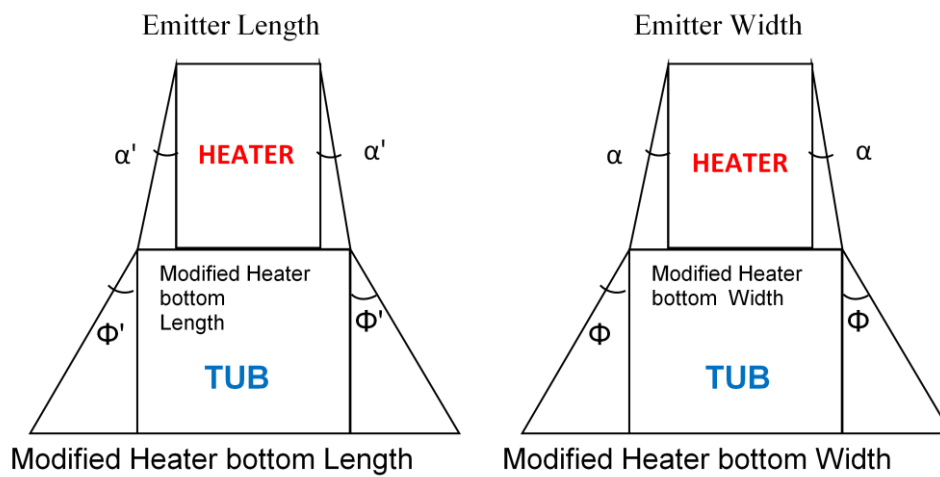


Figure 4.23 The angle spreading from the heat source and in the TUB.

4.6.3 Spreading Resistance Mathematical Representation.

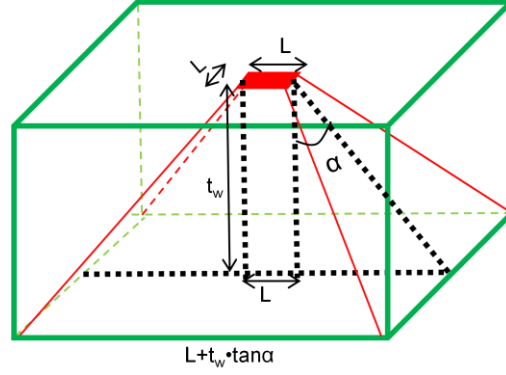


Figure 4.24 Mathematical representations for Tub

The spreading resistance can be modeled as a tapped structure. It is possible to mathematically model the tapped thermal resistance as shown in Figure 4.23. The thermal resistance of a small section with thickness dt is given by

$$R_{th} = \frac{dt}{k \cdot A(t)} \quad (4.17)$$

where k is the thermal conductivity of the solid and $A(t)$ is the cross-sectional area at a depth of t from the top. If the width and the length are made equal then

$$R_{th} = \frac{dt}{k \cdot A(t)} = \frac{dt}{k \cdot L'(t)^2} = \frac{dt}{k \cdot (L + 2 \cdot t_w \cdot \tan \alpha)^2} \quad (4.18)$$

where $L'(t) = k \cdot (L + 2 \cdot t_w \cdot \tan \alpha)$, t_w is the height as shown in the Figure 4.24

Integrating (4.12) produces the tapped thermal resistance. For $t_w \gg L$

$$R_{th} = \int_0^{t_w} \frac{dt}{k \cdot (L + 2 \cdot t_w \cdot \tan \alpha)^2} = \frac{1}{k \cdot L \left(\frac{L}{t_w} + 2 \cdot \tan \alpha \right)} \quad (4.19)$$

Joy and Schlig's [22] provides thermal resistance as

$$R_{th} = \frac{1}{k \cdot L \cdot \sqrt{\pi}} \text{ for } L = W \quad (4.20)$$

$$\therefore \sqrt{\pi} = \frac{L}{t_w} + 2 \cdot \tan \alpha \Rightarrow \alpha = \tan^{-1} \left(\frac{\sqrt{\pi}}{2} - \frac{L}{t_w} \right) \quad (4.21)$$

For Joy and Schlig's α is equal to 41° for $t_w \gg L$

A spreading angle of 45 degree is assumed for the derivation of total thermal resistance. L and W are lateral dimensions of the top surface of the solid. Hence $A(t)$ is given by

$$A(t) = (L + 2t)(W + 2t) \quad (4.22)$$

The thermal resistance after integration is equal to

$$R_{th} = \int_0^{t_w} \frac{dt}{k \cdot (A)^2} = \frac{1}{2 \cdot k \cdot (L - W)} \ln \left(\frac{L \cdot (t_w + \frac{W}{2})}{W \cdot (t_w + \frac{L}{2})} \right) \quad (4.23)$$

It has been often assumed, that heat spreads with a constant angle from the power dissipating element. This angle can take any value from zero to 90° depending on the substrate boundaries, but in isotropic structures, 45° is the most commonly used value. Both the concept of thermal resistance and capacitance and the idea that the transient behavior of any packaged component can be expressed by a set of exponential terms comes from the well established thermal–electrical analogy [4-6]. Although distributed in nature, it is still possible to model the thermal system as a lumped network of discrete thermal resistances and capacitances whose response to a step input power is given accordingly by a sum of exponential terms. The thermal resistance between thickness of t_1 and t_2 can also be calculated

$$R_{th}(t_1, t_2) = \int_{t_1}^{t_2} \frac{dt}{k \cdot (L + 2 \cdot t_w \cdot \tan \alpha)^2} = \frac{t_2 - t_1}{k \cdot L^2 \cdot [(1 + a \cdot t_1) \cdot (1 + a \cdot t_2)]} \text{ where } a = \frac{\sqrt{\pi}}{2} - \frac{L}{t_w} \quad (4.24)$$

$$C_{th}(t_1, t_2) = \int_{t_1}^{t_2} \rho \cdot c_p \cdot A(t) \text{ if } A(t) = (L + 2 \cdot t_w \cdot \tan \alpha)^2 \text{ considering } L = W \quad (4.25)$$

$$\Rightarrow C_{th}(t_1, t_2) = \rho \cdot c_p \cdot L^2 \cdot \left. \frac{(1 + a \cdot t)}{3 \cdot a} \right|_{t_2}^{t_1} \quad (4.26)$$

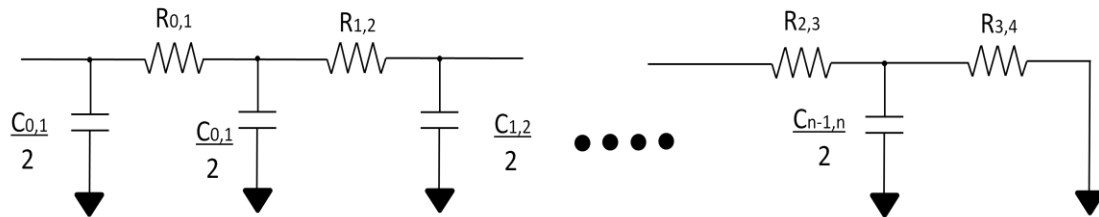


Figure 4.25 Compact modeling of spreading thermal impedance using cauer network.

4.7 Thermal Model For Oxide Bottom

The oxide thickness is very small compared to the lateral dimensions. Hence there is not much thermal spreading in the oxide layer. Therefore, to estimate the thermal resistance and capacitance of the oxide, the formulae to calculate thermal resistance of a slab are used. The thermal resistance of a slab is given by

$$R_{th} = \frac{t_{ox}}{k \cdot L \cdot W} \quad (4.27)$$

where k is the thermal conductivity of the oxide, t_{ox} is the thickness of the oxide, L and W are the internal dimensions of the Si-tub. The thermal capacitance is estimated by using equation (3.25)

where V is given by $V = t_{ox} \cdot L \cdot W$ (4.28)

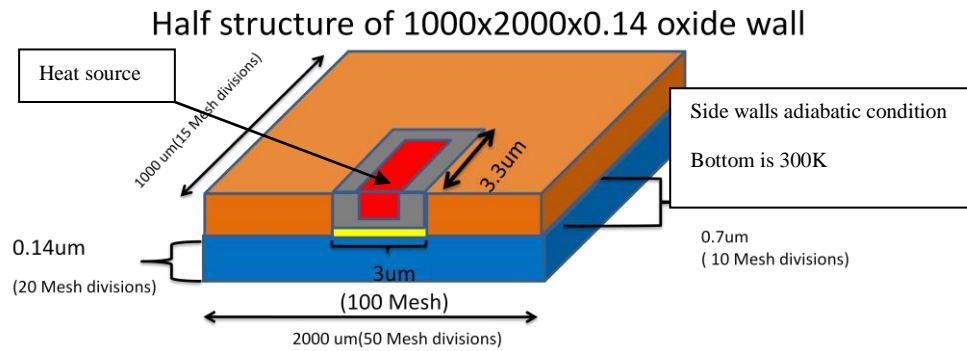
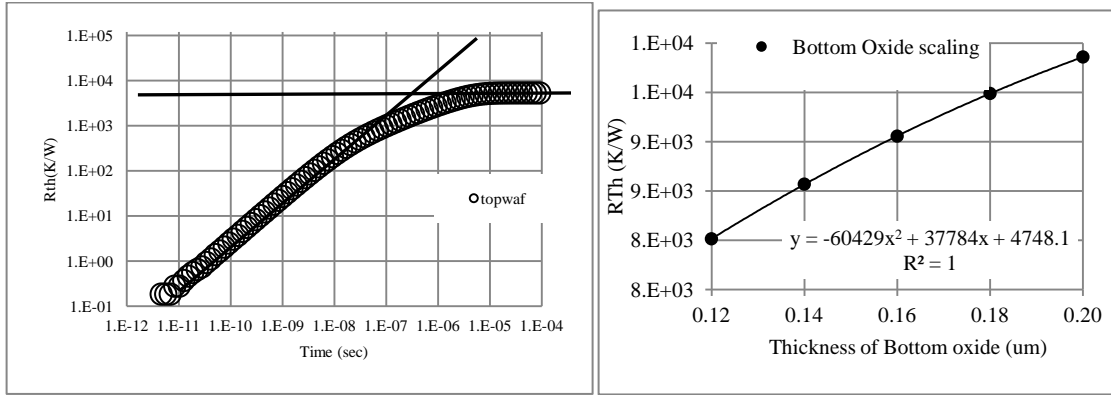


Figure 4.26 3D Davinci simulation for bottom oxide

Figure 4.26 represents the Davinci simulation for the bottom oxide. The bottom of the Tub would be the heat source for this case. From the simulation the thermal characteristic of the oxide can be obtained as shown in Figure 4.27. The side wall of the heater are adiabatic condition with bottom is at ambient temperature. From the lines drawn in Figure 4.27a) the time constants can be calculated. Figure 4.27b) shows how thermal resistance varies with change in thickness of the bottom oxide.



(a) (b)
Figure 4.27 (a) 3D Davinci bottom oxide simulation result (b) Rth of Oxide vs thickness of Oxide

Table 4.1 Simulation result

Input	Masana	Waterloo[33]	Davinci
Rw	4996.9	5321	5315.272
Tau(w)	9.49e-8		3e-7

4.8 Thermal Model For Wafer

The Joy and Schlig's (J & S) method [12] is used to calculate the wafer thermal resistance and capacitance. J & S is used for large wafer thickness applications. In this case, the Masana approach overestimates the thermal capacitance. An equivalent time constant is calculated for a single pole RC network which would require the same total energy to "charge" for the thermal transient response $T(t)$. The single pole thermal capacitance is calculated from the equivalent time constant obtained from the thermal transient response.

$$R_{th} = \frac{1}{k \cdot L \cdot \sqrt{\pi}} \quad (4.29)$$

Joy and Schlig's method for the calculation of wafer thermal resistance involves the evaluation of numerical integration which is not computationally efficient. An analytical expression is derived for the temperature response in a semi-infinite medium for the case of a planar heat source. Using the approximation $H \rightarrow 0$ where H is the heat in (3.41), and using surface heat capacitance, C' , instead of volume heat capacitance, the expression for the transient temperature response becomes [13]

$$T(t) = \frac{P}{c'} \int_0^t \left\{ \operatorname{erf} \left(\frac{\sqrt{\pi} t_w}{\sqrt{4 \cdot u}} \right) \cdot \operatorname{erf} \left(\frac{\sqrt{\pi} t_L}{\sqrt{4 \cdot u}} \right) \cdot \left(\frac{1}{\sqrt{\pi \cdot k \cdot u}} \right) \right\} du \quad (4.30)$$

where $t_w = W^2/4\pi k$, $t_L = L^2/4\pi k$, $C' = \rho_c \cdot A$ is the surface heat capacitance and $A = L \cdot W$.

The integral of (4.30) can be evaluated using an approximation for the error function $\operatorname{erf}(x)$ given by [34]

$$\operatorname{erf}(x) = \sqrt{1 - \left(\exp - \left(\frac{2x}{\sqrt{\pi}} \right)^2 \right)} \quad (4.31)$$

Using the above approximation and putting $L=W$, the expression for $Z_{th}(t) = T(t)/P$ from (4.30) results to

$$Z_{th}(t) = \frac{1}{c'} \int_0^t \left\{ \left[1 - \exp \left(-\frac{t_w}{t} \right) \right] \cdot \left[\left(\frac{1}{\sqrt{\pi \cdot k \cdot u}} \right) \right] \right\} du \quad (4.32)$$

Equation (4.32) is evaluated using [35] to give an analytical expression for thermal impedance $Z_{th}(t)$ for the case $L=W$. This result in

$$Z_{th}(t) = \frac{2}{c' \cdot \sqrt{\pi \cdot k}} \left\{ \sqrt{t} \cdot \left[1 - \exp \left(\frac{t_w}{t} \right) \right] + \sqrt{\pi t_w} \cdot \left[1 - \exp \left(\frac{t_w}{t} \right) \right] \right\} \quad (4.33)$$

For $t \rightarrow \infty$, (4.33) can be evaluated as

$$Z_{th}(t) = \frac{2}{c'} \cdot \sqrt{\frac{t_w}{k}} \quad (4.34)$$

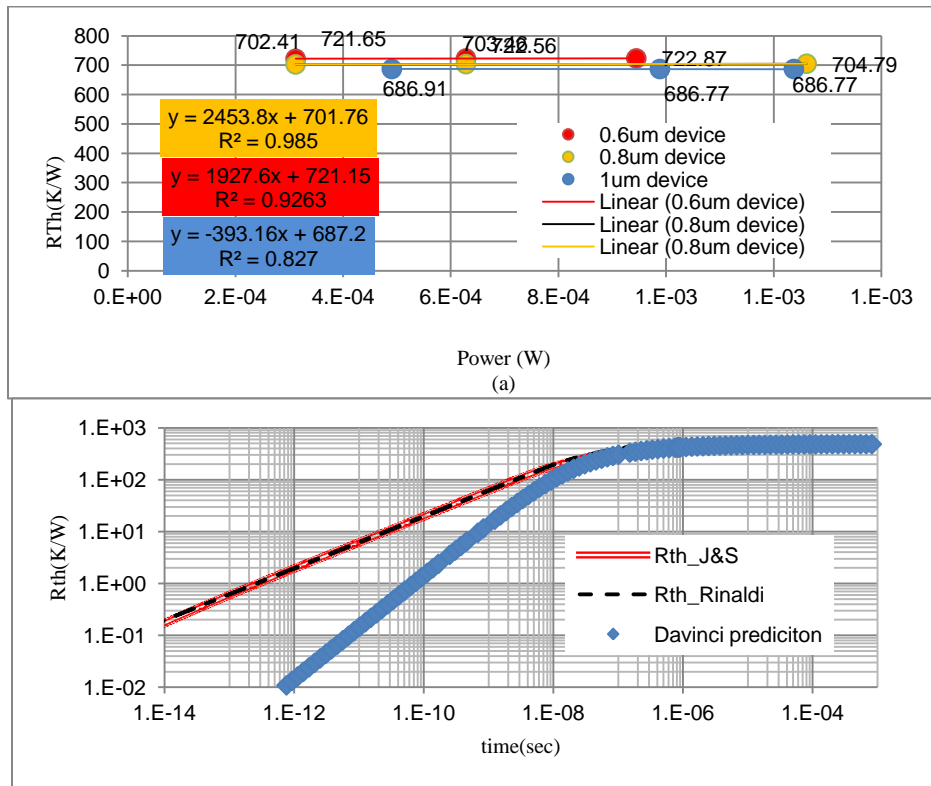


Figure 4.28 (a) Wafer simulation result of 0.6um, 0.8um and 1um device (b) theoretical model vs Davinci simulation with respect to time

Table 4.2 Summary for wafer result

	0.6um device	0.8um device	1um device
Davinci	722.34	702.59	687.2
Waterloo[33]	552	532	514.5
Rth, Schroeder	531.09	510.26	491.695
Rth,J&S	676.2	649.68	626.045

Figure 4.28 summaries the wafer simulation results with the to mathematical representation. The reason for the Davinci prediction slope 1 compare to mathematical model is because Davinci is limited by the number of mesh points. Evolution of is explained in Appendix B.

4.9 Thermal Model for VIA

VIA are generally holes made with metal of high conductivity. Therefore the simple thermal impedance model uses to model the VIA as in (4.35). In this VIA study, the dimensions used are assumed to be $L=1.515\mu\text{m}$ and $W=3.2\mu\text{m}$.

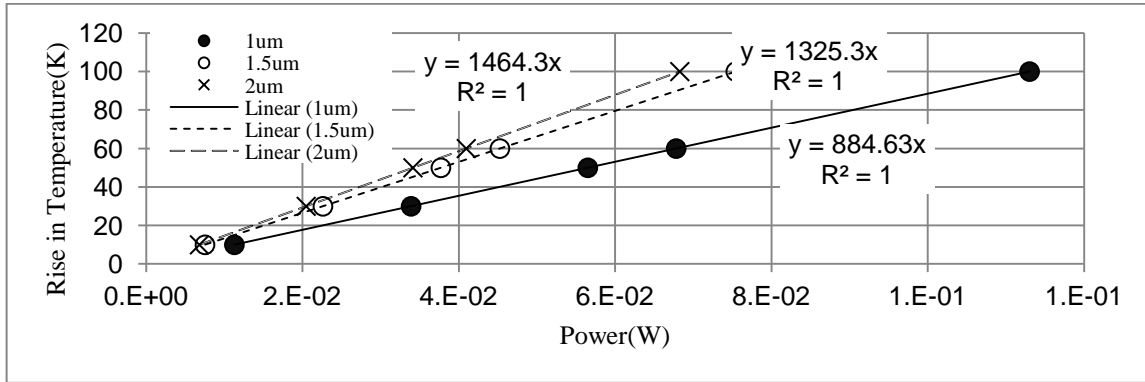


Figure 4.29 VIA Davinci simulation result for 1, 1.5 and 2um via thickness on AL

Table 4.3 Summary of via results

VIA Thickness	Rth (W/K)		
	simple model	medici model	Waterloo Model
1	825.0825083	1179.4	825
1.5	1237.623762	1325.28	1.24E+03
2	1650.165017	1464.34	1.65E+03

$$R_{th} = \frac{t}{k \cdot L \cdot W} \quad (4.35)$$

4.10 Thermal model Solder Bump Connection

Solder/wafer bumps for interconnect design takes less space compared to traditional carrier based systems. They are used for connecting face-down IC chips onto substrates, circuit boards, or carriers in applications such as in the flip-chip, Chip Scale Package (CSP), and Wafer Level Packaging (WLP)[35]. Increasing operating frequencies and data rates, along with decreasing bump sizes results in

higher thermal impedance. It is important to characterize thermal impedance of the line, especially for high frequency microwave devices using solder bump packaging before tap out.

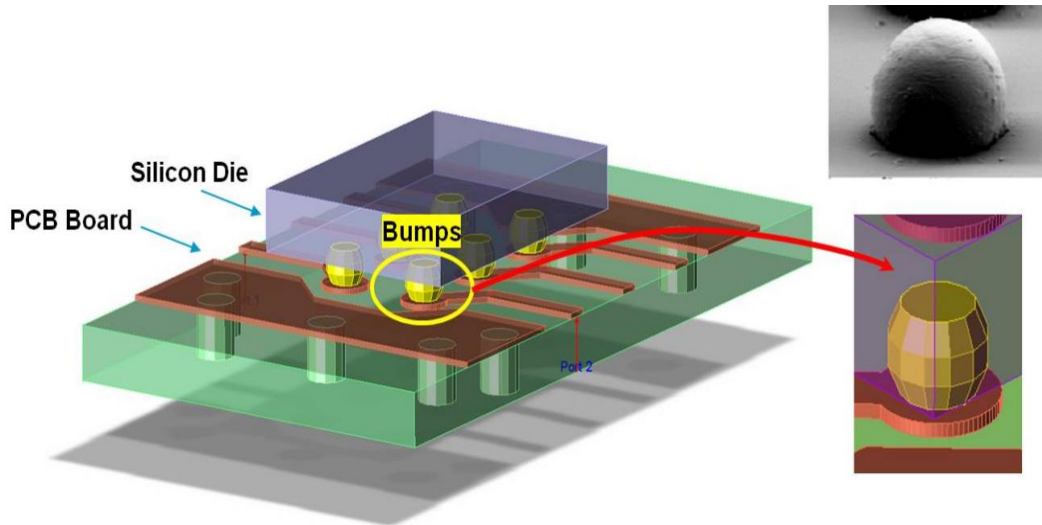


Figure 4.30 Photo and 3D models of typical solder bumps[35]

A complete electrical analogy from theoretical analogy for lossy transmission line electrical network is proposed in this section. It is necessary to mathematically model the line to compare it with simulation of the device. When devices are measured, connection line to the pad and the bond wires add to the thermal impedance. A model is being proposed for this lossy transmission line. Such a line is presented in Figure 4.31, where heat flows through the wire. The silicon dioxide represents the top oxide insulation. A thermal network for this structure is proposed in Figure 4.32. It is assumed the material in the line is aluminum (Al).

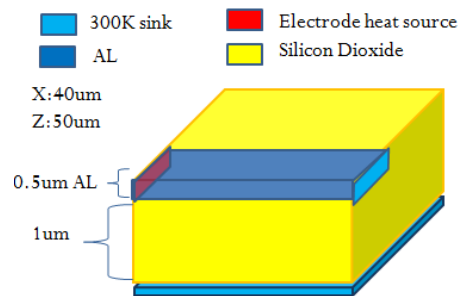


Figure 4.31 Assumed 3D structure of the lossy transmission line

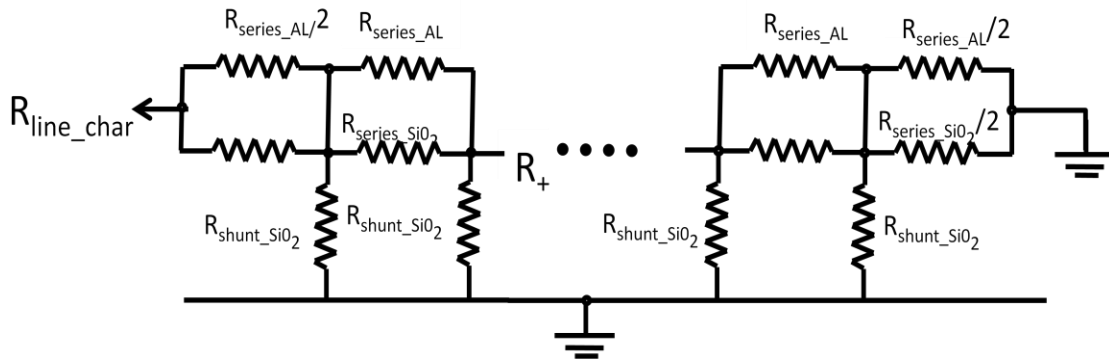


Figure 4.32 Electrical analogy of the Transmission Line

In Figure 4.31, R_{series_AL} represent the thermal resistance because of the heat flow through the Al line. Since the conductivity of aluminum is very high, it's conductivity does not vary with temperature, but remains almost constant. Therefore a temperature dependent model for aluminum conductivity is not necessary. R_{series_SiO2} is the thermal resistance because of heat flow through the silicon dioxide to end of the AL line. This means, while heat has a lower resistive path flow through the aluminum, some heat can flow around the silicon dioxide horizontally to the each ambient temperature point. This is unlikely in most cases because silicon dioxide conductivity is much less than that of aluminum, and heat like its electrical analogy counterpart current would travel through the list resistive path. R_{shunt_SiO2} represents the thermal resistance because of heat flow through the SiO_2 to bottom. In many cases, the bottom of the wafer can be considered ambient temperature point. This resistance forms a parallel connection along the line as shown in Figure 4.32. Since the wafer is connected in series with the bottom silicon dioxide with silicon dioxide thermal conductivity is 110 times less than silicon. Therefore, wafer shunt thermal resistance can be ignored.

Table 4.4 Conductivity of material used

	Conductivity (WK ⁻¹ cm ⁻¹)(k)
Silicon	1.546
Silicon Dioxide	0.014
Aluminum	2.5

4.10.1 Calculating The R_{shunt} For Electrical Analogy

The shunt resistance, R_{shunt} /micron is obtained from finite isotropic channel with strip heat source calculation (university of waterloo)[33]. Appendix D provides details on how the calculation is being obtained.

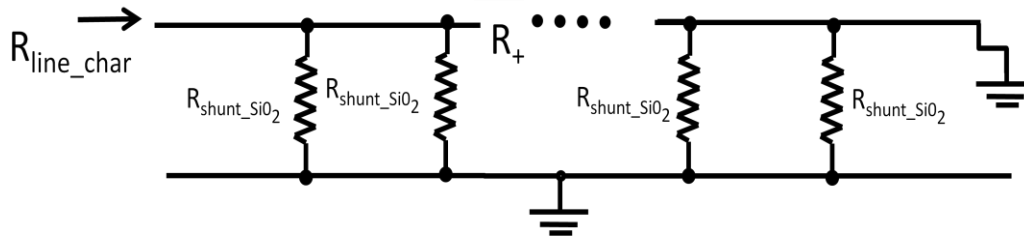


Figure 4.33 R_{shunt} for Electrical Analogy

The thermal resistance of a 1 μ m length for a given width can be obtained from [33]. Therefore

$$R_{SHUNT'} = L \cdot \left(\frac{R_{th \text{ Line waterloo}}}{1\mu m} \right) \quad (4.36)$$

$$R_{shunt_SiO_2} = \frac{R_{SHUNT'}}{i} \quad (4.37)$$

where $R_{SHUNT'}$ is obtained from [33], $\frac{R_{th \text{ Line waterloo}}}{1\mu m}$ is the thermal impedance per micron length, i is the number of element in the network.

4.10.2 Electrical Analogy For R_{series}

The next step is to model the thermal impedance around the Aluminum (AL) line. Heat can flow through the AL strip. Also some heat would flow through the silicon dioxide horizontally to reach ambient. The thermal conductivity of AL is significantly higher than silicon dioxide as show in Table 4.4. Therefore a simpler model as in Figure 4.34 can be assumed.

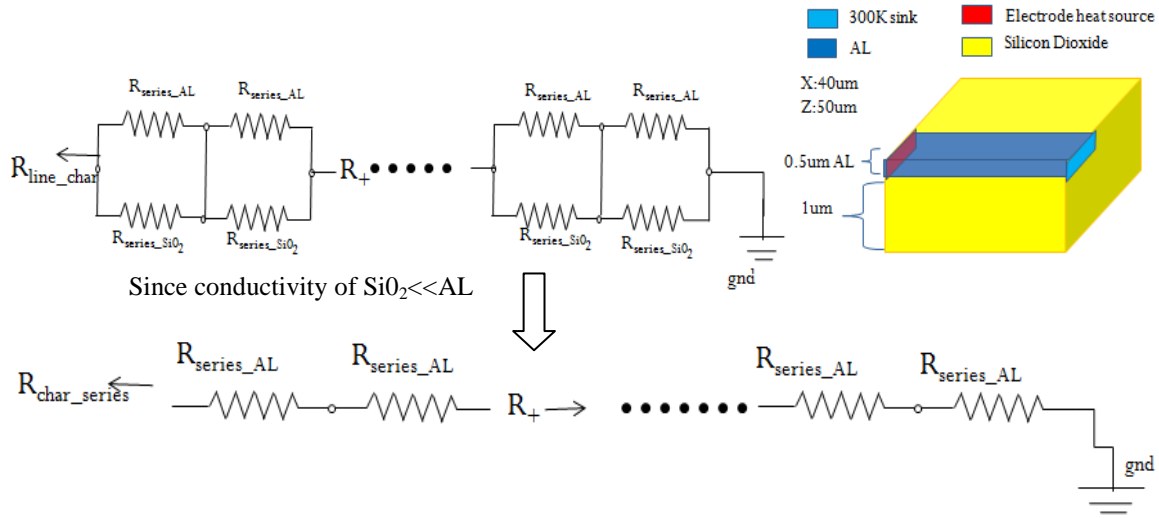


Figure 4.34 Electrical Analogy for the Al line 1 dimension heat flow

Simple model Equation (4.35) can be used for this purpose. For this calculation $W=5\mu\text{m}$ $L=1-40\mu\text{m}$ $t=0.5\mu\text{m}$ where considered.

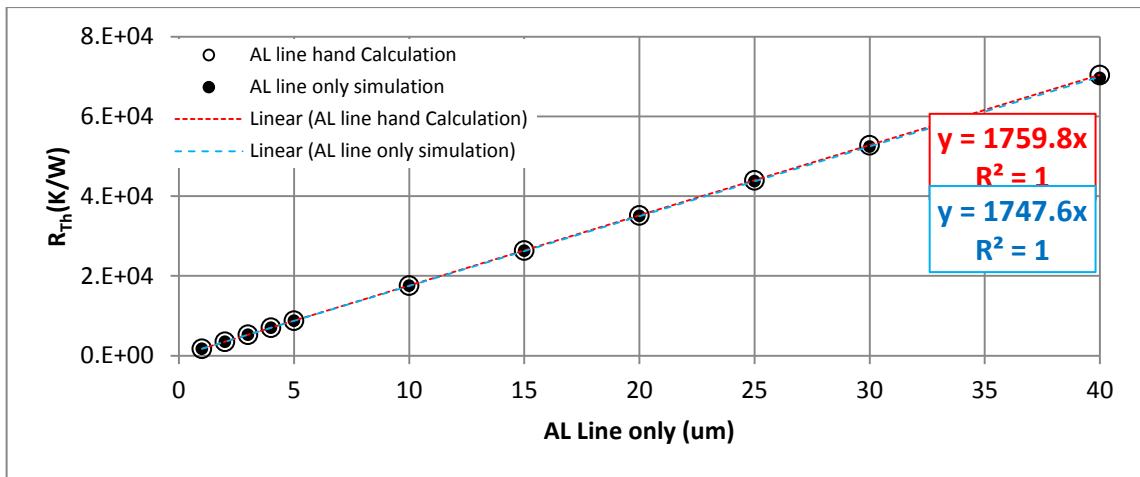


Figure 4.35 Dimensional simulation and calculation for AL line

4.10.3 Simplified Electrical Analogy

The simplified model is represented in Figure 4.34 and its line characteristic equation is shown in (4.38). This equation is used to solve a spreadsheet for the thermal resistance.

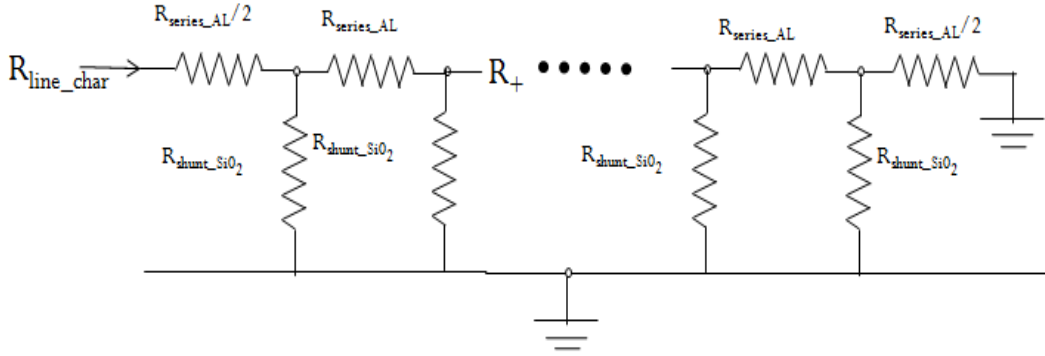


Figure 4.36 Simplified line model

$$R_{line_char} = \frac{R_{series_AL}}{2} + \frac{1}{\left[\frac{1}{R_{shunt_SiO_2}} + \frac{1}{\left(\frac{R_{series_AL}}{2} + R_+ \right)} \right]} \quad (4.38)$$

4.10.4 Davinci Simulation With T Source And Sink At End Of AL Line Only

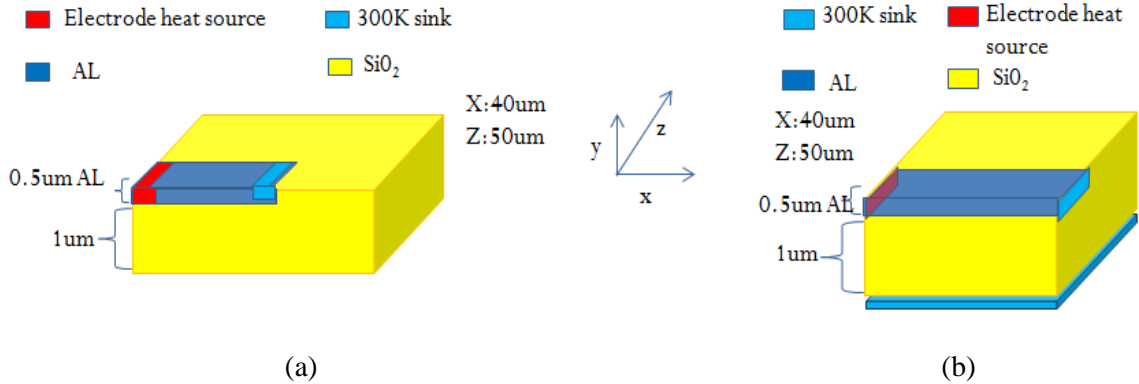


Figure 4.37 (a) Simulation with T source and sink at end of AL line only (5um AL Line Width (z)) (b) simulation that corresponds to waterloo lossy line transmission line.

Figure 4.37 compares two different types of Davinci simulations where in case (a), the simulation is done with a heat source remaining constant at one point and the heat sink distance is varied.

The length of the AL line in the case of (a) always ends at the ambient T, but there would be silicon dioxide present after the end of the line still it reaches the total horizontal length of the cube which is 40um in this structure. For Figure 4.37 (b) is simulated to compare results with Waterloo calculation[33]. In this case wherever the AL line ends, ambient T ends and also the horizontal structure ends. The Waterloo lossy line calculation transmission estimates would replicate these simulation results since it is this structure Waterloo assumes. As soon in the results in Figure 4.38, electrical analogy anticipates the simulation results.

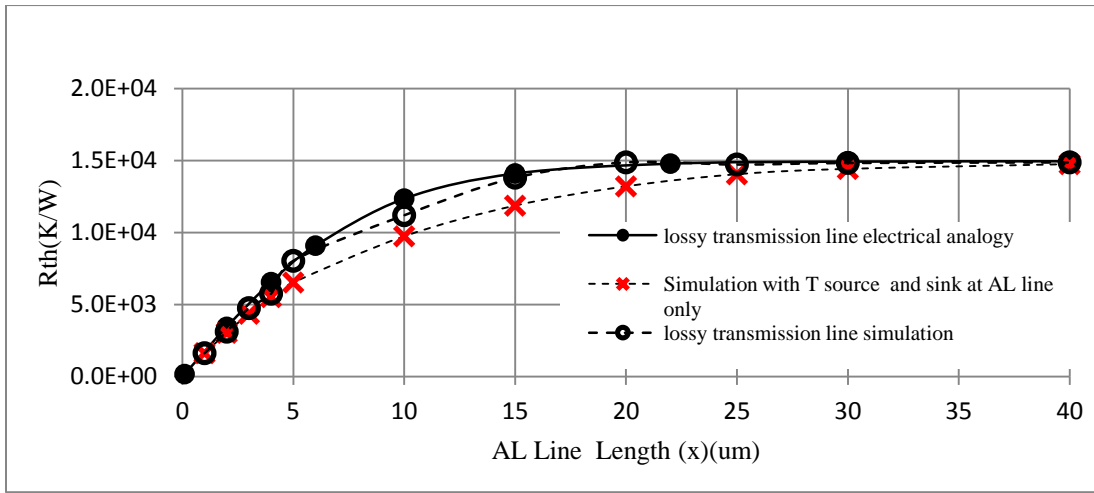


Figure 4.38 Simulation with T source and sink at end of AL line only (5um AL Line Width (z))

4.10.5 R_{Th} Dependence On Width Of The Transmission Line

The Davinci simulation (compared to the electrical analogy) with temperature source and sink at the ends of the Al line of various widths only with SiO₂ thickness of 1µm is explored. For different line widths the thermal impedance would vary. Therefore in Figure 4.37, the z (width) is varied and the results is presented in Figure 4.39.

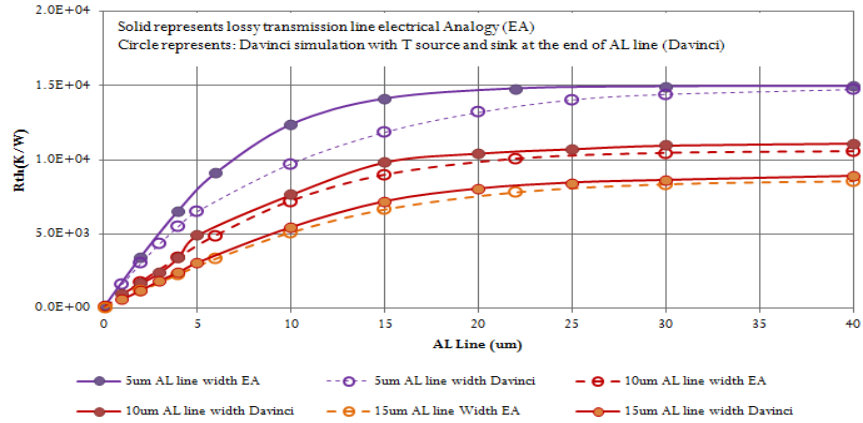


Figure 4.39 Simulation and Calculated result

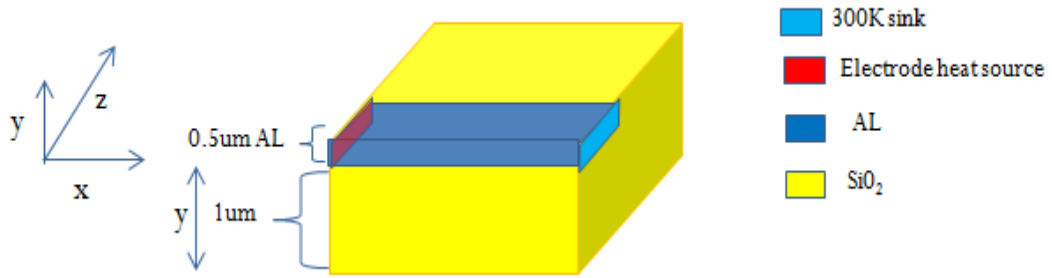


Figure 4.40 Davinci structure representation of variable top oxide thickness

4.10.6 R_{Th} Dependence On Top Oxide Thickness

For Figure 4.40, if the via thickness varies the thickness of the top oxide would also vary. There it is necessary to have a model available of variable via thickness and top insulation thickness. Simulation and simple electrical analog can be used to model with variable thickness; the result of this is presented in

Figure 4.41. Appendix D provides a scaling tool to determine the thermal impedance with thickness dependence.

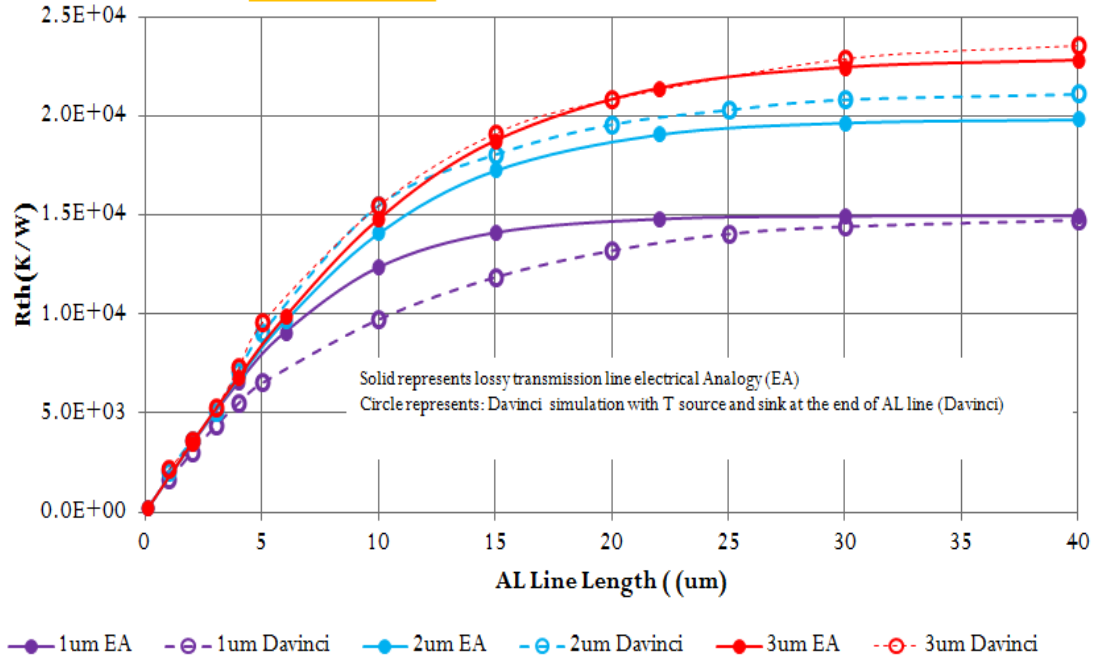


Figure 4.41 Comparison between Davinci simulation to EA for variable top oxide thickness

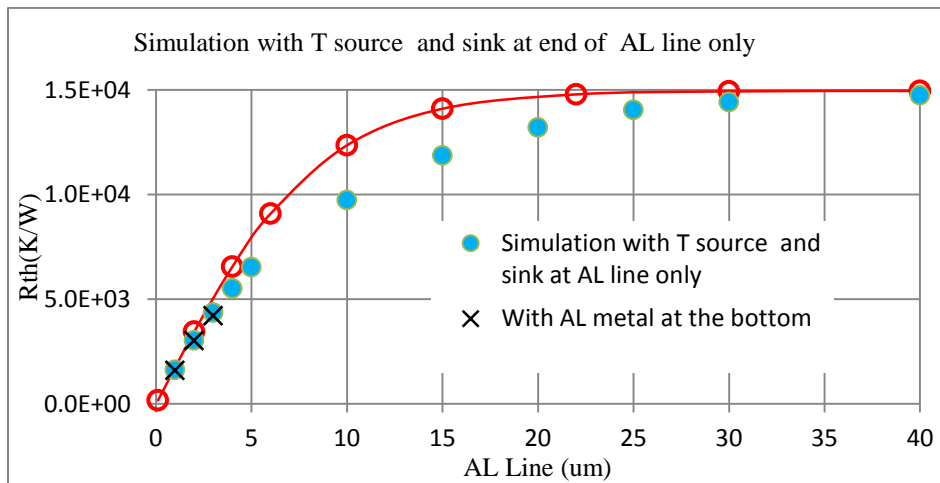


Figure.4.42 Compares the 3D simulation results to simple EA model proposed.

4.10.7 Multiple Solder Bump Connections

There are several connection generally made to a device like connection to the collector, base and emitter. This means that of each device there are parallel connections of R_{line_char} are being made. This means that more connection to the device would reduce the thermal characteristic impedance of the line.

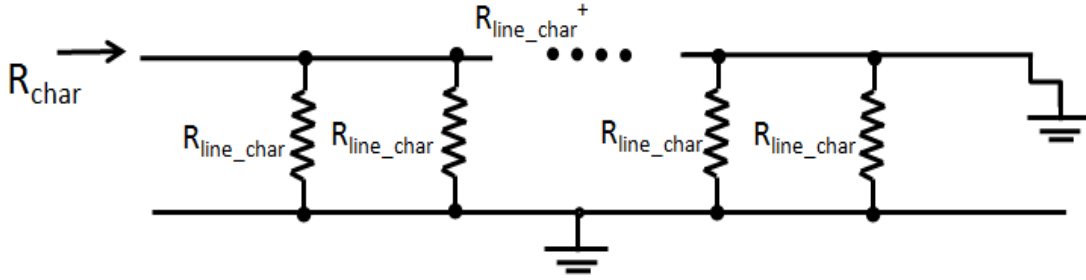


Figure 4.43 Multiple solder bump connections

$$\frac{1}{R_{char}} = \sum_{1}^n \frac{1}{R_{line_char}(n)} \quad (4.39)$$

Where n is number of connection to the device.

4.11 Summary

This chapter covered all the elements in the proposed model in Figure 4.6. For each element a mathematical model is presented along with 3D Davinci simulation and electrical analogy. Therefore of any device electrical analogy can be developed that can be used to model. That model can be implemented in the circuit.

Solder/wafer bumps for interconnect design takes less space compared to traditional carrier based system. They are used for connecting face-down IC chips onto substrates, circuit boards, or carriers in applications such as flip-chip, Chip Scale Package (CSP), and Wafer Level Packaging (WLP). Increasing operating frequencies and data rates, along with decreasing bump sizes results to higher thermal impedance. It is important to characterize thermal impedance of the line specially of high frequency microwave devices using solder bump packaging before tap out. The electrical analogy for the

transmission line formed of the heat flow from heat source to the end of the solder bump is being proposed. This represents the heat flow from the silicon tub and top oxide through the AL line to the end of the solder bump. The network can be simplified considering the thermal heat conductivity in silicon is much higher than silicon dioxide therefore more heat would flow through the silicon and aluminum then compared to silicon dioxide. From the TCAD simulation and mathematical analogy it can be shown that characteristic impedance is dependence on the length of the aluminum line and it gets saturated.

The thermal spreading resistance from the heat source which is lightly doped collector to base junction to the ambient temperature at the bottom of the wafer. The study is performed to understanding how the thermal spreading resistance varies with geometric structure. Also it exposes how thermal resistance when the deep trench thickness and bottom oxide thickness is varies. Electrical analogies are developed for each case. The Tub of the HBT consists of the buried layer, base, collector composite and sink. The heat source can be modeling into a planer structure in order to derive a theatrical analogy. From the TCAD simulation results, optimization is done to evaluate the thermal heat spreading in each case. This provides the spreading angle for the heat source as well as the heating caused by the side walls of the heater. The heat source can be modeled to a planer structure which be used to perform a mathematical approach to calculate heat spreading in TUB. The spreading resistance of the silicon tub is calculated by modeling the tub into section of small slab. Following assumption has been considered

- the thermal resistance increase linearly from bottom slab to the top
- the time constant from each slap remains constant.

CHAPTER 5

3D DAVINCI SIMULATION RESULTS AND DEVICE SCALING

5.1 HBT Davinci Structure With Ambient Temperature At The Bottom

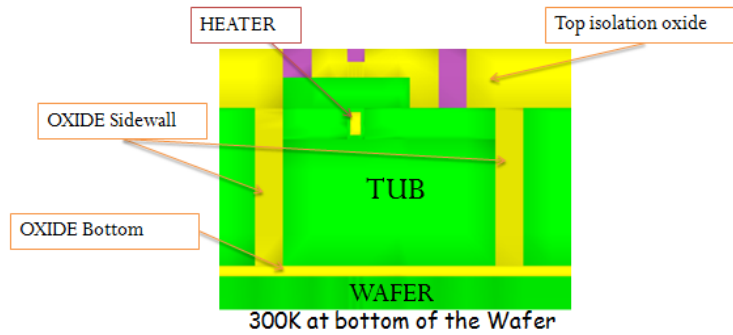


Figure 5.1 3D structure used for simulation

In this section simulation results for Figure 5.1 is being presented. In this case, heat is only allowed to follow through the bottom of the wafer. The heat source is at the lightly doped collect to base regions is represented in Davinci as thermal electron. TI- Sunnyvale has provided all the dimension for their devices which are being simulated using Davinci. Adiabatic boundary condition are considered while doing Davinci simulation at the top, left, right and back for a half structure.

Table 5.1 Thermal conductivity use for the materials

		k(W/(cm-K))	c(J/Kg/K)
Green section	Silicon	1.546790[3]	720.78222[3]
Yellow section	Oxide wall and bottom	0.014006	3000.00000

Temperature (T) is measured using the material properties from Table 5.1. T_0 is set to 300 K. R_0 (R_{th} at 300 K) is the linear coefficient of the polynomial which represent Rise in Temperature ($T-T_0$) versus power which can be calculated from Figures 5.2 to 5.4 reflecting the 3D Davinci simulation results.

From these results, scaling for device length versus thermal impedance can be achieved. Figure 5.5 explores different scaling schemes where linear, polynomial and exponential trend line are to the simulated data fitted. This would provide an approximate estimation of thermal impedance with reference to TUB area. Some the devices are hypothetical and are simulated only to determine the behavior of the trend line. The linear coefficient of the polynomial fit is the Rth0 which is Rth at 300K and the quadratic term of the polynomial fit is the power dependent thermal resister (dRdP).

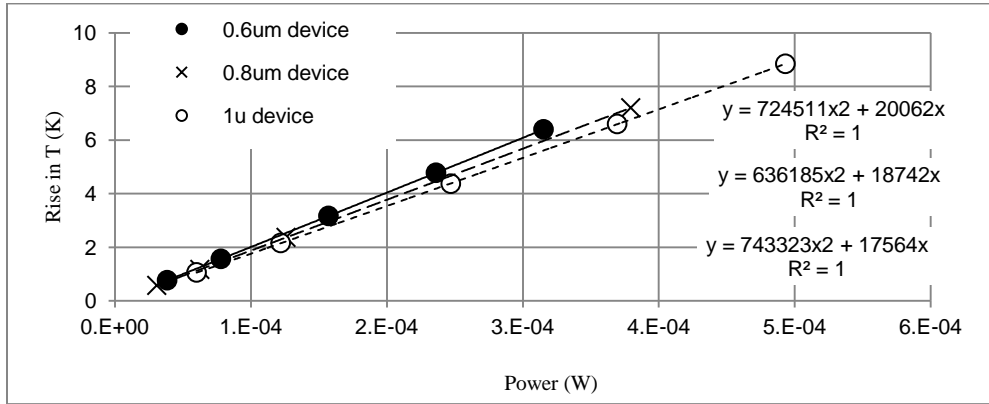


Figure 5.2 Davinci Simulation results 0.6, 0.8um and 1um device simulation results

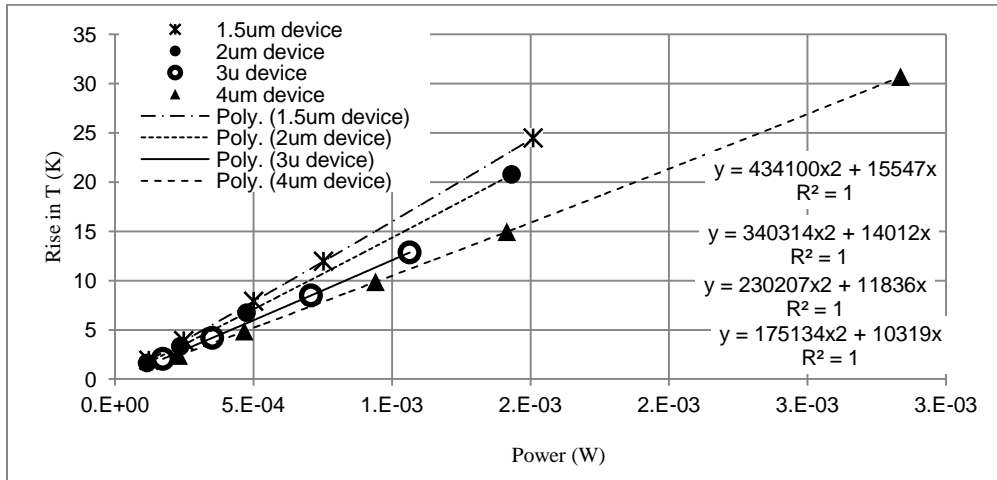


Figure 5.3 Hypothetical devices 1.5um,2um, 3um and 4um device simulation results

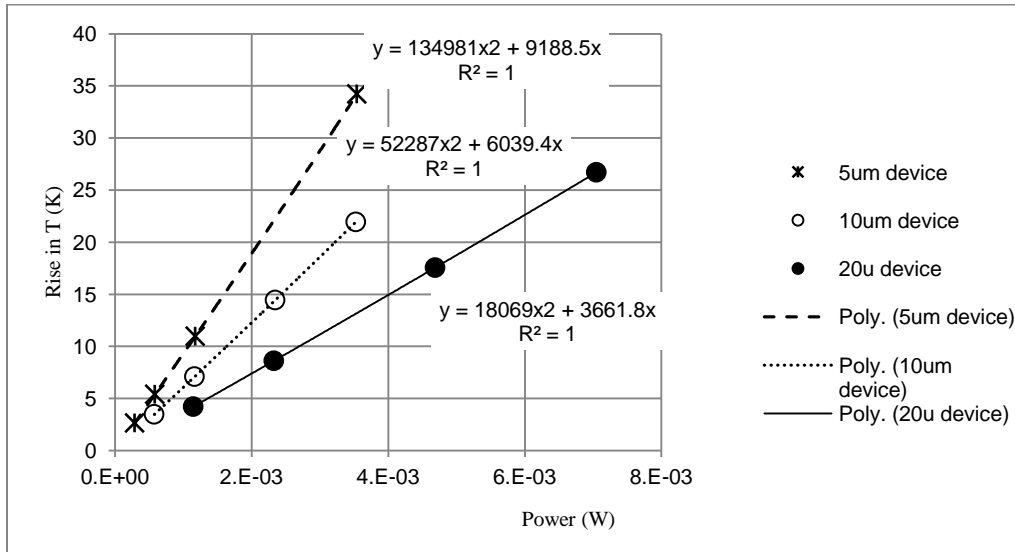


Figure 5.4 5um, 10um and 20um device simulation results

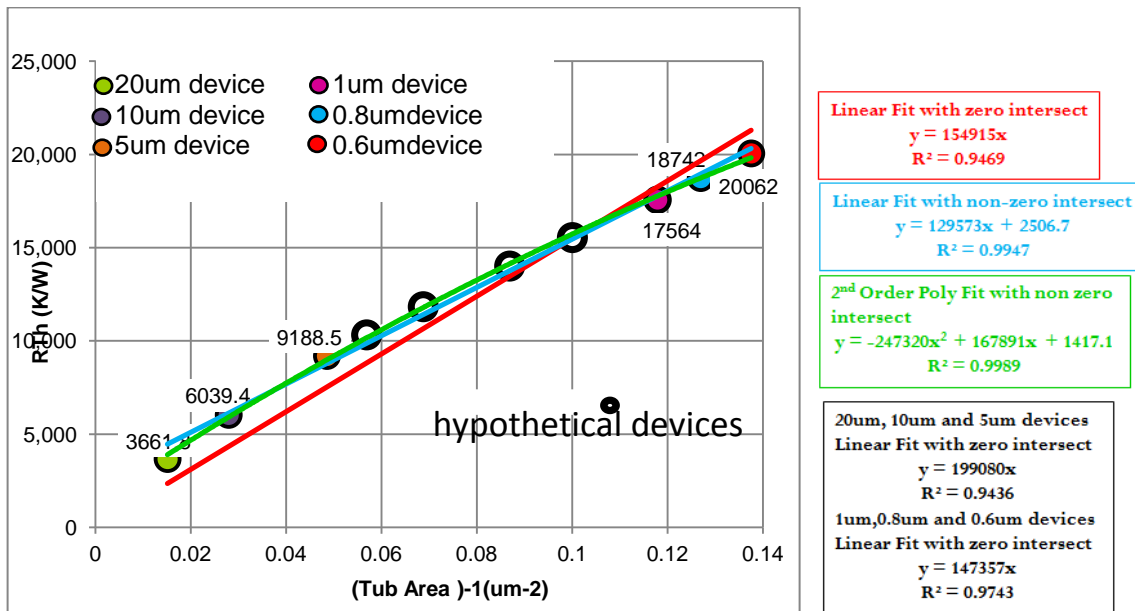


Figure 5.5 R_{Th} scaling for LV Devices

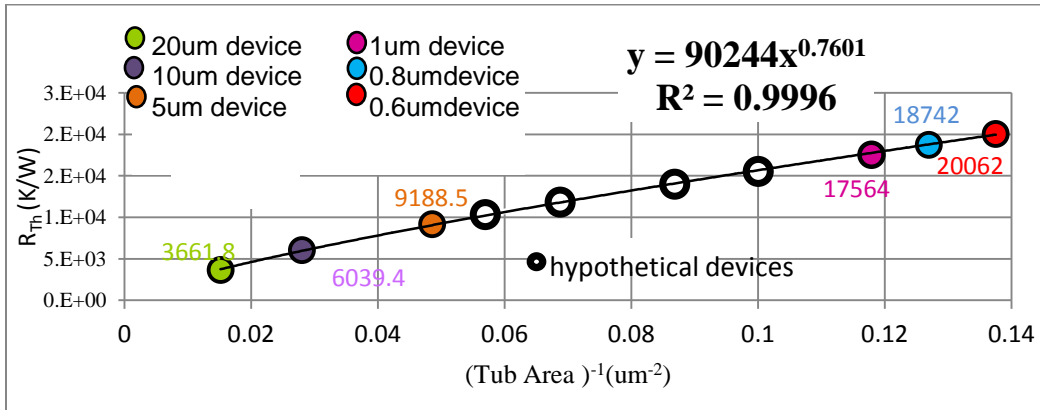


Figure 5.6 R_{Th0} scaled results

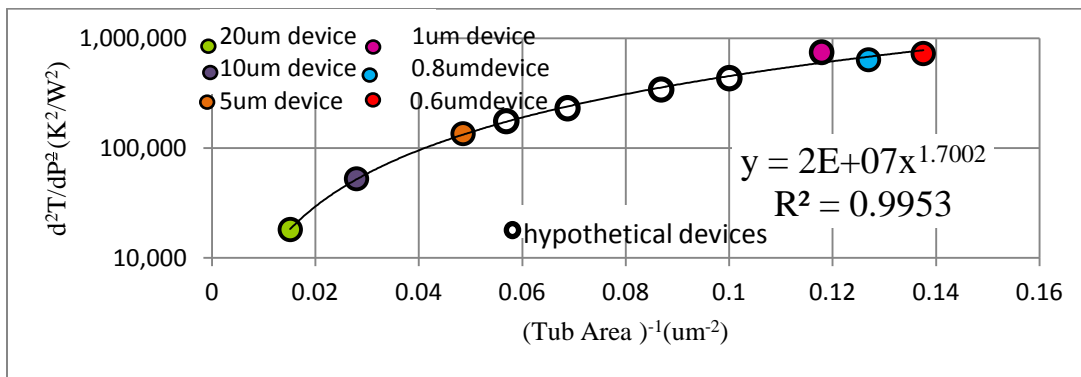


Figure 5.7 Quadratic term scaled

Texas Instrument has supplied 0.4um, 0.6um, 0.8um, 1um, 5um, 10um and 20um emitter length Low Voltage (LV) devices for measurement and simulation. Figure 5.6-5.7 explores different scaling that can be explored for the R_{th0} and $dRdP$. The purpose of these simulations is to develop a model that can predict the R_{th0} and $dRdP$ for devices of different Tub area. The different circles from Figure 5.2 to 5.10 represents different devices with different emitter length.

Table 5.2 Summary of results for the 3D structure with ambient at the bottom

	0.6 micron LV Device	0.8 micron LV Device	1 micron LV Device	5 micron LV Device	10 micron LV Device	20 micron LV Device
Tub+oxide*	10371.4	9688.55	9548.95	8679.8	4844.6	2645.9
Wafer	722.34	702.59	687.2	653.2	602.4	543.1
Total	11093.74	10391.14	10236.15	9333	5447	3189

5.2 HBT Davinci Simulation With Solder Bump Connection

When an HBT is connected with solder bumps it means that ambient temperature is at the top. Generally the bottom of the wafer is connected to a high thermal conductive metal which makes the bottom ambient also. Therefore heat can flow to the environment through the top as well as the bottom of the wafer. The simulation described in 5.1 section does not consider the fact the heat passes to the ambient temperature surface through the top collection. Therefore a separate structure simulation is needed where there are characteristics impedance of the line can be included. The bond wires are approximately 4um diameter wire with 18000K/W thermal impedance.

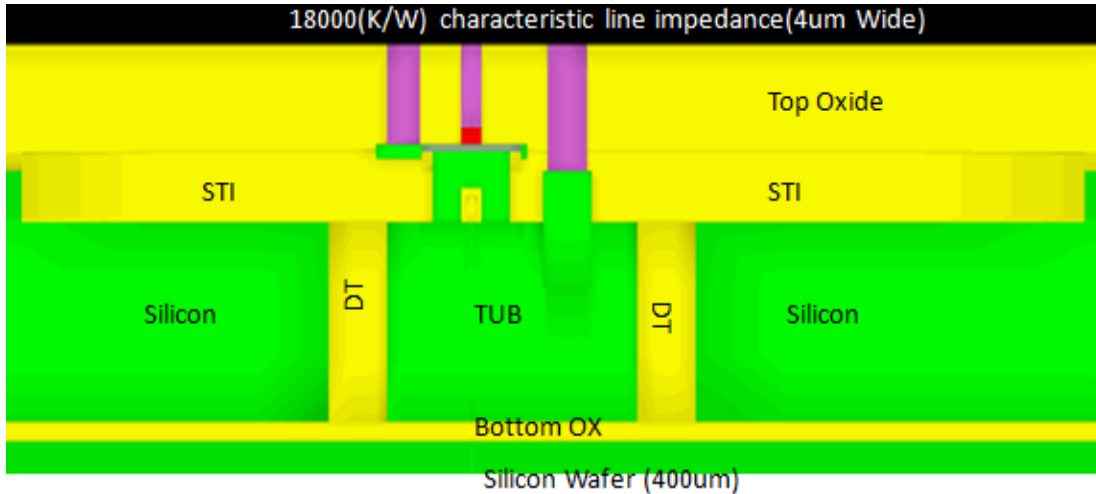


Figure 5.8 Simulation of device with 4um wide line and 5um STI

This representation in Figure 5.8 corresponds to actually measurements. Since fabrication, width of the DT from device to device may vary, simulation of different DT width is done. The overall results

are being compared to measurement. This also provides a scaling tool for the DT width that can be used to model devices.

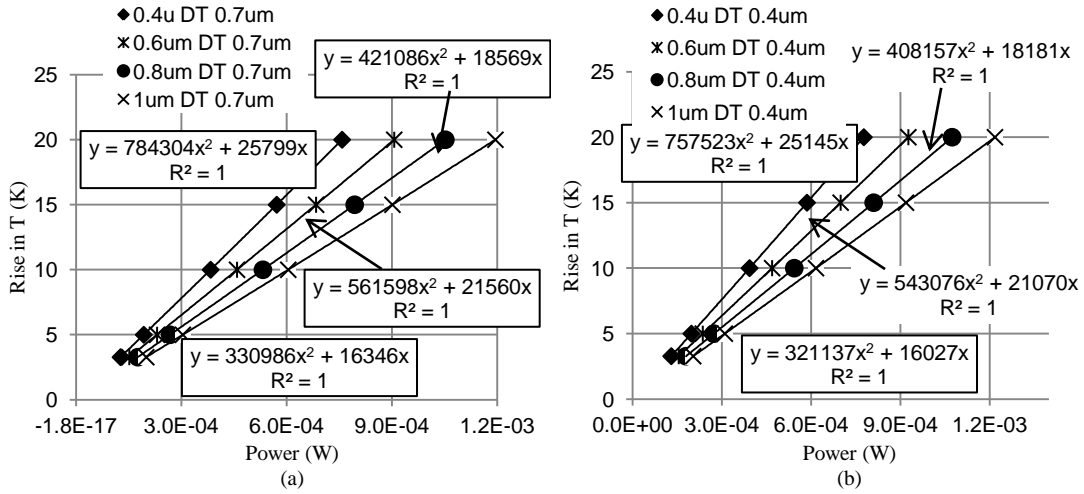


Figure 5.9 Simulation results for 0.4 um, 0.6um, 0.8um and 1um width (a) 0.7um deep trench width (b) 0.4um deep trench width

In Figure 5.9 simulation results for 0.4 micrometer (um), 0.6um, 0.8um and 1um are extracted for 0.7um and 0.4um deep trench width. The linear coefficients (Rth0) for the 0.7um is higher compared to 0.4um DT width. That is acceptable because a wider DT should trap more heat compared to a thin DT. This also shows the simulations are behaving in the direction consistent meaning smaller devices have larger Rth0 and dRdP. Similar simulation study is being done for 5um, 10um and 20um device sizes.

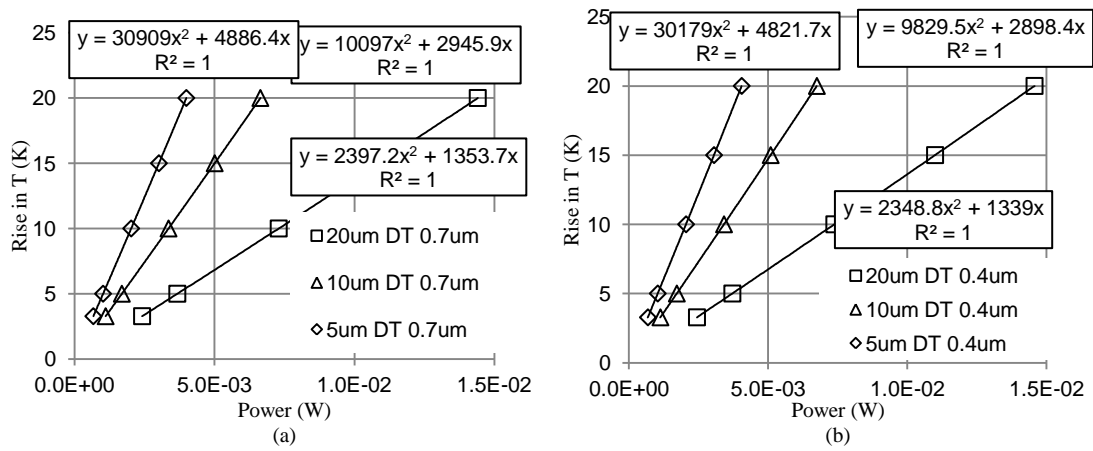


Figure 5.10 Simulation results for 5 um, 10um and 20um with (a) 0.7um deep trench width (b) 0.4um deep trench width

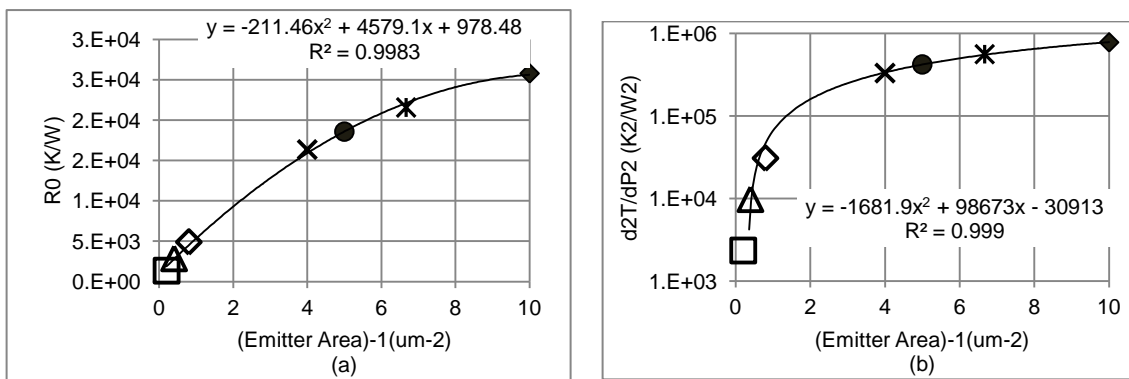


Figure 5.11 (a) Scale for Rth0 (b) Scaling for dRdP

5.3 Davinci Simulation With Variable DT

It is possible to vary the width of the DT for each device which can indicate several important characteristics of the device.

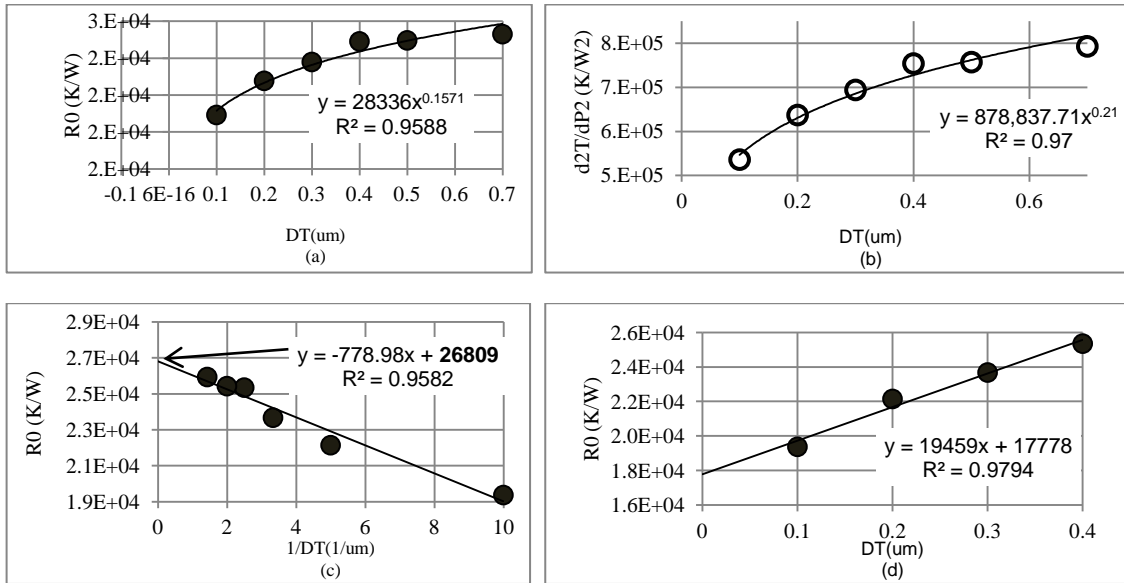


Figure 5.12 (a) R_0 (b) dR/dP (c) infinite and (d) zero resistivity sidewall scaled results for 0.4um device

Figure 5.12 shows the scaling that can be achieved for the 0.4um device. Also from Figure 5.12 c) if the DT is of infinite resistivity, extrapolation can be done to evaluate the resistance. Actual simulation is done with adiabatic boundary condition at the side wall to compare with the extrapolation.

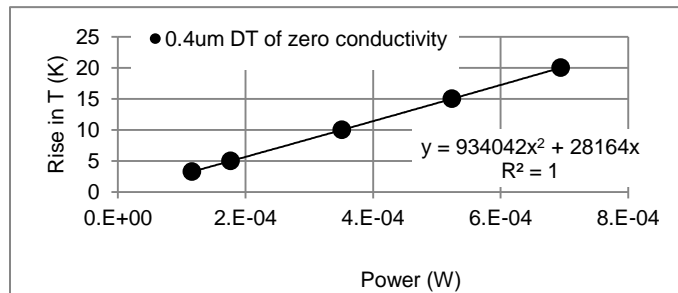


Figure 5.13 D simulation of 0.4um device with infinite DT resistance.

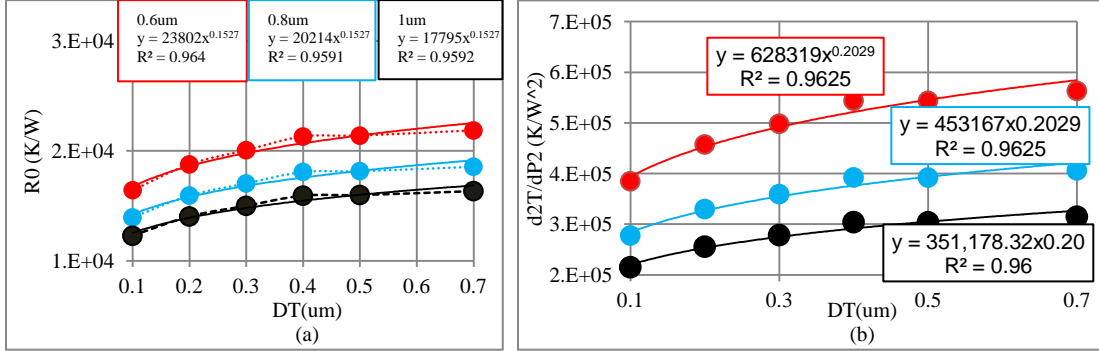


Figure 5.14 (a) R0 (b) dRdP for 0.6um, 0.8um and 1um device

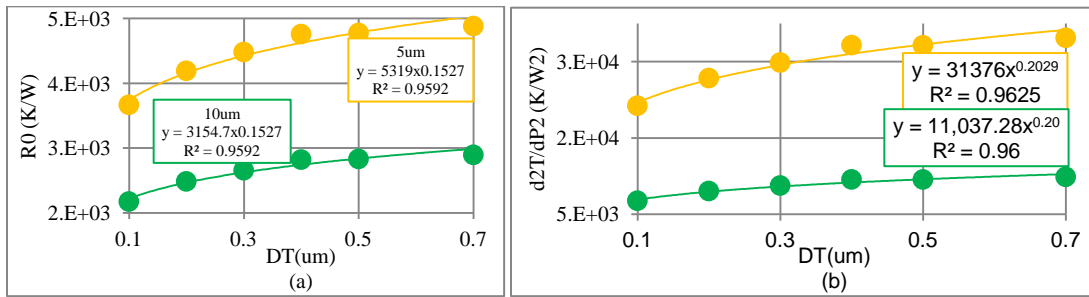


Figure 5.15 (a) R0 (b) dRdP for 5um and 10um device

From the simulation results in Figure 5.13 -5.14, extrapolation similar to 5.12 are done can compared to results from high resistivity DT simulation which is presented in Table 5.3. The simulation results has been satisfactory because the extrapolation is within 10% of the simulated result.

Table 5.3 Comparison between 3D simulation and DT extrapolation

E(um)	extrapolation	Simulation
0.4	26809	28164
0.6	22565	23879
0.8	19163	21644
1	16870	18371
5	5042.4	5357.2
10	2990.7	3075.5

5.4 Conclusion

Table 5.4 lists all the device simulation results with measurement. The measurement of the devices tracks the simulation and is for a good fit. This provides a good estimation of Rth of each device. In Table 5.4 lists the TCAD simulation result to measurement, where the DT of each device were chosen which matches to the measurement[40]. A Scaling procedure is being developed [38][40] which takes into account the area of the tub, area of side walls, deep trench width, bottom oxide and respective thermal conductivities. The result of the scaling is shown in Figure 5.16 which reflects the TCAD closely follows the measurement produced by [39][40]

Table 5.4 Summary of measurement result to TCAD

Devices (um)	UTA Rth 1X (K/W)	UTA Rth 2X (K/W)	Rth TCAD
0.4	17127.97	17183.46	19515.27
0.6	15119.61	15136.53	16544.25
0.8	14278.25	14343.57	14079.88
1	12755.68	12773.89	12400.64
5	5537.864	5717.725	4937.732
10	3442.538	3310.098	2940.435
20	1964.834	1800.098	1358.245

$$W_{tub} = W_e + \Delta W$$

$$L_{tub} = L_e + \Delta L$$

$$A_{bottom} = L_{tub} \cdot W_{tub}$$

$$Perimeter = 2 \cdot (L_{tub} + W_{tub})$$

$$A_{side} = Perimeter \cdot h_{DT}$$

$$\frac{1}{R_{th}} \approx \frac{k_{iso} \cdot A_{bottom}}{t_{iso-oxide}} + \frac{k_{tr} \cdot A_{side}}{t_{DT}}$$

W_e – Width of the emitter in m

L_e – Length of the emitter in m

ΔW – Total offset of the emitter width wrt tub in m

ΔL – Total offset of the emitter length wrt tub in m

A_{bottom} – Area of the tub in m^2

h_{DT} – Height of the deep trench in m ~ 1.65 μm

k_{iso} – Conductivity of the isolation oxide

k_{tr} – Conductivity of the trench oxide

$t_{iso,oxide}$ – Thickness of the isolation oxide in m ~ 0.14 μm

t_{DT} – Thickness of the deep trench in m ~ 0.6 μm

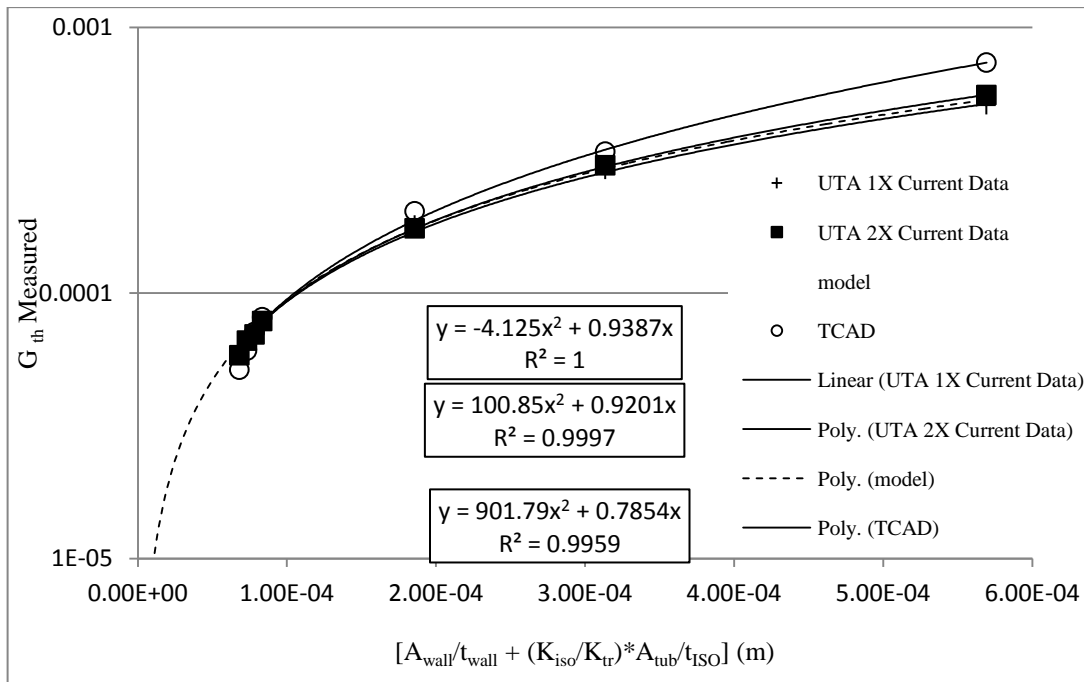


Figure 5.16 Scaling of devices

Figure 5.16 shows that Medici simulation can be used to develop a scaling function to predict thermal resistance in a device. The measurement is compared to the simulation and their scaling trench line is almost identical. UTA 1X and UTA 2X are measurement of devices where in case of 1X the devices were operated at the SOA power and in case of 2X twice the amount of power was provided in order to determine the variation of dRdP term.

CHAPTER 6

CONCLUSION AND FUTURE WORK

Hetero-junction bipolar junction transistors (HBT) are electrically isolated from adjacent devices by the presence of a silicon dioxide trench. This traps heat within an device which is referred as self heating. It has very important role in the analog circuit design. Self-heating occurs when a HBT is heated up by the power consumed in it HBT. This self heating depends on the structure of the device, connection to the ambient and its bias regions. These dependencies on thermal effects are investigated and analyzed in this dissertation. This research emphasizes self-heating and the factors that it depends on. Analysis of these factors, their dimensional dependence, mathematical model and equivalent electrical analogy of the thermal network is proposed in this research.

The first chapter covers a brief description of the HBT and its properties. It covers the processes used to fabricate the devices that are supplied by Texas-Instruments. An introduction of simulation models available is covered in Chapter 2. Finally the industry standard model for HBT are being introduced and compared with one another. High Current Model (HICUM) is introduced and compared to other industry model. The HICUM model has a one element thermal network which can be used to model the thermal characteristics of a device. The general thermal impedance model is explained and the heat flow in material is explained in chapter 3. The mathematical models for the heat flow equation are introduced. Four different mathematical representations with its compact thermal model is also briefly explained in chapter 3. This chapter covers the mathematical model and the electrical analogy model needed for all the different layers of the HBT. Chapter 4 introduces the compact model developed for the HBT based on TCAD simulation and electrical analogy. If each thermal impedance value of the compact model is calculated with accuracy, the more accurate thermal model for self-heating can be obtained. A new technique has been developed to extract each thermal impedance of the element compact model for the dielectrically isolated bipolar junction transistor in chapter 4. The new method uses the thermal simulation tool – Davinci. There are several conditions to extract the seed values for the compact model.

After Davinci simulations using these conditions, the curve fitting method in MathLab and optimization method in ICCAP is used to calculate the final values of the compact model.

The device is non-isothermal and asymmetric. Therefore, the temperature of each emitter region is different. The maximum temperature of the device is at the lightly doped collect to base region. In Chapter 4 a technique has been introduced to locate and estimate the depletion region at the lightly doped collect to base region. After estimation of the heat source, it is important to convert the heat source into a planar structure in order to develop a mathematical model. This is done by considering a heater spreading angle. Heat flow through the tub with an angular spread thus giving rise to spreading resistance. The simulation and modeling of this spreading resistance is being proposed. The model of the heat flow through the silicon dioxide, wafer and side walls are being simulated in TCAD and electrical analogy is being developed. Other components like via, line pad connection which would contribute to thermal resistance of a device are being explored and modeled. All the components in Figure 4.6 are being simulated and modeled. This difference should be considered to use the proposed method. The main differences are in the wafer thermal resistance and the distributed thermal resistance. The value of the wafer thermal resistance is over calculated by the compact model calculation than that by the simulation extraction in all three cases. The value of the distributed thermal resistance is under calculated by the compact model calculation than that by the simulation extraction in all three cases. The last section of chapter 4 discuss the distributive nature of the line connects. In chapter 5 all the simulations for the entire device are being covered and a scaling tool for all the devices is being proposed. The total simulation is being compared to measurement result and the simulation. Simulations resulted to a 0-20% error compared to measurement but if the dimensions of the deep trench are varied, simulation can result to an accuracy of 5%. This suggests the deep trench thermal dimension and properties can be different than what is accepted of it.

There are several studies that have not been covered in this study which can be done in future. Adjacent heating is an important element in thermal modeling and TCAD simulation can be done to model the effect of adjacent heating. The effect of hot carrier on thermal resistance very important

because trapping of hot carriers in the deep trench can change the thermal conductivity of deep trench isolation. This would always be a reliability study. Effect of thermal resistance on collector current can be explored. Multiple emitter device study on thermal resistance is another important area. Layout and its parasitic impedance and its contribution to thermal heating is become a major concern. Layout also has effects on adjacent heating in devices.

APPENDIX A

MATERIAL PROPERTIES

The mass density, specific heat, and thermal conductivity of a material used in Equation (A.1) are given by the following expressions[11]:

$$\begin{aligned} \rho &= \text{Density} \\ c &= A.SP.HEA + B.SP.HEA \cdot T + C.SP.HEA \cdot T^2 + D.SP.HEA \cdot T^{-2} \\ &\quad + F.SP.HEA \cdot T^3 + G.SP.HEA \cdot T^4 \\ \lambda &= [A.TH.CON + B.TH.CON \cdot T + C.TH.CON \cdot T^2 \\ &\quad D.TH.CON \cdot T^{-E.THON.CON}]^{-1} \end{aligned} \quad (A.1)$$

Table A.1 Thermal property of material used

	Units	Silicon	Silicon Oxide	Aluminium	polysilicon
A.TH.CON	cm-K/W	0.03	71.4	0.4	0.437
B.TH.CON	cm/W	1.56E-03	0	0	0
C.TH.CON	cm/W/K	1.65E-06	0	0	0
D.TH.CON	cm/W/K ^{E.TH-1}	0	0	0	0
E.TH.CON		0	0	0	0
A.SP.HEA	J/kg/K	850.9	3000	910	737
B.SP.HEA	J/kg/K ²	1.52E-01	0	0	0
C.SP.HEA	J/kg/K ³	0	0	0	0
D.SP.HEA	J-K/kg	-1.58E+07	0	0	0
F.SP.HEA	J/kg/K ⁴	0	0	0	0
G.SP.HEA	J/kg/K ⁵	0	0	0	0
DENSITY	kg/cm ³	2.32E-03	2.26E-03	2.70E-03	2.32E-03
At T=	300				
λ	WK cm ⁻¹	1.546790	0.014006	2.500000	2.288330
c	J Kg ⁻¹ K ⁻¹	720.78222	3000.00000	910.00000	737.00000

APPENDIX B

INFINITE MESH POINT ANALYSIS

A recursive distributed model for the thermal impedance of a SiGe HBT is explained in [37]. The thermal impedance model based on the physical heat transfer equation results in a compact expression which is a fractional order (1/2 order) system [37].

$$Z_{TH}(p) = \frac{R_{TH}}{(1 + \sqrt{R_{TH} \cdot C_{TH} \cdot p})} \quad (\text{B.1})$$

where p is the Laplace variable, R_{TH} and C_{TH} represent the thermal resistance and capacitance respectively. The device temperature rise transient response is the inverse Laplace transform of $Z_{TH}(p)$ and leads to

$$T_{rise}(t) = \Delta T \cdot \left(1 - \exp\left(-\frac{t}{\tau}\right) \operatorname{erfc}\left(\sqrt{\frac{t}{\tau}}\right) \right) \quad (\text{B.2})$$

where $\Delta T = P_{diss}(t) \cdot R_{TH}$ and $\tau = R_{TH} \cdot C_{TH}$. The upper cutoff frequency, f_u is defined by:

$$f_u \approx \frac{1}{2 \cdot \pi \cdot k^{2n} \cdot R_0 \cdot C_0} \quad (\text{B.3})$$

where n is the number of RC elements in the network and k is the recursivity co-efficient which provides degree of liability. From (B.2) and (B.3), the cutoff frequency f_c can be estimated as

$$f_u \approx k^{2n} \cdot f_c \quad (\text{B.4})$$

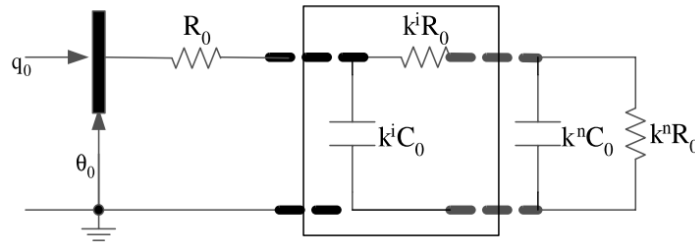


Figure B.1: A recursive RC network for the thermal impedance. q_0 represents the power flow and θ_0 represents the temperature rise

The present of finite number of elements in the circuit it is seen in the electronic simulation a shift occurs from about a slope of 2 to a slope of 1. For a cascade of balanced Cauer network, the corner

frequency is $f_{cn} = 2/(3 \pi \tau_{tot})$ and for a single section the corner frequency is $f_c = 1/(\pi \tau_{tot})$ [12]. Therefore in case of TCAD simulation, the number of mesh points is limited, which can result of slope of 1 instead of $1/\pi$. Because of this limitation, sometime it is better to perform layer by layer simulation.

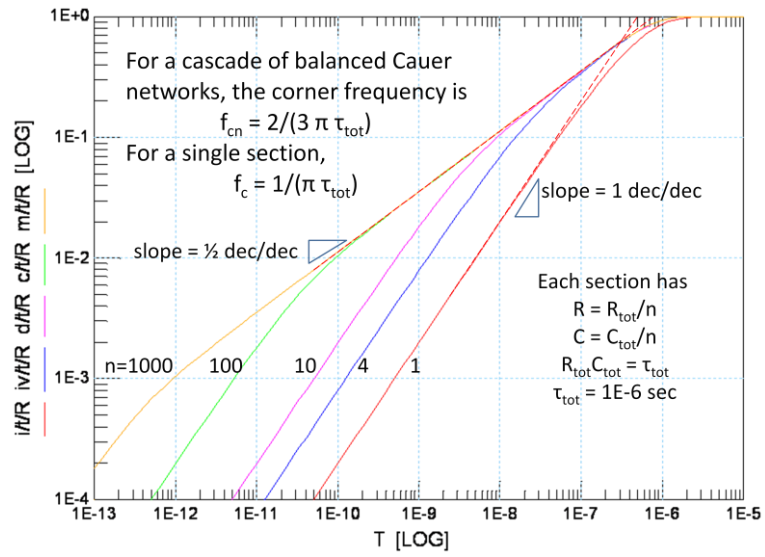


Figure B.2 Effect of changing number of sections for RC distributive line.[38]

APPENDIX C

DAVINCI CODE FOR TCAD SIMULATION

Code of Davinci simulation can be written in different form depending on the user's choice.

There are two basic ways of creating a structure in Davinic. First one is to write the mesh point description in Davinci itself like shown in the example code. The other is to upload from TSUPREME4 simulation which is a fabrication tool. After the structure of a device is defined, the device can be simulated to extract any parameter or properties. The example sample code of Davinci provides the structure of 10micromenter device and its transient thermal impedance extraction :

TITLE Davinci -10u device total simulation

```
COMMENT Grid generation
COMMENT Mesh Specifications
MESH ^DIAG.FLI
COMMENT X-MESHING
MESH OUT.FILE=MDEX16M
COMMENT Basic structure - Box
X.MESH X.MIN=0 X.MAX=0.125 N.SPACES=5
X.MESH X.MIN=0.125 X.MAX=1.145 N.SPACES=3
X.MESH X.MIN=1.145 X.MAX=1.515 N.SPACES=3
X.MESH X.MIN=1.515 X.MAX=1.915 N.SPACES=2
X.MESH X.MIN=1.915 X.MAX=50 N.SPACES=7 RATIO=1.4

Y.MESH Y.MIN=-1 Y.MAX=0 N.SPACES=3
Y.MESH Y.MIN=0 Y.MAX=0.4 N.SPACES=8
Y.MESH Y.MIN=0.4 Y.MAX=2.05 N.SPACES=6
Y.MESH Y.MIN=2.05 Y.MAX=2.19 N.SPACES=4
Y.MESH Y.MIN=2.19 Y.MAX=400 N.SPACES=18 RATIO=1.4

Z.MESH Z.MIN=0 Z.MAX=10 N.SPACES=4
Z.MESH Z.MIN=10 Z.MAX=10.35 N.SPACES=2
Z.MESH Z.MIN=10.35 Z.MAX=10.55 N.SPACES=3
Z.MESH Z.MIN=10.55 Z.MAX=10.9 N.SPACES=2
Z.MESH Z.MIN=10.9 Z.MAX=100 N.SPACES=10 RATIO=1.4

REGION NAME=WALL OXIDE Y.MIN=-1 Y.MAX=400 X.MIN=-1000 X.MAX=1000 Z.MIN=-500
Z.MAX=500
REGION NAME=WAFER silicon Y.MIN=0 Y.MAX=400 X.MIN=-1000 X.MAX=1000 Z.MIN=-500
Z.MAX=500
REGION NAME=WALL2 OXIDE Y.MIN=-1 Y.MAX=2.19 X.MIN=-4.375 X.MAX=1.915 Z.MIN=0
Z.MAX=10.9
REGION NAME=TUB silicon Y.MIN=0 Y.MAX=0.4 X.MIN=-2.295 X.MAX=1.145 Z.MIN=0
Z.MAX=10.35
REGION NAME=TUB silicon Y.MIN=0.4 Y.MAX=2.05 X.MIN=-3.975 X.MAX=1.515 Z.MIN=0
Z.MAX=10.55
```

REGION NAME=TUB silicon Y.MIN=-0.667 Y.MAX=0 X.MIN=-3.975 X.MAX=1.515 Z.MIN=0
Z.MAX=10.55

REGION NAME=HIGHK OXIDE Y.MIN=0 Y.MAX=0.4 X.MIN=-0.125 X.MAX=0.125 Z.MIN=0
Z.MAX=6

REGION NAME=Resistor OXIDE Y.MIN=0.1 Y.MAX=0.3 X.MIN=-0.075 X.MAX=0.075 Z.MIN=0
Z.MAX=4

REGION NAME=bottomox OXIDE Y.MIN=2.05 Y.MAX=2.19 X.MIN=-1000 X.MAX=1000
Z.MIN=-500 Z.MAX=500

ELECTR NAME=cathode TOP

ELECTR NAME=Emitter-h Y.MIN=.15 Y.MAX=.25 X.MIN=0 X.MAX=0.025 Z.MIN=-1 Z.MAX=2
THERMAL

ELECTR NAME=Heat_sink BOTTOM THERMAL

COMMENT COLLECTOR PROFILE

PROFILE REGION=WAFER N-TYPE N.PEAK=5E15 UNIFORM OUT.FILE=S1SI
MATERIAL REGION=Resistor A.TH.CON=20000 B.TH.CON=0 C.TH.CON=0 A.SP.HEA=.00001
MATERIAL REGION=HIGHK A.TH.CON=.00000001 B.TH.CON=0 C.TH.CON=0
A.SP.HEA=.00001

COMMENT Regrids on doping

REGRID DOPING LOG RATIO=3 SMOOTH=-1
+ IN.FILE=S1SI
PLOT.3D BOX GRID BOUND TITLE="Doping Regrid 1" FILL

COMMENT Regrids on doping

REGRID DOPING LOG RATIO=3 SMOOTH=-1
+ IN.FILE=S1SI
+ OUT.FILE=S1SM
PLOT.3D BOX GRID BOUND TITLE="Doping Regrid 2" FILL

COMMENT Regrids on doping

REGRID DOPING LOG RATIO=3 SMOOTH=-1
+ Y.MAX=0.4
+ IN.FILE=S1SI
+ OUT.FILE=S1SM
PLOT.3D BOX GRID BOUND TITLE="Doping Regrid 2" FILL

FILL

COMMENT MODELING THE TRANSISTOR

MODELS CONMOB CONSRH AUGER

COMMENT Initial solution

SYMB CARRIERS=2 ILUCGS LAT.TEMP COUP.LAT
METHOD ILU.ITER=700 MAX.TEMP=3000000
SOLVE T(Emitter-h)=300
SOLVE OUT.FILE=S1SS

```

PRINT TEMPERAT
SAVE OUT.FILE=S1SMS.tdf TDF

COMMENT TRANSIENT ANALYSIS OF RTH CALCULATION

COMMENT Read in simulation mesh
MESH IN.FILE=S1SM
LOAD IN.FILE=S1SS

COMMENT Create columnar format for all the temperatures
COMMENT Max temp points

EXTRACT NAME=toptub CONDITIO="@Y=0.4" EXPRESSI="max(@tl;@toptub)"
+PRINT
EXTRACT NAME=topox CONDITIO="@Y=2.05" EXPRESSI="max(@tl;@topox)"
+PRINT
EXTRACT NAME=topwaf CONDITIO="@Y=2.19" EXPRESSI="max(@tl;@topwaf)"
+PRINT
MODELS CONMOB CONSRH AUGER
SYMB CARRIERS=2 ILUCGS LAT.TEMP COUP.LAT
METHOD ILU.ITER=700 MAX.TEMP=200000

LOG OUT.FILE=151_HS_CBC8_time.tif TIF

SOLVE OUT.FILE=S1S100A01
SOLVE T(Emitter-h)=5200 T(Heat_sink)=300 TSTEP = 3.44E-14 TSTOP =
3.44E-14
SOLVE T(Emitter-h)=5200 T(Heat_sink)=300 TSTEP = 4.65E-14 TSTOP =
4.65E-14
SOLVE T(Emitter-h)=5200 T(Heat_sink)=300 TSTEP = 5.68E-14 TSTOP =
5.68E-14
PRINT TEMPERAT

SAVE OUT.FILE=151_HS_CBC8_time.tdf TDF

```

APPENDIX D

WATERLOO SPREADING RESISTANCE

University of Waterloo provides an application can calculate two- and three-dimensional thermal spreading resistance for isoflux rectangular and strip sources on a rectangular disk, a semi-infinite rectangular cylinder or a half space, two-layer system with different thicknesses and thermal conductivities, and an isotropic medium with constant properties. For the finite problem a uniform heat transfer coefficient boundary condition is applied to the lower surface. The general expression with dependance on several dimensionless geometric and thermal parameters, for the spreading resistance of an isoflux, rectangular heat source on a two-layer rectangular isofux channel with convective or conductive cooling at one boundary is being used. The effect of heat distribution over strip sources on two-dimensional spreading resistances is discussed. [39]

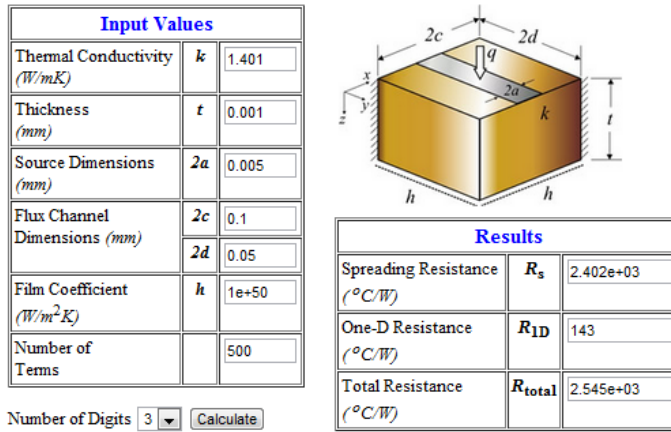


Figure D.1 Strip simulation from [12]

APPENDIX E

HEAT SOURCE PROPERTY USING THERMAL ELECTRODE IN TCAD

For simulation in TCAD to obtain transient analysis for thermal impedance it is necessary to use thermal electrode as heat source. When heat is dissipated in the device where heat is power in electrical analogy term, it is necessary for all the power to be consumed at the heat source. If a very high thermal resistive material is used, meaning a high resistance, almost all the power would get dissipated within the resistive material [38]. To have uniform heat flow on the surface, the high resistive material is wrapped around a very high conductive material.

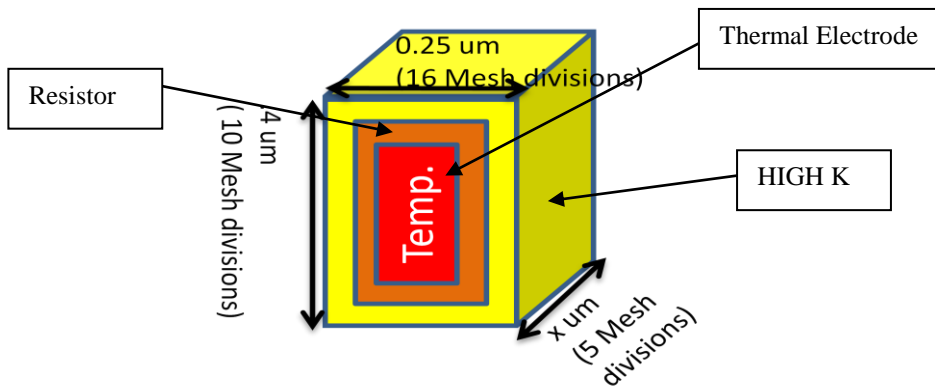


Figure E.1 Heater Structure using thermal electrode.

Table E.1 Material Properties in Heat structure

	Units	High K	Resistor
λ	$\text{WK}^{-1} \text{cm}^{-1}$	1E+08	5E-05
c	$\text{J Kg}^{-1} \text{K}^{-1}$	1E-08	1E-08

APPENDIX F

APPROXIMATION OF 2-POLE MODEL TO 1-ELEMENT MODEL

In the HICUM and METRAM model file, the thermal network is a 1-pole circuit. Since a multi-pole circuit is used to match the measured result, it is necessary to find a process of converting a multi-pole circuit to 1-pole circuit. In this section, a mathematical approach is explained to convert a 2-pole circuit to 1-pole circuit. Similarly, a 3-pole circuit can be converted to 2-pole circuit and then to 1-pole circuit. It is necessary that the approximated 1-pole circuit has the same starting and settling dc value and also crosses the 1/e load line.

Two scenarios are considered to convert a 2-pole to a 1-pole circuit. The first scenario is when the two poles are very close to each other.

Taking into this consideration the following equation

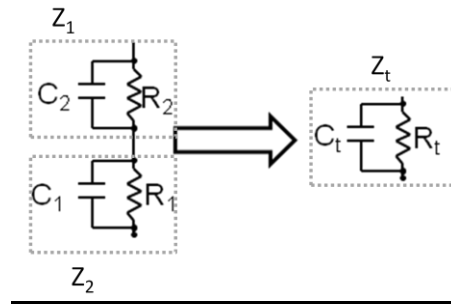


Figure F.1 The conversion of 2 pole to 1 pole.

$$Z_t(s) = Z_1(s) + Z_2(s) = \frac{R_1}{1 + sR_1C_1} + \frac{R_2}{1 + sR_2C_2} \quad (F.1)$$

Let $a = R_1C_1$ and $b = R_2C_2$ and let Z represent the impedance of the networks respectively.

Then,

$$Z_t(s) = \frac{R_1}{1 + sa} + \frac{R_2}{1 + sb} \quad (F.2)$$

$$= \exp(-t) \left[\left(\left(R_1/a \right) \times \exp\left(\frac{1}{a}\right) \right) + \left(\left(R_2/b \right) \times \exp\left(\frac{1}{b}\right) \right) \right] \quad (\text{F.3})$$

If $a \approx b$, then

$$Z_t(t) = \frac{\left(R_1/a \right) + \left(R_2/b \right)}{s + (1/b)} = \frac{R_t}{1 + sR_t C_t} \quad (\text{F.4})$$

Therefore, if $R_t = b \times \left[\left(R_1/a \right) + \left(R_2/b \right) \right] = R_1 + R_2$

Then

$$b = R_t C_t$$

So
$$C_t = \frac{\left[\frac{R_t}{\left(R_1/a \right) + \left(R_2/b \right)} \right]}{R_t} = \left[\frac{1}{\left(R_1/a \right) + \left(R_2/b \right)} \right] \quad (\text{F.5})$$

The load line is the 3dB point or the 1/e ratio of the two pole model. Now, if the horizontal solid line lies in the shaded region of the diagram then, ω_z is approximately equal to ω_1 [6] represented. If the 1/e or 3dB line (horizontal solid line) is in the shaded region as represented, ω_z is equal to ω_{z1} . Finally if the 1/e or the 3dB line is very near the bottom of the impedance axis it is assumed that ω_z is equal to ω_2 .

$$Z_t(s) = Z_1(s) + Z_2(s) = \frac{R_1}{1 + sR_1 C_1} + \frac{R_2}{1 + sR_2 C_2} \quad (\text{F.6})$$

$$Z_T = \frac{(R_1 + R_2) \left(1 + s \frac{C_1 R_1 R_2 + C_2 R_1 R_2}{R_1 + R_2} \right)}{(1 + sR_1 C_1)(1 + sR_2 C_2)} \quad (\text{F.7})$$

The one pole model is


```

z=1/((R1*C1*R2+R2*C2*R1)./(R1+R2));

p1=1/(R1*C1);
p2=1/(R2*C2);

%The representation for the 2-pole circuit

for k=1:length(w)

    ZTH(k)=(R1./(1+j*w(k)/p1))+(R2/(1+j*w(k)/p2));

    mag(k)=abs(ZTH(k));

    phase(k)=angle(ZTH(k));

end

%The conversion of 2-pole to one pole

for k=1:length(w)

    if (log10(R1+R2)< log10((R1+R2)/2)<log10(R2))

        pz=p1;

    elseif (log10(R2)> log10((R1+R2)/2)>0.000001*log10(R2))

        pz = (C2.*R2.*R2)./(R1+R2)

    else

        pz=p2;

    end

    ZTHq(k) = K./(1+j*w(k)/pz);

    magz(k)=abs(ZTHq(k));

    phasez(k)=angle(ZTHq(k));

end

% Values of the single pole model

R3=R1+R2;

C3=R3/pz

```

```
subplot(2,2,1), semilogx(w/(2*pi),20*log10(mag))
xlabel('Frequency,Hz'),ylabel('Impedance,dB')
grid
title('2 pole circuit')
subplot(2,2,2), semilogx(w/(2*pi),phase)
grid
xlabel('Frequency,Hz'), ylabel('Phase,deg')
subplot(2,2,3), semilogx(w/(2*pi),20*log10(magz))
grid
xlabel('Frequency,Hz'),ylabel('Impedance,dB')
title('Single pole Circuit')
subplot(2,2,4), semilogx(w/(2*pi),phasez)
xlabel('Frequency,Hz'), ylabel('Phase,deg')
grid
```

APPENDIX G

TEMPERATURE NODE IN SPECTRE

In this Section the procedure to add the dt and tl node to Spectre has been described.

Adding of the thermal pin in spectreS.

1. Copy the NPN cell-view to your new library.
2. Open the 'Symbol' of the copied NPN

Add pins 'dt', 'tl' and 'S'.

- a. Direction -> 'input-output', type-> 'square'
 - b. Add label cdsTerm("dt"), cdsTerm("tl") and cdsTerm("C")
 - c. Save
3. Next go to [Design -> Create Cellview From Pin List] and specify the IO pins 'C B E S dt tl', change the view name to 'spectreS' and choose the Tool/Data Type to 'Composer Symbol'. Then click on Ok.
 4. Next go to [Design -> Create Cellview From Cellview].

- a. Specify view name -> spectreS
- b. View name -> spectreS
- c. Tool/Data type - 'Composer Symbol'

A modify/replace window should pop up and check on modify.

The SpectreS window should pop up and it would contain the additional pins.

Save

5. Go to Tools at the icfb window menu and open up CDF and click on edit.
 - a. CDF type -> base
 - b. Add the appropriate library and cell name of the copied npn
 - c. Go to the simulation into field and click edit
 - i. Choose simulator to be 'spectreS'
 - ii. Change the 'termOrder' field to 'C B E S dt tl'
 - iii. netlistProcedure -> 'ansSpectreSDevPrim'

- iv. prefix -> 'Q'
- d. Go to the Overall Component Parameter section
 - i. modelType – VBIC
 - ii. Choose file name example ' N15W0402A1'
 - iii. Change the simModel to appropriate name example
' N15W0402A1VH' (for vbic models the file should end with VH)
- e. Click on OK

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BIOGRAPHICAL INFORMATION

Ardasheir Sayek Rahman received his Bachelor of Science degree in Electrical & Electronic Engineering from Michigan Technological University. His undergraduate research was based on the fading effect of monticarlo area scene for mobile vehicles. After finishing his bachelor's degree he started his graduate studies at The University of Texas at Arlington, Texas, United States of America in spring 2006. He started his research in the Analog Integrated Circuits Design Research Laboratory under the guidance of Dr. Ronald L. Carter in 2006. His research interest focuses on the analog circuit design and the thermal effect modeling and characterization. He worked as a graduate research assistant and graduate teaching assistant at UTA from spring 2006 to spring 2008. He has worked at Maxim Inc as an analog design engineer. He join Phd program under Dr. Ron Carter supervising in spring of 2009 where he concentrated on TCAD simulation and characterization of HBT devices.