MITIGATION OF HOT-SPOTS IN HIGH-END MICROPROCESSORS USING BULK AND THIN FILM THERMOELECTRIC COOLERS

by

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Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE IN MECHANICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

December 2012

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ACKNOWLEDGEMENTS

First of all, I would like to express my sincere gratitude to my advisor Dr. Dereje Agonafer for the continuous support of my Master study and research, for his patience, motivation, enthusiasm, and immense knowledge. His guidance helped me in all the time of research and writing of this thesis. I would even like to thank him for encouraging me and giving an opportunity to participate, publish and present conference paper in ASME International Mechanical Engineering Congress and Exposition, November 09-15, 2012, Houston, Texas, USA. Also I would like to thank him for EMNCPC Scholarship. I could not have imagined having a better advisor and mentor for my Master study.

Besides my advisor, I would like to thank the rest of my thesis committee: Dr. A. Haji-Sheikh and Dr. Seiichi Nomura, for their encouragement, insightful comments, and hard questions.

From the day I joined Electronics MEMS Nano-electronics Systems Packaging Center (EMNSPC) Ms. Sally Thompson has so helpful basically regarding the official work. I thank to all the members of EMNSPC Lab especially Thiagarajan Raman and Betsegaw Gebrehiwot for their help when I came across the problems during my research and for making the Lab a fun place to work. I will always remember EMNSPC team for making EMNSPC Lab more like a home to me.

Finally, I take this opportunity to express the profound gratitude from my deep heart to my beloved parents Mr. Somal Hirachan and Ms. Seema Hirachan, grandparents, and my siblings for their love and continuous support – both spiritually and materially. I would also like to thank someone special for loving and understanding me; it's my fiancé Binu Pannachan. I would even like to thank my sano buwa and sani aama Mr. Deepak Hirachan and Ms. Tara Hirachan for supporting me and motivating me in my studies. I would like to thank my brother

Preyesh Hirachan for always being there for me. To those who indirectly contributed in this research, your kindness means a lot to me. Thank you very much.

November 7, 2012

ABSTRACT

MITIGATION OF HOT-SPOTS IN HIGH-END MICROPROCESSORS
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COOLERS

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Due to localized high heat fluxes, hot-spots are created in silicon chips. Cooling of the hot-spots is one of the major thermal challenges in today's integrated circuit (IC) industry. Many researches have been conducted to find ways to cool hot-spots using different techniques as uniform heating is highly desired.

First part of the thesis focuses on cooling of hot-spot using conventional thermoelectric cooler (Melcor_CP1.0-31-05L.1) and a micro heat pipe. A chip package with conventional integrated heat spreader and heat sink was designed. Hot-spot was created at the center of the silicon die with background heat at rest of the area. The heat flux on the hot-spot was much greater than rest of the area. Forced convection was used to cool IC package, temperature was observed at active side of the silicon die. After that a copper conductor was used to take away heat directly from the hot-spot of the silicon die to the other end of the conductor which was cooled using the thermoelectric cooler. Finally the conductor was replaced by a heat pipe and comparison between three cases was done to study the cooling performance using the CFD based commercial software, ANSYS Icepak. The effect of trench on silicon die was also studied.

Second part of the thesis deals with thermal and structural aspects of design when thin film thermoelectric cooler (TFTEC) was embedded in the flip chip package for hot spot removal. A full thermo-mechanical model of flip chip package, heat spreader, under fill, solder balls, substrate, copper pads, printed circuit board and heat sink was designed along with TFTEC. Background heat at bottom face of silicon die and hot spot at center of the silicon die was created which represents the heat generated by the transistors in the chip package. Modeling and finite element analysis was done using ANSYS Workbench. Maximum junction temperature in the die, shear stress in solder balls and copper pads, and normal stress in the die of conventional flip chip package was compared with flip chip with TFTEC embedded in integrated heat spreader and flip chip package with TFTEC embedded in the silicon die for hot spot removal.

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NOMENCLATURE

TEC	thermoelectric cooler
CFD	computational fluid dynamics
FEA	finite element analysis
IHS	integrated heat spreader
TIM	thermal interface material
INS	insulator
HS	hot-spot
HSK	heat sink
MPH	micro heat pipe
K	thermal conductivity [W/mK]
B.C	boundary conditions
E	young's modulus of elasticity (GPa)
CTE	coefficient of thermal expansion
υ	Poisson's ratio
FC	flip chip
BGA	ball grid array
PCB	printed circuit board

CHAPTER 1

INTRODUCTION

1.1 Description of Hot-Spots Problem and Motivation

In 1965 co-founder of Intel, Gordon Moore, observed that the number of transistors per square inch on integrated circuits had doubled every year since the integrated circuit was invented. Moore predicted that this trend would continue for the foreseeable future. In subsequent years, the pace slowed down a bit, but data density has doubled approximately every 18 months. According to Moore's Law the number of transistor on integrated circuits will double roughly every 18 months. Most experts, including Moore himself, expect Moore's Law to hold for at least another two decades [1]. As shown in Figure 1.1, illustrates projected logarithmic increases in on-chip transistor density and logarithmic decreases in feature size over the next ten years, while chip size is expected to remain unchanged [2].

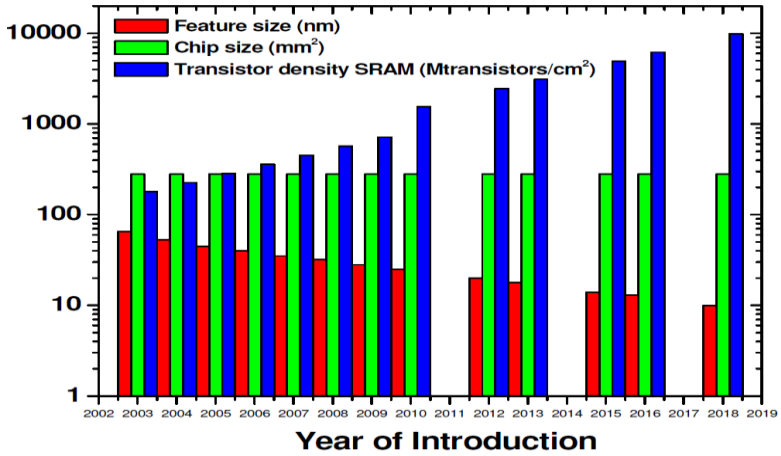


Figure 1.1 ITRS predictions of feature size, chip size and transistor density for high performance microprocessor chips, 2005 [2]

Shrinking feature size and increasing transistor density, and faster circuit speed is leading to higher power chip dissipation and high heat flux [3]. Roadmap projections for the high-performance chip shows that maximum chip power dissipation will exceed 300W and the maximum chip heat flux will exceed 150 W/cm^2 with in next few years [4]. The increase in performance demands have resulted in greater non-uniformity of on-chip power dissipation, creating localized hot-spots [4]. It is expected that the heat flux emerging form hot-spot in the next generation microprocessor may exceed 1000W/cm^2, six times more than an average heat flux in die, with temperature of around 30°C more than an average die temperature [3]. This excess heat from the high-heat-flux hot-spot may result in decrease in the operational speed by some 10%-15% and chip may experience an accelerated failure rate [3].

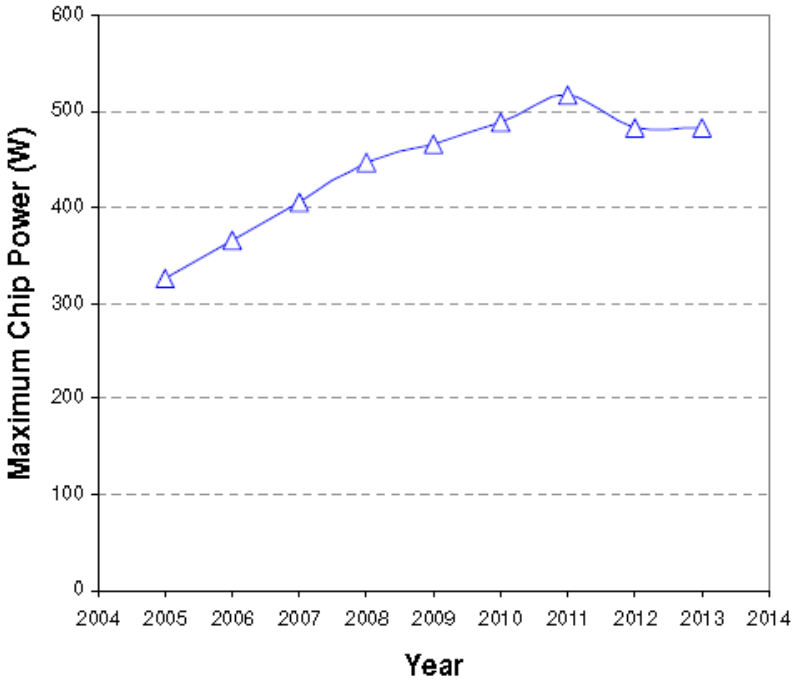


Figure 1.2 iNEMI road map for chip power in high performance servers, 2006 [5]

The major goal of thermal management in electronic packaging is to transfer the heat generated by the IC from the chip to the ambient environment to keep the junction temperature

(highest temperature on the active side of the silicon die) below the acceptable limit. Due to the localized high heat flux or hot spot in the silicon die, it limits the IC's performance, reliability and yield, which are very sensitive to small changes in temperatures. In IC industry now hot spot is one of the biggest and growing problems including the variety of devices like microprocessors, graphics processors, ASICs and other high-performance CMOS ICs. Due to placing of transistors in close proximity in order to reduce "time of flight" delays within a single functional block, in most of the electronic devices hot spots are generally created by the performance-sensitive circuits as power is dissipated by both transistors and interconnect. Some of the examples can be placement of core processors in close proximity with cache memory. Core processors dissipates significant amount of heat while the cache memory dissipates little heat. Other examples of hot spots in ICs can are clock generators or analog channels operating at gigabit per second speeds. In some CMOS processors1 cooling these hot spots could produce speed gains of 30-200% [24].

Figure 1.3 shows the heat flux variation in silicon die due to uneven distribution of power. Examples of on-chip hot spots are shown in Figure 1.4 and 1.5. Figure 1.4 shows two different Intel chips containing hot spot regions [7] and figure 1.5 shows a typical on-chip heat flux map with accompanying temperature map [8].

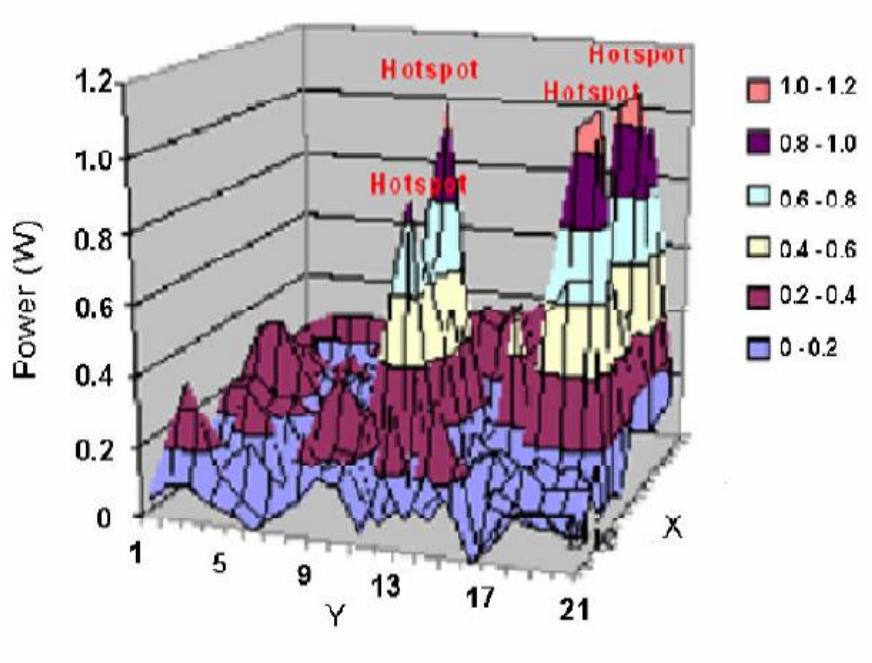


Figure 1.3 Typical heat flux map [6]

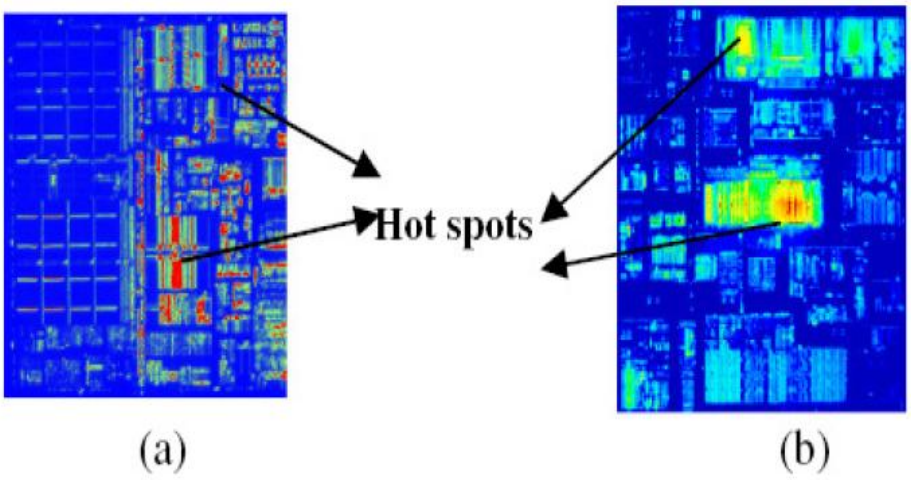


Figure 1.4 (a) Hot spots resulting from non-uniform power on an Intel Pentium ® III processor and (b) Intel Itanium ® processor [7]

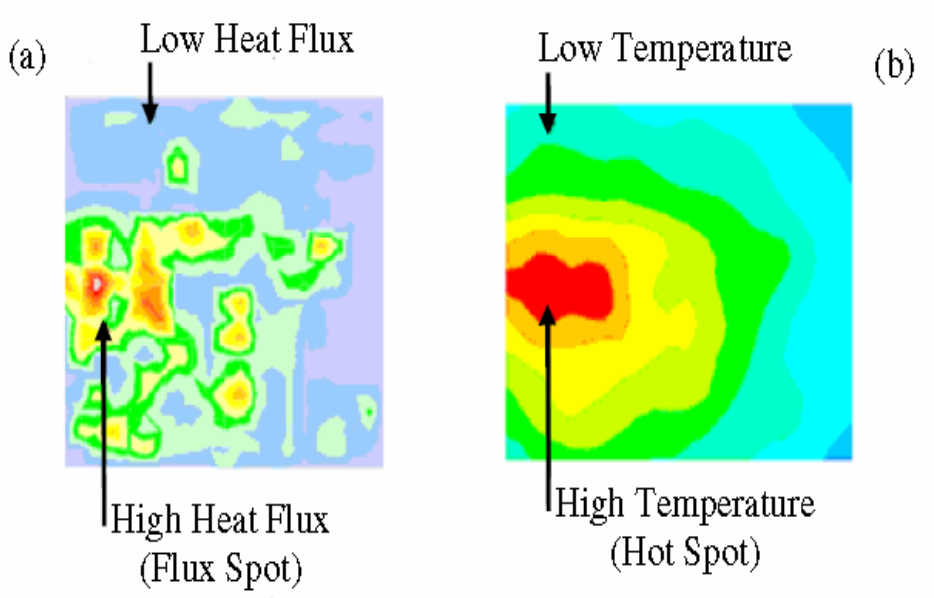


Figure 1.5 (a) Typical die power map and (b) hot spot on the corresponding temperature map [8]

Various system level cooling techniques like air cooling, hybrid cooling, or refrigeration cooling are used for electronic cooling applications, but those techniques are not focused of the cooling of local high heat flux due to hot spot [4]. These cooling techniques result in unnecessary overcooling of large areas of chip [1]. Hence, cooling of hot spots rather than lowering the average die temperature is becoming focus of current thermal design.

1.2 Cooling Techniques in Electronic Packaging

The cooling techniques in electronic packaging can be classified into two categories. The first one is passive cooling techniques and the second one is active cooling techniques.

1.2.1 Passive cooling techniques

Passive cooling techniques are widely used for thermal management in electronic packaging in today's integrated circuit (IC) industries. In passive cooling techniques there are no moving parts and does not require external power supply. The method generally used for passive cooling is conduction, spreading of heat and natural convection [10]. Highly conducting

metals like aluminum and copper are used widely in electronic packaging application to take away the heat from the electronic packaging. Though diamond has high thermal conductivity of around 2300W/mK due to its high price and difficulty in attaching to electronics it is not used in electronic packaging application [9]. The research in passive cooling generally focuses on engineering high thermal conductivity materials and low thermal resistances interfaces [10]. Advantages of passive cooling are low cost, low complexity and high reliability (no moving parts) [9, 10]. While the disadvantages include low heat removal, bulkiness and inability to cool below sub ambient temperatures [10]. The other disadvantages of passive cooling include limited heat removal capacity compared to hot spot heat fluxes and to active techniques [9].

1.2.2 Active cooling techniques

Active cooling techniques contain moving parts and it even requires electrical power supply or external energy. Active cooling techniques are more expensive compared to passive cooling techniques as heat is pumped from heat source to heat sink [9, 10]. Heat sink coupled with fan is one of the most common active cooling techniques which increase the overall heat transfer coefficient [9].But forced convection techniques which uses heat sink coupled with fan cannot be used to cool the hot-spots which is created in the electronic packaging. The other active cooling techniques involve micro-channel heat sinks, jet impingement cooling and even thermoelectric coolers or TEC. Micro-channel heat sinks and jet impingement cooling techniques uses fluid to remove heat from the electronics [9, 10].

Water is good liquid to remove high heat flux in electronic packaging due to its properties like high thermal conductivity, high density, high specific heat and low viscosity. Although water can remove large amount of heat but as it is also a good conductor of electricity so it cannot be used in contact with the electronics. In order to eliminate the contact of water with electronics, water is generally enclosed in copper or aluminum plates placed inside the electronics with several layers of contact resistance in thermal stack. These contact resistance degrades the cooling performance, so thermally conductive and electrically resistive dielectric

fluids are used to eliminate these contact resistance from the electronics. Since dielectric fluid has low thermal conductivity, both water and dielectric fluid are almost the same from performance point of view. In order to increase the cooling performance of the liquid used in electronic packaging the liquid can be pressurized and boiled which increases the heat transfer coefficient but it requires large system to operate. Since many components must work in conjunction to remove heat for electronics, due to large thermal solution volume reliability becomes the major concern [9]. TEC can be used directly or indirectly for the hot-spot cooling in electronic packaging application. Both conventional bulk TEC and thin film TEC can be used for hot-spot cooling in the electronic packaging application. Micro TEC is generally embedded inside the integrated heat spreader or silicon die itself for hot-spot cooling. In this study conventional bulk TEC along with micro heat pipe was used for hot-spot cooling in high power device.

CHAPTER 2

THERMOELECTRIC COOLER

2.1 Historical Background of Thermoelectric Cooler

The physical principle of the modern thermoelectric modules was basically discovered in 1800s although it was commercially available only after 1960. In 1821 the German scientist Thomas Seebeck discovered that when two junctions of different current carrying conductor are maintained at different temperatures than current flows through a closed circuit of the conductor. In 1834 a French watchmaker and part-time physicist, Jean Peltier while investigating the Seebeck Effect, found that the opposite phenomenon when the current is passed through the closed circuit of two different conductors then heat is absorbed in one junction and rejected at the other one. Twenty years later, William Thomson (known as Lord Kelvin) described the relationship between Seebeck and Peltier Effects and even explained it in a better way but still the phenomenon had no practical application.

In the 1930s, Russian scientists started studying about the earlier thermoelectric work in an effort to construct power generators for the use of remote locations throughout the country. Eventually the interest of thermoelectricity caught rest of the world and inspired in the development of thermoelectric modules. Today's thermoelectric module uses a modern semiconductor technology in with a doped semiconductor material instead an electric conductor. Thermoelectric works on various principles like Seebeck, Peltier and Thomson effects along with several other phenomenon.

2.2 Introduction to Thermoelectric Cooler

Thermoelectric coolers (TEC) are the solid-state heat pump which uses Peltier effect to transport heat from one side of the device to the other side, with the consumption of electric current. The hot and cold side of the device depends on the direction of the current applied.

Thermoelectric cooler is composed of two types of material one is positively charged p-type of semi-conductor which is deficiency of electrons, while the other is negatively charged n-type semi-conductor having excess of electrons. These p-type and n-type semiconductor are heavily doped with electrical carriers. One p-type semi-conductor and one n-type semiconductor are connected electrically by an electric conductor to make a pair of thermoelectric pallet. These elements are arranged into array which is electrically connected in series but thermally connected in parallel.

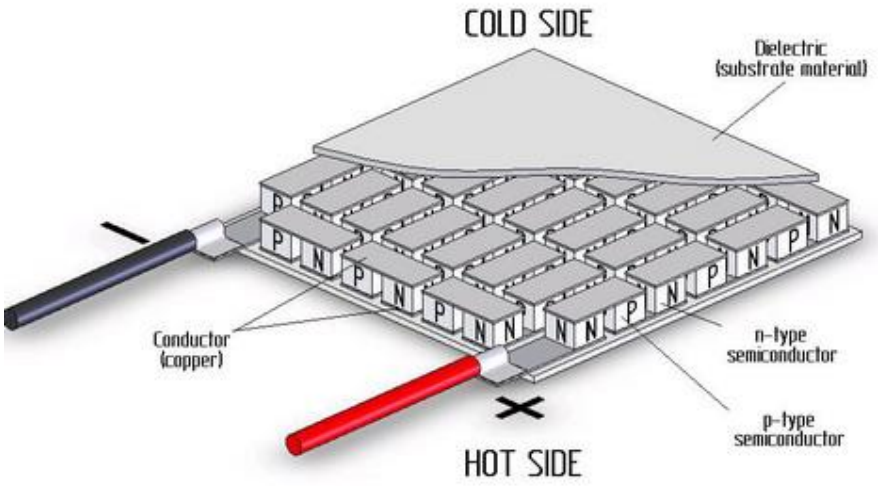


Figure 2.1 Bi-Te single-stage thermoelectric cooler

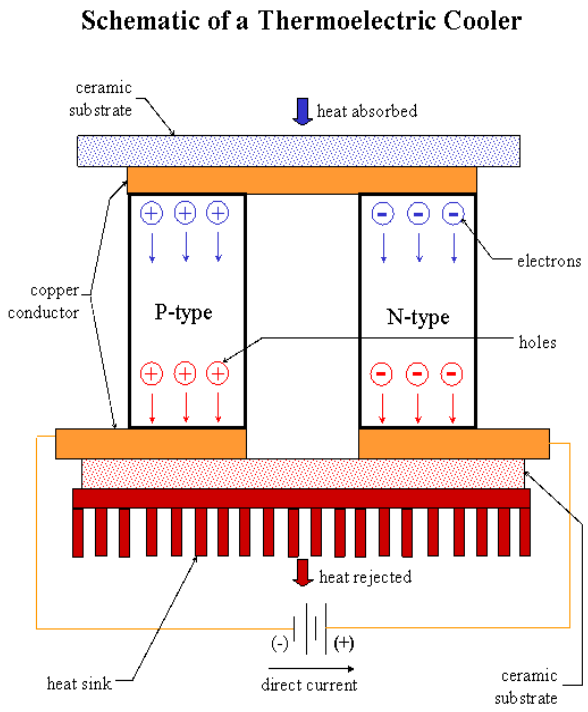


Figure 2.2 Thermoelectric cooler operating principles [11]

The p-type semiconductor is doped with atoms that has less electrons than necessary to complete the atomic bond in crystal lattice whereas the n-type semiconductor is doped with atoms that has more electrons than necessary to complete the atomic bond with in the crystal lattice. When the direct current or voltage is applied the conduction of electrons takes place in p-type semiconductor and extra electrons move to the conduction band from n-type semiconductor to complete the atomic bond. In the p-type semiconductor due to conduction of electrons, the electrons leaves the holes (atoms within the crystal lattice that now have local positive charges), the electron leaving one hole enters the next available hole, so the process of electrons entering and leaving the hole continuous. Finally when the electrons leaves the p-type semiconductor and enters the electrical conductor on the cold side of TEC, this electrons jumps out to a higher energy level to match a higher energy level of electrons already moving in the electric conductor. These additional electrons from cold side of electrical conductor enter into

the n-type of semiconductor. Both to create holes in p-type semiconductor and match the energy level of incoming electrons in n-type semiconductor, additional energy are required. This extra energy comes by absorbing heat from the colder side of TEC. The newly created holes in p-type semiconductor and electrons in n-type of semiconductor travel towards the hot-side of TEC. Electrons from hot-side of electrical conductor moves into p-type semiconductor and the drop into holes, releasing excess energy in the form of heat whereas when the electrons leaves n-type semiconductor and enters the electrical conductor they fall down to lower energy level releasing heat [11].

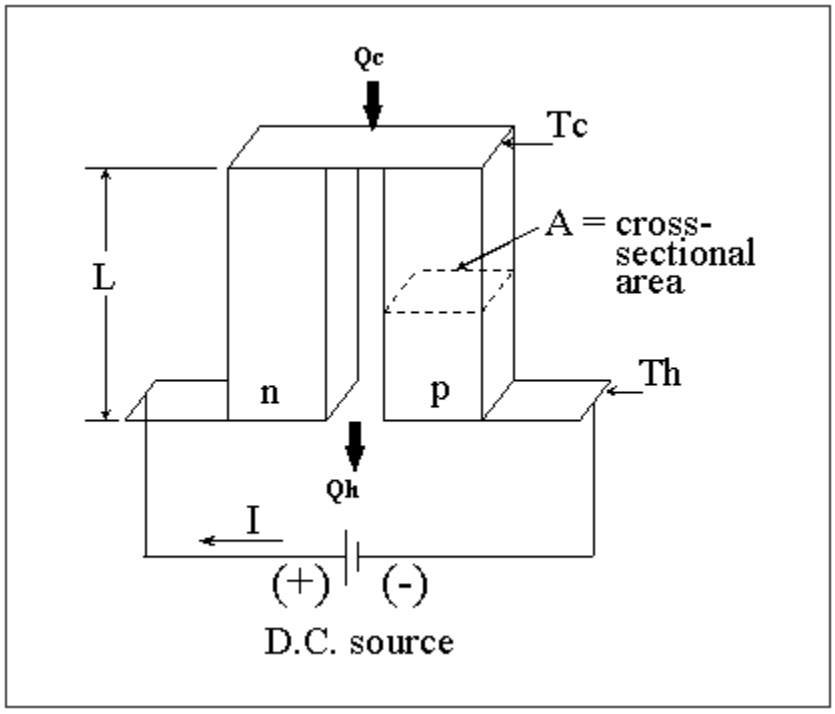


Figure 2.3 Thermoelectric couple [11]

The mathematical equation governing the operating principle of thermoelectric cooler are

$$Q_c = 2N\left[\propto IT_c - \frac{1}{2}\rho I^2\frac{L}{A} - K\frac{A}{L}(T_h - T_c)\right] \quad 2.1$$

$$V = 2N\left[\propto (T_h - T_c) + \rho I\frac{L}{A}\right] \qquad 2.2$$

Where,

L = element height or length

A = cross-sectional area

Q_c = heat load

T_c = cold-side temperature

T_h = hot-side temperature

I = applied current

Additionally,

α = Seebeck coefficient

ρ = electrical resistivity

K = thermal conductivity

V = voltage

N = number of couples

At the right hand side of equation 2.1, the first term $\propto IT_c$ is Peltier cooling effect. The second term $\frac{1}{2}\rho I^2\frac{L}{A}$ represents the Joule heating effect. The Joule heating is associated due to passage of electrical current, so 1/2 the heat goes towards the cold side and 1/2 the heat goes towards the hot side. The last term $K\frac{A}{L}(T_h - T_c)$ represents the Fourier effect in which heat conducts from a higher temperature to lower temperature. So the cooling at the cold side of TEC due to Peilter effect is reduced nu the loss associated with electrical resistance and thermal conduction [11].

At the right hand side of equation 2.2, the first term, $\propto (T_h - T_c)$ represents the Seebeck voltage. The second term $\rho I\frac{L}{A}$ represents the voltage related by Ohm's law [11].

2.3 Principles Theory of Thermoelectricity

The thermoelectric module works on three basic principles Seebeck effect, Peltier effect and Thomson effect. Beside this effect there are two more effects which impact the principal of thermoelectricity i.e Joule effect and Fourier effect.

2.3.1 Seebeck effect

Seebeck effect was discovered by Thomas Johann in the 1800s. The Seebeck effect is a phenomenon in which a temperature difference between two dissimilar electrical conductors or semiconductors produces a voltage difference between the two substances. The voltage developed over the loop can be measured by inserting a voltmeter into a loop, it is also known as thermocouple voltage. The voltage produced by Seebeck effect are small, numerous such devices are connected in series to increase the output voltage or in parallel to increase the maximum current.

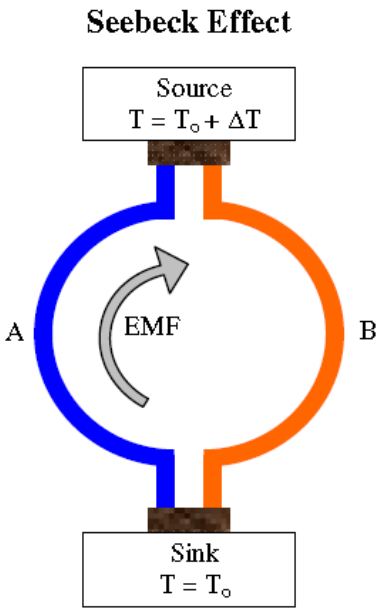


Figure 2.4 Conceptual schematic of the Seebeck effect for material A and B [10]

As shown in Figure 2.4 when two junction of a circuit composed of material A and B is maintained at different temperatures, where lower junction is kept a lower temperature and upper junction is kept at higher temperature, then voltage is induced in the circuit.

An electric potential develops at a junction formed by two dissimilar materials at different temperatures is given by

$$V = \propto (T_h - T_c) \quad 2.3$$

$$dV = \propto_{12} dT \quad 2.4$$

Where,

V = Seebek Voltage

α = Seebeck coefficient

T_h = Hot side temperature

T_c = Cold side temperature

Thus,$\propto_{12}$ can be either positive or negative. It is positive, if p-type of conductor is electrically positive with respect to n-type of semiconductor, when the thermocouple is open at cold junction [12].

Where,

$$\propto_{12} = \propto_1 - \propto_2 \quad 2.5$$

2.3.2 Peltier effect

Peltier effect was discovered by the French physicist Jean-Charles-Athanase Peltier in 1834. The Peltier effect is a phenomenon in which cooling of one junction and heating of another junction takes places when an electric current is passed circuit containing two dissimilar conductors or semiconductors.

As shown in Figure 2.5, when a current is made to flow through a junction composed of materials A and B, heat is generated at the lower junction, and absorbed at the upper junction.

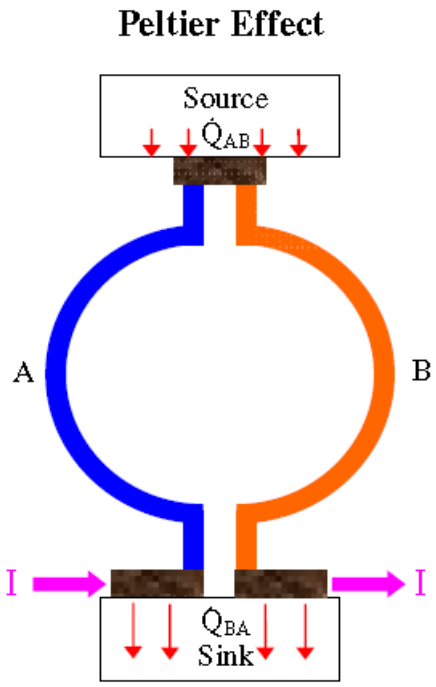


Figure 2.5 Conceptual schematic of the Peltier effect for material A and B [10]

The hot and cold side and the temperature gradient produced depend upon the direction and magnitude of the current. Thus the amount of heat pumped to thermoelectric is

$$q_p = \pi_{12} I \qquad 2.6$$

Where,

π_{12} = Peltier coefficient

I = current

The relationship between Seebeck effect and Peltier effect was given by William Thompson as

$$\pi = \alpha T \qquad 2.7$$

$$\therefore q_p = \alpha I T \qquad 2.8$$

2.3.3 Thomson effect

Thomson effect was discovered by William Thomson in 1854, later Lord Kelvin. Thomson effect is a phenomenon in which heat flows into or out of a conductor or semiconductor when an electric current flows in a conductor or semiconductor with two junction points kept at different temperatures, the direction of the heat flow depends upon the direction of the current in a conductor or semiconductor. Any temperature gradient previously existing will be changed by an application of a current. The heat is expressed as

$$q_T = \zeta I \frac{dT}{dx} \tag{2.9}$$

Where, ζ is a Thomson effect

2.3.4 Joules effect

Joule effect was first studied by James Prescott Joule in 1841. Joule heating is a phenomenon in which the passage of electric current through the conductor or semiconductor releases the heat. The heat generated due to Joules effect is equal to the product of square of current in an electrical conductor or semiconductor and the electrical resistance of conductor or semiconductor in which the current is passed. It is given by

$$q_J = I^2 R \tag{2.10}$$

Where, R is the resistance and I is the current

2.3.5 Fourier effect

Fourier effect or Fourier conduction states that the rate of heat flow through a homogenous solid is directly proportional to the area of cross-section at right angles to the direction of heat flow and to the temperature difference along the path of the heat flow. Due to Fourier effect heat from the hot side of the TEC flows towards the colder side of, reducing the cooling performance of the TEC. The greater the temperature gradient between hotter and

colder sided of TEC the more heat is transferred form the hotter side towards the colder side. It is given by the equation

$$q_F = -KA\frac{dT}{dX} \tag{2.11}$$

Where,

q_F = rate of heat flow,

K = thermal conductivity

A = area of cross-section

X = conducting length

2.4 Thermoelectric Cooling Theory

The thermoelectric cooler consists of number thermoelectric pallet. Each thermoelectric pallet is made of branch of p-type and n-type semiconductor connected by an electric conductor. Thus heat transported from heat source to heat sink in each branch of semiconductor in a thermoelectric cooler is given by

$$q_p = \propto_p IT - K_p A_p \frac{dT}{dx} \tag{2.12}$$

$$q_n = \propto_n IT - K_n A_n \frac{dT}{dx} \tag{2.13}$$

Where,

q_p = heat transported by p-type semiconductor

q_n = heat transported by n-type semiconductor

$\propto_p$ = Seebeck coefficient of p-type semiconductor

$\propto_n$ = Seebeck coefficient of n-type semiconductor

K_p = thermal conductivity of p-type semiconductor

K_n = thermal conductivity of n-type semiconductor

A_p = cross section area of p-type semiconductor

A_n = cross section area of n-type semiconductor

T = absolute temperature

I = electric current

$\frac{dT}{dx}$ = temperature gradient

Also there is a heat generated in each branch of thermoelectric pallet due to Joule effect. Due to the heat generation there is a non-uniform temperature gradient in the thermoelectric pallet, which is given by

$$-K_p A_p \frac{d^2T}{dT^2} = \frac{I^2 \rho_p}{A_p} \qquad 2.14$$

$$-K_n A_n \frac{d^2T}{dT^2} = \frac{I^2 \rho_n}{A_n} \qquad 2.15$$

Where,

ρ_p = electrical resistivity for p-type semiconductor

ρ_n = electrical resistivity for n-type semiconductor

The term $\frac{I^2 \rho}{A}$ represents the Joule heating.

Assuming that Seebeck coefficient is independent of temperature, which leads to Thomson effect, is zero. Also setting the boundary condition at heat source as $T = T_1$ at $x = 0$ and at heat sink as $T = T_2$ at $x = L_p$ or L_n.

From equation 2.14 and 2.15 we get,

$$K_p A_p \frac{dT}{dx} = -\frac{I^2 \rho_p (x - L_p/2)}{A_p} + \frac{K_p A_p (T_2 - T_1)}{L_p} \qquad 2.16$$

$$K_n A_n \frac{dT}{dx} = -\frac{I^2 \rho_n (x - L_n/2)}{A_n} + \frac{K_n A_n (T_2 - T_1)}{L_n} \quad 2.17$$

Combining equation 2.12 and 2.16, rate of heat flow at $x = 0$ is

$$q_p(x = 0) = \alpha_p I T_1 - \frac{K_p A_p (T_2 - T_1)}{L_p} - \frac{I^2 \rho_p L_p}{2A_p} \quad 2.18$$

Now, combining equation 2.13 and 2.17, rate of heat flow at $x = 0$ is

$$q_n(x = 0) = \alpha_n I T_1 - \frac{K_n A_n (T_2 - T_1)}{L_n} - \frac{I^2 \rho_n L_n}{2A_n} \quad 2.19$$

Adding q_p and q_n at $x = 0$, from equation 2.18 and 2.19 net heat flow or total cooling power can be obtained as

$$q_C = (\alpha_p - \alpha_n) I T_1 - K(T_2 - T_1) - I^2 R/2 \quad 2.20$$

Where the thermal conduction of the two branches on parallel is

$$K = \frac{K_p A_p}{L_p} - \frac{K_n A_n}{L_n} \quad 2.21$$

The electrical resistance of two branches in series is

$$R = \frac{L_p \rho_p}{A_p} - \frac{L_n \rho_n}{A_n} \quad 2.22$$

2.5 Figure of Merit

The thermoelectric figure of merit (ZT) is a dimensionless parameter, which considers the usefulness and thermoelectric capacity of semiconductor being used in the thermoelectric device. The thermoelectric figure of merit Z is given by

$$Z = \frac{(\alpha_p - \alpha_n)^2}{(\sqrt{K_p \rho_p} + \sqrt{K_n \rho_n})^2} \quad 2.23$$

In equation 2.20 we can that Peltier cooling term $(\alpha_p - \alpha_n)IT_1$ varies linearly with electric current I, but the Joule heating term $I^2R/2$ varies with the square of current. So we can analyze that once we increase the current in the TEC there is cooling in one side of TEC due to Peltier cooling and the heat is supplied to the colder side of TEC due to Joule heating. With increase in current as Joule heating increases more compared to Peltier cooling, the cooling becomes ineffective after certain current $I_q$at which the cooling power reaches the maximum value. By setting the equation $dq_c/dI = 0$, we get

$$I_q = \frac{(\alpha_p - \alpha_n)T_1}{R} \tag{2.24}$$

The maximum cooling is than

$$(q_C)_{max} = \frac{(\alpha_p - \alpha_n)^2 {T_1}^2}{2R} - k(T_2 - T_1) \tag{2.25}$$

From equation 2.25 it can be observed that the cooling becomes ineffective if the temperature difference is high. So by setting $(q_C)_{max} = 0$ we get,

$$(T_2 - T_1)_{max} = \frac{(\alpha_p - \alpha_n)^2 {T_1}^2}{2RK} \tag{2.26}$$

Where, thermoelectric figure of merit is given by

$$Z = \frac{(\alpha_p - \alpha_n)^2}{2KR} \tag{2.27}$$

So equation 2.26 can be written as

$$(T_2 - T_1)_{max} = \frac{1}{2} Z T_1^{\ 2} \qquad 2.28$$

The material for the thermoelectric is selected with the help of thermoelectric figure of merit. The value of ZT has to be one or higher than one. Pure metal has low α which leads to low thermal conductivity. Where as in insulators electrical resistivity is low which leads to higher Joule heating. Values of K or ρ cannot be changed in metals or insulators so the value of thermoelectric figure of merit is always low. Where as in semiconductors the value of K or ρ can be adjusted individually by doping to match the requirements of TEC. Bi_2Te_3/Sb_2Te_3 combination of semiconductors is used commercially in present state as it has ZT value around 2.4 [12].

2.6 Coefficient of Performance

The performance of any refrigeration is usually assessed in terms of quantity known as coefficient of performance (COP). Coefficient of performance is the ratio of cooling power (q_c) to the rate of electric energy supplied (W).Which is given as

$$COP = \frac{q_c}{W} \qquad 2.29$$

Looking at the branches separately,

$$W_p = \alpha_p I(T_2 - T_1) + \frac{I^2 \rho_p L_p}{A_p} \qquad 2.30$$

$$W_n = -\alpha_n I(T_n - T_n) + \frac{I^2 \rho_n L_n}{A_n} \qquad 2.31$$

Both the Seebeck effect Joule effect will be overcome by the electrical power

$$W = (\alpha_p - \alpha_n) I(T_2 - T_1) + I^2 R \qquad 2.32$$

The coefficient of performance is

$$COP = \frac{q_c}{W} = \frac{(\alpha_p - \alpha_n)IT_1 - \frac{1}{2}I^2R - K(T_2 - T_1)}{(\alpha_p - \alpha_n)I(T_2 - T_1) + I^2R} \quad 2.33$$

By setting d(COP)/dI equals to zero, gives the optimum current which yields maximum COP.

$$I_{COP} = \frac{(\alpha_p - \alpha_n)(T_2 - T_1)}{R[(1 + ZT_M)^{1/2} - 1]} \quad 2.34$$

Where, T_M, equals to $(T_1+T_2)/2$, is the mean temperature

The corresponding coefficient of performance

$$COP_{max} = \frac{T_1[(1 + ZT_M)^{1/2} - T_2/T_1]}{(T_2 - T_1)[(1 + ZT_M)^{1/2} + 1]} \quad 2.35$$

COP for a single stage thermoelectric module basically lies between 0.3 and 0.7. The COP can be greater than 1.0 only when the module is pumping against the positive temperature gradient. The Figure 2.6 shows a normalized graph of COP versus I/I_{max}. Each line corresponds with a constant DT/DT_{max} [11]

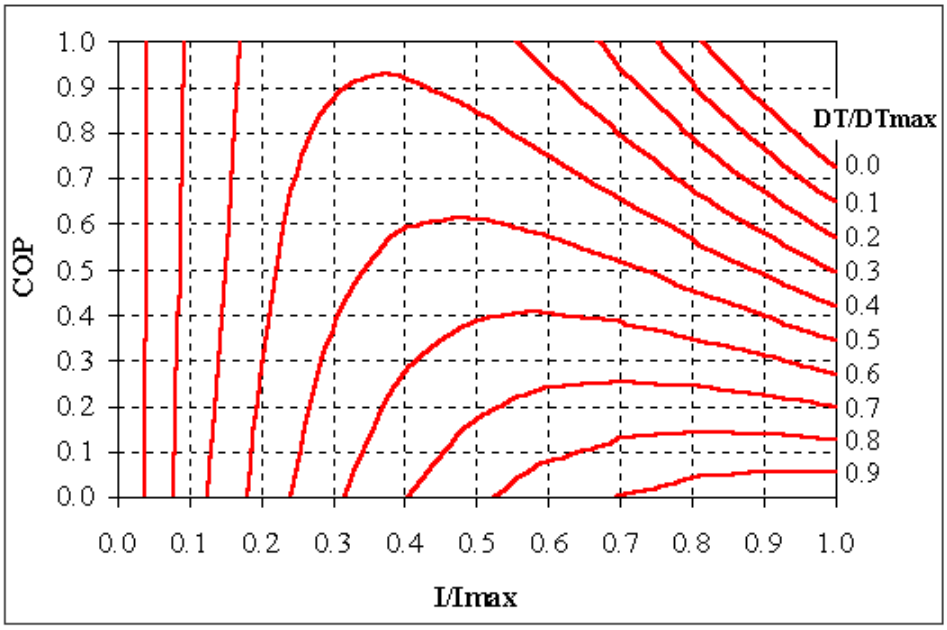


Figure 2.6 COP versus I/I_{max} [11]

Where,

I/I_{max} = ratio of input current to the module's I_{max} specification

DT/DT_{max} = ratio of the required temperature difference to the module's DT_{max} specification

The sample of thermoelectric performance curve shows the relationship between ΔT and other parameters.

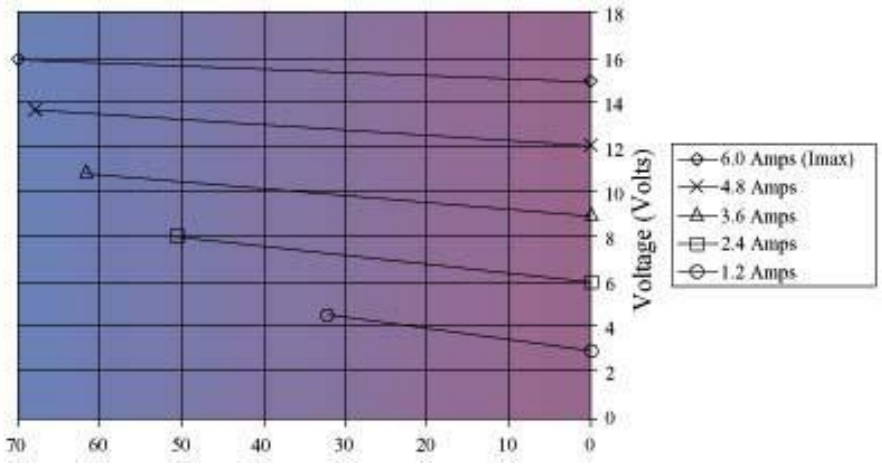


Figure 2.7 Performance curve (ΔT vs. Voltage) [33]

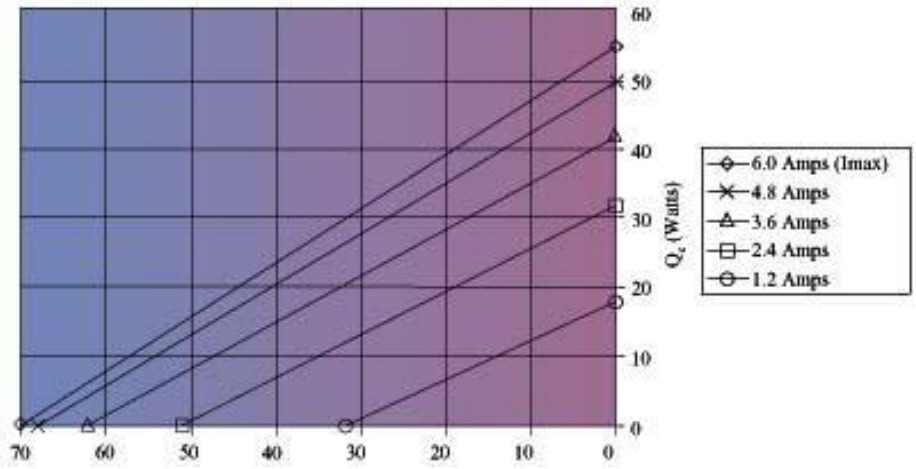


Figure 2.8 Performance curve (ΔT vs. Q_C) [33]

2.7 Others Factors of Thermoelectric Cooler

2.7.1 Reliability and mean time between failures

Due to the solid state construction thermoelectric coolers are highly reliable. Form the results of various test performed mean time between failures (MTBF) of thermoelectric cooler is between 200,000 to 300,000 hours at room temperature. MTBF of thermoelectric cooler at elevated temperature at 80 ^{o}C is reported to around 100,000 hours [33].

2.7.2 Moisture and vibration effect

2.7.2.1 Moisture

Thermoelectric material in thermoelectric module must be sealed and protected from the moisture. The presence of moisture will cause an electro-corrosion and will degrade thermoelectric materials, conductors and solders. Moisture can cause an electrical path to ground causing electric short or even hot side to cold side thermal short in a thermoelectric module. A proper sealing is required to protect thermoelectric elements form moisture in a thermoelectric module [33].

2.7.2.2 Shock and vibration

Thermoelectric devices have been successfully subjected to shock and vibration requirements of aircraft, ordinance, space vehicles, shipboard and various other such systems. Thermoelectric device is found to quite strong in tension and compression while it is found to be relatively weak in shear. To operate thermoelectric devices in sever shock or vibration environment, design of the assembly should be done with proper care to insure compressive loading of thermoelectric device [33].

2.8 Types of Thermoelectric Cooler

Thermoelectric cooler can be classified into two types the first one being the conventional thermoelectric cooler and second one thin film thermoelectric cooler

2.8.1 Conventional thermoelectric cooler

Conventional thermoelectric cooler also referred as bulk thermoelectric cooler because of their size and fabrication process. The Figure 2.9 shows the commercially available conventional thermoelectric cooler. Conventional thermoelectric coolers are made using the bulk technology. The large pellets are cut from boules of material; these modules are referred to as 'bulk' thermoelectric modules. Earlier in space cooling application conventional thermoelectric cooler was used. It can be even used for temperature control in instrumentation, telecommunications etc. [14].

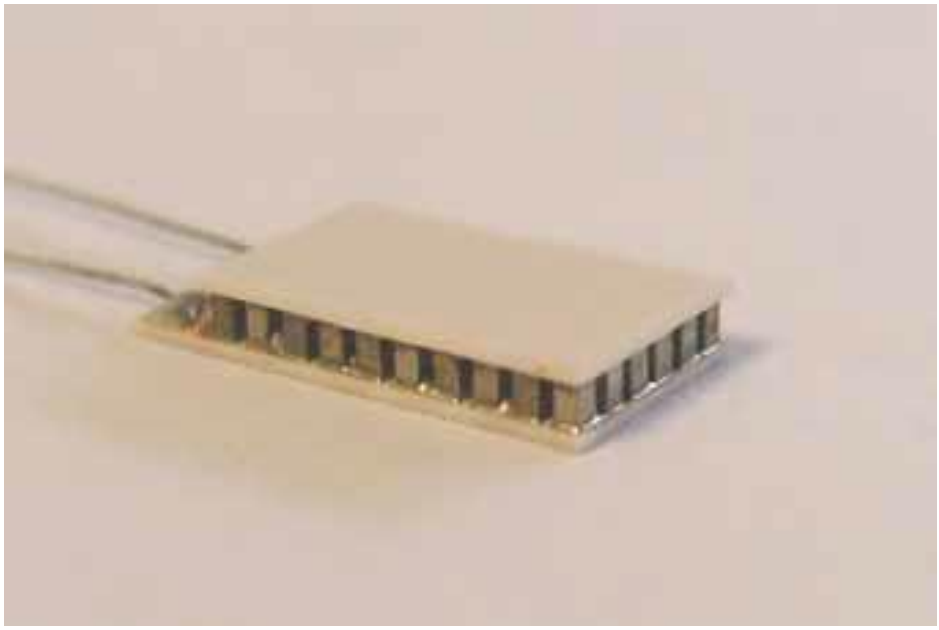


Figure 2.9 Standard, commercially available TEC. The size of the device is 6.2 mm x 10.3 mm x 1.8 mm [14]

2.8.2 Thin-film thermoelectric cooler

Materials for thin-film thermoelectric materials can be grown by conventional semiconductor deposition methods, and devices can be fabricated using conventional semiconductor micro-fabrication techniques. Thin film thermoelectric cooler has high flux cooling abilities resulting from the low leg heights [14]. Generally thermoelectric materials for TFTEC are made by tellurium for p type Sb_2Te_3 films and bismuth and tellurium for n type Bi_2Te_3 films. Various techniques like co-evaporation, co-sputtering, and electrochemical deposition are used to deposit bismuth telluride-based material. The Figure 2.10 show the thin film thermoelectric cooler embedded in the integrated heat spreader.

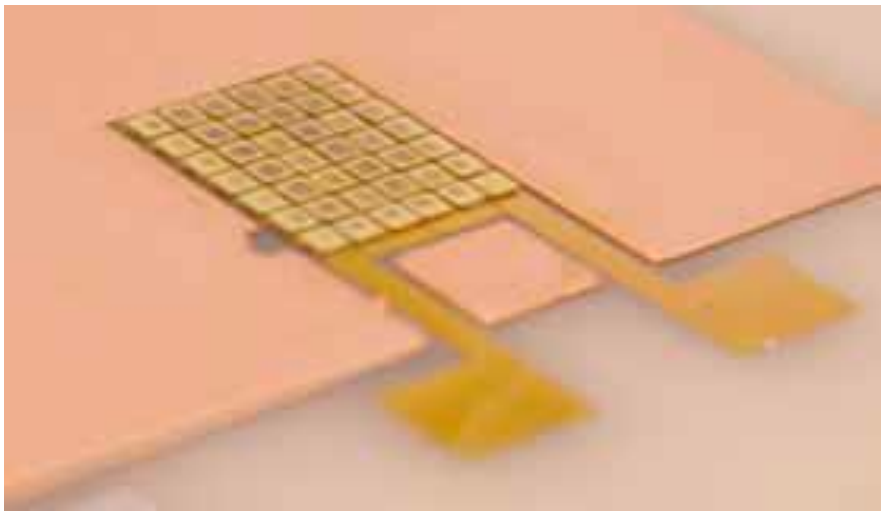


Figure 2.10 Thin film thermoelectric modules available from Nextreme. This device is 3.5 mm x 3.0 mm x 0.1 mm in size. Devices as small as 0.3 mm x 0.3 mm x 0.1 mm are feasible [14]

2.9 Advantages and Disadvantages of Thermoelectric Cooler

2.9.1 Advantages of thermoelectric cooler

- TECs can be used for hot spot cooling in electronic packaging
- Thermoelectric cooler can be used to cool below ambient temperature
- TEC gives precise temperature control in electronic packaging
- There are no moving parts in TEC, so no mechanical wear and tear and maintenance free
- Can be used for space application in zero gravity or in any orientation
- TECs are small in size and weight and are highly reliable
- Can be used as both heater and cooler just by changing the direction of the current
- Environment friendly and no chemicals or CFC used

2.9.2 Disadvantages of thermoelectric cooler

- Efficiency is very less
- Material degrades on the cold side due to moisture due to moisture
- Mechanical loadings like shock and vibrations can damage the TEC

CHAPTER 3

HEAT PIPE

3.1 Introduction to Heat Pipe

The idea of heat pipe was first suggested by R.S.Gaugler in 1942, but in 1962 it was invented 1962 by G.M. Gtover after that heat pipe got due appreciation due to its remarkable properties. A heat pipe is a device that can transfer large amount of heat from point to another with almost no loss of heat. Heat pipe combines the principles of both thermal conductivity and phase transition to efficiently transfer heat between two points.

Heat pipe for electronic packaging application typically consists of sealed tube or enclosed metal vessel made of copper or aluminum. Heat pipe is evacuated removing all the air from inside it and is filled with a fraction volume of a working fluid or coolant. Some fluids will be in gaseous phase and some will be liquid phase due to the partial vacuum pressure that is near or below the partial pressure of the fluid inside the heat pipe. The diffusion of working gas with any other gas is eliminated as vacuum is used, so large amount of heat is transported from one point to the other.

As shown in Figure 3.1 the heat pipe consists of three section evaporator section, adiabatic section and condenser section. Heat pipe is filled with conducting fluid kept at low pressure. Heat is absorbed in the evaporator section of the heat pipe which leads to evaporation of fluid inside the heat pipe, the fluid transports large amount of heat from evaporator section to condenser section due to latent heat of evaporation. At condenser section the fluid cools to liquid phase releasing the heat due to latent heat of condensation. The liquid than, returns back to evaporator section due to gravity or capillary action where it evaporate

once more and repeats the cycle. The speed at which the heat is transferred depends on the rate at which the fluid is cooled at the condenser of the heat pipe.

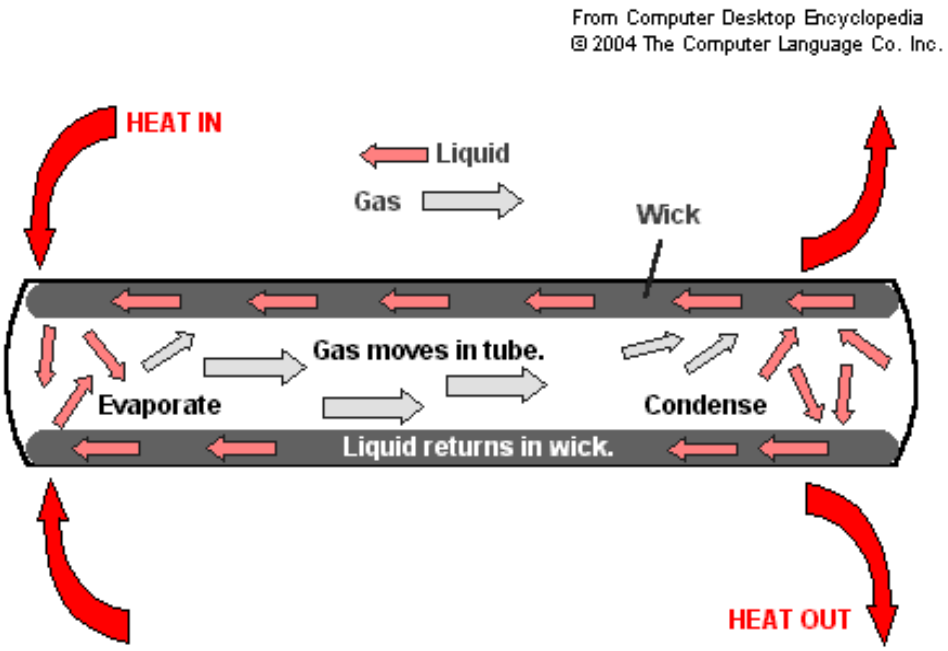


Figure 3.1 Conventional heat pipe [15]

3.1.1 Material used for heat pipe construction

As different fluids can be functional at certain temperature ranges and also the working vessel needs to be compatible with the working fluid used in heat pipes. The working fluid can create corrosion in the working vessel and even damage the vessel due to chemical reaction [17]. The Table 3.1 shows the typical operating characteristics of heat pipe

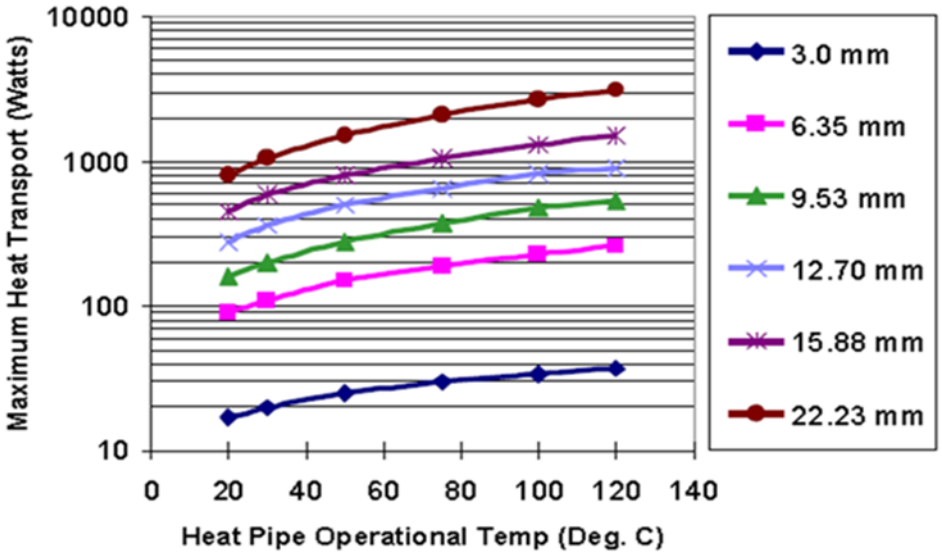


Figure 3.2 Performance of copper water groove heat pipe at vertical orientation (gravity assist) [17]

Copper-water heat pipes are widely used for electronic packaging application as copper is compatible with water and can work well within the temperature range of 5ºC to 230ºC. Heat pipe does not work when the temperature of the pipe is lower than the freezing point of the working fluid. When heat pipe placed vertically the problem of freezing and thawing may destroy the join of a heat pipe. The Figure 3.2 shows the performance of copper water groove heat pipe at vertical orientation [17].

Table 3.1 Typical operating characteristics of heat pipe [17]

Temperature Range (°C)	Working Fluid	Vessel Material	Measured axial[δ] heat flux (kW/cm^2)	Measured surface[δ] heat flux (W/ cm^2)
-200 to -80	Liquid Nitrogen	Stainless Steel	0.067 @ -163°C	1.01 @ -163°C
-70 to +60	Liquid Ammonia	Nickel, Aluminum, Stainless Steel	0.295	2.95
-45 to +120	Methanol	Copper, Nickel, Stainless Steel	0.45 @ 100°C[x]	75.5 @ 100°C
+5 to +230	Water	Copper, Nickel	0.67 @ 200°C	146@ 170°C
+190 to +550	Mercury* +0.02% Magnesium +0.001%	Stainless Steel	25.1 @ 360°C*	181 @ 750°C
+400 to +800	Potassium *	Nickel, Stainless Steel	5.6 @ 750°C	181 @ 750°C
+500 to +900	Sodium *	Nickel, Stainless Steel	9.3 @ 850°C	224 @ 760°C
+900 to +1,500	Lithium *	Niobium +1% Zirconium	2.0 @ 1250°C	207 @ 1250°C
1,500 + 2,000	Silver*	Tantalum +5% Tungsten	4.1	413

[δ]Varies with temperature
[x]Using threaded artery wick
*Tested at Los Alamos Scientific Laboratory
*Measured value based on reaching the sonic limit of mercury in the heat pipe
Reference of "Heat Transfer", 5th Edition, JP Holman, McGraw-Hill

3.2 Types of Heat Pipes

Heat pipes can be classified in to two types the first one is conventional heat pipe and the second being the micro heat pipe.

3.2.1 Conventional heat pipe (CHP)

The conventional heat pipe generally consists of a wick structure which exerts a capillary pressure on the liquid phase of the working fluid. Wick is basically a sintered metal powder or a series of groove parallel to the pipe axis as shown in the Figure 3.3. Wick is basically made of steel, aluminum, nickel or copper in various ranges of pore sizes.

The main purpose of the wick material is to exert capillary pressure on the condensed fluid so that the fluid returns to evaporator from condenser after being cooled. The wick structure even helps in distributing the liquid around the evaporator section or anywhere where heat can be received by the heat pipe. With increase in pore size the permeability of the wick increases and by increasing the wick thickness the heat transport capability of the heat pipe increases. The thermal conductivity of working fluid in the wick sets the overall thermal resistance of the heat pipe at evaporator. If gravity is used to pump the condensed fluid from condenser to evaporator of the heat pipe then wick structures can be eliminated.

Figure 3.3 Wick structures [19]

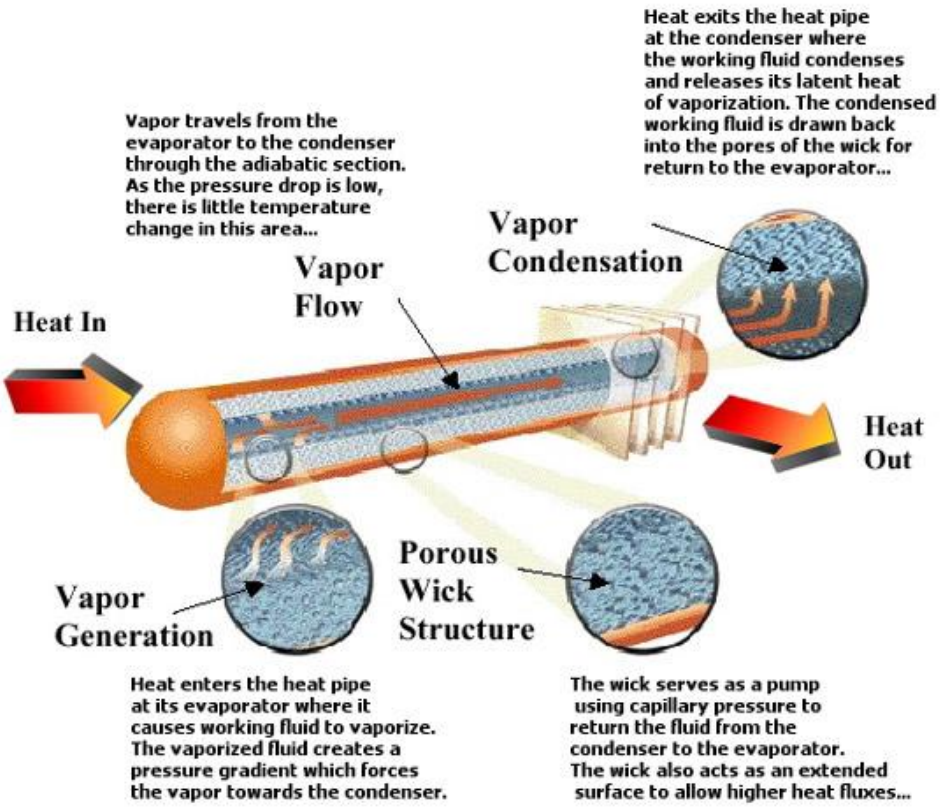


Figure 3.4 Conventional heat pipe [20]

3.2.2 Micro heat pipe (MHP)

In 1984 Cotter introduced the theory of micro heat pipe. He defined a micro heat pipe as “so small that the mean curvature of the liquid-vapor interface is comparable in magnitude to the reciprocal of the hydraulic radius of the total flow channel" [21].

A MHP is a very small device usually of square of triangular shape with a hydraulic diameter on the order of 100 § and a length of several centimeters. Usually MHP has hydraulic diameter of 5 § to 500 §, which is much smaller compared to CHP. As shown in the Figure 3.5 and 3.6 MHP generally does not have a wick structure. MHP uses sharp edges of the pipe’s cross section which assists the return of the condensate to the evaporator section after being cooled at the condenser section [21].

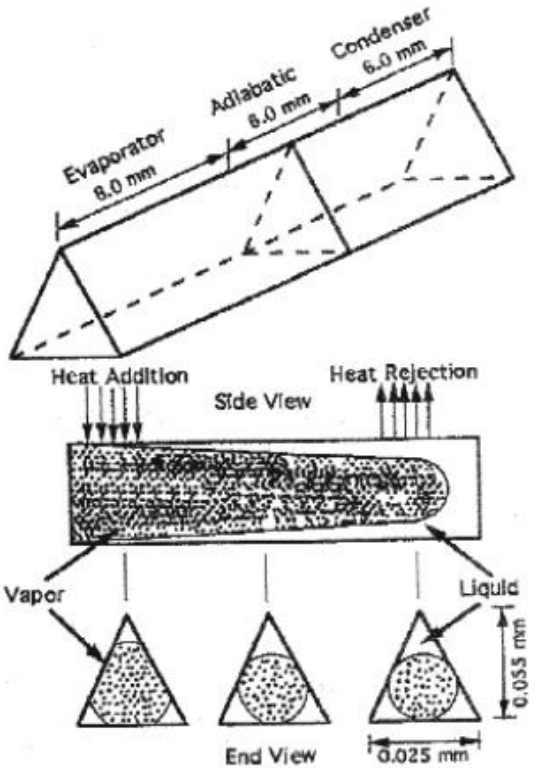


Figure 3.5 Schematically triangular shaped micro heat pipe [21]

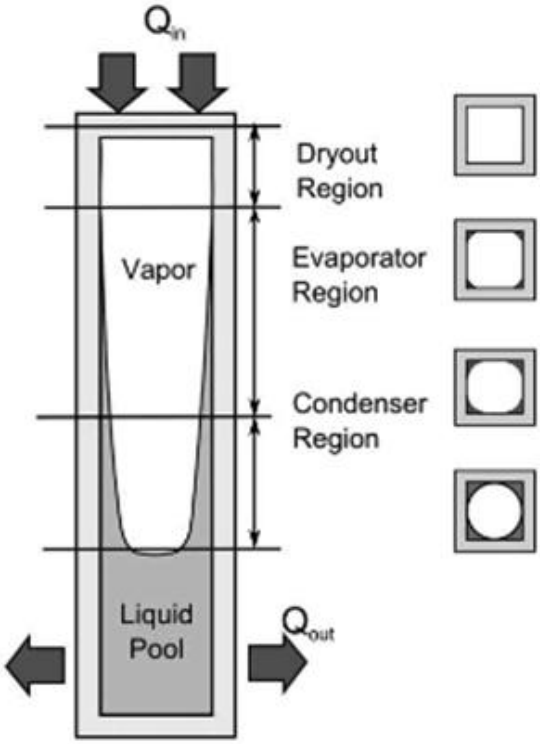


Figure 3.6 Square shaped micro heat pipe [22]

3.3 Advantages and Limitations of Heat Pipe

3.3.1 Advantages of heat pipe in hot-spots cooling

A heat pipe has a lot of advantages in electronic cooling application compared to other devices. As heat pipe uses condensation and evaporation in a closed two-phase cycle to transport large amount of heat, the heat transport capability of heat pipe is several magnitude of orders higher than even the best conductor like diamond. Heat pipe has low thermal resistance which leads to low heat loss while transporting heat from evaporator to condenser. Heat pipe maintains nearly constant source temperature, as with increase in heat flux in evaporator the rate of vaporization of working fluid also increases [18].

In heat pipe both the evaporator and condenser works independently. The area where heat is added to evaporator can differ in shape and size from the condenser in which it is being

cooled. Heat from small area of high heat flux, hot-spots of electronic chips can be transported from evaporator and can be to be dissipated in larger area at the condenser to be cooled by an external device, so that the fluid vaporized in evaporator does not exceed the fluid condensed in condenser [18].

3.3.2 Limitations of heat pipe

Heat pipe transports large amount of heat from one point to other ranging from few watts or several kilowatts, depending on the application. The effective thermal conductivity of the heat pipe will reduce once it operated beyond its capacity. There are several limitations that affect the maximum heat transport capability of a heat pipe. The five major limitations that must be addressed while designing heat pipes operating temperatures are viscous, sonic, entrainment/flooding, capillary and boiling.

3.3.2.1 Viscous

Flow of vapor from condenser to evaporator depends on the difference of the pressure between the condenser and the evaporator. At low pressure this pressure difference is not enough to overcome the viscous force. This viscous force of the fluid will prevent the vapor to flow in the heat pipe and caused the heat pipe to operate below the recommended operating temperature. The potential solution for the viscous limitation is either to increase the operating temperature of the working fluid or to change the used different alternative working fluid. In 1983 Dunn and Reay found the viscous limitations, given by the equation

$$q_v = \frac{r_v^{\,2} L \rho_v P_v}{16 \mu_v L_{eff}} A_v \qquad 3.1$$

Where,

q_v = viscous limit

r_v = vapor core radius

L = latent heat of vaporization

P_v = vapor pressure within the heat pipe

L_{eff} = effective heat pipe length

3.3.2.2 Sonic

Vapor in the heat pipe will reach the sonic velocity when exiting the evaporator and will result to a constant heat pipe transport power and large temperature gradient The main reason for sonic limitation is due to the bad combination of power and operating temperature. In heat pipe the vapor velocity varies due to evaporation and condensation in the heat pipe. It is due to too low power at operating temperature of heat pipe. This problem occurs during the start-up but as the heat pipe system will take the adequate power and large temperature gradient will self-correct the as the heat pipe warms up. Sonic limitation in the heat pipe is given by the equation

$$q_s = A_v P_v L\left(\frac{\gamma R_v T_v}{2(\gamma + 1)}\right)^{1/2} \quad 3.2$$

Where,

q_s = sonic limitation

P_v = vapor pressure within the heat pipe

L = latent heat of vaporization

γ = ratio of specific heat

R_v = gas constant

T_v = vapor temperature

3.3.2.3 Entrainment/flooding

In heat pipe the liquid and vapor flow in opposite directions the high velocity vapor may pick up the liquid droplets or entrained in the vapor flow. This prevents condensate from returning to evaporator. This is due to heat pipe being operated above the designed power input or at too low operating temperature. This entrainment results in excess liquid accumulation in

condenser and dry out of the wicking structure. The potential solution for this problem is to increase the vapor space diameter or to increase the operating temperature. It is very important to evaluate when the onset of entrainment begins in a counter-current, two phase flow. The most commonly used criteria to determine this onset is when the Weber number (W_e) is equal to unity. Weber number is defined as the ratio of the viscous shear force resulting from the liquid surface tension. It is given by the equation

$$W_e = \frac{2(r_{h,g})\rho_v {V_v}^2}{\sigma} \tag{3.3}$$

Where,

W_e = weber number

$r_{h,g}$ = hydraulic radius of the groove

V_v = vapor velocity

σ = surface tension of the fluid

The Weber number must be less than one to prevent the entrainment of liquid in the vapor flow. The vapor velocity is given by the equation

$$V_v = \frac{Q}{A_v \rho_v L} \tag{3.4}$$

Where, Q is local heat flux

Maximum heat transfer capacity based on entrainment limitation is given by the equation

$$q_e = A_v L \left(\frac{\sigma \rho_v}{2r_{h,g}}\right)^{1/2} \tag{3.5}$$

Where, q_e is the maximum heat transfer capacity

3.3.2.4 Capillary

This limitation occurs when the total sum of resisting pressure such as gravitational, liquid and vapor flow and pressure drops exceeds the capillary pumping heat of the heat pipe wick structure. For heat pipe operate capillary pumping pressure must be greater than all other resisting pressure. This problem occurs with the heat pipe input power exceeds the design heat transport capacity of the heat pipe. This problem can be solved by modification of heat pipe design or wick structure and even by reducing the input power. The governing equation is expressed by the equation

$$\Delta P_c \geq \Delta P_h + \Delta P_v + \Delta P_l \qquad 3.6$$

Where,

ΔP_c = capillary pumping pressure

ΔP_h = hydrostatic pressure drop is due to the body forces

ΔP_v = pressure drops are due to viscous forces in the vapor

ΔP_l = pressure drops are due to viscous forces in the liquid

3.3.2.5 Boiling

Due to too much of heat applied to the evaporator of the heat pipe boiling may occur and hence trap bubble in the wick. Tis trapping of the fluid may block the return of the fluid to the evaporator which may lead to dry out of the wick, which is known as boiling limit. Film boiling in a heat pipe initiates at 5-10 W/cm^2 for screen wicks and 20-30 W/cm^2 for powder metal wicks. High radial heat flux cause this problem, which results in heat pipe dry out and large thermal resistance. This problem can be solved by using with higher heat flux capacity or by spreading out the heat load. For a heat pipe with an axial evaporator, boiling limit is given by the following equation

$$q_b = \frac{2\pi L_e K_e T_v}{L\rho_v \ln(r_i/r_v)}\left(\frac{2\sigma}{r_n} - \Delta P_{c,m}\right) \qquad 3.7$$

Where,

q_b = boiling limit

K_e = effective conductivity

r_i = inner radius of heat pipe

r_v = vapor core radius

r_n = nucleation radius

CHAPTER 4

HOT-SPOTS COOLING TECHNIQUES IN ELECTRONIC PACKAGING

Many researches have been conducted to remove the heat from IC to keep the junction temperature (highest temperature on the active surface of the die) below the acceptable temperature limit. Hot spot has become one of the major thermal challenges in today's IC industry as it limits the IC's performance, reliability and yield.

Various micro-channel heat sink are being used for hot spot cooling in the electronic chip as liquid has a capacity to dissipate more heat than air. Figure 4.1 shows the micro-channel heat sink with water as a fluid for hot spot cooling in electronic chips. As liquid has higher heat transfer coefficient than air, water can be used in micro-channel heat sink but as it is a good conductor of electricity it has to be electrically insulated from the electronics which degrades the cooling performance. Even various dielectric fluids which are thermally conductive and electrically resistive can be used in micro-channel heat sink instead of using the water.

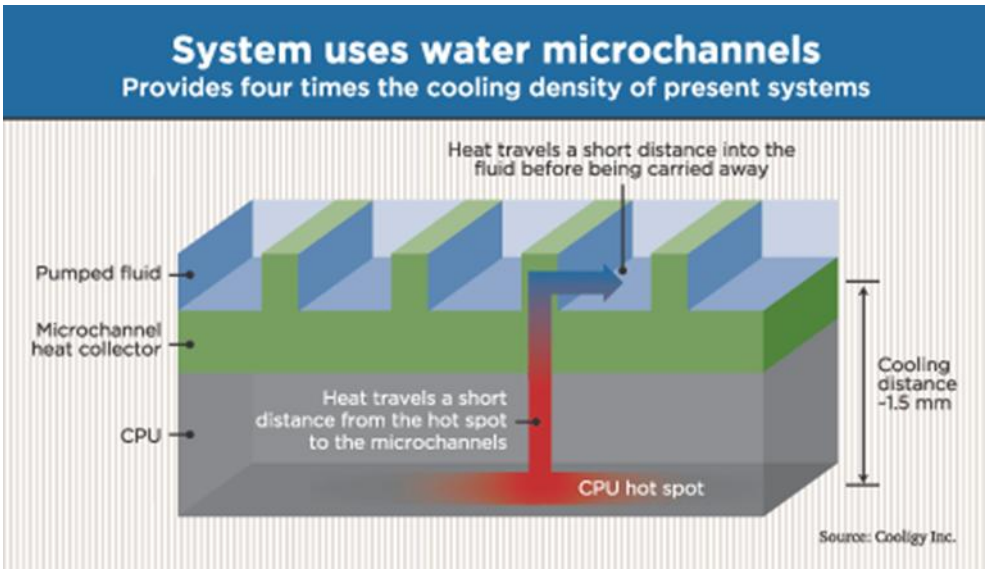


Figure 4.1 Micro-channel heat sink using water as a fluid for hot spot cooling [23]

To increase the heat transfer coefficient of dielectric fluid it has to be pressurized and boiled but it require large system and huge power to operate. For micro-channel heat sink even requires pump to circulate liquid in a micro channel. As many mechanical system works together for a micro-channel heat sink reliability is the biggest concern.

Immersion cooling can also be used for hot spot cooling. Intensive boiling heat transfer with dielectric fluid from back of the chip can be obtained by encapsulating the chip in a bath of dielectric fluid with the heat sink serving as one side of an enclosure. The technique can reduce the temperature of the hot spot of the chip and uniform heating can be achieved in the active side of the silicon chip [24]. The Figure 4.2 shows the basic liquid immersion cooling system. The problem is very little is known about immersion cooling with confined boiling in presence of severe hot spots and still a lot of research has to be done to before commercializing this technique. Even various new fabrication techniques like liquid filing procedures along with hermetic sealing of the dielectric fluid would be needed to bring this technique in the market [24].

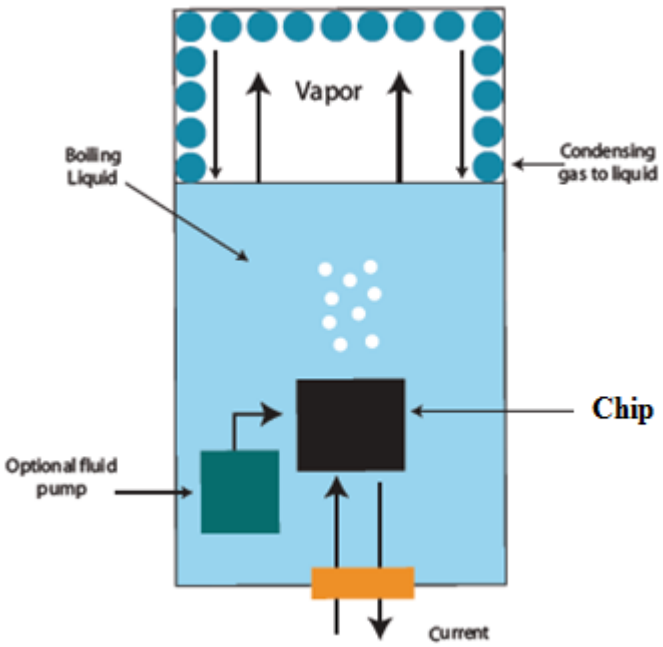


Figure 4.2 Basic immersion cooling system [25]

To remove the hot spots a millimeter-sized high thermal conductivity spreader can be attached to the back side of the chip. Using high thermal conductivity meat like diamond, SiC or copper disc reduces the severity of the hot spot. High thermal conductivity metals can even be embedded in the heat sink itself with close proximity to the hot spot to enhance the transfer of heat from hot spot. But the manufacture if this kind heat sink is much more expensive than a conventional heat sinks and even coefficient of thermal expansion (CTE) mismatch between various components in a chip package is a major concern [24].

Even jet impingement cooling has been studied for the purpose hot spot cooling in electronic packaging. In jet impingement cooling technique an array of micro jets with non-uniform liquid droplets are sprayed on the surface of a chip with hot spot. The liquid droplets evaporate and take away the heat from the hot spot of the chip to achieve uniform heating. But still this technique is far way in the research stage and the achievable performance parameter has yet to be determined. Even jet impingement technique requires a lot of additional space and would be far heavier and less reliable than using a TEC [24]. The Figure 4.3 shows the jet

impingement cooling technique used in electronic packaging application and Figure 4.4 show the water cooling technique proposed by IBM.

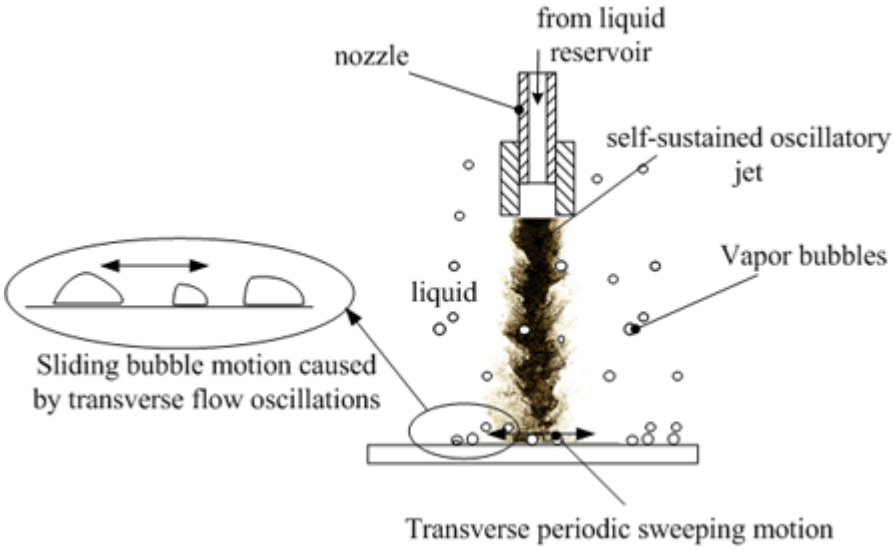


Figure 4.3 Phase change jet impingement heat transfer system [26]

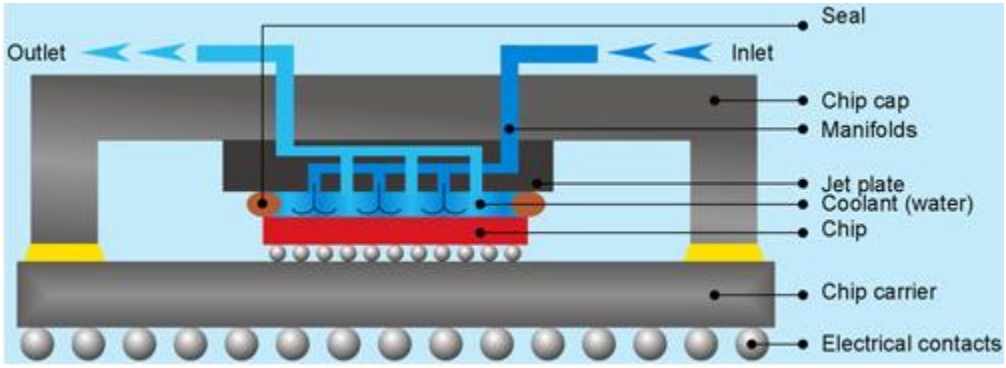


Figure 4.4 Water cooling technique proposed by IBM [27]

Conventional Thermoelectric Cooler (CTEC) has been proposed for the hot spot cooling in the electronic packaging. As shown in Figure 4.5, CTEC has been attached to the back side of a flip chip and which basically cools the entire surface area of the chip [24]. In this thesis, study was done using conventional thermoelectric along with micro heat pipe (MHP) for cooling the hot spots in high power electronic devices. Micro heat pipe was used to transport heat

directly from hot spot of a silicon chip to the integrated heat spreader be cooled using the CTEC. Even trench of was used to enhance localized cooling of the hot spot. The thermal and CFD analysis showed that using CTEC and MHP along with trench gives a good solution for hot spot cooling.

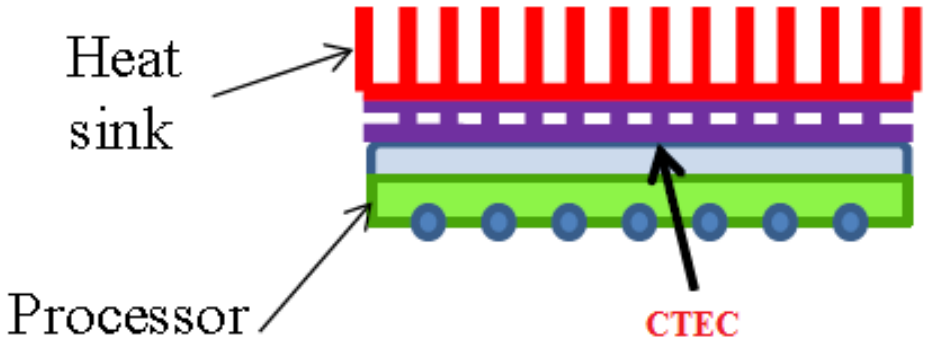


Figure 4.5 CTEC used to cool the chip package

TFTEC gives a very good solution for hot spot cooling in the electronic packaging. TFTEC can be embedded in the chip package which removes the heat directly from the hot spots by cooling the area of high heat flux**.** Figure 4.6 shows the embedded thermoelectric cooler. Viatcheslav Litvinovitch et al. [29], Kong Hoon Lee et al. [30], Bao Yang [3] has proposed the techniques of hot spot cooling using micro thermoelectric cooler. G. Jeffrey Snyder et al. [31] and David S. Chau et al. [28] proposed few techniques of hot spot cooling by embed TFTEC for hot spot cooling. The Figure 4.7 and 4.8 shows hot spot cooling techniques with TFTEC embedded in silicon die and integrated heat spreader.

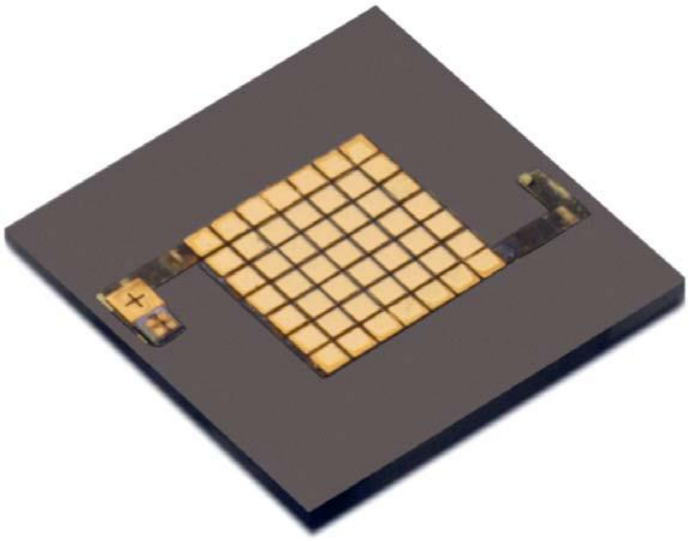


Figure 4.6 Embedded thermoelectric cooler [24]

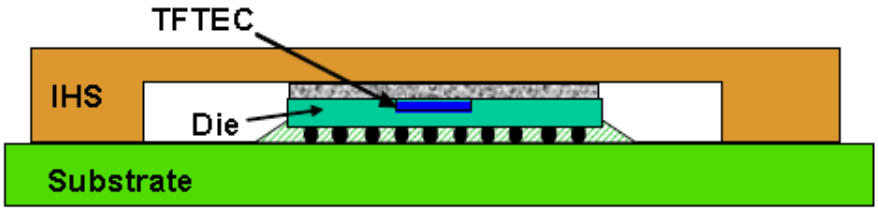


Figure 4.7 TFTEC embedded in silicon die [28]

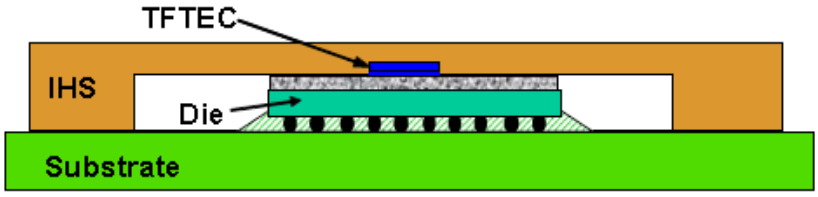


Figure 4.8 TFTEC embedded in the integrated heat spreader [28]

CHAPTER 5

REMOVING THE HOT SPOTS FROM HIGH POWER DEVICE USIGN MICRO-HEAT PIPE AND THERMOELECTRIC COOLER

Shlomo Novotny et al. [32] proposed the hot spot cooling techniques using thermal conductor and TEC which was found to be not that effective for hot spots cooling as thermal conductivity of copper conductor (widely used in electronic packaging) was not high enough to take lot of heat away from hot spots. In this case study an innovative cooling technique of hot spot in high power device using TEC and micro heat pipe was presented. The chip package featuring a micro heat pipe that connects the TEC with the die (shown in Figure 5.1 (c)) is investigated by using a CFD based commercial software. In this chip package integrated heat spreader (IHS-2) is also used at cold side of TEC to enhance the cooling at condenser section of micro heat pipe.

5.1 Concept of Chip Package with Micro Heat Pipe, TEC and Trench

A chip package with a Micro-Heat Pipe, TEC with trench is shown in the Figure 5.4. This assembly includes a TEC, micro heat pipe, a die with a hot-spot, integrated heat spreader (IHS-1, IHS-2), heat sinks (HSK-1, HSK-2) , thermal interface material (TIM-1, TIM-2 and TIM-3) and insulators (INS-1, INS-2, INS-3). Square groove was made in two central fins of the Heat Sink (HS-1) to accommodate TEC for cooling. The micro heat pipe passes through the heat sink (HSK-1), integrated heat spreaders (IHS-1 and IHS-2) and insulator (INS-3). For comparison conventional chip package without TEC (as show in Figure 5.1) and chip package with TEC and copper conductor (as shown in Figure 5.2) are also depicted.

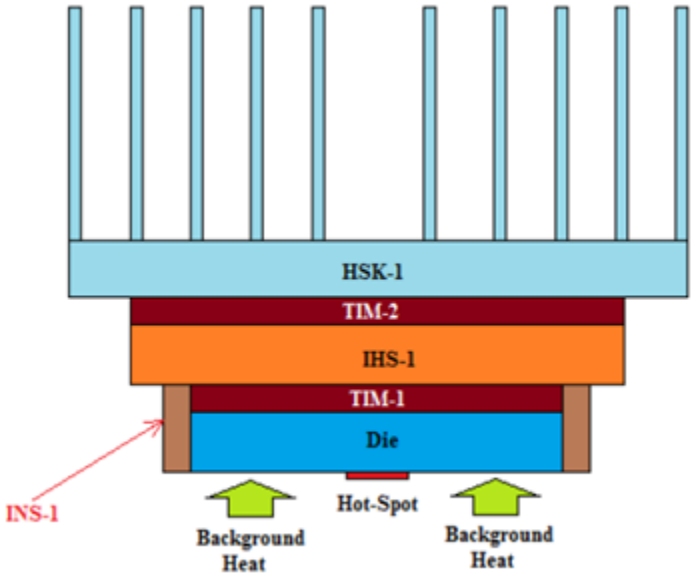


Figure 5.1 Conventional chip package (Figure not to Scale)

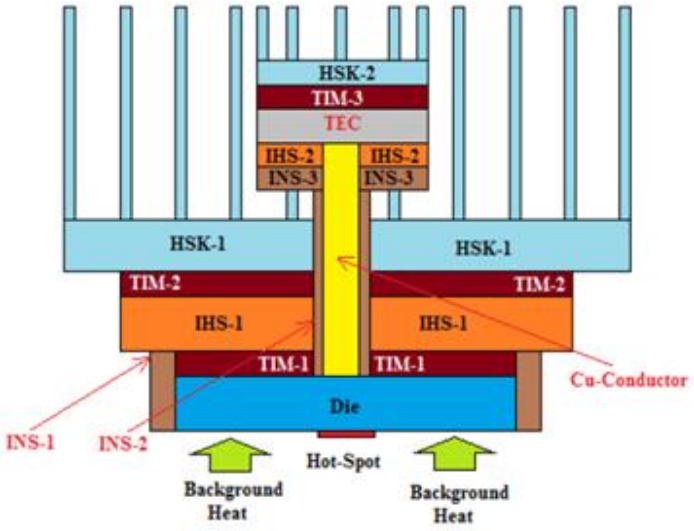


Figure 5.2 Chip package with Cu-conductor and TEC (Figure not to Scale)

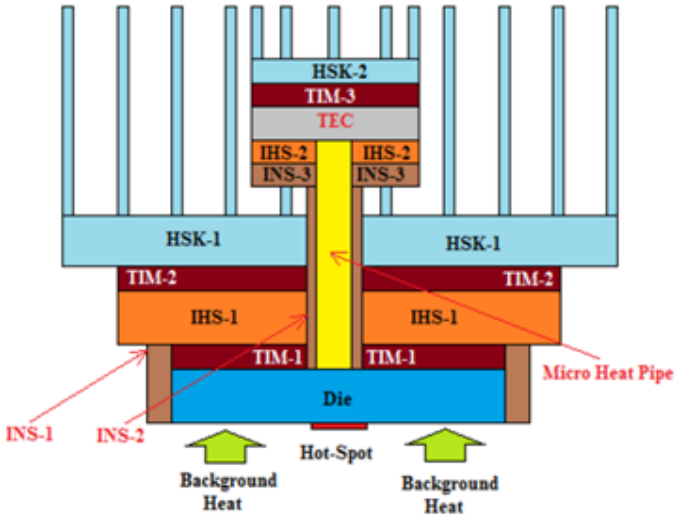


Figure 5.3 Chip package with micro heat pipe and TEC (Figure not to Scale)

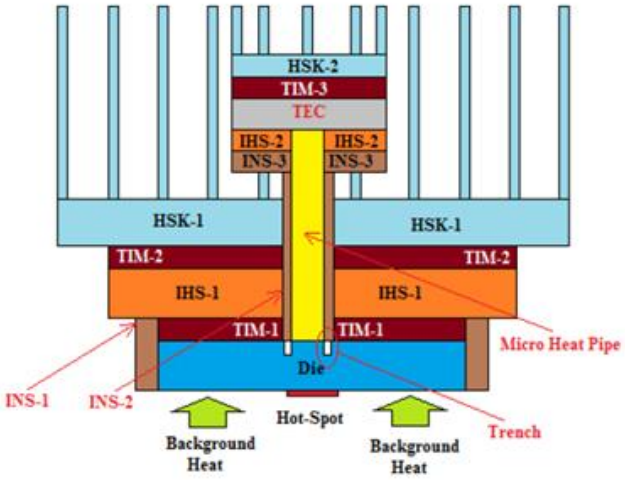
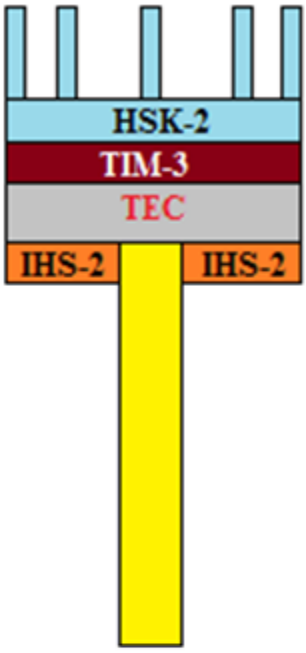


Figure 5.4 Chip package with micro heat pipe and TEC and trench (Figure not to Scale)



(a)

(b)

Figure 5.5 Cut section front view of HSK-2, TEC, IHS-2, TIM-3 and micro heat pipe. (a) Front view and (b) bottom view. In bottom view IHS-2 blocks TEC, TIM-3 and HSK-2

(Figure not to scale)

5.2 Modeling Methodology

5.2.1 Modeling of chip package

3D numerical model was created in ANSYS Workbench DesignModeler, ANSYS Icepak was used to analyze the cooling performance of the chip package. Micro heat pipe, Cu-conductor and insulator (INS-2) were modeled as a block in ANSYS Icepak.

Table.5.1 Geometry and material properties

Model Component	Geometry (w x l x h)	Material	K W/mK	B.C
Die	13mm x 11mm x 750µm	Silicon	120	70 W/cm^2
Hot-Spot	400µm x 400µm	---	---	1250 W/cm^2
INS-1	1mm thick	Epoxy-Resin Typical	0.2	---
TIM-1	13mm x 11mm x 175µm	---	30	---
IHS-1	31mm x 31mm x 1.5mm	Cu	387.6	---
TIM-2	31mm x 31mm x 175µm	---	30	---
HSK-1 (Base)	60mm x 50 mm x 5.08mm	Al	240	---
HSK-1 (Fin)	1.45mm x 50mm x 20mm (10 Fins)	Al	240	---
INS-2	0.2 mm thick	Epoxy-Resin Typical	0.2	---
INS-3	0.75mm thick	Epoxy-Resin Typical	0.2	---
IHS-2	15mm x 15mm x 2mm	Cu	387.6	---
TIM-3	15mm x 15mm x 175µm	---	30	---
HSK-2 (Base)	15mm x 15 mm x 5.08mm	Al	240	---
HSK-2 (Fin)	1.45mm x 15mm x 20mm (5 Fins)	Al	240	---
Trench	100µm wide 300µm deep	Filled with Air	0.026 1	---

Geometry parameters and material properties used in this numeric model are listed in Table.5.1 unless otherwise noted.

5.2.2 Thermoelectric cooler in ANSYS Icepak

A pre-made thermoelectric, Melcor_CP1.0-31-05L.1 from ANSYS Icepak Macro library is taken with electrical properties already provided by Lairds Technology, Inc. to the software and is placed vertically. TEC was loaded to Icepak model for analysis.

Specification for Melcor_CP1.0-31-05L.1 thermoelectric cooler:

G-factor=0.79mm, Imax=3.9Amps, Vmax=7.6Volts, Qmax=8.2Watts, N=31 and dTmax=67ºC

Where,

G-factor	ratio of cross-sectional area and height
Imax	maximum current
Vmax	maximum voltage
Qmax	maximum heat
N	number of thermocouples
dTmax	maximum temperature gradient

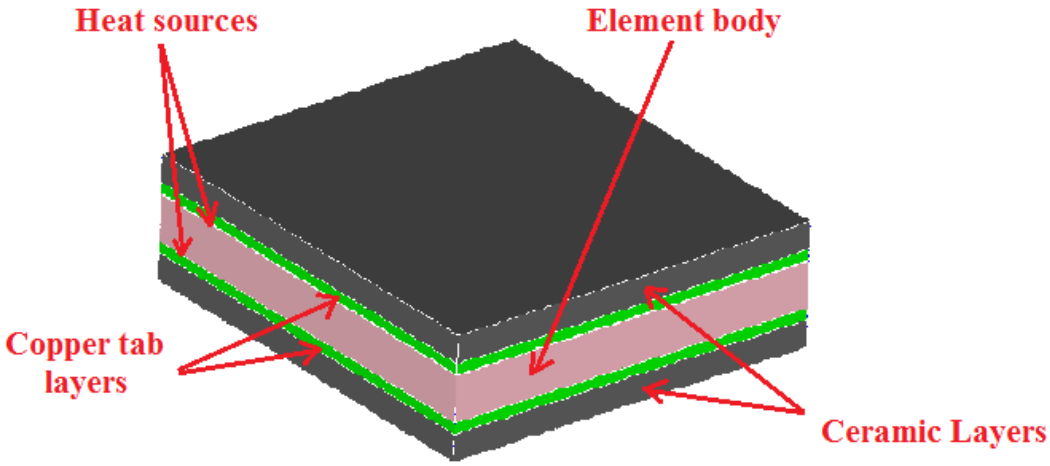


Figure 5.6 Compact TEC model in ANSYS Icepak

Figure 5.7 shows the compact model of TEC in ANSYS Icepak. The TEC model in ANSYS Icepak comprises of five blocks and two sources. The central block is a main body or lumped thermoelectric elements, two blocks next to central block are ceramic copper tap and

the outer most blocks are the ceramic blocks. Two heat sources one is the hot side with positive power and the other is a cold side with negative power. The thermoelectric cooler properties are temperature dependent.

The dimension of thermoelectric cooler is 15mm by 15mm with total thickness of 3.2 mm. Melcor properties was used for the thermoelectric cooler with the current in the thermoelectric cooler varied from 0.5Amp to 3.5Amp.

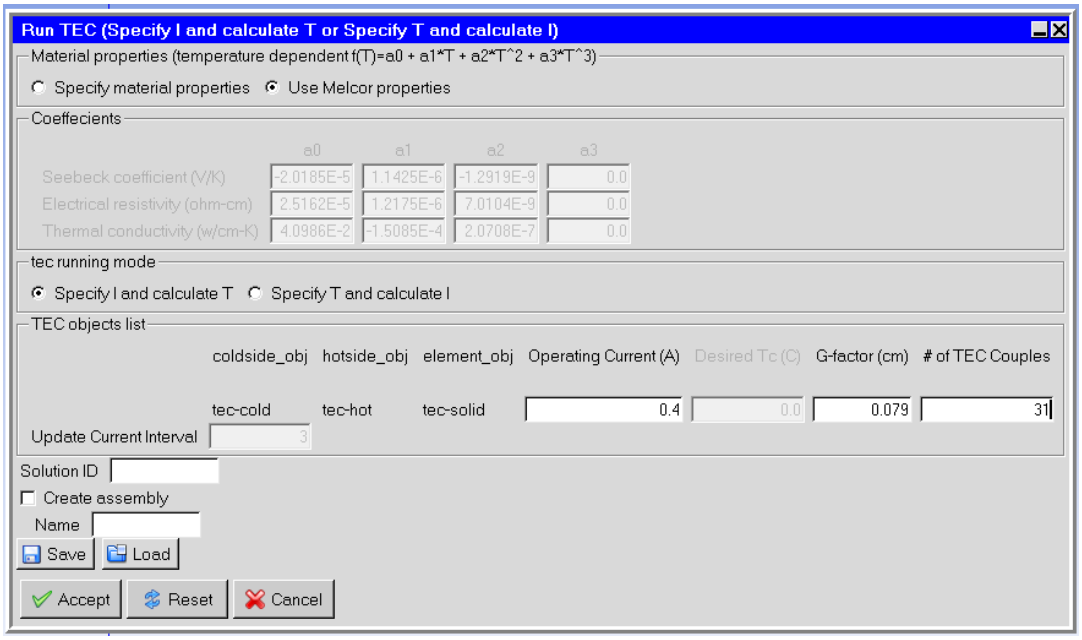


Figure 5.7 Macro window for specifying current for TEC in Ansys Icepak

5.2.3 Modeling of micro heat pipe

Heat pipe is a device that transports large amount of heat from evaporator to the condenser by using latent heat of evaporation of working fluid [35]. Due to the difficulty in phase change modeling, in electronic packaging application, investigators prefer to model heat pipe as a highly conduction solid block [35]. The conductivity should be large enough to result in the same heat rate as taken by evaporation and condensation of heat pipe fluid [35]. The conductivity value should be between 20,000 to 50,000W/mK [34, 35]. In this paper the conductivity values was chosen as 20,000W/mK along the direction of heat flow and

387.6W/mK (Thermal conductivity of heat pipe material i.e Cu) in the other directions as shown in Figure 5.8. The heat pipe as shown in Figure 5 .3, Figure 5.4 and Cu-conductor as shown in Figure 5.2 were insulated (INS-2).

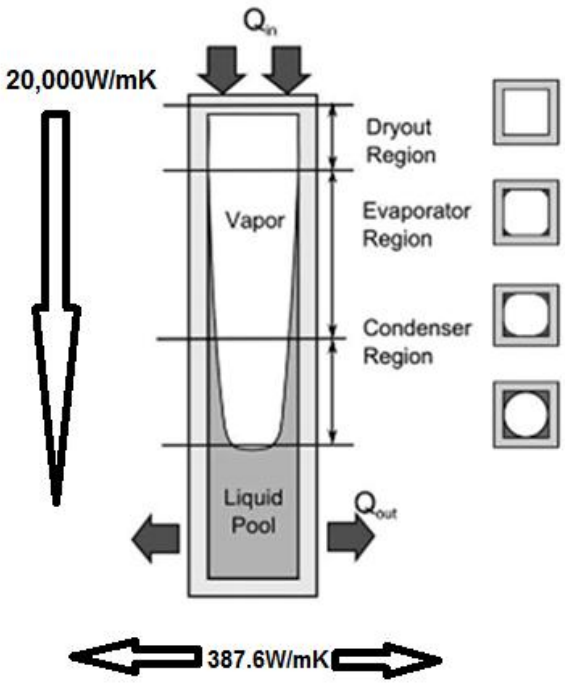


Figure 5.8 Micro heat pipe modeling

Table 5.2 Geometry of micro-heat pipe and Cu-conductor

Model Component	Geometry (w x l x h)
Micro heat pipe	1mm x 1mm x 12.06mm
Cu-conductor	1mm x 1mm x 12.06mm

5.2.4 Description of heat sink

The Heat Sink (HSK-1) has a base of 50mm in the direction of flow and 60mm across the flow. Base was 5.08mm thick. The heat sink has 10 straight fins, which run along the entire

length of the heat sink at 50mm base side. Heat sink fins was cut at regular intervals. The geometry and material property of the heat sink are given in Table 5.1

Square groove of 16mm wide and 5mm depth was cut in two central fins of the heat sink to accommodate the thermoelectric cooler. The Straight Fin Heat Sink (HSK-2) was used to cool the hot side of TEC. There are 5 straight fins in Heat Sink (HSK-2). Two fins at the corner, one at the center, fins are aligned parallel to the fins of Heat Sink (HSK-1), and remaining two fins of Heat Sink (HSK-2) coincides with the two central fins of Heat Sink (HSK-1) as shown in Figure 5 .2, 5.3 and 5.4 and Figure 5.10 and Figure 5.11.

5.2.5 Thermal contact resistance

In order to model the thermal behavior of the chip package more realistically the contact resistance was applied at various interface within the FEA model. Contact resistance of $3.3 \times 10^{-7} m^2K/W$ was applied at the interface between copper conductor and silicon die and even between cold side of the thermoelectric cooler and integrated heat spreader (HIS-2) as shown in Figure 5.9 (a) .

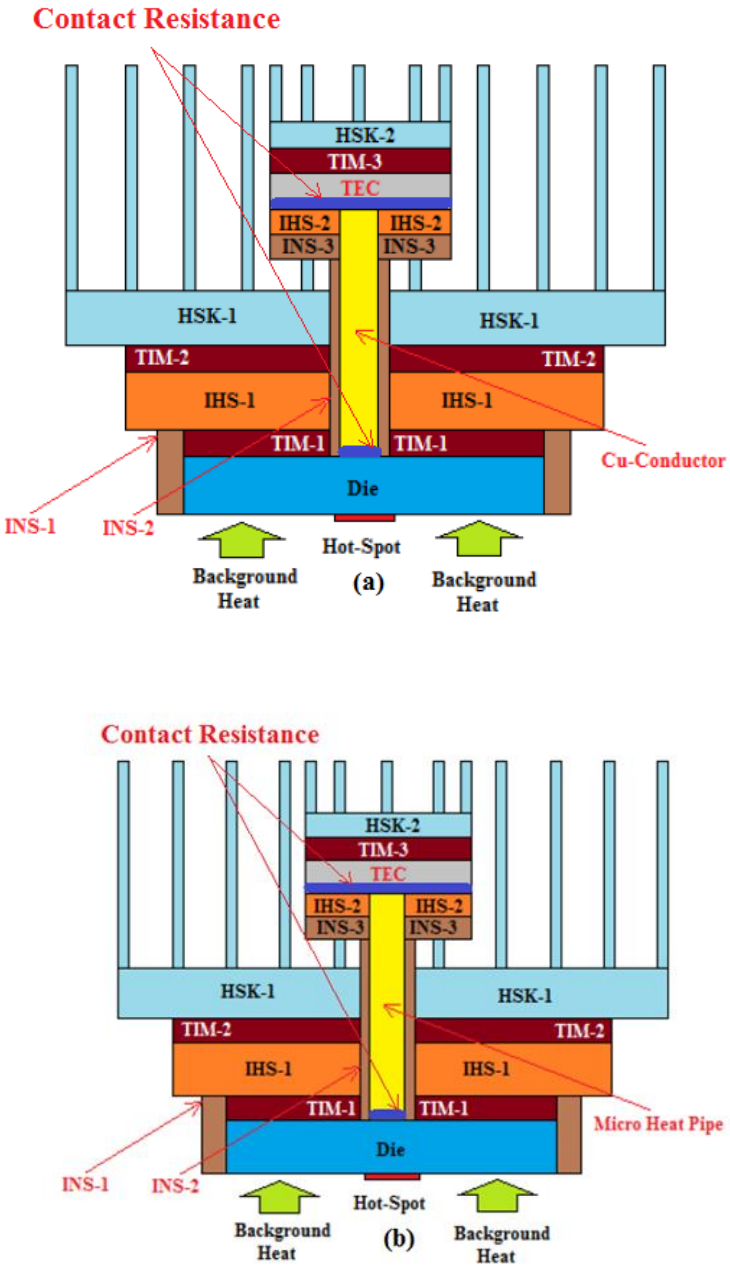


Figure 5.9 (a) Chip package with Cu-conductor and TEC, and (b) chip package with micro heat pipe and TEC

Contact resistance of $3.3x10^{-7}m^2K/W$ was also applied at the interface between micro heat pipe and silicon die and even between cold side of the thermoelectric cooler and integrated heat spreader (HIS-2) as shown in Figure 5.9 (b).

5.3 Computational Fluid Dynamics

A complete chip package was modeled in ANSYS Workbench DesignModeler and ANSYS Icepak. A cabinet in the CFD model was created to have a domain size of 52mm in length (x direction), 62mm in width (z direction) and 28.1mm in height (y direction). Computational domain in Cartesian coordinates is shown in Figure 5.10 and Figure 5.11 . An opening was created equivalent to the face of cabinet at airflow velocity of on z-y plane with turbulent flow (zero equation). A grill is modeled with dimensions equivalent to the face of the cabinet. Adiabatic thermal conditions are assumed at top, bottom, and sidewall of the cabinet. Gravity effect was included and total number of iterations was 100. An ambient air temperature of 20ºC was considered.

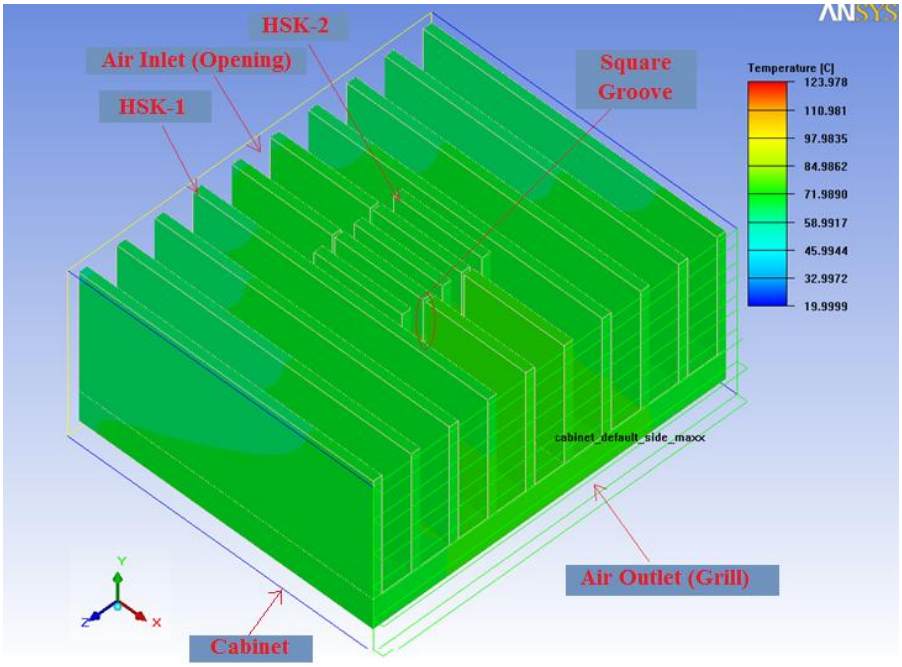


Figure 5.10 A complete chip package in ANSYS Icepak.

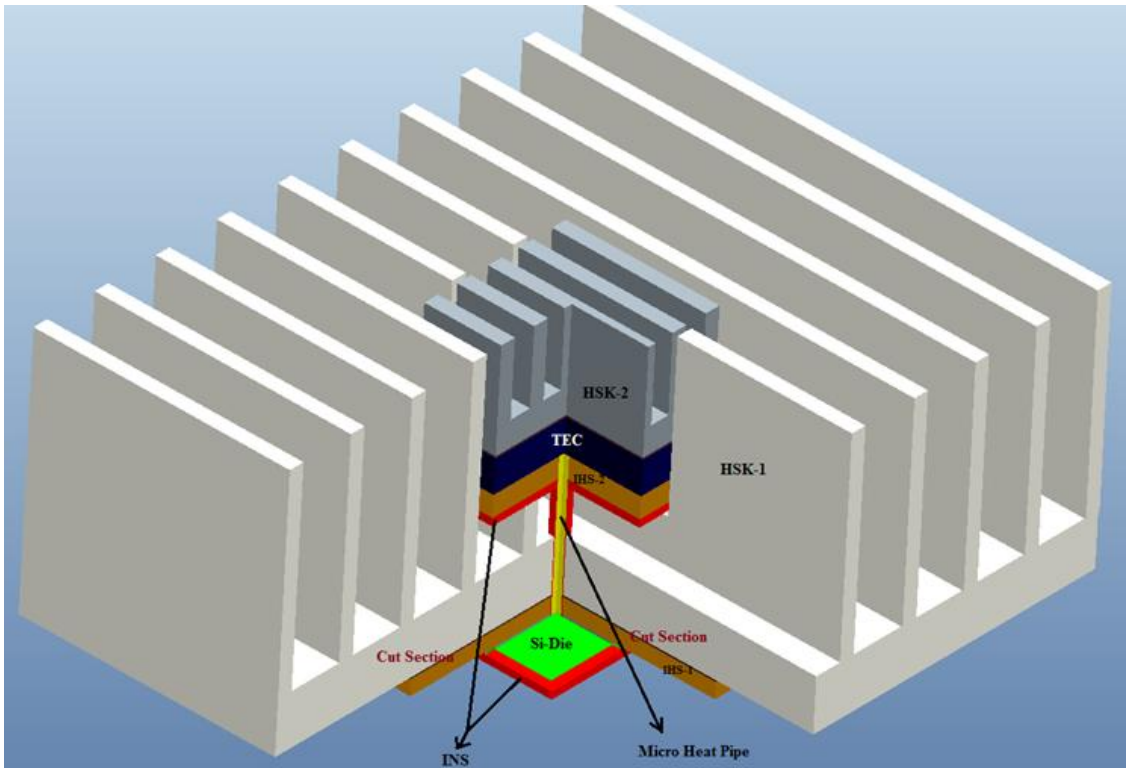


Figure 5.11 Cut section view of the complete chip package in Pro/ENGINEER

As shown in Figure 5.10 the air flows in the positive direction of x-axis. The air flows from opening of the cabinet and the air exits from the grill. The temperature was measured in active side of silicon in the direction parallel and perpendicular to the air flow as shown in Figure 5.12.

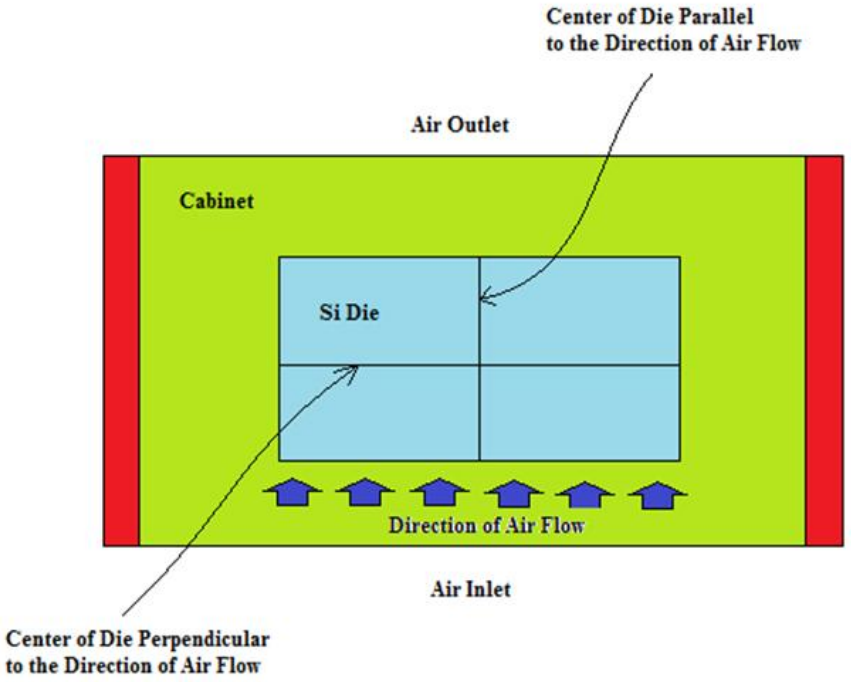


Figure 5.12 Top view of Si-die along with cabinet (Other components of chip package are not shown in the figure, Figure not to scale)

5.3.1 Zero equation turbulent flow

The nature of the problem for forced convection is determined by certain values of dimensionless group called Reynolds number. Reynolds number is given by the equation

$$R_e = \frac{\rho E L}{\mu} \qquad 5.1$$

Where,

R_e = Reynolds number

ρ = density of the fluid

E = mean velocity of an object relative to the fluid

L = characteristics linear dimensions

μ = dynamic viscosity of the fluid

When, R_e is greater than 10^5 turbulent model is used but and R_e is less than 10^5 laminar model is used.

Zero equation or mixing length model was used as it is more accurate and economical for electronic packaging simulations. For zero equation the viscosity of the fluid is

$$\mu_t \equiv \rho l_m{}^2 S \tag{5.2}$$

Where,

l_m = distance across with the turbulent mixing takes place (size of turbulent eddies)

S = modulus of mean rate of strain tensor also defined as

$$S = \sqrt{2S_{ij}S_{ij}} \tag{5.3}$$

Where mean strain rate is given by

$$S_{ij} = \frac{1}{2}\left(\frac{du_i}{dx_j} + \frac{du_j}{dx_i}\right) \tag{5.4}$$

Fluid conductivity is given by the equation

$$k_t = \frac{\mu_t C_p}{Pr_t} \tag{5.5}$$

Where,

k_t = fluid conductivity

μ_t = turbulent viscosity

Pr_t = Prandtl number

5.3.2 Mesh

The Mesher-HD or hex-dominant mesher was the mesh selected for the chip package including the cabinet. The maximum element size of the mesh was selected as 0.25mm x 0.25mm x 0.25 mm in x-direction, y-direction and z-direction respectively. Figure 5.13 shows the mesh in silicon die.

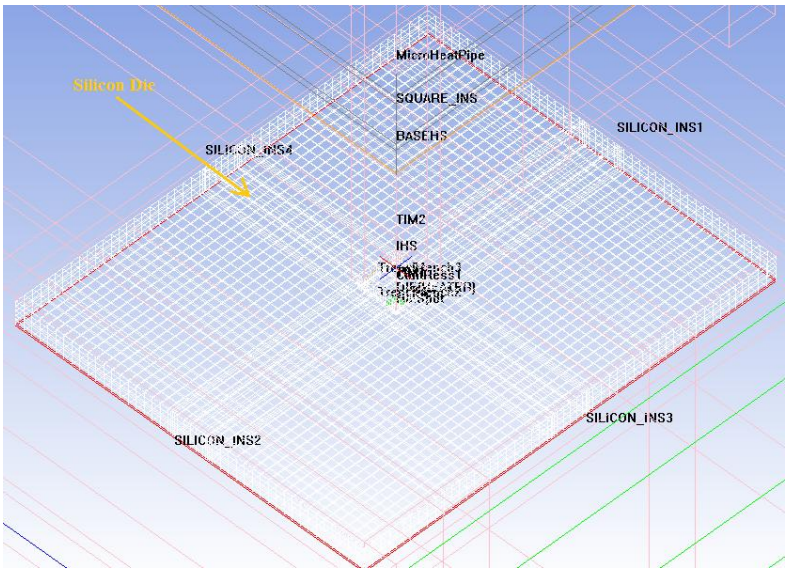


Figure 5.13 Mesh in silicon die with hot spot

The Mesher-HD or hex-dominant mesher is the defult mesh in ANSYS IcepaK. Hex-dominant mesh is very robust and highly automated unstructured mesh generator that can handle grids or virtually unlimited size and complexity. Hex-dominant mesh generally consists of hexahedral elements but including triangular or pyramidal cells and it uses advanced meshing algorithms to allow the most appropriate cell type to generate body-fitted meshes for most general CAD geometries. Hex-dominant masher even produces good mesh for complicated models.

5.4 Results and Discussions

In the first case, the maximum temperature of the hot spot using the conventional techniques was found to be around 127.5ºC, 120ºC and 114.5ºC for the air flow velocity of 2m/s, 2.5m/s and 3m/s respectively as shown in Figure 5.14 and Figure 5.15. Increasing the flow velocity of the air leads to overcooling of the entire chip package. For higher rates of air flow acoustic generated by the fan would be unbearable. From the Figure 5.14 and Figure 5.15 it can be even seen that the overall temperature gradient in the active side of silicon is very high. Although by conventional cooling techniques the maximum junction temperature can be lowered by increasing the flow of air but the overall temperature gradient in the in the active side of the silicon die is constant.

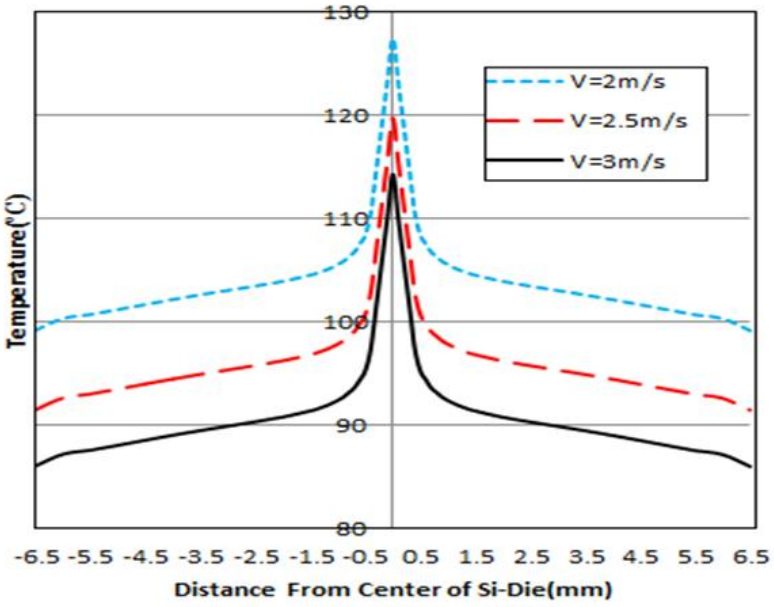


Figure 5.14 Temperature distributions across hot spot on active side of the die for various velocity of air flow (V). Die perpendicular to the direction of air flow at center for conventional chip package without TEC.

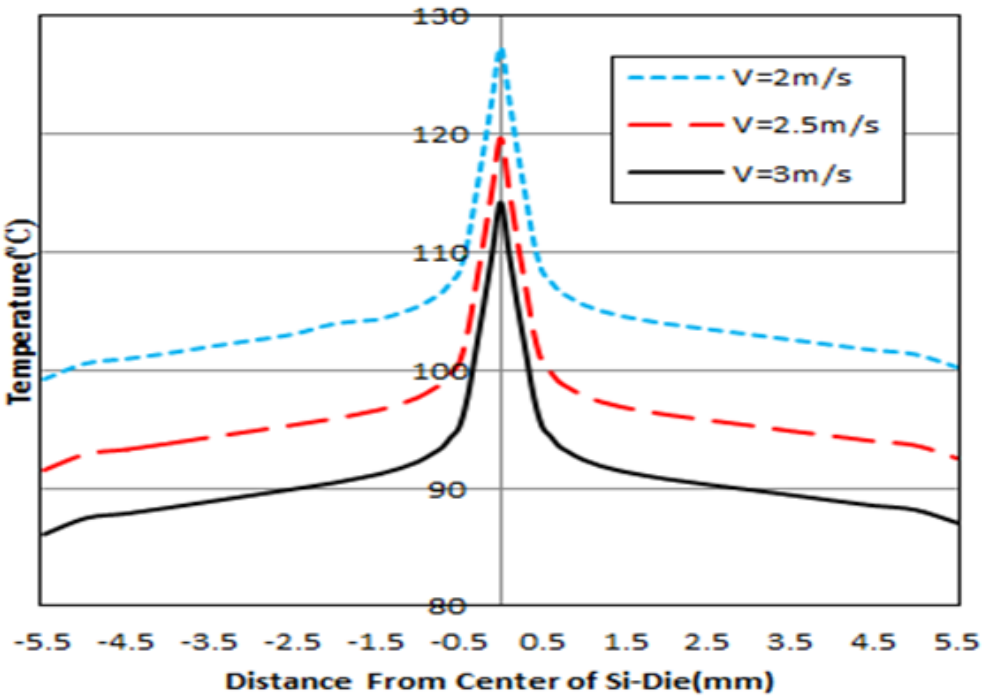


Figure 5.15 Temperature distributions across hot spot on active side of the die for various velocity of air flow (V). Die parallel to the direction of air flow at center for conventional chip package without TEC.

Figure 5.16 shows the temperature profile of conventional package with hot spot.

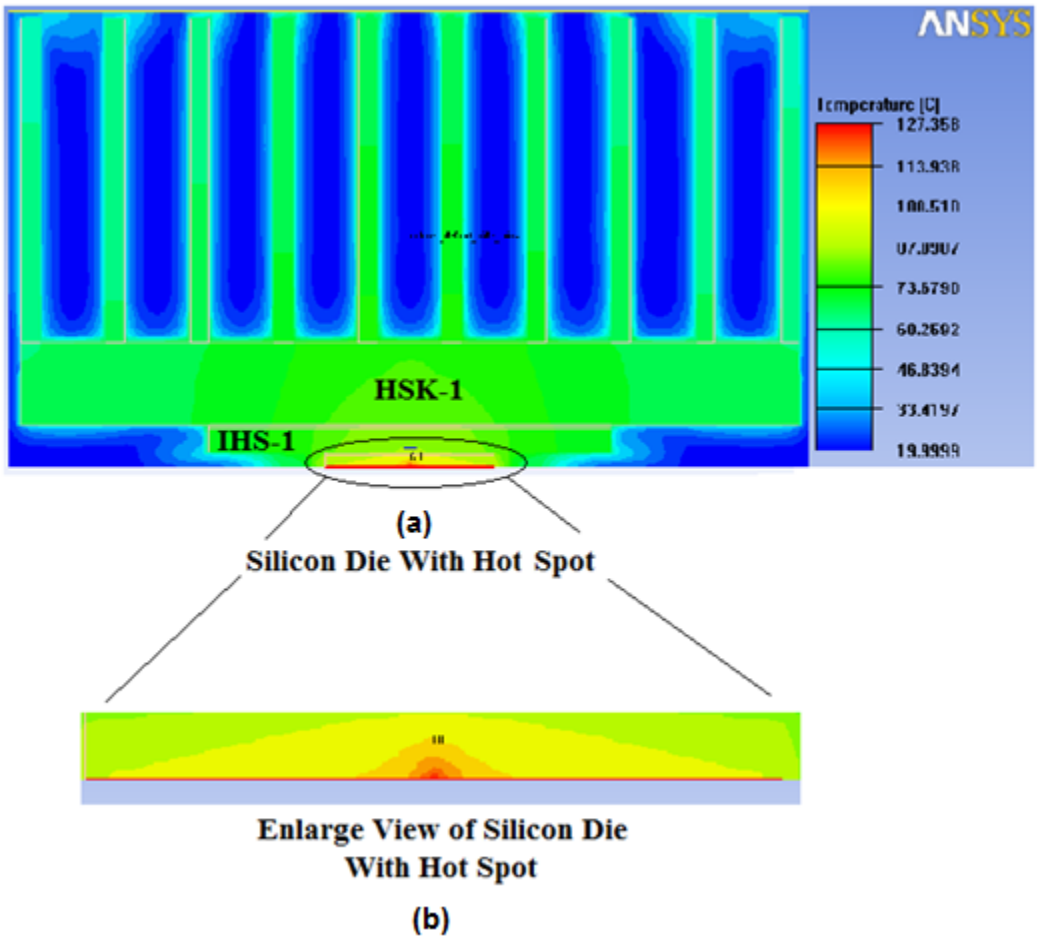


Figure 5.16 (a) Temperature profile of conventional chip package with hot spot in the direction perpendicular of air flow with air flow of 2m/s and (b) enlarge view of silicon die with hot spot

The addition of the micro heat pipe, TEC, integrated heat spreader (IHS-2) and heat sink (HSK-2) in conventional techniques of cooling does not provide much resistance for the air flow, so the comparison was made at the air flow velocity of 2m/s for all the cases. For the air velocity of 2m/s the maximum temperature of hot-spot was found to be about 25ºC more than the maximum temperature without the hot-spot as shown in Figure 5.17 and Figure 5.18. When micro heat pipe and thermoelectric cooler was used along with trench the peak temperature of the hot-spot was reduced from 127.5ºC to 108ºC (As shown in Figure 5.17 and Figure 5.18).

This significant cooling of the hot-spot is the result of combined effect of Micro Heat Pipe, TEC and trench. The cooler ring was formed around the hot spot with the second ring at slightly elevated temperature. From Figure 5.17 and Figure 5.18 it can be see that the maximum temperature gradient in active side of the silicon die is also reduced in conventional chip package with micro heat pipe, TEC and trench.

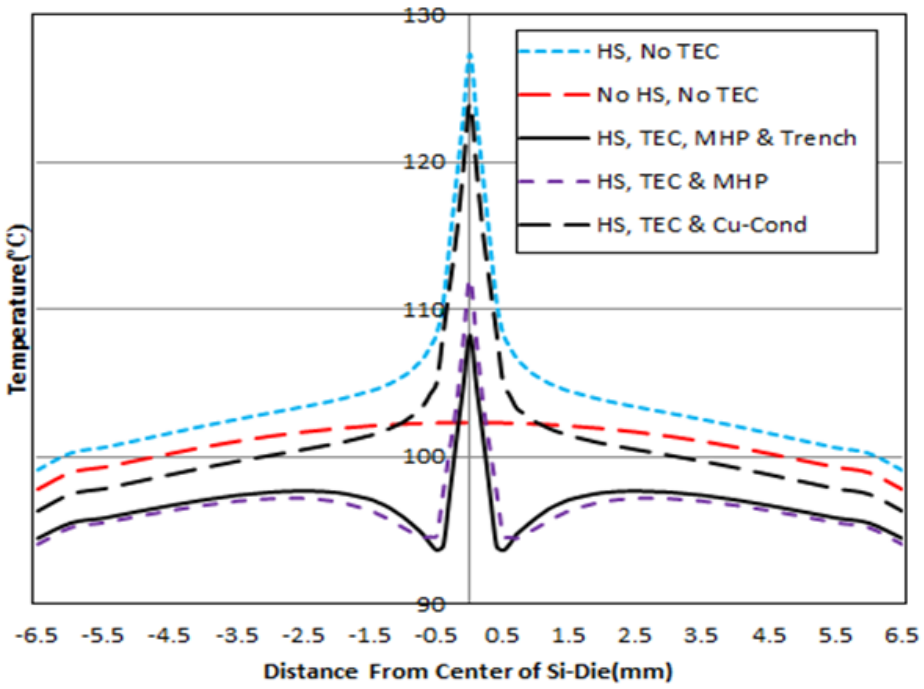


Figure 5.17 Temperature distribution across hot spot on active side of the die for velocity of air flow at 2m/s and TEC powered with current of 2Amp. Die perpendicular to the direction of air flow at center. Light Blue Dashed Line: Conventional Chip Package without TEC. Red Dashed Line: Conventional Chip Package without Hot Spot and without TEC. Black Solid Line: Chip Package with TEC, Micro Heat Pipe and Trench (300mm deep). Purple Dashed Line: Chip Package with TEC &Micro Heat Pipe. Back Dashed Line: Chip Package with TEC & Cu-Conductor.

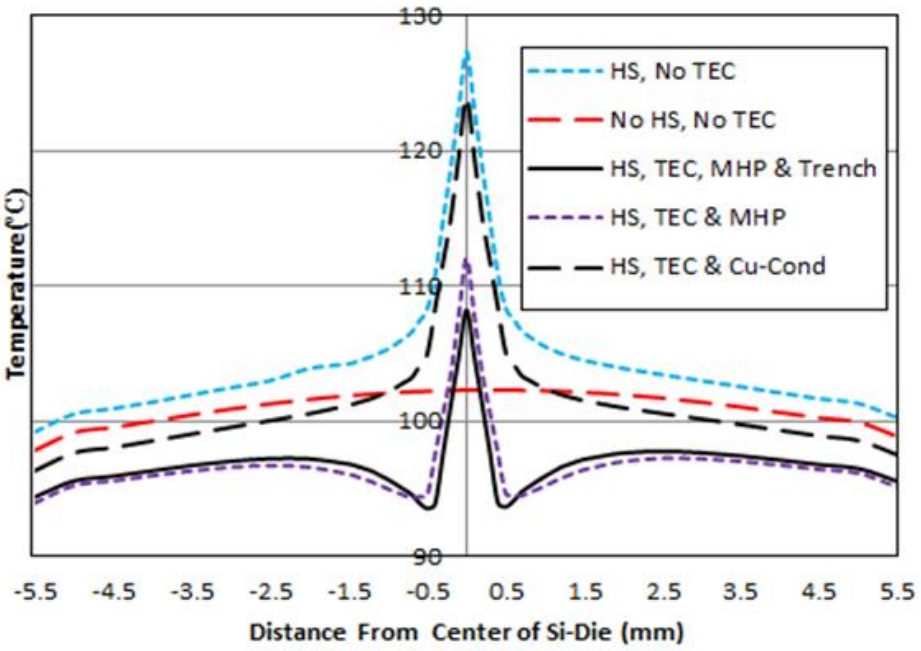


Figure 5.18 Temperature distribution across hot spot on active side of the die for velocity of air flow at 2m/s and TEC powered with current of 2Amp. Die parallel to the direction of air flow at center. Light Blue Dashed Line: Conventional Chip Package without TEC. Red Dashed Line: Conventional Chip Package without Hot Spot and without TEC. Black Solid Line: Chip Package with TEC, Micro Heat Pipe and Trench (300mm deep). Purple Dashed Line: Chip Package with TEC &Micro Heat Pipe. Back Dashed Line: Chip Package with TEC & Cu-Conductor.

Using the trench in chip package with micro heat pipe and TEC the temperature of the hot-spot was reduced from 112ºC to 108ºC. The trench blocks the background from the surrounding die, so the heat transfer takes place directly from the hot-spot to the micro heat pipe to be cooled using the TEC on the other side.

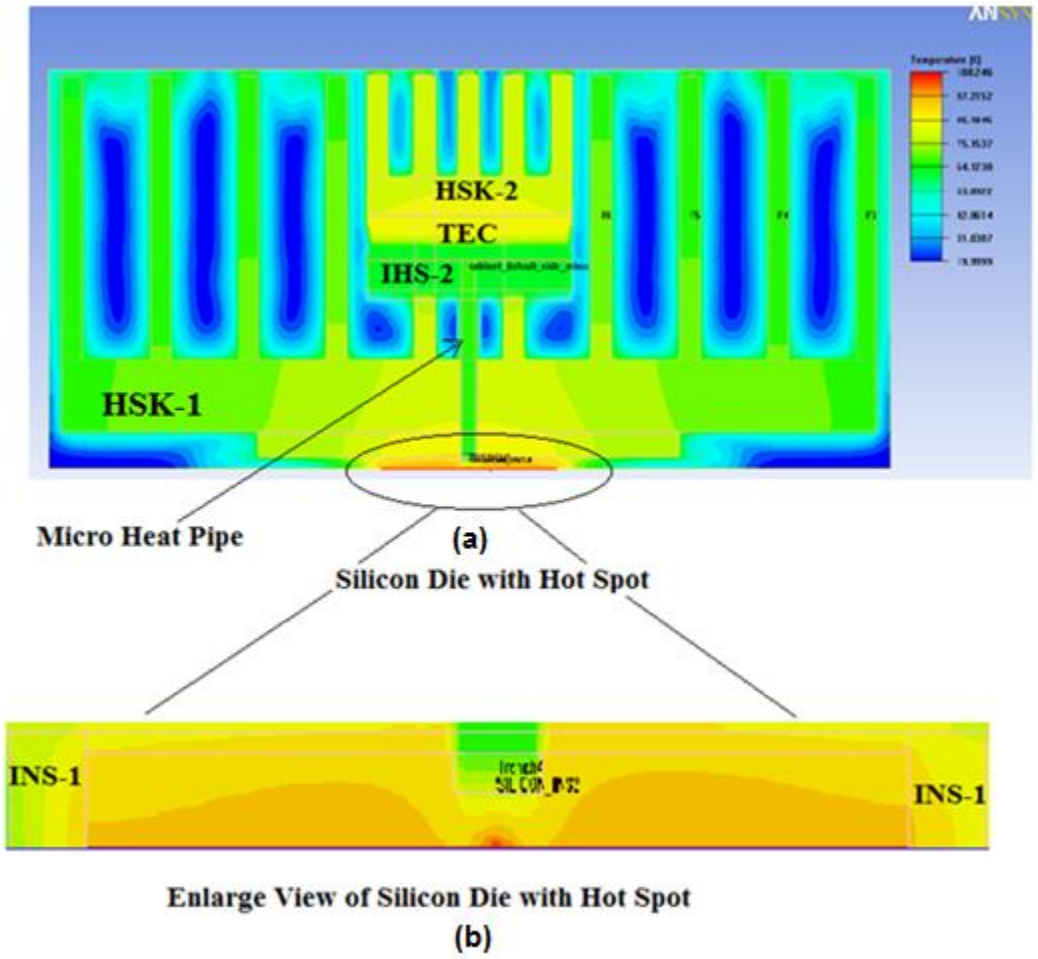


Figure 5.19 (a) Temperature profile in the direction perpendicular of air flow for chip package with micro heat pipe TEC and trench with air flow of 2m/s (TEC powered with 2 Amp of current) and (b) enlarge view of silicon die with hot spot

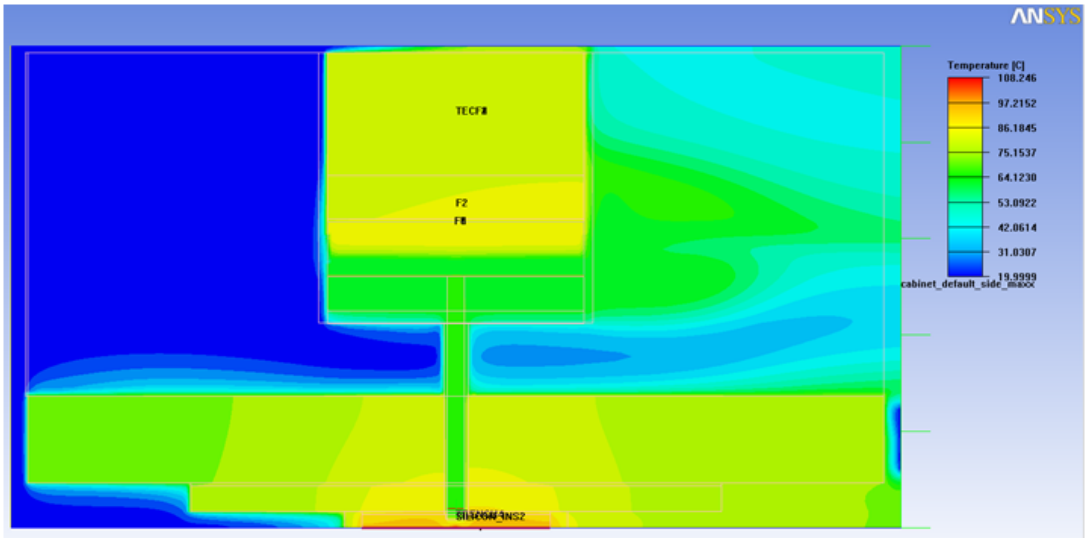


Figure 5.20 Temperature profile in the direction of air flow for chip package with micro heat pipe TEC and trench with air flow of 2m/s and TEC powered with 2 Amp of current.

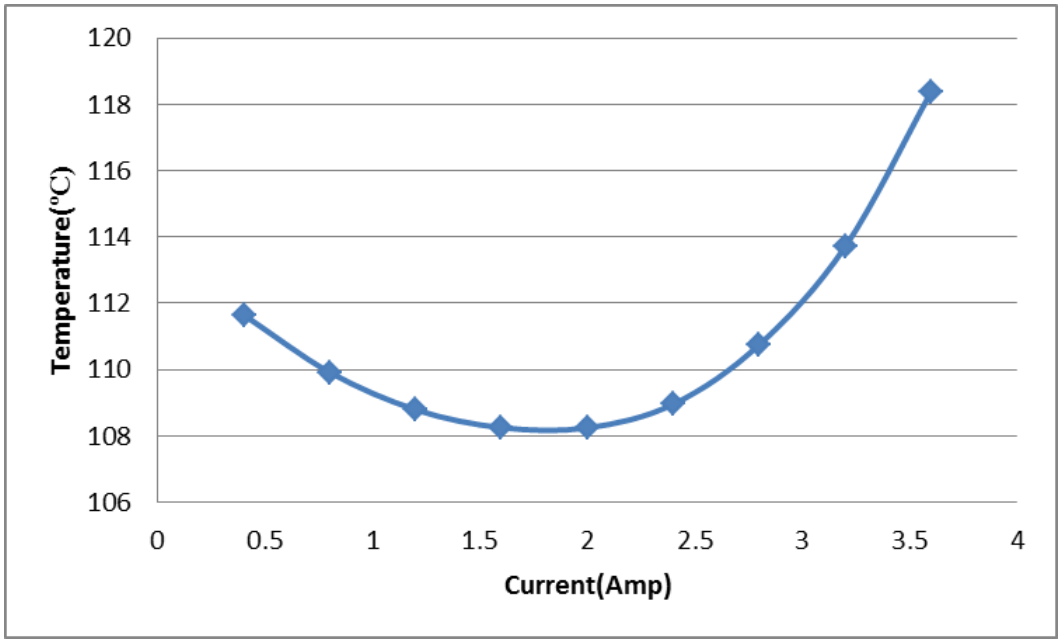


Figure 5.21 Maximum Temperature in Hot Spot Versus Current in TEC. Chip Package with MHP, TEC and trench (300µm).

As shown in Figure 5.21 when TEC was powered at 2Amp of current the hot-spot temperature was found to be lowest. It was observed that when the current in the TEC was

increased the cooling performance increases but after the optimum current the cooling becomes ineffective and the temperature of the hot-spot increases with increase in current. The efficiency of TEC decreases after the optimum current because heat generated inside the TEC from Joule's heating increases and even due to high temperature gradient in TEC an additional heat is added to colder side of TEC from hotter side.

5.5 Conclusion and Future Work

5.5.1 Conclusion

In this case study, the concept of micro heat pipe with TEC and trench has been investigated using the CFD based commercial software to cool the hot-spots in silicon die due to localized high heat flux. Based on numerical results using the micro heat pipe, TEC and trench the temperature of hot-spot was reduced by around 20ºC when compared to the conventional cooling techniques. The chip package with and without trench was also compared and it was found that with trench showed a temperature decrease of around 4ºC. Trench helps in reducing the parasitic heat load from the surrounding die and hence enhances the cooling in localized high heat flux area. Hence, using the micro heat pipe with TEC and trench gives an optimum solution for hot-spots removal in IC's without violating the real state allocated in the mother board.

5.5.2 Future work

In future along with thermal analysis structural analysis can be done to study the structural expects of design along with thermal analysis. Even thermal and power cycling can be done in future to study the reliability of the thermal solution of hot spot cooling using TEC and micro heat pipe along with trench.

CHAPTER 6

ANALYSIS OF FLIP CHIP WITH EMBEDED THIN FLIM THERMOELECTRIC COOLER FOR HOT SPOT COOLING: THERMAL AND STRUCTURE

David S. Chau al el. [28] proposed the technique of cooling the hot spots using thin film thermoelectric cooler directly over the hot spot but structural expects of the design was not considered. In this case study the hot spot cooling techniques with thin film thermoelectric cooler embedded in integrated heat spreader and in the silicon die itself was studied both from thermal and structural aspects.

The case study was done for the flip chip ball grid array (FCBGA) package as shown in Figure 6.3, Figure 6.4 and Figure 6.5. Figure 6.1 and Figure 6.2 shows pictures of flip chip ball grid array.

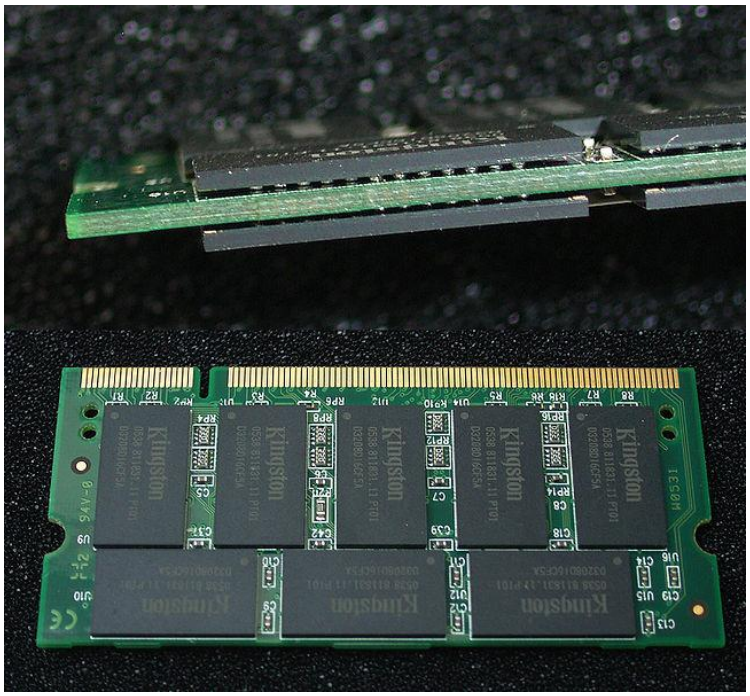


Figure 6.1 Flip chip BGA assembled on PCB [38]

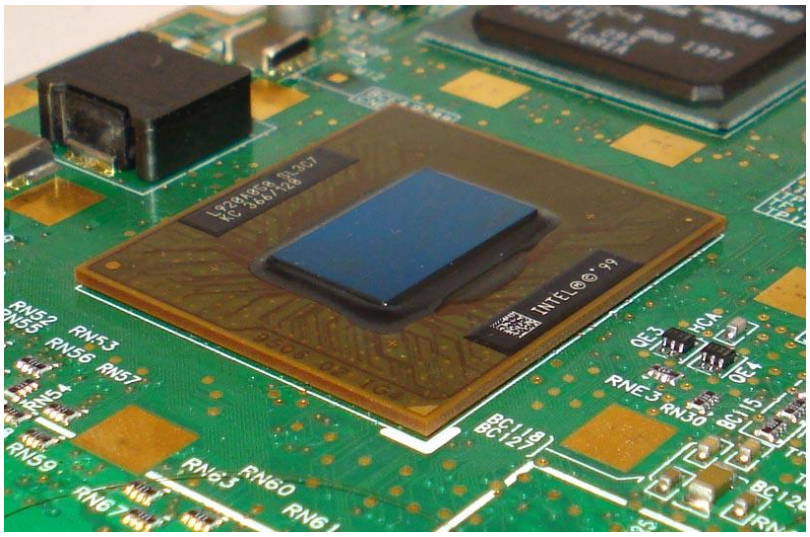


Figure 6.2 Intel mobile celeron in a BGA2 package (FCBGA-479) [38]

6.1 Chip Package Description

The typical architecture of a flip chip microprocessor is presented in Figure 6.3. The chip package consists of heat sink (HSK), thermal interface material (TIM-1 and TIM-2), integrated heat spreader (IHS), die, under fill and solder bumps, substrate, copper pads, solder balls and printed circuit board (PCB).

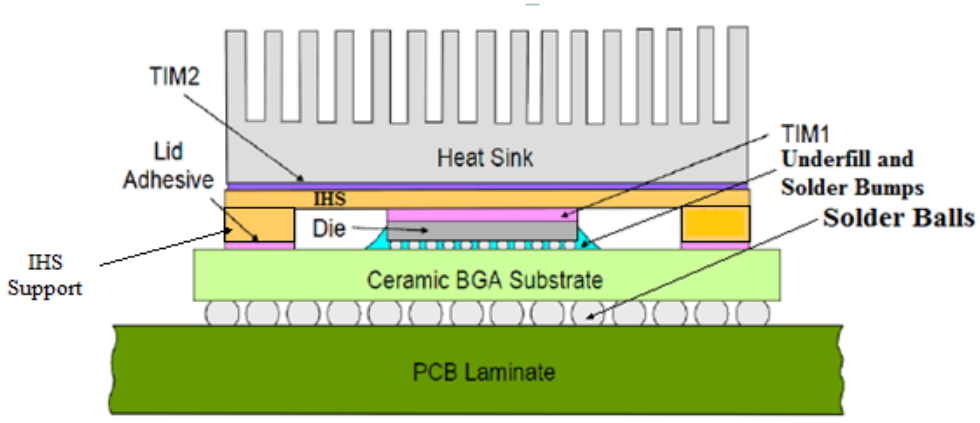


Figure 6.3 Conventional chip package (Case-I)

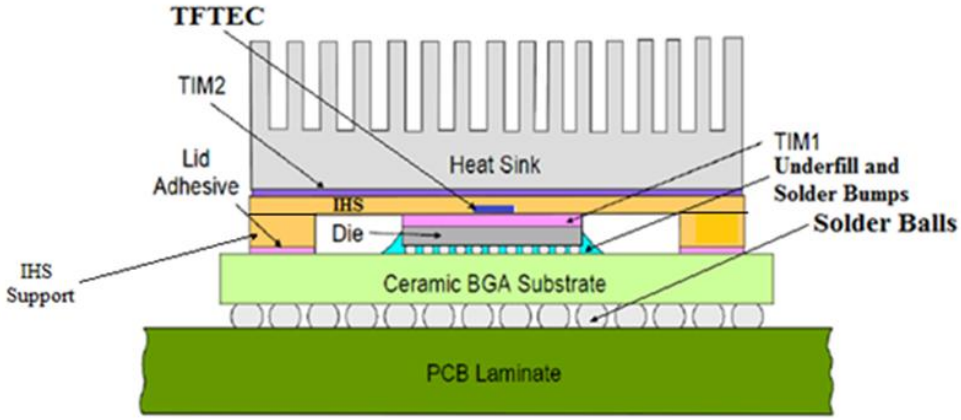


Figure 6.4 Chip package with TFTEC embedded in the IHS (Case-II)

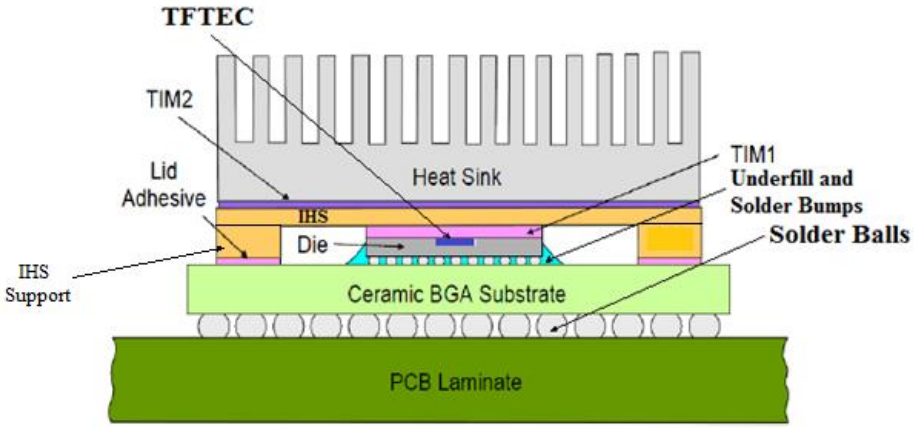


Figure 6.5 Chip package with TFTEC embedded in die (Case-III)

As shown in Figure 6.4 and Figure 6.5 when TFTEC were embedded in the IHS and die respectively for eliminating the hot spots form the chip package.

6.2 Modeling Methodology

6.2.1 Modeling of chip package

The chip package along with TFTEC was modeled in ANSYS Workbench DesignModeler. As shown in Figure 6.7, background heat of 90W was supplied to bottom face of the silicon die and 1.75W heat was supplied to 400µm x 400µm area at the center of the bottom face of the silicon die to create the hot spot. Power supplied to this background heat and hot spot represents the heat generated by the transistors on the active side of the silicon chip. An effective heat transfer coefficients of 720W/m^{2}K was applied to the top face of the heat sink (HSK), including the effects of the heat sink fins, imposed as a boundary condition on the heat sink. Ambient temperature of the chip package was taken as 22^{o}C. Figure 6.6 shows the model of complete chip package in ANSYS Workbench.

It is unnecessary and impractical to model each and every layer of the chip package, so some features can be ignored or combined so that model runs faster [36]. Effective properties were taken for solder bump and under fill [36].

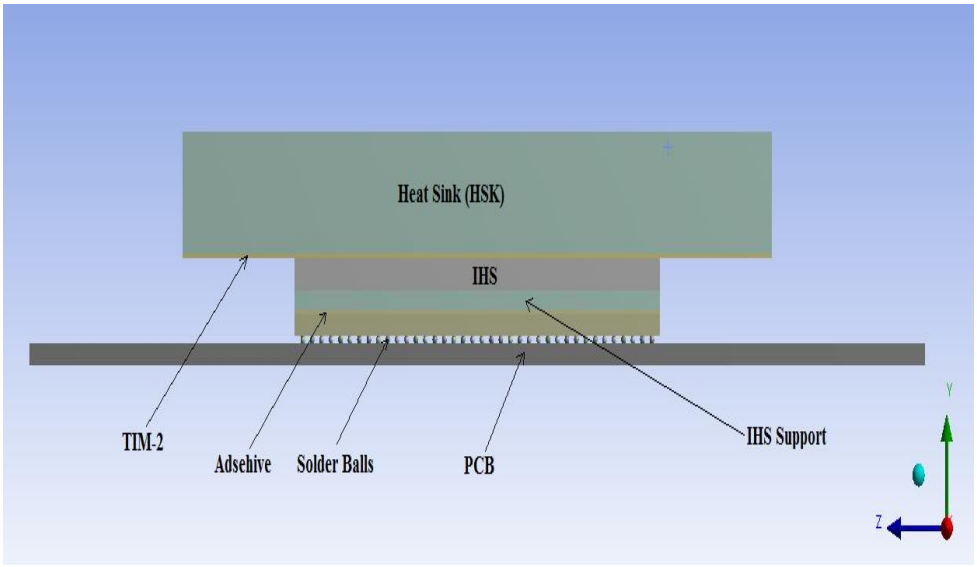


Figure 6.6 Complete chip package in ANSYS Workbench DesignModeler (X-axis outwards)

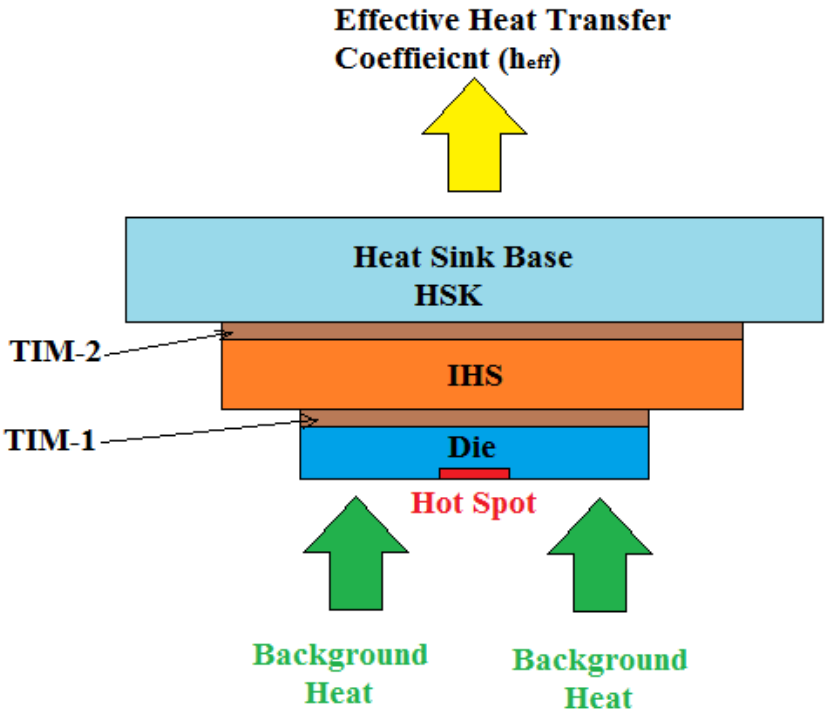


Figure 6.7 Boundary conditions in chip package

Assumptions in modeling

- All component of the chip package were considered to be in perfect contact with each other
- The current carrying conductor and all thermoelectric elements were considered to be perfectly insulated electrically
- Effective heat transfer coefficient was given only at the top of the heat sink with represents the forced convection

The solder balls were arranged in numbers as 38 x 38 in a square format and Cu-pads were placed at top and bottom of the solder balls. The other properties of solder balls and copper pads are given in Table 6.1 and Table 6.2.

Geometry parameters numeric model are listed in table.6.1 unless otherwise noted.

Table 6.1 Geometry of numerical model

Model Component	Geometry (w x l x h)
Die	13mm x 11mm x 750µm
TIM-1	13mm x 11mm x 175µm
IHS	31mm x 31mm x 1.5mm
TIM-2	31mm x 31mm x 175µm
HSK	50mm x 50 mm x 5.5mm
Under fill and Solder bump	13mm x 11mm x 0.1mm
PCB	76mm x 76mm x 1mm
Substrate	31mm x 31mm x1mm
Solder ball	diameter = 0.3mm, height = 0.28mm and pitch =0.8mm
Copper pad	thickness = 0.03mm

Table 6.2 Material properties of numerical model

Model Component	E(GPa)	CTE(1/°K)	K(W/mK)	υ
Die	150	$3x10^{-6}$	150 @ 298.15°K 100 @ 373.15°K	0.3
TIM-1	$4x10^{-4}$	$1.75x10^{-4}$	30	0.28
IHS	121	$1.73x10^{-5}$	385	0.3
TIM-2	$4x10^{-4}$	$1.75x10^{-4}$	30	0.28
HSK	68	$2.40x10^{-5}$	247	0.3
Under fill and Solder bump	14.5	$2x10^{-5}$	1.3	0.28
PCB	21.9 (X or Z); 9.99 (Y)	$17x10^{-6}$ (X or Z); $70x10^{-6}$(Y)	13	0.28
Substrate	25.99 (X or Z); 11(Y)	$17x10^{-6}$ (X or Z); $52x10^{-6}$(Y)	3	0.39 & 0.11
Solder ball	41	$2.21x10^{-5}$	57	0.36
Copper pad	121	$1.73x10^{-5}$	385	0.3

6.2.2 Modeling of heat spreader

The four sided heat spreader was modeled with width of integrated heat spreader support (IHS support) to be 5mm as shown Figure 6.8 and Figure 6.9. Copper was used as a material for IHS support. The material properties for the IHS support are the same as the material properties of copper pad as given in Table 6.2. Lid adhesive as shown in Figure 6.3, Figure 6.4 and Figure 6.5 has the thickness of 0.1mm with young modulus of elasticity 7GPa, coefficient of thermal expansion $4.8x10^{-5}$ $1/^{o}K$, poison's ratio 0.35 and thermal conductivity 0.2W/mK.

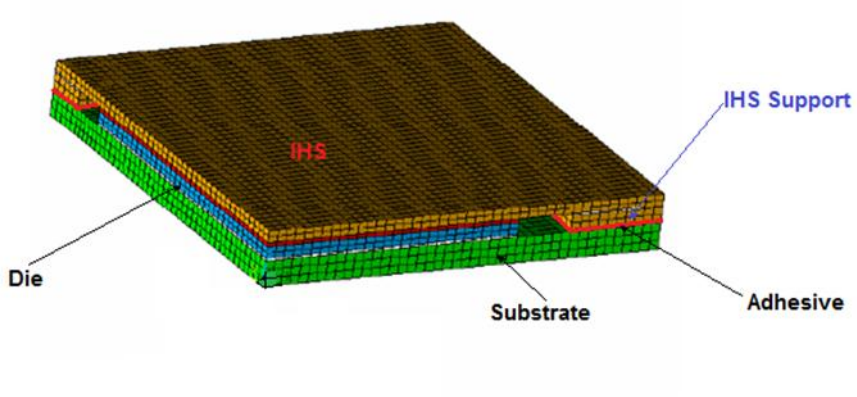


Figure 6.8 Quarter symmetric model of chip package with four sided heat spreader

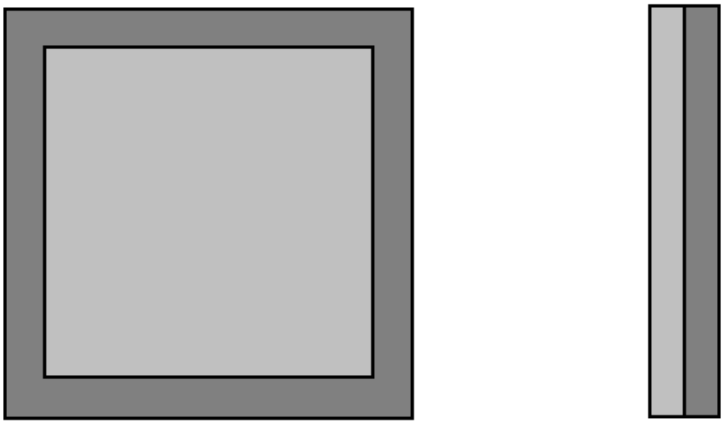


Figure 6.9 Four sided heat spreader

6.2.3 Modeling of thin film thermoelectric cooler

The 3D numerical model of thermoelectric cooler created in ANSYS Workbench. The thermoelectric cooler was made with 49 thermoelectric couple; each pair thermoelectric couple consists of p-type semiconductor and n-type semiconductor connected electrically in series and thermally in parallel connected by a current carrying copper conductor at top and bottom. Thermoelectric element is connected to the current carrying copper conductor by a solder joint as shown in the Figure 6.10.

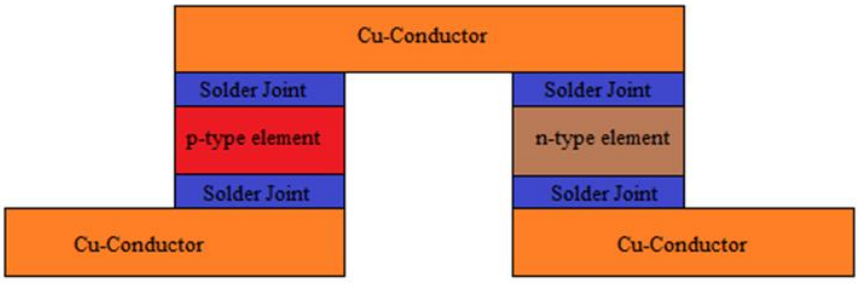


Figure 6.10 Single thermoelectric couple.

Table 6.3 Geometry of numerical model of thin film thermoelectric cooler

Model Component	Geometry (w x l x h)
p-type and n-type semiconductor	0.15mm x 0.15mm x 20μm
Solder Joint	0.15mm x 0.15mm x 10μm
Cu-conductor	0.32mm x 0.32mm x 30μm

Table 6.4 Thermoelectric properties of p-type semiconductor and n-type semiconductor

Model Component	Material	Seebeck Coefficient (μV/K)	Electrical Resisitvity (ohm x m)
n-type element	Bi_2Te_3	-240	$9x10^{-6}$
p-type element	Sb_2Te_3	185	$3.5x10^{-6}$

Table 6.5 Material and electrical properties of different elements of thermoelectric cooler

Model Component	E(GPa)	CTE(1/°K)	K(W/mK)	υ	Electrical Resisitvity (ohm x m)
p-type element	4.8	$14.4x10^{-6}$	1.5	0.3	$9x10^{-6}$
n-type element	4.8	$14.4x10^{-6}$	0.5	0.3	$3.5x10^{-6}$
Solder Joint	41	$2.21x10^{-5}$	57	0.36	$1x10^{-7}$
Cu-Conductor	121	$1.73x10^{-5}$	385	0.3	$1.68x10^{-8}$

As shown in Figure 6.11 the current tap and voltage tap has the dimensions of 0.371mm x 0.2mm x 0.03mm, both current tap and voltage tap are made of copper with material properties as mention in Table 6.5 for Cu-conductor. As shown in Figure 6.11, side Cu-conductors has the dimensions of 0.683mm x 0.15mm x 0.03mm and the dimensions of both current conductor and earthling conductor are 0.32mm x 0.15mm x 0.03mm. Spacing between each copper conductor is 0.04mm.

The space between different elements of thermoelectric cooler was filled with TEC mold, having the outer dimensions of 2.6mm x 2.6mm x 0.100mm. TEC mold as shown in

Figure 6.12 has a young modulus of elasticity 7GPa, coefficient of thermal expansion 4.8×10^{-5} ppm/^{o}C, poison's ratio 0.35 and thermal conductivity 0.2W/mK.

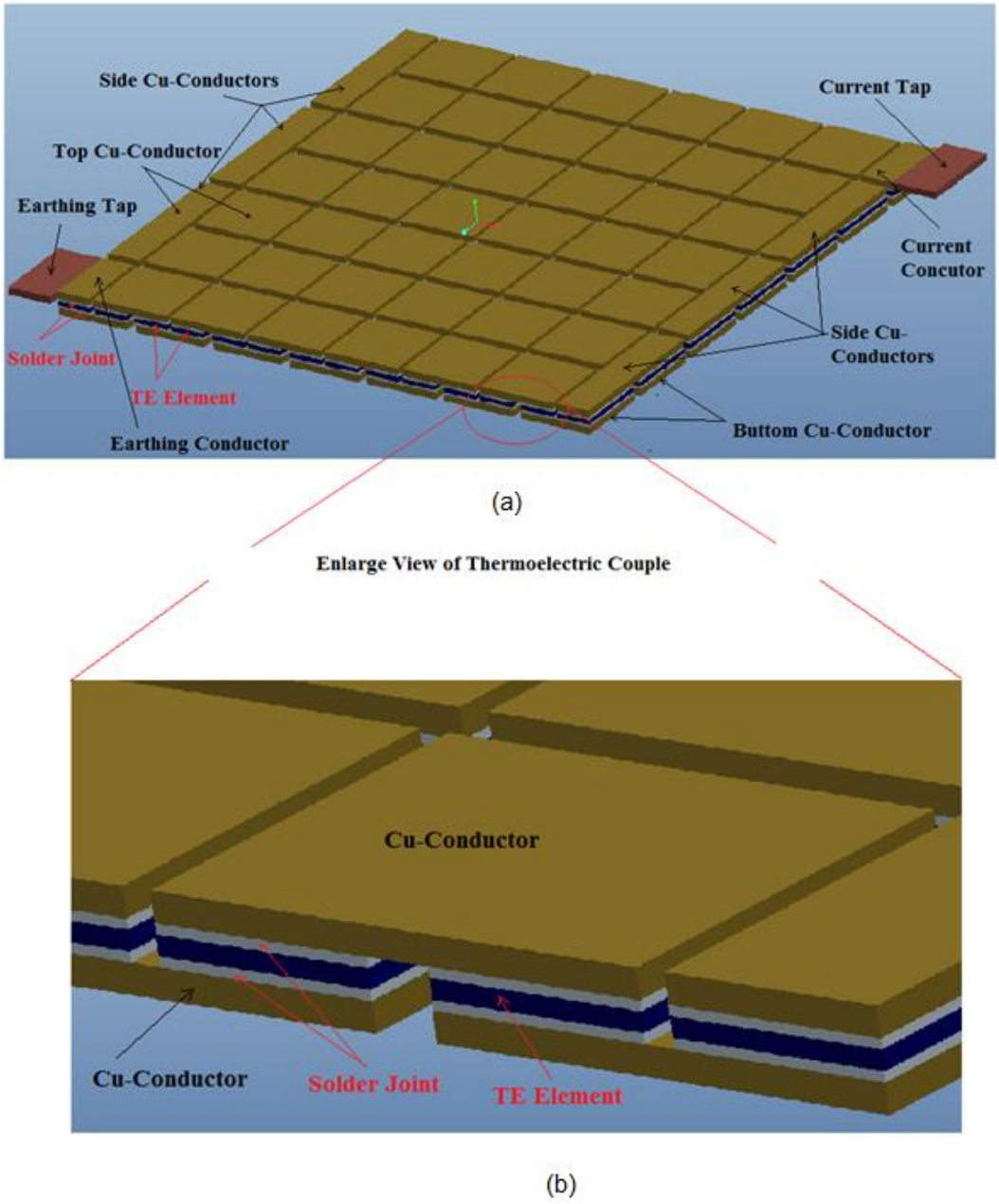


Figure 6.11 (a) Isometric view of thin film thermoelectric cooler in Pro/E and

(b) enlarged view of thermoelectric couple

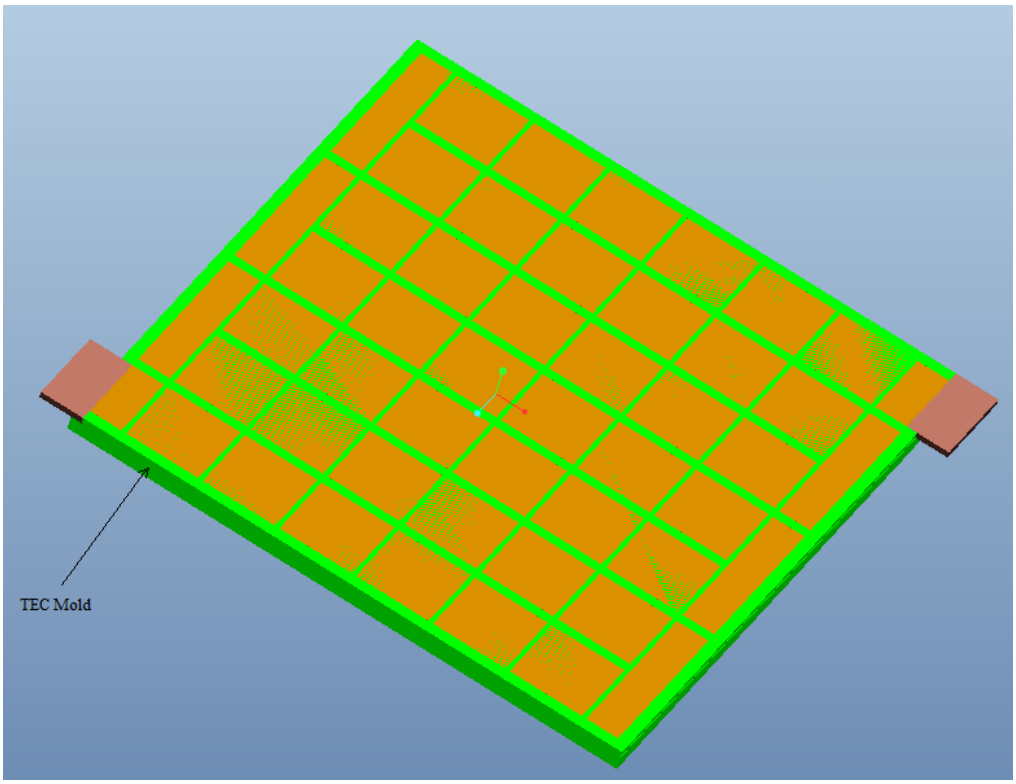


Figure 6.12 Isometric view of thin film thermoelectric cooler with TEC Mold in Pro/E

As shown in Figure 6.13 and Figure 6.14, when TFTEC was embedded in the IHS, Cu-conductors were used to supply current in the TEC. The dimensions of the Cu-conductors as shown in Figure 6.14 are

W = 0.371mm

T = 0.03mm

L1 = 14.2mm

L2 = 0.15mm and

H = 0.07mm

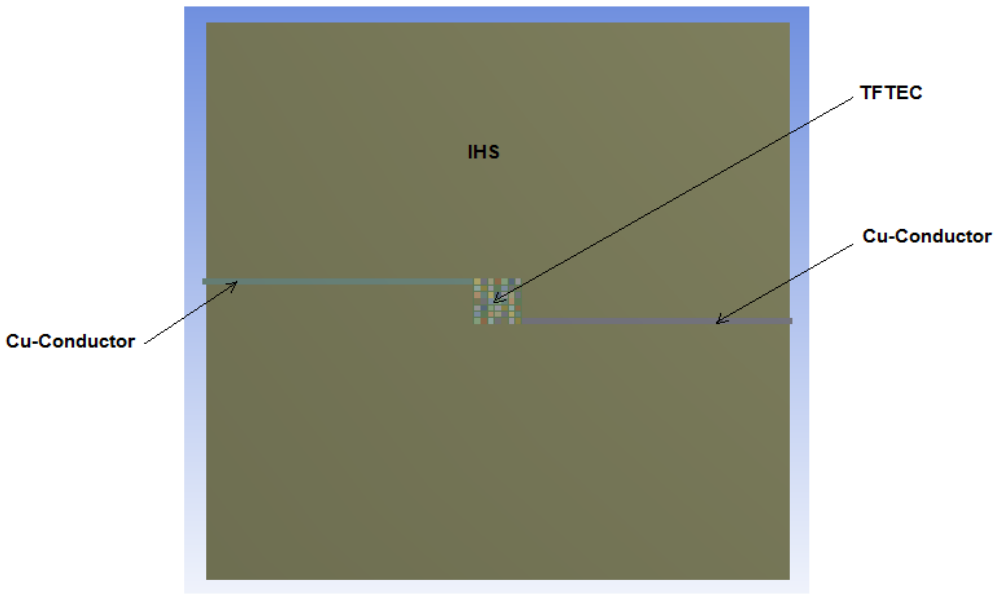


Figure 6.13 TFTEC embedded in IHS along with Cu-Conductors to supply current in TFTEC (Bottom view in ANSYS Workbench)

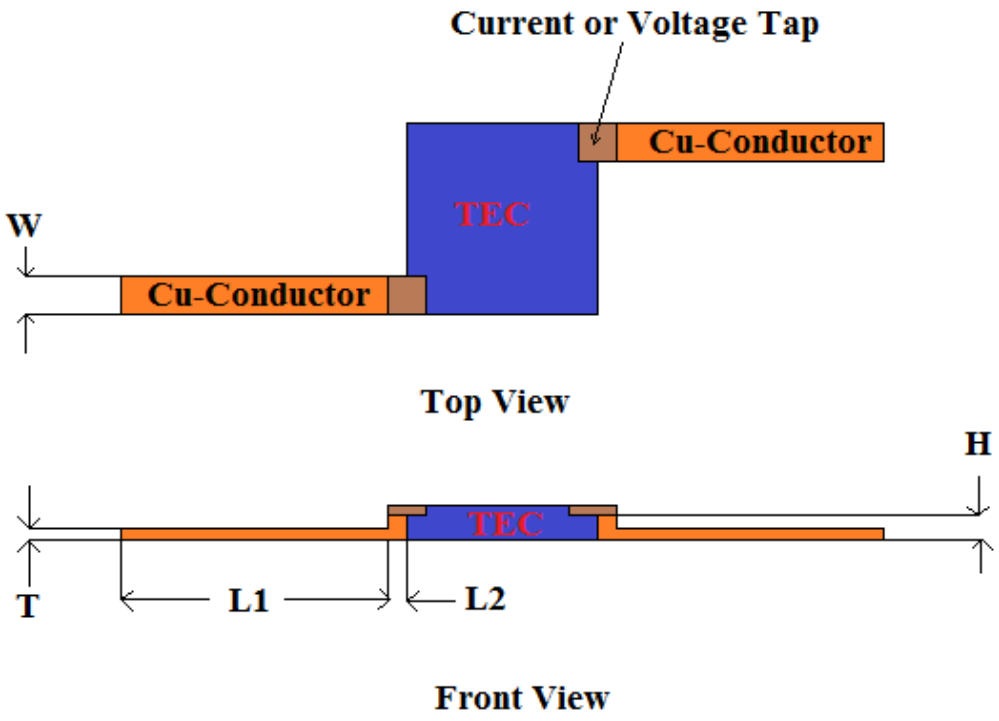


Figure 6.14 Cu-conductors to supply current in TFTEC, when TFTEC was embedded in IHS

(Figure not to scale)

When TFTEC was embedded in the silicon die to supply current or power in TFTEC Cu-conductors was used as shown in the Figure 6.15 and Figure 6.16. Dimensions of the Cu-conductors as shown in Figure 6.16 are

W2 = 0.371mm

T2 = 0.03mm

LL = 4.15mm

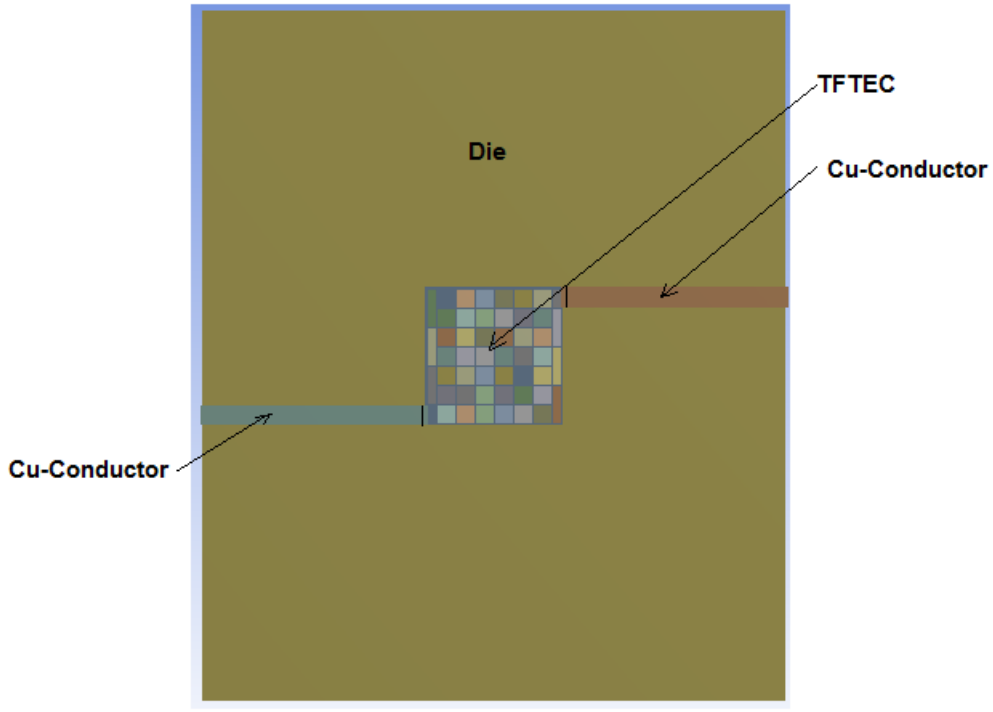


Figure 6.15 TFTEC embedded in silicon die along with Cu-Conductors to supply current in TFTEC (Top view in ANSYS Workbench)

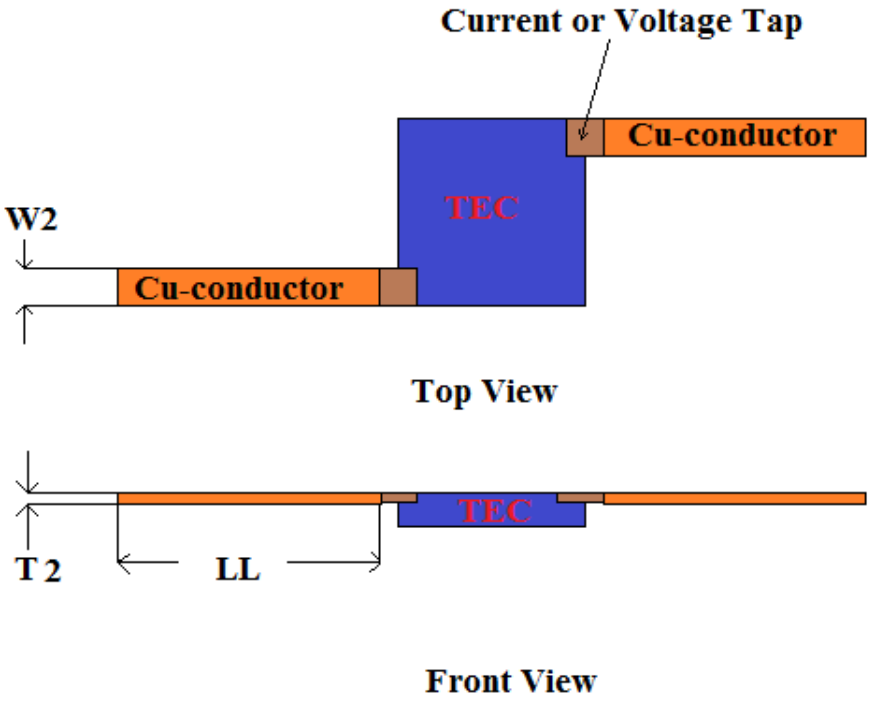


Figure 6.16 Cu-conductors to supply current in TFTE when TFTEC was embedded in the silicon die (Figure not to scale)

6.3 Mesh

TFTEC was meshed separately as compared to the mesh in other components of the chip package. Each edge of component of TFTEC was divided into 5 elements, while the mold was meshed separately relative to the mesh in the components of TFTEC.

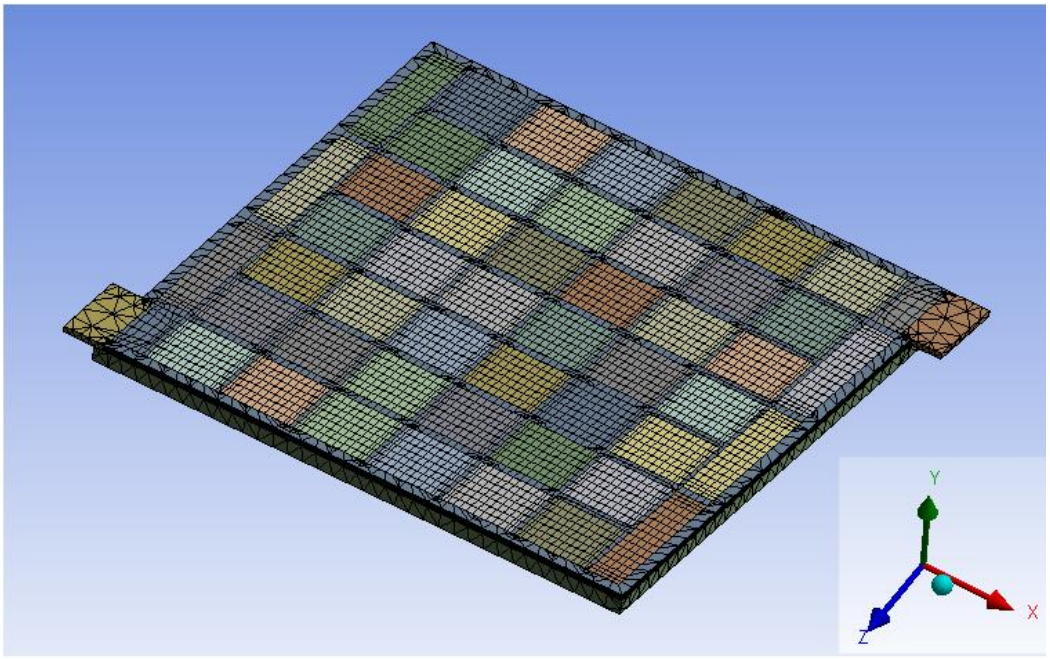


Figure 6.17 Mesh in TFTEC and TEC mold in ANSYS Workbench

Fine mesh was created in the entire chip package with mesh relevance selected as 26. The minimum edge length for the mesh was selected as 1.0×10^{-6}m. The Figure 6.17 shows the mesh in the entire chip package.

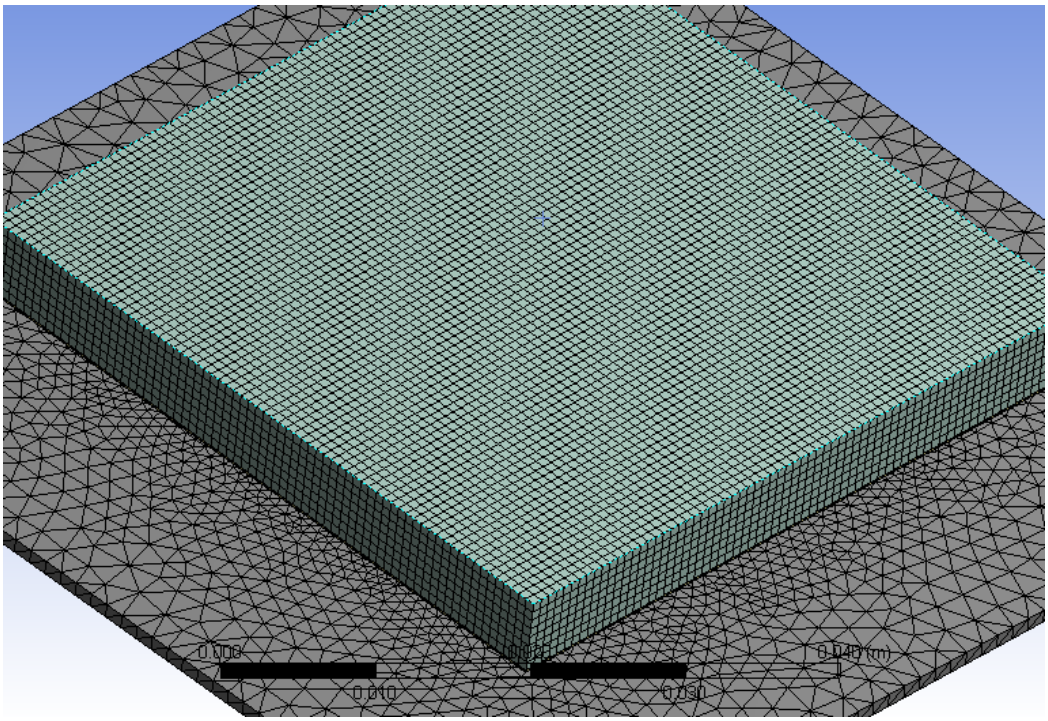


Figure 6.18 Mesh in the chip package in ANSYS Workbench

6.4 Results and Discussion

6.4.1 Thermal analysis

In case-I for conventional flip chip package with hot spot and without TFTEC the maximum junction temperature found to be around 122°C. In case-II for TFTEC embedded in the HIS of chip package and operated at current of 5Amp, maximum junction temperature was found to be around 108°C. In case-III when TFTEC was embedded in the silicon die and operated at current of 5Amp, maximum junction temperature was found to be around 106°C. Figure 6.19, Figure 6.20 and Figure 6.21 shows the temperature profile in active side of silicon die (bottom view) for case-I, case-II and case-III respectively.

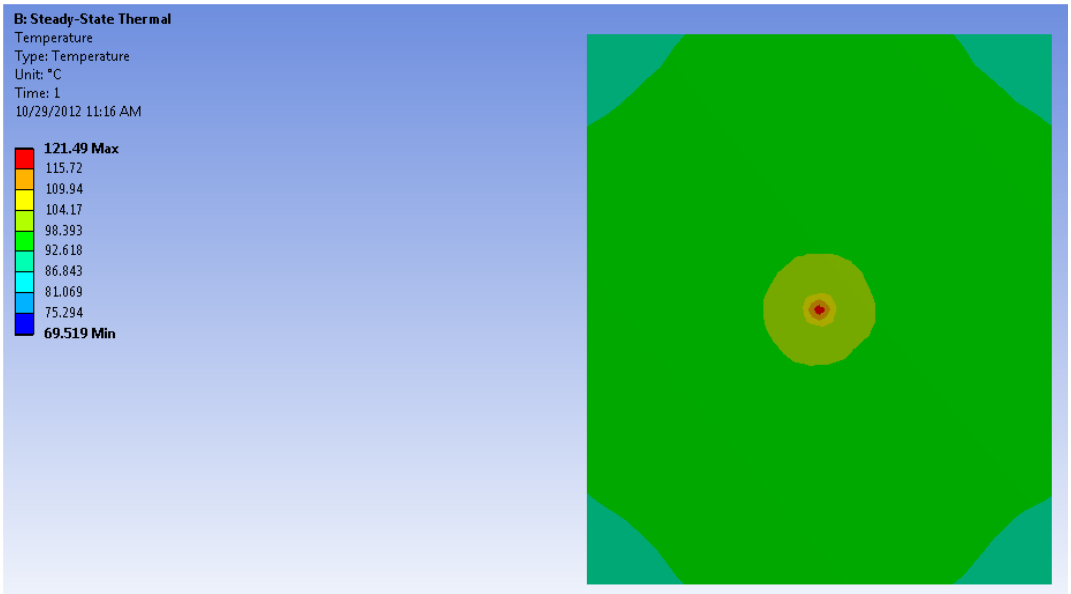


Figure 6.19 Temperature profile in active side of die (a) for conventional chip package with hot spot (Case-I)

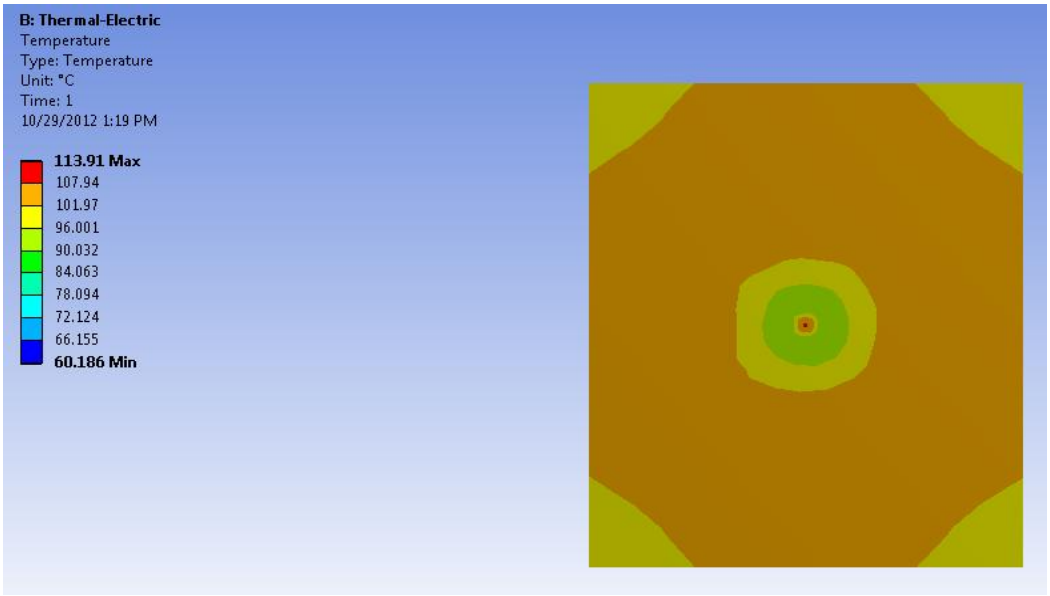


Figure 6.20 Temperature profile in active side of die (a) for conventional chip package with hot spot (Case-I), (b) for conventional chip package with hot spot and TFTEC embedded in IHS (Case-II), (TFTEC operated at current of 5Amp)

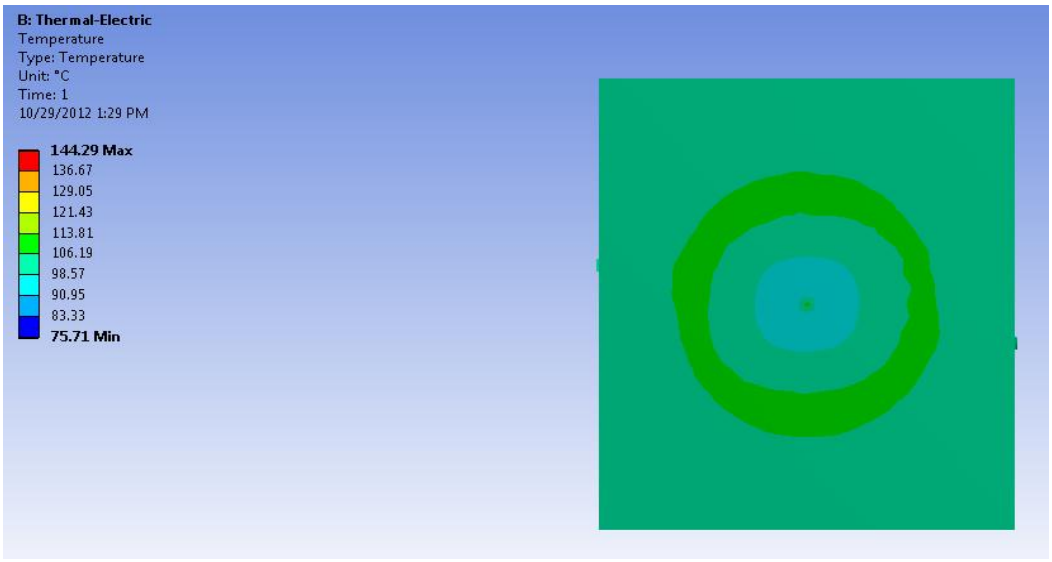


Figure 6.21 Temperature profile in active side of die for conventional chip package with hot spot and TFTEC embedded in die (Case-III), (TFTEC operated at current of 5Amp)

It was observed from Figure 6.22, that when the current in the TFTEC was increased the cooling performance increases but after the certain current the cooling becomes ineffective and the temperature of the hot-spot increases with increase in current. The efficiency of TFTEC decreases after the certain value of current because heat generated inside the TFTEC from Joule's heating increases and even due to high temperature gradient in TFTEC an additional heat is added to colder side of TFTEC from hotter side.

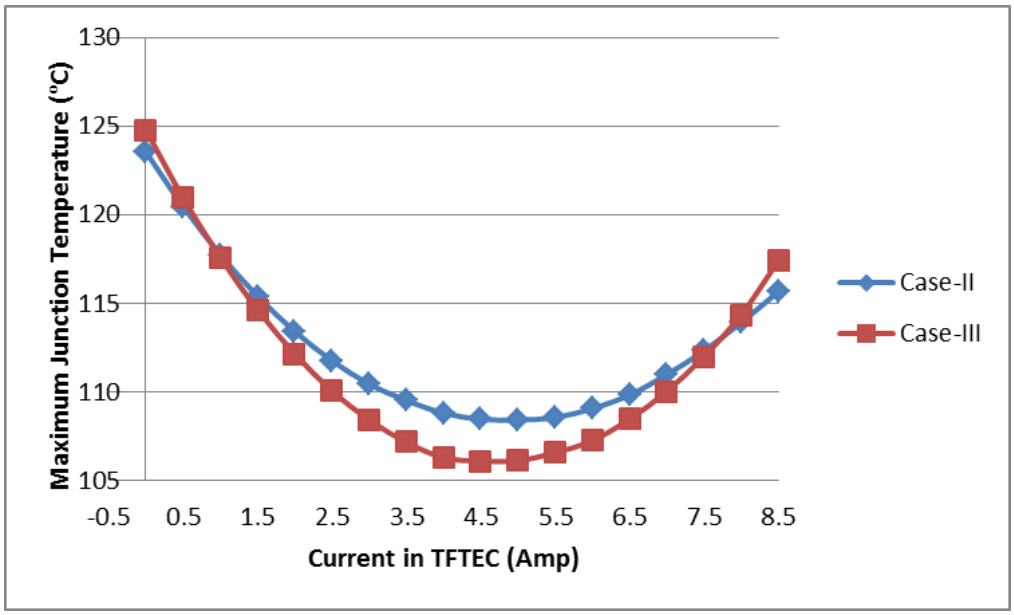
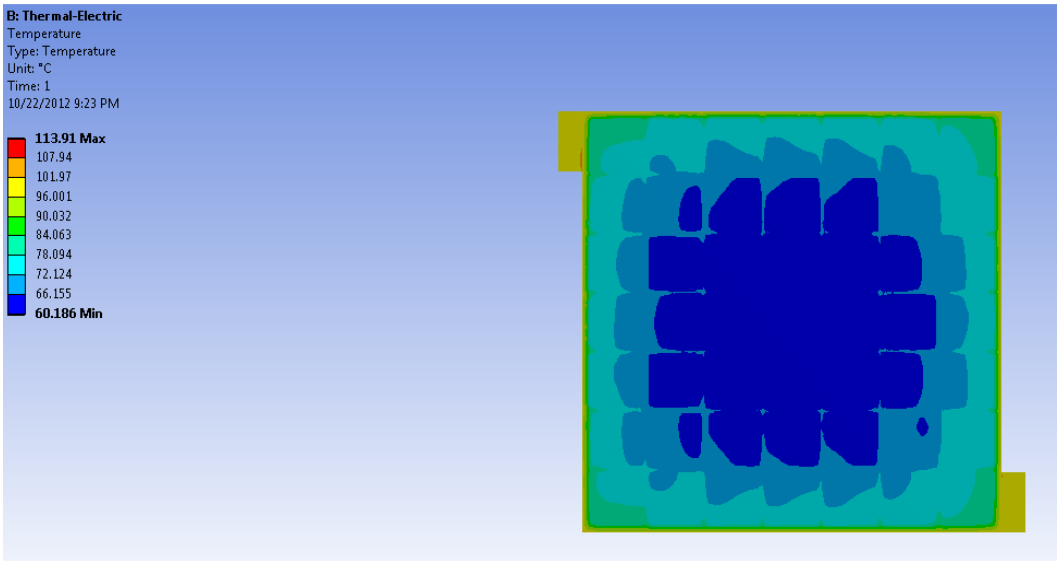
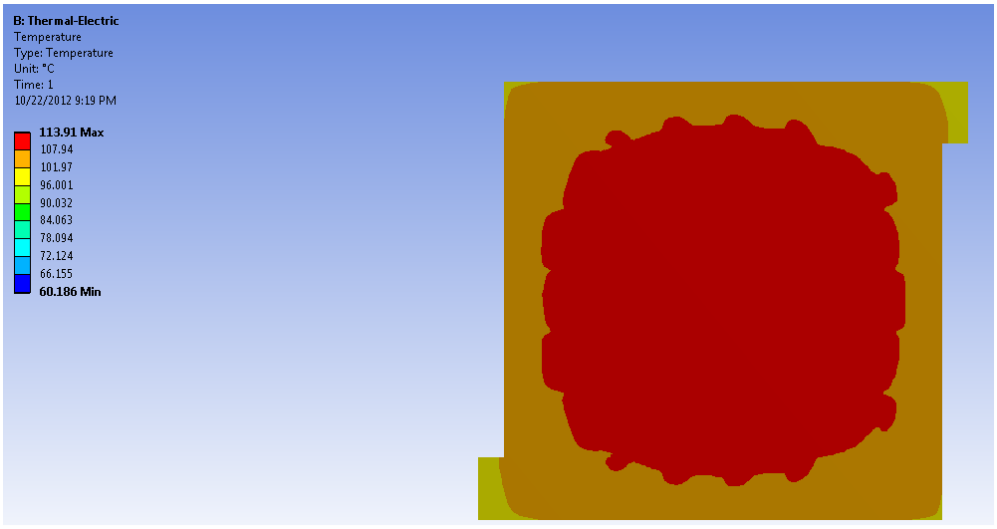


Figure 6.22 Plot of current in TFTEC v/s maximum junction temperature in the chip for case-II (when TFTEC was embedded in IHS) and case-III (when TFTEC was embedded in silicon die)

In case-II when TFTEC was embedded in IHS, though the maximum junction temperature was reduced to 108^{o}C, but still the overall maximum temperature of the chip package was found to be around 114^{o}C, which was at hot side of TFTEC as shown in Figure 6.23 (b) . In case-III when TFTEC was embedded in silicon die though the maximum junction temperature was reduced to 106^{o}C, overall maximum temperature in the chip package was found to be 144^{o}C which was at hot side of TFTEC as shown in Figure 6.24 (b). Figure 6.23 and Figure 6.24 shows the temperature profile in cold and hot side of TFTEC for case-II and case-III respectively, when TFTEC was operated at a current of 5Amp.

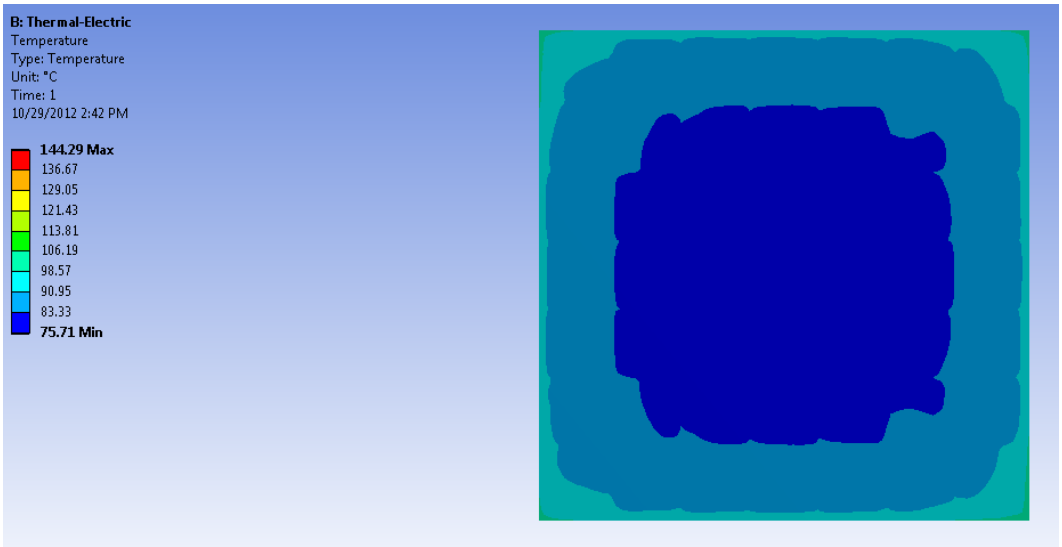


(a)

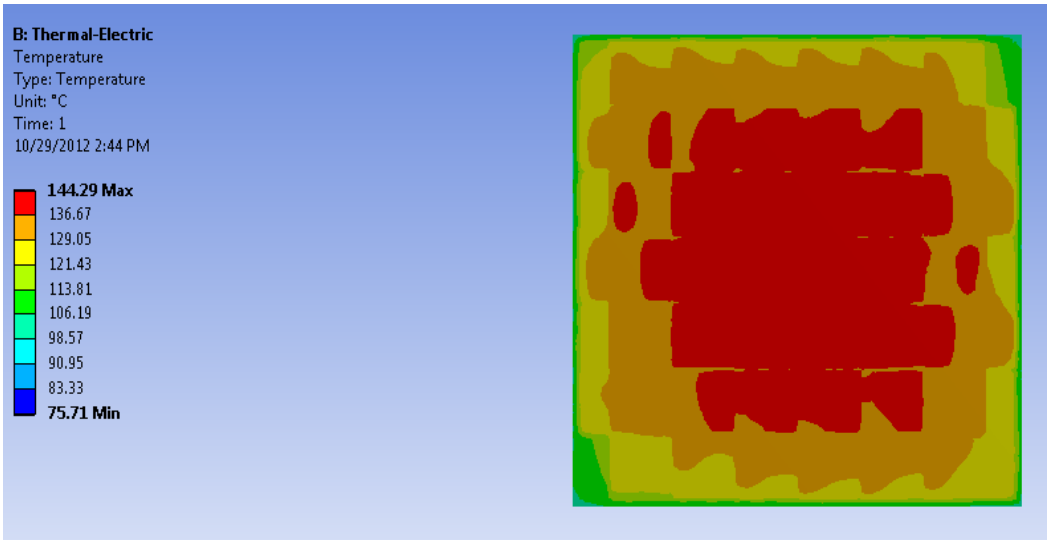


(b)

Figure 6.23 Temperature profile of TFTEC when TFTEC was embedded in IHS (a) bottom view showing colder side of TFTEC and (b) top view showing hot side of TFTEC (TFTEC operated at current of 5Amp)

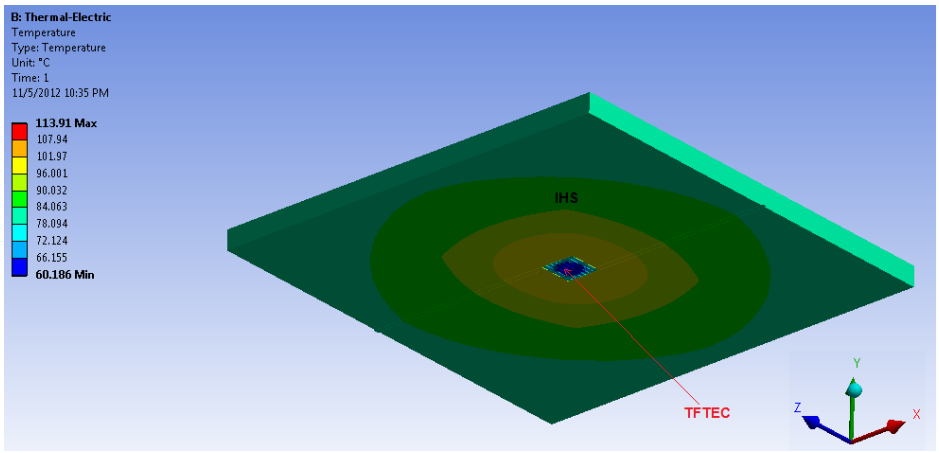


(a)

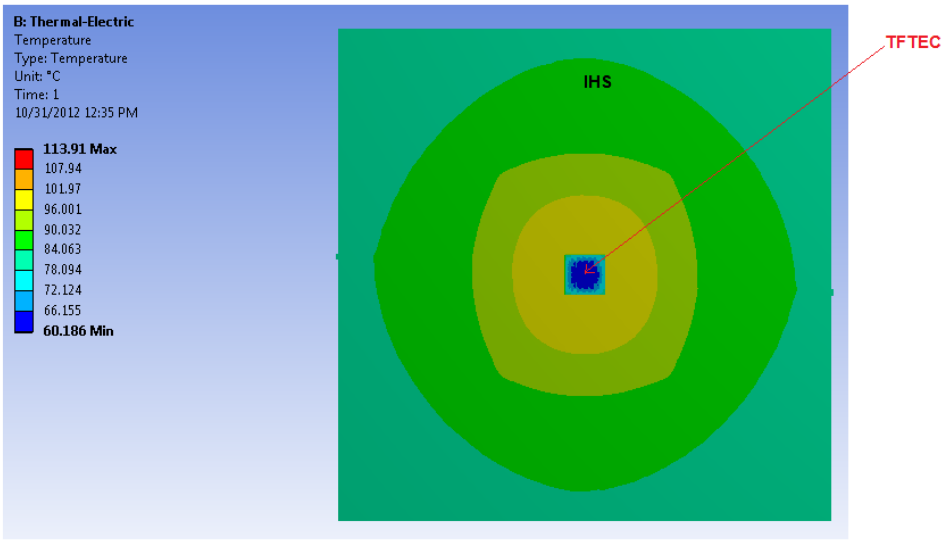


(b)

Figure 6.24 Temperature profile of TFTEC when TFTEC was embedded in silicon die (a) bottom view showing colder side of TFTEC and (b) top view showing hot side of TFTEC (TFTEC operated at current of 5Amp)

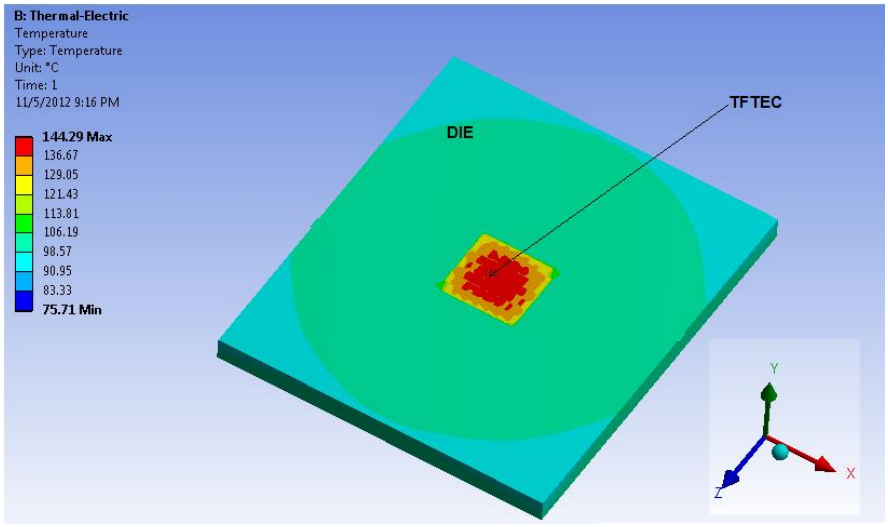


(a)

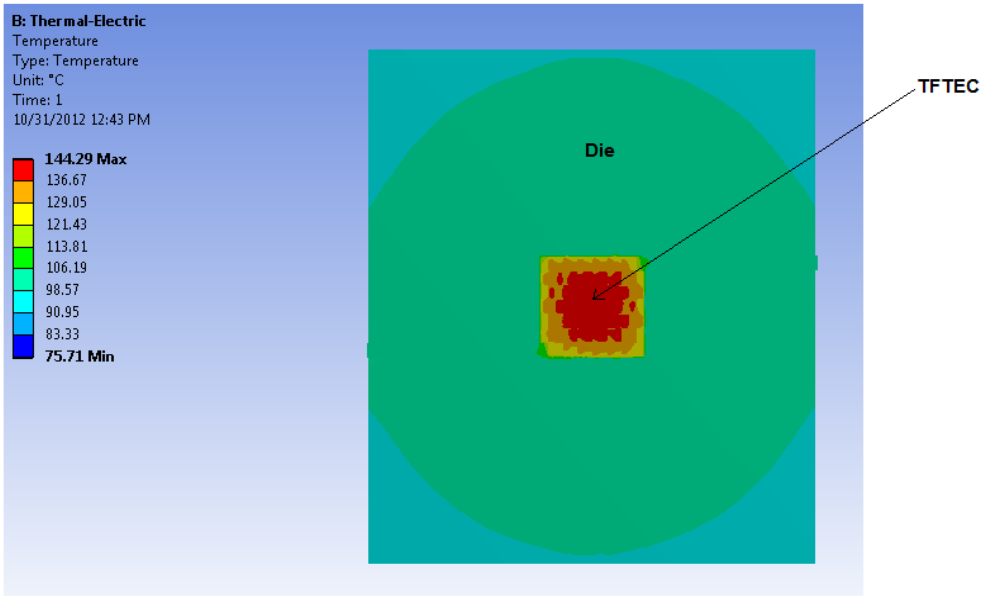


(b)

Figure 6.25 Temperature profiles of IHS and TFTEC embedded in IHS (a) isometric view in ANSYS workbench showing colder side of TFTEC and (b) bottom view in ANSYS workbench showing colder side of TFTEC



(a)



(b)

Figure 6.26 Temperature profiles of die and TFTEC embedded in die (a) isometric view in ANSYS workbench showing hotter side of TFTEC and (b) top view in ANSYS workbench showing hotter side of TFTEC

6.4.2 Structure analysis

For all the three cases as shown in Figure 6.3, Figure 6.4 and Figure 6.5 structure analyses was done to analyze structural expects of design. In flip chip package the there is a bending stress induced in the die. Due to the coefficient of thermal expansion mix match between various components used in the chip package the solder ball and copper pad faces the shear stress (σ_{xy}). The shear stress (σ_{xy}) in solder ball and copper pad and normal stress (σ_y) in the die was compared for all the three cases. TFTEC was operated at current of 5Amp for case-II and case-III.

As shown in Figure 6.27, shear stress was compared for three different cases the value of maximum shear stress in solder balls was found to be highest for case-II which was $1.43x10^7$Pa when TFTEC was embedded in the IHS and was found to be lowest in case-I which was $1.1x10^7$Pa for conventional chip package without TFTEC. Maximum shear stress was found to be $1.26x10^7$ Pa when TFTEC was embedded in die. For all the three cases the maximum shear stress was found to be almost equal in solder balls.

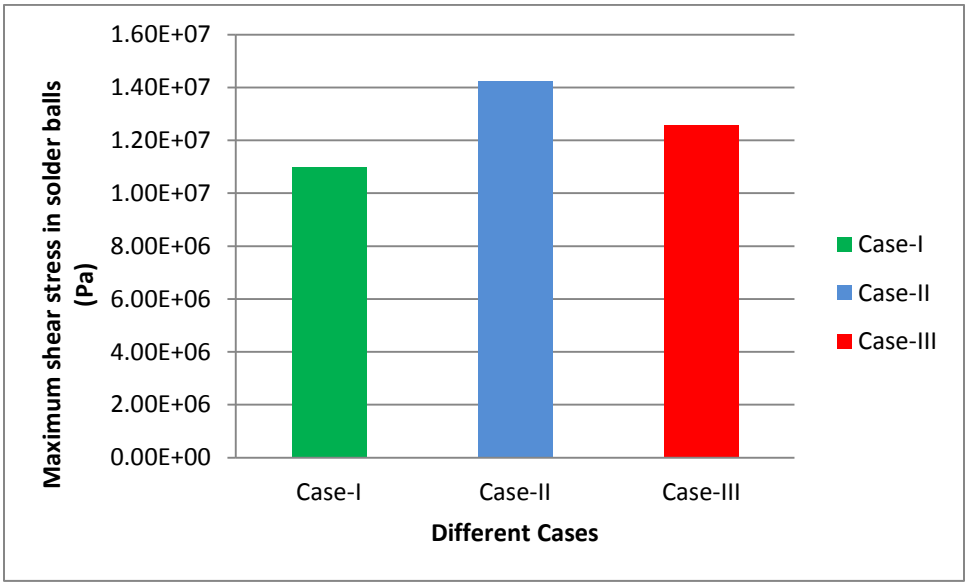


Figure 6.27 Shear stress in solder balls for three different cases

As shown in Figure 6.28, shear stress was compared for three different cases in copper pads and maximum shear stress was found to be highest in case-II, 7.01×10^7Pa when TFTEC was embedded in the IHS. Maximum shear stress in copper pads was found to be lowest for case-I, 4.84×10^7Pa for conventional chip package without TFTEC. Maximum shear stress in copper pads was found to be 6.03×10^7Pa when TFTEC was embedded in die. From the result of all the three cases it can be observed that maximum shear stress value does not differ much.

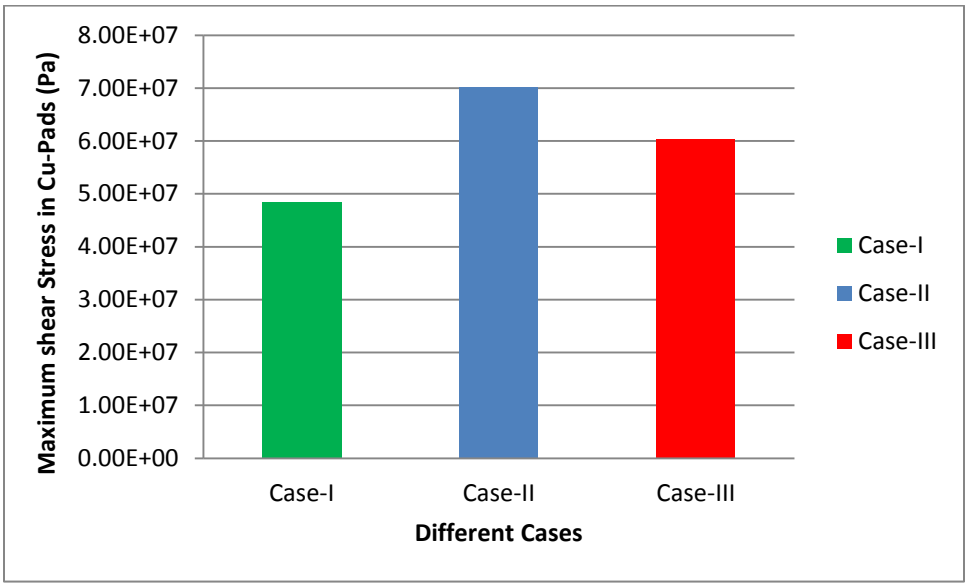


Figure 6.28 Shear stress in copper pads for three different cases

Figure 6.29 gives the comparison of normal stress in the die all the three cases mentioned in Figure 6.3, Figure 6.4 and Figure 6.5. It can be observed form Figure 6.29, Figure 6.30, Figure 6.31 and Figure 6.32 that for case-III when TFTEC was embedded in the die, normal stress in the die was found to be very high which is 1.17×10^8Pa as compared to case-I for conventional chip package where normal stress was found to be 1.21×10^7Pa and for case-II when TFTEC was embedded in IHS, where normal stress in the die was found to be 2.60×10^7Pa.

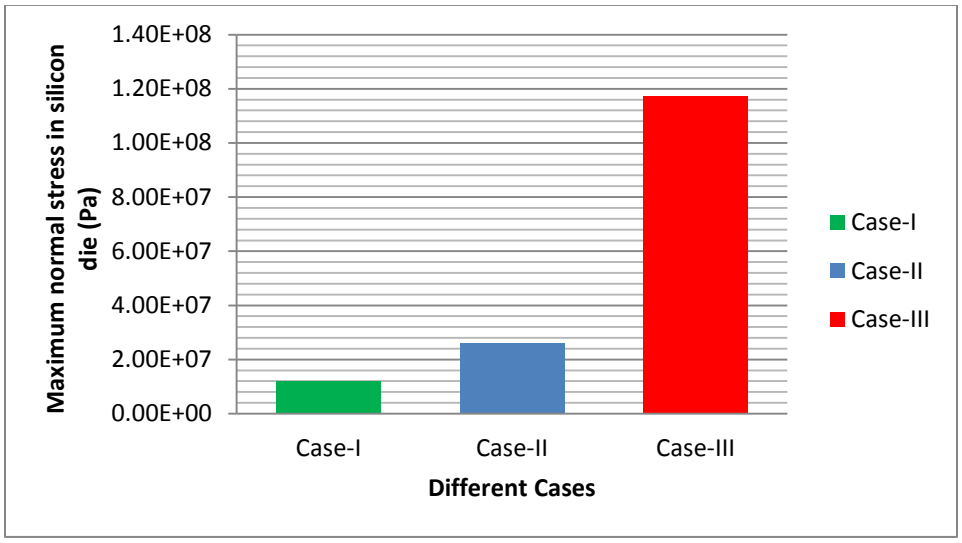


Figure 6.29 Normal stresses in silicon die for three different cases

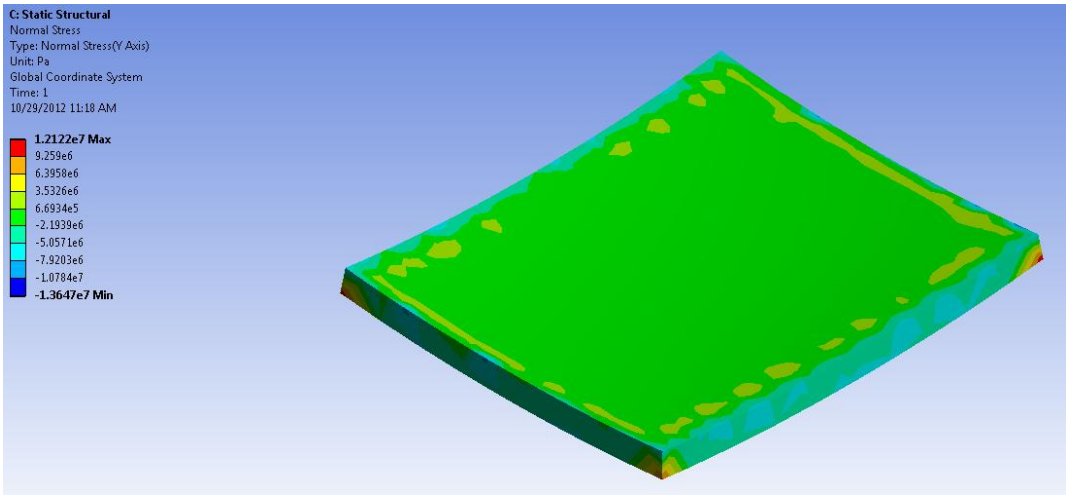


Figure 6.30 Normal stress profile in silicon die for conventional chip package without TFTEC (Case-I)

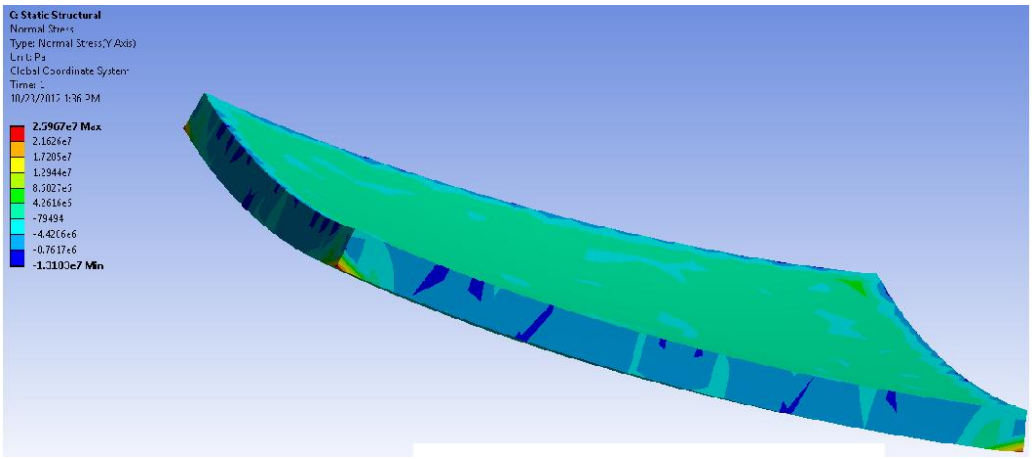


Figure 6.31 Normal stress profile in silicon die for conventional chip package with TFTEC embedded in IHS and operated at current of 5Amp (Case-II)

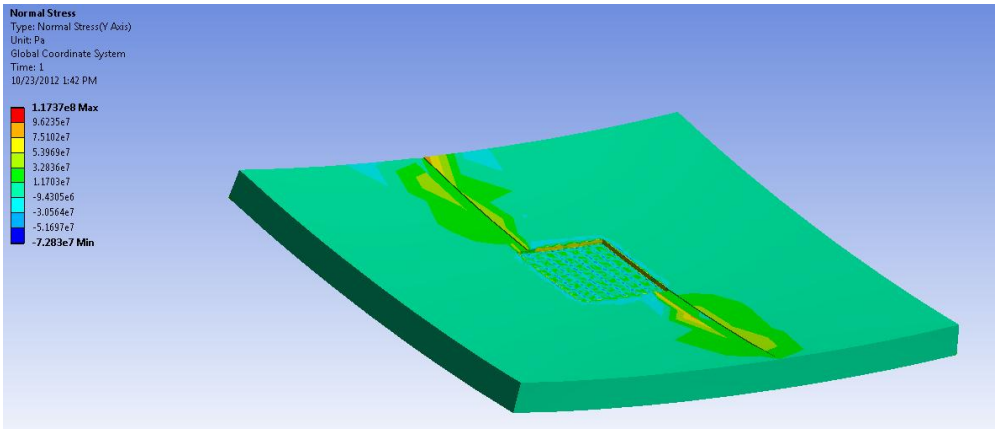


Figure 6.32 Normal stress profile in silicon die for conventional chip package with TFTEC embedded in silicon die and operated at current of 5Amp (Case-III)

6.5 Conclusion and Future Work

6.5.1 Conclusion

In this case study, the thermal and structural analysis was done for hot-spot cooling in flip chip using embedded TFTEC. It was observed from the numerical results that when TFTEC was embedded in IHS and silicon die and operated at the current of 5Amp, maximum junction temperature of the hot spot was reduced by around 14^{o}C and 16^{o}C respectively compared to the conventional chip package without TFTEC embedded in it . But the overall temperature of the chip package was found to be very high for chip package with TFTEC embedded in silicon die as heat from hot side of TFTEC was not dissipated properly due to low thermal conductivity of TIM material. Maximum shear stress in solder balls and copper pads was found to be almost same for all three cases. But normal stress in the die was found to be very high when TFTEC was embedded in the silicon die, compared to the normal stress in the die when TFTEC was embedded in IHS and conventional chip package without embedded TFTEC.

6.5.2 Future Work

Future work can be thermal and power cycling to study the reliability of the chip package with TFTEC embedded in IHS. Even the designed can be optimized for hot spot cooling by using vapor chamber at hot side of TFTEC to remove the heat form hot side of TFTEC more effectively. Even cooling performance for different thermoelectric leg height can be studied.

REFERENCES

[1] WEPOBEDIA (online), http://www.webopedia.com/TERM/M/Moores_Law.html.

[2] ITRS. The International Technology Roadmap for Semiconductors. [Online] 2005. http://www.ITRSnemi.org.

[3] Bao Yang, Peng Wang, Avram Bar-Cohen, “Thermoelectric Mini-Contact Cooler For Hot-Spot Removal In High Power Devices”, Electronic Components and Technology Conference, IEEE, pp. 997-1002, 2006

[4] Peng Wang, Avram Bar-Cohen, “On-chip hot spot cooling using silicon thermoelectric microcoolers”, American Institute of Physics, J. Appl. Phys. 102, 034503 (2007); doi: 10.1063/1.2761839

[5] iNEMI, Electronics Manufacturing Initiative Technology Roadmap, 2006, http://www.nemi.org.

[6] Cooling a microprocessor chip. Mahajan, R., Chiu, C., and Chrysler, G. 8, s.l.: IEEE, Vol. 94, pp. 1476-1486.

[7] R. Mahajan, “Thermal management of CPUs: A perspective on trends, needs and opportunities,” Oct. 2002. Keynote presentation at the 8th Int’l Workshop on thermal Investigations of ICs and Systems.

[8] R. Viswanath, V. Wakharkar, A. Watwe, and V. Lebonheur, “Thermal Performance Challenges from Silicon to Systems,” Intel Technology Journal, Quarter 3, 2000.

[9] Horacio Cesar Nochetto, “Hotspot Remediation using Germanium Self Cooling Technology” , Master Thesis, Department of Mechanical Engineering, University of Maryland College Park, 2011

[10] Viatcheslav Litvinovitch, “Miniature Thermoelectric Coolers for On-Chip Hot Spots”, Master Thesis, Department of Mechanical Engineering, University of Maryland College Park, 2009

[11] TE Technology, Inc., http://www.tetech.com/FAQ-Technical-Information.html

[12] Vaidhei Bharat Patel, “Experimental/Computational Analysis of Active Cooling of Stacked Device Using Multidimensional Configured Thermoelectric Modules”, Master Thesis, Department of Mechanical and Aerospace Engineering, University of Texas at Arlington, Arlington, TX, USA, May 2012

[13] Edited by David M. More, “CRC Handbook of Thermoelectrics”, CRC Press, Inc.

[14] Dr. Seri Lee, Chief Technology Officer, Nextreme Thermal Solutions, “Thermoelectric Cooling and Power Generation”

[15] The Free Dictionary, http://encyclopedia2.thefreedictionary.com/Heat+Pipe

[16] THERMACORE: Thermal Management Solutions, http://www.thermacore.com/thermal-basics/heat-pipe-technology.aspx

[17] Heat Pipe Selection, http://www.enertron-inc.com/enertron-resources/PDF/How-to-select-a-heat-pipe.pdf

[18] Sri Jaimdram A/L Munusamy, “Heat Pipes in Electronic Packaging”, Master Thesis

[19] Electronics Cooling, “http://www.electronics-cooling.com/1996/09/heat-pipes-for-electronics-cooling-applications/”

[20] Shuttle Connecting Technologies, “http://www.shuttle.eu/_archive/older/en/ss40g_faq.htm”

[21] http://ws.ajou.ac.kr/~mems/mhp.htm

[22] Arys Chatterjee, Joel L. Plawsky, Peter C. Wayner Jr., “Disjoining pressure and capillarity in a constrained vapor bubble heat transfer system”, Advanced in Colloid and Interface Science 168 (2011) 40-49

[23] EE Times News and Analysis,” http://www.eetimes.com/electronics-news/4046037/Startup-throws-cold-water-on-hot-CPUs”

[24] Nextreme Thermal Solutions. Inc.

[25] EMPFASIS, “http://www.empf.org/empfasis/2007/Nov07/heat.html”

[26] Oregon State University, “http://web.engr.oregonstate.edu/~narayavi/jets.html”

[27] “http://www.xbitlabs.com/news/coolers/display/20061031075540.html”

[28] David S. Chau, Greg Chrysler, Sridhar Narasimhan, Deepak Ganapathy and Kelly Lofgren, “Feasibility Study of Using Solid State Refrigeration Technologies for Electronic Cooling”, IEEE, pp. 464-469, 2006

[29] Viatcheslav Litvinovitch, Peng Wangand Avram Bar-Cohen, “Superlattice μTEC Hot Spot Cooling”, IEEE, pp. 229-239, 2010

[30] Kong Hoon Lee and Ook Joong Kim, “Simulation of the Cooling System Using Thermoelectric Micro-Coolers for Hot Spot Mitigation”, 2007 International Conference of Thermoelectrics, IEEE, pp. 279-282, 2008

[31] G. Jeffrey Snyder, Marco Soto, Randy Alley, David Koester and Bob Conner, “Hot Spot Cooling using Embedded Thermoelectric Coolers “, 22nd IEEE SEMI-THERM Symposium, IEEE, 2006

[32] Shlomo Novotny, Hohn Dunn, Marlin Vogel, “Active Temperature Gradient Reducer”, United States Patent, Patent No. US 6,581,388 B2, Jun. 24 2003

[33] Electronics Cooling Methods in Industry, MPE 635: Electronics Cooling

[34] Dongmei Li, G.Q Zhang, Kailin Pan, Xiaosong Ma, Lei Liu1, Jinxue Cao, “Numerical Simulation on Heat Pipe for High Power LED Multi-Chip Module Packaging”, International Conference on Electronic Packaging Technology & High Density Packaging”, ICEPT-HDP, pp. 393-397, 2009

[35] Omer Emre Orhan, Ilker Tari, “Numerical Investigation on Cooling of Small Form Factor Computer Cases”, Engineering Applications of Computational fluid Mechanics Vol. 2 , No. 4, pp. 427-435, 2008

[36] Ron Zhang, Rajesh Katkar, Michael Huynh and Laura Mirkarimi, “Flip chip assembly process optimizations and material selections through validated simulations”, Invensas Corp

[37] Sheng-Liang Li, Chun-Kai Liu, Chung-Yen Hsu, Ming-Che Hsieh, Ming-Ji Dai and Sheng-Tsai Wu, “Thermo-mechanical Analysis of Thermoelectric Modules”, Electronics and Optoelectronics Research Laboratories, Industrial Technology Research Institute

[38] http://en.wikipedia.org/wiki/Ball_grid_array

[39] Jieyi Long, Seda Ogrenci Memik and Matthew Grayson, “Optimization of an On-Chip Active Cooling System Based on Thin-Film Thermoelectric Coolers”, EDAA, 2010

[40] Luciana W. da Silva, Massoud Kaviany, Andrew DeHennis, and Jeffrey S. Dyck, ” Micro Thermoelectric Cooler Fabrication: Growth and Characterization of Patterned Sb2Te3 and Bi2Te3 Films”

[41] L M Goncalves, J G Rocha, C Couto, P Alpuim, GaoMin, D M Rowe and J H Correia, “Fabrication of flexible thermoelectric microcoolers using planar thin-film technologies”, IOP Publishing, Journal of Micromechanics and Microengineering, pp. S169-S173, 2007

[42] Ihtesham Chowdhury, Ravi Prasher, Kelly Lofgreen, Gregory Chrysler, Sridhar Narasimhan, Ravi Mahajan, David Koester, Randall Alley and Rama Venkatasubramanian, “On-chip cooling by superlattice-based thin-film thermoelectrics”, NNANO, Nature Nanotechnology, Macmillan Publishers Limited, pp. 235-238, 2009

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