DESIGN AND PRINTED CIRCUIT BOARD LEVEL IMPLEMENTATION OF A NARROW BAND LC VCO

by

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ABSTRACT

DESIGN AND PRINTED CIRCUIT BOARD LEVEL

IMPLEMENTATION OF A NARROW

BAND LC VCO

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A Voltage Controlled Oscillator (VCO) using a 0.6 μm CMOS technology has been designed and fabricated. The design's tuning range is from 390 MHz to 410 MHz, with the center frequency being 400 MHz. The oscillator is powered by a 2.5 volt power supply. The controlling voltage varies from 0.87 to 1.6 volts. Simulation of the LC VCO was carried out in the Advanced Design System (ADS) program. For the printed circuit board level implementation, the layout was first performed using the ADS program, and then its image was transferred on to a printed circuit board. The device footprints were incorporated in the circuit board layout. The dimension of the copper board was 1.5 x 0.6 inches. The frequency of oscillations on the printed circuit board was found to be 381.14 MHz while the simulations in ADS, showed a frequency of 391 MHz, which represents a deviation of 2.55 %. By changing the capacitor of the tank circuit on the board, the frequency of oscillation varies from 300.47 MHz to 464.8 MHz as seen on the spectrum analyzer. The oscillator output current was 5 mA and its output power was 7 mW.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Oscillators are an integral part of many electronic systems. Their applications range from clock generation in microprocessors to carrier synthesis in cellular telephone. Most applications require that oscillators be tunable, that is, their output frequency be a function of voltage, which is a control input to the oscillator [1]. These oscillators are called Voltage Controlled Oscillators (VCO).

Voltage controlled oscillators are used in Phase Locked Loops (PLL) which in turn is used to synchronize carrier recovery in communication systems [1]. Many of the past works have shown LC oscillators being tunable with a limited tuning range with the frequency versus voltage curve being close to linear [2]. Most recently, a VCO which adopts a series/parallel reconfigurable structure of inductor arrays has been designed in order to obtain the required tuning range [3]. This thesis work makes use of MOSFET varactors as capacitors in order to make the frequency tunable and get a linear curve of frequency versus voltage. Also the usage of multiple inductors has been avoided in order to obtain a smaller layout area on the board for the desired oscillation frequency.

An LC VCO with a tuning range from 390 MHz to 410 MHz, centered at 400 MHz has been designed. The simulations are carried out using ADS from Agilent. In order to change the frequency of oscillation, a varactor diode is used whose capacitance varies inversely with the potential difference across it. The 0.6 μm model files from Metal Oxide Semiconductor Implementation System (MOSIS) are used for simulation.

Most of the work done previously indicate the use of Integrated circuits to manufacture VCOs which incur higher cost and slower turn-around-time. Recent work has shown the use of

a differential Colpitts oscillator which has a problem of start-up during oscillations [5]. The limitation of using a differential oscillator is the larger layout area. This work shows the use of a single-ended Colpitts LC VCO that can be implemented on a printed circuit board (PCB) using discrete transistors, capacitors and inductors but with easy start-up and high linearity. The advantages of this kind of VCO are that it is simple to manufacture within a reasonable time frame.

PCB level implementation involves the careful routing of the width and length of the interconnects so as to mitigate parasitic resistances, capacitances and inductances which would otherwise affect the frequency of oscillation. The guidelines are obtained from the application note from Semtech for a 2-layer board design [4]. A program called Advanced Design System (ADS) from Agilent is used to simulate the oscillator circuit, produce a board layout, and finally a gerber file for board fabrication. The frequency of oscillation on the PCB was 381.14 MHz and the power consumption was about 7 mW. Attributes that account for the frequency shift include RC parasitic elements, board layout and non-ideal discrete transistors, capacitors and inductors [6]. This kind of an oscillator is used in applications such as ASK transmitters, time interleaved sigma-delta modulators and PLLs to filter clock jitter in source-synchronous serial link applications [7] [8] [9].

1.2 Thesis outline

Chapter 2 gives an overview of MOSFET devices. The characteristics and advantages of MOSFETs over bipolar transistors have been discussed. Chapter 3 provides an outline on voltage controlled oscillators where the single ended and differential LC oscillators are described. Chapter 4 focuses on the design part of the LC VCO for the required oscillation frequency and the board level implementation of the same. The simulation results of the design are also provided. This is concluded by Chapter 5 which gives the results and conclusions

obtained using the proposed method of implementation. Future possible improvements on this design are also conveyed.

CHAPTER 2

OVERVIEW OF MOSFETs

2.1 MOSFET Devices

MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) are widely used in the area of digital integrated circuit designs because they allow high density, they have a relatively simple manufacturing process, and they dissipate low power. Bipolar devices are preferred in stand-alone analog integrated circuits due to their higher transconductance and high current driving capability. To reduce system cost and increase portability, increased levels of integration and reduced power levels are required. This compels the associated analog circuits to use MOS-compatible technologies. This is achieved by using a process technology called BiCMOS which provides the usage of both bipolar and MOS transistors, allowing greater design flexibility [10].

2.1.1 The CMOS technology

The symbols used here for NMOS and PMOS devices are shown in Figure 2.1.

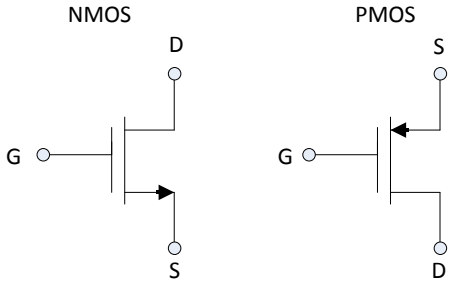


Fig 2.1: MOS Symbol

The G, D and S symbols represent Gate, Drain and Source, respectively. The arrow indicates the direction of current flow. In a NMOS transistor, current flows from drain to source while in a

PMOS transistor, it flows from source to drain. A perspective view of the physical structure of a NMOS enhancement type transistor is shown in figure 2.2 [11].

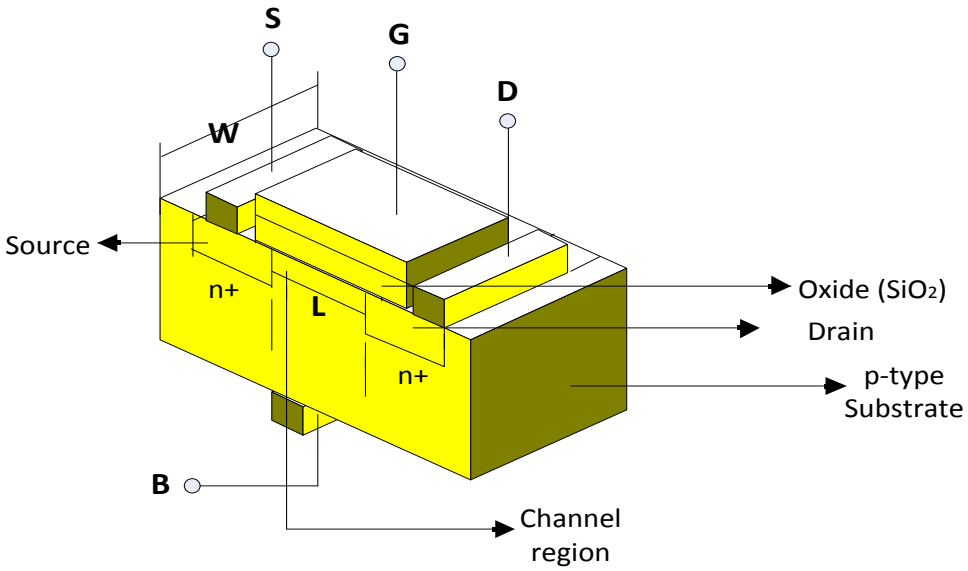


Fig 2.2: Physical structure of the enhancement-type NMOS transistor

The CMOS structure is manufactured on a single p-type substrate. Two heavily doped n-type regions, indicated in figure 2.2 as source and drain regions, are created in the substrate. A thin layer of silicon dioxide (SiO_2) is grown on the surface of the substrate, covering the source and drain regions. It acts as an electrical insulator. Metal is deposited on top of the oxide layer to form the gate electrode. A voltage applied to the gate controls the flow between source and drain in the channel region, which is characterized by its length (L) and width (W) [11].

In CMOS technologies, both NMOS and PMOS transistors are manufactured on the same wafer. While the NMOS transistor is implemented directly in the p-type substrate, the PMOS transistor is fabricated in a specially created n-region, known as an n-well. The two devices are isolated from each other by a thin region of oxide that functions as an insulator. Figure 2.3 shows a cross-section of a CMOS integrated circuit.

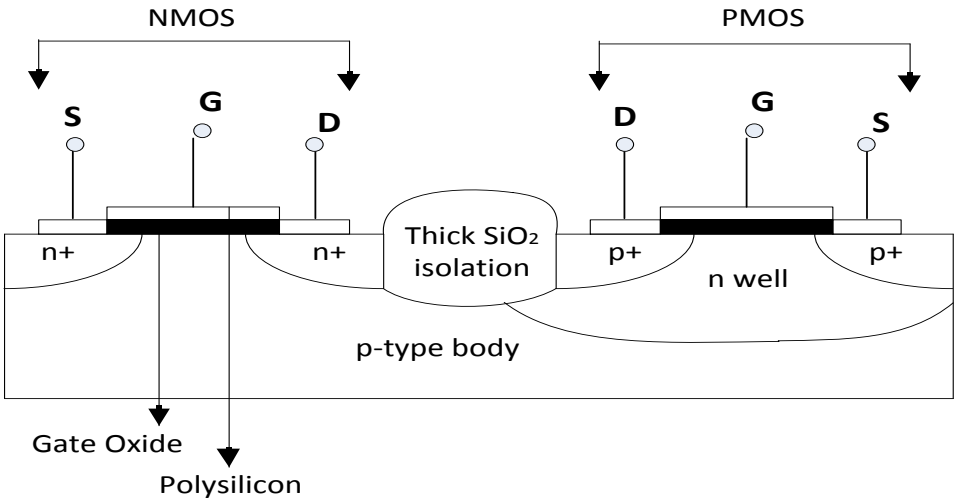


Fig 2.3: Cross-section of a CMOS integrated circuit

2.1.2 Derivation of I-V Characteristics

The value of the gate-source voltage at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel from source to drain is called the threshold voltage –V_{th}. When the gate-source voltage (V_{GS}) is less than that of the threshold voltage (V_{th}), the MOSFET operates in the cut-off region. The drain current (I_D) in this region is almost zero.

When V_{GS} is above V_{th} and when a drain-source voltage (V_{DS}) of small magnitude is applied, a drain current I_D starts flowing through the induced n-channel. Thus, when,$V_{DS} < V_{GS} - V_{th}$ the transistor operates in the triode region and the value of drain current (I_D) is given by [1]:

$$I_D = \mu_n \mathrm{C_{ox}} \frac{W}{L}\left[(V_{GS} - V_{th})^2 - \frac{1}{2}V_{DS}^2\right] \quad (2.1)$$

When V_{GS} is above V_{th} and when a drain-source voltage (V_{DS}) greater than the overdrive voltage ($V_{GS} - V_{th}$) is applied, the transistor operates in the saturation region. In the saturation region of operation, the drain current is almost constant. The drain current is given by [1]:

$$I_D = \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \quad (2.2)$$

Thus, equation (2.2) occurs when the condition $V_{DS} \geq V_{GS} - V_{th}$ is satisfied. Since the drain current remains almost constant, the transistor can be used as a current source which supplies constant current [1].

Figure 2.4 shows the operation of an n-channel MOSFET with positive V_{GS} and V_{DS}. Figure 2.5 shows the I_D-V_{DS} characteristics of a MOSFET device [10].

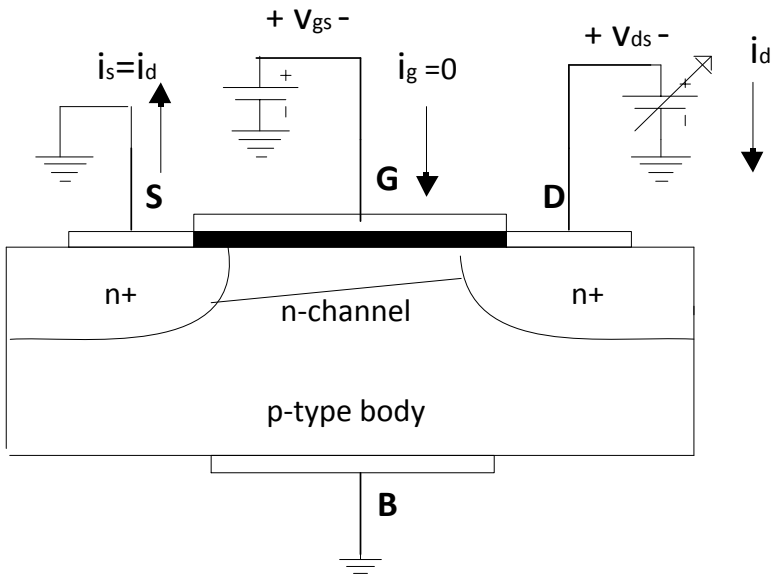


Fig 2.4: Operation of a NMOS transistor as V_{DS} is increased

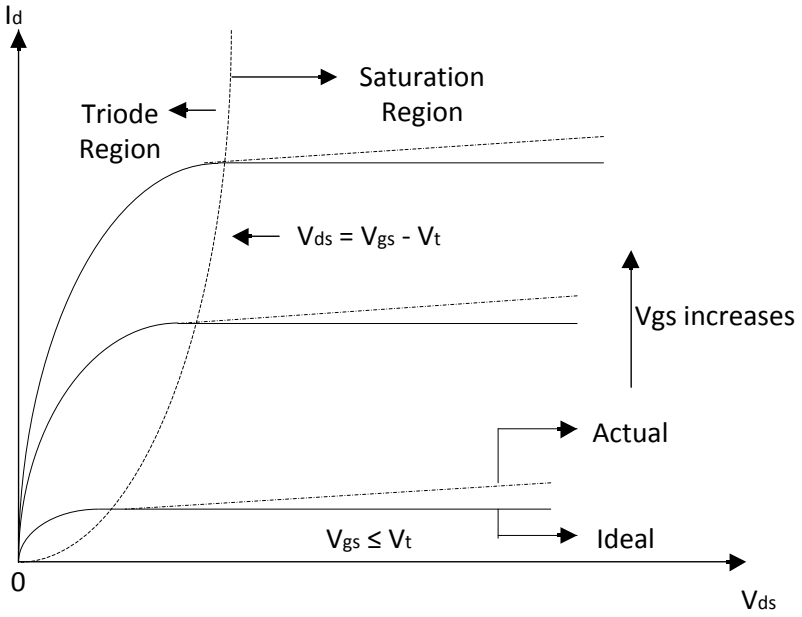


Fig 2.5: The I_D – V_{DS} characteristics of a MOSFET device

2.1.3 The MOS small signal model

Small-signal models are used to simplify the calculation of current gain and terminal impedances. The complete small signal model of a MOSFET is shown in figure 2.6.

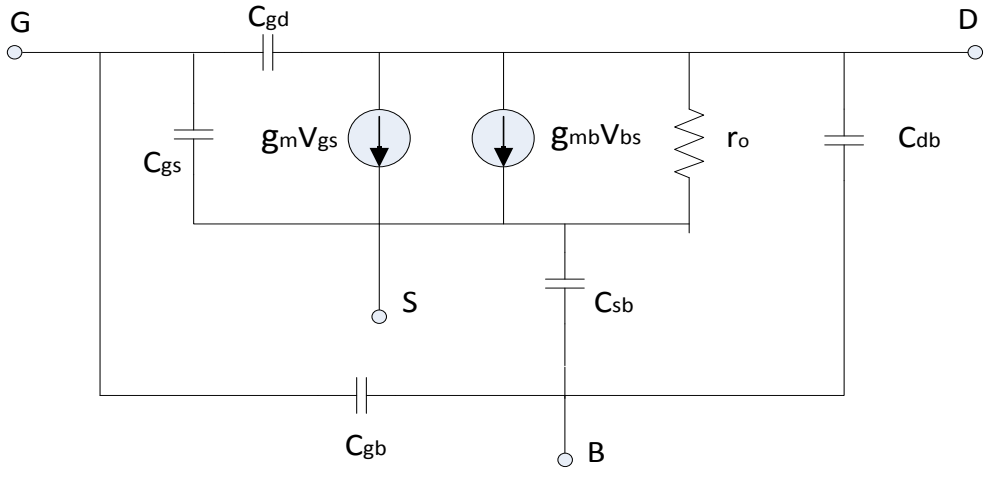


Fig 2.6: Small-signal MOS transistor equivalent circuit

The transconductance of a MOSFET is the ratio of change in its drain current to the change in gate-source voltage, keeping the drain source voltage constant. It is denoted by g_m and is given by [10]:

$$g_m = \frac{\partial \mathrm{I_D}}{\partial V_{GS}} \tag{2.3}$$

The intrinsic gate-source and gate-drain capacitances in the triode region of operation are given by [10]:

$$C_{GS} = C_{GD} = \frac{C_{OX} WL}{2} \tag{2.4}$$

where, C_{OX} is the oxide capacitance per unit area from gate to channel. In the saturation region of operation gate-source capacitance is given by [10]:

$$C_{GS} = \frac{2}{3} WLC_{OX} \tag{2.5}$$

Also, the gate-drain capacitance is assumed to be zero. The gate of a MOS transistor is insulated from the channel by the SiO_2 dielectric. As a result, the low-frequency gate current is essentially zero and the input resistance is infinite. The output resistance (r_o) is given by:

$$\frac{\Delta V_{DS}}{\Delta I_D} = r_O = \frac{1}{\lambda I_D} \tag{2.6}$$

where,λ is the channel length modulation parameter.

CHAPTER 3

VOLTAGE CONTROLLED OSCILLATOR

3.1 Overview of VCO

A voltage controlled oscillator (VCO) is an electronic oscillator whose frequency is designed to be controlled by varying a DC voltage input [14]. While current controlled oscillators are also feasible, they are not widely used in RF systems because of difficulties in varying the inductance value of high-Q inductors by means of a current [12]. An ideal VCO is a circuit that generates a periodic output whose frequency is a linear function of a control voltage (V_{cnt}), given by [1].

$$\omega_{out} = \omega_0 + V_{cnt}K_{VCO} \tag{3.1}$$

where, ω_0 is the free-running frequency, K_{VCO} is the gain of the VCO (specified in rad/s/V) [12]. The achievable range ($\omega_2 - \omega_1$) is called the tuning range of the VCO.

Figure 3.1 shows the basic mathematical model of the VCO and its voltage and frequency tuning characteristics [1].

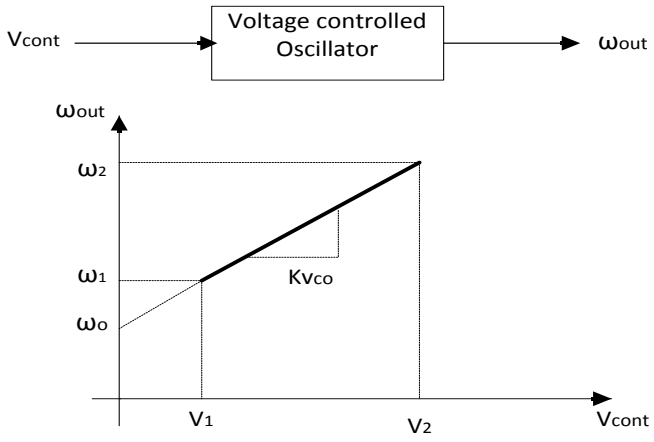


Fig 3.1: Definition of a VCO and its tuning characteristics

3.1.1 Performance parameters of VCOs

a) Center Frequency: The center frequency is determined by the environment in which the VCO is used.

b) Tuning range: The required tuning range is dictated by two parameters: the variation of the center frequency with fabrication process and temperature, and the frequency range necessary for the application. An important design consideration of VCOs is the variation of the output phase and frequency due to the noise present on the control line. The noise in the output frequency is proportional to the VCO gain, where gain is the ratio of output frequency in radians to the input control voltage in volts. Thus to reduce the effect of noise in the control voltage, the VCO gain must be reduced. This is in direct conflict with a wide required tuning range. The gain for a VCO is defined as [1].

$$K_{VCO} = \frac{\Delta\omega_{out}}{\Delta V_{cont}} \geq \frac{\omega_2 - \omega_1}{\mathrm{V}_2 - \mathrm{V}_1} \tag{3.2}$$

c) Linearity: The tuning characteristic of a VCO exhibits non-linearity which means that gain (K_{VCO}) is not constant for the entire tuning range. When VCOs are used in phase-locked loops, their settling behavior degrades due to such non-linearity [1].

In practice, oscillators typically exhibit a high gain region in the middle of the tuning range and low gain at the two extremes as shown in figure. 3.2. The ω_{out} is the output angular frequency in radians and V_{cont} is the control voltage in volt.

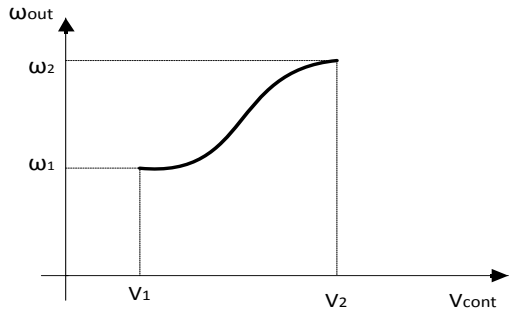


Fig 3.2: Nonlinear characteristics of VCO

d) Phase noise: Phase noise degrades the performance of communication and radar systems. In microwave fixed frequency oscillators, high-Q resonators are employed in order to achieve low phase noise. These high-Q resonators are typically high-permittivity dielectric resonators [13]. Phase noise or timing jitter in oscillators is of major concern in wireless and optical communications. It is a major contributor to the bit-error rate of communication systems, and creating synchronization problems in other clocked and sampled-data systems.

A perfect oscillator would oscillate at a single frequency, but due to the inherent device non-linearity, harmonics are caused. The presence of harmonics results in undesired power levels at the harmonics. This effect is the major contributor to some unwanted phenomena such as inter-channel interference, leading to increased bit-error rates in RF communication systems.

Another manifestation of the same phenomenon is jitter. It is important in clocked and sampled-data systems. Jitter is uncertainty in switching instants caused by noise leads to synchronization problems. Characterizing how noise affects oscillators is therefore crucial for practical applications [18].

3.1.2 Applications of VCO

3.1.2.1 Phase-locked loop

One of the major applications of a VCO is in phase-locked loops (PLL). A phase-locked loop is a feedback system that operates on the excess phase of nominally periodic signals. A simple PLL consists of a phase detector (PD), a low-pass filter (LPF) and a VCO. Figure 3.3 shows a simple PLL.

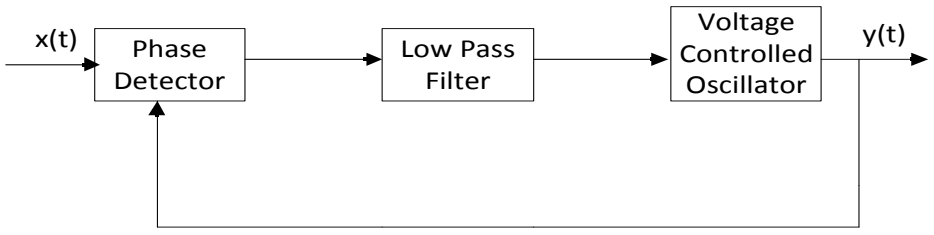


Fig 3.3: A simple PLL comprising of a VCO

The phase detector serves as an “error amplifier” in the feedback loop, thereby measuring the phase difference,$\Delta\varphi$, between the input signal and output signal, $x(t)$ and $y(t)$, respectively. The loop is considered locked if $\Delta\varphi$ is constant with time, a result of which is that the input and the output frequencies are equal. In the locked condition, all the signals in the loop have reached a steady state. The PLL operates as follows - the phase detector produces an output whose dc (direct current) value is proportional to $\Delta\varphi$. The low-pass filter suppresses high frequency components in the phase detector output, allowing the dc value to control the VCO frequency with a phase difference equal to $\Delta\varphi$. Thus, the LPF generates the proper control voltage to the VCO [12].

3.1.2.2 Frequency Multiplication

Frequency synthesizers are used in synthesizing a desired frequency by modifying a PLL. This PLL is modeled such that the output frequency is a multiple of the input frequency by a factor M. The frequency multiplication circuit is shown in figure 3.4. It makes use of a $\div M$ circuit which divides the incoming frequency by a factor of M. Optionally, a charge pump/ low pass filter (CP/LPF) block can be used in order to generate a frequency signal to the VCO. Thus, if the output frequency of a PLL is divided by M and applied to the phase-frequency detector, then the output frequency is given by $f_{out} = M\, f_{in}$. The $\div M$ circuit is realized as a counter that produces the output pulse for every M input pulses. The concept of frequency multiplication is used to design frequency synthesizers which produce variable frequencies [1].

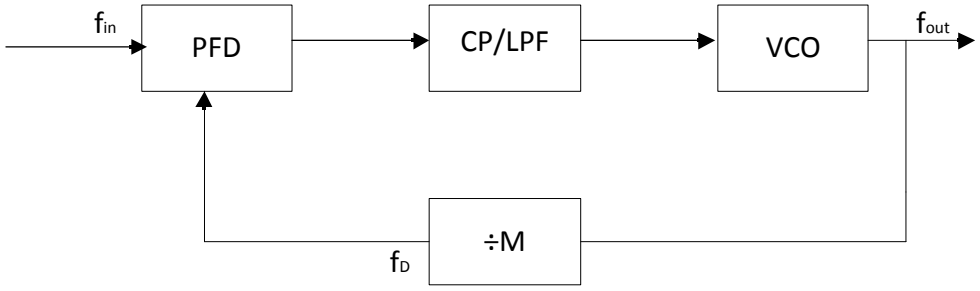


Fig 3.4: Frequency Multiplication

VCOs are used as clock generators, which provide a timing signal to synchronize operations in a digital circuit. Voltage-controlled crystal oscillators are used in many areas such as digital television, modems, transmitters and computers. VCOs find applications even in electronic jamming equipment, function generators and in the production of electronic music, to generate variable tones [20].

3.2 Types of CMOS Oscillators

A simple oscillator produces a periodic output at a fixed frequency. Consider a unity-gain negative feedback circuit as shown in figure 3.5 [1].

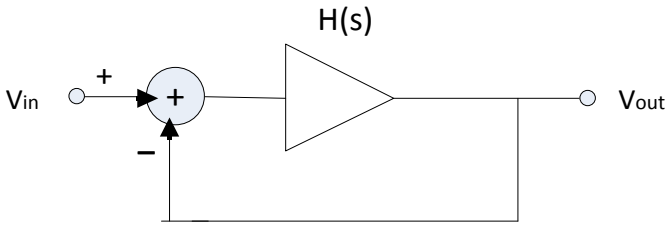


Fig 3.5: Unity-gain feedback system

The transfer function is given by [1]:

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1 + H(s)} \tag{3.3}$$

Here, the complex frequency (s) is given by $s = j\omega$. In equation (3.3), if $H(s) = -1$, the closed loop gain approaches infinity at the free-running frequency ω_0. Under this condition, the circuit amplifies its own noise components at ω_0 indefinitely.

Oscillation occurs in a negative feedback circuit that has a loop gain that satisfies two conditions [1]:

a) $|H(j\omega_0)| \geq 1$

b) $\angle H(j\omega_0) = 180°$

These conditions are called the Barkhausen's criteria and are necessary for the circuit to oscillate. Considering the above criteria, there are two types of CMOS oscillators that are implemented in today's technology, namely, ring oscillators and LC oscillators.

3.2.1 Ring Oscillators

A ring oscillator consists of a number of gain stages in a loop. A three stage ring oscillator is shown in figure 3.6.

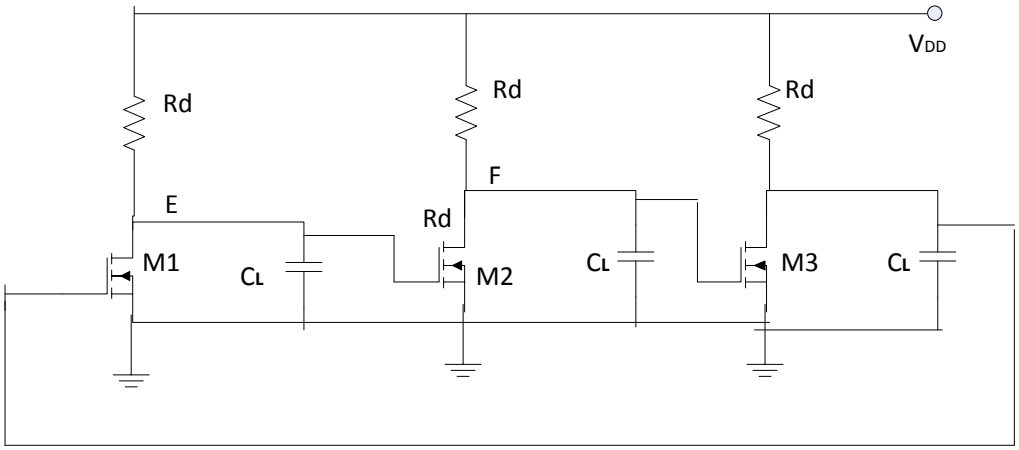


Fig 3.6: Three-stage ring oscillator

The loop gain of each stage is given by: $-A_0/(1+\frac{s}{\omega_{3dB}})$. Since there are three stages, the total gain of the loop is given by [1]:

$$H(s) = -\frac{{A_0}^3}{(1+\frac{s}{\omega_{3dB}})^3} \tag{3.4}$$

The circuit oscillates only if the frequency-dependent phase shift equals $180°$, that is, if each stage produces a phase shift of $60°$. The frequency at which this occurs is given by [1]:

$$\tan^{-1}\frac{\omega_{osc}}{\omega_{3dB}} = 60° \tag{3.5}$$

From equation (3.5), the oscillation frequency is obtained as $\omega_{osc} = \sqrt{3}\omega_{3dB}$.The minimum voltage gain per stage must be such that the magnitude of the loop gain at ω_{osc} is equal to one [1].

$$\frac{{A_0}^3}{\left[\sqrt{1+\left(\frac{\omega_{osc}}{\omega_{3dB}}\right)^2}\right]^3} = 1 \tag{3.6}$$

From equations (3.5) and (3.6), the voltage gain is found to be two $(A_0 = 2)$.

In summary, a three-stage ring oscillator oscillates if it has a low-frequency gain of two per stage and it oscillates at a frequency of $\sqrt{3}\omega_0$, where, ω_{3dB} is the 3-dB bandwidth of each stage. The frequency of oscillations for an *N*-stage ring oscillator is given by [1]:

$$f_{osc} = \frac{1}{2NT_D} \tag{3.7}$$

where, N is the number of amplifier stages and T_D is the delay of each stage.

A three-stage ring oscillator using CMOS inverters is shown in figure 3.7.

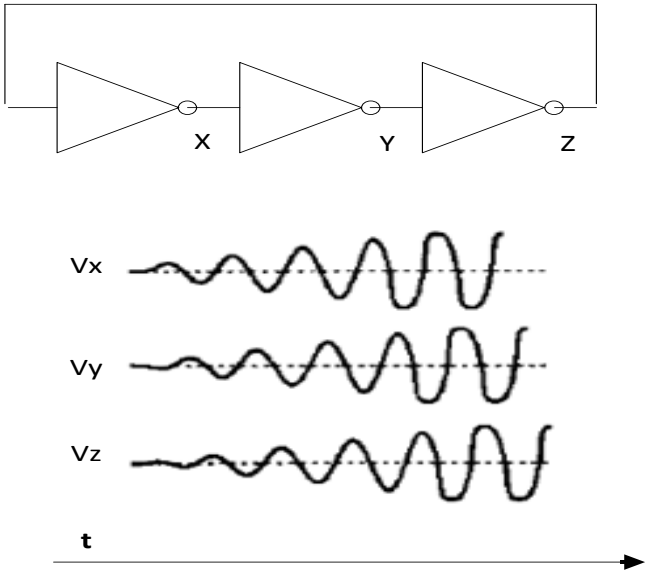


Fig 3.7: Ring oscillator using CMOS inverters

Ring oscillators having more than three stages are also feasible, provided the total number of inversions in the loop is odd, so that a positive feedback is realized. This ensures the circuit does not latch-up. On the other hand, the differential implementation can use an even number of stages by simply configuring one stage such that it does not invert [1]. Figure 3.8 shows the single-ended and differential ring oscillators implementation.

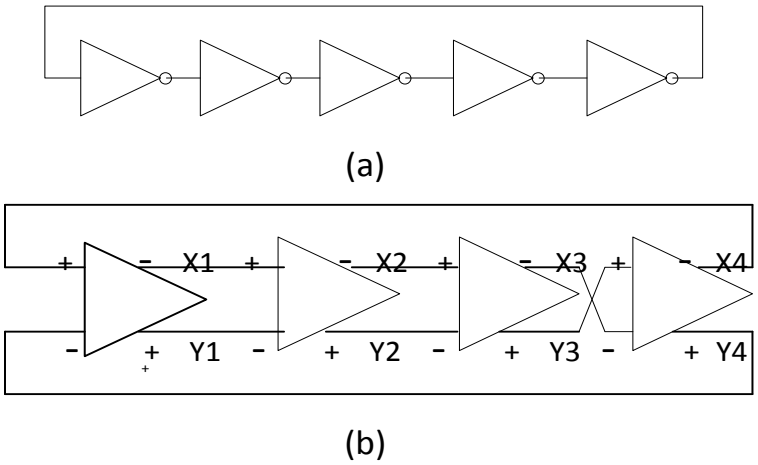


Fig 3.8: (a) Five-stage single-ended ring oscillator (b) Four-stage differential ring oscillator

3.2.2 LC Oscillators

An inductor, L_1, placed in parallel with a capacitor, C_1, resonates at a resonance frequency given by [1]:

$$\omega_{res} = \frac{1}{\sqrt{L_1 C_1}} \tag{3.8}$$

At this frequency the impedances of the inductor ($jL_1\omega_{res}$), and the capacitor,$1/(j\omega_{res}C_1)$, are equal and opposite, thereby yielding an infinite impedance. In practice, the inductors and capacitors suffer from resistive losses, such as the series resistance of the metal wire used in the inductor.

Figure 3.9 shows an LC tank circuit with the resistive component. The quality factor, Q, of the inductor can be defined as $\omega C/G$. The equivalent impedance is given by [1]:

$$Z_{eq} = \frac{R_s + sL_1}{1 + L_1 C_1 s^2 + sR_s C_1} \tag{3.9}$$

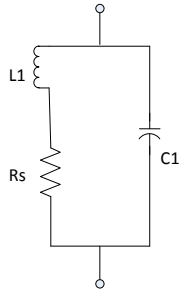


Fig 3.9: Resistive LC Tank

The magnitude of the impedance is given by:

$$\left|Z_{eq}(s=j\omega)\right|^2 = \frac{{R_s}^2 + \omega^2 {L_1}^2}{(1 - L_1 C_1 \omega^2) + \omega^2 {R_s}^2 {C_1}^2} \tag{3.10}$$

From the above equation, it can be seen that the impedance does not go to infinity at any $s = j\omega$. Thus, the circuit has a finite Q. The magnitude of Z_{eq} reaches a peak in the vicinity of $\omega = \frac{1}{\sqrt{L_1 C_1}}$, but the actual resonance frequency has some dependency on R_s.

3.2.2.1 Negative resistance Oscillators

Figure 3.10 shows a simple LC tank circuit stimulated by a current impulse. The tank responds with a decaying oscillatory behavior because, in every cycle, some of the energy that oscillates between the capacitor and inductor is lost in the form of heat in the resistor. If a resistor of value $-R_P$ is placed in parallel with R_P, then the equivalent resistance is infinity, since $(-R_P) \parallel R_P = \infty$. With this condition, the tank oscillates indefinitely [1].

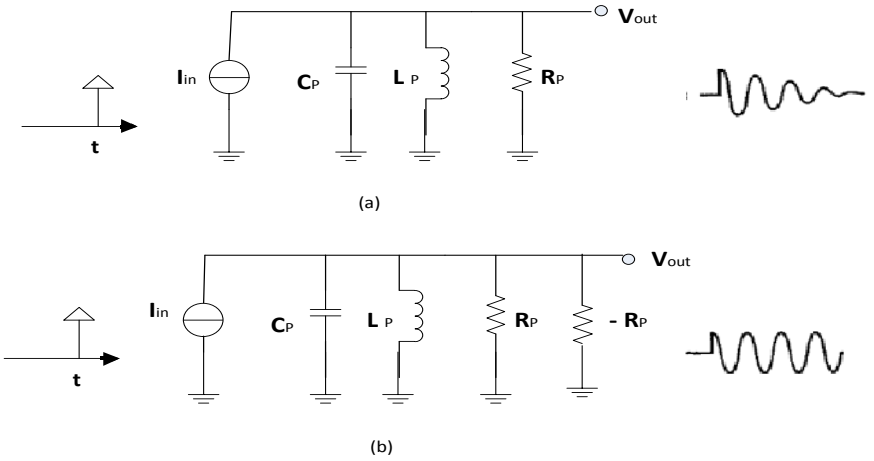


Fig 3.10: LC tank showing (a) decaying impulse response (b) addition of negative resistance to cancel loss in R_P

This implies if a one-port circuit exhibiting negative resistance is placed in parallel with a tank, they oscillate. Figure 3.11 shows the use of an active circuit to provide negative resistance [1].

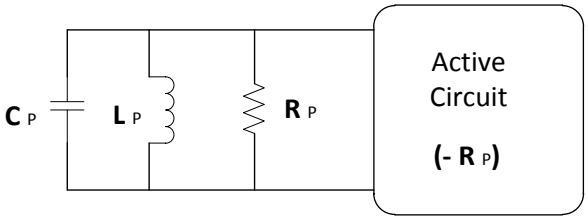


Fig 3.11: Use of an active circuit to provide negative resistance

A circuit can provide negative resistance, if the loop gain is sufficiently negative, that is, if the feedback is sufficiently positive. As an example, a positive feedback is applied around a source follower. The follower introduces no signal inversion and neither does the feedback network. The feedback is implemented using a cascade of a source follower (M_1) and a source degenerate transistor (M_2) as shown in Figure 3.12. The current source I_b provides the bias current for M_2 [1].

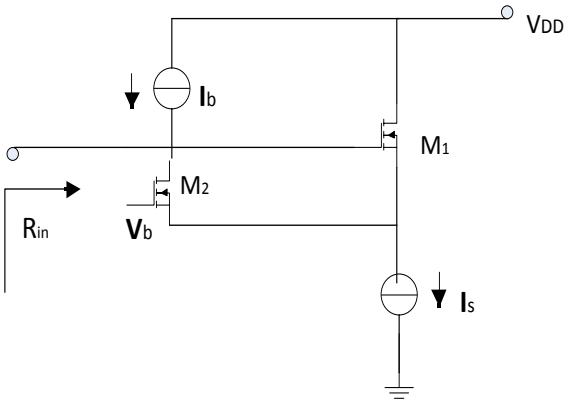


Fig 3.12: Source follower with positive feedback to create negative input impedance

The equivalent circuit of figure 3.12 is shown in figure 3.13.

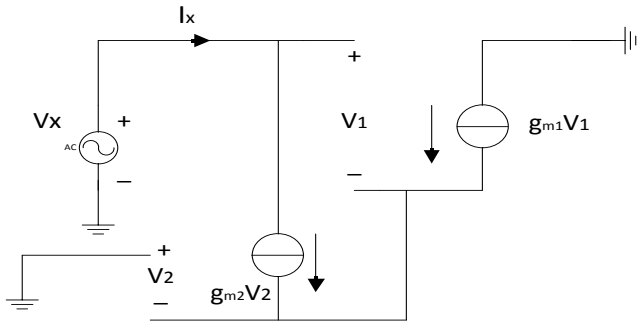


Fig 3.13: Equivalent circuit of the negative resistance amplifier

From figure 3.13, the current I_X is given by [1]:

$$I_X = g_{m2}V_2 = -g_{m1}V_1 \tag{3.11}$$

and

$$V_X = V_1 - V_2 = -\frac{I_X}{g_{m1}} - \frac{I_X}{g_{m2}} \tag{3.12}$$

Thus [1],

$$\frac{V_X}{I_X} = -\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right) \tag{3.13}$$

If $g_{m1} = g_{m2} = g_m$, then,

$$\frac{V_X}{I_X} = -\frac{2}{g_m} \tag{3.14}$$

Using this concept, an oscillator is constructed as shown in figure 3.14. Here, R_P denotes the equivalent parallel resistance of the tank [1]. In order to attain sustained oscillations, the parallel resistance of the active circuit has to be greater than the negative resistance of the active circuit $\left(\frac{1}{g_m}\right)$.

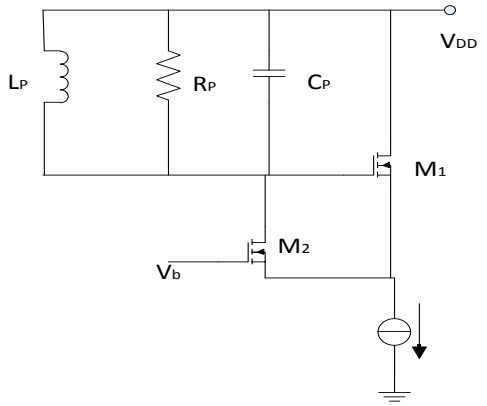


Fig 3.14: Oscillator using negative input resistance of a source follower with positive feedback

If the small signal resistance presented by M_1 and M_2 to the tank is less negative than $-R_P$, then the circuit experiences large voltage swings such that each transistor is nearly off for part of the period, thereby giving an average resistance of $-R_P$ [1]. The circuit in figure 3.14 can be redrawn as shown in figure 3.15.

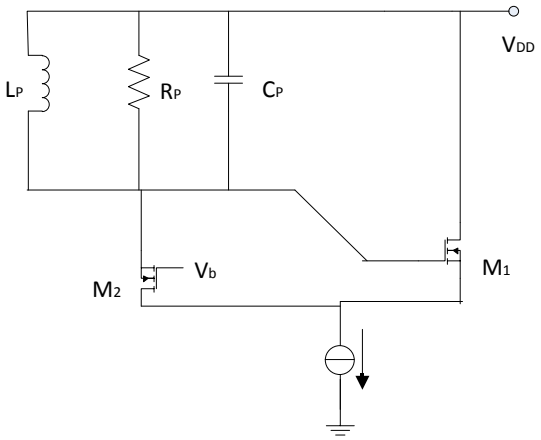


Fig 3.15: Redrawing of the topology shown in figure 3.14

Figure 3.16 shows the differential topology. If the drain current of M_1flows through the tank circuit and the drain voltage of $M_1$is applied to the gate of M_2, it gives a differential version of the single-ended circuit of figure 3.15..

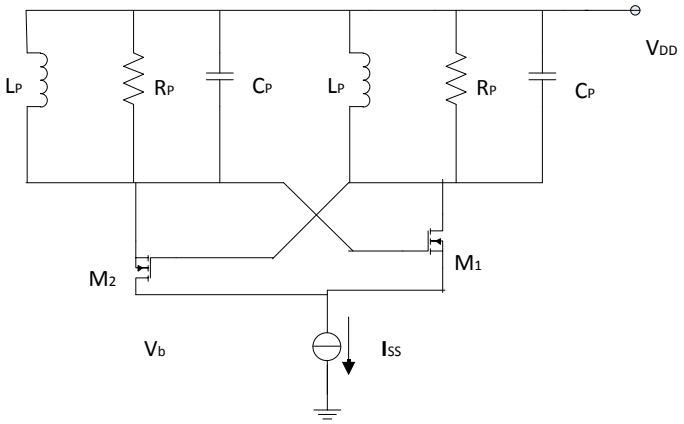


Fig 3.16: Differential LC oscillator topology

A cross-coupled pair is obtained by ignoring the bias paths and merging the two tank circuits into one. Figure 3.17 shows that the cross-coupled pair must provide a negative resistance of $-R_P$ between the nodes X and Y to enable oscillation. This negative resistance is equal to $-\frac{2}{g_m}$, giving, $R_P \geq \frac{1}{g_m}$.

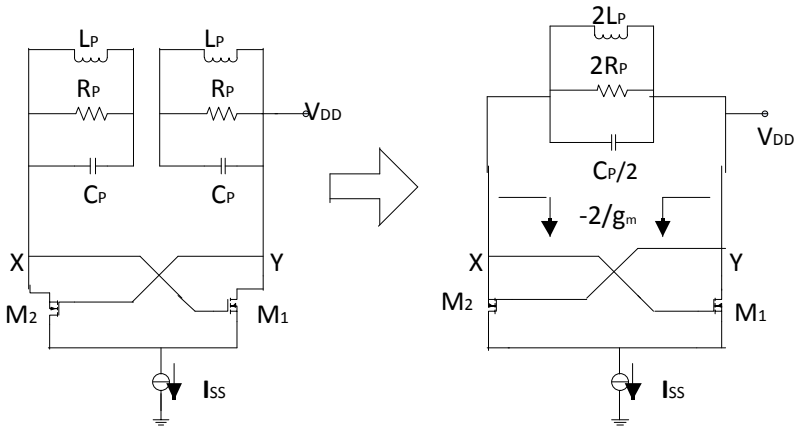


Fig 3.17: Negative-Gm oscillator

The circuit can be viewed as either a feedback system or a negative resistance in parallel with a lossy tank. This topology is called a negative-Gm oscillator [1].

3.2.2.2 Tuning in LC VCO

The oscillation frequency of LC topologies is given by [1]:

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}} \tag{3.15}$$

Equation (3.15) suggests that only the inductor and the capacitor values can be varied to tune the frequency while other parameters such as the MOSFET transconductance and the bias currents affect the oscillation frequency negligibly [1].

Since it is difficult to vary the value of monolithic inductors, the capacitor in the tank circuit is changed in order to tune the oscillator. Capacitors whose value can change with a change in voltage are called varactors. A reverse biased p-n junction can serve as a varactor. The voltage dependence on the capacitance is given by [1]:

$$C_{var} = \frac{C_o}{\left(1 + \frac{V_R}{\varphi_B}\right)^m} \tag{3.16}$$

where C_o is the zero-bias value, $V_R$is the reverse-bias voltage, φ_B is the built-in potential of the junction, and *m* is a value typically between 0.3 and 0.4.

In order to make the oscillator tunable, the varactor diodes are added to the cross-coupled LC oscillator, as shown in figure 3.18.

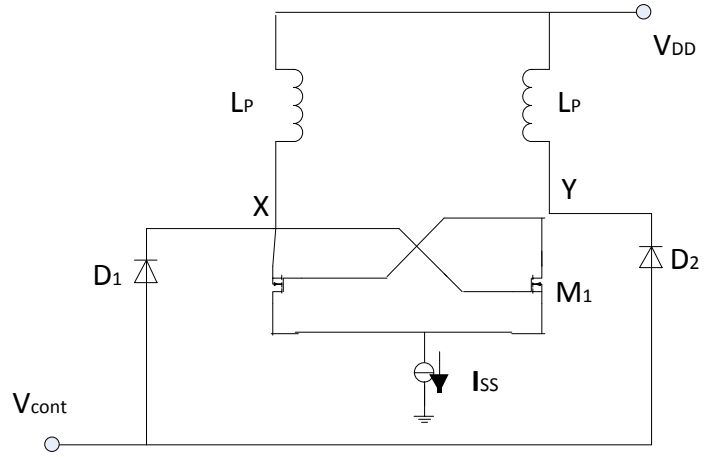


Fig 3.18: LC oscillator using varactor diodes

To avoid forward-biasing D_1 and D_2, significantly, V_{cont} must not exceed V_X or V_Y by a few hundred millivolts. For example, if the peak amplitude at each node is *A*, then V_{cont} must satisfy $0 < V_{cont} < V_{DD} - A + 300mV$ [1]. Here it is assumed that a forward bias of $300\,mV$ creates negligible current. The circuit suffers from the trade-off between the output swing and the tuning range. This affect is predominant in most LC oscillators.

Since the swings at X and Y are typically large, the capacitances of D_1 and D_2varies with time. Nonetheless, the average value of capacitance is still a function of V_{cont}which provides the tuning range [1]. The design of a 400 MHz LC VCO is based on the above concept.

CHAPTER 4

DESIGN SUMMARY AND RESULTS

This chapter describes two VCO designs: the first design includes the LC tank circuit differential oscillator and the second design involves the Colpitt's oscillator. The LC voltage controlled oscillator is simulated in ADS at the desired frequency of 400 MHz. The varactor diode is simulated using a FET varactor shorting its source and drain terminals. The variable capacitance is formed between the gate and source-drain combination. The tuning range is from 390 MHz to 410 MHz. The voltage supply used to power the VCO is 2.5 V.

In order to practically implement the VCO on a printed circuit board, the Orcad capture and layout program is used. The footprints are assigned to the various devices in the VCO. A netlist is created and a layout is prepared which conforms to the schematic. A two-layered board is prepared and the components are purchased from vendors. The components are then soldered onto the board and tested for the desired frequency range, voltage ranges, power levels and linearity.

4.1 LC VCO simulation in ADS

Using ADS, the transient output, the frequency spectrum and the phase noise are plotted. The performance of the oscillator is determined by the quality factor of the LC resonator. A spiral inductor is used in the resonator [21]. These inductors have low quality factors, of the order of 3 to 5, at 400 MHz. If a low phase noise design is required, the inductor should be installed off-chip.

4.1.1 LC Oscillator operation

Figure 4.1 shows the cross-coupled LC oscillator [15]. The LC tank circuit forms the drain load. Frequency dependent signals are then cross-coupled to the other devices' gate, which create a

negative impedance of value $-\frac{1}{g_m}$ at the drain terminal.

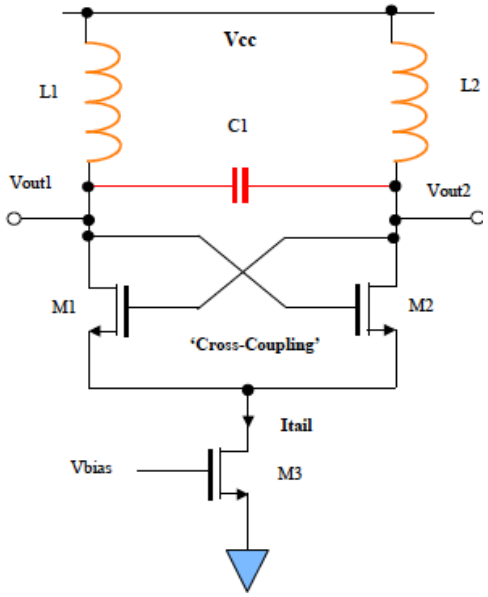


Fig 4.1: LC Tank circuit [15]

In that case, series resistance of the inductor is given by [15]:

$$R_s = \frac{2\pi f L}{Q_u} \tag{4.1}$$

For sustained oscillations to occur, the series resistance of the inductor should be less than the negative impedance at the drain terminals of the MOSFET. Thus [15],

$$\frac{1}{g_m} \geq \frac{2\pi f L}{Q_u} \tag{4.2}$$

where

$$g_m \cong \frac{2I_D}{V_{gs}-V_t} \tag{4.3}$$

Therefore,

$$\frac{V_{gs}-V_t}{2I_D} \geq \frac{2\pi f L}{Q} \tag{4.4}$$

or,

$$I_D = \frac{Q(V_{gs} - V_t)}{4\pi f L} \tag{4.5}$$

To ensure reliable start-up, LC oscillators are designed to have a startup safety factor of at least two [15],

$$\frac{2}{g_m} > R_P = \frac{2\pi f L}{Q_u} \tag{4.6}$$

4.1.2 Phase noise calculations

Ring oscillators are very small, but their high phase noise compared to LC-VCOs results in excessive timing jitter. LC-VCOs have superior phase noise, but their on-chip spiral inductors occupy a large area [16].

In order to calculate phase noise, Leeson's equation is used. Leeson's equation is given by [15],

$$L(f_m) = 10\, Log_{10}\left\{\frac{FkT}{2P_{avs}}\left[1 + \frac{f_c}{f_m} + \left(\frac{f_o}{2f_m Q_L}\right)^2\left(1 + \frac{f_c}{f_m}\right)\right]\right\} \tag{4.7}$$

Here, f_c denotes the corner frequency, f_m is the offset from the output frequency, Q_L is the loaded Q, f_0 is the output frequency.

The $\frac{FkT}{2P_{avs}}$ term represents the phase perturbation, $\frac{f_o}{2f_m Q_L}$ designates the resonator Q, while the $\left(1 + \frac{f_c}{f_m}\right)$ denotes the flicker effect.

The key parameter in determining the phase noise in oscillators is the loaded Q of the resonator. In CMOS oscillators the loaded Q of a spiral inductor is typically in the range of 3 to 5. If a tighter phase noise specification is required, then the inductor will be have to be off-chip.

The specifications for the LC VCO to be simulated are found in table 4.1:

Table 4.1 List of specifications desired by the LC VCO

Parameter	Specification	Unit
Center Frequency	400	MHz
Tuning Bandwidth	390-410	MHz
Phase Noise (10kHz offset)	>80	dBc/Hz
Supply voltage	2.5	V

In order to achieve the required phase noise performance, the minimum loaded Q is determined. The values of the circuit/resonator are fed into the ADS simulation tool as shown in figure 4.2. It shows a PhaseNoiseMod block. This block phase modulates one large signal frequency with noise to produce pure phase noise without amplitude noise. The PM_DemodTuned block is a tuned demodulator that selects the input harmonic closest to the specified F_{nom} frequency and generates a baseband output voltage synchronous to the instantaneous phase of the selected carrier frequency. For a center frequency of 400 MHz, the resultant Q was found to be 5. This value of Q is used further in the VCO design in order to find the resistance and inductance calculations of the circuit.

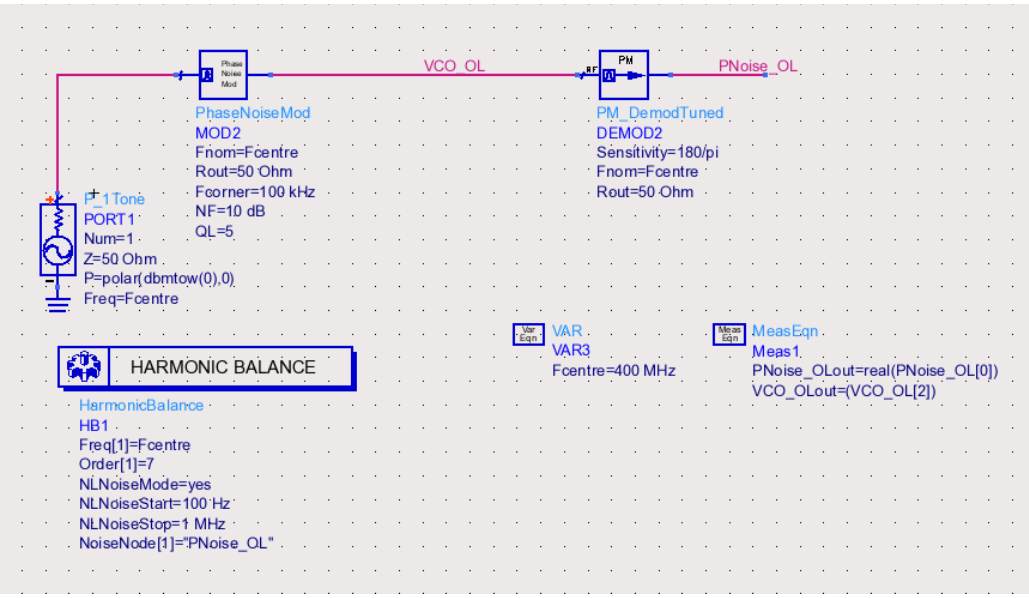


Fig 4.2: ADS simulation to calculate phase noise at 400 MHz

The loaded Q of the resonator is determined by the loaded Q of the inductor and the loaded Q of the varactor. Here, a MOSFET with its source and drain terminals shorted, is used as a varactor.

4.1.3 Frequency control

There are two types of varactors that can be implemented as a MOSFET. In the first type of varactor, a FET is connected as a diode with bulk connected to the drain and source while a reverse bias is applied to the gate as shown in figure 4.3.

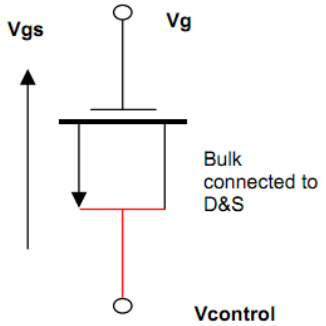


Fig 4.3: Implementation of a varactor by connecting together the source, drain and bulk of the MOSFET and applying a reverse bias across it [15]

A plot of capacitance versus control voltage, where $V_{control} - V_g = V_{gs}$, is shown figure 4.4.

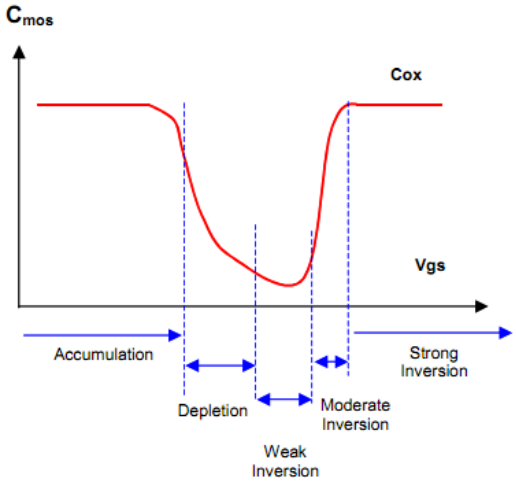


Fig 4.4: Capacitance variation of a PMOS capacitor with bulk, source and drain connected together [15]

The disadvantage of this type of capacitor is that the control voltage needs to be kept below weak inversion in order to maintain the capacitance reduction with increasing control voltage [15].

In the second type of varactor, the voltage is applied across the gate and bulk only with the source and drain unconnected. This is known as the accumulation varactor and is shown in figure 4.5.

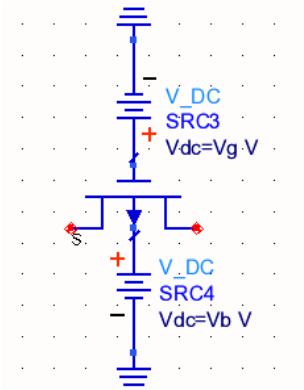


Fig 4.5: Accumulation varactor with source and drain terminals open and potential applied across gate and bulk [15]

Figure 4.6 shows a typical tuning characteristic curve of an accumulation varactor. The actual simulations using the MOSFET varactor are shown in figure 4.8.

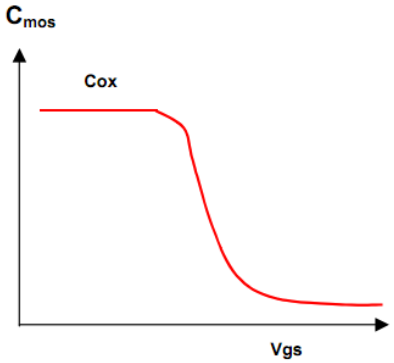


Fig 4.6: Capacitance variation of the accumulation varactor

The characteristic is more predictable since the capacitance always falls with increasing control voltage. For the LC VCO design, the accumulation varactor is used.

4.1.4 Varactor design

The MOSFET varactor changes its capacitance when its control voltage is varied. In order to find the minimum, maximum and nominal capacitances, the following equations are used [12]:

$$C_{max} = \frac{3.9\varepsilon_o WLN}{t_{ox}} \tag{4.8}$$

$$C_{min} = C_{gdo}W \tag{4.9}$$

where, C_{gdo} is the gate-drain capacitance, W and L are the width and length of the MOSFET, respectively, 3.9 is an empirical constant, N is the number of fingers, $\varepsilon_o = 8.854$ x 10^{-12} F/m and $t_{ox} = 9.59$ x 10^{-9} m.

Simulations are carried out for different values of W and L of the MOSFET, in order to find the minimum, maximum and nominal value of capacitances. They are tabulated in table 4.2.

Table 4.2 Maximum, minimum and nominal capacitance values for different width and length of FET

W (µm)	L (µm)	C_{MAX} (pF)	C_{NOM} (pF)	C_{MIN} (pF)
100	10	22.034	12.154	2.275
500	10	110.54	60.98	11.437
600	10	132.552	73.07	13.586
700	10	154.626	85.187	15.749
600	5	65.939	36.37	6.81
650	5	71.43	39.426	7.422
800	5	87.887	48.46	9.034
600	4	52.599	29.08	5.578
650	4	56.979	31.47	5.963
700	4	61.358	33.89	6.422
500	1	10.467	5.88	1.293
600	1	16.455	9.886	3.317

The schematic and simulation results of a p-type accumulation varactor with $W = 650\,\mu m$, $L = 4\,\mu m$ and $N = 5$ is shown in figures 4.7 and 4.8 respectively.

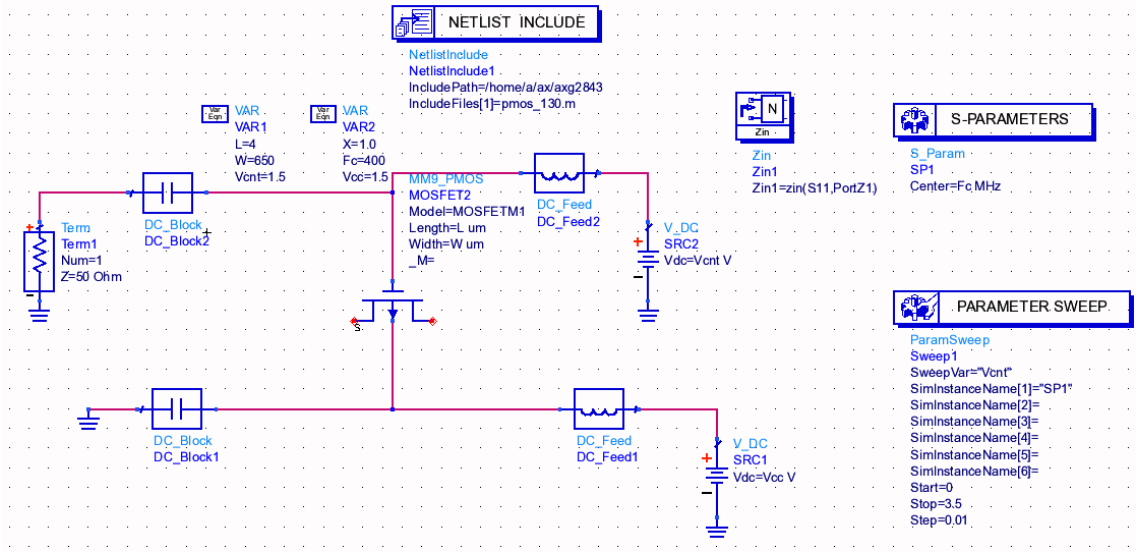


Fig 4.7: Schematic of a FET accumulation varactor with $W = 650\ \mu m$, $L = 4\ \mu m$ and $N = 5$

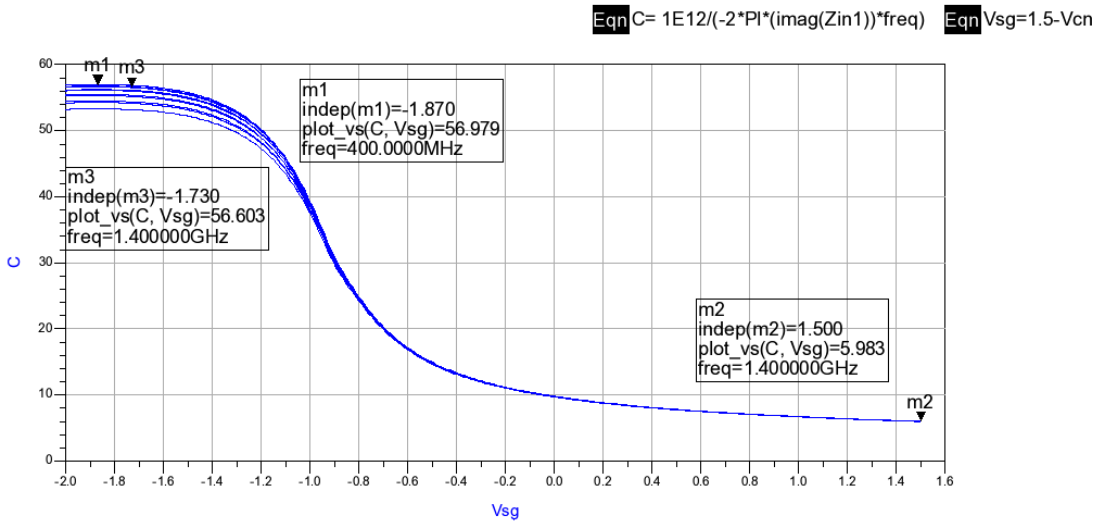


Fig 4.8: Simulation results of a FET accumulation varactor with$W = 650\ \mu m$, $L = 4\ \mu m$ and $N = 5$

An effective capacitance of 158 pF is used for the simulation of a 400 MHz oscillator with L=2 nH. The effective capacitance of 158 pF is caused by using two capacitances of 79 pF placed in parallel, for the desired frequency of oscillation (400 MHz).

4.1.5 Resonator Q and Bandwidth calculation

The overall unloaded Q of the resonator will depend on the loaded Q's of the inductor and varactor. If the varactor gate length is minimized and on-chip inductors are used, then the overall Q will be dominated by the inductor. The overall Q of the resonator is given by:

$$\frac{1}{Q_{resonator}} = \frac{1}{Q_{inductor}} + \frac{1}{Q_{varactor}} \tag{4.10}$$

The schematic and the simulation results for the unloaded Q of the resonator are shown in figure 4.9 and 4.10, respectively. The value of the loaded Q is found to be 5.27.

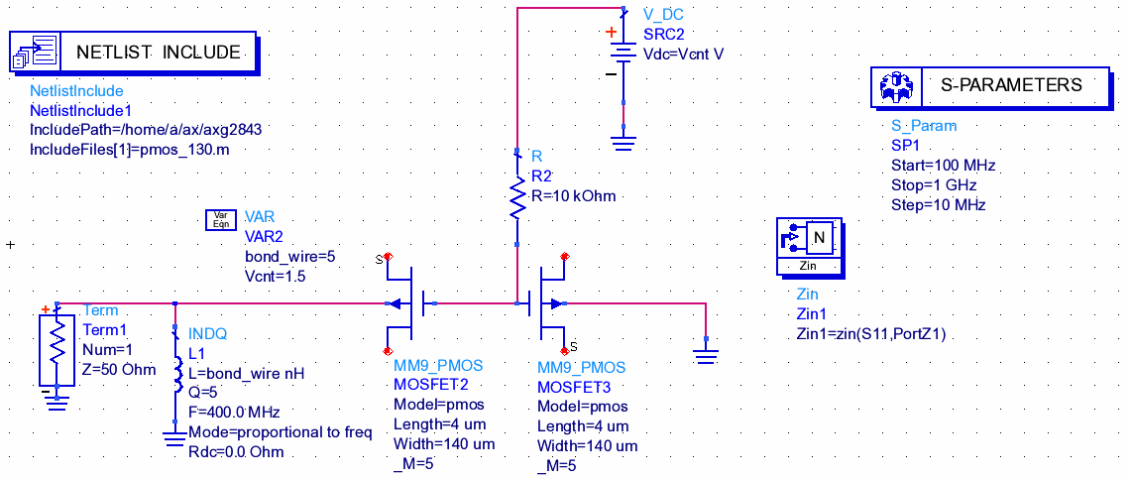


Fig 4.9: Schematic of the varactor to find the unloaded Q of the resonator

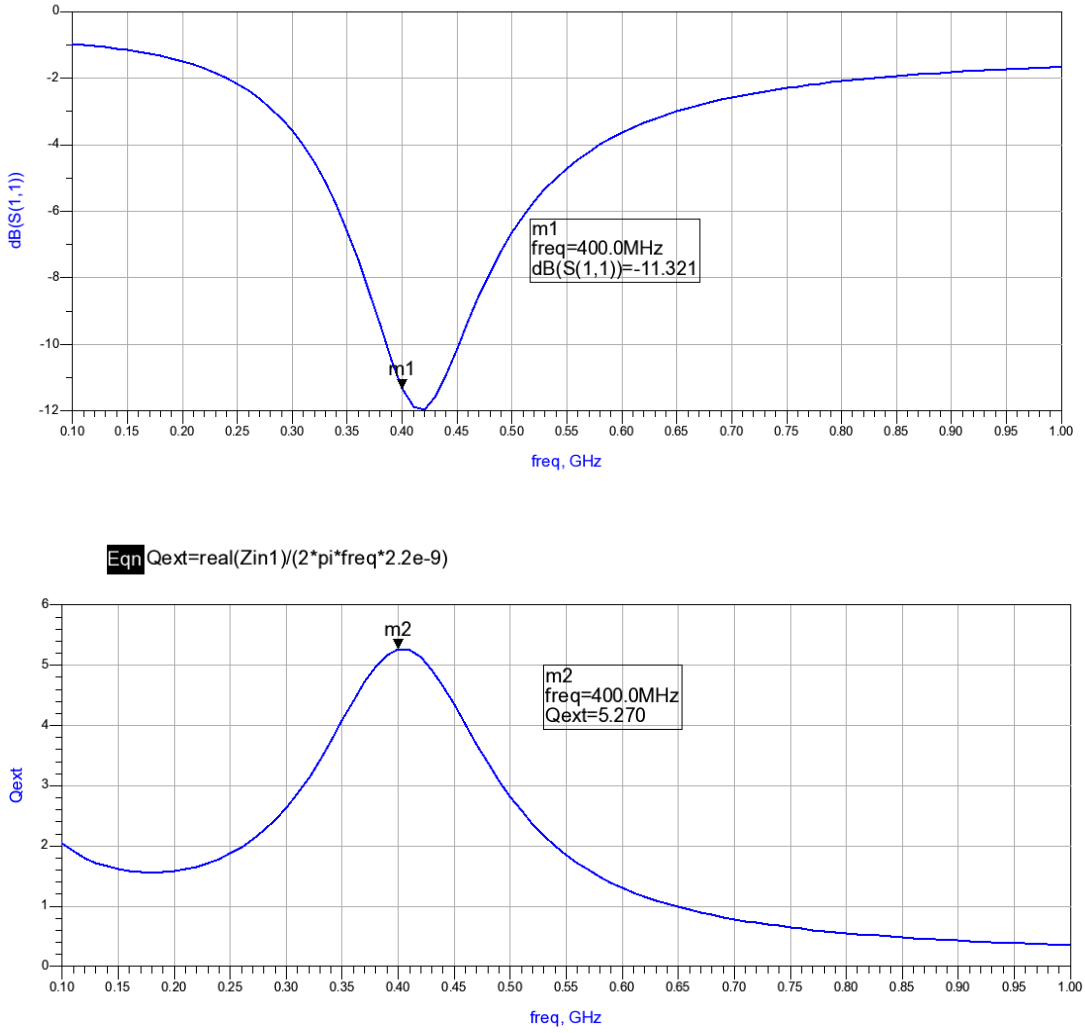


Fig 4.10: Frequency response of the reson ator shown in figure 4.9 showing the loaded Q

4.1.6 Amplifier G_m calculation

In order to determine the minimum negative g_m of the cross-coupled amplifier, the loss of the resonator is found first. R_{eq} is calculated as [15]:

$$R_{eq} = Q2\pi f_o L \tag{4.11}$$

An inductance of 4 nH is assumed. Using the values of L =4 nH, Q =5.2 and f_o=400 MHz, R_{eq} is found to be 51.88 Ω. Thus, the minimum g_m required for oscillation is given by [15]:

$$g_m > \frac{1}{R_{eq}} \tag{4.12}$$

Thus, g_m must be at least 20 mS. To give it sufficient margin, g_m is taken to be 30 mS. The start-up safety factor (A) is [15]:

$$A = \frac{30\ mS}{20\ mS} = 1.5 \tag{4.13}$$

Here, $g_m = g_{m(p)} + g_{m(n)}$, where

$$g_m = \sqrt{2K_{(n\ or\ p)} I_D \frac{W}{L}} \tag{4.14}$$

Re-arranging the terms in the equation (4.14), gives the minimum $\frac{W}{L}$ ratio for oscillation, which is [15]:

$$\frac{W}{L} = \frac{{g_m}^2}{2KI_D} \tag{4.15}$$

For n-channel MOSFETs, $K_n = \mu_n C_{ox}$, $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$. Using typical values for Silicon, $\varepsilon_{ox} = 3.97\varepsilon_0\ F/m$, $t_{ox} = 9.6 \text{ x } 10^{-9}\ m$ and $\mu_n = 471 \text{ x } 10^{-4}\ cm^2/V/s$, the value of K_n is obtained as $K_n = 171.7 \text{ x } 10^{-7}$. Similarly, $K_p = \mu_p C_{ox}$ and for $\mu_p = 136 \text{ x } 10^{-4}\ cm^2/V/s$, $K_p = 49 \text{ x } 10^{-6}$.

Table 4.3 List of $\left(\frac{W}{L}\right)_n$ and $\left(\frac{W}{L}\right)_p$ values for different drain currents (I_D)

I_D(mA)	$\left(\frac{W}{L}\right)_n$	$\left(\frac{W}{L}\right)_p$
1	90	300
5	20	60
10	9	30

If the drain current is too high it would result in large power consumption, and if the value of $\left(\frac{W}{L}\right)$ to is too large it would cause the layout area to be large. Hence, an optimum value of 20 and 60 are chosen for $\left(\frac{W}{L}\right)_n$ and $\left(\frac{W}{L}\right)_p$, respectively, for sustained oscillations.

The simulation results showed that a value of W=324 μm had to be used for L = 0.6 μm technology. The various values of control voltage and their corresponding frequencies are tabulated in table 4.4.

Table 4.4 Control voltage versus frequency of oscillations

V_{cntrl} (volts)	**Frequency (MHz)**
0.87	**410.67**
0.88	409.67
0.90	408.33
0.92	407.00
0.93	406.50
0.95	405.35
0.98	404.20
1.00	403.40
1.05	402.00
1.08	401.12
1.10	**400.801**
1.15	399.50
1.20	398.40
1.25	397.14
1.29	396.20
1.32	395.25
1.36	394.32
1.45	392.15
1.50	391.40
1.60	**390.40**

The linearity of the VCO frequency versus the control voltage is shown in figure 4.11:

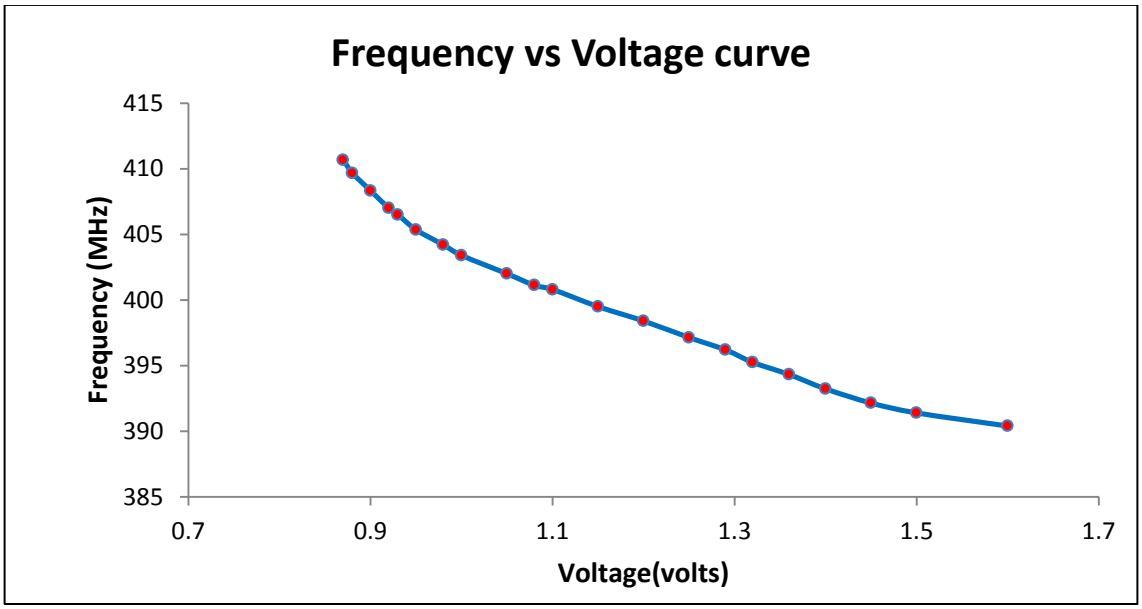


Fig 4.11: Frequency versus voltage curve showing the linearity of the LC VCO

4.1.7 Phase noise performance

The equation to estimate the phase noise in the LC VCO is given by [15]:

$$L(\Delta\omega) = \frac{kTR_{eff}[1+A]\left(\frac{\omega_o}{\Delta\omega}\right)^2}{\frac{V_A}{2}} \tag{4.16}$$

where, A is the start-up safety factor (A=1.5), V_A is the peak-voltage across the resonator, R_{eff} is the effective equivalent series resistance of the resonator and $\Delta\omega$ is the radial frequency offset from the carrier. Also,

$$R_{eff} = \frac{\omega L}{Q_{res}} = \frac{2\pi \text{ x } 400 \text{ x } 10^6 \text{x } 4 \text{ x } 10^{-9}}{5.161} = 2\Omega$$

Taking T=293 K, $k = 1.38 \text{ x } 10^{-23}$, $\Delta\omega = 10\ kHz$ and $V_A = 2.5\ V$ the phase noise is obtained as:

$$L(\Delta\omega) = \frac{1.38\ X\ 10^{-23}\ X\ 293\ X\ 2\ X\ (1+1.5)\ X\left(\frac{400\ X\ 10^6}{10\ X\ 10^3}\right)}{\frac{2.5}{2}} = 2.58X10^{-11} \quad \text{W} \tag{4.17}$$

$$L(\Delta\omega)(dB) = 10\ Log_{10}(2.58X10^{-11}) = -105.88\ dBc/Hz.$$

The phase noise has been calculated based on equation (4.17) for frequencies of 390.40 MHz, 400.801 MHz and 410.67 MHz and tabulated in table 4.5:

Table 4.5 Phase noise at different frequency of oscillations

V_{cntrl} (volts)	Frequency (MHz)	Phase Noise (dBc/Hz)
1.6	390.400	-138.0
1.1	400.801	-121.0
0.87	410.670	-106.0

Figures 4.12 and 4.13 show the complete LC VCO circuit simulated in ADS and the BSIM models used.

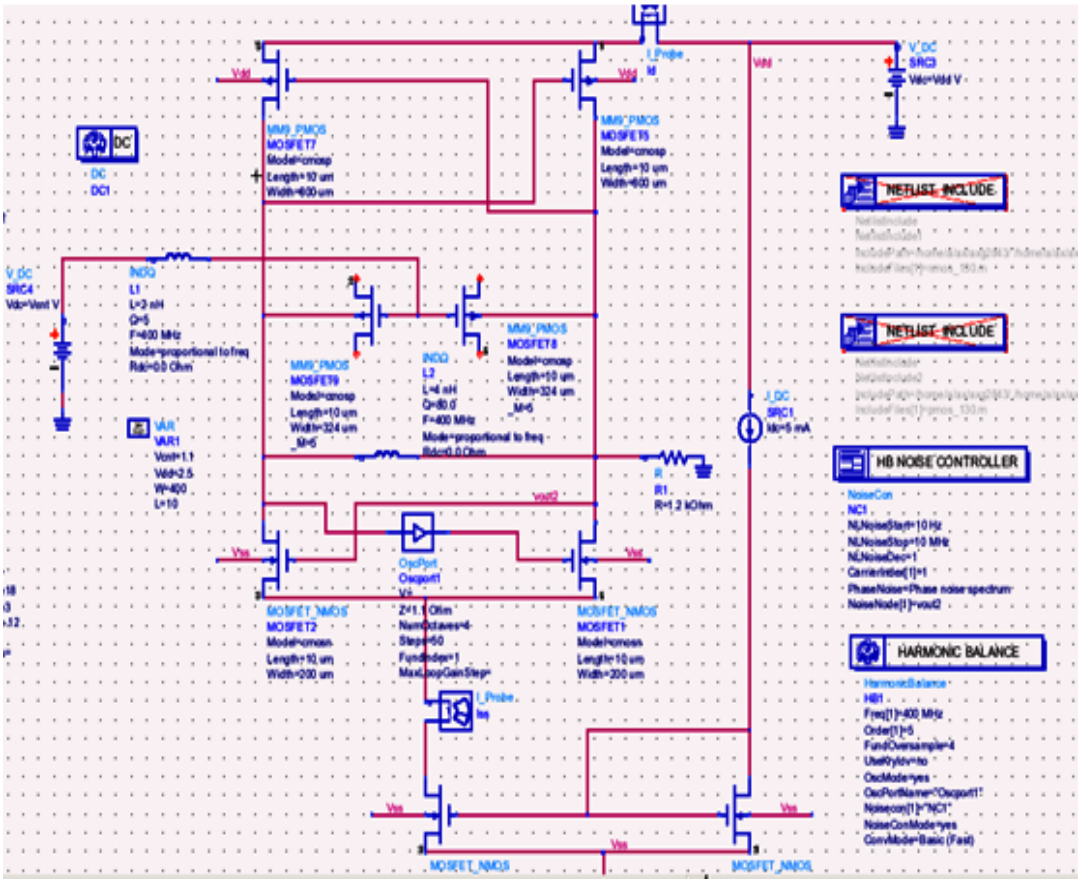


Fig 4.12: LC VCO simulation in ADS

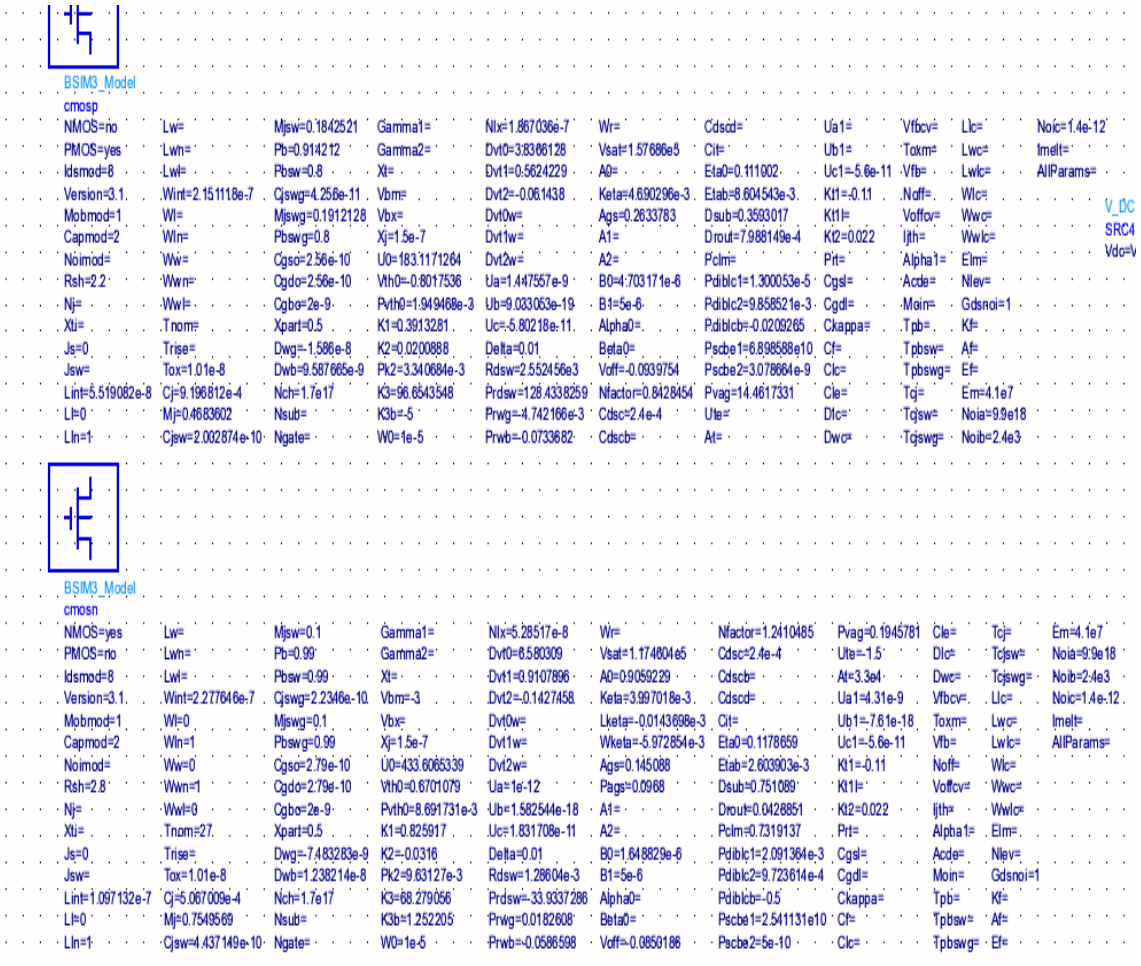


Fig 4.13: BSIM models for pmos and nmos transistors used in the LC VCO

Figures 4.14, 4.15 and 4.16 show the voltage spectrum, transient and phase noise, respectively, at 390 MHz. The oscillations have low distortion as seen in figures 4.14 and 4.15. Figure 4.16 denotes the phase noise where the phase noise denoted as *pnmx* is plotted against the frequency values.

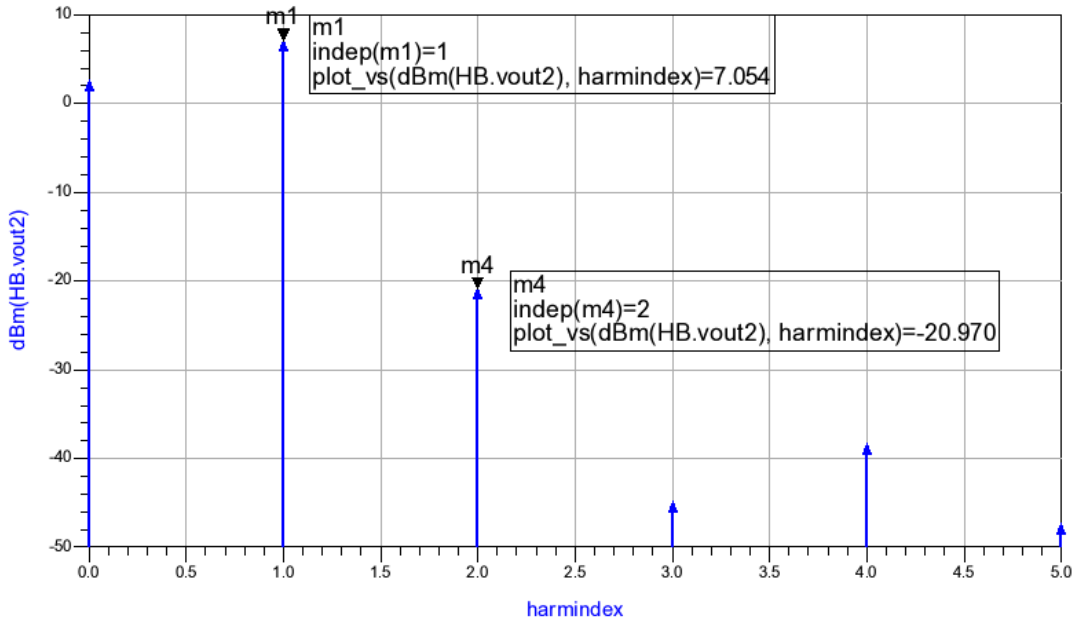


Fig 4.14: Voltage spectrum of the LC VCO at 390 MHz

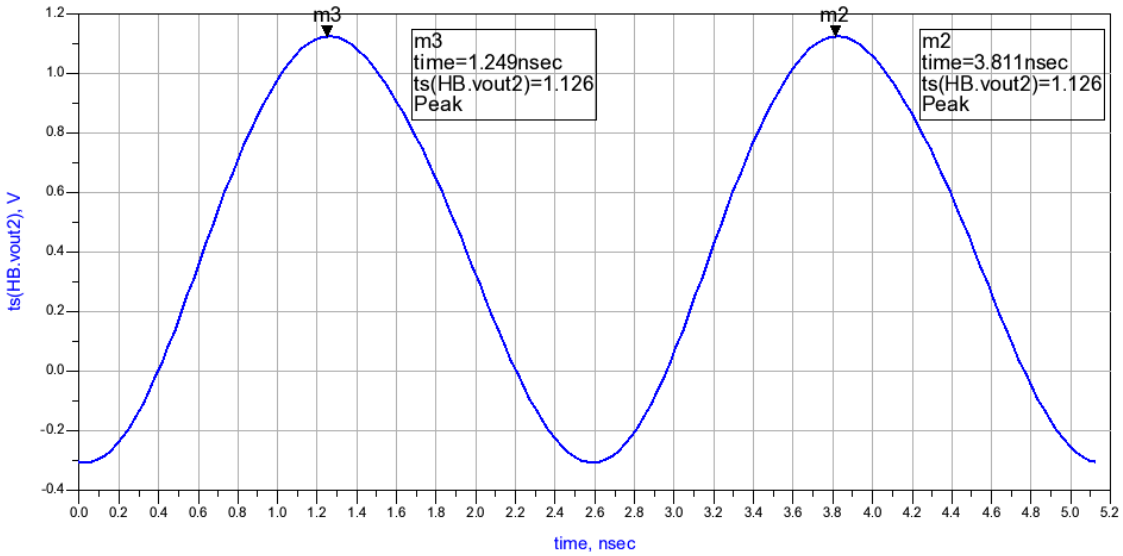


Fig 4.15: Transient output of the LC VCO at 390 MHz

The frequency of oscillation can be calculated as:

$$f = \frac{1}{\Delta T} = \frac{1}{3.811 - 1.249}\ ns = 390.32\ MHz$$

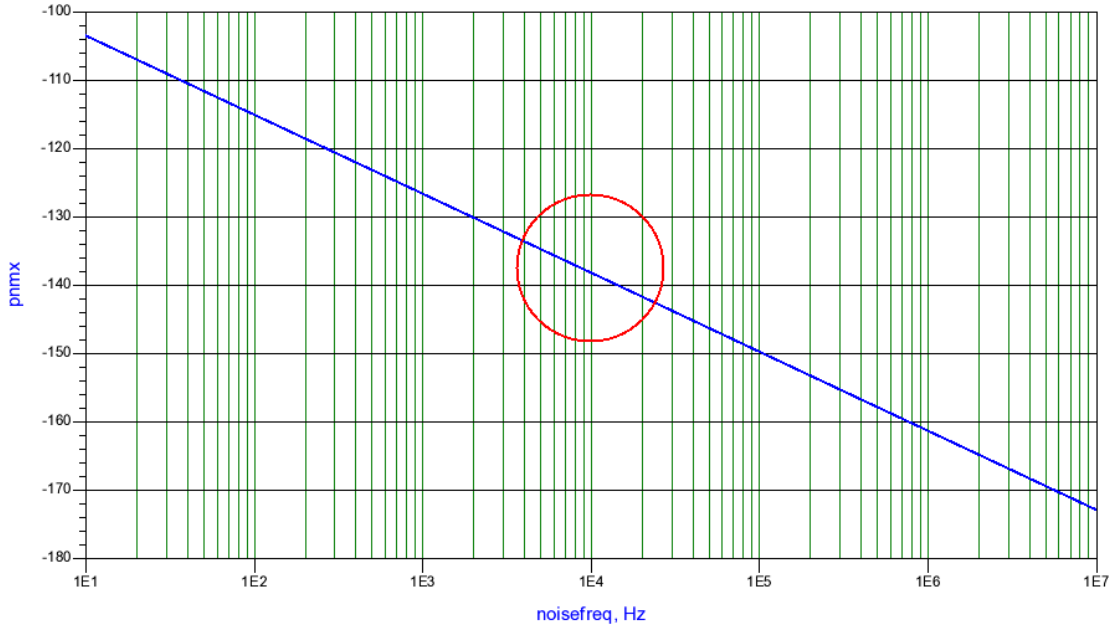


Fig 4.16: Phase noise of the LC VCO at 390.32 MHz

Figure 4.17, figure 4.18 and figure 4.19 show the voltage spectrum, transient output and phase noise, respectively, at 400 MHz. The phase noise at 10 kHz offset is circled in the figure.

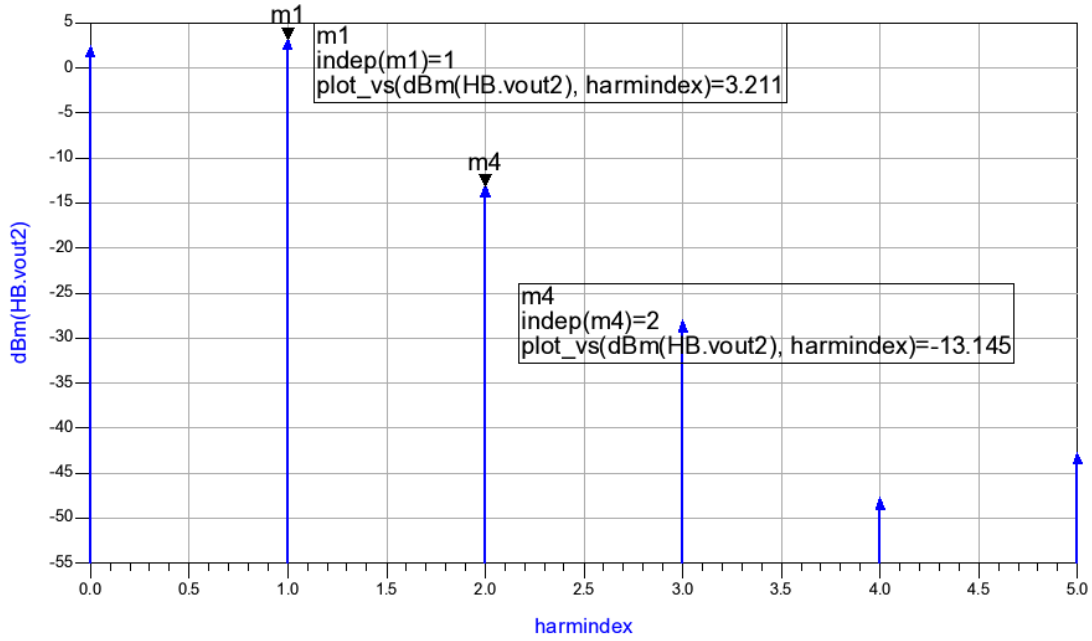


Fig 4.17: Voltage spectrum of the LC VCO at 400 MHz

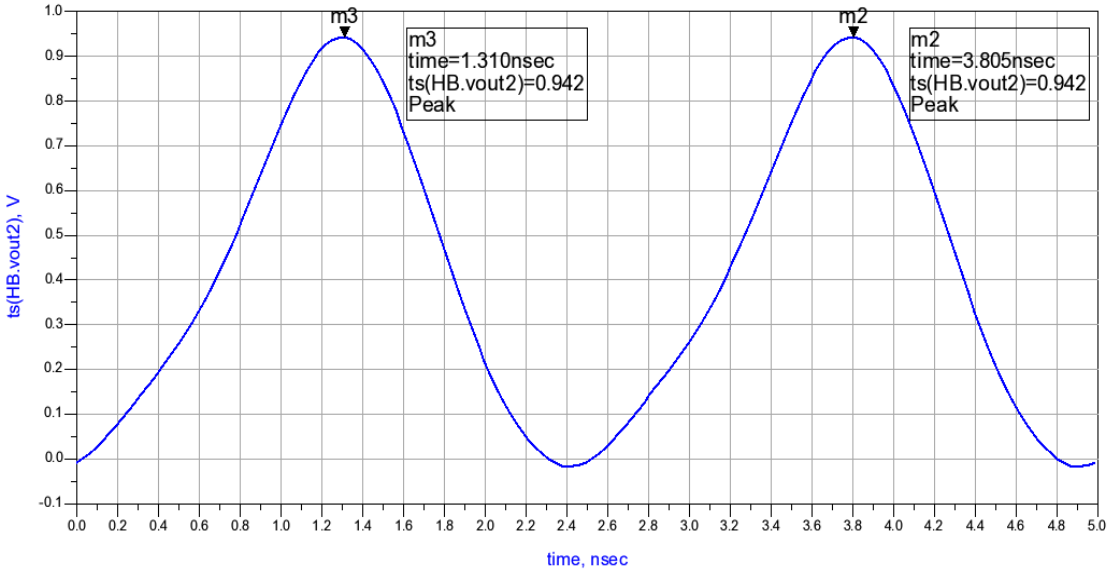


Fig 4.18: Transient output of the LC VCO at 400 MHz

The frequency of oscillation is calculated as:

$$f = \frac{1}{\Delta T} = \frac{1}{3.805 - 1.310}\ ns = 400.801\ MHz$$

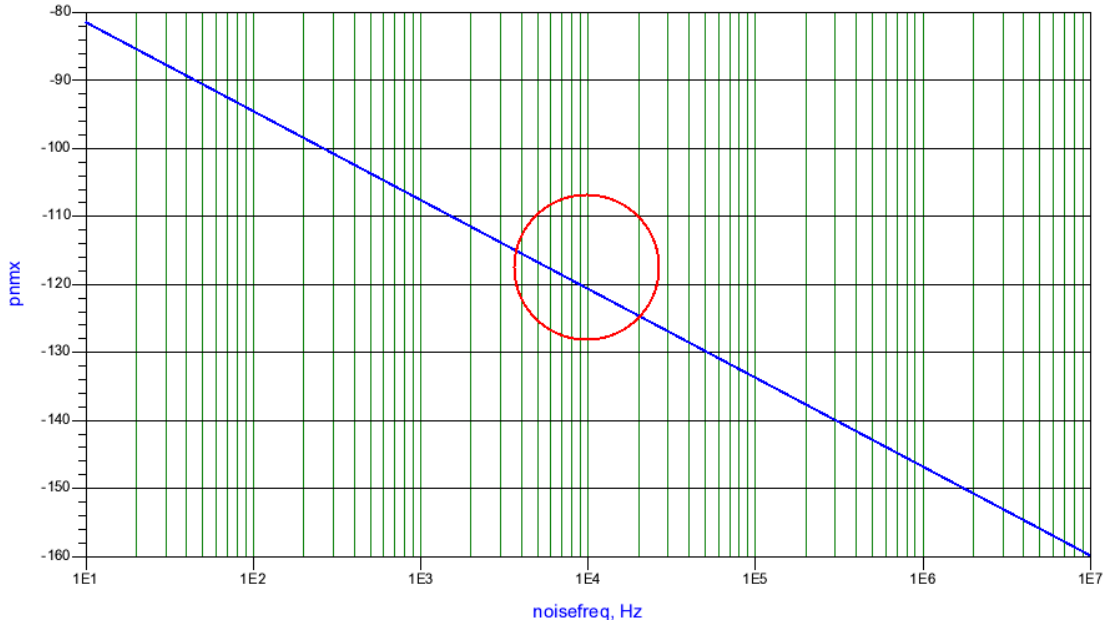


Fig 4.19: Phase noise of the LC VCO at 400.801 MHz

Figure 4.20, figure 4.21 and figure 4.22 show the voltage spectrum, transient output and phase noise, respectively, at 410 MHz.

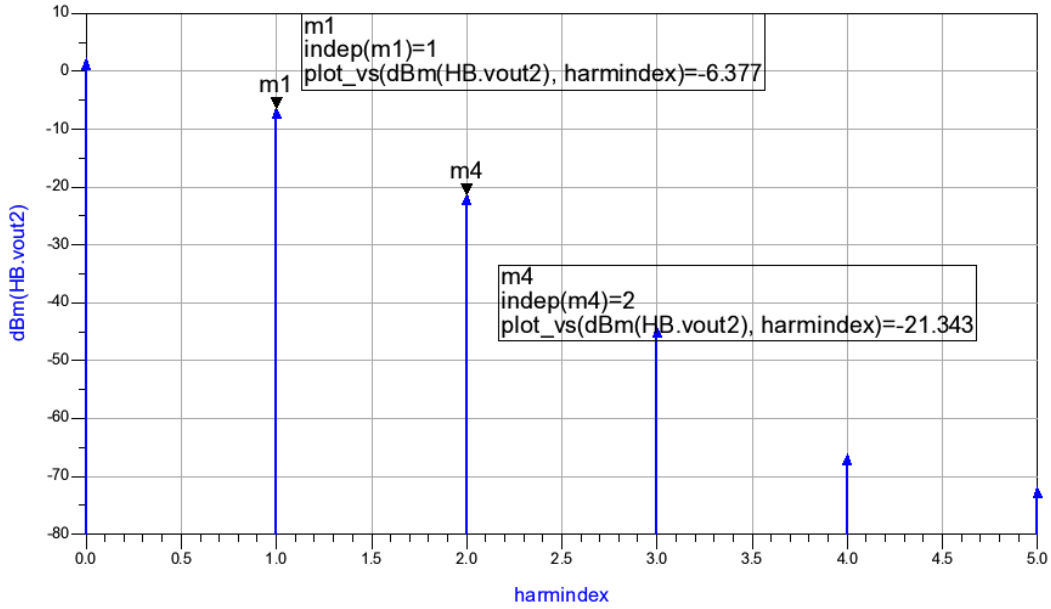


Fig 4.20: Voltage spectrum of the LC VCO at 410 MHz

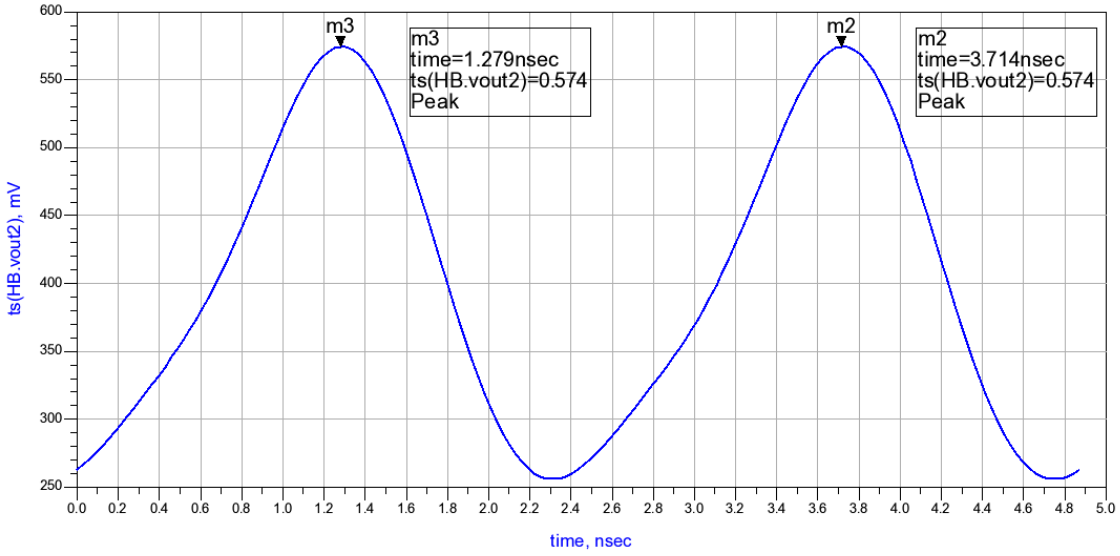


Fig 4.21: Transient output of the LC VCO at 410 MHz

The frequency of oscillation is calculated as:

$$f = \frac{1}{\Delta T} = \frac{1}{3.714 - 1.279} ns = 410.67\ MHz$$

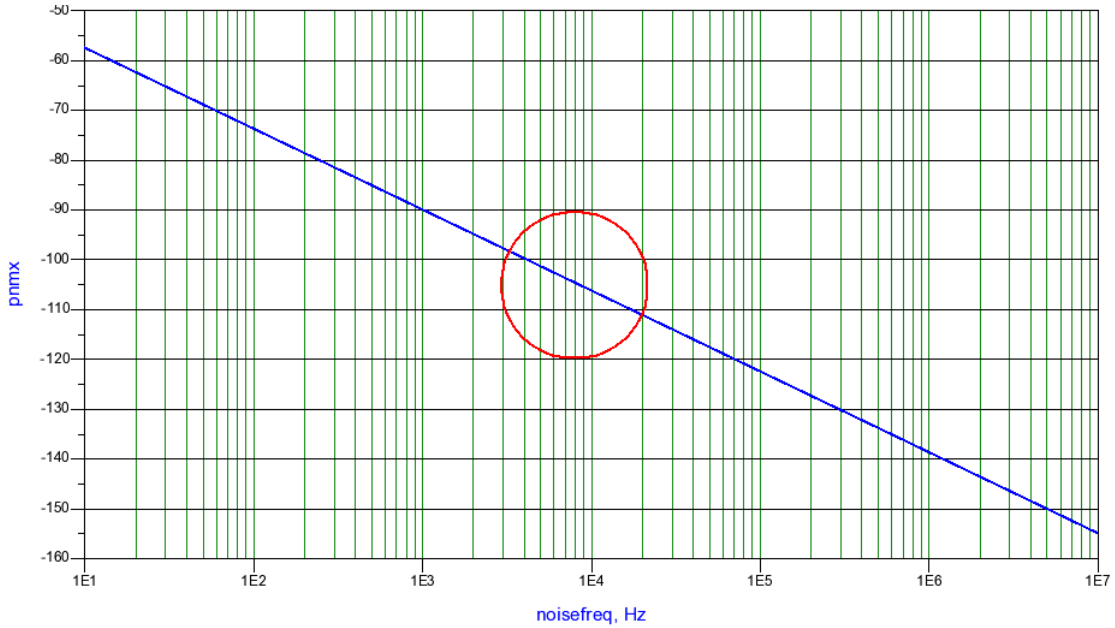


Fig 4.22: Phase noise of the LC VCO at 410.67 MHz

4.2 Colpitts Oscillator Design

4.2.1 Colpitts oscillator design

The oscillator used for a printed circuit board level implementation is a Colpitts oscillator. The theory and simulations of the previous chapter are applicable in designing a Colpitts oscillator since it is the half circuit of the previously described oscillator. Some of the advantages of the Colpitts oscillator are simple design and good stability at high frequency [1]. A simple design involving few capacitors and inductors is a good choice for an oscillator design to minimize parasitics involved during fabrication. This enhances the spectral purity of the wave.

4.2.2 Schematic of the LC Colpitts oscillator in ADS

In order to implement the VCO design on a printed circuit board, the ADS schematic and layout programs were used [17]. The simulations included IC level implementation. The discrete oscillator was built. A Colpitts oscillator's frequency is determined by a tank circuit using two capacitors and an inductor. The feedback needed for oscillation is taken from a voltage divider made of two capacitors. The frequency of oscillation is given by [17]:

$$f_0 = 1/(2\pi\sqrt{L(\frac{C_1C_2}{C_1+C_2})}) \quad (4.17)$$

Figure 4.23 shows the schematic of the Colpitts oscillator in ADS. A BJT in the common collector configuration is used. The desired BJT is a BFR360F which has a high transition frequency of 11 GHz and is denoted as X_1 and X_2 in the figure. Transistor X_2 serves as a buffer. The output of the oscillator gives ripples which can be eliminated with a high Q circuit composed of a capacitor and inductor tied between the output and the voltage supply. The DC supply used is 5 V. The capacitor C_9 is used as a DC blocking capacitor while the Inductor L_2 is used to block any high frequency harmonics entering the spectrum analyzer. The resistors R_1, R_2, R_3 and R_4 are used for biasing the circuit. The capacitors C_1, C_2, C_3 and the inductor L_1 form the tank circuit. The characteristics for the BFR360F BJT are given in table 4.6.

Table 4.6: Characteristics of BRF360F transistor

Symbol	**Acronym**	**Value**	**Units**
I_S	Saturation current	68.82 E-18	A
β_F	Forward beta	147	---
Vaf	Forward Early voltage	20	V
Ise	Base-Emitter leakage saturation current	150E-15	A
Re	Emitter resistance	78.2E-3	Ohm
Cje	Base-Emitter zero-bias depletion cap	400E-15	F
T_f	Forward transit time	9.22E-12	sec

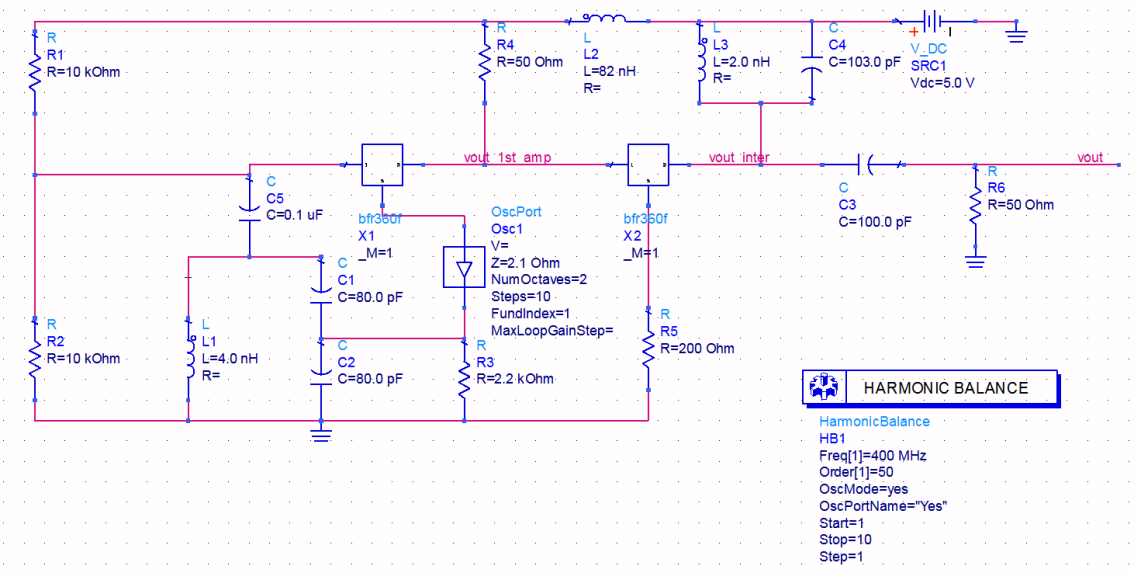


Fig 4.23: Colpitts Oscillator schematic in ADS

Figure 4.24 shows the oscillations before and after the buffer transistor used in the oscillator circuit. It acts to nullify the ripples and drive a 50 ohm impedance line. Figure 4.25 shows the harmonics of 391 MHz. The 1st harmonic lies 27 dB below the fundamental frequency of 391 MHz.

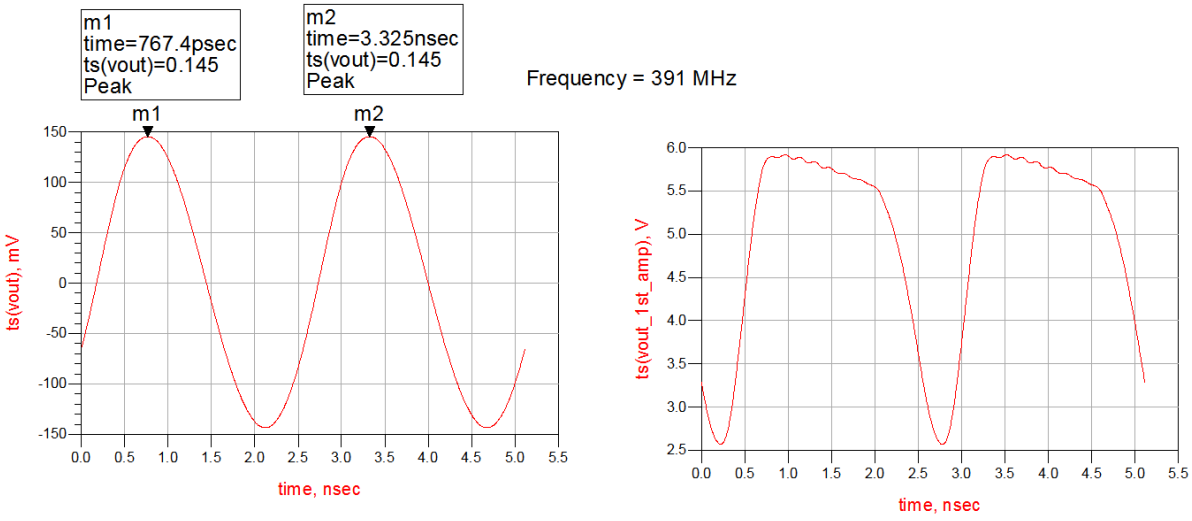


Fig 4.24: Oscillation frequencies in the schematic after and before the buffer transistor

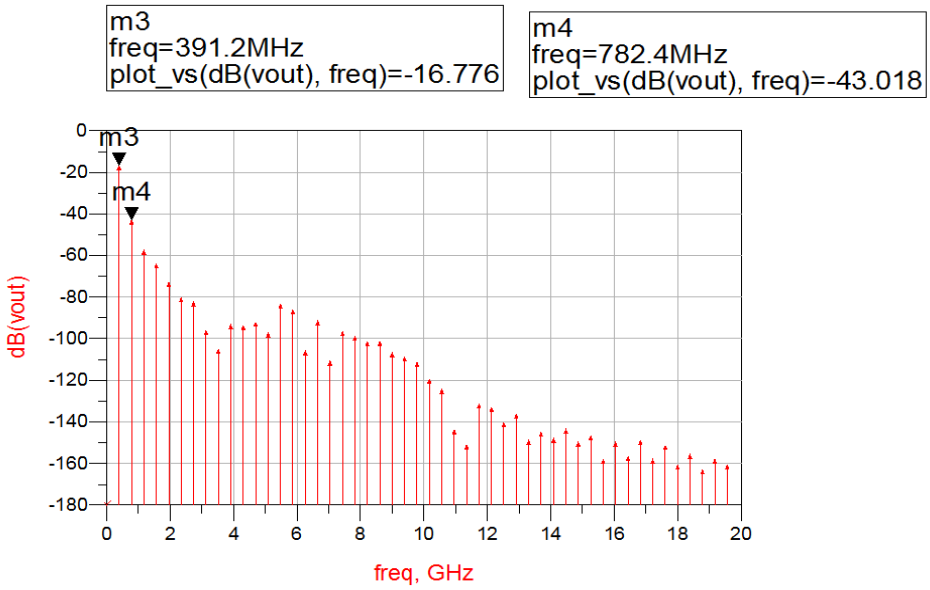


Fig 4.25: Harmonics of the oscillator at 391.2 MHz

By changing the capacitance, a different value of frequency is obtained. This shows the tunability of the oscillator. A capacitance of 45 pF gives a frequency of 461 MHz while a capacitance of 100 pF gives a frequency of 352.2 MHz. Table 4.7 gives the capacitance versus frequency values. The voltage versus frequency curve is plotted as shown in figure 4.26.

Table 4.7: Capacitance versus Frequency values

Capacitance (pF)	Frequency (MHz)
45	461
50	452.1
55	441.7
60	430.3
65	419.6
70	410.8
75	399.5
80	391.2
85	380.2
90	370.6
95	362.4
100	352.2

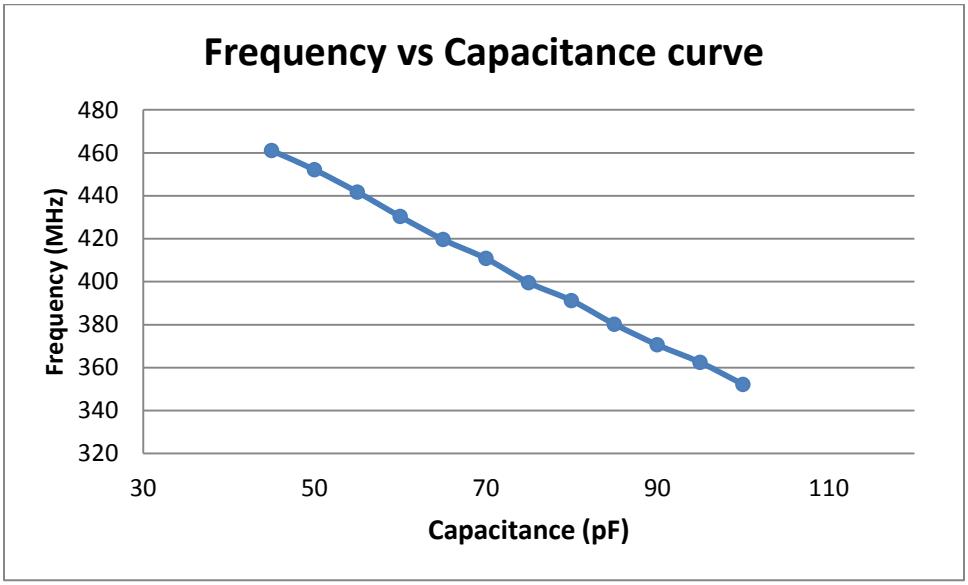
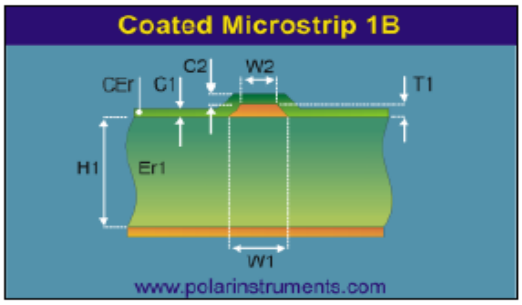


Fig 4.26: Frequency versus capacitance curve of the oscillator

4.2.3 Layout of the LC VCO

The layout of the oscillator was designed using ADS. The width of the transmission lines were designed to have characteristic impedance of 50 ohm. Figure 4.27 shows the transmission line width calculations for the FR4 board with the given dielectric, characteristic impedance and height. The circuit uses two layers of which the top layer is used for signals, and the bottom layer serves as the ground. The EM (Electro-Magnetic) simulation is carried out in order to show the frequency response not captured by analytical models. Planar EM simulators provide an arbitrary planar geometry. It is used when there is more than one layer and when coupling between the layers is significant. Figure 4.28 shows the oscillator layout in ADS. The frequency of oscillation simulated in layout is found to be 374.7 MHz as shown in Figure 4.29. This shows the parasitic effects of interconnects due to which the frequency of simulation reduces in simulation.



				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	12.3500	+/-	0.0000	12.3500	12.3500
Substrate 1 Dielectric	Er1	4.3000	+/-	0.0000	4.3000	4.3000
Lower Trace Width	W1	22.0000	+/-	0.0000	22.0000	22.0000
Upper Trace Width	W2	21.0000	+/-	0.0000	21.0000	21.0000
Trace Thickness	T1	2.0000	+/-	0.0000	2.0000	2.0000
Coating Above Substrate	C1	1.0000	+/-	0.0000	1.0000	1.0000
Coating Above Trace	C2	0.5000	+/-	0.0000	0.5000	0.5000
Coating Dielectric	CEr	4.0000	+/-	0.0000	4.0000	4.0000
Impedance	Zo	49.47		-----	49.47	49.47
Delay (ps/in)	D	153.975		-----	153.975	153.975
Inductance (nH/in)	L	7.618		-----	7.618	7.618
Capacitance (pF/in)	C	3.112		-----	3.112	3.112

Fig 4.27: Transmission line width calculation

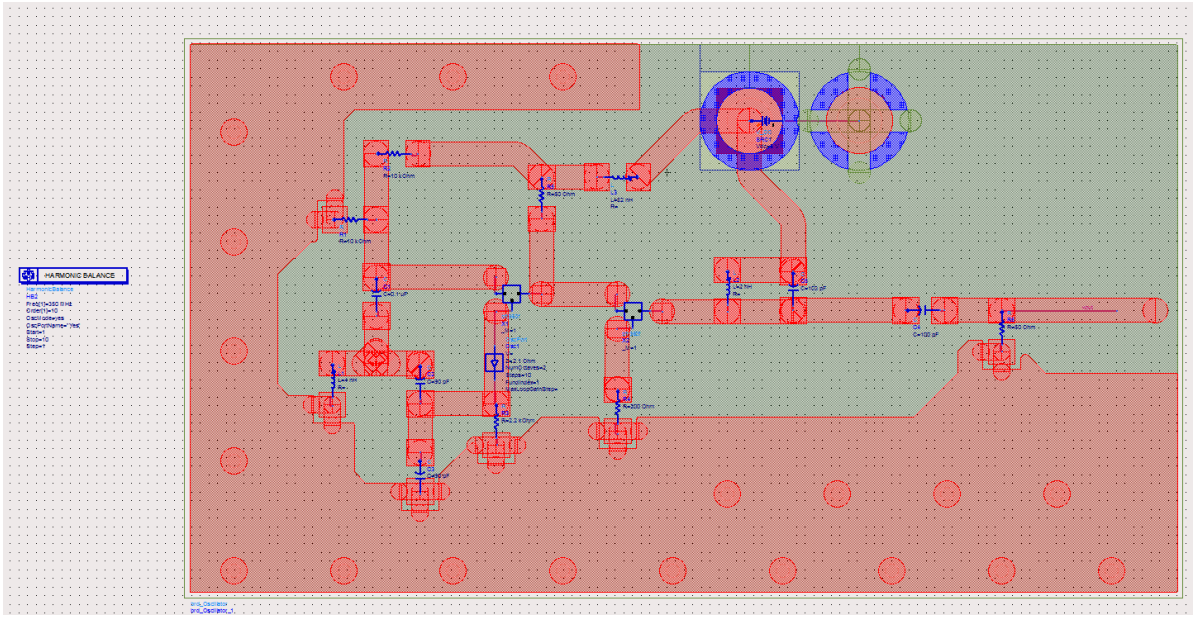


Fig 4.28: Oscillator layout in ADS

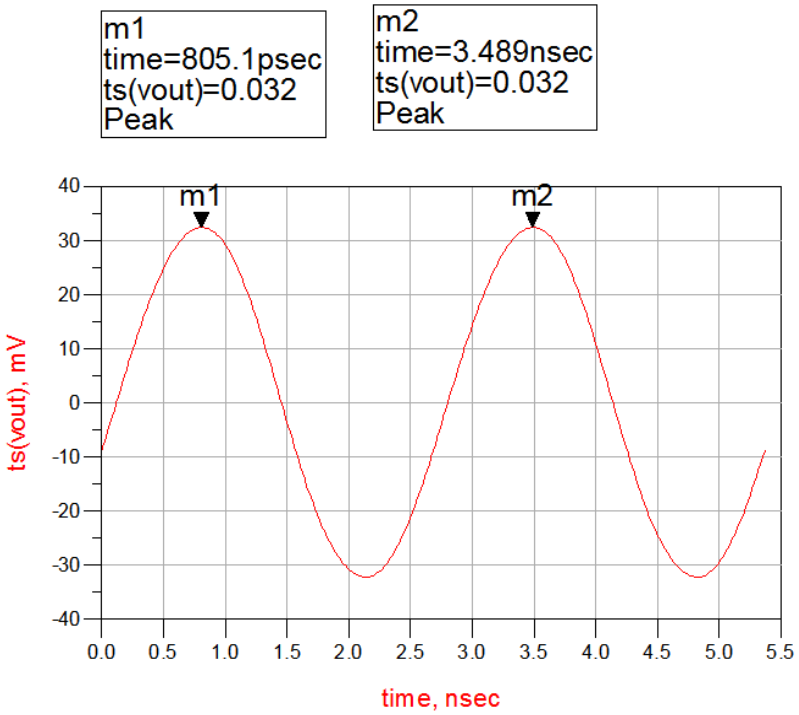


Fig 4.29: Frequency of oscillation in Layout

4.3 Fabrication and measurements of the VCO

The dimensions of the fabricated two sided copper clad board are 1.5” x 0.6”. A gerber file is created from this final layout which is used by the PCB vendor to make the board [19]. Once the board has been designed, the components are soldered on to the board carefully so that they conform to both the location and their orientation. The LC VCO printed circuit board is shown in figure 4.30.

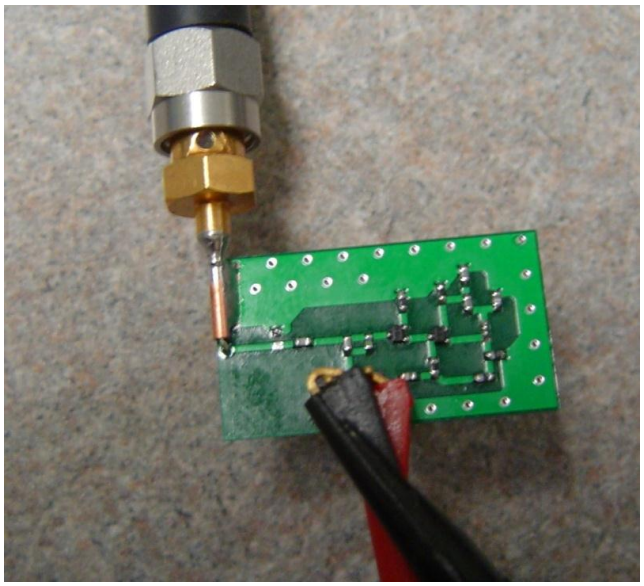


Fig 4.30: The printed circuit board of the LC VCO

The frequency of oscillation was found to be at 381.14 MHz as shown in Figure 4.31. The input DC voltage at which the oscillations start is 6.5 V and the current drawn is 5 mA. The amplitude was found to be -9.17 dBm. The tank circuit comprised of a capacitance of 75 pF and an inductance of 3.9 nH.

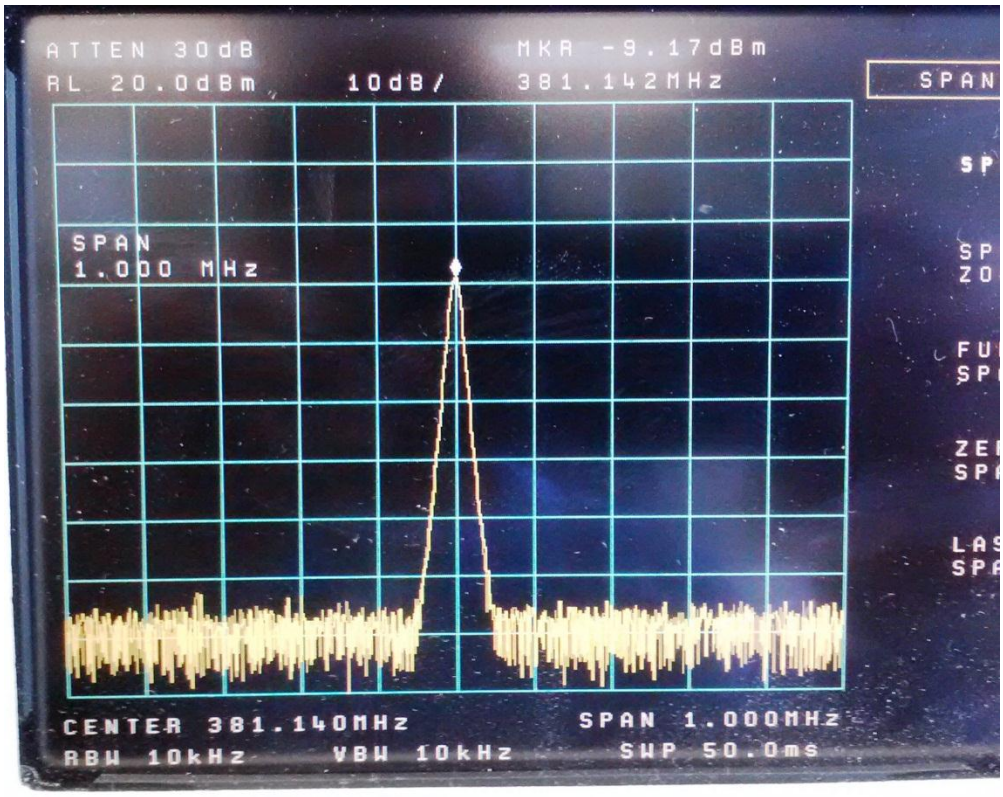


Fig 4.31: Frequency of oscillations at 381.14 MHz on a Spectrum Analyzer

Changing the value of capacitance in the tank circuit, produces a different oscillation frequency. When a capacitance of 45 pF is used, the frequency of oscillation is 464.8 MHz and – 10.67 dBm as shown in figure 4.32. A capacitance of 105 pF gives an oscillation frequency of 300.47 MHz and amplitude of -9.5 dBm. Figure 4.33 shows the oscillation frequency at 300.47 MHz. Table 4.8 shows the difference between the theoretical and measured values:

Table 4.8: Difference between the theoretical and measured values

Theoretical values	**Measured values**
Frequency = 381.14 MHz	Frequency = 391 MHz
V_{DC} = 5 V	V_{DC} = 6.5 V
I_{DC} = 5 mA	I_{DC} = 5.1 mA
L_{Tank} = 4.0 nH	L_{Tank} = 3.9 nH
C_{Tank} = 80 pF	C_{Tank} = 80 pF
V_{out} = -14.13 dBm	V_{out} = -9.17 dBm

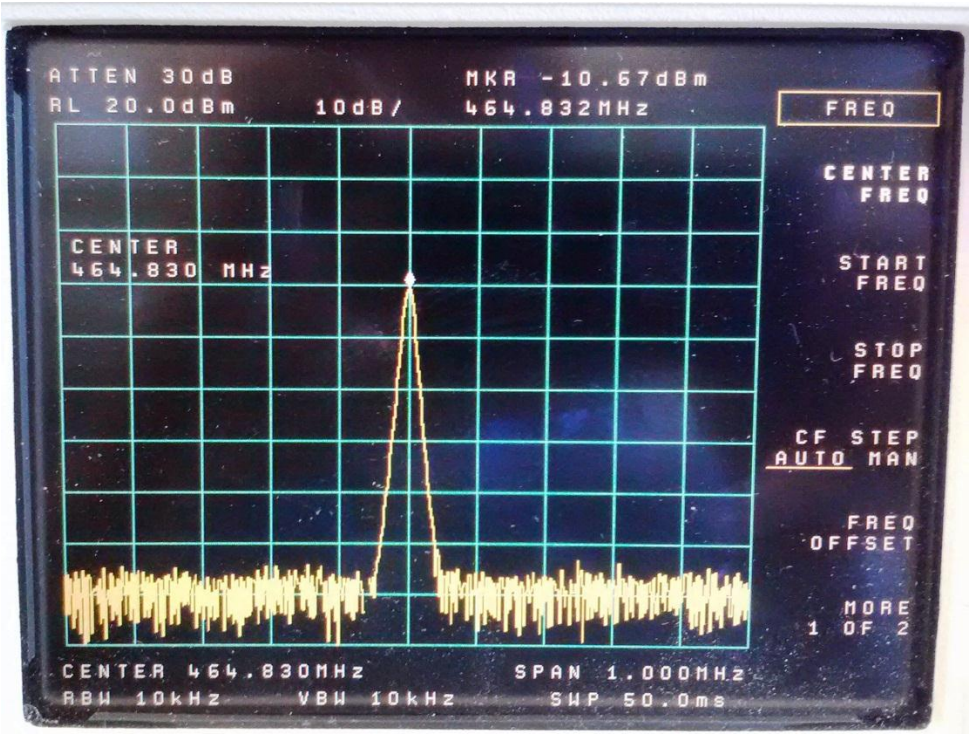


Fig 4.32: Frequency of oscillations at 464.8 MHz

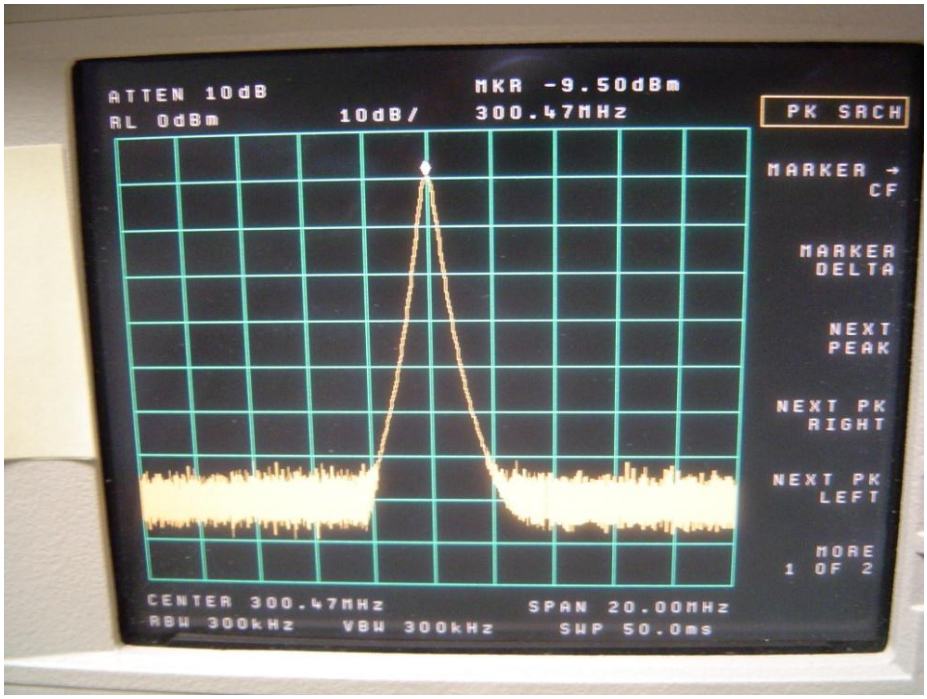


Fig 4.33: Frequency of oscillations at 300.47 MHz.

The board layout and the parasitics, which include interconnect inductances, resistances and capacitances are the main causes for a 2.55% frequency difference (from 391 MHz to 381.14 MHz) between the ADS design performance and the experimental results. The board layers have some finite resistance and capacitance which causes the frequency to shift from an ideal value to the actual value. Computing the capacitance of the lines on the FR4 with ε_r = 4.3, the parasitic capacitance per unit length caused by the board is found to be 67.54 pF/m. Using this value in simulations would result in a frequency of 395.92 MHz instead of the ideal value of 381.14 MHz as shown in figures 4.34 and 4.35.

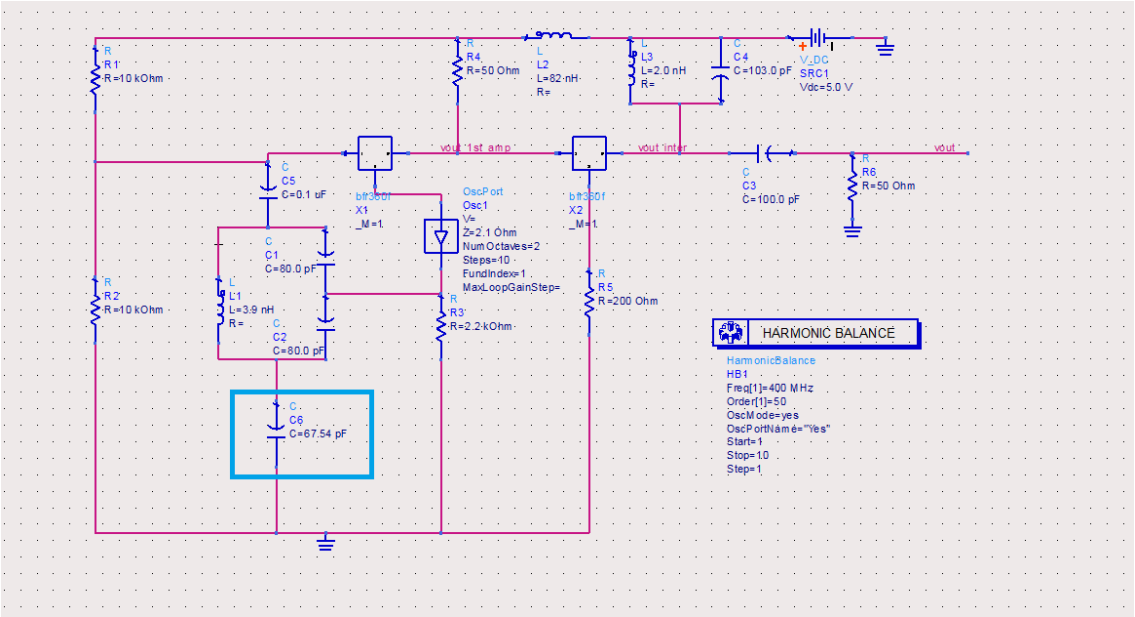


Fig 4.34: Circuit of the oscillator including the parasitic capacitance

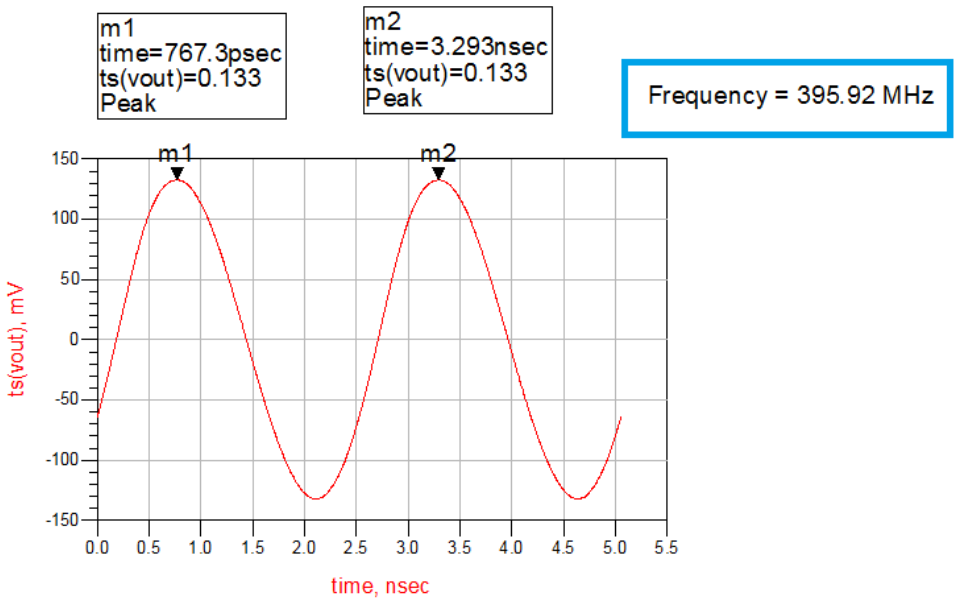


Fig 4.35: Simulation showing the frequency change due to the parasitic capacitance

Another factor which causes the frequency variation is that the components which were used in the design were not ideal. An inductance of 3.9 nH was available which was used in place of an ideal value of 4 nH used in simulations in the tank circuit. Using a value of 3.9 nH in simulations would result in a frequency of 395.69 MHz as shown in figures 4.36 and 4.37. This shows the effect of change in frequency using the practical value of 3.9 nH on the board for the oscillations.

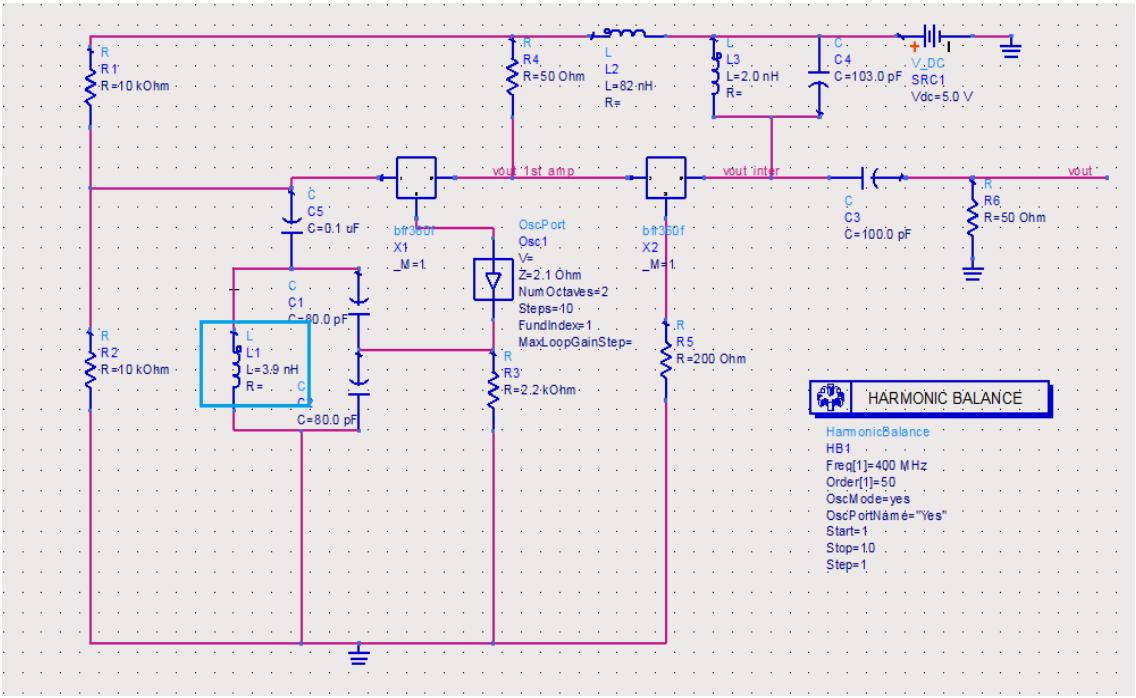


Fig 4.36: Circuit showing the ideal 3.9 nH inductance used in the oscillator tank circuit

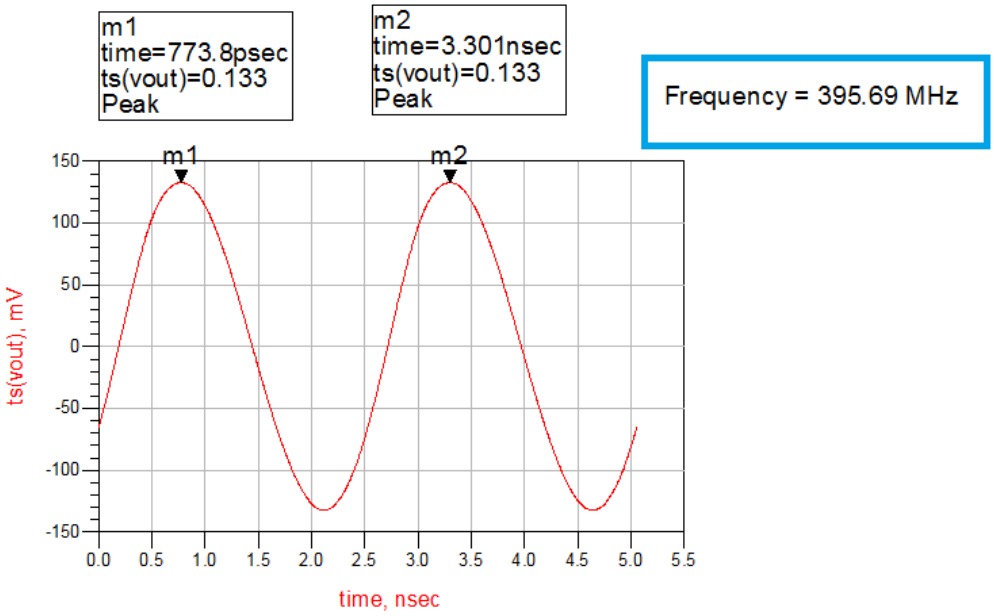


Fig 4.37: Simulations using the 3.9 nH inductance in the oscillators tank circuit

The copper interconnects add some parasitic capacitance to the calculated frequency which again cause a frequency deviation from the ideal value. Using figure 4.27 for calculating the capacitance of the copper interconnects, its value is found to be 56.3 pF. The simulation including this parasitic capacitance is shown in figure 4.38. The resulting frequency is 398 MHz as shown in figure 4.39.

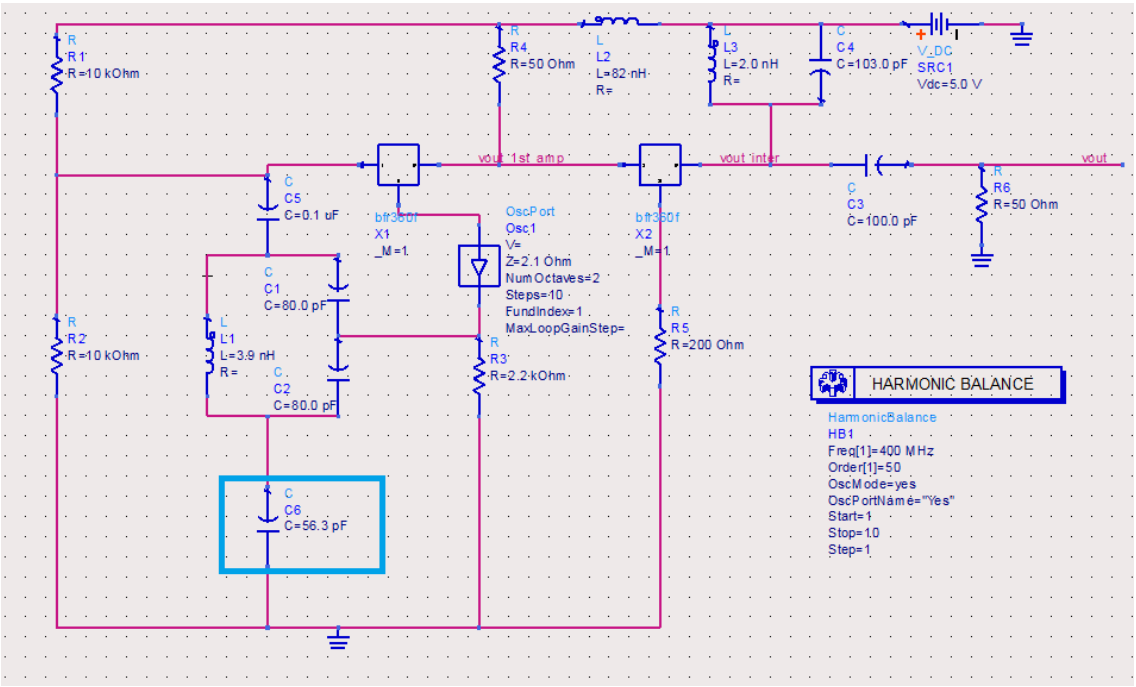


Fig 4.38: Circuit showing the interconnect capacitance of 56.3 pF

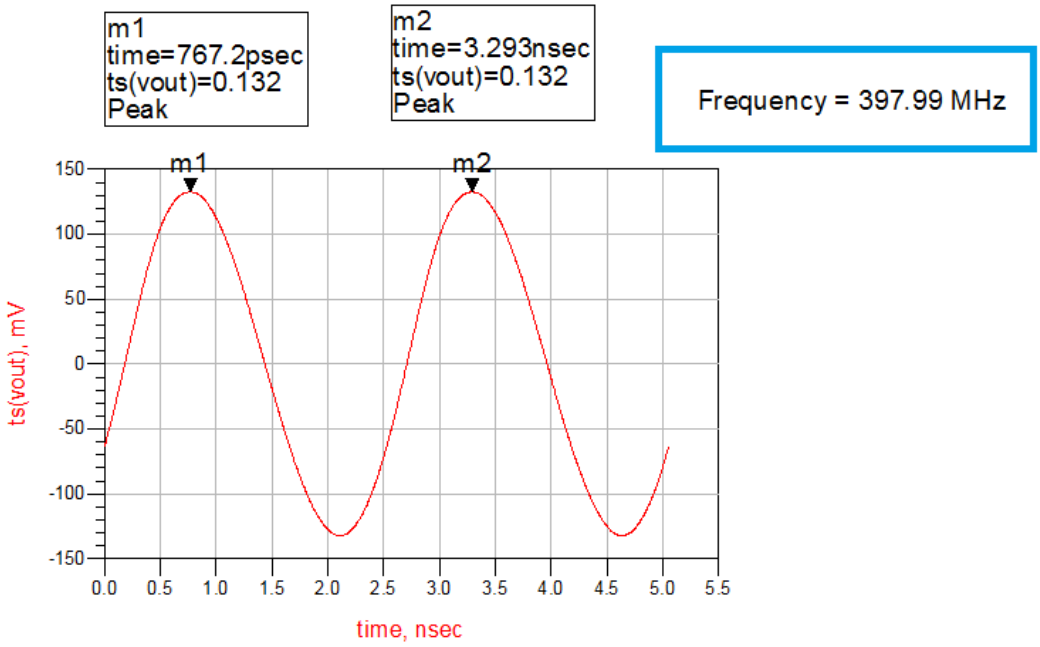


Fig 4.39: Frequency of oscillations using the interconnect parasitics

The capacitors, inductors and resistors have some tolerance values. This also accounts to the change in frequency of oscillations. The inductance of 3.9nH used has a tolerance value of ±5 %. This shows that the inductance of 3.9 nH used can vary from 4.095 nH to 3.705 nH. Simulating these inductance values gives a frequency of 386.7 MHz and 405 MHz, respectively, as shown in figures 4.40 and 4.42.

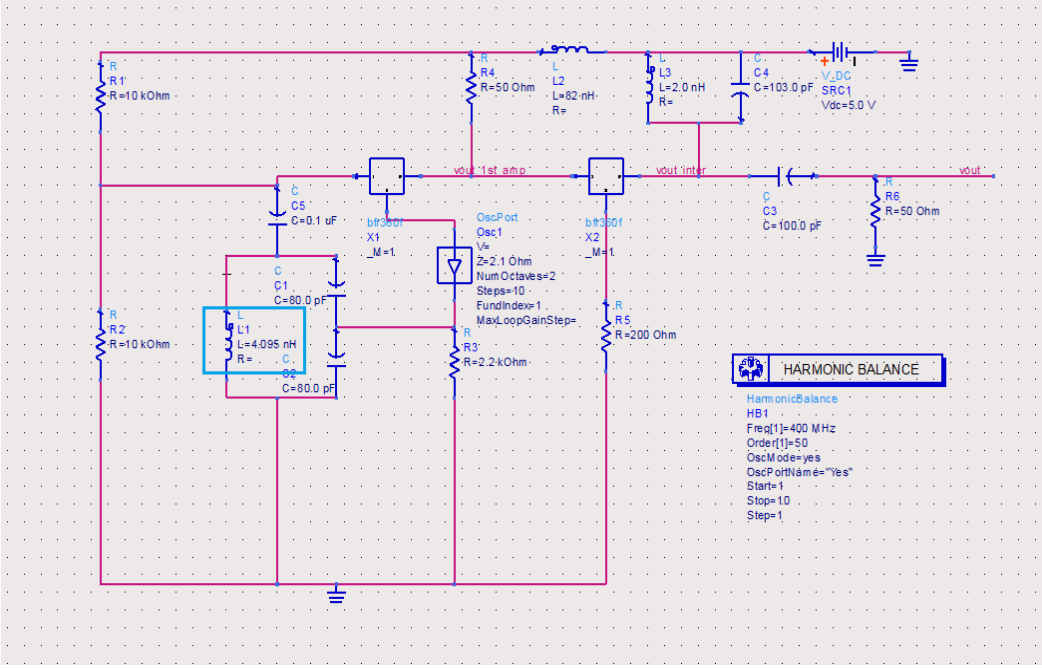


Fig 4.40: Inductance of 4.095 nH used in the oscillator tank circuit

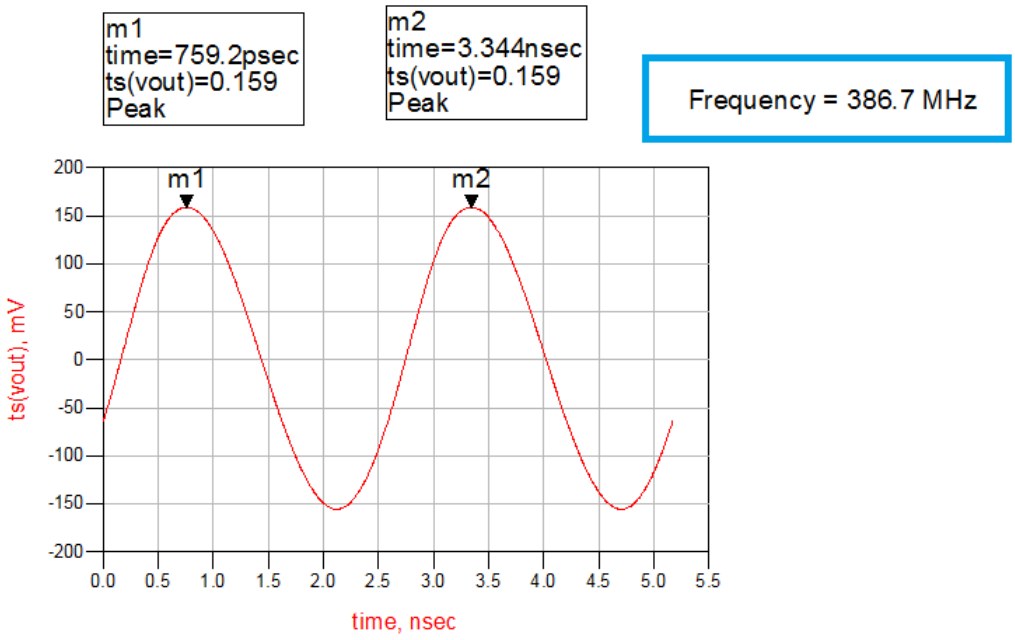


Fig 4.41: Frequency of oscillations using the 4.095 nH inductance

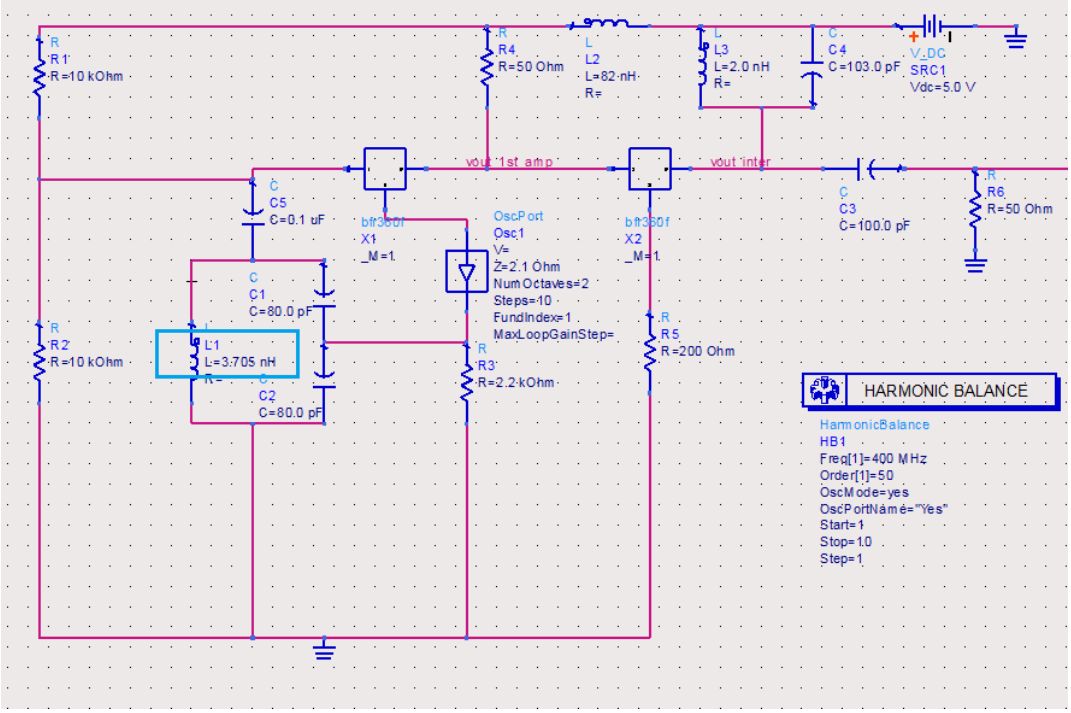


Fig 4.42: Inductance of 3.705 nH used in the oscillator tank circuit

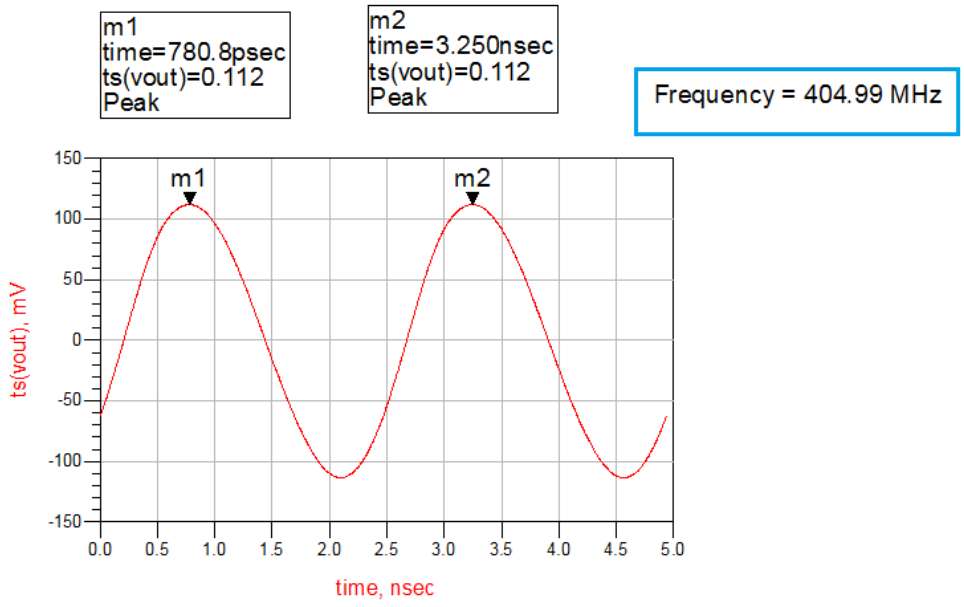


Fig 4.43: Frequency of oscillations using the 3.705 nH inductance

The capacitance of 80 pF used on the board also had tolerance values of ±5 % according to the data sheet obtained. Thus the capacitance can vary from 84 pF to 76 pF. This gives a frequency of 382.7 MHz and 400 MHz, respectively, as shown in figures 4.44 and 4.46.

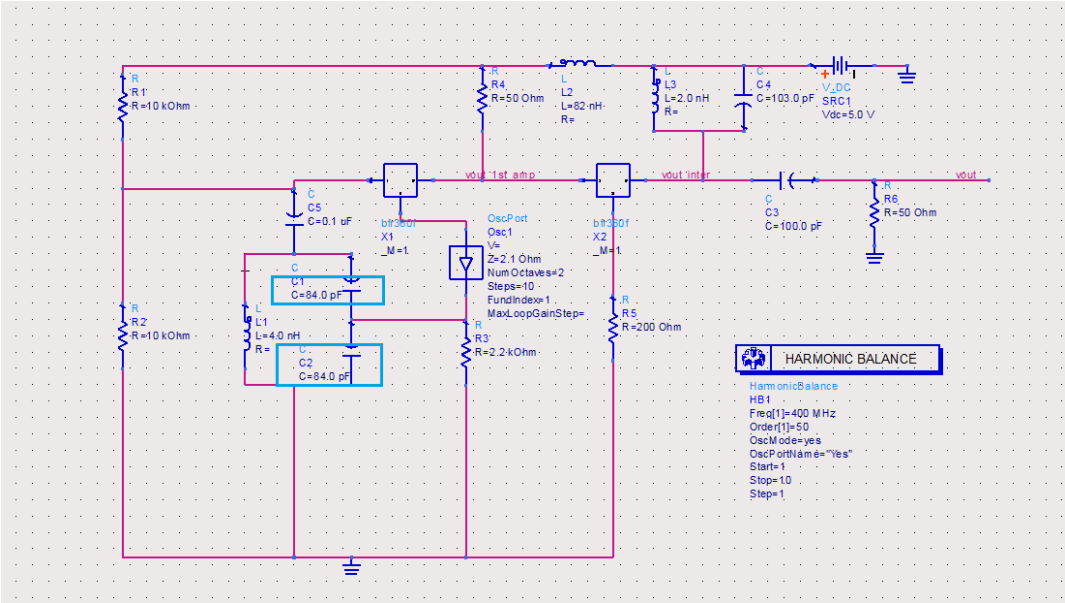


Fig 4.44: Capacitance of 84 pF used in the oscillator tank circuit

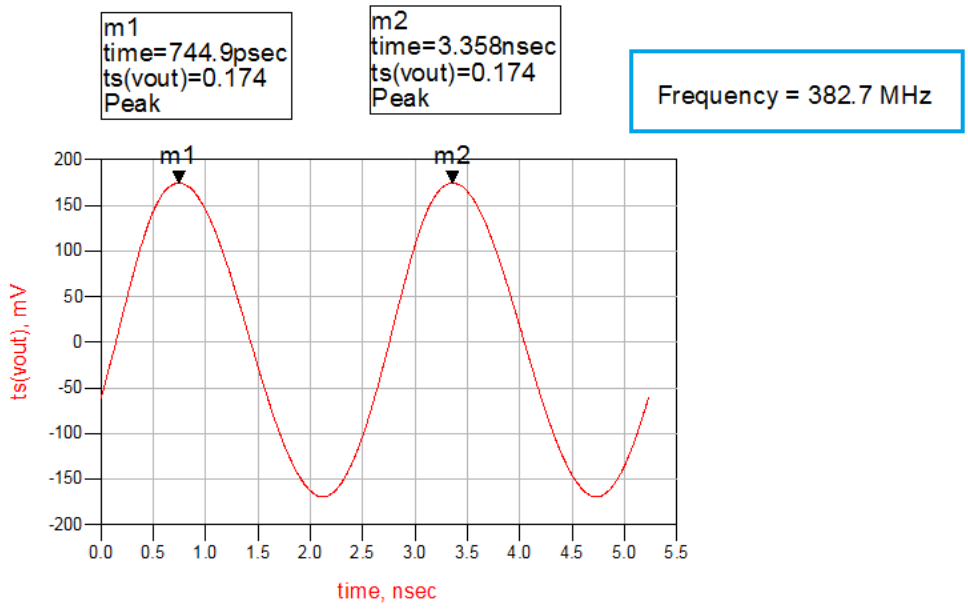


Fig 4.45: Frequency of oscillations using the 84 pF capacitance

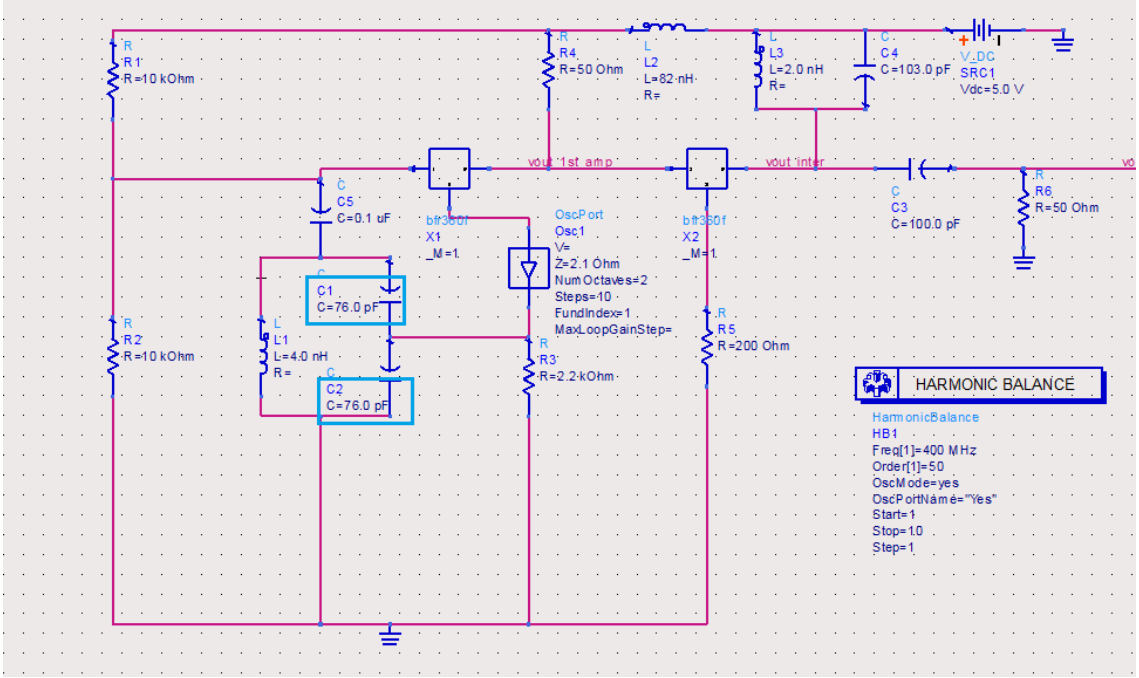


Fig 4.46: Capacitance of 76 pF used in the oscillator tank circuit

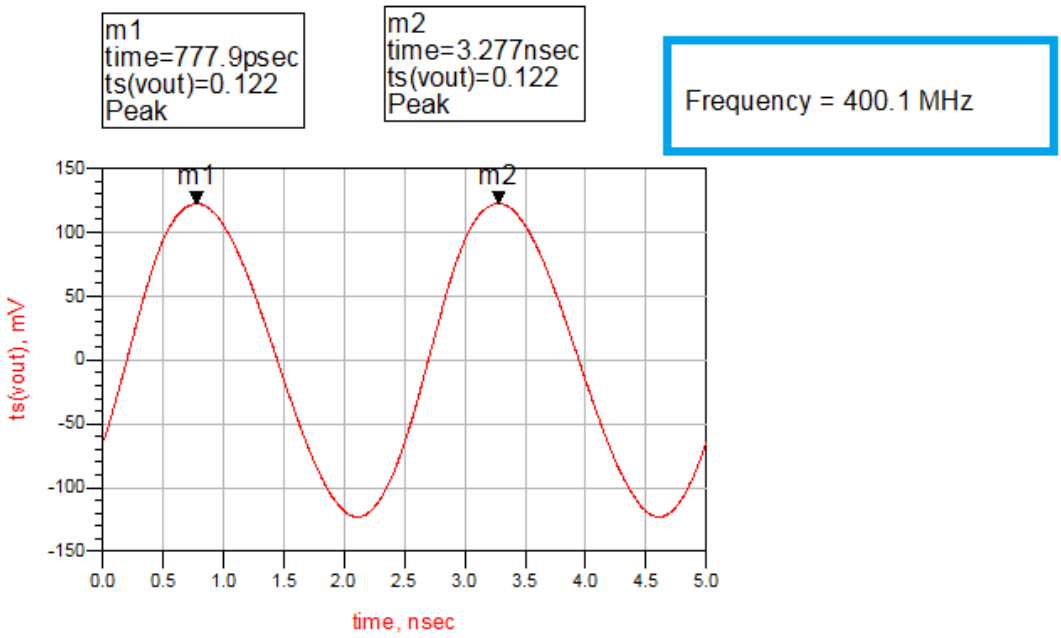


Fig 4.47: Frequency of oscillations using the 76 pF capacitance

CHAPTER 5

CONCLUSION

5.1 Conclusion and future work

The differential LC VCO designed here meets the specifications of linearity, phase noise and frequency of oscillations during simulation. As seen from figures 4.18, the center frequency is at 400 MHz for which the phase noise is at -120 dBc/Hz at 10 kHz offset. As proposed, the MOSFET varactors exhibit a linear behavior as seen from the graph of frequency versus tuning voltage curve in figure 4.11. Hence, this VCO finds applications in linear amplifiers and crystal oscillators.

When compared with the previous work of differential LC VCO, the printed circuit board level design of thesis work shows that the oscillations occur without any start-up issues and are highly linear. Layout area is optimized by the usage of less number of inductors. The frequency of oscillation occurs at 381.14 MHz on the PCB from an ideal value of 391 MHz on the simulations which represents about 2.55% variation. The voltage that triggers the oscillation is 6.5V compared to that of 5V of theoretical calculations. The current drawn by the circuit is 5 mA while the power consumed is 7 mW. The solder pads, the cable resistance, SMA connector resistance, component mismatch are some of the reasons for the variation in frequency and higher input voltage. This work is comparable to the printed circuit board level implementation of LC VCOs for applications such as ASK transmitters and sigma-delta modulators which are currently being studied [7] [8].

Future work can include choosing the exact value of the discrete components with better tolerances so that any frequency drift due to additional capacitance, resistance or inductance is avoided. Inclusion of a tunable capacitor or inductor can help the frequencies to shift to the desired frequency of oscillation taking into account the impact of layout. The usage

of integrated circuits in place of discrete components can minimize the frequency drift and voltage fluctuations due to minimal parasitics of the ICs. The coupled LC tanks along with the usage of SiGe BiCMOS technology can help achieve a larger tuning range of the VCOs and a better match between the theoretical and practical oscillation frequencies [32].

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BIOGRAPHICAL INFORMATION

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