MODELING AND CHARACTERIZATION OF THE INSULATED GATE BIPOLAR TRANSISTOR IN THE NEAR-THRESHOLD REGION

by

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Abstract

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The Insulated Gate Bipolar Transistor (IGBT) is a power semiconductor device widely used in high-speed switching applications. Due to aging and internal heating, the device is prone to a failure mechanism known as latch-up in which, changes in the threshold voltage and the on-state voltage of the device may ultimately lead to loss of switching control.

Since IGBTs are typically operated at high voltages and currents, the datasheets do not provide information on the static characteristics of the device for voltages close to the threshold, which is a useful region for understanding the underlying device physics.

In this thesis a simplified IGBT model is presented that attempts to provide a magnified view of the static characteristics close to the threshold voltage. The model is developed based on the device structure and is optimized to fit the measured characteristics in the near-threshold voltage range.

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Chapter 1

Introduction

The Insulated Gate Bipolar Transistor (IGBT) is a power semiconductor device that incorporates the structural elements and device physics of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and a Bipolar Junction Transistor (BJT) in a single monolithic structure. This gives it the dual advantage of low switching losses of the MOSFET and the high current capability of the BJT. The currently available IGBTs have current ratings of 1 to 1000 A, voltage ratings of 200 to 750 V, and frequency range of 60 Hz to 100 kHz [1].

IGBTs are the preferred choice in majority of the power electronic applications because they reliably provide efficient power delivery and energy management at a reduced cost and size. The prime areas in which IGBTs are extensively used are: high power switching applications like the electronic ignitions systems for vehicles, adjustable motor drives for electronic appliances like refrigerators and air-conditioners, inverters for hybrid and electric cars as well as traction systems of electric trains, control circuitry for industrial lighting purposes and robotics, and high voltage and switch mode power supplies [1, 2]. Given the extensive array of applications that IGBTs cover, device manufacturers use various fabrication methods to build robust structures that can withstand the high voltages and currents [2, 3].

1.1 Latch-Up

An important failure mechanism in the IGBT is latch-up. The device is latched when there is an upsurge of current well beyond the critical value specified by the Safe Operating Area (SOA) and the gate loses control of the device. The device current

becomes independent of gate voltage, and the output current characteristic curves for different gate voltages reduce to a single curve. This is manifested in the form of a reduction in the output resistance [2].

Latch-up can occur in either the static or dynamic mode. In the static mode, latch-up occurs during steady state operation. In this case, the output current is very high even if the output voltage is held at a low value. This type of latching is not localized, and it covers the entire active area of the device. In the dynamic mode, latch-up occurs during turn-off in AC applications when both the output current and output voltage are high. Typically, latching current density for the dynamic mode is less than that of static mode. Increase in temperature increases the current gain of the internal BJT causing the latching current density limit to decrease [2].

Device manufacturers provide latch-up immunity by adjusting the doping profiles of the device structure [2, 3]. While these methods do increase the current rating and the lifetime of the device, some measurable external indicators are required for identifying impending device failure.

1.2 Failure Precursors

Imminent device failure can be predicted by monitoring the deviation of certain electrical parameters, known as failure precursors, from their expected values in a given operating range. For the IGBT, two such failure modes recognized are device aging due to degradation in the electrical properties of the device structure and increased device temperature [3].

Device aging could result in increased leakage current or gate oxide breakdown, which would then result in loss of gate control leading to latch-up [4]. Also, an external

short-circuit could cause the device to get latched to high current conduction state, which would then increase the device temperature leading to burnout [2].

The threshold voltage is the gate voltage at which the IGBT starts conducting and a measurable output current is obtained. The on-state voltage is the output voltage beyond which the output current saturates. Since the IGBT is extensively used as a power switch, its turn-on mechanism involves having a gate voltage higher than the threshold and an output voltage higher than the on-state voltage. Based on the voltage mode of the application (i.e. either DC or AC), the IGBT can be turned-off either by dropping the gate voltage below the threshold value or by decreasing the output voltage below the on-state value [2, 4].

The threshold voltage and the on-state voltage are two such electrical parameters that can be used as failure precursors. Device aging and temperature increase have contrasting effects on these parameters. As the device ages, the threshold voltage increases while the on-state voltage decreases. In the case of rise in the operating device temperature, the threshold voltage is seen to decrease while the on-state voltage increases [4, 5]. Given that both these parameters show opposite effects, monitoring the device parameters that determine their value can give an indication of the failure mode due to which the device may fail.

1.3 Thesis Outline

In this thesis the static characteristics of the IGBT are modeled in the voltage range that is very close to the device threshold voltage. This is done to provide a magnified view of the device characteristics and the parameters affecting the threshold and the on-state voltage. Measurements in this region can be taken using ordinary laboratory power supplies without the need for expensive power network analyzers.

Modeling in this region provides insight on how the device begins conducting before it reaches its operating value. Any changes in the characteristics in this region will, thus, be indicative of changes occurring within the device due to aging or temperature increase.

In Chapter 2, the basic structure of IGBT along with its operating principle is discussed. The different types of structures commercially available and their uses are also described.

In Chapter 3, the different techniques of modeling a semiconductor device are presented following the requirements of what is considered to be a good model. The manufacturer's model of the IGBT sample used in this thesis is presented.

In Chapter 4, the experimental set-up used for taking measurements on the IGBT sample is explained. Based in the measurements obtained, a model is developed which will be used to fit the measured data points. The derivation of the model based on the observed regions of operation is discussed.

In Chapter 5, parameter extraction techniques performed on the measured data are described and an initial guess for the device parameters is made.

In Chapter 6, the optimization procedure of fitting the simulated curves to measured data points is elaborated. Both the extraction and optimization procedures are performed using the IC-CAP software provided by Agilent Technologies.

In Chapter 7, the optimized device parameters are compared with those used by the device manufacturer and a comparison is made with the results obtained using the manufacturer's model. Lastly conclusions are drawn from the observed results and refinements to the model in the form of future work are presented.

Chapter 2

IGBT Device Structures

2.1 Basic Device Structure

The IGBT is a hybrid of a an n-type enhancement MOSFET and pnp BJT connected in a pseudo-Darlington configuration [2]. The basic IGBT structure, as shown in Figure 2-1, is composed of several layers of p- and n-type silicon whose doping concentrations depend on the region they emulate.

The p+ substrate forms the emitter region of the BJT (BJT.E). The n- drift region doubles as the base region for the BJT (BJT.B) and the drain region of the MOSFET (MOS.D). The p body region forms the collector of the BJT (BJT.C) and acts as the body region for the MOSFET (MOS.B). The n+ region forms the source region for the MOSFET (MOS.S).

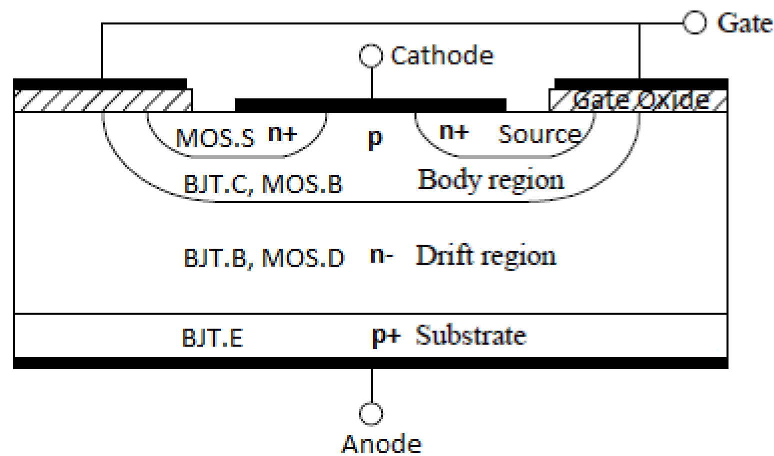

Figure 2-1: Basic IGBT Structure [6]

The drift region is relatively thick and is lightly doped to support high breakdown voltages while the device terminals are connected to the heavily doped regions [7]. A metal contact is used to short the source of the MOSFET and the collector of the BJT (or

body of the MOSFET) to form the external cathode (K), a polysilicon layer atop the oxide layer forms the gate contact (G) and a metal contact on the p+ substrate forms the anode (A). The simplified IGBT equivalent circuit and circuit symbol is shown in Figure 2-2.

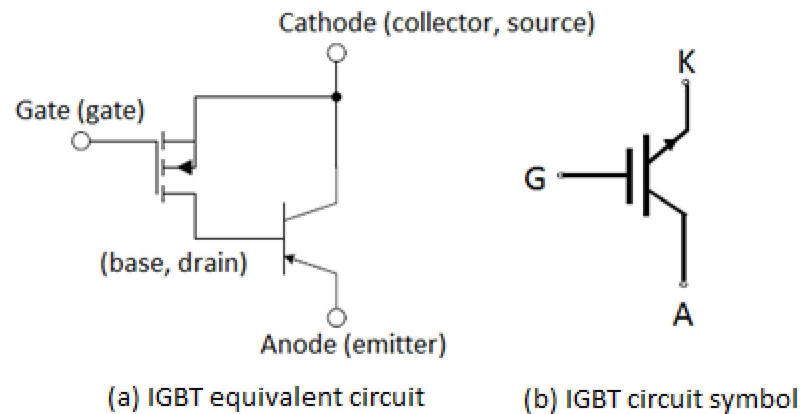

Figure 2-2: (a) IGBT simplified equivalent circuit [6, 8] and (b) IGBT symbol [9]

2.2 Operating Principle

2.2.1 Turn-on or Forward Conduction Mode

A positive voltage on the anode terminal of the IGBT forward-biases the emitter-base junction formed by the p+ substrate and n- drift region. This causes holes to be injected from the p+ emitter into the n- base region [9].

When a positive voltage is applied to the gate of the IGBT, electrons in the p-body region migrate towards the gate oxide. If the applied voltage is above the threshold value, an inversion layer is formed in the p- body, which acts as the channel between the n+ source and the n- drift region [6, 10].

Electrons can now flow from the source into the drift region and this forms the base current for the BJT. Since the IGBT has a large base width, significant recombination takes place in the drift region. Since the collector-base junction formed by

the p body and n- drift region is reverse-biased, the remaining holes are swept into the collector of the BJT [9].

The IGBT is considered an ambipolar device since current in the device is due to both electrons and holes. The injected holes (i.e. minority carriers in the drift region) modulate the conductivity of the drift (base) region and are, therefore, responsible for the reduction in the on-state voltage of the device at the anode terminal [6].

2.2.2 Turn-off Mode

By decreasing the gate voltage below the threshold, the electron flow from the source to drift region can be abruptly cut-off. However, due to the presence of holes in the drift region the IGBT does not stop conducting current from the anode to the cathode.

Removal of the holes is achieved either by sweeping them into the collector or through recombination with the electrons in the drift region, which are injected in the form of MOSFET drain current. The presence of this hole current in the IGBT is manifested in the form of a tail current seen during the turn-off period [6].

2.3 Types of Device Structures

From the operating principle it is seen that a trade-off exists between high current conduction, high breakdown voltage and fast switching (i.e. faster turn-off) requirements. Depending on the required breakdown voltage and switching speed, IGBTs are commonly classified into three types: Punch Through (PT), Non-Punch Through (NPT), and Field Stop (FS), as shown in Figure 2-3. The carrier profiles and electric field distribution vary in these structures and are optimized for the required application [2].

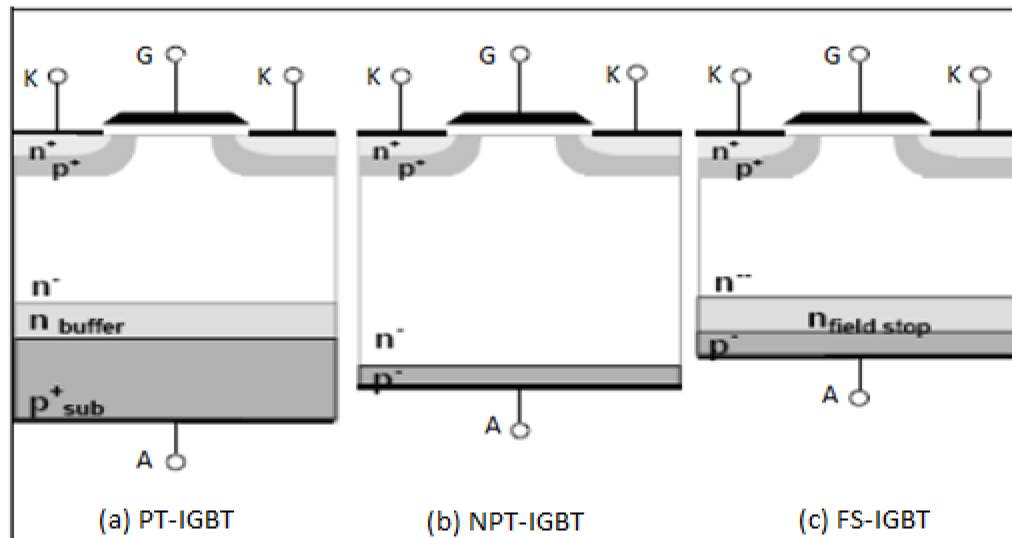

Figure 2-3: Types of IGBT structure [10]: (a) PT-IGBT, (b) NPT-IGBT and (c) FS-IGBT

The NPT structure is also referred to as a symmetric structure because it has the same value of forward and reverse breakdown voltage. Since the hole carrier distribution is uniform over the drift region, holes flow in this region due to the drift mechanism rather than diffusion. The electric field distribution over the large base width makes the structure rugged and therefore well-suited for AC applications where the device must support large voltages in both directions [2].

The PT and FS IGBTs, also known as asymmetric IGBTs, have a n-type buffer layer that performs two functions. Firstly, it provides electrons for recombination with the holes. This reduces the turn-off time of the device, which results in faster switching. Secondly, it reduces the width of the n- drift region which leads to a reduction in the breakdown voltage that can be supported by the device. This makes asymmetric IGBTs suitable for DC applications wherein the device is not required to have a large reverse breakdown voltage since it is assumed that current will flow only in the forward direction [2, 6].

Another classification can be made based on the location of the gate. The gate can be fabricated on top of the device to form a horizontal MOSFET underneath the oxide or it can be “trenched” into the p body to form a vertical MOSFET. These are called planar gate and trench gate IGBTs respectively and are shown in Figure 2-4.

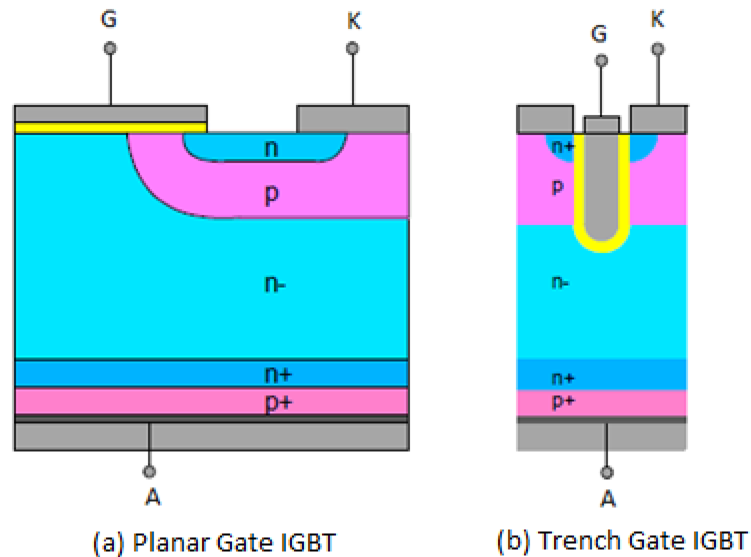

Figure 2-4: IGBT classification based on gate structure [10]: (a) Planar Gate IGBT and (b) Trench Gate IGBT

The trench gate IGBT provides the advantage of reducing the on-state voltage of the device without sacrificing the breakdown voltage. This is achieved through the formation of an accumulation layer along the sides of the trenches, which connects the n+ source to the n- drain region. This improves conduction by decreasing the channel resistance of the MOSFET and thus improving electron injection in the drift region. Also, it improves the cell density by reducing the active area needed to achieve the same breakdown voltage as compared to the planar gate [2, 13].

Chapter 3

IGBT Modeling Techniques

3.1 Device Model Requirements

Device models for power semiconductors are designed based on their required purpose and can be roughly categorized as [9, 14]:

1) Models for studying device-circuit interactions: These are preferred device models supplied simulator vendors or power semiconductor device manufacturers for giving an accurate picture of how the device would behave as part of a circuit under loading conditions.
2) Models for understanding the internal device physics: These device models are sufficiently simple to perform parameter extraction but are not very accurate because they treat the device as stand-alone entities. In other words, while they give a reasonable picture of how the device behaves on its own, they may not be suitable modeling the device as part of a circuit.

For an IGBT, there is no compact model available that allows for the study of its internal conduction mechanism. The parameterized IGBT models available from commercial model libraries represent averaged characteristics without provision to adjust parameters specific to a particular device [15]. Also, the commercially available models contain parameters that may not be pertinent to the set-up in which the device is used. Since the datasheet provides information on electrical characteristics only for the operating range, it is difficult to extrapolate the manufacturer’s model to specific voltage ranges of interest.

In [14] and [15] the requirements for a basic IGBT model that provides sufficient accuracy and availability along with simple parameter extraction techniques are enumerated as follows:

1) Extractable from Electrical Measurements:

   For best accuracy, all parameters must be extractable from the following three experimental set-ups:

   i) DC characteristics
   ii) Gate-charge plot
   iii) Inductive load switching or zero-voltage switching.

2) Extractable from Datasheet Information:

   For every model, an additional parameter extraction method should be provided using data sheet information only.

3) Good Static Performance:

   The model should provide reasonably accurate dc characteristics for high and low voltages.

4) Good Dynamic Performance:

   The inductive load switching set-up should include high and low voltage effects along with the variation in tail current at different clamp voltages.

5) Available in Public Domain:

   The model must be accessible in public domain so that it is available for implementation on a variety of circuit simulators.

3.2 Model Types

While the basic purpose of any device model is to provide reasonably accurate simulation of device characteristics, there are several approaches that can be taken to developing a model:

1) Behavioral Models:

Also, known as functional or empirical models, this category does not include the internal device physics of the IGBT but views it as a “black-box” wherein the external characteristics are described with curve-fitting algorithms or look-up tables. This approach is useful when only the effect of the device as part of a larger circuit needs to be observed.

While the DC characteristics may be modeled accurately enough, the transient behavior is difficult to model using this approach due to the interactions of other circuit elements during switching [9].

2) Semi-Mathematical Models:

In this category, part of the model is based on physics while part of the model is built using existing circuit models. The “lumped-charged” model is an example of this type. Here, the internal BJT is modeled with physics-based equations while empirical equations are used for the internal MOSFET [15]. These models are not as accurate as the mathematical models since none of the existing BJT models can compare to the wide-base internal BJT of the IGBT. But the advantage of this type of modeling is that it can be implemented on a variety of circuit simulators. However, this has been done only for the PT-IGBTs for low voltage applications while the NPT-IGBTs await validation [14, 15].

3) Mathematical Models:

This category of models is based on the semiconductor device physics and it tries to analytically solve the device equations. Model complexity depends on how well the device equations can emulate the internal physics and how many features of the IGBT are considered. The Hefner model implemented

in SPICE and SABER simulators is one such example and is the most widely used IGBT model [9].

However, the disadvantage is that solving these equations in one, two or three dimensions, requires complex and time-consuming computations. Also, to construct such models propriety information regarding the doping profile, internal device structural properties, carrier lifetimes, etc. is required, which makes it feasible only to device manufacturers [2].

4) Semi-Numerical Models:

   In this category, the wide base of the IGBT is discretized into a finite number of elements. Another approach is to describe the derivatives in the diffusion and transport equations using finite differences while other device parts are described analytically. These models yield the most accurate results but at the cost of high computing speed and implementation in complex circuit simulators [9].

5) Macro Models:

   In this approach, a macro model of the IGBT is built using discrete devices. These discrete devices are then described in terms of model parameters that will fit the observed IGBT characteristics. The advantage of this method is that it helps in understanding the physical behavior of the device in terms of minimum model parameters and in the desired voltage region.

3.3 Manufacturer's Model

In this thesis, the STGB10NB60ST4 IGBT obtained from STMicroelectronics was measured and modeled. A model file was available for this sample which was analyzed in

PSpice A/D. The sub-circuit given in the model file was constructed using PSpice Schematics and is shown in Figure 3-1.

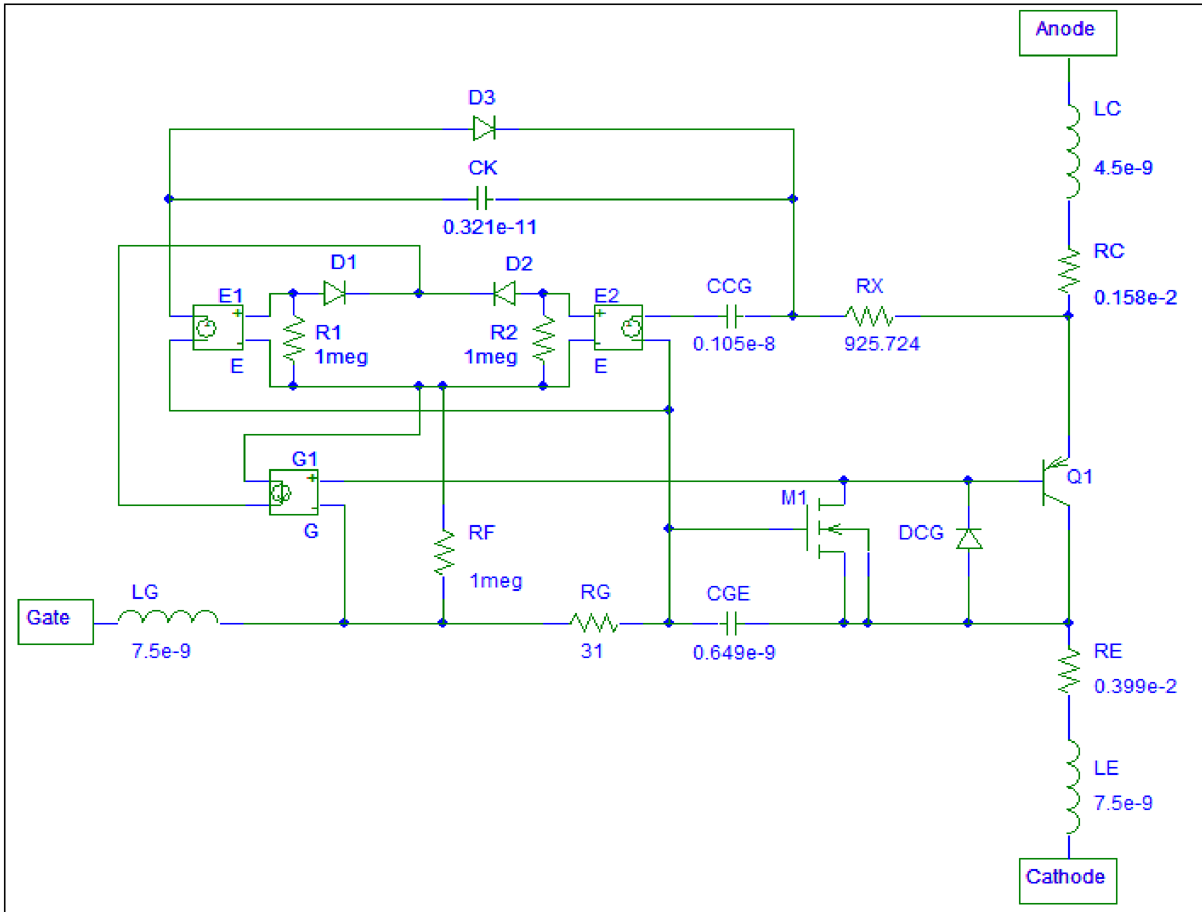

Figure 3-1: PSpice Schematic of Manufacturer's IGBT Model

The sub-circuit follows the analytical modeling method and is made up of discrete devices with model parameters supplied by the manufacturer.

This sub-circuit is more suited for modeling the dynamic characteristics of the IGBT given the placement of capacitors and diodes. If only static simulation needs to be observed, the sub-circuit can be simplified by eliminating all branches containing capacitors because capacitors are considered open-circuit in DC analysis.

Also, the controlled sources to which the reverse-biased diode D3 connects can be eliminated along for DC calculations because they are used for modeling the transit time of charge carriers under switching conditions. The inductors and resistors connected to the terminals can be removed for the same reason since they represent the parasitic elements.

Diode DCG models the high voltage reverse breakdown and, therefore, in the case of low voltage measurements, it can be eliminated. Thus, to model only the static characteristics at low voltages, only the BJT and MOSFET are the necessary circuit elements.

The description of the model parameters [16] used by the manufacturer for defining the BJT and MOSFET models is shown in Tables 3-1 and 3-2 respectively. The focus of the model parameters included by the manufacturer for defining the MOSFET and BJT devices is on modeling the high current characteristics and the transit time which are not necessary for current purposes. Therefore, in the following chapter simplified model using only those parameters of the MOSFET and BJT which are important for simulating the low current and low voltage characteristics is developed.

Table 3-1: List of BJT model parameters for manufacturer's model

Model Parameters	Description	Value
IS	Saturation current	24.5E-15 A
ISE	Base-emitter leakage saturation current	141E-18 A
NE	Base-emitter leakage emission co-efficient	1.974
NC	Base-collector leakage emission co-efficient	2.714
BF	Ideal maximum forward current gain	0.864
VAF	Forward Early voltage	894.9 V
IKF	Forward beta high current roll-off	8.034 A
NK	Forward beta roll-off slope exponent	0.887
BR	Ideal reverse maximum current gain	0.00389
TF	Ideal forward transit time	1E-06 s
ITF	High current parameter for effect on TF	1 A
VTF	Voltage describing V_{BC} dependence on TF	10 V
XTF	Co-efficient for bias dependence of TF	0.1

Table 3-2: List of MOSFET model parameters for manufacturer's model

Model Parameters	Description	Value
VTO	Zero-bias threshold voltage	3.418 V
KP	Transconductance parameter	2.512 A/V^2
THETA	Mobility modulation	0.0986 /V

The static characteristics in the form of the output and transfer characteristics for the manufacturer's sub-circuit based on the voltage ranges used in the device datasheet are shown in Figures 3-2 and 3-3 respectively. The same results were obtained when only the MOSFET and BJT were used in the sub-circuit.

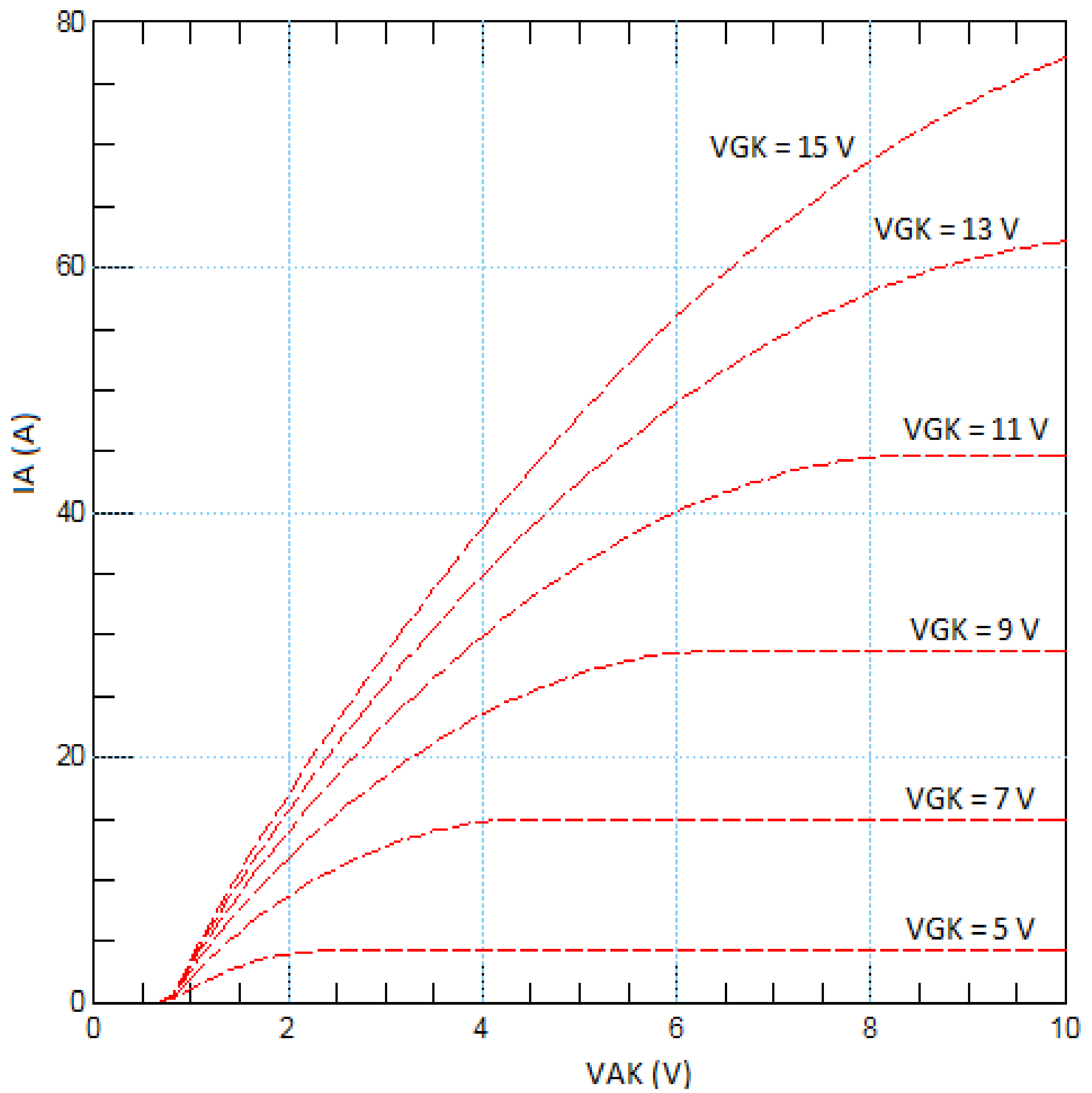

Figure 3-2: Output characteristics using manufacturer's model

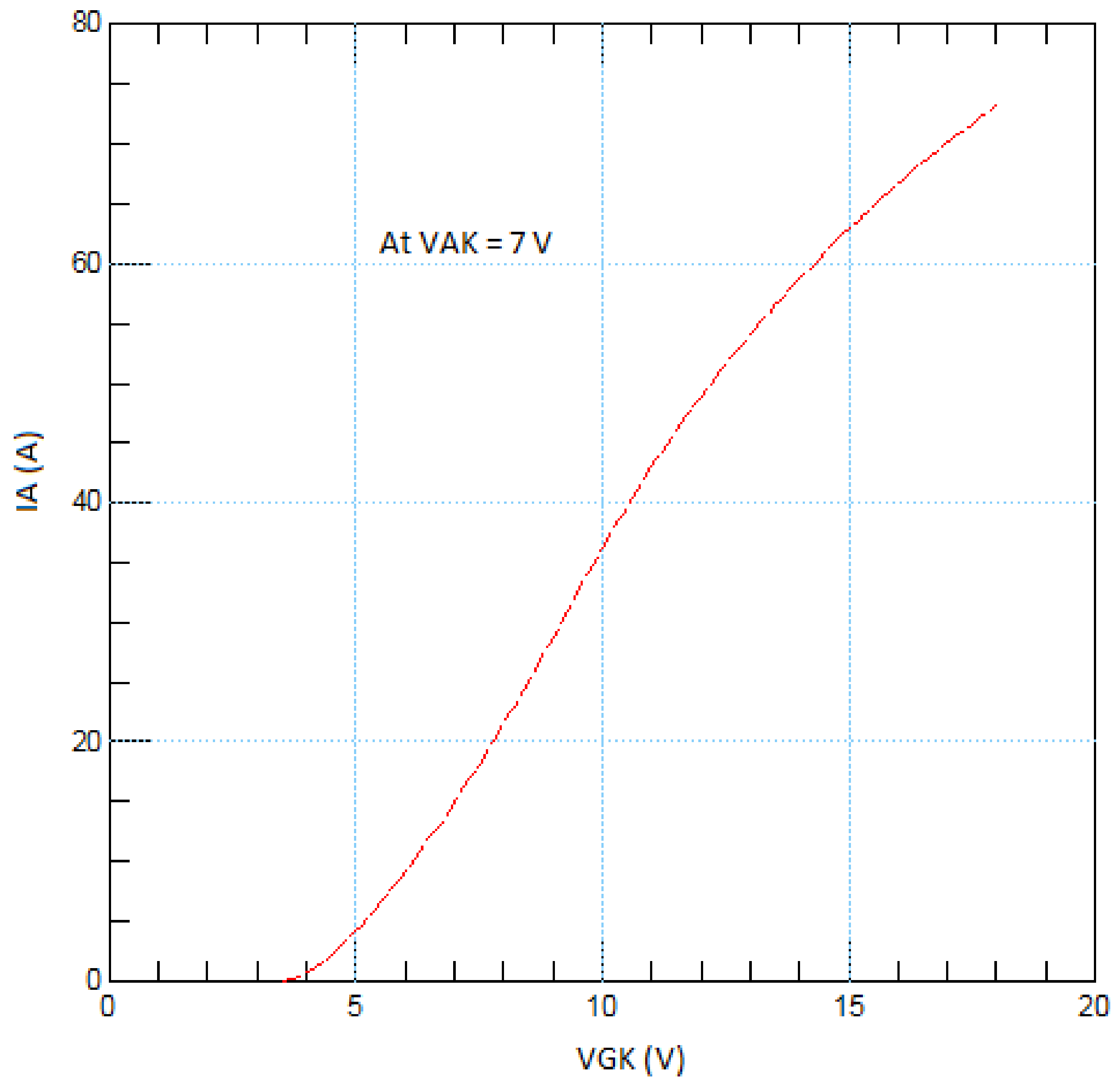

Figure 3-3: Transfer characteristics using manufacturer’s model

Chapter 4

IGBT Model Development

In this thesis a simple Darlington-like connection between a MOSFET and BJT is used to develop an analytical model for the IGBT based on the observed behavior of the device in the near-threshold voltage range. The static characteristic curves are obtained using the set-ups described in the next section.

4.1 Experimental Set-Up

The two sets of static characteristics are obtained for the IGBT using the following set-ups:

1) Transfer Characteristics:

   A voltage source, V_{GK}, connected between the gate and cathode of the IGBT is swept from 3.5 V to 4.8 V. The anode current, I_A, is measured versus V_{GK} while the anode voltage, V_{AK}, is held constant at 3 V.

2) Output Characteristics:

   A voltage source, V_{AK}, is connected between the anode and cathode of the IGBT and is swept from 0.1 V to 3V. Another voltage source (V_{GK}) is connected between the gate and cathode of the IGBT to perform a secondary sweep from 4.5 V to 4.8 V. The anode current, I_A, is measured versus V_{AK} for different values of V_{GK}.

The measured values are imported in the IC-CAP software under the respective set-ups. These set-ups are simulated for the same voltage range to obtained simulated values which are then directly compared with the measured values to see how well the

proposed model fit the characteristics. The measured data obtained for the above mentioned set-ups are included at the end of the chapter.

4.2 Model Parameters

The list of SPICE model parameters [16] used to describe the observed characteristics of the in terms of current equations for the MOSFET and BJT are defined in Table 4-1. These parameters will be referenced in the equations that will describe the observed regions of operations. The initial values, extraction procedure and optimization of these parameters are explained in Chapter 5.

Table 4-1: List of BJT and MOSFET model parameters

SPICE Model Parameter (BJT)	Description (BJT)
IS	Saturation current
NF	Forward current emission co-efficient
ISE	Base-emitter leakage saturation current
NE	Base-emitter leakage emission co-efficient
BF	Ideal maximum forward current gain
VAF	Forward Early voltage
SPICE Model Parameter (MOSFET)	Description (MOSFET)
VTO	Zero-bias threshold voltage
KP	Transconductance parameter
NFS	Surface-fast state density

4.3 Circuit Analysis

It is observed that given the aforementioned values of terminal voltages, the BJT is always in the forward active conduction mode. This means that the collector-base junction of the BJT is reverse-biased and the emitter-base junction is forward biased. The region of operation for MOSFET varies with the terminal voltages and is discussed in depth in the following sections. The experimental-setup along with the macro model and the directions of current flow and voltage notations are included in Figure 4-1.

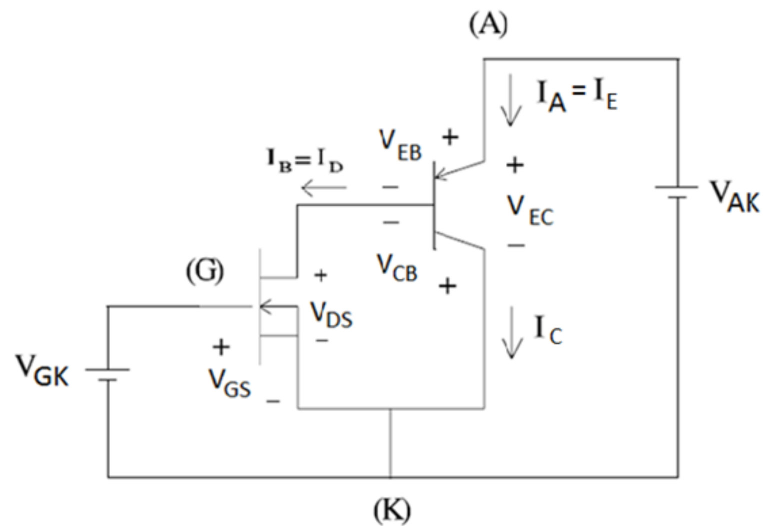

Figure 4-1: IGBT Macro-Model [17] and Experimental Set-Up

The voltage equations for the sub-circuit based on Kirchhoff's voltage law are given by equations (4.1) to (4.4).

$$V_{GK} = V_{GS} \tag{4.1}$$

$$V_{DS} = -V_{CB} \tag{4.2}$$

$$V_{AK} = V_{EC} \tag{4.3}$$

$$V_{AK} = V_{EB} + V_{DS} \tag{4.4}$$

Likewise, the current equations for the circuit based on Kirchhoff's current law are given equations (4.5) to (4.7).

$$I_A = I_E \tag{4.5}$$

$$I_E = I_B + I_C \tag{4.6}$$

$$I_B = I_D \tag{4.7}$$

4.4 Observed Regions of Operation

In the following equations, all voltages and currents are defined with subscripts and all SPICE model parameters are denoted in uppercase. The thermal voltage is defined as

$$V_T = \frac{q}{kT}$$

where q is the electron charge, k is the Boltzmann's constant and T is the Kelvin temperature. SPICE has a default value of $T = 300\ K$ due to which $V_T \cong 0.026\ V$. Since the body of the MOSFET is tied to ground $V_{BS} = 0\ V$ and so $V_{TH} = VTO$. Thus, the saturation condition for MOSFET defined as $V_{DS} \geq V_{GS} - V_{TH}$ becomes $V_{DS} \geq V_{GK} - VTO$.

4.4.1 Output Characteristics

4.4.1.1 Diode Region

This region of analysis is for the voltage range $V_{AK} \leq 0.5\ V$. This corresponds to the forward biased characteristics of the BJT base-emitter junction and the near-cutoff condition for the MOSFET.

Since V_{EB} cannot be measured directly for the IGBT, a separate set-up consisting only of simulated values was created in IC-CAP. In this set-up, the base of the BJT was taken to be an external terminal and the voltage at this terminal was measured when input of $I_B = 0\ A$ was applied to it in addition to the voltages applied in the output characteristics set-up. From these simulations it is observed that in this region $V_{CB} < \frac{V_{EB}}{100}$, so that $V_{EB} \cong V_{AK}$. This effect can be seen in the graph shown in Figure 4-2, which plots V_{EB} and V_{CB} as a function of V_{AK}.

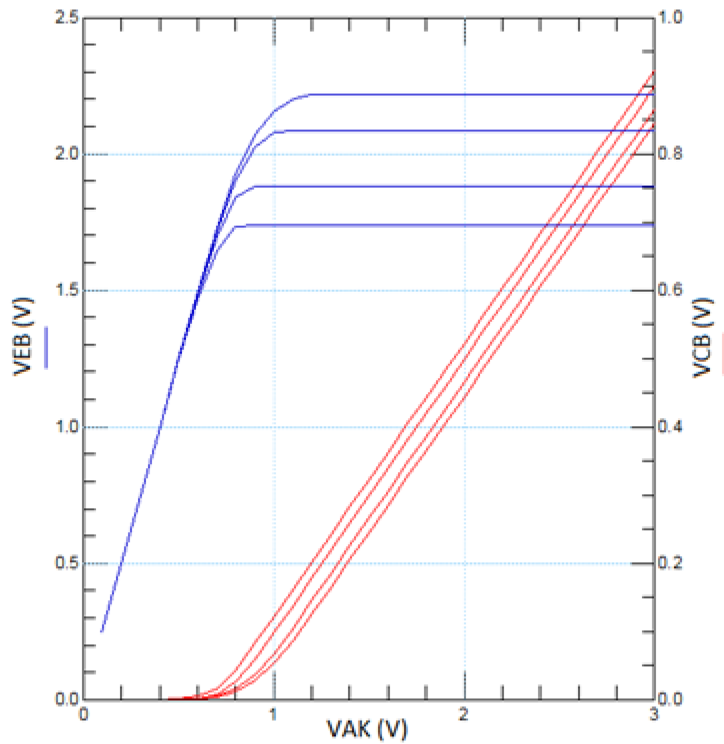

Figure 4-2: BJT voltages in the diode region

Also, since $-V_{CB} = V_{Ds} \cong 0$, $V_{DS} \ll V_{GK} - VTO$ for all values of V_{GK} and, therefore, it is assumed that $I_D = I_B \cong 0\ A$. This explains why the output current is almost independent of V_{GK}.

According to [17], the Gummel-Poon equation for the BJT in forward active mode for the collector current is given by equation (4.7) and that for the base current is given by equation (4.8).

$$I_C = IS\left(\exp\left(\frac{V_{EB}}{NF\,V_T}\right) - \exp\left(\frac{V_{CB}}{V_T}\right)\right) - \frac{IS}{BR}\left(\exp\left(\frac{V_{CB}}{V_T}\right) - 1\right) - ISC\left(\exp\left(\frac{V_{CB}}{NC\,V_T}\right) - 1\right) \tag{4.7}$$

$$I_B = \frac{IS}{BF}\left(\exp\left(\frac{V_{EB}}{NF\,V_T}\right) - 1\right) + ISE\left(\exp\left(\frac{V_{EB}}{NE\,V_T}\right) - 1\right) + \frac{IS}{BR}\left(\exp\left(\frac{V_{CB}}{V_T}\right) - 1\right) + ISC\left(\exp\left(\frac{V_{CB}}{NC\,V_T}\right) - 1\right) \tag{4.8}$$

where BR is the ideal maximum reverse current gain of the BJT, ISC is the base-collector leakage saturation current and NC is the base-collector emission co-efficient.

Assuming that V_{CB} = 0 V and I_B = 0 A, the emitter current defined by equation (4.6), which is also the anode current as defined equation (4.5) is then given in terms of model parameters as shown in equation (4.9).

$$I_A = I_E = I_C + 0 = IS\left(\exp\left(\frac{V_{EB}}{NF\,V_T}\right) - 1\right) \tag{4.9}$$

where $V_{EB} \cong V_{AK}$.

This is the current equation which governs the output current characteristics of the IGBT when the anode voltage is less than one diode drop. The IGBT output current will follow this exponential characteristic irrespective if the gate voltage is above the threshold voltage or not. Thus, while the literature suggests that the IGBT follows the turn-on characteristics of the MOSFET [2], it is not entirely true if the anode voltage is less than the emitter-base diode voltage.

4.4.1.2 Linear Region

This region of analysis is for the voltage range $V_{AK} < V_{AK(on)}$ where $V_{AK(on)}$ is the on-state voltage of the IGBT given by $V_{AK(on)} = V_{EB} + V_{DS(sat)} = V_{EB} + V_{GK} - VTO$.

In this region, the MOSFET is in the linear region, since $V_{DS} < V_{GK} - VTO$. The drain current of the MOSFET starts injecting electrons in the drift region thereby increasing the background doping concentration. This causes the holes injected by the emitter-base current to recombine with the electrons in the base region. Now I_A begins to show dependence on V_{GK} but since $V_{DS} < V_{EB}$ the BJT characteristics are still dominant in the output current characteristics.

Since V_{CB} is still less than V_{EB}, its effect as shown in the current equations (4.7) and (4.8) is ignored. Therefore, the anode current in this region as defined by the circuit equations (4.5) and (4.6) is given in terms of the model parameters in equation (4.10).

$$I_A = \left(1 + \frac{1}{BF}\right) IS\left(\exp\left(\frac{V_{EB}}{NF\,V_T}\right) - 1\right) + ISE\left(\exp\left(\frac{V_{EB}}{NE\,V_T}\right) - 1\right) \quad (4.10)$$

Here the base recombination effect plays an important role in determining the anode current which in turn determines the value for $V_{AK(on)}$ based on the gate voltage. In terms of device physics, if more recombination takes place in this voltage range, fewer holes reach the collector region which means that the output current takes longer to saturate and this causes the on-state voltage value to increase. In other words, the anode current of the IGBT will not saturate if the MOSFET remains in the linear region.

4.4.1.3 Saturation Region

In this region of analysis, $V_{AK} > V_{AK(on)}$ i.e. $V_{AK} > V_{EB} + V_{GK} - VTO$. This corresponds to the saturation region for the MOSFET since $V_{DS} > V_{GK} - VTO$.

The output characteristics are similar to those of the MOSFET [17] with the added effect of the current gain of the BJT. The anode current is, therefore, defined according to equation (4.5), (4.6) and (4.7) as

$$\mathrm{I_A = I_E = I_C + I_B = (1 + BF)I_B = (1 + BF)I_D}$$

and in terms of model parameters it is defined as given by equation (4.11)

$$\mathrm{I_A = (1 + BF)\frac{KP}{2}(V_{GK} - VTO)^2} \quad (4.11)$$

4.4.2 Transfer Characteristics

4.4.2.1 Sub-Threshold Region

In this region of analysis, $\mathrm{V_{GK} < VTO}$ but $\mathrm{V_{DS} > V_{GK} - VTO}$. Here the MOSFET is in weak inversion and the anode current shows exponential characteristics [17] given by equation (4.12)

$$\mathrm{I_A = (1 + BF)I_D = (1 + BF)I_{on}\exp\left(\frac{V_{GK} - V_{on}}{n\,V_T}\right)} \quad (4.12)$$

where $I_{on} = I_D$ when $V_{GK} = V_{on}$,

$V_{on} = VTO + n\ V_T$ = the boundary voltage between regions of weak and strong inversion. Noting again that $\mathrm{V_{BS} = 0\ V}$, [17] gives

$$\mathrm{n = 1 + \frac{q\,NFS}{C'_{ox}}} \quad (4.13)$$

C'_{OX} = oxide capacitance per unit area.

It should be noted that this exponential characteristic is not the same as the one seen in the diode region. The current in this region is independent of the voltage at the anode. In the sub-threshold region MOSFET current is low because the gate voltage is less than the threshold voltage i.e. V_{GK} < VTO, whereas in the diode region the drain

current is low because the drain voltage is less than the difference of the gate and threshold voltage i.e. $\mathrm{V_{DS}} < \mathrm{V_{GK}} - \mathrm{VTO}$.

<u>4.4.2.2 Saturation Region</u>

In this region, $\mathrm{V_{GK}} > \mathrm{VTO}$ and $\mathrm{V_{DS}} > \mathrm{V_{GK}} - \mathrm{VTO}$. The anode current equation is the same as that given by equation (4.11) for the saturation region in the output characteristics.

The graph showing the measured values of the output and transfer static characteristics of the IGBT is shown in Figure 4-3. The different regions of operation described in the above sections are also illustrated.

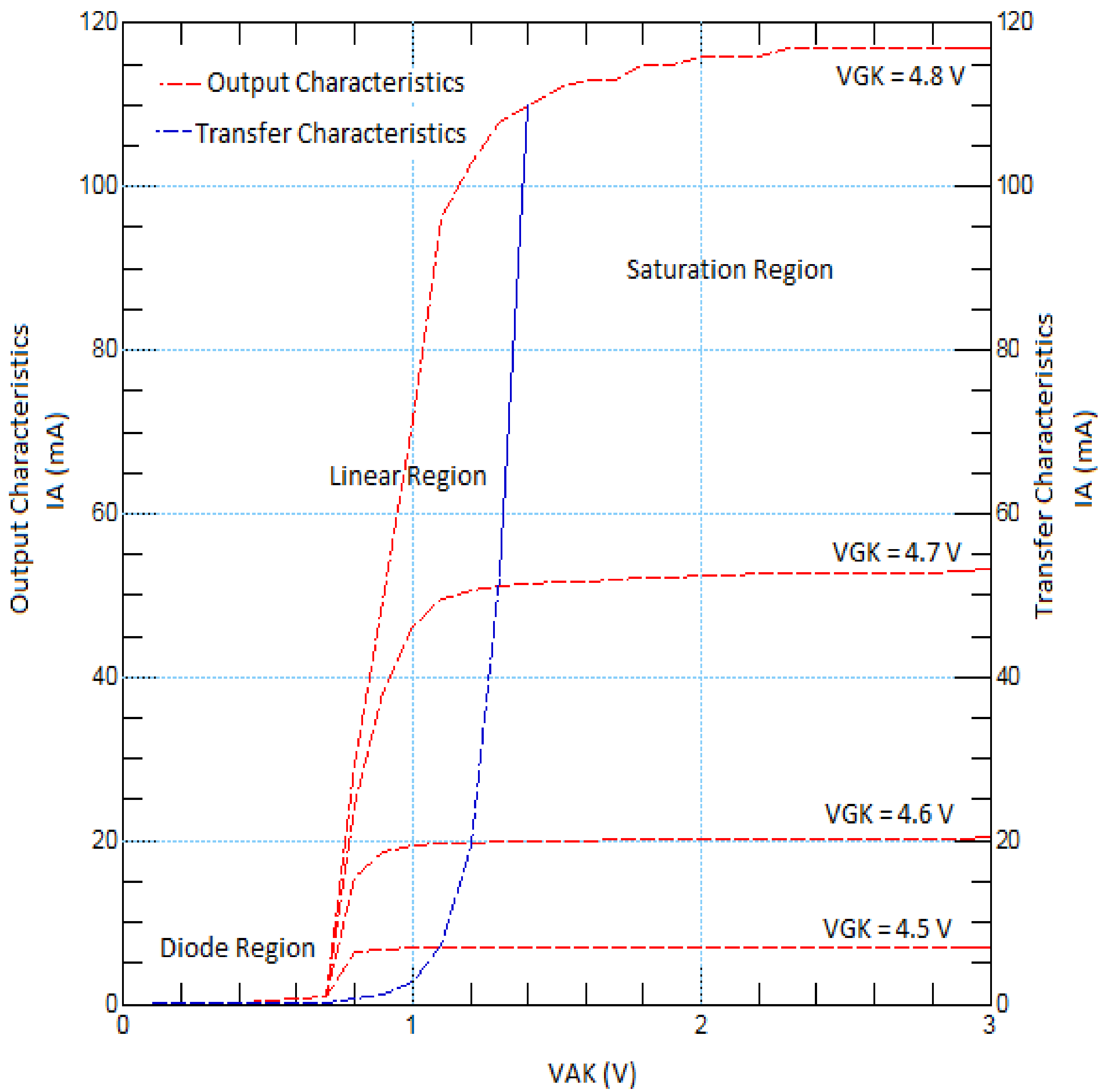

Figure 4-3: Regions of operation with respect to measured static characteristics

Chapter 5

Parameter Extraction

5.1 Parameter Extraction Procedure

In order to build a model that will fit the measured characteristics of the IGBT, a set of device parameters based on the device equations were defined. Since the IGBT is a composite structure of a MOSFET and a BJT, the typical SPICE parameter values of neither device will fit the observed characteristics. To fit the measured characteristics with the simulated model, a parameter extraction and optimization outlined below is carried out. Although the model parameters affect both, the output and transfer characteristics, extraction is carried in the regions of operation where their effect is most prominent. This is done using the equations that describe the observed characteristics.

The parameter extraction process is carried out as follows:

1) Parameters are initially estimated from observed measured values of the device under test (DUT).
2) Using these parameters a circuit simulation is carried out in IC-CAP using the similar experimental set-ups in which measurements are taken.
3) A comparison of the measured and simulated data points gives an error value.
4) The extracted parameters are varied to minimize the error value. This process is called optimization and is carried out until the parameters converge to give minimum error.

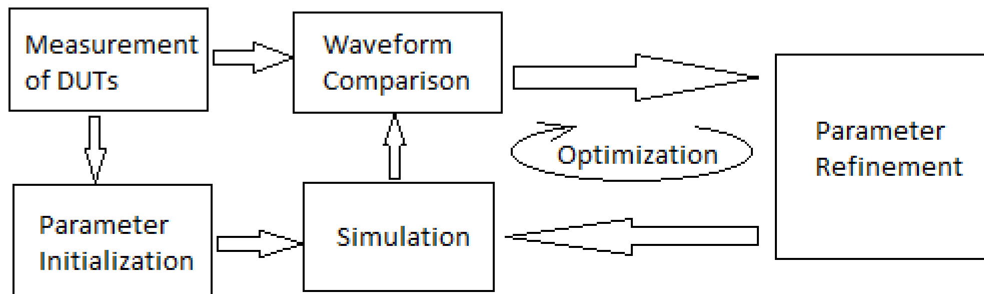

Figure 5-1: Parameter extraction and optimization procedure block diagram [18]

In the all the extraction procedures that follow, the term "log" refers to the natural logarithm denoted as "ln".

5.2 Parameter Extraction from Transfer Characteristics

5.2.1 VTO and KP Extraction

The threshold voltage of the device is the first parameter that is extracted from the transfer characteristics curve. Although the measurements give a rough estimation, it is not possible to distinguish the region of weak inversion from strong inversion for the MOSFET from only the measurements.

The threshold voltage and the transconductance parameter are extracted using the equation (4.11) of the anode current in the saturation region.

To simplify the equation, it is assumed that BF = 1 since the drift region i.e. the base region of the BJT is very wide, approximately of the order of 100 μm. Also, since measurements are taken at such low voltages, BF is governed by the low-current region characteristics of the BJT as given in [17].

Therefore, the equation in terms of the model parameters used for the extraction of VTO and KP is given by equation (5.1)

$$I_A = KP(V_{GK} - VTO)^2 \qquad (5.1)$$

Therefore,

$$\sqrt{I_A} = \sqrt{KP}\,(V_{GK} - VTO) \tag{5.2}$$

Using equation (5.2) a linear curve-fitting for the plot shown in Figure 5-2 is done which will give the values for VTO and KP as defined by equations (5.3) and (5.4) respectively.

$$VTO = X - \text{intercept} = \frac{Y\text{–intercept}}{\text{Slope}_{KP}} \tag{5.3}$$

$$KP = (\text{Slope}_{KP})^2 \text{ where } \text{Slope}_{KP} = \frac{d(\sqrt{I_a})}{d(V_{GK})} \tag{5.4}$$

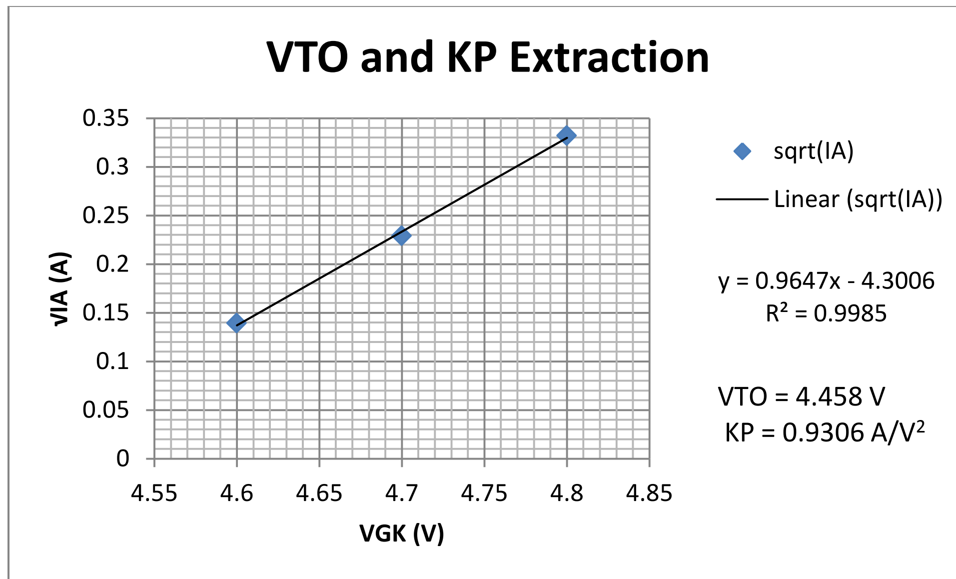

Figure 5-2: Linear curve-fitting for VTO and KP parameter extraction

5.2.2 NFS Extraction

NFS is a model parameter defined as the number of fast superficial states which characterizes the exponential dependence of the current in weak inversion. It determines the slope of the $\ln(I_A)$ v/s V_{GK} curve in the sub-threshold region [17] and is dependent on the value of the oxide capacitance per unit area.

The oxide capacitance, C_{OX}, is that value of Miller capacitance shown in Figure 5-3 when the depletion region under the gate is not formed i.e. the value of the depletion capacitance, C_{dep} is zero. In this case the oxide capacitance value is the maximum value of the reverse transfer capacitance, $C_{res,}$ specified in the datasheet [19].

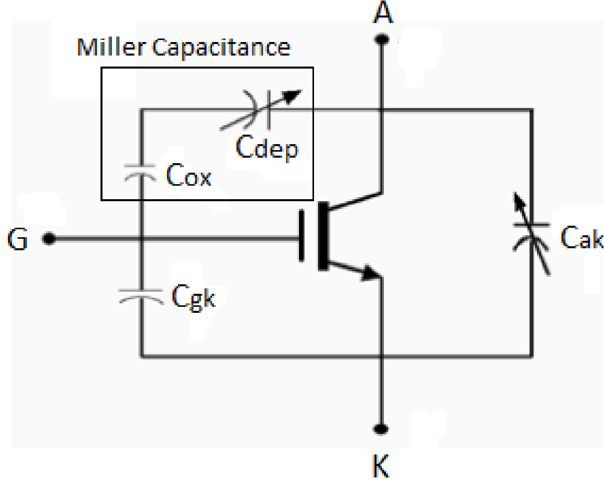

Figure5-3: IGBT capacitances [19]

For the IGBT used in this thesis, the value is found to be C_{OX} = 500 pF. Although the gate area of the device is not known, according to [20], the active area (A) for the device is 0.12 cm^2. Thus, the minimum value for $C'_{OX} = \frac{C_{OX}}{A} = 4.166\ \mathrm{nF/cm^2}$.

Taking the log of the sub-threshold current equation (4.12) and assuming BF = 1, equation (5.5) is obtained.

$$\ln\left(\frac{I_A}{2}\right) = \ln(I_{on}) + \frac{V_{GK}-V_{on}}{n\,V_T} \quad (5.5)$$

Differentiating both sides of equation (5.5) with respect to V_{GK},

$$\mathrm{Slope}_{NFS} = \frac{d\left(\ln\left({}^{I_A}/_2\right)\right)}{d(V_{GK})} = \frac{1}{n\,V_T}$$

and solving for NFS using equation (4.13), the following equation is obtained

$$\text{NFS} = \left(\frac{1}{\text{Slope}_{\text{NFS}}\,\text{V}_\text{T}} - 1\right)\frac{\text{C}'_{\text{ox}}}{q} \tag{5.6}$$

The plot for $\ln(I_A)$ v/s V_{GK} showing the linear curve fitting equation based on which NFS is extracted is shown in Figure 5-4.

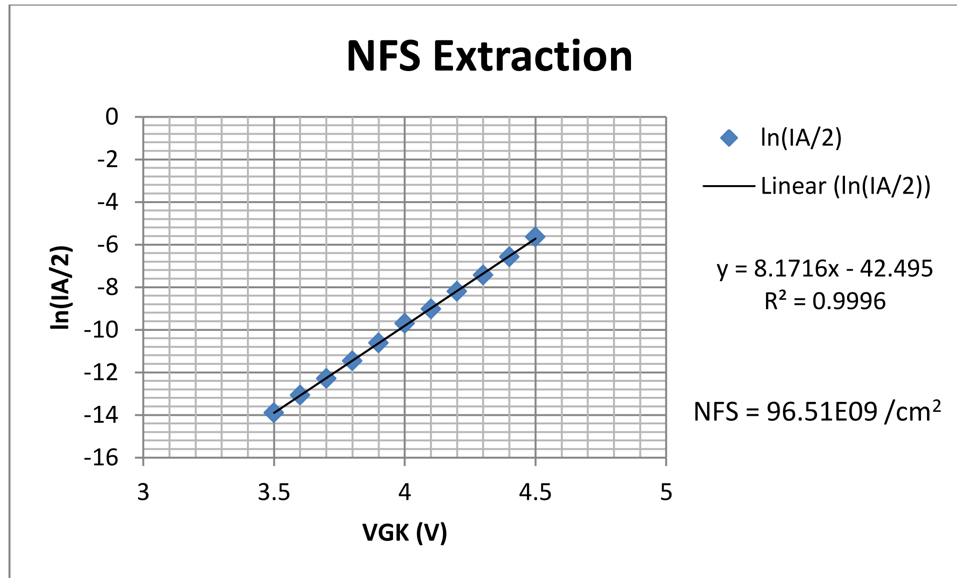

Figure 5-4: Linear curve-fitting for NFS parameter extraction

5.3 Parameter Extraction from Output Characteristics

5.3.1 IS and NF Extraction

Using the anode current equation (4.9) and the condition $\text{V}_{\text{EB}} \cong \text{V}_{\text{AK}}$ for the diode region, taking log on both sides will yield equation (5.7)

$$\ln(\text{I}_\text{A}) = \ln(\text{IS}) + \frac{\text{V}_{\text{AK}}}{\text{NF}\,\text{V}_\text{T}} \tag{5.7}$$

Using (5.7) a linear curve-fitting done on the plot of $\ln(I_A)$ v/s V_{AK} shown in Figure 5-5 will give

$$\text{IS} = \text{e}^{\text{Y-intercept}} \tag{5.8}$$

$$\mathrm{NF} = \frac{1}{\mathrm{Slope_{NF}}\,\mathrm{V_T}} \text{ where } \mathrm{Slope_{NF}} = \frac{\mathrm{d(ln(I_A))}}{\mathrm{d(V_{AK})}} \quad (5.9)$$

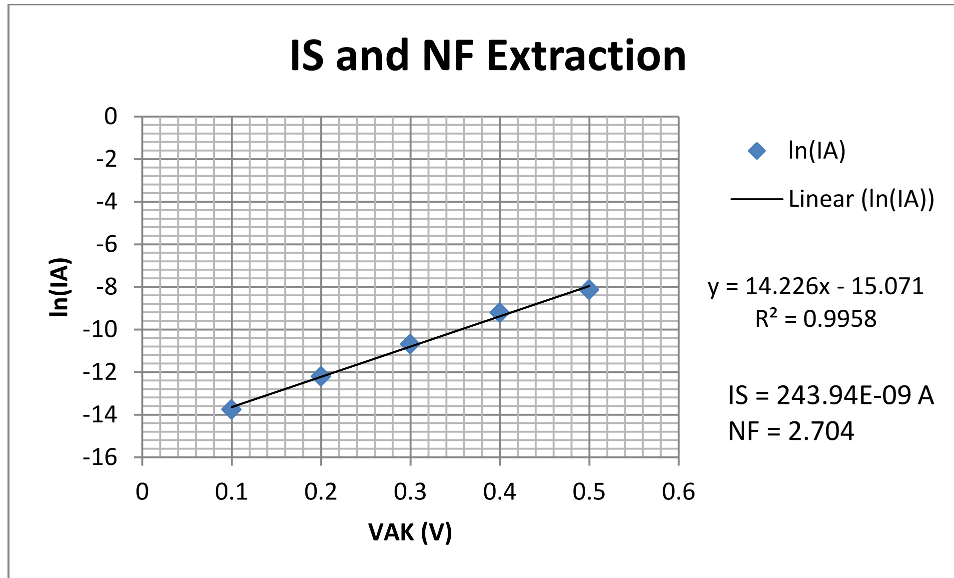

Figure 5-5: Linear curve fitting for IS and NF parameter extraction

5.3.2 VAF Extraction

The Early voltage effect is seen in the form of a slope in the saturated portion of the output characteristics. Since the higher values V_{GK} take longer to saturate, this parameter is extracted from the highest available V_{GK} curve using the following equation (5.10) applied to the plot shown in Figure 5-6.

$$\mathrm{VAF} = -(\mathrm{X} - \mathrm{intercept}) = \frac{\mathrm{Y{-}intercept}}{\mathrm{Slope_{VAF}}} \text{ where } \mathrm{Slope_{VAF}} = \frac{\mathrm{d(I_A)}}{\mathrm{d(V_{AK})}} \quad (5.10)$$

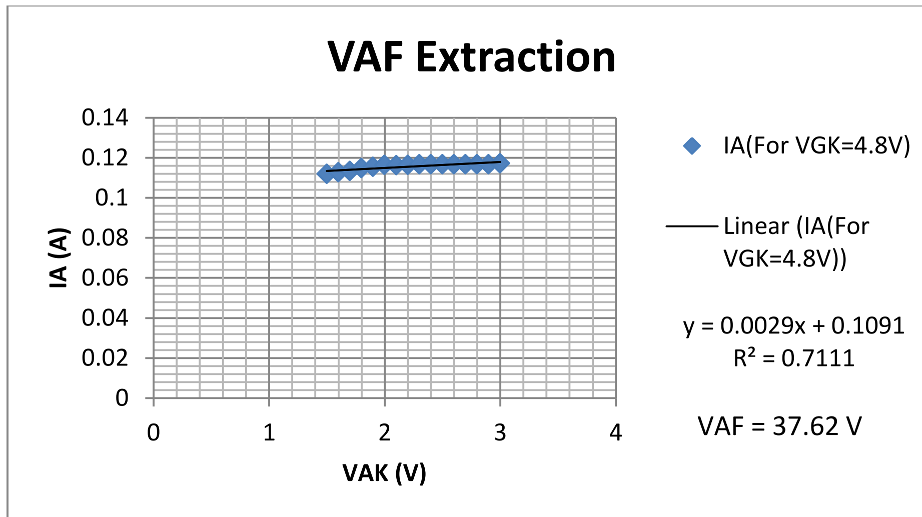

Figure 5-6: Linear curve-fitting for VAF parameter extraction

5.3.3 ISE and NE Initial Approximation

The current equation (4.10) of the linear region is dependent on IS and NF along with ISE and NE. A parameter extraction of the ISE and NE parameters cannot be performed since the level of interdependence between these and IS and NF is not known. Thus, the typical SPICE values are taken as the initial approximation for ISE and NE based on which optimization as described in the next section is performed.

The starting values for the parameter optimization procedure, also known as the seed values, for all the model parameters and how they were obtained are shown in Table 5-1. Since the effect of the model parameters, IS, NF, and NFS are most visible in the log scale, the results of the simulation obtained using the extracted values are shown in both the linear and log scales in Figures 5-7 to 5-10. The optimization procedure using these seed values is described in the next chapter.

Table 5-1: List of Extracted Parameters

SPICE Model Parameter	Seed Value
IS	284.94E-09 A (extracted)
NF	2.704 (extracted)
ISE	100E-15 A (typical)
NE	1.7 (typical)
BF	1 (assumed)
VAF	37.62 V (extracted)
VTO	4.458 V (extracted)
KP	0.9306 A/V^2 (extracted)
NFS	96.51E09 $/cm^2$ (extracted)

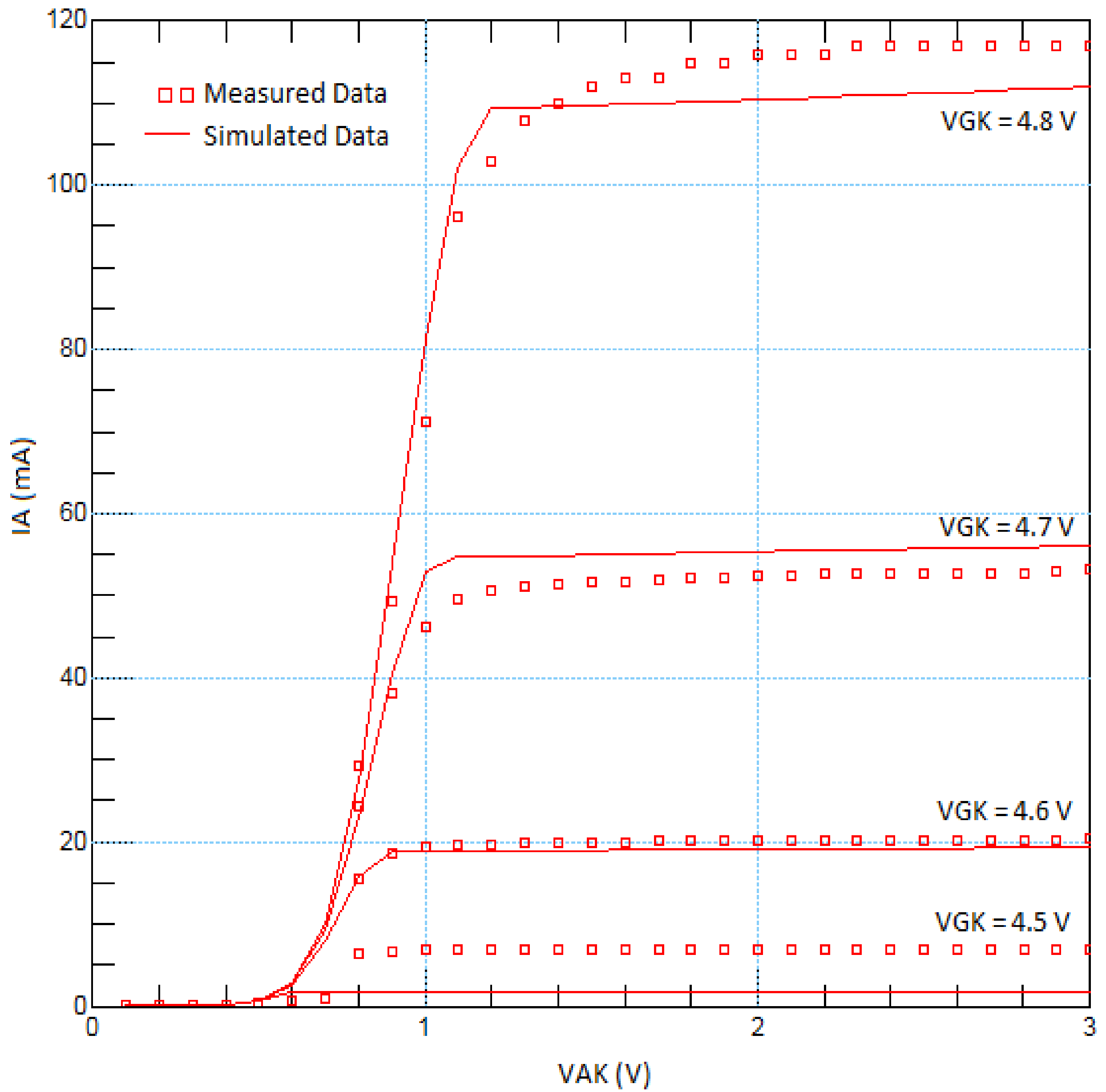

Figure 5-7: Output characteristics simulation after parameter extraction in linear scale

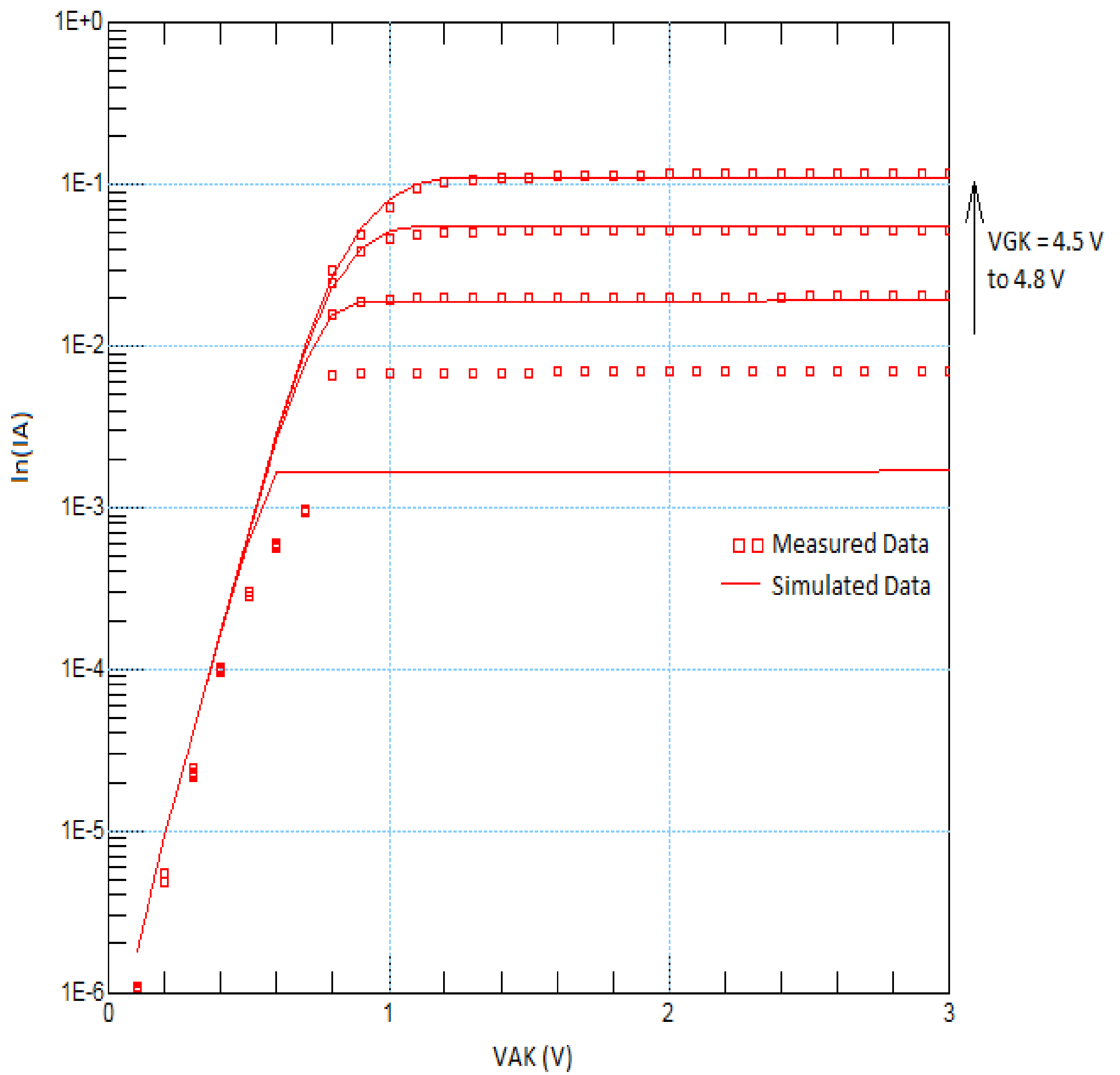

Figure 5-8: Output characteristics simulation after parameter extraction in log scale

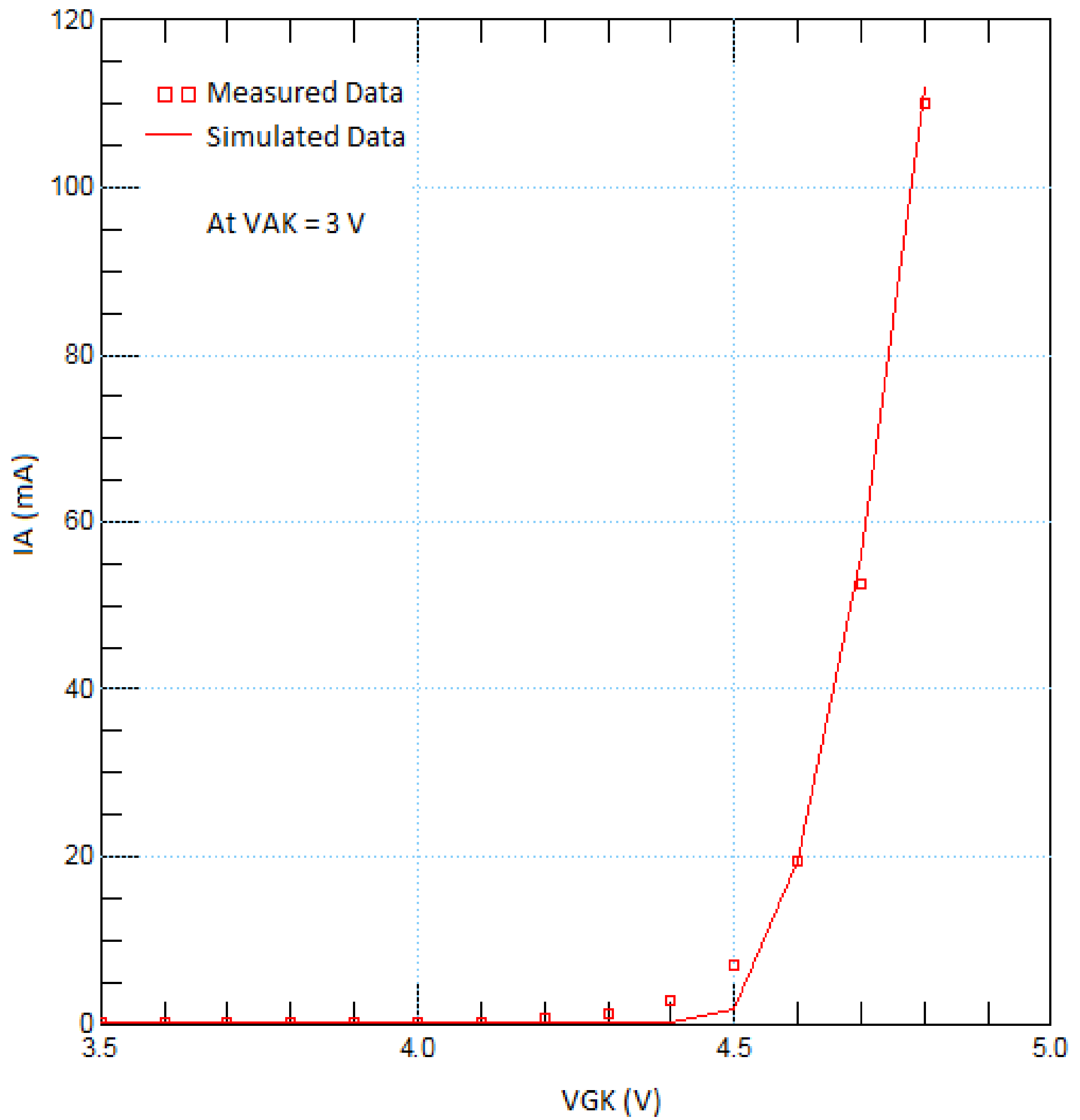

Figure 5-9: Transfer characteristics simulation after parameter extraction in linear scale

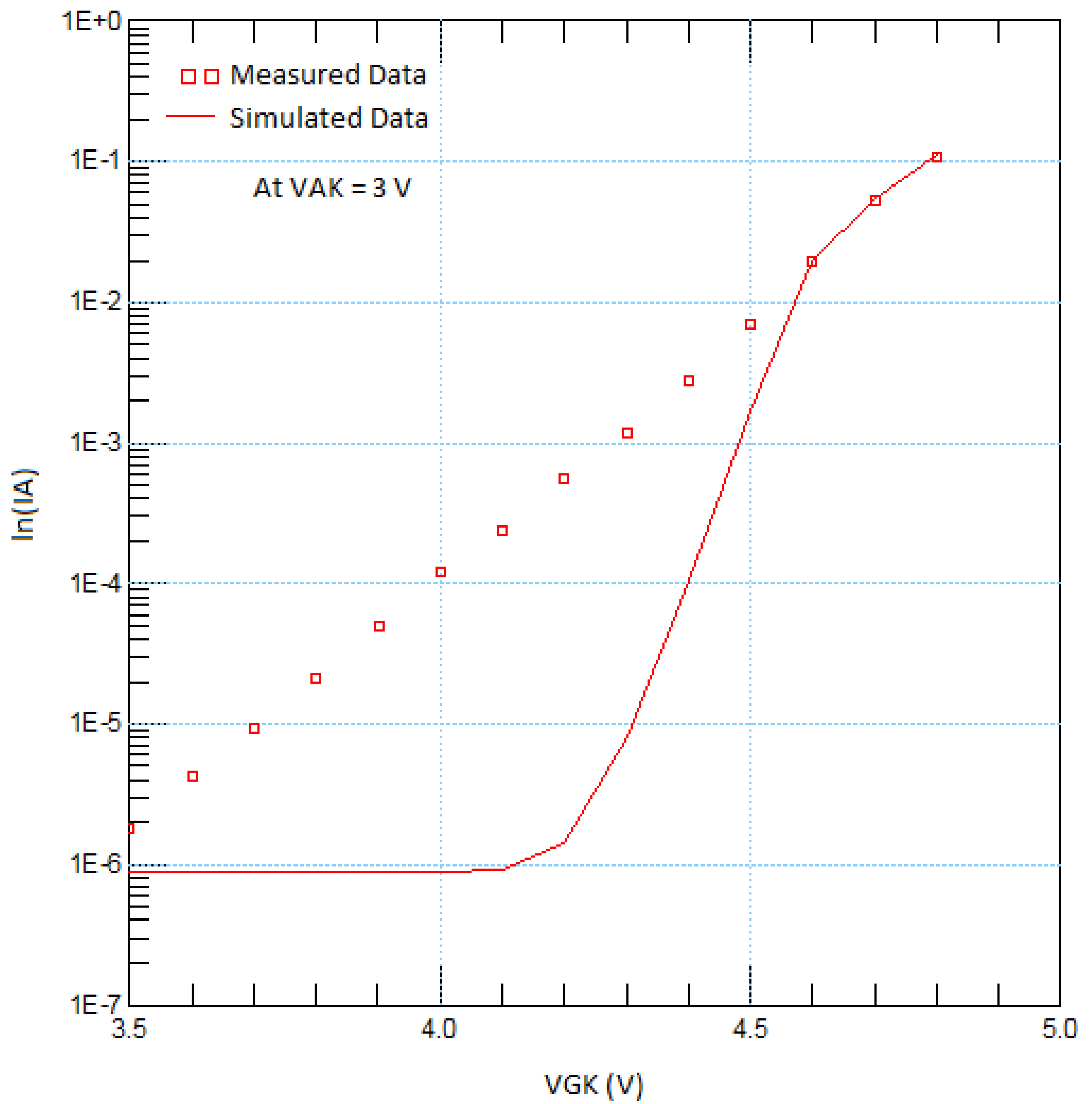

Figure 5-10: Transfer characteristics simulation after parameter extraction in log scale

Chapter 6

Parameter Optimization

Parameter optimization refers to the process in which an algorithm finds the minimum error between the measured and simulated data values. Since the error between the two data sets is due to the incorrect values of model parameters, the algorithm will find the minimum error as a function of the model parameters [18]. In this thesis the Levenberg-Marquardt algorithm is used, which is a standard curve-fitting method used for solving non-linear least squares problems occurring because the error is not a linear function of the model parameters. The Levenberg-Marquardt method iteratively improves the model parameter values to minimize the sum of the squares of the errors between the simulated and measured data points is [21]. The optimization results obtained in the following sections, the MAX error denotes the maximum error between the measured and simulated data and the RMS error denotes the root mean square deviation between the measured and simulated data.

In this thesis the optimization procedure is done depending on the regions of operation described in Chapter 4. The parameters are optimized in the voltage ranges in which they show the most effect on the current characteristics. The voltage ranges for running the optimization are carefully selected to obtain the best fit between the measured and simulated data. Table 6-1 lists the parameters along with the set-ups and voltage range in which they are optimized.

Table 6-1: List of optimization set-ups and voltage ranges

Optimization Order	Set-Up	Voltage Range	Model Parameter
1	Transfer Characteristics	Sub-Threshold Region V_{GK} = 3.5 V to 4.5 V V_{AK} = 3 V	VTO NFS
2	Output Characteristics	Diode Region V_{AK} = 0.1 V to 0.5 V V_{GK} = 4.5 V to 4.8 V	IS NF
3	Output Characteristics	Linear Region V_{AK} = 0.8 V to 1.2 V V_{GK} = 4.7 V to 4.8 V Saturation Region V_{AK} = 1.3 V to 3V V_{GK} = 4.5 V to 4.8 V	ISE NE BF KP VAF

6.1 Sub-Threshold Region Optimization

The optimization process begins by first optimizing the threshold voltage and the NFS parameter which defines the current in the sub-threshold region. Both these parameters are important in terms of defining the threshold voltage for the device. In the

manufacturer's model and all other presently available IGBT models show an abrupt switch in the current as the MOSFET moves from weak inversion to strong inversion. However, in practice this is not true and the current change form weak inversion to strong inversion is more subtle. The NFS parameter correctly accounts for this change but is not the most accurate measure of this phenomenon.

The optimization algorithm is run in the voltage range specified in Table 6-1 on the $\ln(I_A)$ data.The results of the optimization in this region are given in Table 6-2 and the transfer characteristics simulation using the optimized value are shown in the linear and log scales in Figures 6-1 and 6-2 respectively.

Table 6-2: Optimization results in the sub-threshold region

Model Parameter	Seed Value	Optimized Value	MAX Error	RMS Error
VTO NFS	4.458 V 96.51E09 /cm^2	4.457 V 767.1E09 /cm^2	2.640%	1.116%

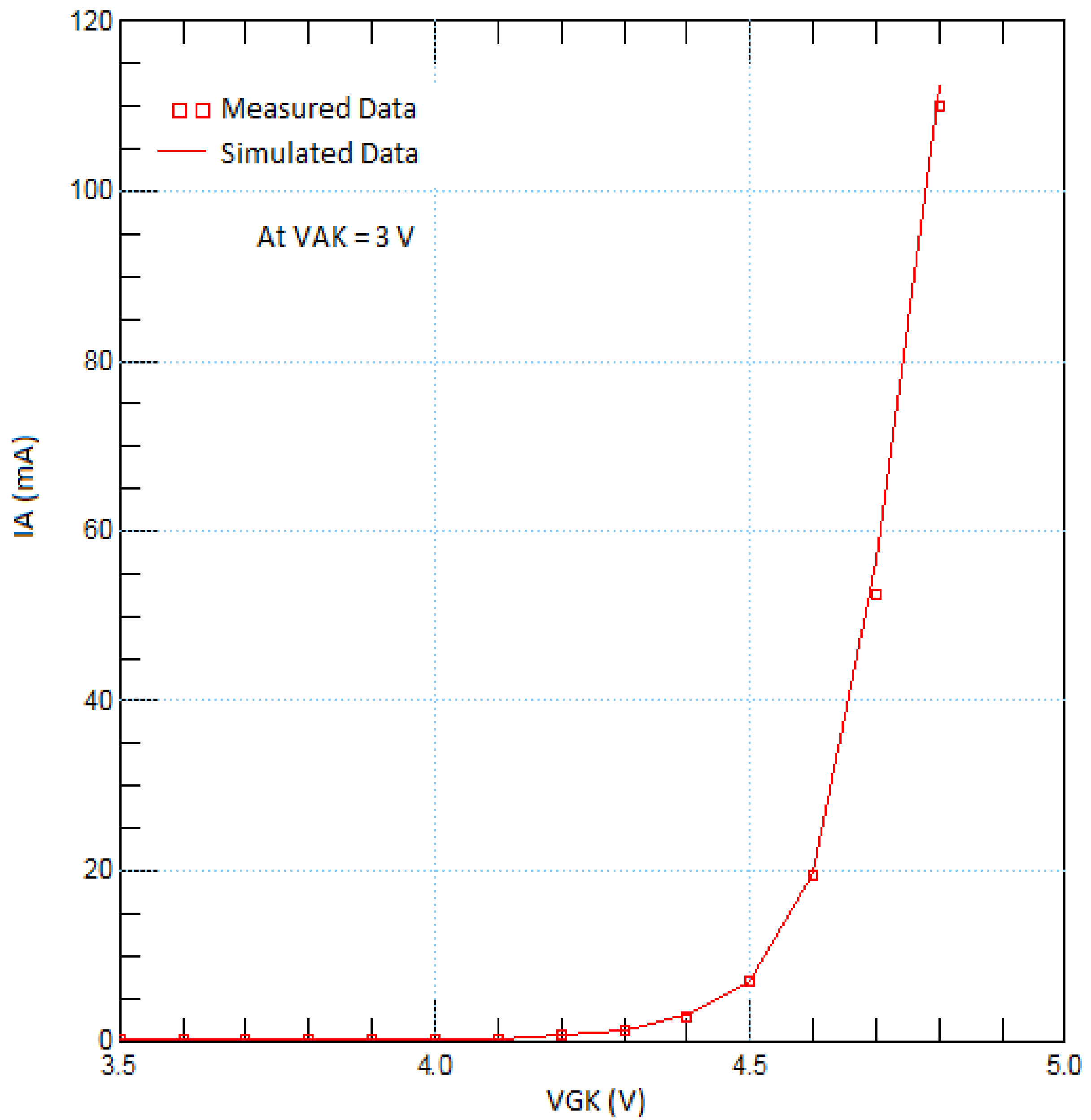

Figure 6-1: Transfer characteristics simulation results after optimization in linear scale

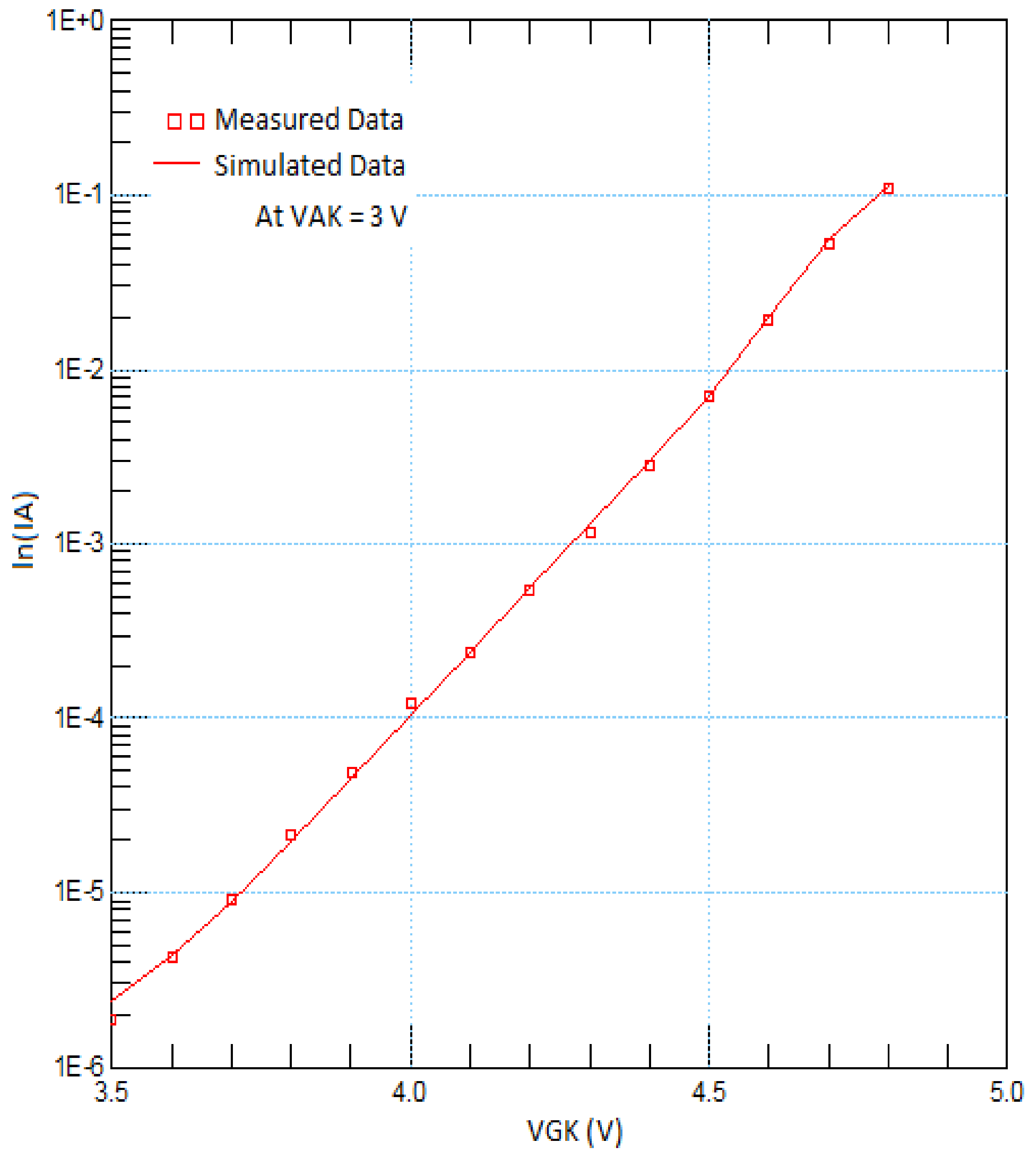

Figure 6-2: Transfer characteristics simulation results after optimization in log scale

6.2 Diode Region Optimization

The optimization algorithm is run on the log current characteristics for the voltage ranges given in Table 6-1 in the diode region to optimize the model parameters IS and NF. The optimization results are shown in Table 6-3. The simulation result for the output characteristics in the log scale is shown in Figure 6-3.

Table 6-3: Optimization results in diode region

Model Parameter	Seed Value	Optimized Value	MAX Error	RMS Error
IS NF	284.94E-09 A 2.704	175.7E-09 A 2.792	3.085%	1.227%

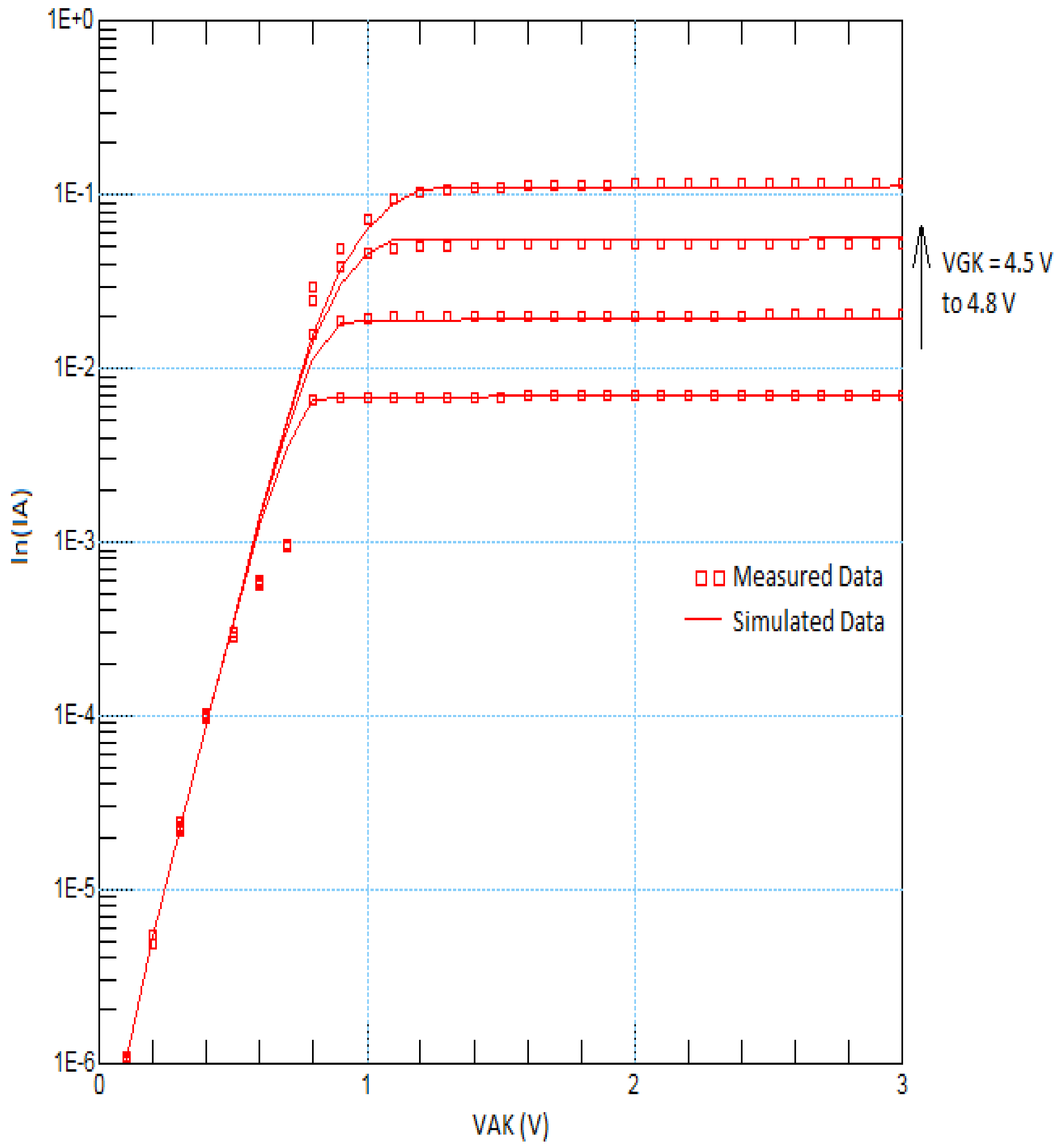

Figure 6-3: Output characteristics simulation result in log scale after optimization

6.3 Linear and Saturation Region Optimization

The current characteristics in saturation region of the transfer characteristics set-up are imported into the output characteristics set-up. Both data sets are used to optimize the model parameters BF, KP and VAF. It is observed that VAF has a noticeable effect only for the higher values of V_{GK}. For the model parameters ISE and NE, optimization is performed only on the V_{GK} = 4.7 V and V_{GK} = 4.8 V curves because the linear region is observable only for these two curves. For gate voltages very close to threshold (V_{GK} = 4.5 and 4.6 V), the MOSFET is observed to directly switch from sub-threshold to saturation region. The results of the first round of optimization are shown in Table 6-4. The simulation result for the output characteristics in linear scale is shown in Figures 6-4.

Table 6-4: Optimization results in the linear and saturation regions

Model Parameters	Seed Value	Optimized Value	MAX Error	RMS Error
BF	1	0.8	7.468%	3.892%
KP	0.9306 A/V^2	1.028 A/V^2		
VAF	37.62 V	15.67 V		
ISE	100E-15 A	123.8E-15 A		
NE	1.7	3.032		

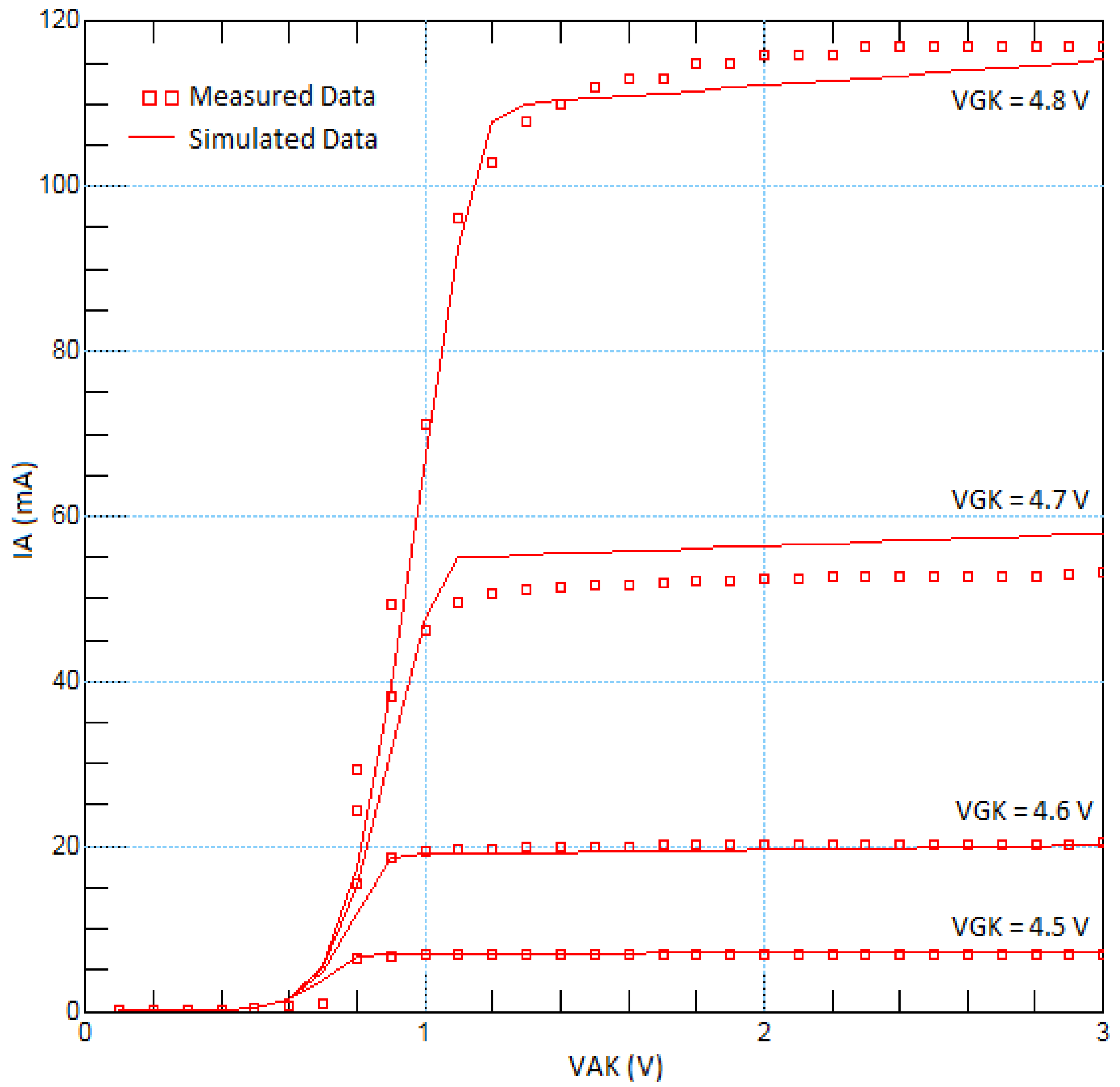

Figure 6-4: Output characteristics simulation result in linear scale after optimization

6.4 Optimization Refinement

The optimization procedure is repeated to reduce the MAX and RMS error values for all set-ups. The optimization refinement begins with adjusting the threshold voltage. When the threshold voltage moves, the slope of the saturation region in the transfer characteristics also affected. To adjust that, the saturation region in the output characteristics is adjusted. Finally, the diode region is optimized. The set-ups, voltage ranges and the order in which the model parameters are optimized is shown in Table 6-5.

Table 6-5: List of optimization refinement set-ups and voltage ranges

Optimization Order	Set-Up	Voltage Range	Model Parameter
1	Transfer Characteristics	Sub-Threshold Region V_{GK} = 3.5 V to 4.5 V V_{AK} = 3 V	VTO NFS
2	Output Characteristics	Saturation Region V_{AK} = 1.3 V to 3V V_{GK} = 4.5 V to 4.8 V	BF KP VAF
3	Output Characteristics	Diode Region V_{AK} = 0.1 V to 0.5 V V_{GK} = 4.5 V to 4.8 V	IS NF

The combined results of the optimization refinement procedure are shown in Table 6-6.

Table 6-6: Optimization refinement results

Model Parameters	Optimized Value	Refined Optimized Value	MAX Error	RMS Error
VTO NFS	4.457 V 767.1E09/cm^2	4.466 V 779.1E09/cm^2	1.60%	0.8042%
BF KP VAF	0.8 1.028 A/V^2 15.67 V	0.5235 1.284 A/V^2 11.10 V	6.409%	3.38%
IS NF	175.7E-09 A 2.792	116.3E-09 A 2.770	2.658%	1.226%

The results of simulation after the refinement are shown in Figures 6-5 to 6-8.

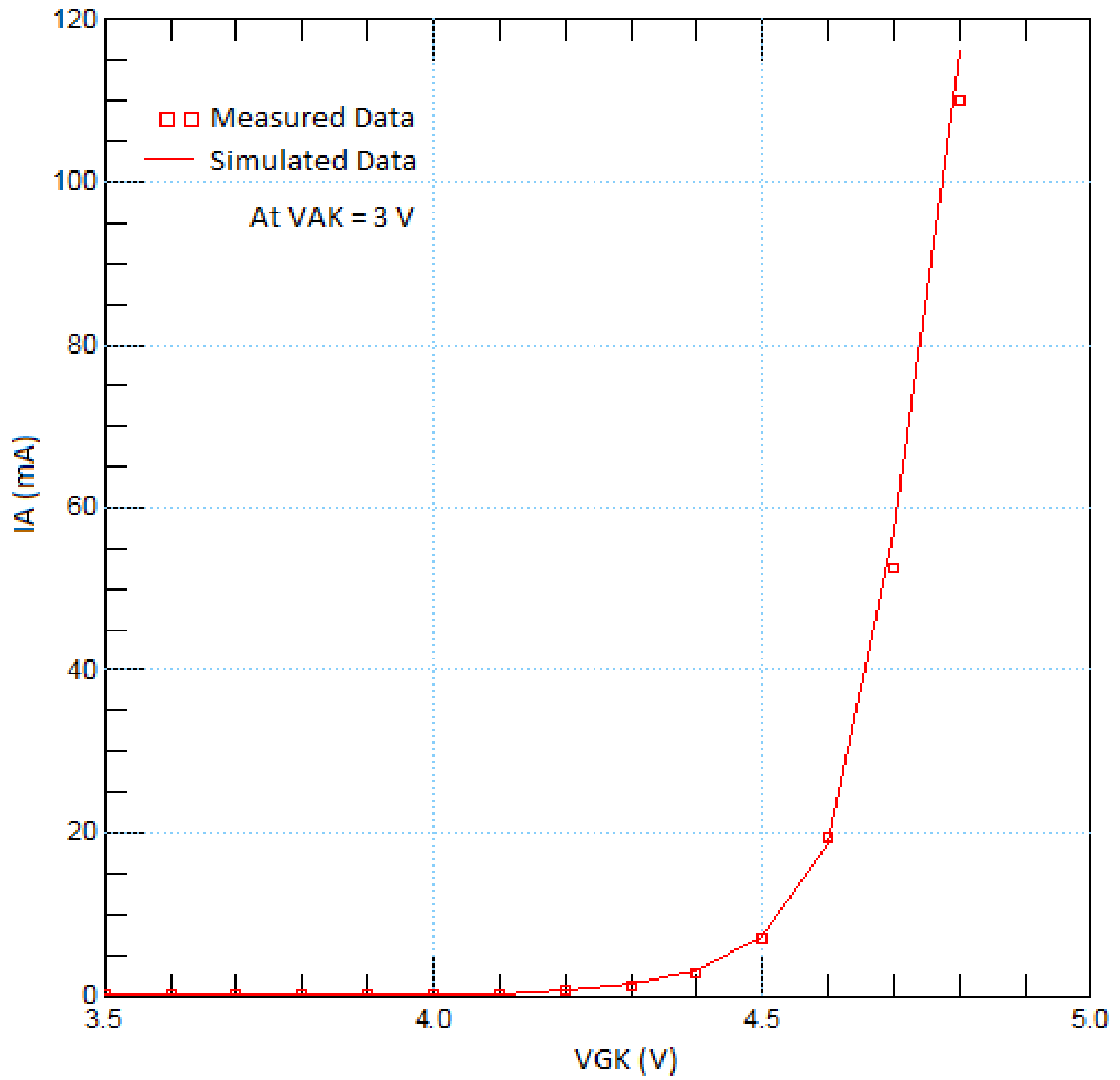

Figure 6-5: Transfer characteristics simulation result in linear scale after optimization refinement

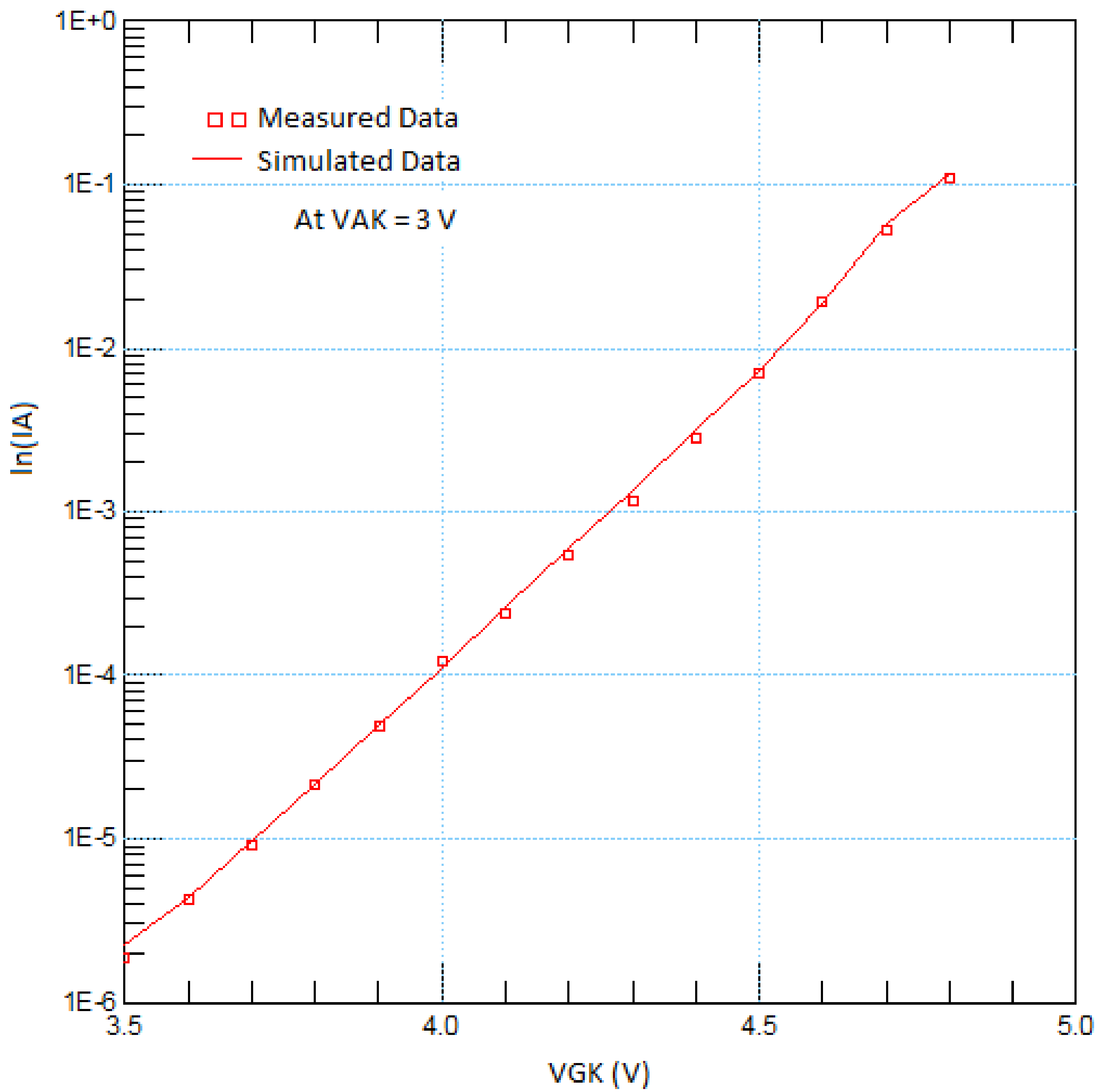

Figure 6-6: Transfer characteristics simulation result in log scale after optimization refinement

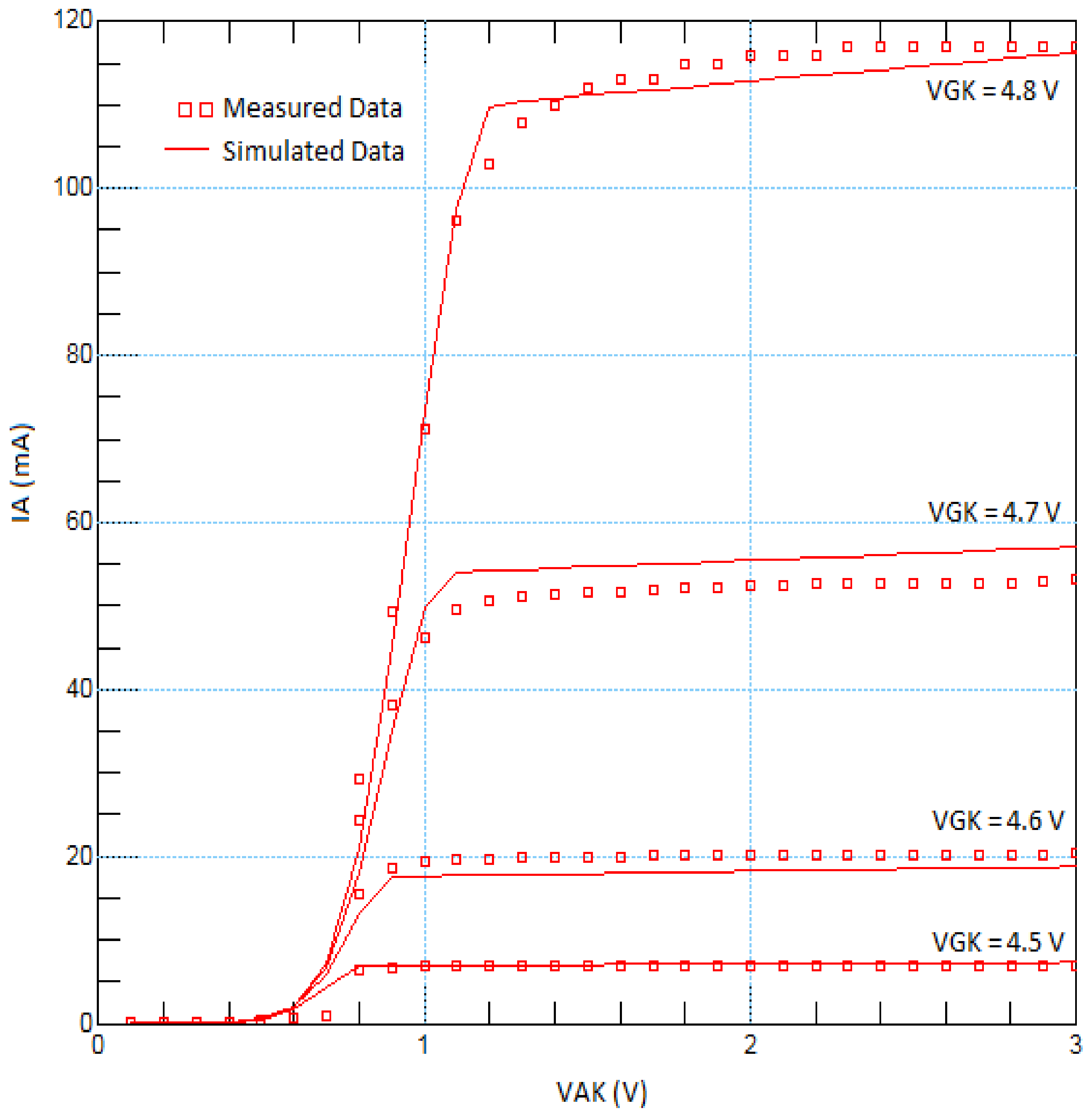

Figure 6-7: Output characteristics simulation result in linear scale after optimization refinement

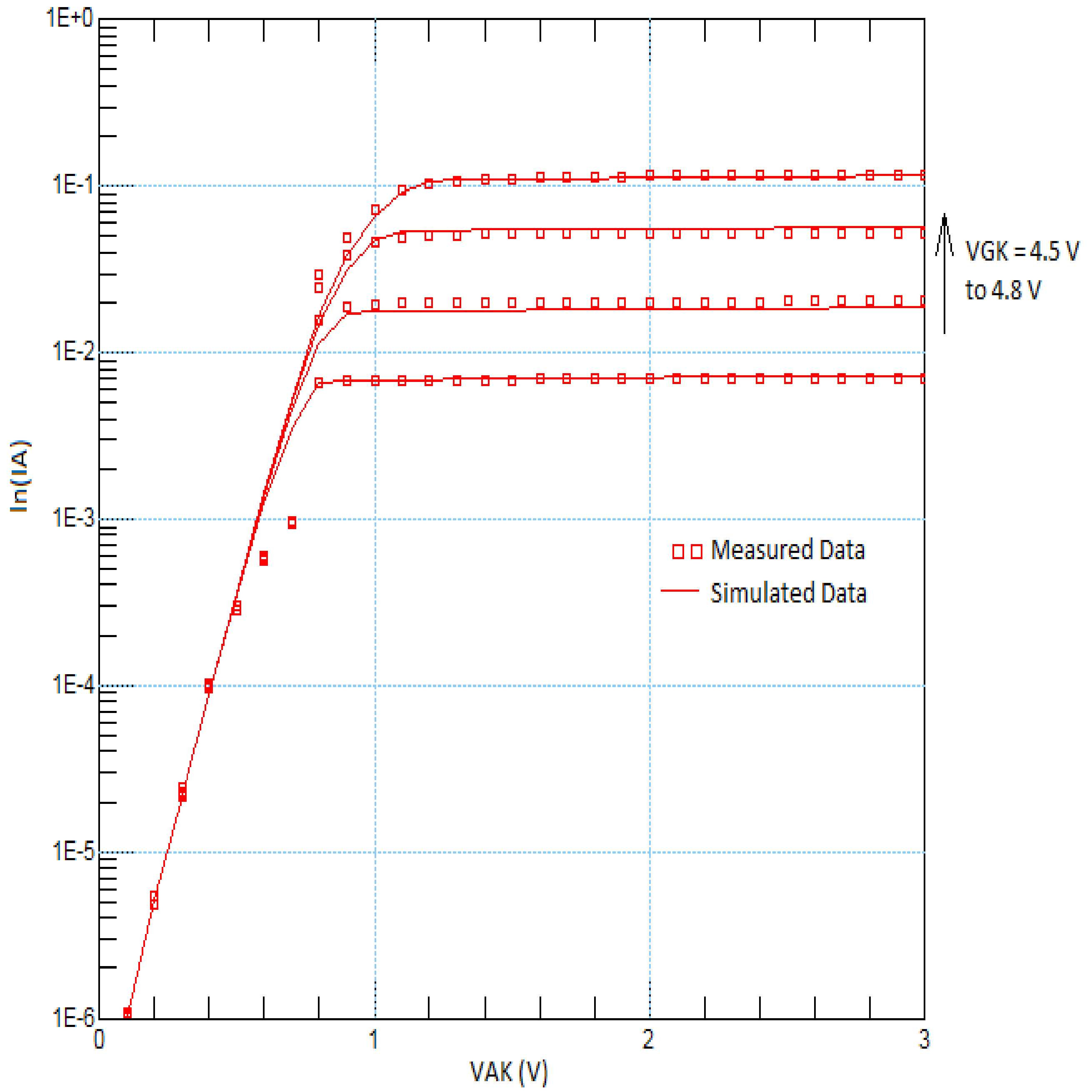

Figure 6-8: Output characteristics simulation result in log scale after optimization refinement

Chapter 7

Conclusion and Future Work

7.1 Comparison with Manufacturer's Model

The final model parameters obtained after optimization refinement for the near-threshold model for defining the low voltage static characteristics are compared with those used by the manufacturer in Table 7-1.

Table 7-1: Model Parameter Comparison

Model Parameters (BJT)	Description	Near-Threshold Model	Manufacturer's Model
IS	Saturation current	116.3E-09 A	24.5E-15 A
NF	Forward current emission co-efficient	2.770	-
ISE	Base-emitter leakage saturation current	123.8E-15 A	141E-18 A
NE	Base-emitter leakage emission co-efficient	3.032	1.974
BF	Ideal maximum forward current gain	0.5235	0.864
VAF	Forward Early voltage	11.10 V	894.9 V

Table 7-1 – *Continued*

Model Parameters (MOSFET)	Description	Near-Threshold Model	Manufacturer's Model
VTO	Zero-bias threshold voltage	4.466 V	3.418 V
NFS	Surface-fast state density	779.1E09 /cm^2	-
KP	Transconductance parameter	1.284 A/V^2	2.512 A/V^2

As evidenced from Table7-1 the manufacturer's model parameters are developed for simulations at high current and voltages as can be seen from the values of BF and KP, which are approximately twice the value of those in the near-threshold model. On the other hand, the low current modeling parameters of IS and ISE in the near-threshold model are about three orders of magnitude larger than those in the manufacturer's model.

7.2 Conclusions

As seen in Tables 3-1 and 3-2, the BJT and MOSFET models given by the manufacturer include additional parameters such as IKF and NK for modeling the bipolar current characteristics under high level injection conditions and THETA for modeling the MOSFET current characteristics at high currents.

The manufacturer's model does not include the NFS parameter used for modeling the sub-threshold current. It is observed that if the sub-threshold current modeling is not included the threshold voltage gets optimized to a value higher than its

true value. By monitoring the change in NFS, the change in sub-threshold current can be noted, which may be indicative of a changing threshold voltage. Monitoring the change in threshold voltage is important for knowing the viability of the device. Increase in internal device temperature will cause the threshold voltage to decrease, which will cause the device to switch to saturation before the intended gate voltage is reached. In case of aging, the threshold voltage will increase which will require that the gate voltage be decreased below the intended value to turn-off the device. In either case, if device is not turned-off correctly, ultimately latch-up might occur. As a result, the near-threshold model gives a better indication of the changes in the threshold region compared to the manufacturer's model. A comparison of the transfer characteristics of the two models is shown in Figure 7-1.

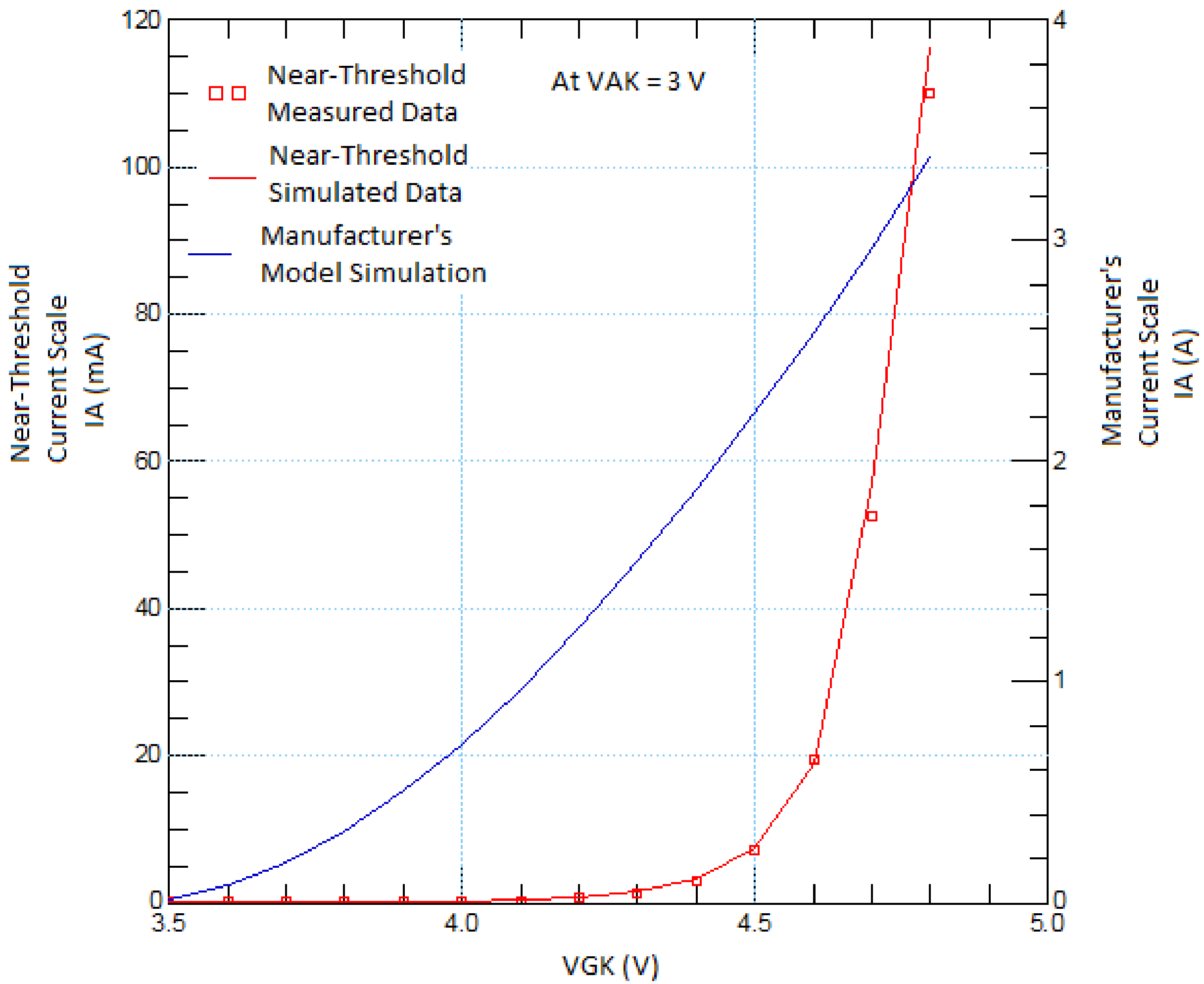

Figure 7-1: Transfer characteristics comparison of near-threshold and manufacturer's model

The result of comparison of the output characteristics of the two models is shown in Figure 7-2.

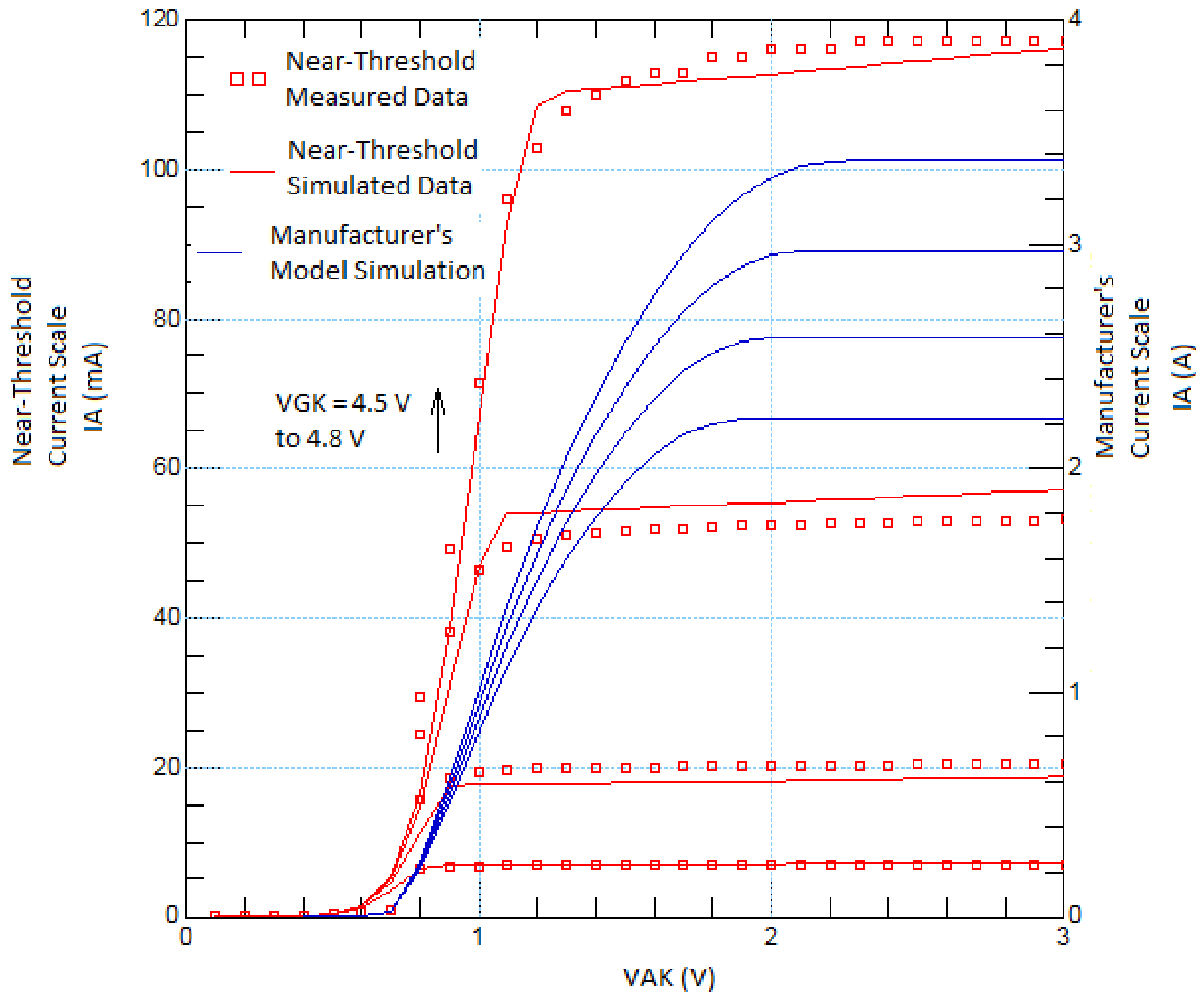

Figure 7-2: Output characteristics comparison of near-threshold and manufacturer's models

Since the threshold voltage value for the near-threshold model is higher than that of the manufacturer's model, the effect of higher threshold voltage on the on-state voltage can be seen in Figure 7-1. The manufacturer's model overestimates the current at low voltages. As a result, it overestimates the value of the on-state voltage, $V_{AK(on)}$. If

the device is nearing latch-up and due to aging the threshold voltage increases, then the on-state voltage will decrease. The manufacturer's model will not be able to correctly estimate the voltage at which current saturation will begin.

To estimate $V_{AK(on)}$ correctly, the model parameters, IS, NF, ISE and NE can be monitored. By comparing the value of these parameters under normal operating conditions with those extracted when the device is under stress, it can be estimated if the voltage at which current saturation begins has decreased. This can prove as a valuable indicator of impending device failure.

7.3 Future Work

The model developed in this thesis can be expanded further to include the temperature dependence of the model parameters. This will show how sensitive the parameters to changes in temperature.

Another avenue of research is finding the correlation between temperature increase and latch-up. Based on the current study that latch-up leads to internal temperature increase, which causes the junctions to breakdown, a hypothesis is proposed that the converse may also be true. That is, increase in the internal temperature of the device causes junction breakdown which then leads to latch-up.

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Farah Vandrevala was born in the city of Mumbai, India on November 14, 1988. She received her Bachelor of Engineering degree in Electronics and Telecommunication from Rajiv Gandhi Institute of Technology, University of Mumbai, Mumbai, India, in September 2010. She started her graduate career as an Electrical Engineering master's student at the University of Texas at Arlington in August 2010. She joined the Analog Integrated Circuits Research Group at the University of Texas at Arlington in June 2011 and started her research work in semiconductor device modeling under the expertise of Dr. Ronald L. Carter. She was awarded an Electrical Engineering scholarship in August 2011 and August 2012. From September 2012 to present she has worked as a student associate under Dr. Carter. Her research interests include semiconductor device physics, semiconductor device modeling and quantum electronics.