ANALYSIS AND MODELING OF SELF HEATING IN SILICON GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTORS

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ABSTRACT

ANALYSIS AND MODELING OF SELF HEATING IN
SILICON GERMANIUM HETEROJUNCTION
BIPLOAR TRANSISTORS

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Silicon Germanium (SiGe) hetero junction bipolar transistors (HBTs) have been established as a strong technology contender for a host of circuit applications including analog, mixed signal and Radio Frequency (RF) designs. Due to the effect of technology scaling, self heating plays a significant role in the performance of SiGe HBTs. This thesis paper does an extensive analysis on the effect of self heating and uses different DC and time domain methods to extract the self heating parameters thermal resistance (R_{TH}) and thermal capacitance (C_{TH}). An expression for thermal resistance considering thermal conductivity as a function of temperature is derived. Also a method to convert a multi pole thermal model to a single pole thermal model is introduced.

The VBIC (Vertical Bipolar Inter Company) model is used for all the simulations. Simulations are performed using Cadence and ICCAP (Integrated circuit characterization and Analysis Program) tools. Measurements are done using Agilent 4142 DC source and Agilent 6000 series oscilloscope. National Semiconductor's SiGe HBTs from their CBC8 process are used for getting real data.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS iii

ABSTRACT iv

LIST OF ILLUSTRATIONS viii

LIST OF TABLES x

Chapter Page

1. INTRODUCTION 1

1.1 Properties and principle of operation of HBTs 2

1.2 Summary 4

2. SELF HEATING OF A TRANSISTOR 5

2.1 Introduction 5

2.1.1 Definition of thermal terms 6

2.1.2 Thermal-electrical analogy 6

2.2 Derivation of the expression 7

2.2.1 Thermal resistance in one-dimension 7

2.2.2 Temperature dependence of thermal resistance 8

2.2.3 Thermal resistance in one-dimension after applying Kirchhoff's transformation 9

2.2.4 Thermal capacitance in one-dimension 10

2.3 Summary 11

3. MODELING OF HBTs 12

3.1 Introduction 12

3.1.1 Physics based Models 12

3.1.2 Physics Based Analytical Models 13

3.1.3 Black Box Analytical Models 14

3.1.4 Table based models 14

3.2 Choice of Model 15

3.2.1 The VBIC Model 15

3.3 Masana's method 17

3.3.1 Derivation of expressions for R_{TH} and C_{TH} 18

3.3.2 Electric Circuit Representation 21

3.3.3 Conversion of Foster network to Cauer network 23

3.3.4 Steps involved in the thermal modeling of a device 23

3.3.5 Example 24

3.4 Joy and Schlig Thermal Resistance 27

3.4.1 Model description 27

3.4.2 Simulations 28

3.5 Summary 31

4. DC METHOD FOR THERMAL RESISTANCE MEASUREMENT 32

4.1 Introduction 32

4.2 Bovolon's method 32

4.3 Temperature measurement 34

4.4 Measurement results 35

4.4.1 Step by step procedure for thermal resistance calculation using the DC method 35

4.4.2 Plots and circuit diagrams 35

4.5 Summary 46

5. TIME DOMAIN METHOD FOR MEASUREMENT OF THERMAL RESISTANCE AND THERMAL CAPACITANCE 47

5.1 Introduction 47

5.2 ICCAP measurement and modeling tool 47

5.2.1 Optimization using ICCAP 49
5.3 Circuit setup 50
5.4 Measurement results 52
5.4.1 Results and Plots of optimizations 52
5.4.2 Summary of results 61
5.5 Conversion from multi-pole model to a single pole model 62
5.6 Summary 65
6. CONCLUSION AND RECOMMENDATION FOR FUTURE WORK 66
REFERENCES 68
BIOGRAPHICAL INFORMATION 71

LIST OF ILLUSTRATIONS

Figure Page

1.1 The energy band diagram of an HBT. 3

2.1 The thermal network in VBIC Model 7

3.1 Schematic of the VBIC model. 16

3.2 Volume for the calculation of thermal resistance 19

3.3 Volume for applying VAM 20

3.4 Foster and Cauer network representation 22

3.5 Foster network representation of thermal network for a SiGe HBT 24

3.6 Cauer network representation of thermal network for a SiGe HBT 24

3.7 Time Response of the Foster and Cauer networks. 25

3.8 Heat source, simulating transistor power dissipation located below the surface of a semi-infinite medium 27

3.9 Matlab simulation of thermal response at the centre of the emitter. 29

3.10 The curve in figure 3.9 is fitted with a 3-pole expression using the curve fitting tool in Matlab. 29

3.11 Matlab simulation of thermal response at the edge of the emitter. 30

3.12 The curve in figure 3.11 is fitted with a 3-pole expression using curve fitting tool in Matlab.. 31

3.11 Matlab simulation of thermal response at the edge of the emitter. 30

4.1 Reverse Gummel set up for temperature measurement 36

4.2 Plot of estimated temperature for a 5 um^2 device. Only the points used for curve fitting to a parabola is shown.. 36

4.3 Forward Gummel set up… 37

4.4 Forward Gummel plot at temperature T_1 for a 5 um^2 device... 38

4.5 Forward Gummel plot at temperature T_2 for a 5 um^2 device. 38

4.6 Tcommon emitter set up. 39

4.7 Common emitter I_c vs V_{ce} plot at temperature T_1 for a 5 um^2 device 40

4.8 Common emitter I_c vs V_{ce} plot at temperature T_2 for a 5 um^2 device. 40

4.9 Common emitter V_{be} vs V_{ce} plot at temperature T_1 for a 5 um^2 device. 41

4.10 Common emitter V_{be} vs V_{ce} plot at temperature T_2 for a 5 um^2 device.. 41

4.11 Common emitter power vs V_{ce} plot at temperature T_1 for a 5 um^2 device.. 42

4.12 Common emitter power vs V_{ce} plot at temperature T_1 for a 5 um^2 device. 42

4.13 Thermal resistance vs V_{ce} plot for a 5 um^2 device.. 43

4.14 Thermal resistance vs V_{ce} plot for a 2.5 um^2 device.. 43

4.15 I_c vs V_{bc} plot from forward Gummel setup. 45

5.1 General functionality of ICCAP system 48

5.2 Optimization flow diagram. 50

5.3 Circuit setup for time domain measurements.. 51

5.4 Optimization done using ICCAP for low voltage NPN 0.15 um^2 SiGe HBT device 53

5.5 Optimization done using ICCAP for low voltage NPN 0.2 um^2 SiGe HBT device 54

5.6 Optimization done using ICCAP for low voltage NPN 0.25 um^2 SiGe HBT device 55

5.7 Optimization done using ICCAP for low voltage NPN 1.25 um^2 SiGe HBT device 56

5.8 Optimization done using ICCAP for high voltage NPN 2.5 um^2 SiGe HBT device. 57

5.9 Optimization done using ICCAP for high voltage PNP 0.25 um^2 SiGe HBT device 58

5.10 Optimization done using ICCAP for high voltage PNP 2.5 um^2 SiGe HBT device 59

5.11 Optimization done using ICCAP for high voltage PNP 5 um^2 SiGe HBT device 60

5.12 Comparison of 1-pole, 2-pole & 3-pole fit for a 5um^2 high voltage PNP device.. 61

5.13 Frequency response plot for the 3-pole model and the 1-pole model for a 0.15 um^2 NPN device.. 64

5.14 The plot in figure 5.13 is re-plotted with a log Y-axis. 64

LIST OF TABLES

Table Page

1.1 Comparison of performance between different transistor types 4

2.1 Thermal – Electrical analogy 7

3.1 Comparison between calculated R's and C's of the Foster network and
measured thermal parameters for two SiGe HBT devices.. 25

3.2 Calculated pole values for the curve in figure 3.10 30

3.3 Calculated pole values for the curve in figure 3.12 31

4.1 Thermal resistance values calculated for 5 um^2 and 2.5 um^2 device 44

5.1 Bias levels and results after optimization for low voltage NPN 0.15 um^2 SiGe HBT device.... 53

5.2 Bias levels and results after optimization for low voltage NPN 0.2 um^2 SiGe HBT device...... 54

5.3 Bias levels and results after optimization for low voltage NPN 0.25 um^2 SiGe HBT device.... 55

5.4 Bias levels and results after optimization for low voltage NPN 1.25 um^2 SiGe HBT device.... 56

5.5 Bias levels and results after optimization for high voltage NPN 2.5 um^2 SiGe HBT device 57

5.6 Bias levels and results after optimization for high voltage PNP 0.25 um^2 SiGe HBT device .. 58

5.7 Bias levels and results after optimization for high voltage PNP 2.5 um^2 SiGe HBT device 59

5.8 Bias levels and results after optimization for high voltage PNP 5 um^2 SiGe HBT device........ 60

5.9 Summary of results obtained in time domain measurements. 61

5.10 Summary of conversion of multi pole values in table 5.8 to single pole values
using energy conservation.. 63

CHAPTER 1

INTRODUCTION

Next-generation communications systems will place increasingly stringent demands upon the supporting technologies. Market and industry expectations call for emerging wireless communications infrastructure to support data and multimedia alongside voice, providing high value content to wireless communications, thereby requiring extremely high data rates. Additionally, the transmission of this content should be of high quality, with interruption free data transfer and mobile voice indistinguishable from wire-line voice. Also, these systems will be required to operate at higher frequencies (well into the GHz range) as regulators allocate these higher frequency ranges for wireless communications in order to provide bandwidth for additional subscribers and content [1]. Finally, perhaps representing the most crucial component to the success of emerging wireless communications systems, customers expect mobile handsets to decrease in size, increase in functionality, sustain longer battery life, and remain affordable.

Silicon-Germanium (SiGe) Hetero-junction Bipolar Transistor (HBT) BiCMOS technology can address all of these concerns, and has established itself as strong technology contender for a host of circuit applications including analog, mixed signal, RF and millimeter wave. The peak unity gain frequency (f_T) of state-of-the-art SiGe HBTs far exceeds that of standard Si BJTs and rivals the best of III-V technologies. The compatibility of SiGe with Si permits higher yield and superior levels of system complexity and integration, leveraging the benefits of best-of-breed Si CMOS to offer powerful "mixed-signal" solutions. With the ability to fabricate high performance analog circuits alongside powerful CMOS logic on a single silicon wafer, SiGe HBT BiCMOS technology enables powerful "system-on-a-chip" (SoC) architectures

that facilitate reduced chip count, reduced power consumption, reduced packing complexity, and overall reduced cost [2].

The operating temperature plays a significant role in the performance of hetero-junction bipolar transistors. The adoption of advanced isolation techniques such as silicon-on-insulator (SOI) and deep trench oxide isolation (DTI) to meet the demand for higher speed has degraded the heat spreading across a chip. The poor thermal conductivity of silicon dioxide increases self-heating. The localized heating under the active area of a device due to the trapped heat is called self-heating and is characterized by thermal spreading impedance. This is strongly dependent on the device structure and materials being used for isolation [3]. It is reported [3] that the effect of self-heating is more prominent with transistors with reduced geometries. As a consequence of self-heating, the operating temperature of a device increases beyond the ambient temperature. A more detailed discussion of the effect of self-heating on the performance of transistors is done in the following chapters. This thesis focuses on the self-heating aspects of the HBTs and applies this knowledge to the characterization of these devices. Different methods from estimating the thermal behavior using the structural properties of the device to characterizing these devices from the DC and time-domain measured data have been used. National Semiconductors SiGe HBTs from their CBC8 process have been measured.

1.1 Properties and principle of operation of HBTs

The HBT is used in a circuit in the same way as a BJT. The main difference compared to the BJT, is the improved gain and frequency properties. The emitter in an HBT uses a different material than the base. This material has a higher energy band gap than the base. The band gap in a material is the energy required to move an electron from the valence band to the conduction band. Figure 1.1 shows a principal structure of the energy bands of an HBT.

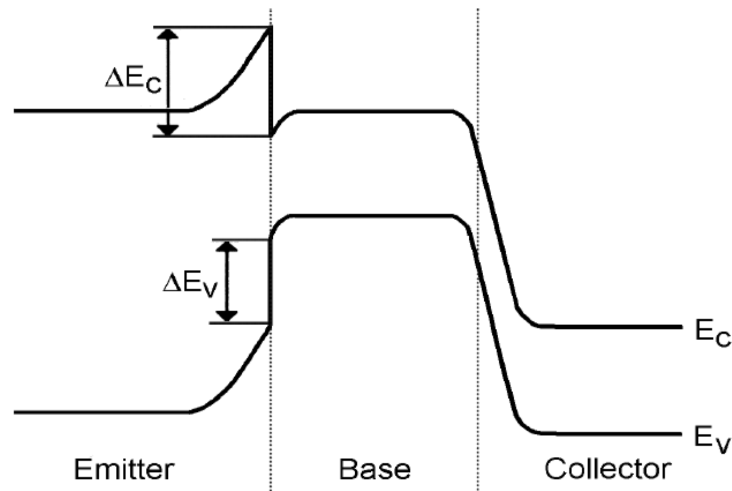

Figure 1.1 the energy band diagram of an HBT [40].

Incorporation of material like Ge into the crystal lattice of the silicon creates a compressive strain in the material (because the Ge atom requires a larger atomic separation), and as a result, reduces the bandgap of the material of the base. In a typical HBT, this bandgap difference between layers of semiconductor materials affects the injection of carriers between the two sides of the junctions. The electrons coming from the emitter have a very high potential energy when they enter the base region, due to the increased band gap in the emitter compared to the base. This causes the current gain to increase significantly more than the normal BJT. The main limitation to the current gain is the re-combinations in the base. The width of the base is therefore important. The gain can be increased even more by making the base narrower, but this increases the base resistance. The operating frequency of a bipolar transistor is inversely proportional to the square of the base width. Hence, there is a trade-off between gain, bandwidth and base resistance in selecting the base doping.

In [4-7] different transistor types are compared, a summary of which is reproduced in Table 1.1. From this data the superior performance of an HBT over a BJT is obvious. From all the transistors mentioned in table 1.1, HBTs are preferred for power amplifiers and oscillators

due to high power density and low phase noise. The choice of the transistor depends not only on performance but also on the application and the production cost.

Table 1.1 Comparison of performance between different transistor types [41].

	MESFET	**HEMT**	**BJT**	**HBT**	**DHBT***
f_t [GHz]	Medium	Medium	Low	High	High
f_{max} [GHz]	Medium	High	Low	Medium	Medium
DC Gain	Medium	High	Low	High	High
Noise figure	Medium	Low	Medium	High	High
Phase noise	Medium	High	Medium	Low	Low
Power Density	Medium	Medium	Medium	High	High
Low voltage	Good	Good	Poor	Medium	Good
Breakdown	Medium	Medium	Medium	High	High/Low
Single supply	No	No	Yes	Yes	Yes

*DHBT stands for double hetero structure bipolar transistor.

An HBT can be made of many types of materials. Four of the most common materials are Si/Ge, AlGaAs/GaAs, InGaP/GaAs, and InP/InGaAs. The SiGe HBT is a rather new Si transistor where the base is composed of a SiGe alloy. The amount of Ge introduced in the base varies from process to process, but is usually in the interval from 8 to 15 % [8]. The Ge concentration in the base can have a gradient between the emitter edge and the collector edge, to avoid large lattice mismatch and thus reduce faults in the lattice and traps.

1.2 Summary

The importance of fast transistors in the present world is discussed and the role of SiGe HBTs to fit that requirement is substantiated. As the miniaturization of the transistors continues the role of self heating in the performance of the transistors becomes more relevant and has to be studied and modeled accurately to help circuit designers.

CHAPTER 2

SELF HEATING OF A TRANSISTOR

2.1 Introduction

The previous chapter discussed why transistor heating has become an important issue. There are three mechanisms by which a device can get heated:

a. Package thermal effects

This is characterized by the chip to package to ambient thermal impedance [3]. The thermal time constant due to this is large in value, which differs for different package types and is important in designing the cooling system for the unit. Typical package thermal resistance values range from 5 to 200 K/W [9]. This thermal resistance can also be affected by the quality of the die attachment and the heat sink units.

b. Thermal coupling between transistors

The second mechanism by which a device can get heated is by power dissipation in the adjacent chips or devices. This effect is called adjacent heating and can be characterized by thermal coupling resistance [10]. The effect of thermal coupling can be reduced by properly spacing the devices. But in a world of miniaturization spacing the devices apart for preventing thermal coupling may not be desirable.

c. Self-heating of the transistor

The third mechanism by which a device can get heated, which is the primary focus of this paper, is by the temperature increase caused by the power dissipation in its own p-n junctions. This is called self heating and can be characterized by the thermal resistance and thermal capacitance of the device. This can be modeled by either a single pole RC network or multi-pole RC network for improved modeling accuracy. Usually a single pole RC network is

adopted for thermal impedance representation [11]. The values of the thermal resistance and capacitance of a device depend on the structural composition of the device and the device dimensions. The use of technologies like silicon on insulator and deep trench isolation causes the device to be packed inside the walls which has a very low thermal conductivity. This aggravates the problem of self heating by trapping the heat inside the walls and it is the primary mechanism to be considered on heating of a transistor.

2.1.1 Definition of thermal terms

2.1.1.1 Thermal resistance

Thermal resistance is defined as the ratio of the difference in temperatures between two isothermal surfaces and the total heat flow between them. Thermal resistance R_{TH} can be expressed as

$$R_{TH} = \frac{T_J - T_A}{P} \quad (2.1)$$

where T_J is the junction temperature, T_A is the ambient temperature, and P is the heat flow rate. The unit for R_{TH} is K/W.

2.1.1.2 Thermal capacitance

Thermal capacitance (C_{TH}) is a measure of how much heat energy can be stored and dissipated in a device. The unit of C_{TH} is J/K.

2.1.2. Thermal-electrical analogy [10]

From the definitions of thermal resistance, the temperature increase, ΔT, can be written as

$$\Delta T = R_{TH} \times P \quad (2.2)$$

where P is the power dissipation.

In a VBIC model the thermal effects are modeled by implementing an additional thermal network as shown in figure 2.1. The thermal network models the interaction between electrical characteristics and the thermal effects.

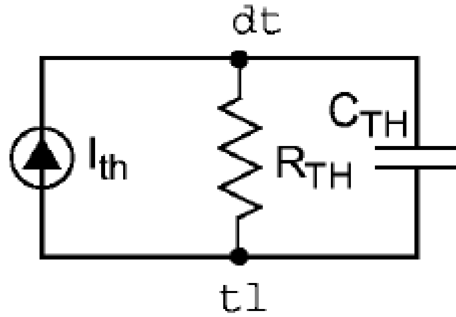

Figure 2.1. The thermal network in VBIC Model [12].

The above thermal sub-circuit with I_{TH} = P X 1 A/W and Z_{TH} = Z_{TH} X 1 Ohm W/K couples the instantaneous power dissipation in the device to the thermal network. Thus, from equation 2.2 the voltage level of the temperature node dt (as per VBIC syntax) is numerically equal to the local temperature rise K, which is used to calculate the instantaneous electrical characteristics of the transistor.

It is clear that the temperature rise in the thermal network is analogous to the voltage rise in an electrical network. Similarly the heat flow, thermal resistance and thermal capacitance have their equivalent terms in an electrical network. Table 2.1 summarizes this analogy between thermal and electrical networks.

Table 2.1 Thermal – Electrical analogy

Thermal		**Electrical**	
Temperature	T in K	Voltage	V in volt
Heat flow	P in W	Current	I in Amp
Thermal resistance	RTH in K/W	Resistance	R in ohm
Thermal capacitance	CTH in J/K	Capacitance	C in Farad

2.2 Derivation of the expressions

2.2.1 Thermal resistance in one-dimension

The heat conduction equation is

$$\vec{\nabla}\left(K \cdot \vec{\nabla} T\right) + Q_v = \rho c \frac{\partial T}{\partial t} \tag{2.3}$$

where K is is the thermal conductivity, Q_v is the thermal energy generated by the internal heat source in a unit volume, ρ is the density and c is the specific heat of the substance. In steady state the heat conduction equation can be written as

$$\vec{\nabla}\left(K \cdot \vec{\nabla} T\right) + Q_v = 0 \qquad (2.4)$$

The above equation is integrated as

$$\iiint \vec{\nabla}\left(K \cdot \vec{\nabla} T\right) dxdydz = -\iiint Q_v \, dxdydz \qquad (2.5)$$

In one dimensional heat conduction, equation 2.5 can be evaluated to be

$$KA\frac{dT}{dx} = -Q \qquad (2.6)$$

where A is the area of thermal source and where Q is the thermal energy. Re-arranging and integrating equation 2.6

$$\int_{T1}^{T2} dT = -\int_{x1}^{x2} \frac{Q}{KA} dx \qquad (2.7)$$

$$T_2 - T_1 = \frac{Q}{KA}(x_1 - x_2) \qquad (2.8)$$

As explained above the thermal resistance is defined as the ratio of the temperature difference across a material and the heat flow between them. Hence

$$Rth = \frac{T_2 - T_1}{Q} = \frac{x_1 - x_2}{KA} = \frac{L}{KA} \qquad (2.9)$$

2.2.2 Temperature dependence of thermal resistance

The thermal conductivity of a substance changes with temperature [13]. For many materials used in semiconductor devices the thermal conductivity K(T) can be expressed as

$$K(T) = K_{ref}\left(\left[\frac{T}{T_{ref}}\right]^{-\alpha}\right) \qquad (2.10)$$

Here K_{ref} is the thermal conductivity at a reference temperature T_{ref}. For silicon the value for α is normally taken to be 4/3.

Since the thermal resistance is inversely proportional to the thermal conductivity, an increase in temperature of the device due to self-heating results in an increase in thermal resistance. The change in thermal resistance is quite large, changing by a factor of more than 2 over the temperature range -50°C to 200°C [13].

2.2.3 Thermal resistance in one-dimension after applying Kirchhoff's transformation

To get an expression for R_{TH} as a function of temperature, Kirchhoff's transformation can be used. The heat conduction equation is

$$\vec{\nabla}\left(K(T) \cdot \vec{\nabla}T\right) + Q_v = \rho c \frac{\partial T}{\partial t} \tag{2.11}$$

In the steady state

$$\vec{\nabla}\left(K(T) \cdot \vec{\nabla}T\right) + Q_v = 0 \tag{2.12}$$

Re-arranging equation 2.12 gives

$$\vec{\nabla}\left(K(T) \cdot \frac{\partial T}{\partial U} \vec{\nabla}U\right) = -Q_v \tag{2.13}$$

From Kirchhoff's transformation U is defined as

$$U = \int_{T_0}^{T} \frac{K(T)}{K_0} dT \tag{2.14}$$

Differentiating equation 2.14

$$\frac{\partial U}{\partial T} = \frac{K(T)}{K_0} \tag{2.15}$$

Substituting equation 2.15 into 2.13 gives

$$K_0.\nabla^2 U = -Q_v \tag{2.16}$$

If heat flow is in the x-direction equation 2.16 can be integrated

$$K_0.A\frac{dU}{dx} = -Q \tag{2.17}$$

where A is the area of the heat source and Q is the thermal energy in x-direction.

Integrating again

$$\int dU = -\int_{x1}^{x2} \frac{Q}{K_0.A} dx \tag{2.18}$$

Hence

$$U = \frac{Q}{K_0.A}(x_1 - x_2) = \frac{QL}{K_0.A} \tag{2.19}$$

The functional relationship of K with temperature for Si is [14]

$$K(T) = K_0(\left[\frac{T}{T_0}\right]^{-1.2}) \tag{2.20}$$

Substituting this into the equation 2.14

$$U = \int_{T_0}^{T} \frac{K(T)}{K_0} dT = \int_{T_0}^{T} \frac{K_0(\left[\frac{T}{T_0}\right]^{-1.2})}{K_0} dT \tag{2.21}$$

$$U = 5T_0^{1.2}(T_0^{-0.2} - T^{-0.2}) \tag{2.22}$$

Using equation 2.19 and 2.22,

$$5T_0^{1.2}(T_0^{-0.2} - T^{-0.2}) = \frac{QL}{K_0.A} \tag{2.23}$$

Taking partial derivative of equation 2.23 gives,

$$\left[\frac{T_0}{T}\right]^{1.2} \partial T = \frac{L}{K_0.A} \partial Q \tag{2.24}$$

Therefore the thermal resistance Rth is,

$$R_{TH} = \frac{\partial T}{\partial Q} = \frac{L}{K_0.A}\left[\frac{T}{T_0}\right]^{1.2} \tag{2.25}$$

Equation 2.1 can be written as,

$$T = T_A + (R_{TH} \times P) \tag{2.26}$$

Substituting equation 2.26 in equation 2.25, it becomes a non-linear equation in R_{TH} which can be solved for getting the value for R_{TH}.

2.2.4 Thermal capacitance in one-dimension

In equation 2.11 the last term, $\rho c \frac{\partial T}{\partial t}$ represents the time varying portion of the heat flow. In one dimension the thermal capacitance is expressed as [14]

$$C_{TH} = c_P \rho V \tag{2.27}$$

where c_P is the specific heat, ρ is the density and V is the volume of the material. The units are W-s/Kg-K for c_P, kg/m^3 for ρ and m^3 for V.

2.3 Summary

Different thermal terms are defined and the equation for the thermal resistance and capacitance is derived. The dependence of the thermal resistance on temperature is discussed and the thermal resistance equation is derived considering this variation. This equation can be used to model R_{TH} as a function of temperature and to develop methods to measure R_{TH} considering the variation of its value with temperature.

CHAPTER 3

MODELING OF HBTs

3.1 Introduction

A transistor model is supposed to mimic the transistor's terminal behavior for any biasing condition, excitation and ambient temperature. It assists the designer in understanding transistor operation in a given circuit. But the model itself, often provided by a third party such as a foundry, is often inadequate.

Most transistor models fall in one of the four categories.

3.1.1 Physics based Models

Physics based models are the most accurate models. They are based on exact knowledge of the device dimensions, doping profiles, etc. The model itself is built on the device material properties like the drift-diffusion equations, the Schrodinger equation, and thermal diffusion equations often in three dimensions. Model errors are caused by such things as the traps in the crystal lattice. An example of a physical model is given in [15].

The main advantage with this kind of model is high accuracy so that it describes almost exactly the physical behavior of the device. The main disadvantages with this kind of model are large simulation time and lack of known physical details. Typical simulation time for one single device, biased at one operating point can be several hours. In a circuit with multiple components, the simulation time becomes impractical even with the fastest computers today. The circuit designer does not usually have the necessary details of a particular process to use physical models. Usually foundries and manufactures do not want to give out such detailed information of their processes.

3.1.2 Physics Based Analytical Models

Physics based analytical models are the commonly used approach in today's modeling. This approach mainly consists of four different steps. 1) Study the physical properties of the device. 2) Analytically solve the device equations. 3) Simplify the solutions by removing the discontinuities in the functions involved and its derivatives, in such way that the final equations are easily solved on a computer. 4) Create a circuit model which describes the analytical solutions.

Usually, for a bipolar transistor, a one-dimensional representation can be a good approximation to the intrinsic behavior of a real device. Using several assumptions, these equations can be simplified resulting in ordinary differential equations and solutions obtained using the boundary conditions. Using this approach, a circuit model can be found by combining several nonlinear resistors, capacitors and controlled current and voltage sources. Two good examples of this kind of modeling are the Ebers-Moll model [16] and the Gummel-Poon model [17].

Many modern device models have been invented using the four steps explained above, for example, HICUM (High Current Model) [18-20], Philips MEXTRAM [21], and VBIC-95 (Vertical Bipolar Intercompany) model [22].

The main advantages with this kind of models are short simulation time and accuracy. The analytical equations are easily solved on computers. Complete circuits with many active and passive components can be simulated within minutes. It is also easy to understand the behavior of models which are built up this way. Also they usually have good accuracy in the operating area where the model is valid.

However the validity of the model depends on the validity of the physical analysis of the device and the validity of all the approximations made during the process to derive the final circuit model. Examples of this are limited bandwidth and the limited signal levels where the model can be used.

3.1.3 Black Box Analytical Models

The ‘black box’ model is based on empirical measurements. The relationships between the input and output responses to known excitation are described by a set of mathematical equations.

The main advantage with this kind of model is short simulation time since the mathematical equations are easily solved on computers. The ‘black box’ model is very useful when the structural layout and composition of the device is unknown.

The main disadvantage with this kind of model is the lack of physical parameters so that it cannot give direct physical explanations of device properties. Also the validity of the model depends on how the mathematical equations fit to the data from devices. Theoretically, one should use an infinite number of responses to ensure a valid model for all possible kinds of excitations.

3.1.4 Table based models

The look up table model use tabular data instead of analytical equations. The tabular data are usually obtained by measurements. The model uses a data table to store the complete measurement data sets. Since the measurement cannot cover the entire range of operation, this method relies on interpolation to get the required model values. Reference [23] shows an example of this model type.

The main advantage with this kind of model is a short simulation time. The simulations can be very fast, due to the use of look up tables. Also the model is process independent. Almost any device can be modeled with this model, as long as all the necessary measurements can be made. The accuracy depends on how detailed the measurements are, and how well-behaved the device is.

The main disadvantage with this kind of models is the lack of physical parameters and it cannot give direct physical explanations of device properties. Also the measurements may get

very complex and might require specialized measurement equipment to find certain properties of the device.

3.2 Choice of Model

The model must be chosen to satisfy the application in which it is used. As discussed in the previous chapters, this thesis paper deals with the self heating of transistors. Hence the choice of model is dependent on the following factors:

a) A model that would be helpful in characterizing the self-heating of a transistor.

b) A model that would be supported by the software tools ICCAP and Cadence which have been used extensively in this research work for thermal characterization.

c) A model that has strong historical precedence.

Taking all this in to consideration, a physics based analytical model, VBIC is chosen for this thesis.

3.2.1 The VBIC Model

The VBIC model [22] was developed by a consortium of large companies in the BJT industry like Motorola, Texas Instruments, Analog Devices, Hewlett-Packard, IBM, etc. The main purpose of making this model was to look at all published models at that time, and select the best feature from them all. The result was the VBIC model. The model is an open source model with all information publicly available. Figure 3.1 shows the schematic of the VBIC model.

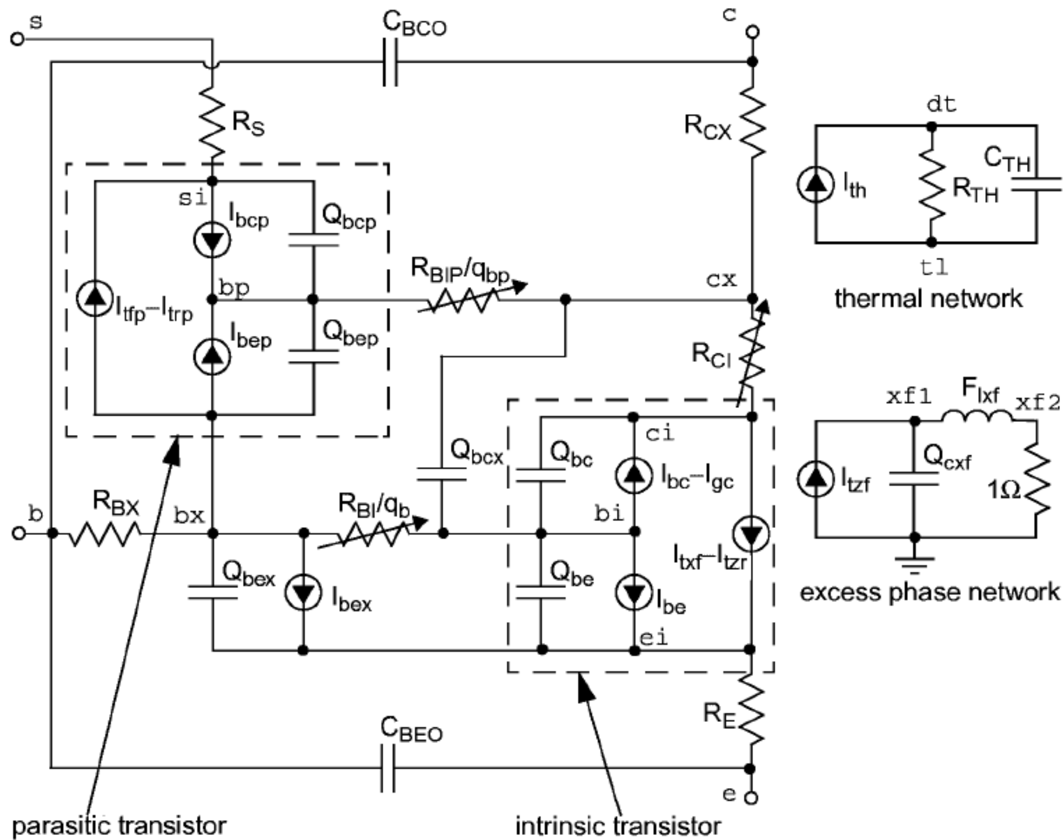

Figure 3.1 Schematic of the VBIC model [22].

The VBIC model is based on Gummel Poon (GP) model. Basic improvements in VBIC over GP include [31] modeling of self heating which was not present in GP, separation of I_c and I_b without being empirically related through β_F, full parasitic PNP modeling, Early effect modeling based on depletion charge, constant overlap capacitances, base emitter break down modeling and improved depletion and diffusion charge models. The VBIC model is discussed in detail by [24]. The VBIC model was originally made for silicon BJT's, but it has all the necessary features needed for modeling an HBT.

3.2.1.1 Temperature parameters in VBIC

VBIC has several temperature parameters. The parameters which model the self heating are R_{TH} and C_{TH}. The major temperature dependent parameter is the saturation current I_S. The other temperature parameters include temperature exponent X_{IS} of the forward

saturation current I_S, the temperature exponent X_{II} of the saturation currents I_{BEI}, I_{BCI}, I_{BEIP}, $I_{BCIP,}$ the temperature coefficient T_{NF} of N_F, temperature exponents of the base, collector and emitter resistances X_{RB}, X_{RC}, and $X_{RE,}$ temperature coefficient T_{AVC} of the base collector weak avalanche parameters A_{VC1} and A_{VC2} and temperature exponent X_{VO} of the epitaxial drift saturation voltage V_o.

At normal operating temperatures only $R_{TH,}$ C_{TH} and I_S plays a significant role and the temperature dependence of all other parameters are negligible. Since this thesis paper is on the self heating of devices, concentration has been given to extract R_{TH} and C_{TH} of the HBT device. For this work, different methods have been used from physics based models and physics based analytical models. In this chapter two such methods are introduced. In the first method Masana's equations [25] have been used to calculate the thermal resistance and thermal capacitance of the device from the knowledge of the device structure and the materials used to fabricate it. In the second method Joy and Schlig's [27] equations have been used to get the time dependent temperature response of the device from which the thermal resistance and thermal capacitance is calculated by optimization in Matlab. The fourth chapter introduces a DC based technique to estimate thermal resistance and the fifth chapter explains a time domain method to get the thermal resistance and thermal capacitance values.

3.3 Masana's method [25]

During the initial stages of the design when the details of the system to be designed are not well known, simulators are of little help. Instead, estimation methods using the structure of the system and its thermal behavior are advantageous due to the immediate availability of the results. The physics based models which depend on the solution of numerous complex equations, which are again dependent on different boundary conditions, takes a long time to be solved and does not convey any useful information about the geometry of the system. The model presented here overcomes these limitations. Masana's method has been used here to

model the thermal behavior of the device. The description and the equations used in the section 3.3.1 have been taken from [25].

3.3.1 Derivation of expressions for R_{TH} and C_{TH}

The time dependent equation for the conduction of heat in a solid is given by

$$\nabla^2 T = \frac{1}{\alpha_p}\frac{\partial T}{\partial t} \qquad (3.1)$$

where T is the temperature, α_p is the thermal diffusivity at constant pressure and ∇^2 stands for the Laplacian operator,

$$\nabla^2 = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}$$

In the electric domain, the corresponding basic equation for the potential is the wave equation

$$\nabla^2 V = \frac{1}{v^2}\frac{\partial^2 V}{\partial t^2} \qquad (3.2)$$

where v is the velocity of potential waves and V is the potential.

The difference between the two equations is that the heat diffusion equation has a dependence on the first derivative with respect to time, while the wave equation has a dependence on the second derivative with respect to time. This means that in the electric equivalent circuit there will be two different types of reactive elements, while in the thermal equivalent circuit there will be only one. There is a resistance to heat flow through a medium, related to its thermal conductivity which corresponds to its thermal resistance. There is also heat storage within the medium that is related to its heat capacity. This corresponds to its thermal capacitance. There is nothing similar to the magnetic field in heat transfer, so there is no thermal inductance.

To formalize the method to calculate Rth, consider a volume with constant cross-section, S. Assume a constant temperature across S, constant and uniform heat flux q across S, zero heat flux outside the volume and a steady state condition.

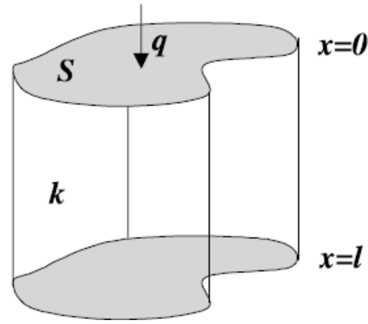

Figure 3.2 Volume for the calculation of thermal resistance [25].

Integrate equation 3.1 in one-dimension, find the constant of integration using the boundary conditions and then applying the condition of constant flux through S gives [25]

$$\frac{dT}{dx} = -\frac{q}{k} \tag{3.3}$$

where k is the thermal conductivity of the medium. The rate of heat input to the volume is W=qS. Integrating Equation 3.3 and substituting for q as q=W/S gives

$$\frac{T_0 - T_l}{W} = \frac{l}{kS} = R_{TH} \tag{3.4}$$

where T_0 and T_l are the temperatures at x=0 and x=*l* respectively. That is the thermal resistance between any two isothermal surfaces can be obtained, by solving equation 3.1 subject to the applicable boundary conditions and dividing the temperature difference by the rate of heat flow between the surfaces.

The integration is performed along a path of length l with a cross-section S. The relevant characteristic of the medium filling the volume is the thermal conductivity k. Thermal capacity is a magnitude associated with heat storage and accordingly the integration has to be performed for the volume V=lS, with the heat capacity c_p as the relevant characteristic of the medium filling that volume. With these considerations [14]

$$C_{TH} = V\rho c_p \tag{3.5}$$

where ρ is the density of the medium with units kg/K, V is the volume in m^3 , and c_p is the specific heat with units J/Kg-K.

A transistor made out of different layers of materials can be represented by an equivalent RC network. Each RC cell represents a layer and according to the variable angle method (VAM) [26], its thermal resistance is calculated using the volume sketched below. The heat source, its projection on the next layer boundary and the edges defined by the spreading angles α_1, α_2, β_1 and β_2 delimit this volume as shown in figure 3.3. These angles are associated with the source dimensions x and y respectively. In the general case, the spreading is different for each side of the heat source according to its placement with respect to substrate.

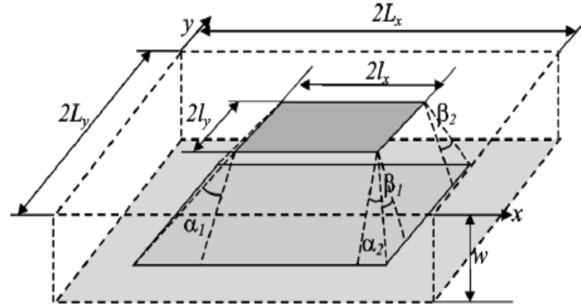

Figure 3.3 Volume for applying VAM [25].

Using equation 3.4 the thermal resistance for that particular volume is given by [25]

$$R_{TH} = \frac{1}{k}\int_0^w \frac{dz}{[(l_x + z\ tan\alpha_1)+(l_x + z\ tan\alpha_2)][(l_y + z\ tan\ \beta_1)+(l_y + z\ tan\beta_2)]} \tag{3.6}$$

After integration [12]

$$R_{TH} = \frac{1}{4kl_x}\frac{1}{(\gamma_e \tan\alpha - \tan\beta)}\ ln\frac{l_x + w\ tan\ \alpha}{l_x + w\ tan\ ^{\beta}/_{\gamma_e}} \tag{3.7}$$

where $\gamma_e = l_y/l_x$ and $\gamma_s = L_y/L_x$ are the aspect ratios of the heating element and substrate respectively. The spreading angles are given by [25]

$$(\tan\alpha)_i = \frac{(\tan\alpha_1 + \tan\alpha_2)_i}{2} = \left(1 + \frac{1-\rho_L}{1+\rho_L}\frac{l_{xn}}{\varepsilon_x{}^2}\right)\frac{w_n + [\rho_s/(1+\rho_s)]l_{xn}}{w_n + [1/(1+\rho_s)]l_{xn}}\Bigg|_i$$

$$(\tan\beta)_i = \frac{(\tan\beta_1+\tan\beta_2)_i}{2} = \left(1+\frac{1-\rho_L}{1+\rho_L}\frac{l_{xn}}{\varepsilon_y{}^2}\frac{\gamma_e}{\gamma_s}\right)\frac{w_n+[\rho_s/(1+\rho_s)]l_{xn}\gamma_e}{w_n+[1/(1+\rho_s)]l_{xn}\gamma_e}\Bigg|_i \quad (3.8)$$

where its boundary dependence comes through ρ_s and ρ_L which are constants used in equations 3.6 and equation 3.8. ρ_s and ρ_L are defined as

$$\rho_s = \frac{k_i}{k_{i+1}}; \rho_L = \frac{k_i}{k_L} \quad (3.9)$$

where K_i and k_{i+1} represent the thermal conductivity of the present and the next layer respectively and k_L represents the thermal conductivity of the lateral boundary of the system.

The dependence on system geometry comes through the aspect ratios γ_e and γ_s, the normalized dimensions $l_{xn}=l_x/L_x$ and $w_n=w/L_x$ and the eccentricity parameters that take into consideration the source to substrate offset [25].

$$\varepsilon_x = \frac{\sqrt{L_{x1}L_{x2}}}{L_x}; \varepsilon_y = \frac{\sqrt{L_{y1}L_{y2}}}{L_y} \quad (3.10)$$

Since it is assumed that the heat flow is confined in the volume in figure 3.3, the walls of it have to be taken as adiabatic. This approximation is valid because the influence of the outer volume will be negligible in the overall heat conduction. Consequently, the same volume considered for the calculation of thermal resistance has to be used for the calculation of thermal capacitance in equation 3.5. The volume is given by [25]

$$V = 4\left[l_x l_y w + (l_x \tan\beta + l_y \tan\alpha)\frac{w^2}{2} + \tan\beta\tan\alpha\ \frac{w^3}{3}\right] \quad (3.11)$$

Since the expressions forming R_{TH} and C_{TH} are closed form equations, a spreadsheet has been used to perform the calculations.

3.3.2 Electric Circuit Representation

As mentioned above the device made out of layers of different materials can be represented by an equivalent RC network. Figure 3.4 gives the most common circuit representations, Foster and Cauer networks.

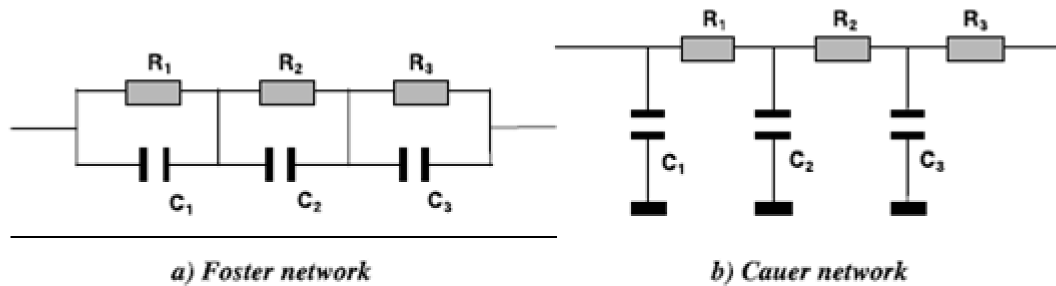

Figure 3.4 Foster and Cauer network representation [25].

In the Foster network, the time constants coincide with the RC products of each section. In the Cauer network, each time constant depends on all the R's and C's of the circuit, so determining the R and C values from time constants is not straight forward. Since either the Foster or Cauer network can be derived from identical driving point impedance, conversion from one to other is always possible.

Despite that, a given time constant set can be uniquely represented in the same way by each of the two circuits, it must be pointed out that the circuit form which is suitable for faithfully representing the system from the physical point of view is just the Cauer one. In an electrical circuit, the effective flow of ac current through a capacitor is by the accumulation of equal and opposite charges on its plates. In a thermal system heat flows only in one direction. There is no negative heat particle. Hence in the thermal regime there is no entity corresponding to the negative charges in electrical circuits. In the R_{TH}, C_{TH} representation of thermal circuits all the capacitors must be connected to a common reference ground [28].

This implies that the electro-thermal analogy is valid only for the Cauer network. Each time constant of the thermal transient depends on all the resistances and capacitances. For this reason it is theoretically incorrect to establish a direct correspondence between a certain time constant of the thermal transient curve and the thermal properties of a given part of the solid.

3.3.3 Conversion of Foster network to Cauer network

First of all the input impedance expression is found for the Foster network. For example for a 3-pole Foster network the input impedance will be

$$Z_{in}(s) = \frac{R_1}{1+sR_1C_1} + \frac{R_2}{1+sR_2C_2} + \frac{R_3}{1+sR_3C_3} \tag{3.13}$$

where all the R's and C's here are of the Foster network. This can be written as,

$$Z_{in}(s) = \frac{s^2(R_1R_2R_3C_2C_3 + R_1R_2R_3C_1C_3 + R_1R_2R_3C_1C_2) +}{s^3(R_1R_2R_3C_1C_2C_3) + s^2(R_1R_3C_1C_3 + R_2R_3C_2C_3 + R_1R_2C_1C_2) + s(R_1C_1 + R_2C_2 + R_3C_3) + 1}$$

$$\frac{s(R_1R_3C_3+R_1R_2C_2+R_2R_3C_3+R_2R_1C_1+R_3R_1C_1+R_3R_2C_2)+(R_1+R_2+R_3)}{s^3(R_1R_2R_3C_1C_2C_3)+s^2(R_1R_3C_1C_3+R_2R_3C_2C_3+R_1R_2C_1C_2)+s(R_1C_1+R_2C_2+R_3C_3)+1} \tag{3.14}$$

Now the Cauer method for synthesis of passive electrical networks can be applied to the input impedance expression to get the individual circuit element values. For this the below following algorithm is used [28].

1. $i = 1,2,3$ Since here a 3- pole circuit is considered.

2. $Z_1(s) = Z_{in}(s)$

Since the denominator of Zin(s) is one order higher than the numerator, start with the admittance expression.

3. $\dfrac{1}{Z_i(s)} = sC_{i,cauer} + Y_i^{'}(s)$

4. $\dfrac{1}{Y_i^{'}(s)} = R_{i,cauer} + Z_{i+1}(s)$

5. Repeat steps 3 and 4 until the remainder is zero either for step 3 or step 4.

3.3.4 Steps involved in the thermal modeling of a device

The steps involved in modeling the thermal network of a device are mentioned below.

1. Find the R's and C's of the Foster network representation using the material property and geometry information of each layer using the method described in section 3.3.1.

2. Find the input impedance expression of the Foster network.
3. Using the Cauer method of network synthesis, calculate the R's and C's of the Cauer network representation.

3.3.5 Example

A spreadsheet has been used to calculate the R's and C's of the Foster network using Masana's method. The R's and C's for a SiGe HBT with dimensions l_x=0.125um, l_y=10um, L_x=2.22um, L_y=11.6um and w=2um calculated using this spreadsheet is given below.

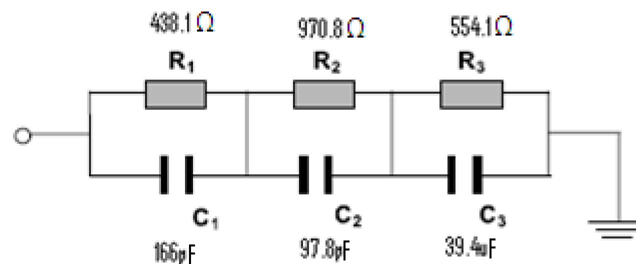

Figure 3.5 Foster network representation of thermal network for a SiGe HBT.

Now applying the Cauer method of network transformation, the Cauer network would be

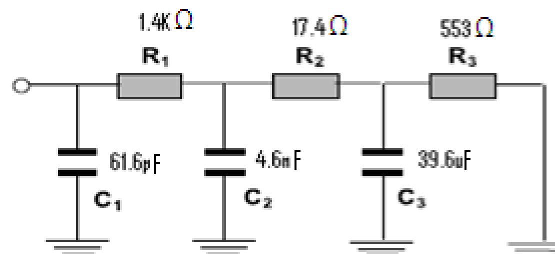

Figure 3.6 Cauer network representation of thermal network for a SiGe HBT.

In-order to verify these circuits electrical simulations are performed with a unit current step as the input. The simulation results are shown below.

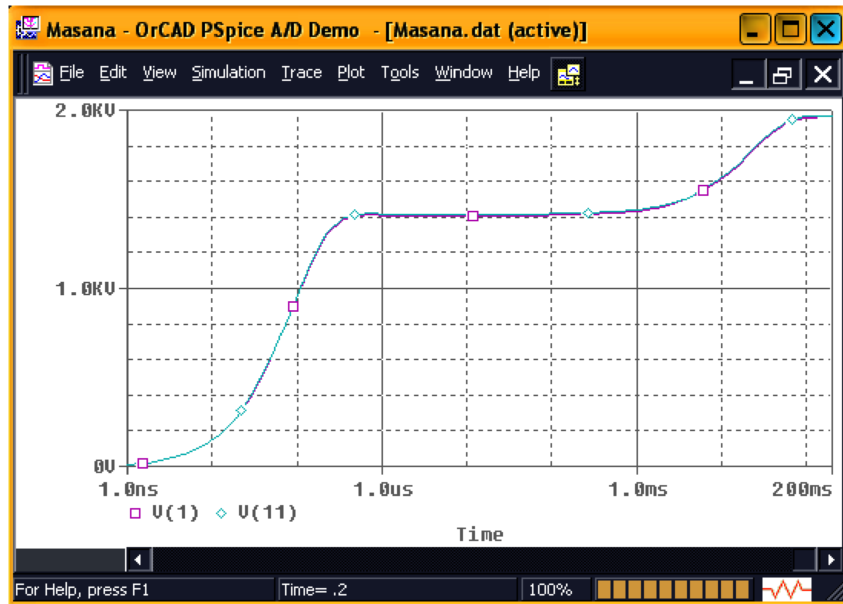

Figure 3.7 Time Response of the Foster and Cauer networks. V (1) is the Foster response and V (11) is the Cauer response.

It is clear from the above plot, a particular circuit can be represented in either Foster form or in Cauer form with same time domain response.

3.3.5.1 Comparison between calculated and measured data

The R's and C's of the Foster thermal equivalent circuit calculated for two different devices are compared with the values estimated from the measurement.

Table 3.1 Comparison between calculated R's and C's of the Foster network and measured thermal parameters for two SiGe HBT devices.

Equi. Ckt Component	5um^2 device		2.5um^2 device	
	Calculated	Measured	Calculated	Measured
R1	438.1	968.2	840.1	1180
R2	970.8	1.31E+03	1710	1320
R3	554.1	9.80E+02	496.6	4268
C1	1.66E-10	2.99E-09	9.15E-11	6.58E-07
C2	9.78E-11	3.38E-07	5.55E-11	8.90E-04
C3	3.94E-05	1.62E-06	9.52E-05	1.28E-09

3.3.5.2 Reasons for the mismatch

As it is observed from table 3.1, there is mismatch between the measured and the calculated values of thermal resistances and thermal capacitances.

The reasons for this mismatch are summarized below.

In the method used to calculate the R's and C's, adiabatic side walls have been assumed for the volume under consideration each time the R and C of a layer was found. The influence of the sidewalls will be hardly noticeable as long as the lateral substrate dimensions are a few times the base of the pyramidal flow path. But in the case of a transistor in some layers lateral substrate dimensions are comparable to the dimensions of the base of the pyramidal flow path [29].

In defining the thermal resistance between two isothermal surfaces as the quotient of the temperature difference between the surfaces and the rate of heat flow between the surfaces, two limitations are implicit. First, the thermal resistance has to be calculated between iso-thermal surfaces, and second the heat that flows into the first surface has to flow out through the second surface. In reality both the surfaces are not iso-thermal and not all power flowing through the first surface flows out through the second surface, since certain amount goes out through additional conductive heat flow paths.

The thermal conductivity is a function of temperature. In practice there might be hot spot formation. A hot spot is formed when high power is dissipated and the current concentrates into a small area. Thus, the effective area is reduced and the thermal resistance increases [30].

It is also assumed that the bottom of the substrate is at a fixed reference temperature. In practice, various situations can occur like poor bottom cooling will result in wider heat spreading. The model will therefore be largely dependent on the actual boundary conditions.

3.4 Joy and Schlig Thermal Resistance

Reference [27] presents a mathematical model of the three dimensional transient heat flow which takes into account the physical structure of the device and the actual region of power dissipation. At any point within the device, the model predicts the time-dependent temperature response to a power dissipation as a function of time.

3.4.1 Model description

Several assumptions are made regarding the structure of the device. The effect of all chip boundaries except the one closest to the device is neglected. The surface of the chip may be considered to be adiabatic. This permits using symmetry in the real medium which is a semi-infinite homogeneous half space for analysis.

The source of power dissipation in a bipolar transistor is mainly in that part of the collector base depletion region that carries the bulk of the injected current. This region of power dissipation is approximated by a solid rectangular parallelepiped submerged beneath the surface of the semi-infinite medium as shown below.

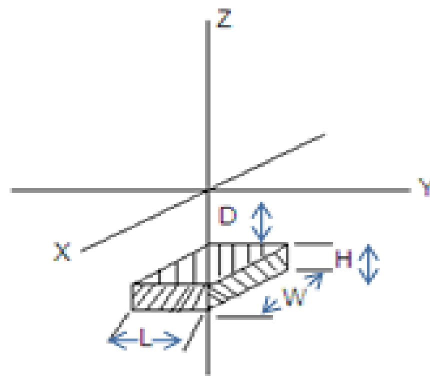

Figure 3.8 Heat source, simulating transistor power dissipation located below the surface of a semi-infinite medium [27].

The volume in which the power is dissipated is shown as the shaded region of dimensions $L \times W \times H$ located at a depth D below the surface. For a transistor L and W would

correspond to the length and width of the emitter stripe, H the approximate thickness of the depletion region and D the depth of the collector base depletion junction below the surface.

First finding an expression for temperature for an instantaneous point source and then integrating it throughout the volume of heat source, the increase in temperature at any point in the semi-infinite medium to a step increase P in the power dissipation at time=0 is given by [27]

$$T(x,y,z,t) = \frac{P}{8C}\int_0^t \left[erf\left(\frac{W/_2+x}{\sqrt{4ku}}\right) + erf\left(\frac{W/_2-x}{\sqrt{4ku}}\right)\right].\left[erf\left(\frac{L/_2+y}{\sqrt{4ku}}\right) + erf\left(\frac{L/_2-y}{\sqrt{4ku}}\right)\right].\left[erf\left(\frac{z+D+H}{\sqrt{4ku}}\right) + erf\left(\frac{-D-z}{\sqrt{4ku}}\right) + \left[erf\left(\frac{z-D}{\sqrt{4ku}}\right) + erf\left(\frac{D+H-z}{\sqrt{4ku}}\right)\right]\right]du \quad (3.15)$$

where C=ρcV and V=L×W×H, in which ρ represents the density of the solid and c represents the specific heat of the solid.

The thermal resistance which is a function of position is the ratio of the final value of the temperature increase to the power dissipated.

$$R_{TH}(x,y,z) = T(x,y,z,\infty)/_P \quad (3.16)$$

3.4.2 Simulations

Matlab is used to plot equation 3.15. The integration is performed by dividing the area under the graph into a number of rectangles and the code is written to calculate the sum of the areas of those rectangles. A 5 um^2 device is considered here.

1. The thermal response at the centre of the emitter area for a 5 um^2 SiGe HBT device is plotted using equation 3.16 in figure 3.9.

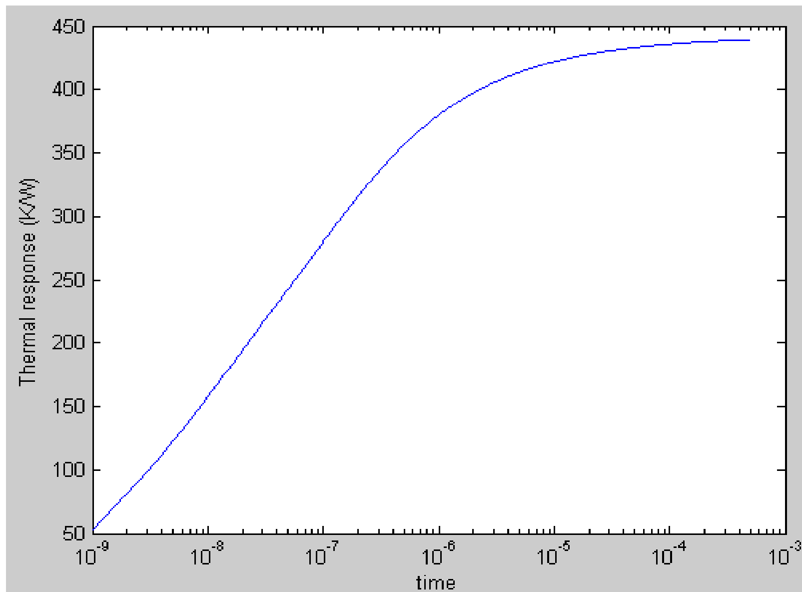

Figure 3.9 Matlab simulation of thermal response at the centre of the emitter.

The simulated curve is fitted with a 3-pole electrical impedance expression to get the R_{TH} and C_{TH} values.

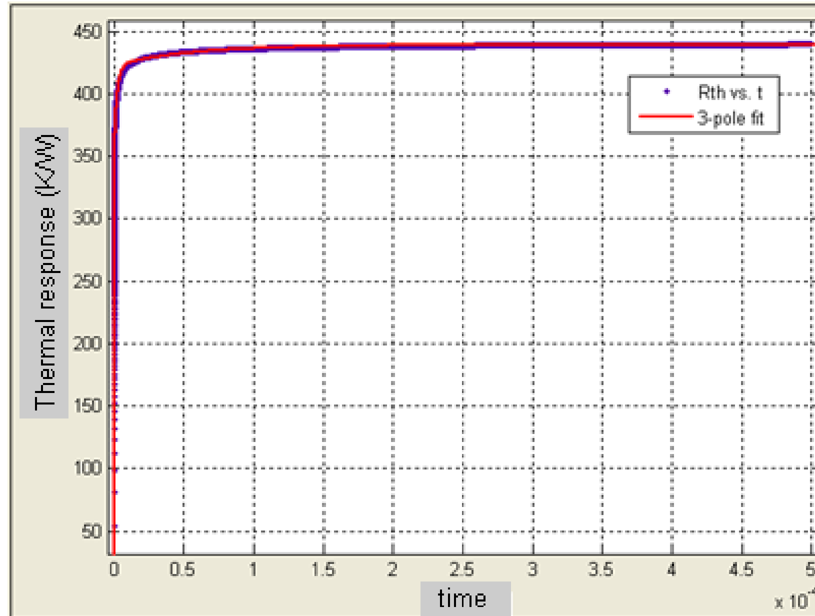

Figure 3.10 The curve in figure 3.9 is fitted with a 3-pole expression using the curve fitting tool in Matlab.

Table 3.2 Calculated pole values for the curve in figure 3.10

	Pole-1	Pole-2	Pole-3
R	342.4	80	16.29
Tau	5.20E-08	2.66E-06	5.47E-05

2. The thermal response at the edge of the emitter area for a 5 um^2 SiGe HBT device is plotted using equation 3.16 in figure 3.11.

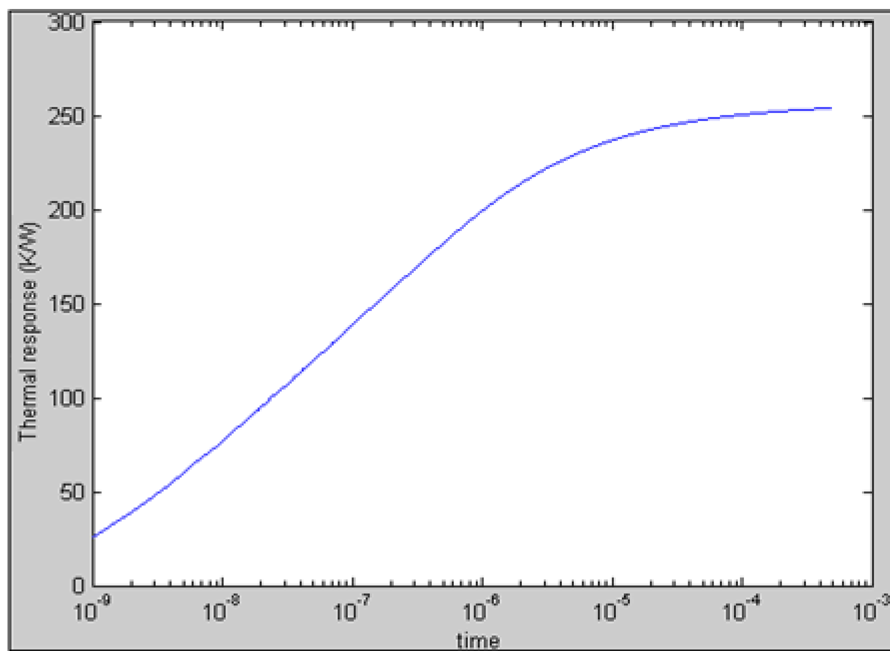

Figure 3.11 Matlab simulation of thermal response at the edge of the emitter.

The simulated curve is fitted with a 3-pole expression to get the R_{TH} and C_{TH} values.

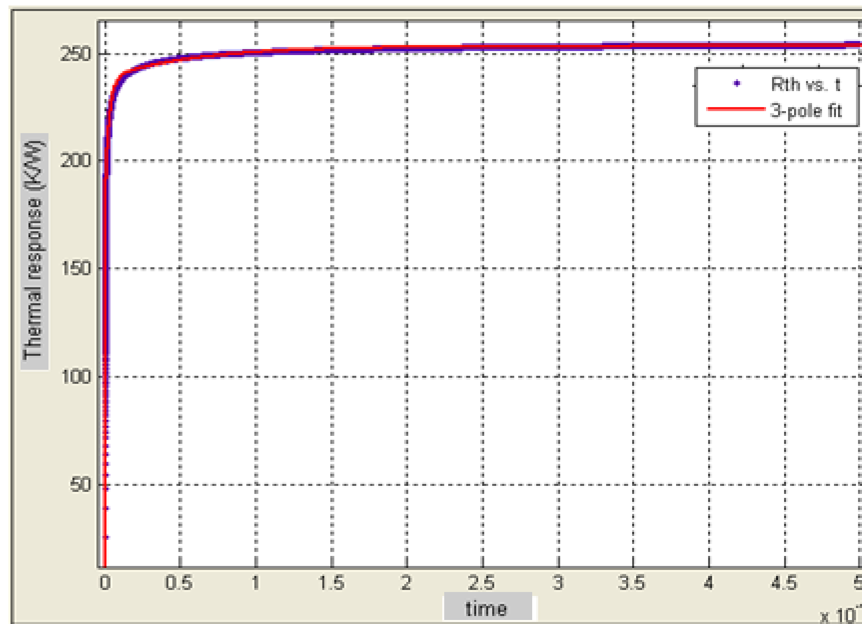

Figure 3.12 The curve in figure 3.11 is fitted with a 3-pole expression using curve fitting tool in Matlab.

Table 3.3 Calculated pole values for the curve in figure 3.12

	Pole-1	Pole-2	Pole-3
R	174.7	63.55	15.15
Tau	5.70E-08	2.60E-06	5.90E-05

3.5 Summary

This chapter discussed the different types of modeling a transistor. Two methods of finding the thermal resistance and capacitance of an HBT device is introduced and verified using calculations and simulations.

CHAPTER 4

DC METHOD FOR THERMAL RESISTANCE MEASUREMENT

4.1 Introduction

Thermal resistance is a critical parameter which determines the HBT operating temperature and thereby influences the transistor performance through the temperature dependence of various parameters. As is discussed in the previous chapters thermal resistance is defined as the ratio of the excess temperature due to self-heating to the dissipated power. Since it is not possible to access the junction temperature directly, thermal resistance has to be estimated from its impact on electrical properties.

How the thermal resistance is determined depends on the requirements. If it is to be used as a model parameter for a small HBT, a constant value is sufficient. But in the case of thermally critical large scale HBTs, or if thermal interaction plays a critical role, a thermal admittance matrix or a non-linear thermal resistance may be necessary.

There are several ways to determine the thermal resistance of an HBT. In this thesis paper two different methods have been used to get the thermal resistance values of SiGe HBTs using the measured data from real devices. The first is a DC method which is explained in this chapter and the second is a time-domain measurement based method which is discussed in the next chapter.

4.2 Bovolon's method

The first method is based on [32]. The decrease of V_{be} with temperature is a well known characteristic in all bipolar transistors [33]. Since V_{be} of the transistor varies linearly for a wide range of temperatures; the change of V_{be} for a small change in junction temperature, T_j, around the value T_{j1} can be written as follows.

$$V_{be}(T_j) = V_{be}(T_{j1}) + \frac{\Delta V_{be}}{\Delta T_j}\bigg|_{T_{j1}} (T_j - T_{j1}) \tag{4.1}$$

The junction temperature of a device can be written as

$$T_j = T_0 + (R_{TH} \times P) \tag{4.2}$$

where P is the power dissipated which can be written as $P=V_{ce}I_c+V_{be}I_b$ and T_0 is the substrate temperature.

Using this in equation 4.1, the linear dependence of V_{be} on temperature can be written as [34,35]

$$V_{be}(T_0, P_{diss}) = V_{be}(T_{j1}) + \frac{\Delta V_{be}}{\Delta T_j}\bigg|_{T_{j1}} (T_0 + R_{TH} \times P_{diss} - T_{j1}) \tag{4.3}$$

Equation 4.3 can be written for two different substrate temperatures but with the same power dissipation as follows.

$$V_{be}(T_1, P_{diss1}) = V_{be}(T_{j1}) + \frac{\Delta V_{be}}{\Delta T_j}\bigg|_{T_{j1}} (T_1 + R_{TH} \times P_{diss1} - T_{j1}) \tag{4.4}$$

$$V_{be}(T_2, P_{diss1}) = V_{be}(T_{j1}) + \frac{\Delta V_{be}}{\Delta T_j}\bigg|_{T_{j1}} (T_2 + R_{TH} \times P_{diss1} - T_{j1}) \tag{4.5}$$

Equation 4.3 can be written for two different power dissipations but at the same substrate temperature as follows.

$$V_{be}(T_1, P_{diss1}) = V_{be}(T_{j1}) + \frac{\Delta V_{be}}{\Delta T_j}\bigg|_{T_{j1}} (T_1 + R_{TH} \times P_{diss1} - T_{j1}) \tag{4.6}$$

$$V_{be}(T_1, P_{diss2}) = V_{be}(T_{j1}) + \frac{\Delta V_{be}}{\Delta T_j}\bigg|_{T_{j1}} (T_1 + R_{TH} \times P_{diss2} - T_{j1}) \tag{4.7}$$

Subtracting equation 4.5 from equation 4.4, an expression for $\frac{\Delta V_{be}}{\Delta T_j}\Big|_{T_{j1}}$ can be obtained.

Subtracting equation 4,7 from equation 4.6 and substituting this value for $\frac{\Delta V_{be}}{\Delta T_j}\Big|_{T_{j1}}$ an expression for R_{TH} can be obtained. Hence thermal resistance, R_{TH}, can be written as

$$R_{TH}(P_{diss1}) = \left(\frac{V_{be}(T_1,P_{diss1}) - V_{be}(T_1,P_{diss2})}{P_{diss1} - P_{diss2}}\right) \Bigg/ \left(\frac{V_{be}(T_1,P_{diss1}) - V_{be}(T_2,P_{diss1})}{T_1 - T_2}\right) \quad (4.8)$$

The difference in temperature and power in doing measurements to calculate R_{TH} must be kept small enough so that the interpolation is valid. This method neglects the Early effect, quasi-saturation and the avalanche multiplication effects [32].

4.3 Temperature measurement

The junction temperature is calculated using reverse Gummel measurements. This configuration has been selected for the temperature calculation since the collector region is more lightly doped than the emitter region. The transistor equation for the reverse Gummel configuration for low level injection can be written as,

$$I_E = I_S\left(exp\,\frac{V_{bc}}{\eta\, V_T} - 1\right) \quad (4.9)$$

Hence

$$V_{bc} = \eta\, V_T ln\frac{I_E}{I_S} \quad (4.10)$$

where V_T=kT/q, in which k is the Boltzmann constant, T is the temperature, η is the ideality factor and q is the electron charge.

When both sides of equation 4.10 are differentiated

$$dV_{bc} = \eta\, V_T d(ln\, I_E) \quad (4.11)$$

Hence temperature T can be written from equation 4.11 as,

$$T = \frac{q}{\eta\, k}\frac{d(V_{bc})}{d(ln\, I_E)} \quad (4.12)$$

An additional shunt current, V_{bc} / R_{shunt} can be added to equation 4.9. The calculation obtained from equation 4.12 yields an effective temperature. A plot of this effective temperature versus V_{bc} gives a parabola. The ideality factor is assumed to be one in this plot. Since at the

minimum of this parabola, the first derivative would be zero, the value of the ideality factor is at its minimum which will be closest to the assumption made. Hence the minimum point of this parabola gives the best estimation of the junction temperature [36].

4.4 Measurement results

The measurements have been performed on 5 um^2 and 2.5 um^2 SiGe HBT devices from National Semiconductors. The wafers are probed using Cascade Infinity probes with 150 um pitch. An Agilent 4142 DC source, which can be controlled using ICCAP software, has been used in the measurements.

4.4.1 Step by step procedure for thermal resistance calculation using the DC method.

Following are the steps involved:

1. The forward Gummel measurements are done to check the device by verifying the currents and beta. (Figure 4.3)
2. The junction temperature is measured using the reverse Gummel setup. (Figure 4.1)
3. The output characteristics and the power plots are made using the common emitter configuration.
4. The junction temperature of the device is increased using an external heat source.
5. Steps 1 to 3 are repeated for the increased temperature.
6. Thermal resistance is calculated using equation 4.8.

4.4.2 Plots and circuit diagrams

4.4.2.1 Temperature measurement

As discussed in section 4.3 a reverse Gummel setup is used for temperature measurement.

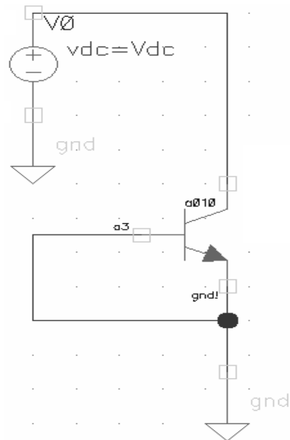

Figure 4.1 Reverse Gummel set up for temperature measurement.

The emitter and base are connected together and shorted to ground. The collector voltage is varied from -350 mV to -800 mV. The reverse Gummel measurements are done and estimated temperature is plotted using equation 4.12.

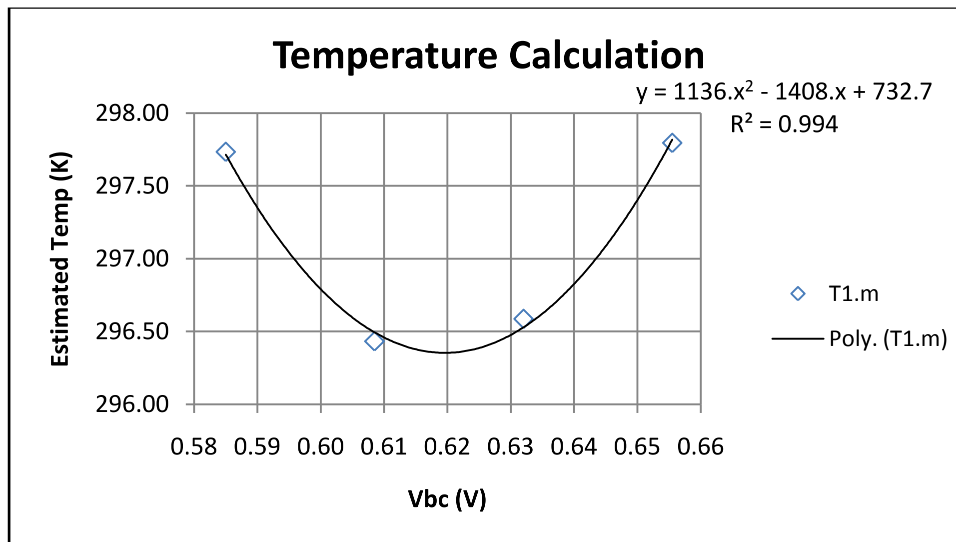

Figure 4.2 Plot of estimated temperature for a 5 um^2 device. Only the points used for curve fitting to a parabola is shown.

From the above plot the junction temperature is assumed to be the minimum of the parabola which in this case is 296.4°K (T_1). A similar plot is made after heating the device using an external source to get the elevated temperature T_2.

4.4.2.2 Forward Gummel measurement

The forward Gummel measurements are done in order to verify the functionality of the device.

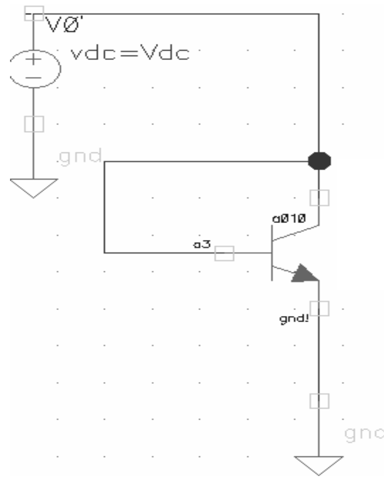

Figure 4.3 the forward Gummel set up.

The collector and base is connected together and the voltage is varied from 400 mV to 900 mV. The forward Gummel plots for the two temperatures are given below. The error observed in the very low current region is due to the accuracy limitation of the measurement setup.

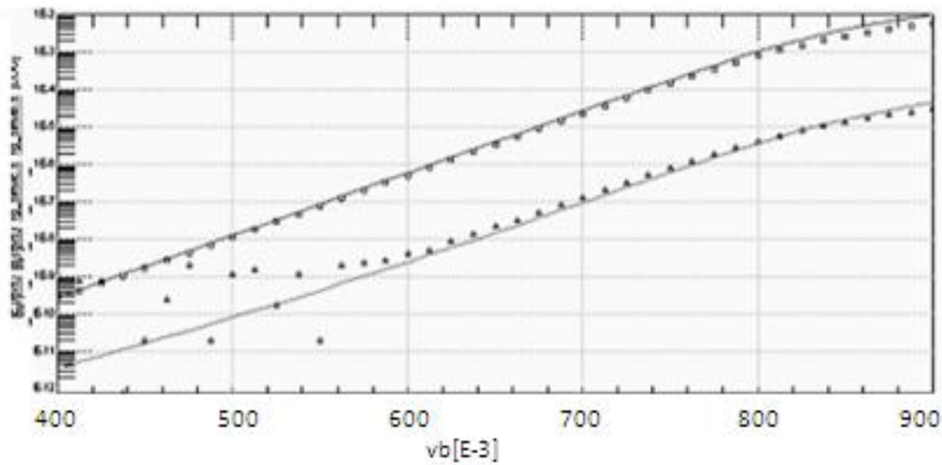

Figure 4.4 Forward Gummel plot at temperature T_1 for a 5 um^2 device. Continuous line is simulated data using ADS; Data symbols are measured data

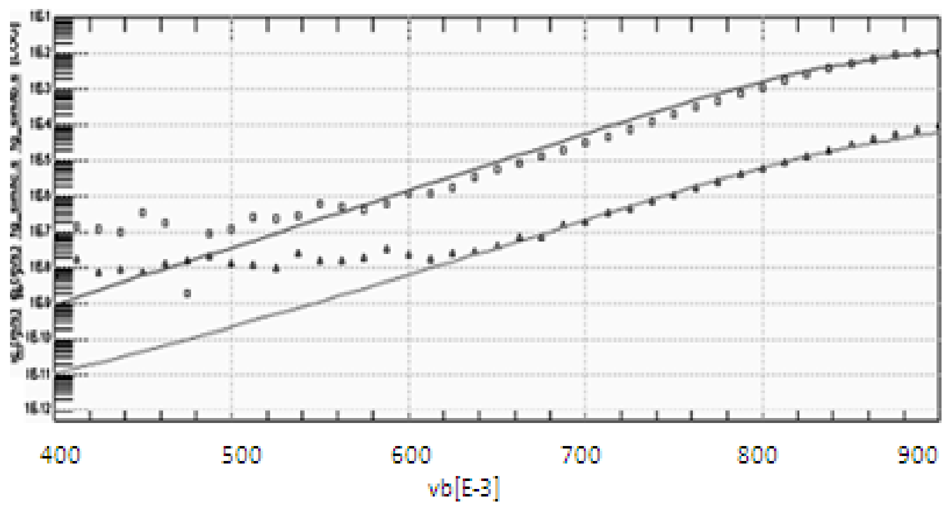

Figure 4.5 Forward Gummel plot at temperature T_2 for a 5 um^2 device. Continuous line is simulated data using ADS; Data symbols are measured data

4.4.2.3 Common emitter measurement

The circuit set up used for common emitter measurements is shown in figure 4.6.

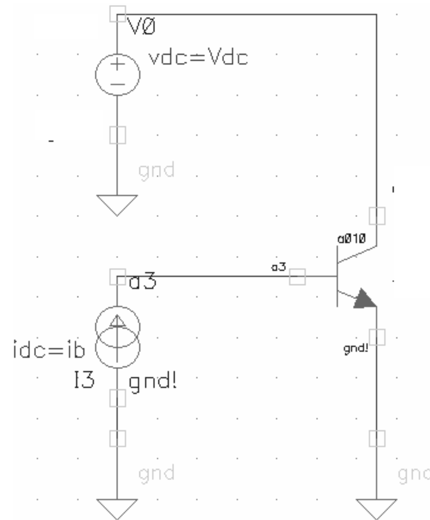

Figure 4.6 the common emitter set up.

A constant current source is used to set the base current to a desired value. It is varied from 20 uA to 50 uA in 10 uA steps. The I_c vs V_{ce}, V_{be} vs V_{ce} and the Power vs V_{ce} plots are shown below. The values of V_{be}, V_{ce} and power from these measurements are used in equation 4.8 to calculate the value of thermal resistance.

I_c vs V_{ce} plots:

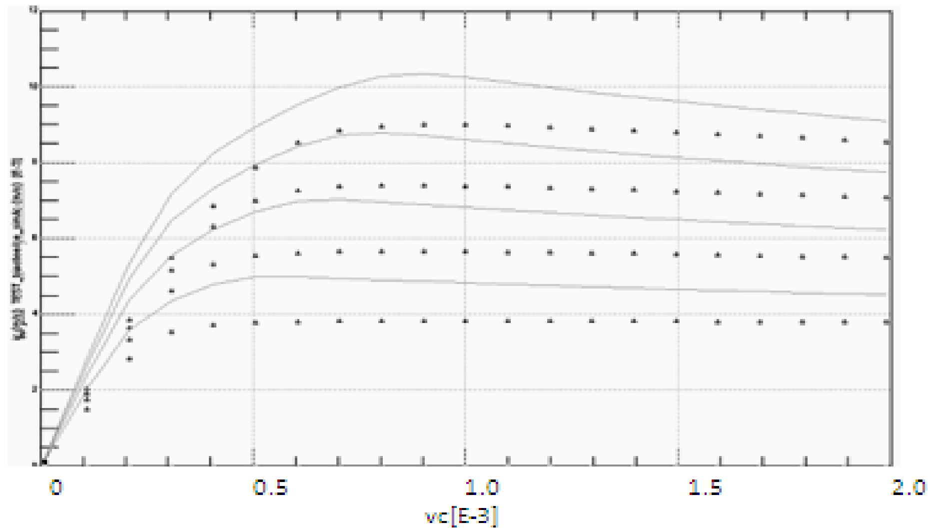

Figure 4.7 Common emitter I_c vs V_{ce} plot at temperature T_1 for a 5 um^2 device. Continuous line is simulated data using ADS; Data symbols are measured data Ib = 20uA, 30uA, 40uA, 50uA

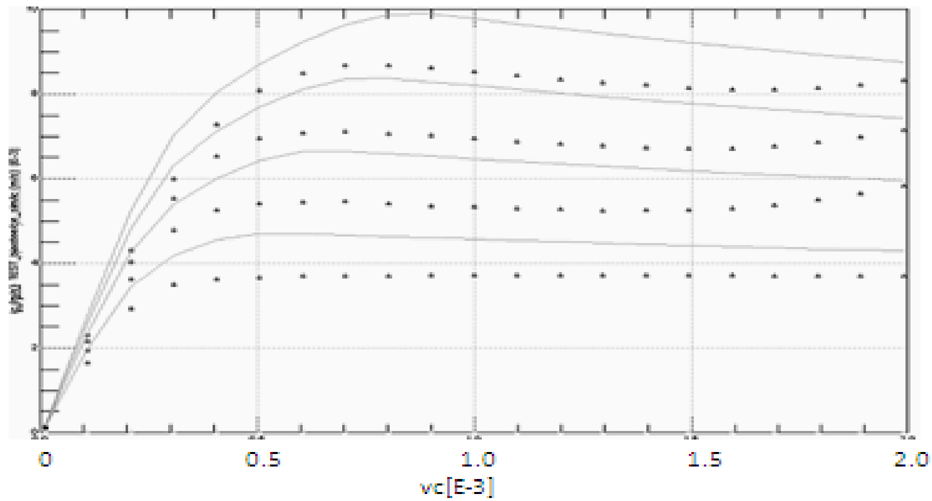

Figure 4.8 Common emitter I_c vs V_{ce} plot at temperature T_2 for a 5 um^2 device. Continuous line is simulated data using ADS; Data symbols are measured data Ib = 20uA, 30uA, 40uA, 50uA

V_{be} vs V_{ce} plots:

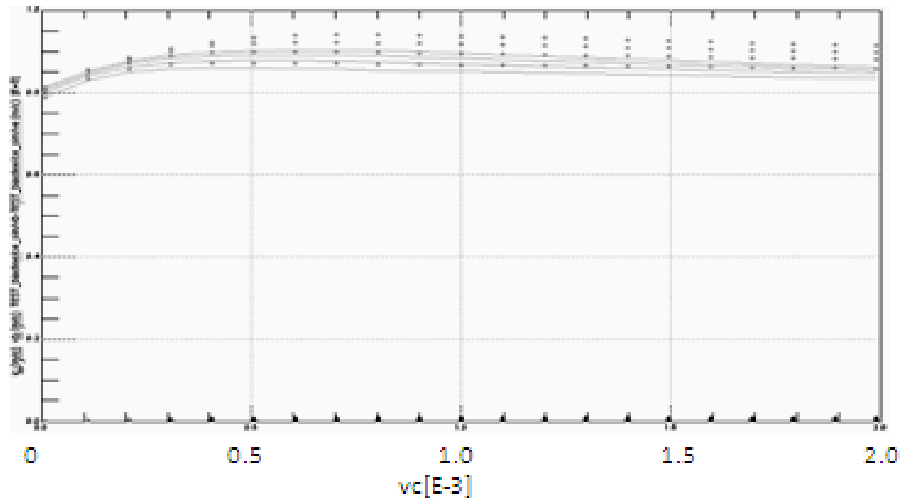

Figure 4.9 Common emitter V_{be} vs V_{ce} plot at temperature T_1 for a 5 um^2 device.
Continuous line is simulated data using ADS; Data symbols are measured data
Ib = 20uA, 30uA, 40uA, 50uA

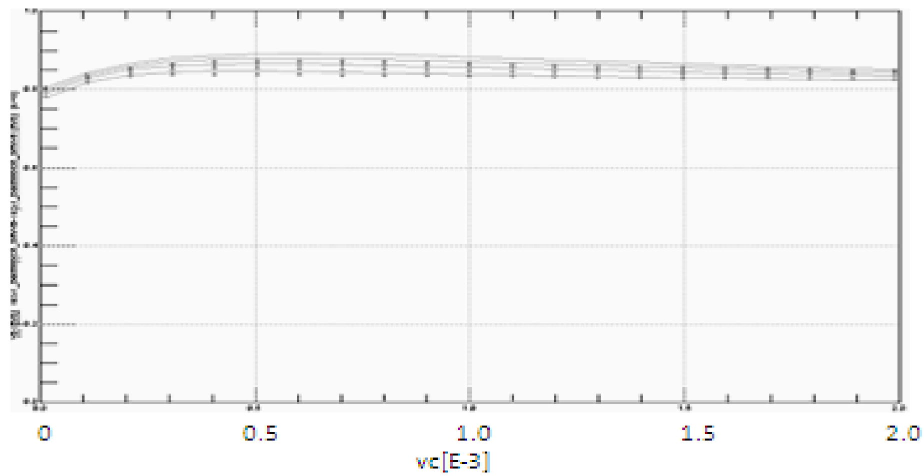

Figure 4.10 Common emitter V_{be} vs V_{ce} plot at temperature T_2 for a 5 um^2 device.
Continuous line is simulated data using ADS; Data symbols are measured data
Ib = 20uA, 30uA, 40uA, 50uA

Power vs V_{ce} plots:

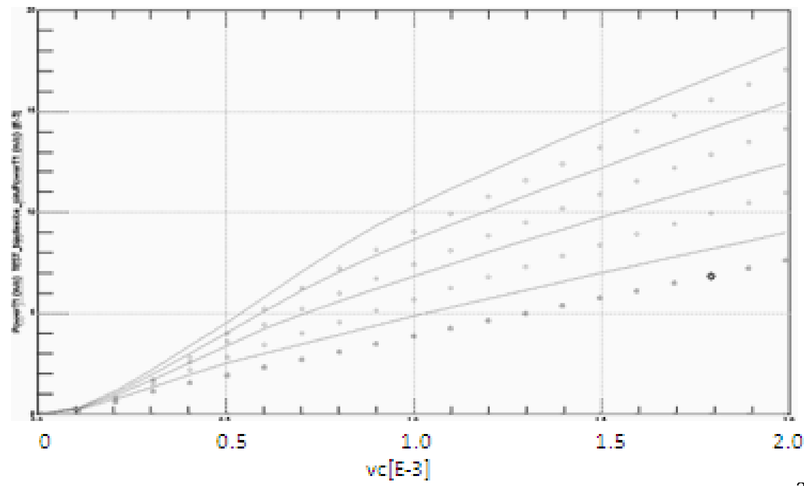

Figure 4.11 Common emitter power vs V_{ce} plot at temperature T_1 for a 5 um^2 device. Continuous line is simulated data using ADS; Data symbols are measured data
Ib = 20uA, 30uA, 40uA, 50uA

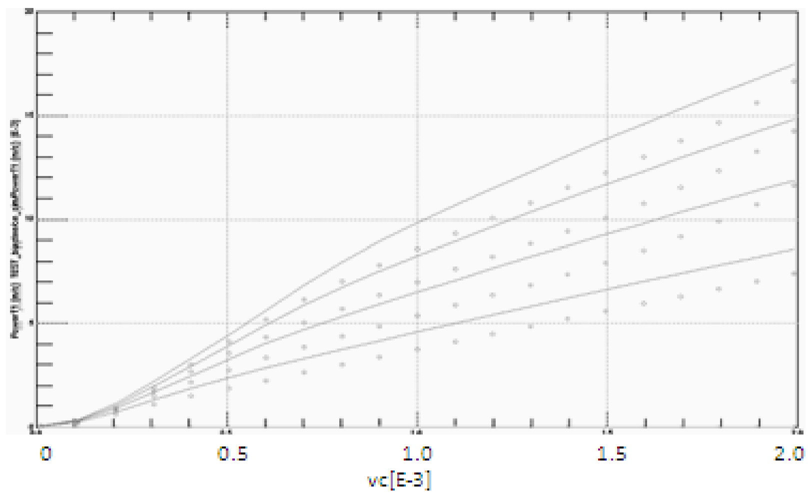

Figure 4.12 Common emitter power vs V_{ce} plot at temperature T_1 for a 5 um^2 device. Continuous line is simulated data using ADS; Data symbols are measured data
Ib = 20uA, 30uA, 40uA, 50uA

4.4.2.4 R_{TH} calculation

The thermal resistance is calculated using equation 4.8 using the data from the plots in the section 4.4.2. The calculated value of R_{TH} is plotted vs V_{ce} in figure 4.13 and 4.14..

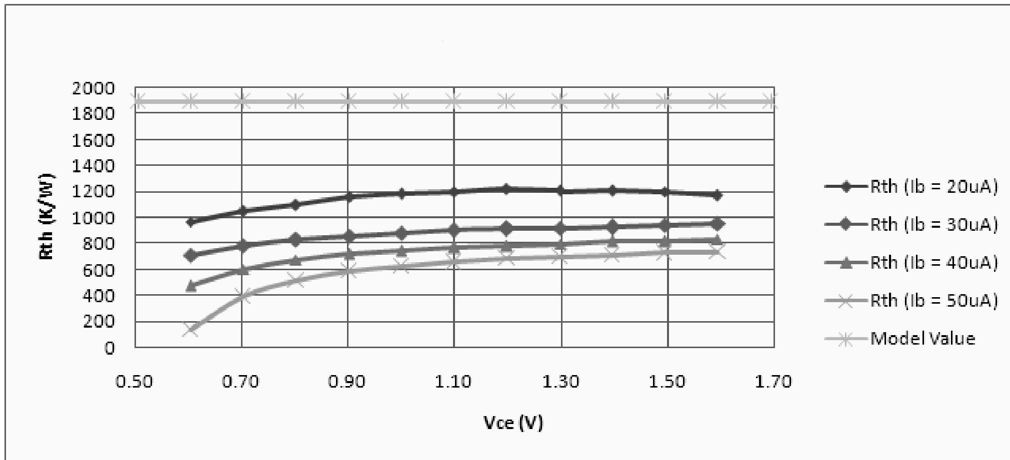

Figure 4.13 Thermal resistance vs V_{ce} plot for a 5 um^2 device.

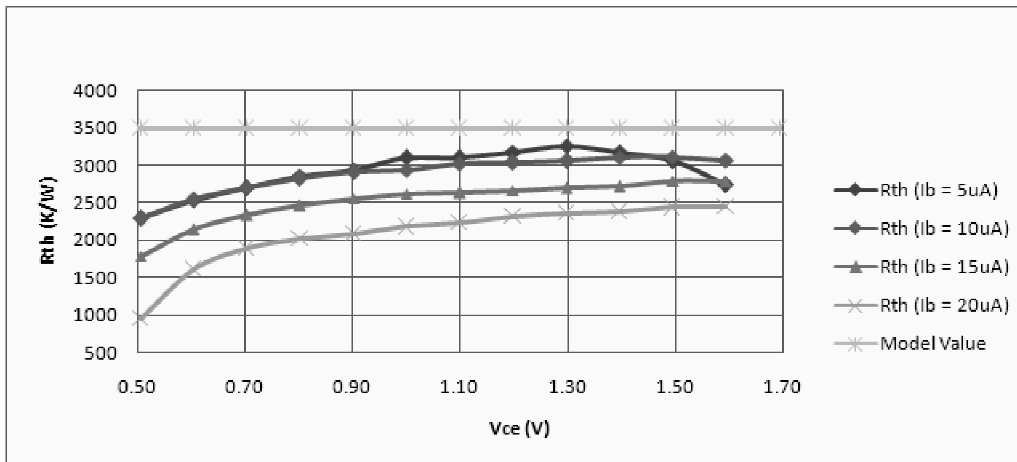

Figure 4.14 Thermal resistance vs V_{ce} plot for a 2.5 um^2 device.

Thermal resistance is treated as a constant parameter in most compact models. But in reality it is a function of power dissipation and ambient temperature [38]. Hence the exact value of the thermal resistance for a device depends on its bias conditions.

As V_{ce} increases the power dissipated in the device increases. It is obvious from the above plots that thermal resistance increases with increase in power. As the power increases the thermal conductivity of silicon, silicon dioxide and silicon-germanium decreases as per the relation [13][30].

$$k(T) = k_{ref}\left(\frac{T}{T_{ref}}\right)^{-\alpha} \tag{4.13}$$

where k_{ref} is the thermal conductivity at the reference temperature T_{ref}. The value of k_{ref} and α varies for different materials. Since thermal resistance is inversely proportional to the thermal conductivity it increases as power increases.

The thermal resistance calculated for different base currents is summarized in the table below. Here the point at which the device enters the linear region is selected for the thermal resistance calculation.

Table 4.1 Thermal resistance values measured for 5 um^2 and 2.5 um^2 device.

0.25 um × 20um device				
Base Current	**20uA**	**30uA**	**40uA**	**50uA**
Rth (K/W)	1156	860.2	768.6	654.8

0.25 um × 10um device				
Base Current	**5uA**	**10uA**	**15uA**	**20uA**
Rth (K/W)	2944.2	2911.2	2558.8	2091.2

4.4.2.5 Calculation of VBIC parameters IS and NF

The VBIC parameters IS and NF are calculated from the forward Gummel measurement data using two methods.

Method 1:

Extract these parameters from the transistor current equation using two points on the forward Gummel plot [37]. From the reverse Gummel measurements in figure 4.2, the minimum of the derivative in equation 4.6 occurs at V_{bc} equal to 620 mV. Hence two points 580 mV and

680 mV which are around this voltage are taken for the calculation of IS and NF. Using these values of Vbc and the corresponding Ic in the transistor current equation, two equations are obtained with two unknowns IS and NF, from which the values of IS and NF are obtained to be

IS = 86.18 aA

NF = 1.0237

Method 2:

The second method to find IS and NF is done using the optimization utility in ICCAP by optimizing I_c. Again the optimization range is selected from 580 mV to 680 mV.

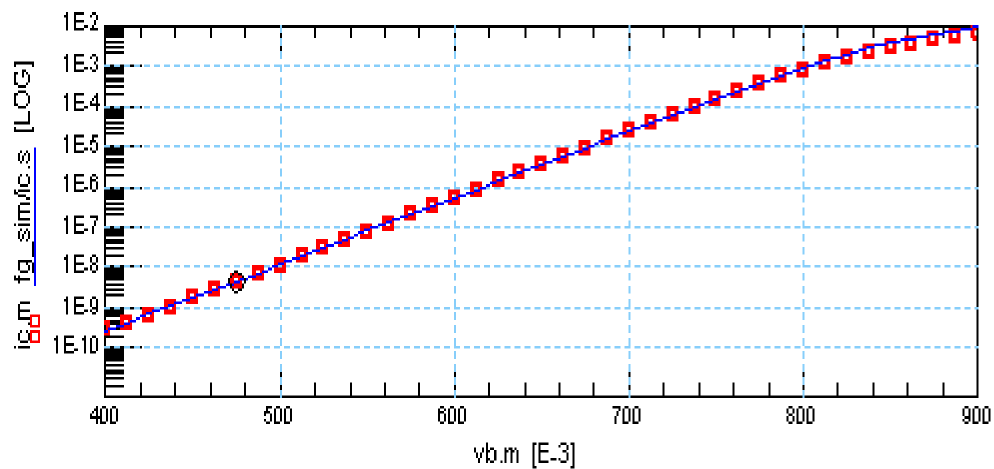

Figure 4.15 I_c vs V_{bc} plot from forward Gummel setup.

The optimization of I_c in the V_{bc} range of 580 mV to 680 mV gives

IS = 67.95 aA

NF = 1.016

The second method takes into account all data in the range 580 mV to 680 mV, whereas the first method considers only the end points of this range. The second method also comprehends the reverse Early effect and the parameters appropriate to the model values used. These might be the source of the discrepancy in the two results.

4.5 Summary

The DC method for thermal resistance calculation is explained, and the measurement results are provided for two different SiGe HBT devices from National Semiconductor. Bovolon's method explained in this chapter is effective since it allows calculating thermal resistance from small areas of the output I/V curve. Other methods which require large difference in dissipated power or large temperature offsets may simply fail if hot spot formation takes place during measurement. Also this method yields a vast number of equations that allow for determination of the thermal resistance at various power levels. Since R_{TH} is a parameter that is calculated indirectly from its influence on electrical quantities, one can expect a comparatively high uncertainty resulting in scattering of values. Therefore, a method that allows averaging over many points is always preferable over a method that only yields a few values.

CHAPTER 5

TIME DOMAIN METHOD FOR MEASUREMENT OF THERMAL RESISTANCE AND THERMAL CAPACITANCE

5.1 Introduction

The method described in chapter 4 is a DC method in which only the thermal resistance can be extracted. This chapter explains a time domain method in which both the thermal resistance and thermal capacitance can be extracted.

The effect of thermal resistance of a device is to show a resistance towards the heat flow in the device, and that of the thermal capacitance is to store heat in the device. If a voltage pulse input is given to a device, the heat generated in the device cannot flow through it instantaneously. When the pulse input to the device goes to a high level, the resulting temperature change in the device depends on the thermal time constant of the device [36]. As described in chapter 4, the V_{be} of a device decreases with temperature almost linearly [33]. This causes the V_{be} voltage to decrease at a rate dependent on the thermal time constant. The time domain method explained in this chapter tries to exploit this behavior of the bipolar transistors to extract the thermal time constant. The ICCAP modeling tool from Agilent is used for optimizing the values of the thermal resistance and thermal capacitance.

5.2 ICCAP measurement and modeling tool

The ICCAP modeling system is used to measure a semiconductor device, model the device characteristics and analyze the resulting data. The process flow of a typical ICCAP measurement system is shown in figure 5.1. Different simulators like spectre, ADS, hpspice etc. can be linked to the ICCAP tool. In the time domain method explained here, ICCAP is mainly used for optimization.

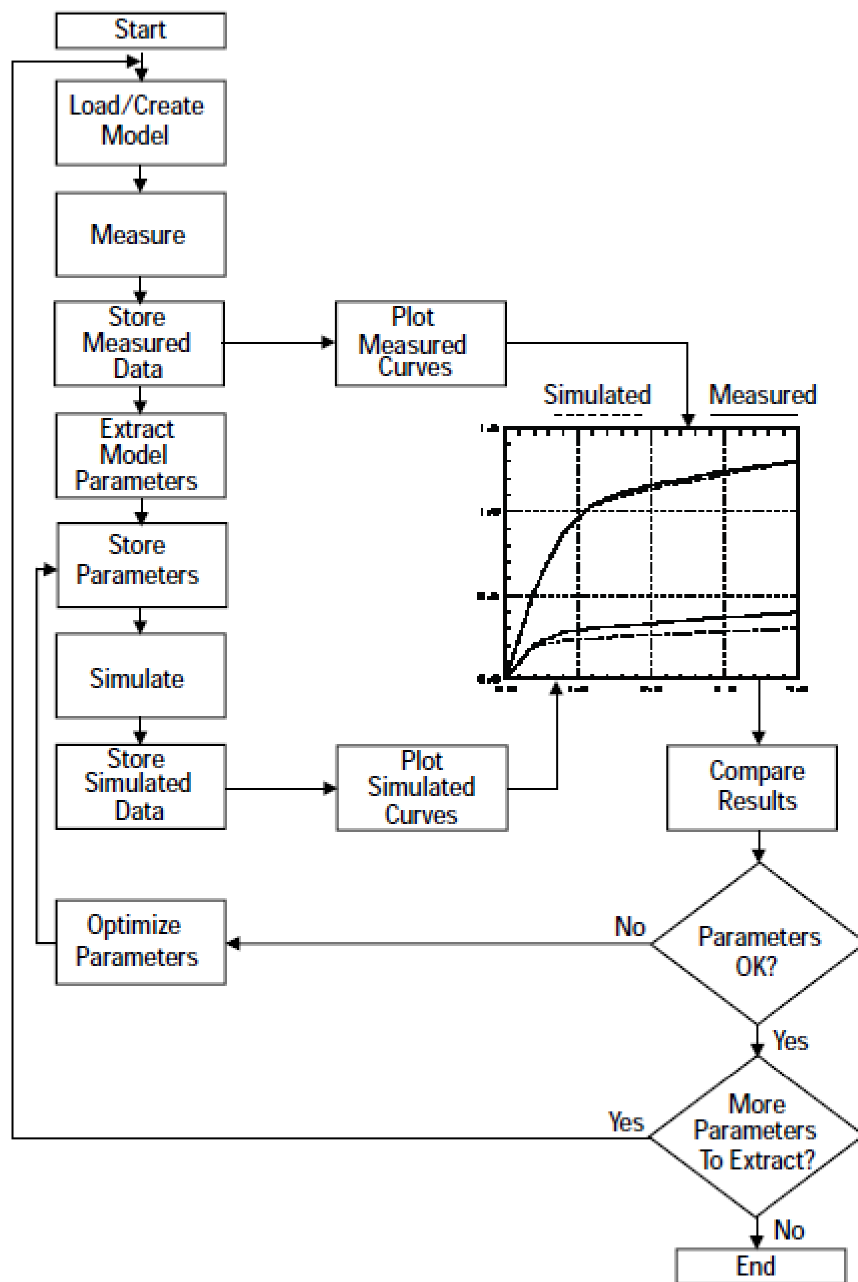

Figure 5.1 General functionality of ICCAP system [39].

5.2.1 Optimization using ICCAP

Optimization is performed to achieve the best possible fit between the measured and simulated data. The optimization flow chart is shown in figure 5.2. Given a set of measured data, the optimizer iteratively solves for a set of model parameters which produce simulated data that optimally approximates the measured data. The algorithm works as follows [39]:

a) Using the circuit description and model parameter values extracted from measured data, the optimizer invokes the currently selected simulator to obtain a set of simulated data from the model parameters. This step is called function evaluation.

b) The optimizer compares the simulated data with the measured data and calculates the RMS error between them.

c) Based on these results, the optimizer calculates a new set of model parameter values and again compares the simulated data with the measured data.

d) This process continues with another function evaluation until the RMS error between the simulated and measured data either falls below a specified range, or no further improvement is possible.

The three optimization models available are Levenberg-Marquardt, random and hybrid. If the model is well behaved and local minima are not a problem, the Levenberg-Marquardt optimization is used. Hybrid optimization is used when local minima are a problem. Random optimization is mainly used before a Levenberg-Marquardt optimization to reduce the error to an acceptable limit. The Levenberg-Marquardt method is a non-linear, least squares fit algorithm. This combines the steepest descent and Gauss-Newton methods. It calculates the specified model parameters until the RMS error between measured and simulated data is minimized. Random optimization makes random guesses of the parameter values until the specified RMS error value is obtained. Hybrid optimization is a combination of the random and Levenberg-Marquardt optimizers. The input table supplied with the optimizer is used to specify the target,

simulated data and weights to be applied to each. The minimum and maximum value along which the optimizer must work is set using the options table.

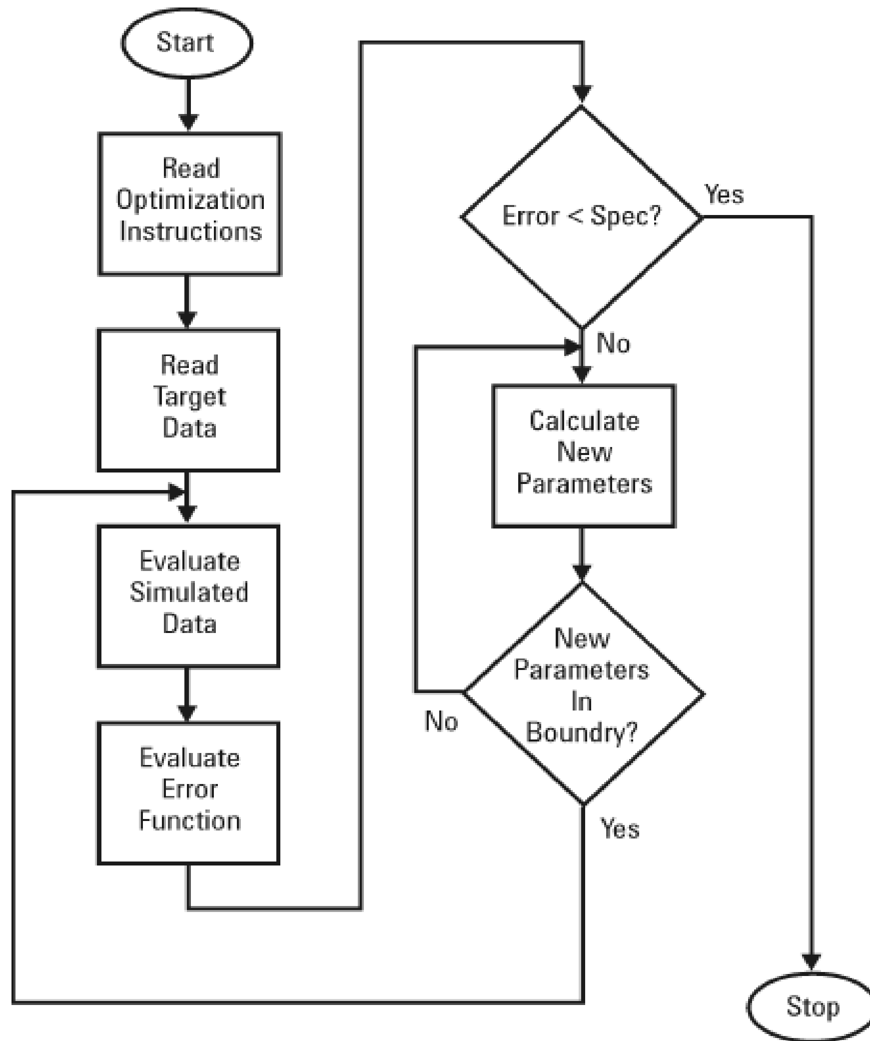

Figure 5.2 Optimization flow diagram [39].

5.3 Circuit setup

The common base configuration is selected for measurements to avoid the use of large resistances when smaller dimension devices are used. For a common emitter configuration with smaller devices the emitter resistance value has to be large in order to have small currents in the device. This maintains the safe operating area (SOA) limits. This large resistance together

with the oscilloscope input capacitance results in a low pass filtering effect which filters the high frequency components in the V_{be} voltage. This can cause a higher slope for V_{be} measured in the oscilloscope than the actual slope when the input pulse to the transistor goes from a low level to a high level. This results in incorrect readings of peak values for V_{be} and a wrong estimation of the thermal resistance. Hence common base configuration has been selected for all measurements. The circuit set up used in ICCAP for optimization is shown below.

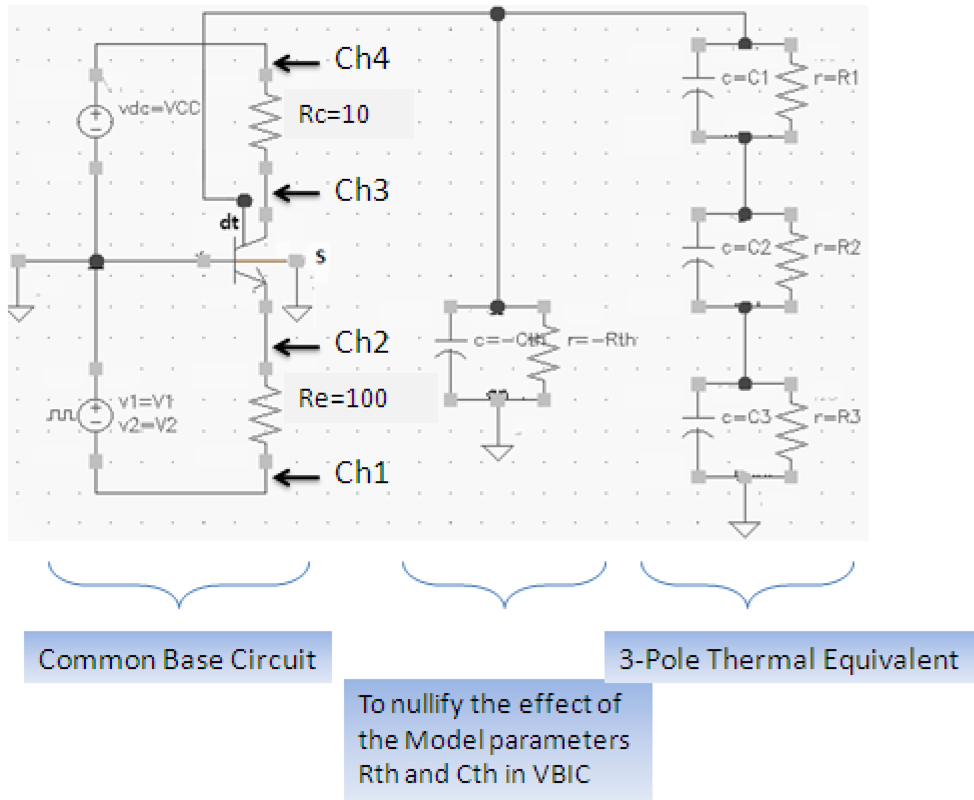

Figure 5.3 Circuit setup for time domain measurements.

The middle leg in the above circuit is to nullify the effect of the R_{TH} and C_{TH} values used in the VBIC model file. And the third leg is a 3-pole model which gave good results with most of the measured data. The values of resistances and capacitances of this 3-pole model are varied by the ICCAP optimizer to get a best fit with the measured data. A Foster network or a Cauer

network can be used here. After optimization one can be converted to the other using network synthesis techniques.

5.4 Measurement results

The measurements have been performed on the NPN and PNP, SiGe HBTs of different dimensions, fabricated by National Semiconductors in their CBC8 process. The wafers are probed using Cascade Infinity probes with 150 um pitch. An Agilent 6000 series oscilloscope and function generator is used in the measurement. The circuit is probed at four points in the circuit as shown in figure 5.3. The simulations are done in ICCAP using the spectre simulator. The data taken from the measurement is given as input to ICCAP which then optimizes the R_{TH} and C_{TH} values to get the best fit between the measured and simulated curves. The bias levels for each device are carefully chosen after simulations in-order to maintain the device in the safe operating area (SOA) limits provided by National Semiconductor.

5.4.1 Results and Plots of optimizations

As mentioned in section 5.1, in the time domain method, the thermal resistance and capacitance is calculated from the thermal tail of the V_{be} voltage. After giving the measured V_{be} voltage as the input to ICCAP, it optimizes the simulated V_{be} voltage to match the measured one by changing the values of R_{TH} ad C_{TH}. The optimization is done for a 3-pole network or 2-pole network to get the best fit possible. In all the optimizations done, the model values received from National Semiconductor is given as the starting value for optimization. Also the part of the Vbe curve where the transition happens is optimized at first to get a reasonable approximation for R_{TH} and C_{TH} and then the optimization is performed on the whole time range. The resistance and capacitance of this 3-pole network is designated as R_1, C_1, R_2, C_2, and R_3, C_3. In this section the plots of optimizations done for different devices are shown with the obtained results. The results are tabulated in the order from longest time constant to the shortest time constant. In the tables Rlong and τ,long corresponds to the longest time constant, Rmed and τ,med to the middle time constant and Rshort and τ,short to the shortest time constant.

Plot for a low voltage NPN 0.15 um^2 device is shown in figure 5.4.

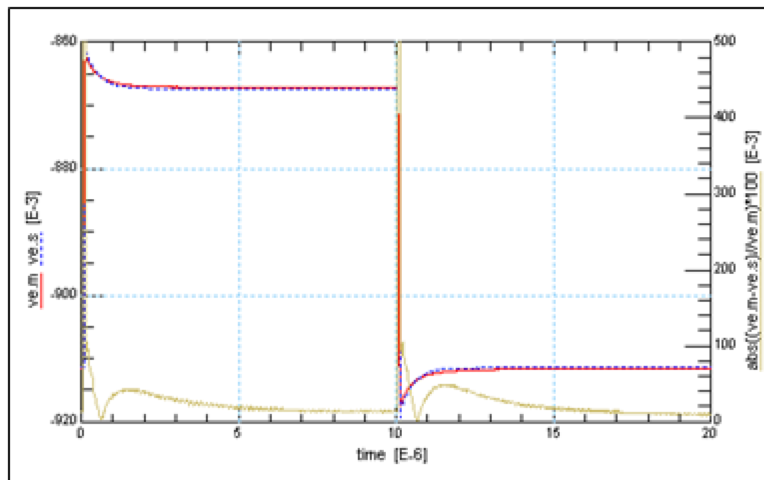

Figure 5.4 Optimization done using ICCAP for low voltage NPN 0.15 um^2 SiGe HBT device. Solid line represents measured data; Dotted line represents simulated data

Table 5.1 Bias levels and results after optimization for low voltage NPN 0.15 um^2 SiGe HBT device

VCC	1V		
Vpulse 1 (V1)	-1.03V	**Vpulse 2 (V2)**	-0.91V

Rlong	9.25K	**τ,long**	379.5n
Rshort	19.29K	**τ,short**	4.94n
Rth Meas (Rth,tot)	28.5K		

Plot for a low voltage NPN 0.2 um^2 device is shown in figure 5.5.

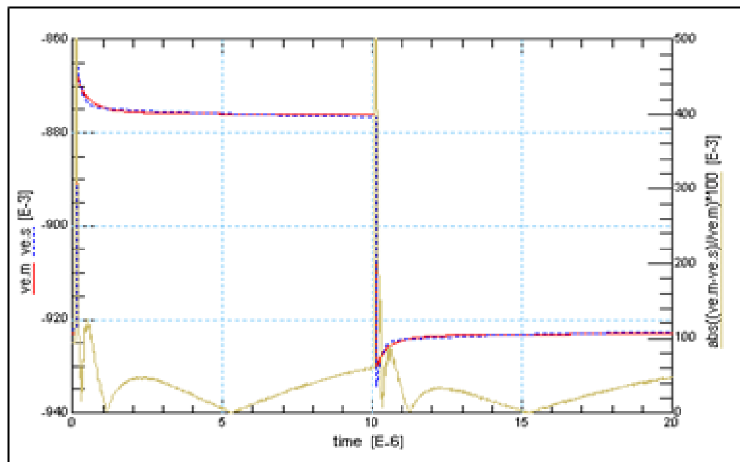

Figure 5.5 Optimization done using ICCAP for low voltage NPN 0.2 um^2 SiGe HBT device. Solid line represents measured data; Dotted line represents simulated data

Table 5.2 Bias levels and results after optimization for low voltage NPN 0.2 um^2 SiGe HBT device

VCC	1V		
Vpulse 1 (V1)	-1.1V	Vpulse 2 (V2)	-0.95V

Rlong	2.23K	τ,long	5.72u
Rmed	10.25K	τ,med	145.4n
Rshort	7.87K	τ,short	119.6p
Rth Meas (Rth,tot)	20.35K		

Plot for a low voltage NPN 0.25 um^2 device is shown in figure 5.6.

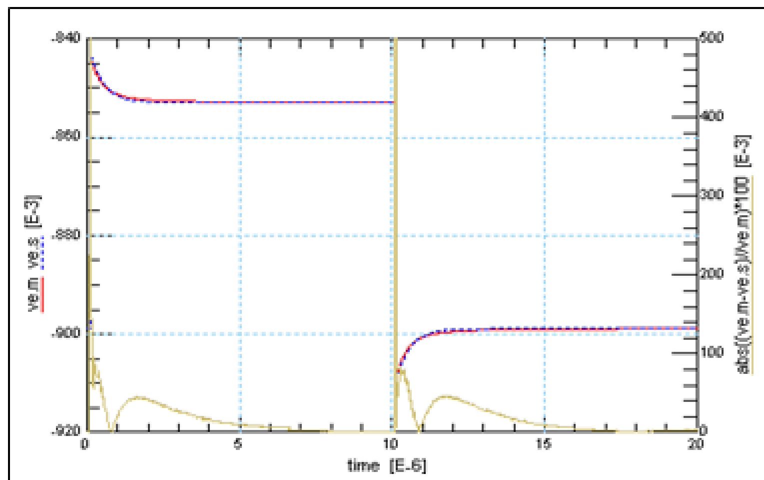

Figure 5.6 Optimization done using ICCAP for low voltage NPN 0.25 um^2 SiGe HBT device. Solid line represents measured data; Dotted line represents simulated data

Table 5.3 Bias levels and results after optimization for low voltage NPN 0.25 um^2 SiGe HBT device

VCC	1V		
Vpulse 1 (V1)	-1.065V	**Vpulse 2 (V2)**	-0.90V

Rlong	7.44K	**τ,long**	423.1n
Rshort	12.74K	**τ,short**	391.9p
Rth Meas (Rth,tot)	20.18K		

Plot for a low voltage NPN 1.25 um^2 device is shown in figure 5.7.

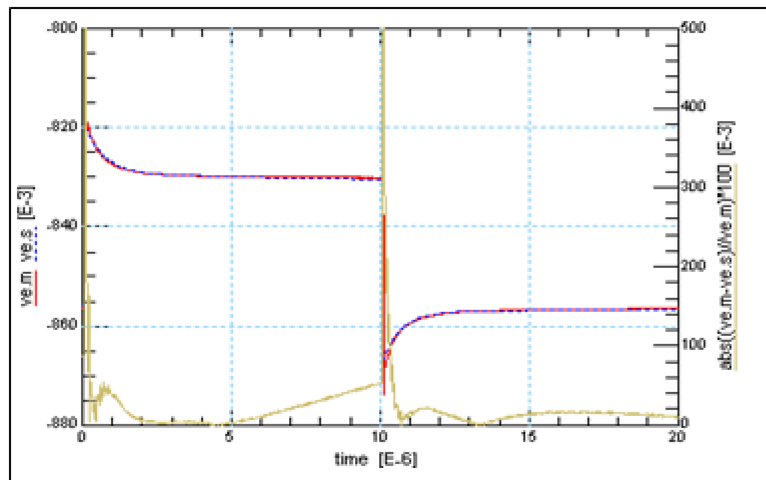

Figure 5.7 Optimization done using ICCAP for low voltage NPN 1.25 um^2 SiGe HBT device. Solid line represents measured data; Dotted line represents simulated data

Table 5.4 Bias levels and results after optimization for low voltage NPN 1.25 um^2 SiGe HBT device

VCC	1V		
Vpulse 1 (V1)	-1.2V	**Vpulse 2 (V2)**	-0.95V

Rlong	976.2	**τ,long**	19.76u
Rmed	3.003K	**τ,med**	594.5n
Rshort	4.621K	**τ,short**	131.5p
Rth Meas (Rth,tot)	8.6K		

Pot for a high voltage NPN 2.5 um^2 device is shown in figure 5.8.

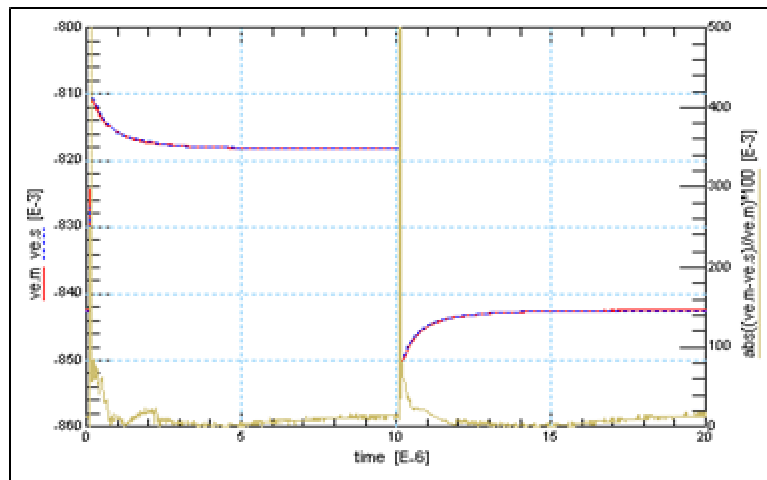

Figure 5.8 Optimization done using ICCAP for high voltage NPN 2.5 um^2 SiGe HBT device. Solid line represents measured data; Dotted line represents simulated data

Table 5.5 Bias levels and results after optimization for high voltage NPN 2.5 um^2 SiGe HBT device

VCC	2V		
Vpulse 1 (V1)	-1.08V	**Vpulse 2 (V2)**	-0.904V

Rlong	838.4	**τ,long**	1.317u
Rmed	1.393K	**τ,med**	385.9n
Rshort	1.367K	**τ,short**	8.51n
Rth Meas (Rth,tot)	3.59K		

Plot for a high voltage PNP 0.25 um^2 device is shown in figure 5.9.

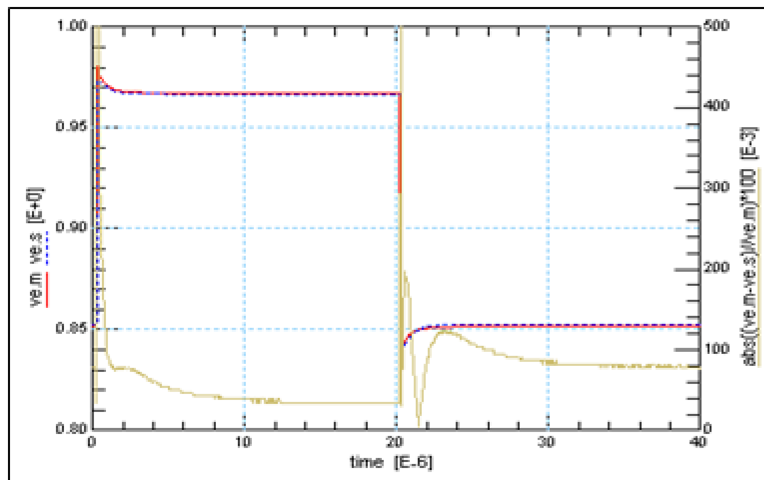

Figure 5.9 Optimization done using ICCAP for high voltage PNP 0.25 um^2 SiGe HBT device. Solid line represents measured data; Dotted line represents simulated data

Table 5.6 Bias levels and results after optimization for high voltage PNP 0.25 um^2 SiGe HBT device

VCC	-2V		
Vpulse 1 (V1)	1.1V	**Vpulse 2 (V2)**	1.3V

Rlong	4.196K	**τ,long**	626.6n
Rshort	11.68K	**τ,short**	723.4p
Rth Meas (Rth,tot)	15.87K		

Plot for a high voltage PNP 2.5 um^2 device is shown in figure 5.10.

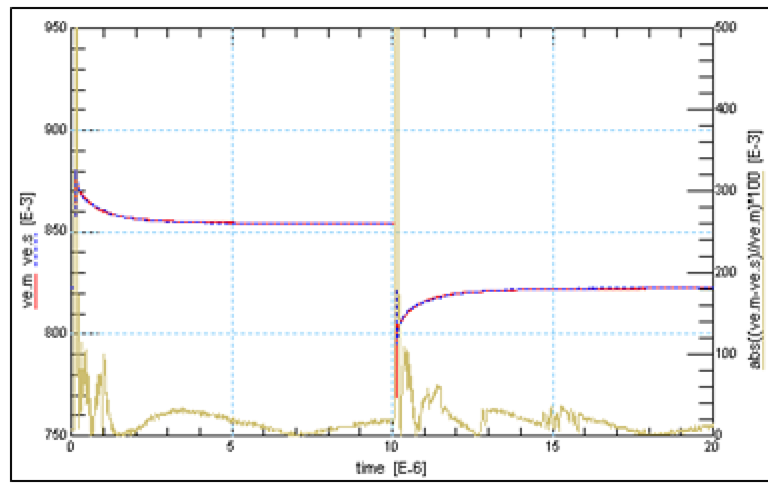

Figure 5.10 Optimization done using ICCAP for high voltage PNP 2.5 um^2 SiGe HBT device. Solid line represents measured data; Dotted line represents simulated data

Table 5.7 Bias levels and results after optimization for high voltage PNP 2.5 um^2 SiGe HBT device

VCC	-2V		
Vpulse 1 (V1)	1.28V	**Vpulse 2 (V2)**	0.938V

Rlong	1.975K	**τ,long**	1.067u
Rmed	2.08K	**τ,med**	104.7n
Rshort	245	**τ,short**	14.88n
Rth Meas (Rth,tot)	4.298K		

Plot for a high voltage PNP 5 um^2 device is shown in figure 5.11.

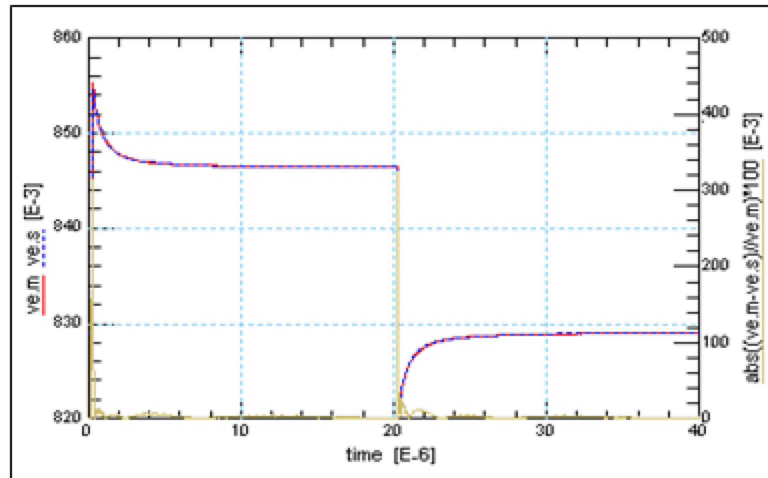

Figure 5.11 Optimization done using ICCAP for high voltage PNP 5 um^2 SiGe HBT device. Solid line represents measured data; Dotted line represents simulated data

Table 5.8 Bias levels and results after optimization for high voltage PNP 5 um^2 SiGe HBT device

VCC	-2V		
Vpulse 1 (V1)	1.1V	**Vpulse 2 (V2)**	1.4V

Rlong	258.3	**τ,long**	3.352u
Rmed	1.026K	**τ,med**	574.7n
Rshort	1.392K	**τ,short**	13.37n
Rth Meas (Rth,tot)	2.676K		

5.4.2 Summary of results

The results obtained from time domain measurements are summarized in table 5.9.

Table 5.9. Summary of results obtained in time domain measurements.
LV stands for low voltage and HV for high voltage.

Type	Device	Rlong	τ,long	Rmed	τ,med	Rshort	Cshort
LV NPN	0.15 um^2	9250	3.80E-07			19290	2.56E-13
LV NPN	0.2 um^2	2230	5.72E-06	10250	1.45E-07	7870	1.52E-14
LV NPN	0.25 um^2	7440	4.23E-07			12740	3.08E-14
LV NPN	1.25 um^2	976.2	1.98E-05	3003	5.95E-07	4621	2.85E-14
HV NPN	2.5 um^2	838	1.32E-06	1393	3.86E-07	1367	6.23E-12
HV PNP	0.25 um^2	4196	6.27E-07			11680	6.19E-14
HV PNP	2.5 um^2	1975	1.07E-06	2080	1.05E-07	245	6.07E-11
HV PNP	5.0 um^2	258.3	3.35E-06	1026	5.75E-07	1392	9.60E-12

5.4.3 Frequency response

In-order to get better insight to the frequency response of the thermal model, the data from the 5 um^2 high voltage PNP device is fit to a 1-pole, 2-pole and 3-pole model. The frequency response can be plotted for each as shown below.

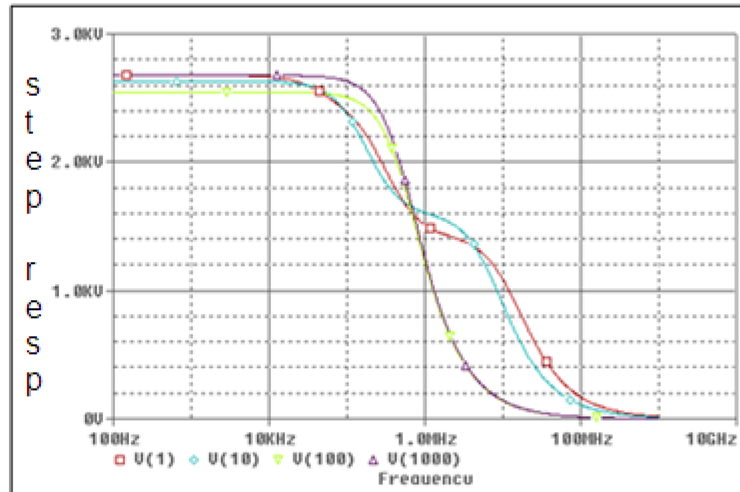

Figure 5.12 Comparison of 1-pole, 2-pole & 3-pole fit for a 5um^2 high voltage PNP device.
V(1) represents a 3 Pole fit; V(10) represents a 2 Pole fit; V(100) represents a 1 Pole fit;
V(1000) represents a pole fit with fixed R_{TH}

5.5 Conversion from multi-pole model to a single pole model

As shown in figure 3.1, VBIC models the self heating using only a single resistance and capacitance. But the optimizations described in section 5.4 are done to multi pole circuits in order to get the best fit. Hence these multi pole models have to be converted to single pole models in order to use them in the VBIC model file.

The principle that must be observed when fitting a multi pole data to a single pole data is energy conservation. The single pole impulse temperature change should store the same energy as the multi pole data [36]. The energy of a 3-pole Foster network is equated to the energy of a 1-pole network.

$$C_v \times \Delta P \times \left[\int_0^\infty R_1\left(1 - e^{\frac{-t}{\tau_1}}\right)dt + \int_0^\infty R_2\left(1 - e^{\frac{-t}{\tau_2}}\right)dt + \int_0^\infty R_3\left(1 - e^{\frac{-t}{\tau_3}}\right)dt\right] = C_v \times \Delta P \times \int_0^\infty R_S\left(1 - e^{\frac{-t}{\tau_S}}\right)dt \quad (5.1)$$

where R_s and τ_s are the resistance and time constant of the single pole network respectively, C_v is the heat capacity of the material and ΔP is the change in thermal power.

The single pole network resistance R_s and time constant τ_s are defined as

$$R_s = R_1 + R_2 + R_3 \quad (5.2)$$

$$\tau_s = R_s C_s \quad (5.3)$$

Perform the integration in equation 5.1.

$$(R_1 t + R_2 t + R_3 t)\big|_0^\infty + R_1\tau_1 e^{\frac{-t}{\tau_1}} + R_2\tau_2 e^{\frac{-t}{\tau_2}} + R_3\tau_3 e^{\frac{-t}{\tau_3}}\Big|_0^\infty = R_s\tau_s\big|_0^\infty + R_s\tau_s e^{\frac{-t}{\tau_s}}\Big|_0^\infty \quad (5.4)$$

Since first part of both sides represent the same value, equation 5.4 can be written as

$$R_1\tau_1 e^{\frac{-t}{\tau_1}} + R_2\tau_2 e^{\frac{-t}{\tau_2}} + R_3\tau_3 e^{\frac{-t}{\tau_3}}\Big|_0^\infty = R_s\tau_s e^{\frac{-t}{\tau_s}}\Big|_0^\infty \quad (5.5)$$

This can be evaluated to be

$$R_1\tau_1 + R_2\tau_2 + R_3\tau_3 = R_s\tau_s \quad (5.6)$$

Using equations 5.6, 5.2 and 5.3, the capacitance of the single pole network C_s can be written as

$$C_s = \frac{R_1\tau_1+R_2\tau_2+R_3\tau_3}{(R_1+R_2+R_3)^2} \quad (5.7)$$

The multi pole values obtained in section 5.4 is converted to single pole values using equations 5.2 and 5.7 and is summarized in table 5.10.

Table 5.10 Summary of conversion of multi pole values in table 5.9 to single pole values using energy conservation. LV stands for low voltage and HV for high voltage.

Type	Device	1-pole Cs	1-pole Rs	1-pole τ
LV NPN	0.15 um^2	4.43E-12	2.85E+04	1.26E-07
LV NPN	0.2 um^2	3.44E-11	2.04E+04	7.00E-07
LV NPN	0.25 um^2	7.74E-12	2.02E+04	1.56E-07
LV NPN	1.25 um^2	2.85E-10	8.60E+03	2.45E-06
HV NPN	2.5 um^2	1.28E-10	3.59E+03	4.58E-07
HV PNP	0.25 um^2	1.05E-11	1.59E+04	1.66E-07
HV PNP	2.5 um^2	1.26E-10	4.30E+03	5.41E-07
HV PNP	5.0 um^2	2.06E-10	2.68E+03	5.51E-07

The frequency response for the 3-pole model and the 1-pole model is plotted for a low voltage 0.15 um^2 NPN device in figure 5.13 and figure 5.14.

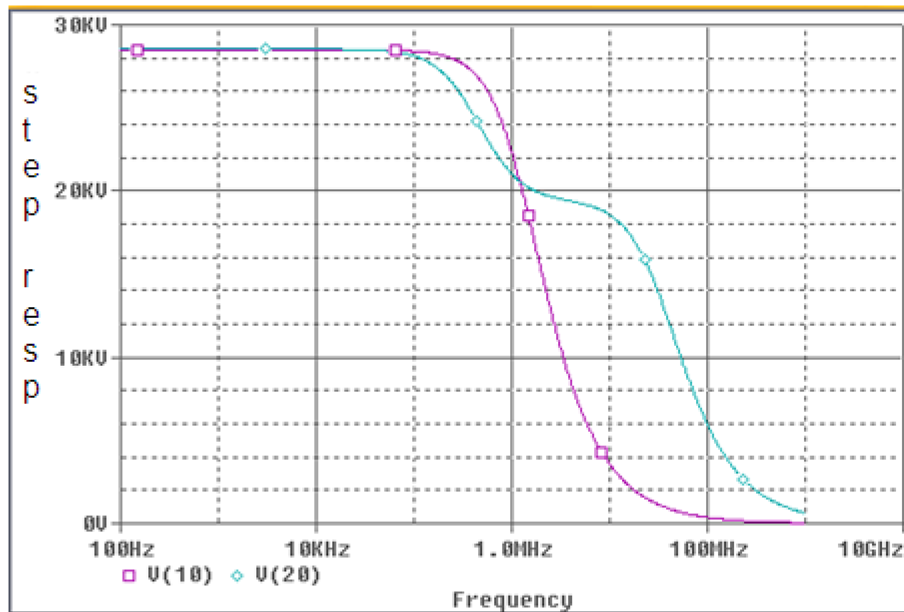

Figure 5.13 Frequency response plot for the 3-pole model and the 1-pole model for a 0.15 um^2 NPN device. V(10) represents the single pole response and V(20) the 2-pole response.

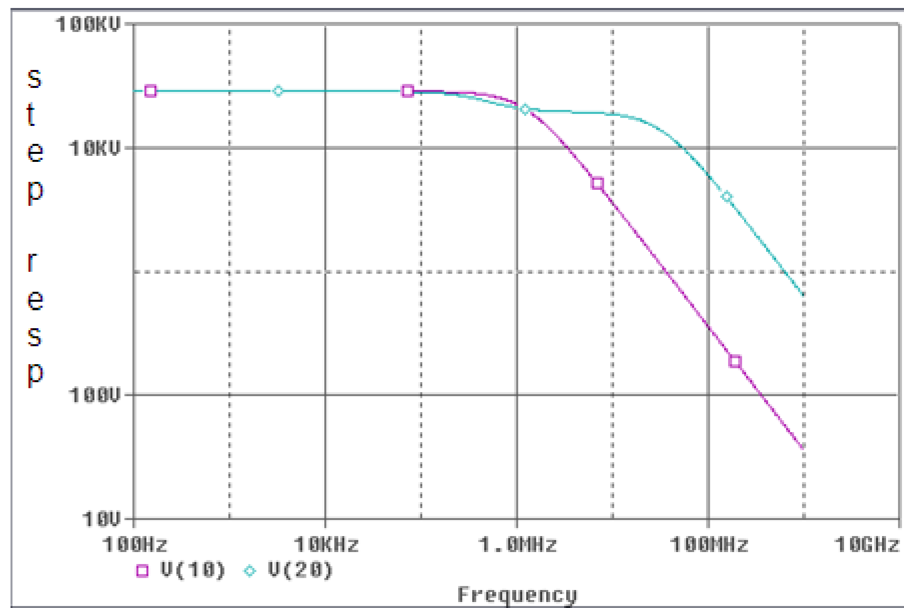

Figure 5.14 The plot in figure 5.13 is re-plotted with a log Y-axis.

5.6 Summary

The time domain method for thermal resistance and thermal capacitance calculation is explained and the measurement results are provided for different SiGe HBT devices from National Semiconductors. A method based on energy conservation is introduced to convert the multi pole thermal model obtained from the time domain method to a single pole thermal model. These calculated values can be used in the VBIC model files to get a good modeling of thermal behavior of the device.

CHAPTER 6

CONCLUSION AND RECOMMENDATION FOR FUTURE WORK

Extensive analysis has been done on the effect of self heating in SiGe HBTs and different methods to extract the self heating parameters have been tried.

The thermal resistance is treated as a constant parameter in the VBIC model file. But since the thermal conductivity of substance is a function of temperature, the thermal resistance varies with temperature. An expression has been derived for thermal resistance, considering thermal conductivity as a function of temperature.

As discussed in chapter 5, a multi pole model is necessary to exactly model the thermal behavior of the device. But VBIC has provision only for a single pole for modeling self heating. An expression based on energy conservation is derived for converting a multi pole model into a single pole model.

Masana's method and Joy and Schlig's equations have been used to calculate the thermal resistance and thermal capacitance values, using the device dimensions and material constant values for different sizes of SiGe HBTs.

A time domain method has been used to extract the thermal resistance and thermal capacitance values for different SiGe HBT devices from National Semiconductor. Also a DC technique based on Bovolon's method has been used to extract the thermal resistance values.

This thesis paper has given emphasis to self heating of transistors. The heat generated in the adjacent devices can also play a significant role in the performance of transistors since the devices are getting closer in the current technologies. This research work can be extended to study the effect of adjacent heating in SiGe HBTs. And it would be interesting to study the

effect of self heating and adjacent heating in commonly used circuits like current mirrors, operational amplifiers, power amplifiers etc.

The methods used in this thesis to measure the thermal resistance assume that it is a constant parameter. But as explained in chapter 2, the thermal resistance varies with temperature. It would be worthwhile to research on methods to measure the thermal resistance considering it as a function of temperature.

It would also be worthwhile to research on determining the safe operating area, i.e. to determine the voltage and current levels, for SiGe HBTs in which the effect of self heating would be negligible.

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