THERMAL CHARACTERIZATION OF DIELECTRICALLY ISOLATED BIPOLAR JUNCTION TRANSISTOR

by

DAEWOO KIM

Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

THE UNIVERSITY OF TEXAS AT ARLINGTON

December 2008

Copyright © by Daewoo Kim 2008

All Rights Reserved

ACKNOWLEDGEMENTS

I would like to express appreciation to Prof. Ronald L. Carter for providing me with the opportunity to research in this project under his guidance. It is my honor to work with him. He provided me continuous support whenever I met an obstacle in this project. I am also thankful to Prof. W. Alan Davis and Prof. Howard T. Russell, Jr. for their continual advice and help in the research in this project. They encouraged me to overcome any problem which I met in this research. I will never forget their supports.

I would like to thank Prof. Donald Butler and Prof. Seong Jin Koh for agreeing to be members of the committee and I also express my appreciation to my research group members. I really enjoyed the time that I have spent with my colleagues.

National Semiconductor Corporation and the Electrical Engineering Department at UTA are both gratefully appreciated for providing financial support to my research.

I would like to thank my family for their continuous support. I could not finish my research without her, the support of my lovely wife, Jung-Hyun Kim. I really thank for her help.

October 10, 2008

ABSTRACT

THERMAL CHARACTERIZATION OF DIELECTRICALLY ISOLATED BIPOLAR JUNCTION TRANSISTOR

Daewoo Kim, PhD.

The University of Texas at Arlington, 2008

Supervising Professor: Dr. Ronald L. Carter

Since the integrated circuit (IC) was invented in 1960, the operating speed of semiconductor devices has steadily increased and the number of semiconductor devices in an IC chip has grown by a size reduction of the devices. This trend has led to the rapid increase of power consumption and heat generation per unit area. As a result of this increase, thermal characterization of semiconductor devices has become more important.

It is especially important to consider thermal characteristics of the dielectrically isolated complementary bipolar junction transistor (DIBJT) which offers many advantages. However, a major disadvantage of this device is an increase in self-heating.

The DIBJT device is fabricated on a silicon-on-insulator wafer, which has an isolation oxide between the bulk wafer and the epitaxial Si layer. Each DIBJT is also surrounded by an isolation trench, which is usually fabricated by oxide or other insulating material. Therefore, the heat generated by the DIBJT device cannot easily transfer to the heat sink.

This research explored the five element compact model, for the thermal impedance of a DIBJT. The thermal resistance can be calculated using the maximum temperature of the DIBJT or the estimated base collector junction temperature of the DIBJT. There is around 4.7% difference between the thermal resistance calculated using the maximum temperature point and the thermal resistance calculated using the estimated base collector junction temperature.

A new technique for modeling and characterizing the thermal coupling is proposed. The modified five element compact model explains the thermal coupling between adjacent DIBJTs. The thermal coupling varies inversely with the space between DIBJTs. The thermal coupling coefficients of three test structures are measured and the relation is explained in mathematical form. The measurements and theory provide engineers a design criterion when thermal effects are considered.

The simulations were done primarily with the program, Davinci, and the measurements were taken with a HP4142B Modular DC Source/Monitor which is interfaced with the software program, ICCAP.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS iii

ABSTRACT iv

LIST OF ILLUSTRATIONS xiv

LIST OF TABLES xv

Chapter Page

1. INTRODUCTION 1

2. LITTERATURE REVIEW 7

2.1 Introduction 7

2.2 Bipolar Junction Transistor Models 8

2.2.1 Ebers-Moll Model 8

2.2.2 Gummel-Poon Model 10

2.2.3 Vertical Bipolar Inter-Company Model 11

2.3 Process Technology in VIP10 13

2.3.1 Silicon on insulator (SOI) technology 13

2.3.2 Double polysilicon BJT structure 15

2.4 Thermal Property for Electronic Materials 17

2.4.1 Major thermal values for electrical materials 17

2.4.2 General heat equation 18

2.4.3 Thermal resistance by heat equation.. 19

2.4.4 Thermal capacitance by heat equation..................................... 21

2.5 Thermal Network and Two Simulation Examples 21

2.5.1 Thermal network in the VBIC model 21

2.5.2 Calculation of thermal characteristics
in the DAVINCI simulation tools 22

2.6 Thermal Effects………. 28

2.6.1 Self-heating... 28

2.4.2 Thermal adjacent coupling 29

2.7 Thermal Modeling for BJT 30

2.8 Compact Thermal Model for Dielectrically Isolated BJT 33

2.9 Review of Compact Thermal Model for DIBJT.................................... 37

2.10 Summary... 41

3. THERMAL CHARACTERISTICS IN A SINGLE BJT 43

3.1 Introduction... 43

3.2 Review of Five Element Compact Thermal Model for DIBJT 44

3.3 Thermal Characteristic for a Multi-Finger DIBJT.................................. 53

3.4 Five Element Compact Model for a Multi-Finger DIBJT 56

3.5 Thermal Resistance by the Junction Temperature.................................. 61

3.6 Compare the Thermal Resistance Values
in the Five Element Compact Model 63

3.7 Conclusion 65

4. THERMAL ADJACENT COUPLING BETWEEN BJTS 67

4.1 Introduction 67

4.2 Thermal Adjacent Device Model 68

4.3 Temperature Measurement 74

4.4 Measurement of Thermal Adjacent Coupling 76

4.5 Measurement of Thermal Adjacent Coupling in Series 85

4.6 Conclusion 93

5. CONCLUSION AND FUTURE WORK 95

Appendix

A. LAYOUTS OF THE TEST STRUCTURES 99

B. ONE SAMPLE CODE OF DAVINCI 102

REFERENCES 107

BIOGRAPHICAL INFORMATION 118

LIST OF ILLUSTRATIONS

Figure Page

1.1 Cross section of VIP10 transistor 4

2.1 Ebers-Moll model for NPN transistor 9

2.2 Gummel-Poon model 10

2.3 VBIC model 12

2.4 Schematic of the SIMOX technology 13

2.5 Schematic of the wafer bonding technology 15

2.6 Process flows for epitaxial-base, double-poly self-aligned bipolar transistor. (a) EAS (Epitaxy-After-Sidewall) approach, (b) EBS (Epitaxy-Before-Sidewall) approach.. 16

2.7 Simple thermal network in the one-dimensional case (a) Front view (b) Top view 19

2.8 Thermal network in the VBIC model.. 22

2.9 A constant heat source structure. The heat source is on the top and the heat sink is on the bottom 25

2.10 A resistor heat source structure. The p-type doped resistor is located on the top and the heat sink is on the bottom. The voltage is applied between two electrodes 25

2.11 Simulation results for structure in Figure 2.9, which is simulated by Davinci and then curve fitted – the dots are the simulated results and the line is curve fitted to one pole model of the thermal impedance (Equation 2.18).. 26

2.12 Simulation results for structure in Figure 2.10, which is simulated by Davinci and then curve fitted – the dots are the simulated results and the red line is curve fitted one pole model of the thermal impedance (Equation 2.18) 27

2.13 The VBIC model output characteristics for a device at V_{BE} = 0.7 [V]. Curves labeled with a T value are I-V characteristic with self-heating off by varied temperature from 300 K to 304 K. The I-V characteristic with self-heating on with a fixed ambient temperature at 300 K is also shown. 28

2.14 Simplified circuit model for the effect of the thermal adjacent coupling 30

2.15 Compact model of the thermal network 31

2.16 Simple DIBJT diagram 33

2.17 Physical diagram to logical thermal diagram 34

2.18 Top view of a BJT with a concept of the cooling fin 35

2.19 Cross section of the simple DIBJT geometry 37

2.20 Plot of the transient thermal impedance of simulated data (Model) by equation (2.31) and simulated data (ANSYS) using 3-D ANSYS 40

3.1 Five element compact thermal model for DIBJT 44

3.2 Model for the Si tub 45

3.3 Two dimensional truncated pyramid structure in x-y dimension 46

3.4 Two dimensional truncated pyramid structure in z-y dimension 47

3.5 Two dimensional truncated pyramid model for the isolation oxide 48

3.6 Two dimensional truncated pyramid model for the silicon substrate 49

3.7 Top view of silicon tub and trench 50

3.8 Top view of silicon tub, trench and outer silicon 51

3.9 Half structure of double poly DIBJT. The bottom is the thermal boundary where the heat flows through. All other sides are the adiabatic boundaries where no heat flows through. 53

3.10 Simulation setup - the specific positions for measuring temperature 54

3.11 Electro-thermal model for the DIBJT (Three-pole model) 55

3.12 Three-pole model and curve fitting results 55

3.13 Modified five element compact model.. 57

3.14 Simulation and curve fitting results of first condition. $Z_{TH} = Z_{TUB} + Z_{bOx}$ when $Z_{dist} \to \infty$, $Z_{tr} \to \infty$, $Z_{W} \to 0$ 58

3.15 Simulation and curve fitting results of second condition. $Z_{TH} = Z_{TUB} + Z_{tr}$ when $Z_{bOx} \to \infty$, $Z_{W} \to \infty$, $Z_{dist} \to 0$ 59

3.16 Simulation and curve fitting results of third condition. $Z_{TH} = Z_{TUB} + Z_{tr} + Z_{dist}$ when $Z_{bOx} \to \infty$, $Z_{W} \to \infty$ 59

3.17 Final thermal impedance values for the five element compact model after curve fitting. 60

3.18 Final thermal impedance values for the five element compact model in the thermal circuit. Units are [K/W] for the thermal resistance and [W-sec/K] for the thermal capacitance.. 60

3.19 I-V characteristics at V_B=0.74 [V] and V_C = 1 to 3 [V]................................ 62

3.20 Temperature profile at the 2.14 um from the top surface............................... 62

3.21 The difference between two methods for three devices [%] 64

4.1 Thermal model for the thermal adjacent coupling between two BJTs. BJT1 and BJT2 are connected by the common $Z_{dist,m}$ which is useful for calculating the thermal adjacent coupling coefficient in BJT2 due to the self-heating in BJT1 69

4.2 Top view of two adjacent BJTs.. 70

4.3 Simplified circuit model for the effect of the thermal adjacent coupling 72

4.4 VCVS thermal adjacent coupling model 73

4.5 Forward Gummel setup for measuring temperature 74

4.6 One sample of measurements 75

4.7 Diagram of the test structure 1. The distance between the central BJT and the outer BJT is 2 um 76

4.8 An example of the temperature measured for the test structure 1 in various powers consumed by the central BJT 78

4.9 Diagram of the test structure 2. The distance between the central BJT and the outer BJT is 2 um 78

4.10 An example of the temperature measured for the test structure 2 in various powers consumed by the central BJT 80

4.11 The transient response of the thermal adjacent coupling impedance for the test structure 1. The results are normalized 82

4.12 The transient response of the thermal adjacent coupling impedance for the test structure 2. The results are normalized 82

4.13 Thermal adjacent coupling coefficient of the test structure 1. The space between trenches is varied from 2 um to 16 um 84

4.14 Thermal adjacent coupling coefficient of the test structure 2. The space between trenches is varied from 2 um to 16 um 84

4.15 Diagram of the test structure 3. The distance between BJTs is 2 um 86

4.16 Partial diagram of the test structure 3 to measure the thermal adjacent coupling coefficient in position one 86

4.17 One sampled measurement results of position one in the test structure 3 88

4.18 Partial diagram of the test structure 3 to measure the thermal adjacent coupling coefficient in position two 89

4.19 One sampled measurement results of position two in the test structure 3 90

4.20 Partial diagram of the test structure 3 to measure
the thermal adjacent coupling coefficient in position three 91

4.21 One sampled measurement results of position three
in the test structure 3. 92

4.22 Thermal adjacent coupling coefficients in the test structure 3........................ 93

LIST OF TABLES

Table Page

1.1 Thermal conductivity of Si and SiO_2 2

1.2 National Semiconductor complementary bipolar processes 3

2.1 Thermal resistances, thermal capacitances and thermal time constants
for two structures in Figure 2.9 and Figure 2.10 27

2.2 Comparison between electrical terms and thermal analogy terms 31

3.1 The thermal resistance values in the five element compact model
by the equation of the compact model and the extraction method
using thermal simulation 63

4.1 Averaged thermal adjacent coupling coefficients of the structure 1
and the structure 2 81

4.2 Averaged thermal coupling coefficients of the structure 1
and the structure 2 in the measurements and the simulations. 81

4.3 Thermal resistances in a single BJT and a BJT (as a ratio of
the R_{TH} of an isolated device) surrounded by four BJTs and
eight BJTs. The space between the trenches is 2 um. 85

4.4 Averaged thermal adjacent coupling coefficients of the structure 3 92

CHAPTER 1

INTRODUCTION

Since the integrated circuit (IC) was invented in 1960, the operating speed of semiconductor devices has steadily increased and the number of semiconductor devices in an IC chip has grown according to Moore's Law. A size reduction of the devices by improvements in fabrication technology is the primary reason for this increase in the operating speed and the number of semiconductor devices. This trend has lead to the rapid increase of power consumption and heat generation. As a result of this increase, the thermal characterization of semiconductor devices has become more important.

The dielectrically isolated bipolar junction transistor (DIBJT) is fabricated on a silicon-on-insulator wafer, which has an isolation oxide between the bulk wafer and the epitaxial Si layer [1]-[6]. Each bipolar junction transistor (BJT) is also surrounded by an isolation trench, which is usually fabricated by oxide or other insulated material [5]. This offers many advantages, such as reduced parasitic capacitances and leakage currents, increased packing density and improved radiation hardness [1]. However, a major disadvantage of this device is an increase in self-heating [7]-[12]. It is especially important to consider thermal characteristics of the DIBJT [7][8]. The heat generated by the DIBJT device cannot easily transfer to the heat sink. The oxide used in the trench and buried isolation has a low thermal conductivity (Table 1.1) and blocks the

flow of heat away from the device. This causes higher operating temperature, which degrades the device performance. That in turn substantially affects the frequency and time responses [9]. The thermal resistance of a DIBJT can be three or more times larger than that of a junction isolated BJT which is fabricated on the bulk Si wafer [7].

Table 1.1 Thermal conductivity of Si and SiO_2 [52]

	Si	SiO2
Thermal conductivity [W/cm-K]	1.412	0.014

A double poly DIBJT which is used for this research and developed by National Semiconductor is shown in Figure 1.1 [13]. This process, called VIP10, offers a good solution for today's high speed amplifiers. This provides high bandwidth and low power consumption. The VIP10 is the latest designs in National Semiconductor's VIP (Vertically Integrated PNP) (Table 1.2) [13].

Thermal effects in the IC can be categorized into three different cases; self-heating in each device [11]-[12], thermal coupling between transistors on the same chip [14]-[19], and package thermal effects which raises the overall temperature of the chip [8]-[11]. In this paper, self-heating and thermal coupling is analyzed for the DIBJT and the modeling and characterization of thermal effects are also explained. The thesis is described as follows.

Table 1.2 National Semiconductor complementary bipolar processes [13]

Process	**VIP1**	**VIP2**	**VIP3**	**VIP10**	**Units**
Year	1986	1988	1994	2000	
NPN f_t	0.4	0.8	3.0	9.0	GHz
NPN β	250	250	150	100	
NPN V_a	200	150	150	120	V
PNP f_t	0.2	0.5	1.6	8.0	GHz
PNP β	150	80	60	55	
PNP V_a	60	40	50	40	V
Cjs	2.0	1.5	0.5	0.005	pF
Emitter Width	15	11	2	1	um
Minimum Transistor Area	20000	18000	2400	300	um^2
Max Supply V	36	36	32	12	V
Isolation	JI	JI	JI	DI	
Other	Implanted Emitter, Base	Implanted Emitter, Base	Poly Emitter	Double Poly	

* JI – Junction Isolation

* DI – Dielectric Isolation

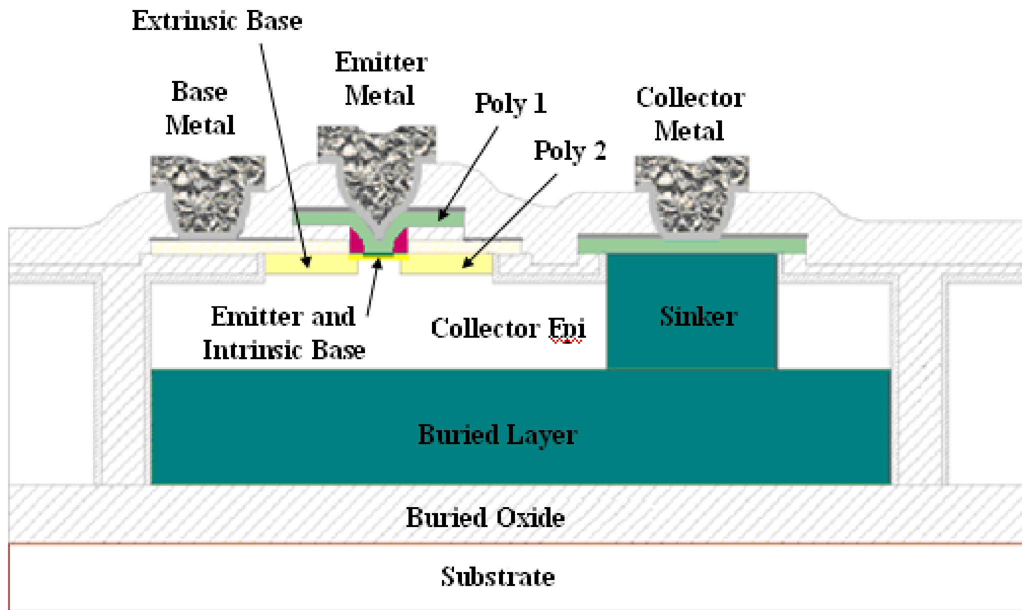


Figure 1.1 Cross section of VIP10 transistor [13]

In chapter 2, a brief review of bipolar junction transistor models is introduced: the Ebers-Moll model, the Gummel-Poon model and the VBIC (Vertical Bipolar Inter-Company) model. There is a discussion on how each model improved on its predecessor.

VIP10 process provides the BiCMOS technology to fablicate an integrated circuit. This VIP10 process uses the silicon-on-insulator and double poly-silicon technologies to provide a good solution for today's high speed amplifiers, which provides wide bandwidth and low power consumption. These two technologies are briefly reviewed. General heat transfer in various cases and the relationship between electrical behavior and thermal behavior in a BJT is briefly reviewed. The definition of

thermal resistance and thermal capacitance is discussed, and an equivalent thermal network for the VBIC model is introduced. The method used to calculate the theoretical thermal impedance of a one-dimensional material is introduced. The method to use thermal CAD (Computer Aided Design) to find thermal impedance is also explained. The thermal effects in the BJT are explained – self-heating and adjacent coupling.

The most widely adopted thermal model consists of one thermal resistance and one thermal capacitance. This model described in chapter 3 is used in the VBIC model. The five element compact model suggested by Carter [74][75] is studied, and a new method to extract each value of the five element compact model is proposed by using the thermal simulation tool, Davinci. Each value of the five element compact model is determined for the three BJTs (1X2X1, 1X5X1 and 8X5X1). The notation describes the number of emitters X length of each emitter X width of each emitter. The five element model is calculated in both the method which is suggested by Dr. Carter and the simulation method. Then these values are compared.

In chapter 4, a theoretical model for thermal adjacent coupling is proposed. The model is a modified version of the five element compact model which is explained in chapter 3. Mathematical expression of the thermal adjacent coupling is proposed. The voltage-controlled voltage-source concept is adopted into the thermal network to implement the thermal adjacent coupling between the BJTs. The technique used to measure the temperature of the BJT is explained. This method uses the forward Gummel setup.

Two structures are designed to measure the thermal coefficient between BJTs. The first structure has a central BJT surrounded by four BJTs that intercept the heat flow. A second structure has a central BJT surrounded by eight BJTs that intercept the heat flow. Each structure is measured to find the thermal adjacent coupling, and the same structure is simulated for comparison. The distance between the trenches for each device varies from 2 μm to 16 μm. The thermal coupling is forced as a function of this distance. Another structure which has eight columns by three rows of BJTs is designed to measure the thermal adjacent coupling between the central BJT and the left side BJTs.

Finally, conclusions are given and proposed future extensions are provided.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The bipolar junction transistor (BJT) was invented by a research team at Bell laboratories in 1947. Since then transistor theory has been extended to include high frequency, high power and switching behaviors. Many breakthroughs have been made in transistor technology, particularly in zone-refining, diffusion, epitaxial, planar, ion implantation, lithography, and dry etching technologies.

It is important to define an accurate model for the bipolar junction transistor. Three primary models have been developed: the Ebers-Moll model [21][22], the Gummel-Poon model [23][24] and the VBIC (Vertical Bipolar Inter-Company) model [25]-[28]. The general summary of these models are introduced in section 2.2 and the improvements from the previous model are explained briefly.

High performance BiCMOS technology is mainly applied to mainframe computers, high speed analog-digital systems, and optical fiber network systems and so on[29]-[31]. The VIP10 process also provides BiCMOS technology for design of an integrated circuit. This VIP10 process uses the silicon-on-insulator and double poly-silicon technologies to provide a good solution for today's high speed amplifiers. The VIP10 process device provides wide bandwidth and low power consumption. These

two technologies (silicon-on-insulator and double poly-silicon technologies) are briefly reviewed.

General heat transfer in various cases is explained in [32][33]. However the main concern here is the thermal characteristic of a bipolar junction transistor and the relationship between electrical behavior and thermal behavior in a BJT. In this chapter, a general definition of thermal impedance is explained, and the thermal network in the VBIC model is also explained. The mathematical expressions used in the simulation tool, Davinci, are described, and the thermal effects in the BJT are explained – self-heating and adjacent coupling.

2.2 Bipolar Junction Transistor Models

2.2.1 Ebers-Moll Model

The Ebers-Moll model which is shown in Figure 2.1 is a one-dimensional BJT model, which focuses attention on the recombination in the base region [21]. When it was developed, the reverse current gain was more significant than it is in modern epitaxial transistors. The Ebers-Moll terminal current relations depend on the superposition of two current components: one coming from the emitter junction and the second from the collector. The Ebers-Moll model is based on several assumptions such as low level injection, uniform doping in each region with abrupt junctions, one-

dimensional current flow, negligible recombination-generation in the space charge regions and negligible electric fields outside of space charge regions.

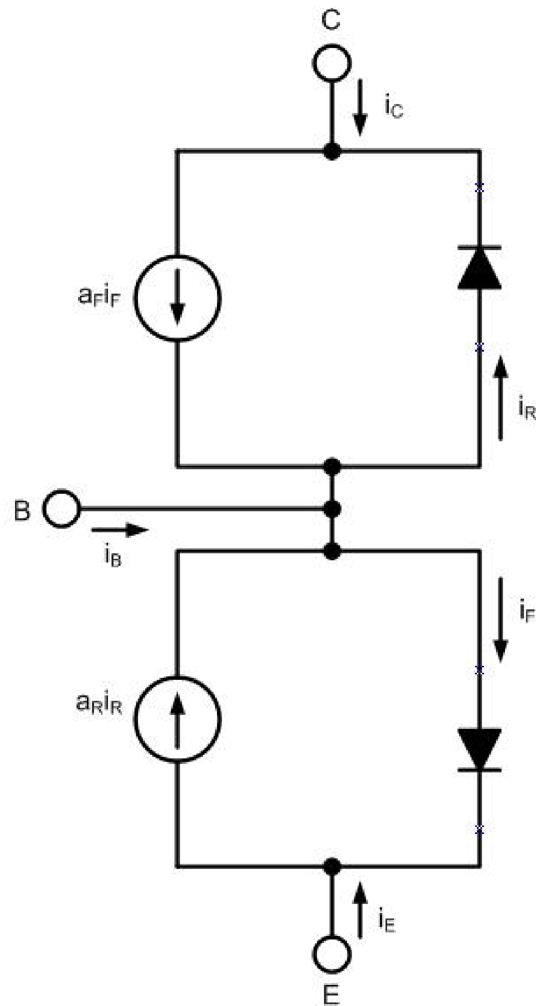


Figure 2.1 Ebers-Moll model for NPN transistor

The Ebers-Moll model contains two diodes and two current sources (Figure 2.1). The two diodes represent the base emitter and base-collector diodes. The current sources quantify the transport of minority carriers through the base region. These

current sources depend on the current through each diode. I_E is the saturation current of the base-emitter diode and I_C is the saturation current of base-collector diode. The α_F term is the forward transport factor and the α_R term is the reverse transport factor.

2.2.2 Gummel-Poon Model

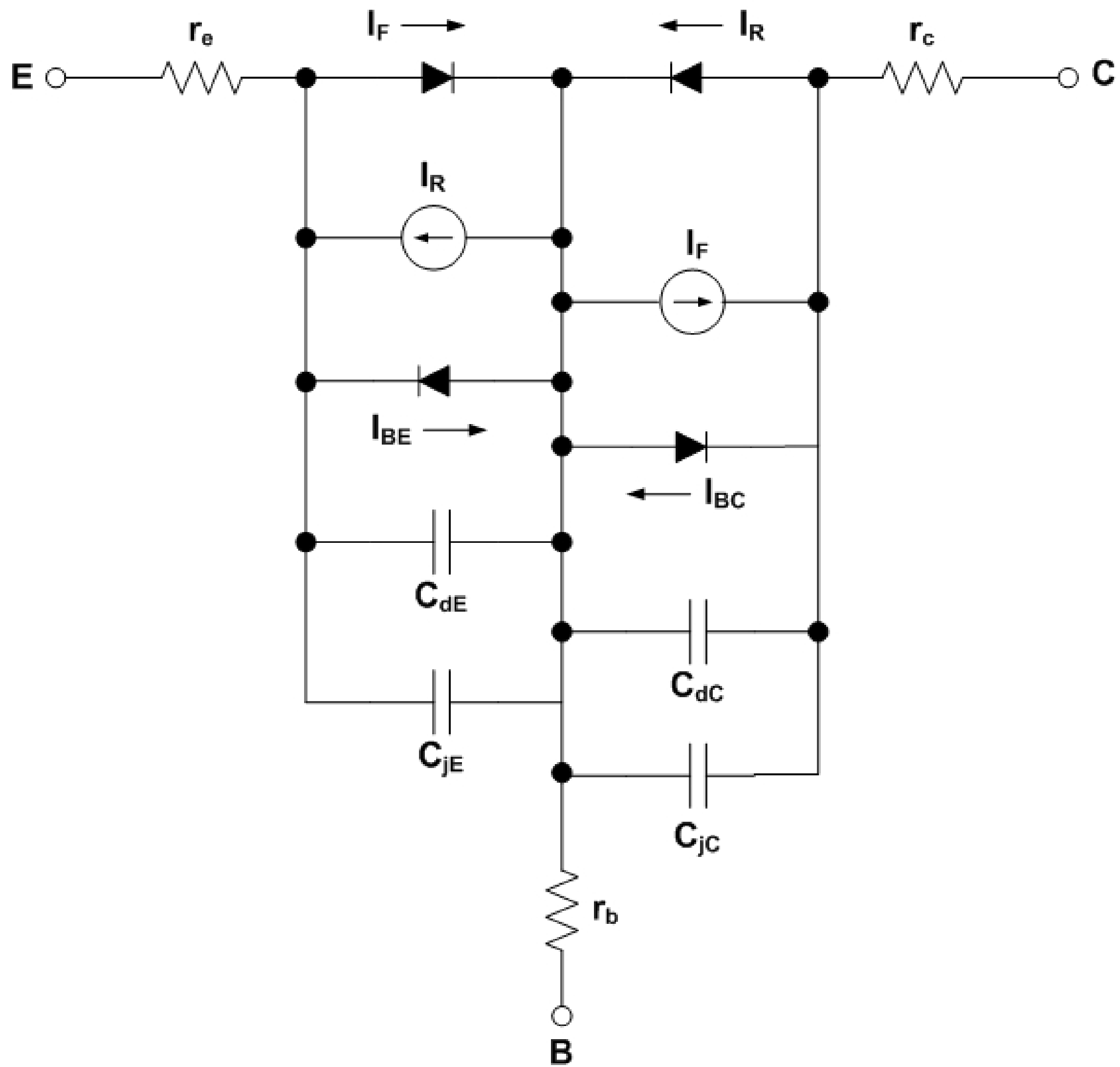


Figure 2.2 Gummel-Poon model

The Ebers-Moll model does not take into account the base resistance, the resistance in the quasi-neutral collector region, the non-uniform doping profiles, and charges in the depletion layer widths with bias voltages. However, it is widely used in the nonlinear circuit analysis program called SPICE (Simulation Program with Integrated Circuit Emphasis) and gives sufficiently accurate results for many applications if the base resistance and the resistance in the quasi-neutral collector region are added to the model [23]. The Ebers-Moll model also neglects the hole-electron generation in the reverse-biased collector-base depletion region and the recombination in the forward-biased emitter-base depletion region. The Gummel-Poon model shown in Figure 2.2 takes into account these effects.

The major improvements in the Gummel-Poon model are the inclusion of the high injection effect, Early effect, terminal series resistance, generation/recombination current sources, auger recombination, band gap narrowing, current crowding and the Kirk effect.

2.2.3 Vertical Bipolar Inter-Company Model

The Gummel-Poon(GP) model is the most widely used BJT model, but it has become too inaccurate for some modern technologies. BJT device technology such as reduced base width, shrinking device dimensions and changes in device structures have improved over the past few decades [25]. These improvements are the major reason for the decrease in accuracy of the GP model. As modern transistors trend toward smaller dimensions, second order effects become more important. In 1995, a US industry

consortium proposed a new bipolar transistor model (Figure 2.3), called VBIC95 (Vertical Bipolar Inter-Company) [25]. The VBIC95 model aimed to be similar to the standard Gummel-Poon model as much as possible. Today, it has changed its name to VBIC. The VBIC model includes several features that make it distinct from the GP model such as the parasitic substrate PNP transistor, the quasi-saturation behavior, self-heating and excess phase effects [26], Early effect modeling based on depletion charge, an improved depletion and diffusion charge model, base-emitter breakdown modeling, self-heating modeling and improved temperature modeling [28].

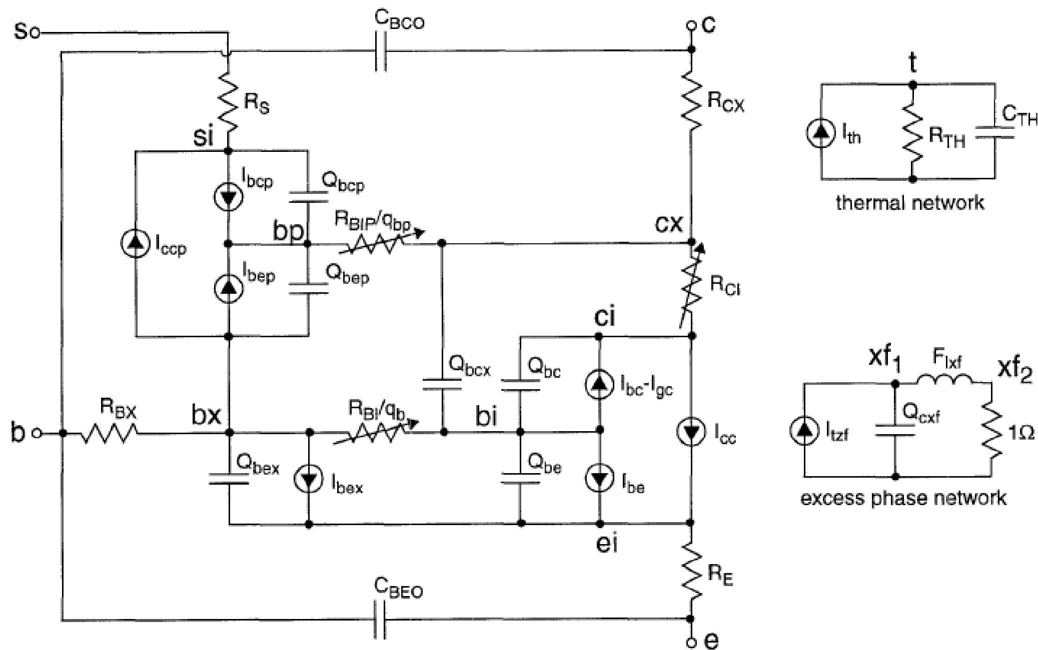


Figure 2.3 VBIC model [25]

2.3 Process Technology in VIP10

2.3.1 Silicon on insulator (SOI) technology

SOI technology has been developed to increase operating speed by reducing parasitic area and to increase soft-error immunity for high packing density of the random access memory [29]-[31][34]. Many efforts have been done to provide the good methods to fabricate SOI substrates [35]-[37].

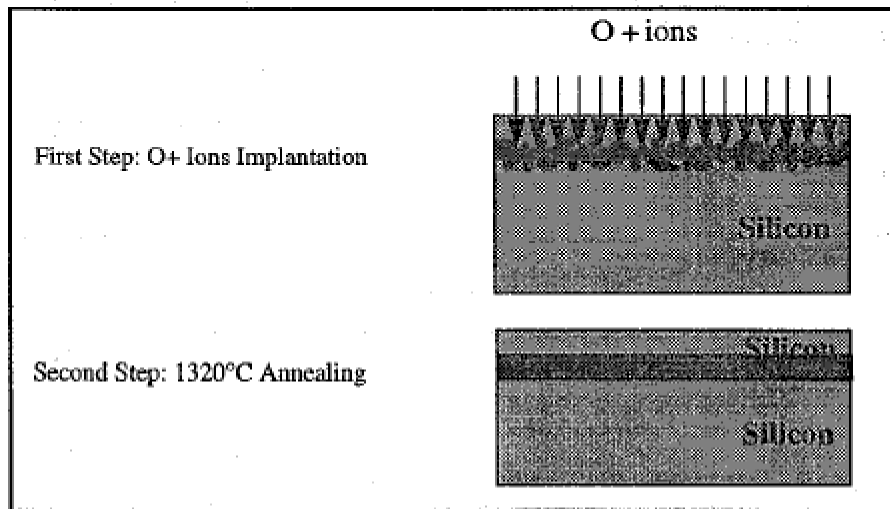


Figure 2.4 Schematic of the SIMOX technology [30]

SOI substrates can be made of bulk silicon wafers by oxygen ion implantation into the surface of the silicon wafer [38]-[40]. The simple schematic of the SIMOX technology is shown in Figure 2.4. The isolation oxide is formed by implantation of oxygen below the surface of the wafer. This implantation requires extremely high doses

compared to implanting dopants. The structure resulting from such a high-dose implant of oxygen depends strongly upon the dose and energy of the implant. In conventional ion implantation, the ions damage the silicon crystal structure. As a result, following implantation, the wafer is annealed and the crystal structure is reestablished by a process called solid-phase epitaxy. This SIMOX technology can produce thin SOI material. The main disadvantage of the SIMOX technology is the use of non-standard equipment and the need of higher temperature annealing.

SOI substrates can also be obtained by thinning silicon wafers bonded to an insulator layer on the other silicon substrates [40]-[42]. This is another method used to fabricate SOI structures (Figure 2.5). The wafer which will become the substrate is oxidized, creating the desired isolation oxide thickness. A second wafer which will become the site for active devices is pressed into close contact with the substrate wafer, and this combined wafer is heated in a furnace. Bond strength generally increases with temperature. Finally, the second wafer (active device layer) is thinned to leave a final silicon layer of the desired thickness. This thinning can be done several ways. A major amount of the silicon can be removed by etching or grinding. Wafer bonding is the preferred method of producing thick SOI material where the isolation oxide and silicon active device layer are thicker than 1 μm. Bonded SOI substrates are suitable for fabricating both vertical and lateral bipolar transistors.

The soft-error and latch-up problems are a major concern not only for high density memory circuits but for bipolar logic circuits. SOI substrates can be used to improve these problems. A major disadvantage of full dielectrically isolated structure is

poor thermal conductivity caused by the dielectric material. The self-heating effects of bipolar transistors on SOI substrates are reported through measurements and simulations [43].

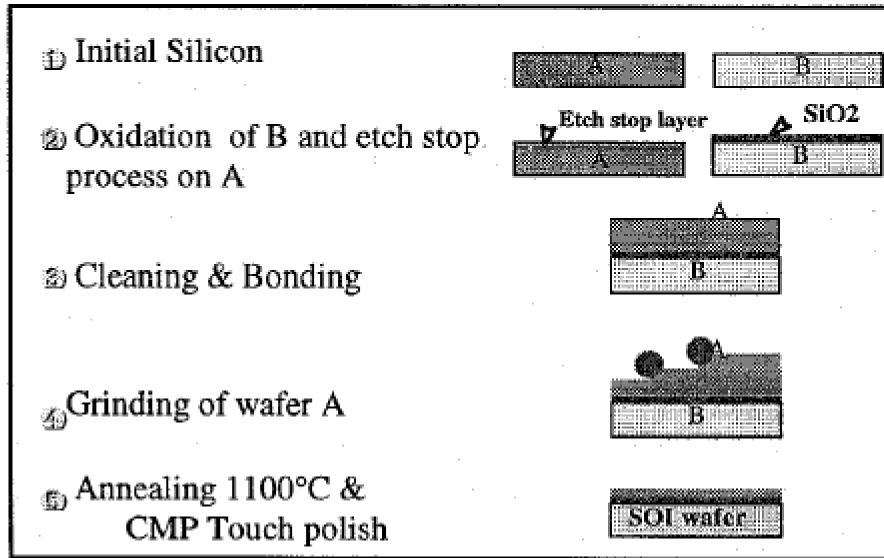


Figure 2.5 Schematic of the wafer bonding technology [30]

2.3.2 Double polysilicon BJT structue

High speed bipolar VLSI has depended on available high speed NPN BJT devices, whose parasitic capacitance has been reduced by using polysilicon in the bipolar technology [44]-[48]. The single polysilicon BJT uses polysilicon in the emitter regions. However, a double polysilicon BJT uses it in both emitter and base regions (Figure 2.6). The polysilicon layer is used as a diffusion source to form a shallow emitter junction. This serves as a low resistivity contact for the shallow emitter. The polysilicon layer is as heavily doped as the single crystal silicon emitter. In a double

polysilicon BJT device, heavily doped extrinsic base regions are formed and contacted by boron doped polysislicon layers. Emitter and base areas of this BJT device are generally much smaller than those of single polysilicon BJT device. The reduced base parasitic resistances and base collector capacitances especially combined with the double polysilicon BJT device are the reasons for the increase in the circuit speed.

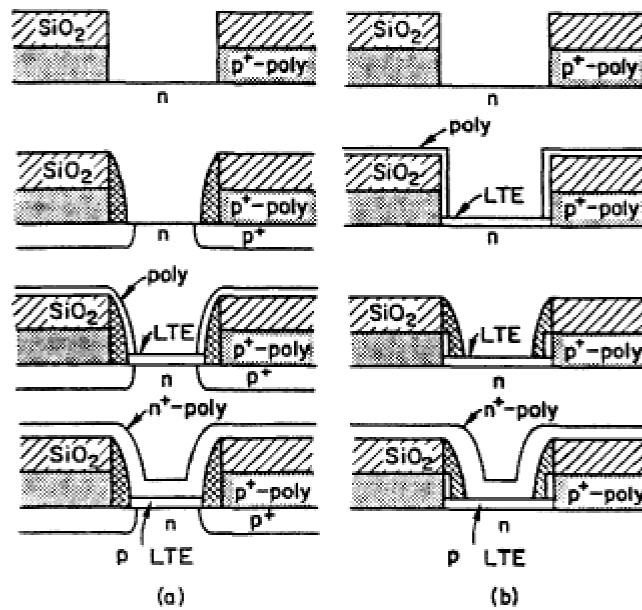


Figure 2.6 Process flows for epitaxial-base, double-poly self-aligned bipolar transistor. (a) EAS (Epitaxy-After-Sidewall) approach, (b) EBS (Epitaxy-Before-Sidewall) approach [48]

2.4 Thermal Property for Electronic Materials

2.4.1 Major thermal values for electrical materials

Heat exists in a solid material because of the presence of energy. Most of material can be categorized by two types – insulator or conductor. Phonon generation from the random vibration of atoms in a lattice structure is the largest source of heat. However, conductors transfer most of their thermal energy using free electron movement. Each material has different primary transfer methods for heat flow. Therefore each material has a unique set of thermal and physical properties.

Thermal conductivity is defined by the time rate of heat transfer between opposite faces of a unit surface of material through a unit length, where the temperature difference is one degree Kelvin [49]. Thermal conductivity indicates the efficiency of a material to allow heat flows from a higher temperature region to a lower temperature region as given by :

$$H = \kappa \frac{dT}{dx} \tag{2.1}$$

where H is the heat flux, κ is the thermal conductivity and dT/dx is the temperature gradient. The units are [W/m^2] for H, [W/m-K] for κ, and [K/m] for dT/dx in steady state.

Materials can absorb heat energy and release it. Thermal capacity is defined as the amount of thermal energy required to raise the temperature of one mole of material by one Kelvin [50], that is :

$$C = \frac{dQ}{dT} \tag{2.2}$$

where C is the heat capacity, Q is the thermal energy and T is the temperature. The units are [W-s/mol-K] for C, [W-s] for Q and [K] for T. A more common property for the thermal capacity is the specific heat, which is the thermal capacity divided by the mass. The unit of the specific heat is [W-s/Kg-K].

2.4.2 General heat equation

The general time dependant differential equation for heat flow with an internal heat source is [51]:

$$\vec{\nabla}\left(\kappa \cdot \vec{\nabla} T\right) = -Q_V + \rho \cdot C \frac{\partial T}{\partial t} \tag{2.3}$$

where T is temperature as a function of a time and space, Q_V is the thermal energy generated by the internal heat source in a unit volume, κ is the thermal conductivity, ρ is the density of the material, and C is the heat capacity of the material.

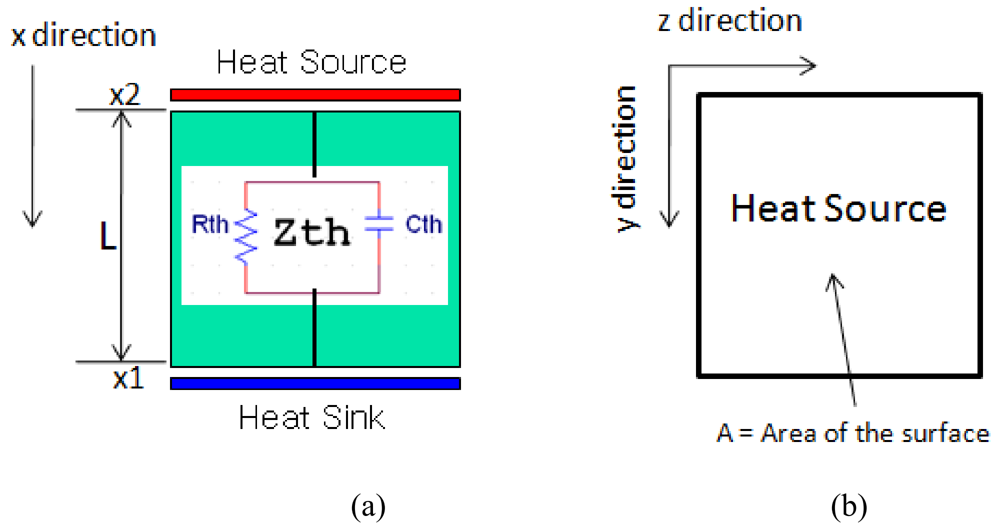
2.4.3 Thermal resistance by heat equation

The general definition of the thermal resistance is the temperature difference across a material when a unit of heat energy flows through it in a unit time. In steady state, equation (2.3) can be modified to

$$\vec{\nabla}\left(\kappa \cdot \vec{\nabla} T\right) = -Q_V \qquad (2.4)$$

$$\vec{\nabla}\left(\kappa \cdot \vec{\nabla} T\right) \cdot dxdydz = -Q_V \cdot dxdydz \qquad (2.5)$$

$$\iiint \vec{\nabla}\left(\kappa \cdot \vec{\nabla} T\right) \cdot dxdydz = -\iiint Q_V \cdot dxdydz \qquad (2.6)$$



(a) (b)
Figure 2.7 Simple thermal network in the one-dimensional case.
(a) Front view (b) Top view

In the one dimensional case (x-direction in Figure 2.7), equation (2.6) is modified to

$$\kappa \cdot A \cdot \frac{dT}{dx} = -Q \qquad (2.7)$$

where A is the area of the thermal source from $\iint dydz$ and Q is the thermal energy in the x-direction from $\iiint Q_V \cdot dxdydz$.

$$dT = -\left(\frac{Q}{\kappa \cdot A}\right)dx \tag{2.8}$$

Integrating both sides of the equation (2.8)

$$\int_{T1}^{T2} dT = \frac{-Q}{\kappa \cdot A}\int_{x1}^{x2} dx \tag{2.9}$$

$$\Delta T = T2 - T1 = Q\frac{L}{\kappa \cdot A} \tag{2.10}$$

where L is the thickness between the heat source and the heat sink :

$$L = x2 - x1 \tag{2.11}$$

Then the thermal resistance can be defined as :

$$R_{TH} = \frac{\Delta T}{Q} = \frac{L}{\kappa \cdot A} \tag{2.12}$$

where ΔT is the temperature difference between the heat source and the heat sink, Q is the thermal energy, L is the thickness between the heat source and the heat sink, κ is the thermal conductivity, and A is the area of the thermal source. The units are [W/m-K] for κ, [m] for L and [m^2] for A.

2.4.3 Thermal capacitance by heat equation

The general definition of the thermal capacitance, C_{TH}, is the heat quantity stored in a particular volume. In equation (2.3), the last term, $\rho \cdot C \cdot \partial T / \partial t$, describes the time-varying portion of the heat flow. In the one-dimensional case (Figure 2.7), the thermal capacitance is :

$$C_{TH} = c_P \cdot \rho \cdot V \tag{2.13}$$

where c_P is the specific heat of the material, ρ is the density of the material, and V is the volume of the material ($V = A \cdot L$). The units are [W-s/Kg-K] for c_P, [Kg/m^3] for ρ, and [m^3] for V.

2.5 Thermal Network and Two Simulation Examples

2.5.1 Thermal network in the VBIC model

The simplest thermal network which is used in the VBIC (Vertical Bipolar Inter-Company) model associates all of the thermal resistance from the device with a single thermal resistance and all of the thermal capacitance of the device with a single thermal capacitance. This network is shown in Figure 2.8. The total thermal resistance is represented by R_{TH} [K/W] and the total thermal capacitance is represented by C_{TH} [W/K]. I_{TH} [A] is the power which is consumed by the device divided by 1 volt and dt is the temperature of the device after I_{TH} is applied to the combination of R_{TH} and C_{TH}.

The ambient temperature is represented by tl. So, the device temperature (dt) for the thermal network can be calculated by equation (2.14).

$$dt = tl + I_{TH} \cdot R_{TH}\left(1 - \exp\left(-\,{}^{t}\!/_{\tau}\right)\right) \tag{2.14}$$

where τ is the thermal time constant ($\tau = R_{TH} \cdot C_{TH}$) in seconds.

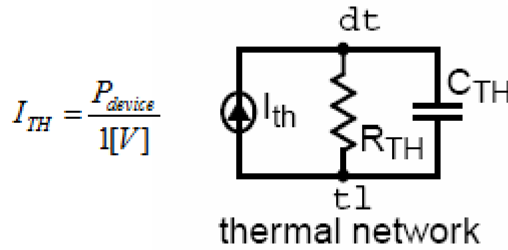


Figure 2.8 Thermal network in the VBIC model [25]

2.5.2 Calculation of thermal characteristics in the DAVINCI simulation tool

The thermal impedance cannot be calculated directly by Davinci, which is a three-dimensional device simulator that models the electrical, thermal, and optical characteristics of semiconductor devices. However, Davinci can calculate the lattice temperature using the heat equation. A Davinci module called the Lattice Temperature Advanced Application Module (LT-AAM) can be used to perform non-isothermal electrical analysis by simultaneously solving the electrical and thermal equations. The current flow and recombination of carriers increases the lattice temperature in a device. To compute the spatially-dependent lattice temperature, the heat flow equation is [52]:

$$\rho \cdot c_P \frac{\partial T}{\partial t} = H + \vec{\nabla}\left(\lambda(T)\vec{\nabla}T\right) \tag{2.15}$$

where ρ is the mass density of the material, c_P is the specific heat of the material, H is the heat generation term and λ is the thermal conductivity of the material. The units are [g/cm^3] for ρ, [J/g-K] for c_P, [W/cm^3] for H, and [W/cm-K] for λ. The total heat generation in the semiconductor is modeled by equation (2.16) [52].

$$H = H_n + H_p + H_U \tag{2.16}$$

where H_n is the lattice heating due to electron transport, H_p is the lattice heating due to hole transport and H_U is the lattice heating due to carrier recombination/generation.

After solving the heat flow equation, Davinci calculates the time dependent lattice temperature at each node. This temperature can be used to compute the thermal impedance from the node and the heat sink. In equation (2.14) the temperature, dt, is related to the thermal current and the thermal step response of the thermal impedance. Equation (2.14) can be modified as :

$$\frac{dt(t) - tl}{I_{TH}(t)} = R_{TH}\left(1 - \exp\left(-\,t/\tau\right)\right) \tag{2.17}$$

Equation (2.17) can be rewritten as :

$$Z_{TH}(t) = \frac{T_{source}(t) - T_{\sin k}}{P(t)} = R_{TH}\left(1 - \exp\left(-\,t/\tau\right)\right) \tag{2.18}$$

where $Z_{TH}(t)$ is the thermal step response of the thermal impedance which consists of one thermal resistance and one thermal capacitance [$R_{TH} \| C_{TH}$], $T_{source}(t)$ is the time dependent temperature at each node [dt], $T_{\sin k}$ is the constant temperature at the heat sink [tl], and $P(t)$ is the total power [$I_{TH}(t) \times 1[V]$]. The units are [K] for $T_{source}(t)$, [K] for $T_{\sin k}$, and [W] for $P(t)$. It is assumed that $T_{source}(t)$ is the time dependent maximum lattice temperature in the device. The usual way to characterize the thermal network is the analysis of the thermal response to a step in the applied power, and this thermal response can be called the transient thermal impedance [53]. The transient thermal impedance is called the thermal step response in this paper. The thermal step response of the thermal network can be expressed by a multi-pole model as shown in equation (2.19).

$$
\begin{aligned}
Z_{TH}(t) = R_{TH1}\left[1 - \exp\left(\frac{-t}{\tau_{TH1}}\right)\right] + R_{TH2}\left[1 - \exp\left(\frac{-t}{\tau_{TH2}}\right)\right] \\
+ \cdots + R_{THn}\left[1 - \exp\left(\frac{-t}{\tau_{THn}}\right)\right]
\end{aligned}
\tag{2.19}
$$

To extract values for the thermal resistances and thermal time constants in equation (2.19), a curve fitting method is used. Origin [54], a curve fitting program provides various functions to analyze data. The optimization function in ICCAP2008 is also used [55].

Two examples are done to verify that the temperature computed by Davinci can be used to calculate the thermal impedance in the time domain. One uses a constant heat source to generate heat and the other uses a resistor source to generate heat.

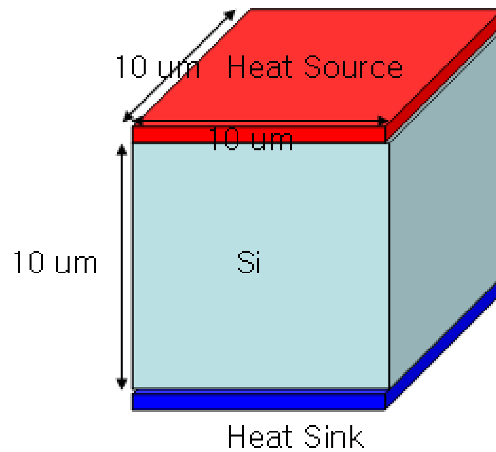


Figure 2.9 A constant heat source structure. The heat source is on the top and the heat sink is on the bottom.

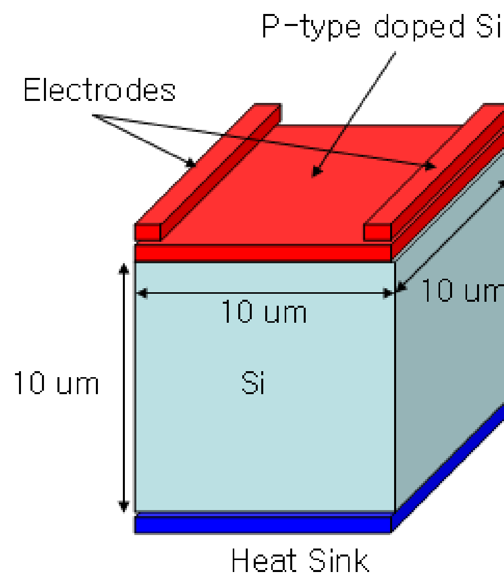


Figure 2.10 A resistor heat source structure. The p-type doped resistor is located on the top and the heat sink is on the bottom. The voltage is applied between two electrodes.

A constant heat source is a heat source that has a constant temperature. The heat source generates a time dependent heat flux to the heat sink. A doped Si (top layer in Figure 2.10) is used for a resistor in the Davinci simulation. The resistance of a doped

Si depends on the doping concentration. If it is highly doped, then there is low heat dissipation and small heat flux. If a voltage is applied across each end of a resistor, current flows through the resistor and heat is generated. This heat is used to compute the thermal impedance of the device. However, more heat is generated in the middle of the resistor so the thermal impedances which are simulated using a constant heat source and a resistor source are different. The thermal impedance caused by a resistor source is always higher than that by a constant heat source. These two structures are shown in Figure 2.9 and Figure 2.10. Each simulation of these structures is done and curve fitted to a one pole model of the thermal impedance (Equation 2.18) using Origin. The results are shown in Figure 2.11, Figure 2.12 and in Table 2.1.

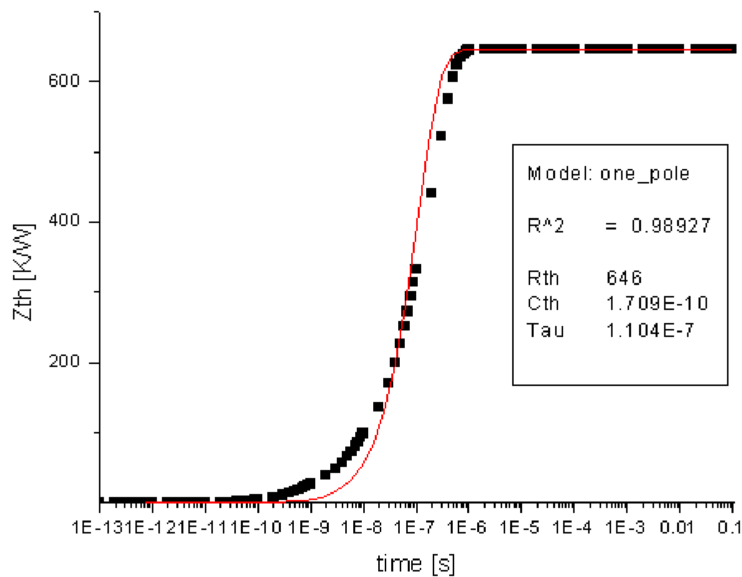


Figure 2.11 Simulation results for structure in Figure 2.9, which is simulated by Davinci and then curve fitted – the dots are the simulated results and the line is curve fitted to one pole model of the thermal impedance (Equation 2.18).

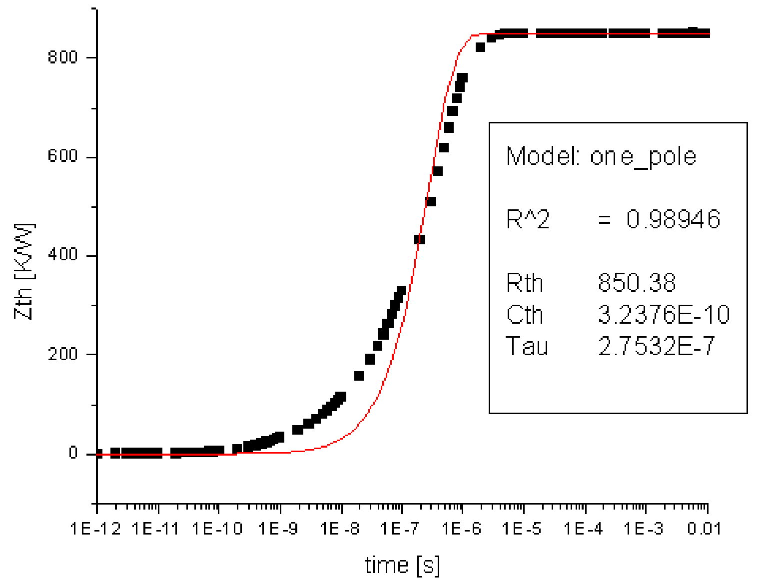


Figure 2.12 Simulation results for structure in Figure 2.10, which is simulated by Davinci and then curve fitted – the dots are the simulated results and the line is curve fitted one pole model of the thermal impedance (Equation 2.18).

Table 2.1 Thermal resistances, thermal capacitances and thermal time constants of two structures in Figure 2.9 and Figure 2.10.

	Constant Heat	Resistor Heat
Rth [K/W]	646	850.4
Cth [W-s/K]	1.709E-10	3.2376E-10
Tau [s]	1.104E-7	2.7532E-7

2.6 Thermal Effects

2.6.1 Self-heating

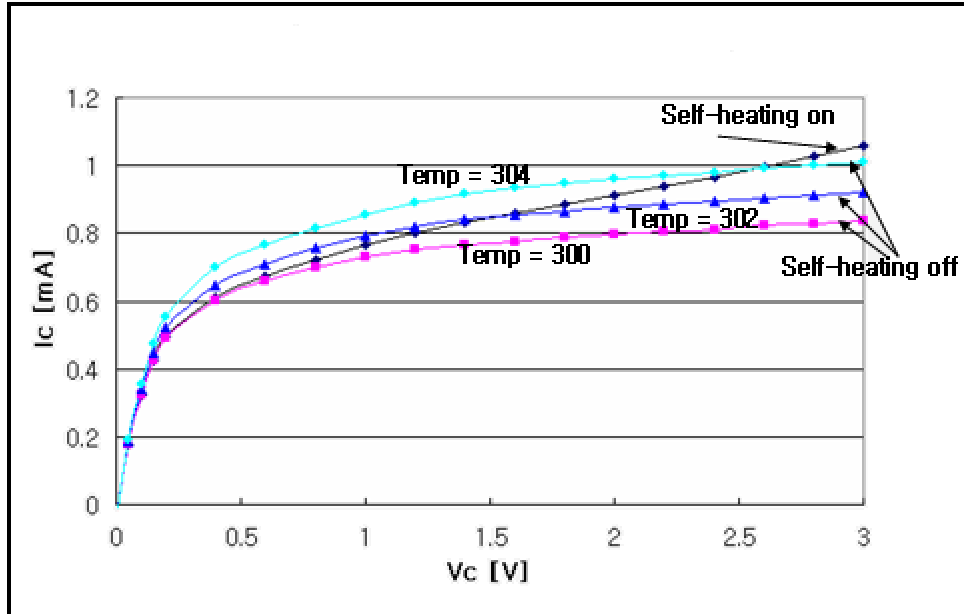


Figure 2.13 The VBIC model output characteristics for a device at V_{BE} = 0.7 [V]. Curves labeled with a T value are I-V characteristic with self-heating off by varied temperature from 300 K to 304 K. The I-V characteristic with self-heating on with a fixed ambient temperature at 300 K is also shown.

Self-heating lays a very important role in the analog circuit design [9]-[11]. The property of self-heating can be extracted by several methods [56]-[58] and be modeled using a numerical method and a physical method [59]-[69]. Self-heating occurs when the BJT is heated up by the power consumed by the same BJT. This causes the characteristics of the BJT to be changed significantly. So, the constant power is provided to the BJT and this increases the temperature of the BJT. This increased temperature affects the characteristics of the BJT such as the number of intrinsic

carriers and the band-gap. These changed characteristics affect the current of the BJT. This increased current effects the temperature of the BJT again. After some time, the BJT is in the steady state condition.

In Figure 2.13, three simulations are done with self-heating off and the I-V characteristics are computed over a temperature range from 300 K to 304 K. Another simulation is done with self-heating on and I-V characteristic is computed at a fixed ambient temperature of 300 K. The later current curve intersects all three current curves. This means the BJT is working at the temperature from 300 K to 304 K. First, the BJT is working near 300 K when the collector voltage is varied from 0 V to 0.5 V and then the BJT is working near 302 K when the collector voltage is varied from 1.3 V to 1.6 V. Finally, the BJT is working over 304 K when the collector voltage is over 2.7 V.

2.6.2 Thermal adjacent coupling

The concept of the thermal adjacent coupling is shown in Figure 2.14 and explained in [70]-[72]. Two BJTs are placed close together. BJT1 consumes a certain power and this will affect its own temperature by the self-heating effect. It also affects the temperature of BJT2 by thermal adjacent coupling. Usually, the thermal effect of the BJT is only modeled by self-heating. However, the space between BJTs today has become very short. So, thermal adjacent coupling has become important.

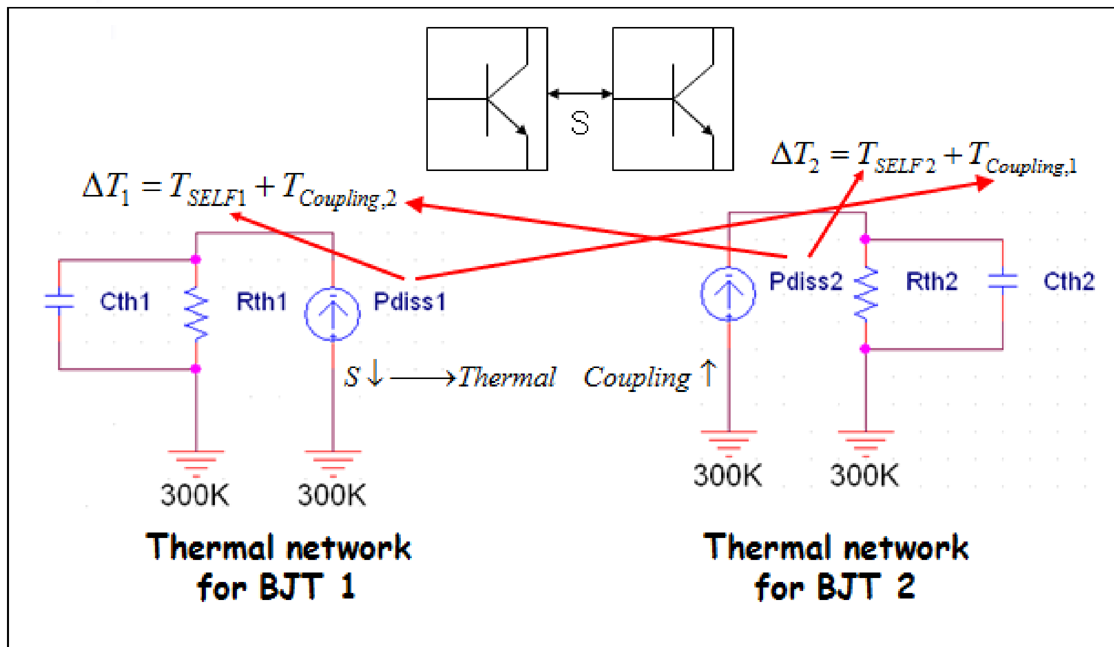


Figure 2.14 Simplified circuit model for the effect of the thermal adjacent coupling.

2.7 Thermal Modeling for BJT

The thermal impedance model is generally based on the assumption that all of the heat is generated uniformly in the rectangular volume of the collector space-charge region (SCR). Adiabatic surfaces for the boundaries except the bottom boundary are also assumed, which mean that heat cannot flow out through the surface.

A comparison between electrical definitions and thermal definitions is summarized in Table 2.2.

Table 2.2 Comparison between electrical terms and thermal analogy terms

	Electrical Term	Electro-Thermal Term
Resistance	R [Ohm]	R_{TH} [K/W]
Capacitance	C [C]	C_{TH} [W-s/K]
Current	I [A]	P_{TH} [W]
Potential difference	V [V]	T [K]

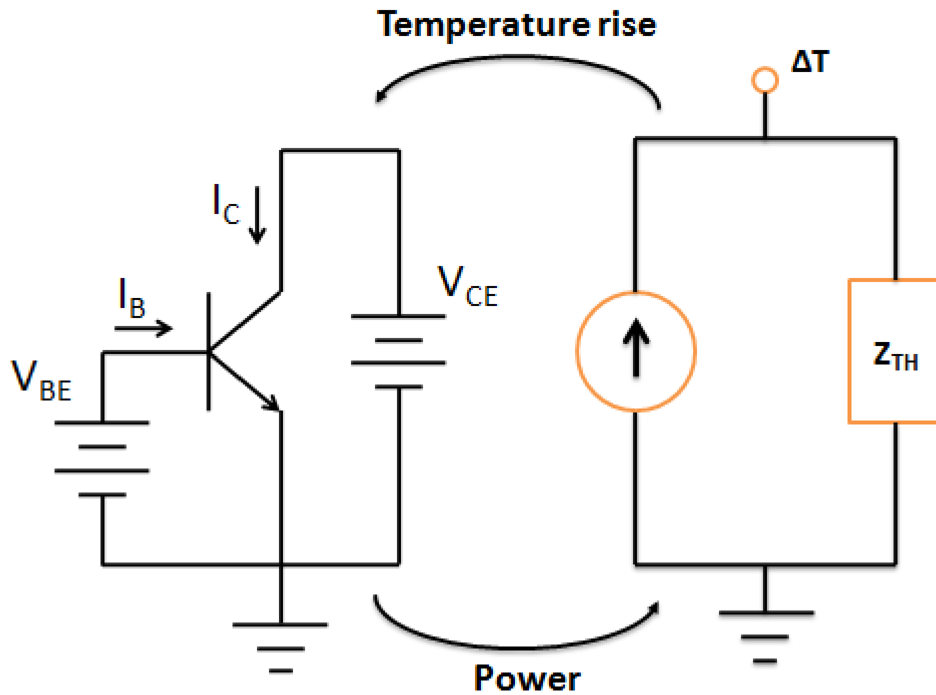


Figure 2.15 Compact model of the thermal network

Thermal modeling of a BJT is conceptually straightforward, although it can be tedious and complex to implement in practice (Figure 2.15). The dissipated power of the thermal network included with the BJT model is :

$$P_{TOTAL} = I_C \cdot V_{CE} + I_B \cdot V_{BE} \tag{2.20}$$

where I_C is the collector current, V_{CE} is the collector-emitter voltage, I_B is the base current, and V_{BE} is the base-emitter voltage. The local temperature rise, ΔT, from the thermal network is coupled back to the BJT.

A series combination of one or more Z_{TH} blocks which consists of one thermal resistance, R_{TH}, and one thermal capacitance, C_{TH}, is normally used as the thermal network. This implies that the response from a step change, $\Delta T(t)$, is the sum of one or more exponential terms with different weights and time constants. The most common thermal network (Figure 2.8) is a single parallel combination of a thermal resistance and a thermal capacitance. However, representation of a thermal resistance and a thermal capacitance as an electrical resistance and an electrical capacitance is not directly applicable, since the temperature is not constant over the substrate.

The low accuracy of the single exponential model was reported in [56]. The best compromise between complexity and accuracy happens when a three-pole model is used. However, the single-pole model is still the only one widely available in circuit simulators such as the SGP model and the VBIC model in SPICE.

2.8 Compact Thermal Model for Dielectrically Isolated BJT

A compact thermal model for a vertical BJT with dielectric isolation (DIBJT) achieved by using silicon-on-insulator (SOI) was proposed by [7]. The isolated Si is referred to as the Si tub (Figure 2.16). The Si tub is represented by a homogeneous medium with finite thickness and with an adiabatic top surface. This means that heat cannot flow through the top surface. The interface between the Si tub and the isolation oxide is assumed to be at a uniform temperature and the heat is assumed to flow through the substrate – thermal boundary (Heat Sink) only. The model represents a single DIBJT device with two parallel heat flow paths that carry heat away from the heat source (Figure 2.17).

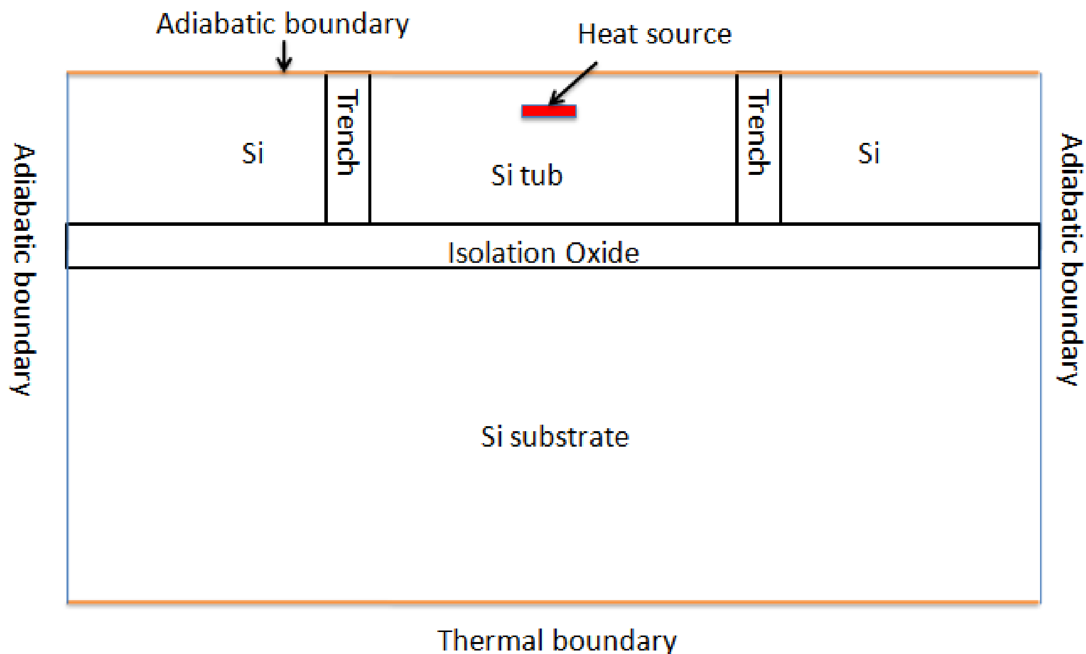


Figure 2.16 Simple DIBJT diagram.

The main assumption for the compact thermal model in [74] is that the entire Si tub is considered to be at nearly constant temperature and that the inner SiO_2 boundary at the trench and isolation region is constant. It is also assumed that the thermal characteristic of the device is primarily determined by the isolation oxide since the thermal conductivity of the silicon is much greater than that of the oxide (Table 1.1).

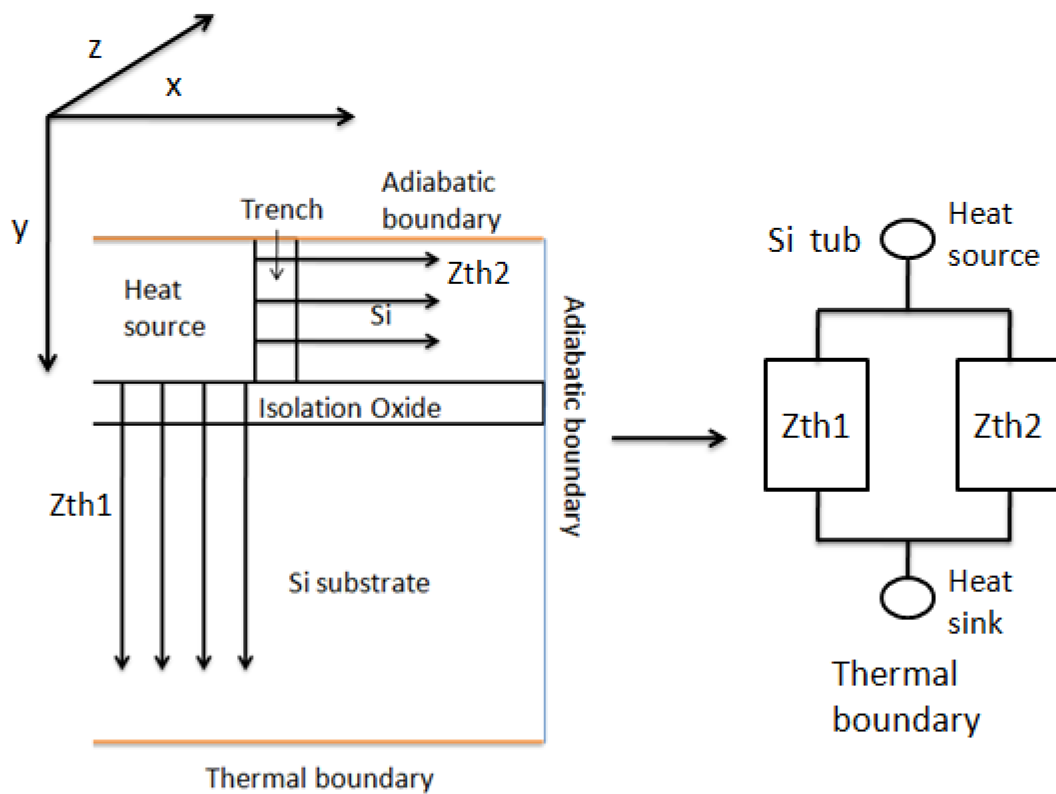


Figure 2.17 Physical diagram to logical thermal diagram.

The heat flux through the isolation oxide and the trench walls can be treated by the one-dimensional circuit in Figure 2.17, and the total thermal impedance is the parallel combination of the Z_{TH1} through the isolation oxide and Si substrate and the

Z_{TH2} through the trench walls and the outer silicon. Since all heat flux is treated as one-dimensional, the outer silicon can be divided into four regions which surround each trench wall. Each region can be modeled by a cooling fin which has an increasing cross-sectional area (Figure 2.18). The parallel combination of each thermal impedance in the four regions is the Z_{TH2}.

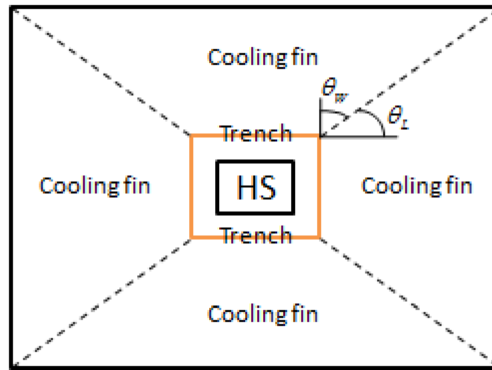


Figure 2.18 Top view of a BJT with a concept of the cooling fin.

The characteristic thermal length in the outer silicon [74] is :

$$\frac{1}{m_{Si}} = \sqrt{\frac{\kappa_{Si} \cdot d_{TUB}}{h_{Ox}}} \tag{2.21}$$

where κ_{Si} is the thermal conductivity of the Si, d_{TUB} is the thickness of the Si tub and h_{Ox} is the isolation oxide heat transfer coefficient defined by :

$$h_{Ox} = \frac{\kappa_{Ox}}{d_{box}} \tag{2.22}$$

where κ_{Ox} is the thermal conductivity of the oxide and d_{box} is the thickness of the isolation oxide. The steady state heat transfer coefficient of the trench [74] is :

$$h_{tr} = \frac{\kappa_{tr}\kappa_{Si} m_{Si} K_1(m_{Si} C_n)}{d_{tr}\kappa_{Si} m_{Si} K_1(m_{Si} C_n) + \kappa_{tr} K_0(m_{Si} C_n)} \tag{2.23}$$

The constant C_n is $\frac{(L_{TUB} + 2d_{tr})}{(2\tan\theta_L)}$ for the x direction and $\frac{(W_{TUB} + 2d_{tr})}{(2\tan\theta_W)}$ for the z direction. θ_L and θ_W are the thermal spreading angles for the cooling fins which are assumed to be 45 degrees (Figure 2.18). K_I is a modified Bessel function of the second kind of order I.

The thermal resistance of the heat path through the isolation oxide [74] is :

$$\rho_{TH1} = \frac{1}{h_{ox} W_{TUB} L_{TUB}} \tag{2.24}$$

The thermal resistance of the heat path through the trench [74] is :

$$\rho_{TH2} = \frac{1}{2h_{tr} d_{TUB} (W_{TUB}\gamma_z + L_{TUB}\gamma_x)} \tag{2.25}$$

where :

$$\gamma_x = \frac{\kappa_{Si} m_{Si} K_1\left[\frac{m_{Si}\left(W_{TUB}+2d_{tr}\right)}{2\tan\theta_L}\right]}{h_{tr} K_0\left[\frac{m_{Si}\left(W_{TUB}+2d_{tr}\right)}{2\tan\theta_L}\right]+\kappa_{Si} m_{Si} K_1\left[\frac{m_{Si}\left(W_{TUB}+2d_{tr}\right)}{2\tan\theta_L}\right]} \tag{2.26}$$

$$\gamma_y = \frac{\kappa_{Si} m_{Si} K_1\left[\frac{m_{Si}\left(W_{TUB}+2d_{tr}\right)}{2\tan\theta_W}\right]}{h_{tr} K_0\left[\frac{m_{Si}\left(W_{TUB}+2d_{tr}\right)}{2\tan\theta_W}\right]+\kappa_{Si} m_{Si} K_1\left[\frac{m_{Si}\left(W_{TUB}+2d_{tr}\right)}{2\tan\theta_W}\right]} \tag{2.27}$$

2.9 Review of Compact Thermal Model for DIBJT

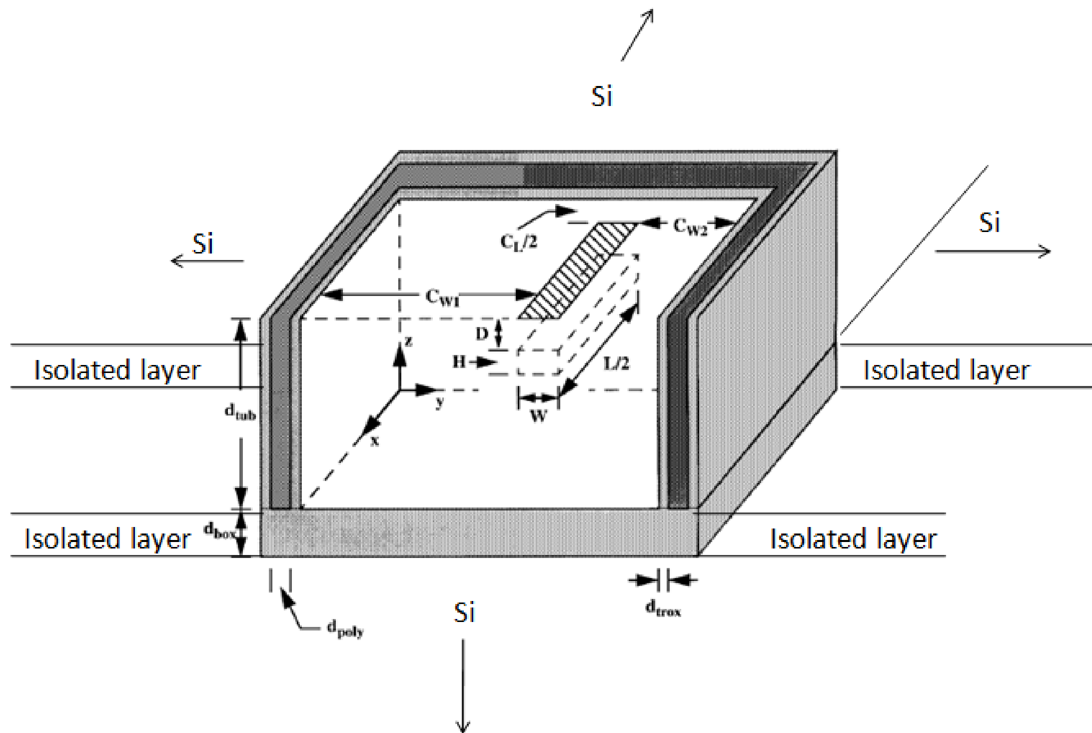


Figure 2.19 Cross section of the simple DIBJT geometry [7].

A review is given here of the previous work of D. T. Zweidinger [7]. The DIBJT structure is based on a silicon-on-insulator (SOI) bipolar junction transistor (BJT) with trenches and an isolation layer defining the isolated region (active device region) which is referred as the silicon tub. The Si tub is represented by a homogeneous medium with finite thickness and with an adiabatic top surface [7]. This means that heat cannot flow through the top surface. The interface between the Si tub and the isolation oxide is assumed to be at a uniform temperature and the heat is assumed to flow through the substrate – thermal boundary (Heat Sink) only.

The simplified DIBJT geometry which is used for the model is shown in Figure 2.19. The heat source represents the base-collector space charge region and is represented by a rectangular volume. The thickness of the heat source can be estimated using the depletion approximation, and the uniform power dissipation is assumed [7].

The increased temperature at any point within the silicon tub can be [7] :

$$\nabla^2 \Delta T_{TUB}(x,y,z,t) + \frac{g(x,y,z,t)}{\kappa_{Si}} = \frac{1}{\alpha_{Si}} \frac{\partial \Delta T_{TUB}(x,y,z,t)}{\partial t} \tag{2.28}$$

where ΔT_{TUB} is the increased temperature, $g(x,y,z,t)$ is the internal energy generation density, κ_{Si} is the thermal conductivity of the silicon, α_{Si} is the thermal diffusivity and t is time. Using following boundary and initial conditions :

$$\left[\frac{\partial \Delta T_{TUB}(x,y,z,t)}{\partial n} - H_{trn}(t) \cdot \Delta T_{TUB}(x,y,z,t) \right]_{n=x,y=0} = 0 \tag{2.29a}$$

$$\left[-\frac{\partial \Delta T_{TUB}(x,y,z,t)}{\partial n}+H_{trn}(t)\cdot \Delta T_{TUB}(x,y,z,t)\right]_{n=x,y=L_{TUB},W_{TUB}}=0 \tag{2.29b}$$

$$\left[-\frac{\partial \Delta T_{TUB}(x,y,z,t)}{\partial z}+H_{bOx}(t)\cdot \Delta T_{TUB}(x,y,z,t)\right]_{z=0}=0 \tag{2.29c}$$

$$\frac{\partial \Delta T_{TUB}(x,y,z,t)}{\partial z}\Big|_{z=0}=0 \tag{2.29e}$$

$$\Delta T_{TUB}(x,y,z,0)=0 \tag{2.29f}$$

where $H_{trn}(t)$ and $H_{bOx}(t)$ are normalized heat-transfer coefficients [7]. The solution of equation (2.28) using the conditions from equation (2.29a) to (2.29f) :

$$\Delta T_{TUB}(x,y,z,t)=\frac{\alpha_{Si}}{\kappa_{Si}}\int_{t'=0}^{t}dt'\int_{V}G(x,y,z,t,x',y',z',t')\cdot g(x,y,z,t)dv' \tag{2.30}$$

Assuming the transient response in power dissipation at time $t'=0$, the increased temperature can be expressed :

$$\begin{aligned} Z_{TH}(x,y,z,t)=\frac{1}{\rho_{si}c_{Psi}V}\int_t &\left[\sum_{m=1}^{\infty}\exp\left[-\alpha_{si}\beta_m^2 t\right]\frac{1}{N(\beta_m)}\cdot X(\beta_m,x)X'(\beta_m)\right] \\ &\cdot\left[\sum_{n=1}^{\infty}\exp\left[-\alpha_{si}\gamma_n^2 t\right]\frac{1}{N(\gamma_n)}\cdot Y(\gamma_n,y)Y'(\gamma_n)\right] \\ &\cdot\left[\sum_{p=1}^{\infty}\exp\left[-\alpha_{si}\eta_n^2 t\right]\frac{1}{N(\eta_n)}\cdot Z(\eta_n,y)Z'(\eta_n)\right]dt \end{aligned} \tag{2.31}$$

where X,Y,Z are the eigenfunctions, β_m,γ_n,η_p the eigenvalues and N is the normalization integrals [7].

Their results show that the calculated thermal impedance using equation (2.31) is well matched with the measured data that is extracted for the Harris devices [7]. However, there is approximately 17% error between the calculated thermal impedance with equation (2.31) and the simulated values determined by the finite difference method used in the program, ANSYS, in the steady-state as shown in Figure 2.20. This error is explained as partially attributed to numerical errors associated with limitations of the finite element mesh in ANSYS [7].

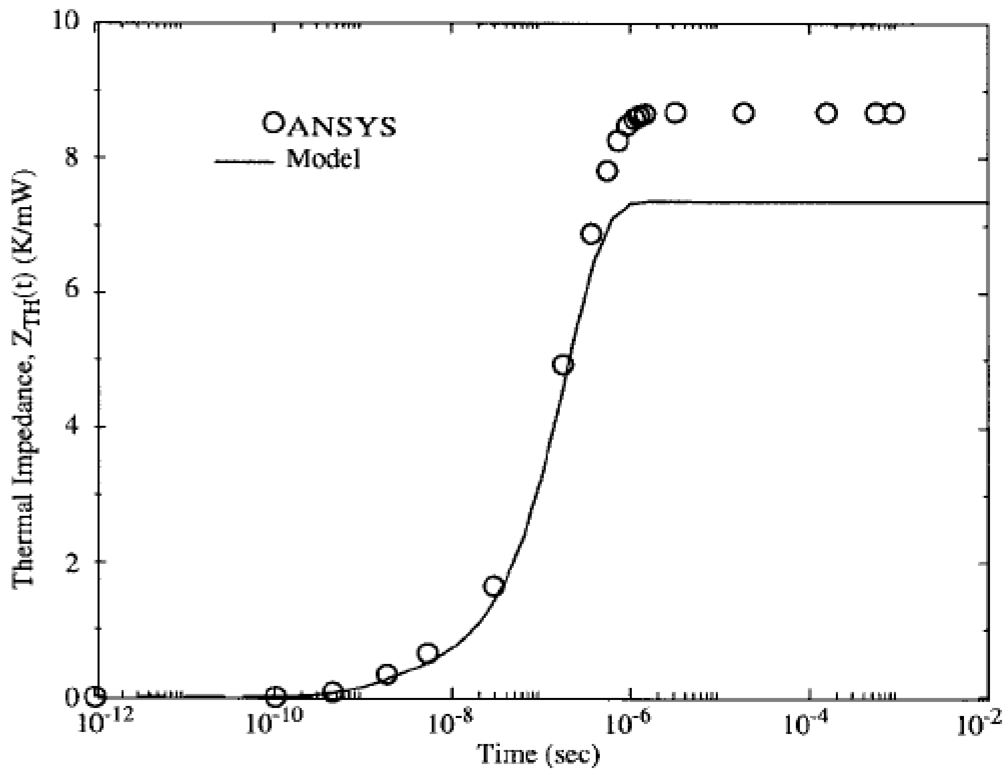


Figure 2.20 Plot of the transient thermal impedance of simulated data (Model) by equation (2.31) and simulated data (ANSYS) using 3-D ANSYS [7]

2.10 Summary

A brief review of bipolar junction transistor models – the Ebers-Moll model, the Gummel-Poon model and the VBIC model is provided. In this paper, the VBIC model is used to characterize the Dielectrically Isolated BJT fabricated by National Semiconductor. Because of the separate thermal network in the VBIC model, the thermal characteristics can be easily modified and calculated.

Silicon on insulator technology has been developed to increase operating speed by reducing parasitic area and to increase soft-error immunity for high packing density of the random access memory. The one is the SIMOX for the thin active device region and the other is wafer bonding for the relatively thick active device region.

General thermal properties for electric materials are explained. Thermal conductivity is defined by the time rate of heat transfer as it conducts between opposite faces of a unit surface of material through a unit length, and the temperature varies by one Kelvin. And this thermal conductivity indicates the efficiency of a material. Materials can absorb heat energy and release it. Thermal capacity is defined as the amount of thermal energy required to raise the temperature of one mole of material by one Kelvin.

The general time dependant differential equation for heat flow with an internal heat source is reviewed. From the general time dependent differential equation for heat flow, the thermal resistance and the thermal capacitance are derived.

The general meaning of thermal impedance is defined by the temperature difference between heat source and heat sink divided by the power consumed by the

heat source in the thermal network and can be calculated using Davinci simulation. After calculation of the thermal impedances, these can be used in the VBIC model to simulate a thermal behavior of bipolar junction transistor.

Two thermal effects are explained in this chapter. Self-heating is the fact that the BJT is heated up by the power consumed by the BJT. Thermal adjacent coupling is the fact that the power consumed in one BJT affects the temperature of the near BJTs. Usually, the thermal effect of the BJT is only modeled by self-heating. However, the space between BJTs today has become very short. So, thermal adjacent coupling has become important.

The general thermal impedance model is explained and the compact thermal model for DIBJT also briefly explained.

CHAPTER 3

THERMAL CHARACTERISTICS IN A SINGLE BJT

3.1 Introduction

One of the most widely adopted thermal models is a one-pole model which consists of one thermal resistance and one thermal capacitance which is used in the VBIC model and SGP model. However, it is reported that this simple one-pole model is not accurate enough. A more accurate model uses the three-pole model [7][56].

The compact model which is represented by the combination of the thermal resistances and the thermal capacitances is explained. The five element compact model which was suggested by Dr. Carter [74][75] is studied and a new method to extract each value of the five element compact model is proposed by using the thermal simulation tool, Davinci. This method uses the maximum temperature in the BJT device to calculate each value of the five element compact model. However, the material is non-isothermal. So, the temperature of each emitter region is different. This difference of the temperatures of each emitter region should be evaluated.

Each value of the five element compact model for the two structures of the BJTs is calculated in both the previous method [74][75] and the proposed simulation method. These values are compared to evaluate the proposed method.

3.2 Review of Five Element Compact Thermal Model for DIBJT

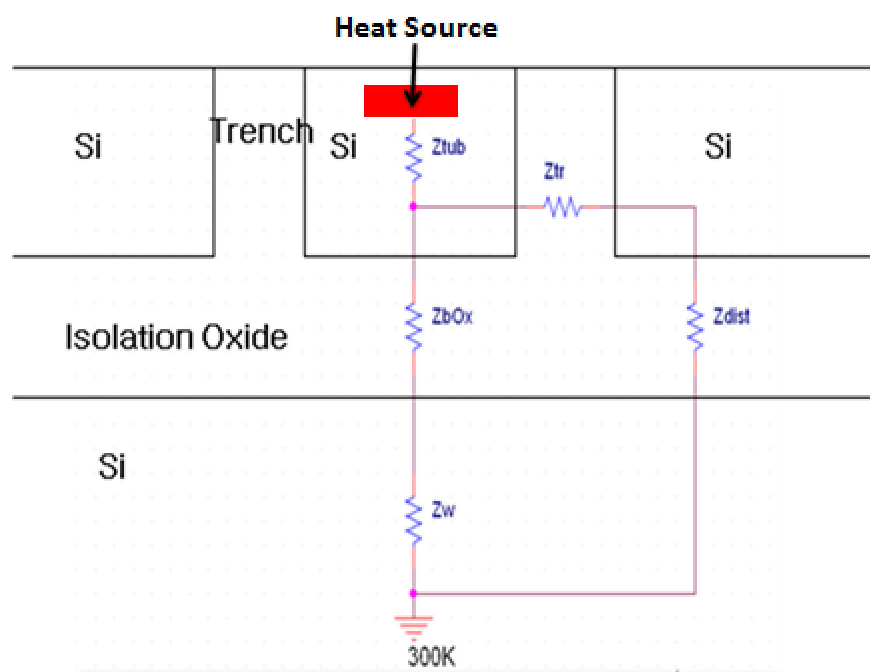


Figure 3.1 Five element compact thermal model for DIBJT [74][75]

The five element compact model (Figure 3.1) is proposed on the basis of the previous work [7][61]. The interface between the Si tub and the isolation and trench oxide is assumed to be at a uniform temperature. The model of the Si tub can be approximated by the spreading resistance below the source and the isolation for the thermal characteristic in the compact model of [7]. However, the interface temperature between the Si tub and the isolation oxide depends on the distance between the heat source and a given point. It is also assumed that the substrate is at an ambient temperature in [7]. However, the thermal characteristic of the Si substrate can be

modeled by using the concept in [61]. The total thermal impedance from the heat source to the heat sink, which is the thermal ground with a constant temperature, is the series and parallel combination of each thermal impedance in the five element compact model (Figure 3.1) and can be written as :

$$Z_{TH} = Z_{TUB} + \left(Z_{bOx} + Z_{W}\right) \| \left(Z_{tr} + Z_{dist}\right) \tag{3.1}$$

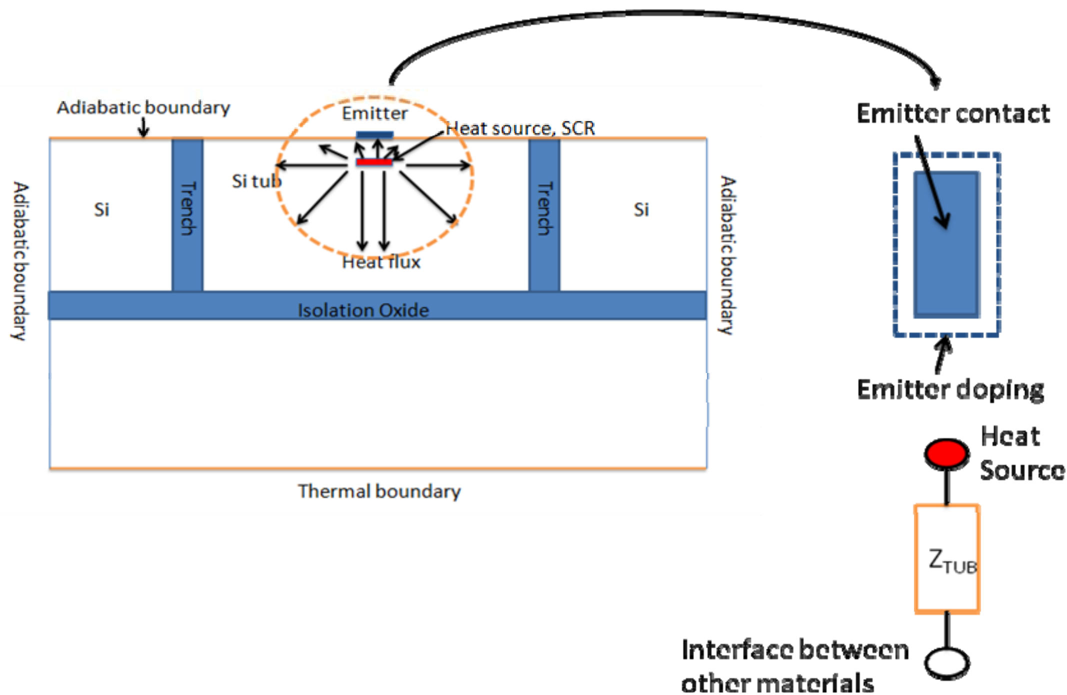


Figure 3.2 Model for the Si tub

To model the thermal impedance in the Si tub, it is assumed that the interface between the Si tub and other materials – the isolation oxide for the bottom and the trench material for the side walls - are isothermal. Also the heat source, which is

represented by the base-collector space charge region (SCR), is a finite rectangular parallelepiped volume in the Si tub. The parameters for the thermal impedance model for the DIBJT are generally fixed by the device geometry. However, the thickness of the base-collector space charge region depends on the electrical bias of the device and can be changed by the operating conditions. There is a difference between the emitter doping geometry and the emitter contact geometry. The emitter contact geometry is used to calculate the values for the five element compact model. The depth of the base-collector junction is used for the distance between the surface of the wafer and the heat source (Figure 3.2).

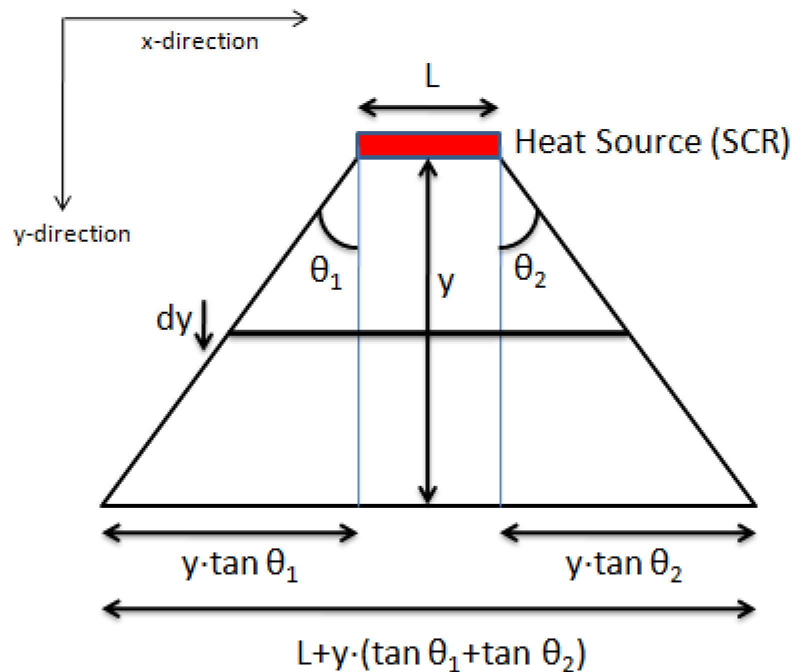


Figure 3.3 Two dimensional truncated pyramid structure in x-y dimension

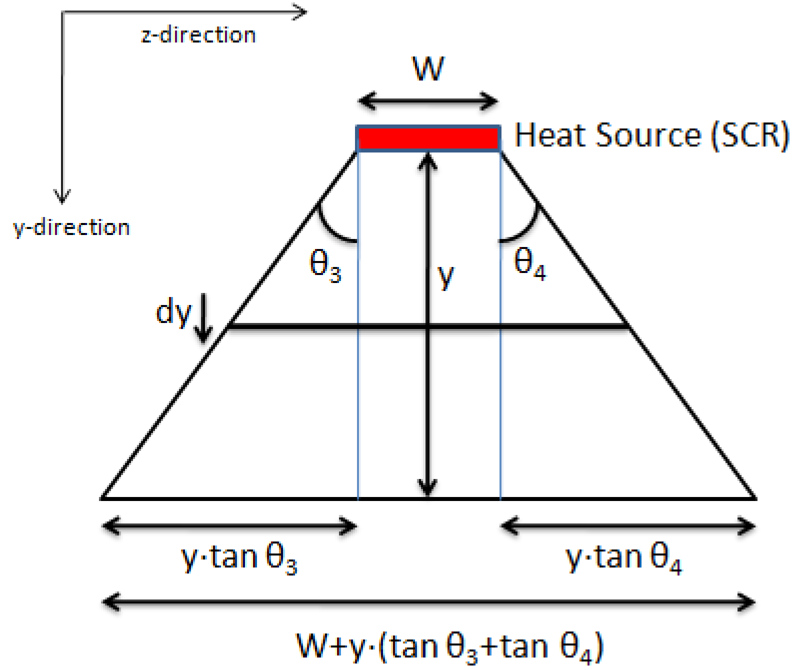


Figure 3.4 Two dimensional truncated pyramid structure in z-y dimension

This Si tub can be represented by a rectangular parallelepiped and splits into five regions of heat flow forming truncated pyramids. Since the wafer surface is assumed to be an adiabatic, the heat flow through the top part can be ignored. A two-dimensional truncated pyramid structure is shown in Figure 3.3 and Figure 3.4.

The rectangular heat source is defined by the length, L and the width, W. The bottom geometry at a distance d from the heat source is defined by $L + y(\tan\theta_1 + \tan\theta_2)$ and $W + y(\tan\theta_3 + \tan\theta_4)$ where θ_0, θ_1, θ_3 and θ_4 are the angle between the heat source and the bottom heat sink. The incremental thermal resistance, ΔR_{TH}, is defined by [74] :

$$\Delta R_{TH} = \frac{\Delta y}{\kappa_{Si}\left(L + y(\tan\theta_1 + \tan\theta_2)\right)\left(W + y(\tan\theta_1 + \tan\theta_2)\right)} \tag{3.2}$$

This can be integrated from 0 to the thickness (y) between the heat source and the bottom interface [74]:

$$R_{TH} = \frac{1}{\kappa_{Si}\left(L \cdot y(\tan\theta_1 + \tan\theta_2) - W \cdot y(\tan\theta_3 + \tan\theta_4)\right)} \times \ln\left(\frac{L\left(W + y(\tan\theta_3 + \tan\theta_4)\right)}{W\left(L + y(\tan\theta_1 + \tan\theta_2)\right)}\right) \tag{3.3}$$

Equation (3.3) can be used to calculate the thermal resistance of the five regions. The total thermal resistance of Si tub is :

$$R_{TH,TUB} = R_{TH,Bottom} \parallel R_{TH,Left} \parallel R_{TH,Right} \parallel R_{TH,Back} \parallel R_{TH,Front} \tag{3.4}$$

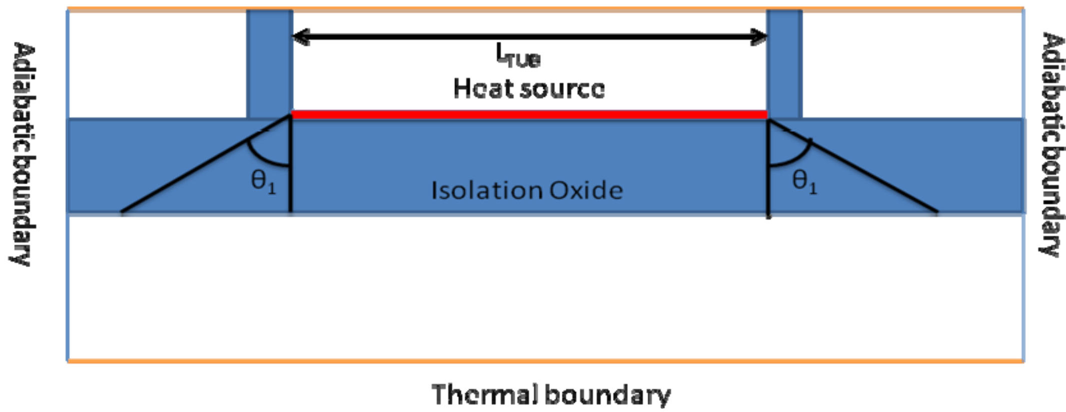


Figure 3.5 Two dimensional truncated pyramid model for the isolation oxide.

The isolation oxide can also be modeled by the truncated pyramid as shown in Figure 3.5. The thermal resistance of the isolation oxide is [74]:

$$R_{TH,bOx} = \frac{1}{\kappa_{Ox}\left(2 \cdot L_{TUB} \cdot d_{bOx} \tan\theta_1 - 2 \cdot W_{TUB} \cdot d_{bOx} \tan\theta_2\right)} \times \ln\left(\frac{L_{TUB}\left(W_{TUB} + 2 \cdot d_{bOx} \tan\theta_2\right)}{W_{TUB}\left(L_{TUB} + 2 \cdot d_{bOx} \tan\theta_1\right)}\right) \tag{3.5}$$

where κ_{Ox} is the thermal conductivity of the oxide, L_{TUB} is the length of the Si tub, W_{TUB} is the width of the Si tub, θ_1 is the angle in x-direction and θ_2 is the angle in z-direction.

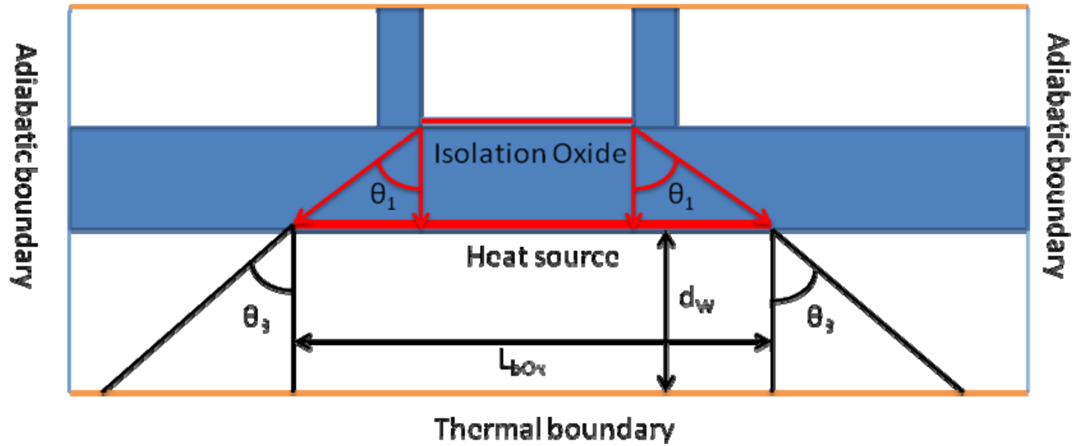


Figure 3.6 Two dimensional truncated pyramid model for the silicon substrate.

For modeling the thermal resistance of the silicon substrate, the concept which is proposed by [61] can be used or the truncated pyramid structure can also be used. The silicon substrate is modeled by the truncated pyramid as shown in Figure 3.6. The thermal resistance of the wafer is [74]:

$$R_{TH,W} = \frac{1}{\kappa_{Si}\left(2 \cdot L_{bOx} \cdot d_W \tan\theta_3 - 2 \cdot W_{bOx} \cdot d_W \tan\theta_4\right)} \times \ln\left(\frac{L_{bOx}\left(W_{bOx} + 2 \cdot d_W \tan\theta_4\right)}{W_{bOx}\left(L_{bOx} + 2 \cdot d_W \tan\theta_3\right)}\right) \tag{3.6}$$

where L_{bOx} is the length of the heat source, W_{bOx} is the width of the heat source, θ_3 is the angle in x-direction and θ_4 is the angle in z-direction.

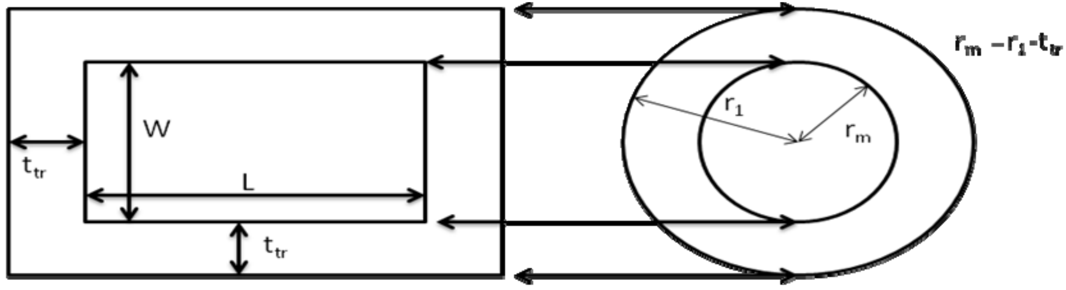


Figure 3.7 Top view of silicon tub and trench.

The thermal resistance of the trench is modeled as a cylindrical region with the circumference given by the perimeter of the tub-trench periphery as shown in Figure 3.7. It is reasonable to assume a cylindrical approximation for a rectangular structure. The thermal resistance of the trench is [75]:

$$R_{TH,tr} = \frac{\ln\left(\frac{r_1}{r_1 - t_{tr}}\right)}{2 \cdot \pi \cdot \kappa_{Ox} \cdot d_t} \tag{3.7}$$

where r_1 is a radius, t_{tr} is a thickness of the trench, κ_{Ox} is the thermal conductivity of the oxide and d_t is the distance from the heat source to the surface of the outer trench.

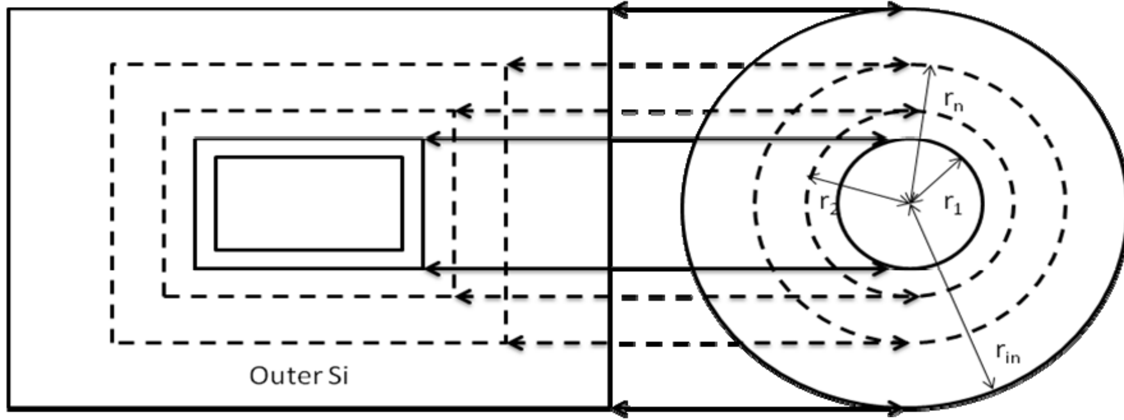


Figure 3.8 Top view of silicon tub, trench and outer silicon.

The model for the thermal distributed resistance is divided into two parts: the first one is the outer silicon ($R_{TH,dist-Si}$) and the second one is the outer isolation oxide ($R_{TH,dist-dOx}$). The silicon region is modeled by using the same concept used for the thermal resistance of the trench as shown in Figure 3.8. The nth $R_{TH,dist-Si}$ is [75]:

$$R_{TH,dist-Si,n} = \frac{\ln\left(\frac{r_{n+1}}{r_n}\right)}{2 \cdot \pi \cdot \kappa_{Si} \cdot d_t} \tag{3.8}$$

where r_{n+1} is a radius of (n+1)[th] circle, r_n is the radius of the nth circle, κ_{Si} is the thermal conductivity of the silicon and d_t is the distance from the heat source to the surface of the thermal boundary.

$R_{TH,dist\text{-}dOx}$ is also assumed to have the cross-sectional area of $\pi \cdot r_1^2$ which is the same cross-sectional area of $R_{TH,dist-Si,n}$ and is [75]:

$$R_{TH,dist-Ox,n} = \frac{t_{bOx}}{\kappa_{Ox} \cdot \pi \cdot r_1^2} \tag{3.9}$$

where t_{bOx} is the thickness of the isolation oxide, κ_{Ox} is the thermal conductivity of the silicon and r_1 is a radius of the first circle.

The thermal distributed resistance is the series and parallel combination of the $R_{TH,dist\text{-}Si}$ and the $R_{TH,dist\text{-}dOx}$ and is defined by

$$\begin{aligned} R_{TH,dist} = & \left(R_{TH,dist-Si,1} + R_{TH,dist-Ox,1}\right) \| \left(R_{TH,dist-Si,2} + R_{TH,dist-Ox,2}\right) \| \cdots \\ & \| \left(R_{TH,dist-Si,\infty} + R_{TH,dist-Ox,\infty}\right) \end{aligned} \tag{3.10}$$

The five element compact model is well studied in [74][75]. However, these researches focused mainly on the value of the thermal resistance. In DC simulations, each value of the thermal resistances cannot be used without the thermal adjacent coupling. When the thermal adjacent coupling is considered, the temperature of the BJT depends upon its own thermal resistance and the thermal adjacent coupling. When the temperature of the BJT is only considered in its own thermal resistance, the total thermal resistance is computed and this value is used to calculate the temperature of the BJT. In AC small signal simulation, the values of the thermal capacitances should be considered. So, the method used to calculate or extract the thermal capacitance is

considered. In the next chapter, a new technique is proposed to extract the thermal resistances and the thermal capacitances using thermal simulations.

3.3 Thermal Characteristic for a Multi-Finger DIBJT

A mathematical method on the thermal resistance for the DIBJT is summarized in the previous chapters. In this chapter, the numerical method is studied by the simulation using Davinci. This program was developed by Synopsys to simulate a device with thermal effects. The half structure of a DIBJT is shown in Figure 3.9. This structure is based on the VIP10 BJT process provided by National Semiconductor. The VIP10 BJT process uses a double poly silicon structure to improve the beta. Also a shallow trench is adopted to block the side current effect between the collector and the base.

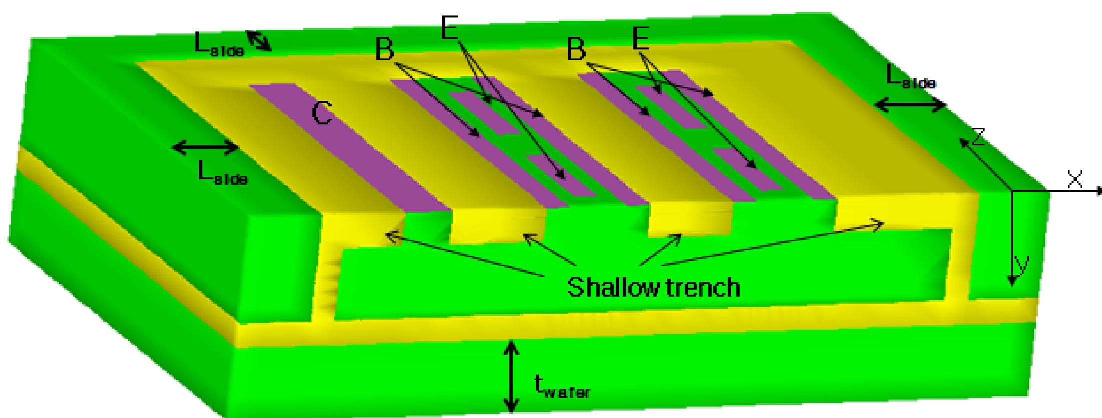


Figure 3.9 Half structure of double poly DIBJT. The bottom is the thermal boundary where the heat flows through. All other sides are the adiabatic boundaries where no heat flows through.

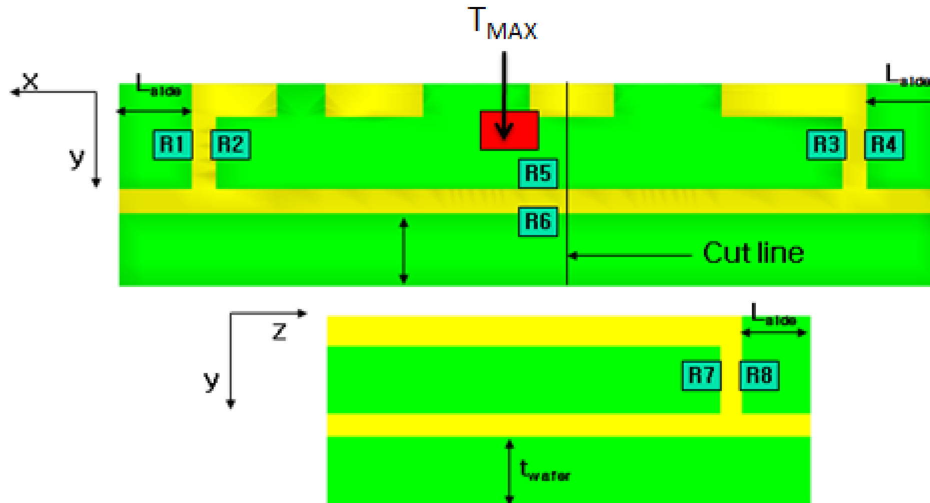


Figure 3.10 Simulation setup – the specific positions for measuring temperature.

The connections on the top of the polysilicons and metals are ignored in order to simplify simulation. This is mainly related in the number of meshes. The distance between the outer trench and the side boundary should be greater than the thickness of the wafer. The temperatures of the specific positions (R1 - R8) are computed to calculate the thermal impedances (Figure 3.10).

The average temperature of the points (R2, R3, R5, R7) are used to calculate the thermal impedance of the silicon tub, and the average temperature of the points (R1, R4, R6, R8) are used to calculate the thermal impedance of the trench and isolation oxide. The difference between the averaged temperature (R1, R4, R6 and R8) and the temperature of the thermal sink on the bottom is used to calculate other thermal impedances. The diagram is shown in Figure 3.11.

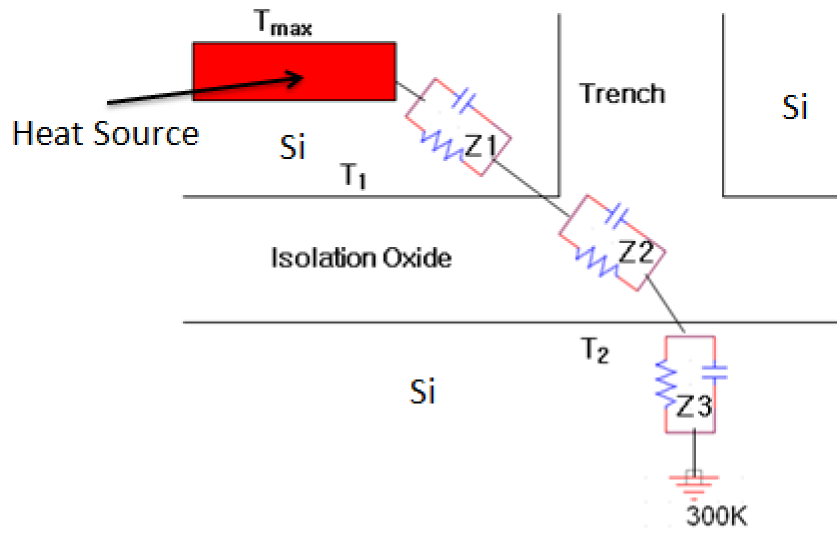


Figure 3.11 Thermal model for the DIBJT (Three-pole model).

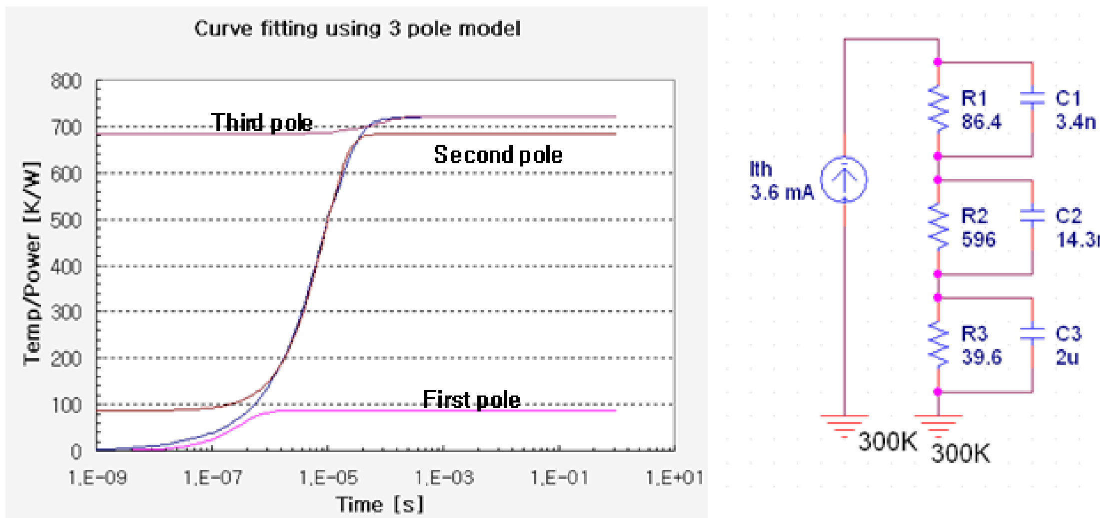


Figure 3.12 Three-pole model and curve fitting results.

To analyze the simulation results, the three-pole model is chosen [7]. The result is shown in Figure 3.12. The total power which is consumed by the DIBJT is

around 3.6 [mW] and the maximum temperature in the DIBJT is around 302.6 [K]. Each thermal impedance is determined by the curve fitting method in the Origin program. This program is developed by Origin Lab and provides a data analysis and graphing workspace for scientists and engineers. The curve fitting equation is:

$$
\begin{aligned}
R_{TH,Total} = R_{TH1}\left(1-\exp\left(\frac{-t}{\tau_{TH1}}\right)\right) + R_{TH2}\left(1-\exp\left(\frac{-t}{\tau_{TH2}}\right)\right) + \\
R_{TH3}\left(1-\exp\left(\frac{-t}{\tau_{TH3}}\right)\right)
\end{aligned}
\tag{3.11}
$$

where R_{TH1} , R_{TH2} and R_{TH3} are thermal resistances and τ_{TH1} , τ_{TH2} and τ_{TH3} are thermal time constants. The thermal time constant is :

$$\tau_{TH} = R_{TH} \cdot C_{TH} \tag{3.12}$$

where R_{TH} is the thermal resistance and C_{TH} is the thermal capacitance.

3.4 Five Element Compact Model for a Multi-Finger DIBJT

As explained in the previous section, the five element model for the DIBJT is related in the physical structure of the DIBJT. The mathematical method used to calculate each thermal resistance is sometimes useful but also has limitations. The mathematical model does not provide an accurate thermal time constant. Consequently, the numerical method is adopted to provide this thermal time constant. The mathematical model assumes the whole silicon tub is the heat source which is used to

calculate the thermal resistance of the isolation oxide and the thermal resistance of the trench. However, this assumption is not true in the simulation using Davinci. The temperature of the center bottom is different from the temperature of the side bottom in the silicon tub. If this difference is considered, the same temperature points in the DIBJT are used for the temperature node for the five element model (Figure 3.13).

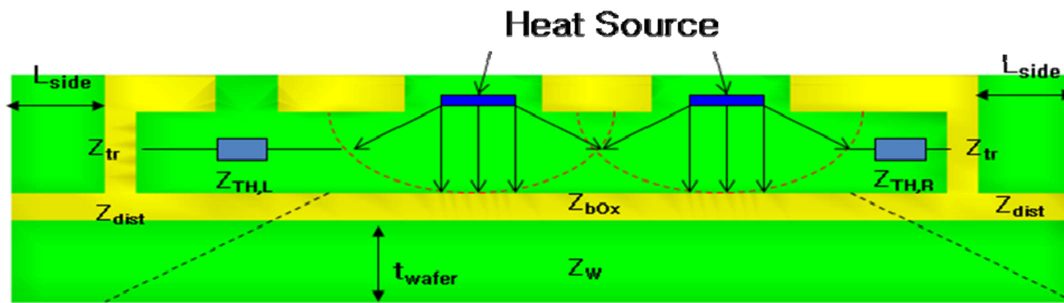


Figure 3.13 Modified five element compact model.

Each thermal impedance of the five element model only approximates the real structure. To calculate these five thermal impedances, some conditions are set and simulations are run using these conditions. The first condition is :

$$Z_{TH} = Z_{TUB} + Z_{bOx}$$

when $Z_{dist} \to \infty$, $Z_{tr} \to \infty$, $Z_W \to 0$. The heat flows through Z_{TUB} and Z_{bOx} only. The second condition is :

$$Z_{TH} = Z_{TUB} + Z_{tr}$$

when $Z_{bOx} \to \infty$, $Z_W \to \infty$, $Z_{dist} \to 0$. The heat flows through Z_{TUB} and Z_{tr} only.

The third condition is :

$$Z_{TH} = Z_{TUB} + Z_{tr} + Z_{dist}$$

when $Z_{bOx} \to \infty$, $Z_W \to \infty$. The heat flows through Z_{TUB}, Z_{tr} and Z_{dist} only.

The simulation results of the three conditions are shown in Figure 3.14, Figure 3.15 and Figure 3.16. The four thermal impedances of the five element model are calculated by the simulation of three conditions. The last unknown thermal impedance is Z_W. It also can be calculated by the curve fitting method using the normal simulation results. The final results are shown in Figure 3.17 and Figure 3.18.

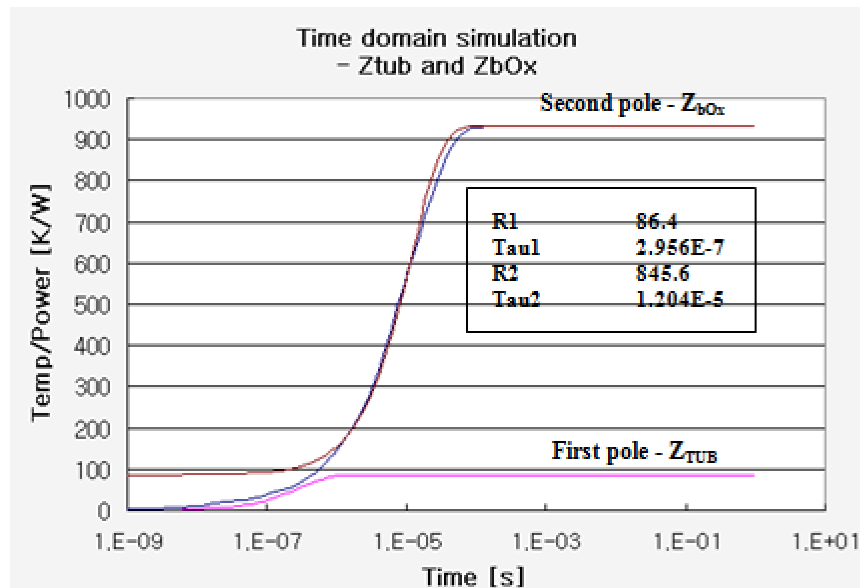


Figure 3.14 Simulation and curve fitting results of first condition. $Z_{TH} = Z_{TUB} + Z_{bOx}$ when $Z_{dist} \to \infty$, $Z_{tr} \to \infty$, $Z_W \to 0$.

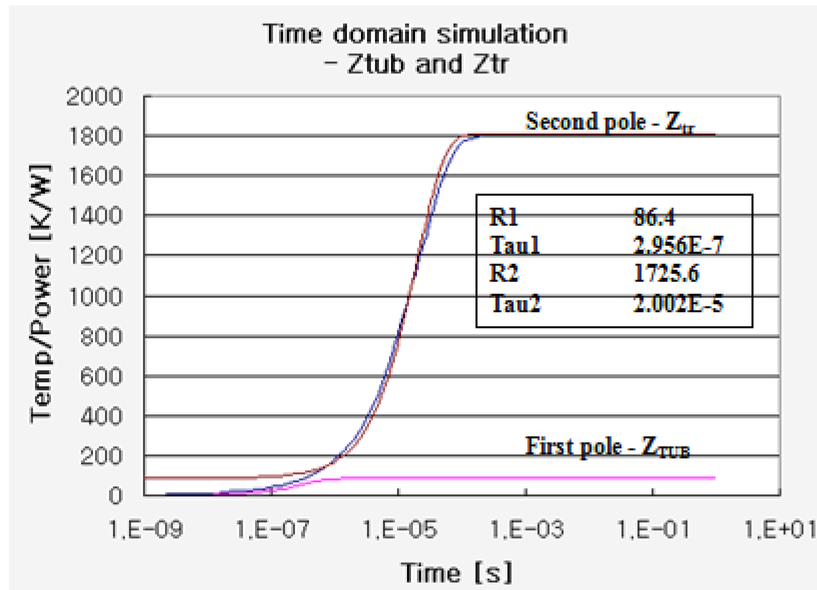


Figure 3.15 Simulation and curve fitting results of second condition. $Z_{TH} = Z_{TUB} + Z_{tr}$ when $Z_{bOx} \to \infty$, $Z_{W} \to \infty$, $Z_{dist} \to 0$.

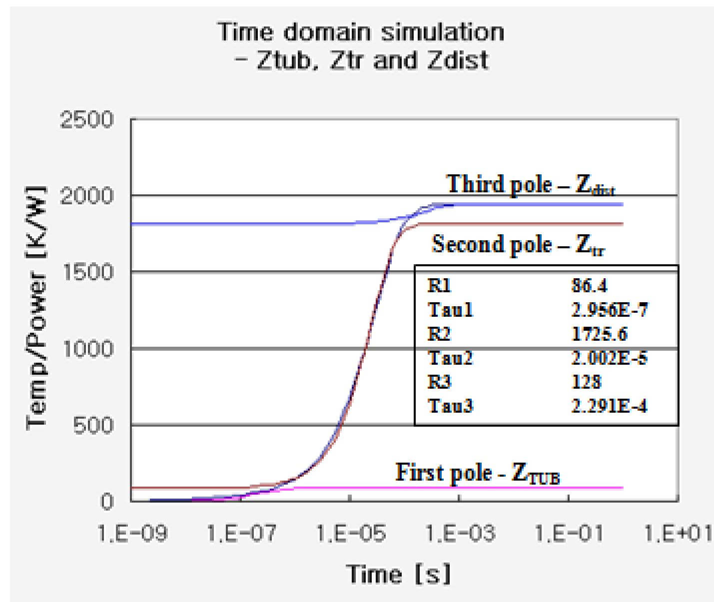


Figure 3.16 Simulation and curve fitting results of third condition. $Z_{TH} = Z_{TUB} + Z_{tr} + Z_{dist}$ when $Z_{bOx} \to \infty$, $Z_{W} \to \infty$.

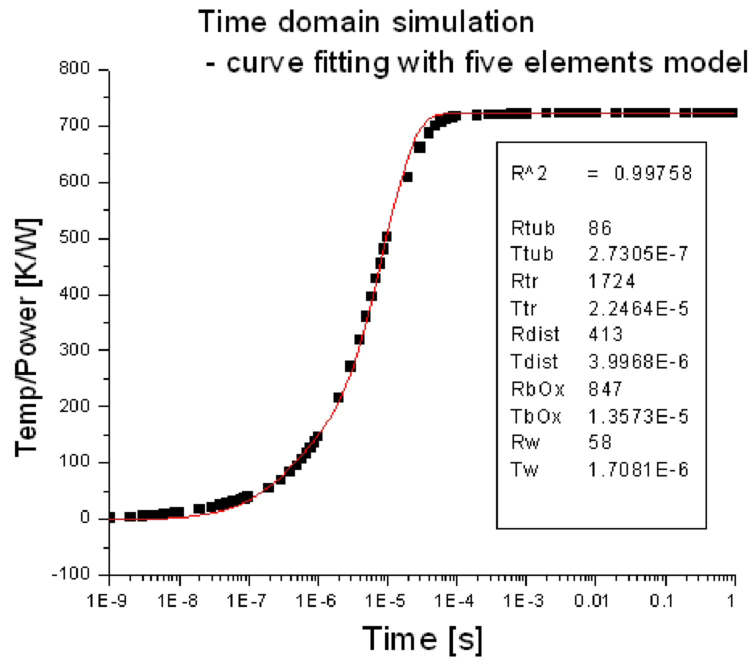


Figure 3.17 Final thermal impedance values for the five element compact model after curve fitting.

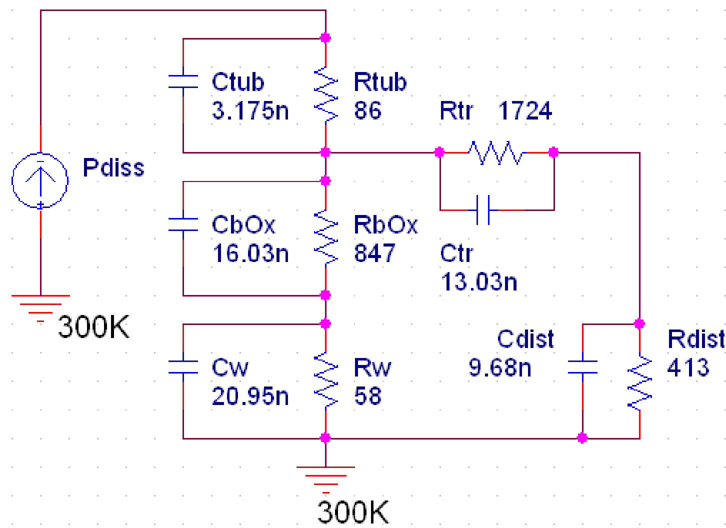


Figure 3.18 Final thermal impedance values for the five element compact model in the thermal circuit. Units are [K/W] for the thermal resistance and [W-sec/K] for the thermal capacitance.

3.5 Thermal Resistance by the Junction Temperature

The device is non-isothermal. So, the temperature of each emitter region is different. The maximum temperature of the device is not the temperature of the space charge region which is assumed as the heat source of the device. So, the difference between these two temperatures should be evaluated.

The junction temperature can be determined by the current-voltage characteristics [76]. If a constant power is consumed by the BJT, the BJT will have the same I-V characteristics with either self-heating on and a constant ambient temperature or self-heating off and a constant device temperature. First, the simulation is run at a fixed device temperature with self-heating off and the I-V curve is obtained. Then, another simulation is run at a fixed ambient temperature with self-heating on, and the I-V curve is obtained. These two I-V curves will intersect at a certain point. At this point, the device consumes the same power. So, the temperature at that point will be a junction temperature at the specific bias. The results are shown in Figure 3.19. The thermal resistance calculated by the maximum temperature method is around 722 [K/W] and that by the junction temperature method is around 688 [K/W]. There is around 4.7% difference between these two schemes. This difference should be considered to calculate the thermal impedance of the DIBJT. The temperature profile at 2.14 [um] from the top surface is shown in Figure 3.20. The maximum temperature of the device will be located at the area that will be affected by the heat which can be generated by the space charge region. This space charge region is assumed by the heat source.

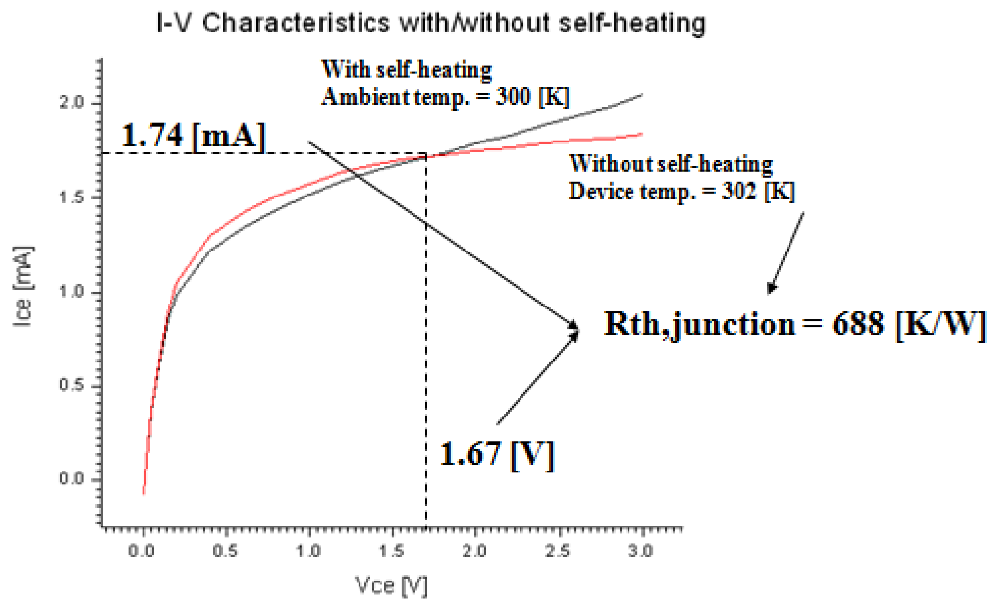


Figure 3.19 I-V characteristics at V_B = 0.74 [V] and V_C = 1 to 3 [V].

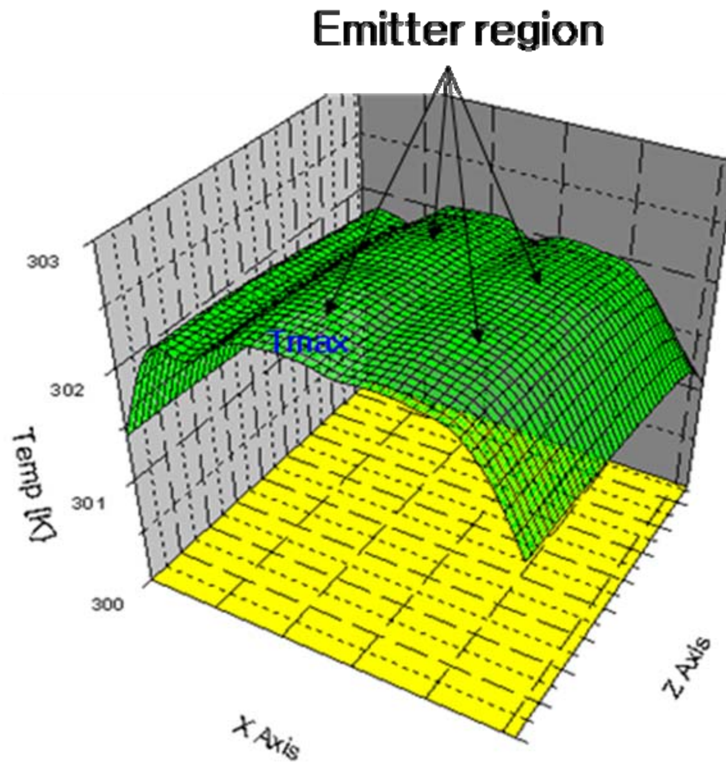


Figure 3.20 Temperature profile at the 2.14 um from the top surface.

3.6 Compare the thermal resistance values in the five element compact model

The values of the thermal resistances in the five element compact model are calculated in three structures; 1X2X1, 1X5X1 and 8X5X1. The notation is (number of emitter)X(emitter length)X(emitter width). And then, the values of the thermal resistances are computed by the simulation method. The tub area is normalized by that of 1X2X1. These values are compared in Table 3.1.

Table 3.1 The thermal resistance values in the five element compact model by the equation of the compact model and the extraction method using thermal simulation.

	1X2X1		1X5X1		8X5X1	
	Compact Model	Simulation (Davinci)	Compact Model	Simulation (Davinci)	Compact Model	Simulation (Davinci)
R_{TUB}	640	640	420	422	86	86
R_{bOx}	3970	3530	3050	3210	743	847
R_W	230	210	210	170	101	58
R_{tr}	2880	3000	2550	2340	1330	1724
R_{dist}	190	350	180	320	136	413

* Units are [K/W] for all values.

The main differences are in the wafer thermal resistance and the distributed thermal resistance. The value of the wafer thermal resistance is over calculated by the compact model calculation than that by the simulation extraction in all three cases. The difference comes from the estimated angles and the dimension of the estimated heat

source (Figure 3.6). The angles are usually assumed at 45 degree. However, it is difficult to calculate the effective angles. The dimension of the heat source is assumed by the bottom area of the isolated layer (Figure 3.6). The area is also depended upon the angles which are used to calculate the thermal resistance of the isolation oxide (Figure 3.5). These angles are also assumed at 45 degree. So, the calculated area of the heat source used to calculate the thermal resistance of the wafer is underestimated. These all errors make the difference in the wafer thermal resistance.

The value of the distributed thermal resistance is under calculated by the compact model calculation compared to the simulation extraction in all three cases. The distributed thermal resistance depends upon the trench area. The area of the trenches is estimated by the ring shape in Figure 3.7. This causes the error and the side thermal resistance in Figure 3.13 ($Z_{TH,L}$ and $Z_{TH,R}$) is ignored in calculation the distributed thermal resistance. These two are the main reason for the difference in the value of the distributed thermal resistance.

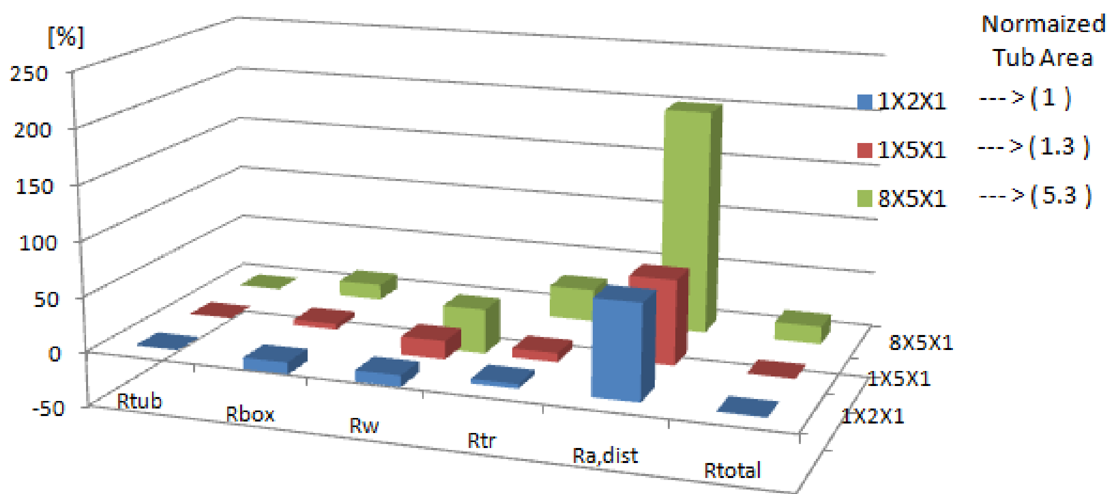


Figure 3.21 The difference between two methods for three devices [%].

The tub area is the key to the mismatch in the values of the thermal resistances. If the tub area is increased, the percentage of the mismatch is also increased (Figure 3.21).

3.7 Conclusion

The five element compact model is developed on the basis of the previous work. As each thermal impedance value of the five element compact model is calculated, the more accurate thermal model for self-heating has been obtained and also the thermal coupling has been implemented by the modified five element compact model which has a modified distributed thermal impedance.

The five element model for the DIBJT is related in the physical structure of the DIBJT. The mathematical method used to calculate each thermal resistance is sometimes useful but also has limitations. The mathematical model does not necessarily provide an accurate thermal time constant. Consequently, the numerical method is adopted to provide this thermal time constant

The device is non-isothermal. So, the temperature of each emitter region is different. The maximum temperature of the device is not the temperature of the space charge region which is assumed as the heat source of the device. So, the difference between these two temperatures should be evaluated. There is around 4.7% difference between the total thermal resistance values by these two methods. This difference should be considered when using the proposed method.

The values of the thermal resistances in the five element compact model are calculated in three structures and then, the values of the thermal resistances are computed by the simulation method. These values are compared to evaluate the proposed method. The main differences are in the wafer thermal resistance and the distributed thermal resistance. The value of the wafer thermal resistance is over calculated by the compact model calculation than that by the simulation extraction in all three cases. The value of the distributed thermal resistance is under calculated by the compact model calculation than that by the simulation extraction in all three cases. The tub area is the key of the mismatch in the values of the thermal resistances. If the tub area is increased, the percentage of the mismatch is also increased.

CHAPTER 4

THERMAL ADJACENT COUPLING BETWEEN BJTS

4.1 Introduction

In recent years, the technology of silicon processing has developed rapidly. The silicon-on-insulator technology is common in the manufacturing of ICs and the dimension of the BJT is shrunk by the improved processing technology. The space between each device is minimized to increase the number of chips in one wafer, and this increases the thermal coupling between devices. However, a little has been done to measure the thermal adjacent coupling between BJTs.

In this chapter, a theoretical model for thermal adjacent coupling is proposed. The model is a modified version of the five element compact model which is explained in the previous chapter. The mathematical expression for this thermal adjacent coupling is proposed. The voltage-controlled voltage-source concept is adopted to model the thermal network coupling between BJTs. The technique used to measure the temperature of an adjacent BJT is explained.

Two structures are designed to measure the thermal adjacent coupling coefficient between BJTs. The first structure has a central BJT surrounded by four BJTs that intercept the heat flow. A second structure has a central BJT surrounded by eight BJTs that intercept the heat flow. Each structure is measured to find the thermal

adjacent coupling coefficient, and the same structure is simulated for comparison. The distance between the trenches for each BJT varies from 2 um to 16 um. The thermal adjacent coupling is found as a function of this distance. Another structure which has eight columns by three rows of BJTs is designed to measure the thermal adjacent coupling coefficients between the central BJT and the left side BJTs.

4.2 Thermal Adjacent Device Model

Advanced process technologies have been provided to fabricate superior BJTs which have low parasitic capacitances, low leakage currents, high packing density, high radiation hardness, and low power consumption. For these purpose, the SOI process technology and the deep trench isolation technology is used to fabricate VIP10 devices. In this isolation technique, a thin isolation oxide separates the substrate wafer from the active device region, and a very narrow and relatively deep trench is etched around the device to be isolated. The trenches are filled with an insulating material. Thus the device is surrounded on five sides by insulating materials. Usually, the thermal conductivity of the insulating material is relatively high (Table 1.1). So, the devices are affected by the thermal heating.

The dielectrically isolated BJT which is used widely in integrated circuits is modeled in previous chapters. The five element compact model was suggested for describing the thermal effects (Figure 3.1). One of these five elements, $Z_{dist,m}$ is related

to the heating effect from the thermal adjacent coupling. The thermal model is shown in Figure 4.1.

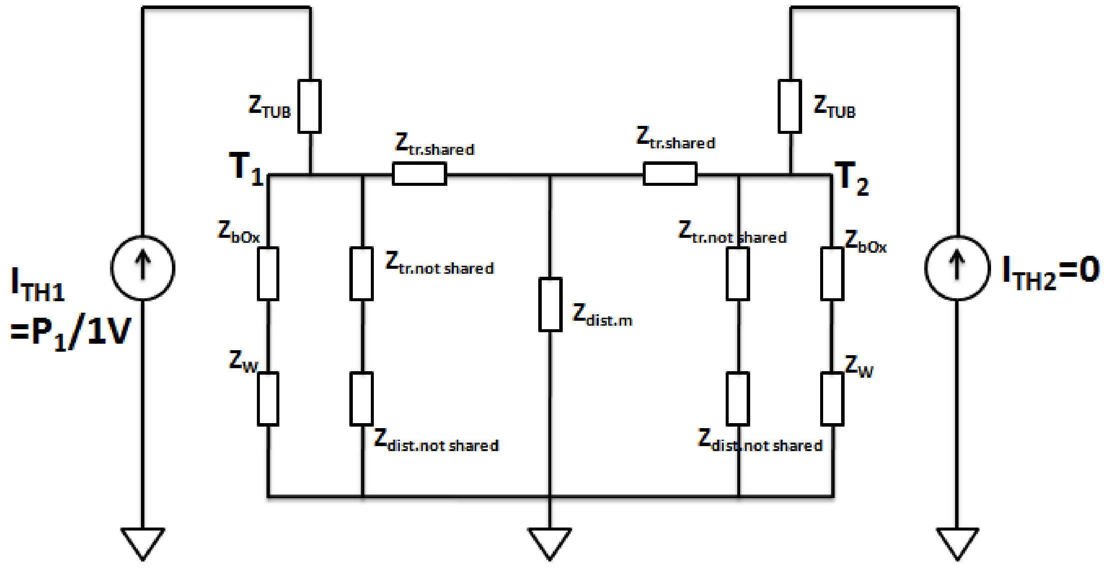


Figure 4.1 Thermal model for the thermal adjacent coupling between two BJTs. BJT1 and BJT2 are connected by the common $Z_{dist,m}$ which is useful for calculating the thermal adjacent coupling coefficient in BJT2 due to the self-heating in BJT1.

Each thermal impedance in Figure 4.1 consists of a thermal resistance and a thermal capacitance. This combination determines the thermal delay and the thermal frequency response. The delay is a function of the physical dimension of each part of the thermal impedance. I_{TH} is the thermal current which is defined by the total power divided by 1 [V]. The thermal adjacent coupling coefficient is $a_{12} = T_2 / T_1$.

The thermal resistance of $Z_{dist.m}$ is modified by the adjacent BJT. The value of this resistance depends on the number of adjacent BJTs, the thickness of the epitaxial layer, the thickness of the isolation oxide, the geometry of the silicon tub, etc.

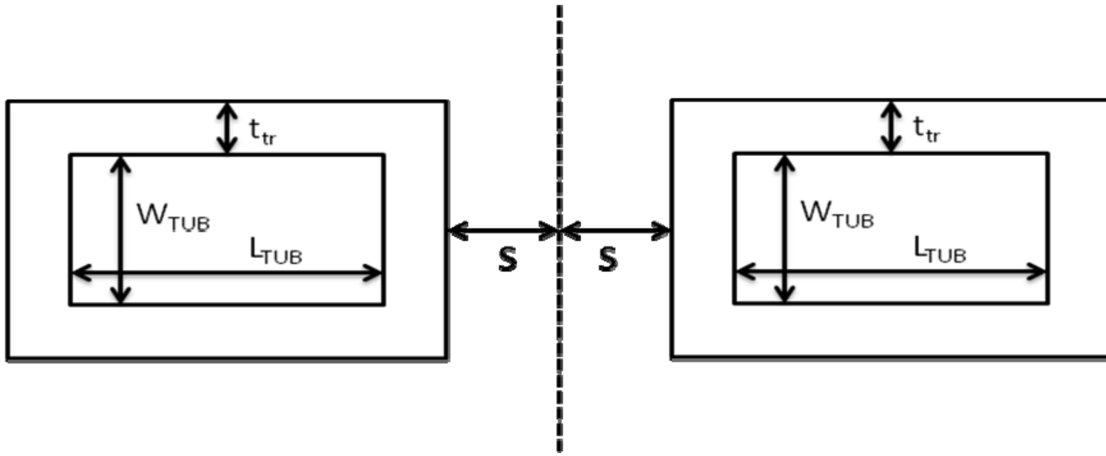


Figure 4.2 Top view of two adjacent BJTs

A top view of two adjacent BJTs with the separation 2S and device area, $A_{device} = (L_{TUB} + 2 \cdot t_{tr})(W_{TUB} + 2 \cdot t_{tr})$, is shown in Figure 4.2. The fraction of the useful area for the heat flow is [70]:

$$f(s) = 1 - r \tag{4.1}$$

where r is the ratio of the BJT area to the total epitaxial area used per BJT. This value is defined by [70]:

$$r = \frac{(L_{TUB} + 2 \cdot t_{tr})(W_{TUB} + 2 \cdot t_{tr})}{(L_{TUB} + 2 \cdot t_{tr} + S)(W_{TUB} + 2 \cdot t_{tr} + S)} \tag{4.2}$$

where L_{TUB} is the length of the silicon tub, W_{TUB} is the width of the silicon tub, and t_{tr} is the thickness of the trench.

The $R_{dist.m}$ can be evaluated as [70] :

$$R_{dist.m} = \frac{1}{2\pi \cdot \kappa_{Si} \cdot t_{epi}(r_o / r_H + 1)} \propto \frac{C}{f(s)} \tag{4.3}$$

where κ_{Si} is the thermal conductivity of the silicon, r_o is the perimeter of the silicon tub, r_H is the healing length, C is a constant and t_{epi} is the thickness of the epitaxial layer. The r_o and r_H are defined by [77] :

$$r_o = \frac{2 \cdot (L_{TUB} + W_{TUB}) + 8 \cdot t_{tr}}{2\pi} \tag{4.4}$$

$$r_H = \sqrt{\frac{\kappa_{Si} \cdot t_{epi} \cdot t_{bOx}}{\kappa_{Ox}}} \tag{4.5}$$

where L_{TUB} is the length of the silicon tub, W_{TUB} is the width of the silicon tub, t_{tr} is the thickness of the trench, κ_{Si} is the thermal conductivity of the silicon, κ_{Ox} is the thermal conductivity of the oxide, t_{epi} is the thickness of the epitaxial layer, and t_{bOx} is the thickness of the isolation oxide.

The simplified circuit model for the effect of the thermal adjacent coupling is shown in Figure 4.3. Each BJT consumes a certain amount of power and this generates the thermal current. Each thermal current flows through the thermal network of each BJT and increases the temperature of each BJT. Also, the thermal current increases the temperature of an adjacent BJT by thermal adjacent coupling. These relations are defined by :

$$\Delta T_1 = Z_{TH1} \cdot I_{TH1} + c_{TH,12} \cdot I_{TH2} \quad (4.6)$$

$$\Delta T_2 = c_{TH,21} \cdot I_{TH1} + Z_{TH2} \cdot I_{TH2} \quad (4.7)$$

where Z_{TH1} is the thermal impedance of BJT1, Z_{TH2} is the thermal impedance of BJT2, $c_{TH,12}$ is the thermal coupling impedance from BJT2 to BJT1, $c_{TH,21}$ is the thermal coupling impedance from BJT1 to BJT2, I_{TH1} is the thermal current of BJT1 and I_{TH2} is the thermal current of BJT2. Thermal current is the power consumed by the device divided by 1 [V].

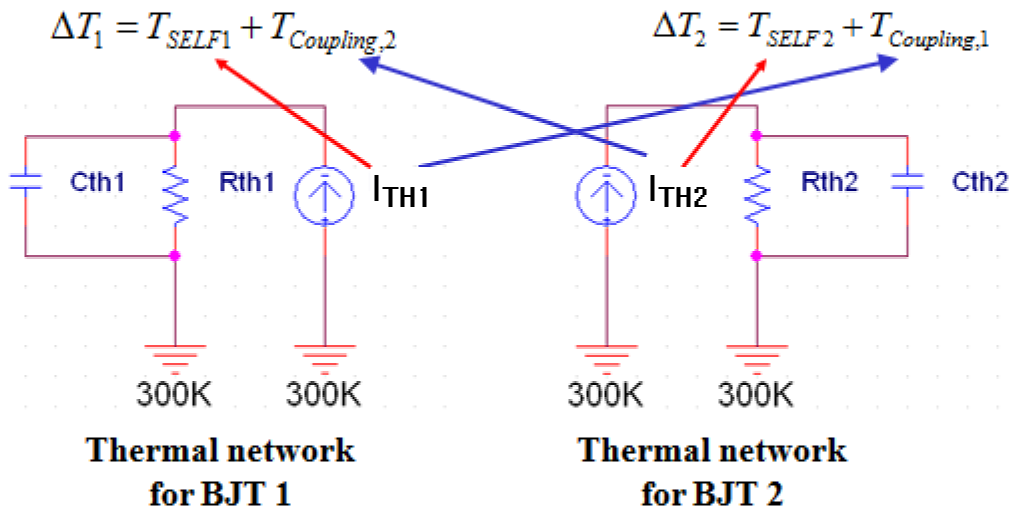


Figure 4.3 Simplified circuit model for the effect of the thermal adjacent coupling.

Another approach to modeling thermal adjacent coupling uses the increased temperature by self-heating. While self-heating is related to the power consumed by the BJT, the thermal adjacent coupling is related to the temperature difference between the

temperature of a BJT and the temperature at another location. So, equation (4.6) and (4.7) can be modified as :

$$\Delta T_1 = Z_{TH1} \cdot I_{TH1} + a_{12} \cdot (Z_{TH2} \cdot I_{TH2}) = T_{rise1} + a_{12} \cdot T_{rise2} \tag{4.8}$$

$$\Delta T_2 = a_{21} \cdot (Z_{TH1} \cdot I_{TH1}) + Z_{TH2} \cdot I_{TH2} = a_{21} \cdot T_{rise1} + T_{rise2} \tag{4.9}$$

where Z_{TH1} is the total thermal impedance of BJT1, Z_{TH2} is the total thermal impedance of BJT2, $a_{12}(= c_{TH,12} / Z_{TH2})$ is the thermal adjacent coupling coefficient from BJT2 to BJT1, $a_{21}(= c_{TH,21} / Z_{TH1})$ is the thermal adjacent coupling coefficient from BJT1 to BJT2, I_{TH1} is the thermal current of BJT1 and I_{TH2} is the thermal current of BJT2.

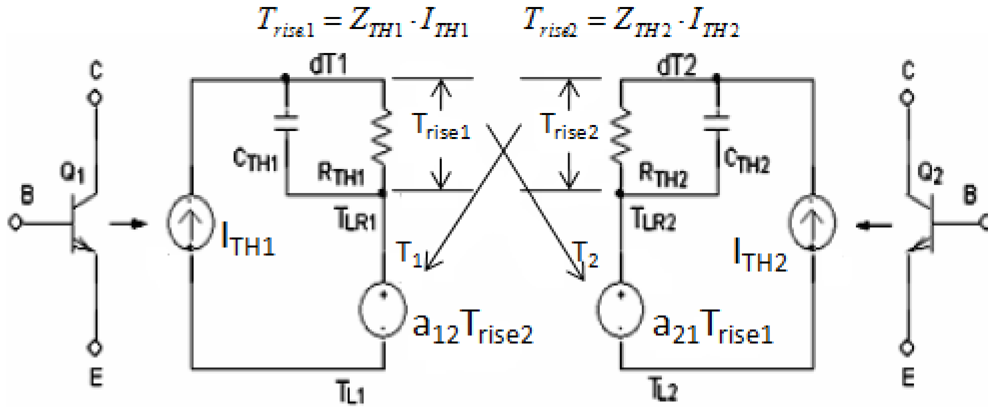


Figure 4.4 VCVS thermal adjacent coupling model [70].

The simplified circuit model (Figure 4.3) can be modified to provide a more explicit relationship between the thermal adjacent coupling coefficients and the changed temperature by power which is consumed by each BJT. The effect of the thermal adjacent coupling is modeled by a voltage-controlled voltage-source (VCVS) in Figure 4.4. A thermal adjacent coupling coefficient (a_{ij}) depends on the number of adjacent devices, the spacing between the devices, nature of the shared wall, device dimensions and operating conditions of the adjacent devices.

4.3 Temperature Measurement

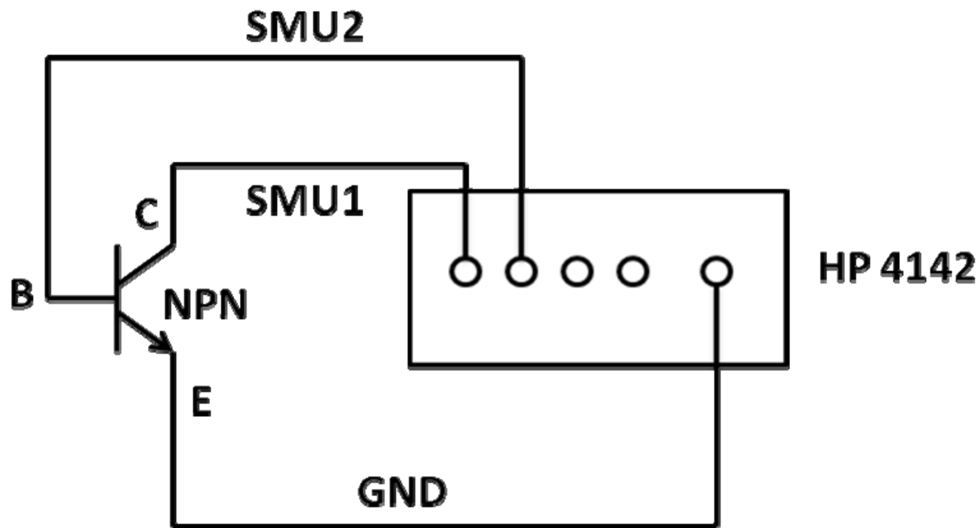


Figure 4.5 Forward Gummel setup for measuring temperature.

The forward Gummel setup is shown in Figure 4.5. A linear voltage sweep is applied between the base and the emitter of the BJT. The base and the collector are

provided with the same voltage by the HP4142 Modular DC Source/Monitor. In this setup, the emitter current is a function of the base-emitter voltage. The following equations describe the relationship between the temperature and the emitter current:

$$I_E = I_B + I_C = (1 + 1/\beta) \cdot I_S \cdot \exp\left(\frac{V_{BE}}{\eta kT/q}\right) \tag{4.10}$$

$$\ln(I_E) = \ln[(1 + 1/\beta) \cdot I_S] + \frac{V_{BE}}{\eta kT/q} \tag{4.11}$$

$$\frac{d(\ln(I_E))}{d(V_{BE})} = \frac{1}{\eta kT/q} \tag{4.12}$$

$$T = \frac{q}{\eta k} \cdot \frac{d(V_{BE})}{d(\ln(I_E))} \tag{4.13}$$

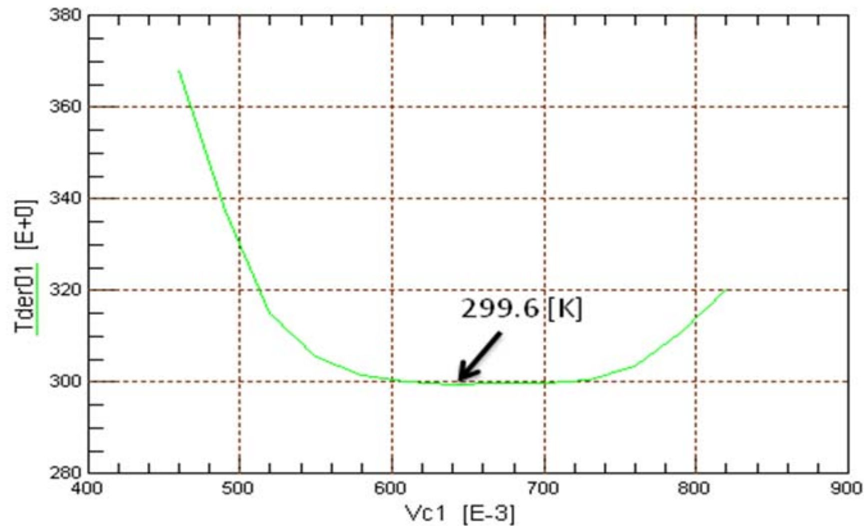


Figure 4.6 One sample of measurements.

A transform function in ICCAP is written using equation (4.13). One sampled pseudo-temperature plot is shown in Figure 4.6. Equation 4.10 ignores the effect of a shunt current due to the measurement apparatus and the effect of high-level-injection. Consequently, the minimum temperature of the Tder01 vs. V_{CE} plot is the silicon tub temperature of the BJT [73].

4.4 Measurement of Thermal Adjacent Coupling

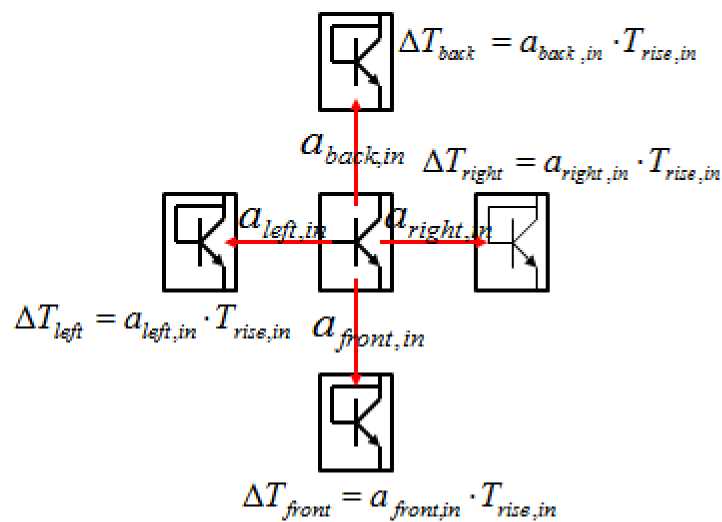


Figure 4.7 Diagram of the test structure 1. The distance between the central BJT and the outer BJTs is 2 um.

In Figure 4.7, the central BJT is separated by 2 um from the outer four BJTs. The outer four BJTs share the collector and emitter connections together. The central BJT is made to consume a range of power levels and thus generates different heat. The

averaged temperature of the outer four BJTs is measured using the forward Gummel method which is explained in the previous chapter. The temperature caused by self-heating is relatively small so it can be neglected. The mathematical relationship between the central BJT and the outer four BJTs is :

$$T_{Measured} = Average(\Delta T_{left}, \Delta T_{right}, \Delta T_{back}, \Delta T_{front}) + T_{Ambient} \tag{4.14}$$

where ΔT_{left}, ΔT_{right}, ΔT_{back} and ΔT_{front} are the increased temperatures caused by the consumed power in the central BJT, and $T_{Ambient}$ is the room temperature. Equation (4.14) can be written using the thermal adjacent coupling coefficient :

$$T_{Measured} = Average(a_{left,in}, a_{right,in}, a_{back,in}, a_{front,in}) \cdot T_{rise,in} + T_{Ambient} \tag{4.15}$$

where $a_{left,in}$, $a_{right,in}$, $a_{back,in}$ and $a_{front,in}$ are the thermal adjacent coupling coefficients for each outer BJT and $T_{rise,in}$ is the increased temperature of the central BJT. This temperature can be calculated by :

$$T_{rise,in} = Z_{TH,in} \cdot \Delta P_{in} = Z_{TH,in} \cdot (V_{BE,in} \cdot I_{B,in} + V_{CE,in} \cdot I_{C,in}) \tag{4.16}$$

The averaged thermal adjacent coupling coefficient is defined from equation (4.15) and it is :

$$a_{Average,in} = \frac{\Delta T_{Measured}}{\Delta T_{rise,in}} = \frac{\Delta T_{Measured}}{\Delta P_{in}} \cdot \frac{1}{Z_{TH,in}} \tag{4.17}$$

The one sampled measurement result for the test structure is shown in Figure 4.8. The slope of the trend line indicates the average thermal coupling resistance due to the adjacent device heating effect.

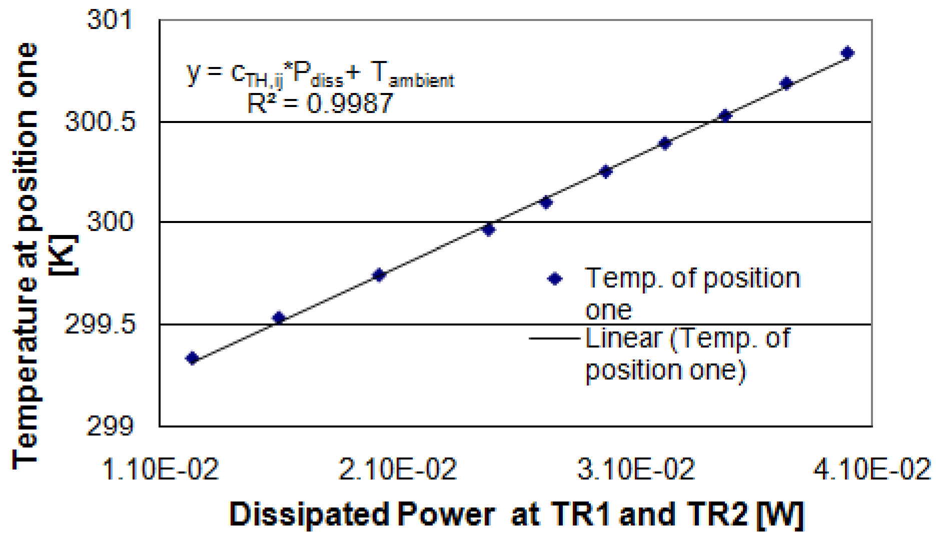


Figure 4.8 An example of the temperature measured for the test structure 1 in various powers consumed by the central BJT.

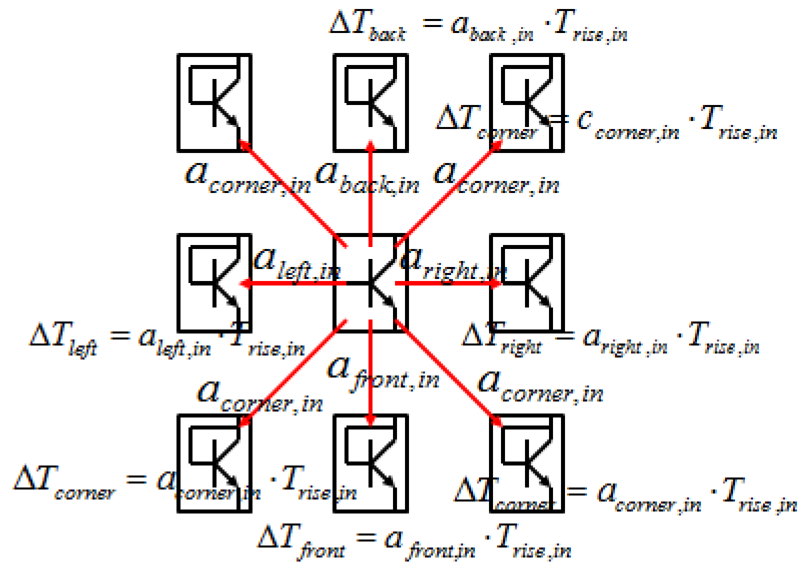


Figure 4.9 Diagram of the test structure 2. The distance between the central BJT and the outer BJTs is 2 um.

Another test structure is shown in Figure 4.9. The outer eight BJTs share the collector and emitter connections together. The same method can be used to calculate the average thermal adjacent thermal coefficient. The averaged temperature at the outer eight BJTs is :

$$\begin{aligned} T_{Measured} &= Average\left(\Delta T_{left}, \Delta T_{right}, \Delta T_{back}, \Delta T_{front}, 4 \cdot \Delta T_{corner}\right) \\ &+ T_{Ambient} \end{aligned} \tag{4.18}$$

where ΔT_{left}, ΔT_{right}, ΔT_{back}, ΔT_{front} and ΔT_{corner} are the increased temperature at the outer BJTs by the consumed power in the central BJT. $T_{Ambient}$ is the room temperature. Equation (4.18) can be written using the thermal adjacent coupling coefficient :

$$\begin{aligned} T_{Measured} &= Average\left(a_{left,in}, a_{right,in}, a_{back,in}, a_{front,in}, 4 \cdot a_{corner,in}\right) \cdot T_{rise,in} \\ &+ T_{Ambient} \end{aligned} \tag{4.19}$$

where $a_{left,in}$, $a_{right,in}$, $a_{back,in}$, $a_{front,in}$ and $a_{corner,in}$ are the thermal adjacent coupling coefficients for each outer BJT and $T_{rise,in}$ is the increased temperature of the central BJT. This temperature can be calculated by :

$$T_{rise,in} = Z_{TH,in} \cdot \Delta P_{in} = Z_{TH,in} \cdot \left(V_{BE,in} \cdot I_{B,in} + V_{CE,in} \cdot I_{C,in}\right) \tag{4.20}$$

The averaged thermal adjacent coupling coefficient is defined from equation (4.19) and it is :

$$a_{Average,in} = \frac{\Delta T_{Measured}}{\Delta T_{rise,in}} = \frac{\Delta T_{Measured}}{\Delta P_{in}} \cdot \frac{1}{Z_{TH,in}} \quad (4.21)$$

The one sampled measurement result for the test structure is shown in Figure 4.10. The slope of the trend line indicates the averaged thermal coupling resistance due to the adjacent device heating effect.

The measurements for test structure 1 and test structure 2 are done using the HP4142 Modular DC Source/Monitor, which is interfaced with the software program, ICCAP. The averaged results are in Table 4.1.

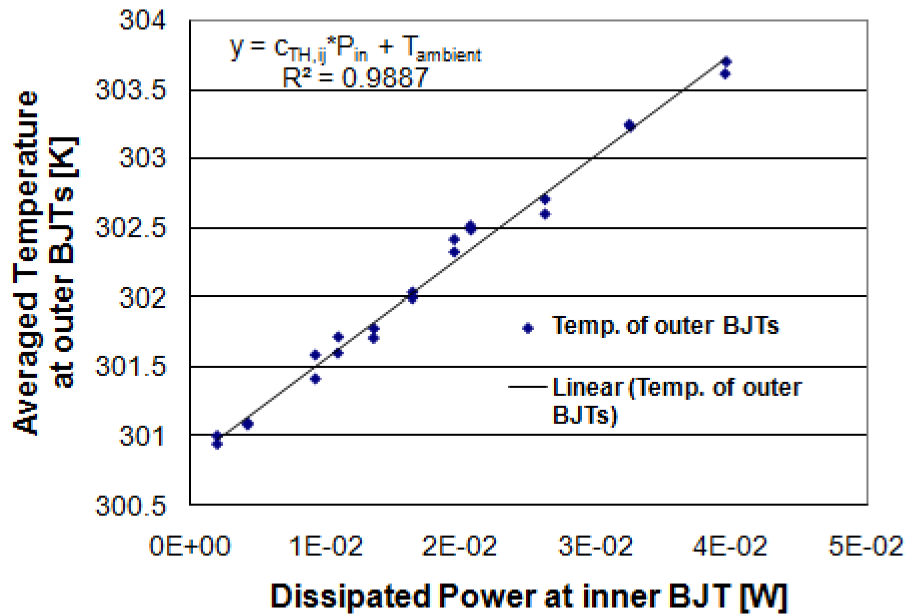


Figure 4.10 An example of the temperature measured for the test structure 2 in various powers consumed by the central BJT.

Table 4.1 Averaged thermal adjacent coupling coefficients of the structure 1 and the structure 2.

	Structure 1	Structure 2
Averaged thermal coupling coefficient [%]	8.0	8.2
Standard deviation [%]	0.44	0.44

Table 4.2 Averaged thermal coupling coefficients of the structure 1 and the structure 2 in the measurements and the simulations.

	Structure 1	Structure 2
Measurements [%]	8.0	8.2
Simulation [%] (DAVINCI)	8.3	11

There is not a big difference between the thermal adjacent coupling coefficients of the test structure 1 and test structure 2. However, there is a difference between the thermal adjacent coupling coefficients of the test structure 1 and test structure 2 in the simulation using DAVINCI (Table 4.2). This mismatch between the measurements and the simulations may be caused by connection between the outer BJTs. The outer BJTs in both test structures share the collector and emitter connections together. In test structure 1, the measured temperature is averaged temperature of the outer four BJTs. However, the measured temperature in test structure 2 is the averaged temperature of the outer eight BJTs. It is reasonable to assume that the temperature of the four corner BJTs is less than the temperature of the center four BJTs which have more shared silicon between the trench walls.

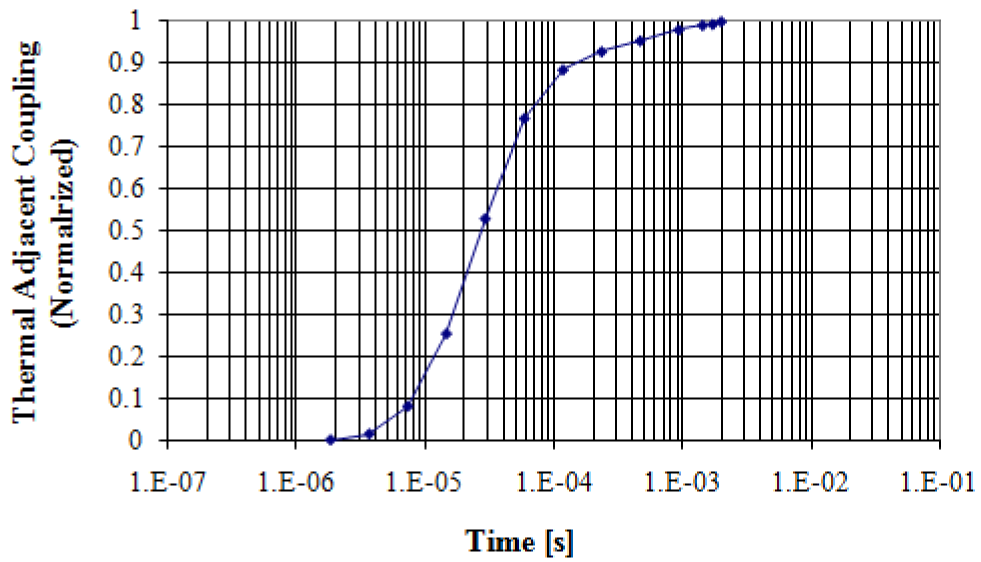


Figure 4.11 The thermal step response of the thermal adjacent coupling impedance for the test structure 1. The results are normalized.

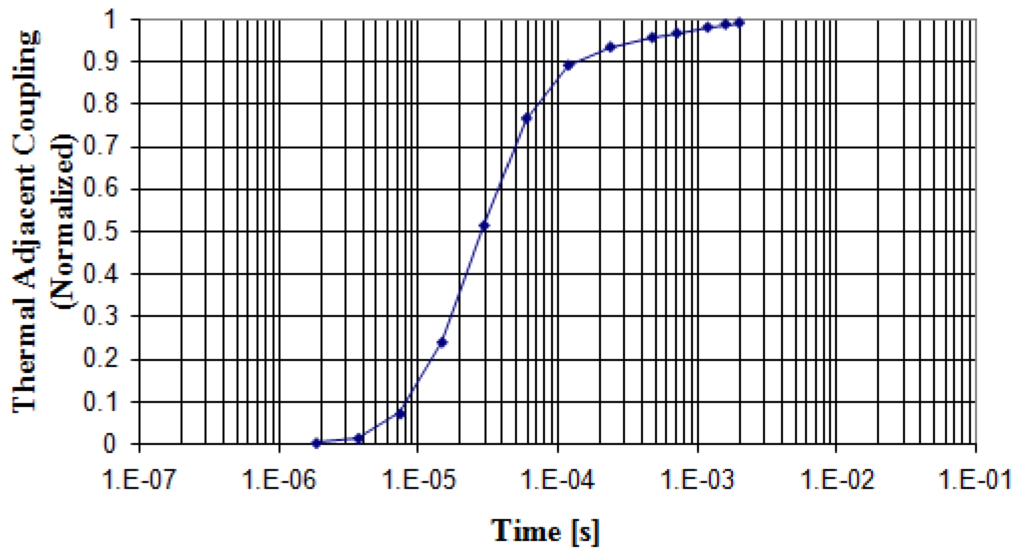


Figure 4.12 The thermal step response of the thermal adjacent coupling impedance for the test structure 2. The results are normalized.

The thermal step response of the thermal adjacent coupling impedances in test structure 1 and test structure 2 are computed in Figure 4.11 and Figure 4.12. The thermal time constant of the thermal adjacent coupling impedance for the test structure 1 is around 45.1 us, which is calculated by the curve fitting method in Origin. The thermal time constant of the thermal adjacent coupling impedance for the test structure 2 is around 45.6 us, which is calculated by the curve fitting method in Origin.

Several simulations are done to find the relation between the thermal adjacent coupling coefficient and the space from the trench wall to the trench wall. The space is varied from 2 um to 16 um and the thermal adjacent coupling coefficient is calculated by :

$$a_{average,in} = \frac{T_{Measured,averaged} - T_{Ambient}}{T_{rise,in}} \tag{4.22}$$

where $T_{Measured,averaged}$ is the average temperature which is computed in left, right, and back, front BJTs, $T_{Ambient}$ is the ambient temperature (300K), $T_{rise,in}$ is the increased temperature at the center BJT.

The simulation results of the various distances are shown in Figure 4.13 for the test structure 1 and Figure 4.14 for the test structure 2. There is an explicit relation between the thermal adjacent coupling coefficient and the distance. :

$$a_{out,in} = C_{out,in} \cdot \ln\left(S_{out,in}\right) + C_1 \tag{4.23}$$

where $C_{out,in}$ is a slope constant, $S_{out,in}$ is the distance between the central BJT and the outer BJTs in test structure 1 and test structure 2, and C_1 is a compensation constant.

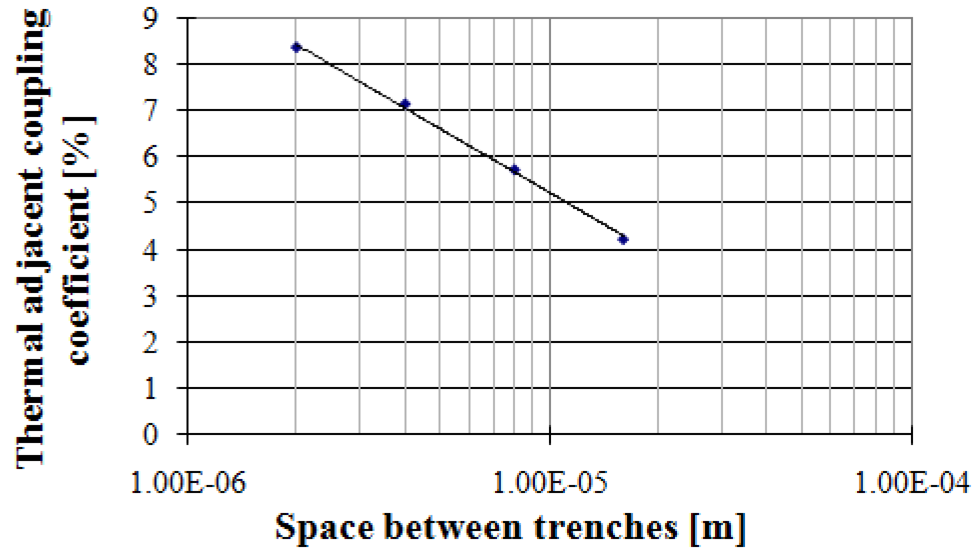


Figure 4.13 Thermal adjacent coupling coefficient of the test structure 1. The space between trenches is varied from 2 um to 16 um.

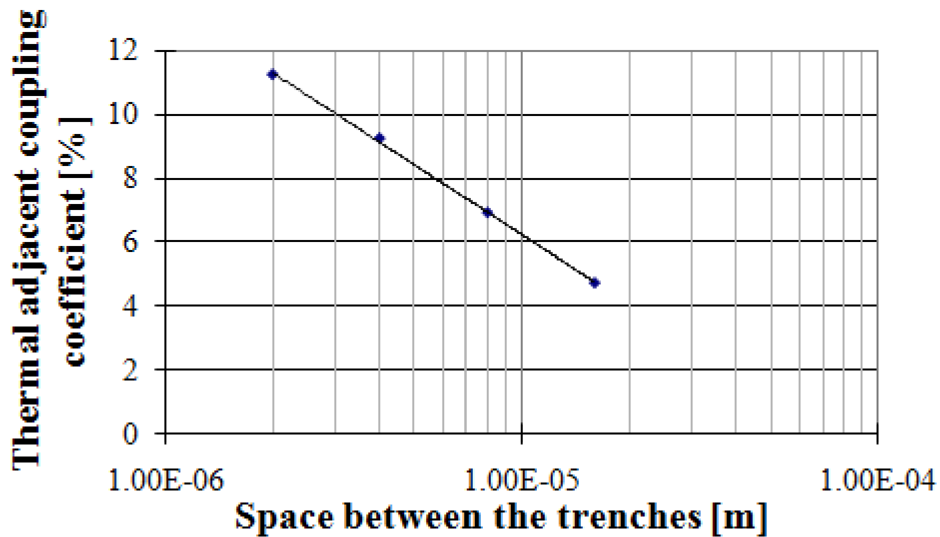


Figure 4.14 Thermal adjacent coupling coefficient of the test structure 2. The space between trenches is varied from 2 um to 16 um.

The thermal impedances of the central BJT in test structure 1 and test structure 2 are affected by the outer BJTs since the outer BJTs intercept the heat flow. The thermal resistances of the thermal impedances in both test structures are computed and summarized in Table 4.3.

Table 4.3 Thermal resistances in a single BJT and a BJT (as a ratio of the R_{TH} of an isolated device) surrounded by four BJTs and eight BJTs. The space between the trenches is 2 um.

	Single BJT	Central BJT - Structure 1 (Four BJTs)	Central BJT - Structure 2 (Eight BJTs)
Ratio of R_{TH} Simulation [%] (DAVINCI)	100	131	132

This simulation result show the thermal resistance of a BJT is increased by around 30% when the BJT is surrounded by the four BJTs. There is also a difference between the test structure 1 and the test structure 2. However, the difference is only around 1%. Therefore, the corner effect in the thermal resistance from the four corner BJTs can be ignored.

4.5 Measurement of Thermal Adjacent Coupling in Series

As shown in Figure 4.15, two central BJTs used to generate heat are located in the eight by three BJT geometry. These two BJTs share the base, emitter and collector

connections together and are used by the heat source. Each BJT in position 1(P1), position 2(P2) and position 3(P3) is used to measure temperature using the forward Gummel method.

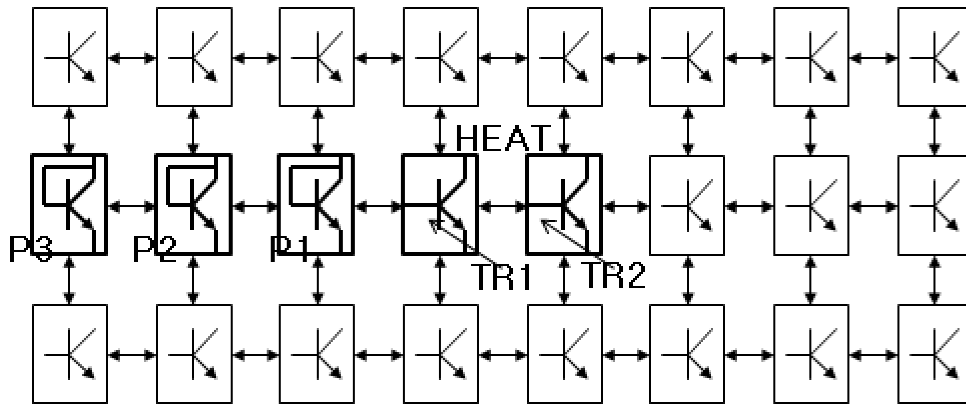


Figure 4.15 Diagram of the test structure 3. The distance between BJTs is 2 um.

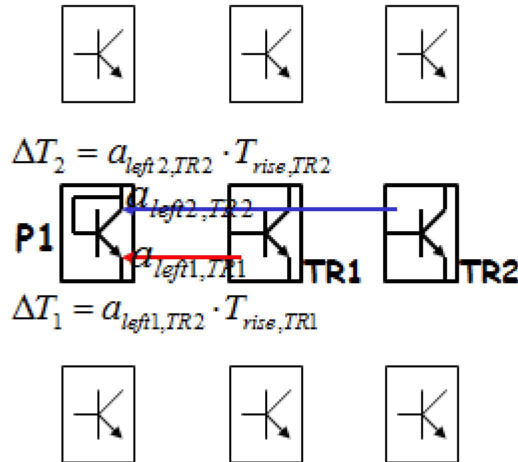


Figure 4.16 Partial diagram of the test structure 3 to measure the thermal adjacent coupling coefficients in position one.

TR1 and TR2 share base, emitter and collector connections together and are made to consume a range of power levels controlled by the constant base voltage and

the varied collector voltage to generate different heat. The emitter is connected to the ground. This heat affects the BJT in position one by the thermal adjacent coupling. The increased temperature by the heat sources (two central BJTs) is :

$$T_{Measured,position1} = \Delta T_{1,posiont1} + \Delta T_{2,position1} + T_{Ambient} \quad (4.24)$$

where $\Delta T_{1,position1}$ is the increased temperature caused by TR1 on BJT P1, $\Delta T_{2,position1}$ is the increased temperature caused by TR2 on BJT P1 and $T_{Ambient}$ is the ambient temperature. Equation (4.24) can be converted using the thermal adjacent coupling coefficients :

$$T_{Measured} = a_{left1,TR1} \cdot T_{rise,TR1} + a_{left2,TR2} \cdot T_{rise,TR2} + T_{Ambient} \quad (4.25)$$

where $a_{left1,TR1}$ is the thermal adjacent coupling coefficient between the heat source (TR1) and BJT P1. Also, $a_{left2,TR2}$ is the thermal adjacent coupling coefficient between the heat source (TR2) and BJT P1. $T_{rise,TR1}$ and $T_{rise,TR2}$ are the increased temperature at TR1 and TR2 :

$$T_{rise,TR1} = T_{rise,TR2} = \frac{1}{2} \cdot P_{DISS,Total} \cdot Z_{TH} \quad (4.26)$$

Thus, equation (4.25) can be written as :

$$T_{Measured} = T_{rise,TR} \cdot \left(a_{left1,TR1} + a_{left2,TR2}\right) + T_{Ambient} \quad (4.27)$$

The thermal adjacent coupling coefficients are :

$$a_{left1,TR1} + a_{left2,TR} = 2 \cdot \frac{\Delta T_{Measured}}{\Delta P_{DISS,Total}} \cdot \frac{1}{Z_{TH}} \tag{4.28}$$

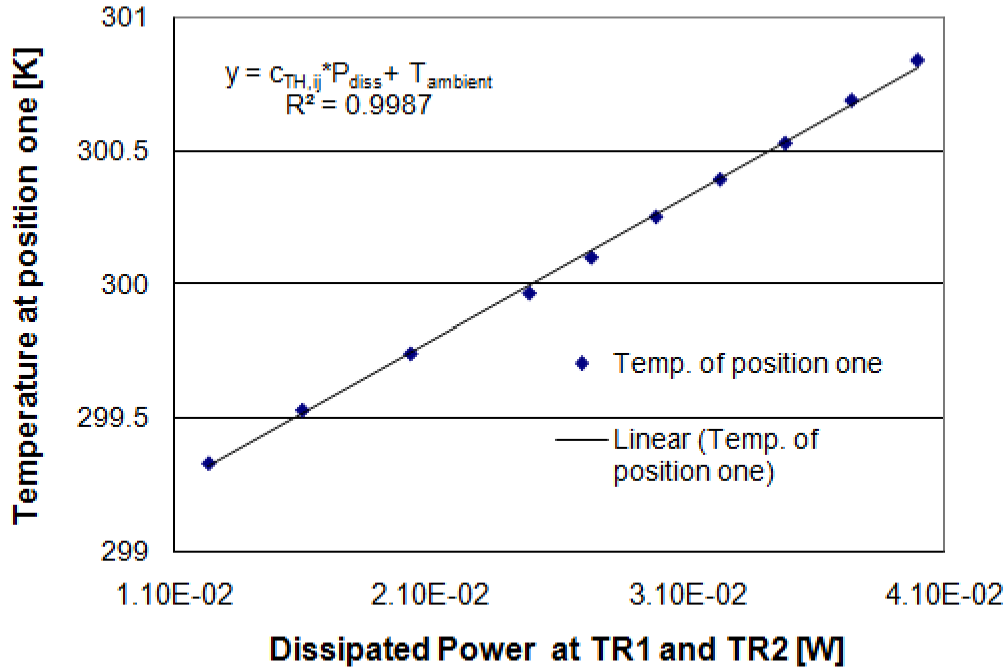


Figure 4.17 One sampled measurement results of position one in the test structure 3.

The same procedure can be used to measure the thermal adjacent coupling coefficient in position two in Figure 4.18. The relationship between the measured temperature and the thermal adjacent coupling coefficients are :

$$T_{Measured} = a_{left2,TR1} \cdot T_{rise,TR1} + a_{left3,TR2} \cdot T_{rise,TR2} + T_{Ambient} \tag{4.29}$$

where $a_{left2,TR1}$ is the thermal adjacent coupling coefficient between the heat source (TR1) and BJT P2. Also, $a_{left3,TR2}$ is the thermal adjacent coupling coefficient between

the heat source (TR2) and BJT P2. $T_{rise,TR1}$ and $T_{rise,TR2}$ are the increased temperature at TR1 and TR2 :

$$T_{rise,TR1} = T_{rise,TR2} = \frac{1}{2} \cdot P_{DISS,Total} \cdot Z_{TH} \tag{4.30}$$

Thus, equation (4.29) can be written as :

$$T_{Measured} = T_{rise,TR} \cdot \left(a_{left2,TR1} + a_{left3,TR2}\right) + T_{Ambient} \tag{4.31}$$

The thermal adjacent coupling coefficients are :

$$a_{left2,TR1} + a_{left3,TR} = 2 \cdot \frac{\Delta T_{Measured}}{\Delta P_{DISS,Total}} \cdot \frac{1}{Z_{TH}} \tag{4.32}$$

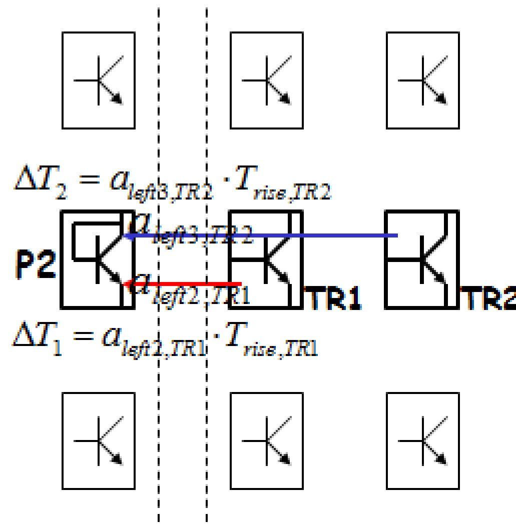


Figure 4.18 Partial diagram of the test structure 3 to measure the thermal adjacent coupling coefficients in position two.

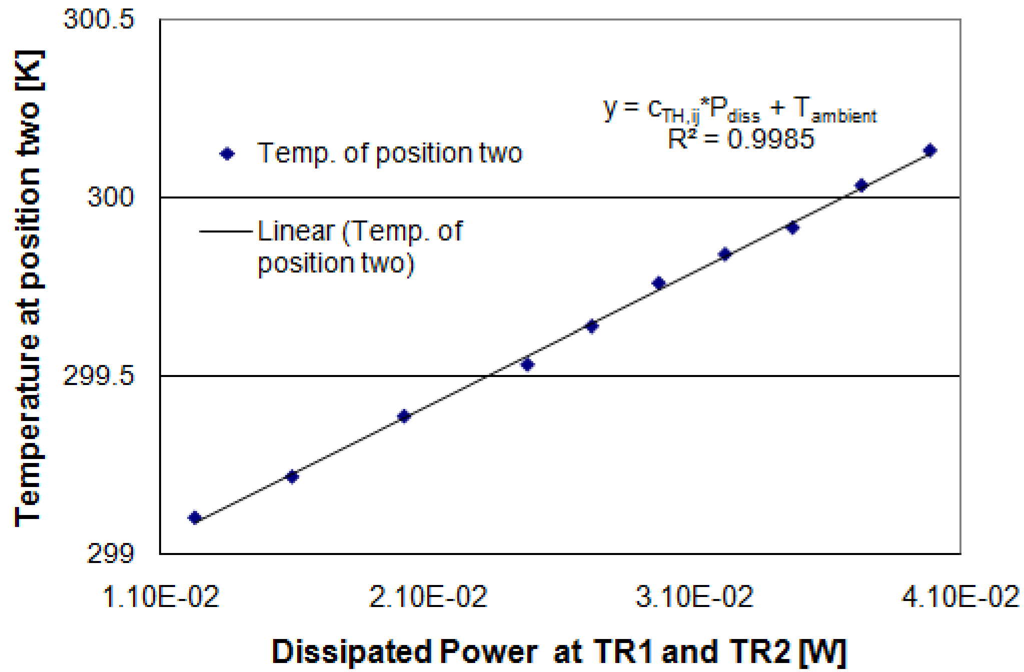


Figure 4.19 One sampled measurement results of position two in the test structure 3.

The same procedure can be used to measure the thermal adjacent coupling coefficient in position three in the Figure 4.20. The relationship between the measured temperature and the thermal adjacent coupling coefficients are :

$$T_{Measured} = a_{left3,TR1} \cdot T_{rise,TR1} + a_{left4,TR2} \cdot T_{rise,TR2} + T_{Ambient} \tag{4.33}$$

where $a_{left3,TR1}$ is the thermal adjacent coupling coefficient between the heat source (TR1) and BJT P3. Also, $a_{left4,TR2}$ is the thermal adjacent coupling coefficient between the heat source (TR2) and BJT P3. $T_{rise,TR1}$ and $T_{rise,TR2}$ are the increased temperature at TR1 and TR2 :

$$T_{rise,TR1} = T_{rise,TR2} = \frac{1}{2} \cdot P_{DISS,Total} \cdot Z_{TH} \tag{4.34}$$

So, the equation (4.33) can be written as :

$$T_{Measured} = T_{rise,TR} \cdot \left(a_{left3,TR1} + a_{left4,TR2}\right) + T_{Ambient} \tag{4.35}$$

The thermal adjacent coupling coefficients are :

$$a_{left3,TR1} + a_{left4,TR} = 2 \cdot \frac{\Delta T_{Measured}}{\Delta P_{DISS,Total}} \cdot \frac{1}{Z_{TH}} \tag{4.36}$$

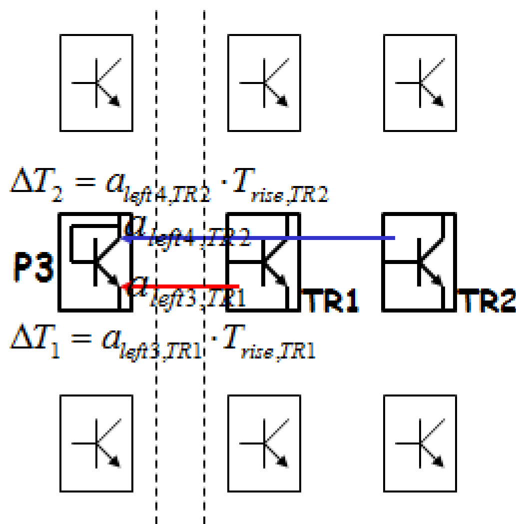


Figure 4.20 Partial diagram of the test structure 3 to measure the thermal adjacent coupling coefficients in position three.

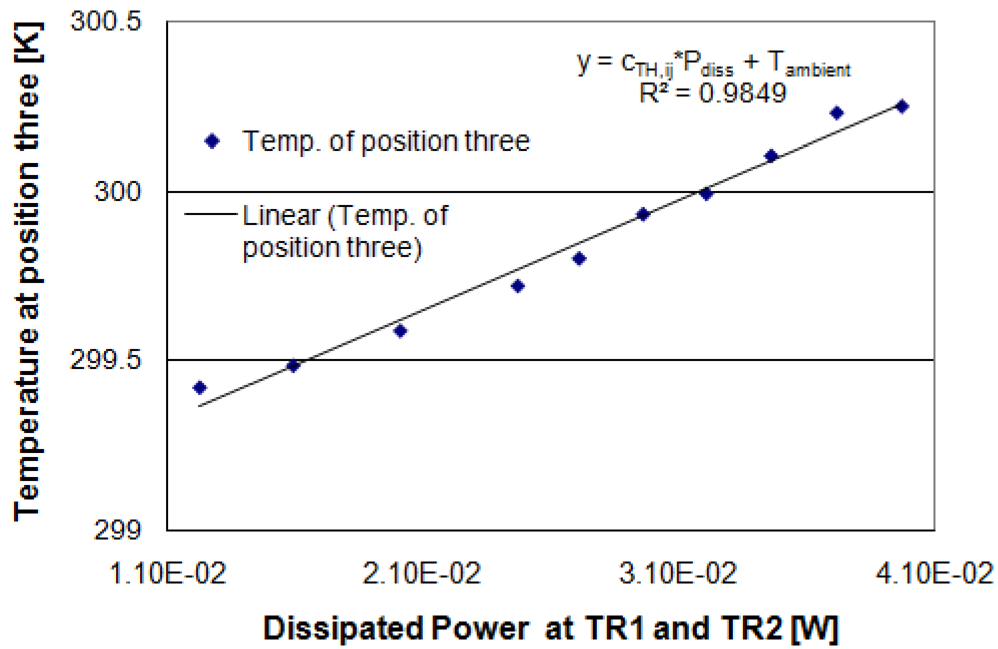


Figure 4.21 One sampled measurement results of position three in the test structure 3.

Table 4.4 Averaged thermal adjacent coupling coefficients of the structure 3

	Position 1	Position 2	Position 3
Thermal Adjacent Coupling coefficients [%]	12.1	8.5	7.1

The measured thermal adjacent coupling coefficients are summarized in Table 4.4. The thermal adjacent coupling coefficients in each position (n) are the sum of $a_{left,n-1}$ and $a_{left,n}$. If the first thermal adjacent coupling coefficient ($a_{left,1}$) is found, the rest of the thermal adjacent coupling coefficients can be calculated. The value of $a_{left,1}$ is around 7.3 [%] in the other measurement. Each value of the thermal adjacent coupling coefficients is shown in Figure 4.22.

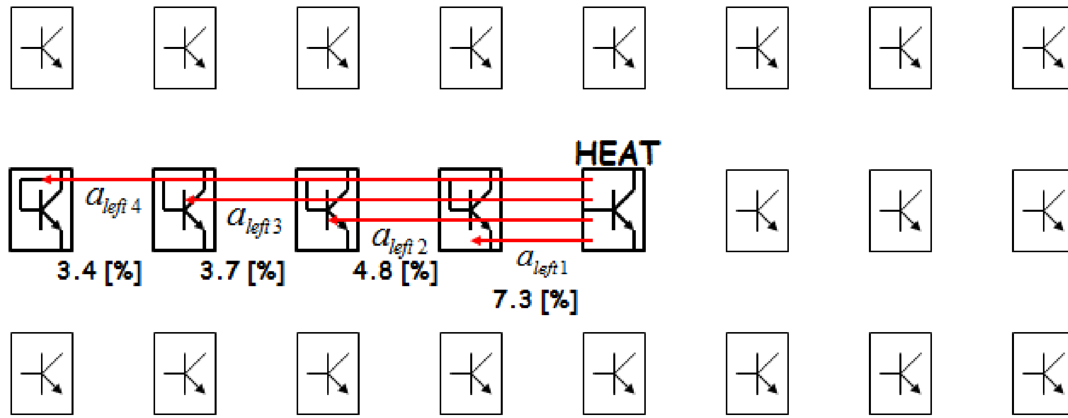


Figure 4.22 Thermal adjacent coupling coefficients in the test structure 3.

There is a possible mathematical relation between the thermal adjacent coupling coefficient and the order of the position for BJT. It can be :

$$a_{left,n} = S_{slope} \cdot \ln(n_{position}) + SC_1 \tag{4.37}$$

where S_{slope} is a slope constant, $n_{position}$ is the order of the position for BJT, and SC_1 is a compensation constant.

4.6 Conclusion

The mathematical expression of the thermal adjacent coupling is proposed in equation 4.6 and equation 4.7. The voltage-controlled voltage-source concept is

adopted into the thermal network to implement the thermal adjacent coupling between the BJTs.

Two structures were designed to measure the thermal adjacent coupling coefficient between BJTs. The main purpose for these two structures was to measure the thermal adjacent coupling coefficient and to check how the four corner BJTs affect the thermal adjacent coupling. The measured thermal adjacent coupling coefficients in both structures are almost same. The possible explanation for this may be the connections between outer BJTs. In test structure 1, the measured temperature is the average temperature of the outer four BJTs. However, the measured temperature in test structure 2 is the average temperature of the outer eight BJTs. It is reasonable to assume that the temperature of the four corner BJTs in test structure 2 is less than the temperature of the other four BJTs which have more shared silicon with the central BJT in test structure 2.

Each structure is also simulated by Davinci for comparison. The distance between the trenches varies from 2 um to 16 um. The relationship between the thermal adjacent coupling coefficient and the distance can be expressed by a log function in equation 4.23.

The thermal coupling coefficients in the series of BJTs (Test structure 3) are measured and the relation is explained in the mathematical form from equation 4.24 to equation 4.36. The relationship between the thermal adjacent coupling coefficient and the order of BJT position can be expressed by a log function given in equation 4.37.

CHAPTER 5

CONCLUSION AND FUTURE WORK

Self-heating is very important role in the analog circuit design. Self-heating occurs when a BJT is heated up by the power consumed by the same BJT. Thermal adjacent coupling is the fact that the power consumed in one BJT affects the temperature of adjacent BJTs. These two thermal effects are investigated and analyzed in this dissertation. This research emphasizes self-heating and thermal adjacent coupling of both a single device and multiple devices.

The general thermal impedance model is explained and the compact thermal model for DIBJT is also briefly explained in chapter 2. The five element compact model is developed on the basis of the previous work. If each thermal impedance value of the five element compact model is calculated with accuracy, the more accurate thermal model for self-heating can be obtained. A new technique has been developed to extract each thermal impedance of the five element compact model for the dielectrically isolated bipolar junction transistor in chapter 3. The new method uses the thermal simulation tool – Davinci. There are several conditions to extract the seed values for the five element compact model. After Davinci simulations using these conditions, the curve fitting method in Origin and optimization method in ICCAP is used to calculate the final values of the five element compact model. The previous method focuses on calculating the thermal resistances of the five element compact model. However, this

new method can extract the thermal resistances and the thermal capacitances. Therefore, more accurate circuit simulation results for the thermal effects can be implemented.

The device is non-isothermal. Therefore, the temperature of each emitter region is different. The maximum temperature of the device is not the temperature of the space charge region which is assumed as the heat source of the device. So, the difference between these two temperatures should be evaluated. There is around 4.7% difference between the total thermal resistance values by these two methods in section 3.5. This difference should be considered to use the proposed method.

The values of the thermal resistances in the five element compact model are calculated in three structures in section 3.6. Then, the values of the thermal resistances are computed by the proposed method. These values are compared to evaluate the proposed method. The main differences are in the wafer thermal resistance and the distributed thermal resistance. The value of the wafer thermal resistance is over calculated by the compact model calculation than that by the simulation extraction in all three cases. The value of the distributed thermal resistance is under calculated by the compact model calculation than that by the simulation extraction in all three cases. The tub area is the key to the mismatch in the values of the thermal resistances. If the tub area is increased, the percentage of the mismatch is also increased

The five element compact model has been developed for the thermal effects. One of these five elements, $Z_{dist,m}$ is related to the heating effect from an thermal adjacent coupling. The modified five element compact thermal model is explained in chapter 4. The value of this impedance depends on the number of adjacent BJTs, the

thickness of the epitaxial layer, the thickness of the isolation oxide, the geometry of the silicon tub, etc. The mathematical expression of the thermal adjacent coupling is proposed in equation 4.8 and equation 4.9. The voltage-controlled voltage-source concept is adopted into the thermal network to implement the thermal adjacent coupling between BJTs. The technique to measure the temperature of BJT is explained in section 4.3.

Two structures were designed to measure the thermal adjacent coupling coefficient between BJTs. The main purpose for these two structures was to measure the thermal adjacent coupling coefficient and to check how the four corner BJTs affect the thermal adjacent coupling. The measured thermal adjacent coupling coefficients in both structures are almost same values in section 4.4. The possible explanation for this may be the connections between outer BJTs. In test structure 1, the measured temperature is the average temperature of the outer four BJTs. However, the measured temperature in test structure 2 is the average temperature of the outer eight BJTs. It is reasonable to assume that the temperature of the four corner BJTs in test structure 2 is less than the temperature of the other four BJTs which have more shared silicon with the central BJT in test structure 2.

Each structure is also simulated by Davinci for comparison. The distance between the trenches varies from 2 um to 16 um. The relationship between the thermal adjacent coupling coefficient and the distance can be expressed by a log function in equation 4.23.

The thermal coupling coefficients in the series of BJTs (Test structure 3) are measured and the relationship is explained in the mathematical form in section 4.5.

In this paper, the measurements are in the DC domain and the simulations are in the time domain. The delay time in self-heating or the thermal adjacent coupling should be considered in the real circuit simulations. The new technique to extract the thermal impedance gives this delay time (thermal time constant) in self-heating, and the circuit simulation results with these values are well evaluated [77]. In the thermal adjacent coupling, it is hard to extract the thermal time constant by measurements. The estimated thermal time constant can be calculated by Davinci simulation. However, the values are not evaluated by the measurements. So, characterizing and measuring the thermal adjacent coupling coefficient in time domain will be one of the future work.

APPENDIX A

LAYOUTS OF THE TEST STRUCTURES

Test structure 1 is designed to measure the thermal coupling between the inner device and the outer four devices which are tied together and located at left, right, back and front and the test structure 2 has four more devices at each corner to check the corner effect. The structure layouts are shown in Figure A.1 and A.2.

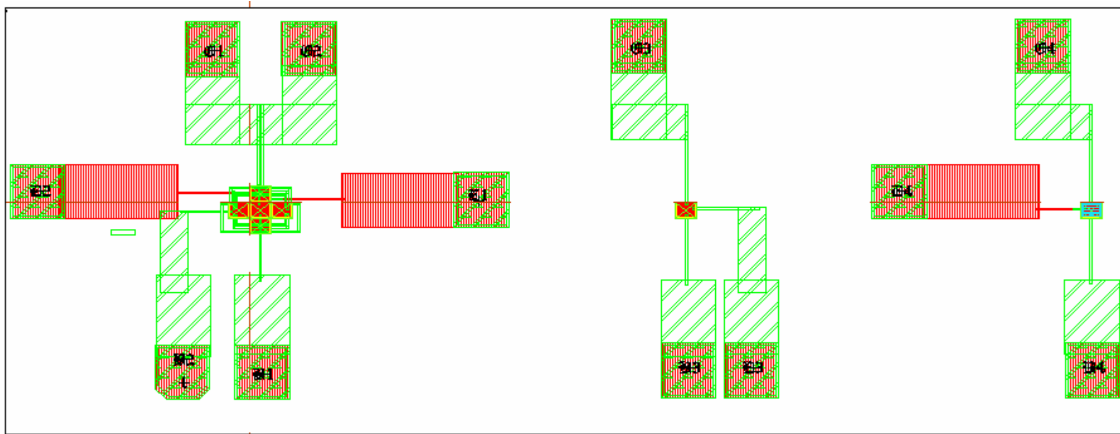


Figure A.1. Layout of the test structure 1.

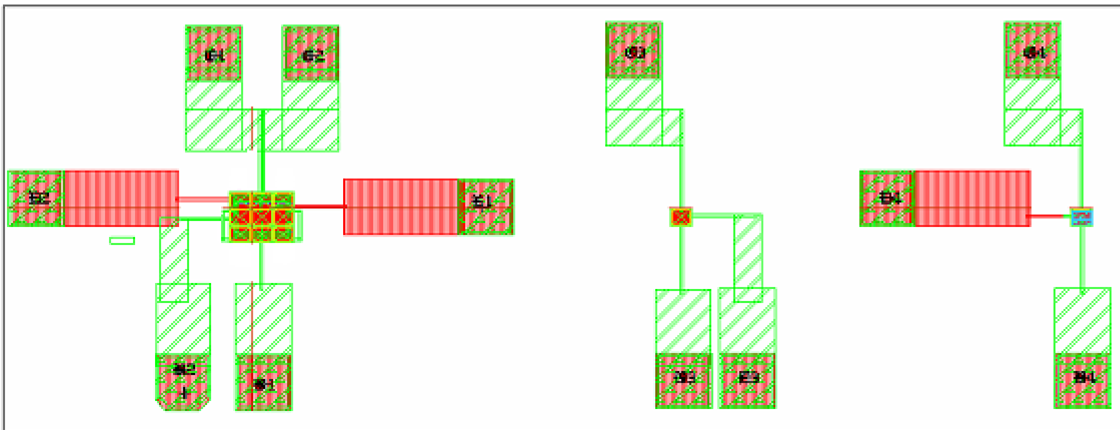


Figure A.2. Layout of the test structure 2.

Test structure 3 is designed to measure the thermal coupling in the series. The center two devices are tied together and shared the connections such as the emitter, the base and the collector. Other devices have the shared emitter and the independent base and collector. The structure is shown in Figure A.3.

Figure A.3. The layout of the test structure 3.

APPENDIX B

ONE SAMPLE CODE OF DAVINCI

The code that was written for the simulation – Davinci consists of three parts. The structure is defined in the first part, the doping and other conditions are defined second part and the simulation conditions such as bias are defined the last part. The sample code of Davinci is :

```
TITLE Davinci - Self heating of single emitter BJT

COMMENT Mesh Specifications
MESH ^DIAG.FLI

COMMENT X-MESHING

COMMENT Isolation - Left side 2000um
X.MESH  X.MIN=-2001  X.MAX=-1       N.SPACES=5

COMMENT Basic structure - Box
X.MESH  X.MIN=-1     X.MAX=0        N.SPACES=2
X.MESH  X.MIN=0      X.MAX=5.0      N.SPACES=5
X.MESH  X.MIN=6.0    X.MAX=7.0      N.SPACES=2
X.MESH  X.MIN=7.0    X.MAX=10.0     N.SPACES=3
X.MESH  X.MIN=10.0   X.MAX=11.0     N.SPACES=4
X.MESH  X.MIN=11.0   X.MAX=14.0     N.SPACES=3
X.MESH  X.MIN=14.0   X.MAX=16.0     N.SPACES=2
X.MESH  X.MIN=16.0   X.MAX=20.0     N.SPACES=4
X.MESH  X.MIN=20.0   X.MAX=21.0     N.SPACES=2

COMMENT Isolation -Right side 2000 um
X.MESH  X.MIN=21.0   X.MAX=2021.0   N.SPACES=5

COMMENT Y-MESHING
COMMENT Basic structure - Box
Y.MESH  Y.MIN=-1     Y.MAX=0        N.SPACES=1
Y.MESH  Y.MIN=0      Y.MAX=0.8      N.SPACES=8
Y.MESH  Y.MIN=0.8    Y.MAX=2.0      N.SPACES=2
Y.MESH  Y.MIN=2.0    Y.MAX=4.0      N.SPACES=3
Y.MESH  Y.MIN=4.0    Y.MAX=5.0      N.SPACES=1

COMMENT Bottom 400 um
Y.MESH  Y.MIN=5.0    Y.MAX=405      N.SPACES=3
```

```
COMMENT Z-MESHING
Z.MESH  Z.MIN=0        Z.MAX=5.0       N.SPACES=5
Z.MESH  Z.MIN=5.0      Z.MAX=8.0       N.SPACES=3
Z.MESH  Z.MIN=8.0      Z.MAX=10.0      N.SPACES=2
Z.MESH  Z.MIN=10.0     Z.MAX=11.0      N.SPACES=2

COMMENT Back 2000 um
Z.MESH  Z.MIN=11.0     Z.MAX=2011.0    N.SPACES=5

COMMENT REGION SPECIFICATIONS
REGION       SILICON

COMMENT Isolation
COMMENT Isolation-Top
REGION  OXIDE Y.MAX=0

COMMENT Isolation - Bottom separation Oxide
REGION  OXIDE      X.MIN=-2001          X.MAX=2021.0
+                  Y.MIN=4.0            Y.MAX=5.0
+                  Z.MIN=0              Z.MAX=2011.0

COMMENT Isolation – Left Trench
REGION  OXIDE      X.MIN=-1             X.MAX=0
+                  Y.MIN=0              Y.MAX=4.0
+                  Z.MIN=0              Z.MAX=11.0

COMMENT Isolation – Right Trench
REGION  OXIDE      X.MIN=20.0           X.MAX=21.0
+                  Y.MIN=0              Y.MAX=4.0
+                  Z.MIN=0              Z.MAX=11.0

COMMENT Isolation – Back Trench
REGION  OXIDE      X.MIN=0              X.MAX=20.0
+                  Y.MIN=0              Y.MAX=4.0
+                  Z.MIN=10.0           Z.MAX=11.0


COMMENT ELECTRODE SPECIFICATIONS
ELECTR  NAME=Base          X.MIN=5.0    X.MAX=7.0
+                          Z.MIN=0      Z.MAX=8.0
+                          Y.MIN=-1     Y.MAX=0.0

ELECTR  NAME=Collector            X.MIN=14.0   X.MAX=16.0
```

```
+                                     Z.MIN=0       Z.MAX=8.0
+                                     Y.MIN=-1      Y.MAX=0.0
ELECTR  NAME=Emitter                  X.MIN=10.9    X.MAX=12.9
+                                     Z.MIN=0       Z.MAX=5.0
+                                     Y.MIN=-1      Y.MAX=0.0

COMMENT  Boundary Condition
ELECTR  NAME=Heat_sink                BOTTOM        THERMAL

COMMENT  Doping profile
PROFILE N-TYPE N.PEAK=5E15 UNIFORM OUT.FILE=S1SI

COMMENT EMITTER PROFILE
PROFILE N-TYPE N.PEAK=1E20   Y.MIN=0  DEPTH=0.0 Y.CHAR=0.10
+        X.MIN=10      X.MAX=11             Z.MIN=0       Z.MAX=5.0
+ XY.RAT=0.75 ZY.RAT=0.75

COMMENT BASE PROFILE
PROFILE P-TYPE N.PEAK=1E17   Y.MIN=0.0     Y.CHAR=0.2
+        X.MIN=5.0     X.MAX=7.0    XY.RAT=0.75
+        Z.MAX=8.0     ZY.RAT=0.75
PROFILE P-TYPE N.PEAK=4E17   Y.MIN=0.3     Y.CHAR=0.14
+        X.MIN=5.0     X.MAX=7.0    XY.RAT=0.75
+        Z.MAX=8.0     ZY.RAT=0.75

COMMENT COLLECTOR PROFILE
PROFILE N-TYPE N.PEAK=1E18   X.MIN=14.0    X.MAX=16.0
+        Z.MIN=0       Z.MAX=8.0    Y.MIN=0       Y.MAX=4.0    Y.CHAR=0.27
PROFILE N-TYPE N.PEAK=1E18   X.MIN=0.0     X.MAX=20.0
+        Z.MIN=0       Z.MAX=8.0    Y.MIN=2.0     Y.MAX=4.0    Y.CHAR=0.17


COMMENT   Regrids on doping
REGRID    DOPING  LOG  IGNORE=OXIDE RATIO=2  SMOOTH=1  ^Z.REGRID
+        IN.FILE=S1SI            OUT.FILE=S1SM

PLOT.3D   BOX  BOUND  GRID  SCALE  FILL
+          CAMERA=(-1100,-1000,-1100)
+        TITLE="1st Doping Regrid"


COMMENT CHECK STRUCTURE
PLOT.2D Z.PLANE=0 BOUND GRID JUNC SCALE FILL
PLOT.2D Y.PLANE=2.0 BOUND GRID JUNC SCALE FILL
```

```
PLOT.2D X.PLANE=11.0 GRID SCALE FILL

COMMENT MODELING THE TRANSISTOR
MODELS ANALYTIC        FLDMOB   PRPMOB   CONSRH   AUGER   BGN

COMMENT  Initial solution
SYMB     CARRIERS=0 ILUCGS
METHOD   ILU.ITER=700
SOLVE    V(Collector)=0 V(Base)=0
SYMB     CARRIERS=2 ILUCGS
SOLVE    V(Collector)=0.0 V(Base)=0.0 OUT.FILE=S1SS

PRINT TEMPERAT
SAVE OUT.FILE=S1SMS.tdf TDF



COMMENT TRANSIENT ANALYSIS OF A DI BJT

COMMENT Read in simulation mesh
MESH IN.FILE=S1SM
LOAD    IN.FILE=S1SS


COMMENT Create columnar format for all the temperatures

$ Max temp points
EXTRACT NAME=Tmax INITIAL=0 EXPRESSI="max(@tl;@Tmax)"
+PRINT

EXTRACT NAME=nTmax EXPRESSI="@node.num"
+       COND=!(@tl<@Tmax) print


MODELS ANALYTIC          FLDMOB   PRPMOB   CONSRH   AUGER   BGN
SYMB  NEWTON CARRIERS=2 LAT.TEMP COUP.LAT BLOCK.MA
LOG  OUT.FILE=851_1e_time.tif TIF
SOLVE OUT.FILE=S1S100A00
SOLVE  V(Base)=0.8 V(Collector)=2 TSTEP=1E-13 TSTOP=100E-3

PRINT TEMPERAT
                        SAVE OUT.FILE=Transient_DIBJT_time.tdf TDF
```

REFERENCES

[1] J. R. Schwank, V. Ferlet-Cavrois, M. R. Shaneyfelt, P. Paillet and P. E. Dodd, "Radiation Effects in SOI Technologies", *IEEE Transactions on Nuclear Science*, Vol. 50, No. 3, pp. 522-538, June 2003.

[2] Q. Quyang, J. Cai, T. Ning, P. Dldiges and J. B. Johnson, "A Simulation Study on Thin SOI Bipolar with Fully or Partially Depleted Collector", *Bipolar/BiCMOS Circuits and Technology Meeting,* pp. 28-31, September 2002.

[3] M. Ieong and P. Oldiges, "Technology modeling for emerging SOI devices", *Simulation of Semiconductor Processes and Devices*, pp. 225-230, September 2002.

[4] O. W. Purbo and C. R. Selvakumar, "High-Gain SOI Polysilicon Emitter Transistors", *Electron Device Letters*, Vol. 12, No. 11, pp. 635-637, November 1991.

[5] D. Shain and R. Badilo, "A Trench Isolated SOI Bipolar Process", *SOS/SOI Technology Conference*, pp. 83-84, October 1990.

[6] L. Geppert "A Better Bipolar Transistor for Wireless ICs", *IEEE Spectrum*, Vol. 40, No. 12, pp. 20-21, December 2003.

[7] J. S. Brodsky, R. M. Fox and D. T. Zweidinger, "A Physics-Based Dynamic Thermal Impedance Model for Vertical Bipolar Transistors on SOI Substrates," *IEEE Transactions on Electron Devices*, Vol. 46, No. 12, pp. 2333-2339, December 1999.

[8] B. G. Malm, E. Haralson, T. Johansson and M. Ostling, "Self-Heating Effects in a BiCMOS on SOI Technology for RFIC Applications," *IEEE Transactions on Electron Devices*, Vol. 52, No. 7, pp. 1423-1428, July 2005.

[9] R. M. Fox, S. G. Lee and D.T. Zweidinger, "The effects of BJT self-heating on circuit behavior," *IEEE J. of Solid-State Circuits*, Vol. 28, No. 6, pp 678 −685, June 1993.

[10] R. C. Joy and E. S. Schlig, "Thermal Properties of Very Fast Transistors," *IEEE Transactions on Electron Devices*, Vol. 17, No. 8, pp. 586-594, August 1970.

[11] S. G. Lee, "A Review of Self-Heating Effects on Bipolar Circuits," *Proc. Southcon/94 Conf.*, pp. 138-142, March 1994.

[12] C. Anghel, R. Gillon and A. M. Ionescu, "Self-Heating Characterization and Extraction Method for Thermal Resistance and Capacitance in HV MOSFETs," *IEEE Electron Device Letters*, pp. 1-3, 2004.

[13] http://www.national.com/nationaledge/aug01/860.html

[14] N. Nenadovic, S. Mijalkovic, L. K. Nanver, L. K. Vandamme, V. Alessnadro, H. Schellevis, and J. W. Slotboom, "Extraction and Modeling of Self-Heating and Mutual Thermal Coupling Impedance of Bipolar Transistors," *IEEE J. Solid-State Circuits*, vol. 39, No. 10, pp. 1764-1772, October 2004.

[15] Y. S. Chung and B. Baird, "Electrical-Thermal Coupling Mechanism on Operating Limit of LDMOS Transistor," *IEDM.2000*, pp.83-86, December 2000.

[16] N. Nenadovic, V. d'Alessandro, F. Tamigi, A. Griffo, L. K. Nanver and J. W. Slotboom, "Thermal Instability in Two-Finger Bipolar Transistors," *European Solid State Device ESSDERC '03, 33rd Conference*, September 2003.

[17] L. La Spina, N. Nenadovic, V. d'Alessandro, L. K. Nanver, and N. Rinaldi, "FEAT – A Simulation Tool for Electrothermal Analysis of Multifinger Bipolar Transistors," *Eurocon 2005*.

[18] D. J. Walkey, T. J. Smy, R. G. Dickson, J. S. Brodsky, D. T. Zweidinger, and R. M. Fox, "Equivalent Circuit Modeling of Static Substrate Thermal Coupling Using VCVS Representation," *IEEE J. Solid-State Circuits*, vol. 37, No. 9, pp. 1198-1206, September 2002.

[19] D. L. Blackburn, "A Review of Thermal Characterization of Power Transistors," *IEEE Trans. Electron Devices*, vol. 23, pp. 831-838, August 1976.

[20] R. L. Carter and W. A. Davis and H. R. Russell, Research Review for National Semiconductor - Santa Clara, 27 pp., February 2005.

[21] J. J. Ebers and J. L. Moll, "Large-signal behavior of junction transistors," *Proc. IRE*, vol. 42, No. 12, pp. 1761-1772, December 1954.

[22] M. G. Rowlands, "Improved Method for Evaluating the Static Parameters of the Ebers-Moll Transistor Model", *Electronics Letters*, Vol. 12, No. 1, pp. 34-36. January 1976.

[23] http://eesof.tm.agilent.com/docs/iccap2002/MDLGBOOK/7DEVICE_MODELING/3TRANSISTORS/1GummelPoon/GP_DOCU.pdf.

[24] M. Rittweger, A. Wien, K. Brenndorfer and I. Wolff, "Device Modeling of Plastic Molding Packaged Bipolar Transistors by Use of 3D EM Simulations', *Wireless Communications Conference*, pp. 134-137, August 1997.

[25] C.C. McAndrew, J.A. Seitchik, D.F. Bowers, M. Dunn, M. Foisy, I. Getreu, M. McSwain, S. Moinian, J. Parker, D.J. Roulston, M. Schroter, P. Van Wijnen, L.F. Wagner, "VBIC95, the vertical bipolar inter-company model ," *IEEE Journal of Solid-State Circuits*, vol. 31, No. 10, pp. 1476 – 1483, October 1996.

[26] X. Cao, J. McMacken, K. Stiles, P. Layman, J. J. Lion, A. Ortiz-Conde, and S. Moinian, "Comparison of the New VBIC and Conventional Cummel-Poon Bipolar Transistor Models," *IEEE Transaction of Electron Device*, vol. 47, No. 2, pp. 427-433, February 2000.

[27] F. Lin, T. Zhou, B. Chen, B. L. Ooi, and P. S. Kooi, "Extraction of VBIC Model for SiGe HBTs Made Easy by Going through Gummel-Poon Model," *Proc. SPIE* , vol. 4228, pp. 249-258, 2000.

[28] G. W. Huang, K. M. Chen, J. F. Kuan, Y. M. Deng, S. Y. Wen, D. Y. Chiu and M. T. Wang, "Silicon BJT Modeling Using VBIC Model," *Microwave Conference*, pp. 240 – 243, December 2001.

[29] A. O. Adan, T. Naka, A. Kagisawa and H. Shimizu, "SOI as a Mainstream IC Technology", *IEEE International SOI Conference*, pp. 9-12, October 1998.

[30] A. J. Auberton-Herve, “SOI : Materials to Systems”, *International Electron Devices Meeting*, pp. 3-10, December 1996.

[31] S. Krishnan, J. G. Fossum and M. M. Pelella, “BiMOS Modeling for Reliable SOI Circuit Design”, *IEEE International SOI Conference*, pp. 140-141, October 1996.

[32] M. N. Ozisik, *Heat Conduction*, 2nd ed. New York: Wiley, 1993.

[33] M. M. Yovanovich, Y. S. Muzychka, and J. R. Culham, “Spreading Resistance of Isoflux Rectangles and Strips on Compound Flux Channels,” *J. Thermophysics and Heat Transfer*, vol. 13, No. 4, pp.495-500, December 1999.

[34] Y. H, T. Houston, R. Rajgopal, K. Joyner and C. Teng, “Isolation Techniques for 256Mbit SOI DRAM Application”, *IEEE International SOI Conference*, pp.26-27, October 1995.

[35] B. E. Kareh, B. Chen and T. Stanley, “Silicon On Insulator – An Emerging High-Leverage Technology”, *IEEE Transactions On Components, Packagine, and Manufacturing Technology*, Vol. 18, No. 1, pp. 187-194, March 1995.

[36] A. Marshall, C. R. Cleavelin, W. Xiong, C. Pacha, C. Russ, K. V. Arnim, T. Schulz, K. Schruefer, G. Knoblinger and P. Patruno, “Slicon on Insulator – The Perfect Material for Implantable Electronics?”, *IEEE Engineering in Medicine and Biology Workshop*, pp. 118-121, November 2007.

[37] F. Driussi, D. Esseni, L. Selmi, D. Buca, S. Manti, M. Luysberg, R. Loo, D. Nguyen, M. Reiche, M. Schmidt, M. C. Lemme and H. Kurz, “Fabrication, Characterization and Modeling of Strained SOI MOSFETs with Very Large

Effective Mobility", *37th European Solid State Device Research Conference*, pp. 315-318, September 2007.

[38] I. Hamaguchi, T. Fujita, T. Yano and K. Kajiyama, "Reduced Dislocation Density in SIMOX Wafer by Multi-Energy Single Implantation", *IEEE International SOI Conference*, pp. 12-13, October 1992.

[39] F. Udrea, D. Garner, K. Sheng, A. Popescu, H. T. Lim and V. I. Milne, "SOI power devices", *Electronics & Communication Engineering Journal*, Vol. 12, No. 1, pp. 27-40, Feburary 2000.

[40] V. A. Kushner, K. Park, D. K. Schroder and T. J. Thornton, "Low-Frequency-Noise Spectroscopy of SIMOX and Bonded SOI Wafers", *IEEE Transactions on Electron Devices*, Vol. 54, No. 12, pp. 3378-3382, December 2007.

[41] A. Ogura, 'Highly Uniform SOI Fabrication by Applying Voltage during KOH Etching of Bonded Wafers", *IEEE International SOI Conference*, pp. 58-59, October 1995.

[42] I. V. Grekhov, L. S. Kostina, T. S. Argunova, E. I. Beliakova, T. V. Kudriavseva, M. Gutkin, E. D. Kim and S. C. Kim, "Fabrication of High Quality SOI Bonding Materials by Modified Direct Wafer Bonding Technique", *22nd International Conference on Microelectronics*, pp. 487-490, May 2000.

[43] H. Nishizawa, S. Azuma, T. Yoshitake, K. Yamada, T. Ikeda, H. Masuda and A. Anzai, "A Fully SiO_2-Isolated Self-Aligned SOI-Bipolar Transistor for VLSIs", *Bipolar Circuits and Technology Meeting*, pp. 53-58, September 1991.

[44] J. D. Hayden, J. D. Burnett, J. R. Pfiester and M.P. Woo, "A new Technique for Forming a Shallow Link Base in a Double Polysilicon Bipolar Transistor", *IEEE Transactions on Electron Devices*, Vol. 41, No. 1, pp. 63-68, January 1994.

[45] K. O. Kenneth and W. S. Brad, "Effects of Buried Layer Geometry on Characteristics of Double Polysilicon Bipolar Transistors", *IEEE Electron Device Letters*, Vol. 19, No. 5, pp.160-162, May 1998.

[46] J. Jomash, G. Ghibaudo, F. Balestra and J. L. Pelloie, "Impact of Self-Heating Effects on the Design of SOI Devices Versus Temperature", *IEEE International SOI Conference*, pp.114-115, October 1995.

[47] Y. Feng, "Silicon Direct Bonding on Vacuum and Force", *IEEE International Conference on Mechatronics and Automation*, pp. 491-496, June 2006.

[48] E. Ganin, T. C. Chen, J. M. C. Stork, B. S. Meyerson, J. D. Cressler, G. Scilla, J. Warnock, D. I. Harame, G. L. Patton and T. H. Ning, "Epitaxial-Base Double-Poly Self-Aligned Bipolar Transistors", *Electron Devices Meeting*, pp. 603-606, December 1990.

[49] http://en.wikipedia.org/wiki/Thermal_conductivity

[50] http://en.wikipedia.org/wiki/Specific_Heat

[51] http://en.wikipedia.org/wiki/Heat_equation

[52] Synopsys, *Taurus Medici Davinci User Guide*, 2006.

[53] M. Carmona, S. Marco, J. Palacin, and J. Samitier, “A Time-Domain Method for the Analysis of Thermal Impedance Response Preserving the Convolution Form”, *IEEE Transactions of Components and Packaging Technology*, Vol. 22, No. 2, pp. 238-244, June 1999.

[54] http://www.originlab.com/index.aspx?s=8&lm=10

[55] http://eesof.tm.agilent.com/products/iccap_main.html

[56] David T. Zweidinger, Robert NI. Fox, Jonathan S. Brodsky, Taewon Jung, and Sang-Gug Lee, “Thermal Impedance Extraction for Bipolar Transistors,” *IEEE Transactions on Electron Devices*, Vol. 43, No. 2, pp. 342-346, February 1996.

[57] J. A. Lonac, A. Santarelli, I. Melczarsky and F. Filicori, “A Simple Technique for Measuring the Thermal Impedance and the Thermal Resistance of HBTs”, *13th GAAS Symposium*, pp.197-200, 2005.

[58] T. Lopez and R. Elferich, “Thermal Impedance Extraction Technique for Power MOSFETs”, *IEEE Power Electronics Specialists Conference*, pp. 2140-2146, June 2007.

[59] W. Jin, W. Jiu, S. K. H. Fung, P. C. H. Chan and C. Hu, “SOI Thermal Impedance Extraction Methodology and Its Significance for Circuit Simulation”, *IEEE Transactions on Electron Devices*, Vol. 48, No. 4, pp. 730-736, April 2001.

[60] S. F. Shams, C. C. McAndrew, I. S. Lim, and A. Zlotnicka, “SiGe HBT Self-Heating Modeling and Characterization from AC Data,” *IEEE BCTM 5.2*, 2002.

[61] A. Pacelli, P. Palestri, and M. Mastrapasqua, "Compact Modeling of Thermal Resistance in Bipolar Transistors on Bulk and SOI Substrates," *IEEE Transactions on Electron Devices*, vol. 49, No. 6, pp.1027-1033, June 2002.

[62] T. Vanhoucke, and G. A. M. Hurkx, "A New Analytical Model for the Thermal Resistance of Deep-Trench Bipolar Transistors," *IEEE Transactions on Electron Devices*, vol. 53, No. 6, pp.1379-1388, July 2006.

[63] D. T. Zweidinger, S. G. Lee, and R. M. Fox, "Compact Modeling of BJT Self-Heating in SPICE," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 12, No. 9, pp.1368-1375, September 1993.

[64] Y. Zhu, J. K. Twynam, M. Yagura, M. Hasegawa, T. Hasegawa, Y. Eguchi, A. Yamada, E. Suematsu, K. Sakuno, H. Sato, and N. Hashizume, "Analytical Model for Electrical and Thermal Transients of Self-Heating Semiconductor Devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, No. 12, pp.2258-2263, December 1998.

[65] N. Rinaldi, "Small-Signal Operation of Semiconductor Devices Including Self-Heating, with Application to Thermal Characterization and Instability Analysis," *IEEE Transactions on Electron Devices*, vol. 48, No. 2, pp.323-331, February 2001.

[66] F. Tamigi, N. Nenadovic, V. d'Alessandro, L. K. Nanver, N. Rinaldi, and J.W. Slotboom, "Modeling of Thermal Resistance Dependence on Design Parameters in Silicon-on-Glass Bipolar Transistors," *Proc. 24th International Conference on Microelectronics*, vol. 1, pp. 257-260, May 2004.

[67] N. Rinaldi, and V. d'Alessandro, "Theory of Electrothermal Behavior of Bipolar Tranistors: Part I – Single-Finger Devices," *IEEE Transactions on Electron Devices*, vol. 52, No. 9, pp.2009-2021, September 2005.

[68] N. Rinaldi, and V. d'Alessandro, "Theory of Electrothermal Behavior of Bipolar Tranistors: Part II – Two-Finger Devices," *IEEE Transactions on Electron Devices*, vol. 52, No. 9, pp.2022-2033, September 2005.

[69] N. Rinaldi, and V. d'Alessandro, "Theory of Electrothermal Behavior of Bipolar Tranistors: Part III – Impact Ionization," *IEEE Transactions on Electron Devices*, vol. 53, No. 7, pp.1683-1697, July 2006.

[70] M. M. Hossain, D. Kim, A. Chaugule, W. A. Davis, H. T. Russel and R. L. Carter, "Adjacent Device Thermal Effects Modeling and Characterization in Dielectrically Isolated Bipolar Technology", *ICSICT '06. 8th International Conference on Solid-State and Integrated Circuit Technology*, pp. 1256-1259, October 2006.

[71] W. Liu, "Thermal Coupling in 2-Finger Heterojunction Bipolar Transistors", IEEE Transaction on Electron Devices, Vol. 42, No. 6, pp. 1033-1038, June 1995.

[72] D. J. Walkey, T. J. Smy, R. G. Dickson, J. S. Brodsky, D. T. Zweidinger and R. M. Fox, "A VCVS-based Equivalent Circuit Model for Static Substrate Thermal Coupling", *Proceedings of the 2001 Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 102-105, September 2001.

[73] A. Chaugule, "Analysis and Characterization of Thermal Effects in Analog Circuits," MS Thesis, EE Department, UTA, December 2005.

[74] S. T. Nashiney, “Compact Thermal Modeling of Dielectrically-Isolated Bipolar Junction Transistors and Developments in Circuit Simulation”, MS Thesis, EE Department, UTA, August 2003.

[75] S. Rajaraman, “Analysis and Modeling of Thermal Impedance for Dielectrically-Isolated Bipolar Junction Transistors”, MS Thesis, EE Department, UTA, December 2003.

[76] B. L. Ooi, B. Chen, F. Lin, P. S. Kooi and C. S. Hui, “A Fast and Practical Approach to the Determination of Junction Temperature and Thermal Resistance for BJT/HBT Device”, *Microwave and Optical Technology Letters*, Vol. 35, No. 6, pp. 499-502, December 2002.

[77] Md Mahbub Hossain, “Thermal Effects on Analog Integrated Circuit Design,” Ph.D Thesis, EE Department, UTA, May 2007.

BIOGRAPHICAL INFORMATION

Daewoo Kim received his Bachelor of Engineering degree in Electrical & Electronic Engineering from Chun-Ang University. After his graduate, he started his career as a researcher in LG Semicon in Korea. He started his graduate studies at San Jose State University, California, United States of America in fall 1999. He transferred to California State University, Sacramento in spring 2000. He started his ph.D degree in Electrical Engineering at the University of Texas at Arlington in fall 2003. He joined the Analog Integrated Circuits Design Research Laboratory under the guidance of Dr. Ronald L. Carter in fall 2006. His research interest focuses on the thermal effect modeling and characterization. He worked as a graduate research assistant at UTA from fall 2007. He has received the TPEG and STEM doctoral fellowships at UTA.