THE DESIGN OF A PRECISION CURRENT MIRROR USING A HIGH-GAIN CURRENT AMPLIFIER

by

MEI-PING PUA

Presented to the Faculty of the Graduate School of
The University of Texas at Arlington in Partial Fulfillment
of the Requirements
for the Degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

December 2008

ACKNOWLEDGEMENTS

I would like to thank my supervisors Dr. Howard T. Russell, Jr., Dr. Ronald L. Carter, and Dr. W. Alan Davis for their guidance, patience, support, and encouragement throughout my study. As a new graduate student, I had scant knowledge and experience. Dr. Russell gave me great help in my research no matter in theoretical or lab experiment. Dr. Carter and Dr. Davis showed me their kindness and support during my learning process. I am also grateful to my research teammates. They are very kind to share, teach, and discuss all the information they know.

I thank God for giving me my family. Without the unconditional support and encouragement of my family, I could not be able to complete graduate school.

Last, I would like to thank my friends – Xu Lei, Suwon Park, church elders and Boram Seo who sincerely and faithfully pray for all my needs and my mental health during my study.

December 6, 2008

ABSTRACT

THE DESIGN OF A PRECISION CURRENT
MIRROR USING A HIGH-GAIN
CURRENT AMPLIFIER

MEI-PING PUA, M.S.

The University of Texas at Arlington, 2008

Supervising Professor: Dr. Howard T. Russell, Jr.

An improved high gain, precision, low sensitivity current mirror is designed around a feedback circuit. This mirror utilizes a buffered Widlar current mirror to drive the constant input reference current, two beta helpers to compensate for the loss of base current and an active load, and a feedback loop in the amplifier. This design provides a comparison node for detecting the input error signal. The output collector current is substantially equal to the input reference current when driving multiple transistor loads. The circuit has been fabricated with National's VIP10 process, which caters to the high gain bipolar technology. Measurement results obtained are a good reflection of the precision and low sensitivity to indicate a substantial agreement to the simulated results.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1

CURRENT MIRRORS

1.1 Introduction

Current mirrors find widespread applications in analog integrated circuits to generate bias currents for multiple sub-circuits connected as mirror loads [1, 2]. Current mirrors are circuits designed specifically to reflect an input reference current through active devices keeping the output current constant regardless of loading. Ideally, the output current is equal to the input reference current multiplied by a desired current gain. If the gain is unity, the input reference current is replicated to the output leading to the name *current mirror.*

The advantage of using current mirrors in biasing circuits is superior insensitivity of circuit performance to variations in power supply and temperature. In addition, current mirrors are frequently more economical than resistors in terms of the die area required to provide bias current of certain values, particularly for small values of bias current. When applied as the load element of a transistor amplifier, the amplifier voltage gain can be increased at low voltages. In practice, however, the output current is not an accurate reflection of the input reference current since real transistor-level current mirrors suffer many deviations from idea behavior.

1.2 Key Concepts in Current Mirrors

1.2.1. Widlar Current Mirror

The basic current mirror topology, known as the Widlar mirror, is shown in Figure 1.1. Transistor Q_1 functions as a diode-connected device since the base and collector are connected. This forces collector-base voltage V_{BC1} to zero. In addition, the base-emitter voltages of transistor Q_1 and Q_2, are equal to each other.

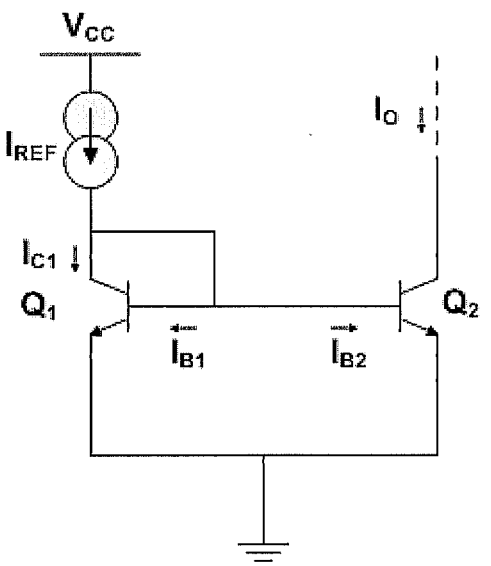


Figure 1.1 A Widlar current mirror

The mirror is driven by the constant input reference current I_{REF} while the output is the collector current of transistor Q_2 with the collector-base junction of Q_1 shorted. This connection forces Q_1 to operate in the forward-active region. For near-ideal current reflection, Q_2 must also operate in the forward-active region. Assuming the transistors in this circuit have very high βs, the base currents of Q_1 and Q_2 are very small and can be omitted. Thus, the output current is almost equal to the input reference current. With identical transistors Q_1 and Q_2, it follows that

$$I_{REF} = I_{C1} + I_{B1} + I_{B2} \tag{1.1}$$

since $I_{C1} = I_{C2} = I_O$,

$$I_{REF} = I_O + \frac{2I_O}{\beta}$$

$$I_O = \frac{I_{REF}}{1+\frac{2}{\beta}} \tag{1.2}$$

The current gain of this mirror is given by

$$\frac{I_O}{I_{REF}} = \frac{1}{1+\frac{2}{\beta}} \tag{1.3}$$

1.2.2 Buffered Widlar Current Mirror

Figure 1.2 shows the buffered Widlar current mirror where Q_3 is referred to as a *beta helper* [1]. If Q_1 and Q_2 are identical, the emitter current of transistor Q_3 is

$$\begin{aligned} I_{E3} &= I_{B1} + I_{B2} = \frac{2I_{C1}}{\beta} \\ I_{B3} &= \frac{I_{E3}}{\beta+1} = \frac{2}{\beta(\beta+1)} I_{C1} \end{aligned} \tag{1.4}$$

Kirchoff current law at the collector of Q_1 gives

$$I_{C1} = I_{REF} - \frac{2}{\beta(\beta+1)} I_{C1} = 0$$

Since $I_{C1} = I_{C2} = I_O$

$$I_{REF} = I_{C1}\left[1+\frac{2}{\beta(\beta+1)}\right] \tag{1.5}$$

from which I_O is expressed as

$$Io = \frac{I_{REF}}{1+\frac{2}{\beta(\beta+1)}} \tag{1.6}$$

Equation (1.6) shows that the systematic gain error from finite β has been reduced by a factor of [β + 1] which is the current gain of emitter follower Q_3.

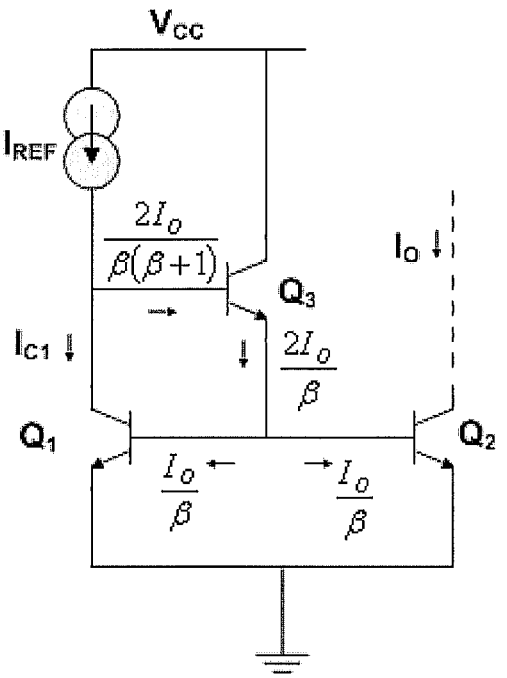


Figure1.2 A buffered Widlar current mirror

1.2.3 Wilson Current Mirror

The basic circuit of the Wilson current mirror is shown in Figure 1.3 [4]. The operation of this current mirror is based on two assumptions:

1. all three transistors have the same common-emitter current gain β, and
2. transistor Q_1 and Q_2 are matched, so their collector currents are equal at the same base current.

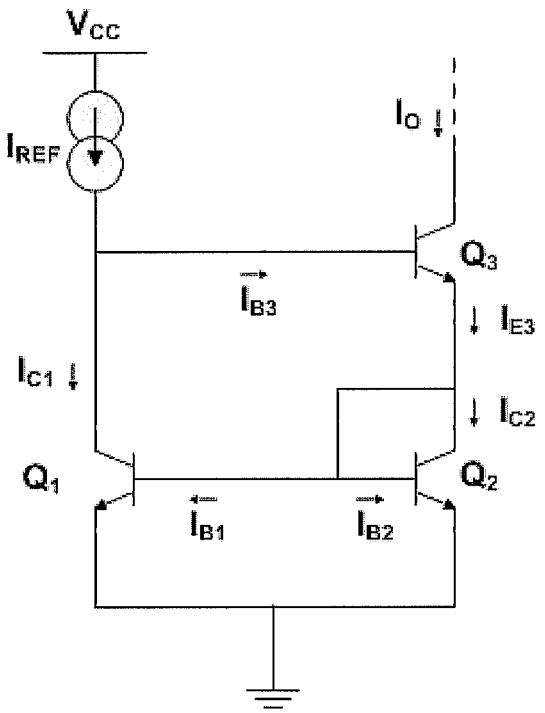


Figure 1.3 Wilson current mirror

From Figure 1.3,

$$I_{REF} = I_{B3} + I_{C1} \tag{1.9}$$

$$I_{E3} = I_{C2} + I_{B1} + I_{B2} \tag{1.10}$$

Under assumption 2, collector and base currents of Q_1 and Q_2 are equal, so that (1.10) can be rewritten as

$$\begin{aligned} I_{E3} &= I_{C2} + 2I_{B2} = \left(1 + \frac{2}{\beta}\right) I_{C2} \\ I_{C1} &= I_{C2} = \left(\frac{\beta}{\beta + 2}\right) I_{E3} \end{aligned} \tag{1.11}$$

with (1.11) inserted into (1.9)

$$I_{REF} = I_{B3} + \left(\frac{\beta}{\beta+2}\right) I_{E3}$$
$$I_{REF} = \frac{I_{C3}}{\beta} + \left(\frac{\beta}{\beta+2}\right)\left(\frac{\beta+1}{\beta}\right) I_{C3} \qquad (1.12)$$

since $I_{C3} = I_{CO}$, I_{CO} is expressed as

$$I_{C3} = \frac{1}{1+\frac{2}{\beta(\beta+2)}} I_{REF}$$
$$I_O = \frac{1}{1+\frac{2}{\beta(\beta+2)}} I_{REF} \qquad (1.13)$$

This section has introduced mirror circuits developed from simple topologies, such as the Widlar current mirror, the buffered Widlar current mirror, and the Wilson current mirror. However, these topologies are not capable of accurate reflection of the input reference current into the output current after driving multiple loads. Based on this issue, R.G Thompson and F. Matsumoto have designed topologies to approach the result as close as the ideal current mirror. At this point, extensive research has been done to study the precise replication of the input reference current from which the current mirror UTA246P was designed. UTA246P has been designed with a topology that allows ten to twenty loads to be driven with a desired current gain is unity.

CHAPTER 2

KEY CONFIGURATIONS FOR PROPOSED CURRENT MIRROR

2.1 Introduction

In this chapter, several important fundamental configurations will be introduced in order to better understand the proposed current mirror topology. The first section of this chapter will introduce and briefly analyze the R.G. Thomson current mirror circuit, which is the prior art for the proposed current mirror. The next section will include the concept of basic feedback.

2.1.1 R.G. Thomson Current Mirror

In April 1988, R.G. Thomson filed a patent for a current mirror in "*Current Reference for Feedback Current Source*" [3]. This circuit is shown in Figure 2.1. In his patent, the input reference current, I_{REF}, and feedback loop consisting of Q_1, Q_2, Q_3 and Q_6, applied the simple Widlar current mirror topology. The amplifier stage consists of Q_3, Q_4, Q_5, and Q_6. This topology utilizes a resistor, R_{Bias}, and transistor Q_4 as a common emitter stage to achieve the desired current gain. Transistors Q_O, Q_{L1}, and Q_{Lm} represent the load transistors. The relation between the output current and the input reference current is shown in the equation below (See Appendix A1.1):

$$I_{CO} = \frac{I_{REF}}{\left(1+\frac{2}{\beta_n}\right)\left(\beta_n+\frac{1}{\beta_n}+\frac{m+3}{\beta_n\beta_p}\right)} + \frac{I_{RBias}}{\beta_n+\frac{1}{\beta_n}+\frac{m+3}{\beta_n\beta_p}} \tag{2.1}$$

$$I_{CO} = k_r I_{REF} + I_{offset}$$

where m represents the numbers of load transistors. The term k_r represents the mirror current gain while offset current is I_{offset}.

Equation (2.1) can be rewritten in terms of sensitivity and precision indicates by replacing m with

$$m = \beta_p \frac{I_L}{I_{CO}} \tag{2.2}$$

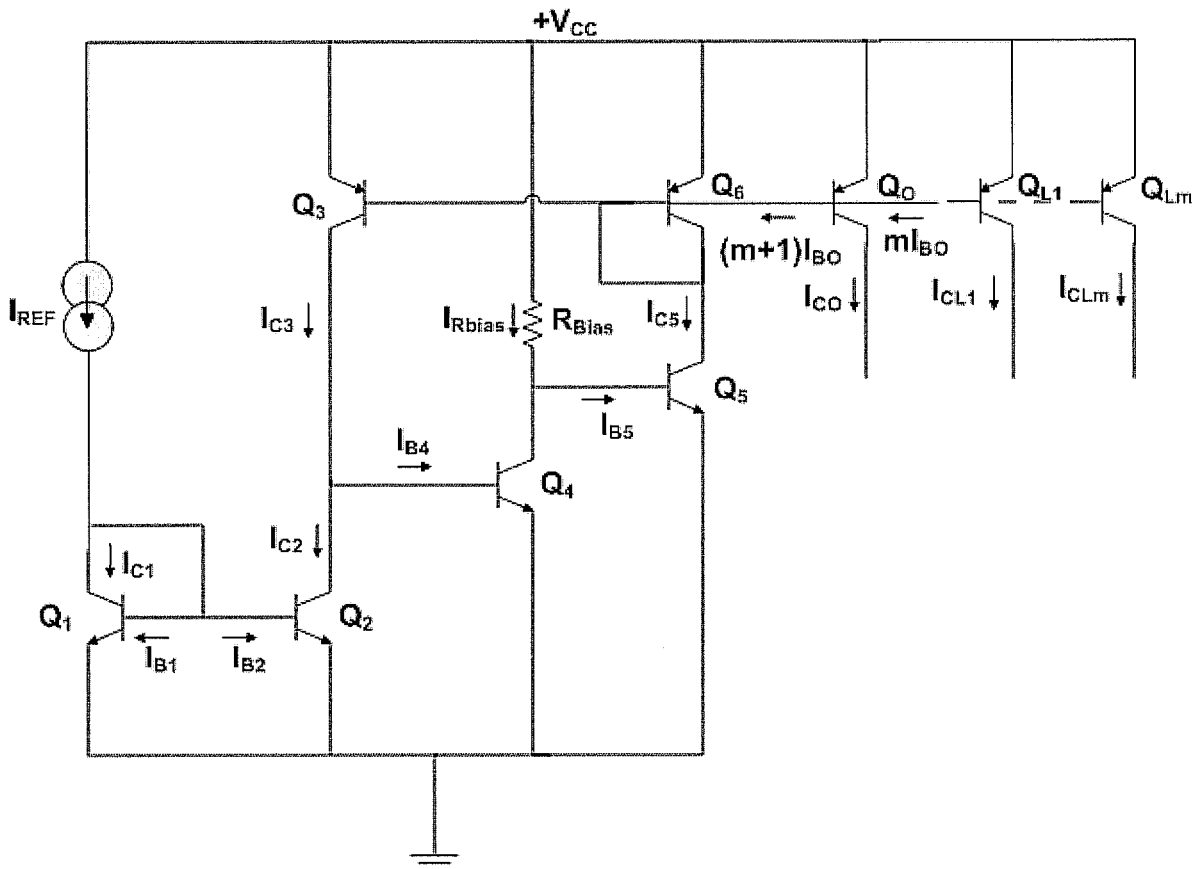


Figure 2.1 Current reference for feedback current source

Inserting (2.2) into (2.1), yields

$$I_{CO} = -\left[\frac{\frac{1}{\beta_p}}{\beta_n + \frac{1}{\beta_n} + \frac{3}{\beta_n \beta_p}}\right] I_L + \left[\frac{1}{\left(1+\frac{2}{\beta_n}\right)\left(\beta_n + \frac{1}{\beta_n} + \frac{3}{\beta_n \beta_p}\right)}\right] I_{REF} + \left[\frac{1}{\beta_n + \frac{1}{\beta_n} + \frac{3}{\beta_n \beta_p}}\right] I_{RBias} \tag{2.3}$$

$$I_{CO} = n_1 I_L + n_2 I_{REF} + I_{offset}$$

$$n_1 = \left[\frac{\frac{1}{\beta_p}}{\beta_n + \frac{1}{\beta_n} + \frac{3}{\beta_n \beta_p}} \right] \tag{2.4}$$

$$n_2 = \left[\frac{1}{\left(1 + \frac{2}{\beta_n}\right)\left(\beta_n + \frac{1}{\beta_n} + \frac{3}{\beta_n \beta_p}\right)} \right] \tag{2.5}$$

The detail explanation of n_1 and n_2 will be introduced in Chapter 3.

2.1.2 Basic Feedback Concepts

Feedback has become an important concept in circuit design topologies, and can be negative or positive [1]. Figure 2.2 shows the basic elements of a feedback system represented by a block diagram. The functional relationships between these elements are easily seen. An important factor to remember is that the block diagram represents flowpaths of control signals, but does not represent the flow of energy through the system or process.

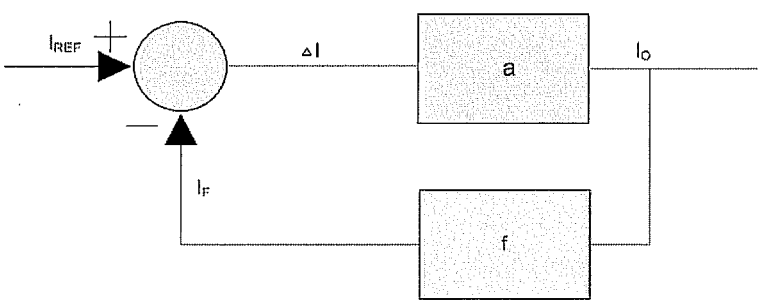


Figure 2.2 Feedback block diagram

In control systems, feedback consists of comparing a sample of the output of a system with the input and making a correction accordingly. In an amplifier circuit, the output should be a multiple of the input; therefore, for a feedback amplifier, the input is compared with attenuated version of the output.

Another aspect of Figure 2.2 is that it shows that the current is a signal-flow diagram only because the proposed current mirror is focused on the current; otherwise, the signal-flow diagram could show either a voltage or a current. The block labeled *a* is called the forward gain while the block labeled *f* is called the feedback function. The gain of the basic amplifier when the feedback network is not present is called the *open-loop gain* of the amplifier. The function of the feedback network is to sense the output signal I_o and develop a feedback signal I_F, which is equal to $f I_o$, where *f* is usually less than unity. This feedback signal is subtracted from the input signal I_{REF}, and the difference ΔI is applied to the basic amplifier. The gain of the system when the feedback network is present is called the *closed-loop gain*. For the basic amplifier we have

$$I_O = a\Delta I = a\left(I_{REF} - I_F\right) = a\left(I_{REF} - fI_0\right) \tag{2.6}$$

and thus

$$\frac{I_O}{I_{REF}} = \frac{a}{1+af} = \frac{1}{f}\left(\frac{af}{1+af}\right) = \frac{1}{f}\left(\frac{T}{1+T}\right) \tag{2.7}$$

where T is the *loop gain* which is the product af.

Chapter 3 will introduce the improvement current mirror topology. The differences between prior art, R.G Thomson circuit, and proposed current mirror topology are replacing R_{bias} with an active load, and adding two beta helper configurations, as well as feedback to obtain a higher loop gain for the proposed current mirror topology.

CHAPTER 3

CURRENT MIRROR UTA246P

3.1 Introduction

Having analyzed the different current mirrors (Chapter 1), and studied the key configurations extensively, the improvement study of the proposed current mirror is presented in this Chapter. This study describes the performance of the proposed current mirror designed to supply low-sensitivity, precise bias currents to multiple circuits connected as loads. The topology used in this mirror advances the art of current mirror circuit design by incorporating an adjustable bias circuit to compensate for the loss of base current from the input reference current, by applying feedback to enhance current regulation and to reduce sensitivity of the output current to additional loads, and by using NPN and PNP transistors for a fast response [2].

3.1.1 Description of the Proposed Topology

The schematic for the current mirror proposed in this thesis is shown in Figure 3.1. All NPN and PNP transistors have identical emitter areas [2]. The output current of this circuit is transistor Q_O which collects base currents from PNP transistors consisting of the collector current of transistor Q_O and the m load transistors Q_{L1} through Q_{Lm}. It is assumed that all base and collector currents are equal because all emitter areas are equal. This circuit uses $(m + 1)I_{BO}$ as the total bias current for the $(m + 1)$ output PNP transistors where I_{BO} is a base current of a single transistor. The function of current mI_{BO} at the base of transistor Q_O represents the load current I_L necessary to bias the load transistors Q_{L1} through Q_{Lm}. The load current I_L will affect the precision of I_{CO} by adding more transistors on the bias chain. Furthermore, the study of the sensitivity of I_{CO} to I_L is considered in this research.

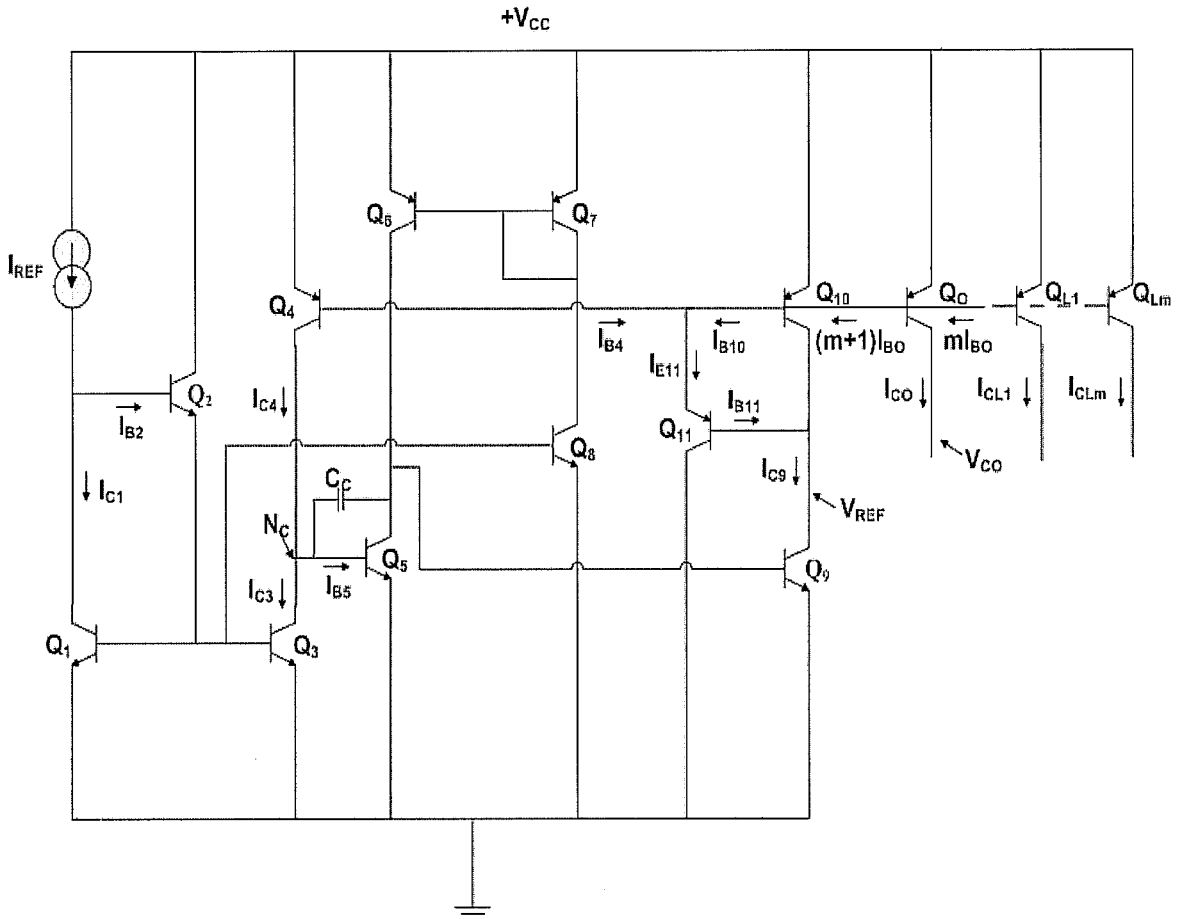


Figure 3.1 Schematic of the proposed topology

The input reference current I_{REF} uses a buffered Widlar current mirror to provide the current to this circuit design. The beta helper, Q_2, reduces the gain error from the input by a factor of $(\beta+1)$. This stage is often used in bipolar current mirrors with multiple outputs. Therefore, the input reference current consists of the base current of transistor Q_2 and the collector current of transistor Q_1, and can be expressed as

$$I_{REF} = I_{B2} + I_{C1} \tag{3.1}$$

The base current of transistor Q2 is very small due to the beta helper stage. However, the emitter current of transistor Q_2 provides base current for transistor Q_1, Q_3, and Q_8. It is

expressed in (3.2). Since it can be assumed the collector currents that Q_1, Q_3, and Q_8 are equal then

$$I_{E2} = I_{B1} + I_{B3} + I_{B8} = 3I_{B3} = \frac{3I_{C3}}{\beta_n} \tag{3.2}$$

The topology of the current mirror consists of a feedback circuit to provide control of the output current. The feedback loop includes PNP Q_4, Q_{10}, and Q_{11}. Transistor Q_{11} is another beta helper whose emitter current is the summation of transistor base currents in the feedback loop, this whose emitter current can be expressed as:

$$I_{E11} = I_{B4} + I_{B10} + ... + (m+1)I_{BO} \tag{3.3}$$

NPN transistors Q_5 and Q_9 make up the amplifier with Q_6 serving as an active load for Q_5. Transistor Q_7 and Q_8 bias Q_6 from the input reference current. In this manner, the feedback *f* achieves unity gain. The feedback circuit's comparison node is denoted as N_C. The input to the amplifier is the base current of Q_5 which is the difference between I_{C4} and I_{C3} that is

$$I_{B5} = I_{C4} - I_{C3} \tag{3.4}$$

These relations can be expressed as:

$$I_{C5} = I_{C6} - I_{C9} \tag{3.5}$$

$$I_{C8} = I_{B6} + I_{B7} + I_{C7} \tag{3.6}$$

The voltage at the collector of Q_O (V_{CO}) is set equal to V_{REF} to eliminate the Early effect. This mirror topology is incorporates a simple way to reduce the mirror instability by placing a capacitor C_C across the collector base junction of transistor Q_5, as shown in Figure 3.1. In theoretical, from (3.1) to (3.6), output collector current I_{CO} of PNP transistor Q_O refers to input reference current I_{REF} is expressed as (See Appendix B1.2):

$$I_{CO} = \frac{\left[1+\frac{1}{\beta_n\left(\frac{2}{\beta_p}+1\right)}\right]}{\left[1+\frac{3}{\beta_n(\beta_n+1)}\right]\left[1+\frac{1}{\beta_n^2}+\frac{m+3}{\beta_n^2\beta_p(\beta_p+1)}\right]} I_{REF} \qquad (3.7)$$

From (3.7), the numerator term is due to the transistor Q_9; the left term in the denominator is due to transistor Q_1, Q_3, and Q_8 while the load transistors cause the right term. This equation can be written as

$$I_{CO} = k_r I_{REF} + I_{offset}$$

where k_r is defined as the mirror gain function and I_{offset} is the offset current which is zero for this circuit [3]. Equation (3.7) shows that I_{CO} differs from I_{REF} only by the factor of betas of NPN transistor β_n and betas of PNP transistor β_p. Typically, the value of β is greater than 100; in addition, value of β_n for NPN is usually much greater than for PNP. In such case, current gain of proposed circuit from Equation 3.7 could be estimated by following two conditions,

1. $\frac{1}{\beta_n\left(\frac{2}{\beta_p}+1\right)} \approx 0$, so the numerator approach to 1 (3.7), and
2. $\frac{3}{\beta_n(\beta_n+1)} \approx 0$, and $\frac{1}{\beta_n^2}+\frac{m+3}{\beta_n^2\beta_p(\beta_p+1)} \approx 0$, so the denominator approach to 1 as well.

As a result, the effect of m on I_{CO} is significantly reduced, and the Equation 3.7 shows the current gain from this mirror topology is almost approached to be unity gain, $\frac{I_{CO}}{I_{REF}} \rightarrow 1$.

Next, from Equation (3.7) can be derived the term of the sensitivity for this design. To represent I_{CO} in terms of I_{REF} and I_L, m in Eq. (3.7) is replaced with

$$m = \beta_p \frac{I_L}{I_{CO}} \tag{3.8}$$

Inserting Eq. (3.8) into Eq. (3.7), yields

$$I_{CO} = -\left[\frac{\frac{1}{\beta_n^2(\beta_p+1)}}{1+\frac{1}{\beta_n^2}+\frac{3}{\beta_n^2\beta_p(\beta_p+1)}}\right] I_L + \left[\frac{1+\frac{1}{\beta_n\left(\frac{2}{\beta_p}+1\right)}}{1+\frac{1}{\beta_n^2}+\frac{3}{\beta_n^2\beta_p(\beta_p+1)}}\right] I_{REF} \tag{3.9}$$

$$I_{CO} = n_1 I_L + n_2 I_{REF}$$

With a constant input reference current I_{REF}, I_{CO} is a straight-line function of I_L. The slope of this function with respect to I_L is the coefficient n_1 that is defined by the sensitivity of I_{CO} to I_L that is [3]

$$n_1 = S(I_{CO}, I_L) = \left.\frac{dI_{CO}}{dI_L}\right|_{I_{REF}} \tag{3.10}$$

The slope of the function with respect to I_{REF} characterizes the precision of the output I_{CO}. With a constant load current I_L, the coefficient n_2 is defined by the precision of I_{CO} to I_{REF} where [3]

$$n_2 = S(I_{CO}, I_{REF}) = \left.\frac{dI_{CO}}{dI_{REF}}\right|_{I_L} \tag{3.11}$$

In this case, the sensitivity coefficient of n_1 ideally approaches to zero in unit A/A. On the other hand, the precision coefficient of n_2 ideally approaches to unity in unit A/A.

3.1.2 Simulation

SPICE VBIC transistor models are used in the simulation the performance of this proposed mirror (See Appendix A.2). The settings listed below are adopted in this analysis:

1. NSC provides the parameters of all the circuit models,
2. set to 10V for the supply voltage $+V_{CC}$,
3. provide constant input reference current I_{REF} at 100μA,
4. set V_{CO} = 8.445V where the collector of PNP transistor Q_O, in order to cancel the Early effect. This value is approximately equal to V_{REF}'s,
5. set to 1.25KΩ for all the emitter resistors, and 2 beta helper resistors are set 10KΩ, and
6. vary the load current I_L from zero to 50μA. The load current is the base current I_{BO} of PNP transistor Q_O.

Figure 3.2 and Figure 3.3 illustrate the analog environment settings

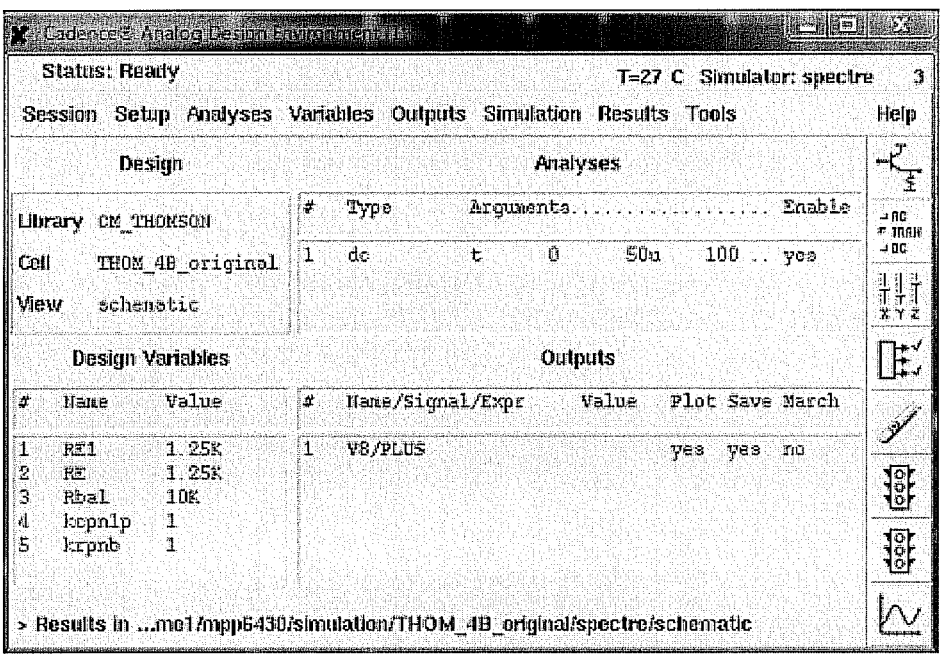


Figure 3.2 Cadence – analog design environment

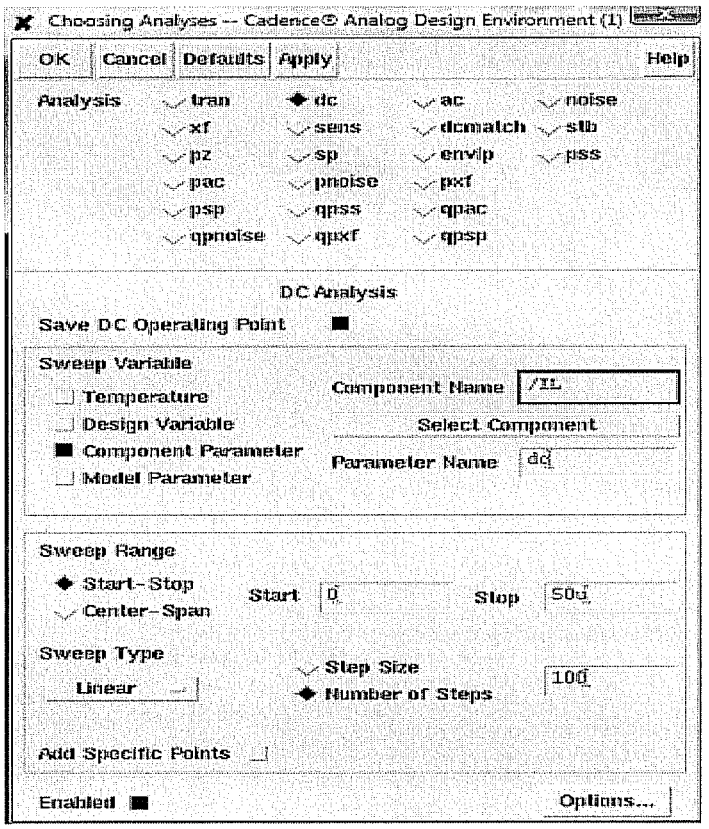
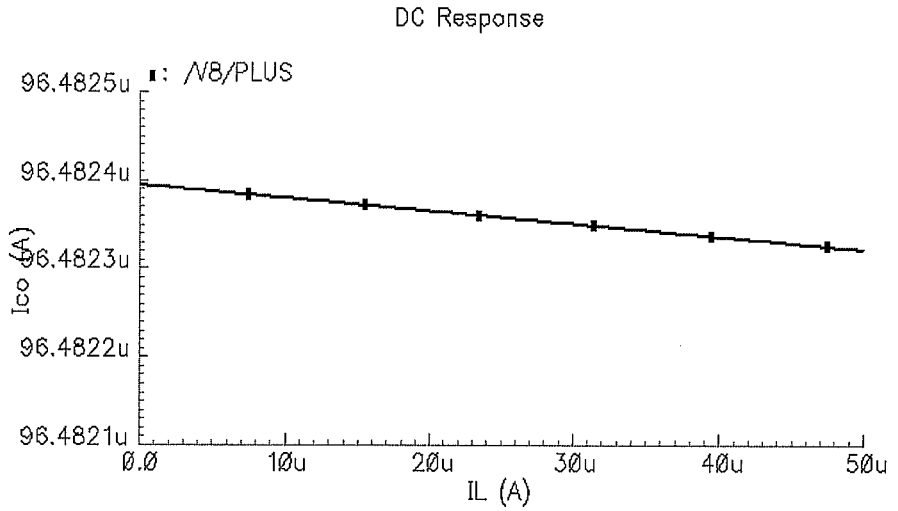


Figure 3.3 DC analysis with I_L setting

Finally, the simulation result for the mirror, is plotted for a constant I_{REF} in Figure 3.4(a). The plot indicates a straight-line relationship between I_{CO} and I_L with a negative slope, and in Figure 3.4(b) shows that the difference is in the range of pA.



(a)

File

Curve name map:

Curve1 - /V8/PLUS

Curve table:

	X value	Curve1
M2 (anchor)	5u	96.482387205u

Delta-curve table:

	dX value	Curve1

Delta-curve/delta-X (slope) table:

	Curve1

Curve name map:

Curve1 - /V8/PLUS

Curve table:

	X value	Curve1
M2 (anchor)	45u	96.482328369u

Delta-curve table:

	dX value	Curve1

(b)

Figure 3.4 (a) Output current I_{CO} verses load current I_L (b) two specific load currents to determine output current

3.1.3 Comparisons

Table 2.1 contains the simulated results for comparing this proposed topology with the eight other designs. The table contains analytical current gain inverse formulas, simulation of sensitivity coefficient, and precision coefficient. Along the slope plot from Figure 3.4(b) is shown the sensitivity and precision coefficients n_1 and n_2 which are

$$n_1 = -1.4714\mu \, A/A$$

$$n_2 = 0.964827 \, A/A$$

From the Table 3.1, the results show that the current gain for each design is a function of β and m. The difference percentage of the proposed current mirror is between input reference current I_{REF} and output current I_{CO} is approximately 3.65%. However among the eight designs, this proposed circuit has the significantly least sensitive to I_L. Thus, in long term the I_{CO} of this proposed circuit has stable current when more load transistors are added.

Table 3.1 Comparisons from simulation

Mirror Topology (I_{REF} = 100μA)	**Current Gain Inverse**	**Sensitivity Coefficient n_1 (μA/A)**	**Precision Coefficient n_2 (A/A)**	**Error Precision (%)**
Widlar	$1+\frac{m+2}{\beta}$	-970,669.3	0.970597	2.9403
Base current	$1+\frac{m+2}{\beta(\beta+1)}$	-9,670.88	0.991993	0.8007
Wilson	$1+\frac{1}{\beta+1}+\frac{m+2}{\beta(\beta+1)}$	-9,598.65	0.990325	0.9675
Thomson	$\left(1+\frac{2}{\beta_n}\right)\left(\beta_n+\frac{1}{\beta_n}+\frac{m+3}{\beta_n\beta_p}\right)$	-236.57	0.992497	0.7503
Matsumoto	$\left(1+\frac{1}{\beta^2}+\frac{m+2}{\beta^3}\right)$	-162.61	0.970949	2.9051
Proposed circuit	$\left(1+\frac{1}{\beta_n\left(\frac{2}{\beta_p}+1\right)}\right)^{-1}\left[1+\frac{3}{\beta_n(\beta_n+1)}\right]\left(1+\frac{1}{\beta_n^2}+\frac{m+3}{\beta_n^2\beta_p(\beta_p+1)}\right)$	-1.4714	0.964827	3.5173

3.1.4 Fabrication

This proposed circuit, named as UTA246p, has been fabricated on National Semiconductor Corporation's proprietary SOI bonded wafer process and packaged in 14 pin DIP. The die is 28 mils by 22 mils, and the layout is shown in Figure 3.5

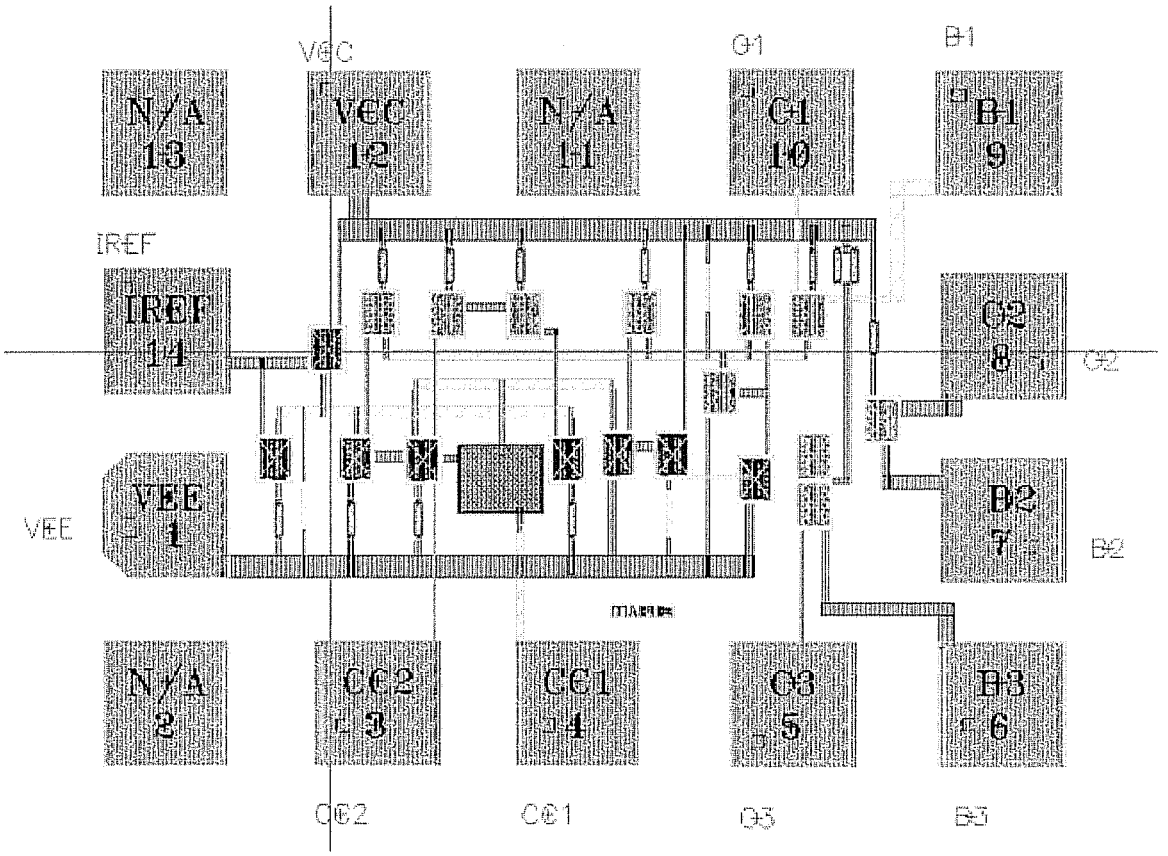


Figure 3.5 UTA246P layout

CHAPTER 4

TEST AND MEASUREMENT RESULTS

4.1 Introduction

The conclusions derived in Chapter 3 are verified in this chapter from actual tests that measure the performance of the UTA246P. The accuracy and the sensitivity of the output current, I_{CO}, depends on the change of load current, which behaves in a similar manner multiple transistor loads.

4.1.1 Clarification of Elements

The transistors and op-Amps used in the testbench are listed below:

1. PNP transistor: 2N3906
2. NPN transistor: 2N3904
3. op-Amp: TLC274

4.1.2 Testbench Analysis

A 10V voltage supply, V_{CC}, is used to bias the proposed current mirror. This voltage is generated from a simple emitter follower configuration shown in Figure 4.1. This circuit includes a 15V power supply V_{PS}, a 4.3KΩ resistor, a 10V zener diode, and a 10μF capacitor as the basic elements. The formulas used in calculating the 10V supply voltage from this configuration are derived in below where

$$I_{bias} = \frac{V_{PS} - V_{ZENER} - V_{BE1}}{R} = \frac{15V - 10V - 0.7V}{4.3K} = 1.0mA \tag{4.1}$$

is the Zener diode bias current. The 10V for V_{CC} is obtained by using KVL where

$$\begin{aligned} V_{CC} &= V_{ZENER} - V_{BE1} + V_{BE2} = 10V - 0.7V + 0.7V \\ V_{CC} &= 10V \end{aligned} \tag{4.2}$$

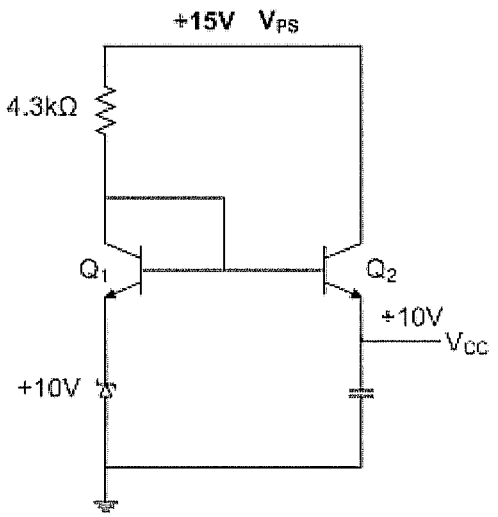


Figure 4.1 Voltage supply, V_{CC} = 10V

The 10V supply voltage V_{CC} from Figure 4.1 is connected to Pin 12 of the proposed current mirror chip. Pin 10 is the collector of the output transistor Q_O which is biased at 8.4V to cancel the Early effect. This voltage is produced by the voltage reference circuit shown in Figure 4.2 where the 10KΩ R_{TP1} is used to adjust the voltage it its desired value of 8.4V. This circuit is also used to measure Q_O's collector current (I_{CO}) by measuring the voltage across the 100KΩ feedback resistor. That is,

$$I_{CO} = \frac{V_n - V_O}{R_{F1}} \tag{4.3}$$

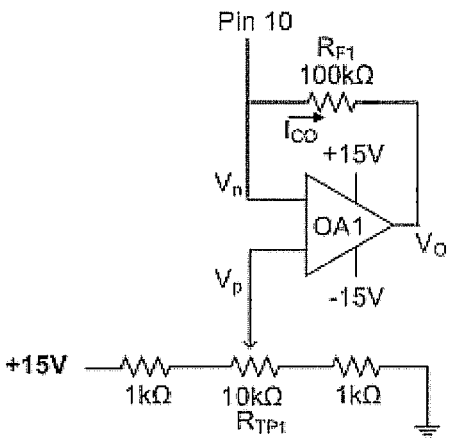


Figure 4.2 Output collector voltage, V_{CO}

The input reference current, I_{REF}, is set by an current mirror consisting of op-amp OA2, a 50KΩ pot, a PNP transistor Q_3, and 4 resistors, as shown in Figure 4.3. I_{REF} is adjusted by the 50KΩ pot R_{TP2} to obtain 100μA at the collector of Q_3 which is connected to Pin 14.

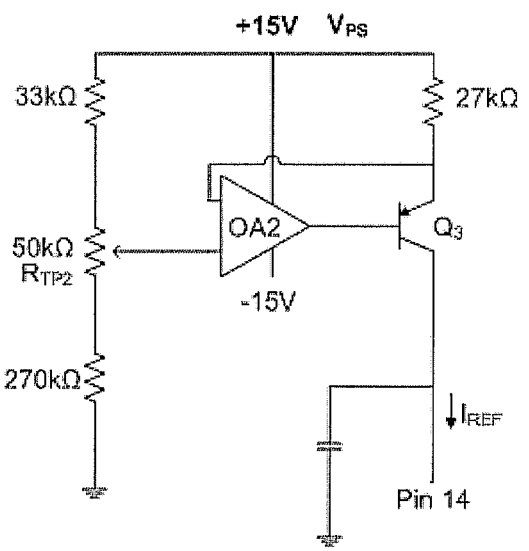


Figure 4.3 Input reference current, I_{REF}

The load current, I_L is generated from a buffered Widlar current mirror circuit consisting of transistors Q_4, Q_5 and Q_6, and the 100KΩ pot R_{TP3}. This current is applied to Pin 9 on the proposed current mirror chip as shown in Figure 4.4.

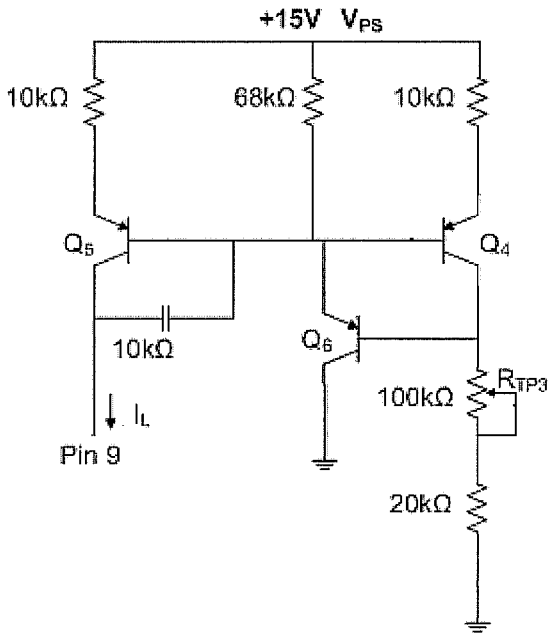


Figure 4.4 Load current, I_L

Finally, the circuits in Figures 4.1 through 4.4 are connected to the proposed current mirror chip shown in Figure 4.5.

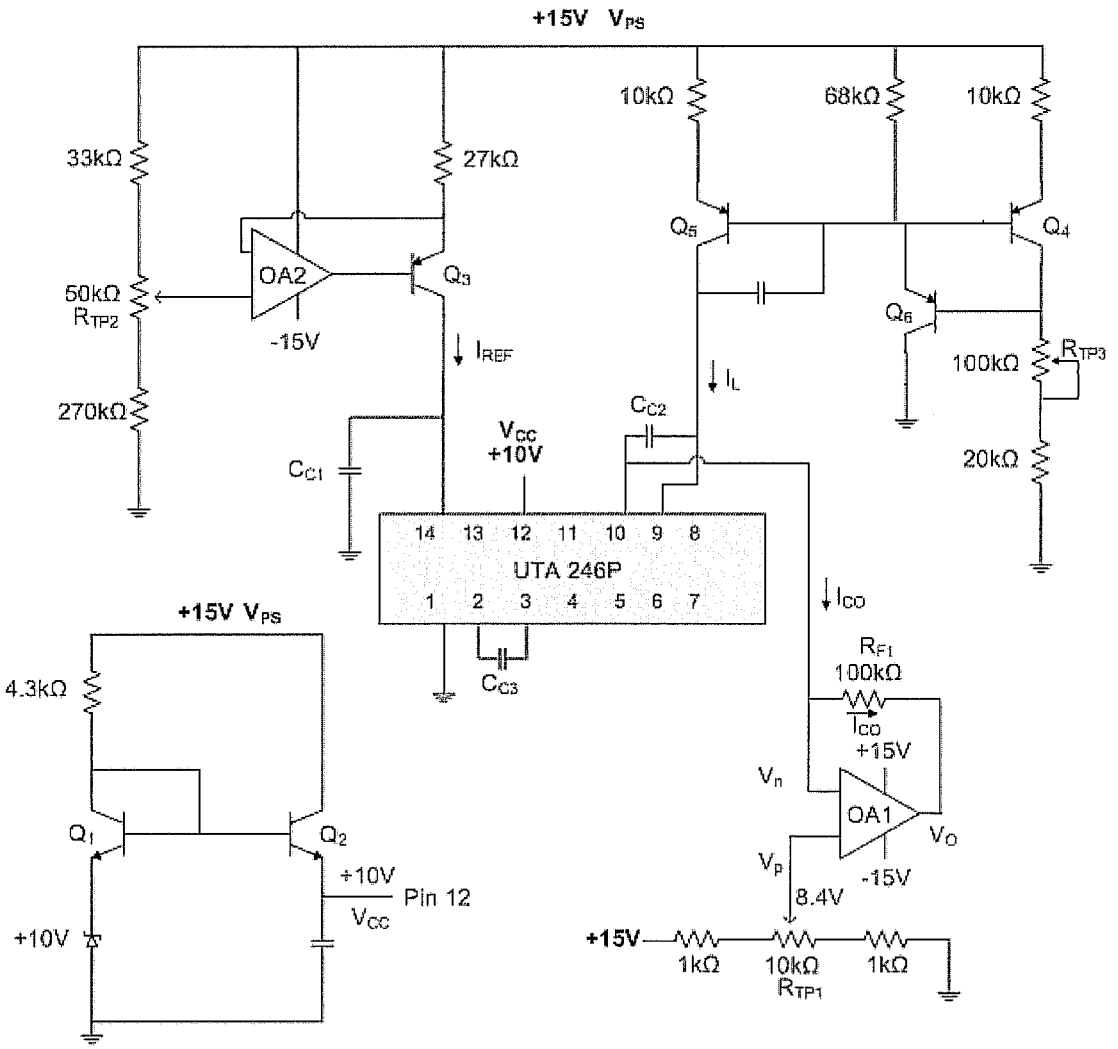


Figure 4.5 Completed testbench

4.1.3 Measurement Results

Using the testbench in Figure 4.5, the input reference current (I_{REF}), the collector output current (I_{CO}), the load current (I_L) and the calculation precision coefficient (n_2) are listed in Table 4.1 (See Appendix B). The precision output current, n_2, is calculated by Equation (3.11). And the plot is show in Figure 4.6.

Table 4.1 Precision output current

R_{L9}	I_{ref}(μA)	I_L(μA)	I_{cout}(μA)	n_2(μA)
17.931KΩ	93.68091	46.06447	86.57796	92.41793
24.250KΩ	93.68270	34.05872	86.59352	92.43278
33.104KΩ	93.68158	24.95143	86.60308	92.44408
55.443KΩ	93.68158	14.89919	86.61531	92.45714
67.711KΩ	93.68091	12.19902	86.61575	92.45827
177.99KΩ	93.68247	4.64019	86.62376	92.46528

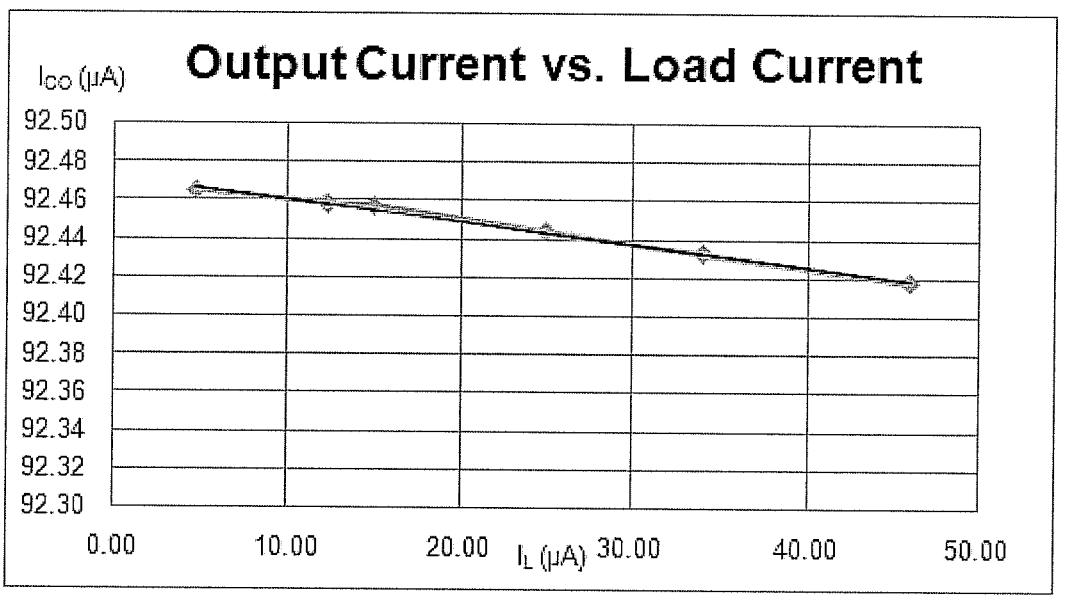


Figure 4.6 Precision output current verses load current

$$n_1 = -1266.7\mu\, A/A$$

$$n_2 = 0.92465\, A/A$$

The sensitivity in actual measurement is not as good as simulation result because the testing equipment are not precise enough and the noise interruption. However, the precision output current n_2 is still a considerate result.

CHAPTER 5

CONCLUSION AND FUTURE WORK

The proposed current mirror using National's VIP10 process is presented in this thesis. It uses Thomson's circuit presented in *Current Reference for Feedback Current Source* as a prior art. This thesis achieves the goal of precision and low sensitivity of I_{CO}. Equation (2.1) shows the current gain is less than unity under offset current and (3.7) the proposed circuit eliminates the offset current. The simulation performance of the proposed mirror is compared to other mirror circuits and indicates that the proposed design has the least sensitivity (n_1) to I_L and a reasonably good precision to I_{REF} (n_2). Several desirable features have been applied are listed below:

1. Q_2 functions as a beta helper. The emitter current compensates for the loss of base current of transistor Q_1, Q_3, and Q_8,

2. Q_4 is combined with the buffered Widlar current mirror at the collector of Q_3 so that the base error signal, can detect the difference between output current and input reference current, is developed at comparison node,

3. a single capacitor is added between comparison node and base of Q_5 for frequency compensation, and

4. active load is included in the feedback amplifier to improve the feedback to achieve a large loop gain.

Although actual measurements were affected by external noise, the initial characteristic of the proposed current mirror chip indicates the values of n_1 and n_2 are within range of simulation

results. Thus, the measure and analysis results are still in good compliance with each other. Future research involves the study of improving current gain and low power dissipation.

APPENDIX A

ON THE MATHEMATICAL FORMALISM OF THE CURRENT REFERENCE FOR FEEDBACK CURRENT SOURCE

A1. Calculation of the Current Reference for Feedback Current Source

$$I_{REF} = I_{C1} + I_{B1} + I_{B2} \tag{A1.1}$$

$$I_{C3} = I_{B4} + I_{C2} \tag{A1.2}$$

$$I_{Rbias} = I_{C4} + I_{B5} \tag{A1.3}$$

$$I_{C5} = I_{B3} + I_{B6} + I_{C6} + (m+1)I_{BO} \tag{A1.4}$$

Now, for simplicity, two assumptions are made in this calculation:

1. the β_n of all NPN transistors are identical, and
2. the β_p of all PNP transistors are identical.

Since $I_{B1} = I_{B2}$, then (2.1) can be written as

$$I_{REF} = I_{C2}\left(1+\frac{2}{\beta_n}\right)$$
$$I_{C2} = \frac{I_{REF}}{\left(1+\frac{2}{\beta_n}\right)} \tag{A1.5}$$

and substituting into (1.2)

$$I_{C3} = \frac{I_{C4}}{\beta_n} + \frac{I_{REF}}{1+\frac{2}{\beta_n}}$$
$$I_{C4} = \beta_n\left(I_{C3} - \frac{I_{REF}}{1+\frac{2}{\beta_n}}\right) \tag{A1.6}$$

Inserting (A1.6) into (A1.3) yields

$$I_{Rbias} = \beta_n\left(I_{C3} - \frac{I_{REF}}{1+\frac{2}{\beta_n}}\right) + I_{B5} \tag{A1.7}$$

Simplifying (B1.4) where $I_{B3} = I_{B6} = I_{BO}$, and gives

$$I_{C5} = I_{C6} + (m+3)I_{BO} = I_{C6} + \frac{(m+3)I_{CO}}{\beta_p} = \left[\frac{(m+3)}{\beta_p} + 1\right] I_{C0} \tag{A1.8}$$

Inserting (A1.7) into (A1.8) to get output current relates to input reference current

$$I_{CO} = \frac{I_{REF}}{\left(1+\frac{2}{\beta_n}\right)\left(\beta_n + \frac{1}{\beta_n} + \frac{m+3}{\beta_n \beta_p}\right)} + \frac{I_{RBias}}{\beta_n + \frac{1}{\beta_n} + \frac{m+3}{\beta_n \beta_p}} \tag{A1.9}$$

Through the analysis here, (A1.9) not only includes term of I_{REF} but also I_{RBias} which is offset term.

APPENDIX B

ON THE MATHEMATICAL FORMALISM OF THE PROPOSED TOPOLOGY

B1. Calculation of the Proposed Topology

Figure A1.1 is the original schematic of the proposed topology from the cadence.

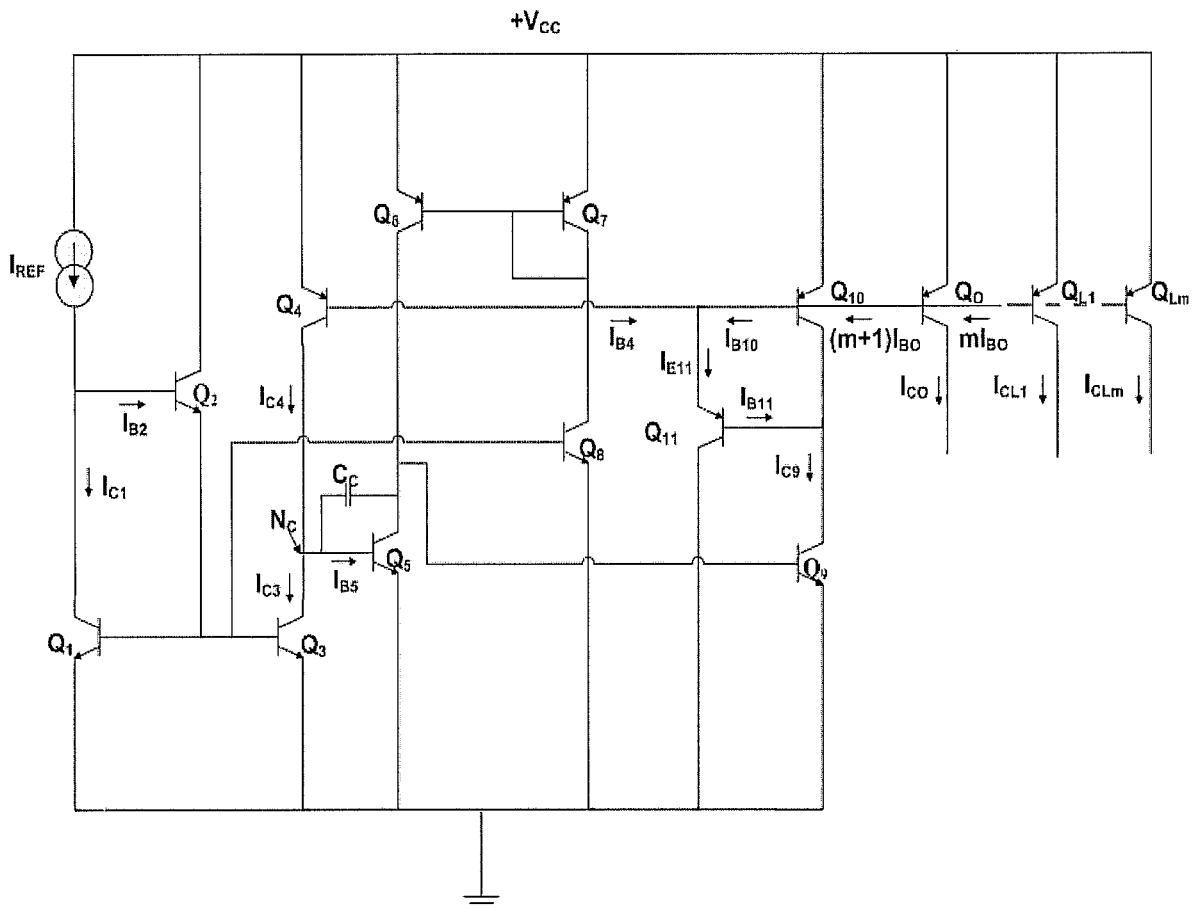


Figure B1.1 Schematic of UTA246P

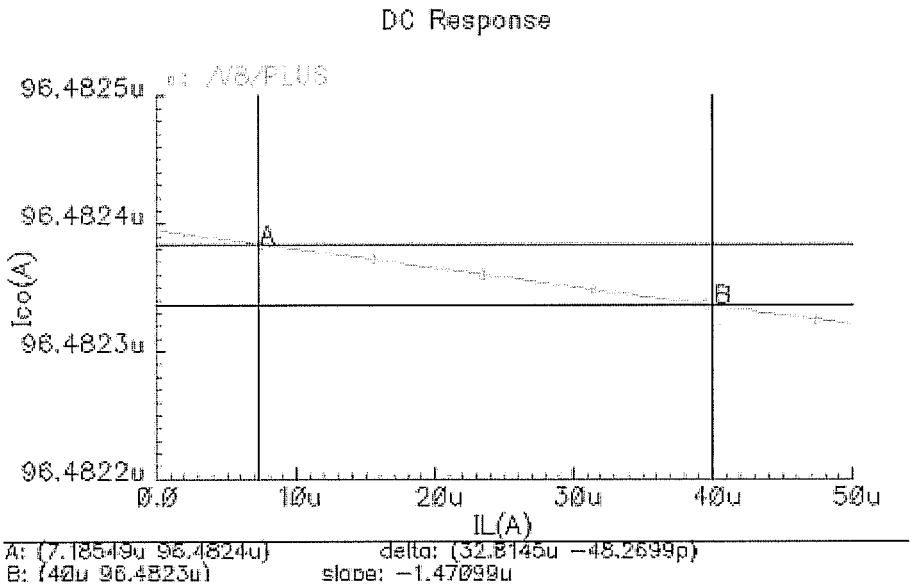


Figure B1.2 Simulation result

B2. Calculation of the Proposed Topology

The current mirror topology, shown in Figure A1, contains seven equations defined in Chapter Three, shown below:

$$I_{REF} = I_{B2} + I_{C1} \tag{B2.1}$$

$$I_{E2} = I_{B1} + I_{B3} + I_{B8} \tag{B2.2}$$

$$I_{C3} = I_{C4} - I_{B5} \tag{B2.3}$$

$$I_{C5} = I_{C6} - I_{C9} \tag{B2.4}$$

$$I_{C9} = I_{B11} + I_{C10} \tag{B2.5}$$

$$I_{E11} = I_{B4} + I_{B10} + (m+1)I_{BO} \tag{B2.6}$$

$$I_{C8} = I_{B6} + I_{B7} + I_{C7} \tag{B2.7}$$

For simplicity, two assumptions are made in this calculation:

1. all β's of NPN transistors are identical, and
2. all β's of PNP transistors are identical.

Since $I_{B4} = I_{B10} = I_{BO}$, then (B2.6) can be written as

$$I_{E11} = (m+3)I_{BO} = \frac{m+3}{\beta_p} I_{CO} \tag{B2.8}$$

substituting for I_{B11} in (B2.5) provides

$$\begin{aligned} I_{C9} &= \frac{I_{E11}}{\beta_P + 1} + I_{C10} \\ I_{C9} &= \left[\frac{m+3}{\beta_P(\beta_P + 1)} + 1 \right] I_{CO} \end{aligned} \tag{B2.9}$$

(B2.4) can be written as

$$\begin{aligned} I_{C5} &= I_{C6} - \frac{I_{C9}}{\beta_n} \\ I_{C5} &= I_{C6} - \left[\frac{m+3}{\beta_n \beta_p (\beta_p + 1)} + \frac{1}{\beta_n} \right] I_{CO} \end{aligned} \tag{B2.10}$$

Rearranging (B2.7) gives

$$I_{C8} = 2I_{B7} + I_{C7} = \frac{2I_{C7}}{\beta_p} + I_{C7} = \left(\frac{2}{\beta_p} + 1 \right) I_{C7} \tag{B2.11}$$

$$I_{C7} = \frac{I_{C8}}{\frac{2}{\beta_P} + 1} \tag{B2.12}$$

since $I_{C7} = I_{C6}$, thus

$$I_{C6} = \frac{I_{C8}}{\frac{2}{\beta_p} + 1} \tag{B2.13}$$

Inserting (B2.10) and (B2.13) into (B2.3) gives

$$I_{C3} = I_{C4} - \frac{I_{C6}}{\beta_n} + \left[\frac{1}{\beta_n^2} + \frac{m+3}{\beta_n^2 \beta_p (\beta_p + 1)}\right] I_{CO} = \left[1 + \frac{1}{\beta_n^2} + \frac{m+3}{\beta_n^2 \beta_p (\beta_p + 1)}\right] I_{CO} - \frac{I_{C6}}{\beta_n}$$

$$= \left[1 + \frac{1}{\beta_n^2} + \frac{m+3}{\beta_n^2 \beta_p (\beta_p + 1)}\right] I_{CO} - \frac{I_{C8}}{\frac{2}{\beta_p} + 1}$$

(B2.14)

since $I_{C3} = I_{C8}$, then this expression can be rewritten as

$$\left[1 + \frac{1}{\beta_n \left(\frac{2}{\beta_p} + 1\right)}\right] I_{C3} = \left[1 + \frac{1}{\beta_n^2} + \frac{m+3}{\beta_n^2 \beta_p (\beta_p + 1)}\right] I_{CO}$$

$$I_{C3} = \frac{\left[1 + \frac{1}{\beta_n^2} + \frac{m+3}{\beta_n^2 \beta_p (\beta_p + 1)}\right]}{\left[1 + \frac{1}{\beta_n \left(\frac{2}{\beta_p} + 1\right)}\right]} I_{CO} \qquad \text{(B2.15)}$$

Finally, the relationship between the input reference current I_{REF} and the collector current I_{CO} of the output transistor is from the combination of (B2.2) and (B2.15), and then inserted into (B2.1),

$$I_{CO} = \frac{\left[1 + \frac{1}{\beta_n \left(\frac{2}{\beta_p} + 1\right)}\right]}{\left[1 + \frac{3}{\beta_n (\beta_n + 1)}\right]\left[1 + \frac{1}{\beta_n^2} + \frac{m+3}{\beta_n^2 \beta_p (\beta_p + 1)}\right]} I_{REF} \qquad \text{(B2.16)}$$

(B2.16) obviously shows that the current gain nearly approaches to unity because $\beta >> 1$.

APPENDIX C

ALL DATA FROM MEASUREMENT

Using Op-Amp TLC274 To Test I_{cout}

Set V_{CC} = 10V, V_{CO} = 8.003V, R_{REF} = 89.725kΩ, R_{CO} = 89.958kΩ

a. R_L = 17.931kΩ

	V_{ref}	I_{ref}(μA)	V_L	I_L(μA)	V_{cout10}	I_{cout}(μA)
1	8.40510	93.6762329	0.82609	46.0704924	7.78800	86.57373
2	8.40530	93.6784620	0.82601	46.0660309	7.78850	86.57929
3	8.40560	93.6818055	0.82596	46.0632424	7.78830	86.57707
4	8.40580	93.6840346	0.82593	46.0615693	7.78850	86.57929
5	8.40580	93.6840346	0.82592	46.0610117	7.78860	86.58040
Average	**8.40552**	**93.6809139**	**0.825982**	**46.0644694**	**7.78838**	86.5779586

b. R_L = 24.250kΩ

	V_{ref}	I_{ref}(μA)	V_L	I_L(μA)	V_{cout10}	I_{cout}(μA)
1	8.40550	93.6806910	0.82599	34.0614433	7.78950	86.59041
2	8.40570	93.6829200	0.82596	34.0602062	7.78990	86.59486
3	8.40560	93.6818055	0.82592	34.0585567	7.78970	86.59263
4	8.40580	93.6840346	0.82588	34.0569072	7.79000	86.59597
5	8.40580	93.6840346	0.82587	34.0564948	7.78980	86.59374
Average	**8.40568**	**93.6826971**	**0.825924**	**34.0587216**	**7.78978**	86.59352142

c. R_L = 33.104kΩ

	V_{ref}	I_{ref}(μA)	V_L	I_L(μA)	V_{cout10}	I_{cout}(μA)
1	8.40540	93.6795765	0.82608	24.9540841	7.79050	86.60153
2	8.40540	93.6795765	0.82601	24.9519696	7.79060	86.60264
3	8.40560	93.6818055	0.82599	24.9513654	7.79070	86.60375
4	8.40570	93.6829200	0.82595	24.9501571	7.79060	86.60264
5	8.40580	93.6840346	0.82593	24.9495529	7.79080	86.60486
Average	**8.40558**	**93.6815826**	**0.825992**	**24.9514258**	**7.79064**	86.60308144

d. R_L = 55.443kΩ

	V_{ref}	I_{ref}(μA)	V_L	I_L(μA)	V_{cout10}	I_{cout}(μA)
1	8.40510	93.6762329	0.82615	14.9008892	7.79130	86.61042
2	8.40540	93.6795765	0.82609	14.8998070	7.79160	86.61375
3	8.40570	93.6829200	0.82605	14.8990855	7.79180	86.61598
4	8.40580	93.6840346	0.82599	14.8980034	7.79190	86.61709
5	8.40590	93.6851491	0.82600	14.8981837	7.79210	86.61931
Average	**8.40558**	**93.6815826**	**0.826056**	**14.8991938**	**7.79174**	86.61530937

e. R_L = 67.711kΩ

	V_{ref}	I_{ref}(μA)	V_L	I_L(μA)	V_{cout10}	I_{cout}(μA)
1	8.40520	93.6773475	0.82602	12.1991995	7.79140	86.61153
2	8.40540	93.6795765	0.82607	12.1999380	7.79150	86.61264
3	8.40560	93.6818055	0.82600	12.1989042	7.79190	86.61709
4	8.40570	93.6829200	0.82598	12.1986088	7.79200	86.61820
5	8.40570	93.6829200	0.82597	12.1984611	7.79210	86.61931
Average	**8.405520**	**93.6809139**	**0.826008**	**12.1990223**	**7.79178**	86.61575402

f. R_L = 177.99kΩ

	V_{ref}	I_{ref}(μA)	V_L	I_L(μA)	V_{cout10}	I_{cout}(μA)
1	8.40540	93.6795765	0.82598	4.6405978	7.79210	86.61931
2	8.40560	93.6818055	0.82591	4.6402045	7.79240	86.62265
3	8.40570	93.6829200	0.82588	4.6400360	7.79270	86.62598
4	8.40580	93.6840346	0.82588	4.6400360	7.79260	86.62487
5	8.40580	93.6840346	0.82589	4.6400921	7.79270	86.62598
Average	**8.405660**	**93.6824742**	**0.825908**	**4.6401933**	**7.79250**	86.62375775

Summarize the average data from a through f

R_{L9}	I_{ref}(μA)	I_L(μA)	I_{cout}(μA)	n_2(μA)
17.931KΩ	93.68091	46.06447	86.57796	92.41793
24.250KΩ	93.68270	34.05872	86.59352	92.43278
33.104KΩ	93.68158	24.95143	86.60308	92.44408
55.443KΩ	93.68158	14.89919	86.61531	92.45714
67.711KΩ	93.68091	12.19902	86.61575	92.45827
177.99KΩ	93.68247	4.64019	86.62376	92.46528

REFERENCES

1. P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits, Fourth Edition*, John Wiley & Sons, Inc., New York, NY, 2001.

2. Howard T. Russell, Jr., Ronald L. Carter, W. Alan Davis; "*A Wide-Band All-NPN Current Mirror for Precision Biasing of Multiple Circuits*", *Invited Paper*, accepted for publication in the Proceedings of the 9th International Conference on Solid-State and Integrated Circuit Technology, October 20-23, 2008, Beijing.

3. R.G. Thompson, "*Current reference for feedback current source*," U.S. Patent 4,739,246, April 19, 1988.

4. A. S. Sedra and K. C. Smith, *Microelectronic Circuits, 4th Edition*, Oxford University Press, Inc., New York, 1998.

5. P. Horowitz and W. Hill, *The Art of Electronics, 2nd Edition*, Cambridge University Press, Inc., New York, 1989.

6. S. Franco, Design *with Operational Amplifiers and Analog Integrated Circuits, 2nd Edition*, The McGraw-Hill Companies, Inc., New York, NY, 1998.

7. http://en.wikibooks.org/wiki/Analogue_Electronics/Current_Mirrors/Wilson

BIOGRAPHICAL INFORMATION

Mei-Ping Pua was born in Yong Peng, Malaysia. She received her Associate degree of Science from Collin County Community College and Bachelor's degree in Electrical Engineering from University of Texas at Arlington in 2003 and 2005, respectively. In addition, she received her Master of Science in Electrical Engineering from The University of Texas at Arlington in 2008. Her current research interests focus on design of precision biasing current mirror circuit.