THE THERMAL EFFECTS OF SELF HEATING OF TRANSISTORS ON ANALOG AMPLIFIER DESIGN AND EVALUATION

by

KAMAL RANJAN SINHA

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DEDICATED TO MY WIFE AND DAUGHTER

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ABSTRACT

THE THERMAL EFFECTS OF SELF HEATING OF TRANSISTORS ON ANALOG AMPLIFIER DESIGN AND EVALUATION

Kamal Ranjan Sinha, PhD.

The University of Texas at Arlington, 2008

Supervising Professor: Ronald L. Carter

Electrothermal effects play a major role in the performance of modern silicon-on-insulator (SOI) bipolar junction transistors (BJTs). This research work examines the influence of electrothermal feedback within a single device and within a circuit composed of such devices. Specifically, the frequency-domain thermal effects of self-heating in SOI BJTs on the performance of analog integrated circuits, with emphasis on current mirrors, and current-feedback operational amplifiers (CFOA), are investigated through analytical formulation, simulation, and measurement.

For the extensive analysis and characterization of self-heating thermal effects, the Vertical Bipolar Inter-Company (VBIC) models for SOI BJTs are developed from fundamental physical device considerations. Extensive simulations have been done to

validate the models using the SPECTRE simulator. Analytical formulations for the output impedance of the current mirrors, designed using SOI BJTs, are developed incorporating the effect of dynamic self-heating. This shows that a thermally induced "zero-pole doublet" in the transfer function of the output impedance can show a peaking effect in the frequency response. Such thermal effects have been demonstrated through frequency-domain measurements, using a precision impedance analyzer (Agilent 4294A) and an impedance probe (Agilent 42941A), on the test structures of current mirrors, fabricated using the VIP10^{TM} bipolar process technology. Self-heating tolerant current mirror topologies are identified and verified experimentally.

Self-heating influenced parameters of the conventional CFOA are identified through both analytical formulations and simulations. The analysis shows that the frequency response of the open-loop transimpedance, common-mode rejection ratio (CMRR), and power supply rejection ratio (PSRR) of the CFOA can be influenced by the dynamic self-heating. The techniques to design self-heating tolerant CFOAs are proposed, and their performances are demonstrated through simulation. Two new optimized topologies of CFOAs are designed and fabricated using the VIP10^{TM} bipolar process technology as test chips, and frequency-domain and time-domain thermal effects are verified through extensive measurement. The verification of the thermal tail and the thermally induced longer settling time in the step response of the CFOA, in the non-inverting unity gain configuration, is accomplished through a time-domain measurement using an Agilent Infiniium DSO81204B digital oscilloscope, along with an 1169A InfiniiMax II series probe amplifier.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1

INTRODUCTION

The operating temperature plays a significant role in the performance of modern bipolar junction transistors (BJTs) [1]. The adoption of advanced isolation techniques such as silicon-on-insulator (SOI) substrate and deep trench oxide isolation (DTI) in modern bipolar technologies to meet the demand for higher speed has degraded the heat spreading across a chip. The poor thermal conductivity of silicon dioxide, 0.014 W(cm-K)$^{-1}$ [2], influences self-heating and mutual thermal coupling [3]. The localized heating under the active area of a device due to the trapped heat is called self-heating and characterized by thermal spreading impedance, Z_{th}, which is a frequency dependent parameter. This is strongly dependent on the device structure and materials being used for isolation [3]-[5]. It is reported [5] that the effect of self-heating is more prominent with bipolar transistors with reduced geometries. As a consequence of self-heating, the operating temperature of a device increases beyond the ambient temperature of non-isolated transistors.

In the context of integrated circuits, the temperature of each transistor will be defined by the power dissipation of the respective transistor, and thermal coupling among nearby transistors. This causes a non-isothermal scenario among the constituent transistors leading to a temperature gradient. This affects the performance of the most

important analog circuit building blocks like current mirrors, basing circuits, bandgap reference circuits, voltage regulator circuits, operational amplifiers, and trans-linear circuits [5]-[6]. The continuous downscaling trend of device features further aggravates the thermal effects due to the increase in thermal resistance and power densities. Because of the increase in the power density of a chip, the other category of the thermal effect called “inter-device thermal coupling” comes into picture as well.

. Thermal effects have always been a concern for analog circuits, which are dealt with high power dissipation [5], but even low power analog circuits, designed using SOI BJTs, are not an exception. Analog circuit performance may be degraded severely by self-heating due to the change in both the small-signal and large-signal parameters [5]. Both current mirror and biasing circuits are examples of analog circuits, which get impacted severely by such effects.

The study of the thermal effects of self-heating on fundamental blocks of analog circuits - current mirrors, amplifier circuits, and trans-linear circuits - have been done extensively through analytical formulations, simulations and measurement in this research work. Several analytical models have been developed to characterize the effect static and dynamic self-heating. Various current mirrors and Current Feedback Operational Amplifiers (CFOAs) are fabricated, and DC, frequency-domain, and time-domain measurements are carried out to characterize the thermal effects of self-heating. Finally, design techniques have been identified that can be used to design self-heating tolerant current feedback amplifier circuits.

1.1 Effect of Temperature on the Bipolar Junction Transistor

1.1.1 Effect of Temperature on the Collector Current

Both the large-signal and small signal performance of BJTs are strongly dependent on temperature due to a very strong temperature dependence of the saturation current and base-emitter voltage of the transistor. The circuit symbol for an *npn* transistor with terminal currents and voltages is shown in Fig. 1.1.

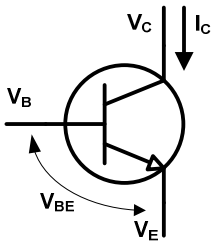


Figure 1.1 Circuit Symbol for the *npn* bipolar junction transistor.

An approximate expression for collector current, I_C, in the forward-active region can be expressed as [7],

$$I_C = IS(T)\cdot\left(1+\frac{V_{CE}}{V_A}\right)\cdot\exp\left(\frac{V_{BE}}{V_T}\right) \tag{1.1}$$

where V_A is the Early voltage due to electrical effects only, V_{CE} is the collector-emitter voltage, V_{BE} is the base-emitter voltage, V_T is the thermal voltage, and IS is the saturation current, which can be expressed as [7]

$$IS(T) = \frac{q\cdot AE\cdot \tilde{D}_n(T)\cdot n_i^2(T)}{Q_B} \tag{1.2}$$

where q is the electron charge, AE is the base-emitter junction area, and $Q_B = N_B W_B$ is the total base doping per unit area. The variables, N_B and W_B represent the base impurity

concentration and base charge neutral width, respectively. The temperature dependence of diffusion constant of electrons, $D_n(T)$, can be expressed as [8]-[9]

$$\tilde{D}_n(T) = V_T \tilde{\mu}_n(T) = \frac{C \cdot kT^{-m+1}}{q} \tag{1.3}$$

where $\tilde{\mu}_n(T)$ is the base-region electron mobility, defined as $\tilde{\mu}_n(T) = CT^{-m}$. The exponent, m, depends on the doping level in the base, but is approximately - 1.0 [5]. The temperature dependent expression of the intrinsic carrier concentration, $n_i(T)$, can be expressed as [2], [8]

$$n_i^2(T) = N_C(T) N_V(T) \cdot exp\left(-\frac{V_G(T)}{V_T}\right) \tag{1.4}$$

where $N_C(T)$, $N_V(T)$, and $V_G(T)$ are the temperature dependent conduction band effective density of states, valence band effective density of states, and bandgap volatge respectively. The substitution of (1.2) - (1.4) into (1.1) yields

$$I_C(T) = \frac{C_t}{Q_B} \cdot T^{4-m} \exp\left(-\frac{V_{G0}}{V_T}\right) \exp\left(\frac{V_{BE}(T)}{V_T}\right)\left(1 + \frac{V_{CE}}{V_A}\right) \tag{1.5}$$

where C_t is the temperature-independent parameter. The expression (1.5) can be simplified as

$$I_C(T) = C_t \cdot T_{op}^{(4-m)} \exp\left(\frac{q(V_{BE} - V_{G0}(N_B))}{KT_{op}}\right) \cdot \left(1 + \frac{V_{CE}}{V_A}\right) \tag{1.6}$$

where T_{op} is the device operating temperature, V_{G0} is the band-gap voltage of silicon extrapolated to 0 K [7]. This shows that I_C depends on $T^{(4-m)} \sim T^3$. Thus, the collector current responds to temperature very quickly and hence to the self-heating, which

essentially increases the device temperature through power dissipation. This can also be verified through the simulation of the output characteristics of the *npn* transistor in the common-emitter (*CE*) configuration with temperature as a sweep parameter in Fig 1.2.

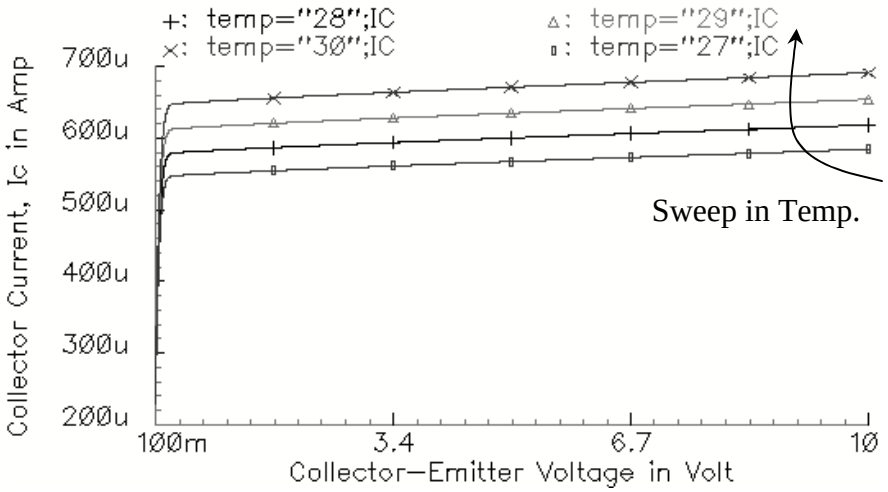


Figure 1.2 Effect of temperature on the output characteristics of the *npn* transistor.

1.1.2 Effect of Temperature on the Base-Emitter Voltage

The base-emitter voltage temperature feedback coefficient at a fixed collector current of the *npn* transistors can be defined as [9]

$$\varphi = \left.\frac{\partial V_{BE}}{\partial T}\right|_{I_C} \tag{1.7}$$

The expression (1.7) can be evaluated using (1.6) as

$$\varphi(I_C,T) = \left.\frac{\partial V_{BE}}{\partial T}\right|_{I_C} = \frac{k}{q}(4-m) - \frac{k}{q}\cdot\ln\left[\frac{I_C}{C_t\cdot(1+{}^{V_{CE}}\!/_{V_A})\cdot T^{4-m}}\right] \tag{1.8}$$

where k is Boltzmann's constant, q is the electronic charge, and m is the mobility power factor for $\mu = \mu_0\left({}^{T}\!/_{T_0}\right)^{-m}$. The logarithmic relationship makes φ a weak function of

temperature and current. The temperature independent formulation can be approximated from (1.8) to be [9]

$$\varphi(I_C,T_0)=\left.\frac{\partial V_{BE}}{\partial T}\right|_{I_C}=\frac{k}{q}(4-m)-\frac{k}{q}\cdot\ln\left[\frac{I_C}{C_t\cdot(1+{}^{V_{CE}}\!/_{V_A})\cdot T_0^{4-m}}\right] \tag{1.9}$$

where T_0 (different from the device operating temperature for an SOI transistor with self-heating) is the ambient temperature. The base-emitter temperature coefficient for a typical *npn* transistor can be approximated as – 2.0 mV/°C [7]. The SPECTRE simulation (with a physics based VBIC models provided in Tables 2.9 and 2.10) shown in Fig. 1.3 shows that the base-emitter temperature coefficients for the *npn* and *pnp* transistors are ~ -1.5 mV/°C , and -1.38 mV/°C respectively at 27 °C.

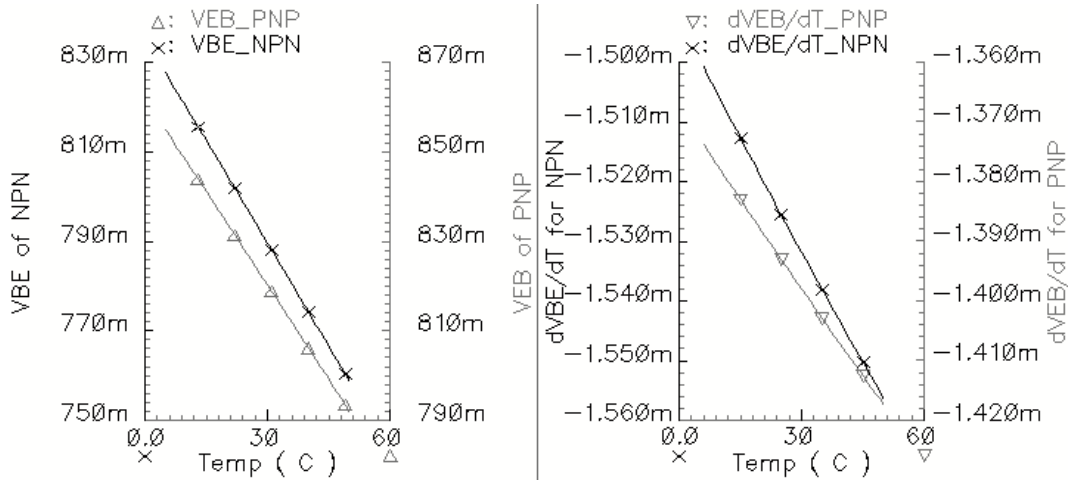


Figure 1.3 Typical response of V_{BE} versus temperature for the *npn* and *pnp* transistors with an emitter area of 40 μm^2.

1.1.3 Characterization of Temperature Dependency

As explained in section 1.1.1, temperature is a critical factor which can influence the large-signal output characteristics of bipolar transistors. The variation of the collector and base current with temperature can be defined as the fractional change

in the collector and base current per degree centigrade of temperature variation. This is called the fractional temperature coefficient, TC_{FX}, and can be expressed as [7]

$$TC_F(I_X) = \frac{1}{I_X} \cdot \frac{\partial I_X}{\partial T} \tag{1.10}$$

This parameter is usually preferred in the characterization of the performance of biasing circuits and bandgap reference circuits. The analytical formulations for the collector and base temperature fractional coefficient can be expressed as [10]

$$TC_F(I_C) = \frac{1}{T}\left(XTI - \frac{V_{BE}}{NF \cdot V_T} + \frac{V_G}{V_T} \right)\left[1 - 2 \cdot \frac{I_C}{IKF} \cdot K_{q1} NK \cdot \left(1 + 4. \frac{I_{be}}{IKF} \right)^{(NK-1)} \right] \tag{1.11}$$

$$TC_F(I_B) = \left[\frac{1}{T \cdot \beta_F I_B} \left(I_{be}(XTI - XTB) + \frac{V_G - \frac{V_{BE}}{V_T}}{V_T} \right) + \frac{\beta_F I_{ben}}{NE} \left(XTI - NE \cdot XTB + \frac{V_G - V_{BE}}{V_T} \right) \right] \tag{1.12}$$

These expressions are applicable in the forward-active region and details of the parameters are provided in chapter 2 and [10].

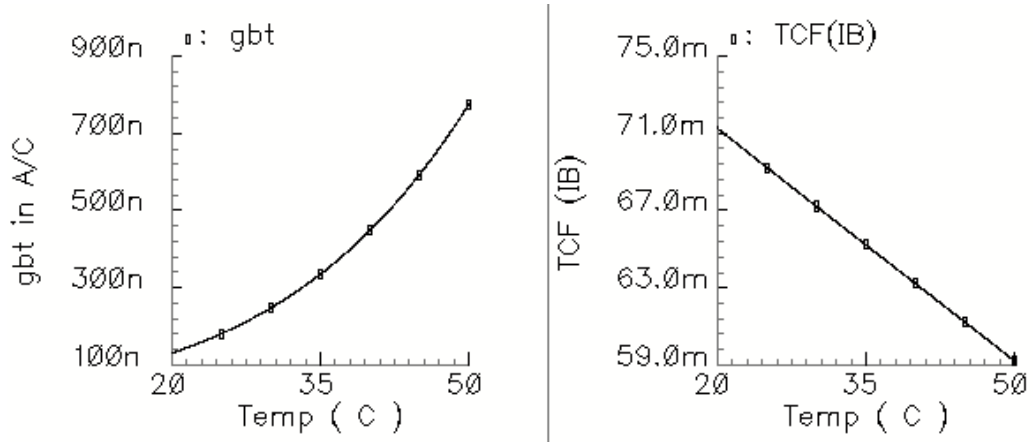
For the small-signal analysis, the change in current with a change in temperature is the parameter of interest. Hence, the change in the collector and base current with a change in the ambient temperature under a constant bias is known as the collector, and base thermal transconductance, respectively, and can be expressed as [11]-[13]

$$g_{ct} = \frac{\partial I_C}{\partial T} \tag{1.13}$$

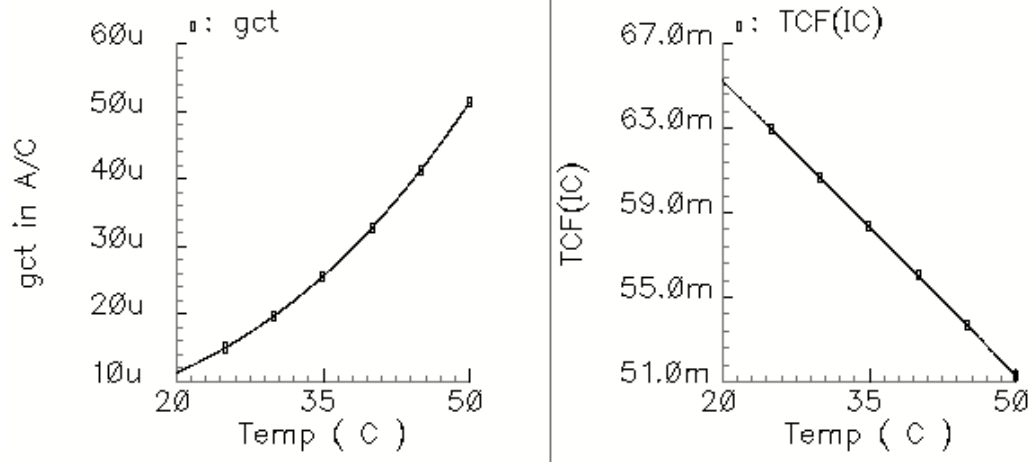
$$g_{bt} = \frac{\partial I_B}{\partial T} \tag{1.14}$$

These parameters will be used extensively in the analysis of thermal effects of dynamic

self-heating in chapters 3 and 4. The simulation using the SPECTRE simulator for thermal transconductance and fractional temperature coefficients for the base and collector currents for the *npn* transistor using the VBIC model [14] is shown in Fig. 1.4.



(a)



(b)

Figure 1.4 The thermal transconductance and fractional temperature coefficient of (a) the base current (b) the collector current versus temperature for an 8x *npn* transistor (8 times the emitter area of a 1x (5 μm^2) device) at V_{BE} = 0.76 V.

From the simulations in Fig. 1.4, it is seen that the thermal transconductance and fractional temperature coefficient of the base current for the *npn* transistor are 206.02 nA/°C, and 6.8%, respectively, and those for the collector current are 16.82 μA/°C and

6.19%, respectively at 27 °*C*, which is close to the value 7% for $TC_F(I_C)$, previously reported [6].

1.2 Thermal Feedback Mechanism in Integrated Circuits

It is well known that the component density in integrated circuits has been increasing to meet the demand of a higher speed of operation and reduced die size. This has increased a demand on the power density of the chip. However, there is a reliability constraint from on the maximum operating temperature that the chip can handle for a certain percentage of risk tolerance. For silicon devices, the junction temperature is limited to 75-85°C [16] for safe operation. With increasingly higher power density but limited operating temperature, the thermal resistance of the devices must be reduced to sustain the demand of high power density. There are three different kinds of thermal feedback mechanisms found in integrated circuits, based on thermal impedance characterization: 1) package thermal effects, 2) thermal coupling between two transistors, and 3) direct heating of a transistor by its own power.

1.2.1 Thermal Effects in Integrated-Circuit

The first mechanism of package thermal feedback in integrated circuits can be characterized through the package thermal impedance. The overall change in chip temperature can be expressed as [5]

$$\Delta T_{chip} = \Delta P_{chip} \cdot Z_{TH}(pkg) \tag{1.15}$$

where $Z_{TH}\ (pkg)$ is called the chip-to-package-to-ambient thermal impedance [5]. The change in temperature due to the change in overall chip power is a function of time with a large package thermal time constant (the product of overall thermal resistance and

thermal capacitance). Hence, a change in temperature can not keep up with rapid changes in power due to the low-pass nature of the thermal impedance, which is strongly dependent on the types of package used and quality of the heat sink. This leads to the concept of “thermally significant power” and is considered as a key metric in the design of a cooling solution for complex integrated circuits. Thermal transients induced by the thermal effect of package thermal impedance can be triggered instantaneously after a power change and may extend upto 100s of mili-second [11].

The second thermal feedback mechanism prevailing among devices on the same die can be attributed to the coupling of power from one chip or device to another due to the existence of a high temperature gradient in proximity. This is called inter-device heating and can be characterized by a thermal coupling resistance [17]-[18]. The effect of thermal coupling can be mitigated by proper spacing between devices [18]. However, this is not an attractive technique from the die area constraint in integrated circuits.

The third thermal feedback mechanism, the primary focus of this research work, is the rise in the temperature of the emitter junction of a transistor through its own static power dissipation. This is called self-heating and can be characterized by the thermal impedance of the device itself [4]-[6], [11]-[13]. This effect can be represented by either a single pole *RC* network as an approximation or multiple pole *RC* network to enhance the modeling accuracy of thermal effects. In general, the thermal impedance is modeled with a single-pole low-pass filter [4], [11] without relaxing much accuracy.

The magnitude of thermal resistance, R_{th}, which depends on the bipolar process technology, plays a significant role in dictating the device characteristics under thermal

influence of self-heating. The self-heating has been identified as a concern in modern advanced complementary bipolar process technologies, most notably the Vertically Insulated PNP (VIP10^{TM}), developed by National Semiconductor, and the Complementary Extra Fast Complementary Bipolar Process (XFCB) developed by Analog Devices. The prevalent use of oxide isolation in place of junction isolation in modern bipolar process technologies traps heat under the active area of devices due to lower thermal conductivity of silicon dioxide, SiO_2, aggravating the thermal effects

1.2.2 Intrinsic Thermal Effects in the Bipolar Transistor

As explained in the previous section, self-heating – heating of a transistor through its own power dissipation – is one of the most important concerns for an SOI bipolar process technology. This is characterized by the thermal impedance and it scales up with the reduction in the size of the device. Apart from this effect, the adjacent devices can influence a neighboring device's temperature due to temperature gradient among devices. This is defined as inter-device heating and can be characterized by an inter-device or mutual thermal coupling coefficient. However, such an effect can be mitigated by proper layout and maintaining proper spacing between adjacent devices [17]-[18].

A simplistic cross section of the XFCB [1] process architecture is shown in Fig. 1.5. The fully dielectric isolation has been achieved through the use of trench isolation and bonded wafer technology to realize an SOI substrate. As shown in Fig. 1.5, the active area of the device appears to be surrounded by silicon dioxide, SiO_2, preventing the peripheral lateral heat flow, leading to the concept of "Self-heating".

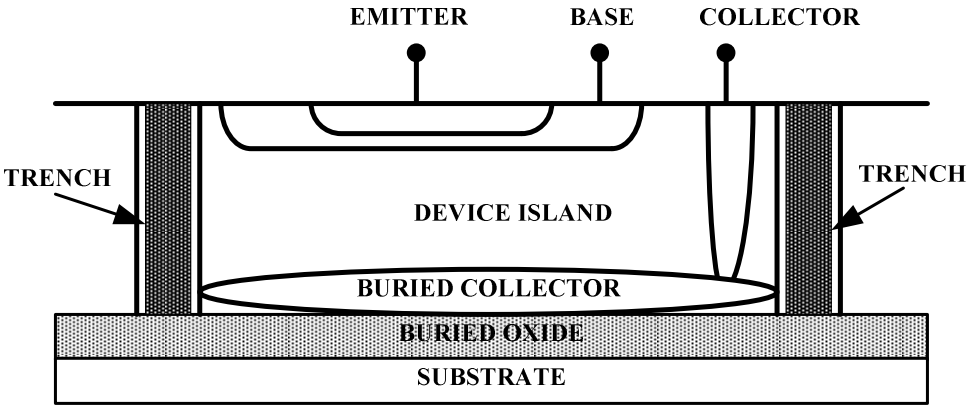


Figure 1.5 Cross section of the bipolar transistor in XFCB process [1].

However, such a structure offers low parasitic capacitance extending the frequency capability of the device.

1.2.3 Modeling Self-Heating through an Electro-Thermal Model

Self-heating can be categorized into static and dynamic thermal effects [4], [19]. Under dc bias, static self-heating can be represented by an electro-thermally coupled model [13] as shown in Fig. 1.6.

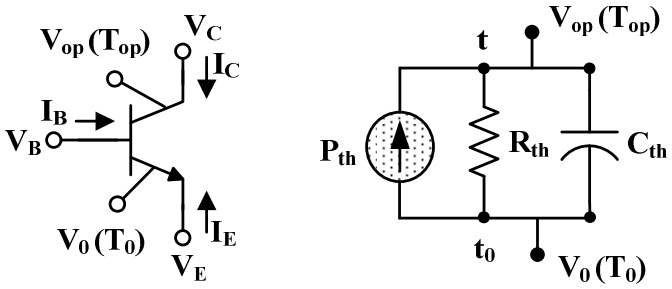


Figure 1.6 Electro-thermal model for an SOI bipolar junction transistor. Thermal network is modeled with a single-pole *RC* network as in the VBIC model [20].

The temperature rise ΔT [K] (treated as $(V_{op} - V_0)$ in electrical equivalent circuit) of a device due to the static self-heating is given by the product of the power dissipated, P_{th} [W/1V] and the thermal resistance, R_{th} [K/W] as

$$\Delta T = P_{th} \cdot R_{th} \tag{1.16}$$

The voltage level of the node "t" of Fig. 1.6 is equal to the rise in the local temperature of the device based on the VBIC model formulation [17]. Thus, the voltage rise in the electrical network is equivalent to the temperature rise in the thermal network. The consideration of this equivalency is advised while interpreting the electro-thermal network in this dissertation.

Assuming $I_B(V_B, T_{op})$ and $I_C(V_B, V_C, T_{op})$ are large-signal currents in Fig. 1.6, the device operating temperature, T_{op}, can be expressed in terms of the static power defined as $P_{th} = I_B V_{BE} + I_C V_{CE}$, ambient temperature T_0, and thermal resistance, R_{th}, as

$$T_{op} = f\left(I_B, V_B, I_C, V_C, T_0, R_{th}\right) = T_0 + P_{th} \cdot R_{th} = T_0 + \left(I_B V_{BE} + I_C V_{CE}\right) \cdot R_{th} \tag{1.17}$$

The total thermal spreading impedance, Z_{th} (the response of emitter temperature to collector power variation), can be approximated with a single pole-function as [4]

$$Z_{th}(s) = \frac{R_{th}}{1 + sR_{th}C_{th}} \tag{1.18}$$

where R_{th}, and C_{th} are the thermal resistance and thermal capacitance expressed in K/Watt and Joules/K, respectively. The values of the thermal resistance and capacitance are strongly dependent on the device structure and size [10]. With single pole thermal network approximation, the thermal impedance, Z_{th}, represents a low-pass filter transfer function with the thermal cutoff frequency defined as $f_{th} = 1/2\pi R_{th} C_{th}$. The thermal effect is modeled through the electro-thermal interaction as shown in Fig. 1.6, in which the electrical network dissipated power is coupled to the thermal network which raises the device temperature and fedback to electrical network.

1.3 Why Self-heating is important to model

In the conventional junction isolated bipolar process technology, the heat under the active area of a device was able to spread out across the chip because of the higher thermal conductivity of silicon, 1.412 W/cm-K [2]. Hence, all devices on a die were assumed to be at an isothermal condition and hence the error in analysis was negligible despite the ignorance of self heating effects. However, this is not true for the SOI BJTs in which the fully dielectrically isolation techniques are used. The active area in an SOI BJT is essentially encapsulated within silicon dioxide (SiO_2) as shown in Fig. 1.5. This traps the heat within a transistor and hence creates a non-isothermal condition among the devices on the same die based on power level of each transistor. Self-heating has been shown to affect the analog circuit's performance through two mechanisms [11].

The first mechanism increases the collector current of the transistor, and can be significant even with a negligible amount of power dissipation. This mechanism primarily affects the small-signal reverse admittance, y_{12}, and output admittance, y_{22}, of the transistor in the common-emitter configuration. The values of y_{12} and y_{22} are shown to be largely affected by the dynamic self-heating [19]. This is the principal reason for the degradation of the frequency response of output impedance of current mirrors. Such distortions in the small-signal parameters can significantly affect the frequency response of high-gain amplifiers – both Voltage Feedback Operational Amplifiers (VFOA) and Current Feedback Operational Amplifiers (CFOA).

The current mirror is one of the most fundamental circuit configurations in analog circuit design, and is of interest here because it solely relies on the close

electrical matching of V_{BE} between two transistors under isothermal conditions for maintaining its mirroring characteristics. Nonetheless, the electrical matching of V_{BE} is perturbed because of the differences in temperature of transistors due to the differences in power level. As shown in Fig. 1.7, there will be a power level difference between Q_0 and Q_1 even at the same reference current and output current because of difference in the collector-emitter voltages of transistors, Q_0 and Q_1.

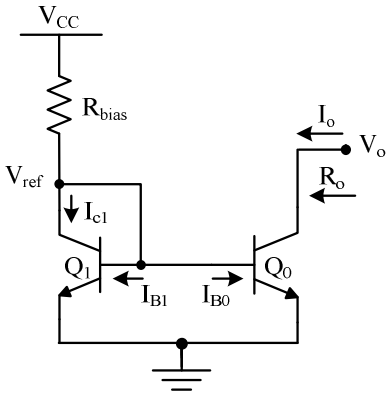


Figure 1.7 Simple bipolar current mirror.

Since the device temperature will be dictated by self-heating through (1.16), there will be mismatch in V_{BE} between Q_0 and Q_1, and hence there will be mismatch between the reference current, I_{ref}, and output current, I_o. The errors will further be aggravated by the higher mismatch between the output voltage of Q_0, V_o, and input reference voltage, V_{ref}, which causes a higher power mismatch. Moreover, Fox and Lee [5] predicted that local thermal effects can induce a variation in excess of 2 to 1 in the gain of a two stage op-amp. In addition, time dependent offset voltage can be seen due to self-heating in the CFOA as reported by [17]. Another typical circuit whose performance is degraded by thermal effects of self-heating is the self-biased V_{BE}-based

current generator [18]. It has been identified that techniques that enhance the output resistance of current mirrors – cascoding (cascade of a common-emitter and a common-base stage), and negative series-series feedback (the feedback offered by the resistor in the emitter of the common-emitter transistor) – can reduce the errors due to self-heating [6], [18].

The second mechanism is significant only when there is a large swing of power or large power dissipation in the circuits. This mechanism, apart from affecting the small-signal parameters of a transistor, is the main source of thermal errors in the large-signal transient response of translinear circuits [20], so-called because their operation depends on the linearity of the transconductance with the collector current. The exponential dependence of I_C on V_{BE} as illustrated by (1.1) holds true over many orders of magnitude ignoring the effect of self-heating. However, this characteristic may be impaired by self-heating. The class AB buffers [21] are the perfect example of a translinear circuit, whose performance depends on the close electrical matching of the base-emitter voltages of the constituent devices. Brodsky and Zweidinger showed [11] that the electrical transient can be completed very quickly based on circuits while the self-heating induced transient continues for fairly long time based on the thermal time constant (typically 5 μs) of the devices. This essentially extends the settling time, limiting the usage of buffer or amplifier in unity gain configuration for precision applications. Thermally induced errors are mostly restricted to precision circuits which depend on close matching of transistor's characteristics.

As explained earlier, the bipolar transistors fabricated using SOI technology exhibit greater sensitivity to thermal effects caused by excessive self-heating because of the ever increasing tendency to reduce device geometry and operate at higher current density. The resulting high junction temperature can have deleterious effects on the reliability of the transistors [3] and induce shifts in their I-V characteristics. This can not be ignored and hence the accurate modeling of the effect of self-heating is a must.

1.4 Architecture of Dissertation

This research work provides extensive and detailed analysis of thermal effects of self-heating in SOI bipolar junction transistors, characterizing both the large-signal and the small-signal thermal effects. It tackles various areas such as physics based SPICE Gummel-Poon (SGP) and Vertical Bipolar Inter-Company (VBIC) model parameters development, frequency-domain characterization of dynamic self-heating through the analytical formulations, simulation and measurement, time-domain measurement of thermal tails, and development of two new self-heating tolerant CFOA circuit topologies.

Chapter 2 provides a brief introduction to methodology used to develop physics based SGP and VBIC model parameters for CAD simulations. Some of the key model equations are illustrated to discuss why and how parameter values are calculated or approximated or assumed. Finally, the proposed model response has been verified through some of the basic simulations using the SPECTRE simulator.

Chapter 3 gives an introduction to the definition and the classification of different types of self heating thermal effects. It also introduces unique analytical

formulations of dynamics self-heating effects in an SOI bipolar junction transistor configured in the common-emitter configuration with and without emitter degeneration resistor, and in cascode configuration. Several circuits are analyzed from static self-heating perspective and techniques to reduce such effects are discussed as well.

Chapter 4 explores the effects of self-heating on various current mirrors. This chapter is essentially focused on the modeling and characterization of the output impedance and admittance of different current mirrors and identifies the current mirror topologies which can mitigate the frequency domain non-ideal effects. Several current mirrors are fabricated, and DC and frequency domain measurement are reported, substantiating the analytical formulations.

Chapter 5 provides an overview of classical circuit topology of the CFOA. It provides an extensive study on the impact of dynamic self-heating on the open-loop transimpedance response, $Z_T(s)$, Common Mode Rejection Ratio (CMRR), and Power Supply Rejection Ratio (PSRR). It also provides simulation test circuits for the simulation of the open-loop transimpedance, CMRR, and PSRR frequency response. It does investigate the origin of thermal tail in the large-signal step response of the class AB buffers.

Chapter 6 proposes two new CFOA circuit topologies to suppress the effects of self-heating. The key merits and demerits of the new circuits are highlighted, and compared with the well-known classical CFOA circuit topology from self-heating perspective. Various design techniques are suggested to develop self-heating tolerant CFOAs circuit topologies.

Chapter 7 provides the fabrication and packaging details of the designed CFOAs. It also provides extensive details on the dc, frequency-domain, and time-domain measurement of various parameters of the CFOAs: Cascode current mirror based CFOA – CFOA I, and Folded-cascode input stage based CFOA– CFOA II.

Finally, chapter 8 concludes summarizing the overall accomplishment of this research work and provides very useful insight and recommendation for future work in this field.

Several appendices are provided for more detailed explanation on the specific topics, discussed briefly within the chapters. Appendix A summarizes the list of all SPICE Gummel-Poon (SGP) model parameters and few key device physics equations, which are extensively used in chapter 2. Appendix B provides the derivation of the output impedance of the bipolar transistor in the common-emitter (*CE*) configuration including the effect of dynamic self-heating through an indefinite-admittance matrix approach. It provides a theoretical background to assess the location of thermally induced zero and pole from the transfer function of the output impedance. Appendix C provides a detailed derivation for the admittance parameters of the bipolar transistor in the *CE* configuration with emitter degeneration resistor through the indefinite admittance matrix approach, and shows how the emitter degeneration helps in reducing the effective base and collector thermal transconductances. Appendix D provides a theory to assess the minimum value of the feedback resistor required in the closed-loop operation of a CFOA to avoid oscillation in the time-domain response. Appendix E provides an analytical formulation showing how thermal tail of the class AB buffer

depends on the bias current. Appendix F provides the frequency domain measurement of the on-die pad and DIP package parasitic.

1.5 Summary

This chapter outlined the dependency of collector current and base-emitter voltage of bipolar transistors on temperature. The temperature of the active emitter area of the bipolar transistor, fabricated in an SOI bipolar process technology, gets elevated due to the thermal effects of self-heating. The consequences of thermal effects of SOI BJTs are highlighted and their impacts on the performance of analog circuits are provided briefly. An introduction to the modeling of the effects of self-heating has also been presented briefly. This chapter provides basic information about the thermal effects of self-heating, and detail analysis will be provided in the chapters to come.

CHAPTER 2

DEVELOPMENT OF BIPOLAR JUNCTION TRANSISTOR MODELS FOR CAD SIMULATIONS

This chapter presents a physics based method to calculate the SGP and VBIC model parameters for the well-known advanced bipolar process technologies - Dielectrically Isolated Bipolar Junction Transistors (DIJBT) [23]-[24] and Extra Fast Complementary Bipolar process (XFCB) [25].

While there are many MOS transistor models publicly available from TSMC, there are only two industry standard BJT models – SGP and VBIC – for integrated-circuit design simulations. Ironically, there is not even a single well-documented BJT SGP or VBIC model for advanced bipolar process technology in the public-domain. Hence, there is a need to have SGP and VBIC models for CAD simulations for designers. To address this issue, physics based SGP and VBIC models have been developed based on the architectural assumptions for an SOI double-poly bipolar process technology. Extensive device physics formulations and several approximations in compliance with published literature are used to generate a complete list of values for the SGP and VBIC model parameters. The physics based model takes emitter, base and collector doping concentration, and the areas of the base-emitter and base-collector junctions as inputs and calculates possible SGP parameters, incorporating the impact of oxide isolations.

2.1 Dielectrically Isolated Bipolar Junction Transistor (DIBJT)

To meet the demand of ever-increasing bandwidth requirement in high speed analog integrated circuits, there was a necessity to develop a *pnp* transistor with comparable performance of an *npn* transistor. To address this issue, National Semiconductor came up with a technology called VIP10^{TM} (Vertically Integrated *pnp*) to design the most power-efficient and high-speed amplifiers on the market today. Complementary bipolar transistor designs, by using high-performance *npn* and *pnp* bipolar transistors, can offer the best combinations of features required in today's high speed amplifiers: wide bandwidth, low power consumption, low supply voltages, large output swing, high output current and low distortion [24].

2.1.1 Process Architecture

The cross-section view of the VIP10^{TM} bipolar process is shown in Fig. 2.1.

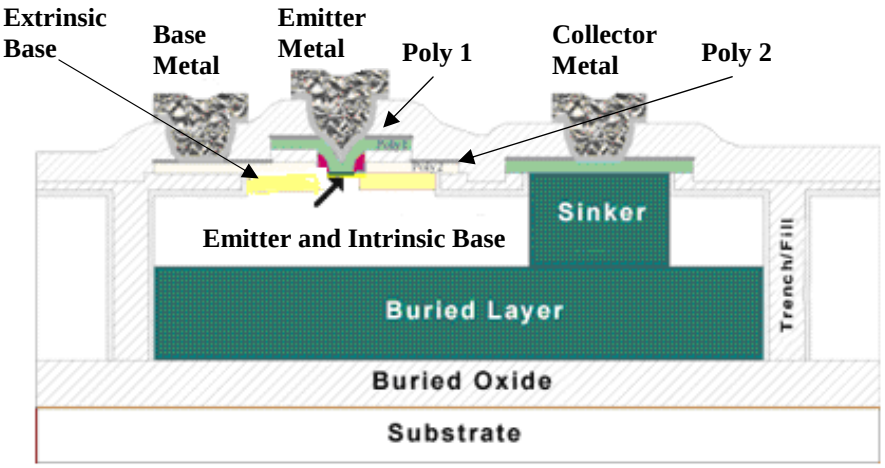


Figure 2.1 Cross-section view of the VIP10^{TM} transistor [23].

The excellent performance of the VIP10^{TM} transistor stems from its advanced process architecture. As shown in Fig. 2.1, the active region of the transistor is SOI, which is

fabricated using bonded wafer techniques. This oxide isolation produces a buried oxide layer that isolates the bottom of the epitaxial tubs from the substrate. The *p* and *n* type buried layers are followed by epitaxial growth. The tub holds the base, emitter and collector of the bipolar transistor. Trenches are anisotropically etched into the silicon and filled to form the isolation sidewalls. Consequently, the VIP10^{TM} transistor collectors are fully dielectrically isolated (DI) from one another. They have no *pn* junction between the collectors and substrate or well, unlike the previous generation junction isolated (JI) collectors [23]. This reduces the collector-substrate depletion capacitance, C_{js}, in comparison with a junction isolated transistor because of the lower permittivity of oxide compared to silicon, and hence SOI transistors offer better AC performance. The base-collector depletion capacitance, C_{bc}, is the next parasitic capacitance to address. This play a critical role in high speed designs due to the Miller effect. In conventional high speed transistors, a lightly doped intrinsic base is contacted by a highly doped extrinsic base diffusion and this extrinsic base region produces a large base sidewall capacitance. The VIP10^{TM} eliminates this problem with dielectric isolation at the sidewalls.

Two different polysilicon layers, *n*+ and *p*+, are used for emitter and base contacts. A poly 2 (*p*+ polysilicon) regions defines the extrinsic base region. A hole inside the poly 2 geometry is the emitter window and intrinsic base. The emitter is separated from the extrinsic base by a nitride spacer. The emitter is contacted by the poly 1 (*n*+ polysilicon), allowing the base contact to be very close to the emitter, reducing the extrinsic parasitic base resistance, r_{bb}. Both polysilicon layers are salicided

(polysilicon treated with titanium to form $TiSi_2$ [2]), further reducing the parasitic resistances in series with emitter, base and collector.

The most common AC figure of merit of the bipolar transistor is the transition frequency, f_T, – where the magnitude of the short-circuit common-emitter current gain becomes unity. A higher value of the transition frequency requires a low value of the diffusion capacitance for a given operating point. Some of the key parameters of the VIP10™ process [23] are provided in Table 2.1.

Table 2.1 Public-Domain SGP Model Parameters for the VIP10™ Process [23].

Process	**VIP1**	**VIP2**	**VIP3**	**VIP10**
Year	1986	1988	1994	2000
NPN f_T	0.4	0.8	3.0	9.0
NPN Beta, β_F	250.0	250.0	150.0	100.0
NPN V_A	200.0	150.0	150.0	120.0
PNP f_T	0.2	0.5	1.6	8.0
PNP Beta, β_F	150.0	80.0	60.0	55.0
PNP V_A	60.0	40.0	50.0	40.0
Collector-substrate capacitance, C_{js}	2.00	1.50	0.50	0.01
Emitter Width	15.0	11.0	2.0	1.0
Minimum Transistor Area	20000.0	18000.0	2400.0	300.0
MAX Supply Voltage	36.0	36.0	32.0	12.0
Isolation	JI	JI	JI	DI

2.1.2 SPICE Gummel-Poon (SGP) Model

The SPICE Gummel-Poon (SGP) model has been the industry standard bipolar transistor model for more than 20 years [20], [26]-[27]. The formulations of the model account for key physical phenomena and mechanisms that control the behavior of the junction isolated BJTs. Fig. 2.2 shows the equivalent circuit of the SGP model for the

npn bipolar transistor. It is a three-terminal – emitter, base, and collector – model, and consists of three current sources, I_{cc}, I_{bc} and I_{be}, two capacitances associated with the depletion and diffusion charges, Q_{bc} and Q_{be}, stored between the base and collector terminals, and between the base and emitter terminals, respectively. It has three parasitic resistances: 1) bias dependent base resistance, R_b, 2) fixed collector resistance, R_c, due to the collector sheet resistance and collector contact resistance, and 3) fixed emitter resistance, R_e, due to the emitter sheet resistance and emitter contact resistance. The most basic of all variants of the SGP model is the integral charge control model for the dc current passing through the emitter and collector terminals [27]-[28]. This model has adequately addressed the second-order effects - low-current effects, complete description of base width modulation, and high-level injection [20].

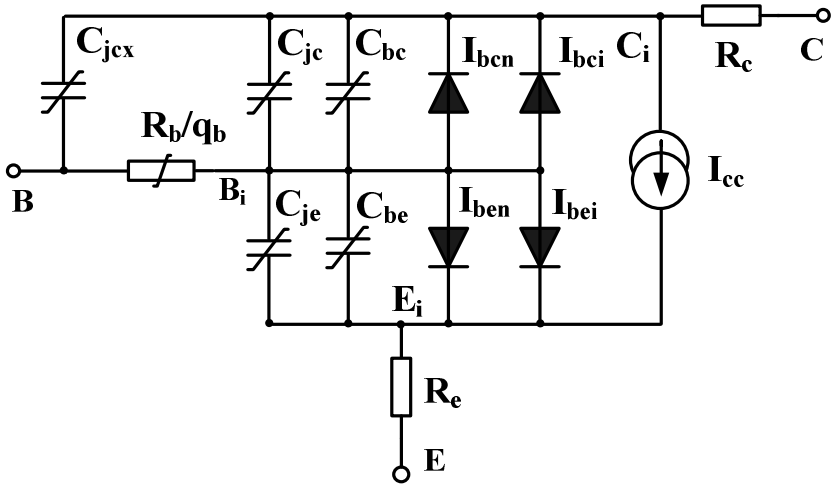


Figure 2.2 Equivalent circuit of SGP model [20].

A prominent reason for the decrease in accuracy of the SGP model is due to changes in BJT process technology over the past decades. Reduced base width in modern bipolar process technology leads the approximations, made in the Early effect

modeling in the SGP model, to give unacceptably large errors in the modeling of output conductance, g_o, in modern devices [28].

This model does not have the provision to simulate the effect of self-heating, which is considered as one of the most dominant thermal issues in a modern BJT. The details of the SGP model parameters are provided in Appendix A.

2.1.3 Vertical Bipolar Inter-Company (VBIC) Model

McAndrew, and Seitchik pointed out [20] that the SGP model for the bipolar transistor has become too inaccurate for low risk design in modern technologies. The VBIC model has enabled to overcome the major deficiencies of the SGP model. Most importantly, it has addressed the most common physical effects, such as accurate output conductance, g_o, modeling, bias dependent collector resistance, R_c, modulation, parasitic substrate transistor modeling, parasitic overlap capacitances of the base-emitter and base-collector junction in the double poly bipolar process technology, weak avalanche multiplication in the base-collector junction, and self-heating found in modern bipolar process technologies - VIP10^{TM} [23] and XFCB [25].

Figure 2.3 shows the equivalent circuit for the VBIC model of the *npn* bipolar transistor. Quasi-saturation is modeled with the elements R_c, C_{bcx}, and C_{bcq} [27]. The intrinsic and parasitic transistors base resistances, R_{bi} and R_{bip}, are modulated by the normalized intrinsic and parasitic base charges, q_b and q_{bp} (to be discussed in section 2.3.2), respectively. Self-heating model includes thermal resistance, R_{th}, and thermal capacitance, C_{th}, along with the thermal power source, I_{th}, which couples the power generated in the transistor to the thermal network. The local temperature rise at node

"*dT*" in the thermal network is linked to the electrical model through the temperature mappings of model parameters. Excess phase effect has also been modeled through a second order *RLC* network as shown in Fig. 2.3. A weak avalanche current, I_{gc}, is included for the base-collector junction as shown in Fig. 2.3. The constant capacitances, C_{BEO} and C_{BCO} are included to model the extrinsic base-emitter and base-collector overlap capacitances in the double poly bipolar process, respectively.

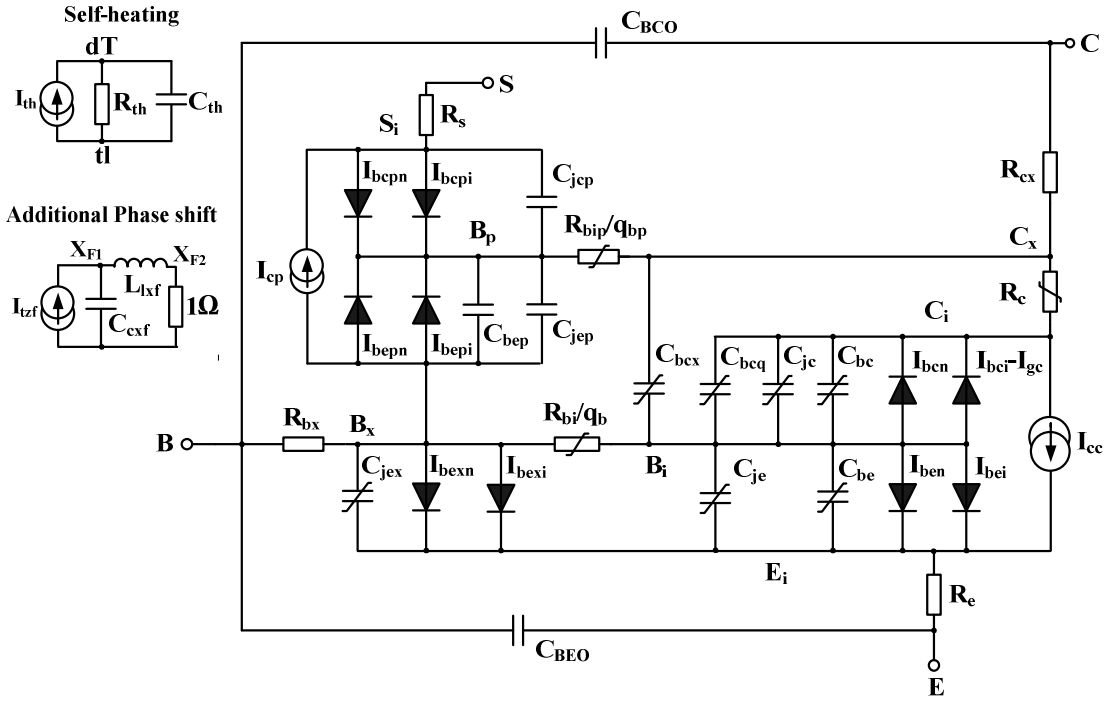


Figure 2.3 The equivalent circuit for the VBIC bipolar transistor model [26].

In summary, the key enhancements in the VBIC model over the SGP model are improved Early effect modeling, quasi-saturation modeling, parasitic substrate transistor modeling, parasitic fixed capacitance modeling, avalanche multiplication modeling, improved temperature dependency modeling, decoupling of base and collector current, and electrothermal (self-heating) modeling.

2.2 SGP Model Parameters Estimation

2.2.1 Doping Profile for the Bipolar Transistor

Consider a hypothetical *npn* transistor structure with doping concentrations and minority-carrier life time in respective regions as shown in Fig. 2.4.

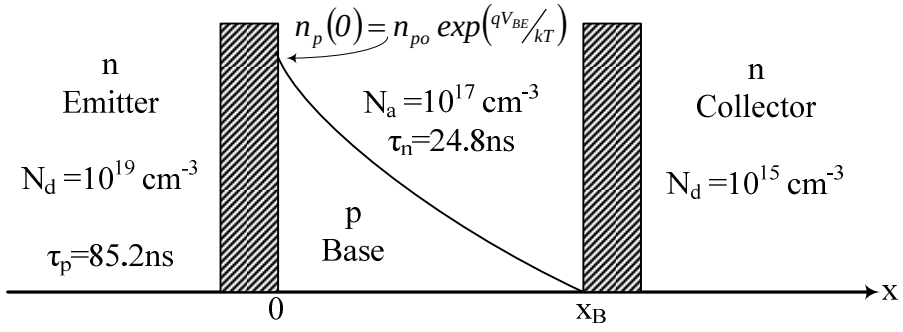


Figure 2.4 Doping concentration profile of the assumed high performance *npn* bipolar transistor in the forward-active region [2].

Some of the key input parameters, along with description, are provided in Table 2.2. These input values are used to calculate the parameters shown in Table 2.3.

Table 2.2 Doping Profile and Device Feature Size for a Hypothetical Transistor.

Parameter Details	**Values for NPN**	**Values for PNP**	**Units**
Emitter doping concentration (n/p type)	1.0×10^{19}	1.0×10^{19}	cm^{-3}
Base doping concentration (p/n type)	1.0×10^{17}	1.0×10^{17}	cm^{-3}
Collector doping concentration (n/p type)	5.0×10^{15}	5.0×10^{15}	cm^{-3}
Intrinsic-carrier concentration (n_i)	1.45×10^{10}	1.45×10^{10}	cm^{-3}
Thermal voltage, V_T	2.57×10^{-02}	2.57×10^{-02}	Volt
Active base-emitter area, *AE*	5.0×10^{-08}	5.0×10^{-08}	cm^2
CNR base width, x_B	5.0×10^{-05}	5.0×10^{-05}	cm
Active base-collector area, *AC*	5.0×10^{-07}	5.0×10^{-07}	cm^2

2.2.2 Techniques to Derive NPN Model Parameters

A hypothetical transistor physical structure is considered with attributes provided in Table 2.2 and few important parameters – diffusion constant, minority carrier life time, diffusion length, zero-bias depletion width, and etc – are calculated as provided in Table 2.3 using the device physics equations provided in Appendix A.

Table 2.3 Calculation of Basic Parameters for the *NPN* and *PNP* Transistors.

NPN: Calculated Paramters		**Units**	**PNP: Calculated Parameters**		**Units**
Nominal Temperature	298.00	Kelvin	Nominal Temperature	298.00	Kelvin
Electronic Charge(q)	1.60E-19	Colomb	Elec. Charge(q)	1.60E-19	Colomb
Permittivity Si	1.04E-12	F/cm^2	Permittivity Si	1.04E-12	F/cm^2
Dn in Base @ 1E17	1.80E+01	cm^2/s	Dp in Base @ 1E17	8.00E+00	cm^2/s
Tmin in Base	2.48E-05	sec	Tmin in Base	2.48E-05	sec
Dp in Emitter @ 1E19	1.85E+00	cm^2/s	Dn in Emitter @ 1E19	2.96E+00	cm^2/s
Tmin in Collector	4.33E-05	sec	Tmin in Collector	4.33E-05	sec
Dp in Collector @ 1e15	1.20E+01	cm^2/s	Dn in Collector @ 1e15	3.50E+01	cm^2/s
Ln in NPN base	2.11E-02	cm	Lp in PNP base	1.41E-02	cm
Lp in NPN Collector	2.28E-02	cm	Ln in PNP Collector	7.02E-01	cm
Base Transit Time	6.94E-11	sec	Base Transit Time	1.56E-10	sec
Built-in Potential of B-C	7.32E-01	V	Built-in Potential of B-C	7.32E-01	V
Built-in Potential of E-B	9.28E-01	V	Built-in Potential of E-B	9.28E-01	V
Zero-Bias BC Depltion Width	4.46E-05	cm	Zero-Bias BC Depltion Width	4.46E-05	cm
Zero-Bias EB Depltion Width	1.10E-05	cm	Zero-Bias EB Depltion Width	1.10E-05	cm
VBE for IKF	8.09E-01	V	VBE for IKF	8.09E-01	V
Tmin in Emitter	8.52E-08	sec	Tmin in Emitter	8.52E-08	sec
Lp in Emitter	3.97E-04	cm	Ln in Emitter	5.02E-04	cm

2.2.2.1 Estimation of DC SGP Model Parameters

This section is focused on the calculation of the SGP model parameters that are attributed to describe the dc response of the bipolar transistors. The forward beta, β_F and Early voltage, V_A, of the VIP10^{TM} [23]-[24] bipolar process are 100 and 120 V, respectively as provided in Table 2.1. From device physics, the forward beta, β_F, can be expressed as [7]

$$\beta_F = \frac{1}{\frac{W_B^2}{2\tau_b D_n} + \frac{D_p}{D_n}\frac{W_B}{L_P}\frac{N_B}{N_E}} \tag{2.1}$$

It can be inferred from (2.1) that β_F can be maximized by maximizing the ratio of emitter to base doping and minimizing the base width. The evaluation of (2.1) using the values of the parameters in Table 2.3 gives $\beta_F = 120$. Assuming that the value of the forward beta, β_F, and the Early voltage, V_A, of the hypothetical *npn* transistor is 30% higher than the values for the VIP10™ *npn* transistor, provided in Table 2.1, the value of the forward beta, and the Early voltage is approximately 130 and 156, respectively.

Since the transistor doping profile, in general, is optimized for the forward direction, the value of reverse beta, β_R, has been reported to be 1.0 in most of the literature [26], [29]. The smaller base size and lower ratio of base to collector concentration for the assumed transistor structure shown in Fig. 2.4 and Table 2.2, the value of reverse beta is approximated to be 3.0. The transistor emitter current in the reverse active should show a large dependency on the emitter-collector voltage, V_{EC}, because the base-collector junction is forward bias while the base-emitter junction is reversed bias. To model the wider depletion width in the base at the base-emitter junction (in inverted mode), the value of reverse Early voltage can be approximated to be 5.0 [26]. The temperature dependency of beta can be modeled using the temperature coefficient parameter, *XTB*. This temperature dependence of β_F is due to the extremely high doping density in the emitter, which causes the emitter injection efficiency, γ, to increase with temperature. A typical fractional temperature coefficient of β_F is +7000

ppm/°C [7]. The temperature exponent parameter of for the forward-beta, *XTB*, used in this model is 1.7 based on the model previously reported [10].

The transport saturation current, *IS*, can be expressed as [8]

$$IS = AE \cdot \frac{qD_n n_i^2}{x_B N_B} \tag{2.2}$$

Using the parameters defined in Tables 2.2 and 2.3, (2.2) is found to be 6.06×10^{-18} A. From (2.2), it is evident that the saturation current is proportional to the square of the intrinsic carrier concentration, n_i, which can be expressed as [7]

$$\mathrm{n_i^2(T)} = AT^3 \exp\left[-\frac{V_{G0}}{V_T}\right] \tag{2.3}$$

Equations (2.2) and (2.3), after some algebraic manipulation gives:

$$IS(T) = \frac{C_t}{Q_B} \cdot T^{4-n} \cdot \exp\left[-\frac{V_{G0}}{V_T}\right] \tag{2.4}$$

Where C_t is the temperature independent term. The temperature exponent of saturation current, *XTI*, can be conservatively approximated as 3.5 [5].

The temperature dependent expression for the Si bandgap energy, E_g, can be expressed as [8]

$$E_g = 1.17 - \frac{4.73 \cdot 10^{-04} \cdot T^4}{T + 651} \tag{2.5}$$

The substitution of T = 297 K into (2.5) yields E_g = 1.125 eV.

The forward current in a *pn* junction varies as $exp(V_a/nV_T)$ with *n* designated as the ideality factor. For the diffusion current, the ideality factor, *n*, can be represented by *NF* with a value of 1.0, and for space charge recombination current, *n* can be

represented by *NE* with a value of 2.0 [2], [8]. A similar explanation holds true for the values of the ideality factors, *NR* and *NC*, in reverse-mode. The values for *NF* and *NR* can be approximated to be 1.0 because they are estimated from the mid range of the I_C over V_{BE} curve where linearity exists. The values for *NC* and *NE* can be approximated to be 2.0 because they are extracted from the non-linear region of the I_C-V_{BE} curve. In the voltage range where n is between 1.0 and 2.0, the current is due to the combination of diffusion and space-charge recombination currents. The space charge recombination saturation current, *ISE* and *ISC*, for the base-emitter and base-collector junction can be expressed as [8]

$$ISX = \frac{AX \cdot qW_{dx}n_i}{2\tau_{o,eff}} \tag{2.6}$$

where X represents emitter or collector, W_{dx} is the depletion width at the base-emitter junction or base-collector junction, and $\tau_{o,eff}$ is the effective minority carrier life time in the space charge region. Using the parameters defined in Table 2.3, (2.6) is found to be 7.5×10^{-15} A for *ISE* and 5.97×10^{-16} A for *ISC*.

At a higher voltage, there is a possibility for a higher level of minority-carrier injection into the base, which is characterized by the "knee" current. The I_C-V_{BE} characteristics start to deviate from its linear relationship from the knee current. Under high level injection, the excess minority charge is very close to the majority carrier of the semiconductor material. In this region, current begins to follow $exp\ (V_a/2V_T)$. For high level injection to occur, the criteria of (2.7) needs to be satisfied [30]-[31]

$$V_{BE\ or\ BC} > 2V_T \cdot \ln\left[\frac{N_B}{n_i}\right] \tag{2.7}$$

The forward-mode and reverse-mode high level injection parameter, *IKF* and *IKR* defined by (2.8) and (2.9), can be calculated based on the value of V_a given by (2.7)

$$IKF = IS \cdot \exp\left[\frac{V_a}{NF \cdot V_T}\right] \tag{2.8}$$

$$IKR = ISC \cdot \exp\left[\frac{V_a}{NR \cdot V_T}\right] \tag{2.9}$$

Equation (2.7) gives $V_{BE} > 0.809$ *V*. The corresponding high level injection current parameters, *IKF* and *IKR*, can be evaluated using (2.8) to 3.04 mA with $V_{BE} = 0.87$ V, and 30.4 mA with $V_{BC} = 0.87$ V, respectively.

2.2.2.2 Estimation of AC SGP Model Parameters

This section deals with the parameters, which describe the *C-V* characteristics of the device. The total capacitance for the *pn* junction is the sum of the depletion capacitance, C_j, and diffusion capacitance, C_d. The nonlinear charge elements or equivalently the voltage-dependent depletion capacitances shown in Fig. 2.2 are determined by (2.10) [7]-[8].

$$C_{jX} = AX \cdot CJOX \cdot \left[1 - \frac{V_{aX}}{V_{biX}}\right]^{-MJX} \tag{2.10}$$

where X represents either the base-emitter junction or the base-collector junction. The variables *AX*, V_{biX}, *CJOX*, and V_{aX}, represent the junction area, built-in potential as

defined by (2.11), zero-bias depletion capacitance as defined by (2.12), and the reverse bias voltage of the base-emitter junction or base-collector junction.

$$VJX = V_T \ln\left[\frac{N_X N_B}{n_i^2}\right] \tag{2.11}$$

$$CJOX = AX \cdot \sqrt{\frac{\varepsilon \cdot q \cdot N_X N_B}{2 \cdot VJX \cdot (N_X + N_B)}} \tag{2.12}$$

In these expressions, N_X represents the doping concentration of either the emitter or the collector, and N_B represents the doping concentration of the base. The depletion capacitance is dominant under the reverse bias while the diffusion capacitance, defined as the capacitance associated with incremental changes in the injected minority-carrier charge in the base as dictated by (2.13), is dominant in the forward bias.

$$C_d = TFF \cdot g_m \tag{2.13}$$

Equations (2.11) and (2.12) yield VJE = 0.928 V, and CJEO = 4.7×10^{-15} F for the base-emitter junction, and VJC = 0.732 V, and CJCO = 1.03×10^{-14} F for the base-collector junction, respectively with the parameters defined in Table 2.3. The grading coefficient for the base-emitter junction, MJE, and the base-collector junction, MJC, is assumed to be 0.33 for a lineally graded junction [7] and 0.25 for a non-linearly graded junction. The collector substrate capacitance, C_{js}, is assumed to be 5.0×10^{-15} F [23], the same as the *npn* transistor. The built-in potential of the Si-SiO_2 interface can be approximated to be twice the Fermi potential, and is shown by

$$VJS = 2 \cdot \phi_n = 2V_T \ln\left(\frac{N_C}{n_i}\right) \tag{2.14}$$

This is equal to the surface potential for a MOS structure and can be evaluated to VJS = 0.655V using the values of N_C and n_i from Tables 2.2 and 2.3 The junction grading coefficient, *MJS*, the Si-SiO_2 interface is 0.0 due to the lack of depletion capacitance at the interface.

SPICE uses different expressions for the capacitance calculations. It chooses one expression over the other based on the bias level. The bias level is dictated by the parameter called the depletion capacitance coefficient, *FC*, whose default value is reported to be 0.5 for SGP model [26], [29]. There is another parameter, *XCJC*, which distributes the collector-base junction capacitance between the inner and the outer base contact. Its default value is 1.0, meaning the base- collector capacitance, C_{bc}, is tied completely to the inner base [33]. Its value is assumed to be 0.8 for this model.

2.2.2.3 Estimation of Transit Time Related SGP Model Parameters

The maximum useful frequency range of a transistor is generally specified by its transition frequency, f_T [8].

$$f_T = \frac{g_m}{2\pi \cdot (C_\pi + C_\mu)} \tag{2.15}$$

Since the diffusion capacitance is most likely to be higher than the depletion capacitances under the forward bias, the total capacitance, C_π+C_μ, can be approximated to C_π, which can be approximated as the diffusion capacitance, C_d, defined by (2.13). The forward transit time, *TF*, which can be viewed as the ratio of charge in transit, Q_e, to the current flow, I_C, which can also be interpreted as the average time per carrier spent in crossing the base region, and can be expressed as [7]

$$TF = \frac{Q_e}{I_C} = \frac{x_B^2}{2D_n} \tag{2.16}$$

where x_B, and D_n are the base charge-neutral region and diffusion constant of an electron in the base, respectively. Equation (2.16) is evaluated to be 69.44 ps using the parameters defined in Table 2.3. The forward transit time, *TF*, from (2.15) using (2.13) can be expressed as

$$TF \approx \frac{1}{2\pi . f_T} \tag{2.17}$$

A typical value of f_T for a high performance *npn* transistor from the VIP10™ process [23] is 9.0 *GHz*. Equation (2.17) can be evaluated to give the value of TF as 17.76 ps with f_T = 9.0 GHz. For accuracy, the value of 17.76 ps is preferred over 69.44 ps for *TF*.

The bias dependence of the effective transit time, *TFF*, in SPICE has been modeled as [26], [34]

$$TFF = TF \cdot \left[1 + XTF \left(\frac{I_F}{I_F + ITF} \right)^2 \cdot \exp\left(\frac{V_{BC}}{1.44 \cdot VTF} \right) \right] \tag{2.18}$$

Where *TF*, *XTF*, *VTF*, and *ITF* are the ideal forward transit time, coefficient for bias dependence of *TF*, coefficient for base-collector bias dependence of *TF*, and collector current dependence parameter of *TF*, respectively. The parameter, *TF*, is the ideal forward transit time modeling the "excess charge" in the base. The parameters, *XTF* and *ITF*, model the collector current dependence of the forward transit time, *TF*, while *VTF* describes the dependency of *TF* on V_{CE}. The parameter, *ITF*, can be approximated to *IKF*, and hence *ITF* is equal to 3.04 mA. Assuming that the forward transit time will be

reduced by 10% due to the bias dependency, the value of *VTF* is obtained as 2.5 from (2.18).

The transit time in the reverse active mode, *TR*, should be higher than *TF* because the device structure and doping profiles are optimized for the operation in the forward-active region. Thus, the reverse base transit time is assumed to be higher than *TF* by a factor of 100 and hence the calculated value of *TR* is 1.776 ns. Since the saturation region is a combination of forward-active and inverse-active operation, inclusion of the parameter *TR* in SPICE models the charge storage that occurs in saturation. The value *TR* is not modulated by the bias current or voltage, unlike *TF*.

The excess phase shift due to the distributed nature of the base in the SGP model is modeled with the second-order *Bessel function* [29], with the resonance parameter ω_o (assumed less than idealized maximum frequency, ω_T). The excess phase shift, *PTF*, can be expressed as [29]

$$PTF = \frac{\omega_T}{\omega_o} \tag{2.19}$$

Assuming $\omega_o = 2.25 \times 10^{09}$ rad/s and $\omega_T = 56.3 \times 10^{09}$ rad/s, the PTF is calculated as 25 degrees using (2.19).

2.2.2.4 Estimation of Ohmic Parasitic Model Parameters

The parasitic resistances in the bipolar transistor are the base resistance, r_{bb}, collector resistance, r_c, and emitter resistance, r_e. It is reported [7] that typical values of the base, emitter, and collector resistances are in the rage of 50.0 to 500.0 Ω, 1.0 to 3.0 Ω, and 20.0 to 500.0 Ω, respectively depending on the process technology. The value of

r_{bb} varies significantly with collector current because of current crowding effect [2], [7]-[8], [29]. The dc base current produces a lateral voltage drop in the base that tends to forward bias the base-emitter junction preferentially around the edges of the emitter at high collector current. Thus, the transistor action tends to occur along the emitter periphery rather than under the emitter itself, and the distance from the base contact to the active base region is reduced. A typical variation of base parasitic resistance with collector current, I_C, is shown in Fig. 2.5.

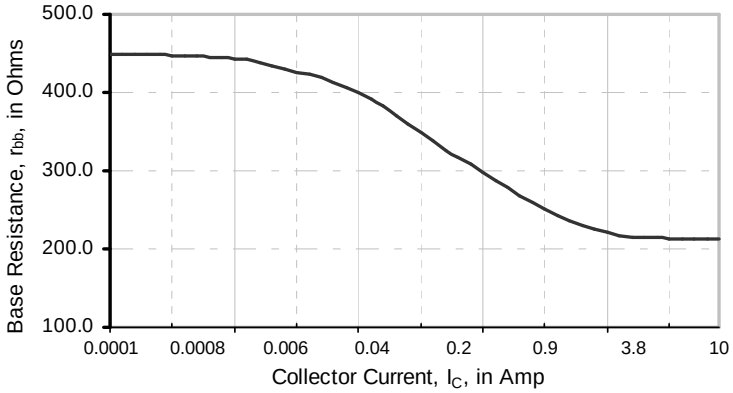


Figure 2.5 Dependence of base resistance on I_C for the *npn* transistor [7].

As shown in Fig. 2.5, the value of base parasitic resistance, r_{bb}, vary by 50% in a typical junction isolated *npn* transistor as the collector current, I_C, varies from 0.1 mA to 10.0 mA. The current dependence of the base resistance in SPICE is expressed as [26], [34].

$$r_{bb} = RBM + 3(RB - RBM)\cdot\left(\frac{Tanz - z}{z - Tan^2 z}\right) \tag{2.20a}$$

$$z = \frac{-1+\sqrt{1+\left(\frac{12}{\pi}\right)^2 \cdot \frac{I_b}{IRB}}}{\frac{12}{\pi^2}\cdot\sqrt{\frac{I_b}{IRB}}} \tag{2.20b}$$

where *RBM* is the minimum base resistance at high base current, *RB* is the base resistance at zero-bias or small base current, and *IRB* is the current where the base resistance falls halfway its minimum value. Extensive details on base parasitic resistance can be found in [29]. In a typical SOI BJT process, there are two components of base region, intrinsic base directly under the emitter and long extrinsic polysilicon (highly doped) base that extends upto the base contact [2], [23]. At a zero bias current, it is reasonable to assume that the base resistance will be dominated by the lightly doped base region of the base shown in Fig. 2.1. Hence the value of *RBM* can be approximately 400 Ω from Fig. 2.5. The base resistance at higher collector current will mainly be dominated by the heavily doped extrinsic base whose resistance is approximated as 30 Ω. The value of *IRB* is assumed to be 1 mA.

In a modern SOI process technology, both base and emitter polysilicon are salicided to minimize the series parasitic of emitter and collector [2]. A typical sheet resistance of salicided polysilicon is reported in the range of 3 Ω/□ and 10 Ω/□ [35]. Assuming the sheet resistance of 5 Ω/□ for emitter and collector, the collector parasitic resistance, r_c, and emitter parasitic resistance, r_e, are 15 Ω and 10 Ω for a 5 μm x 15 μm collector contact and a 5 μm x 10 μm emitter contact, respectively.

2.2.2.5 Estimation of Noise Related SGP Model Parameters

Flicker noise is found in all active devices. It is generated due to several reasons, but is mainly caused by traps associated with contamination, crystal defects. The mean square value of flicker noise, which is always associated with a flow of direct current, can be expressed as [36]

$$I_{nf}^2 = KF \cdot \frac{I^{AF}}{f} \cdot \Delta f \tag{2.21}$$

where *KF*, *AF* and Δf are the flicker noise coefficient, flicker noise exponent, and noise bandwidth, respectively. Typical values for *KF* and *AF* are 10.0×10^{-16} A and 1.0 respectively [39]. Because of extra contribution in flicker noise due to oxide isolation in SOI devices, the values of *KF* and *AF* parameters are assumed to be 1.0 nA and 2.0, respectively.

2.2.3 Techniques to Derive PNP Model Parameters

The doping profiles of the assumed *pnp* transistor are provided in Table 2.2. A similar approach described for the *npn* transistor in section 2.2.2 is used to estimate the model parameter values for a *pnp* transistor. The ratio of hole mobility to electron mobility or vice-versa is extensively used to calculate the *pnp* model parameters wherever applicable. Some of the key model parameters have been directly used from National Semiconductor website [23]-[24]. A generic expression to calculate current based parameters for the *pnp* transistor is

$$pnp \text{ model parameter} = \text{npn model parameter} \cdot \frac{\text{diffusitivity of hole}}{\text{diffusitivity of electron}} \tag{2.22}$$

In the complementary bipolar process, both the *pnp* transistor and the *npn* transistor performance are comparable with the limitation imposed by the lower hole mobility.

2.2.3.1 Estimation of DC SGP Model Parameters

The saturation current can be evaluated as 2.69×10^{-18} A using (2.22) and values of diffusion constant related to the *pnp* device from Table 2.3. Using the analysis discussed in section 2.2.2.1, the temperature exponent of *IS*, *XTI*, can be

approximated as 3.15. The values of the current emission coefficients, *NF*, *NE*, *NR*, and *NC* for the *pnp* device are assumed to be the same as the *npn* device. The recombination saturation currents, *ISE* and *ISC*, can be calculated using (2.6) with the parameters defined in Table 2.3, and are 7.5×10^{-15} A , and 5.97×10^{-16} A, respectively.

The forward and reverse high level injection current parameters, *IKF* and *IKR*, for the *pnp* transistor can be estimated to be 1.35 mA, and 13.5 mA, respectively using (2.22) and the values of diffusion constants from Table 2.3.

Assuming that the value of the forward beta, $\beta_{F,}$ and the Early voltage, V_A, of the hypothetical *pnp* transistor is 30% higher than the values for the VIP10^{TM} *pnp* transistor, provided in Table 2.1, the values of the forward beta, and the Early voltage for the assumed *pnp* transistor are approximately 72 and 52, respectively. Since the transistor doping profile, in general, is optimized for the forward direction, the value of reverse beta, β_R, is reported as 1.0 in most of the published literature [26], [29]. As explained for the *npn* transistor in section 2.2.2.1, the values of reverse beta and Early voltage for *pnp* should be very small, and hence the values of reverse beta, β_R and the reverse Early voltage, *VAR* are assumed to be 3, and 5 V [26], respectively.

The temperature dependency of beta can be modeled using the temperature coefficient parameter, *XTB*, using the similar approach discussed in section 2.2.2 for the *npn* transistor. The dependence of the forward beta on temperature for the *pnp* transistor can be assumed to be lower than that of the *npn* device due to the lower mobility of hole than electron. Thus, equation (2.22) can be used to calculate the parameter, *XTB*, for the *pnp* transistor, and it evaluates as 0.76.

2.2.3.2 Estimation of AC SGP Model Parameters

Using the parameters, defined in Table 2.3 for the *pnp* device, equations (2.11) and (2.12) yields VJE = 0.928V, CJEO = 4.7×10^{-15} F for the base-emitter junction. The grading coefficient for the base-emitter junction, *MJE*, is assumed to be 0.33 for a lineally graded junction [7]. Similarly, the values of *VJC* and *CJCO* are calculated 0.732 V, 1.03×10^{-14}F, respectively using (2.11) and (2.12), respectively for the base-collector junction. The grading coefficient for the base-collector junction, *MJC*, is assumed to be 0.25 for a non-linearly graded junction. The collector substrate capacitance, C_{js}, is assumed to be the same as the *npn* transistor – 5×10^{-15} F. The built-in potential for Si-SiO_2 interface, *VJS*, is assumed to be twice the surface potential for a MOS structure. Equation (2.14) gives VJS = 0.655 V. Due to the lack of depletion capacitance at the Si-SiO_2 interface, the value of MJS can be assumed to be zero.

2.2.3.3 Estimation of Transit Time Related SGP Model Parameters

A typical value for the transition frequency, f_T, for a high performance *pnp* transistor from the VIP10^{TM} process is 8.0 GHz [23]. The forward transit time for the *pnp* transistor, *TF*, is evaluated as 19.9 ps using (2.17). The parameter, *ITF*, can be approximately IKF, and so ITF = 1.35 mA. Assuming that the dependence of forward transit time on the bias voltage for the *pnp* transistor is much stronger than that for the *npn* transistor, the value of *XTF* parameter for the *npn* transistor can be increased by the ratio of electron to hole mobility, and is found to be 22.5. The parameter, *VTF*, is assumed to be 2.5, the same as *npn* transistor. Using similar assumptions for the *npn* transistor, the reverse base transit time, *TR*, for the *pnp* transistor is approximately 1.99

ns. The excess phase shift, *PTF*, is approximately 25 degrees, the same as the *npn* transistor.

2.2.3.4 Estimation of Ohmic Parasitic and Noise Model Parameters

Since the base parasitic resistance related model parameters, *RBM*, *RB*, and *IRB*, will be reduced over those parameters for the *npn* transistors with ratio of hole to electron mobility, the values of *RBM*, *RB*, and *IRB* are found to be 13.33 Ω, 177.78 Ω, and 0.44 mA, respectively using (2.22). However, the collector and emitter parasitic resistance, r_c and r_e, for the *pnp* transistor are increased over the *npn* transistor by the ratio of electron to hole mobility, and are 33.75 Ω and 22.5 Ω, respectively. The flicker noise coefficient, *KF*, is approximately 6.26×10^{-10} using (2.22), and the value of *AF* is assumed to be 2.0, the same as the *npn* transistor.

2.2.4 Summary of the SGP Models

The physics based model parameter values for the hypothetical *npn* and *pnp* transistors with an emitter area of 5.0 μm^2 are summarized in Tables 2.4 and 2.5.

Table 2.4 SGP Model Parameters for the *NPN* Transistor with an Emitter Area of 5 μm^2.

Paramters	**Values**	**Paramters**	**Values**	**Paramters**	**Values**	**Paramters**	**Values**
IS	6.06E-18	NC	2.00	VJE	9.28E-01	XTF	10.00
XTI	3.50	ISE	7.50E-15	MJE	3.33E-01	VTF	2.50
EG	1.13	ISC	5.97E-16	CJC	1.03E-14	ITF	3.04E-03
BF	130.00	IKF	3.04E-03	VJC	7.32E-01	PTF	2.50E+01
BR	3.00	IKR	3.04E-02	MJC	2.50E-01	TR	1.77E-09
XTB	1.70	RB	400.00	XCJC	8.00E-01	KF	1.00E-09
VAF	156.00	IRB	1.00E-03	CJS	5.00E-15	AF	2.00
VAR	5.00	RBM	30.00	VJS	6.55E-01	TNOM	25.00
NF	1.00	RE	15.00	MJS	0.00		
NR	1.00	RC	10.00	FC	5.00E-01		
NE	2.00	CJE	4.70E-15	TF	1.77E-11		

Table 2.5 SGP Model Parameters for the *PNP* Transistor with an Emitter Area of 5 μm^2.

Paramters	Values	Paramters	Values	Paramters	Values	Paramters	Values
IS	2.69E-18	NC	2.00	VJE	9.28E-01	XTF	10.00
XTI	3.15	ISE	7.50E-15	MJE	3.33E-01	VTF	2.50
EG	1.13	ISC	5.97E-16	CJC	1.03E-14	ITF	3.04E-03
BF	71.50	IKF	1.35E-03	VJC	7.32E-01	PTF	2.50E+01
BR	3.00	IKR	1.35E-02	MJC	2.50E-01	TR	1.77E-09
XTB	0.76	RB	177.78	XCJC	8.00E-01	KF	1.00E-09
VAF	52.00	IRB	4.44E-04	CJS	5.00E-15	AF	2.00
VAR	3.00	RBM	13.33	VJS	6.55E-01	TNOM	25.00
NF	1.00	RE	33.75	MJS	0.00		
NR	1.00	RC	22.50	FC	5.00E-01		
NE	2.00	CJE	4.70E-15	TF	1.99E-11		

The following syntax, as an example, can be used to prepare an *npn* transistor model file for the SPETCRE simulator.

.model npn NPN struct=vertical

+IS=6.06E-18 BF=130.0 NF=1.00 VAF=156.00 IKF=3.04E-03

+ ISE=7.50E-15 NE=2.00 BR=3.0 NR=1.00 VAR=5.00

+IKR=3.04E-02 ISC=5.97E-16 NC=2.00 RB=400.0 RBM=30.0

+ IRB=1.0E-03 RE=15.0 RC=10.0 CJC=1.03E-14 VJC=7.32E-01

+ MJC=0.25 CJE=4.7E-15 VJE=9.28E-01 MJE=0.33 XCJC=0.8

+CJS=5.00E-15 VJS=6.55E-01 MJS=0.0 TR=1.77E-09 KF=1.0E-09

+AF=2.00 EG=1.13 XTB=1.7 XTI=3.5 FC=0.5

+TF=1.77E-11 XTF=10.00 VTF=2.50 ITF=1.00E-03 PTF=25.0

The transistor area can be adjusted by the SPECTRE or SPECTRES “multiplier” or “area” parameters.

2.3 VBIC Model Parameters Estimation

2.3.1 Conversion of SGP to VBIC Model Parameters

Since the VBIC model is considered as an advanced model to the SGP model, most of SGP model parameters can be converted to the VBIC model parameters through the mapping scheme previously reported [26], [34], [37]. A summary of the SGP to VBIC model parameter mapping scheme is provided in Table 2.6.

Table 2.6 The VBIC Model Parameters from SGP Parameters through Mapping Table [26], [37] for the *NPN* and *PNP* Transistors with an Emitter area of 5.0 μm^2.

VBIC Model Parameters	**SGP to VBIC Mapping**	**Vertical NPN Transistor**	**Vertical NPN Transistor**
IS	IS*0.9	5.45E-18	2.42E-18
NF	NF	1.00	1.00
NR	NR	1.00	1.00
RBX	RBM	30.00	13.33
RCX	RC	10.00	22.50
RBI	RB-RBM	370.00	164.44
RE	RE	15.00	33.75
CJC	CJC	1.03E-14	1.03E-14
CJEP	(1-XCJC)*CJC	2.06E-15	2.06E-15
PC	VJC	0.73	0.73
MC	MJC	0.25	0.25
CJCP	CJS	5.00E-15	5.00E-15
CJE	CJE	4.70E-15	4.70E-15
PE	VJE	9.28E-01	9.28E-01
ME	MJE	0.33	0.33
IBEI	IS/BF	4.66E-20	3.76E-20
NEI	NF	1.00	1.00
IBEN	ISE	7.50E-15	7.50E-15
NEN	NE	2.00	2.00
IBCI	IS/BR	2.02E-18	8.97E-19
NCI	NR	1.00	1.00
IBCN	ISC	5.97E-16	5.97E-16

Table 2.6 - *Continued*

NCN	NC	2.00	2.00
VEF	VAF*0.5	78.00	26.00
VER	VAR*0.5	2.50	1.50
IKF	IKF*0.9	2.73E-03	1.21E-03
IKR	IKR*0.9	1.52E-02	6.75E-03
TF	TF*0.25	4.42E-12	4.98E-12
QTF		0.30	0.30
XTF	XTF	10.00	22.50
VTF	VTF	2.50	2.50
ITF	ITF	3.04E-03	1.35E-03
TR	TR	1.77E-09	1.99E-09
TD	pi* TF*PTF/180	7.72E-12	8.68E-12
KFN	KF	1.00E-09	6.26E-10
AFN	AF	2.00	2.00
BFN		1.00	1.00
XIS	XTI	3.50	3.15
XII	XTB	1.70	0.76
XIN	XTB	1.70	0.76
EA	EG	1.13	1.13
RCI	RC*10	100.00	225.00

Details of the VBIC model parameters can be found in [38]. The VBIC model parameters in Table 2.6 can be directly mapped from the SGP model parameters. The additional capabilities of the VBIC model can be turned off by setting the non-SGP equivalent parameter values to default values. By doing so, the VBIC model response closely matches the SGP model with exception of the Early effect formulations.

2.3.2 Method to Estimate the VBIC Model Specific Parameters

The base charge, q_b, for the VBIC model is defined as [34]

$$q_b = \frac{q_1}{2} + \sqrt{\left(\frac{q_1}{2}\right)^2 + q_2} \tag{2.23}$$

where q_1 (space charge dependent), and q_2 are defined as [34]

$$q_1 = 1 + \frac{q_{je}}{VER} + \frac{q_{jc}}{VEF} \tag{2.24}$$

$$q_2 = \frac{1}{IKF} \cdot IS \cdot \left(e^{\frac{V_{bei}}{NF \cdot VT}} - 1 \right) + \frac{1}{IKR} \cdot IS \cdot \left(e^{\frac{V_{bci}}{NR \cdot VT}} - 1 \right) \tag{2.25}$$

The calculated values of the parameters, *VER, VEF, IKF, IKR, NF,* and *NR* are provided in Table 2.6. The main collector current, I_{cc}, shown in Fig. 2.3 can be expressed as [26]

$$I_{cc} = \frac{I_{TF} - I_{TR}}{q_b} = \frac{IS}{q_b} \cdot \left(e^{\frac{V_{bei}}{NF \cdot VT}} - 1 \right) - \frac{IS}{q_b} \cdot \left(e^{\frac{V_{bci}}{NR \cdot VT}} - 1 \right) \tag{2.26}$$

The diffusion capacitances of the main transistor shown in Fig. 2.3 are modeled in analogy to the SGP model. The charges stored in the diffusion capacitances, C_{be} and C_{bc} of Fig. 2.3, are calculated by $Q_{be} = T_{FF} \cdot I_F$ in the forward-active mode, and $Q_{bC} = T_R \cdot I_R$ in the reverse-active mode. The forward transit time in the VBIC model is modeled by [26], [34]

$$TFF = TF \cdot (1 + QTF \cdot q_1) \cdot \left[1 + XTF \left(\frac{I_F}{I_F + ITF} \right)^2 \cdot \exp\left(\frac{V_{bci}}{1.44 \cdot VTF} \right) \right] \tag{2.27}$$

The term $(1+QTF \cdot q_1)$ covers the additional dependency of the forward transit time on the base width modulation. The default value of 0.3 for QTF [26] is used in this model.

The overall collector resistance is composed of a constant resistor, R_{cx}, and a variable resistor, $R_{ci,}$ to model quasi-saturation. The quasi-saturation, as implemented in the VBIC model, is essentially based on the Kull model [34]. The current, I_{Rc}, through the resistor, R_c, of Fig. 2.3 can be expressed as [34]

$$I_{Rc} = \frac{I_{epi0}}{\sqrt{1+\left(I_{epi0}\cdot R_{ci}/V0\cdot\left(1+\frac{0.5\sqrt{0.01+V^2_{rci}}}{V0\cdot HRCF}\right)\right)^2}}$$
$$I_{epi0} = \frac{1}{R_{ci}}.\left(v_{rci}+V_T\cdot\left(K_{bci}-K_{bcx}-\ln\frac{1+K_{bci}}{1+K_{bcx}}\right)\right) \quad (2.28)$$
$$K_{bci} = \sqrt{1+GAMM\cdot\exp\left(\frac{v_{bci}}{V_T}\right)}, K_{bcx} = \sqrt{1+GAMM\cdot\exp\left(\frac{v_{bcx}}{V_T}\right)}$$

where R_{ci} is the effective collector resistance in quasi-saturation, *HRCF* is known as high-current *RC* factor with a default value of 1000, *GAMM* is known as the epitaxial (Epi) doping parameter with a default value of 100×10^{-12}, and *Vo* is the epitaxial drift saturation voltage with a default value of 1.5 V [26]. The values used for *HRCF*, *GAMM*, and V_O are 1.0×10^{3}, 1.0×10^{-10}, and 5.0 V, respectively for the *npn* transistor [34]. The additional charge caused by quasi-saturation (base widening phenomena), influences the dynamic behavior of the transistor. This is covered by the parameter *QCO* (epitaxial charge parameter) which models the charge stored in the capacitors, C_{bcx} and C_{bcq}, of Fig. 2.3. Therefore, *QCO* affects the f_T modeling for the low V_{CE} in quasi-saturation. The K_{bcx} and K_{bci} in (2.28) are defined as [26]

$$Q_{bcx} = QCO\cdot K_{bcx}$$
$$Q_{bcq} = QCO\cdot K_{bci} \quad (2.29)$$

The default value of *QCO* for the *npn* transistor is 1.0×10^{-15} C [26]. The weak avalanche current in the base-collector junction is characterized by the model parameters, *AVC1* and *AVC2*, whose default values are reported as 0.15 V^{-1} and 20.0 V^{-1} [26]. However, the values for *AVC1* and *AVC2* are extrapolated for an accuracy from

the experimental data reported by Kloosterman [32], and found approximately 2.0 V^{-1} and 50.0 V^{-1} for the *npn* transistor, and 3.0 V^{-1} and 55.0 V^{-1} for the *pnp* transistor assuming the collector doping concentration of 5.0×10^{15} cm^{-3}.

The VBIC model has provision to split the base-emitter current into intrinsic and extrinsic through the model parameter, *WBE*. The default value of base distribution parameter, *WBE*, is 1.0 [34]. The parameter, *WBE*, also represents the partitioning of the base-emitter depletion capacitance between intrinsic and extrinsic components. The parameter, *IMELT*, is called the explosion current [38] and is used to help convergence and to prevent numerical problems. The default value of *IMELT* is 1 A [38].

The fixed overlap capacitances in the double poly bipolar process technology are calculated based on the following assumptions made in Table 2.7.

Table 2.7 Process Details for Overlap Capacitance Calculation.

Parameters	**Values**	**Units**
Si permittivity	1.04×10^{-12}	F/cm
SIO_2 permittivity	4.04×10^{-12}	F/cm
Thickness of oxide	1.0	μm
Base-emitter overlap area	0.25	μm^2
Base-collector overlap area	0.50	μm^2
Calculated C_{ov} per unit area	4.04×10^{-16}	$F/\mu m^2$

Since the overlap capacitance per unit area is 4.04×10^{-16} $F/\mu m^2$, the base-emitter, and base-collector overlap capacitances, *CBEO*, and *CBCO*, are 1.01×10^{-15} F and 2.02×10^{-15} F, respectively with overlap areas provided in Table 2.7.

2.3.3 Estimation of Self-heating Related Parameters

Fig. 2.6 shows the cross section and top view of the assumed SOI transistor structure. The transistor is assumed to be have an emitter area of 1 μm × 5 μm, and the tub is assumed to have the length of $L_{tub} = L_e + 4$ μm, width of $W_{tub} = W_e + 8$ μm, and depth of 5 μm [31] as shown in Fig. 2.6.

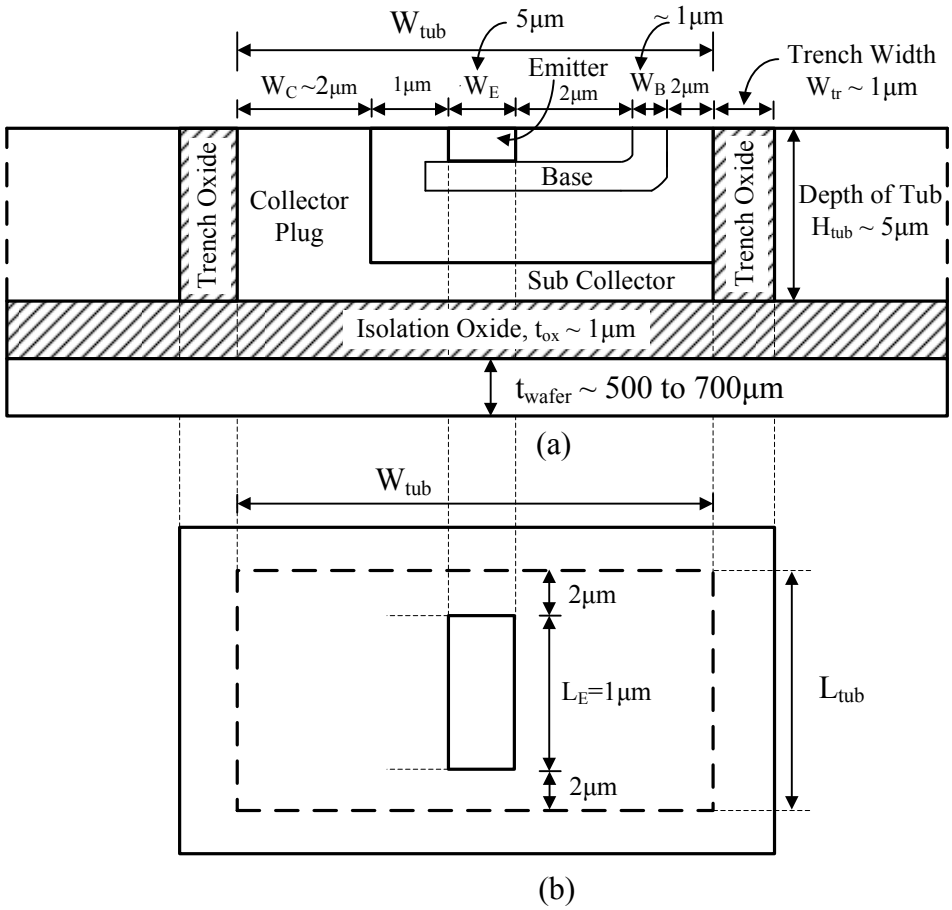


Figure 2.6 (a) Cross-section view (b) Top view of a typical SOI bipolar transistor [31].

The depth of the tub, H_{cell}, is composed of the depth of emitter, base width, collector depletion width at the reverse bias voltage and sub collector thickness. The collector thickness is determined by the breakdown voltage required for the technology or vice-

versa. The isolation oxide thickness, t_{ox}, is assumed to be 1.0 μm. The details of dimensions are provided in Table 2.8.

Table 2.8 Dimensions of the Tub of a Hypothetical Transistor [31].

Parameters	Values	Units
Emitter length, L_e	1.0	μm
Emitter width, W_e	5.0	μm
Minimum tub length, L_{tub}	5.0	μm
Minimum tub width, W_{tub}	13.0	μm
Minimum tub depth, H_{tub}	5.0	μm
Thickens of isolation oxide, t_{ox}	1.0	μm
Thermal conductivity of oxide, κ_{ox}	0.014	W/cm-K
Specific heat of oxide, C_{pox}	1.400	J/g-K
Density of SIO_2, d_{ox}	2.190	gm/cm^3

The thermal resistance, R_{th}, of the transistor structure shown in Fig 2.6 can be expressed as

$$R_{th} = \frac{t_{ox}}{\kappa_{ox} \cdot \left(2 \cdot \left(L_{tub} + W_{tub}\right) \cdot H_{tub} + L_{tub} \cdot W_{tub}\right)} \tag{2.30}$$

The thermal time constant, τ_{th}, is

$$\tau_{th} = R_{th} \cdot C_{th} = \frac{C_{pox} \cdot d_{ox} \cdot t_{ox}^2}{\kappa_{ox}} \tag{2.31}$$

The values of R_{th} and τ_{th} can be calculated using (2.30) and (2.31) and found to be 2915 K/Watt, and 2.19 μs respectively. The thermal capacitance can be calculated using (2.31) and found to be 7.51×10^{-10} Watt-sec/K. More complex relationships exist for multiple emitter and multiple base layouts, which can be used to reduce the value of thermal resistance, R_{th}.

2.3.4 Summary of the VBIC Models

2.3.4.1 VBIC Model for the SOI NPN Transistor

A summary of the VBIC model parameters for the *npn* transistor is provided in Table 2.9. These parameters are not meant to characterize any true proprietary specific SOI process technology.

Table 2.9 Physics Based VBIC Model Parameters for a Hypothetical *NPN* Transistor with an Emitter Area of 5.0 μm^2.

Paramters	**Values**	**Paramters**	**Values**	**Paramters**	**Values**	**Paramters**	**Values**
IS	5.45E-18	NCN	2.00	GAMM	1.00E-10	XVO	0
NF	1.00	VEF	78.00	QCO	1.00E-15	PS	1
NR	1.00	VER	2.50	RS	1.00E+07	MS	0
RBX	30.00	IKF	2.7E-03	FC	0.90	WBE	1
RCX	10.00	IKR	1.52E-02	AJC	-0.50	ISP	0
RBI	370.00	TF	4.42E-12	AJE	-0.50	WSP	1
RE	15.00	QTF	0.30	AJS	-0.50	NFP	1
CJC	1.0E-14	XTF	10.00	AVC1	2.00	IBEIP	0
CJEP	2.1E-15	VTF	2.50	AVC2	50.00	IBENP	0
PC	0.73	ITF	3.04E-03	NCNP	2.00	IBCIP	0
MC	2.5E-01	TR	1.77E-09	IKP	2.00E-04	NCIP	1
CJCP	5.0E-15	TD	7.72E-12	EAIE	1.12	IBCNP	0
CJE	4.70E-15	KFN	1.00E-09	EAIC	1.12	XRE	0
PE	0.93	AFN	2.00	EAIS	1.12	XRB	0
ME	3.3E-01	BFN	1.00	EANE	1.12	XRC	0
IBEI	4.66E-20	XIS	3.50	EANC	1.12	XRS	0
NEI	1.00	XII	1.70	EANS	1.12	TAVC	0
IBEN	7.50E-15	XIN	1.70	TNF	0.00	CTH	1.67E-09
NEN	2.00	EA	1.13	IMELT	1.00E+03	RTH	3.00E+03
IBCI	2.02E-18	RCI	100.00	RBP	1.00	SELFT	1
NCI	1.00	VO	5.00	CBEO	1.01E-16	TNOM	25
IBCN	5.97E-16	HRCF	1.00E+03	CBCO	2.02E-16		

The SPECTRE formatted VBIC model for the *npn* transistor is as follows.

.model npn vbic type=NPN

+IS=5.45E-18 NF=1.0 NR=1.0 RBX=30.0 RCX=10.0

+RCI=100.0 VO=5.0 GAMM=1.0E-10 HRCF=1.1E03 QCO=1.0E-15

+RBI=3.70E02 RE=15.0 RS=1.0E07 FC=9.0E-01 CJC=1.0E-14

+CJEP=2.1E-15 PC=0.73 MC=2.50E-01 AJC=-0.5 CJCP=5.0E-15

+CJE=4.70E-15 PE=0.93 ME=3.33E-01 AJE=-0.5 AJS=-0.5

+IBEI=4.66E-20 NEI=1.0 IBEN=7.50E-15 NEN=2.0 IBCI=2.02E-18

+NCI=1.0 NCN=2.0 IBCN=5.97E-16 AVC1=2.0 AVC2=50.0

+NCNP=2.0 VEF=78.0 VER=2.5 IKP=2.0E-04 IKF=2.73E-03

+IKR=1.52E-02 XTF=10.0 TF=4.42E-12 QTF=0.3 VTF=2.5

+ITF=3.04E-03 AFN=2.0 TR=1.77E-09 TD=7.72E-12 KFN=1.0E-09

+BFN=1.0 EA=1.13 EAIE=1.12 EAIC=1.12 EAIS=1.12

+EANE=1.12 EANC=1.12 EANS=1.12 XIS=3.50 XII=1.70

+XIN=1.7 TNF=0.0 IMELT=1.0E3 RBP=1.0 CBEO=1.01E-16

+CBCO=2.02E-16 XVO=0 PS=1.0 MS=0 WBE=1

+ISP=0.0 WSP=1.0 NFP=1.0 IBEIP=0.0 IBENP=0

+IBCIP=0 NCIP=1 IBCNP=0 XRE=0 XRB=0

+XRC=0 XRS=0 TAVC=0 SELFT=shx*1

+CTH=cthx*1.67E-09 RTH=rthx*3000.0 TNOM=25.0

The user defined variables, *shx*, *cthx*, and *rthx*, can be used to enable or disable the self-heating feature of the VBIC model and modulate the values of R_{th} and C_{th}.

2.3.4.2 VBIC Model for the SOI pnp transistor

A summary of the VBIC model parameters for the *pnp* transistor is provided in Table 2.10.

Table 2.10 Physics Based VBIC Model Parameters for a Hypothetical *PNP* Transistor with an Emitter Area of 5.0 μm^2.

Paramters	**Values**	**Paramters**	**Values**	**Paramters**	**Values**	**Paramters**	**Values**
IS	2.42E-18	NCN	2.00	GAMM	4.44E-11	XVO	0
NF	1.00	VEF	26.00	QCO	2.25E-15	PS	1
NR	1.00	VER	1.50	RS	1.00E+07	MS	0
RBX	13.33	IKF	1.2E-03	FC	0.90	WBE	1
RCX	22.50	IKR	6.75E-03	AJC	-0.50	ISP	0
RBI	164.44	TF	4.98E-12	AJE	-0.50	WSP	1
RE	33.75	QTF	0.30	AJS	-0.50	NFP	1
CJC	1.0E-14	XTF	22.50	AVC1	3.00	IBEIP	0
CJEP	2.1E-15	VTF	2.50	AVC2	55.00	IBENP	0
PC	0.73	ITF	1.35E-03	NCNP	2.00	IBCIP	0
MC	2.5E-01	TR	1.99E-09	IKP	2.00E-04	NCIP	1
CJCP	5.0E-15	TD	8.68E-12	EAIE	1.12	IBCNP	0
CJE	4.70E-15	KFN	6.26E-10	EAIC	1.12	XRE	0
PE	0.93	AFN	2.00	EAIS	1.12	XRB	0
ME	3.3E-01	BFN	1.00	EANE	1.12	XRC	0
IBEI	3.76E-20	XIS	3.15	EANC	1.12	XRS	0
NEI	1.00	XII	0.76	EANS	1.12	TAVC	0
IBEN	7.50E-15	XIN	0.76	TNF	0.00	CTH	1.67E-09
NEN	2.00	EA	1.13	IMELT	1.00E+03	RTH	3.00E+03
IBCI	8.97E-19	RCI	225.00	RBP	1.00	SELFT	1
NCI	1.00	VO	2.22	CBEO	1.01E-16	TNOM	25
IBCN	5.97E-16	HRCF	1.00E+03	CBCO	2.02E-16		

A portion of the SPECTRE formatted VBIC model for the *pnp* transistor is as follows.

.model pnp PNP struct=vertical

+IS=2.42E-18 NF=1.0 NR=1.0 RBX=13.33 RCX=22.50

+RBI=164.4 RE=33.75 CJC=1.0E-14 CJEP=2.1E-15 PC=0.73

.

+CTH=cthx*1.67E-09 RTH=rthx*3000.0 TNOM=25.00

2.4 Validation of Models through CAD Simulations

2.4.1 Beta and f_T versus I_C for the NPN Transistor

The forward dc beta, β_F, and forward transit time, f_T, versus the collector current, I_C, are shown in Figs. 2.7 and 2.8 respectively using the SPECTRE simulator in Virtuoso Analog Design Environment. The details are provided in Table 2.11.

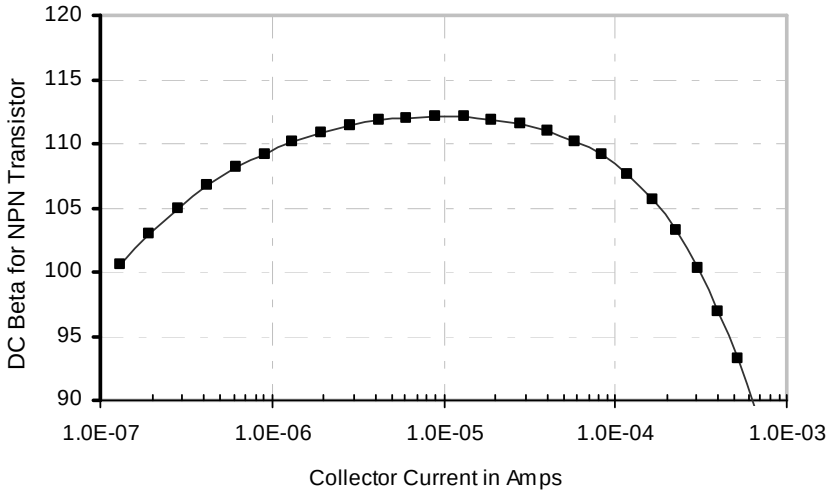


Figure 2.7 Simulation of β_F versus I_C for the *npn* transistor using SGP model of Table 2.4 with an emitter area of 5.0 μm^2.

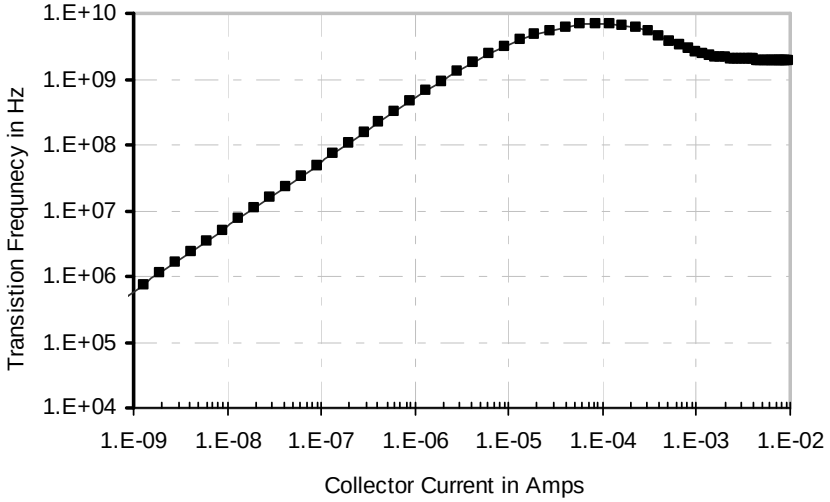


Figure 2.8 Simulation of f_T versus I_C for the *npn* transistor using SGP model of Table 2.4 with an emitter area of 5.0 μm^2.

Table 2.11 Simulation Data for β_F and f_T over the V_{BE} for the *NPN* Transistor Using the SGP Model Parameters of Table 2.4 with an Emitter Area of 5.0 μm^2.

V_{BE} in V	I_C in Amp	Beta (β_F)	f_T in Hz
0.61	1.32×10^{-07}	100.6	7.2×10^{07}
0.62	1.94×10^{-07}	103.0	1.0×10^{08}
0.63	2.85×10^{-07}	105.0	1.5×10^{08}
0.64	4.19×10^{-07}	106.7	2.2×10^{08}
0.65	6.15×10^{-07}	108.1	3.2×10^{08}
0.66	9.03×10^{-07}	109.2	4.6×10^{08}
0.67	1.33×10^{-06}	110.1	6.6×10^{08}
0.68	1.94×10^{-06}	110.9	9.3×10^{08}
0.69	2.85×10^{-06}	111.4	1.3×10^{09}
0.70	4.18×10^{-06}	111.8	1.8×10^{09}
0.71	6.13×10^{-06}	112.0	2.4×10^{09}
0.72	8.98×10^{-06}	112.1	3.1×10^{09}
0.73	$\mathbf{1.31 \times 10^{-05}}$	**112.1**	$\mathbf{3.9 \times 10^{09}}$
0.74	1.91×10^{-05}	111.9	4.8×10^{09}
0.75	2.79×10^{-05}	111.6	5.6×10^{09}
0.76	4.03×10^{-05}	111.0	6.3×10^{09}
0.77	5.81×10^{-05}	110.2	6.8×10^{09}
0.78	$\mathbf{8.30 \times 10^{-05}}$	**109.1**	$\mathbf{7.0 \times 10^{09}}$
0.79	1.17×10^{-04}	107.6	7.0×10^{09}
0.80	1.64×10^{-04}	105.7	6.7×10^{09}
0.81	2.25×10^{-04}	103.3	6.0×10^{09}
0.82	3.03×10^{-04}	100.3	5.3×10^{09}
0.83	4.01×10^{-04}	97.0	4.5×10^{09}
0.84	5.18×10^{-04}	93.2	3.9×10^{09}
0.85	6.54×10^{-04}	89.1	3.3×10^{09}

The maximum value of the forward dc beta, β_F, occurs at V_{BE} = 0.730 V and I_C = 13.1 μA while the maximum transition frequency, f_T, occurs at V_{BE} = 0.780 V and I_C = 83.0 μA as illustrated in Figs. 2.7, 2.8, and Table 2.11. The best combination of β_F and f_T can be found with the base-emitter voltage in the range of 0.73 V and 0.78 V.

2.4.2 Beta and f_T versus I_C for the PNP Transistor

The forward dc beta, β_F, and forward transit time, f_T, versus the collector current, I_C, response are shown in Figs. 2.9 and 2.10 using the SPECTRE simulator in Virtuoso Analog Design Environment. The details are provided in Table 2.11.

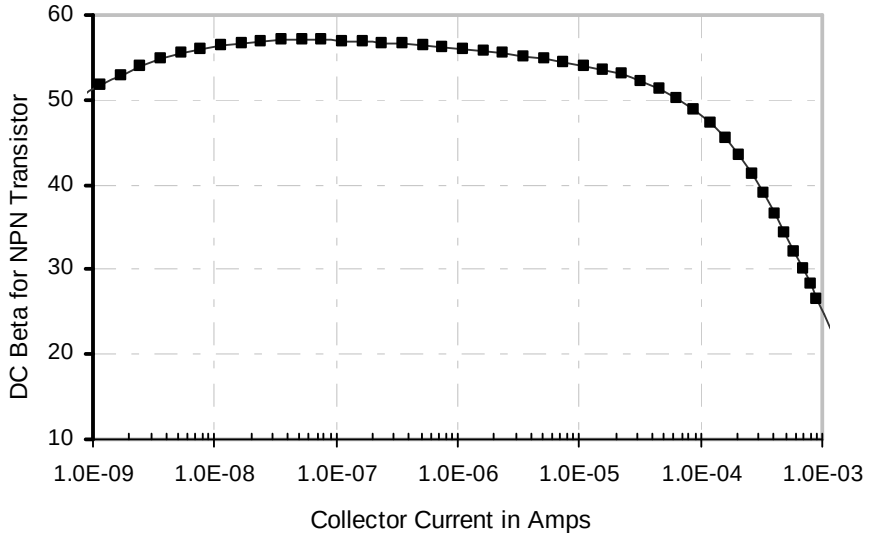


Figure 2.9 Simulation of β_F versus I_C for the *pnp* transistor using SGP model of Table 2.5 with an emitter area of 5.0 μm^2.

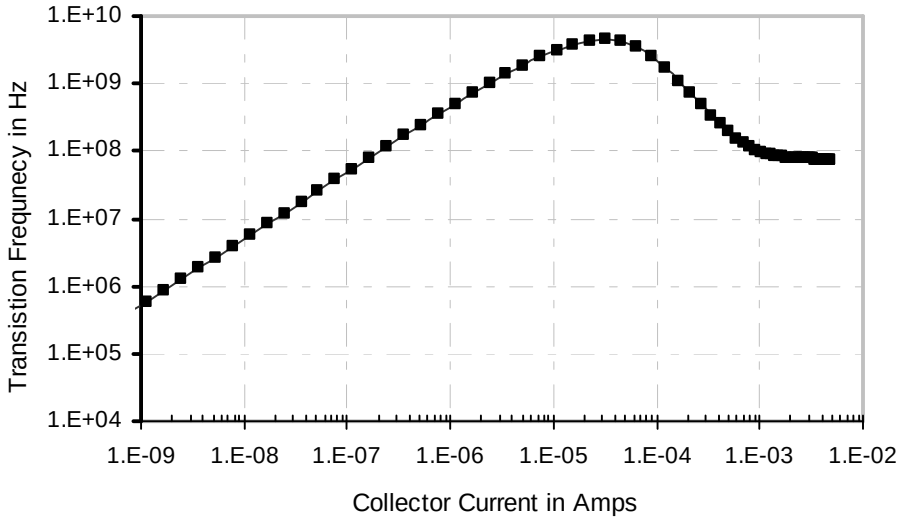


Figure 2.10 Simulation of f_T versus I_C for the *pnp* transistor using SGP model of Table 2.5 with an emitter area of 5.0 μm^2.

Table 2.12 Simulation Data for β_F and f_T over the V_{BE} for the *PNP* Transistor Using the SGP Model Parameters of Table 2.5 with an Emitter Area of 5.0 μm^2.

V_{BE} in V	**I_C in Amp**	**Beta (β_F)**	**f_T in Hz**
0.60	3.60×10^{-08}	57.0	1.8×10^{07}
0.61	5.27×10^{-08}	57.1	2.6×10^{07}
0.62	**7.72×10^{-08}**	**57.1**	**3.8×10^{07}**
0.63	1.13×10^{-07}	57.0	5.5×10^{07}
0.64	1.66×10^{-07}	56.9	8.0×10^{07}
0.65	2.43×10^{-07}	56.7	1.2×10^{08}
0.66	3.56×10^{-07}	56.6	1.7×10^{08}
0.67	5.22×10^{-07}	56.4	2.4×10^{08}
0.68	7.64×10^{-07}	56.2	3.5×10^{08}
0.69	1.12×10^{-06}	55.9	5.0×10^{08}
0.70	1.64×10^{-06}	55.7	7.1×10^{08}
0.71	2.40×10^{-06}	55.4	1.0×10^{09}
0.72	3.50×10^{-06}	55.2	1.4×10^{09}
0.73	5.11×10^{-06}	54.8	1.9×10^{09}
0.74	7.44×10^{-06}	54.5	2.5×10^{09}
0.75	1.08×10^{-06}	54.1	3.1×10^{09}
0.76	1.57×10^{-56}	53.6	3.8×10^{09}
0.77	2.26×10^{-05}	53.0	4.3×10^{09}
0.78	**3.23×10^{-05}**	**52.3**	**4.5×10^{09}**
0.79	4.58×10^{-05}	51.4	4.2×10^{09}
0.80	6.42×10^{-05}	50.2	3.5×10^{09}

The maximum value of the forward dc beta, β_F, occurs at V_{BE} = 0.680 *V* and I_C = 0.764 μA while the maximum transition frequency, f_T, occurs at V_{BE} = 0.780 V and I_C = 32.3 μA as illustrated in Figs. 2.9, 2.10, and Table 2.12. The best combination of β_F and f_T can be found with the base-emitter voltage in the range of 0.74 V and 0.8 V.

2.5 Summary

The SGP and VBIC model parameters for both the *npn* and *pnp* transistors are estimated using device physics formulations and extensive literature review. The functionality of the transistors has been validated through the basic simulations using the SPECTRE simulator. These analytical models can be used in the absence of the public-domain SOI bipolar transistor models. These models will be extensively used in the rest of the chapters for the analysis and simulation of the self-heating thermal effects in current mirrors and current-feedback amplifiers. The model parameters reported in this document are not extracted from any true device measurement data.

CHAPTER 3

MODELING AND CHARACTERIZATION OF THE EFFECTS OF SELF-HEATING ON AN SOI BIPOLAR TRANSISTOR

This chapter provides an approach to the modeling of the thermal effect of self-heating in a silicon-on-insulator (SOI) bipolar process technology. As illustrated in chapter one, the strong dependency of collector current on temperature necessitates the modeling of the non-ideal effects induced by self-heating. This chapter examines the influence of the static and dynamic electrothermal behavior of an SOI bipolar transistor. In particular, the effect of static and dynamic self-heating on the bipolar transistor in the common-emitter (*CE*) configuration will be investigated, and an analytical formulation will be developed to model the thermally induced errors. The effect of the emitter degeneration on self-heating will also be investigated.

First, the large-signal output characteristics of a device will be examined to assess the nature of thermal effects induced by the static self-heating. This will be followed by the examination of the frequency-domain effects of dynamic self-heating on the small-signal characteristics of a device. A general overview on the class of analog circuits which are impacted severely by self-heating will be presented. Different circuit level optimization techniques to minimize the effect of self-heating will be explored. Finally, an approach to model the effect of dynamic self heating on the noise performance of the bipolar transistor will be presented.

The analytical formulations provided in this chapter serve as a foundation to forecast the thermally induced effects in more complex analog circuits, using SOI bipolar transistors.

3.1 Modeling Thermal Effects of Self-Heating

3.1.1 Static Self-Heating

The elevation of the temperature of a transistor due to its own power dissipation is called self-heating. As a result, the collector current of the bipolar transistor increases beyond what would have been obtained without the effect of self-heating. Under dc bias, the static self-heating can be represented by an electrothermal coupled model [6]-[7] illustrated in Fig. 3.1.

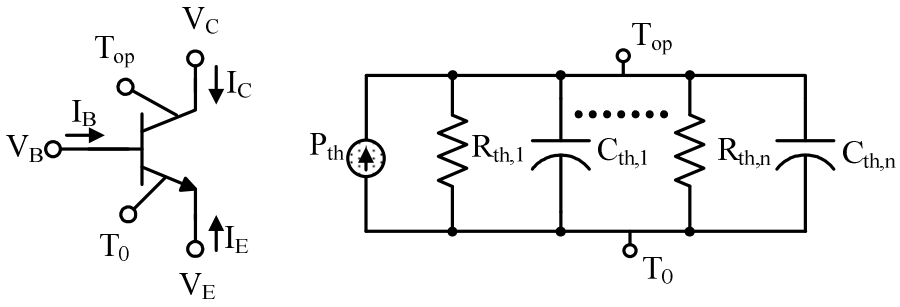


Figure 3.1 Electrothermal model for an SOI BJT.

The variables $I_B(V_B, T_{op})$, $I_C(V_B,V_C, T_{op})$, $P_{th} = I_BV_{BE}+I_CV_{CE}$, T_0, and T_{op} are the large-signal base current, large-signal collector current, static power dissipation in the device, circuit ambient temperature, and device operating temperature, respectively. For the SOI bipolar transistor, the operating temperature, T_{OP}, is always higher than ambient temperature because of self-heating. The total thermal spreading impedance, $Z_{th}(s)$, of

the SOI bipolar transistor can be modeled with a multi-pole function, and can be expressed as [19]

$$Z_{th}(s) = \frac{R_{th,1}}{1 + sR_{th,1}C_{th,1}} + \cdots\cdots + \frac{R_{th,n}}{1 + sR_{th,n}C_{th,n}} \tag{3.1}$$

where $R_{th,i}$ and $C_{th,i}$ are the thermal resistances and thermal capacitances of different parts of the device structure. The thermal impedance in (3.1) can also be approximated with a single pole-function, without sacrificing much accuracy, as [4]

$$Z_{th}(s) = \frac{R_{th}}{1 + sR_{th}C_{th}} \tag{3.2}$$

The expression (3.2) can be identified as the first-order low-pass filter transfer function with the thermal cutoff frequency defined as

$$f_{th} = \frac{1}{2\pi \cdot R_{th}C_{th}} \tag{3.3}$$

Many studies over the years [3]-[6], [19] have shown that the operating temperature of a device can be elevated due to the thermal influence of self-heating, and can be expressed as

$$T_{op} = T_0 + P_{th} \cdot \mathrm{Re}\left(Z_{th}(s)\right) \tag{3.4}$$

In another formulation, the total change in temperature change of a device due to self-heating can be expressed as [40]

$$\Delta T = \Delta T_0 + R_{th} \cdot \Delta P_{th} = \Delta T_0 + R_{th} \cdot \left(I_C \Delta V_C + V_C \Delta I_C\right) \tag{3.5}$$

where ΔT_0, and ΔP_{th}, are the change in ambient temperature, and the change in static power dissipation, respectively. As explained in chapter 1, the collector current and the

base-emitter voltage are very sensitive to electro-thermal effects [19]. Depending on the nature of the input excitation signals to the device, self-heating can be categorized into two types – static self-heating or dc self-heating and dynamic self-heating or ac self-heating. As an example, a circuit under small-signal excitation will be influenced by both static and dynamic self-heating. All of the dc biased circuits are affected by static self-heating through (3.4) and (3.5).

3.1.2 Small-Signal Electro-Thermal Model

The small variation of the electrical signal during the small-signal operation causes an instantaneous change in the power dissipation, and hence in the device temperature. The instantaneous variation of temperature with the applied input excitation, in turn, influences the input and output currents, and hence the parameters of the two-port network or hybrid-π network. This models now the small-signal operation of the bipolar transistor [4]. These parameters, therefore, are affected not only by dc self-heating, but also by dynamic self-heating. Dynamic self-heating is a frequency-dependent phenomenon. To model the electro-thermal interaction, the small-signal hybrid- π model shown in Fig. 3.2 can be used.

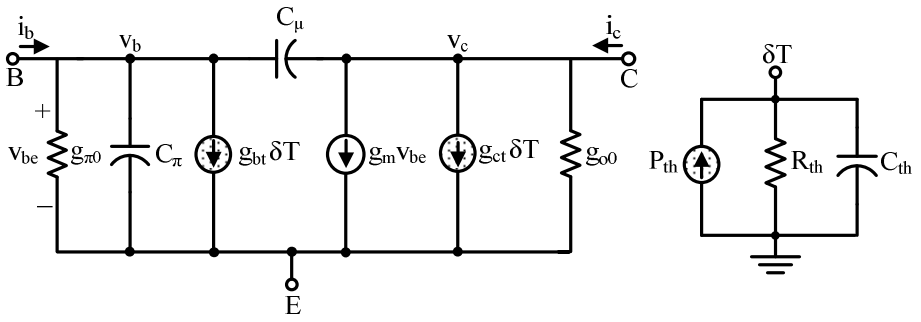


Figure 3.2 BJT equivalent small-signal equivalent circuit with self-heating model.

This model is considered as a consistent electrical-thermal coupled model [12]. The current source, P_{th}, of magnitude equal to the instantaneous power dissipation in the electrical network drives an equivalent electrical circuit (*RC* network approximations) of the thermal network in the SOI bipolar transistor. This rise in temperature is then fedback to the intrinsic electrical network. This perturbs the state of the circuit incrementally and this introduces the concept of "dynamic self-heating". The thermal contribution of dynamic self-heating can be modeled through the two current sources, $g_{bt}\delta T$ at the base and $g_{bt}\delta T$ at the collector as shown in Fig. 3.2 [12]. The terms g_{ct} and g_{bt} are defined as collector and base "thermal transconductances" [12]-[13].

3.2 Modeling the Effect of Dynamic Self-Heating

Two-port interconnection [47] shown in Fig 3.3 can be used to model the effect of dynamics self-heating in a transistor.

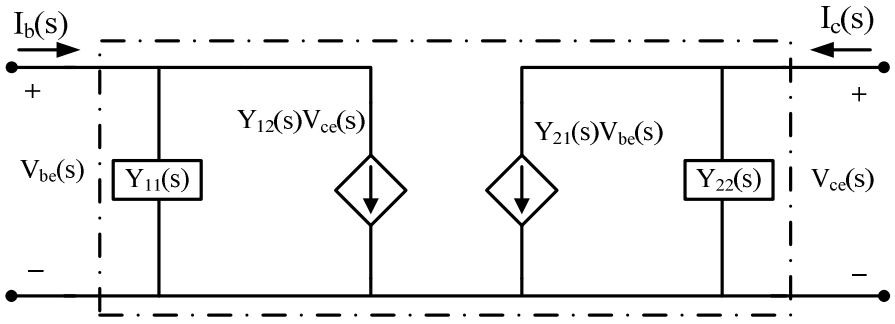


Figure 3.3 Admittance parameters, two-port equivalent circuit.

The terminal voltages and currents can be represented using an admittance matrix as

$$\begin{bmatrix} I_b(s) \\ I_c(s) \end{bmatrix} = \begin{bmatrix} Y_{11}(s) & Y_{12}(s) \\ Y_{21}(s) & Y_{22}(s) \end{bmatrix} \begin{bmatrix} V_{be}(s) \\ V_{ce}(s) \end{bmatrix} \tag{3.6}$$

The very first analysis of dynamic self-heating was reported by Müller [41] and later it was adopted by many authors [5], [6]. According to Müller's model, the two-port short-circuit admittance parameters for the bipolar transistor in the *CE* configuration including the effect of self-heating can be expressed as [6], [41]

$$Y_{mn} = \frac{Y_{mn0} + D_m Z_{th} I_m I_n}{1 - D_m Z_{th} P_{th}} \tag{3.7}$$

where m or n = 1 for the base or 2 for the collector, Y_{mn0} is intrinsic device Y-parameters without the effect of self-heating. From the analysis of (3.7), thermal feedback can be considered as shunt-shunt feedback (voltage sampling, current comparing). This implies thermal feedback reduces both input and output impedances. However, this formulation is based on constant current gain, which is no longer true for the modern dielectrically isolated bipolar process technology [4].

3.2.1 Analytical Formulations of the Admittance Parameters

The small-signal equivalent circuit for a bipolar transistor including the effect of self-heating can be represented as shown in Fig. 3.4.

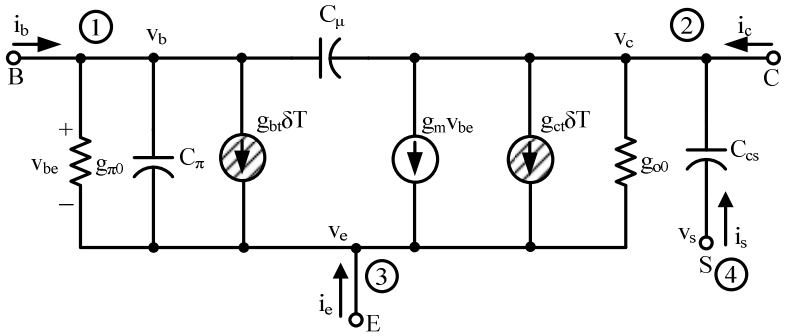


Figure 3.4 Small-signal equivalent circuit for the *npn* transistor with self-heating.

The terminal currents and voltages of the circuit in Fig. 3.4 can be related through a primitive indefinite-admittance matrix as [43]

$$\begin{bmatrix} i_b \\ i_c \\ i_e \\ i_s \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} & y_{13} & y_{14} \\ y_{21} & y_{22} & y_{23} & y_{24} \\ y_{31} & y_{32} & y_{33} & y_{34} \\ y_{41} & y_{42} & y_{43} & y_{44} \end{bmatrix} \begin{bmatrix} v_b \\ v_c \\ v_e \\ v_s \end{bmatrix} + \begin{bmatrix} i_{bs} \\ i_{cs} \\ i_{es} \\ i_{ss} \end{bmatrix} \tag{3.8}$$

where y_{ij} is the small signal admittance parameter and i_{is} is the short-circuit current at the ith terminal when all the terminals are short-circuited to ground. Following the approach (see Appendix B) discussed by Chen [43], equation (3.8) can be expressed as

$$\begin{bmatrix} \mathrm{i_b} \\ i_c \\ i_e \\ i_s \end{bmatrix} = \begin{bmatrix} \mathrm{g}_{\pi 0} + s(C_\pi + C_\mu) & -\mathrm{s}C_\mu & -(\mathrm{g}_{\pi 0} + sC_\pi) & 0 \\ \mathrm{g_m} - \mathrm{s}C_\mu & \mathrm{g}_{o0} + \mathrm{s}(C_\mu + \mathrm{C_{cs}}) & -(g_m + g_{o0}) & -\mathrm{sC_{cs}} \\ -(\mathrm{g_m} + \mathrm{g}_{\pi 0} + sC_\pi) & -\mathrm{g}_{o0} & g_m + g_{o0} + \mathrm{g}_{\pi 0} + sC_\pi & 0 \\ 0 & -\mathrm{sC_{cs}} & 0 & \mathrm{sC_{cs}} \end{bmatrix} \begin{bmatrix} \mathrm{v_b} \\ v_c \\ v_e \\ v_s \end{bmatrix} + \begin{bmatrix} \mathrm{g_{bt}} \\ \mathrm{g_{ct}} \\ -(\mathrm{g_{ct}} + \mathrm{g_{bt}}) \\ 0 \end{bmatrix} \delta T \tag{3.9}$$

To solve (3.9), it is critical to represent the small-signal change in temperature, δT, in terms of terminal voltages and currents in a consistent manner. An equivalent small-signal circuit representation of a transistor in the common-emitter configuration is shown in Fig. 3.5 including the effects of dynamic self-heating in each of the circuit's element.

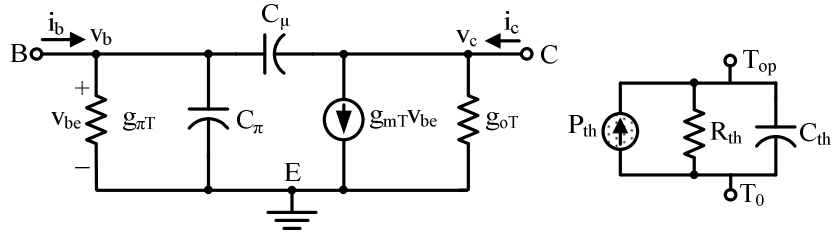


Figure 3.5 BJT small-signal equivalent circuit with self-heating model in the common-emitter configuration.

The effective transconductance, g_{mT}, output conductance, g_{oT}, and input conductance, $g_{\pi T}$, of Fig. 3.5 can be expressed using the theorem of partial differentiation [42] as

$$g_{mT} = \frac{dI_C}{dV_{BE}} = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{T=T_{OP}} + \frac{\partial I_C}{\partial T}\frac{dT}{dV_{BE}} = g_{m0} + g_{m\_th} \tag{3.10}$$

$$g_{oT} = \frac{dI_C}{dV_{CE}} = \left.\frac{\partial I_C}{\partial V_{CE}}\right|_{T=T_{OP}} + \frac{\partial I_C}{\partial T}\frac{dT}{dV_{CE}} = g_{o0} + g_{o\_th} \tag{3.11}$$

$$g_{\pi T} = \frac{dI_B}{dV_{BE}} = \left.\frac{\partial I_B}{\partial V_{BE}}\right|_{T=T_{OP}} + \frac{\partial I_B}{\partial T}\frac{dT}{dV_{BE}} = g_{\pi 0} + g_{\pi\_th} \tag{3.12}$$

where the terms g_{m0}, g_{o0}, and $g_{\pi 0}$ in (3.10)-(3.12) represent the intrinsic device transconductance, output conductance and input conductance, respectively, but at elevated average temperature dictated by (3.4) through static self-heating due to bias voltages and currents. The terms g_{m_th}, g_{o_th}, and g_{π_th} in (3.10)-(3.12) represent dynamic self-heating induced transconductance, output conductance, and input conductance, respectively due to the small-signal change in temperature. These terms can be evaluated as

$$g_{m\_th} = \frac{\partial I_C}{\partial T}\frac{dT}{dV_{BE}} = \frac{\partial I_C}{\partial T}\frac{dP_i}{dV_{BE}}Z_{th} = g_{ct}g_{pbe}Z_{th} \tag{3.13}$$

$$g_{o\_th} = \frac{\partial I_C}{\partial T}\frac{dT}{dV_{CE}} = \frac{\partial I_C}{\partial T}\frac{dP_i}{dV_{CE}}Z_{th} = g_{ct}g_{pce}Z_{th} \tag{3.14}$$

$$g_{\pi\_th} = \frac{\partial I_B}{\partial T}\frac{dT}{dV_{BE}} = \frac{\partial I_B}{\partial T}\frac{dP_i}{dV_{BE}}Z_{th} = g_{bt}g_{pbe}Z_{th} \tag{3.15}$$

The terms g_{ct} and g_{bt} in (3.13)-(3.15) are the collector and base "thermal transconductances" [10]-[13]. The instantaneous power dissipated in the bipolar transistor is P_i. The terms g_{pce} and g_{pbe} represent the change in device power dissipation with a change in the collector and base bias voltages, and can be calculated as [19]

$$g_{pce} = \frac{dP_i}{dV_{CE}} = I_c + V_{ce}\frac{dI_c}{dV_{CE}} = \left(I_c + g_{oT}V_c\right) \tag{3.16}$$

$$g_{pbe} = \frac{dP_i}{dV_{BE}} = I_b + V_b\frac{dI_b}{dV_{BE}} + I_c\frac{dV_{ce}}{dV_{BE}} + V_c\frac{dI_c}{dV_{BE}} = \left(I_b + g_{\pi T}V_{be} + g_{mT}V_c\right) \tag{3.17}$$

Thus, the effective conductance parameters for the hybrid-π model in Fig. 3.5 can be expressed using (3.13)-(3.17) into (3.10)-(3.12) as

$$g_{mT} = \frac{g_{m0} + g_{ct}\cdot\left(I_b + g_{\pi T}V_b\right)\cdot Z_{th}}{1 - g_{ct}V_cZ_{th}} \tag{3.18}$$

$$g_{oT} = \frac{g_{o0} + g_{ct}I_cZ_{th}}{1 - g_{ct}V_cZ_{th}} \tag{3.19}$$

$$g_{\pi T} = \frac{g_{\pi 0} + g_{bt}\cdot\left(I_b + g_{mT}V_c\right)\cdot Z_{th}}{1 - g_{bt}V_bZ_{th}} \tag{3.20}$$

From the analysis, it can be inferred that the three additional terms introduced in (3.13)-(3.15) by the dynamic self-heating will disappear beyond the thermal cutoff frequency, f_{th}, as defined by (3.3) because the thermal spreading impedance, Z_{th}, represents a low-pass filter [4] as shown in Fig. 3.5. Electrically and thermally induced conductances are separated from each other and are shown in Fig. 3.6. As the frequency goes up, the thermally induced component of the overall conductance will disappear and the effective conductance becomes electrical only. Due to the thermal inertia of the

substrate and package, which is modeled by thermal capacitances, the temperature cannot follow the high frequency ac signal, and remains constant at the value determined by the static power dissipation.

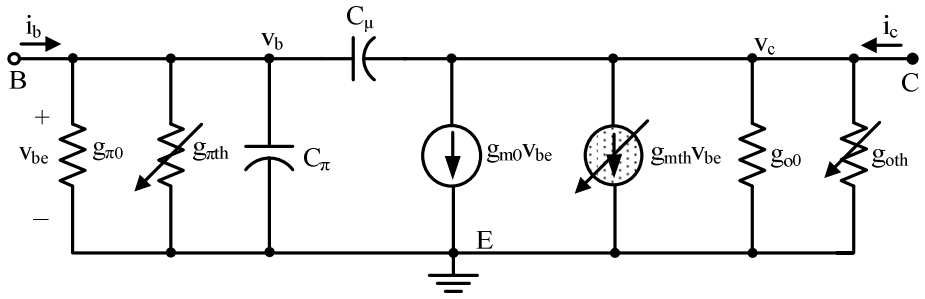


Figure 3.6 Equivalent electrical network with the intrinsic device parameters and thermally induced parameters separated.

As a consequence, dynamic self-heating gets suppressed at frequencies above the thermal cutoff frequency [4], [19]. Thus, the thermal effect of self-heating is a low frequency phenomenon.

As mentioned earlier, the small-signal change in temperature, δT, needs to be expressed in terms of the small-signal base and collector voltages as shown in Fig. 3.7 to solve the matrix (3.9). For this, the overall effects of dynamic self-heating can be lumped into a temperature controlled current sources $g_{bt}\delta T$ at the base, and $g_{ct}\delta T$ at the collector [12], [13] as shown in Fig. 3.7.

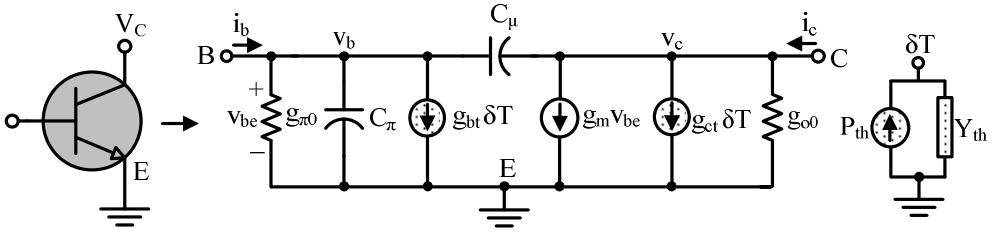


Figure 3.7 Small-signal equivalent circuit for an SOI BJT, including the self-heating model. Thermal admittance is $Y_{th} = 1/R_{th} + sC_{th}$.

This model of Fig. 3.7 can clearly capture the changes in the base and collector currents due to the small-signal changes in temperature at low frequencies. The temperature variation, δT, can be expressed in terms of the small signal base and collector voltages, v_b and v_c, as shown in Fig. 3.7 using McAndrew's concept [12], that states that the current source, P_{th}, should be the explicit function of the branch voltages and branch currents of the dissipative elements of the equivalent electrical network and an implicit function of temperature. Thus, the power conservation principle ensures that the incremental power in the thermal network is equal to the sum of the incremental power dissipation in the equivalent small-signal circuit. This can be expressed for the circuit of Fig. 3.7 using (3.16) and (3.17) as

$$Y_{th}\delta T = \left(I_b + g_{\pi T}V_b + g_{mT}V_c\right)\cdot v_b + \left(I_c + g_{oT}V_c\right)\cdot v_c + \left(g_{bt}V_b + g_{ct}V_c\right)\cdot \delta T \tag{3.21}$$

Equation (3.121) can be simplified and represented in a matrix form as

$$\left[\delta T\right] = \begin{bmatrix} \dfrac{\left(I_b + g_{\pi T}V_b + g_{mT}V\right)}{Y_{th} - \left(g_{ct}V_c + g_{bt}V_b\right)} & \dfrac{\left(I_c + g_{oT}V_c\right)}{Y_{th} - \left(g_{ct}V_c + g_{bt}V_b\right)} \end{bmatrix} \begin{bmatrix} v_b \\ v_c \end{bmatrix} \tag{3.22}$$

This result is similar to the result reported by Sham [13] with a subtle difference. The device intrinsic conductance was used in [13] instead of the effective dc conductances given by (3.18)-(3.20).

The indefinite-admittance matrix of (3.9) can be reduced to (3.23) for the *CE* configuration by contracting the terminals 3 and 4 of Fig. 3.4, and then set to ground.

$$\begin{bmatrix} i_b \\ i_c \end{bmatrix} = \begin{bmatrix} g_{\pi 0} + s(C_\pi + C_\mu) & -sC_\mu & g_{bt} \\ g_m - sC_\mu & g_{o0} + s(C_\mu + C_{cs}) & g_{ct} \end{bmatrix} \begin{bmatrix} v_b \\ v_c \\ \delta T \end{bmatrix} \tag{3.23}$$

The output admittance can be derived using (3.22) into (3.23) as

$$Y_{22}(s) = \left[g_{o0} + s\left(C_{\mu} + C_{cs}\right)\right] + \left[\frac{g_{ct} \cdot \left(I_c + g_{oT} V_c\right)}{Y_{th} - \left(g_{ct} V_c + g_{bt} V_b\right)}\right] \tag{3.24}$$
$$= y_{\text{intrinsic}} + y_{\text{thermal}}$$

A complete derivation of (3.24) can be found in Appendix B. It can be inferred from (3.24) that the output admittance has two parts – thermally induced component ($y_{thermal}$) and electrical only component ($y_{intrisic}$). The thermally induced component will be suppressed at high frequency due to the low-pass nature of thermal impedance. Thus, the behavior of the output admittance will be governed by the electrical only component – $y_{intrinsic}$ at high frequency.

3.2.2 Effect of Dynamic Self-Heating on Output Resistance

The output impedance of the bipolar transistor in the *CE* configuration including the effects of dynamic self-heating can be expressed using (3.24) as

$$Z_o(s) \overset{\Delta}{=} \frac{1}{Y_{22}(s)} = \frac{\dfrac{1}{g_{o0} + X_g R_{th} / \left(1 - MR_{th}\right)} \left(1 + \dfrac{s}{\left(1 - MR_{th}\right) / R_{th} C_{th}}\right)}{\dfrac{R_{th} C_{th} C_{eq}}{g_{o0}\left(1 - MR_{th}\right) + X_g R_{th}} s^2 + \dfrac{R_{th} C_{th} g_{o0} + C_{eq}\left(1 - MR_{th}\right)}{g_{o0}\left(1 - MR_{th}\right) + X_g R_{th}} s + 1} \tag{3.25}$$

where $M = g_{ct}V_c + g_{bt}V_b$, $X_g = g_{ct}(I_c + g_{oT}V_c)$ and $C_{eq} = C_{\mu} + C_{cs}$. A complete derivation of (3.25) can also be found in Appendix B. Assuming $X_g R_{th} >> g_{o0}(1 - MR_{th})$ and $R_{th}C_{th}g_{o0} >> C_{eq}(1 - MR_{th})$, equation (3.25) can be simplified to give a zero and two poles

$$f_z = \left(1 - MR_{th}\right) \cdot f_{th} \tag{3.26}$$

$$p_{1,2} = \frac{-g_{o0} \pm \sqrt{g_{o0}^2 - \dfrac{4 X_g C_{eq}}{C_{th}}}}{2 C_{eq}} \tag{3.27}$$

The zero may be close to the thermal cutoff frequency depending on the values of M, which is dictated by the bias voltages, and the two poles can be real only when $g_{o0}^2 > 4X_g C_{eq}/C_{th}$. This is in general true for a higher value of thermal resistance. Assuming that $\left(g_{o0}^2 - \frac{4X_g C_{eq}}{C_{th}}\right) << g_{o0}$, it can be inferred from (3.27) that the poles are very close to the intrinsic pole of the device, g_{o0}/C_{eq}. The small-signal output resistance at the collector of the bipolar transistor can be obtained from (3.25) by letting s = 0 as

$$r_o = \frac{1}{g_{o0} + \frac{g_{ct}\cdot(I_c + g_{oT}V_c)\cdot R_{th}}{1-(g_{ct}V_c + g_{bt}V_b)\cdot R_{th}}} \tag{3.28}$$

This shows that the output resistance may be reduced either by increasing the value of thermal resistance or by increasing the power dissipation of device with the higher value of bias voltages and currents.

3.2.3 Effect of Dynamic Self-Heating on Voltage Gain

The low-frequency voltage gain of the *CE* amplifier is given by

$$A_V(s) = g_m \cdot r_o \tag{3.29}$$

where g_m and r_o are the transconductance and output resistance of the transistor. The transconductance can be defined as

$$g_m = \frac{I_C}{\eta V_T} \tag{3.30}$$

As seen from (3.28) and (3.30), the output resistance, r_o, and the transconductance, g_m, are affected by self heating, and hence the voltage gain of an amplifier will be affected by self-heating as well.

3.3 Basic Thermal Simulations and Characterization

3.3.1 Thermal Effects of Static Self-Heating

Figure 3.8 shows a simulation setup to simulate the effect of static self-heating. The "dt" node is used to observe the rise in temperature. A resistor of 1 MΩ is used to mimic the open circuit at the node "dt". The dc simulation result is also shown in Fig. 3.8. The simulation was done using the VBIC model provided in Table 2.9.

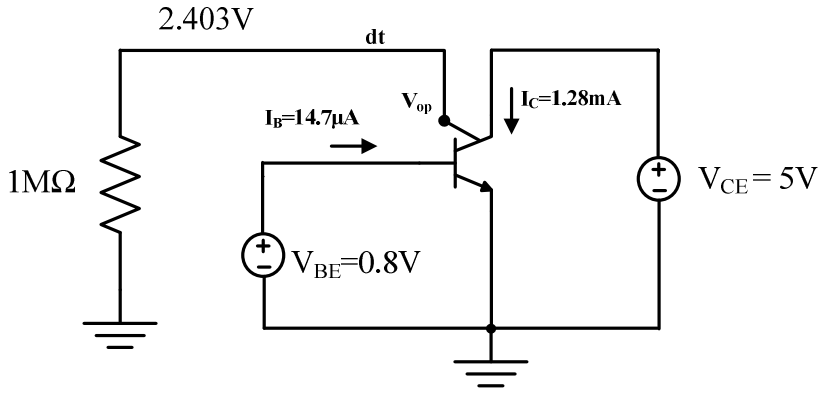


Figure 3.8 Setup to simulate rise in temperature due to self-heating using the VBIC model of Table 2.9, with an emitter area of 40 μm^2.

The calculated power dissipation is 1.28mA·5V + 14.77μA·0.8V = 6.41 mW, and thermal resistance of 8x devices (with an emitter area of 40 μm^2) device is 3000/8 = 375 K/W [31]. The overall rise in temperature is 2.404 K, which is close to the simulated data shown in Fig. 3.8. As a consequence of the rise in device temperature, one of most critical parameters, the collector current, I_C, of the bipolar transistor, and all other related small-signal parameters will be affected. The temperate dependence of the collector is derived in chapter 1 and is repeated here for convenience as

$$I_C(T) = \frac{C_t}{Q_B} \cdot T^{4-m} \exp\left(-\frac{V_{G0}}{V_T}\right) \exp\left(\frac{V_{BE}(T)}{V_T}\right) \cdot \left(1 + \frac{V_{CE}}{V_A}\right) \tag{3.31}$$

The simulation shown in Fig 3.9 shows the effect of static self-heating on the collector current of the *npn* bipolar transistor. This confirms that the collector current increases with self-heating.

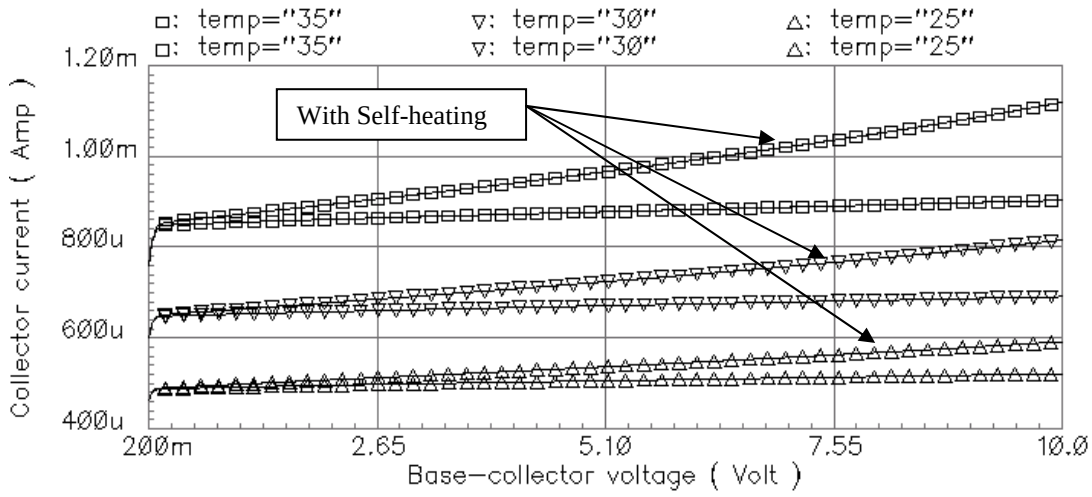


Figure 3.9 Effect of self-heating on the output characteristics of a voltage driven *npn* transistor in the *CE* configuration, with and without self-heating.

It is reported that a current driven transistor is less vulnerable to self-heating than a voltage driven one because of the lower thermal sensitivity of beta in comparison with collector current [6]. This is illustrated in the simulation shown in the Fig. 3.10.

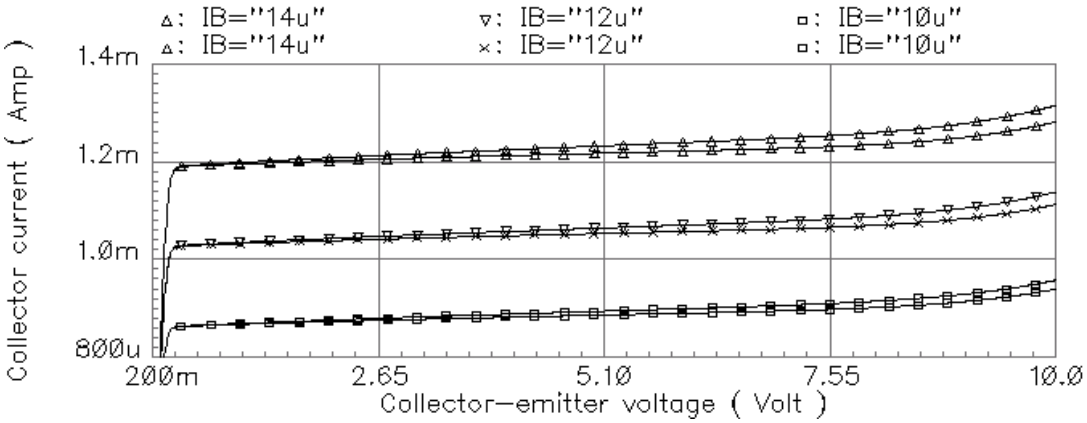
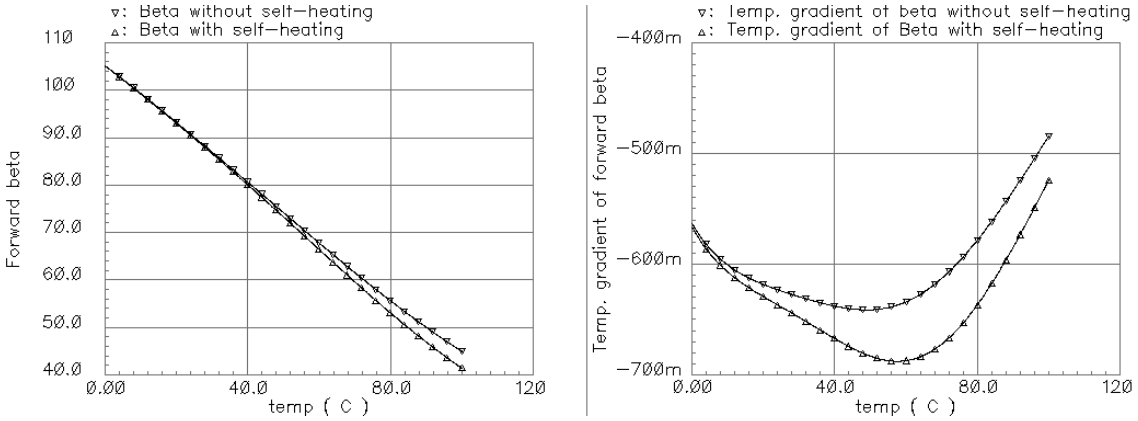


Figure 3.10 Effect of self-heating on the output characteristics of a current driven *npn* transistor in the *CE* configuration, with and without self-heating.

The overall temperature dependence of a transistor is governed by three important parameters, namely the fractional temperature coefficient of base current, TC_{FB}, the fractional temperature coefficient of collector current, TC_{FC}, and the fractional temperature coefficient of beta, $TC_{F\beta}$. The effect of self-heating on $TC_{F\beta}$ is illustrated through the simulation shown in Fig. 3.11 for the *npn* transistor.



(a) (b)

Figure 3.11 (a) DC beta versus temperature (b) temperature gradient of beta for an *npn* bipolar transistor with and without self-heating.

3.3.2 Thermal Effects of Dynamic Self-Heating

The effect of dynamic self-heating on the output impedance characteristics of the bipolar transistor in the *CE* configuration is analytically formulated through (3.25), which shows that there will be a thermally induced "zero-pole doublet" and an intrinsic pole in the output impedance function.

The simulation for the magnitude response of the impedance at the collector of the transistor of Fig. 3.12 is shown in Fig. 3.13.

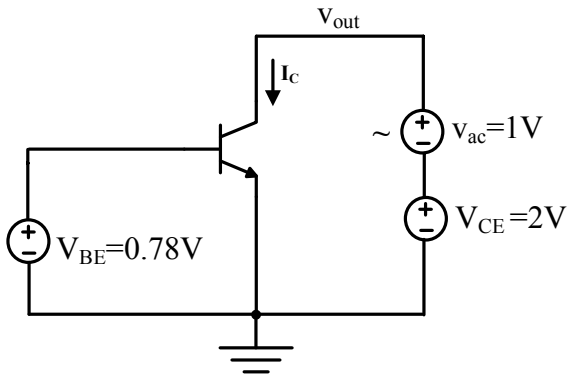


Figure 3.12 The *npn* bipolar transistor in the common-emitter configuration for the simulation of the frequency response of the impedance at the collector.

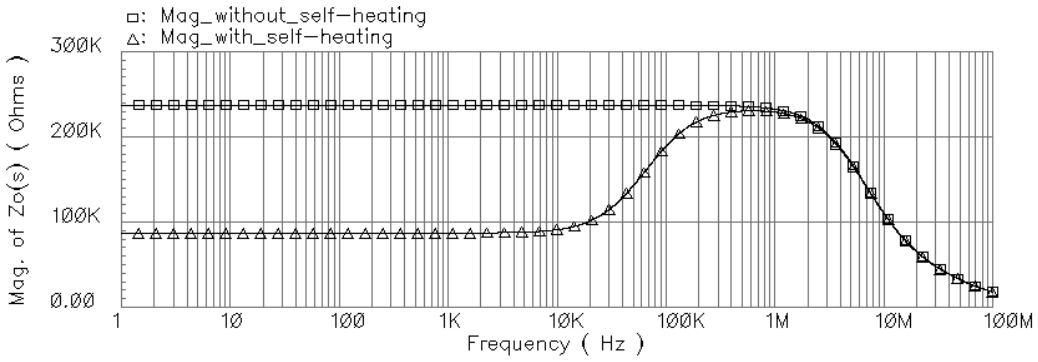


Figure 3.13 Magnitude versus frequency of the output impedance, with and without self-heating, and bias current, $I_{C,}$ of 555.3 μA.

As shown in Fig. 3.13, the magnitude of dc and low-frequency impedance at the collector has decreased by about 50% of the impedance without self-heating. As frequency increases beyond about 10 kHz, there is a range of frequency over which thermally induced non-ideal effects starts to appear. Such range of frequencies depends on thermal time constant of a specific process technology. This frequency response needs to be addressed by circuit designers. To suppress such non-ideal effects, the intrinsic pole and thermally induced “zero-pole” doublet need to be closer together to achieve a pole-zero cancellation. Another parameter which influences the amplifier

performance is transconductance. The affect of self-heating on transconductance is shown in the simulation of Fig. 3.14.

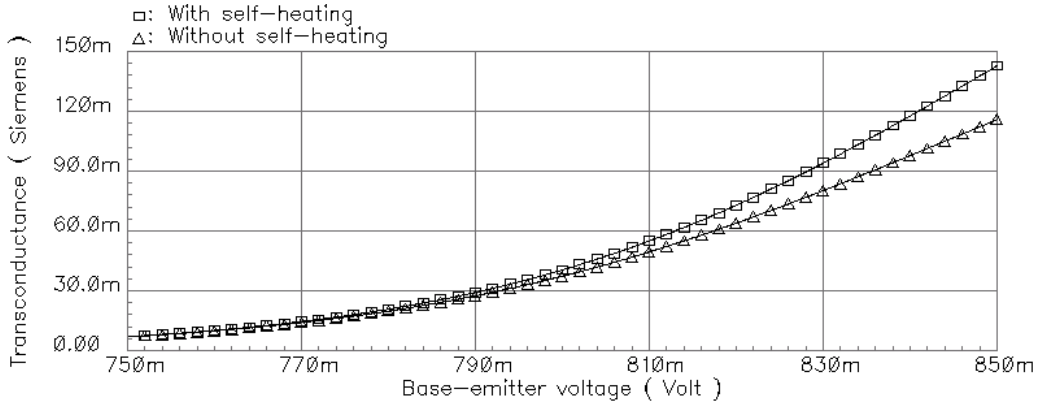


Figure 3.14 Transconductance versus the base-emitter voltage of circuit in Fig. 3.12.

3.4 Modeling the Effects of Dynamic Self-Heating in a Bipolar Transistor with Emitter Degeneration

3.4.1 Effects of Series-Series Feedback on Self-Heating

It is well known [7] that series-series or voltage-current feedback mechanism shown in Fig. 3.15 is widely used to increase both the input and output impedances of a transistor.

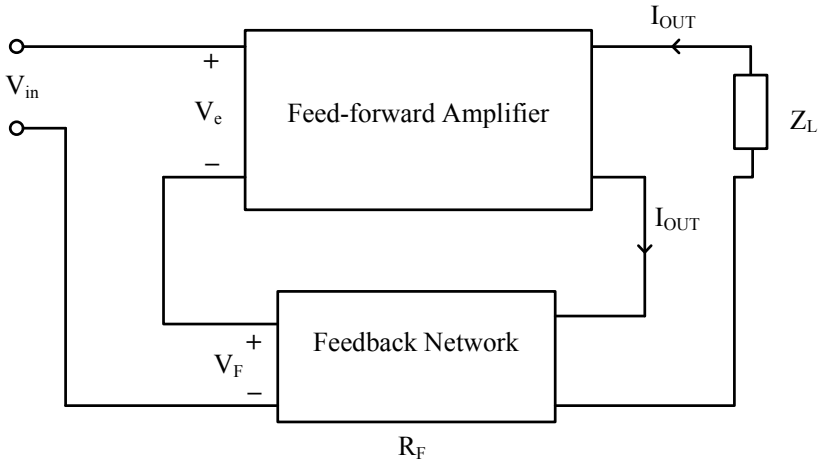


Figure 3.15 Series-series feedback configuration [45].

Under this feedback, the input and output impedances of a circuit can be represented as

$$Z_{if} = Z_i(1+T) \tag{3.32}$$

$$Z_{of} = Z_o(1+T) \tag{3.33}$$

where Z_i, Z_o, and T are the intrinsic input impedance, intrinsic output impedance, and loop gain, respectively. Since this technique can be used to boost the output resistance, it can be used to lower the intrinsic pole frequency so that the thermally induced non-linearity can be minimized. A resistor in the emitter of a transistor offers series-series feedback, and hence can be used to increase the output resistance of a bipolar transistor.

3.4.2 Modeling the Effect of Dynamic Self-Heating on the Small-Signal Admittance Parameters

The small-signal equivalent circuit incorporating the effect of dynamic self-heating for a single stage transistor with an emitter degeneration resistor is shown in Fig. 3.16.

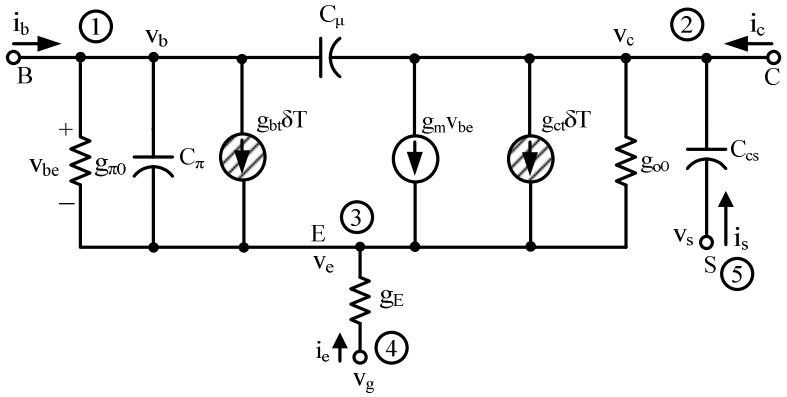


Figure 3.16 Small-signal equivalent circuit for the *npn* transistor with emitter degeneration, incorporating the effect of self-heating.

The terminal currents and voltages of the circuit in Fig. 3.16 can be related through a primitive indefinite-admittance matrix as [42]

$$\begin{bmatrix} i_b \\ i_c \\ i_e \\ i_g \\ i_s \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} & y_{13} & y_{14} & y_{15} \\ y_{21} & y_{22} & y_{23} & y_{24} & y_{25} \\ y_{31} & y_{32} & y_{33} & y_{34} & y_{35} \\ y_{41} & y_{42} & y_{43} & y_{44} & y_{45} \\ y_{51} & y_{52} & y_{53} & y_{54} & y_{55} \end{bmatrix} \begin{bmatrix} v_b \\ v_c \\ v_e \\ v_g \\ v_s \end{bmatrix} + \begin{bmatrix} i_{bs} \\ i_{cs} \\ i_{es} \\ i_{gs} \\ i_{ss} \end{bmatrix} \tag{3.34}$$

where y_{ij} is the small signal admittance parameter, and i_{is} is the short-circuit current at the *i*th terminal when all the other terminals are short-circuited to ground. The current, i_{ss}, stems from the independent sources and/or initial conditions within the n-terminal network if any. The node v_e of Fig. 3.16 is an inaccessible terminal. Following the approach (see Appendix B) discussed by Chen [43], matrix (3.34) can be expressed as

$$\begin{bmatrix} i_b \\ i_c \\ i_e \\ i_g \\ i_s \end{bmatrix} = \begin{bmatrix} y_\pi + sC_\mu & -sC_\mu & -y_\pi & 0 & 0 \\ g_m - sC_\mu & g_{o0} + s(C_\mu + C_{cs}) & -(g_m + g_{o0}) & 0 & -sC_{cs} \\ -(g_m + y_\pi) & -g_{o0} & g_m + g_{o0} + g_E + y_\pi & -g_E & 0 \\ 0 & 0 & -g_E & g_E & 0 \\ 0 & -sC_{cs} & 0 & 0 & sC_{cs} \end{bmatrix} \begin{bmatrix} v_b \\ v_c \\ v_e \\ v_g \\ v_s \end{bmatrix} + \begin{bmatrix} g_{bt} \\ g_{ct} \\ -(g_{bt} + g_{ct}) \\ 0 \\ 0 \end{bmatrix} \delta T \tag{3.35}$$

where $y_\pi = g_{\pi 0} + C_\pi$.

For the common-emitter configuration, terminals 4 and 5 of Fig. 3.16 are contracted and then referenced to ground. With these operations, the circuit of Fig 3.16 can be reduced to the circuit shown in Fig. 3.17.

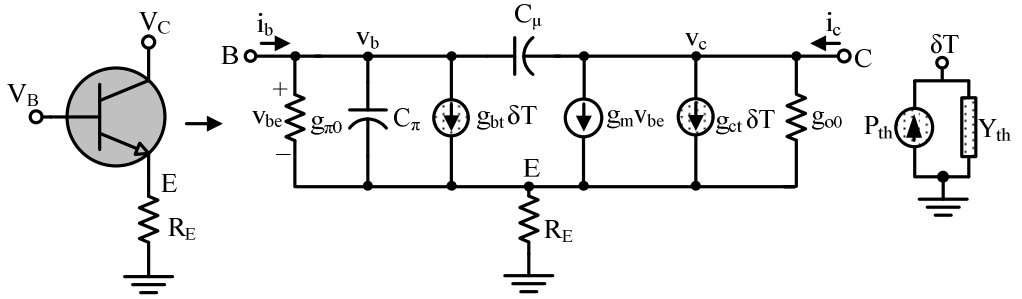


Figure 3.17 Small-signal equivalent circuit for an SOI BJT with emitter degeneration in the common-emitter configuration, including self-heating model.

The indefinite-admittance matrix in (3.31) can be reduced to the two-port admittance matrix in (3.36), characterizing the circuit in Fig. 3.17.

$$I(s) = Y_Q(s) \cdot V(s) + \theta(s) \cdot \delta T(s) \tag{3.36}$$

where Y_Q(s), I(s), V(s), θ(s), and δT(s) are

$$I(s) = \begin{bmatrix} i_b \\ i_c \end{bmatrix} \tag{3.36a}$$

$$Y_Q(s) = \begin{bmatrix} y_\pi + sC_\mu - \dfrac{y_\pi \cdot (g_m + y_\pi)}{g_m + g_{o0} + g_E + y_\pi} & -sC_\mu - \dfrac{y_\pi \cdot g_{o0}}{g_m + g_{o0} + g_E + y_\pi} \\ g_m - sC_\mu - \dfrac{(g_m + g_{o0}) \cdot (g_m + y_\pi)}{g_m + g_{o0} + g_E + y_\pi} & g_{o0} + sC_\mu - \dfrac{(g_m + g_{o0}) \cdot g_{o0}}{g_m + g_{o0} + g_E + y_\pi} \end{bmatrix} \tag{3.36b}$$

$$V(s) = \begin{bmatrix} v_b \\ v_c \end{bmatrix} \tag{3.36c}$$

$$\theta(s) = \begin{bmatrix} g_{bt} - \dfrac{y_\pi \cdot (g_{ct} + g_{bt})}{g_m + g_{o0} + g_E + y_\pi} \\ g_{ct} - \dfrac{(g_m + g_{o0}) \cdot (g_{ct} + g_{bt})}{g_m + g_{o0} + g_E + y_\pi} \end{bmatrix} \tag{3.36d}$$

$$\delta T(s) = \begin{bmatrix} \dfrac{(I_b + g_{\pi T} V_b + g_{mT} V_c)}{Y_{th} - (g_{ct} V_c + g_{bt} V_b)} & \dfrac{(I_c + g_{oT} V_c)}{Y_{th} - (g_{ct} V_c + g_{bt} V_b)} \end{bmatrix} \cdot V(s) \tag{3.36e}$$

The complete derivation of (3.36) can be found in Appendix C. The output admittance of the transistor with emitter degeneration resistor can be evaluated as [44]

$$Y_{22}(s)=\left[g_{o0}-\frac{(g_m+g_{o0})\cdot g_{o0}}{g_m+g_{o0}+g_E+y_\pi}+sC_\mu\right]+\left[\begin{array}{l}\left(g_{ct}-\dfrac{(g_m+g_{o0})(g_{bt}+g_{ct})}{g_m+g_{o0}+g_E+y_\pi}\right)\\ \cdot\left(\dfrac{(I_c+g_{oT}V_c)\cdot Z_{th}}{1-(g_{ct}V_c+g_{bt}V_b)\cdot Z_{th}}\right)\end{array}\right] \qquad (3.37)$$

$$=y_{\text{intrinsic\_re}}+y_{\text{thermal\_re}}$$

It is seen from (3.37) that the effective value of collector thermal transconductance, g_{cteff}, enclosed within a dotted rectangle in (3.37) is drastically reduced from the thermal transconductance of a transistor, g_{ct}, and hence the effect of dynamic self-heating can be reduced proportionally on a single stage transistor with emitter degeneration. A typical response of the output impedance of a single-stage emitter-degenerated amplifier is shown in Fig. 3.18.

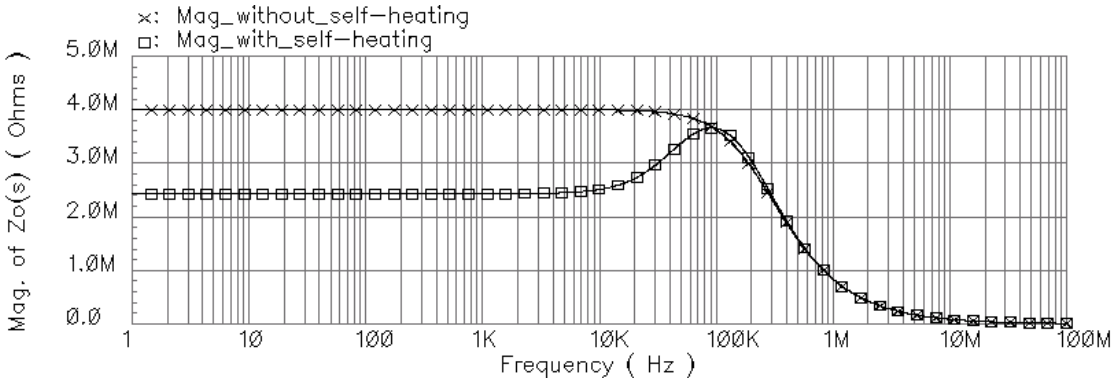


Figure 3.18 Magnitude response of the output impedance of the *npn* transistor with emitter degeneration (R_E = 1kΩ) of Fig. 3.17, with a bias current of 300 μA.

As shown in the simulation, the reduction in the magnitude of low-frequency impedance at the collector can be reduced with a higher value of emitter degeneration resistor. The magnitude of peaking is reduced as well.

3.5 Effect of Cascoding on Self-Heating

3.5.1 The Fundamental Concept of Cascoding

It is well known that a transistor in the common-emitter configuration coverts a voltage signal to a current signal. The cascade of a common-emitter (*CE*) stage and a common-base (*CB*) stage is called a "cascode" topology [7], [45]-[46], providing many useful properties, such as high output resistance, and output shielding. The cascode transistor "shields" the input device from voltage variations at the output. Fig. 3.19 shows a basic cascode configuration in which Q_1 generates a small-signal collector current proportional to V_{in} and Q_2 simply routes the current to load resistance, R_L. The cascode circuit can be used as a single-stage amplifier or as a high output resistance current source.

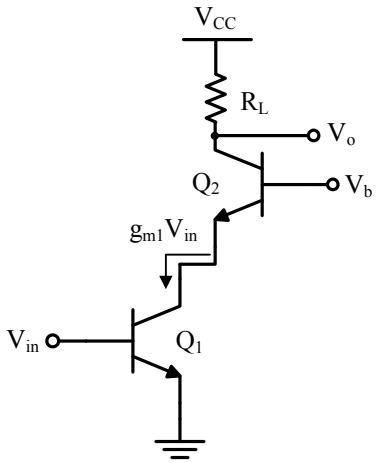


Figure 3.19 Cascode amplifier using bipolar transistors.

An important property of the cascode structure is to offer high dc and low-frequency output impedance and can be expressed as [7]

$$R_o \cong r_{o2}\left(1+\frac{g_{m2}r_{o1}}{1+\frac{g_{m2}r_{o1}}{\beta_0}}\right) \tag{3.38}$$

Assuming $g_{m2}r_{o1} >> \beta_0$, equation (3.38) can be simplified to

$$R_{out} \approx r_{o2}(1+\beta_0) \tag{3.39}$$

Thus, the *CE-CB* configuration can boost the output resistance by a factor of $(1+\beta_0)$ higher than the *CE* stage alone. However, such a structure demands higher voltage headroom as indicated by (3.40).

$$V_O(min) = V_{CE2}(sat) + V_{CE1} \tag{3.40}$$

Cascoding can be extended to have three or more cascode devices as shown in Fig. 3.20 to achieve higher output impedance, but the required high voltage headroom makes such configurations less attractive. An important popular application of this topology is in building constant current sources. The high output impedance yields a constant current source closer to ideal, but at the cost of voltage headroom.

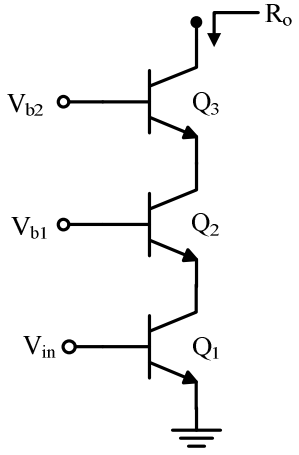


Figure 3.20 Tripe cascode stage using bipolar transistors.

The main idea behind the cascode structure is to convert the input voltage to a current and apply the resulting current to a *CB* stage. However, the input device and the cascode device need not be of the same type. For example, the *npn-pnp* circuit combinations as shown in Fig. 3.21 can perform the same function as the cascode stage.

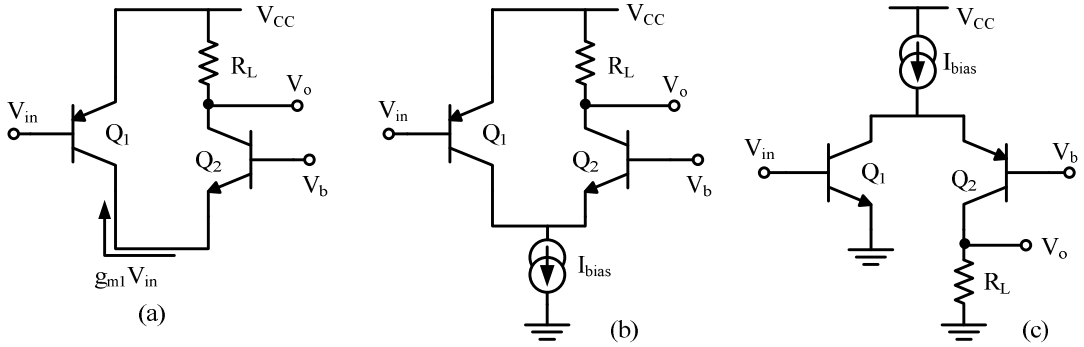


Figure 3.21 (a) Simple folded cascode with the *pnp* transistor as input. (b) Folded cascode with proper biasing. (c) Folded cascode with the *npn* transistor as an input.

The structures of Fig 3.21 are called “folded cascode” stages because the small-signal current is folded up in Fig. 3.21(b) and down in Fig. 3.21(c). But the total bias current in this case must be higher than that of normal cascode structure to achieve comparable performance. The primary advantage of the folded cascode structure lies in the choice of the voltage levels, because it does not “stack” the cascode transistor on top of the input device [45]. This concept will be used in the design of a folded cascode input stage based current feedback operational amplifier (CFOA) in chapter 7.

3.5.2 Modeling Output Impedance of Cascode Structure

The output admittance of a two-stage cascade structure shown in Fig. 3.19 can be expressed using (3.37) as

$$Y_o(s) = \left[g_{o02} - \frac{(g_{m2} + g_{o02}) \cdot g_{o02}}{g_{m2} + g_{o02} + g_{o01} + y_{\pi 2}} + sC_{\mu 2} \right] + [g_{cteff} \cdot M] \tag{3.41}$$
$$= y_{intrinsic} + y_{thermalre}$$

where

$$g_{cteff} = \left(g_{ct} - \frac{(g_{m2} + g_{o02}) \cdot (g_{bt} + g_{ct})}{g_{m2} + g_{o02} + g_{o01} + y_{\pi 2}} \right) \tag{3.41a}$$

$$M = \left(\frac{(I_{c2} + g_{oT2} V_{ce2}) \cdot Z_{th}}{1 - (g_{ct} V_{c2} + g_{bt} V_{be2}) \cdot Z_{th}} \right) \tag{3.41b}$$

The inverse of (3.41) gives the output impedance. It is seen from (3.41a) that the effective value of thermal transconductance, g_{cteff}, may be very small or even go negative for a very low value output conductance of transistor Q_1 of Fig. 3.19, minimizing the effect of self-heating even at dc and low frequency. Thus, cascoding helps in reducing the effect of dynamic self-heating. This can be verified through the simulation shown in Fig. 3.22 for the frequency response of the output impedance of the cascode structure.

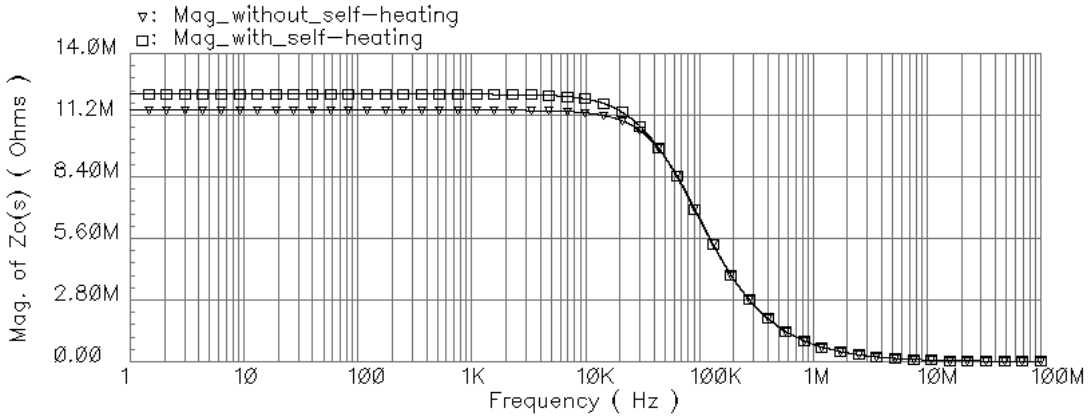


Figure 3.22 Magnitude response of the output impedance of the cascode structure of Fig. 3.19, with a bias current of 450 μA.

As shown in the simulation, it offers very high dc and low-frequency resistance in comparison with the bipolar transistor even with emitter degeneration at the expense of bandwidth. It shows minimal impact of dynamic self-heating. Instead of decreasing the output resistance due to self-heating, it increases the resistance, thereby substantiating the theoretical model derived in (3.41).

3.6 Effect of Self-Heating on the Noise Performance of an SOI Bipolar Transistor

3.6.1 Noise Sources in Active Devices

3.6.1.1 Thermal Noise

Thermal noise is generated by the random thermal motion of electrons and is unaffected by the magnitude of direct-current. The power spectral density of thermal noise modeled as a series voltage in a resistor, *R*, can be expressed as [7]

$$S_V = \frac{\overline{v^2}}{\Delta f} = 4kRT \tag{3.42}$$

where k is Boltzmann's constant, T is the absolute temperature, and Δf is bandwidth in Hz. Thermal noise is present in any linear passive resistor. In the bipolar devices, the parasitic base resistance, r_{bb}, can generate the thermal noise.

3.6.1.2 Shot Noise

Shot noise is associated with direct-current flow and is found in the diodes, MOSFETs, and bipolar transistors [7]. It causes fluctuation in direct-current and is usually modeled as a noise current source with the spectral density in the form of

$$S_I = \frac{\overline{i^2}}{\Delta f} = 2qI_{dc} \tag{3.43}$$

3.6.1.3 Flicker Noise

Flicker noise is found in all active devices and in some discrete passive elements such as carbon resisters. It is mainly caused by traps associated with contamination and crystal defects during processing of a device. The flicker noise is also called 1/f noise because it shows the spectral density in the form of

$$S_I = \frac{\overline{i^2}}{\Delta f} = K_1 \frac{I^a}{f^b} \tag{3.44}$$

where I is the direct-current, K_1, a, and b are constants. With b = 1 in (3.44), the flicker noise spectral density would show a *1/f* frequency dependence. Thus, flicker noise is dominant at low frequency.

3.6.2 Modeling the Effect of Dynamic Self-Heating on Noise

The full small-signal equivalent circuit including noise sources for the bipolar transistor is shown in Fig. 3.23.

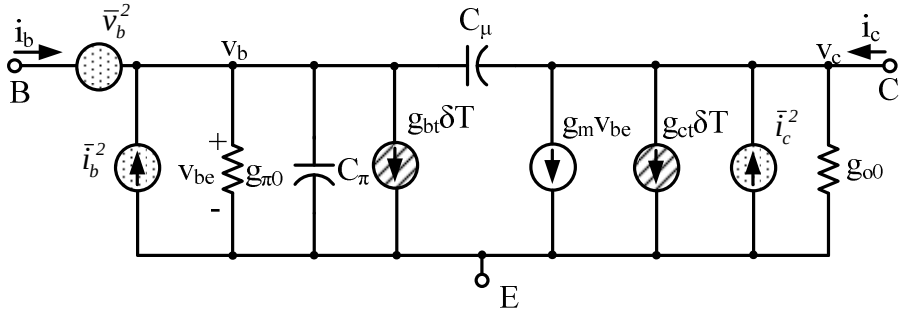


Figure 3.23 A complete bipolar transistor small-signal equivalent circuit with noise sources.

Since they arise from separate, independent physical mechanisms, all noise sources are independent of each other and have mean-square values

$$\overline{v_b^2} = 4kTr_b\Delta f \tag{3.45}$$

$$\overline{i_c^2} = 2qI_C\Delta f \tag{3.46}$$

$$\overline{i_c^2} = 2qI_B\Delta f + K_1\frac{I_B^a}{f}\Delta f \tag{3.47}$$

An equivalent model of the circuit shown in Fig. 3.23 can be represented with a model shown in Fig. 3.24, in which all of the internal noise sources represented by (3.45) through (3.47) are lumped into two equivalent noise sources at the inputs. These are a voltage source with power spectral density of S_{Vi} and a current source with power spectral density of S_{Ii} as shown in Fig. 3.24.

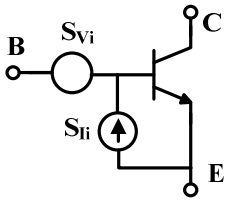


Figure 3.24 Bipolar transistor with equivalent noise generator [48].

The equivalent noise spectral density at the input can be expressed as

$$S_{Vi} = 4K(T+\Delta T)\cdot\left(r_b + \frac{1}{2g_m}\right) \tag{3.48}$$

$$S_{Ii} = 2q\left[I_B + \frac{K_1}{2q}\cdot\frac{I_B^a}{f} + \frac{I_C}{|\beta(j\omega)|^2}\right] \tag{3.49}$$

It is seen from (3.48) and (3.49) that the noise spectral density is dependent on temperature and bias current, which is affected by self-heating.

3.7 Analog Circuits Most Affected through Self-Heating

The performance of several analog circuits depends on the exponential transfer function of the bipolar transistor [7]. This is the basis of the design of analog multiplier circuits. In addition, the non-linear synthesis function circuits, such as square root circuits, and square law circuits, are severely influenced by self-heating. The examples of such circuits are shown in Fig. 3.25.

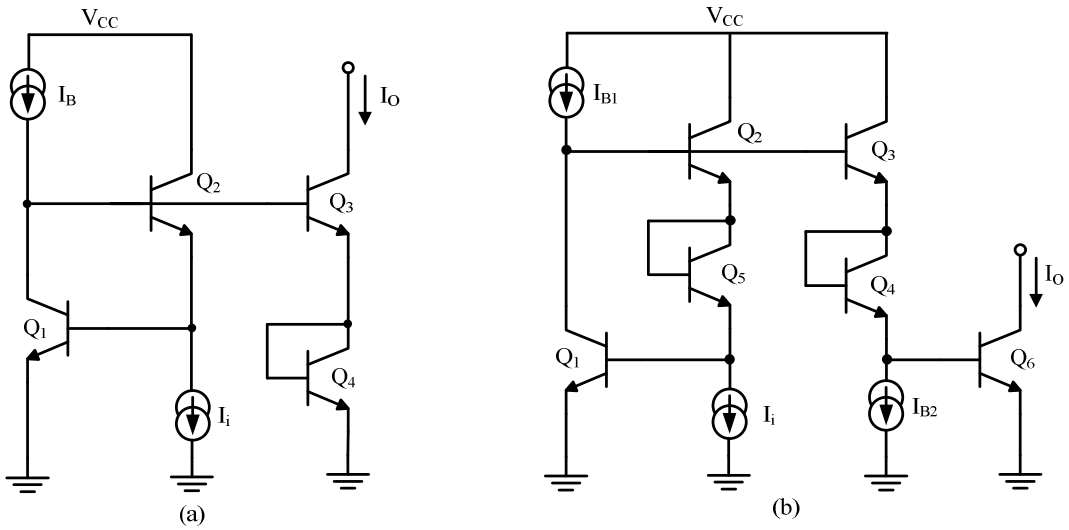


Figure 3.25 Bipolar non-linear function synthesis circuits (a) Square root circuit. (b) Square law circuit.

Assuming the precision exponential transfer characteristics of the bipolar transistor and precise matching of the base-emitter voltage, V_{BE}, of constituent transistors, the dc bias current of output transistor, I_o, for Fig. 3.25 can be expressed as [7]

$$I_o = \sqrt{I_i}\sqrt{I_B}\sqrt{\frac{I_{S3}I_{S4}}{I_{S1}I_{S2}}} \qquad \text{for Fig. 3.25(a)} \qquad (3.50)$$

$$I_o = I_i^2 \frac{I_{B1}}{I_{B2}^2} \frac{I_{S3} I_{S4} I_{S6}}{I_{S1} I_{S5} I_{S2}} \qquad \text{for Fig. 3.25(b)} \qquad (3.51)$$

where I_{Si} is the saturation current of the respective transistor as shown in Fig. 3.25. As explained in chapter one, the base-emitter voltage and saturation currents are highly influenced by self-heating, and hence such circuit's performance will be severely impacted.

In summary, bias circuits, bandgap reference circuits, current conveyor circuits, current mirrors, analog multiplier, and translinear circuits are the circuits of concern. These require special design attention when SOI bipolar transistors are used.

3.8 Summary

This chapter provides an extensive theoretical foundation to characterize the thermal effect of self-heating in the design and analysis of fundamental block of analog circuits. Circuit level design optimization techniques are presented to mitigate the non-ideal thermal effects of self-heating. These effects were verified through the SPECTRE simulator using the physics based VBIC model. The general class of the self-heating influenced analog circuits is identified. An approach to model the effect of dynamic self-heating on noise performance of an SOI bipolar transistor has also been presented.

CHAPTER 4

EFFECTS OF DYNAMIC SELF-HEATING ON THE FREQUNECY RESPONSE OF CURRENT MIRRORS

Current mirror is one of the fundamental blocks in analog integrated circuits design. It is widely used to bias transistors in the integrated circuits. Hence, both the large-signal and small-signal performance of analog integrated circuits are strongly dependent on the performance of current mirrors being used to provide the bias current. The non-ideal thermal effects of self-heating in the frequency response of various current mirrors have been studied extensively in this chapter through design, simulation, and measurement. Frequency-domain non-ideal thermal effects are first identified in the most commonly used simple current mirror, and then the analysis is extended to high performance current mirrors, such as Wilson and cascode current mirrors. These high performance current mirrors perform well to suppress the thermally induced errors.

This chapter begins with the analytical formulations of output admittance and impedance of various well-known current mirrors incorporating the effects of dynamic self-heating. All of the analytical formulations have been substantiated through the extensive simulations using the physics based VBIC models. However, the designs are then laid out and fabricated with the VIP10^{TM} bipolar process technology. The dc measurement for the output resistance of all current mirrors was carried out using modern 6½ digit high Performance digital multimeter – Agilent 34410A. Extensive

frequency-domain measurements were conducted using an Agilent precision impedance analyzer, 4294A, and an 110 MHz impedance probe, 42941A.

4.1 Thermal Effects of Self-Heating on Simple Current Mirror

The large-signal errors caused by self-heating are mostly dominant in biasing circuits as evidenced by Sang Lee [6]. It has been shown by Fox [5] that a voltage driven transistor is more susceptible to self-heating than a current driven transistor. In a simple current mirror shown in Fig. 4.1, the output transistor, Q_0, is being driven from a voltage source derived from the diode connected transistor, Q_1. Consequently, the power level of the transistors Q_0 and Q_1 will be different from each-other even if the reference current, I_{bias}, and mirrored output current, I_o, are the same. Because of power difference, Q_0 can be identified as a hotter device and Q_1 as a cooler device. This creates a temperature gradient between the constituent transistors, leading to the V_{BE} mismatch. Several papers [5]-[6], [10]-[11], [49] have provided an extensive analysis on the effect of self-heating on the large-signal performance of analog circuits. However, only few papers, most notably [13], have treated the frequency-domain effect of self-heating on analog circuits. This research work has treated this effect extensively.

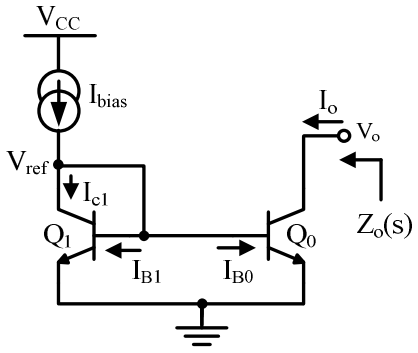


Figure 4.1 Simple current mirror using bipolar transistors.

4.1.1 Modeling of Output Impedance, $Z_o(s)$ with Self-Heating

Current mirror's static performance is dependent on the matching of the base-emitter voltage, V_{BE}, of constituent transistors isothermally [5], [10]. The static error caused by thermal mismatch in V_{BE} of transistors, Q_0 and Q_1, of Fig. 4.1 has been verified experimentally [49], but the effect of dynamic self-heating in bipolar current mirrors has never been treated extensively. The effect of self-heating in a current mirror can be expressed through the electrothermal [6]-[7] model shown in Fig. 4.2.

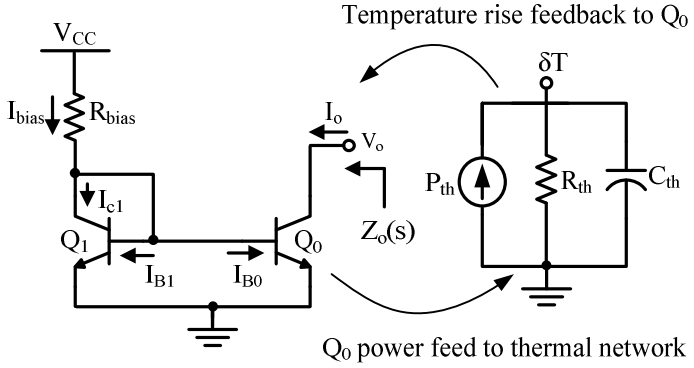


Figure 4.2 Simple bipolar current mirror with an electrothermal model.

Ignoring the resistance looking into the base of Q_1, α_1/g_{m1}, the output impedance of the current mirror of Fig. 4.2 including the effects of dynamic self-heating can be approximated with (3.24) in chapter 3 and repeated here as

$$Z_o(s)=\frac{\dfrac{1}{g_{o0}+X_g R_{th}/(1-MR_{th})}\left(1+\dfrac{s}{(1-MR_{th})/R_{th}C_{th}}\right)}{\dfrac{R_{th}C_{th}C_{eq}}{g_{o0}(1-MR_{th})+X_g R_{th}}s^2+\dfrac{R_{th}C_{th}g_{o0}+C_{eq}(1-MR_{th})}{g_{o0}(1-MR_{th})+X_g R_{th}}s+1} \tag{4.1}$$

where

$$g_{o0}\approx\frac{m\cdot I_{bias}}{V_A} \tag{4.2}$$

$$M = g_{ct}V_c + g_{bt}V_b \tag{4.3}$$

$$X_g = g_{ct}\left(I_c + g_{oT}V_c\right) \tag{4.4}$$

$$C_{eq} = C_\mu + C_{cs} \tag{4.5}$$

where m is the multiplying factor of the transistor, Q_0, and I_{bias} is the bias or reference current as shown in the Fig. 4.2. The denominator of (4.1) is a second-order polynomial in s and hence gives two poles. The nature of the poles may be real or complex valued depending on the basing and size of the transistors being used. Assuming $X_g R_{th} >> g_{o0}(1\text{-}MR_{th})$ and $R_{th}C_{th}g_{o0} >> C_{eq}(1\text{-}MR_{th})$, the denominator and numerator of (4.1) can be simplified to give a zero and two poles as

$$f_z = \left(1 - MR_{th}\right)\cdot f_{th} \tag{4.6}$$

$$p_{1,2} = \frac{-g_{o0} \pm \sqrt{g_{o0}^2 - \dfrac{4X_g C_{eq}}{C_{th}}}}{2C_{eq}} \tag{4.7}$$

The dc and low frequency output resistance can be evaluated using s = 0, and can be expressed as

$$R_o = \frac{1}{g_{o0} + \dfrac{g_{ct}\cdot(I_c + g_{oT}V_c)\cdot R_{th}}{1-(g_{ct}V_c + g_{bt}V_b)\cdot R_{th}}} \tag{4.8}$$

The expression for dc output resistance in (4.8) shows that output resistance reduces with the higher value of thermal resistance and bias voltages. The scenario of “no self-heating” can be simulated by assuming g_{ct} and g_{bt} equal to zero in (4.8). The zero is close to the thermal cutoff frequency and the two poles will be real for

$g_{o0}^2 > 4X_g C_{eq}/C_{th}$ which should be true in general for a simple current mirror with narrow devices (implies larger thermal resistance). It can be inferred from (4.7) that the poles are very close to the intrinsic current mirror's output pole at g_{o0}/C_{eq}. Thus, the movement of intrinsic pole will automatically influence the thermally induced pole's location. This will be useful in thermally induced pole-zero cancellation.

4.1.2 Design, Simulation and Layout

The frequency response of the output impedance, $Z_o(s)$, of simple current mirror shown in Fig. 4.2, with each device area of 40.0 μm^2, R_{th} = 375 K/W, and C_{th} = 16.9 nJ/K, I_{ref} = 225.0 μA, and V_o = 2.0 V, is shown in Fig. 4.3 using the VBIC model parameters listed in Table 2.9.

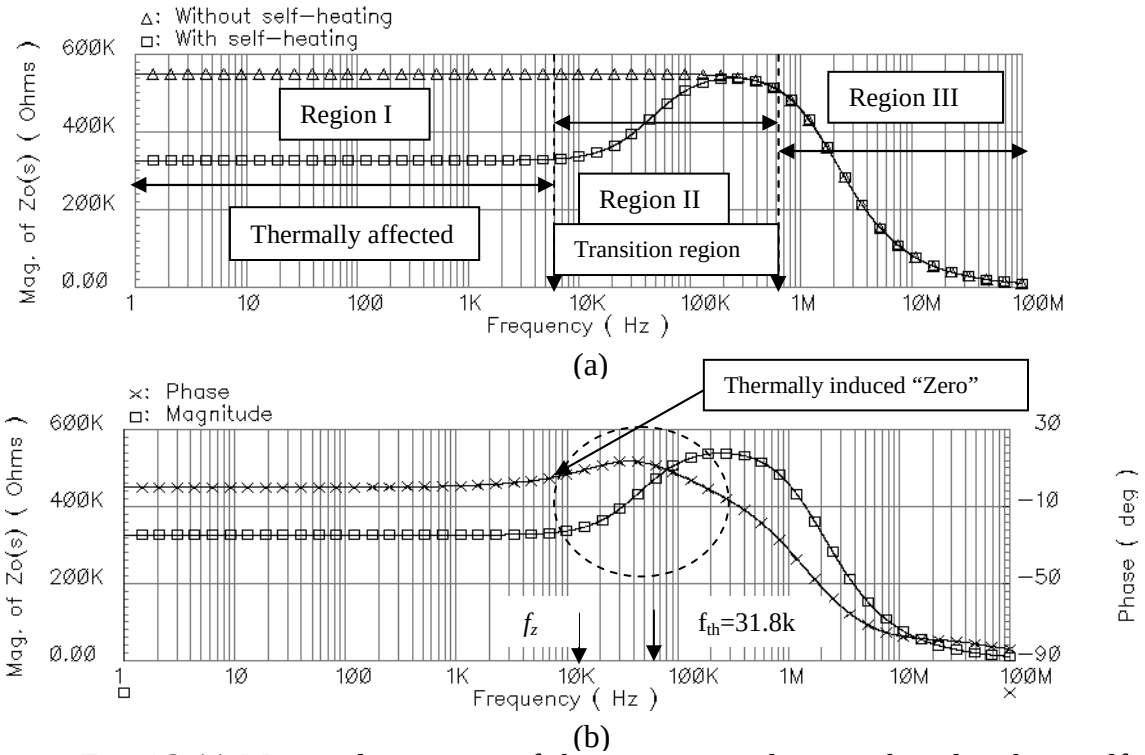


Fig. 4.3 (a) Magnitude response of the output impedance with and without self-heating (b) Frequency response of the output impedance of the simple current mirror of Fig. 4.2 with self-heating enabled.

In region I, where the frequency is lower than thermally induced zero, f_z, given by (4.6), the $y_{thermal}$ in (3.24) is dominant and the effective output resistance is about 50% of what would have been achieved without self-heating as shown in Fig. 4.3(a). The presence of a thermally induced "zero" can also be verified through the phase response in Fig. 4.3(b). As the frequency becomes higher than the thermal cutoff frequency, f_{th} (31.8 kHz in this simulation as shown in Fig. 4.3(b)), the thermally induced conductance parameters defined in (3.13) - (3.15) will be suppressed gradually and hence the effects of dynamic self-heating start to disappear as illustrated in region II. In the high-frequency region III, the impedance response is governed by device intrinsic pole location. The pole-zero factor, defined here as the ratio of the dominant intrinsic device pole frequency to a thermally induced "zero" frequency, is greater than 1.

The frequency response of the output impedance of the simple current mirror of Fig. 4.2 is shown in Fig. 4.4, with and without self-heating to show how self-heating induced "zero" causes peaking like effect in the frequency response.

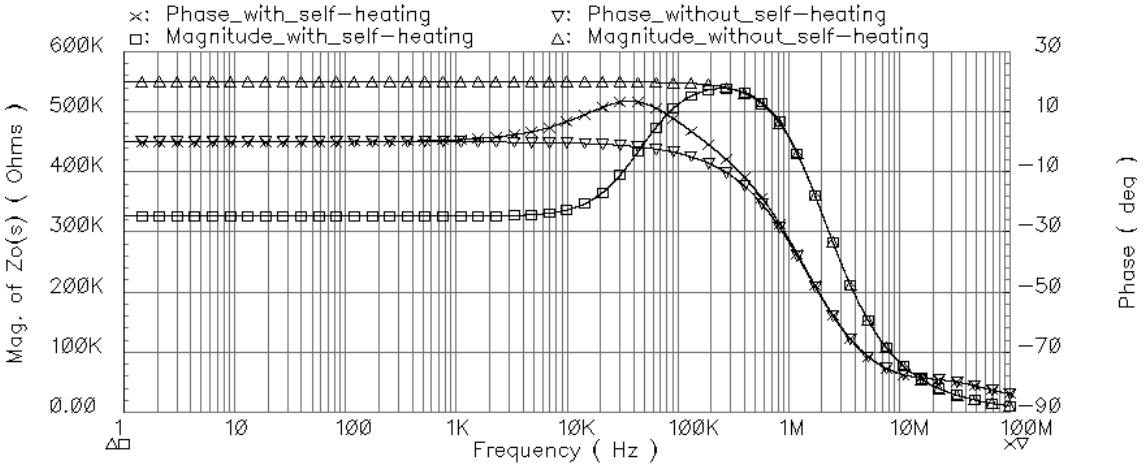


Figure 4.4 Frequency response of the output impedance of the simple current mirror of Fig. 4.2 with and without self-heating, and bias current of 225 μA.

4.1.2.1 Impact of Thermal Resistance in the Frequency Response of $Z_O(s)$

It can be inferred from (4.8) that the dc and low frequency output impedance can be reduced significantly by increasing thermal resistance, a technology dependent parameter. Fig. 4.5 shows that the impact of variation of thermal resistance on the output impedance.

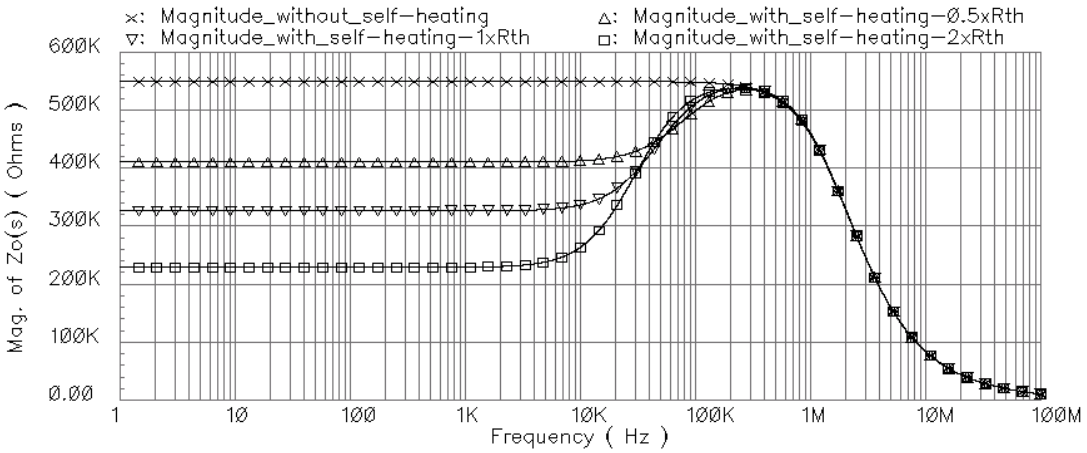


Figure 4.5 Magnitude response of the output impedance of the simple current mirror of Fig. 4.2, with thermal resistance, R_{th}, as a sweep parameter.

As shown in Fig. 4.5, a higher value of thermal resistance induces the large degradation of dc and low-frequency output resistance when self-heating is enabled versus disabled. It is also shown that the thermally induced “zero-pole” doublet has shifted to low-frequency as the value of thermal resistance increases as expected from (4.6) and (4.7). However, the intrinsic device pole frequency is invariant. Thus, the device intrinsic pole frequency is not dependent on thermal resistance. From this simulation, it can be inferred that a smaller device with a higher value of thermal resistance reduces the output resistance, degrading the current mirror performance. Thus, wider device is a better choice to minimize the effect thermal of self-heating.

4.1.2.2 Impact of I_{bias} on the $Z_O(s)$ of a Simple Current Mirror

From first-order analysis, the output resistance of the simple current mirror of Fig. 4.1, without considering the effect of self-heating, is given by

$$R_o = \frac{V_A}{I_o} \tag{4.9}$$

where V_A is the Early voltage and I_o is the output current (assumed close to I_{bias} in this analysis) as shown in Fig. 4.2. This shows that the output resistance will increase with a decrease in the output current. In addition, the reduction in current will also help to minimize the effect of self-heating due to the lower static power dissipation.

Figure 4.6 shows the simulation for the magnitude response of the output impedance of the simple current mirror of Fig. 4.2, which shows that the effect of self-heating becomes more dominant as the static power dissipation increases.

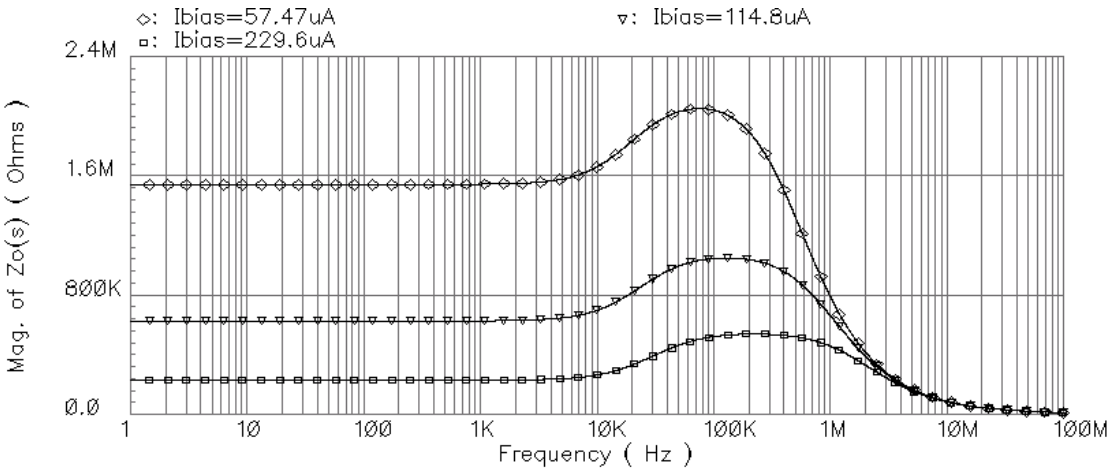


Figure 4.6 Magnitude response of the output impedance of the simple current mirror of Fig. 4.2, with bias current, I_{bias}, as a sweep parameter.

A peaking free frequency response may be possible even in simple current mirror with extremely low bias current.

4.1.2.3 Impact of Transistor Size on the $Z_O(s)$ of a Simple Current Mirror

The effect of self-heating can be reduced by increasing the device area [1]. The area of each transistor (with an emitter area of 5 μm^2) of Fig. 4.2 is increased by a factor of 4, 6, and 8 and the frequency response is obtained as shown in Fig. 4.7. This shows that degradation in the low-frequency output resistance can be reduced by increasing the area of the devices.

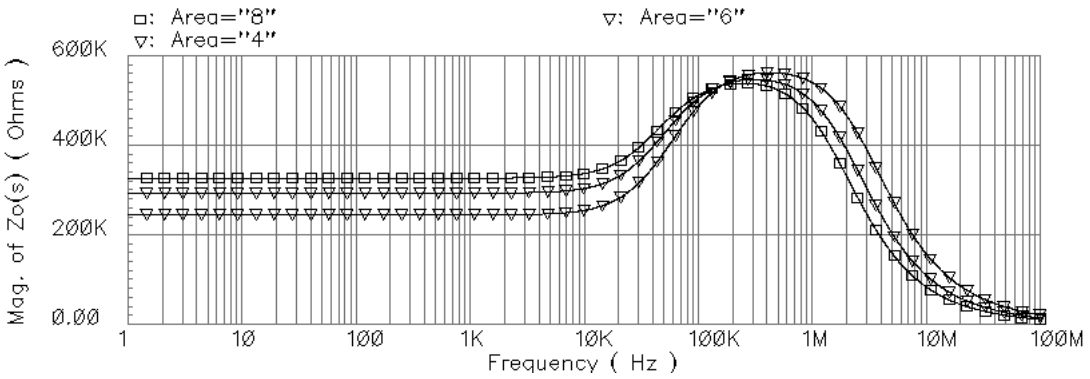


Figure 4.7 Magnitude response of the output impedance of the current mirror of Fig. 4.2, with area of transistor as a sweep parameter but at fixed I_{bias} = 225 μA.

The most important point to note is that the location of the thermally induced "zero" is not influenced by the area of devices because thermal resistance is directly proportional to area while the thermal capacitance is inversely proportional the area of the device, leaving the thermal time constant and cutoff frequency unchanged.

4.1.2.4 Impact of Current Mirror Gain on Output Impedance

In the integrated circuit design, there may be a need to bias different parts of the circuit with different bias currents. As an example, a current mirror with a gain of 1, 2, and 3 is designed as shown in Fig. 4.8. To achieve this, the areas of transistors, $Q_{0,}$ Q_{0a} and Q_{0b}, are selected same as, twice, and thrice the area of Q_1, respectively.

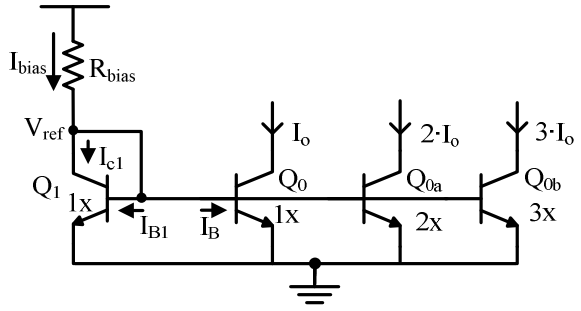


Figure 4.8 Simple current mirror with a gain of 1, 2 and 3.

Increasing area of the transistors reduces the thermal resistance, and hence lowers the impact of self-heating. However, the dc and low-frequency output resistance will be decreased. This is confirmed by the simulation shown in Fig. 4.9.

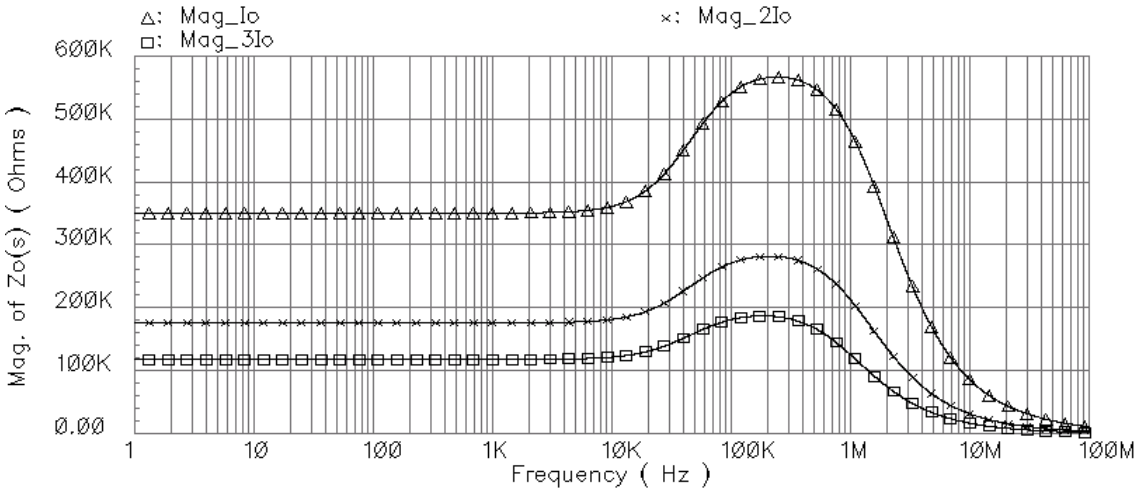


Figure 4.9 Magnitude response of the output impedance of the simple current mirror of Fig. 4.2, with a current mirror gain of 1, 2 and 3, and I_{bias} = 225 μA.

4.1.2.5 Layout of Simple Current Mirror

The current mirror of Fig. 4.2 is laid out as shown in Fig. 4.10 and fabricated using the VIP10^{TM} bipolar process technology. Both transistors, Q_0 and Q_1, have an emitter area of 40 μm^2 and bias resistor, R_{bias}, is 2 kΩ. The die is placed within a dual-in-line (DIP) package.

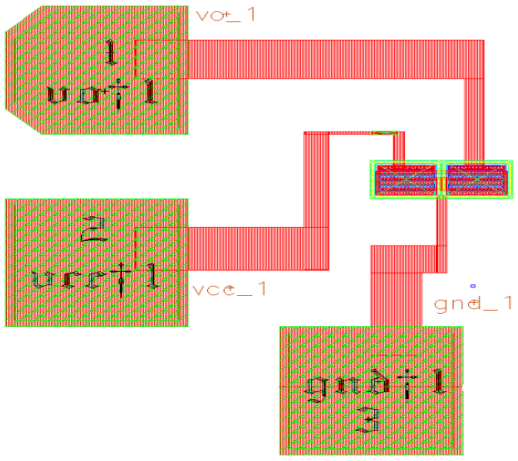


Figure 4.10 Layout of the simple current mirror of Fig. 4.2 (UTA213) [50].

4.1.3 DC Output Resistance Measurement

The dc output resistance of the current mirror of Fig. 4.10 was measured using an Agilent E3631A (triple output power supply) and an Agilent 34410A (6½ digit high performance digital multimeter). The V_{CC} was set to 1.9 V to get a reference current, I_{ref}, of 0.613 mA, and the output voltage, V_O, was varied from 0.2 V to 5.0 V. The measurement result is shown in Fig. 4.11.

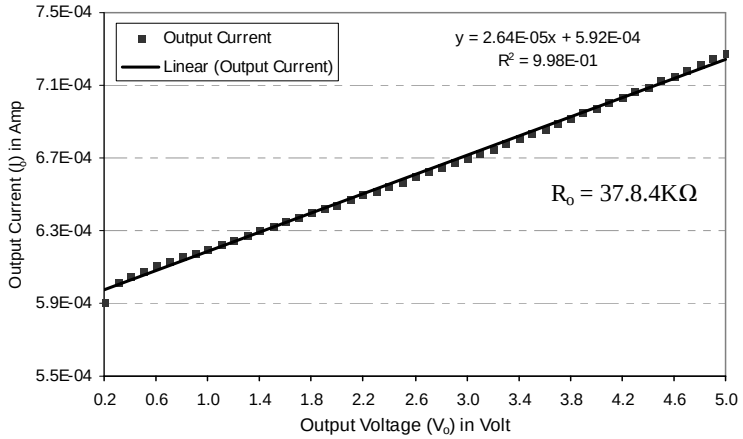


Figure 4.11 Output current versus output voltage for the simple current mirror of Fig. 4.10 with I_{bias} = 0.613 mA.

The measurement data is curve fitted with a linear approximation and giving a dc resistance of 37.8 kΩ. The correlation between simulation and measurement is provided in Table 4.1.

Table 4.1 DC Output Resistance Correlation between Simulation and Measurement.

Simulation Physics Based VBIC Model	Simulation VIP10^{TM} Process Model	Measurement
76.59 kΩ	46.9 kΩ	37.8 kΩ

4.1.4 Frequency-Domain Output Impedance Measurement

The frequency response of the simple current mirror of Fig. 4.10 was measured using a precision impedance analyzer – Agilent 4294A, along with an impedance probe – Agilent 42941A. The composite is capable to measure the impedance between 3 mΩ and 500 MΩ in the frequency range of 40 Hz and 110 MHz with a measurement accuracy of 0.08%. Before measurement, open, short, and matched load calibrations were performed for the analyzer. Thermally induced non-ideal effects can clearly be seen in the measured frequency response shown in Fig. 4.12.

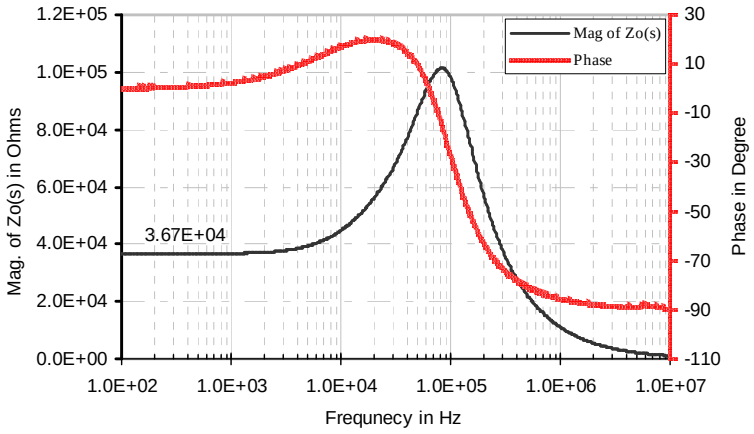


Figure 4.12 Frequency response of the output impedance, $Z_O(s)$, of the simple current mirror, UTA213 (Fig 4.10) with I_{bias} = 642 μA and V_O = 2 V.

From visual inspection, the thermally induced “zero” and “pole” are approximately at 10 kHz, and 70 kHz, respectively. The frequency response beyond 100 kHz is governed by the intrinsic pole, defined by (4.7) with $X_g = 0$. Fig. 4.13 shows exactly the same plot as in Fig. 4.12, but here the y-axis is plotted as a log scale to mimic the Bode plot. Visual inspection of the plot shows that the high frequency (> 100 kHz) magnitude response has the slope of -20 dB/dec, which is a theoretical high frequency characteristic for a single pole first-order system [51]. In addition, the maximum theoretical phase shift achievable through a single-pole first-order system is – 90 degrees [51], which is also confirmed through the phase response shown in Fig. 4.13. This confirms that the high frequency response of the current mirror is indeed governed by the intrinsic pole of the output transistor and the thermal effect is no longer effects the response. But the non-ideal thermal effects appeared between 10 kHz and 100 kHz is because of the thermally induced “zero-pole” doublet.

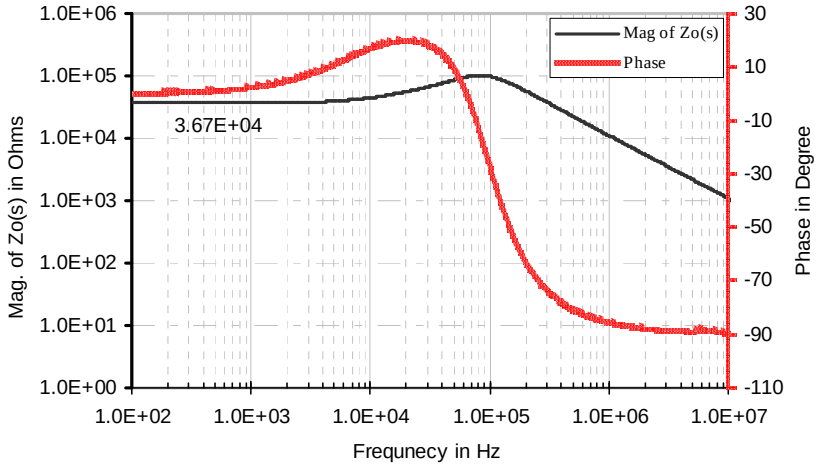


Figure 4.13 Frequency response of the output impedance of the simple current mirror of Fig. 4.10 with $I_{bias} = 642\ \mu A$ and $V_O = 2$ V. Y-axis is in log scale.

The dc and low-frequency output resistance as shown in Figs. 4.12 and 4.13 is about 36.7 kΩ while the high-frequency output resistance, where the effect of self-heating disappears, is about 100 kΩ. Thus, there is about a 63% output resistance reduction due to self-heating. However, such a reduction is a function of bias current as illustrated by another frequency response shown in Fig. 4.14 where the bias current has decreased to 225 μA. The dc and low-frequency output resistance for this case is 225 kΩ while the high-frequency output resistance is 300 kΩ. Thus, there is about 25% output resistance degradation due to self-heating. Thus, it is verified experimentally that the thermal effect of self-heating in the frequency response of a simple current mirror is strongly dependent on the bias current confirming the theory and simulation provided in section 4.1.2.2.

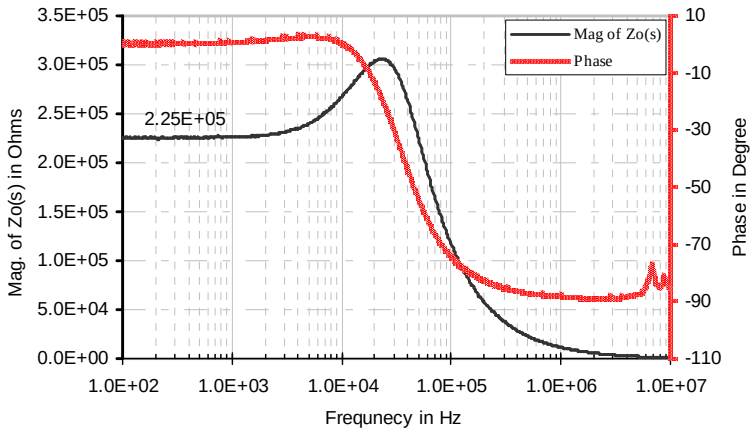


Figure 4.14 Frequency response of the output impedance, $Z_O(s)$, of the simple current mirror of UTA213 (Fig. 4.10) with I_{bias} = 225 μA, and V_O = 2 V.

4.1.5 Thermal Characterization of $Z_O(s)$

The dependence of the thermally induced "zero-pole" doublet and intrinsic pole in the simple current mirror of Fig. 4.2 with a change in the bias current, I_{bias}, is shown

in Fig. 4.15. The bias voltage, V_{CC}, was supplied through a dc power supply, Agilent E3631A, and the voltage at V_O of Fig. 4.2 was supplied through the dc voltage source of impedance analyzer, and both were varied from 1.15 V to 2.5 V to set the bias current, I_{bias}, in the range of 216 μA and 1.29 mA. The magnitude versus frequency plot for each bias current is illustrated in Fig. 4.15 for a comparison. This shows that the magnitude of both low-frequency output resistance and peaking is indeed influenced by the bias current, I_{bias}.

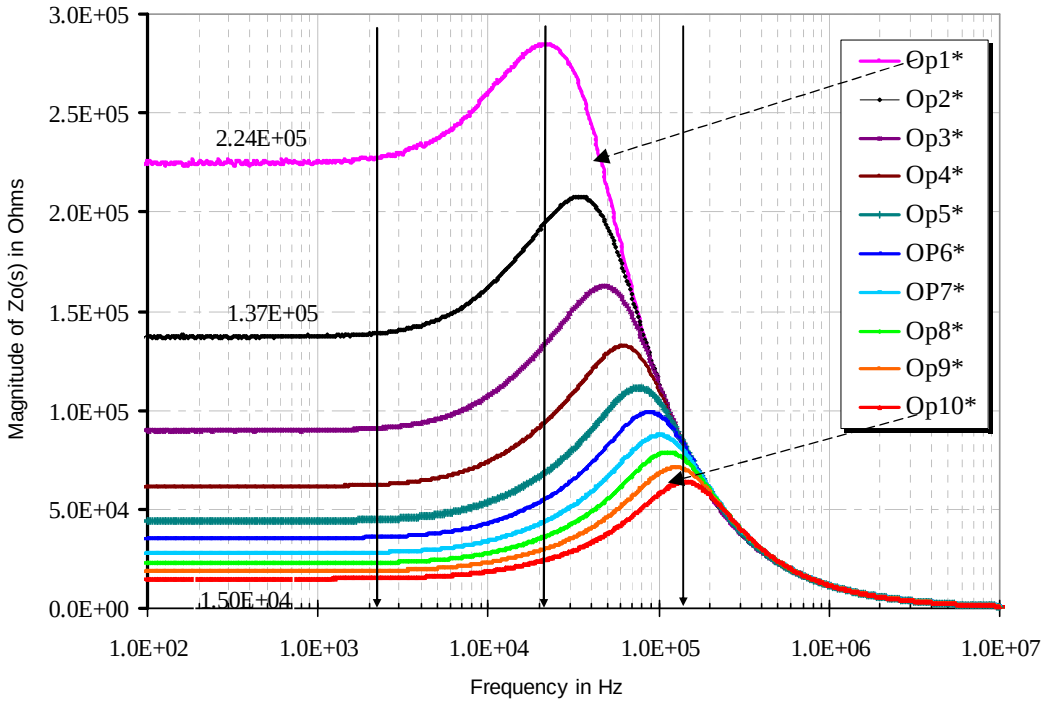


Figure 4.15 Magnitude response of the output impedance, $Z_O(s)$, of the simple current mirror (UTA213) with the I_{bias} as a sweep parameter. *"Opx" definition is provided in Table 4.2.

More specifically, the low-frequency measured output resistance for I_{bias} = 216 μA is ~224 kΩ, while it is 15 kΩ for I_{bias} = 1.29 mA. Table 4.2 summarizes these results in detail.

Table 4.2 Bias Setup for the Measurement of DC Output Resistance of Fig. 4.10.

Op	**V_{CC} in V**	**V_o in V**	**I_o in A**	**Approx. DC R_o**
Op1	1.15	1.15	2.16×10^{-04}	224 kΩ
Op2	1.30	1.30	3.03×10^{-04}	137 kΩ
Op3	1.46	1.46	3.99×10^{-04}	89.7 kΩ
Op4	1.63	1.63	5.04×10^{-04}	61.3 kΩ
Op5	1.80	1.80	6.01×10^{-04}	44.1 kΩ
Op6	1.93	1.93	7.01×10^{-04}	35.2 kΩ
Op7	2.08	2.08	8.06×10^{-04}	27.6 kΩ
Op8	2.21	2.21	9.01×10^{-04}	22.6 kΩ
Op9	2.35	2.35	1.01×10^{-03}	18.5 kΩ
op10	2.50	2.50	1.29×10^{-03}	15.0 kΩ

The details of the dependency of the thermally induced "zero-pole" doublet and intrinsic pole on the bias current are provided in Table 4.3.

Table 4.3 Measurement of DC Output Resistance, Thermally Induced "Zero-Pole" Doublet and Intrinsic Pole as a Function of Bias Current of the Simple Current Mirror of Fig. 4.10.

Opx	**I_o**	**DC Output Resistance, R_o**	**Thermally Induced Zero Frequency**	**Thermally Induced Pole Frequency**	**Intrinsic Pole Frequency**
Op1	2.16×10^{-04} A	224.0 kΩ	2.0 kHz	15.0 kHz	22 kHz
Op2	3.03×10^{-04} A	137.0 kΩ	2.5 kHz	25.0 kHz	35 kHz
Op3	3.99×10^{-04} A	89.7 kΩ	3.0 kHz	38.0 kHz	50 kHz
Op4	5.04×10^{-04} A	61.3 kΩ	4.0 kHz	50.0 kHz	60 kHz
Op5	6.01×10^{-04} A	44.1 kΩ	5.0 kHz	60.0 kHz	80 kHz
Op6	7.01×10^{-04} A	35.2 kΩ	6.0 kHz	70.0 kHz	90 kHz
Op7	8.06×10^{-04} A	27.6 kΩ	7.0 kHz	80.0 kHz	100 kHz
Op8	9.01×10^{-04} A	22.6 kΩ	8.0 kHz	90.0 kHz	125 kHz
Op9	1.01×10^{-03} A	18.5 kΩ	10.0 kHz	95.0 kHz	140 kHz
Op10	1.29×10^{-03} A	15.0 kΩ	10.0 kHz	100.0 kHz	150 kHz

From Table 4.3, it is observed that the thermally induced "zero" moves from 2 kHz to 10 kHz when the bias current increases by a factor of 6 from 216 μA. However, the dc and low-frequency output resistance reduces by a factor ~15.0 as illustrated in Table 4.3. The separation between the thermally induced pole and intrinsic pole depends upon the bias current. This agrees with the trend predicted by the theoretical model of (4.7).

4.2 Thermal Effects of Self-Heating on a Simple Current Mirror with Emitter Degeneration

It is reported [15] that the frequency-domain non-ideality can be reduced by enhancing the output resistance of a current mirror. The output resistance of a current mirror can be improved by using an emitter degeneration resistor shown in Fig. 4.16.

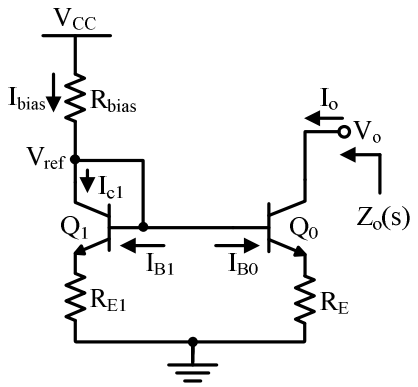


Figure 4.16 Current mirror with emitter degeneration resistor [7].

The output impedance (without incorporating the effect of self-heating) of such a current mirror can be found from a routine circuit analysis and expressed as [47]

$$R_o = r_o\left(1+\beta_0\left(\frac{R_E}{R_{E1}+\frac{\alpha_0}{g_m}+r_\pi+R_E}\right)\right) \tag{4.10}$$

It is clearly seen that the output resistance can be increased with higher value of emitter degeneration resistor.

4.2.1 Modeling of Output Impedance with Self-Heating

The output admittance of the current mirror of Fig. 4.16, including the effect of dynamic self-heating, can be approximated with (3.37), and is repeated here for convenience as

$$Y_{22}(s) = \left[g_{o0} - \frac{(g_m + g_{o0}) \cdot g_{o0}}{g_m + g_{o0} + g_E + y_\pi} + sC_\mu \right] + \left[\left(g_{ct} - \frac{(g_m + g_{o0}) \cdot (g_{bt} + g_{ct})}{g_m + g_{o0} + g_E + y_\pi} \right) \cdot \left(\frac{(I_c + g_{oT} V_c) \cdot Z_{th}}{1 - (g_{ct} V_c + g_{bt} V_b) \cdot Z_{th}} \right) \right] \quad (4.11)$$

$$= y_{\text{intrinsic\_re}} + y_{thermal\_re}$$

The terms $y_{intrinsic\_re}$ and $y_{themral\_re}$ are the intrinsic and thermally induced component of the output admittance parameter, $Y_{22}(s)$. From the analysis, it can be inferred that the magnitude of $y_{thermal\_re}$ in (4.11) is far less than the magnitude of $y_{thermal}$ in (3.24). Therefore, the percentage reduction in the output resistance below f_{th} due to dynamic self-heating is lower in the emitter degenerated current mirror than in the simple current mirror. Because of higher output resistance, the pole-zero factor, as defined in chapter 3, is also reduced. This can further be minimized by using a higher value of R_E. However, this is not an attractive technique in integrated circuits because of reduced compliance.

4.2.2 Design, Simulation and Layout

The current mirror with emitter degeneration is shown in Fig. 4.16. For design, each transistor with an emitter area of 40.0 μm^2, emitter degeneration resistance of 50 Ω

are used with a bias current, I_{bias}, of 225.0 μA, and V_o = 2.0 V. The simulation is done with the VBIC model provided in Table 2.9 with R_{th} = 375 K/W, C_{th} = 16.9 nJ/K. The magnitude response versus frequency is shown in Fig. 4.17, with and without the effect of self-heating.

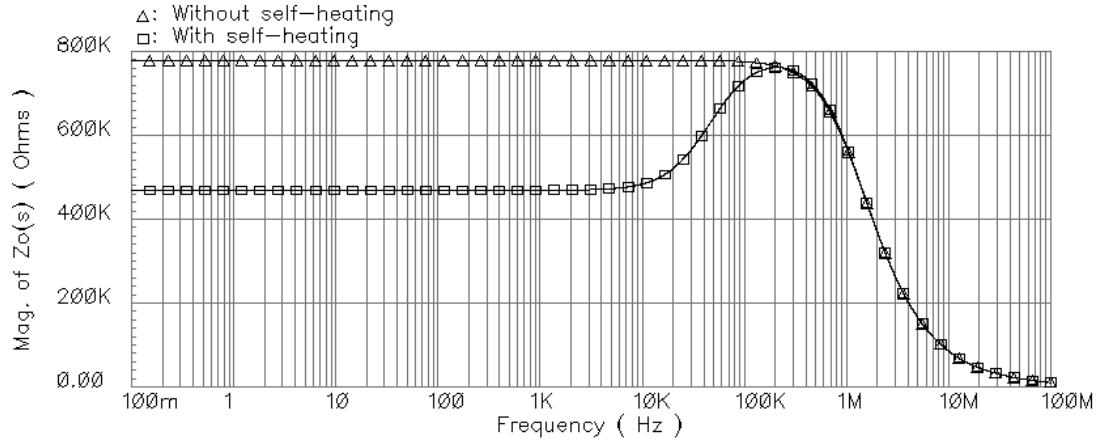


Figure 4.17 Magnitude response of the current mirror in Fig. 4.16 with and without self-heating, with R_E = 50 Ω, and I_{bias} = 225 μA.

The presence of a thermally induced zero can be verified through the phase response shown in Fig. 4.18.

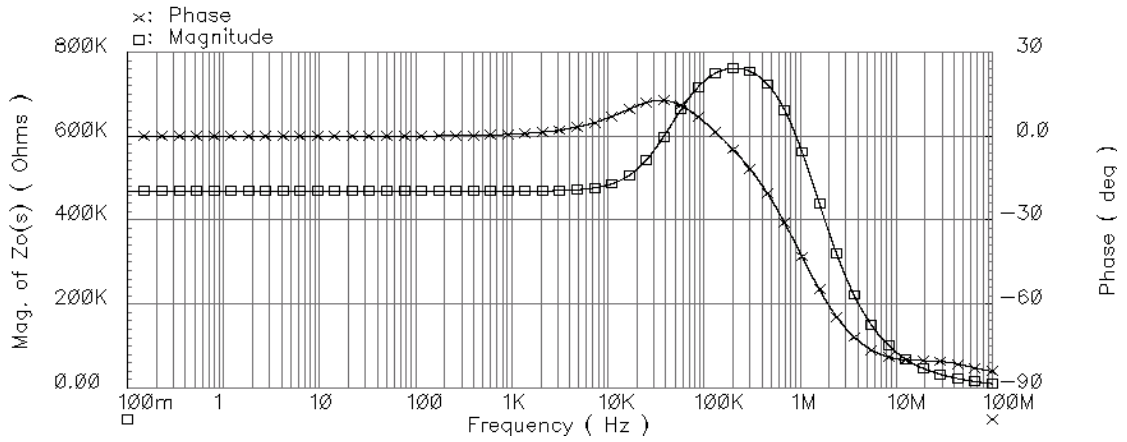


Figure 4.18 Frequency response of the output impedance of the emitter degeneration current mirror in Fig. 4.16 with R_E = 50 Ω, and I_{bias} = 225 μA.

As illustrated in Fig. 4.19, the thermal effect of self-heating can be reduced by using a higher value of emitter degeneration resistor, R_E at the cost of compliance range. It is also verified that the low-frequency output resistance can be improved.

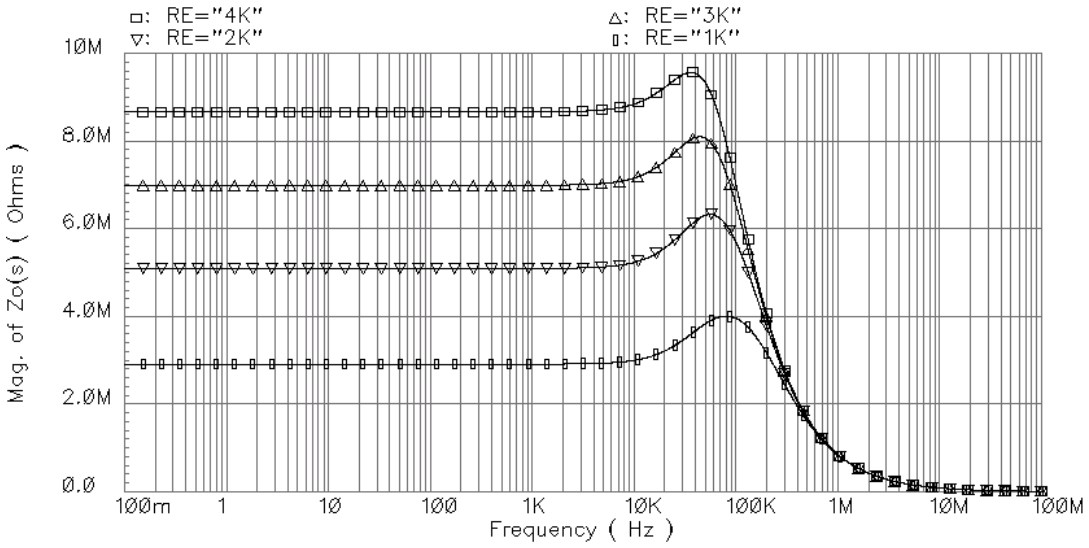


Figure 4.19 Magnitude response of the output impedance of the current mirror with emitter degeneration of Fig. 4.16 with the same bias current of 225 μA.

The percentage degradation of the magnitude of dc output resistance and peaking can be reduced with a higher value of emitter degeneration resistor. This is in agreement with the theoretical model of (4.11).

The current mirror of Fig. 4.16 was laid out as shown in Fig. 4.18 and fabricated with the VIP10^{TM} bipolar process technology. The transistors, Q_0 and Q_1, had an emitter area of 40 μm^2, bias resistor, R_{bias}, was 2 kΩ, and emitter degeneration resistor was 50 Ω. The die was placed within a DIP package.

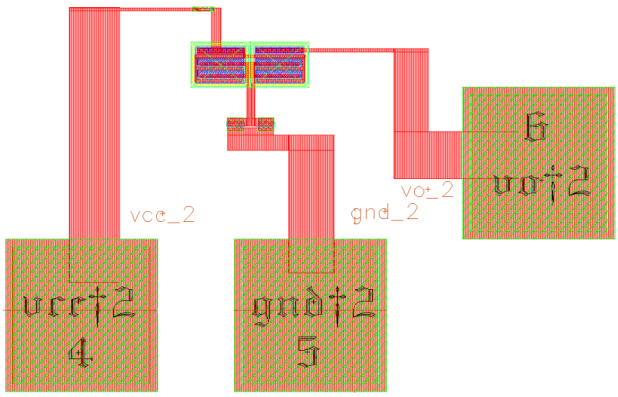


Figure 4.20 Layout of the current mirror of Fig. 4.16 with R_E = 50 Ω [50].

4.2.3 DC Output Resistance Measurement

The dc output resistance of the current mirror of Fig. 4.20 was measured by setting V_{CC} to 1.9 V through the dc power supply, Agilent E3631A to yield I_{ref} of 0.613 mA, and output voltage, V_O, was varied from 0.2 to 10 V using the same Agilent E3631A. The measurement result is shown in Fig. 4.21. The measurement data is curve fitted with a linear approximation and the dc resistance was found to be 107.4 kΩ.

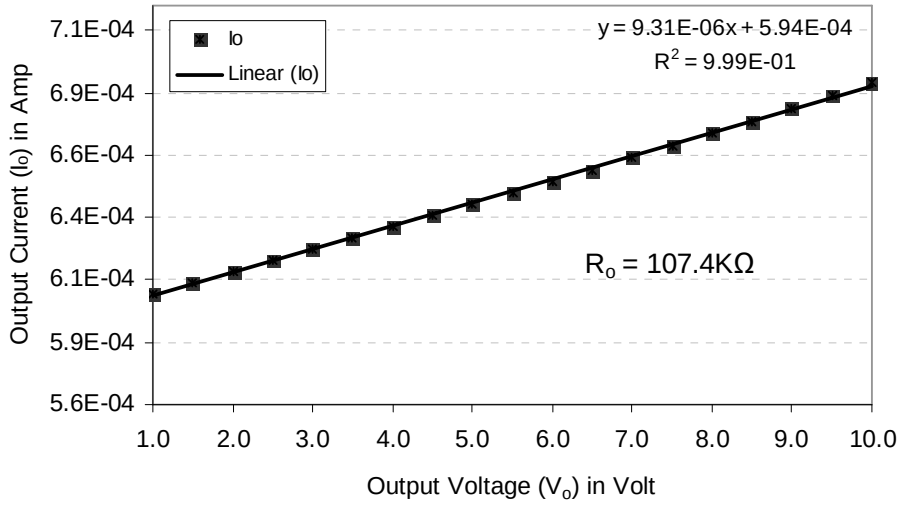
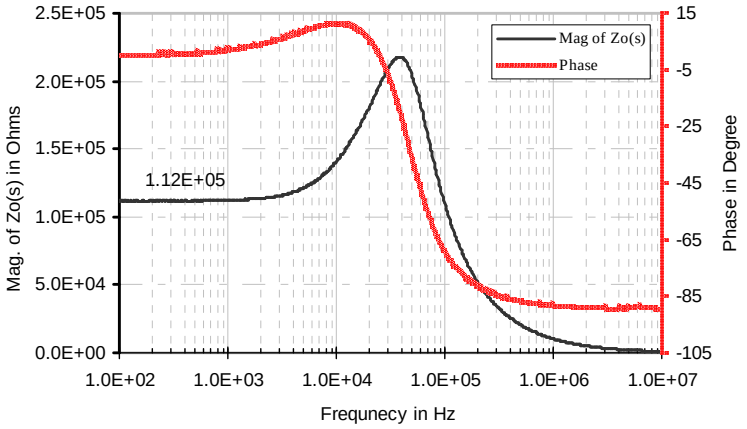


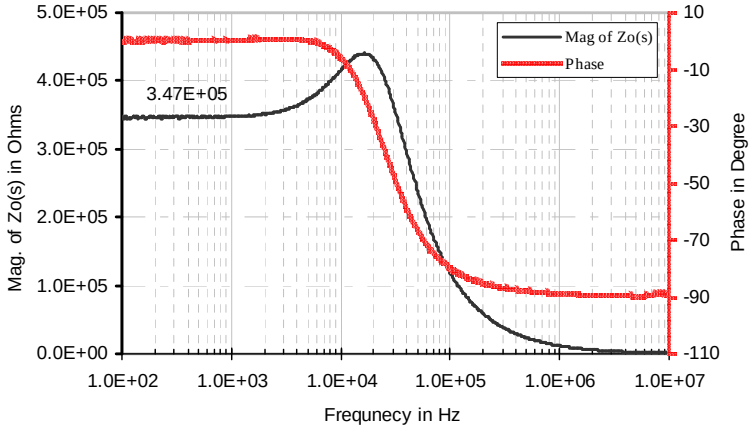
Figure 4.21 DC output current versus voltage of Fig. 4.20 with the bias current, I_{bias}, of 0.613 mA.

4.2.4 Frequency-Domain Output Impedance Measurement

The frequency response of the output impedance of the current mirror of Fig. 4.16 was measured using an impedance analyzer, 4294A, and is shown in Fig. 4.22. This shows how the bias current affects the frequency response and thermally induced non-ideality.



(a)



(b)

Figure 4.22 Frequency response of the output impedance, $Z_O(s)$, of Fig. 4.20, UTA213, with (a) I_{bias} = 613 μA. (b) I_{bias} = 225 μA.

The close inspection of the plots in Figs. 4.22(a) and 4.22(b) shows that the thermally induced "zero" frequency for both cases is almost the same, ~3 kHz. However, there is

a clear difference in the low-frequency output resistance and in the location of the intrinsic pole frequency. The low-frequency output resistance and intrinsic pole frequency from Fig. 4.22(a) are 112 kΩ and 40 kHz, while those from Fig. 4.22(b) are 347 kΩ and 15 kHz, respectively. Since the dc and low-frequency output resistance are higher than a simple current mirror at the same bias current, the percentage degradation in the magnitude of output resistance is lower in comparison with the simple current mirror of Fig. 4.2. This confirms the theory developed in (4.11). The high frequency response is indeed governed by the single-pole first-order system characteristics, much like the simple current mirror. But the non-ideal effects noticeable between 10 kHz and 100 kHz in Fig. 4.22 is because of thermally induced "zero-pole" doublet.

4.3 Thermal Effects of Self-Heating on High Performance Current Mirrors

4.3.1 Design, Simulation and Layout of Cascode Current Mirror

Section 3.5.1 shows that the cascode connection achieves a very high output resistance. Since this is a desirable characteristic of a current mirror, understanding the thermal effects caused by self-heating is important. A bipolar transistor current mirror based on the cascode connection is shown Fig. 4.23.

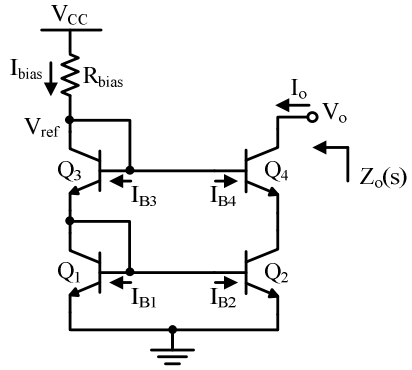


Figure 4.23 Cascode current mirror using bipolar transistors [7].

The output resistance of a cascode current mirror can be found from a routine circuit analysis and expressed as [47]

$$R_o = r_{o4}\left(1+\beta_4\left(\frac{r_{o4}}{\frac{\alpha_1}{g_{m1}}+\frac{\alpha_3}{g_{m3}}+r_{\pi 4}+r_{O2}}\right)\right) \cong r_{o4}\cdot\left(1+\beta_4\right) \qquad (4.12)$$

where it is assumed that $g_{m4}r_{o2} >> 1$. Thus, the output resistance is increased by the factor of $(1+\beta_4)$ over the output resistance of a simple current mirror. An expression for the output admittance of the cascode current mirror of Fig. 4.23 can be approximated using (4.11), replacing g_E with the output conductance of Q_2, g_{o2}, defined as I_o/V_A (V_A is the Early voltage). Details on the output impedance of the cascode connection are provided in section 3.5. As g_{o2} becomes small, the magnitude of $y_{thermal\_re}$ in (4.11) can be very small or even becomes negative. As a consequence, the low-frequency error due to dynamic self-heating will be highly suppressed

For the design of the current mirror of Fig. 4.23, each transistor has an emitter area of 40.0 μm^2, bias current, I_{bias}, is 225.0 μA, and output voltage, V_o, is 2.0 V. The simulation is done with the VBIC model provided in Table 2.9 with R_{th} = 375 K/W, C_{th} = 16.9 nJ/K. The magnitude response versus frequency is shown in Fig. 4.24.

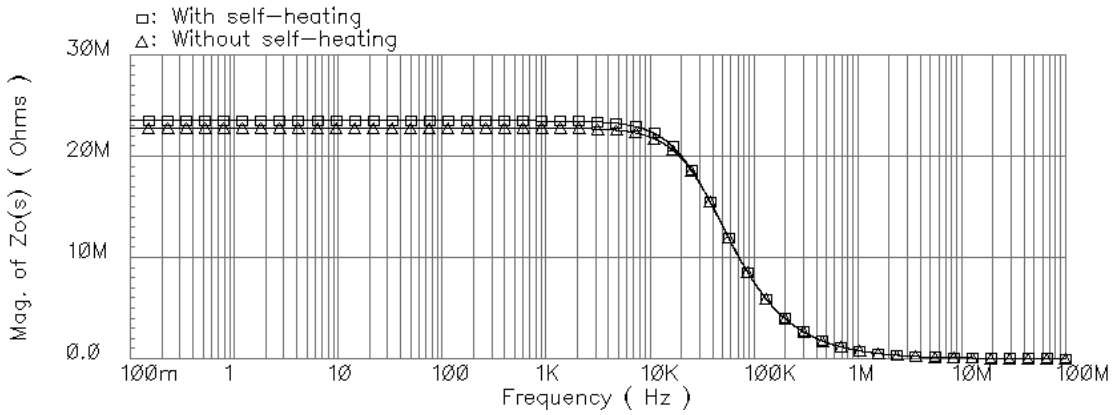


Figure 4.24 Magnitude response of the output impedance of cascode current mirror of Fig. 4.23 with and without self-heating.

It is clearly seen that the cascode current mirror offers very high output resistance with no peaking in frequency response. Ironically, it offers slightly higher output resistance with self-heating than without self-heating. This is opposite to what was found in all other current mirrors.

The current mirror of Fig. 4.23 was laid out as shown in Fig. 4.25 and fabricated with the VIP10™ bipolar process technology. All transistors had an emitter area of 40.0 μm^2, and bias resistor, R_{bias} is 2 kΩ. The die was placed within a DIP package.

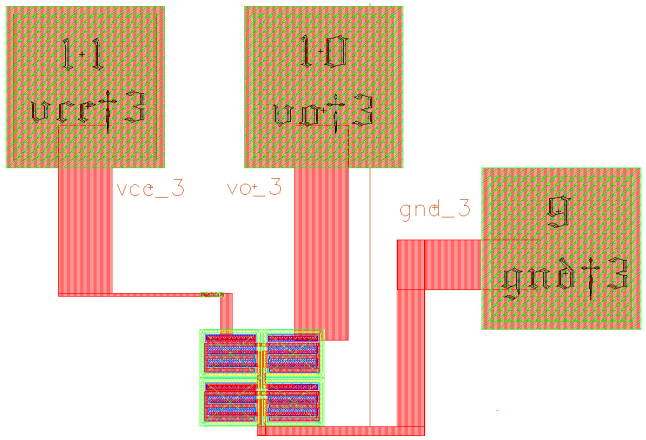


Figure 4.25 Layout of the cascode current mirror of Fig. 4.23 using the VIP10™ bipolar process technology [50].

4.3.2 Design, Simulation and Layout of a Wilson Current Mirror

The Wilson current mirror, shown in Fig. 4.25, is a special type of circuit [7] in which there is a negative feedback through Q_2, activating Q_1 to reduce base current error in Q_3 and raise the output resistance of the overall circuit at the collector of Q_3.

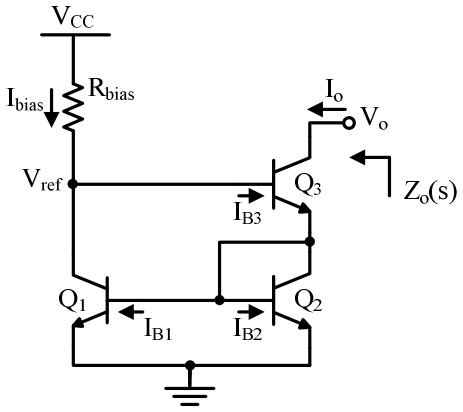


Figure 4.26 Wilson current mirror using bipolar transistor [7].

Due to its ability to regulate the output current, I_o, it offers high output resistance, which can be expressed as [7]

$$R_o = \frac{1}{2g_{m2}} + r_{o3} + \frac{g_{m3}r_{\pi 3}r_{o3}}{2} \approx \frac{\beta_0 r_{o3}}{2} \tag{4.13}$$

For this design, each transistor emitter area is 40.0 μm^2, bias current, I_{bias}, is 225.0 μA, and voltage at the output is set to 2.0 V. The simulation for the magnitude response of the output impedance is shown in Fig. 4.27.

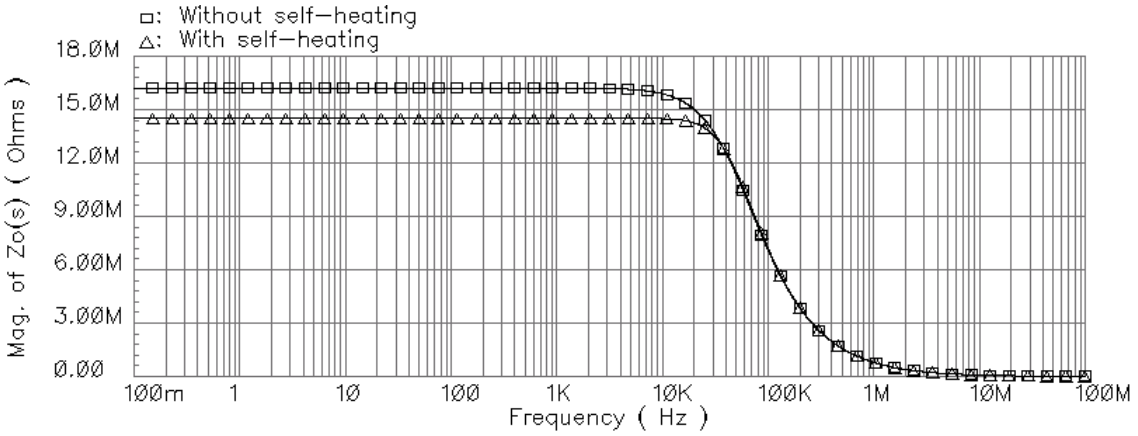


Figure 4.27 Magnitude response of the output impedance of the Wilson current mirror of Fig. 4.26 with and without self-heating.

The current mirror of Fig. 4.26 was laid out as shown in Fig. 4.28 and fabricated with the VIP10^{TM} bipolar process technology. The die was placed within a DIP package.

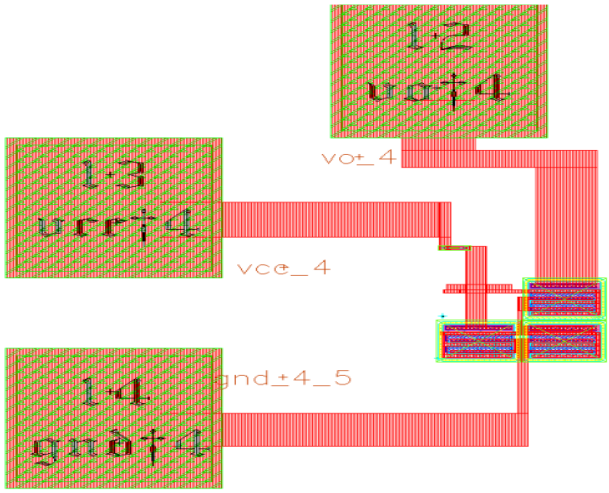


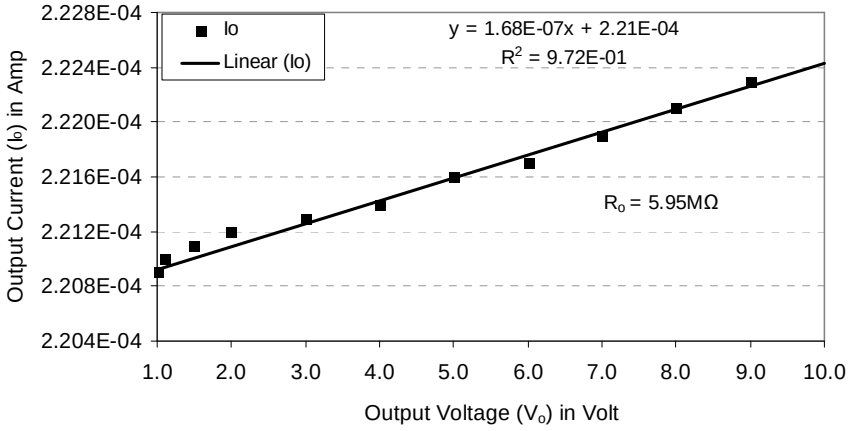
Figure 4.28 Layout of the Wilson current mirror of Fig. 4.26 using the VIP10^{TM} bipolar process technology [50].

4.3.3 DC Output Resistance Measurement

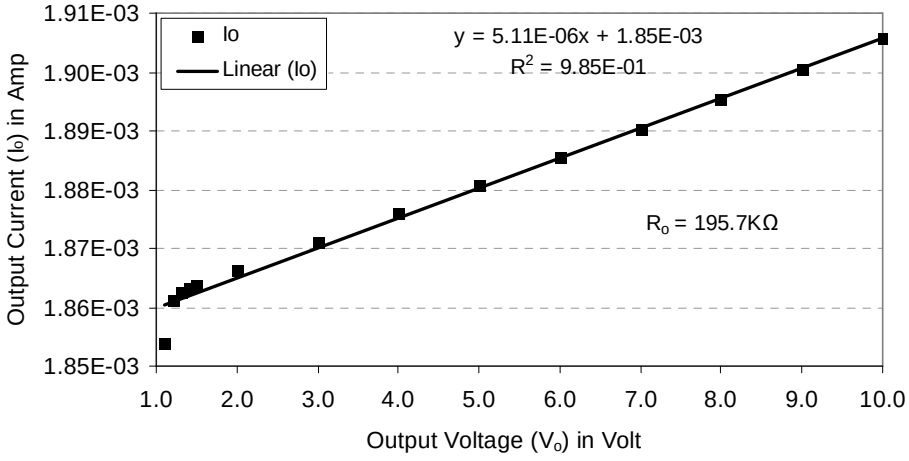
4.3.3.1 Cascode Current Mirror

The dc output resistance of the current mirror of Fig. 4.23 was measured by setting V_{CC} to 2.0 V, and 5.0 V to yield bias current of 230.0 μA, and 1.92 mA,

respectively. For each case, the voltage at V_O of Fig. 4.23 was varied from 1.0 V to 10.0 V using a power supply, Agilent E3631A. The measurement result is shown in Fig. 4.29.



(a)



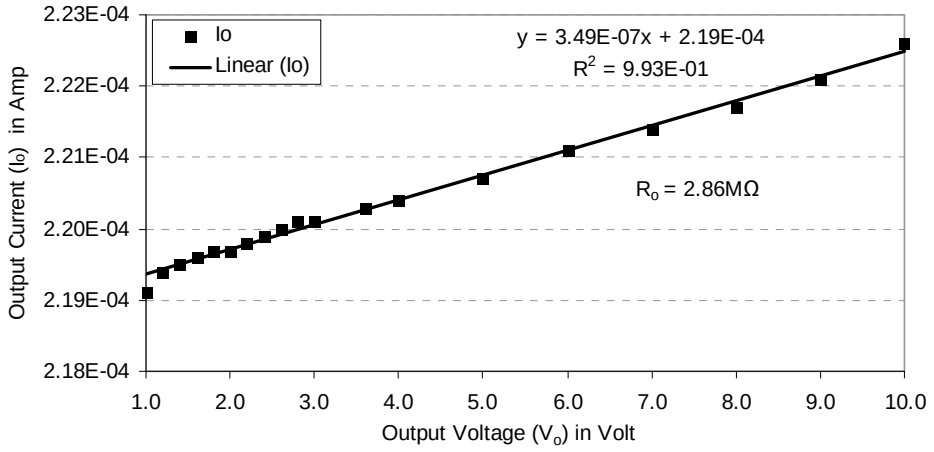
(b)

Figure 4.29 Output current versus output voltage for the cascode current mirror of Fig. 4.25 with (a) I_{bias} = 230 μA. (b) I_{bias} = 1.925 mA.

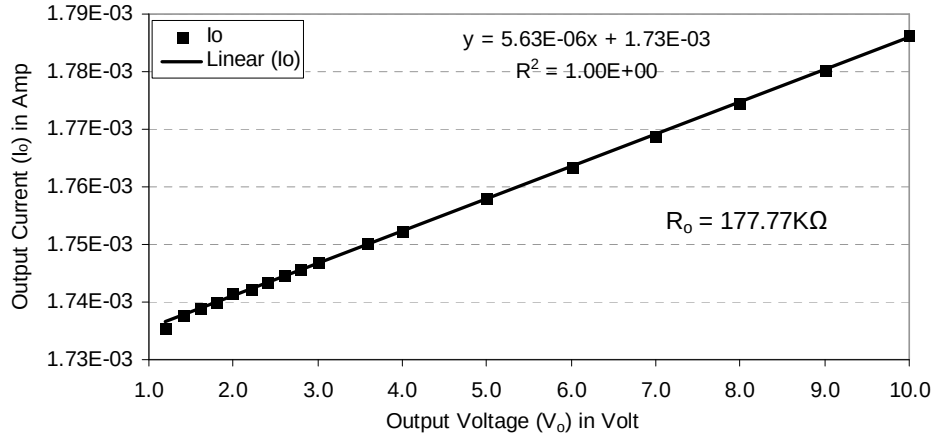
The measurement data is curve fitted with a linear approximation and the dc resistance was found to be 5.95 MΩ with I_{bias} = 230.0 μA, and 1.975 MΩ with I_{bias} = 1.925 mA. It is clearly seen that the dc output resistance is highly dependent on the bias current.

4.3.3.2 Wilson Current Mirror

Likewise, the dc output resistance of the current mirror of Fig. 4.26 was measured by setting V_{CC} to 2.0 V, and 5.0 V to yield bias current of 222.0 μA, and 1.86 mA, respectively. For each case, the voltage at V_o of Fig. 4.26 was varied from 1.0 V to 10.0 V. The measurement result is shown in Fig. 4.30.



(a)



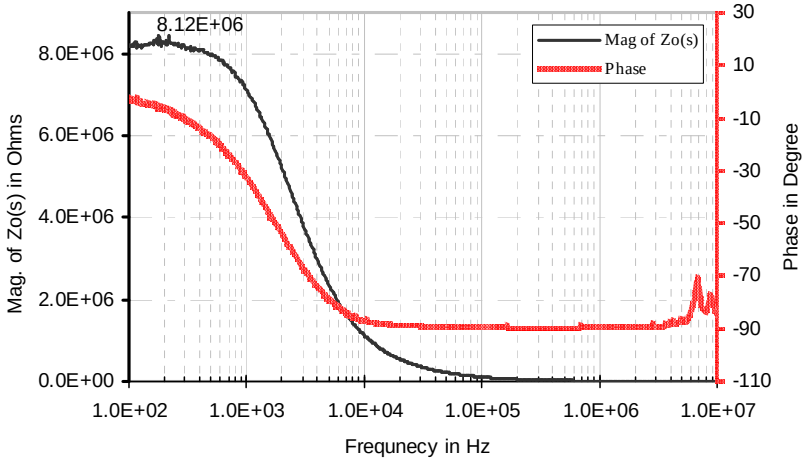
(b)

Figure 4.30 Output current versus output voltage for the Wilson current mirror of Fig. 4.28 with (a) I_{bias} = 222 μA. (b) I_{bias} = 1.86 mA.

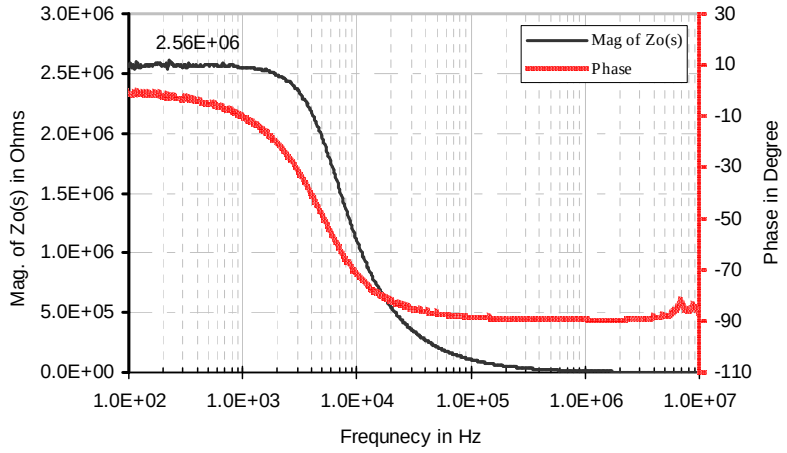
The measurement data is curve fitted with a linear approximation and the dc resistance was found to be 2.86 MΩ with I_{bias} = 222.0 μA, and 177.7 MΩ with I_{bias} = 1.86 mA. This also shows that dc output resistance is dependent on the bias current.

4.3.4 Frequency-Domain Output Impedance Measurement

The measured frequency response of cascode current mirror of Fig. 4.23 and Wilson current mirror of Fig. 4.26 is shown in the Fig 4.31.



(a)



(b)

Figure 4.31 Frequency response of the output impedance, $Z_O(s)$, of (a) cascode current mirror with I_{bias} = 230 μA (b) Wilson current mirror with I_{bias} = 222 μA of UTA213.

These responses do not show thermally induced non-ideal peaking effects, unlike the simple current mirror with and without emitter degeneration due to self-heating. But it is noteworthy to mention that these current mirrors are severely bandwidth limited. It is simply because of the higher output resistance offered by Wilson current mirror – $r_o\beta_0$, and cascode current mirror – $r_o\beta_0/2$ [7]. This clearly shows the possibility of thermally induced zero-pole cancellation, and hence there is no peaking effect.

4.4 General Recommendations to Designers

The primary emphasis of this section is to compare pros and cons of the four well-known topologies for current mirrors, in the design of analog integrated circuits, from the self-heating perspective. Fig. 4.32 shows a composite plot for the simulation of the magnitude response of four current mirrors with the same biasing current of 225 μA with and without the self-heating effect so as to compare their performance.

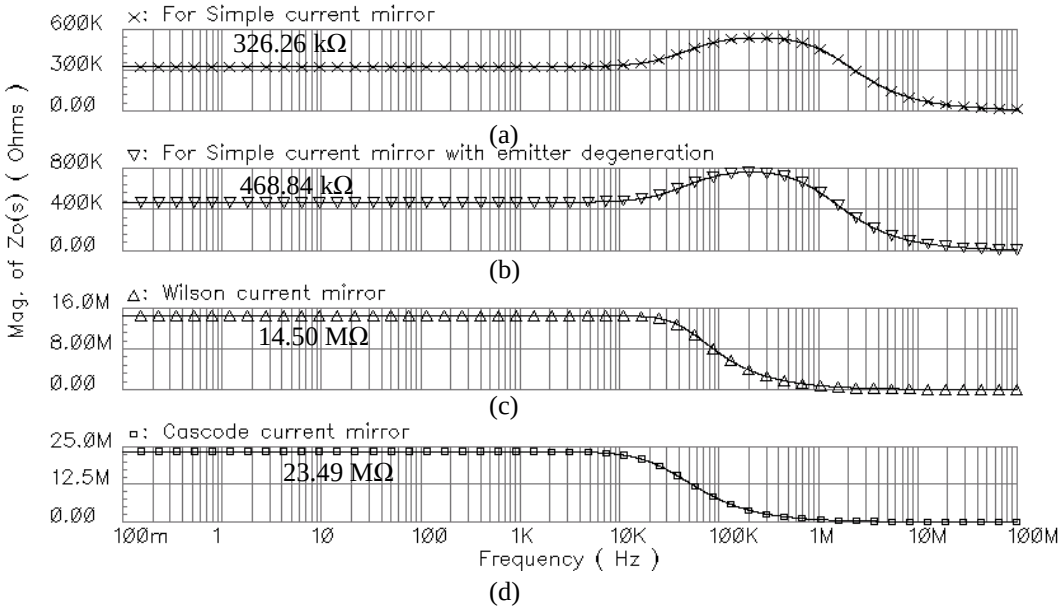


Figure 4.32 Magnitude response of the output impedance with and without self-heating for (a) simple (b) emitter degeneration (c) Wilson (d) cascode current mirror with identical I_{bias} = 225 μA.

This clearly shows how the effect of self-heating is diminishing as the intrinsic output resistance of the current mirror increases. It also shows that the thermally induced peaking does not exist with Wilson and cascode current mirrors, provided the bias current is not too high (in the range of mA). This has further been substantiated through the frequency-domain measurement of current mirrors (UTA213) shown in Fig. 4.33.

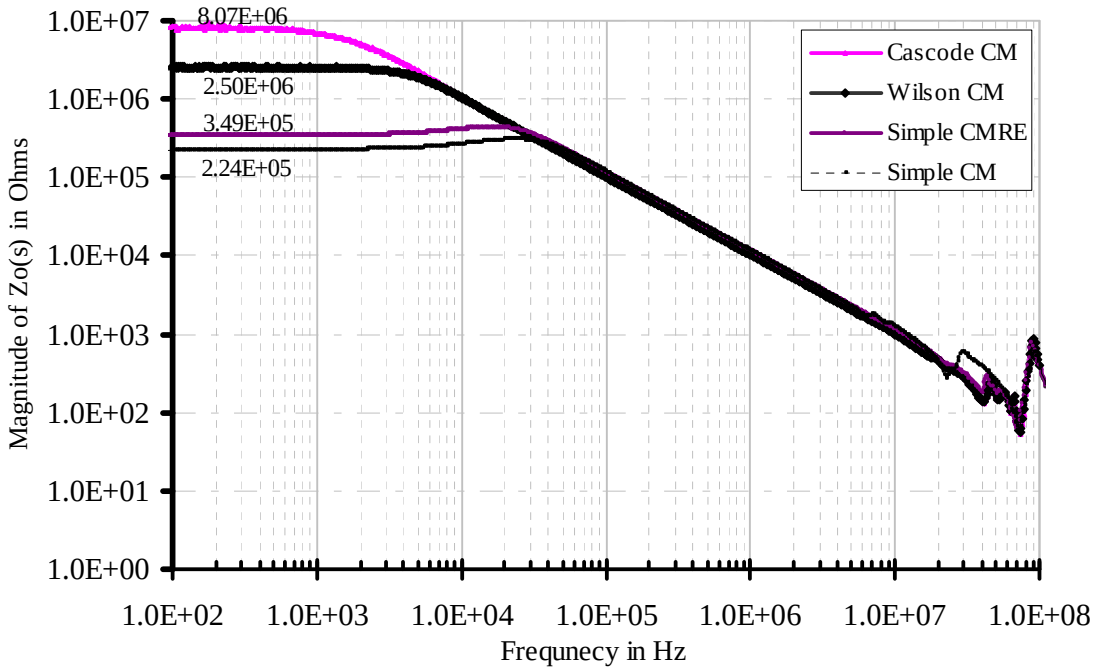


Figure 4.33 Comparison of the frequency response of $Z_O(s)$ of all current mirrors (on UTA213) with same bias current, I_{bias} = ~225 μA. CM stands for current mirror.

The large reduction in the magnitude of the output resistance of simple and emitter degeneration current mirrors as illustrated by both simulation in Fig. 4.32 and measurement in Fig. 4.33. This reduction in the output resistance is simply because of the higher magnitude of thermally induced component of effective output admittance given by 4.11. The peaking in the frequency response is caused by the thermally induced close by zero and pole. The pole-zero factor, as discussed in chapter 3, needs to

be minimized to reduce such non-ideal effects. Since the location of a thermally induced "zero" is almost static (minimal change is found) for a specific process technology based on a thermal time constant, the "pole-zero" factor can only be minimized by reducing the magnitude of the intrinsic dominant pole, which imposes bandwidth limitation.

From the analysis and extensive measurement, this peaking in the magnitude response of $Z_o(s)$ is not only found in simple current mirrors, but also in Wilson and cascode current mirrors under high bias current. However, such peaking is not dominant in these high performance current mirrors, such as Wilson and cascode current mirrors. A thermally induced "zero" imposes a constraint on the achievable bandwidth in amplifier circuits. Thus, the dynamic self-heating is indeed a problem for wideband amplifier circuits using bipolar current mirrors.

It has been proved through both the simulation and measurement that both the reduction in output resistance below thermal-cutoff frequency and the non-ideal peaking between thermal-cutoff frequency and intrinsic device pole frequency, can be minimized by moving the intrinsic device pole toward the thermal cutoff frequency by increasing the output resistance of the current mirror.

4.5 Correlation between Simulation and Measurement

The correlation between the simulation using the VBIC model of the VIP10^{TM} process technology and measurement is summarized in Table 4.4. Both simulation and measurement shows that the static approach and frequency-domain approach give a very close output resistance for all four current mirrors as show in Table 4.4. Measured

and simulated output resistance correlate well within 5% for simple current mirror with and without emitter degeneration, while the correlation is worse for the Wilson and Cascode current mirror.

Table 4.4 Comparison of the Output Resistance for Current Mirrors between Simulations using the VIP10^{TM} VBIC Model and Measurements.

Types of Current Mirror (CM)	**I_{bias} in μA**	**Simulation using VBIC model**		**Measurement**	
		DC R_{out}	AC R_{out}	DC R_{out}	AC R_{out}
Simple Current Mirror	225	264.6 kΩ	268.3 kΩ	230 kΩ	225 kΩ
Simple Current Mirror with R_E = 50 Ω.	225	372.2 kΩ	385.7 kΩ	353 kΩ	349 kΩ
Wilson current mirror	225	4.29 MΩ	4.22 MΩ	2.86 MΩ	2.50 MΩ
Cascode current mirror	225	31.2 MΩ	30.9 MΩ	5.95 MΩ	8.07 MΩ

4.6 Summary

A detailed study of the thermal effect of dynamic self-heating on current mirrors has been presented in this chapter. This work confirms through analytical formulations, simulations, and measurement that a current mirror with high output resistance can be helpful to minimize the thermal effect of self-heating. All of the current mirrors are simulated with the SPECTRE simulator using the physics based VBIC model. However, designs are fabricated with the National's VIP10^{TM} proprietary bipolar process technology. A very good correlation is found between the output resistances measured through a static (dc) approach and frequency-domain approach. Theoretical analysis, simulations, and measurement correlate quite well. This analysis forms a basis for the modeling of the frequency-domain non-ideal thermal effect of self-heating in current mode analog circuits, such as CFOA using bipolar transistors.

CHAPTER 5

THERMAL EFFECTS OF SELF-HEATING ON HIGH-SPEED OPERATIONAL AMPLIFIER DESIGN

Current Feedback Operational Amplifier (CFOA) is a quite popular amplifier topology [48] because of its superior performance over its counterpart, the Voltage Feedback Operational Amplifier (VFOA) in terms of bandwidth and slew rate [22], [53]. It finds wide application in high-speed analog signal processing, such as video processing and in automatic gain control applications. It has better differential gain and phase performance than the VFOA, and its bandwidth is independent of gain [53].

The time dependent offset-voltage and gain error characteristics of a CFOA caused by the thermal effect of static self-heating was studied extensively by Abhijit [17]. As an extension, this work will address the frequency-domain non-ideal thermal effects. The classical topologies of the CFOA [52], [53] are designed, and the frequency-domain thermal effects of self-heating on the key performance parameters, such as such as the open-loop transimpedance gain, common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), are studied. Time-domain thermal effects of self-heating will also be investigated using the large-signal step response of the CFOA, configured in the non-inverting unity gain configuration. Few simulation test circuits are provided for the simulations of the frequency response of the open-loop transimpedance, CMRR, and PSRR of the CFOAs.

5.1 High-Speed Current-Feedback Operational Amplifier

A simplified classical topology of a CFOA is shown in Fig. 5.1. Its operation is solely dependent on the matching characteristics of *npn* and *pnp* devices. Thus, the modern high speed complementary bipolar processes, such as VIP10^{TM} or XFCB, are the best option to take full advantage of this architecture. However, these process technologies impact the circuit's performance because of the associated self-heating effect of such circuits. Self-heating affects current mirrors and the high-gain node, Z, of Fig. 5.1. These are encircled with a dotted line as shown in Fig. 5.1.

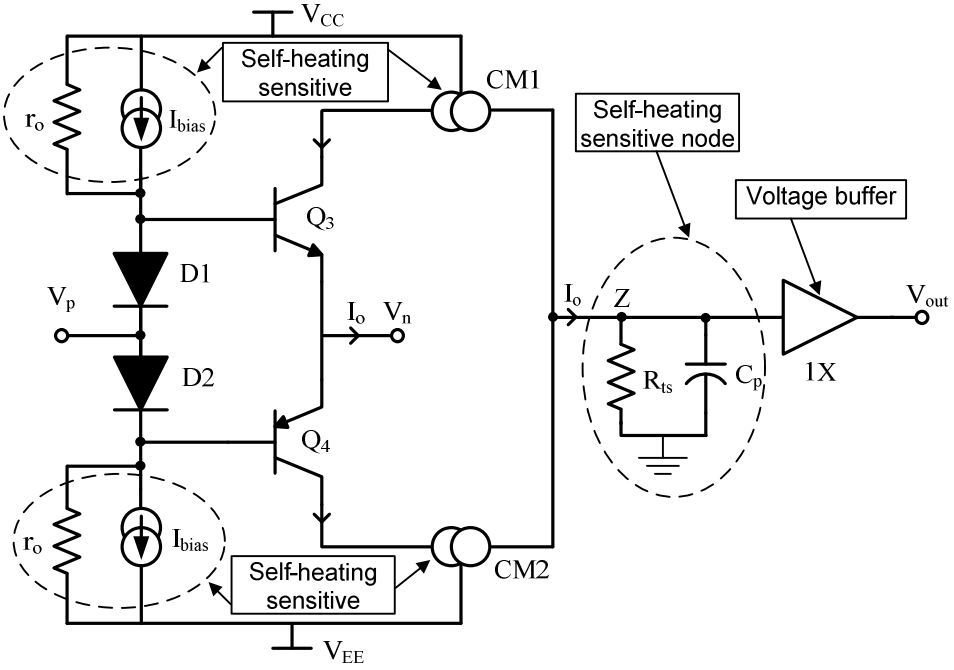


Figure 5.1 Simplified current-feedback amplifier architecture [52], [54].

The current mirror is a good example of circuits which can switch or steer current with a minimum amount of delay. Any generic current feedback amplifier's topology is simply the application of the fundamental principles of current steering [54].

It exploits a circuit topology that emphasizes current-mode operations, which is inherently much faster than voltage-mode operation. It is less prone to the effect of stray node-capacitances. However, it is prone to self-heating induced thermal effects unless design considerations are exercised.

As shown in Fig. 5.1, the non-inverting input V_p, is a high impedance terminal and is buffered directly to the inverting input V_n, through the complementary emitter follower buffers, Q_3 and Q_4. The inverting input impedance at V_n should be in the range of 10 Ω and 100 Ω depending on the sizes of transistors and bias current. Ideally, it is assumed to be zero for the sake of analysis. This is one of the most fundamental distinguishing differences between a CFOA and a VFOA, and also a feature which gives the CFOAs some unique advantages [54].

The collectors of Q_3 and Q_4 drive current mirrors which mirror the inverting input current to the high impedance node, modeled by R_{ts} and C_p. The high impedance node is buffered by a unity gain push-pull buffer. Feedback from the output to the inverting input (not shown in Fig. 5.1) acts to force the inverting input current to zero, hence the term “current feedback”.

5.1.1 Classical CFOA Circuit Topology

A circuit level implementation of the classical current feedback operational amplifier is shown in Fig. 5.2. It has three fundamental stages [48]: an input voltage buffer (Q_5-Q_8), an intermediate transimpedance stage (Q_9-Q_{10}) and (Q_{11}-Q_{12}), and an output voltage buffer (Q_{13}-Q_{16}). The input V_p, and the output V_n, of the input buffer (Q_5-Q_8) constitute the non-inverting and inverting input terminals of the CFOA.

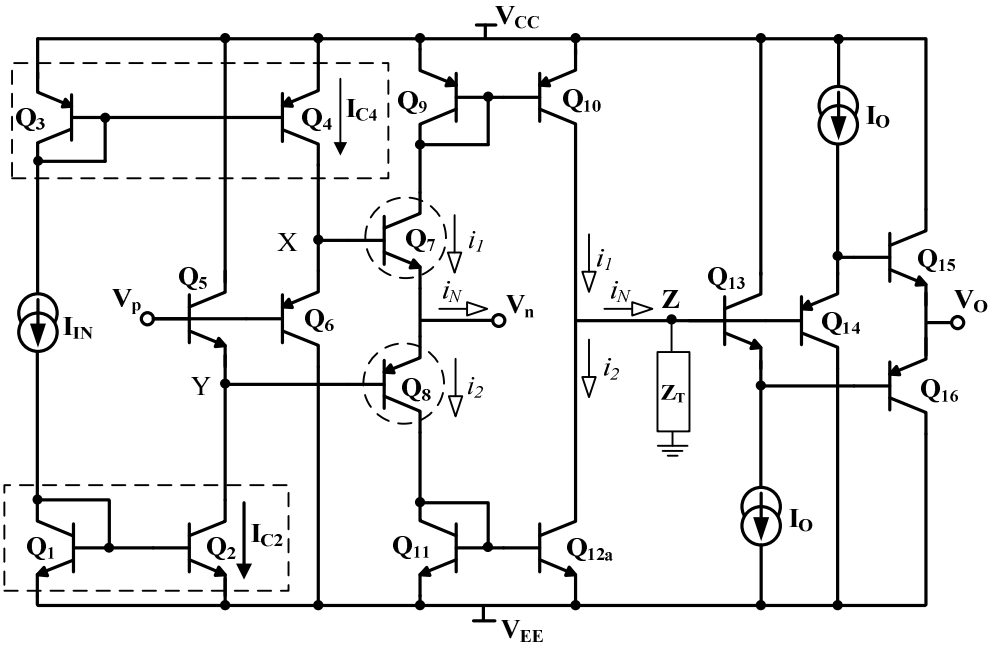


Figure 5.2 Classical CFOA circuit [52], [53]-[55].

The central transimpedance stage converts the current, which flows out of the inverting input, V_n of the CFOA, into a voltage across a high-impedance node, *Z*. This determines the transresistance gain of the CFOA. The output voltage buffer, Q_{13}-Q_{16} simply buffers the '*Z*' node voltage to the output, V_o with the desired low output impedance for external load driving. Since both the input buffer and output buffer are translinear circuits [21], their performances are strongly dependent on the matching of the V_{BE}s in the translinear loop formed by transistors Q_5 through Q_8 and transistor Q_{13} through Q_{16} in Fig. 5.2. The intermediate stage consists of two current mirrors formed by Q_9-Q_{10} and Q_{11}-Q_{12}, whose output impedances are reduced by dynamic self-heating [5], [15], and [19]. Fig. 5.3 shows the classical CFOA circuit in which intermediate stage consists of two Wilson current mirrors formed by Q_9-Q_{10a}-Q_{10b} and Q_{11}-Q_{12a}-Q_{12b}, whose output impedances will be least impacted by the dynamic self-heating.

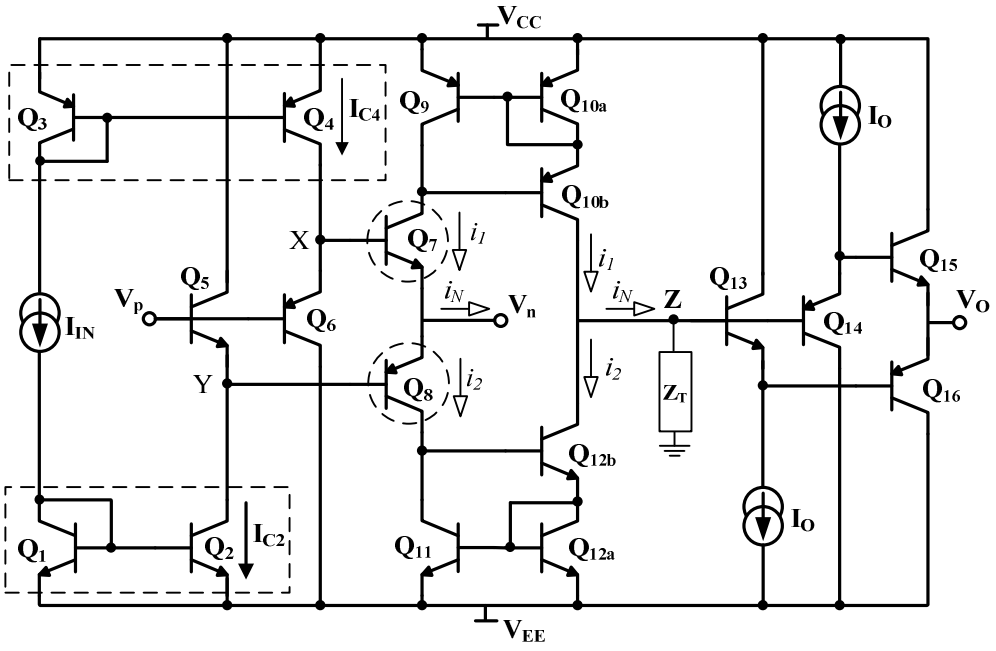


Figure 5.3 CFOA circuit with intermediate stage based on Wilson current mirrors [22], [48], and [55].

5.1.2 Small-Signal Macromodel of a CFOA

The small-signal macromodel for a typical CFOA when used in the non-inverting closed-loop gain configuration is shown in Fig. 5.4.

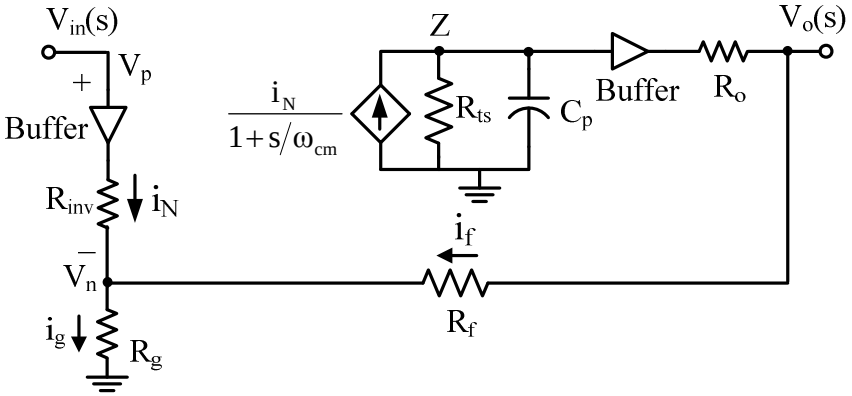


Figure 5.4 Small-signal macromodel of a generic CFOA in the non-inverting closed-loop configuration [57]-[58].

The equivalent resistance, R_{ts}, and parasitic capacitance, C_p, are located at the high-gain node, Z, where ω_{cm} represents the current mirror pole frequency. The output resistance of the input voltage buffer, R_{inv}, is the input resistance at the inverting input terminal, V_n, and the output resistance of the output voltage buffer, R_o, is the output resistance of the CFOA. As shown in Fig. 5.2, the inverting input resistance, output resistance, and transresistance gain of the CFOA can be expressed as [48]

$$R_{inv} = \frac{1}{g_{m7} + g_{m8}} \approx \frac{V_T}{2I_{IN}} \tag{5.1}$$

$$R_o = \frac{1}{g_{m15} + g_{m16}} \approx \frac{V_T}{2I_o} \tag{5.2}$$

$$R_{ts} = r_{os10p} \,||\, r_{os12n} \tag{5.3}$$

where V_T is thermal voltage, I_{IN} and I_o are the quiescent currents in the input and output buffers, and r_{os10p} and r_{os12n} are the output resistance of the current mirrors, Q_9-Q_{10} and Q_{11}-Q_{12}, respectively. Since I_{IN} and I_o increase due to static self-heating as explained in chapter 3, the small-signal input resistance, r_{inv}, and output resistance, r_o, of the CFOA decrease. As formulated in chapter 3, the output impedance of the bipolar transistor, including the effects of dynamic self-heating, can be expressed as [58]

$$r_{os,i}(s) = \frac{r_{o,i}}{1 + \dfrac{g_{ct} \cdot (I_c + g_{oT} V_c) \cdot Z_{th}(s) \cdot r_{o,i}}{1 - (g_{ct} V_c + g_{bt} V_b) \cdot Z_{th}}} \tag{5.4}$$

where $r_{o,i}$ is the small-signal output resistance of the ith transistor without the effects of dynamic self-heating. The terms g_{ct}, g_{bt}, and g_{oT}, are the base and collector thermal transconductances, and the effective output conductance, respectively. The terms I_b, I_c,

V_b, and V_c are the instantaneous base, collector currents and voltages, respectively as discussed in chapter 3. The transimpedance, $Z_T(s)$, and loop-gain, $T(s)$, for the first order small-signal macromodel of Fig. 5.4 can be expressed as [55], [57]

$$Z_T(s) = \frac{R_{ts}}{1 + sR_{ts}C_p} \tag{5.5}$$

$$T(s) \approx \frac{Z_T(s)}{R_f + R_{inv} + R_o} \tag{5.6}$$

Since the value of transresistance, R_{ts}, may be decreased by self-heating, the magnitude of the transimpedance and loop-gain would also decrease. This impacts the gain error of the amplifier. The term for gain error is embedded by a dotted rectangle in the closed-loop non-inverting gain expression for Fig. 5.4 given by [57]

$$\frac{V_o(s)}{V_{in}(s)} = \left(1 + \frac{R_f}{R_g}\right) \cdot \boxed{\frac{1}{1 + \frac{1}{T(0)}}} \cdot \frac{1}{1 + s\frac{R_f R_{ts} C_p}{R_{ts} + R_f}} \tag{5.7}$$

Assuming R_f >> R_{inv} and R_o, and R_{ts} >> R_f, the 3-dB closed-loop bandwidth from (5.7) can be determined by

$$\omega_p = \frac{1}{R_f C_p} \tag{5.8}$$

The expression (5.8) shows that the closed-loop bandwidth of a CFOA is determined by the internal dominant pole capacitor, C_p, and the external feedback resistor, R_f. It is independent of the gain-setting resistor, R_g. This ability to maintain constant bandwidth independent of gain makes a CFOA well suited for wideband programmable gain amplifiers [54]. Because the closed-loop bandwidth is inversely proportional to the

external feedback resistor, R_f, the design of a CFOA is usually optimized for a specific R_f. Increasing R_f from its optimum value lowers the bandwidth, while decreasing it may lead to oscillation and instability because of high frequency parasitic poles [60]-[63].

5.1.3 Development of Stability Criterion

Unlike the VFOA, the CFOA requires a minimum resistance in the feedback path for stable operation in the closed-loop unity gain configuration. This minimum resistance is dependent on the order of the transfer function of high-gain node of the current-feedback amplifiers. This can be modeled with a multi-pole function. For simplicity, the transimpedance can be approximated with a two-pole function as shown in Fig. 5.4, and can be expressed as [57]

$$Z_T(s) = \frac{R_{ts}}{\left(1+\frac{s}{\omega_t}\right)\cdot\left(1+\frac{s}{\omega_{cm}}\right)} \tag{5.9}$$

where ω_t, and ω_{cm} are the dominant pole frequency at high-gain node, Z, and a current mirror pole frequency. The closed-loop gain for Fig. 5.4 can be expressed as

$$\frac{V_o(s)}{V_{in}(s)} = \left(1+\frac{R_f}{R_g}\right)\cdot\frac{\frac{R_{ts}}{R_f}\omega_t\omega_{cm}}{s^2+(\omega_t+\omega_{cm})s+\omega_t\omega_{cm}\frac{R_{ts}}{R_f}} \tag{5.10}$$

The closed-loop bandwidth reported by Mahattanakul [57] has been corrected (details can be found in Appendix D), and can be expressed as

$$\omega_{-3dB} = \omega_n\sqrt{\frac{\left(2-\frac{1}{Q^2}\right)+\sqrt{\left(2-\frac{1}{Q^2}\right)^2+4}}{2}} \tag{5.11}$$

where

$$\omega_n = \sqrt{\frac{R_{ts}}{R_f}\omega_t\omega_{cm}} = \sqrt{\frac{\omega_{cm}}{R_f C_p}} \tag{5.12}$$

$$Q = \sqrt{\frac{1}{R_f C_p \omega_{cm}}} \tag{5.13}$$

For the peaking free frequency response, the Q of (5.13) should be less than 0.707, and hence the criterion on R_f can be expressed as

$$R_f > \frac{2}{C_p \omega_{cm}} \tag{5.14}$$

This is one of the most important criteria which states that the minimum value of the feedback resistor, R_f, is inversely proportional to the parasitic capacitance at the high-gain node and the current mirror's dominant pole.

5.1.4 CMRR Formulations

The common-mode rejection ratio (CMRR), defined as the ratio of the magnitude of the differential gain to the magnitude of the common mode gain, can be expressed as [59]

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| = \frac{\left(g_{m7,8} + \frac{1}{r_{o7,8}}\right)}{\left(\frac{1}{r_{o4,2}} + \frac{1}{r_{o7,8}}\right)} \tag{5.15}$$

It can be inferred from (5.15) that the CMRR of the CFOA in Figs. 5.2 and 5.3 depends upon the output resistance of current mirrors, Q_1-Q_2 and Q_3-Q_4, which provides bias current transistors, Q_5 and Q_6, of the input buffer. It is also strongly dependent on the Early voltage or the output resistance of Q_7 and Q_8 because the collector current of

these transistors can be easily influenced by static self-heating. Thus, a higher value of output resistance (which minimizes the effect of self-heating) for Q_7 and Q_8 yields a better CMRR response. As explained in chapters 3 and 4, self-heating reduces the output resistance of a simple current mirror significantly. As a consequence, the CMRR will also be degraded.

5.1.5 Large-Signal Transient Response of a Buffer

The operating temperature of an SOI BJT can be expressed as [59]

$$T_{op}(t) = T_0 + P_{th}R_{th}\left[1 - exp\left(-\frac{t}{\tau_{th}}\right)\right] \tag{5.16}$$

where the terms T_0, R_{th}, C_{th}, $\tau_{th}=R_{th}C_{th}$, and $P_{th}=I_BV_{BE}+I_CV_{CE}$, are the ambient temperature, thermal resistance, thermal capacitance, thermal time constant of the device, and instantaneous power, respectively. From (5.16), it can be inferred that the operating temperature can reach the steady state temperature, $T_{op}=T_0+P_{th}R_{th}$ only after a finite delay of about $5\tau_{th}$. Since the V_{BE} of a transistor decreases with temperature [7], the magnitude of V_{BE} will also be a function of time. Fig. 5.5 shows a typical buffer.

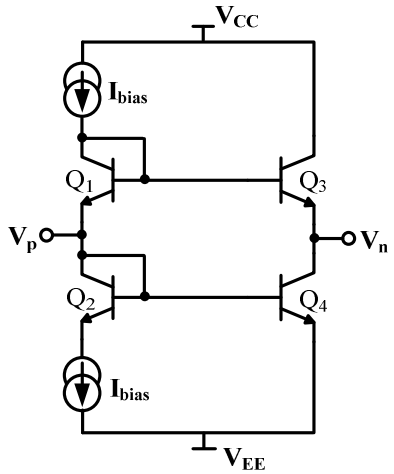


Figure 5.5 Class AB voltage buffer [7].

A large-signal step response of this buffer gets severely impacted by the mismatch in the base-emitter voltages, V_{BE}, of the bipolar transistors due to self-heating. If the transistors Q_1 and Q_3, and Q_2 and Q_4, of Fig. 5.5 are properly matched, the output V_n would follow the input V_p. But due to power mismatch between Q_1 and Q_3, and between Q_2 and Q_4 during a large-signal step excitation, there will be a localized time dependent temperature difference between these transistors, and hence there will be mismatch in the V_{BE} leading to the thermal tail as illustrated in Fig. 5.6.

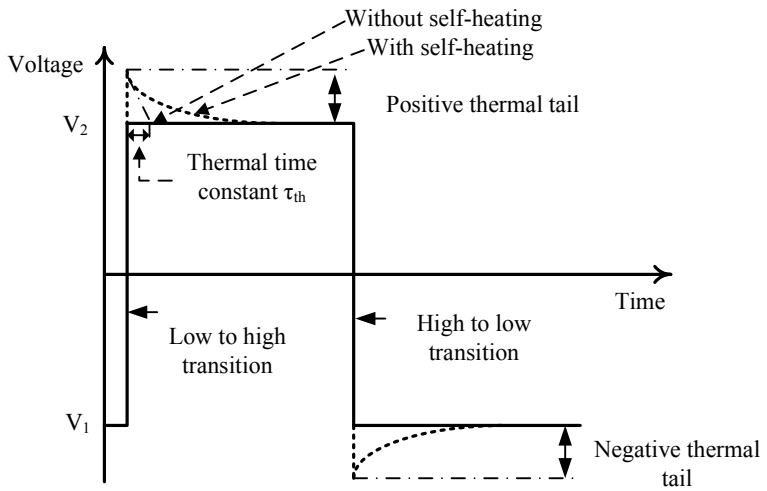


Figure 5.6 Typical step response of a voltage buffer shown in Fig. 5.5.

It is found from analysis provided in Appendix E that the magnitude of thermal tail for a voltage buffer can be expressed as

$$Th_{tail} = KI_{bias}R_{th} \cdot \left.\frac{dV_{BE}}{dT}\right|_{I_{bias}} \tag{5.17}$$

where K and I_{bias} are the technology dependent parameter and bias current for the buffer, respectively. Since the thermal resistance, R_{th}, can be reduced by increasing the area of the transistors, the magnitude of the thermal tail can also be reduced by

increasing the device area. Since both front-end and back-end stages of a CFOA are voltage buffers, the step response of a CFOA follows a similar response shown in Fig. 5.6 unless design care is taken.

5.1.5.1 Impact of Self-Heating on Slew Rate

In the theoretical analysis of the slew rate in current feedback amplifiers, the input stage is assumed to provide current out of inverting terminal on demand from power supplies through current mirrors, Q_1-Q_2, and Q_3-Q_4 of Figs. 5.2 and 5.3. Despite the first-order absence of limiting factor on the slew rate of a CFOA in Figs. 5.2 and 5.4, it is ultimately limited by the ability of Q_4 and Q_2 to supply the current necessary to charge the parasitic capacitances at the base of Q_7 and Q_8, respectively, and the parasitic capacitance of high-gain node, Z. The approximate expression for slew rate can be expressed as [22]

$$SR(pos) = \frac{I_{C4} - I_{B7}}{C_{eqX}} \tag{5.18}$$

$$SR(neg) = \frac{I_{C2} - I_{B8}}{C_{eqY}} \tag{5.19}$$

where I_{C4} and I_{C2} are the currents supplied by simple current mirrors, Q_3-Q_4, and Q_1-Q_2, respectively. The currents, I_{B7} and I_{B8} are the base currents of transistors, Q_7 and Q_8, respectively. The capacitances, C_{eqX} and C_{eqY} are the equivalent parasitic capacitances at node X and Y of Figs. 5.2 and 5.3. Since the performance of a current mirror can be influenced by self-heating, the slew-rate will also be impacted. There may be better slew rate with a higher bias current, but the self-heating effect will dominate the overall performance of the CFOA.

5.2 Simulations and Characterization of the Self-Heating Thermal Effect on the Classical CFOA

For all simulations illustrated in this chapter, the bias currents, I_{IN} and I_O, of Figs 5.2 and 5.3 were set to 250 μA with power supply voltages of V_{CC} = +5 V, and V_{EE} = −5 V. All simulations were based on the VBIC models provided in Tables 2.9 and 2.10. The 1x device represents a transistor with an emitter area of 5 μm^2. The thermal time constant used in the VBIC model was 5 μs with a thermal resistance of 3000 K/W, and thermal capacitance of 1.69 nJ/K for the 1x devices. All transistors of Figs. 5.2 and 5.3 were 8x devices, so that thermal resistance and capacitance scale accordingly.

5.2.1 Effects of Dynamic Self-Heating on the Open-Loop Transimpedance

The intermediate stage of a CFOA is basically implemented with current mirrors, and hence the effect of dynamic self-heating on its frequency response should have the similar effect as current mirrors have. The simulation setup shown in Fig. 5.7 can be used to simulate the frequency response of the open-loop transimpedance, $Z_T(s)$, of a CFOA.

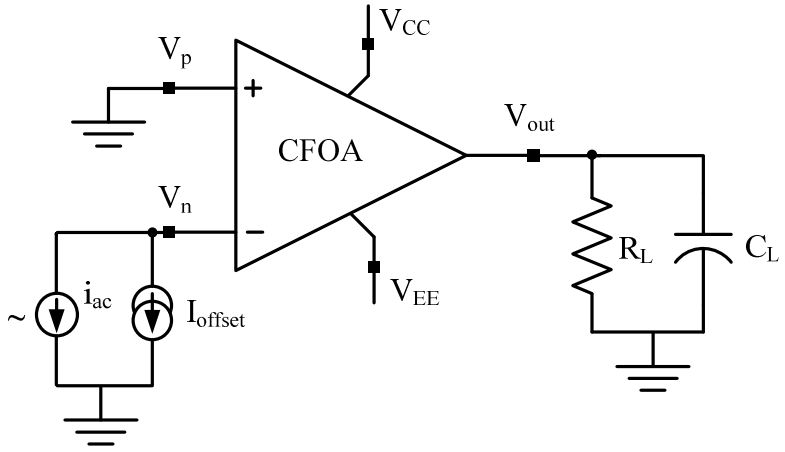


Figure 5.7 Simulation setup for the open-loop transimpedance of a CFOA [47].

The dc current source, I_{offset}, at the inverting terminal is swept with the non-inverting input grounded to find the offset current such that voltage at the output becomes zero. This ensures proper dc bias for all transistors within the CFOA in the open-loop configuration. Upon finding the required value of the dc offset current at the inverting input terminal, an ac current source is connected in parallel with dc current source as shown in Fig. 5.7. With this setup, the magnitude versus frequency response for the open-loop transimpedance can be obtained by taking the ratio of output voltage to the ac input current. Fig. 5.8 shows the magnitude response of $Z_T(s)$ of the CFOA of Fig. 5.2.

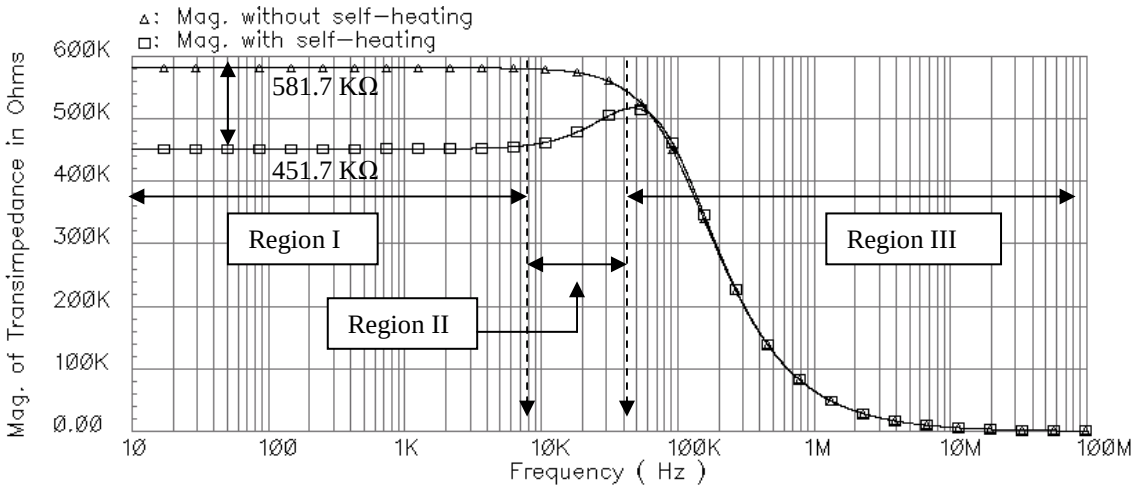


Figure 5.8 Magnitude response of the transimpedance of the CFOA in Fig 5.2, modeled with and without self-heating.

Like the frequency response of the output impedance of a simple current mirror, region I represents the range of frequencies lower than thermal cutoff frequency, f_{th} [4], where the effective transresistance is severely impacted (reduced by about 22%) due to the dynamic self-heating. As the frequency becomes higher than f_{th} (31.8 kHz), the effect of dynamic self-heating starts to diminish, letting the magnitude response be as if there is no effect of self-heating at all. This is illustrated in region II. The inductive effect in

magnitude response immediately after the thermal cutoff frequency is due to the thermally induced "zero-pole doublet" in the effective transfer function of $Z_T(s)$. In the high-frequency region III, the impedance response is governed by the intrinsic single-pole response of the high-gain node. In this region, the thermal effect is completely suppressed due to an equivalent low-pass filter nature of the thermal network.

The reduction in the transimpedance at low frequency and peaking effect around the thermal cutoff frequency can be mitigated by using Wilson current mirrors at the transimpedance stage. This can be verified through the open-loop transimpedance response illustrated in Fig. 5.9 for the CFOA of Fig. 5.3. The dc transimpedance with and without self-heating is 2.42 MΩ and 2.49 MΩ, respectively. Thus, there is a reduction of about 2.8% only in the magnitude of transresistance due to self-heating. The non-ideal peaking effects illustrated in region II of Fig. 5.8 disappears in Fig. 5.9 because the thermally induced zero and pole are so close to the intrinsic dominant pole that the peaking effect is cancelled due to pole-zero cancellation and the magnitude response is governed by the dominant intrinsic single-pole of the high-gain node, *Z*.

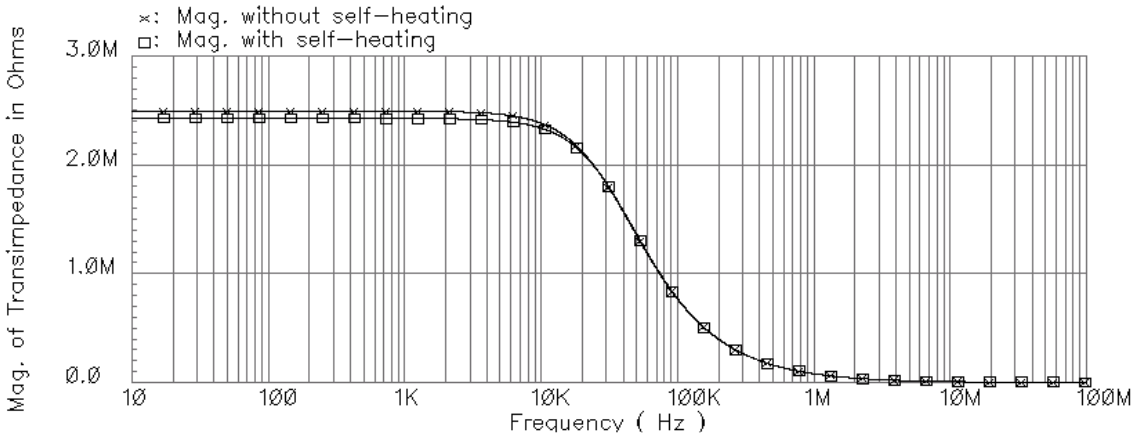


Figure 5.9 Simulated magnitude response of the open-loop transimpedance of the CFOA in Fig. 5.3, modeled with and without self-heating.

These thermal effects can further be reduced by using cascode current mirrors at the transimpedance stage. The composite frequency response of the open-loop transimpedance of the CFOAs of Fig. 5.2 and 5.3 is shown in Fig. 5.10 using the test circuit shown in Fig. 5.7 for a comparison.

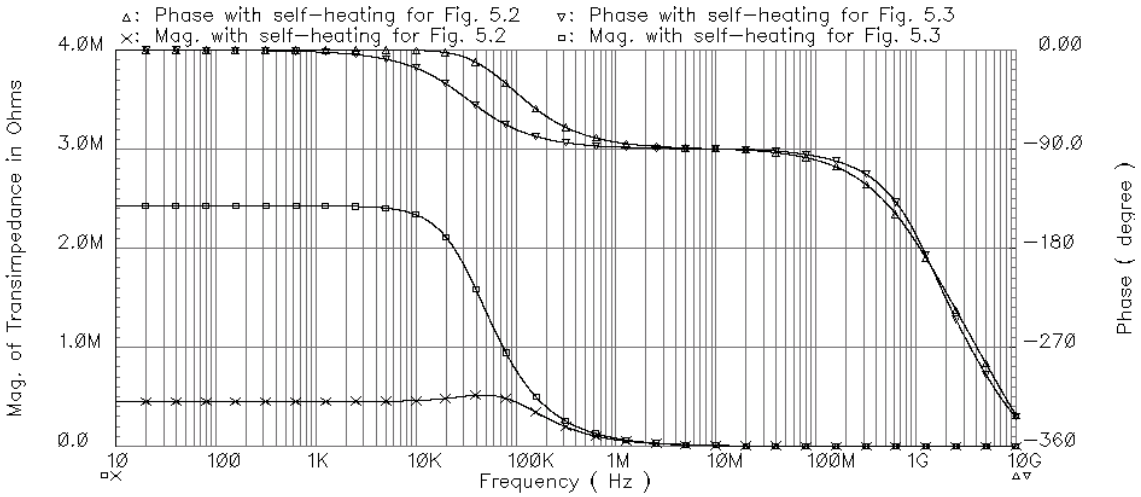


Figure 5.10 Simulated frequency response of the open-loop transimpedance of CFOAs of Fig. 5.2 with I_{offset} = 0.726 μA, and Fig. 5.3 with I_{offset} = – 7.156 μA.

The critical resistance, $R_{critical}$ [47] of a CFOA can be defined as the magnitude of transimpedance at the frequency where there is the phase shift of -180 degrees. From the simulation shown in Fig. 5.10, it can be inferred that the critical resistance for the CFOA in Fig. 5.2 is 43.13 Ω while that for the CFOA in Fig. 5.3 is 70.22 Ω.

This also reflects the minimum resistance that needs to be used as a feedback resistor when using a CFOA in non-inverting unity gain configuration to avoid oscillation. Practically, a much higher value of feedback resistor, R_f, is required to make the closed-loop response free of peaking in the frequency-domain and free of oscillations in the time-domain.

5.2.2 Frequency Response in the Closed-Loop Configuration

The non-inverting unity gain configuration of operational amplifiers is one of the very important configurations both for the design validation and for practical usage. Such a configuration for a CFOA is shown in Fig. 5.11.

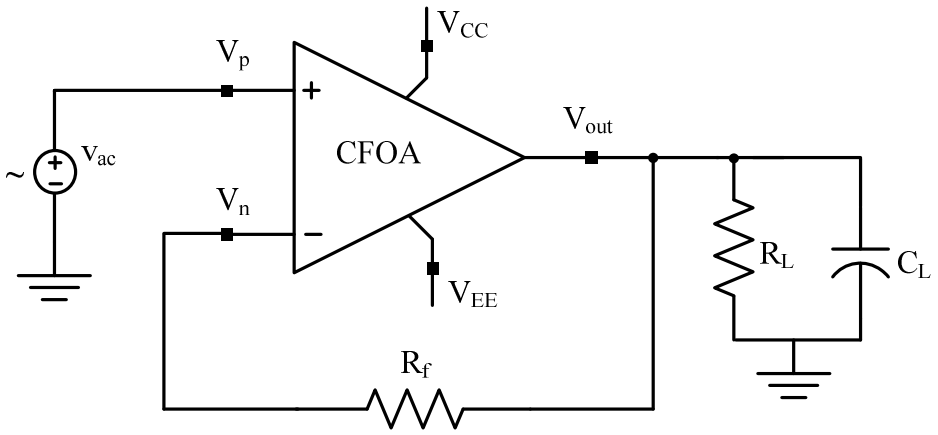


Figure 5.11 A CFOA in the non-inverting unity gain configuration [51].

The impact of feedback resistor, R_f, on the frequency response in the non-inverting unity gain configuration is shown in Fig. 5.12.

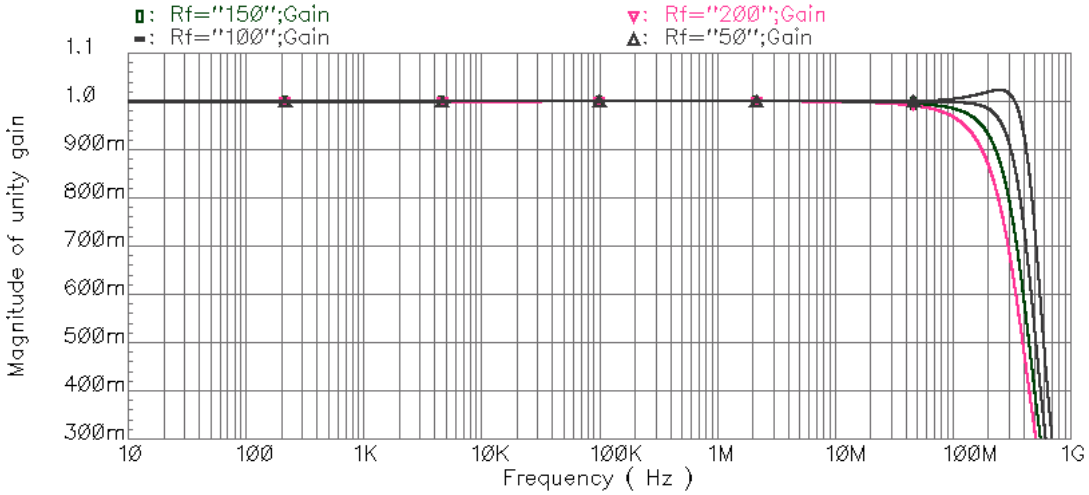


Figure 5.12 Simulated magnitude response for the CFOA of Fig. 5.2 in the non-inverting unity gain configuration with R_L = 25 kΩ and C_L = 0.35 pF.

As illustrated in Fig. 5.12, the peaking in frequency response can be controlled by the value of the feedback resistor. A higher value for the feedback resistor reduces the peaking at the expense of bandwidth, thus validating the theory (5.8). The maximum 3-dB bandwidth for the CFOA in Fig. 5.2 is 418.7 MHz for R_f = 100 Ω without peaking.

5.2.3 Effects of Dynamic Self-Heating on the Common-Mode Rejection Ratio

As evidenced by (5.14), the CMRR frequency response of a CFOA can be vulnerable to dynamic self-heating. The simulation setup shown in Fig. 5.13 can be used to simulate the frequency response of the CMRR of a CFOA.

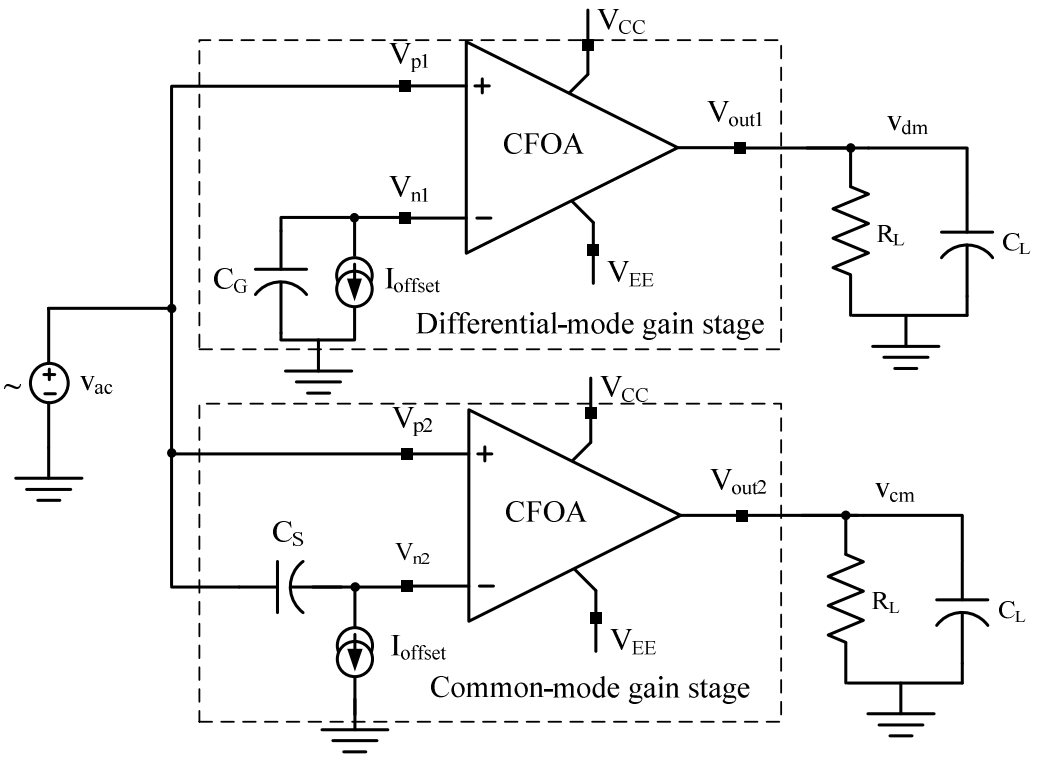


Figure 5.13 Simulation setup for the frequency response of CMRR in the open-loop configuration.

The dc current source, I_{offset}, is used to set V_{out1} and V_{out2} to zero dc wise so as to bias all transistors of the CFOAs in the active-region in the open-loop configuration. A large

value of capacitances, C_G and C_S, (in the range of 100s of μF) as shown in Fig. 5.13, are used to provide an ac short-circuit to get differential-mode response at node V_{out1}, and common-mode response at node V_{out2}, respectively. Assuming that the ac input signal, v_{ac} is 1.0 V, the ratio of the magnitude of v_{dm} over v_{cm} gives the CMRR. The CMRR responses of CFOAs of Figs. 5.2 and 5.3 are shown in Fig. 5.14, with and without self-heating.

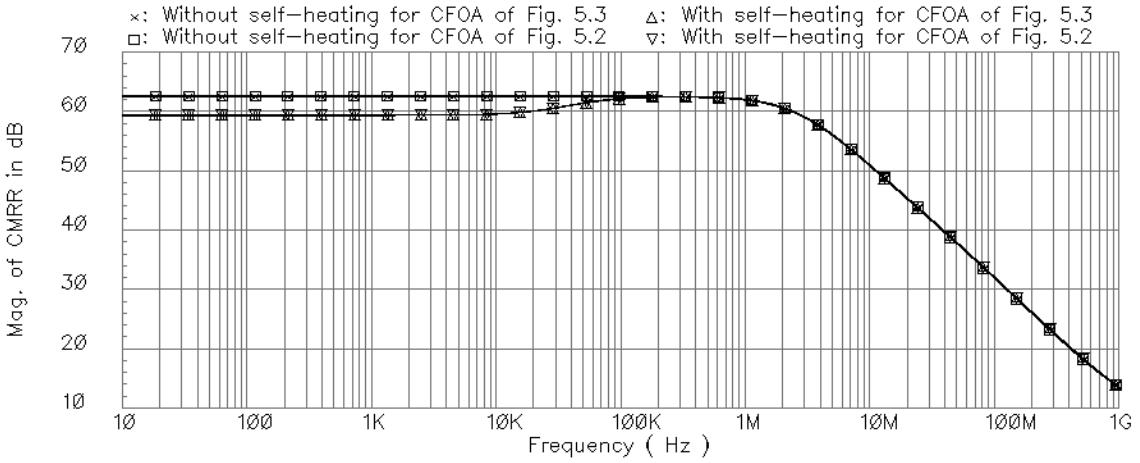


Figure 5.14 Simulated CMRR magnitude response of CFOAs in Figs. 5.2 and 5.3, with and without self-heating.

The low frequency magnitude of the CMRR with and without self-heating is 59.3 dB and 62.57 dB, respectively. Thus, there is a reduction of about 3.27 dB in CMRR at frequencies below the thermal cutoff frequency due to the dynamic self-heating. The effect of self-heating has been suppressed beyond the thermal cutoff frequency. The simulation shown in Fig. 5.14 also proves that the CMRR does not depend on the type of the transimpedance stage. The output resistance of current mirrors, Q_3-Q_4 and Q_1-Q_2, in Fig. 5.2 can be improved by replacing them with Wilson current mirrors or cascode current mirrors and the output impedance of Q_7 can be improved by the reverse or

forward bootstrapping techniques [66]. By doing so, the impact of dynamic self-heating can be minimized on the output resistance of current mirrors and hence on the CMRR of a CFOA. The detailed analysis on this will be provided in the next chapter.

5.2.4 Effects of Dynamic Self-Heating on the Power Supply Rejection Ratio

The power supply rejection ratio (PSRR) can be defined as the ratio of the magnitude of the differential gain, A_{dm}, to the magnitude of the gain from positive or negative power supply to the output, $A_{pos/neg}$, and can be defined as [46]

$$PSRR_{p/n} = \left| \frac{A_{dm}}{A_{pos/neg}} \right| \tag{5.19}$$

The simulation setup shown in Fig. 5.15 can be used to simulate the frequency response of the both positive power supply PSRR and negative power supply PSRR of a CFOA.

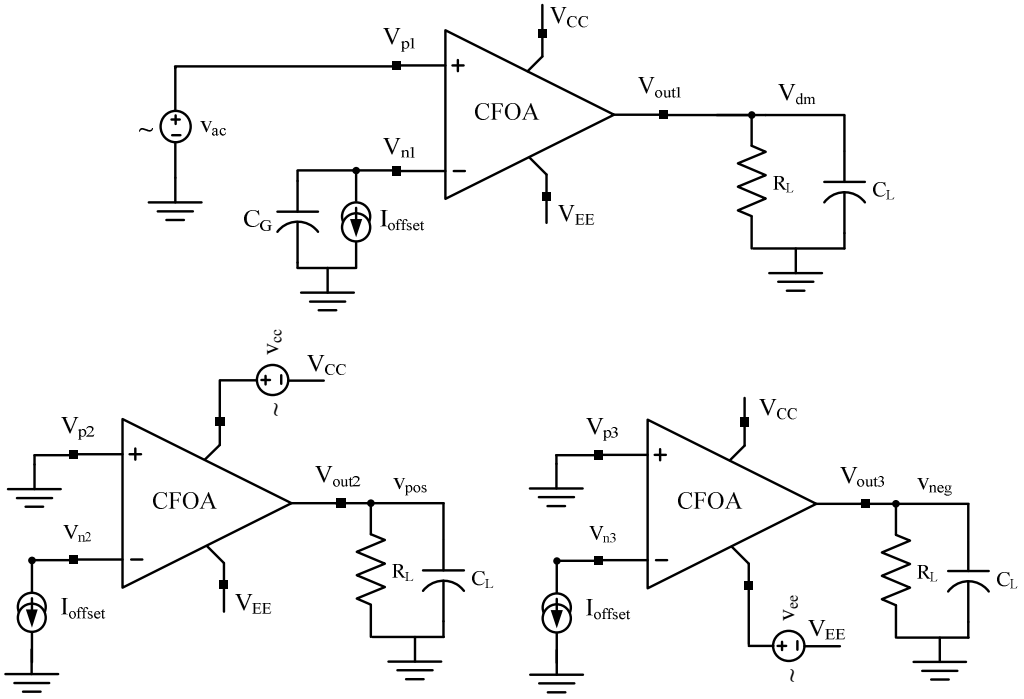


Figure 5.15 Simulation setup for the frequency response of PSRR in the open-loop configuration. v_{cc}, v_{ee}, and v_{ac} are the ac voltage sources.

In Fig. 5.15, the terms, A_{dm}, A_{pos}, and A_{neg} can be defined as v_{dm}/v_{ac}, v_{pos}/v_{vcc} , and v_{neg}/v_{ee}, respectively. The magnitude response of the PSRR of the CFOA of Fig 5.2 is shown in shown in Fig. 5.16, with and without self-heating effect.

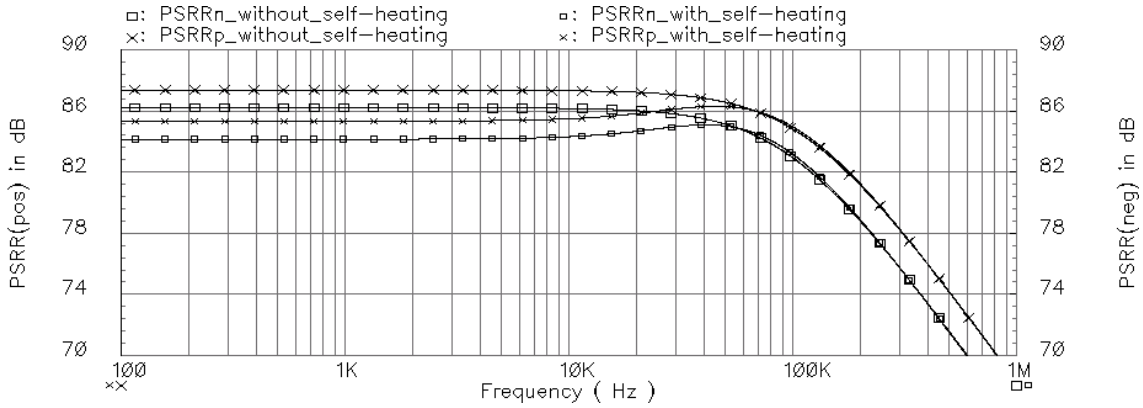


Figure 5.16 Simulated positive PSRR ($PSRR_p$) and negative PSRR ($PSRR_n$) versus frequency of the CFOA of Fig. 5.2, with and without self-heating.

The low frequency magnitude of the $PSRR_p$ with and without self-heating is 87.32 dB and 85.33 dB, while that for $PSRR_n$ with and without self-heating is 86.2 dB and 84.14 dB, respectively. Thus, there is a reduction of ~2 dB in the PSRR due to the dynamic self-heating. A comparison of the PSSR of Fig. 5.2 and 5.3 is shown in Fig. 5.17.

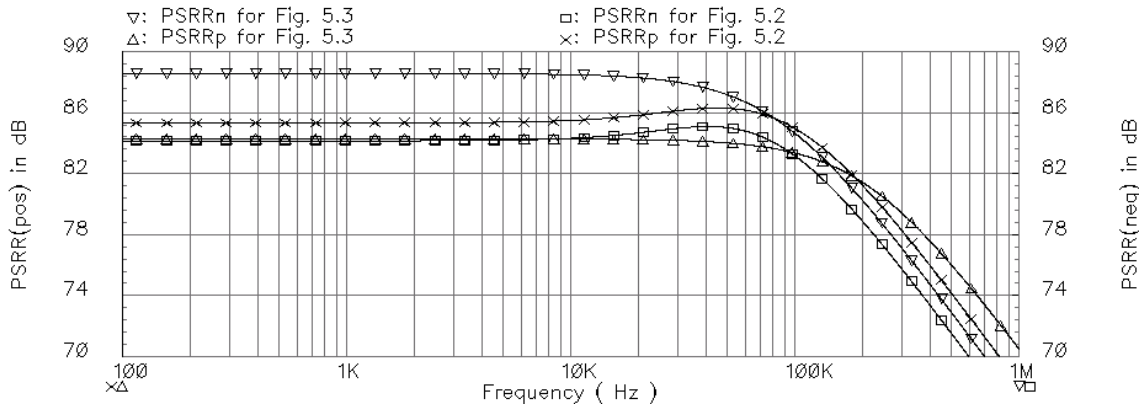


Figure 5.17 Simulated positive PSRR ($PSRR_p$) and negative PSRR ($PSRR_n$) versus frequency of the CFOAs of Figs. 5.2 and 5.3, with self-heating enabled.

5.2.5 Effects of Static Self-Heating on the Step Response

Figure 5.18 shows the simulated large-signal transient step response when the CFOA of Fig 5.2 in the non-inverting unity gain configuration is excited with a -0.5 V to 0.5 V input square wave with rise and fall times of 1 µs and pulse width of 100 µs with 50% duty cycle. As shown in Fig. 5.18, the output can have a positive thermal tail of 0.75 mV and a negative thermal tail of 0.65 mV. The reason for such a small magnitude of thermal tail is the larger size of the transistors being used at the output buffer. The 95% drop in the magnitude of thermal tail happens in 20.0 µs due to the thermal time constant of 5 µs, used in the VBIC model. The electrical transient settle very quickly while thermally induced transient take a much longer time to settle, thus it extends the settling time of the circuit, limiting its usage in precision applications if any.

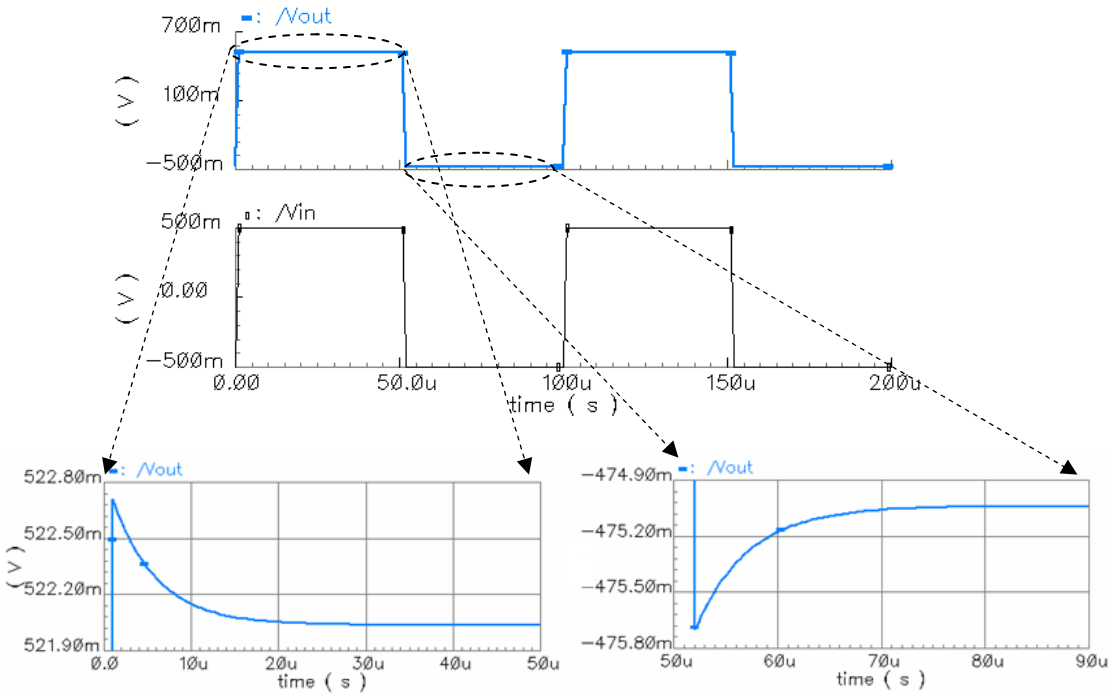


Figure 5.18 Step response of the CFOA of Fig. 5.2 in the non-inverting unity gain configuration shown in Fig. 5.11.

It has also been found that the magnitude of the thermal tail increases with the increase in closed-loop gain of the amplifier. This requires finding the optimal circuit topologies to reduce the thermal tail.

5.3 Layout and Fabrication

The CFOA of Fig. 5.3 was laid out as shown in Fig. 5.19 and fabricated using the VIP10™ bipolar process technology. All transistors emitter areas were 40 μm^2. The die was assembled within a 14 pin DIP package.

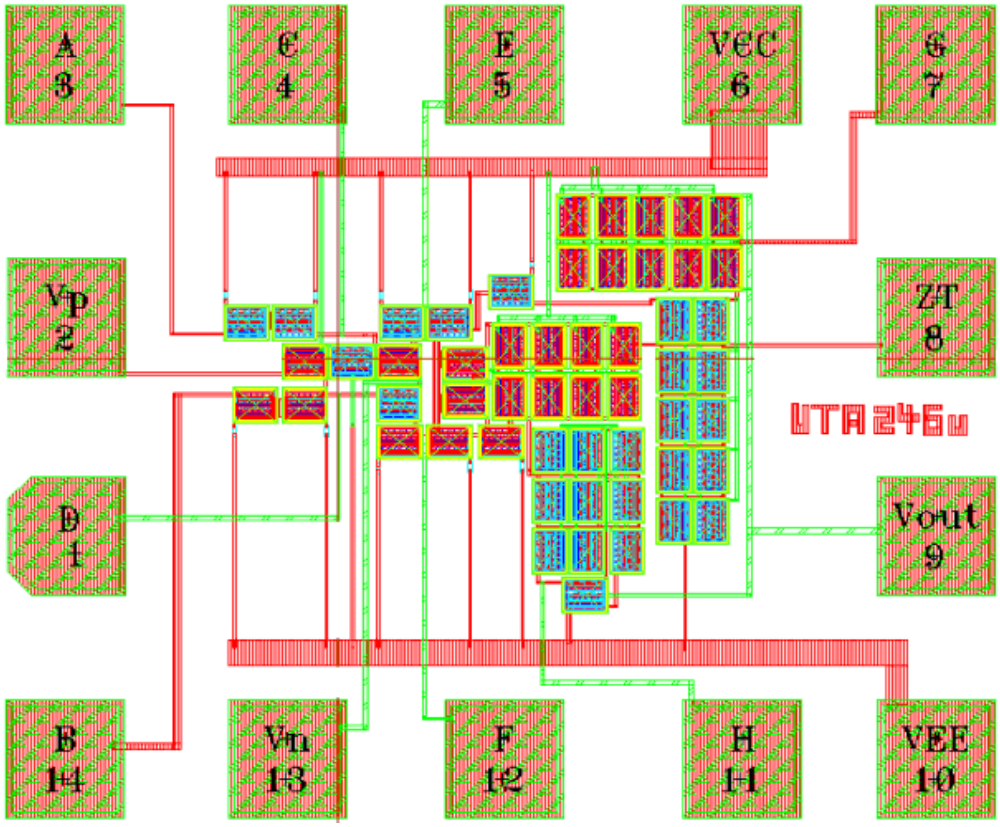


Figure 5.19 Layout of the CFOA of Fig. 5.3 (ID: UTA246U) [65].

This chip, UTA246U, did not work due to a layout error. Hence, the measurement data is not reported.

5.4 Summary

The thermal effect of self-heating on the classical CFOA has been demonstrated through simulations using the VBIC models in the SPECTRE simulator. It is shown that there is a peaking effect in the frequency response of the open-loop transimpedance, $Z_T(s)$, CMRR, and PSRR due to the thermal effect of the dynamic self-heating. New test circuits for the simulation of the open-loop transimpedance, CMRR, and PSRR are presented. It is also illustrated that the thermal tail in the step response of a CFOA in the closed-loop non-inverting unity gain configuration can be reduced by using larger devices.

CHAPTER 6

TECHNIQUES TO DESIGN SELF-HEATING TOLERANT CURRENT-FEEDBACK OPERATIONAL AMPLIFIERS

The primary focus of this chapter is to discuss the design optimization techniques to reduce the self-heating thermal effect on the performance of current-feedback amplifiers. A detailed analysis of self-heating affected parameters of the classical CFOA has been presented in chapter 5, and two new topologies of the CFOA will be proposed in this chapter to mitigate the influence of self-heating on identified parameters. The performance of new CFOA topologies will be compared and contrasted with the conventional CFOA topology as well. These new CFOA circuits were fabricated with the VIP10^{TM} bipolar process technology as test chips for the validation of design functionality and the characterization of the thermal effect of self-heating.

6.1 Design of the Input Stages of a CFOA

It is well known that CFOA generally exhibits a poor CMRR performance, limiting its utilization for precision applications [55]. This will be further reduced by the dynamic self-heating as illustrated in chapter 5. There are several techniques discussed by many others [56], [67] to improve the CMRR of the CFOAs. The design criterion to make a circuit self-heating tolerant is hinged upon the concept of cascoding as discussed in chapters 3 and 4. The proper use of cascoding to shield the variation of

current through any mechanism proves to be a very useful technique in suppressing the non-ideal thermal effects of self-heating. Three different approaches [66] to boost the output resistance of the transistor, Q_7, which partly governs the CMRR performance of the current-feedback amplifiers of Figs. 5.2 and 5.3, are illustrated in Fig. 6.1.

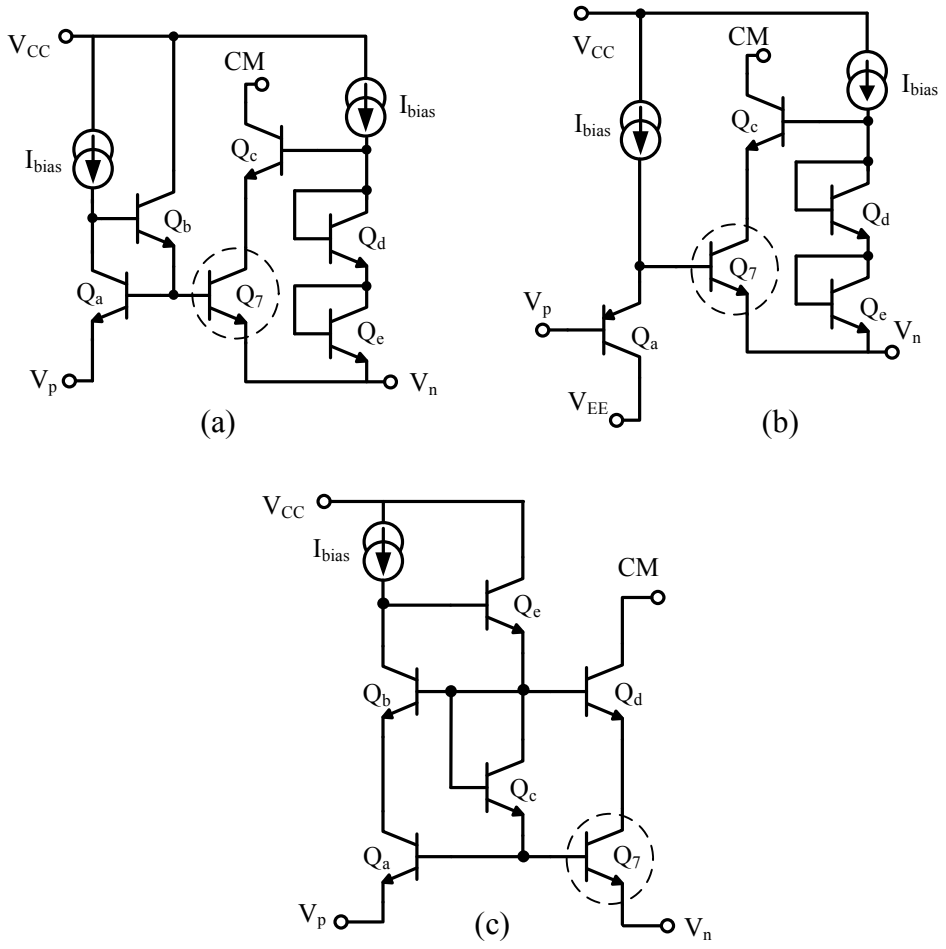


Figure 6.1 Possible input architecture of CFOAs (a) reverse-bootstrapping on a single buffer input stage (b) reverse-bootstrapping on a double buffer input stage (c) symmetrical cell with the forward bootstrapping [66].

The transistor, Q_7, encircled in Fig. 6.1 may represent one of the transistors of the input buffer, Q_5-Q_8, of Figs. 5.2 and 5.3. To increase the small-signal resistance at

the collector of Q_7, the technique illustrated in Fig. 6.1(a) can be used, where Q_c acts as a cascode device which is being biased through the diode connected transistor pair, Q_d/Q_e, and current source, I_{bias}. Since the base of Q_c is biased through the inverting input terminal which follows the non-inverting input terminal, this approach is called reverse-bootstrapping [66]. If the input stage is based on the diamond structure buffer or double buffer [22], the circuit topology of Fig. 6.1(b) can be used. The symmetrical cell structure shown in Fig 6.1(c) can also be used at the input stage of a CFOA to increase the output resistance of Q_7. This cell can also be used for the design of a complete CFOA circuit to suppress the thermal effect of self-heating. A complete circuit implementation of the CFOA using this cell has been reported by Tammam [67].

As explained in chapter 5, the CMRR strongly depends on the type of current mirror being used to bias the input stage, and the transimpedance stage of the CFOA is extremely vulnerable to self-heating unless high performance current mirrors are used. The cascode current mirror and Wilson current mirrors work quite well in the suppression of the thermal effect of self-heating at the transimpedance stage.

6.2 Cascode Current Mirror Based Current-Feedback Operational Amplifier Design – CFOA I

6.2.1 Design and Working Principle

The CFOA of Fig. 6.2 has also three fundamental stages, an input voltage buffer (Q_5-Q_{12}), an intermediate transimpedance stage (Q_{17a}-Q_{17c} and Q_{18a}-Q_{18c}), and an output voltage buffer (Q_{21}-Q_{24}). The transistor pairs, Q_5/Q_7 and Q_9/Q_{11}, are biased with cascode current mirrors, Q_1-Q_4 and Q_{13}-Q_{16}, respectively. Emitter degeneration resistors of 0.5 kΩ are used to improve output resistance of current mirror and to improve the

device matching. The input V_p, and the output V_n, of the input buffer constitute the non-inverting and inverting input of the CFOA. The central transimpedance stage converts the current, i_N, which flows out of the inverting input, V_n of the CFOA, into a voltage across a high-impedance node, *Z*. The output voltage buffer, Q_{21}-Q_{24}, simply buffers the *'Z'* node voltage to the output, O with the desired low output impedance for external load. Since the input buffer, Q_7 through Q_{10}, has employed cascoding techniques, the effect of self-heating on the large-signal transient response will be minimized [11].

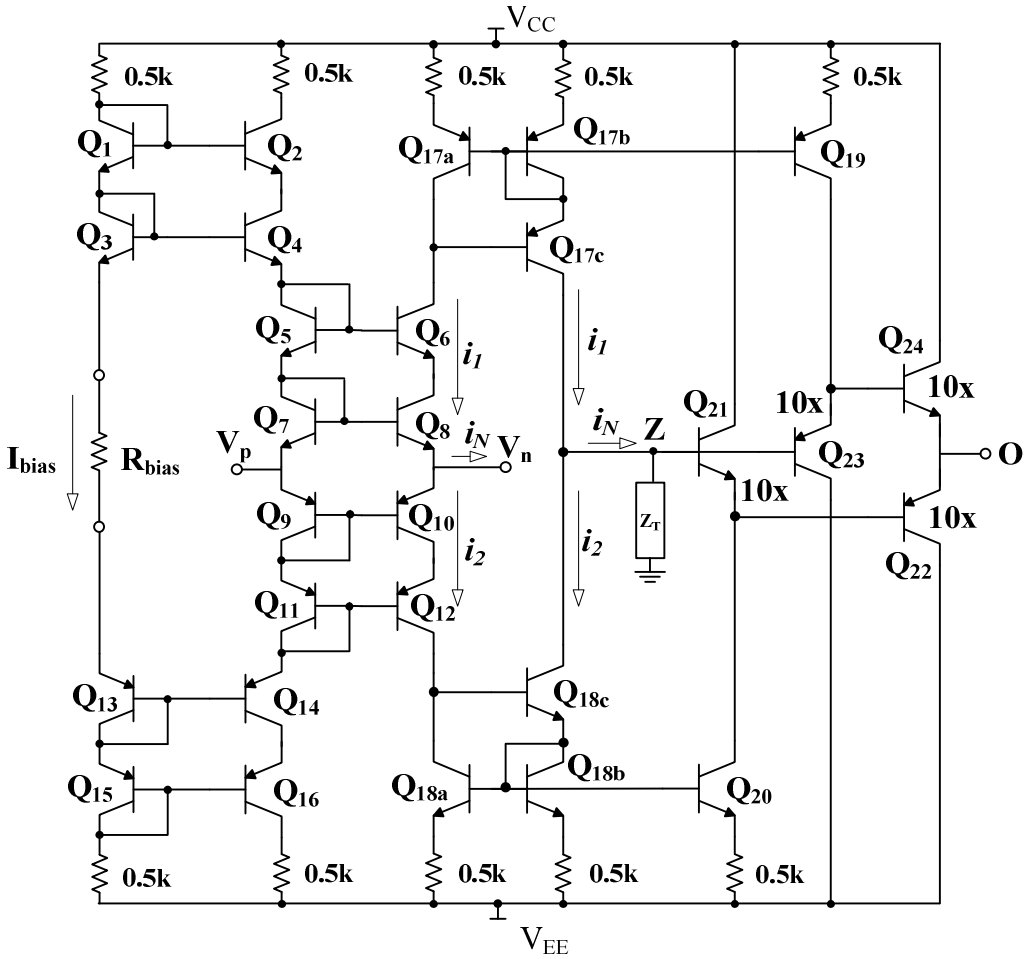


Figure 6.2 Proposed CFOA complete circuit with cascoded input stage biased with cascode current mirrors – CFOA I.

The intermediate stage consists of two Wilson current mirrors formed by Q_{17a}-Q_{17c} and Q_{18a}-Q_{18c} along with emitter degeneration resistor, whose output impedances will be somewhat less impacted by dynamic self-heating [44], [59] unless they are biased with a very large current. All transistors, Q_1 through Q_{20} have an emitter area of 40 μm^2 except the transistors forming the output voltage buffer, Q_{21} through Q_{24}. These have an emitter area of 400 μm^2 (10x of 40 μm^2 devices). The intention of using larger devices at the output is two-fold. One is to improve the matching of V_{BE} of transistors by minimizing the thermal resistance of transistors, which in essence minimizes the temperature elevation. The second is to reduce the value of the feedback resistor, R_f, required for the stable closed-loop operation as required by (5.14). This eventually helps to minimize the magnitude of the thermal tail in the large-signal step response of a CFOA in the closed-loop configuration. In addition, this will also help to drive a large current on demand to the load. The bias current, I_{bias}, is set to 250 μA with the bias resistor, R_{bias}, of 25 kΩ for the power supply of ± 5 V. A major downside of this circuit is the limited common-mode input range (CMIR) due to the vertical stacking of the cascode transistors. The small-signal macromodel shown in Fig. 5.4 of chapter 5 can be used to model the close-loop characteristics of this COFA as well.

6.2.2 Layout and Fabrication

The CFOA of Fig. 6.2 was laid out as shown in Fig. 6.3 and fabricated with the VIP10^{TM} bipolar process technology. The sizes of the transistor were the same as shown in Fig. 6.2, the emitter areas of transistors, Q_1 through Q_{20} were 40 μm^2 (1x devices) The bias resistor, R_{bias}, is an off-chip resistor to have the flexibility in setting the bias

current for the CFOA. The square bonding pad of 100 μm x 100 μm was used for each pin for the electrical connection from the die to package pad through the bonding wire. The die was placed within a 14 pin DIP package.

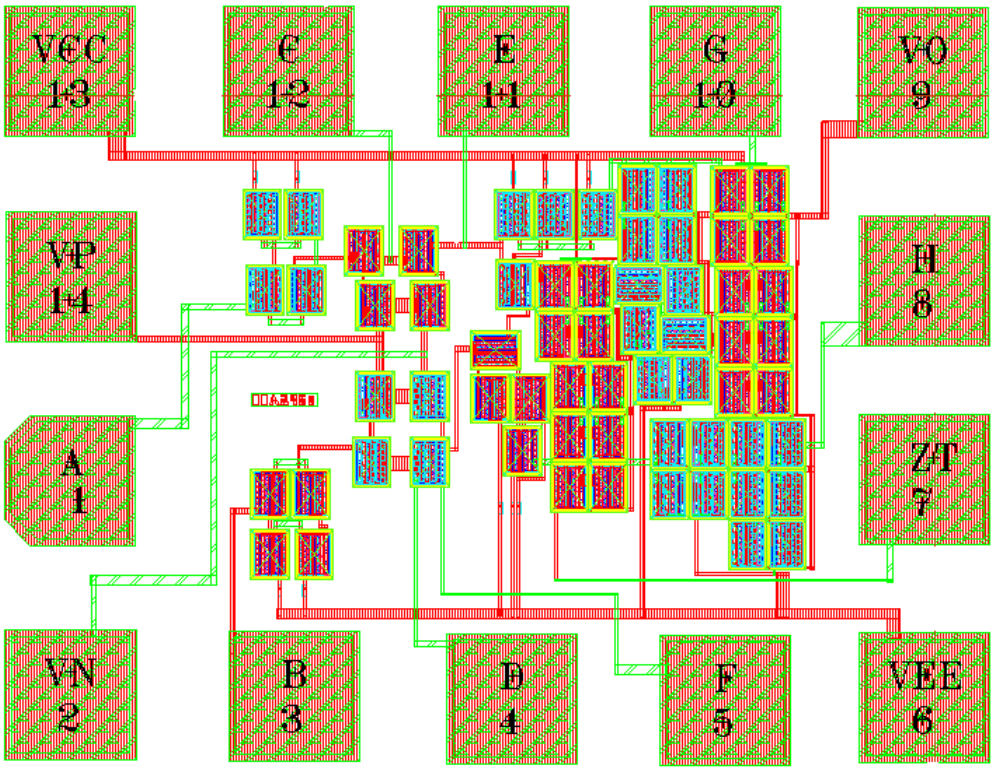


Figure 6.3 Layout of the CFOA of Fig. 6.2 (ID: UTA246S) [65].

6.3 Folded-Cascode Input Stage Based Current-Feedback Operational Amplifier Design – CFOA II

6.3.1 Design and Working Principle

Folded-cascode input stage based CFOA is shown in Fig. 6.4. Single push-pull buffer topology at the input stage is used to get a low input offset-voltage because of the better matching of the base-emitter voltage of the same type of transistor pairs, Q_5/Q_6 and Q_7/Q_8. The major difference between CFOAs of Fig. 6.2 and Fig. 6.4 is the use of cascode versus folded-cascode structure to boost the effective output resistances of the

transistors, Q_8 and Q_{10} of Fig. 6.2, and Q_6 and Q_8 of Fig. 6.4, respectively. In the folded-cascode approach, the effective output impedance of the *npn* transistors, Q_6, and Q_8, are boosted through the *pnp* transistors, Q_{18} and Q_{19}, respectively. The nodes, X and Y are the folding point of the folded cascode structures constituted by transistors pair, Q_6/Q_{18} and Q_8/Q_{19}, which are being biased with the cascode current sources, Q_{13} and Q_{14}, and Q_{15} and Q_{16}, respectively. It is important to note that the emitter area of Q_{13}/Q_{14} are twice the emitter area of Q_2/Q_4, and the emitter degeneration resistor of Q_{13} is half of Q_2 to distribute the same bias current, $I_{bias,}$ between Q_6 and Q_{18}.

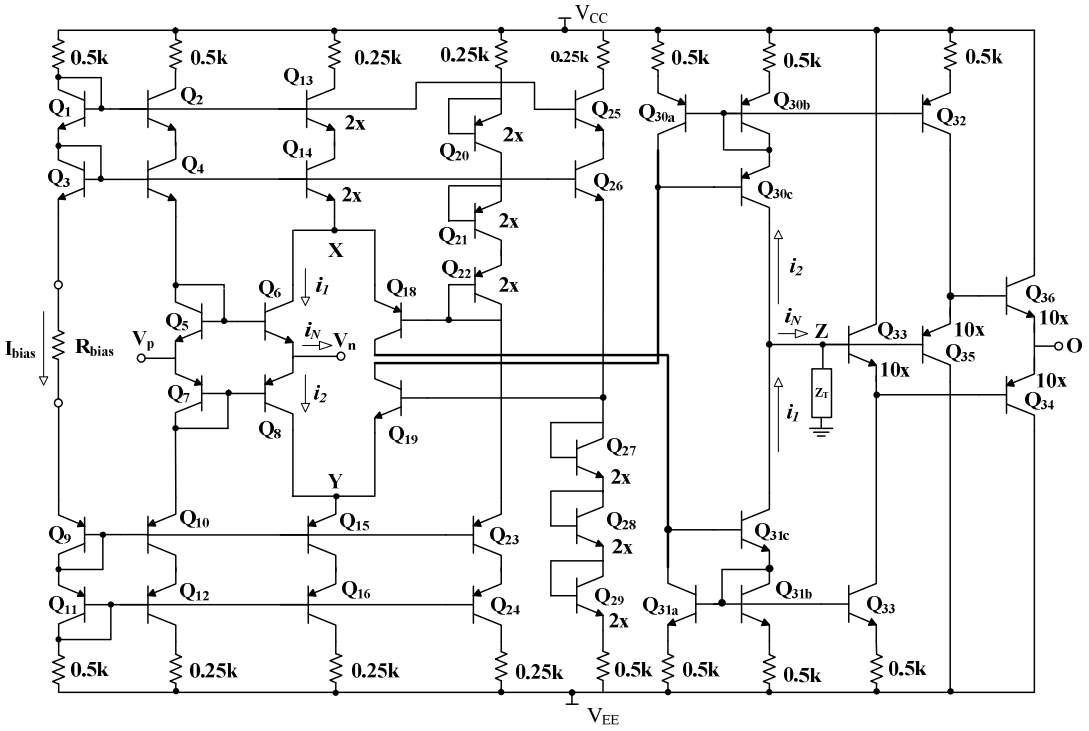


Figure 6.4 Complete circuit of folded-cascode input stage based CFOA – CFOA II. Transistors have an emitter area of 40 μm^2 unless indicated.

This clearly shows that a folded cascode structure requires twice the biasing current of a cascode structure for a comparable performance as discussed in chapter 3. Thus, a

folded cascode structure consumes higher power than a cascode structure for comparable performance [45]. The bias voltage at the base of cascode devices, Q_{18}, is supplied through the diode connected transistors, Q_{20} through Q_{22}, which are biased through the cascode current source, Q_{23} and Q_{24}. Similarly, the bias voltage at the base of cascode device, Q_{19}, is supplied through the diode connected transistors, Q_{27} through Q_{29}, which are biased through the cascode current source, Q_{25} and Q_{26}. The complementary nature of cascode transistor (*pnp*/*npn*) from the input transistor (*npn*/*pnp*) is utilized to save the voltage headroom. However, the increase in the output impedance of folded-cascode structure is lower than that of a cascode structure because of the inferior Early voltage of the *pnp* device compared to the *npn* device. The intermediate stage is implemented with Wilson current mirrors, the same as in Fig. 6.2. The transimpedance node "Z" is buffered to the output, O with a double buffer, Q_{33} through Q_{36}.

The transistor sizes, 1x, 2x, and 10x as shown in Fig. 6.4 represent transistors with an emitter area of 40 μm^2, 80 μm^2, and 400 μm^2, respectively. All emitter degeneration resistors are 0.5 kΩ as shown in Fig. 6.4. The bias current, I_{bias}, is set to 250 μA with a bias resistor, R_{bias}, of 25 kΩ for the power supply of ± 5 V.

6.3.2 Layout and Fabrication

The CFOA of Fig. 6.4 was laid out as shown in Fig. 6.5 and fabricated with the VIP10^{TM} bipolar process technology. The emitter areas of all transistors were 40 μm^2 unless indicated in Fig. 6.4. The bias resistor, R_{bias}, as shown in Fig. 6.4 was not placed on-chip in order to have the flexibility in setting the bias current. The square bonding

pad of 100 μm x 100 μm for each external pin was used for the electrical connection from the die to package pad through the bonding wire. The die was placed within a 14 pin DIP package.

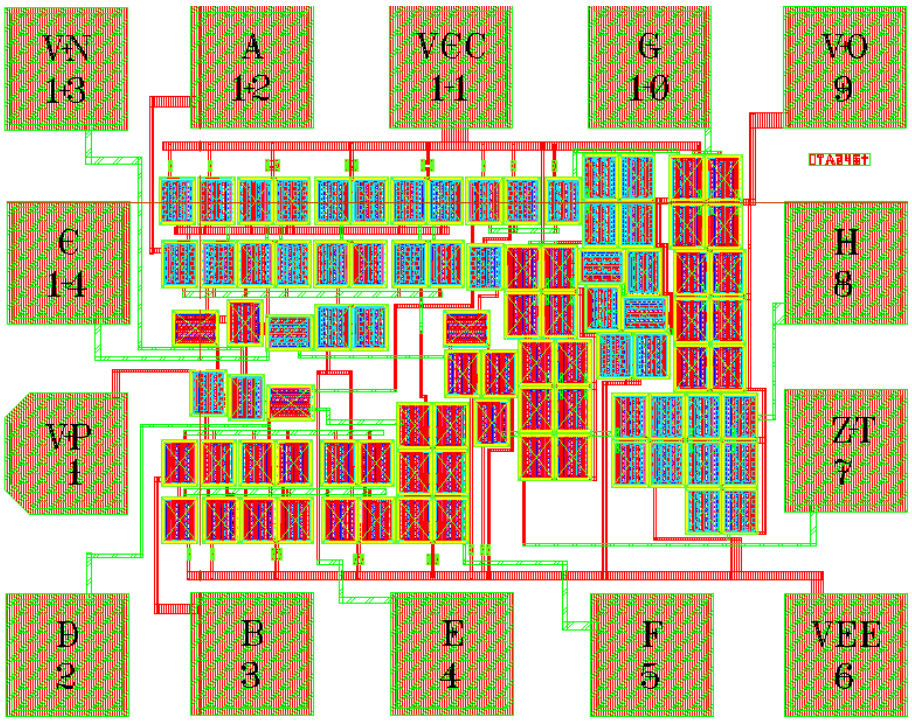


Figure 6.5 Layout of the CFOA of Fig. 6.4 (ID: UTA246T) [66].

6.4 Comparison of CFOA I and CFOA II through Simulations

For all simulations reported in this chapter, the SPECTRE simulator was used to verify the operation and performance of the CFOAs in Figs. 6.2 and 6.4. The technology used in the simulations was based on the proposed VBIC models, provided in Tables 2.9 and 2.10. These models represent transistors with an emitter area of 5 μm^2. To model the effect of self-heating in the VBIC model, a thermal time constant of 5 μs [31] was used, with thermal resistance of 3000 K/W and thermal capacitance of 1.69 nJ/K. For larger devices, the "area" option in the schematic editor of the Virtuoso®

Analog design environment was set to the required value as needed. The power supply voltages for both circuits of Figs. 6.2 and 6.4 are set to V_{CC} = +5 V, and V_{EE} = –5 V.

6.4.1 DC Simulation

The dc input-output characteristics of the CFOAs of Fig. 5.2, 5.3, 6.2, and 6.4 in the closed-loop non-inverting unity gain configuration (as shown in Fig. 5.11 with ac source replaced with dc voltage) are shown in Fig. 6.6.

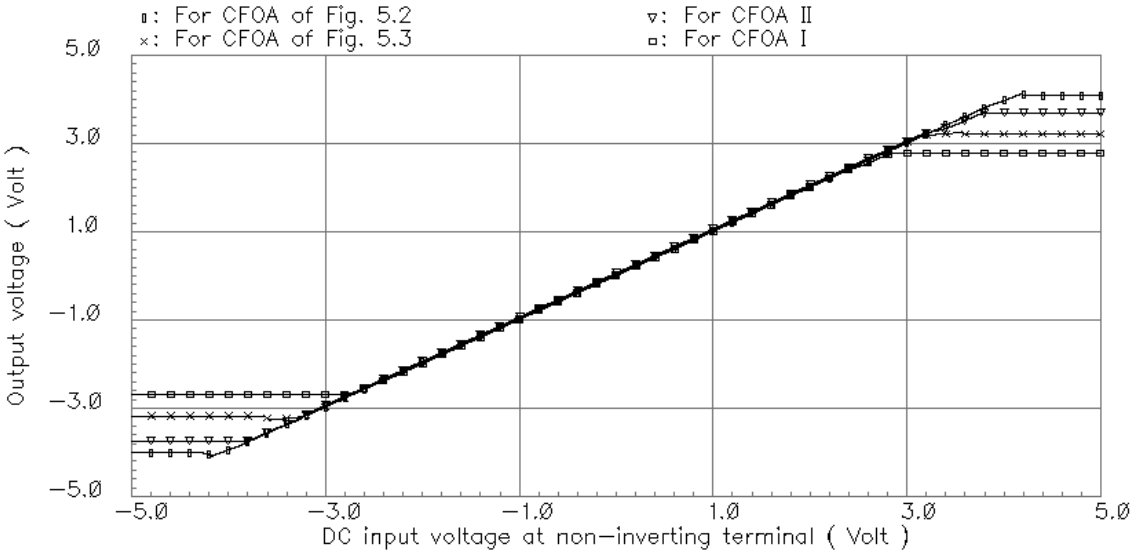


Figure 6.6 Input-output characteristics of CFOAs in the closed-loop non-inverting unity gain configuration with R_f = 1 kΩ and R_L = 2.2 kΩ.

It is clearly seen from Fig. 6.6 that the best CMIR and output dynamic range can be achieved with the classical topology of the CFOA of Fig 5.2, in which the transimpedance stage is implemented with simple current mirrors. The CMIR and dynamic range are reduced for the CFOA in Fig. 5.3 in which the transimpedance is implemented with Wilson current mirrors. The CMIR is very limited for the CFOA I in Fig. 6.2 due to the vertical stacking of transistors in the input stage. The CMIR for the

COFA II of Fig. 6.4 is better than that of CFOA I of Fig. 6.2 because of the folding cascode at the input stage.

6.4.2 Frequency-Domain Simulations

6.4.2.1 Open-Loop Transimpedance Response

The open-loop transimpedance frequency response of the CFOA of Figs. 6.2 and 6.4 using the simulation setup, shown in Fig. 5.6, is shown in Fig. 6.7.

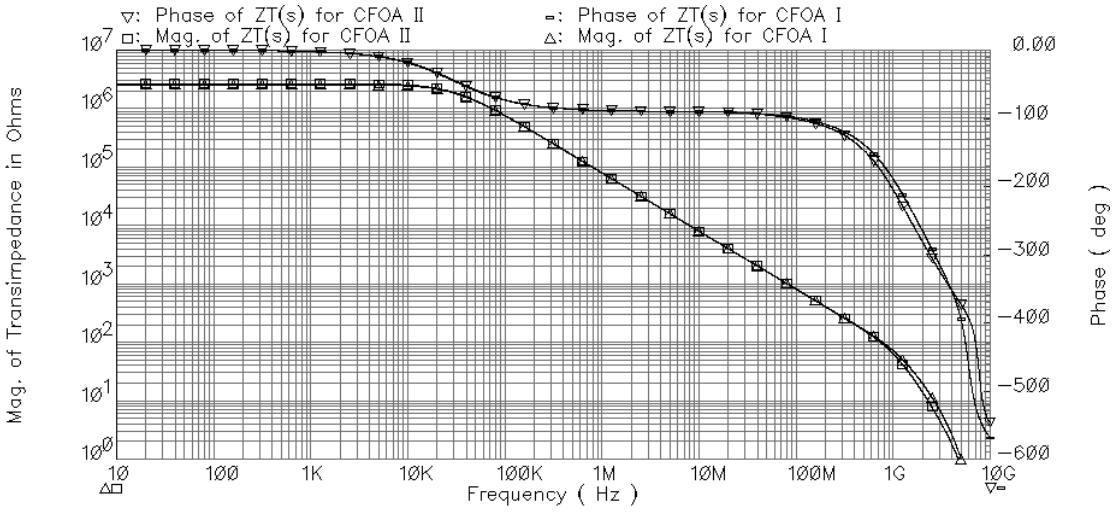


Figure 6.7 Frequency response of the open-loop transimpedance of CFOA I with I_{offset} = -9.767 μA, and CFOA II with I_{offset} = -61.702 μA, with self-heating enabled.

The simulation shows that transresistance, $Z_T(0)$, of both CFOA I and II are very close to each other and their critical resistances are 83.27 Ω and 91.0 Ω, respectively.

Since Wilson current mirrors are used at the transimpedance stage of both CFOA I and CFOA II, the effect of dynamic self-heating is minimized on the frequency response of the transimpedance at a lower frequency, and there is no peaking effects as illustrated in Fig. 6.8 due to the thermally induced pole-zero cancellation.

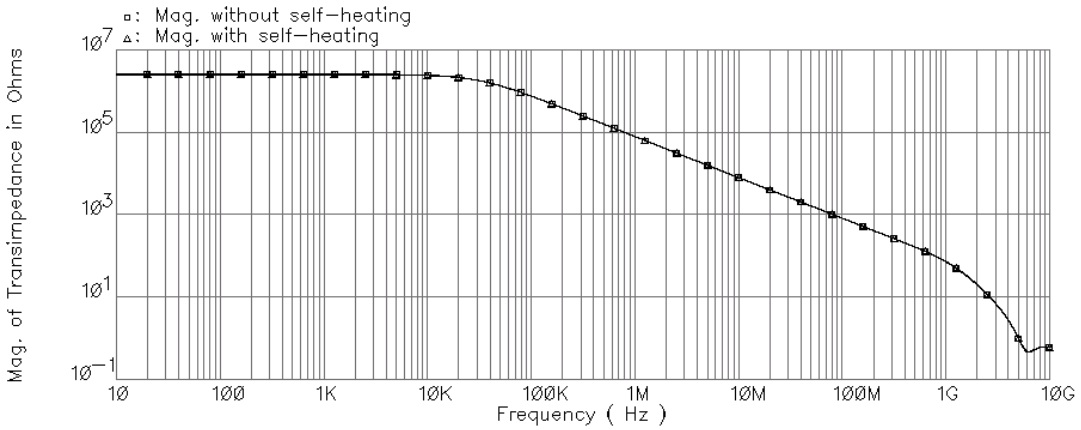


Figure 6.8 Magnitude response of the open-loop transimpedance of the CFOA I of Fig. 6.2, with and without self-heating.

6.4.2.2 Frequency Response in Non-Inverting Unity Gain Configuration

The frequency response of the CFOA I in the non-inverting unity gain configuration is shown in Fig. 6.9 with a feedback resistor, R_f, as a sweep parameter.

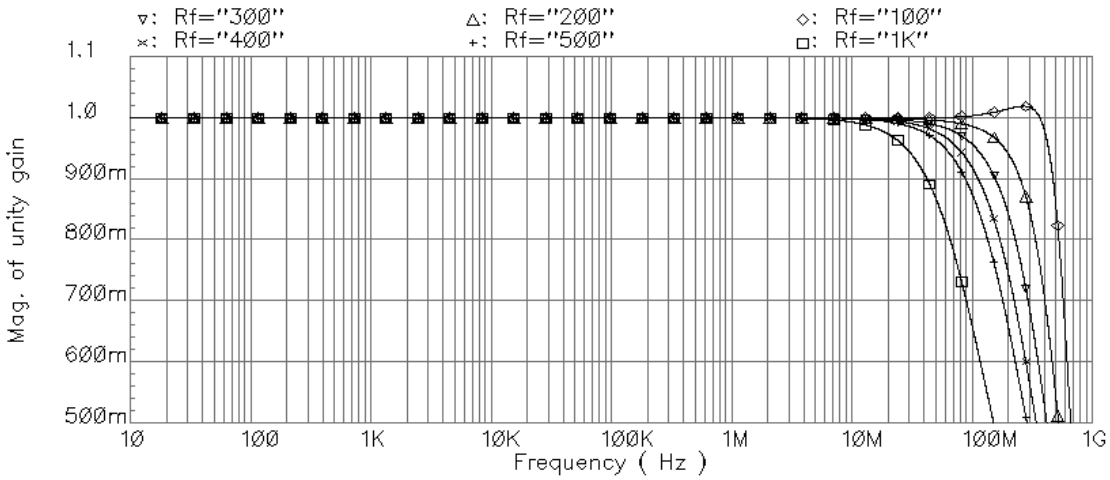


Figure 6.9 Frequency response of the CFOA I of Fig. 6.2 in the non-inverting unity gain configuration (shown in Fig. 5.10) with R_L = 25 kΩ and C_L = 0.35 pF.

As shown in Fig. 6.9, the peaking free response can be obtained for a feedback resistance above 200 Ω, and corresponding maximum 3-dB bandwidth is 400 MHz. The unity gain closed loop 3-dB bandwidth with R_f = 1 kΩ is 90 MHz.

The frequency response of the CFOA II in the non-inverting unity gain configuration is shown in Fig. 6.10 with a feedback resistor, R_f, as a sweep parameter.

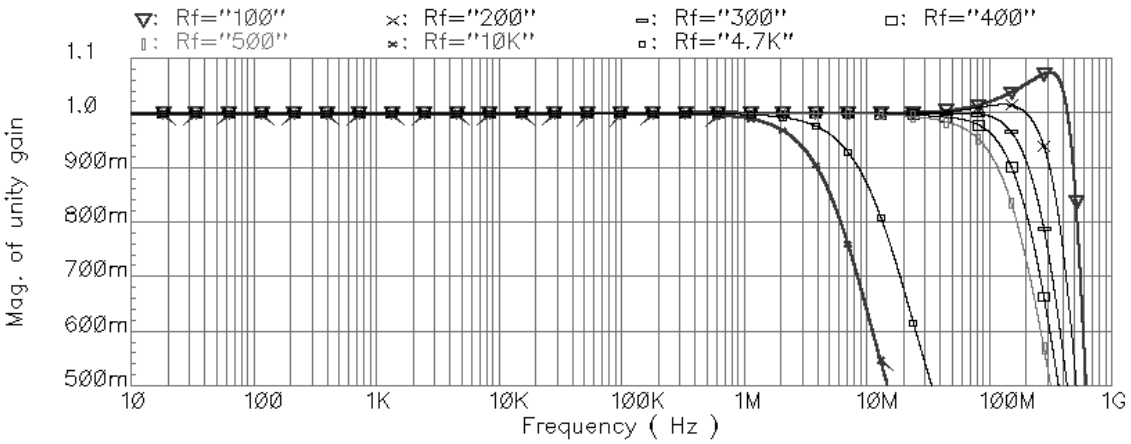


Figure 6.10 Frequency response of the CFOA II of Fig. 6.4 in the non-inverting unity gain configuration (shown in Fig. 5.10) with R_L = 25 kΩ and C_L = 0.35 pF.

As shown in Fig. 6.10, the peaking free response can be obtained for a feedback resistance above 400 Ω, and corresponding maximum 3-dB bandwidth is 300 MHz. The unity gain closed loop 3-dB bandwidth with R_f = 4.7 kΩ, and R_f = 10 kΩ are 20 MHz, and 8 MHz, respectively.

6.4.2.3 CMRR Frequency Response

The frequency response of the CMRR of CFOA I is shown in Fig. 6.11 using the simulation test circuit of Fig. 5.11. As explained in section 6.2.1, the output resistances of Q_8 and Q_{10} of Fig. 6.2 are increased by the presence of Q_6 and Q_{12}, respectively, and the bias current to the input stage is supplied through cascode current mirrors, Q_1-Q_4 and Q_{13}-Q_{16}. This helps to suppress the effect of dynamic self-heating in the frequency response of the CMRR, and to improve the dc magnitude of CMRR as evidenced theoretically in chapter 5. This simulation, shown in Fig. 6.11, shows that there is little

effect of dynamic self-heating on the CMRR response, unlike the CMRR response of a classical CFOA (Fig. 5.2), in which the CMRR is reduced by about 3 dB from the dynamic self-heating. Thus, the cascode current mirrors perform quite well in the suppression of the self-heating thermal effect on the CMRR. In addition, the low frequency CMRR has increased by about 30 dB over the classical CFOA's CMRR.

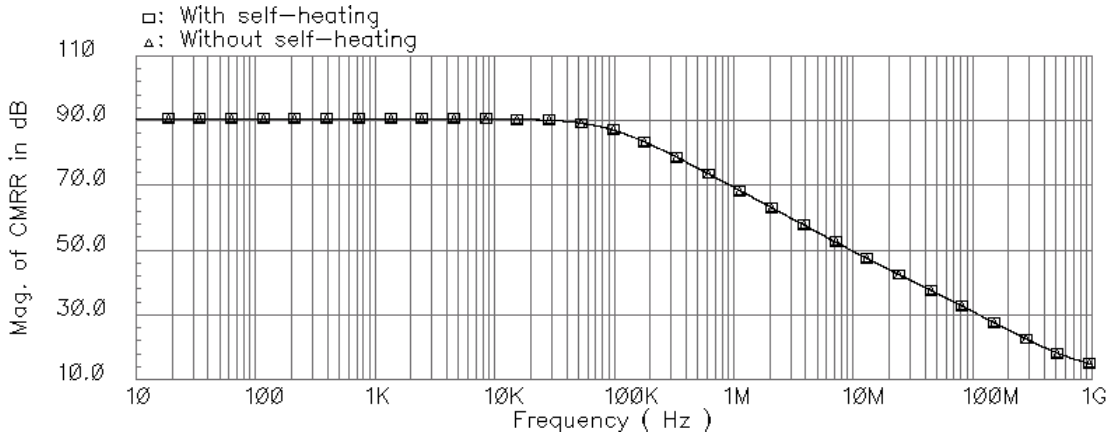


Figure 6.11 Simulated magnitude of CMRR versus frequency response of the COFA I of Fig. 6.2, with and without self-heating.

The CMRR response of the CFOA II of Fig. 6.4 is shown in Fig. 6.12. The dc CMRR with and without self-heating is 65.67 dB and 68.34 dB, respectively.

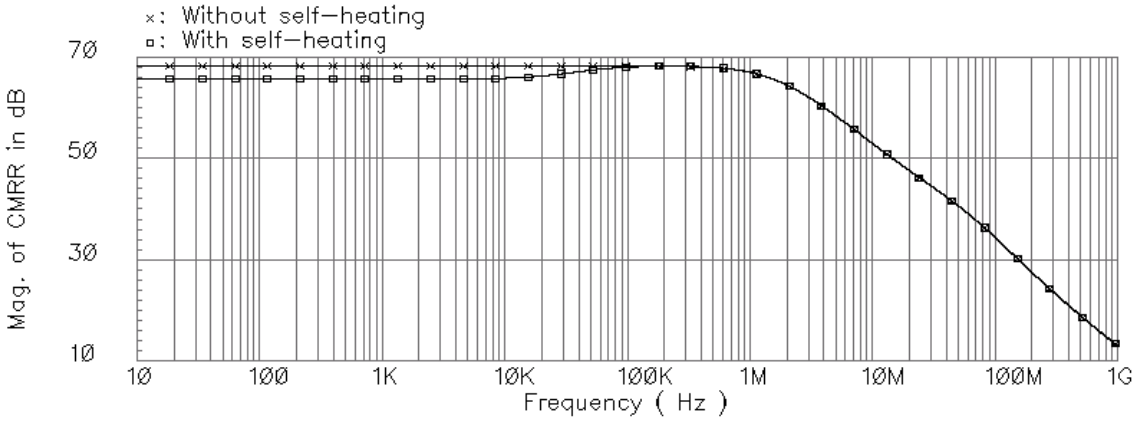


Figure 6.12 Simulated magnitude of CMRR versus frequency of the COFA II of Fig. 6.4, with and without self-heating.

A comparison of the CMRR frequency responses of the classical CFOA of Fig. 5.2, CFOA I, and CFOA II is shown in Fig. 6.13, and their dc values are 59.38 dB, 65.67 dB, and 90.6 dB, respectively.

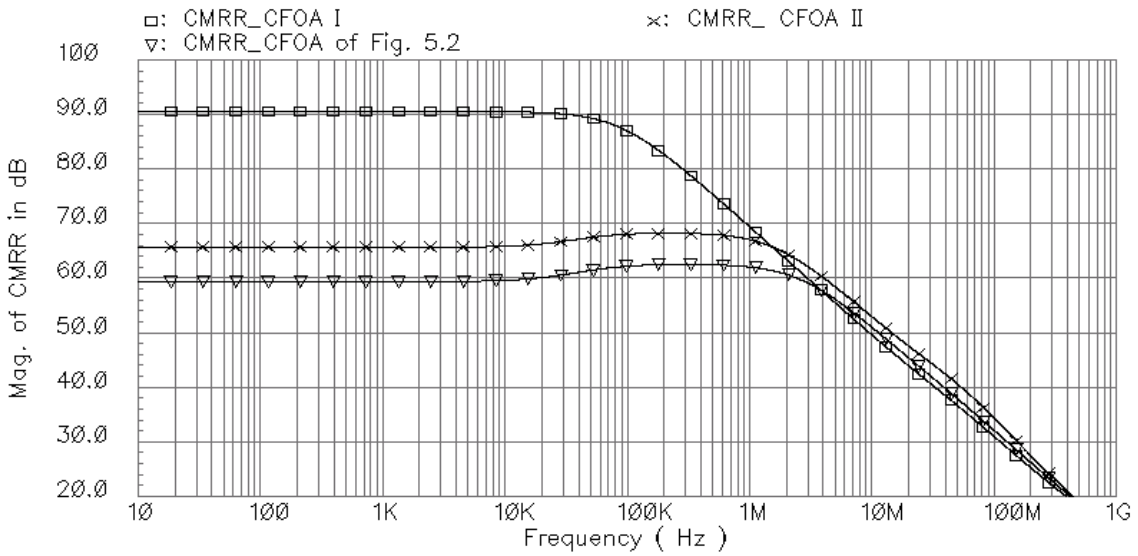
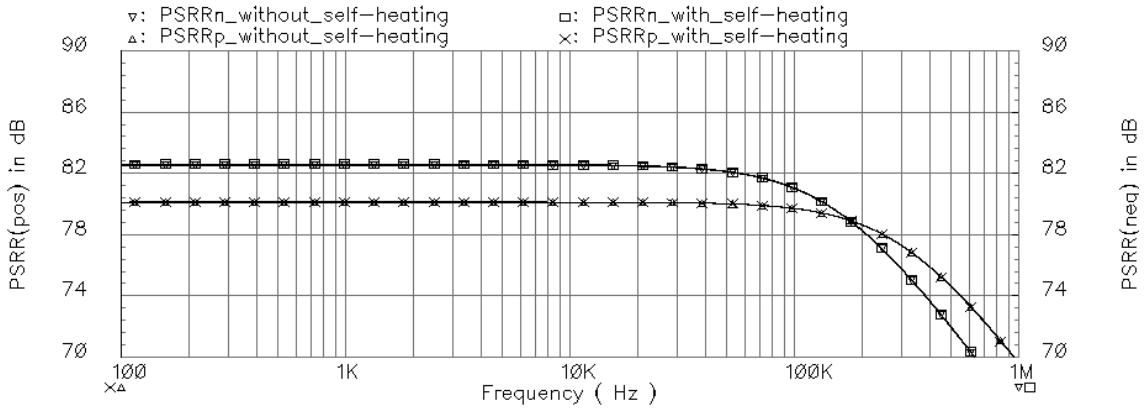


Figure 6.13 Comparison of magnitude of CMRR versus frequency responses of the COFAs of Figs. 5.2, 6.2, and 6.4.

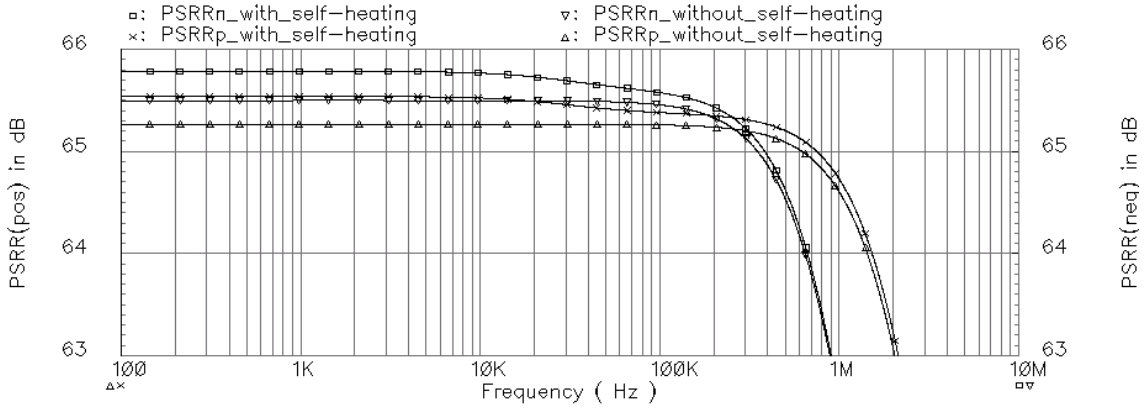
As illustrated in Fig. 6.13, the best CMRR response can be obtained with CFOA I. The dc CMRR of the CFAO II is lower in comparison with CFOA I because of the lower output resistance of the folded cascode structure used in CFOA II over the cascode structure used in CFOA I.

6.4.2.4 PSRR Frequency Response

Figure 6.14(a) shows the magnitude response of $PSRR_p$ and $PSRR_n$ for the CFOA I and their dc and low frequencies magnitude with self-heating enabled are 80.10 dB, and 82.58 dB, respectively. A similar response for the CFOA II is shown in Fig. 6.14(b) where the $PSRR_p$ and $PSRR_n$ with self-heating enabled are 65.53 dB, and 65.78 dB, respectively. There is virtually no effect of self-heating on the PSRR responses.



(a)



(b)

Figure 6.14 Effect of self-heating on the magnitude response of PSRR versus frequency (a) for CFOA I (b) for CFOA II, with and without self-heating.

However, the magnitude of both $PSRR_p$ and $PSRR_n$ for CFOA II is lower than those of CFOA I by about 15 dB. The reason for such a reduction in PSRR of CFOA II is that the effective output resistance of the folded cascode transistor pairs, Q_6/Q_{18} and Q_8/Q_{19} of Fig. 6.4 is lower than the cascode structures, Q_8/Q_6 and Q_{10}/Q_{12} of Fig. 6.2. In addition, the base of Q_{18} is tied to the positive power supply through the diode connected transistors, Q_{20} through Q_{22}, of Fig. 6.4, while the base of Q_{19} is tied to the negative power supply through the diode connected transistors, Q_{27} through Q_{29}, of Fig. 6.4. This has also deteriorated the PSRR response of CFOA II.

6.4.2.5 Non-Inverting Input Impedance Frequency Response

The simulation setup for determining the impedance response of the non-inverting input of a CFOA in the open-loop configuration is shown in Fig. 6.15. The dc current source, I_{offset}, at inverting input is used to drive the output voltage, V_{out}, to zero. It also provides the required bias voltages to keep internal transistors in the forward-active region.

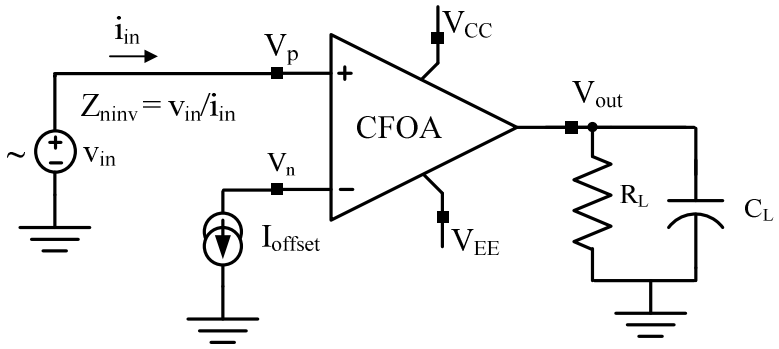


Figure 6.15 Simulation setup for the frequency response of non-inverting input terminal impedance in the open-loop configuration.

The magnitude responses for the non-inverting input terminal impedance for CFOA I and II are shown in Fig. 6.16. The dc and low frequency non-inverting input impedances for CFOA I, and CFOA II are 2.62 MΩ, and 3.26 MΩ, respectively.

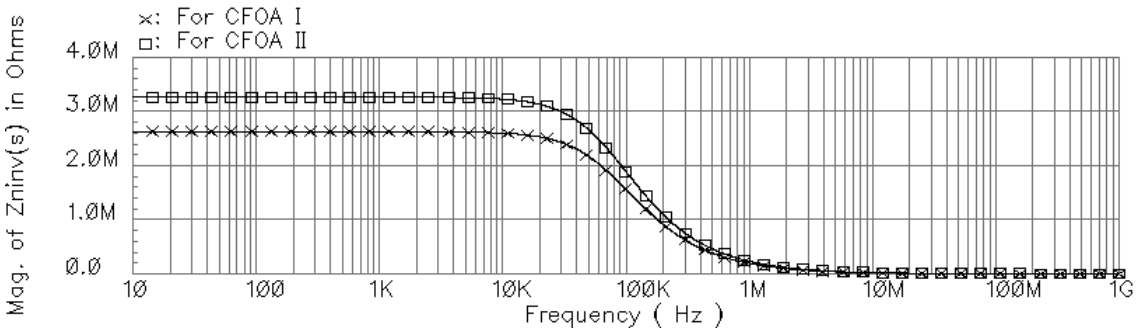


Figure 6.16 Magnitude of non-inverting input terminal impedance versus frequency for the CFOA I and II, with self-heating enabled.

6.4.2.6 Inverting Input Impedance Frequency Response

The simulation setup for the impedance response of the inverting input of a CFOA is shown in Fig. 6.17. The dc current source, I_{offset}, at the inverting input terminal is used to set V_{out} to zero. The inverting terminal is driven with an ac source, i_{in}, and the ratio of voltage, v_{in}, over current, i_{in}, shown in Fig. 6.17 gives the inverting input impedance, and such responses are shown in Fig. 6.18.

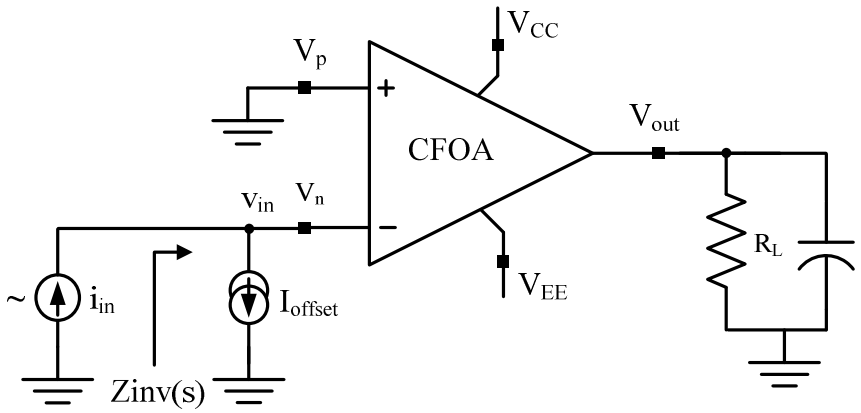


Figure 6.17 Simulation setup for the frequency response of inverting input terminal impedance in the open-loop configuration.

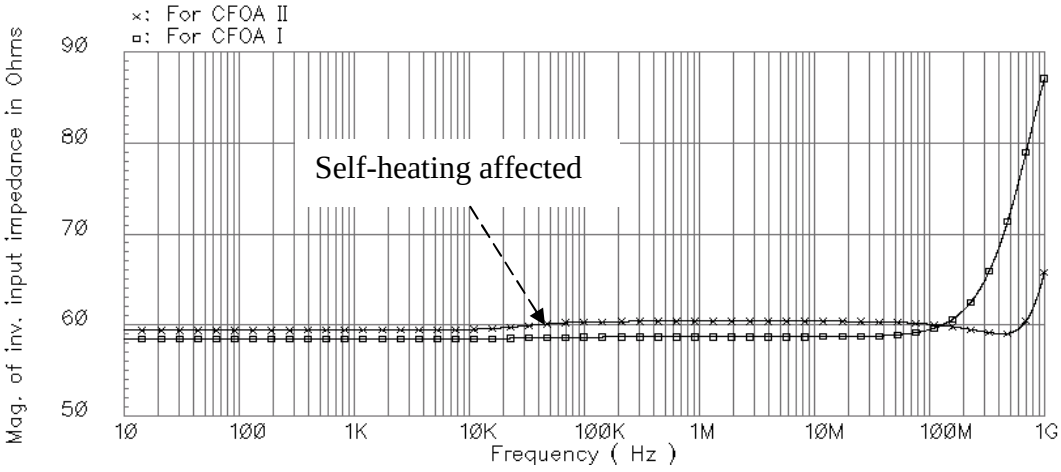


Figure 6.18 Comparison of magnitude of inverting input impedance versus frequency for the CFOA I and CFOA II, with self-heating enabled.

The inverting input terminal impedance, $Z_{inv}(s)$, response of CFOA II is affected by self-heating, while there is no effect of self-heating at all on CFOA I due to the cascode transistors Q_6 and Q_{12} used at the input stage. The dc inverting input impedance, $Z_{inv}(0)$ for CFOA I, and CFOA II are 58.4 Ω, and 59.4 Ω, respectively.

6.4.3 Time-Domain Simulations

A large-signal transient step response for a -0.5 V to 0.5 V input square wave with rise and fall times of 1 μs and pulse width of 100 μs with 50% duty cycle for the CFOA I of Fig. 6.2 in the non-inverting unity gain configuration is shown in 6.19. It is seen that both the positive and negative thermal tail can be as low as 10 μV and a 95% drop in the thermal tail happens in about 20 μs due to the thermal time constant of 5 μs, used in the simulation. A very similar response can be obtained for CFOA II.

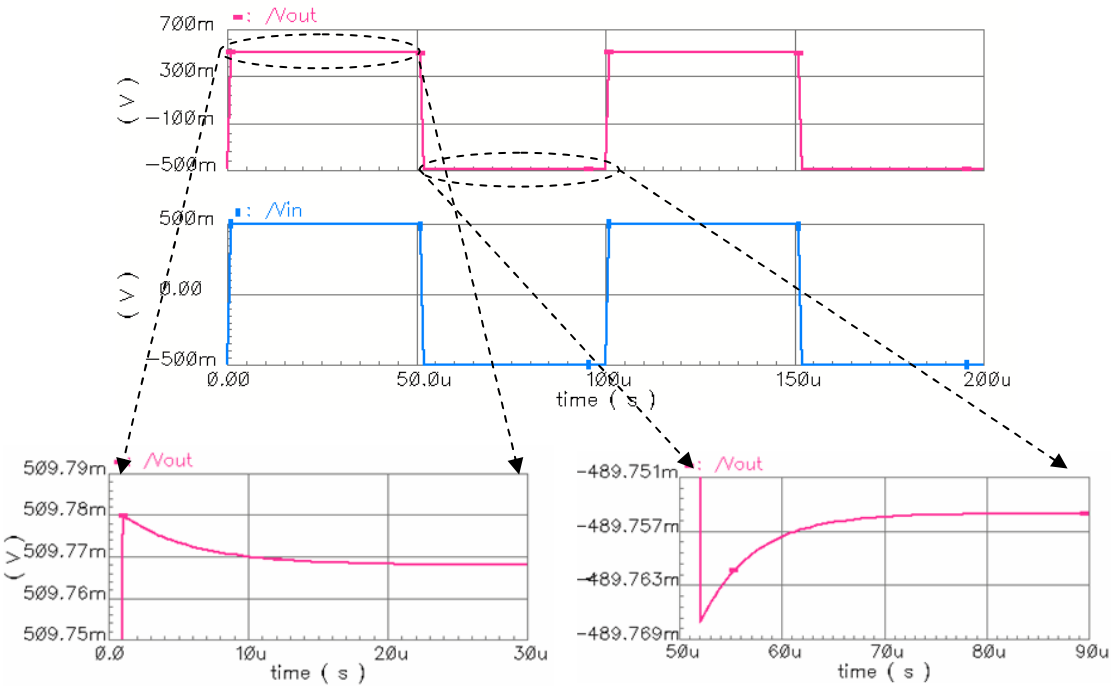


Figure 6.19 Large-signal transient response of the CFOA I, with self-heating enabled.

6.5 Summary of simulated parameters for the CFOAs

A comparison of simulated parameters of all designed CFOAs, characterizing their performances is summarized in Table 6.1.

Table 6.1 Summary of Simulated Parameters for All Designed CFOAs Using the VBIC Models Provided in Tables 2.9 and 2.10.

	Classical COFA of Fig. 5.2	**Classical COFA of Fig. 5.3**	**CFOA I**	**CFOA II**	**Unit**
DC offset current (I_{off})	0.73	-7.16	-9.77	-61.70	μA
Input offset voltage (V_{os})	24.12	24.65	0.24	1.80	mV
$\|(Z_T(0))\|$	0.45	2.42	2.48	2.62	MV/A
Rcritical	43.13	70.22	83.27	91.00	Ω
CMIR (pos/neg)	4.08/4.03	3.20/3.30	2.80/2.78	3.77/3.8	V
Output swing (pos/neg)	4.08/4.01	3.20/3.17	2.77/2.67	3.69/3.17	V
CMRR(0)	59.38	59.33	90.61	65.67	dB
PSRRp(0)	84.14	84.26	80.10	65.53	dB
PSRRn(0)	85.32	88.54	82.58	65.78	dB
SRp with R_f = 1 KΩ	570.00	570.00	450.00	240.00	V/μs
SRn with Rf = 1 KΩ	560.00	560.00	490.00	200.00	V/μs
Maximum 3-dB closed-loop BW	418.70	418.20	400.00	300.00	MHz
R_{in}(Non-inverting terminal)	6.44	7.46	2.62	3.27	MΩ
R_{in}(Inverting terminal)	55.00	55.09	58.45	59.40	Ω
R_{out}(Output impedance) in open-loop configuration	163.67	746.79	787.37	846.98	Ω

6.6 Summary

Two new topologies of self-heating tolerant CFOAs are proposed, and their performances are compared and contrasted with the classical topology of the CFOA. It is also verified through simulation that self-heating tolerant CFOA circuits are CMIR limited. The proposed CFOA circuits are fabricated with the VIP10^{TM} bipolar process technology. The measurement of various parameters of the CFOAs will be presented in the next chapter.

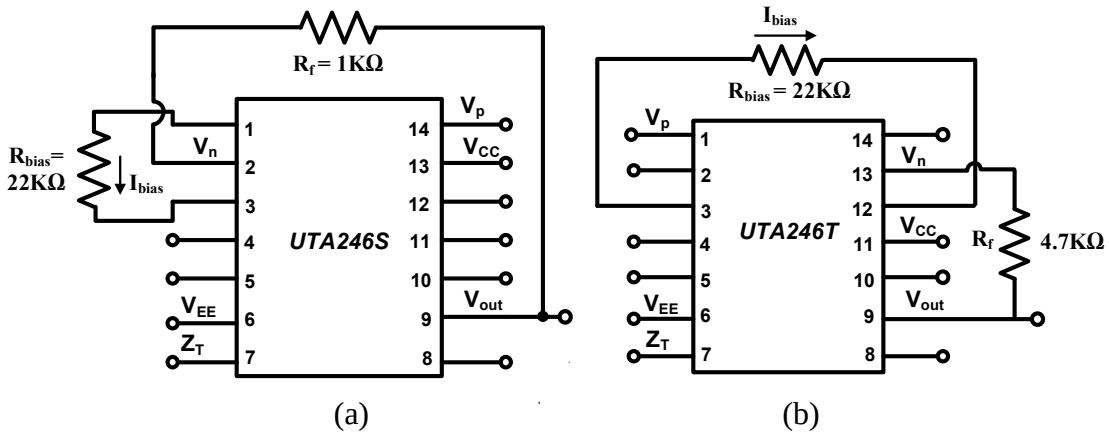
CHAPTER 7

FABRICATION AND MEASUREMENT

This chapter provides the details of the measurement and evaluation of the designed current-feedback amplifiers, UTA246S and UTA246T, which were fabricated with the VIP10^{TM} bipolar process technology. First, the dc measurements of both in the inverting and non-inverting configurations will validate the design functionality. This will also give an understanding of the dependence of the input-offset voltage on the feedback resistor. The details of the measurement of the CMRR and PSRR using different test circuits will be presented next. The measurement of the frequency responses of the open-loop transimpedance, inverting, non-inverting input impedance, and output impedance will be presented using an impedance analyzer. Finally, the measurement of the thermal tail in the step response of the CFOAs will be presented. The chapter concludes with a correlation between simulation and measurement.

7.1 DIP Package Pin Description for CFOA I and CFOA II

The test chips, CFOA I shown in Fig. 6.2, and CFOA II shown in Fig. 6.4, are identified as UTA246S and UTA246T, respectively, and were assembled within a 14 pin DIP package. The pin configurations for UTA246S and UTA246T are shown in Fig 7.1, in which the CFOAs are configured in the non-inverting unity gain configuration. The description for each external pin is provided in Table 7.1.



(a) (b)

Figure 7.1 DIP package for (a) CFOA I (UTA246S) (b) CFOA II (UTA246T), with external bias resistor, and configured in the non-inverting unity gain.

Table 7.1 Pin Description for UTA246S (CFOA I of Fig. 6.2) and UTA246T (CFOA II of Fig. 6.4).

Pin Number	For UTA246S	For UTA246T
1	Pos. bias resistor terminal (A)	Non-inverting input (V_p)
2	Inverting input terminal (V_n)	Internal input (D)
3	Neg. bias resistor terminal (B)	Neg. bias resistor terminal (B)
4	Internal pin (D)	Internal pin (E)
5	Internal pin (F)	Internal pin (F)
6	Neg. power supply rail ($-V_{EE}$)	Neg. power supply ($-V_{EE}$)
7	Transimpedance node(Z_T)	Transimpedance node(Z_T)
8	Internal pin (H)	Internal pin (H)
9	Output terminal (V_{out})	Output terminal (V_{out})
10	Internal pin (G)	Internal pin (G)
11	Internal pin (E)	Pos. power supply rail ($+V_{CC}$)
12	Internal pin (C)	Pos. bias resistor terminal (A)
13	Pos. power supply rail ($+V_{CC}$)	Inverting terminal (V_n)
14	Non-inverting input (V_p)	Internal pin (C)

Since UTA246S and UTA246T were fabricated as test chips, several internal pins were made accessible externally. These internal pins have no physical significance from external interface. These are just for debugging purposes.

7.2 Measurement of CFOA I (UTA246S) Parameters

The positive, V_{CC}, and negative, V_{EE}, rail voltages of Fig. 7.1(a) were provided through an Agilent E3631A power supply. The external bias resistor, R_{bias}, was set to 22 kΩ, and a bias current, I_{bias}, was measured as 305 μA using an Agilent 34410A (6½ digit high performance digital multimeter).

7.2.1 DC Measurement

Figure 7.2 shows a CFOA in the non-inverting gain configuration. The test circuit of Fig. 7.2(a) was wired on a breadboard. The input-offset voltage, V_{os}, defined as a voltage required at the V_p to drive the output voltage, V_{out}, to zero, was measured with different values of the feedback resistor, R_f, and is provided in Table 7.2.

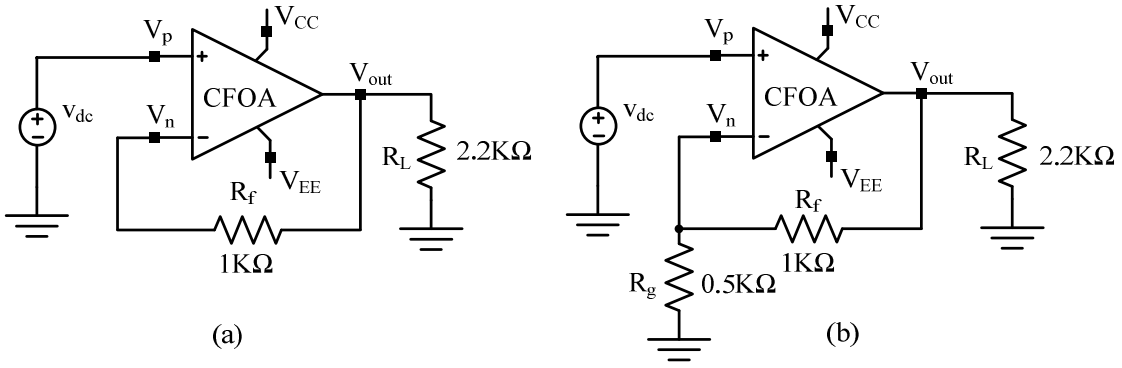
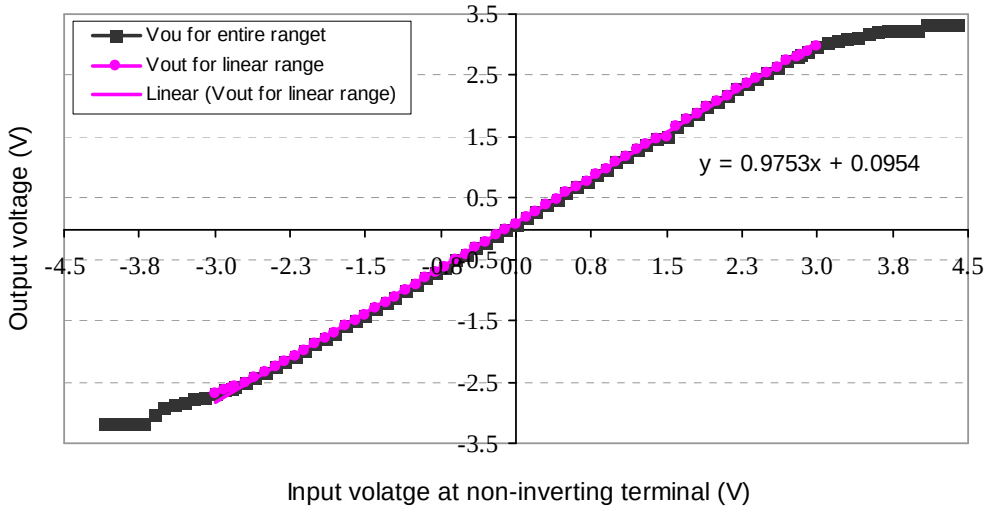


Figure 7.2 A CFOA in the non-inverting gain configuration [52] (a) with a gain of 1. (b) with a gain of 3.

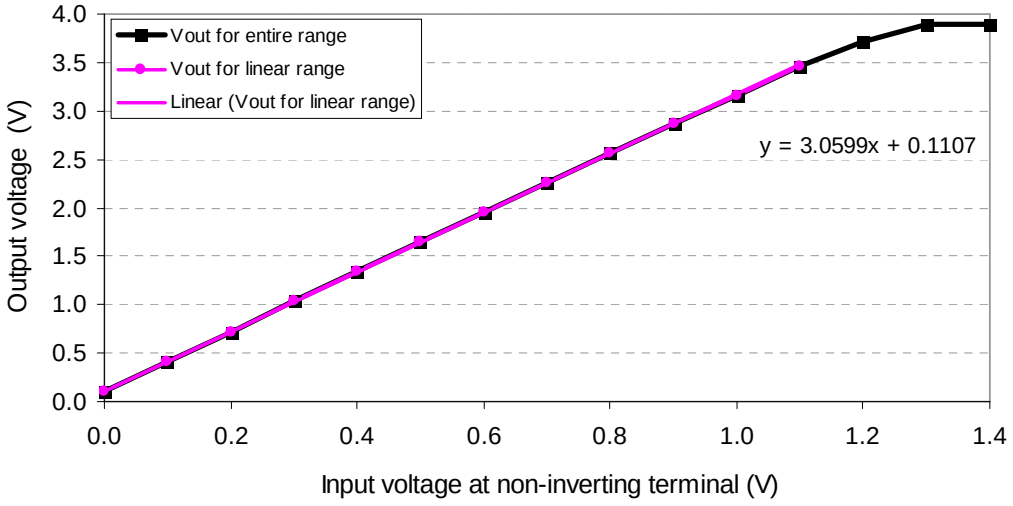
Table 7.2 Input Offset-Voltages for UTA246S in the Non-Inverting Unity Gain Configuration with R_L = 2.2 kΩ.

Feedback resistor, R_f	Simulated V_{os}	Measured V_{os}
0.5 kΩ	-2.00 mV	80.10 mV
1.0 kΩ	-3.36 mV	167.95 mV
4.7 kΩ	-17.60 mV	799.50 mV

As shown in Table 7.2, the measurement shows a higher value of input offset-voltage in comparison with the simulations. Because of a low input offset-voltage, the optimal feedback resistor was chosen as 1 kΩ. The dc transfer characteristics for circuits in Figs. 7.2(a), and 7.2(b) were measured, and are illustrated in Figs. 7.3(a) and 7.3(b), respectively.



(a)



(b)

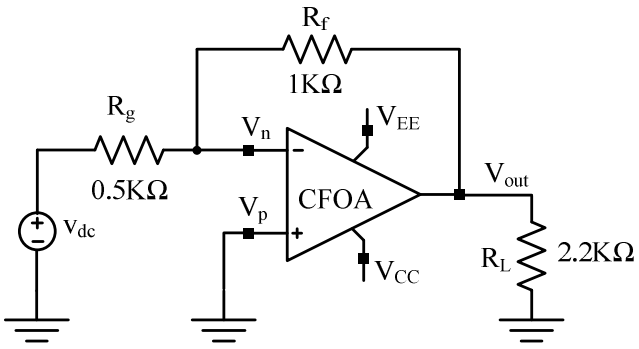
Figure 7.3 Transfer characteristics of the circuits of (a) Fig. 7.2(a). (b) Fig. 7.2(b).

The data in the linear region of Figs. 7.3(a) and 7.3(b) is curve-fitted with a linear regression. The voltage gain is found to be 0.975 V/V versus a theoretical value of 1.0 V/V for the amplifier of Fig. 7.2(a), and 3.06 V/V versus a theoretical value of 3.0 V/V for the amplifier of Fig. 7.2 (b). The CMIR and dynamic output swing for UTA246S can be obtained from Fig. 7.3(a), and are provided in Table 7.3.

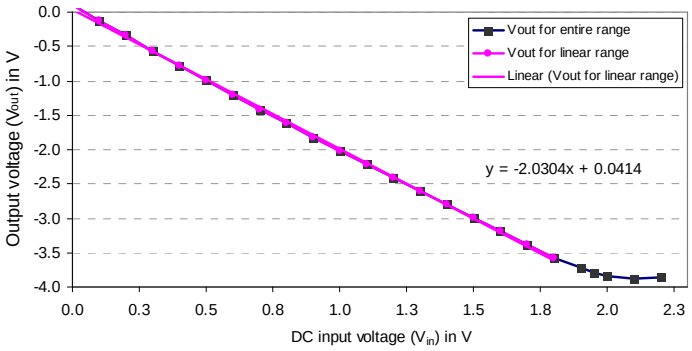
Table 7.3 CMIR and Output Dynamic Range for the CFOA, UTA246S.

Parameters	Simulated	Measured
CMIR	5.8 V	5.1 V
Output dynamic range	5.6 V	5.2 V

Figure 7.4(a) shows an inverting amplifier configuration of the CFOA, UTA246S with a gain of −2 V/V, and a measured dc transfer characteristic is shown in Fig. 7.4(b).



(a)



(b)

Figure 7.4 (a) UTA246S in an inverting gain configuration. (b) Transfer characteristics.

7.2.2 CMRR and PSRR Measurement

The circuit configuration of Fig. 7.5 was used to measure the dc CMRR and PSRR of UTA246S. The circuit was wired on a breadboard. The resistors used in the circuit were carbon film resistors with a 5% tolerance.

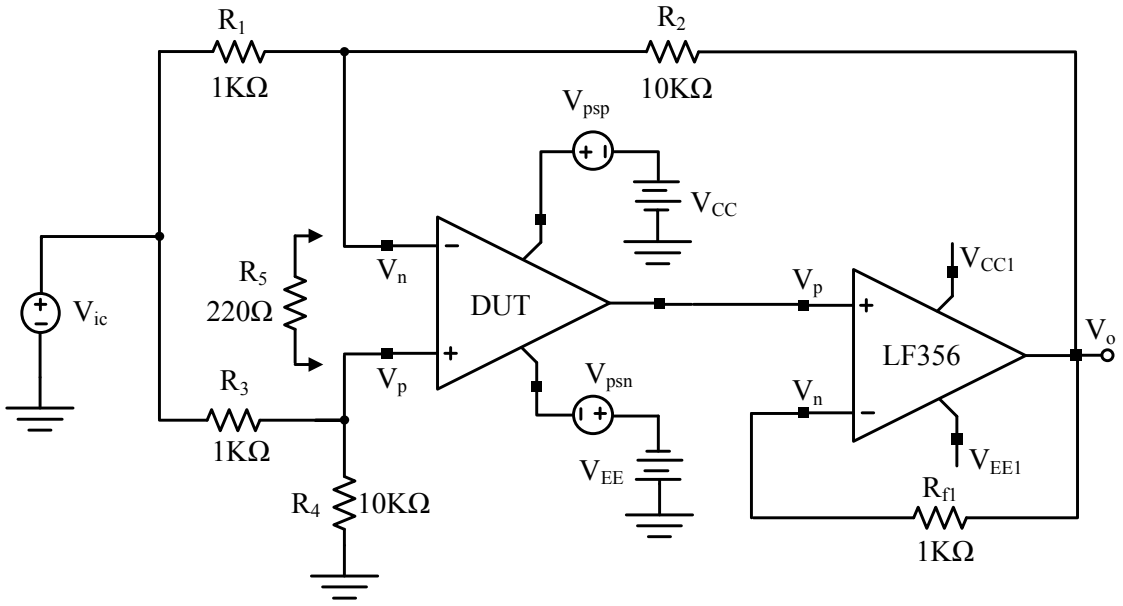


Figure 7.5 CMRR and PSRR test circuit [47]. V_{psp} and V_{psn} are small changes in power supplies.

The observed nodal voltages were recorded from the circuit in Fig. 7.5 with UTA246S as the DUT for the dc CMRR measurement, and are provided in Table 7.4.

Table 7.4 Data Collected for CMRR Measurement.

All voltages are in Volt						
$R_5(i)$	$V_{in}(a)$	$V_o(a)$	$V_{in}(b)$	$V_o(b)$	ΔV_{in}	$\Delta V_o[R_5(i)]$
$R_5(1) = \infty$	+1.00	-0.4375	-1.00	-0.4334	+ 2.00	-0.0041
$R_5(2) = 220\ \Omega$	+1.00	-0.6925	-1.00	-0.6824	+2.00	-0.0101

The CMRR can be obtained [47] using

$$CMRR = \left| \frac{R_4(R_2 + R_4)}{R_3 + R_4} \left[\frac{1}{R_5(1)} - \frac{1}{R_5(2)} \right] \left[\frac{V_{in}(a) - V_{in}(b)}{\Delta V_o[R_5(1)] - \Delta V_o[R_5(2)]} \right] \right| \tag{7.2}$$

Equation (7.2) evaluates to 88.80 dB with the values provided in Table 7.4.

Data taken from the circuit of Fig. 7.5 with UTA246S as the DUT for the $PSRR_p$ and $PSRR_n$ measurement is given in Table 7.5 and 7.6, respectively.

Table 7.5 Data Collected for $PSRR_p$ Measurement.

All voltages are in Volt and V_{ic} = 0 V						
$R_5(i)$	$V_{psp}(a)$	$V_o(a)$	$V_{psp}(b)$	$V_o(b)$	ΔV_{in}	$\Delta V_o[R_5(i)]$
$R_5(1) = \infty$	0.0	-0.4327	1.0	-0.5148	1.0	-0.0821
$R_5(2) = 220\ \Omega$	0.0	-0.6836	1.0	-0.7823	1.0	-0.0987

Table 7.6 Data Collected for $PSRR_n$ Measurement.

All voltages are in Volt and V_{ic} = 0 V						
$R_5(i)$	$V_{psn}(a)$	$V_o(a)$	$V_{psn}(b)$	$V_o(b)$	ΔV_{psn}	$\Delta V_o[R_5(i)]$
$R_5(1) = \infty$	0.0	-0.4329	-1.0	-0.3442	1.0	-0.0887
$R_5(2) = 220\ \Omega$	0.0	-0.6834	-1.0	-0.5674	1.0	-0.1160

The $PSRR_p$ and $PSRR_n$ can be obtained [47] using

$$PSRR_p = \left| (R_2 + R_4) \cdot \left[\frac{1}{R_5(1)} - \frac{1}{R_5(2)} \right] \left[\frac{V_{psp}(a) - V_{psp}(b)}{\Delta V_o[R_5(1)] - \Delta V_o[R_5(2)]} \right] \right| \tag{7.3}$$

$$PSRR_n = \left| (R_2 + R_4) \cdot \left[\frac{1}{R_5(1)} - \frac{1}{R_5(2)} \right] \left[\frac{V_{psn}(a) - V_{psn}(b)}{\Delta V_o[R_5(1)] - \Delta V_o[R_5(2)]} \right] \right| \tag{7.4}$$

Equation (7.3) evaluates as 74.77 dB with the values provided in Table 7.5, and (7.4) can be evaluated as 70.45 dB using the values provided in Table 7.6.

7.2.2.1 CMRR and PSRR Measurement Using a Universal Test Circuit

The circuit configuration of Fig. 7.6 can also be used to measure the CMRR, and PSRR of a CFOA, along with the open-loop offset-voltage, and open-loop gain [47]. The circuit was wired on a breadboard. The resistors used had a 5% tolerance, and capacitors had a 20% tolerance. Measured data from the circuit of Fig. 7.6 with UTA246S as the DUT are provided in Tables 7.7 through 7.9.

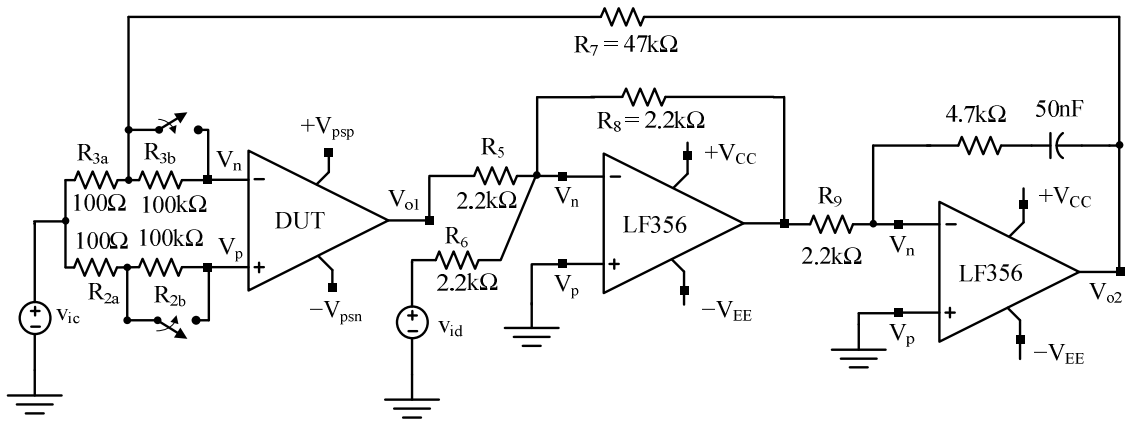


Figure 7.6 A universal test circuit for measuring op-amp parameters [47]. The DUT power supplies are $V_{psp} = +5+\Delta V_{psp}$ and $V_{psp} = -5+\Delta V_{psn}$.

Table 7.7 Data Collected for the Open-Loop Offset Voltage and Open-Loop Gain.

V_{o2} vs V_{id} for $V_{ic} = \Delta V_{psp} = \Delta V_{psn} = 0$	
V_{id} (V)	V_{o2} (V)
-1.0	-3.103
0.0	-3.045
+1.0	-2.996

The offset voltage can be calculated [47] using

$$V_{os} = -\frac{R_{3a}}{R_{3a} + R_7} V_{o2} \tag{7.5}$$

Equation (7.5) gives -6.46 mV with $V_{o2} = -3.045$ V for $V_{id} = 0$ (Table 7.7).

The open-loop gain of an op-amp can be calculated [47] using

$$G_{Vdm}(0) = \frac{R_5}{R_6}\left(1+\frac{R_7}{R_{3a}}\right)\frac{1}{\frac{\Delta V_{o2}}{\Delta V_{id}}} \tag{7.6}$$

The equation (7.6) gives 8.8 kV/V with the values of V_{o2}, provided in Table 7.7, for V_{id} = −1.0 V and V_{id} = +1.0 V. Since equation (7.6) is developed for the open-loop voltage gain measurement for a VFOA, it may not be applicable for the measurement of the open-loop transimpedance of a CFOA.

The CMRR can be calculated [47] using

$$CMRR = -\left(1+\frac{R_7}{R_{3a}}\right)\left(\frac{1}{1-\frac{\Delta V_{o2}}{\Delta V_{ic}}}\right) \tag{7.7}$$

Table 7.8 Data Collected for CMRR Measurement.

V_{o2} versus V_{ic} $V_{id} = \Delta V_{psp} = \Delta V_{psn} = 0$	
V_{ic} (V)	V_{o2} (V)
-1.0	-3.996
1.0	-2.085

The equation (7.7) evaluates as 80.49 dB with the data provided in Table 7.8.

Table 7.9 Data Collected for PSRR Measurement.

For $PSRR_p$		
V_{o2} vs V_{psp} for $V_{id} = V_{ic} = \Delta V_{psn} = 0$		
V_{psp} (V)	ΔV_{psp} (V)	V_{o2} (V)
5.0	0.0	-3.046
5.5	0.5	-3.269
6.0	1.0	-3.486

For $PSRR_n$		
V_{o2} vs V_{psn} for $V_{id} = V_{ic} = \Delta V_{psp} = 0$		
V_{psn} (V)	ΔV_{psn} (V)	V_{o2} (V)
-5.0	0.0	-3.044
-5.5	0.5	-3.253
-6.0	1.0	-3.562

The $PSRR_p$ can be calculated [47] using

$$PSRR_p = -\left(1+\frac{R_7}{R_{3a}}\right)\frac{1}{1-\frac{\Delta V_{o2}}{\Delta\left(\Delta V_{psp}\right)}} \tag{7.8}$$

The equation (7.8) gives 60.71 dB with the data provided in Table 7.9 for $PSRR_p$.

The $PSRR_n$ can be calculated [47] using

$$PSRR_n = -\left(1+\frac{R_7}{R_{3a}}\right)\frac{1}{1-\frac{\Delta V_{o2}}{\Delta\left(\Delta V_{psn}\right)}} \tag{7.9}$$

The equation (7.9) gives 57.64 dB with the data provided in Table 7.9 for $PSRR_n$.

A summary of measured parameters is provided in Table 7.10

Table 7.10 Comparison of Measured Data from the Circuits of Figs. 7.5 and 7.6.

Parameters	With Fig. 7.5	With Fig. 7.6
V_{os}(Open-loop)	N/A	-6.46 mV
CMRR	88.80 dB	80.49 dB
$PSRR_p$	74.77 dB	60.71 dB
$PSRR_n$	70.45 dB	57.64 dB

The measured CMRR and PSRR from the test circuit of Fig. 7.5 are higher than those from the circuit of Fig. 7.6 as shown in Table 7.10. As shown in Table 7.2, the input-offset voltage of UTA246S increases drastically with a higher value of feedback resistor, R_f,. Thus, the circuit of Fig 7.6, in which a large value of feedback resistor, R_7, is recommended, may have some measurement error. As a consequence, the measurement of CMRR and PSRR with the circuit of Fig. 7.6 is highly sensitive to the value of input sources, v_{ic}, v_{id}, v_{psp}, and v_{psn} in Fig. 7.6. Hence, the test circuit of Fig. 7.5

is preferred over the circuit of Fig. 7.6 for the rejection ratios measurement. It is also found that there is a good correlation between simulation and measurement of CMRR and PSRR with the test circuit of Fig. 7.5.

7.2.3 Transient Sine Response Measurement

A Fluke 397 universal waveform generator with a sampling rate of 125 MS/s was used to generate sine and square waves to drive the inverting/non-inverting terminal of UTA246S as needed. The output waveform from the circuit of interest was captured on an Agilent Infiniium DSO81204B – 12 GHz, sampling rate 40 GS/s. The input to DSO81204B is 50 Ω, an active probe (Agilent 1169A) with single ended input resistance of 25 kΩ was used to probe the signal. A 10 MHz sine wave response of UTA246S in the non-inverting unity gain configuration of Fig. 7.2(a) was measured as shown in Fig. 7.7.

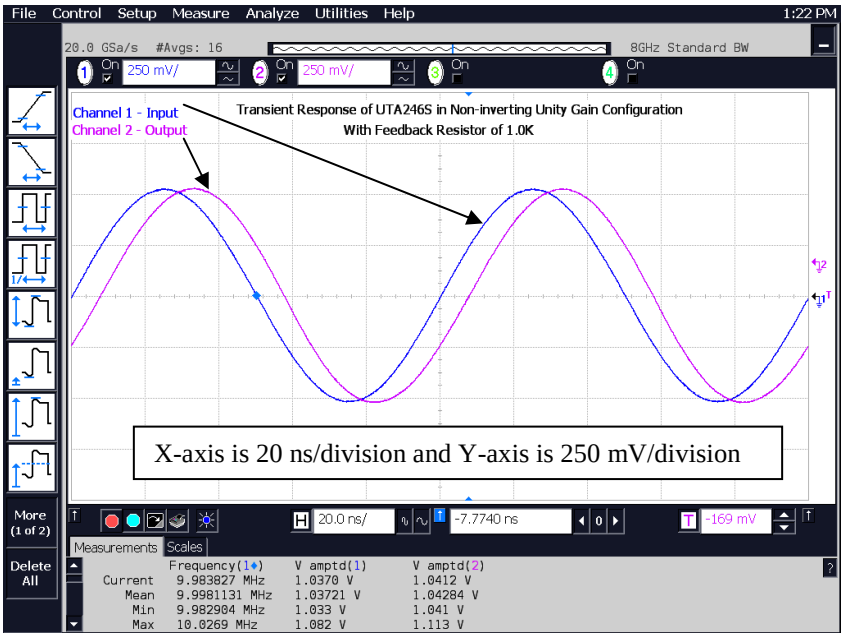


Figure 7.7 Transient sine response of UTA246S, in the non-inverting unity gain configuration of Fig. 7.2(a) with feedback resistor, R_f = 1 kΩ.

It can be inferred from Fig. 7.7 that there is a phase shift of about -45 degrees at 10 MHz. During measurement, a phase shift of -180 degrees was obtained at a frequency of about 25 MHz.

7.2.4 Frequency-Domain Measurement

7.2.4.1 Frequency Response of the Non-Inverting Unity Gain Configuration

The circuit of Fig. 7.2(a) showed a rapid oscillation with a large magnitude in the time-domain step response, and a 20% peaking in the frequency response of the non-inverting unity gain configuration with UTA246S for a value of feedback resistor, R_f, lower than 0.5 kΩ. An optimal value of R_f was found to be 1 kΩ experimentally so as to minimize peaking in the frequency response. This also yields a lower input offset-voltage as well as shown in Table 7.2. The test circuit shown in Fig. 7.2(a) was built on a protoboard. The sine wave transient responses were obtained for over a frequency range of 100 Hz and 50 MHz on DSO81204B, and corresponding magnitude and phase were measured using DSO's utilities feature. Such a response is shown in Fig. 7.8.

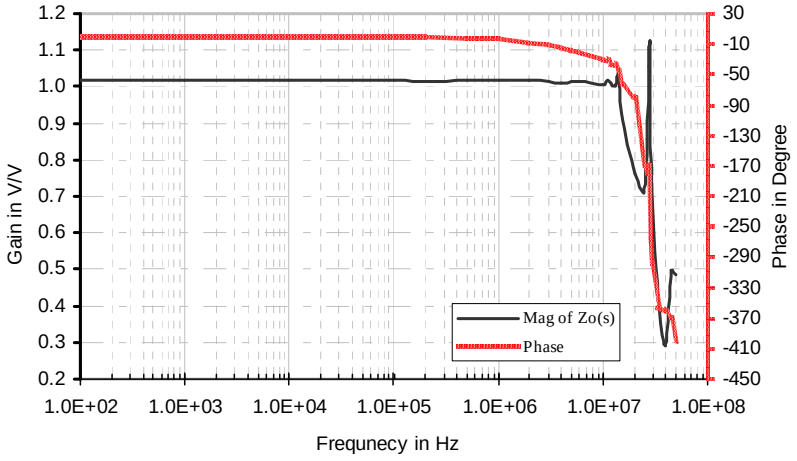


Figure 7.8 Frequency response of UTA246S in the configuration shown in Fig. 7.2(a).

The sine responses beyond 20 MHz were highly influenced by parasitic from the protoboard layout. The measurement of the protoboard and on-chip parasitic elements is provided in Appendix F. From Fig. 7.8, it is found that the maximum measured closed-loop 3-dB bandwidth in the non-inverting unity gain configuration is 11 MHz.

7.2.4.2 Measurement of Open-Loop Transimpedance

Since UTA246S is a test chip, the transimpedance node is externally accessible as shown in Fig. 7.1(a). The test circuit shown in Fig. 7.9 can be used to measure the transimpedance response of a CFOA. The selection of the values of R_f and C of Fig. 7.9 is strongly dependent on the dominant pole frequency of the transimpedance function of a CFOA to be measured. The pole frequency caused by the *RC* network of Fig. 7.9 should be smaller than the dominant pole of the high-gain node, *Z*, of the CFOA to get a true open-loop transimpedance response [52]. The feedback resistance, R_f, stabilizes the dc bias, and the capacitor, *C*, provides a short circuit to high frequencies. Hence the circuit looks like an open circuit for an ac signal. Through iterative measurements, a capacitor of 100 μF and a feedback resistor of 47 kΩ were found to be a good choice.

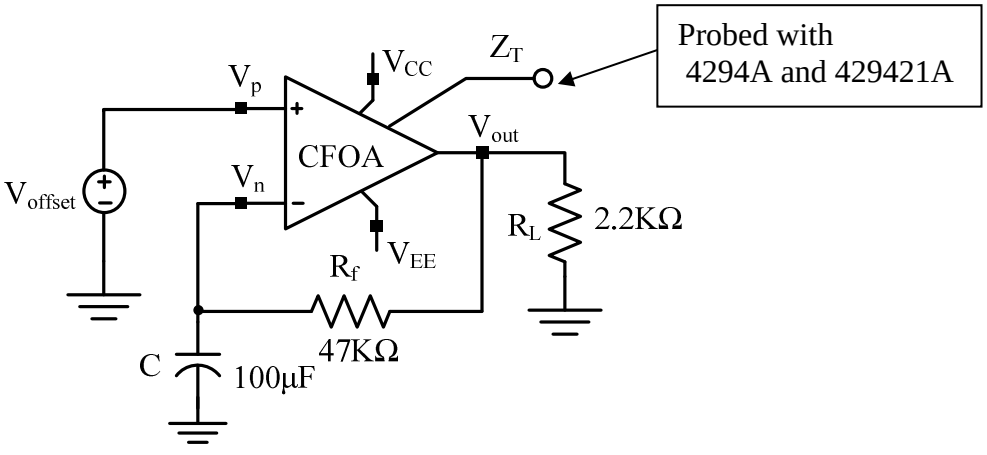


Figure 7.9 Test circuit for measuring the open-loop transimpedance of UTA246S.

An offset voltage, V_{offset}, of +2.61 V was applied to the non-inverting terminal of the test circuit to ensure that V_{out} is close to zero, and an impedance probe was applied at the Z_T terminal of UTA246S as shown in Fig. 7.9. Fig. 7.10 shows such a measured response along with a simulated response (without layout parasitic capacitances).

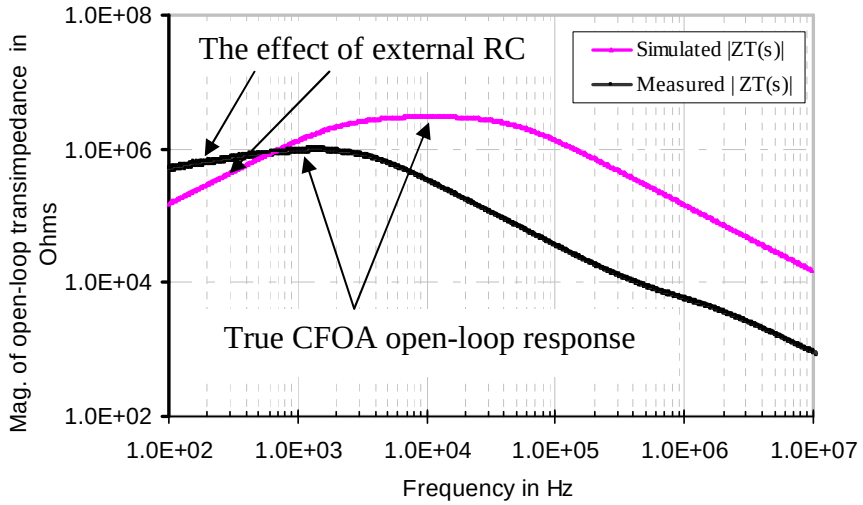


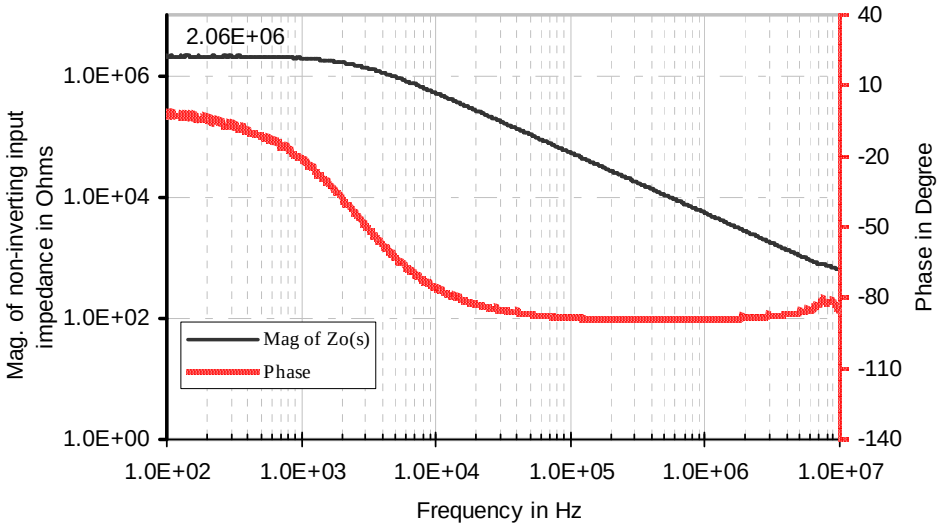
Figure 7.10 Magnitude response of the open-loop transimpedance of UTA246S using circuit of Fig. 7.9.

As illustrated in Fig. 7.10, the low frequency response is influenced by the R_fC network of Fig. 7.9, while the high frequency response can be treated as an open-loop response because the capacitor, C, acts like a short circuit. The large difference between simulation and measurement, as shown in Fig. 7.10, can be attributed to the missing layout parasitic capacitances to some extent. This method discussed in this section is only applicable because of the accessibility of the transimpedance node externally.

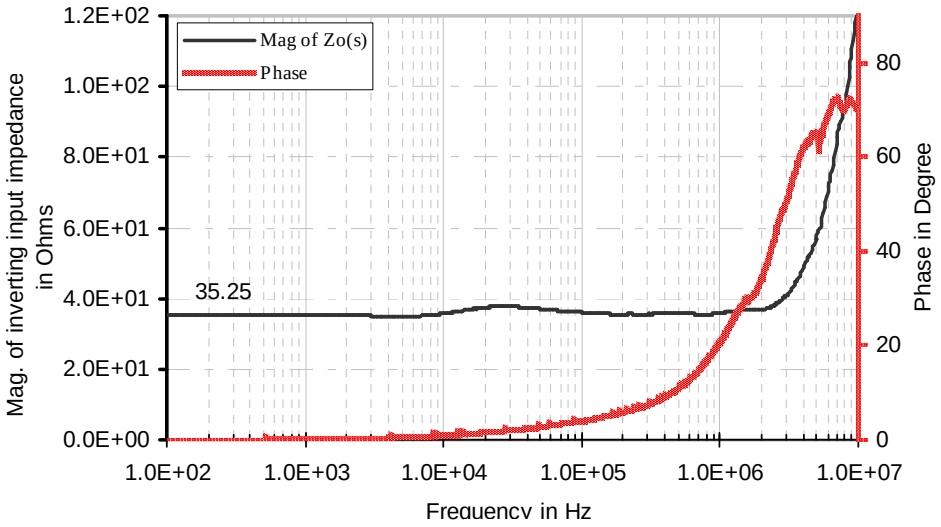
7.2.4.3 Measurement of Non-Inverting and Inverting Input Impedance

The UTA246S chip was configured in the non-inverting unity gain configuration as shown in Fig. 7.2(a), and a dc offset voltage was applied through an Agilent 42941A

probe connected to an impedance analyzer (Agilent 4294A). Under this configuration, the frequency responses of input impedance of both non-inverting and inverting terminals of UTA246S were measured by probing the V_p and V_n terminal of Fig. 7.2(a). Such responses are shown in Figs. 7.11(a) and 7.11(b).



(a)



(b)

Figure 7.11 Frequency response of the input impedance of the (a) non-inverting terminal (b) inverting terminal of the CFOA, UTA246S.

7.2.4.4 Measurement of Output Impedance

A non-inverting unity gain configuration shown in Fig. 7.2(a) with UTA246S was built on a protoboard without any load. The frequency response, obtained by probing the output terminal using an impedance analyzer probe is shown in Fig. 7.12.

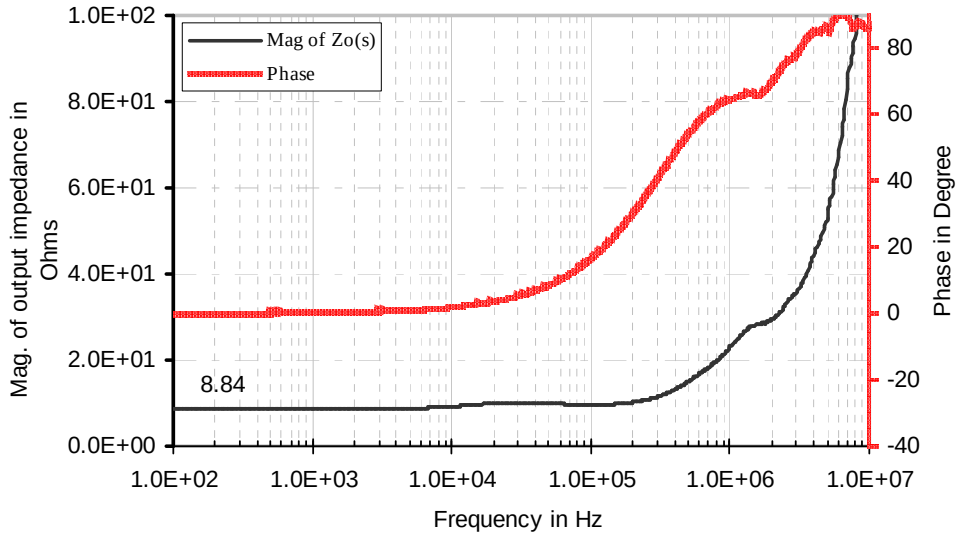


Figure 7.12 Frequency response of the output impedance of UTA246S, in non-inverting unity gain configuration with feedback resistor, R_f = 1 kΩ and no load.

To extract open-loop output impedance, a simulation was done both in the closed-loop and in the open-loop configuration. The simulation data is provided in Table 7.11.

Table 7.11 Simulation Data for the Output Resistance of UTA246S.

Parameters	In open-loop (R_{oopl})	In closed-loop with R_f = 1 kΩ (R_{ocl})	In closed-loop with R_f = 47 kΩ (R_{ocl})
Output Impedance	633.8 Ω	0.22 Ω	9.60 Ω
Return Difference	N/A	2872.73	65.83
Theoretical Return Difference, $1+Z_T(0)/R_f$	N/A	2981.00	64.40

As illustrated in Table 7.11, the reduction in output resistance from open-loop to closed-loop configuration follows expression (7.10).

$$Z_{ocl}(0) = \frac{Z_{oopl}(0)}{1 + Z_T(0)/R_f} \tag{7.10}$$

With a return ratio of 2872.73 from Table 7.11, the measured output resistance in the open-loop can be approximated as 8.84 times 2872.73, which is equal to 2.53 kΩ.

7.2.5 Large-Signal Step Response Measurement

7.2.5.1 Slew Rate Measurement

The CFOA, UTA246S of Fig. 7.2(a) was excited with a -0.5 V to 0.5 V input square wave with a rise and fall times of about 6.3 ns, pulse width of 1 μs with 50% duty cycle. This was produced by a Fluke 397 waveform generator. The step response was obtained using a digital oscilloscope, DSO81204B, and is shown in Fig. 7.13.

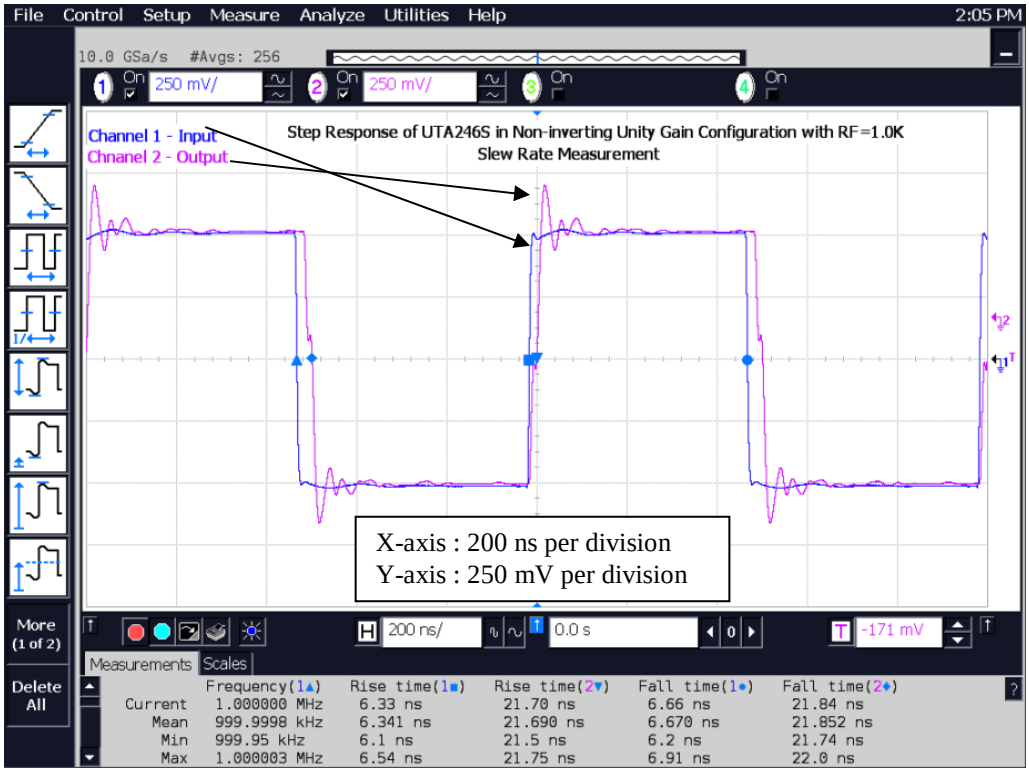


Figure 7.13 Large-signal step response of UTA246S in the unity gain configuration, with R_L = 25 kΩ and C_L = 0.35 pF (DSO acts as a load).

The dependence of slew rate on the amplitude of input square wave was studied experimentally, and measurement data is summarized in Table 7.12.

Table 7.12 Slew Rate of UTA246S in the Non-Inverting Unity Gain Configuration with a Feedback Resistor of 1.0 kΩ.

Parameters	With input pulse of Vp-p = 1 V		With input pulse of Vp-p = 2 V		With input pulse of Vp-p = 4 V	
	Simulation	Measurement	Simulation	Measurement	Simulation	Measurement
Slew Rate, SRp	367.6 V/μs	36.89 V/μs	762 V/μs	52.03 V/μs	1172 V/μs	87.07 V/μs
Slew Rate, SRn	356.8 V/μs	36.65 V/μs	742 V/μs	50.92 V/μs	1081 V/μs	72.97 V/μs

It can be inferred from Table 7.12 that slew rate improves with a large amplitude of pulse. This is a unique advantage of a CFOA over a VFOA.

7.2.5.2 Thermal Tail Measurement

For thermal tail measurement, the circuit of Fig. 7.2(a) was excited with a 10 kHz square wave, which had a -0.5 V low voltage and a 0.5 V high voltage with a rise and fall times of 0.78 μs and pulse width of 100 μs with 50% duty cycle. The measured response is shown in Fig. 7.14.

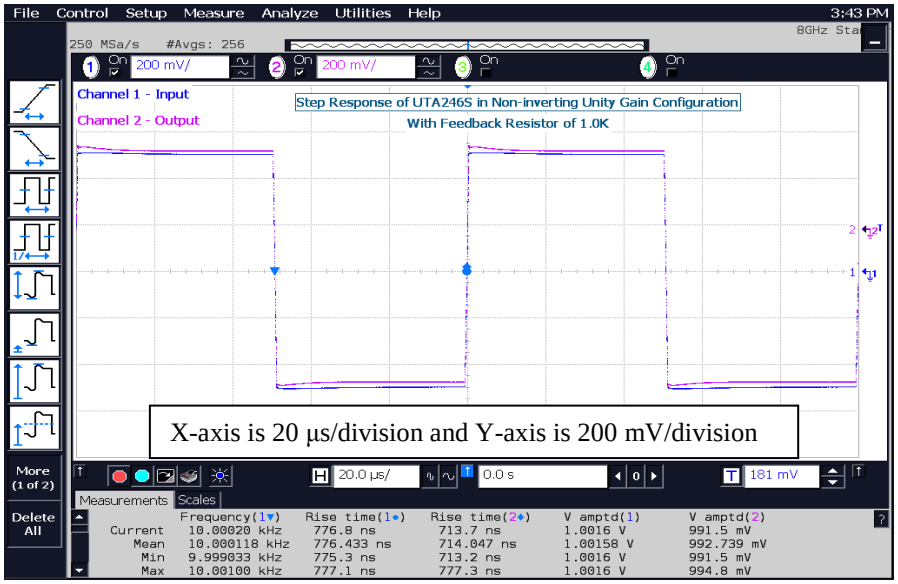
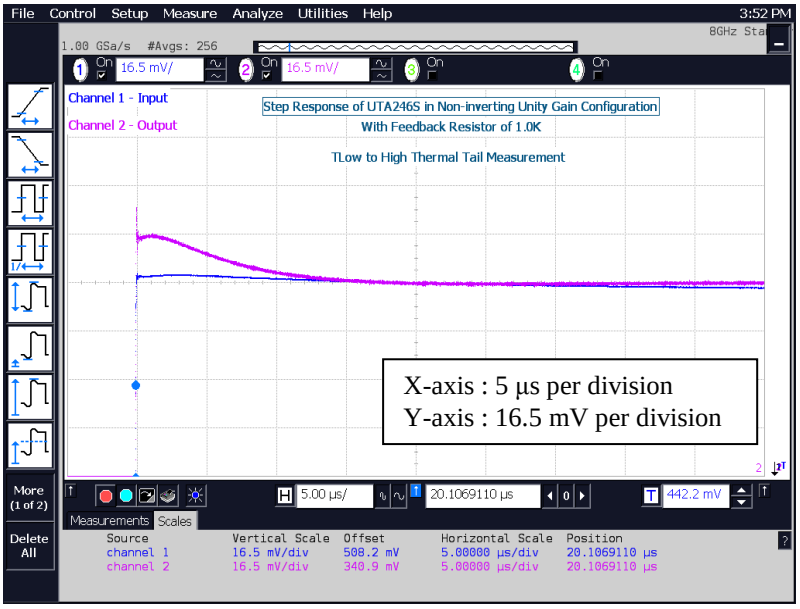
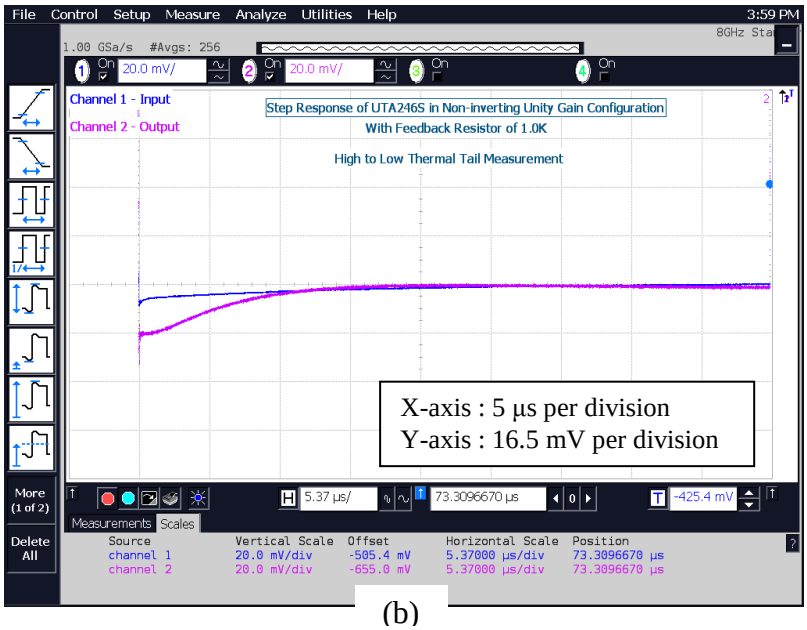


Figure 7.14 Large-signal step response of Fig. 7.2(a) with UTA246S, showing thermal tail.

The positive thermal tail shown in Fig. 7.15(a) and the negative thermal tail shown in Fig. 7.15(b) are 16.5 mV, and 20 mV, respectively. A 95% drop in the magnitude of the thermal tails happens in about 20 µs as illustrated in Fig. 7.15.



(a)



(b)

Figure 7.15 Expanded version of Fig. 7.14 to measure the (a) positive (b) negative thermal tail.

7.2.5.3 Estimation of Thermal Time Constant from a Step Response

To characterize the thermal settling time in the step response shown in Fig. 7.14, it is important to extract the thermal time constant, τ_{th}. One of the methods to extract the thermal time constant is provided here from the raw data of the step response shown in Fig. 7.14. This method is based on the idea of the dependence of relative gain error with time, caused by self-heating. The relative gain error, *RGE*, can be defined as

$$\text{RGE} = \frac{V_{out}(t) - A \cdot V_{in}(t) - V_{oso}}{A \cdot V_{in}(t)} \tag{7.11}$$

where A and V_{oso} are defined for $0 \leq t \leq 50$ μs and found using an averaging technique

$$A = \frac{2 \cdot avg(abs(V_{out}(t)))}{2 \cdot avg(abs(V_{in}(t)))} \tag{7.12}$$

$$V_{oso} = avg(V_{out}(t) - A \cdot V_{in}(t)) \tag{7.13}$$

Figure 7.16 shows a plot of relative gain error versus time for $0 \leq t \leq 20$ μs.

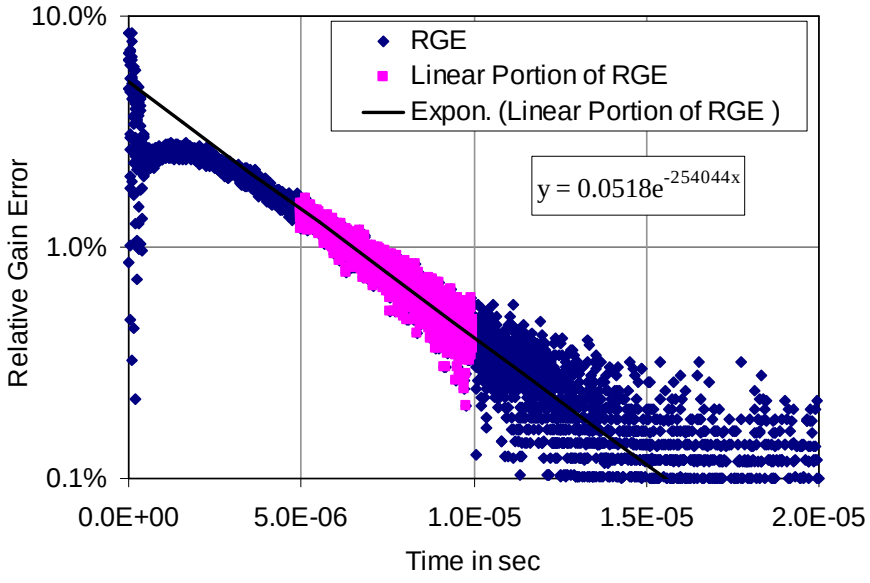


Figure 7.16 Extraction of thermal time constant for Fig. 7.2(a) with UTA246S.

Using an exponential fit to a part of overall data that lies on the theoretical straight line (in this case, 5 μs ≤ t ≤ 10 μs), the magnitude of the thermal tail in terms of gain error for UTA246S is 5.18% with a thermal time constant, τ_{th}, of 3.9 μs.

7.3 Measurement of CFOA II (UTA246T) Parameters

The positive, V_{CC}, and negative, V_{EE}, rail voltages of 5 V for Fig. 7.1(b) were provided through an Agilent E3631A power supply. The external bias resistor, R_{bias}, was set to 22 kΩ, and the bias current, I_{bias}, was measured as 311 μA using an Agilent 34410A (6½ digit high performance digital multimeter).

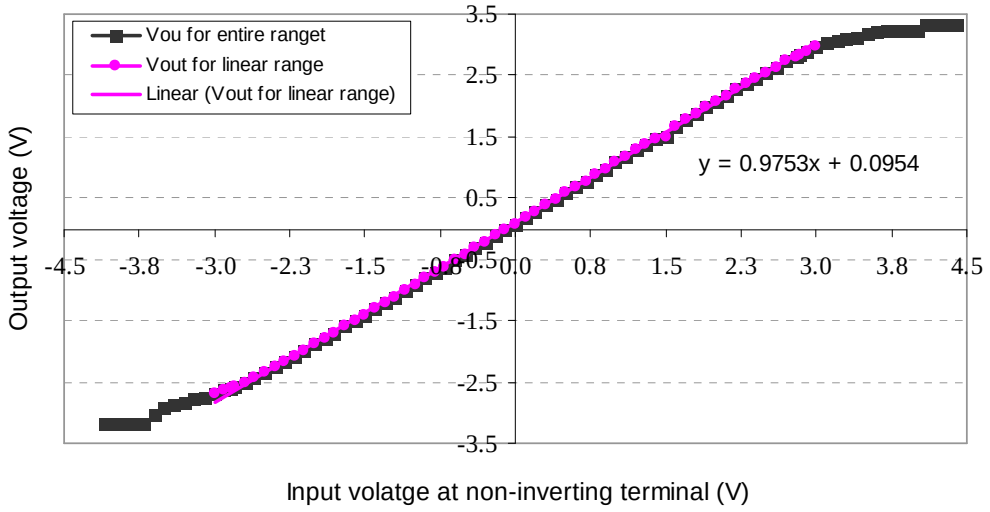
7.3.1 DC Measurement

The input-offset voltage, V_{os}, for UTA246T in the non-inverting unity gain configuration was measured using the circuit of Fig. 7.2(a) with UTA246T as the CFOA. The test circuit was built using a breadboard, and input-offset voltages with various values of feedback resistor, R_f, were measured, and are provided in Table 7.13.

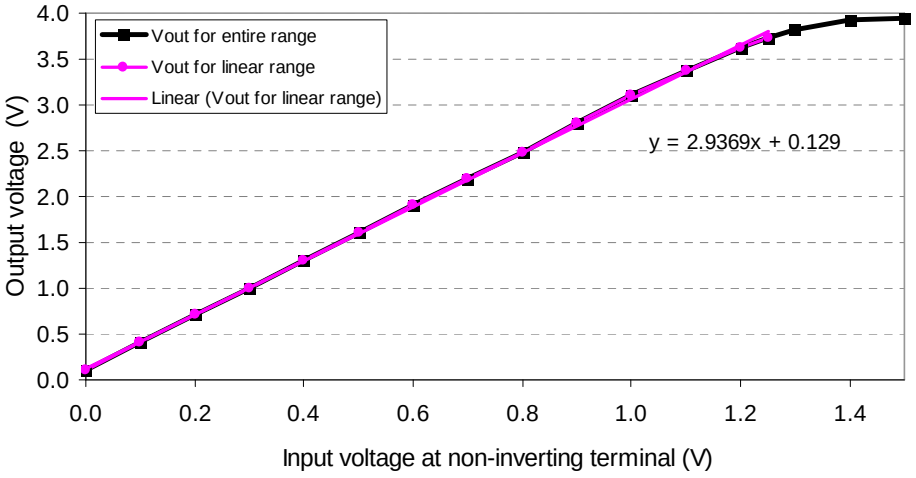
Table 7.13 Input Offset-Voltages for UTA246T Using the Circuit of Fig. 7.2(a).

Feedback resistor, R_f	Simulated V_{os}	Measured V_{os}
1.0 kΩ	-27.85 mV	-41.0 mV
4.7 kΩ	-130.90 mV	-185.0 mV
10.0 kΩ	-278.30 mV	-390.0 mV

Despite the higher value of input offset-voltage in compare to a VFOA, as shown in Table 7.13, with a higher value of feedback resistor, R_f, an optimal value of feedback resistor for the UTA246T was chosen as 4.7 kΩ to minimize the oscillations and settling time. The dc transfer characteristics for circuits in Figs. 7.2(a), and 7.2(b) with UTA246T were measured and are illustrated in Figs. 7.17(a) and 7.17(b), respectively.



(a)



(b)

Figure 7.17 DC transfer characteristics of circuits of Figs. 7.2(a) and Fig. 7.2(b) of UTA246T in the non-inverting configuration with feedback resistor, R_f = 1 kΩ for a gain of (a) 1. (b) 3.

The data in the linear region of Fig. 7.17 is curve-fitted with a linear regression. The voltage gain is found to be 0.975 V/V versus a theoretical value of 1.0 V/V for the amplifier of Fig. 7.2(a), and 2.93 V/V versus a theoretical value of 3.0 V/V for the

amplifier of Fig. 7.2(b) with UTA246T. The CMIR and dynamic output swing of a CFOA can be obtained [46] from Fig. 7.17(a) and are provided in Table 7.14.

Table 7.14 CMIR and Output Dynamic Range for the CFOA, UTA246T.

Parameters	Simulated	Measured
CMIR	6.2 V	6.0 V
Output dynamic range	6.0 V	5.8 V

Figure 7.18 shows the measured dc transfer characteristic of UTA246T, configured for an inverting gain of -2 (Fig. 7.4(a)).

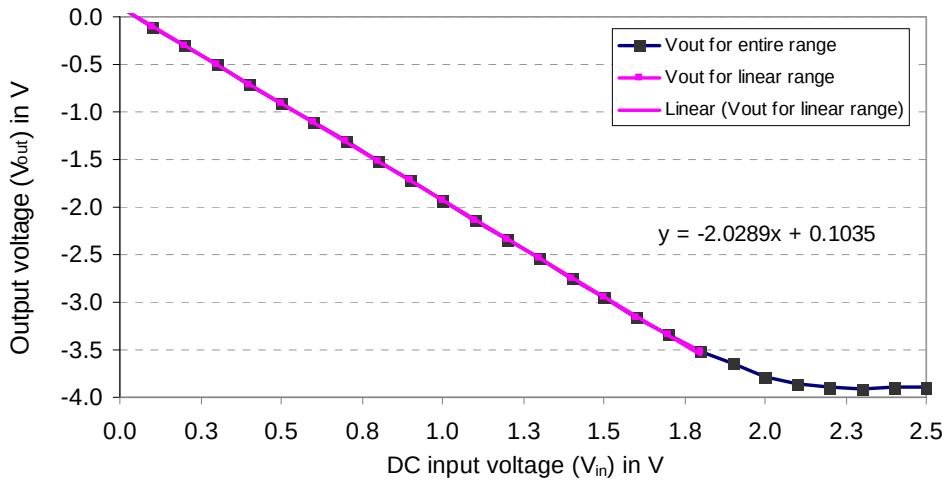


Figure 7.18 Input-output characteristics of UTA246T in the inverting gain configuration with a gain of -2.

7.3.2 CMRR and PSRR Measurement

The circuit configuration of Fig. 7.5 was used to measure the dc CMRR and PSRR of UTA246T as well. The circuit was wired on a breadboard. The resistors used in the circuit of Fig. 7.5 had a 5% tolerance. Data taken from the test circuit in Fig. 7.5 with UTA246T as the DUT for the CMRR measurement are provided in Table 7.15.

Table 7.15 Data Collected for CMRR Measurement.

All voltages are in Volt						
$R_5(i)$	$V_{in}(a)$	$V_o(a)$	$V_{in}(b)$	$V_o(b)$	ΔV_{in}	$\Delta V_o[R_5(i)]$
$R_5(1) = \infty$	+1.00	0.3747	-1.00	0.4019	2.00	-0.0272V
$R_5(2) = 220\ \Omega$	+1.00	0.4133	-1.00	0.5722	2.00	-0.1589V

Equation (7.2) can be evaluated as 71.67dB using the values provided in Table 7.15.

Data taken from the circuit in Fig. 7.5 with UTA246T as the DUT for the $PSRR_p$ and $PSRR_n$ measurement are given in Tables 7.16 and 7.17, respectively.

Table 7.16 Data Collected for $PSRR_p$ Measurement.

All voltages are in Volt and V_{ic} = 0 V						
$R_5(i)$	$V_{psp}(a)$	$V_o(a)$	$V_{psp}(b)$	$V_o(b)$	ΔV_{in}	$\Delta V_o[R_5(i)]$
$R_5(1) = \infty$	-1.0	1.0743	+1.0	0.9259	2.0	0.1484
$R_5(2) = 220\ \Omega$	-1.0	-1.4209	+1.0	-1.2154	2.0	-0.2055

Table 7.17 Data Collected for $PSRR_n$ Measurement.

All voltages are in Volt and V_{ic} = 0 V						
$R_5(i)$	$V_{psn}(a)$	$V_o(a)$	$V_{psn}(b)$	$V_o(b)$	ΔV_{psn}	$\Delta V_o[R_5(i)]$
$R_5(1) = \infty$	-0.5	-1.7129	-1.0	-1.3195	0.5	-0.3934
$R_5(2) = 220\ \Omega$	-0.5	-1.0843	-1.0	-0.85694	0.5	-0.2273

Equation (7.3) can be evaluated as 54.22 dB using the values provided in Table 7.16, and (7.4) can be evaluated as 60.79 dB using the values provided in Table 7.17.

7.3.2.1 CMRR and PSRR Measurement through a Universal Test Circuit

The circuit configuration of Fig. 7.6 was used to measure the open-loop input offset voltage, open-loop gain, CMRR, and PSRR of UTA246T. Data taken from the test circuit in Fig. 7.6 with UTA246T as the DUT are given in Tables 7.18 through 7.19.

Table 7.18 Data Collected for the Open-Loop Offset Voltage and Open-Loop Gain.

V_{o2} vs V_{id} for $V_{ic} = \Delta V_{psp} = \Delta V_{psn} = 0$	
V_{id} (V)	V_{o2} (V)
-1.0	+2.274
0.0	+2.312
+1.0	+2.342

Equation (7.5) gives -4.91 mV using the data provided in Table 7.18.

Table 7.19 Data Collected for CMRR Measurement.

V_{o2} versus V_{ic} $V_{id} = \Delta V_{psp} = \Delta V_{psn} = 0$	
V_{ic} (V)	V_{o2} (V)
-1.0	+1.175
0.0	+1.787
+1.0	+2.401

The equation (7.5) gives 61.71 dB using the data provided in Table 7.19.

Table 7.20 Data Collected for PSRR Measurement.

For $PSRR_p$		
V_{o2} vs V_{psp} for $V_{id} = V_{ic} = \Delta V_{psn} = 0$		
V_{psp} (V)	ΔV_{psp} (V)	V_{o2} (V)
+5.0	0.0	1.795
+5.5	0.5	1.982
+6.0	1.0	2.174

For $PSRR_n$		
V_{o2} vs V_{psn} for $V_{id} = V_{ic} = \Delta V_{psp} = 0$		
V_{psn} (V)	ΔV_{psn} (V)	V_{o2} (V)
-5.0	0.0	1.798
-5.5	0.5	1.779
-6.0	1.0	1.755

The equations (7.8) for $PSRR_p$ and (7.9) for $PSRR_n$ give 61.77 dB and 79.83 dB, respectively with the data provided in Table 7.20.

A summary of measured parameters for UTA246T is provided in Table 7.21.

Table 7.21 Comparison of Measured Data from the Test Circuits of Figs. 7.5 and 7.6.

Parameters	With Fig. 7.5	With Fig. 7.6
V_{os}(Open-loop)	N/A	-4.91 mV
CMRR	71.67 dB	61.71 dB
$PSRR_p$	54.22 dB	61.77 dB
$PSRR_n$	60.79 dB	79.83 dB

Because of the same reasoning for UTA246S discussed in section 7.2.2.1, the circuit of Fig. 7.5 is preferred over the circuit of Fig. 7.6 for the measurement of CMRR and PSRR for UTA246T as well.

7.3.3 Transient Sine Response Measurement

An inverting gain amplifier shown in Fig. 7.4(a) was wired with a UTA246T on a breadboard with 5% carbon film resistors. A sine wave response of the inverting amplifier with a gain of -2 was measured as shown in Fig. 7.19.

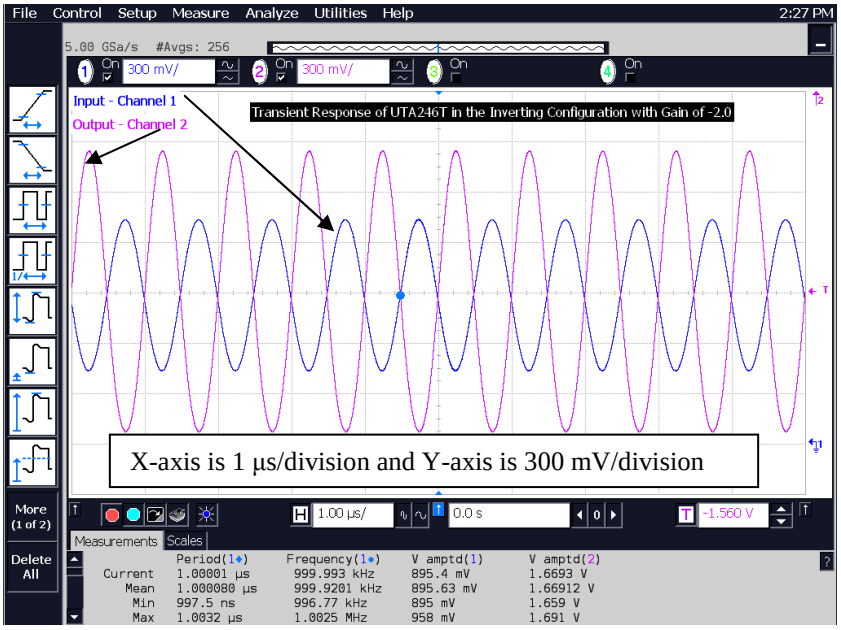


Figure 7.19 Transient 1 MHz sine response of UTA246T in the inverting gain configuration of Fig. 7.4(a) with a gain of -2.

The gain of the amplifier can be found by taking the ratio of the input and output sine wave amplitudes, and is -1.85. During the course of measurement, it was found that the amplification deteriorates beyond 10 MHz. The breadboard parasitic capacitances and inductances play a crucial role in this deteriorating response beyond 10 MHz.

7.3.4 Frequency-Domain Measurement

7.3.4.1 Frequency Response of the Non-Inverting Unity Gain Configuration

The test circuit shown in Fig. 7.2(a) was built on a protoboard. A sine wave transient response was obtained for the frequency range of 100 Hz through 50 MHz on DSO81204B, and corresponding magnitude and phase were measured using DSO's utilities feature. Such a response is shown in Fig. 7.20.

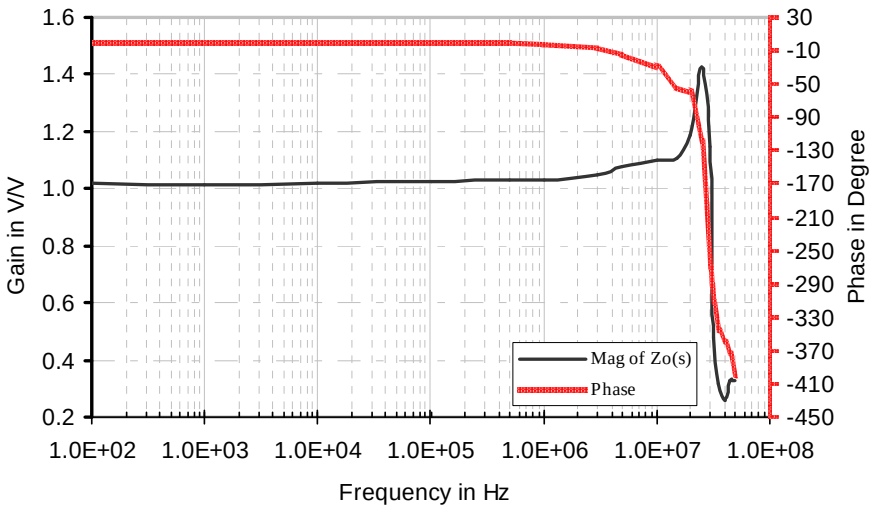


Figure 7.20 Frequency response of UTA246S in the non-inverting unity gain configuration with feedback resistor, R_f = 4.7 kΩ.

As illustrated in Fig. 7.20, UTA246T in the non-inverting unity gain configuration shows about 40% peaking in frequency response. It was found experimentally that the peaking does not go away even with a higher value of feedback resistor, such as 10 kΩ.

The reason could be the third-order open-loop transimpedance function of the UTA246T because of an extra pole due to the folding node X of Fig. 6.4.

7.3.4.1 Measurement of Open-Loop Transimpedance

The measurement of the open-loop transimpedance characteristics of the UTA246T chip was done using the same technique described in section 7.2.4.2 for the UTA246S. Both the measured and simulated responses of the circuit are shown in Fig. 7.21. The input-offset voltages needed in measurement and in simulation were -1.307 V and -2.404 V, respectively.

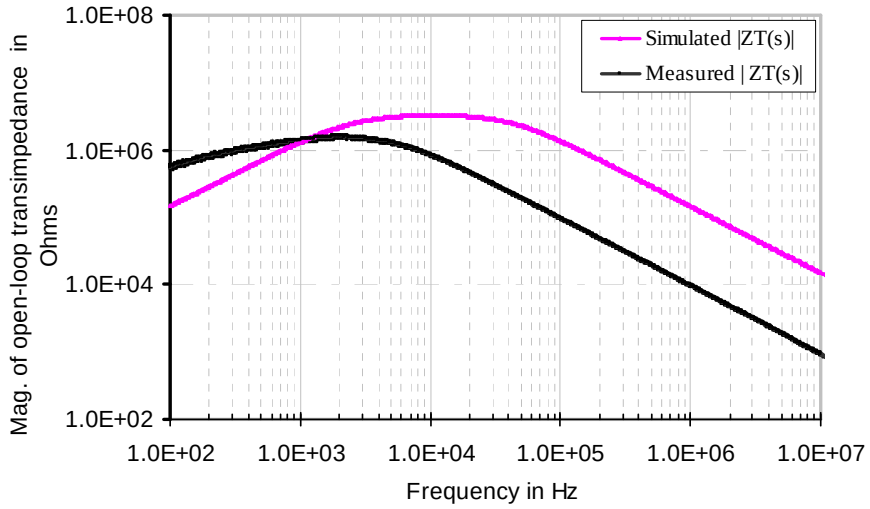
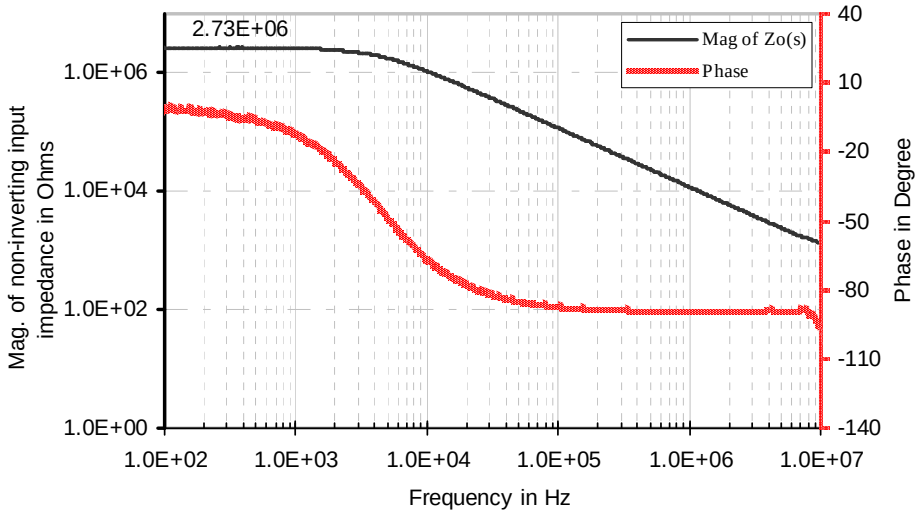


Figure 7.21 Frequency response of the open-loop transimpedance of UTA246T using the test circuit shown in Fig. 7.9.

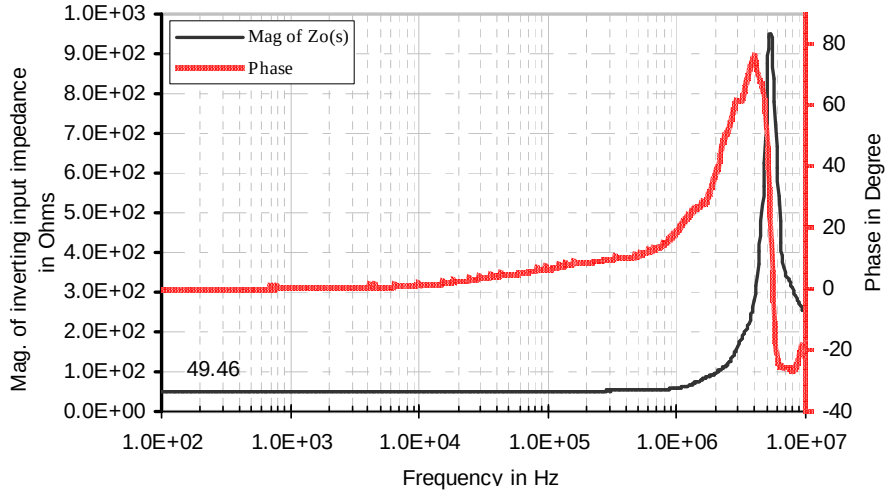
As shown in Fig. 7.21, the transimpedance response is influenced by the R_fC network of test circuit in Fig. 7.9 below 1 kHz and, true transimpedance response is obtained only after 1 kHz. It is also seen that there is a difference between simulation and measurement. Some portion of the difference can be attributed to the missing parasitic capacitances of the layout from the simulation.

7.3.4.2 Measurement of Non-inverting and Inverting Input Terminal Impedance

Following the same approach discussed in section 7.2.4.3 for UTA246S, the frequency responses for the input impedance of both non-inverting and inverting input terminal of the UTA246T were measured by probing the V_p and V_n terminal of Fig. 7.2(a) with UTA246T. Such responses are shown in Fig. 7.22.



(a)



(b)

Figure 7.22 Frequency response of the input impedance of (a) non-inverting terminal. (b) inverting terminal of UTA246T.

7.3.4.3 Measurement of Output Impedance

Like the UTA246S, the non-inverting unity gain configuration of Fig. 7.2(a) was used to measure the frequency response of the output impedance of the UTA246T chip in the closed-loop configuration. Such a response is shown in Fig. 7.23.

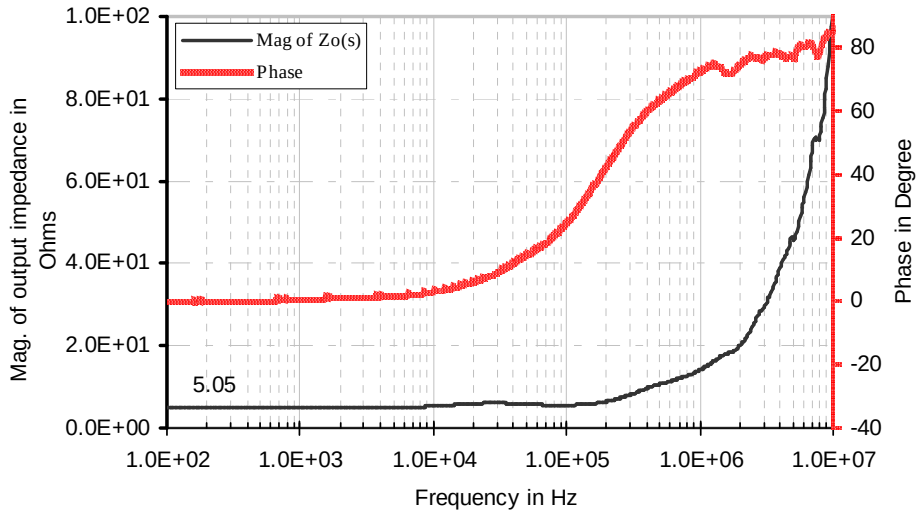


Figure 7.23 Frequency response of the output impedance of UTA246T in the non-inverting unity gain configuration with R_f = 4.7 kΩ and no load.

To extract open-loop output impedance, the simulations were done using a closed-loop and an open-loop configuration. The simulation data is provided in Table 7.22.

Table 7.22 Simulation Data for the Output Resistance of UTA246T.

Parameters	In open-loop (R_{oopl})	In closed-loop with R_f = 4.7 kΩ (R_{ocl})	In closed-loop with R_f = 10 kΩ (R_{ocl})
Output Impedance	691.6 Ω	0.98 Ω	2.10 Ω
Return Difference	N/A	705.70	329.33
Theoretical Return Difference, $1+Z_T(0)/R_f$	N/A	692.48	326.40

As illustrated in Table 7.22, the reduction in output resistance from open-loop to closed-loop configuration follows the expression (7.10). Assuming the return ratio is 705.7, the

measured output resistance in the open-loop configuration can be approximated as 5.05 times 705.7. This is equal to 3.56 kΩ, which is much higher than expectation.

7.3.5 Large-Signal Step Response Measurement

7.3.5.1 Slew Rate Measurement

The circuit of Fig. 7.2(a) with UTA246T and R_f = 4.7 kΩ was built on a protoboard. The non-inverting terminal was excited with a -0.5 V to 0.5 V input square wave with a rise and fall times of about 6.3 ns and pulse width of 1 μs with 50% duty cycle. This was generated by a Fluke 397 waveform generator. The step response was obtained using a digital oscilloscope (Agilent DSO81204B), and is shown in Fig. 7.24.

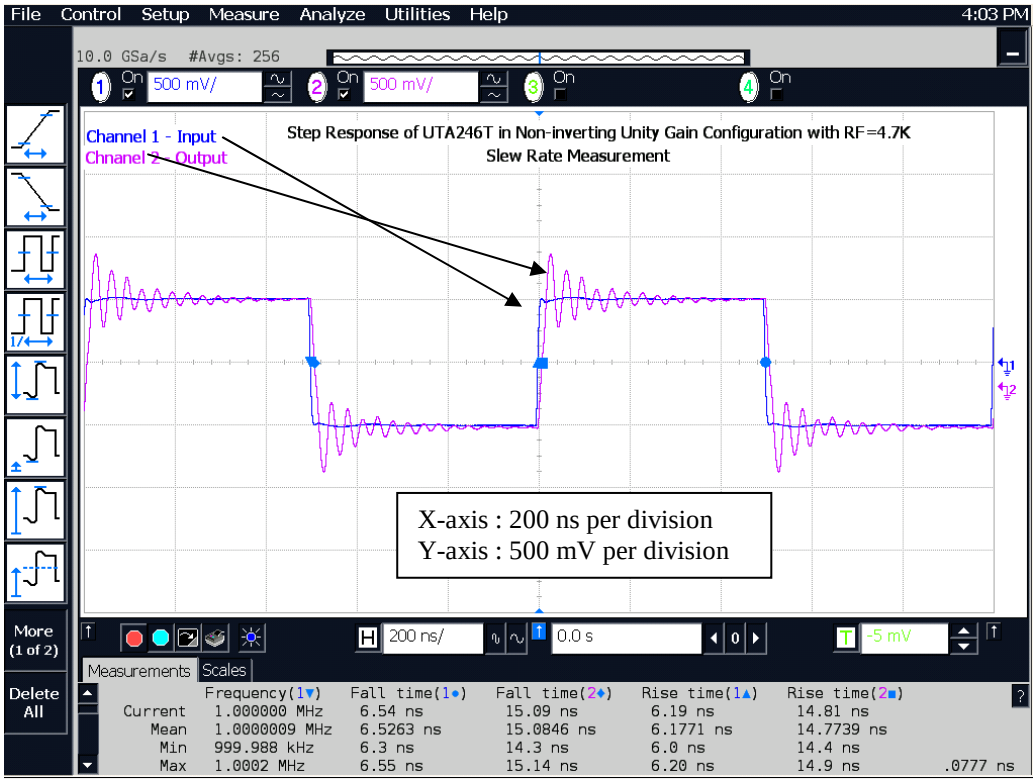


Figure 7.24 Large-signal step response of UTA246T in the non-inverting unity gain configuration, with R_L = 25 kΩ and C_L = 0.35 pF (DSO acts as a load).

As shown in Fig. 7.24, there is clearly oscillation with settling time of ~400ns. The oscillations can be minimized by increasing the value of feedback resistor, R_f, at the cost of increasing the input offset voltage. The effect of a large amplitude square wave on the slew rate was studied, and measurement data is summarized in Table 7.23.

Table 7.23 Slew Rate of UTA246T in the Non-Inverting Unity Gain Configuration with a Feedback Resistor of 4.7 kΩ

Parameters	With input pulse of Vp-p = 1 V		With input pulse of Vp-p = 2 V		With input pulse of Vp-p = 4 V	
	Simulation	Measurement	Simulation	Measurement	Simulation	Measurement
Slew Rate, SRp	62.5 V/µs	54.14 V/µs	139.42V/µs	74.76 V/µs	267.28 V/µs	226.95 V/µs
Slew Rate, SRn	61.5 V/µs	53.03 V/µs	132.13V/µs	76.41 V/µs	231.53 V/µs	123.17 V/µs

7.3.5.2 Thermal Tail Measurement

A measured large-signal transient step response for the UTA246T in the non-inverting unity gain configuration, excited with an input square wave of -0.5 V to 0.5 V, a rise and fall times of 0.78 µs, and pulse width of 100 µs, is shown in 7.25.

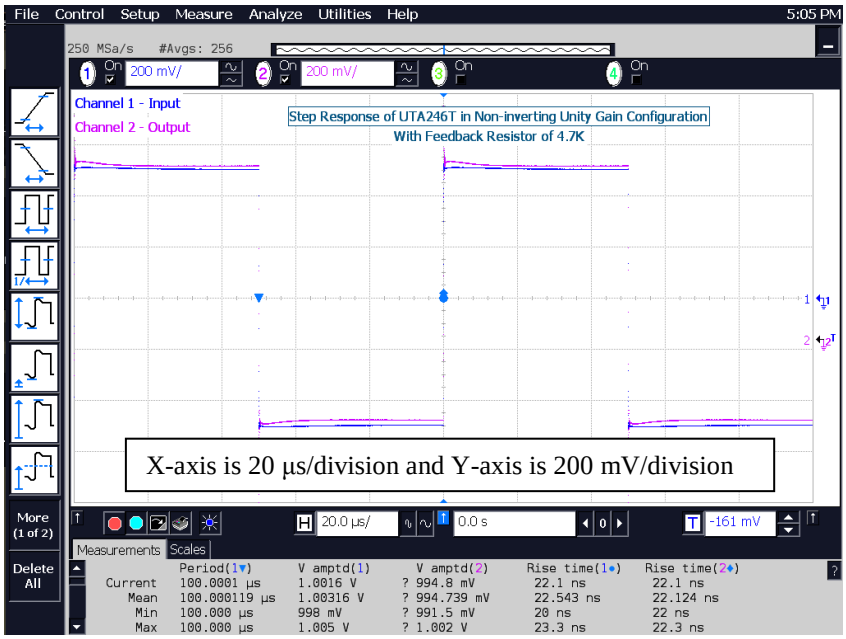
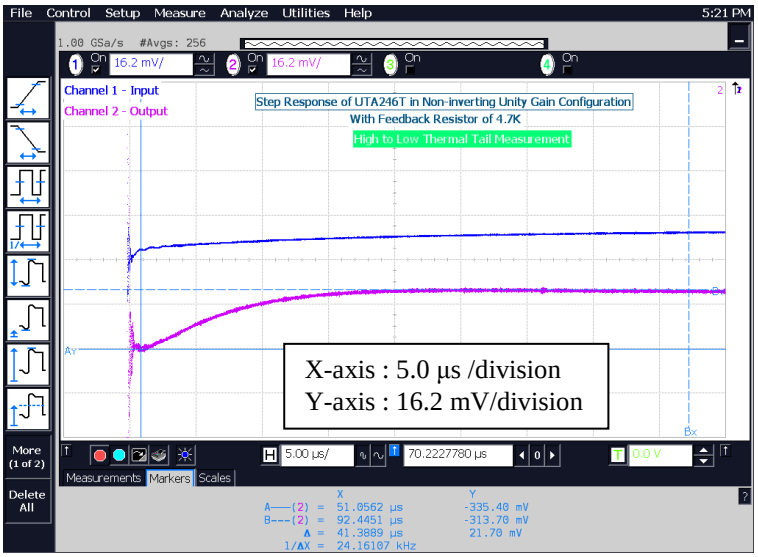


Figure 7.25 Large-signal step response of UTA246T in the non-inverting unity gain configuration of Fig. 7.2(a) with R_f = 4.7 kΩ, showing thermal tail.

The positive thermal tail shown in Fig. 7.26(a) and negative thermal tail shown in Fig. 7.26(b) are 17.20 mV, and 21.7 mV, respectively. A 95% drop in the magnitude of thermal tails happens in about 20 µs as illustrated in Fig. 7.26.

(a)



(b)

Figure 7.26 Expanded version of Fig. 7.25 to measure the positive and negative thermal tail.

7.3.5.3 Estimation of Thermal Time Constant from a Step Response

The thermal time constant of the step response of the UTA246T, shown in Fig 7.25, can be found using the technique described in the section 7.2.5.3. Fig. 7.27 shows a plot of relative gain error versus time for $0 \leq t \geq 20$ μs.

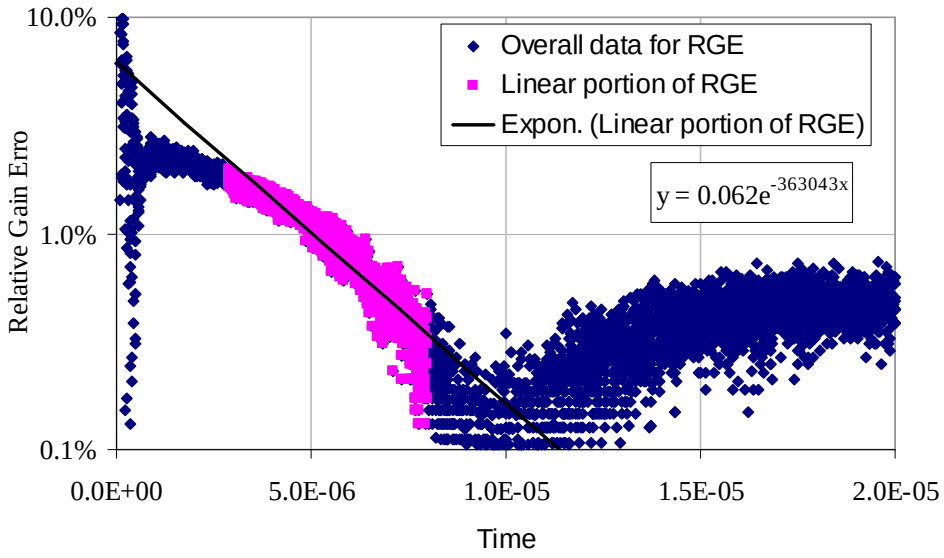


Figure 7.27 Thermal time constant extraction from the step response of Fig 7.25.

Using an exponential fit to the part that lies on the theoretical straight line (in this case, 3 μs $\leq$ t $\geq$ 8 μs), the magnitude of the thermal tail in terms of gain error for UTA246T can be found as 6.2% with a thermal time constant, τ_{th}, of 2.75 μs.

7.4 Simulation and Measurement Correlation

Table 7.23 summarizes both the simulation and the measurement of the parameters of the CFOAs – UTA246S and UTA246T. All simulations reported in this chapter are based on pure circuit simulation without including layout parasitic capacitances. As a consequence, the values for the simulated parameters, especially

those parameters which strongly depend on the parasitic capacitances such as open-loop transimpedance, and slew rate, are much higher than the measurement, and hence some difference is expected. In general, the correlation between simulation and measurement is fairly close for both UTA246S and UTA246T. This is summarized in Table 7.24.

Table 7.24 Correlation between the Simulation and Measurement of Parameters of CFOAs, UTA246S and UTA246T.

Parameters	UTA246S		UTA246T		Unit
	Simulations	Measurement	Simulations	Measurement	
Mag. of open-loop $Z_T(0)$)	2.98	1.06	3.25	1.67	MV/A
CMIR	5.80	5.10	6.20	6.00	V
Output swing	5.60	5.20	6.00	5.80	V
CMRR(0)	89.99	88.80	62.14	71.67	dB
$PSRR_p(0)$	86.94	74.77	74.21	54.22	dB
$PSRR_n(0)$	93.53	70.44	74.75	60.79	dB
SR_p with with Vpp = 1V Rf =1 kΩ/4.7kΩ for (UTA246S)/UTA246T)	368.00	36.89	62.50	54.14	V/μs
SR_n with Rf = 1 kΩ & Vpp = 1V Rf =1 kΩ/4.7kΩ for (UTA246S)/UTA246T)	357.00	36.65	332.00	53.03	V/μs
Non-inverting input impedance $Z_{in}(0)$	2.13	2.06	2.65	2.73	MΩ
Inverting input impedance $Z_{in}(0)$	49.94	35.25	47.70	49.46	Ω
Closed-loop output impedance, $Z_{out}(0)$	0.22	8.84	0.98	5.05	mΩ
Positive/Negative thermal tail	0.015/0.017	16.5/20	0.019/0.020	17.2/21.7	mV

It is experimentally verified that a better CMIR can be achieved with UTA246T over UTA246S, substantiating the design expectations discussed in chapter 6. It is also experimentally verified that the CMRR response of UTA246S is better than that of UTA246T. This is because a cascode structure used in UTA26S at the input stage suppresses the effect of a common-mode signal better than a folded cascode structure used in UTA246T at the input stage. There is a very good correlation between simulated and measured response of inverting input, non-inverting input and output impedances of the CFOAs. However, there is a large difference between simulated and measured slew

rate for the both CFOAs. The most obvious reasons are the missing layout parasitic capacitance at high-gain node, Z, of the CFOAs in the simulation, while extra parasitic capacitances of pad being added into measurement. There is also a large miscorrelation between measured and simulated thermal tail. One of the reasons could be smaller devices being used in the input stages of the both CFOAs.

Table 7.25 summarizes the simulation of the parameters of the CFOAs – UTA246S and UTA246T using the VIP10™ VBIC models and physics based VBIC models provided in chapter 2. Based on the data provided in Table 7.25, there is a difference of about ±10% between each of the parameters, except for I_{offset} and V_{os}.

Table 7.25 Comparison of Simulated Parameters of UTA246S and UTA246T between the VIP10™ VBIC Models and Physics Based VBIC Models.

Parameters	UTA246S		UTA246T		Unit
	VIP10™	Proposed Model	VIP10™	Proposed Model	
Offset dc current at inverting input (I_{off})	-3.62	-9.77	-27.83	-61.70	μA
Input offset voltage in open-loop (V_{os})	50.51	240.00	-43.40	1800.00	μV
Mag. of open-loop $Z_T(0)$)	2.98	2.48	3.25	2.62	MV/A
$R_{critical}$	725.00	83.23	830.00	91.00	Ω
CMIR	5.80	5.60	6.20	6.40	V
Output swing	5.60	5.20	6.00	6.40	V
CMRR(0)	89.99	90.61	62.14	65.67	dB
$PSRR_p(0)$	86.94	80.10	74.21	65.53	dB
$PSRR_n(0)$	93.53	82.58	74.75	65.78	dB
SR_p with R_f = 1 kΩ & Vpp = 1V	368.00	450.00	326.00	240.00	V/μs
SR_n with Rf = 1 kΩ & Vpp = 1V	357.00	490.00	332.00	200.00	V/μs
Non-inverting input $Z_{in}(0)$	2.13	2.62	2.65	3.27	MΩ
Inverting input $Z_{in}(0)$	49.94	58.45	47.70	59.40	Ω
Open-loop Output impedance, $Z_{out}(0)$	633.80	787.37	691.60	846.98	Ω

Thus, it verified that the models proposed in chapter 2 can be reasonably used for the prediction of design functionality using SOI bipolar transistors.

7.5 Summary

The functionality of test chips, UTA246S and UTA246T, were verified experimentally, and various parameters of the COFAs, UTA246S and UTA246T, were measured. Several test circuits were built on a protoboard and/or a breadboard, and measurements were done using state-of-the-art equipment – Agilent Infiniium DSO81204B digital oscilloscope, Active Probe (Agilent 1169A), precision impedance analyzer (Agilent 4294A), along with impedance probe (Agilent 42941A) – for the time-domain and frequency-domain characterization of thermal effects of self-heating on CFOA circuits. The verification of elimination of self-heating induced peaking in the frequency response of the open-loop transimpedance for both COFAs was illustrated experimentally. A correlation between simulation (using the VIP10^{TM} VBIC models) and measurement is presented.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

The thermal effect of self-heating in the modern SOI BJT on the performance of analog integrated circuit has been studied extensively. Analytical formulations to characterize the frequency-domain thermal effect of self-heating on the performance of current mirrors and high-speed current-feedback operational amplifiers (CFOAs) are presented. It is verified that the thermal effect is always limited to a range of frequency below the thermal cutoff frequency, which is a technology dependent parameter. Thermally induced non-ideal effects in the frequency response of current mirrors and CFOAs are identified, and various circuit topologies are suggested and proposed to suppress such thermal effects. Extensive dc, time-domain and frequency-domain measurements were carried out to validate all analytical formulations developed for current mirrors and CFOAs.

Physics based SGP and VBIC models, incorporating the non-ideal physical effects prevalent in the dialectically isolated bipolar process technology, have been developed through extensive literature review and process architectural assumptions. The robustness of the proposed VBIC models was verified through extensive simulations using the SPECTRE simulator. In addition, the developed VBIC models were extensively used in the frequency-domain analysis and characterization of the

thermal effect of self-heating on the various current mirrors and CFOAs, designed in this research work. The validity of these models in predicting the behavior of an analog circuit was substantiated further by having a good correlation between measurement and simulation using these VBIC models. However, these models do not represent any propriety devices characteristics whatsoever. They are an alternative to proprietary SOI bipolar transistor models for the prediction of design functionality and behavior in the early stage of a design cycle.

The method developed by Sham et al. [13] to derive the small-signal change in temperature, caused by dynamic self-heating, in terms of terminal voltages and currents of a circuit under consideration has been reviewed. The method was improved through extensive analytical formulations, extending a similar approach previously discussed by Tenbroek and Lee [19] for the MOSFET devices. Details are provided in chapter 3. The thermal effect of self-heating in the fundamental blocks of analog integrated circuit has been analyzed, and several self-heating mitigation techniques are presented in chapter 3 as well.

An extensive study of the frequency-domain thermal effects of self-heating on current mirrors has been presented through both simulation and measurement in chapter 4. Various closed-form analytical formulations for the output impedance and admittance of the most widely used current mirrors were developed and substantiated through the frequency-domain measurement on current mirrors, fabricated using the VIP10^{TM} bipolar process technology developed by National Semiconductor Corporation, using the state-of-art precision impedance analyzer (Agilent 4294A), along with an

impedance probe (Agilent 42941A). The peaking effects due to the dynamic self-heating in the frequency response of the output impedance of current mirrors were illustrated through the frequency-domain measurement. Such measurements are reported for the first time in chapter 4. Analytical formulations, simulation, and measurement show that cascode and Wilson current mirrors are the best choice for the design of self-heating tolerant circuits at the cost of voltage headroom. It is also verified that optimization technique for the design of self-heating tolerant circuits is hinged upon the use of a cascode structure or cascode current mirror opportunistically. In the design where high voltage headroom due to the vertical stacking of a cascode device can't be tolerated, a folded cascode structure can be used. However, the thermal effect suppression with the folded cascode structure is not as good as with a cascode structure.

Two of the optimized current-feedback operational amplifiers, CFOA I (UTA246S) and CFOA II (UTA246T), were designed and fabricated with the VIP10^{TM} bipolar process technology. The measurement data presented in chapter 7 strongly supports the theory that the thermal effect of self-heating of an SOI BJT can be reduced through the utilization of cascoding at the input stage and Wilson current mirrors at the transimpedance stage of the CFOAs.

8.1 Recommendation for Future Work

As presented in this research work, the power dissipation and temperature rise in an SOI BJT are related through a temperature independent thermal resistance. But the latest advancement in the bipolar process technology and the thrust of decreasing the feature size of devices has pushed the thermal effect of self-heating into the edge, where

the temperature dependence of thermal resistance can't be ignored. It is well-known that the thermal conductivity changes with temperature [2]. Marsh [69] has proved that thermal impedance increases with temperature, based on device simulations. In addition, Bovolon [70] shows that thermal resistance increases with power dissipation which causes the elevation of device operating temperature due to self-heating. The dependence of thermal resistance on temperature has been addressed by Paasschens [71], and it is proved that there is a non-linear relationship between device temperature and power dissipation. This makes the extraction of thermal resistance to be a much more complex task. In addition, the analysis of the thermal effect of self-heating on analog circuits will be an equally challenging task. A new SiGe HBT process technology may also show temperature dependence of thermal resistance. It is worthwhile to understand the thermal effect of self-heating on current mirror and high-speed amplifiers designed with National Semiconductor's "CBC8" SiGe HBT process. This would be a very good topic to pursue as an extension of this research work.

The thermal effect of self-heating has not been studied for the classical VFOA architecture yet. It is worthwhile to study the effect of self-heating on the performance of a VFOA. The analysis of the thermal effect of self-heating on the performance of non-linear circuits, such as an analog multiplier, can be undertaken as future work. The study of the thermal effect of self-heating on the distortion characteristics of both the CFOA and VFOA would be another topic of utmost interest.

APPENDIX A

SGP MODEL PARAMETERS AND KEY DEVICE PHYSICS EQUATIONS

The SGP model parameters are provided in Table A.1.

Table A.1 The SGP Model Parameter and their brief description [33]

STANDARD GUMMEL-POON MODEL PARAMETERS			
PARAMETERS	**PARAMETERS DESCRIPTION**	**TYPICAL VALUES**	**UNIT**
IS	Transport Saturation Current	1.00E-15	A
XTI	Temperature Exponent IS	3.00	
EG	Energy Gap	1.11	eV
BF	Ideal Forward Maximum Beta	150.00	
BR	Ideal Reverse Maximum Beta	0.50	
XTB	Forward and Reverse Beta Temp. Coef.	2.50	
VAF	Forward Early Voltage	100.00	V
VAR	Rreverse Early Voltage	5.00	V
NF	Forward Emission Coefficient	1.00	
NR	Reverse Emission Coefficient	1.00	
NE	B-E Leakage Emission Coefficient	1.70	
NC	B-C Leakage Emission Coefficient	1.30	
ISE	B-E Space Charge Recomb. Saturation Current	1.00E-13	A
ISC	B-C Space Charge Recomb. Saturation Current	1.00E-13	A
IKF	Forward High Level Injection Current	5.00E-02	A
IKR	Reverse High Level Injection Current	3.00E-01	A
RB	Zero Bias Base Resistance	100.00	Ohm
IRB	Current at Medium Base Resistance	1.00E-04	A
RBM	Minium Base Res. atHigh Current	25.00	Ohm
RE	Emitter Series Resistance	5.00	Ohm
RC	Collector Series Resistance	10.00	Ohm
CJE	B-E Zero Bias Depletion Capacitance	1.00E-12	F
VJE	B-E Built-in Potential	0.60	V
MJE	B-E Junction Grading Coefficient	3.30E-01	
CJC	B-C Zero Bias Depletion Capacitance	5.00E-13	F
VJC	B-C Built-in Potential	0.60	V
MJC	B-C Junction Grading Coefficient	4.00E-01	
XCJC	Fraction of CJC Connected to Int. Base	1.00	
CJS	Collector-Substrate Zero Bias Depl. Cap.	0.00	F
VJS	Substrate Junction Built-in Potential	0.00	V
MJS	Substrate Junction Grading Coefficient	0.00	
FC	Forward Capacitance Switching Coef.	0.50	
TF	Ideal forward Base Transit Time	1.00E-12	sec
XTF	Coefficient of TF with Bias dependence	10.00	
VTF	Coefficient of TF dependence on Vbc	5.00	V
ITF	Coefficient of TF dependence on IC	0.02	A
PTF	Excess Phase at frequency 1/(2pi*TF)	0.00	deg
TR	Ideal Reverse Transit Time	5.00E-11	sec
KF	Base-Emitter Flicker Noise Constant	0.00	
AF	Flicker Noise Exponent for Current	1.00E-05	
TEMP	Temperature	25.00	C

The key device physics equations, extensively used in chapter 2, are summarized here for convenience.

The mobility of holes [cm^2/V-sec] is given by [2]

$$\mu_p = \frac{425.6}{1+(1+N_{imp}/2.23\cdot 10^{17})^{0.719}} + 44.9 \qquad \text{(A.1)}$$

where N_{imp} is the impurity concentration in silicon. The mobility of electrons [cm^2/V-sec] is given by [2]

$$\mu_p = \frac{1346}{1+(1+N_{imp}/9.2\cdot 10^{16})^{0.711}} + 68.5 \qquad \text{(A.2)}$$

The minority carrier lifetime [sec] in silicon for either electrons or holes is given by [2]

$$\tau_{\min} = \frac{45\cdot 10^{-06}}{1+(1+7.7\cdot 10^{-18}\cdot N_{imp} + 4.5\cdot 10^{-36}\cdot N_{imp}^2)} \qquad \text{(A.3)}$$

The diffusion coefficient [cm^2/ sec] of electros, D_n, and holes, D_p, is given by [2]

$$D_{p/n} = V_T \cdot \mu_{p/n} \qquad \text{(A.4)}$$

The Early voltage of the bipolar transistor can b expressed as [2]

$$|V_A| = \frac{Q_B}{C_{jc}} \qquad \text{(A.5)}$$

where Q_B is the base majority-charge density and C_{jc} is the depletion capacitance per unit area at the base-collector junction.

APPENDIX B

DERIVATION OF THE OUTPUT IMPEDANCE OF THE BIPOLAR TRANSISTOR WITH DYNAMIC SELF-HEATING

The small signal representation of the *npn* bipolar transistor including the effect of dynamic self-heating is shown in Fig. B.1.

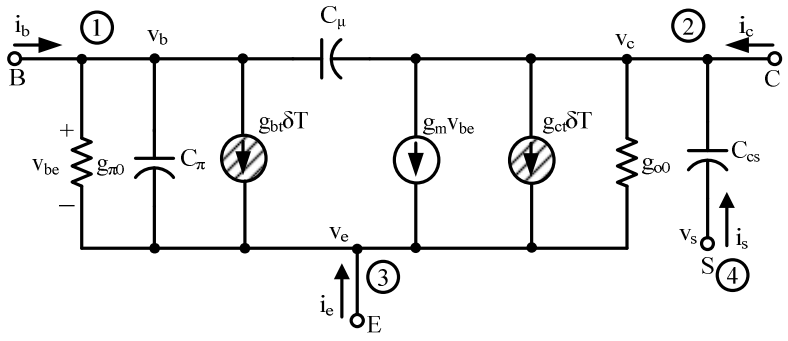


Figure B.1 Small-signal equivalent circuit for the *npn* transistor.

The terminal currents and voltages of Fig. B.1 are related by the equation

$$\begin{bmatrix} i_b \\ i_c \\ i_e \\ i_s \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} & y_{13} & y_{14} \\ y_{21} & y_{22} & y_{23} & y_{24} \\ y_{31} & y_{32} & y_{33} & y_{34} \\ y_{41} & y_{42} & y_{43} & y_{44} \end{bmatrix} \begin{bmatrix} v_b \\ v_c \\ v_e \\ v_s \end{bmatrix} + \begin{bmatrix} i_{bs} \\ i_{cs} \\ i_{es} \\ i_{ss} \end{bmatrix} \tag{B.1a}$$

or more compactly as

$$I(s) = Y(s)V(s) + I_{is} \tag{B.1b}$$

where y_{ij} is the small signal admittance parameter and i_{is} denotes the current flowing into the ith terminal when all terminals are grounded to the reference point. The coefficient matrix Y(s) of (B.1b) is called the indefinite-admittance matrix [43]. Following the rules for writing the primitive indefinite-admittance matrix [43], matrix (B.1a) can be expressed as

$$\begin{bmatrix} i_b \\ i_c \\ i_e \\ i_s \end{bmatrix} = \begin{bmatrix} y_\pi + sC_\mu & -sC_\mu & -y_\pi & 0 \\ g_m - sC_\mu & g_0 + s(C_\mu + C_{cs}) & -(g_m + g_0) & -sC_{cs} \\ -(g_m + y_\pi) & -g_0 & g_m + g_0 + y_\pi & 0 \\ 0 & -sC_{cs} & 0 & sC_{cs} \end{bmatrix} \begin{bmatrix} v_b \\ v_c \\ v_e \\ v_s \end{bmatrix} + \begin{bmatrix} g_{bt} \\ g_{ct} \\ -(g_{ct} + g_{bt}) \\ 0 \end{bmatrix} \cdot \delta T \tag{B.2}$$

The matrix (B.2) is a general matrix which can be used to characterize the small-signal operation in any of the configurations of the bipolar transistor, such as the common-base, common-collector and common-emitter (*CE*). As an example, the matrix (B.2) will be reduced to represent a transistor in the *CE* configuration, for which the terminals 3 and 4 needs to be contracted and then grounded. This can be done by adopting the following steps proposed by Chen [42] on the matrix (B.2).

1. Add row 4 to row 3 of (B.2), and leave row 4 as it is. This gives

$$\begin{bmatrix} \mathrm{i_b} \\ i_c \\ i_e \\ i_s \end{bmatrix} = \begin{bmatrix} \mathrm{y}_\pi + \mathrm{s}C_\mu & -\mathrm{s}C_\mu & -\mathrm{y}_\pi & 0 \\ \mathrm{g_m} - \mathrm{s}C_\mu & g_{o0} + \mathrm{s}(C_\mu + \mathrm{C_{cs}}) & -(g_m + g_{o0}) & -\mathrm{sC_{cs}} \\ -(\mathrm{g_m} + \mathrm{y}_\pi) & -(g_{o0} + \mathrm{sC_{cs}}) & g_m + g_{o0} + y_\pi & \mathrm{sC_{cs}} \\ 0 & -\mathrm{sC_{cs}} & 0 & \mathrm{sC_{cs}} \end{bmatrix} \begin{bmatrix} \mathrm{v_b} \\ v_c \\ v_e \\ v_s \end{bmatrix} + \begin{bmatrix} \mathrm{g_{bt}} \\ \mathrm{g_{ct}} \\ -(\mathrm{g_{ct}} + \mathrm{g_{bt}}) \\ 0 \end{bmatrix} \cdot \delta \mathrm{T} \quad \text{(B.3)}$$

where $\mathrm{y}_\pi = \mathrm{g}_{\pi 0} + \mathrm{C}_\pi$

2. Add column 4 into column 3 of (B.3), and leave column 4 as it is. This gives

$$\begin{bmatrix} \mathrm{i_b} \\ i_c \\ i_e \\ i_s \end{bmatrix} = \begin{bmatrix} \mathrm{y}_\pi + \mathrm{s}C_\mu & -\mathrm{s}C_\mu & -\mathrm{y}_\pi & 0 \\ \mathrm{g_m} - \mathrm{s}C_\mu & g_{o0} + \mathrm{s}(C_\mu + \mathrm{C_{cs}}) & -(g_m + g_{o0}) - \mathrm{sC_{cs}} & -\mathrm{sC_{cs}} \\ -(\mathrm{g_m} + \mathrm{y}_\pi) & -(g_{o0} + \mathrm{sC_{cs}}) & g_m + g_{o0} + y_\pi + \mathrm{sC_{cs}} & \mathrm{sC_{cs}} \\ 0 & -\mathrm{sC_{cs}} & \mathrm{sC_{cs}} & \mathrm{sC_{cs}} \end{bmatrix} \begin{bmatrix} \mathrm{v_b} \\ v_c \\ v_e \\ v_s \end{bmatrix} + \begin{bmatrix} \mathrm{g_{bt}} \\ \mathrm{g_{ct}} \\ -(\mathrm{g_{ct}} + \mathrm{g_{bt}}) \\ 0 \end{bmatrix} \cdot \delta \mathrm{T} \quad \text{(B.4)}$$

3. Remove row 4 and column 4 of (B.4) to get terminals 3 and 4 contracted. This gives

$$\begin{bmatrix} \mathrm{i_b} \\ i_c \\ i_e \end{bmatrix} = \begin{bmatrix} \mathrm{y}_\pi + \mathrm{s}C_\mu & -\mathrm{s}C_\mu & -\mathrm{y}_\pi \\ \mathrm{g_m} - \mathrm{s}C_\mu & g_{o0} + \mathrm{s}(C_\mu + \mathrm{C_{cs}}) & -(g_m + g_{o0}) - \mathrm{sC_{cs}} \\ -(\mathrm{g_m} + \mathrm{y}_\pi) & -(g_{o0} + \mathrm{sC_{cs}}) & g_m + g_{o0} + y_\pi + \mathrm{sC_{cs}} \end{bmatrix} \begin{bmatrix} \mathrm{v_b} \\ v_c \\ v_e \end{bmatrix} + \begin{bmatrix} \mathrm{g_{bt}} \\ \mathrm{g_{ct}} \\ -(\mathrm{g_{ct}} + \mathrm{g_{bt}}) \end{bmatrix} \cdot \delta \mathrm{T} \quad \text{(B.5)}$$

To ground the contracted terminals 3 and 4, row 3 and column 3 of (B.5) are removed. This gives

$$\begin{bmatrix} \mathrm{i_b} \\ i_c \end{bmatrix} = \begin{bmatrix} \mathrm{y}_\pi + \mathrm{s}C_\mu & -\mathrm{s}C_\mu \\ \mathrm{g_m} - \mathrm{s}C_\mu & g_{o0} + \mathrm{s}(C_\mu + \mathrm{C_{cs}}) \end{bmatrix} \begin{bmatrix} \mathrm{v_b} \\ v_c \end{bmatrix} + \begin{bmatrix} \mathrm{g_{bt}} \\ \mathrm{g_{ct}} \end{bmatrix} \cdot \delta \mathrm{T} \quad \text{(B.6)}$$

From (3.121), the small-signal change in temperature, δT, can be expressed as

$$[\delta T] = \begin{bmatrix} \dfrac{(I_b + g_{\pi T}V_b + g_{mT}V_c)}{Y_{th} - (g_{ct}V_c + g_{bt}V_b)} & \dfrac{(I_c + g_{oT}V_c)}{Y_{th} - (g_{ct}V_c + g_{bt}V_b)} \end{bmatrix} \begin{bmatrix} v_b \\ v_c \end{bmatrix} \tag{B.7}$$

The substitution of (B.7) into (B.6) and some algebraic manipulation gives

$$\begin{bmatrix} i_b \\ i_c \end{bmatrix} = \begin{bmatrix} \mathrm{y}_\pi + \mathrm{s}C_\mu & -\mathrm{s}C_\mu \\ \mathrm{g}_\mathrm{m} - \mathrm{s}C_\mu & \mathrm{g}_{o0} + \mathrm{s}(C_\mu + \mathrm{C}_{cs}) \end{bmatrix} \begin{bmatrix} \mathrm{v}_\mathrm{b} \\ v_c \end{bmatrix} + \begin{bmatrix} \dfrac{\mathrm{g}_{\mathrm{bt}} \cdot (I_b + g_{\pi T}V_b + g_{mT}V_c)}{Y_{th} - (g_{ct}V_c + g_{bt}V_b)} & \dfrac{\mathrm{g}_{\mathrm{bt}} \cdot (I_c + g_{oT}V_c)}{Y_{th} - (g_{ct}V_c + g_{bt}V_b)} \\ \dfrac{\mathrm{g}_{\mathrm{ct}} \cdot (I_b + g_{\pi T}V_b + g_{mT}V_c)}{Y_{th} - (g_{ct}V_c + g_{bt}V_b)} & \dfrac{\mathrm{g}_{\mathrm{ct}} \cdot (I_c + g_{oT}V_c)}{Y_{th} - (g_{ct}V_c + g_{bt}V_b)} \end{bmatrix} \begin{bmatrix} v_b \\ v_c \end{bmatrix} \tag{B.8}$$

From (B.8), the output admittance, $Y_{22}(s)$, of the bipolar transistor in the *CE* configuration can expressed as

$$Y_{22}(s) = \left.\frac{i_c}{v_c}\right|_{V_b = 0} = \left[g_{o0} + s(C_\mu + C_{cs})\right] + \left[\frac{g_{ct} \cdot (I_c + g_{oT}V_c) \cdot Z_{th}}{1 - (g_{ct}V_c + g_{bt}V_b) \cdot Z_{th}}\right] \tag{B.9}$$

The reciprocal of (B.9) gives the output resistance as

$$Z_o(s) = \left.\frac{v_c}{i_c}\right|_{V_b = 0} = \frac{1}{\left.\dfrac{i_c}{v_c}\right|_{V_b = 0}} = \frac{1}{Y_{22}(s)} = \frac{1}{g_{o0} + s(C_\mu + C_{cs}) + \dfrac{g_{ct} \cdot (I_c + g_{oT}V_c) \cdot Z_{th}}{1 - (g_{ct}V_c + g_{bt}V_b) \cdot Z_{th}}} \tag{B.10}$$

where it is assumed that

$$\left.\frac{v_c}{i_c}\right|_{V_b = 0} = \frac{1}{\left.\dfrac{i_c}{v_c}\right|_{V_b = 0}} \text{ is defined.}$$

Assuming $\mathrm{M} = (\mathrm{g}_{\mathrm{ct}}\mathrm{V}_\mathrm{c} + \mathrm{g}_{\mathrm{bt}}\mathrm{V}_\mathrm{b})$, $\mathrm{X}_\mathrm{g} = \mathrm{g}_{\mathrm{ct}}(\mathrm{I}_\mathrm{c} + \mathrm{g}_{0\mathrm{T}}\mathrm{V}_\mathrm{c})$, and $C_{eq} = C_{cs} + C_\mu$, (B.10) can be expressed as

$$Z_o(s) = \frac{1}{g_{o0} + sC_{eq} + \dfrac{X_g Z_{th}}{1 - MZ_{th}}}$$

$$= \frac{1}{g_{o0} + sC_{eq} + \dfrac{X_g R_{th}}{1 + sR_{th}C_{th} - MR_{th}}}$$

$$= \frac{1 + sR_{th}C_{th} - MR_{th}}{(g_{o0} + sC_{eq})\left(1 + sR_{th}C_{th} - MR_{th}\right) + X_g R_{th}}$$

$$= \frac{1 - MR_{th} + sR_{th}C_{th}}{(g_{o0} + sC_{eq})(1 - MR_{th} + sR_{th}C_{th}) + X_g R_{th}}$$

$$= \frac{1 - MR_{th} + sR_{th}C_{th}}{g_{o0}(1 - MR_{th} + sR_{th}C_{th}) + sC_{eq}(1 - MR_{th} + sR_{th}C_{th}) + X_g R_{th}}$$

$$= \frac{1 - MR_{th} + sR_{th}C_{th}}{s^2 R_{th}C_{th}C + s(R_{th}C_{th}g_{o0} + C_{eq}(1 - MR_{th})) + (g_{0o}(1 - MR_{th}) + X_g R_{th})} \qquad \text{B.11)}$$

After some algebraic simplification, equation (B.11) can be expressed as

$$Z_o(s) = \frac{\dfrac{\left(1 - MR_{th}\right)}{g_{o0}\left(1 - MR_{th}\right) + X_g R_{th}}\left(1 + \dfrac{s}{\left(1 - MR_{th}\right)/R_{th}C_{th}}\right)}{\dfrac{R_{th}C_{th}C_{eq}}{g_{o0}\left(1 - MR_{th}\right) + X_g R_{th}}s^2 + \dfrac{R_{th}C_{th}g_{o0} + C_{eq}(1 - MR_{th})}{g_{o0}(1 - MR_{th}) + X_g R_{th}}s + 1} \qquad \text{(B.12)}$$

Equation (B.12) gives a zero and two poles. The zero is given by

$$f_z = \left(1 - MR_{th}\right) \cdot f_{th} \qquad \text{(B.13)}$$

Assuming $g_{o0}\left(1 - MR_{th}\right) << XR_{th}$, and $R_{TH}C_{TH}g_0 >> C_{eq}\left(1 - MR_{th}\right)$, the poles can be expressed as

$$p_{1,2} = \frac{-\dfrac{R_{th}C_{th}g_{o0}}{X_g R_{th}} \pm \sqrt{\left(\dfrac{R_{th}C_{th}g_{o0}}{X_g R_{th}}\right)^2 - 4\dfrac{R_{th}C_{th}C_{eq}}{X_g R_{th}}}}{2 \cdot \dfrac{R_{th}C_{th}C_{eq}}{X_g R_{th}}} \qquad \text{(B.14)}$$

$$= \frac{-\frac{C_{th}g_{o0}}{X_g} \pm \sqrt{\left(\frac{C_{th}g_{o0}}{X_g}\right)^2 - 4\frac{C_{th}C_{eq}}{X_g}}}{2 \cdot \frac{C_{th}C_{eq}}{X_g}}$$

$$= \frac{-\frac{C_{th}g_{o0}}{X_g} \pm \frac{C_{th}}{X_g}\sqrt{g_{o0}^2 - 4\frac{XC_{eq}}{C_{th}}}}{2 \cdot \frac{C_{th}C_{eq}}{X_g}}$$

$$p_{1,2} = \frac{-g_{o0} \pm \sqrt{g_{o0}^2 - \frac{4X_gC_{eq}}{C_{th}}}}{2C_{eq}} \qquad \text{(B.15)}$$

The poles will be real only when

$$g_{o0}^2 > \frac{4X_gC_{eq}}{C_{th}} \qquad \text{(B.16)}$$

The zero frequency given by (B.13) may be close to the thermal cutoff frequency depending on the value of M, which is dictated by the bias voltages. The two pole frequencies given by (B.15) can be real only when $g_{o0}^2 > 4X_gC_{eq}/C_{th}$. This is generally true for an SOI bipolar transistor with a large value of thermal resistance (in the range of 3000 K/Watt). Assuming $g_{o0}^2 >> \frac{4X_gC_{eq}}{C_{th}}$, it can be inferred from (B.15) that the poles may be very close to the intrinsic pole of the device, g_{o0}/C_{eq}.

APPENDIX C

ADMITTANCE PARAMETERS FOR THE BIPOLAR TRANSISTOR WITH EMITTER DEGENERATION

The small-signal equivalent circuit of the *npn* bipolar transistor with emitter degeneration including the effect of dynamic self-heating is shown in Fig. C.1.

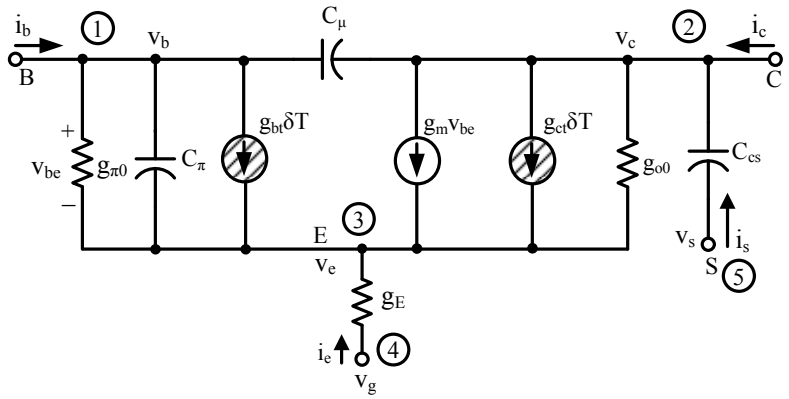


Figure C.1 Small-signal equivalent circuit for an *npn* transistor with emitter degeneration.

The terminal currents and voltages of Fig. C.1 are related by the equation

$$\begin{bmatrix} i_b \\ i_c \\ i_e \\ i_g \\ i_s \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} & y_{13} & y_{14} & y_{15} \\ y_{21} & y_{22} & y_{23} & y_{24} & y_{25} \\ y_{31} & y_{32} & y_{33} & y_{34} & y_{35} \\ y_{41} & y_{42} & y_{43} & y_{44} & y_{45} \\ y_{51} & y_{52} & y_{53} & y_{54} & y_{55} \end{bmatrix} \begin{bmatrix} v_b \\ v_c \\ v_e \\ v_g \\ v_s \end{bmatrix} + \begin{bmatrix} i_{bs} \\ i_{cs} \\ i_{es} \\ i_{gs} \\ i_{ss} \end{bmatrix} \tag{C.1a}$$

or more compactly as

$$I(s) = Y(s)V(s) + I_{is} \tag{C.1b}$$

where y_{ij} is the small signal admittance parameter and i_{is} denotes the current flowing into the *i*th terminal when all terminal are grounded to the reference point. The coefficient matrix Y(s) of (C.1b) is called the indefinite-admittance matrix [43]. The terminal V_e is inaccessible. Following the rules for writing the primitive indefinite-admittance matrix [42], equation (C.1a) for Fig. C.1 can be expressed as

$$\begin{bmatrix} i_b \\ i_c \\ i_e \\ i_g \\ i_s \end{bmatrix} = \begin{bmatrix} y_\pi + sC_\mu & -sC_\mu & -y_\pi & 0 & 0 \\ g_m - sC_\mu & g_{o0} + s(C_\mu + C_{cs}) & -(g_m + g_{o0}) & 0 & -sC_{cs} \\ -(g_m + y_\pi) & -g_{o0} & g_m + g_{o0} + g_E + y_\pi & -g_E & 0 \\ 0 & 0 & -g_E & g_E & 0 \\ 0 & -sC_{cs} & 0 & 0 & sC_{cs} \end{bmatrix} \begin{bmatrix} v_b \\ v_c \\ v_e \\ v_g \\ v_s \end{bmatrix} + \begin{bmatrix} g_{bt} \\ g_{ct} \\ -(g_{ct} + g_{bt}) \\ 0 \\ 0 \end{bmatrix} \cdot \delta T \qquad \text{(C.2)}$$

For the *CE* configuration, the contraction of the terminals 4 and 5 of Fig. C.1 can be done using the same method discussed in Appendix B. The contraction of terminals 4 and 5 reduces the matrix (C.2) to

$$\begin{bmatrix} i_b \\ i_c \\ i_e \\ i_g \end{bmatrix} = \begin{bmatrix} y_\pi + sC_\mu & -sC_\mu & -y_\pi & 0 \\ g_m - sC_\mu & g_{o0} + s(C_\mu + C_{cs}) & -(g_m + g_{o0}) & -sC_{cs} \\ -(g_m + y_\pi) & -g_{o0} & g_m + g_{o0} + g_E + y_\pi & -g_E \\ 0 & -sC_{cs} & -g_E & g_E + sC_{cs} \end{bmatrix} \begin{bmatrix} v_b \\ v_c \\ v_e \\ v_g \end{bmatrix} + \begin{bmatrix} g_{bt} \\ g_{ct} \\ -(g_{ct} + g_{bt}) \\ 0 \end{bmatrix} \cdot \delta T \qquad \text{(C.3)}$$

Assuming terminal 4 as a ground, equation (C.3) can be reduced to

$$\begin{bmatrix} i_b \\ i_c \\ i_e \end{bmatrix} = \begin{bmatrix} y_\pi + sC_\mu & -sC_\mu & -y_\pi \\ g_m - sC_\mu & g_{o0} + s(C_\mu + C_{cs}) & -(g_m + g_{o0}) \\ -(g_m + y_\pi) & -g_{o0} & g_m + g_{o0} + g_E + y_\pi \end{bmatrix} \begin{bmatrix} v_b \\ v_c \\ v_e \end{bmatrix} + \begin{bmatrix} g_{bt} \\ g_{ct} \\ -(g_{ct} + g_{bt}) \end{bmatrix} \cdot \delta T \qquad \text{(C.4)}$$

Since terminal 3 is inaccessible, it needs to be suppressed. Assume that matrix (C.4) after the suppression of terminal 3 can be expressed more compactly as

$$I''(s) = Y''(s)V''(s) + I''_{is} \qquad \text{(C.5)}$$

To suppress the *k*th terminal, the *i*th row and *j*th column element of $Y''(s)$ is given by

$$y''_{ij} = y_{ij} - \frac{y_{ik} y_{kj}}{y_{kk}} \qquad \text{(C.6)}$$

After suppression of terminal 3 using (C.6), equation (C.4) can be reduced to

$$\begin{bmatrix} i_b \\ i_c \end{bmatrix} = \begin{bmatrix} (y_\pi + sC_\mu) - \frac{y_\pi.(g_m + y_\pi)}{g_m + g_{o0} + g_E + y_\pi} & -sC_\mu - \frac{y_\pi.g_{o0}}{g_m + g_{o0} + g_E + y_\pi} \\ (g_m - sC_\mu) - \frac{(g_m + g_{o0}).(g_m + y_\pi)}{g_m + g_{o0} + g_E + y_\pi} & g_{o0} + s(C_\mu + C_{cs}) - \frac{(g_m + g_{o0}).g_{o0}}{g_m + g_{o0} + g_E + y_\pi} \end{bmatrix} \cdot \begin{bmatrix} v_b \\ v_c \end{bmatrix} + \begin{bmatrix} g_{bt} - \frac{y_\pi.(g_{ct} + g_{bt})}{g_m + g_{o0} + g_E + y_\pi} \\ g_{ct} - \frac{(g_m + g_{o0}).(g_{ct} + g_{bt})}{g_m + g_{o0} + g_E + y_\pi} \end{bmatrix} \cdot \delta T$$

(C.7)

The small-signal change in temperature, δT, can be expressed as

$$\delta T = \begin{bmatrix} \dfrac{(I_b + g_\pi V_b + g_m V_c)}{Y_{TH} - (g_{ct} V_c + g_{bt} V_b)} & \dfrac{(I_c + g_{o0} V_c)}{Y_{TH} - (g_{ct} V_c + g_{bt} V_b)} \end{bmatrix} \begin{bmatrix} v_b \\ v_c \end{bmatrix} \tag{C.8}$$

The substation of (C.7) into (C.6) gives

$$\begin{bmatrix} i_b \\ i_c \end{bmatrix} = \begin{bmatrix} (y_\pi + sC_\mu) - \dfrac{y_\pi \cdot (g_m + y_\pi)}{g_m + g_{o0} + g_E + y_\pi} & -sC_\mu - \dfrac{y_\pi \cdot g_{o0}}{g_m + g_{o0} + g_E + y_\pi} \\ (g_m - sC_\mu) - \dfrac{(g_m + g_{o0}) \cdot (g_m + y_\pi)}{g_m + g_{o0} + g_E + y_\pi} & (g_{o0} + s(C_\mu + C_{cs})) - \dfrac{(g_m + g_{o0}) \cdot g_{o0}}{g_m + g_{o0} + g_E + y_\pi} \end{bmatrix} \cdot \begin{bmatrix} v_b \\ v_c \end{bmatrix} \tag{C.9}$$

$$+ \begin{bmatrix} g_{bt} - \dfrac{y_\pi \cdot (g_{ct} + g_{bt})}{g_m + g_{o0} + g_E + y_\pi} \\ g_{ct} - \dfrac{(g_m + g_{o0}) \cdot (g_{ct} + g_{bt})}{g_m + g_{o0} + g_E + y_\pi} \end{bmatrix} \cdot \begin{bmatrix} \dfrac{(I_b + g_\pi V_b + g_m V_c)}{Y_{TH} - (g_{ct} V_c + g_{bt} V_b)} & \dfrac{(I_c + g_{o0} V_c)}{Y_{TH} - (g_{ct} V_c + g_{bt} V_b)} \end{bmatrix} \cdot \begin{bmatrix} v_b \\ v_c \end{bmatrix}$$

From (C.8), the small-signal base and collector current can be expressed as

$$i_b = \left[(y_\pi + sC_\mu) - \frac{y_\pi (g_m + y_\pi)}{(g_E + g_m + g_{o0} + y_\pi)} + \left(g_{bt} - \frac{y_\pi (g_{bt} + g_{ct})}{(g_E + g_m + g_{o0} + y_\pi)} \right) \cdot \left(\frac{I_b + g_\pi V_b + g_m V_c}{Y_{TH} - (g_{ct} V_c + g_{bt} V_b)} \right) \right] v_b \tag{C.10}$$

$$- \left[sC_\mu + \frac{g_{o0} y_\pi}{(g_E + g_m + g_{o0} + y_\pi)} - \left(g_{bt} - \frac{y_\pi (g_{bt} + g_{ct})}{(g_E + g_m + g_{o0} + y_\pi)} \right) \cdot \left(\frac{(I_c + g_{o0} V_c)}{Y_{TH} - (g_{ct} V_c + g_{bt} V_b)} \right) \right] v_c$$

$$i_c = \left[(g_m - sC_\mu) - \frac{(g_m + g_{o0})(g_m + y_\pi)}{(g_E + g_m + g_{o0} + y_\pi)} + \left(g_{ct} - \frac{(g_m + g_{o0})(g_{bt} + g_{ct})}{(g_E + g_m + g_{o0} + y_\pi)} \right) \cdot \frac{(I_b + g_\pi V_b + g_m V_c)}{Y_{TH} - (g_{ct} V_C + g_{bt} V_b)} \right] v_b \tag{C.11}$$

$$+ \left[(g_{o0} + sC_\mu) - \frac{g_{o0}(g_m + g_{o0})}{(g_E + g_m + g_{o0} + y_\pi)} + \left(g_{ct} - \frac{(g_m + g_{o0})(g_{bt} + g_{ct})}{(g_E + g_m + g_{o0} + y_\pi)} \right) \cdot \left(\frac{(I_c + g_{o0} V_c)}{Y_{TH} - (g_{ct} V_c + g_{bt} V_b)} \right) \right] v_c$$

The admittance parameters from (C.10) and (C.11) can be expressed as

$$Y_{11}(s) = \left. \frac{i_b}{v_b} \right|_{v_C = 0}$$

$$= \left[y_\pi + sC_\mu - \frac{y_\pi (g_m + y_\pi)}{(g_E + g_m + g_{o0} + y_\pi)} + \left(g_{bt} - \frac{y_\pi (g_{bt} + g_{ct})}{(g_E + g_m + g_{o0} + y_\pi)} \right) \cdot \left(\frac{I_b + g_\pi V_b + g_m V_c}{Y_{TH} - (g_{ct} V_c + g_{bt} V_b)} \right) \right]$$

$$Y_{12}(s) = \left.\frac{i_b}{v_b}\right|_{v_C=0}$$
$$= \left[-sC_\mu - \frac{g_{o0} y_\pi}{(g_E + g_m + g_{o0} + y_\pi)} + \left(g_{bt} - \frac{y_\pi (g_{bt} + g_{ct})}{(g_E + g_m + g_{o0} + y_\pi)} \right) \cdot \left(\frac{I_c + g_{o0} V_c}{Y_{TH} - (g_{ct} V_c + g_{bt} V_b)} \right) \right]$$

$$Y_{21}(s) = \left.\frac{i_b}{v_b}\right|_{v_C=0}$$
$$= \left[g_m - sC_\mu - \frac{(g_m + g_{o0})(g_m + y_\pi)}{(g_E + g_m + g_{o0} + y_\pi)} + \left(g_{ct} - \frac{(g_m + g_{o0})(g_{bt} + g_{ct})}{(g_E + g_m + g_{o0} + y_\pi)} \right) \cdot \left(\frac{I_b + g_\pi V_b + g_m V_c}{Y_{TH} - (g_{ct} V_C + g_{bt} V_b)} \right) \right]$$

$$Y_{22}(s) = \left.\frac{i_b}{v_b}\right|_{v_C=0}$$
$$= \left[g_{o0} + sC_\mu - \frac{g_{o0}(g_m + g_0)}{(g_E + g_m + g_{o0} + y_\pi)} + \left(g_{ct} - \frac{(g_m + g_{o0})(g_{bt} + g_{ct})}{(g_E + g_m + g_{o0} + y_\pi)} \right) \cdot \left(\frac{I_c + g_{o0} V_c}{Y_{TH} - (g_{ct} V_c + g_{bt} V_b)} \right) \right]$$

From (C.10) and (C.11), it can be inferred that the effective value of collector thermal transconductance, g_{ct}, and base thermal trans conductance, g_{bt}, reduces due to emitter degeneration.

APPENDIX D

MINIMUM FEEDBACK RESISTOR REQUIREMENT IN THE CLOED-LOOP OPERATION OF THE CFOA

The small-signal micromodel of a CFOA in the non-inverting gain configuration is shown in Fig. D.1

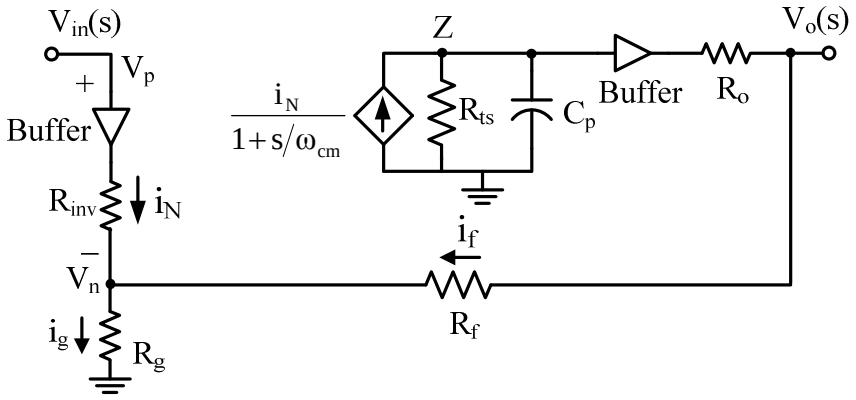


Figure D.1 Small-signal macromodel of a generic CFOA in the non-inverting closed-loop configuration [57]-[58].

The equivalent transimpedance function at the high-gain node, *Z*, of Fig. D.1 can be represented as

$$Z_T(s) = \frac{R_{ts}}{\left(1+\frac{s}{\omega_t}\right)\cdot\left(1+\frac{s}{\omega_{cm}}\right)} \tag{D.1}$$

where ω_{cm} and ω_t are the current mirror pole and transimpedance pole frequencies, respectively. The non-inverting closed-loop gain for Fig. D.1 can be expressed as [57]

$$\frac{V_o(s)}{V_{in}(s)} = \left(1+\frac{R_f}{R_g}\right)\cdot\frac{1}{\left(1+\frac{1}{T(s)}\right)} \tag{D.2}$$

where the loop-gain, T(s), can be expressed as [52]

$$T(s) = \frac{Z_T(s)}{R_f} \tag{D.3}$$

Case I: For $\omega_{cm} > > \omega_t$

The substitution of (D.1) and (D.3) into (D.2) gives

$$\frac{V_o(s)}{V_{in}(s)} = \left(1 + \frac{R_f}{R_g}\right) \cdot \frac{1}{\left(1 + \frac{R_f}{R_{ts}}\right)} \cdot \frac{1}{\left(1 + \frac{s}{\omega_t\left(\frac{R_{ts} + R_f}{R_f}\right)}\right)} \tag{D.4}$$

Assuming $R_{ts} >> R_f$, (D.4) can be simplified as

$$\frac{V_o(s)}{V_{in}(s)} = \left(1 + \frac{R_f}{R_g}\right) \cdot \frac{1}{\left(1 + \frac{R_f}{R_{ts}}\right)} \cdot \frac{1}{\left(1 + \frac{s}{\omega_p}\right)} \tag{D.5}$$

where ω_p is called closed-loop 3-dB bandwidth, and can be expressed as

$$\omega_p = \frac{1}{R_f C_p} \tag{D.6}$$

It is seen from (D.6) that the closed-loop 3-dB bandwidth is independent of the closed-loop gain. This is one of the unique advantages of a CFOA over a VFOA.

Case II: For $\omega_{cm} > \omega_t$,

Equation (D.1) can be expressed as

$$Z_T(s) = \frac{R_{ts}\omega_t\omega_{cm}}{s^2 + (\omega_t + \omega_{cm})s + \omega_t\omega_{cm}} \tag{D.7}$$

The substitution of (D.7) into (D.2) gives

$$\frac{V_o(s)}{V_{in}(s)} = \left(1 + \frac{R_f}{R_g}\right) \cdot \frac{1}{\left(1 + R_f \cdot \frac{s^2 + (\omega_t + \omega_{cm})s + \omega_t\omega_{cm}}{R_{ts}\omega_t\omega_{cm}}\right)} \tag{D.8}$$

$$= \left(1 + \frac{R_f}{R_g}\right) \cdot \frac{1}{1 + R_f \cdot \frac{s^2 + (\omega_t + \omega_{cm})s + \omega_t \omega_{cm}}{R_{ts} \omega_t \omega_{cm}}}$$

$$= \left(1 + \frac{R_f}{R_g}\right) \cdot \frac{R_{ts} \omega_t \omega_{cm}}{R_f \left[\frac{R_{ts} \omega_t \omega_{cm}}{R_f} 1 + \left(s^2 + (\omega_t + \omega_{cm})s + \omega_t \omega_{cm}\right)\right]}$$

$$= \left(1 + \frac{R_f}{R_g}\right) \cdot \frac{\frac{R_{ts}}{R_f} \omega_t \omega_{cm}}{s^2 + (\omega_t + \omega_{cm})s + \omega_t \omega_{cm}\left(1 + \frac{R_{ts}}{R_f}\right)}$$

For $\frac{R_{ts}}{R_f} >> 1$

$$\frac{V_o(s)}{V_{in}(s)} = \left(1 + \frac{R_f}{R_g}\right) \cdot \frac{\frac{R_{ts}}{R_f} \omega_t \omega_{cm}}{s^2 + (\omega_t + \omega_{cm})s + \omega_t \omega_{cm} \frac{R_{ts}}{R_f}} \tag{D.9}$$

A standard second-order transfer function in the frequency-domain be expressed as [51]

$$H(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} = \frac{\omega_n^2}{s^2 + \frac{\omega_n}{Q} s + \omega_n^2} \tag{D.10}$$

where ζ, and ω_n are called the damping ratio, and natural frequency in radians per second, respectively. The variable Q is defined as $1/2\zeta$.

Comparing (D.9) with (D.10) results in the following identifications in (D.11) and (D.12):

$$\omega_n = \sqrt{\frac{R_{ts}}{R_f} \omega_t \omega_{cm}} = \sqrt{\frac{\omega_{cm}}{R_f C_p}} \tag{D.11}$$

$$Q = \frac{\omega_n}{\omega_t + \omega_{cm}} \frac{\sqrt{\frac{R_{ts}}{R_f}\omega_t \omega_{cm}}}{\omega_t + \omega_{cm}} \tag{D.12}$$

For $\omega_t << \omega_{cm}$

$$Q = \sqrt{\frac{\frac{R_{ts}}{R_f}\omega_t \omega_{cm}}{\omega_{cm}^2}} = \sqrt{\frac{\frac{R_{ts}}{R_f}\omega_t}{\omega_{cm}}} = \sqrt{\frac{1}{R_f C_p \omega_{cm}}} \tag{D.13}$$

The 3-dB frequency for (D.10) can be expressed as

$$\omega_{-3dB} = \omega_n \sqrt{\frac{\left(2 - \frac{1}{Q^2}\right) + \sqrt{\left(2 - \frac{1}{Q^2}\right)^2 + 4}}{2}}$$

The peak frequency is given by

$$\omega_p = \omega_n \sqrt{1 - \frac{1}{2Q^2}}$$

For the peaking free frequency response, the following criterion needs to be satisfied.

$$Q < \frac{1}{\sqrt{2}} \text{ or } \zeta > \frac{1}{\sqrt{2}}$$

$$Q = \sqrt{\frac{1}{R_f C_p \omega_{cm}}} < \frac{1}{\sqrt{2}} \tag{D.14}$$

The criterion for the minimum value of the feedback resistor can be developed using (D.14), and expressed as

$$R_f > \frac{2}{C_p \omega_{cm}} \tag{D.15}$$

Thus, it is clearly seen that the minimum value of the feedback resistor is dependent on the parasitic capacitance of the high-gain “Z” node of the CFOA and the current mirror pole frequency.

APPENDIX E

THERMAL TAIL DEPENDENCE ON THE BIAS CURRENT OF THE CLASS AB BUFFER

A classical AB voltage buffer is shown in Fig E.1.

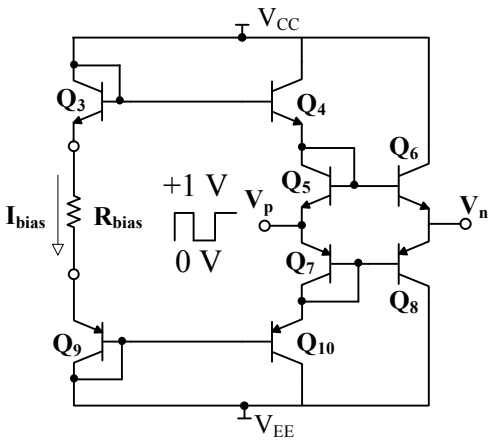


Figure E.1 Class AB voltage buffer [7]. V_p is the input and V_n is the output.

The input V_p is driven with a 0 to 1 V square wave with a rise and fall times of 40 ns, and a period of 100 μs. The simulated positive thermal tail (defined in section 5.1.5) in the step response at V_n is obtained. The bias current, I_{bias}, is swept to provide an understanding of its impact on the magnitude of the thermal tail. The change in the V_{BE} with temperature is simulated for each bias current. This is summarized in Table E.1.

Table E.1 Thermal Tail in the Step Response of Fig. E.1 with the VBIC models of Tables 2.9 and 2.10.

R_{bias}	I_{bias}	dV_{BE}/dT	Th_{tail}	$Th_{tail}/(dV_{BE}/dT)$
4.0×10^{03}	2.70×10^{-03}	1.44×10^{-03}	2.73×10^{-03}	1.90
6.0×10^{03}	1.71×10^{-03}	1.48×10^{-03}	1.78×10^{-03}	1.20
8.0×10^{03}	1.25×10^{-03}	1.52×10^{-03}	1.32×10^{-03}	0.87
1.0×10^{04}	9.78×10^{-04}	1.54×10^{-03}	1.05×10^{-03}	0.68
1.2×10^{04}	8.04×10^{-04}	1.55×10^{-03}	8.75×10^{-04}	0.56
1.4×10^{04}	6.82×10^{-04}	1.57×10^{-03}	7.52×10^{-04}	0.48
1.6×10^{04}	5.93×10^{-04}	1.58×10^{-03}	6.58×10^{-04}	0.42
1.8×10^{04}	5.24×10^{-04}	1.59×10^{-03}	5.86×10^{-04}	0.37
2.0×10^{04}	4.69×10^{-04}	2.60×10^{-03}	5.28×10^{-04}	0.20
2.2×10^{04}	4.25×10^{-04}	1.61×10^{-03}	4.81×10^{-04}	0.30
2.4×10^{04}	3.88×10^{-04}	1.62×10^{-03}	4.42×10^{-04}	0.27
2.6×10^{04}	3.57×10^{-04}	1.63×10^{-03}	4.00×10^{-04}	0.25
2.8×10^{04}	3.31×10^{-04}	1.63×10^{-03}	3.88×10^{-04}	0.24
3.0×10^{04}	3.08×10^{-04}	1.64×10^{-03}	3.56×10^{-04}	0.22

The normalized thermal tail (magnitude of thermal tail over the change in the base-emitter voltage with temperature) versus the bias current, I_{bias}, is shown in Fig. E.2, and the data is curve fitted with a linear approximation. The slope of the line approximately gives the thermal resistance.

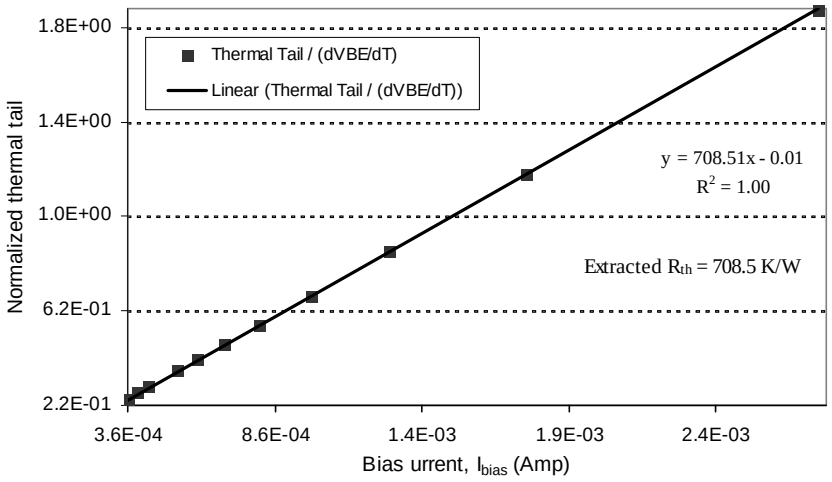


Figure E.2 Normalized thermal tail versus the bias current, I_{bias}.

From Fig. E.2, it can be inferred that thermal tail is directly proportional to the bias current of the buffer. All transistors of the buffer in Fig. E.1 have a thermal resistance of 375 K/W, while the simulation gives the thermal resistance as 708.5K/W. To characterize the thermal tail dependence on the bias current, the following expression is proposed.

$$Th_{tail} \cong KI_{bias}R_{th}\left.\frac{dV_{BE}}{dT}\right|_{I_{bias}} \qquad \text{(E.1)}$$

The parameter, *K*, is assumed to be a technology dependent parameter or a bias dependent, whose value is approximately 2 based on the simulation using the VBIC model of Tables 2.9 and 2.10.

APPENDIX F

PAD PARASITIC IMPEDANCE MEASUREMENT

The interface between an integrated circuit and the external envirionment involves a mechanical robust structure called a package. In order to attach package wires to the die, large “pads” are placed on the perimeter of the chip and are connected to the corresponding nodes in the circuit. The pad size used in UTA246S and UTA246T is 100 μm × 100 μm. The frequency responses of the parasitic impedance of the IC holder holding a 14 pin DIP package of UTA246S, and on-die pad are shown in Figs. F.1 and F.2, respectively.

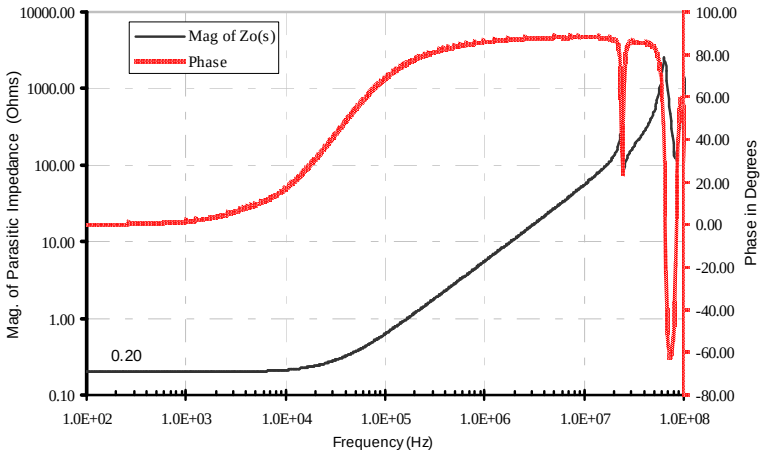


Figure F.1 Frequency response of overall parasitic impedance.

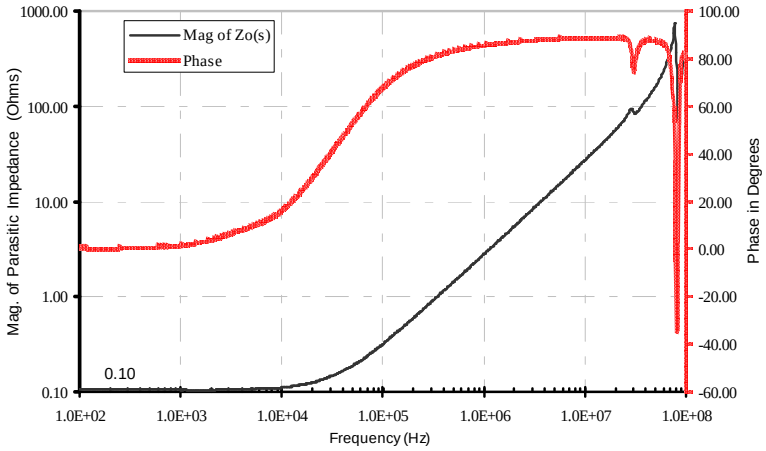


Figure F.2 Frequency response of the on-die pad of UTA246S.

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BIOGRAPHICAL INFORMATION

Kamal Sinha was born in Balra, Nepal in 1978. He received his Bachelor of Technology degree in Electronics and Communication Engineering from National Institute of Technology (formerly REC), Warangal, India in May 2000. He was with Nepal Engineering College, where he taught Microprocessor and Digital Logic Design courses between May 2000 and May 2001. He received his Master of Science degree in Electrical Engineering from the University of Texas at Arlington in May 2003. He started working towards his Ph.D. degree in Electrical Engineering from summer 2003. He has been with Intel Corporation, Folsom, CA since January 2005 as a graphics hardware design engineer, and continued his doctoral studies as a part-time student since then. His areas of interest are the low-voltage high speed serial IO circuit design, power efficient custom digital circuit design, and power management in the high performance 3D computing engine. He is keenly interested to be an academia in the future.