THERMAL EFFECTS AND ANALYSIS ON ANALOG INTEGRATED CIRCUIT DESIGN

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I also thank my wife, my parents and my brother for supporting me. Lastly, I dedicate this to my grandfather who passed away when I newly joined this research group.

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ABSTRACT

THERMAL EFFECTS AND ANALYSIS ON

ANALOG INTEGRATED CIRCUIT

DESIGN

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Dielectrically Isolated Bipolar Junction Transistors (DIBJTs) are used in various high frequency applications. High frequency application requires high gain in these devices, and the gain of DIBJTs is significantly higher than complimentary metal-oxide-semiconductor (CMOS) devices. Thermal heating from the devices itself and from adjacent devices change the device characteristics. This thesis explores the thermal effects from self heating and inter-device heating (thermal coupling) in the time domain of the device as well as at the circuit level.

This research measures and analyzes the thermal modeling of DIBJTs. Different measurement procedures are explored and implemented. After the collection of data from the devices, calculations and analysis of the data were studied. The data was used to characterize the thermal network of the device model file. Finally, real-time reasons were compared with simulated results using the redefined thermal model.

DIBJTs are an essential building block of high speed IC design [2]**.** Full DIBJTs are fabricated by using trench isolation and silicon-on-insulator (SOI) technologies. Advantages of these transistors include reduced parasitic capacitance, low leakage current, latch-up free and

radiation hardened circuitry. On the other hand, a major disadvantage of full DIBJTs is its poor thermal conductivity of the dielectric. The trench silicon oxide isolation has roughly 1% of the thermal conductivity of silicon. Because the die concentration and operating current density tend to increase, to meet the demand of the marker, bipolar transistors exhibit greater sensitivity to thermal effects caused by excessive self-heating, adjacent device heating, and packaging [3].

For the research work National Semiconductor's DIBJTs have been used to extract real work results. The process for these devices to manufacture is called VIP10. Vertical Bipolar Inter Company (VBIC) model is used to model these transistors. A 1-pole thermal circuit network is present in the VBIC network. A more complex thermal model has been developed to better match the real world measurement results from these transistors in time domain. The complex thermal model consists of five time constants circuit. Further analysis was done to convert multiple pole circuit models to single pole circuit models. Furthermore, the effects of adjacent heating devices were also explored.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

The semiconductor industry demands more advanced and smaller devices for high speed communication, high precision circuits, and faster microprocessors. Designers are faced with great challenges to meet high demands in the technological industry. Die concentration and operational speed of transistors are rapidly increasing because of market demand, leading to thermal runaway complication and current crowding effect. The susceptibility of transistors to temperature change requires a more sensitive and accurate modeling of the thermal effects of the device, as well as heating effects from adjacent devices. This research is concentrates on the thermal modeling of Dielectric Isolated Bipolar Junction Transistors (DIBJTs), ameliorating existing thermal models. Three main reasons for thermal effects in DIBJTs are, 1) thermal coupling between adjacent transistors on the same chip, 2) package thermal effects which raise the overall temperature of the chip and, 3) self-heating caused by the internal temperature rise of a particular device[1]. This paper focuses on self-heating aspects and tries to apply this knowledge to practical device characterizations and circuit designs. It also explores thermal coupling between adjacent transistors on the same chip. Several attempts have been made to improve the simulated models to achieve real world measurement results.

DIBJTs are an important building block of high speed IC designs [2]. DIBJTs are manufactured by using trench isolation and silicon-on-insulator (SOI) technologies. Some of the advantages of these transistors are reduced parasitic capacitance, low leakage current, latch-up free and radiation hardened circuitry. A major disadvantage of DIBJTs is the poor thermal conductivity of the dielectric. For this research work, the National Semiconductor's DIBJTs have

been used to extract real world results. The manufacturing process used for these devices is called VIP10.

1.2 Introduction to Dielectrically Isolated Bipolar Junction Transistors (DIBJT) using the VIP10 process

The VIP10 process utilizes deep trench technology on a bonded wafer for complete dielectric isolation and optimal high-speed amplifier performance. This process enables designers to make power-efficient and high-speed amplifiers. The improvements of VIP10 compared to its predecessors are reflected in Table 1. The VIP10 devices provide better bandwidth, lower power consumption and supply voltage, when compared to previous complementary bipolar devices. In addition, they have large output swing, high output current and low distortion [2]. The cross section of this device is represented in Figure 1 [2].

Table 1: National Semiconductor Complementary Bipolar Process [2].

Process	VIP1	VIP2	VIP3	VIP10	Units
Year	1986	1988	1994	2000	
NPN F_t	0.4	0.8	3.0	9.0	GHz
NPN β	250	250	150	100	
NPN V_a	200	150	150	120	V
PNP F_t	0.2	0.5	1.6	8.0	GHz
PNP β	150	80	60	55	
PNP V_a	60	40	50	40	V
Cjs	2.0	1.5	0.5	0.005	pF
Emitter Width	15	11	2	1	µm
Minimum Transistor Area	20000	18000	2400	300	μm^2
Isolation	JI	JI	JI	DI	

Complementary bipolar (CB) processes enables class AB output stages with very low quiescent current and high output drive in analog circuits. Also, the CB process allows high-swing complementary common-emitter output stages, commonly known as "rail-to-rail outputs." On some processes for Metal-oxide-Semiconductor Field Effect Transistors (MOSFETs), these output stages can be a challenge to design with well-controlled frequency and time-domain responses because the output transistors vary from quiescent conditions to sinking or sourcing high currents to near saturation of the output transistors. The low collector resistance and

reduced quasi-saturation effects make VIP10 process well suited for rail-to-rail output stages [4].

Rail-to-rail input stages can be designed on a CB process, by using both PNP and NPN input stages. Other circuitry is required to steer current to the appropriate differential pair depending on the common-mode voltage. Both stages usually require a folded-cascode to shift level. A CB process having high-performance Bipolar Junction Transistors (BJTs) of both types will ensure consistent performance stage when either the input stages is active. The VIP10 process goal was to deliver the highest level of analog performance possible, while minimizing wafer cost and development time. The performance benefits of complementary bipolar analog Integrated Circuits (ICs) can be seen in the analog circuits used in wired broadband applications such as xDSL and cable modems. The most critical analog blocks are the drivers and receivers. Due to differences in device physics, receivers using low base-resistance BJTs have low input noise voltage with a much lower operating current and die area than CMOS designs [4].

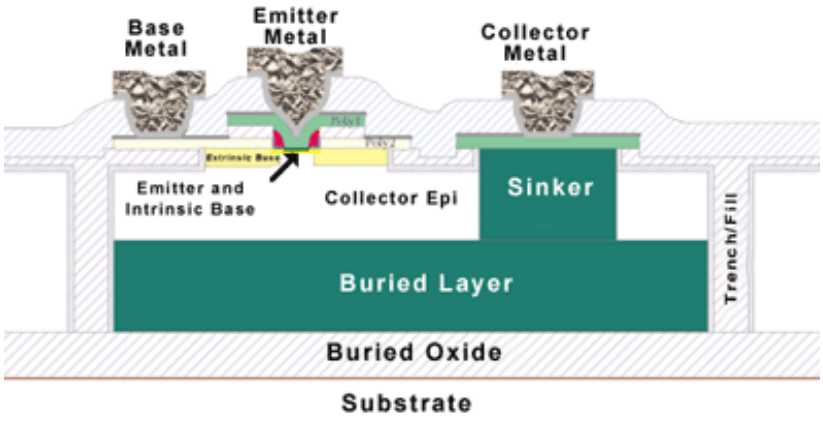


Figure 1: Cross section of a complement [4].

National Semiconductor stated that CB designs yield lower distortion than CMOS due to the higher trans-conductance of BJTs**.** High gate capacitance of large MOSFET devices have problems with stability and power dissipation. In practice, CB designs are superior in combining

low distortion, low power dissipation, and frequency stability. The higher breakdown voltages achieved in high-speed BJTs gives CB line drivers a higher output swing [4].

The minimum channel length of CMOS transistors determines the power-delay product and the IC area. Reducing CMOS channel length is expensive because it is set primarily by lithography. The analogous parameter for bipolar transistors is the vertical dimension of the active base region ("base width"), critical for determining the current gain and the transition frequency. These junction profiles are controlled by implantation and Rapid Thermal Annealing (RTA). Since the minimum feature size for a BJT (usually the emitter stripe width) is less significant than CMOS, a high-performance CB process can be developed with less investment of capital and time. The VIP10 process minimum emitter width is 1um, allowing it to be manufactured at a low cost.

As explained in the introduction, the DIBJT circuits are greatly influenced by thermal effects and accurate modeling tools are necessary to achieve effective practical design results. The Vertical Bipolar Inter Company (VBIC) model has been used to calculate the thermal effects of transistors. The VBIC is preferred over the Spice Gummel Poon (SGP) model because it is a more accurate model and has a self heating parameter. Using the VBIC model, the thermal parameters can be altered to obtain simulated results which accurately reflect the measurement results.

1.3 Introduction to the Vertical Bipolar Inter Company (VBIC) Model

VBIC model for BJT was developed in 1995 to replace the SGP model. VBIC is designed not only to mimic but also to overcome major deficiencies the SGP model lacks. The advantages of VBIC to its predecessor, SGP [5] are:

- Correct Early effect based on the junction charges
- Modified Kull model for quasi-saturation valid for high-injection at the collector junction
- Parasitic substrate transistor
- Weak avalanche current included at the base-collector junction

- Self-heating model defined as embedded in code by a thermal network.
- First-order model of distributed-base for AC and DC emitter current crowding
- Improved single-piecewise junction capacitance model
- Improved complete static temperature mapping
- Inclusion of overlap capacitance
- Improved high-level diffusion capacitance modeling
- Second-order excess phase network consistent with AC->transient
- High-order continuity in equations
- Decoupling of base and collector current
- Improved Heterojunction Bipolar Transistor (HBT) modeling

In Figure 2, the thermal circuit is represented by thermal resistance (R_{th}) and thermal capacitance (C_{th}) network, is used by the VBIC model. The R_{th} and C_{th} results to a 1-pole network (circuit with a single time constant), and does not take into account the different regions of the device that could possibly contribute multiple poles to the thermal network. The thermal network is added to the four terminal transistor networks (collector, base, emitter and substrate) to model the local temperature rise.

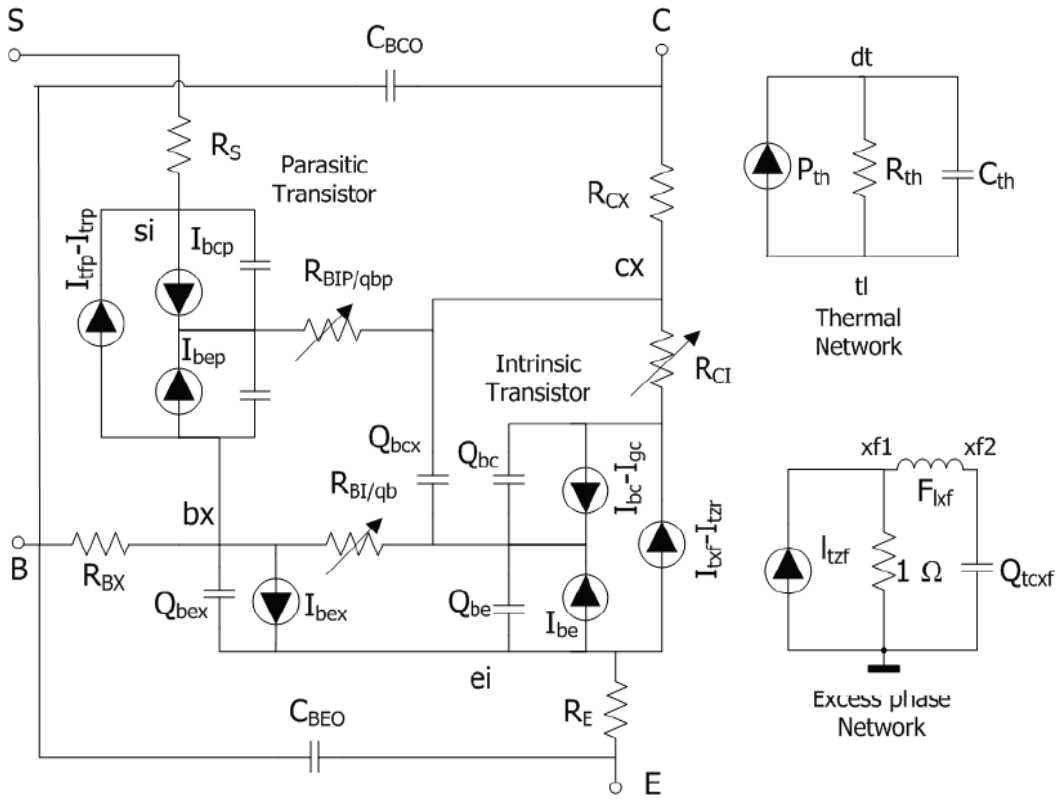


Figure 2: The VBIC Model [5].

1.4 Conclusion

Several procedures were done to determine the R_{th} and C_{th}. The R_{th} can be calculated from the frequency and static domain measurements. It is essential to perform the time domain measurements for the C_{th} calculation.

In the second chapter, the self heating effect of a single device is discussed along with an analytical and mathematical approach of self heating. Measurements of these devices have been made using either 2-pole or 3-pole model. Thermal model has been added to the device model file in order to produce simulated results similar to its measurement. The 2-pole or 3-pole circuit network is then approximated to a 1-pole model.

Chapter three discusses the same approach for calculating R_{th} and C_{th} that is influenced by the adjacent devices. This is referred to as the thermal coupling R_{th} and C_{th}. The

R_{th} is derived from the dc domain measurement and C_{th} is obtained from the time domain measurements.

CHAPTER 2

THERMAL ANALYSIS AND CHARACTERIZATION OF DIELECTICALLY ISOLATED BIPOLAR JUNCTION DEVICES

Chapter 1 introduced the physical structure of a DIBJT and also described the modeling aspects for the device. In this chapter, a description of the thermal effects of a single device and its implementation is discussed. This is followed up with analysis and measurement of devices. Finally, this chapter suggests the changes that can be made in the device model, in order to incorporate the self heating effect of a single device.

2.1 Self Heating Effects on DIBJT

DIBJT can be achieved with the use of trench isolation and silicon-on-insulator (SOI) technologies. Reduced parasitic capacitances, low leakage currents, latch-up free, and radiation hardened circuitry are some advantages of DIBJT [14]. However, a major disadvantage of full dielectric isolation is an increase in self-heating. The silicon-oxide used in the trench and buried isolation has a thermal conductivity of approximately two orders of magnitude lower than that of bulk silicon [14]. This impedes the flow of heat away from device, resulting in higher operating temperature. Bipolar transistors fabricated using these technologies will exhibit greater sensitivity to thermal effects caused by excessive self-heating. With increase in die concentration and higher operating current density, devices are getting more sensitive to temperature. The resulting high junction temperature can have deleterious effects on the reliability of the transistors [15] and induce shifts in their I-V characteristics [16]. Fox and Lee [17] predicted that local thermal effects can induce a variation in excess of 2 to 1 in the gain of a two stage op-amp.

Three mechanisms are mainly considered which contribute to heating effects in BJT circuits [15][17][18]. The first mechanism is adjacent heating effect, can cause a coupling from

the power of one transistor to the temperature of another on the same chip. Another mechanism is the chip-to-package-to-ambient thermal impedance [3] [18]. The total power dissipated on the chip that can be multiplied by this value of the chip-to-package-to-ambient thermal impedance to obtain an overall chip temperature. Thermal transients mediated by the chip-to-package-to-ambient thermal impedance can start less than 1 m-sec after a power change and last for longer period of time. This wide range of time scale is typical of distributed effects such as heat flow. Typical values of package thermal resistance range from 5 to 200 K/W**,** with differences due to different package types. This thermal resistance can also be affected by the quality of the die attachment and by heat sinking. Another effect that can cause cross-chip coupling is the temperature gradient that can arise when power is generated non-uniformly across a chip. [18]

The third and primary mechanism is the rise in a transistor's base emitter junction temperature which is caused by the transistor's own power dissipation.

2.2 Mathematical Representation of self heating effect

The core of VBIC is the transport current model which is the continuity equation for electrons in simple terms, represented in equation 2.1.

$$\nabla \cdot J_e = q\left(\frac{\partial n}{\partial t} + R_e + G_e \right) \qquad (2.1)$$

where J_e is the electron current density, q is the magnitude of the electronic charge, ∂t is the difference in time, n is the electron concentration, and R_e and G_e are the electron recombination and generation rate respectively. The drift-diffusion current is calculated from the equation 2.1. A more complicated version of the equation 2.1 is explained in Chapter 2 of "Design of System on a Chip" by C.C McAndrew [19]. The electron concentration n, R_e and G_e are all temperature dependent. In equation 2.1, the electron recombination and generation rate is represented by simple terms, but the actual term is a combination of several conditions and terms. A more detailed explanation is in provided in McAndrew chapter in 'Designing of System on a Chip'.

$$n = n_i \exp\left(\frac{q \cdot \psi - q \cdot \varphi_e}{kT}\right) \tag{2.2}$$

where n_i = the intrinsic carrier concentration, $n_i = DT^3 e^{-\left(Eg(0)/V_T\right)}$, q is the magnitude of the electronic charge, k is the Boltzmann's constant, T is the temperature in degrees Kelvin, ψ is the electrostatic potential, and φ_e is the electron quasi-Fermi potential.

BJT is very sensitive to temperature change. In the forward region the a simplified version of collector current (I_C) is represented as

$$I_C = I_S\left(1 + V_{CE}/V_A\right)\exp\left(V_{BE}/V_T\right) \tag{2.3}$$

where V_A = the Early Voltage, V_{BE}= base-emitter voltage, V_{CE} = collector-emitter voltage, V_T= thermal voltage, I_S is the saturated current which can be expressed as

$$I_S = \frac{qAn_i^2 D_n}{Q_B} \tag{2.4}$$

where q= electron charge, A = cross section of the emitter, n_i = the intrinsic carrier concentration $\left[n_i = DT^3 \exp\left(-Eg(0)/V_T\right)\right]$,Eg(0) is band-gap voltage of silicon, D_n= the average effective value for the electron diffusion constant in the base $D_n = \mu_n \frac{kT}{q}$, μ_n is the electron mobility, Q_B = number of doped atoms in the base per unit area of the emitter, $Eg = kT\left(\frac{N_C N_V}{n_i^2}\right)$ where N_C is the effective density of states in the conduction band, N_V is the effective density of states in the valance band.

Rewriting equation 2.4 as

$$I_S = C \cdot D_n \cdot n_i^2 \qquad (2.5)$$

where C represents only the temperature independent quantities. Since the intrinsic carrier concentration (n_i) is dependent on the energy band-gap and the electron occupation probability of the energy state, n_i increases rapidly with temperature.

The base current is a factor of I_C and β. β increase with temperature because of the band-gap narrowing effect and can be approximated by the equation below.

$$\beta(T) \approx \exp\left(-\Delta Eg / kT\right) \qquad (2.6)$$

where ΔE_g =effective value of the band-gap reduction in the emitter, k = Boltzmann constant. Because of the heavy doping of the emitter, β often has a tendency to be more sensitive to temperature variation, whereas band-gap narrowing makes the base current less sensitive to temperature. The base current is [3]

$$I_B \approx \frac{qADT^3 \exp\left(-Eg(0)/V_T\right)}{Q_B} \mu_n \frac{kT}{q}\left(1 + \frac{V_{CE}}{V_A}\right)\exp\left(-V_{BE}/V_T\right)\exp\left(-\Delta Eg/kT\right) \ldots\ldots\ldots\ldots$$

$$\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \qquad (2.7)$$

$$I_C = CD_n n_i^2 \left(1 + \frac{V_{CE}}{V_A}\right)\exp\left(-V_{BE}/V_T\right) \qquad (2.8)$$

Equation 2.8 is derived from Equation 2.3 and 2.4. The base emitter voltage is defined by the voltage drop produced across the network among the resistors R_{BX}, R_{BI} and R_E in Figure 2. Respectively the collector emitter voltage is defined voltage across the network among R_{CX}, R_{CI} and R_E in Figure2. There are three important mechanisms that contribute to the calculation of these resistors. These are Shockley-Read-Hall recombination, Auger recombination and

surface hole recombination. All there recombination processes are temperature and time dependent [17][18][19].

The power is represented by the following equation

$$P_{Th} = \left(V_{BE} \times I_B\right) + \left(V_{CE} \times I_C\right) \quad (2.9)$$

Equation 2.9 is a simplified version of the actual VBIC power equation represented in Equation 43 in the McAndrew chapter on 'BJT Modeling with VBIC' in 'Design of System On a Chip'[19].

The rise in temperature is represented by dT. Therefore when the temperature rises the overall temperature become (T + dT) in the above equations. This increase in temperature increases the I_s and β values, thus increasing the power dissipation. The temperature change affects the following factors which are all dependent on each other as shown in the equations 2.8-2.9 [11][13][10]:

- Mobility
- Band gap energy
- I_C and I_B

This rise in temperature can be represented by the product of the thermal impedance (Z_{Th}) and the power.

$$\Delta T = P_{Th} \times Z_{Th} \quad (2.10)$$

The thermal impedance is an exponential model represented in the equation 2.11

$$Z_{th} = R_{th}\left(1 - \exp\left(-t/C_{Th}R_{Th}\right)\right) \quad (2.11)$$

The Early voltage (V_A) measured when V_{BE} conditions is held constant, is very sensitive to small temperature variations caused by self heating [11]. When V_{CB} increases, the collector current increases due to both base width modulation and self-heating.

$$\Delta I_C = \left(\frac{\partial I_C}{\partial V_{CB}} \right)\Big|_T \cdot \Delta V_{CB} + \left(\frac{\partial I_C}{\partial T} \right)\Big|_{V_{CB}} \cdot \Delta T \tag{2.12}$$

From equation 2.12, the rise in temperature with respect to time is derived [12].

$$T_{rise}(t) = \Delta T\left(1 - \exp\left(\frac{-t}{\tau} \right) \right) \tag{2.13}$$

where $\tau = R_{th} \cdot C_{th}$

The thermal resistance (R_{Th}) can be calculated by dividing the temperature difference between two closed isothermal surfaces divided by the total heat flow between them. The thermal capacitance (C_{Th}) is defined as the amount of heat energy that can be stored and dissipated in a device in a given time frame.

$$R_{Th} = \frac{T_j - T_a}{P} \tag{2.14}$$

where T_j = the junction Temperature, T_a= the ambient temperature and, P = total heat flow rate

$$C_{Th} = \rho_S \times C_S \times W \times L \times D \tag{2.15}$$

where ρ_S = specific weight of the substance, C_S= specific heat capacity of the substance

W,L,D = the dimensions

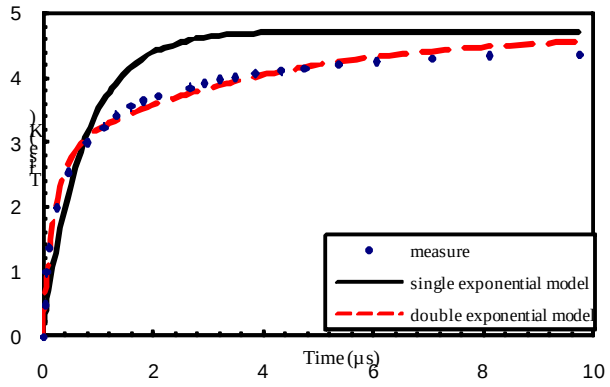


Figure 3: Result in temperature obtained from the single and double exponential models from 8x5x1 npn device.

The Junction temperature (T_j) can be expressed as

$$T_j=T_{amb}+R_{th}(P_{diss}) \tag{2.16}$$

$$T_j=T_{amb}+R_{th}(V_{ce}\cdot I_c +V_{be}\cdot I_b) \tag{2.17}$$

where T_{amb} is this the ambient temperature.

For forward gummel configuration, V_{ce} =V_{be}, the temperature Tj for two different temperature environment can be represented as

$$T_{j1}=T_{amb}+R_{th}(V_{ce}\cdot I_{c1} +V_{be}\cdot I_{b1}) \tag{2.18}$$

The temperature of the environment is increased and the junction temperature of the second environment can be represented as with same V_{ce} and V_{be}:

$$T_{j2}=T_{amb}+R_{th}(V_{ce}\cdot I_{c2} +V_{be}\cdot I_{b2}) \tag{2.19}$$

Comparing equation 2.18 and 2.19 results of R_{th} equation

$$R_{Th} = \frac{T_{j1} - T_{j2}}{V_{CE} \times (I_{c1} + I_{b1} - I_{c2} - I_{b2})} \tag{2.20}$$

Thus R_{th} can be represented as

$$R_{th} = \frac{\partial T}{\partial P_{th}} \tag{2.21}$$

where ∂P_{th} represents change in power

The Junction temperature can be calculated from the following set of equation

$$I_C = I_S e^{\left(V_{be} / V_T \right)} \tag{2.22}$$

$$V_{be} = V_T \ln\left(I_C / I_S \right) \tag{2.23}$$

$$\partial V_{be} = V_T \partial(\ln(I_C)) \tag{2.24}$$

$$Tj = \frac{q}{k}\left(\frac{\partial V_{BE}}{\partial\left(\ln\left(I_c\right)\right)} \right) \tag{2.25}$$

where *k* = boltzmann constant, and q = electronic charge

2.3 Characterization and Modeling of the thermal impedance of Dielectrically Isolated Bipolar junction devices

Figure 4 represents a simplified layout for a similar complementary bipolar process from National Semiconductor Corporation. Trench isolation which is the dotted region in Figure 4 is used in the VIP10 process for the fabrication of these DIBJTs. For this process, a very narrow deep trench is itched around the device [9].

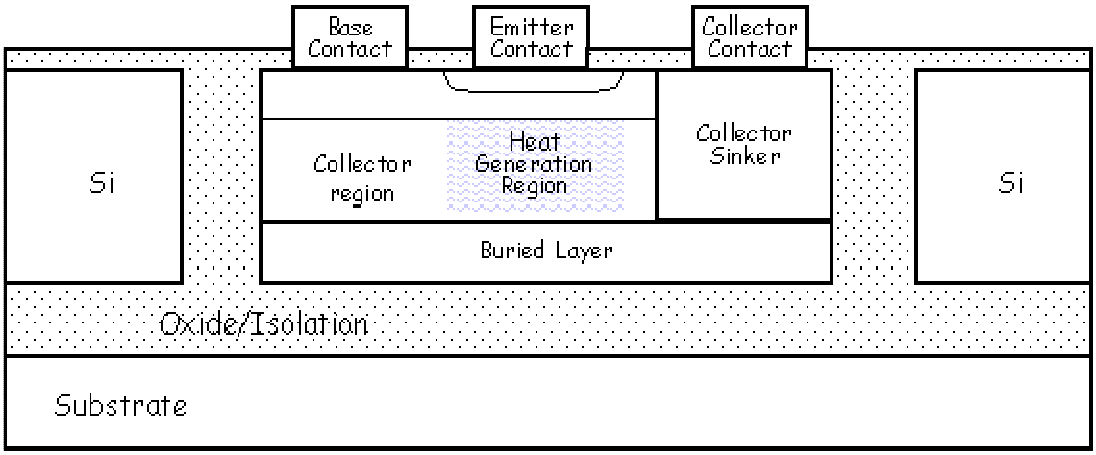


Figure 4: Schematic cross-section of a Dielectrically-Isolated Bipolar Junction Transistor. The Emitter, Base and Collector (including sinker and buried layer) regions are isolated within the dielectric box[11][13].

These trenches are then filled with silicon oxide to offer high resistance to heat flow, and this increases the thermal heating of each device. The thermal impedance for the DIBJT is represented in Figure 5. The five thermal impedance components are

- R_{tub}, C_{tub} the resistance and capacitance representing the active region
- R_{ox}, C_{ox} the resistance and capacitance representing the isolation at the bottom of the tub
- R_w, C_w the resistance and capacitance representing the wafer
- R_{per}, C_{per} the resistance and capacitance representing the peripheral trench region
- R_{dist}, C_{dist} the resistance and capacitance representing the inter device and distributed

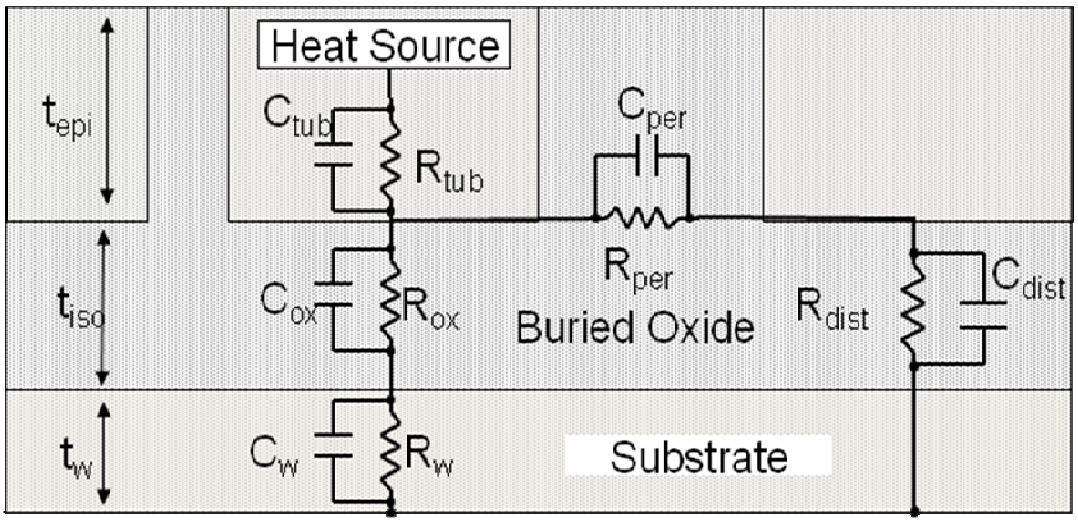


Figure 5: The five pole thermal impedance Model [10][11][12][13].

The individual impedances can be evaluated by using the dimensions of each region and material properties of that region. The total steady-state thermal resistance in static domain is [12]

$$R_{Th} = R_{tub} + \frac{1}{\left(\frac{1}{R_{ox} + R_w} + \frac{1}{R_{per} + R_{dist}} \right)} \tag{2.26}$$

The impedance components in Figure 5 accounts for the five pole thermal resistance. P_{th} is the thermal power. Each thermal resistance in Figure 5 represents a corresponding thermal capacitance that accounts for the thermal effect delay and thermal frequency response. Thermal capacitances are related to the thermal time constants. The time constant (τ_{th}) is the product of the thermal resistance and capacitance. Since the circuit is a five pole structure, it has five time constants represented by five poles. Each of the resistance and capacitance combinations produce a time constant.

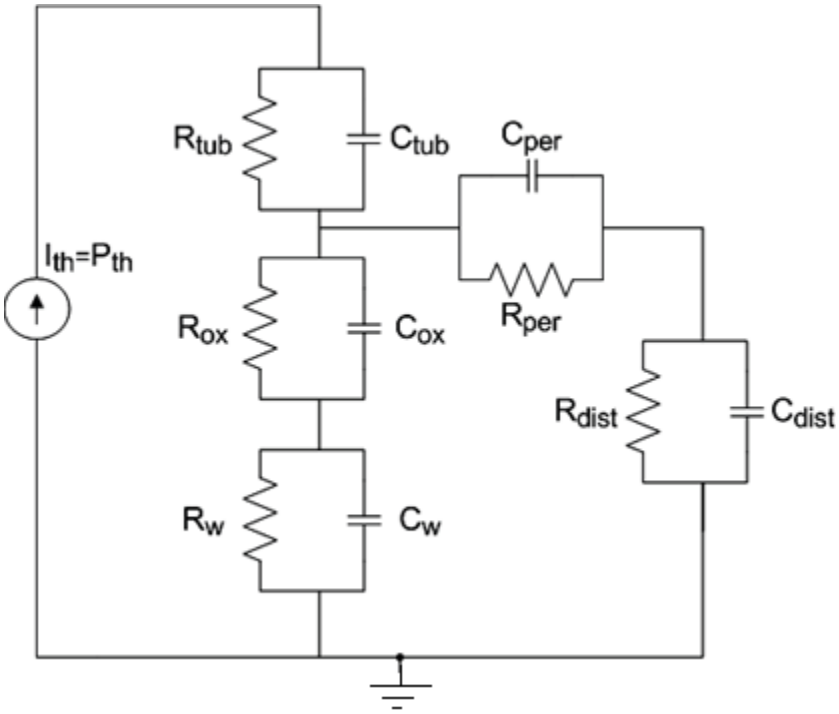
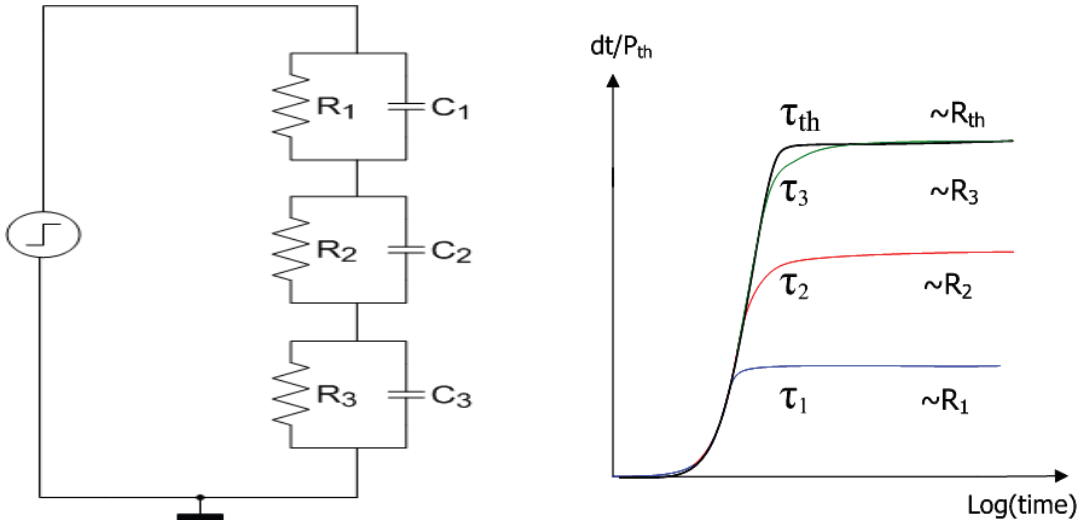


Figure 6: Represents the Thermal circuit model [13].

The symbolic plots in the time domain are shown in Fig. 7(b). The plot shows three time constants corresponding to R_1C_1, R_2C_2 and R_3C_3 time constants. The three time constants are τ_1, τ_2 and τ_3. Equation (2.27) shows the relation among the thermal resistance components and the time constants. A 3-pole network (circuit with three time constant) is a better fit to the measured data compared to 1-pole network.

$$R_{th}(t) = R_1(1+e^{-t/\tau_1}) + R_2(1+e^{-t/\tau_2}) + R_3(1+e^{-t/\tau_3}) \quad (2.27)$$



(a) (b)

Figure 7a): A three plot model b): Thermal resistance.

2.4 VBIC model representation for the self heating effect on the device

The VBIC model was introduced in Chapter 1. Its thermal representation is shown in figure 8 [13].

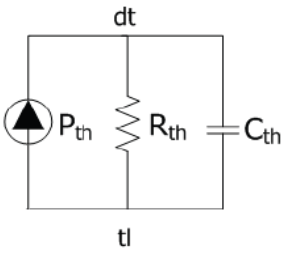


Figure 8: VBIC representation of the thermal heating effect[11].

The dT node represents the rise in temperature per unit voltage meaning a rise of 1K would result to an increase of 1V at the dt node. The tl node represents the ambient temperature. In latest version of VBIC (version:1.1.12), the 'tl' node was grounded. The 'tl' node in this thesis, provided by National Semiconductor, was not internally grounded. The thermal circuit is a single pole structure. In the VBIC parameter model values of R_{th} and C_{th} are given.

When the self heating parameter is assigned the value of '1' in the VBIC parameter model file of the transistors, this addition circuit is incorporated in the simulation. Appendix B shows the process of adding the dt and tl node to the transistor in spectra.

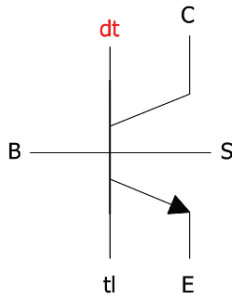


Figure 9: The transistor with the added dt, tl and S nodes [10].

First, self heating is turned on by changing selft to '1' in the model file of the device. Next, a negative R_{th} and C_{th} is added to the circuit at the dT node to cancel the values of the R_{th} and C_{th}, which is provided in the model file of the VBIC model (Rev typ.013). This arrangement is shown in Figure 18. Finally,addition circuit was attached to get the necessary thermal structure desired [10][13]. This is later explained.

2.5 Mathematical Representation of a 2-pole to a 1-pole circuit [6]

In the VBIC model file, the thermal network is a 1-pole circuit. Since a 3-pole circuit is used to match the measured result, it is necessary to find a process of converting a 3-pole circuit to 1-pole circuit. In this section, a mathematical approach is explained to convert a 2-pole circuit to 1-pole circuit. Similarly, a 3-pole circuit can be converted to 2-pole circuit and then to 1-pole circuit. It is necessary that the approximated 1-pole circuit has the same starting and settling dc value and also crosses the 1/e load line.

Two scenarios are considered to convert a 2-pole to a 1-pole circuit. The first scenario is when the two poles are very close to each other.

Taking into this consideration the following equation

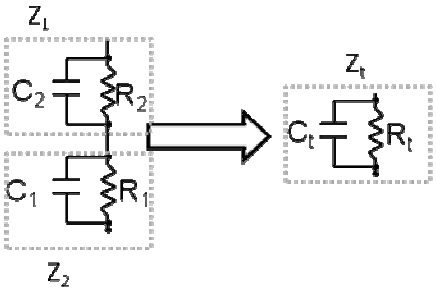


Figure 10: The conversion of 2 pole to 1 pole.

$$Z_t(s) = Z_1(s) + Z_2(s) = \frac{R_1}{1 + sR_1C_1} + \frac{R_2}{1 + sR_2C_2} \tag{2.28}$$

Let a =R_1C_1 and b = R_2C_2 and let Z represent the impedance of the networks respectively.

Then,

$$Z_t(s) = \frac{R_1}{1 + sa} + \frac{R_2}{1 + sb} \tag{2.29}$$

$$= \frac{\left(R_1/a\right)}{\left(1/a\right) + s} + \frac{\left(R_2/b\right)}{\left(1/b\right) + s} \tag{2.30}$$

$$Z_t(t) = \left(\left(R_1/a\right) \times \exp\left(-\frac{t}{a}\right)\right) + \left(\left(R_2/b\right) \times \exp\left(-\frac{t}{b}\right)\right)$$

(2.31)

$$= \exp(-t)\left[\left(\left(R_1/a\right) \times \exp\left(\frac{1}{a}\right)\right) + \left(\left(R_2/b\right) \times \exp\left(\frac{1}{b}\right)\right)\right] \tag{2.32}$$

If a ≈ b, then

$$Z_t(t) = \exp\left(\frac{-t}{a}\right)\left[\frac{R_1 + R_2}{a}\right] \quad \text{in terms of a} \tag{2.33}$$

$$Z_t(t) = \frac{\left(R_1/a\right) + \left(R_2/b\right)}{s + \left(1/b\right)} = \frac{R_t}{1 + sR_tC_t}$$

(2.34)

$$\frac{b \times \left[\left(R_1/a\right) + \left(R_2/b\right)\right]}{bs + 1} = \frac{R_t}{1 + sR_tC_t} \tag{2.35}$$

Therefore, if $R_t = b \times \left[\left(R_1/a\right) + \left(R_2/b\right)\right] = R_1 + R_2$

Then
$b=R_tC_t$

So
$$C_t = \frac{\left[\frac{R_t}{\left(R_1/a\right)+\left(R_2/b\right)}\right]}{R_t} = \left[\frac{1}{\left(R_1/a\right)+\left(R_2/b\right)}\right] \quad (2.39)$$

The second scenario occurs when the poles are far apart

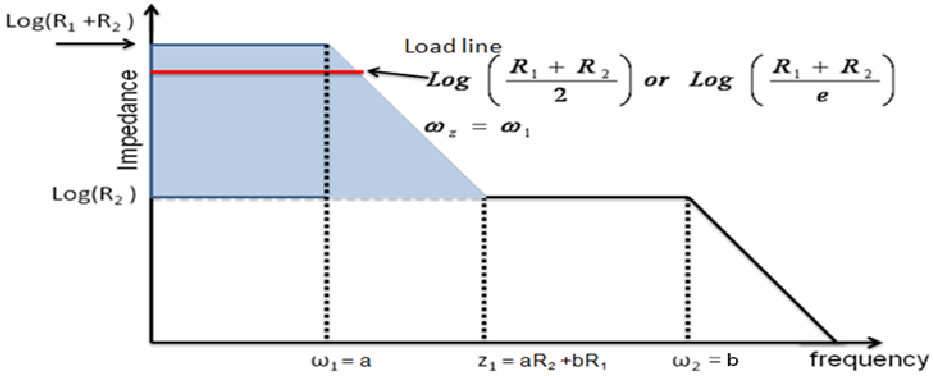


Figure 11: Representing the 3dB and 1/e line in the shaded region for 2-pole circuit (two pole network).

The load line is the 3dB point or the 1/e ratio of the two pole model. Now, if the horizontal solid line lies in the shaded region of the diagram then, ω_z is approximately equal to ω_1[6] represented in Figure 11

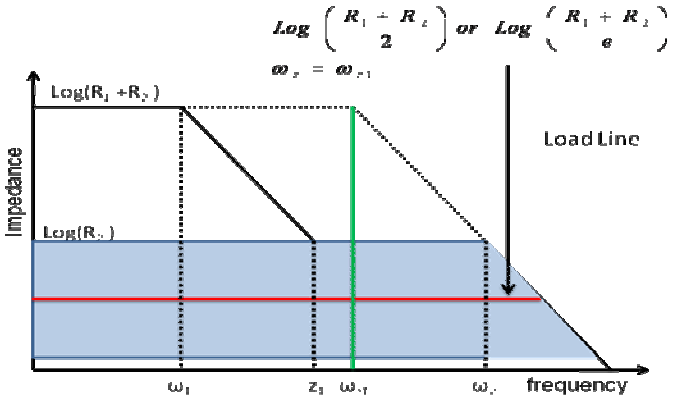


Figure 12: Representing the 3dB and 1/e line in the shaded region for 2-pole circuit (two pole network).

If the 1/e or 3dB line (horizontal solid line) is in the shaded region as represented in Figure 12, ω_z is equal to ω_{z1}.

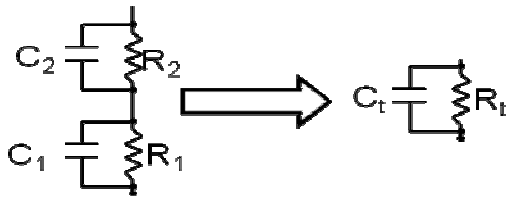


Figure 13: 2 pole networks to 1 pole approximation.

The two pole model has to be

$$Z_t(s) = Z_1(s) + Z_2(s) = \frac{R_1}{1 + sR_1C_1} + \frac{R_2}{1 + sR_2C_2} \tag{2.40}$$

$$Z_T = \frac{(R_1 + R_2)\left(1 + s\dfrac{C_1R_1R_2 + C_2R_1R_2}{R_1 + R_2}\right)}{(1 + sR_1C_1)(1 + sR_2C_2)} \tag{2.41}$$

The one pole model is

$$Z_T = \frac{R_{Th}}{1 + sR_{Th}C_{Th}} \tag{2.42}$$

The slope in bode plot is 20dB.
Therefore,

$$\left(\frac{d20[\mathrm{Log}R]}{d\omega}\right) = 20$$

$$\Rightarrow \frac{20[\mathrm{Log}(R_1 + R_2) - \mathrm{Log}(R_2)]}{\mathrm{Log}\,\omega_2 - \mathrm{Log}\,\omega_{z1}} = 20$$

$$\Rightarrow \mathrm{Log}\,\omega_2 - \mathrm{Log}\,\omega_{z1} = \mathrm{Log}(R_1 + R_2) - \mathrm{Log}(R_2)$$

$$\omega_{z1} = \frac{R_2 \cdot C_2 \cdot R_2}{R_1 + R_2} = \frac{R_2^2 \cdot C_2}{R_1 + R_2}$$

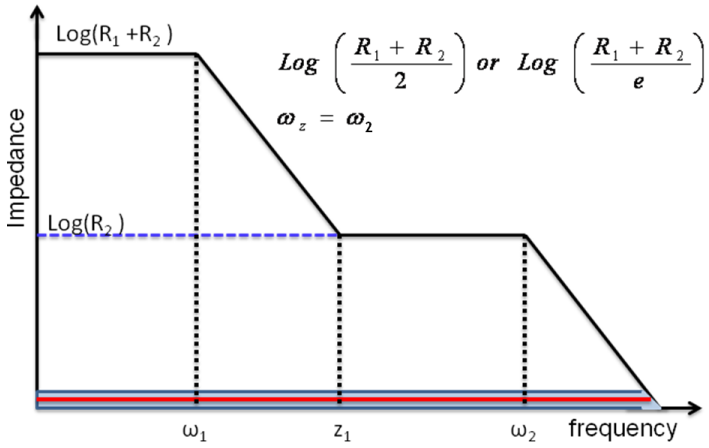


Figure 14: Representing the 3dB and 1/e line in the shaded region 2-pole circuit (two pole network).

Finally if the 1/e or the 3dB line is very near the bottom of the impedance axis it is assumed that ω_z is equal to ω_2.

A Matlab program file is attached in Appendix C. The MatLab and Spice simulations of this approximating are shown below.

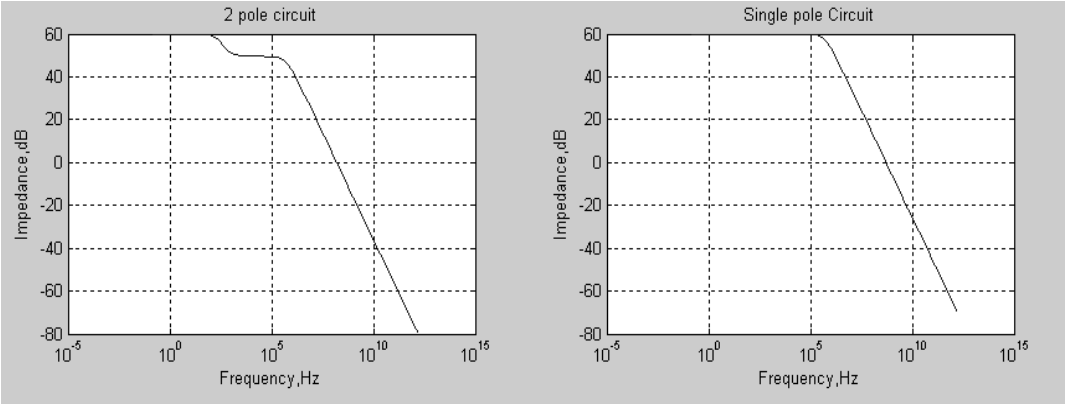


Figure 15: Matlab Simulation Result for 2 pole to 1 pole.

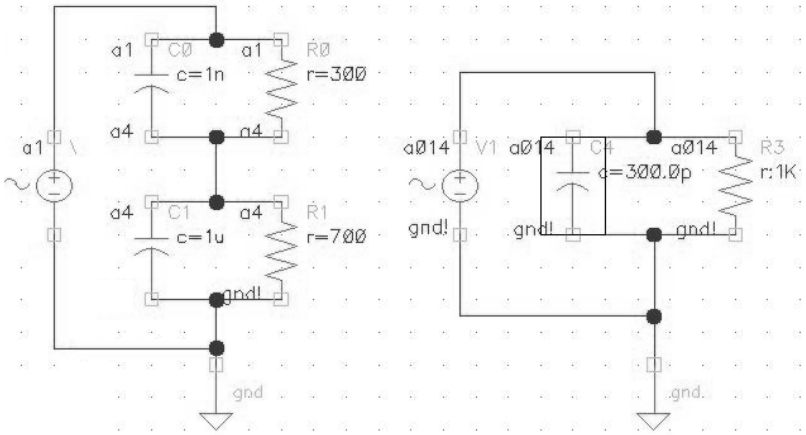


Figure 16: Spice Simulation circuit for 2 pole to 1 pole.

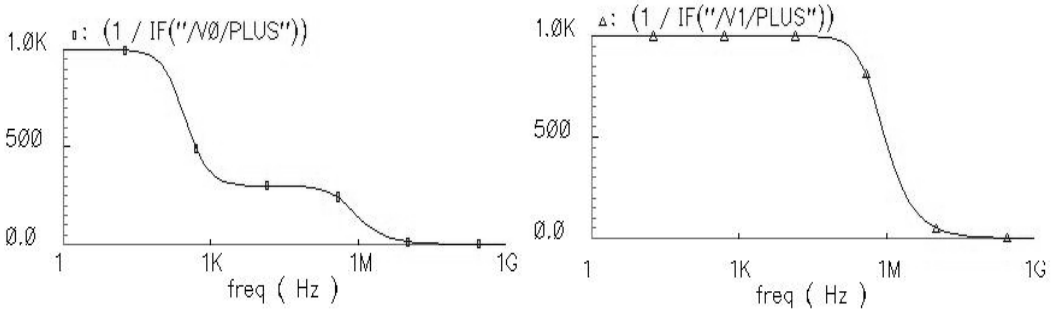


Figure 17: Spice Simulation result for 2 pole to 1 pole approximating.

Figure 15 represents the result of the conversion of a 2-pole circuit to a 1-pole circuit using the mathematical approach. If the R1=300Ω and R2=700Ω, and C1=1pf and C2=1uf, the results from mathematical approach and it's Spice simulation are represented in Figure 15-17. The SPICE simulation is done using the result obtained from the mathematical approximation and is compared with the mathematical result. Figure 17 shows the result from the SPICE simulation. Both the results match accurately.

2.6 Incorporating suggested thermal Model in VBIC

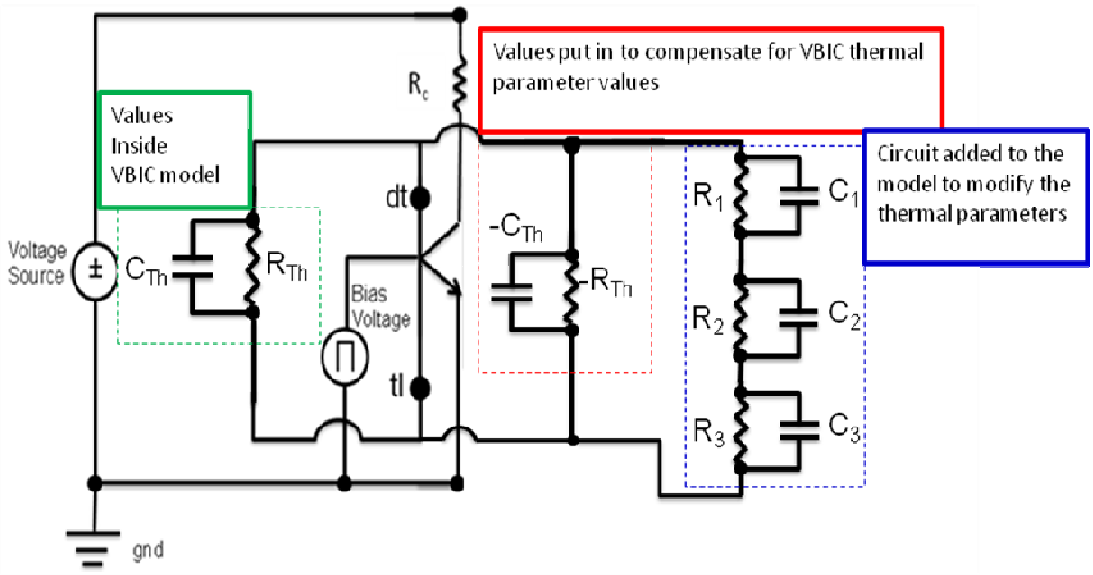


Figure 18: Circuit setup and representation for a 3-pole thermal model.

Figure 18 shows the setup in which the thermal model circuit is added. The NPN transistor used here has an additional dt and tl node which corrosponds to the thermal circuit network in the VBIC model as in Figure 2. When 'selft' is on, the thermal network of Figure 18 is taken into account for simulation. In order to nullify the effects for the VBIC thermal network, a negative C_{Th} and R_{Th} is added to the dt node of the NPN transistor. The values for C_{Th} and R_{Th} are the same as given in the VBIC model file except are are negative. After that, the desired thermal circuit can be added to the dt node. In case of Figure 18, a 3-pole thermal model is added. This procedure of adding the thermal model has been done in Integrated Circuit Characterization and Analysis Program (ICCAP). First the simulation of the circuit was done using the modified thermal network. Then measured data was imported to ICCAP and compared to simulated data. By an optimization process in ICCAP, the respective R_1, C_1, R_2, C_2 R_3 and C_3 were obtained. Because the whole concept behind this is to find better approximate values for R_{Th} and C_{Th} in the VBIC parameter model file, this 3-pole model is converted to a

single pole model. This is done because the VBIC model has only one pole for the thermal circuit. Thus an optimum value for the 1-pole model must be obtained from the 3-pole model. The reason for starting with a 3-pole model instead of 5-pole model as shown in Figure 4 is because when simulating a 5-pole model ICCAP encounters convergence problems.

2.7 Setting up the simulation in ICCAP

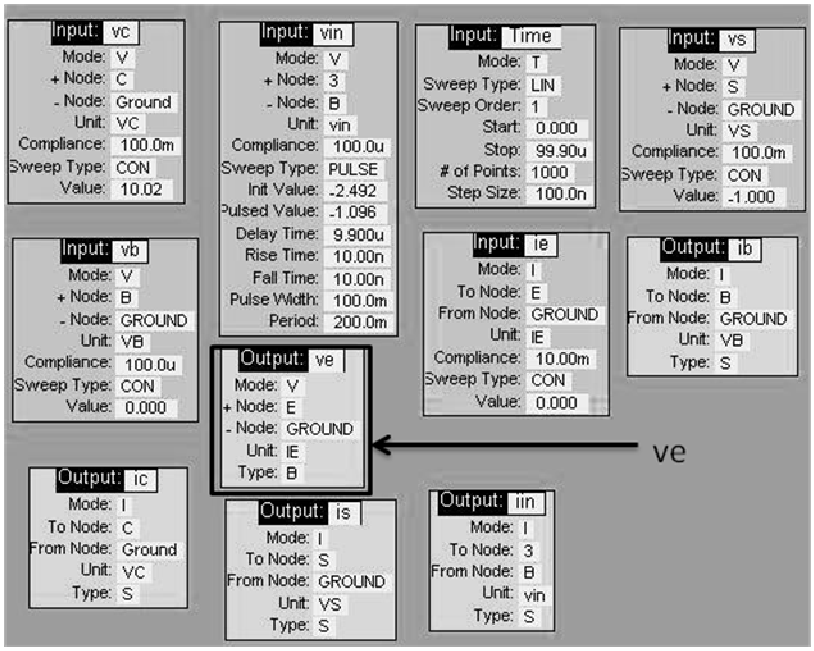


Figure 19: The setup of the circuit in ICCAP.

There are several input and output pins in ICCAP. The ICCAP setup shown in Figure 19 corrosponds to the circuit in Figure 18. Measurement were made using an oscilloscope, a function generator and power supply of the circuit in Figure 18. The base-emiiter voltage (V_{be}) was measured. Since the circuit is a common base circuit, the voltage at emitter of the device corrosponds to the V_{be} voltage.

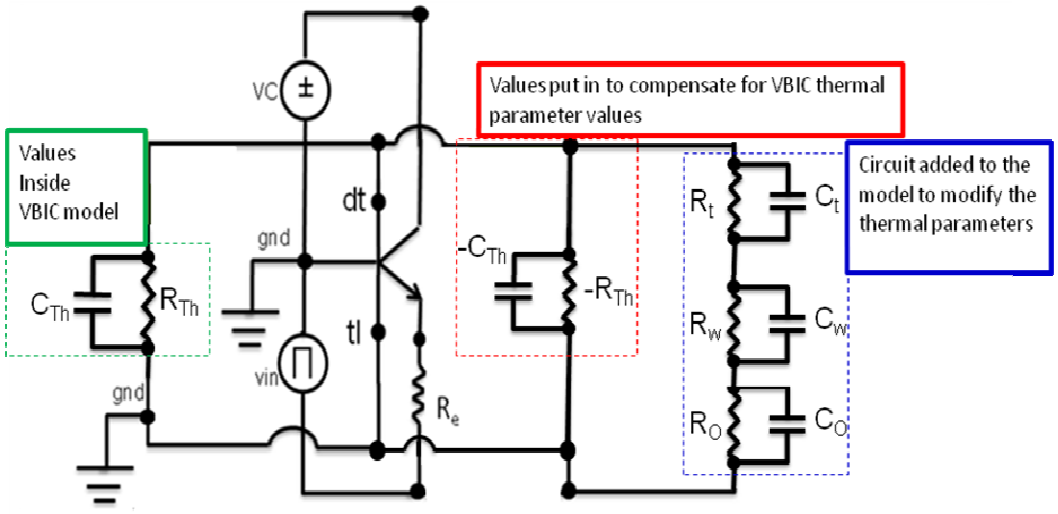


Figure 20: Circuit setup for the calculation of the thermal models [13] in ICCAP.

Now in the output pins of ve as shown in Figure 19, the measured value is imported into ICCAP. Thus ICCAP now has the measured as well as the simulated values. By using ICCAP optimization the C_t, R_t,C_w,R_w,$C_o$and R_o are optimized to match the measured results.

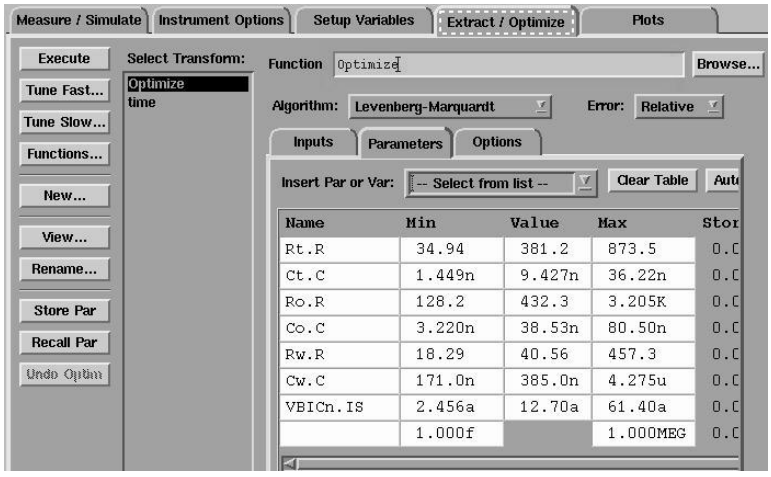
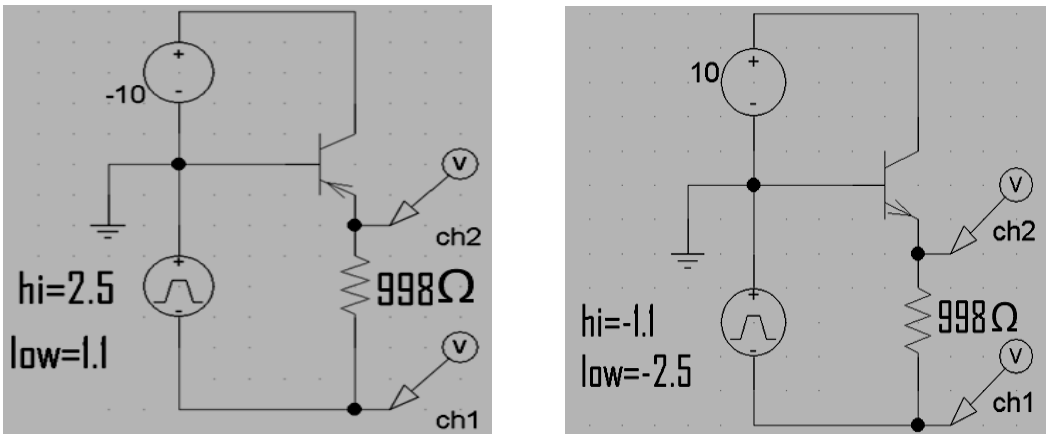


Figure 21: Optimization of thermal network.



a) b)

Figure 22a): Test bench for npn devices for UTA204 and UTA205 b): Test bench for pnp devices for UTA204 and UTA205

Time domain measurements were obtained from the UTA 204 and the UTA 205 chips. The circuit setup is shown in Figures 22 a) and 22 b). The pin-out of the UTA 204 and the UTA 205 chips are shown in Appendix C.

2.8 Discussion of the time domain measurements result from UTA 204 and UTA 205

In this section the time domain measurement results are presented. The overall purpose is to obtain a single time constant (1-pole) thermal circuit. The thermal circuit in VBIC model is not accurate enough to give an accurate simulation result. First optimization is done for the circuit shown in Figure 2.10. After obtaining the first set of C_t, R_t,C_w,R_w,C_o and R_o values, the 3-pole thermal circuit is converted to a 2-pole thermal circuit. This is done by forcing the C_t and R_t values. The 2-pole thermal model is approximately converted to a 1-pole circuit. Force approximation means that the resistors values are sum and fixed, and the capacitor value is optimized to fit the measured data. This process of approximation is named force conversion, since, optimization is done by fixing the R_{th} value to a constant. The forcing prodecure is divided into seven parts and are described below.

1. Do optimizationing to obtain C_t, R_t,C_w,R_w,$C_o$and R_o. Suppose the values are as shown

$C_t = C_{t1}$
$R_t = R_{t1}$
$C_w = C_{w1}$
$R_w = R_{w1}$
$C_o = C_{o1}$
$R_o = R_{o1}$

2. Optimize again, but for a 2-pole circuit, by only varying C_w and modifying $R_w = R_{w1} + R_{o1}$

$C_t = C_{t1}$
$R_t = R_{t1}$
$C_w = C_{w2}$
$R_w = R_{w1} + R_{o1}$
$C_o = 0$
$R_o = 0$

3. Optimize again for a 2- pole circuit, by only varying R_w

$C_t = C_{t1}$
$R_t = R_{t1}$
$C_w = C_{w2}$
$R_w = R_{w2}$
$C_o = 0$
$R_o = 0$

4. Optimize again for a 2 pole circuit, by only varying C_t

$C_t = C_{t2}$
$R_t = R_{t1}$
$C_w = C_{w2}$
$R_w = R_{w2}$
$C_o = 0$
$R_o = 0$

5. Optimize again for a 2 pole circuit, by only varying R_t

$C_t = C_{t2}$
$R_t = R_{t2}$
$C_w = C_{w2}$
$R_w = R_{w2}$
$C_o = 0$
$R_o = 0$

6. Optimize again for a single pole circuit, by only varying C_t and modifying $R_t = R_{t2} + R_{w2}$

$C_t = C_{t3}$
$R_t = R_{t2} + R_{w2}$
$C_w = 0$
$R_w = 0$
$C_o = 0$
$R_o = 0$

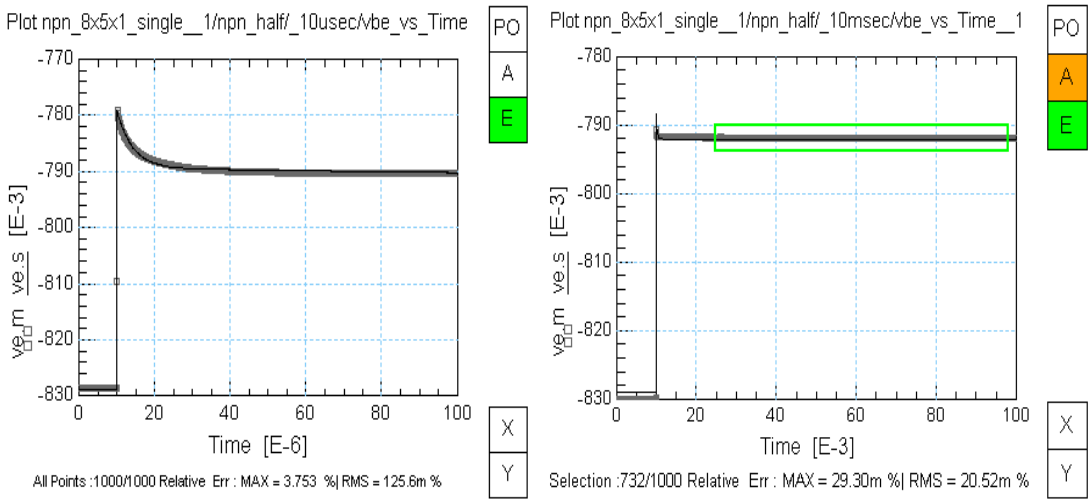
7. Optimize again for a single pole circuit, by only varying R_t

$C_t = C_{t3}$
$R_t = R_{t3}$
$C_w = 0$
$R_w = 0$
$C_o = 0$
$R_o = 0$

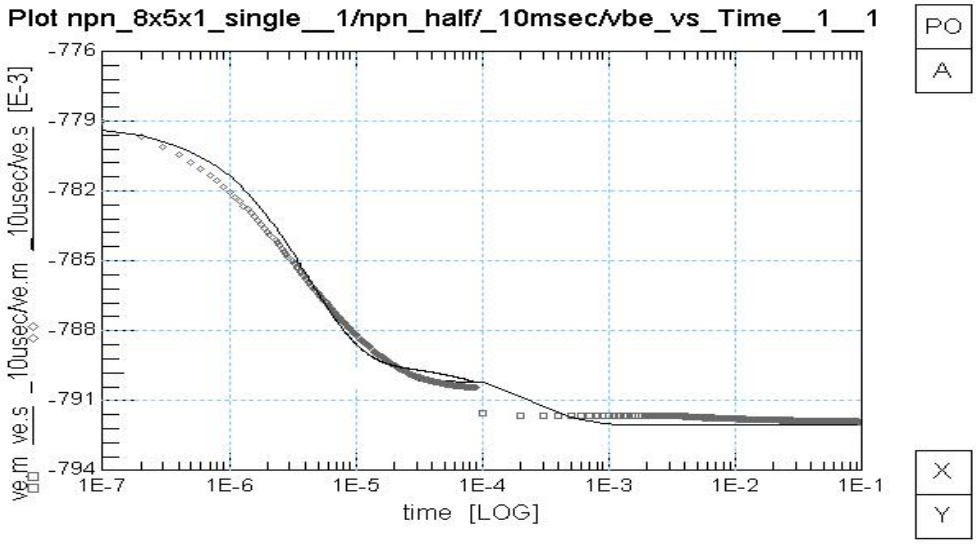
Part 1 has a 3-pole structure. Part 2 through Part 5 describes how to approximate a 3-pole structure to a 2-pole structure. Lastly, Part 6 and Part 7 shows how to approximate a 2-pole structure to a single pole structure.

Conversion approximation of a 2-pole to 1-pole circuit, using the mathematical approach, has been discussed in the previous section. This same approach has been applied to convert a 3-pole to a 2-pole circuit and then the 2-pole is converted to 1-pole circuit.

The forced approximation result and the mathematical result has been compared. The following results were obtained by measurement of a 0.5 and a 1 micron trench oxide thickness npn and pnp DIBJT. A 3-pole model and a 2-pole model were used to fit the measured response first. Then the 3-pole and the 2-pole model were approximated to a 1-pole model by using the mathematical approach.



a) b)

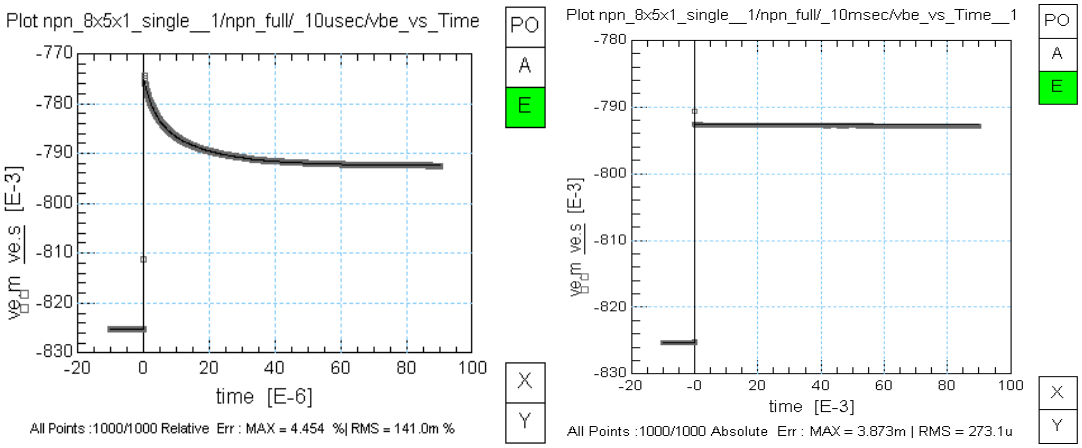


c)

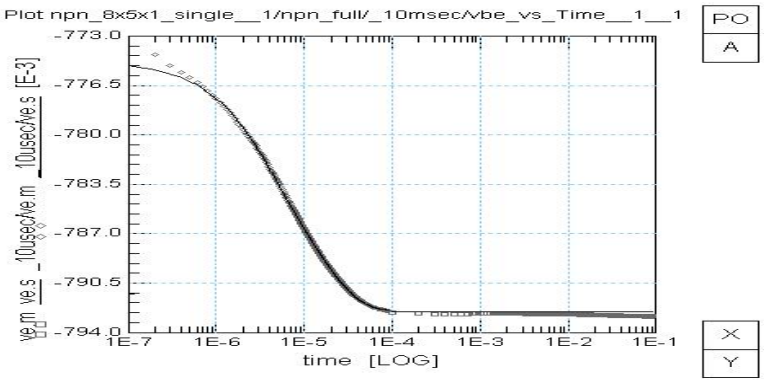
Figure 23: 1-pole simulation and measured result of 0.5 micron trench isolated npn DIBJT for a) 100 microsecond data and simulation in linear time scale b) 100 millisecond data simulation in linear time scale c) Data and simulation collected in Log time scale.

Figure 23 represents the measured results with the optimized simulation results of a 0.5 micron trench isolated npn device. The dotted lines are the data collected and the solid line is the simulated result. The data was collected for a short time range as well as a long time range. The data for the short time range determines the C_{Th} values and the data for the long time

range defines R_{Th} values. In Figure 23 a) 1000 data points were collected for a time range of 100 micro seconds and in Figure 23 b), 1000 data points were collected for time range of 20 milliseconds. The short time range data also helps to examine the device behavior when there would be sudden change in voltage. The long time range provides the settling time of the data. Figure 23 c) represents both the short time and long time data in a Log time scale. The dotted lines are the data and the solid lines are simulated results. The absolute error percentage for the simulated result to its measured is less than 4% as represented in Figure 23 a) and b). The box in Figure 23 b) represents the absolute error within the area of the box.



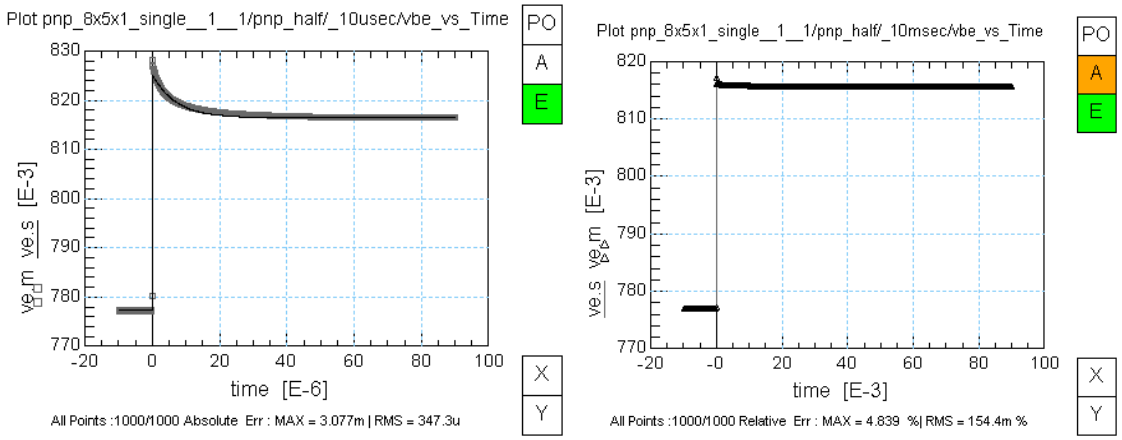
a) b)



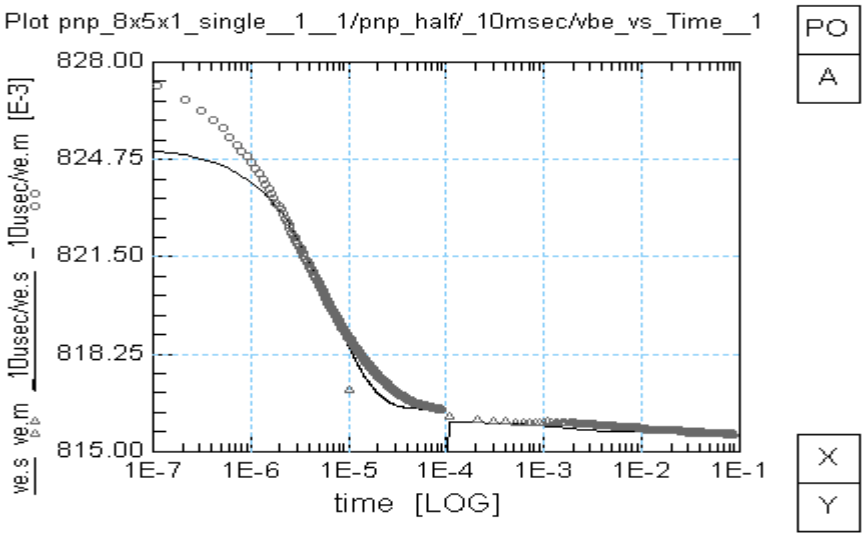
c)

Figure 24: 1-pole simulation and measured result of 1 micron trench isolated npn DIBJT. a) 100 microsecond data and simulation in linear time scale b) 100 millisecond data simulation in linear time scale c) Data and simulation collected in Log time scale.

Same procedure was followed for 1-micron trench isolated npn device. The measured and simulated results of 1000 data points in a time range of 100 micro seconds is represented in Figure 24 a) and 1000 data points in a time range of 100 milliseconds is represented in Figure 24 b). Figure 24 c) represents both the short time and long time data in a Log time scale. The absolute error percentage of the simulated result to data from was less than 5%.



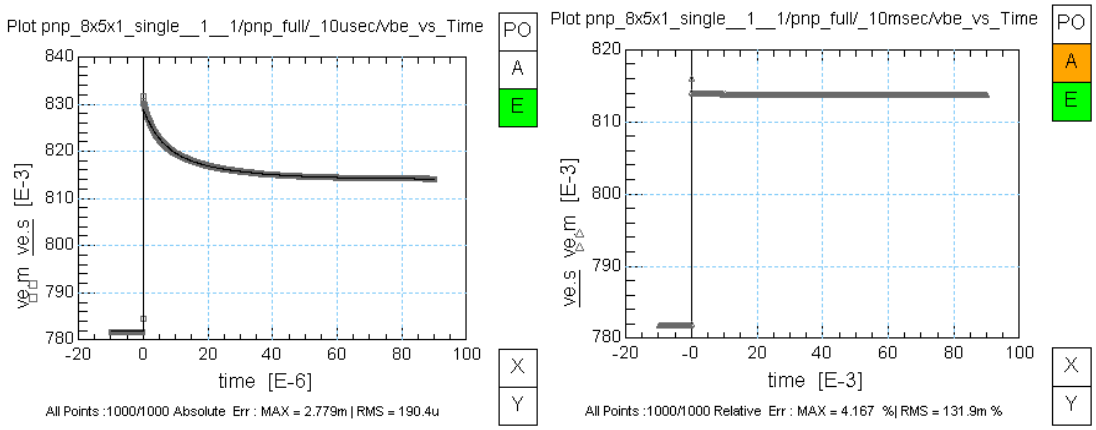
a) b)



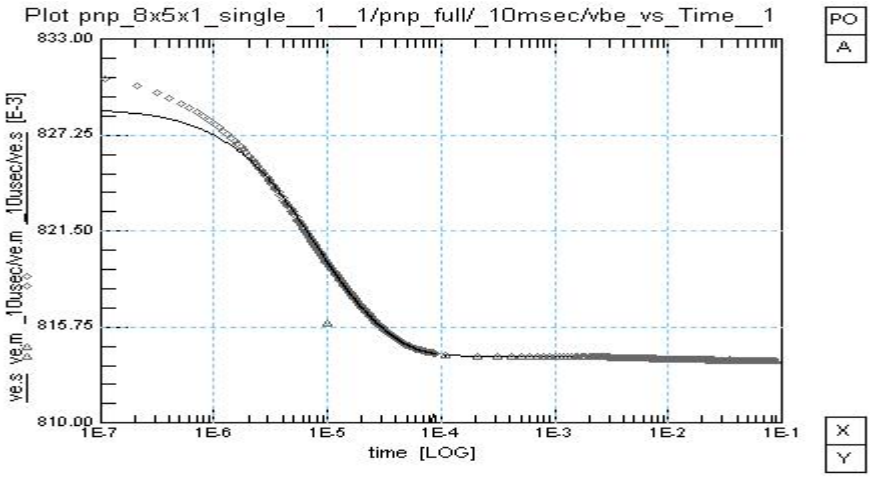
c)

Figure 25: 1-pole simulation and measured result of 0.5 micron trench isolated pnp DIBJT. a) 100 microsecond data and simulation in linear time scale b) 100 millisecond data simulation in linear time scale c) Data and simulation collected in Log time scale.

Figure 25 represents the measurement results with the optimized simulation results for a 0.5 micron trench oxide thickness pnp DIBJT. In Figure 25 a) 1000 data points were collected for a time range of 100 micro seconds. In Figure 25 b), 1000 data points were collected for time range of 100 milliseconds. Figure 25 c) represents both the short time and long time data in a Log time scale. The maximum absolute error of these measurements compared to simulated results were also less than 5%, represented in Figure 25 a) and b).



a) b)



c)

Figure 26: 1-pole simulation and measured result of 1 micron trench isolated pnp DIBJT. 1-pole simulation and measured result of 0.5 micron trench isolated pnp DIBJT. a)100 microsecond data and simulation in linear time scale b) 100 millisecond data simulation in linear time scale c) Data and simulation collected in Log time scale.

Figure 26 represents the measurement results with the optimized simulation results for 1 micron trench oxide thickness pnp DIBJT. In Figure 26 a) 1000 data points were collected for a time range of 100 micro seconds. In Figure 26 b), 1000 data points were collected for time range of 100 milliseconds. Figure 26 c) represents both the short time and long time data in a Log time scale. The maximum absolute error of these measurements compared to simulated results were also less than 5%, represented in Figure 26 a) and b).

2.9: Summary of the measured results

The Rth and Cth measurements for 8x5x1 npn and pnp devices obtained from Figure 23-26 are summarized below.

Table 2: Three pole model circuit results for a single 0.5 micron trench oxide thickness pnp device.

Ro(K/W)	124.8
Rw(K/W)	13.31
Rt(K/W)	302.1
Rth(K/W)	**440.21**
Co(W/K)	188.1n
Cw(W/K)	150.2u
Ct(W/K)	8.321n
Cth(W/K)	**8.126n**
Tau(sec)	
VBICp.IS (Amp)	**24.5a**

Table 3: Three pole model circuit results for a single 1 micron trench oxide thickness pnp device.

3-pole model		2-pole model	
Ro(K/W)	92.57	Rt(K/W)	657.6
Rw(K/W)	14.23	Ro(K/W)	71.12
Rt(K/W)	383.8	Rth(K/W)	**728.72**
Rth(K/W)	**494.5**	Ct(W/K)	13.65n
Co(W/K)	250n	Co(W/K)	126.9n
Cw(W/K)	172u	Cth(W/K)	**.1232n**
Ct(W/K)	7.281n		
Cth(W/K)	7.342n		
VBICp.IS(Amp)	24.15a	VBICp.IS(Amp)	**26.4a**

Table 4: Three pole model circuit results for a single 0.5 micron trench oxide thickness npn devices.

3-pole model		2-pole model	
Ro(K/W)	428.2	Rt(K/W)	181.9
Rw(K/W)	94.58	Ro(K/W)	379.3
Rt(K/W)	170.2	Rth(K/W)	**561.2**
Rth(K/W)	732.98		
Co(W/K)	7.238n	Ct(W/K)	912.1f
Cw(W/K)	27.49u	Co(W/K)	22.27n
Ct(W/K)	5.993p	Cth(W/K)	**.912f**
Cth(W/K)	5.9p		
VBICn.IS(Amp)	13.73a	VBICn.IS(Amp)	**14.8a**

Table 5: Three pole model circuit results for a single 1 micron trench oxide thickness npn device.

3-pole model		2-pole model	
Ro(K/W)	473.4	Rt(K/W)	382.4
Rw(K/W)	63.32	Ro(K/W)	471.5
Rt(K/W)	334.9	Rth(K/W)	**853.3**
Rth	891.62	Ct(W/K)	9.432n
Co(W/K)	27.39n	Co(W/K)	35.20n
Cw(W/K)	1.323u	Cth(W/K)	**7.44n**
t(W/K)	9.430n	Tau(sec)	6.348u
Cth(W/K)	7.051n		
VBICn.IS(Amp)	12.28a	VBICn.IS(Amp)	**12.65a**

Table 6: Summary of all the results after converting to a one pole model.

Single npn 0.5 micron device	
Rth(K/W)	**534.3**
VBICn.IS(Amp)	**15,12a**
Cth(W/K)	**3.03n**
Tau(sec)	**1.619u**
Single npn 1 micron device	
Rth(K/W)	**842.3**
VBICn.IS(Amp)	**12.65a**
Cth(W/K)	**7.76n**
Tau(sec)	**6.53u**
Single pnp 0.5 micron device	
Rth(K/W)	**456.3**
VBICp.IS(Amp)	**23.15a**
Cth(W/K)	**9.02n**
Tau(sec)	**4.115u**
Single pnp 1 micron device	
Rth(K/W)	**712.3**
VBICp.IS(Amp)	**22.1a**
Cth(W/K)	**4.12n**
Tau(sec)	**2.095u**

2.10 Conclusion

From the measured and simulated result presented above, it can be concluded that the results obtained for the simulated 1-pole model has a percentage error of less than 5 percent when compared to the measured results. The value obtained is also very close to the VBIC parameter model. Using the new thermal parameters as represesnted in Table 6, gives better simulation results than the standard VBIC model provided [13].

CHAPTER 3

ADJACENT HEATING DEVICES

The adjacent heating effects are examined in this Chapter of the thesis work. In previous chapter, the effects of self heating have been analyzed and discussed. In this chapter, the effect of a heated device on its surrounding devices has been measured and simulated. A coupling R_{Th} and C_{Th} have been found for each of the adjacent devices.

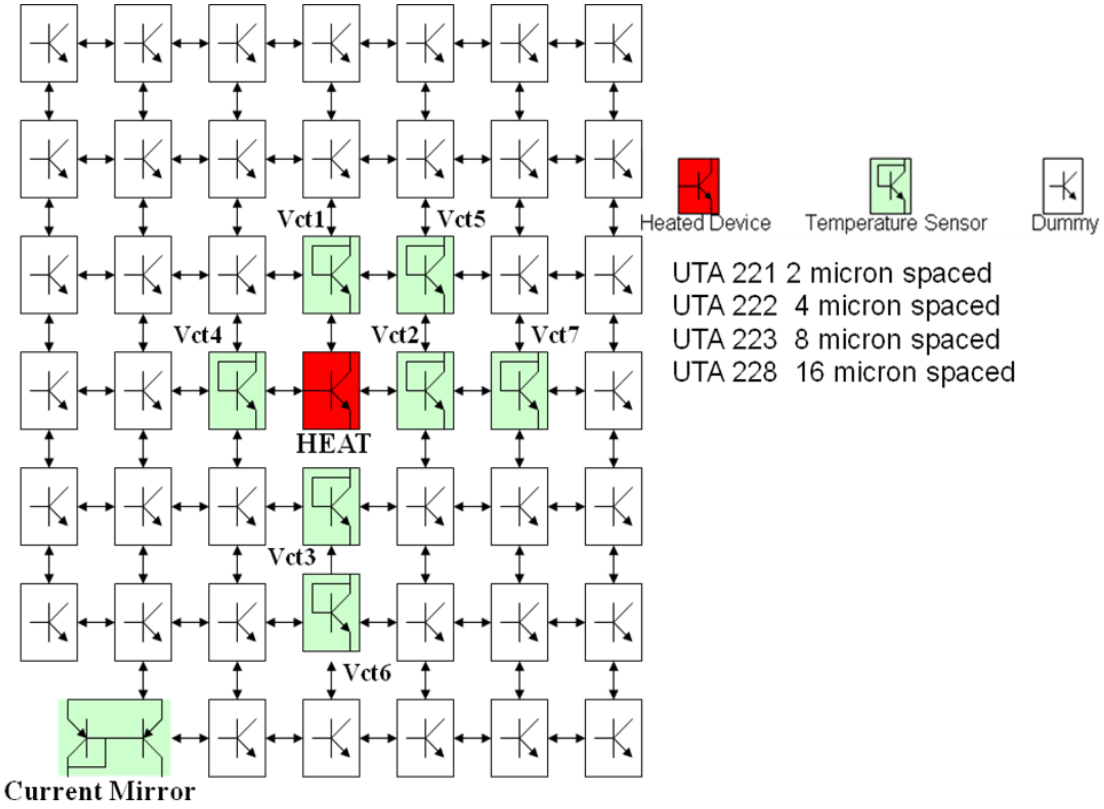


Figure 27: Layout to measure adjacent device heating.

UTA 221,222,223 and 228 are chips designed with different spacing between the transistors. The device in the middle is the heated device, surrounded by Vct1-Vct7, which are used as temperature sensors. They are used to detect any temperature change caused by the power dissipated in the heated device. The dissipated heat can affect the adjacent devices and

can increase the thermal impedance of the adjacent devices. This coupled thermal resistance can be calculated and it can be modeled in the simulation.

3.1 Experimental Setup of the adjacent heating measurements

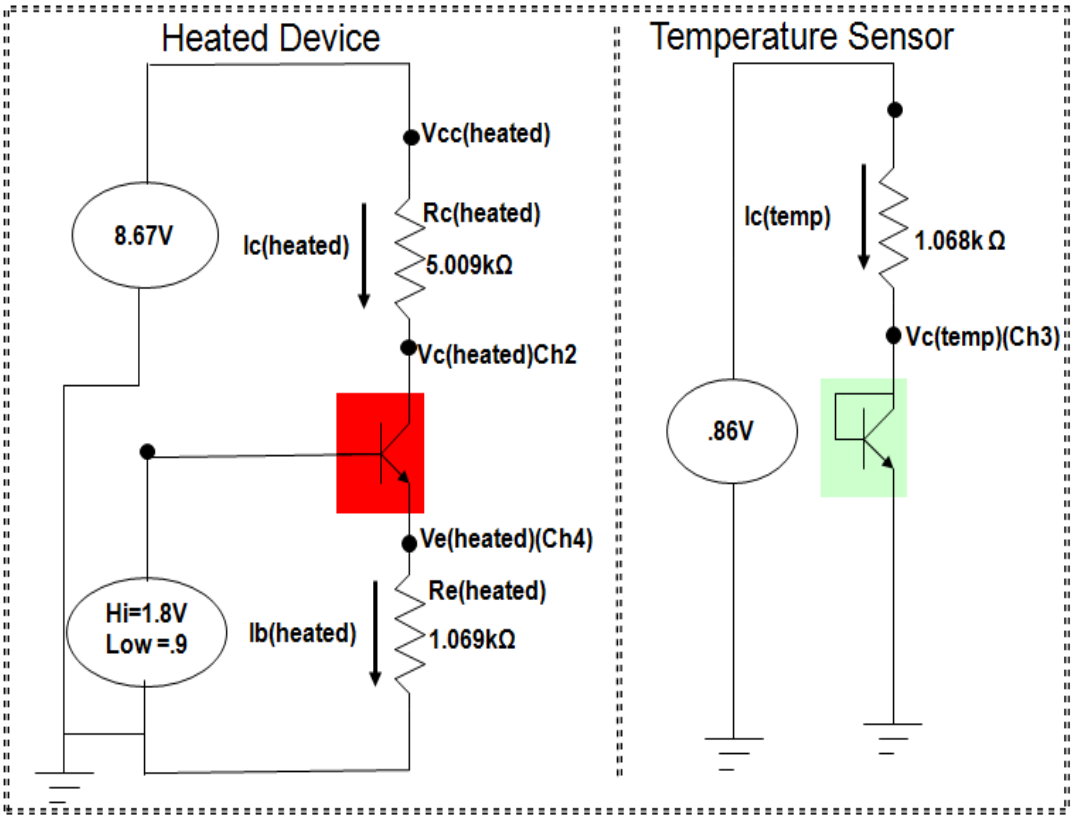


Figure 28: Experimental setup for the adjacent heating device.

Using the setup from Figure 28 and the mathematical approximation from Chapter 2 the coupling R_{th} and C_{th} has been calculated. A square wave of Hi=1.8V and Low 0.9V is used to bias the heated device. A constant bias voltage of 0.86V is used at the temperature sensor. As the square wave goes from Hi to Low and Low to Hi, the power dissipated at the heated device affects the temperature sensor. The coupled thermal resistance can be calculated from

$$R_{Th\ coupled} = \left(\frac{\partial V_{BE}}{\partial T}\right) \times \left(\frac{\partial P_{DISS}}{\partial V_{BE}}\right) \qquad 3.1$$

The difference in temperature can be calculated using equation in 2.23.The changes in ∂V_{BE} and ∂P_{DISS} are measured across the temperature sensor assuming the temperature of the temperature sensor itself remains constant. The ratio of ∂V_{BE} to ∂T is measured from the respective temperature sensor before the adjacent measurement is done. The coupling R_{th} as a fraction of the internal R_{th} of the heated device is represented below. Using the equation represented in equation 3.1, the adjacent heating was calculated. This was done in the time domain and results represented in Figure 29 are in faction of the total thermal impedance of the single heated device. Vct1-Vct5 are the temperature sensors and spacing between devices are labeled respectively.

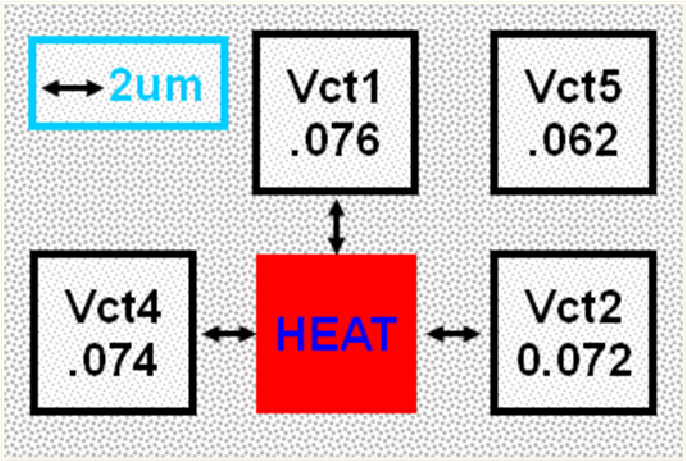


Figure 29: Adjacent heating effect for 2 micron spacing between devices as a percentage of its thermal resistance.

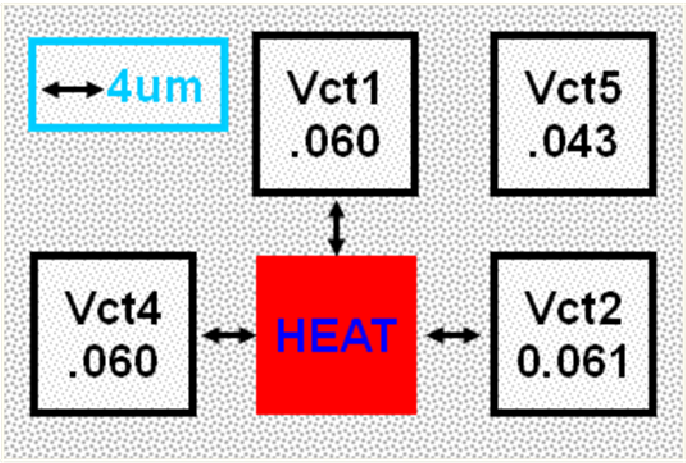


Figure 30: Adjacent heating effect for 4 micron spacing between devices as a percentage of its thermal resistance.

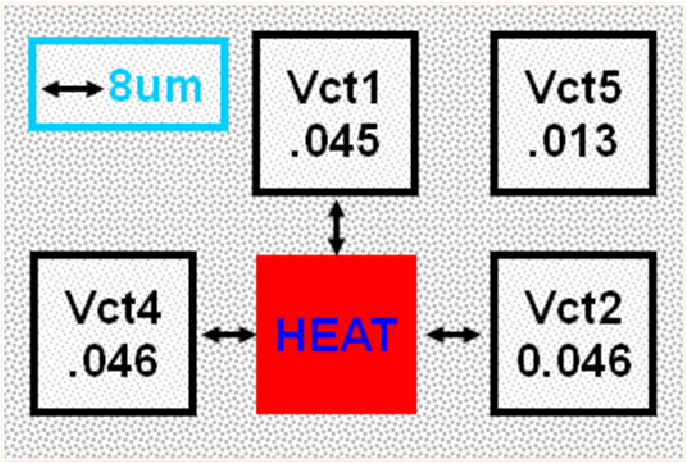


Figure 31: Adjacent heating effect for 8 micron spacing between devices as a percentage of its thermal resistance.

3.2 Conclusion

Results from UTA 208 which has16 micron spacing between devices was not presented because the data obtained were not consistent enough when compared to simulation. The result obtained from UTA 201,202 and 203 have been consistent and a model with the couple impedance can be created. Compared to values for the thermal resistance, the couple thermal resistance is less than five percent of the total thermal resistance. So it can be concluded that adjacent heating has negligible influence on the heating aspect of the devices.

CHAPTER 4

CONCLUSION AND RECOMMENDATION

The main objective of this thesis work has been to accurately model the thermal circuit for a DIBJT. The ability to predict the thermal impedance of these devices is imperative for new designs. Self-heating of devices is known to strongly affect device performance. The most severe self-heating effect in DIBJT is the so-called thermal runaway effect, which may lead to catastrophic failure of the devices. Thermal runaway in a DIBJT is caused by a positive feedback mechanism when the dissipated power causes the temperature to increase the emitter-base junction injects more current which causes additional heating, and so on. The critical current at which the thermal runaway starts is dependent of the thermal resistance, which is the ratio of the temperature increase of the junction to the power dissipated. By integrating an emitter ballast resistance the critical current is increased and thermal runaway can be avoided. In the case of BJTs on SOI material, with silicon dioxide as the buried insulator, the thermal resistance is obviously increased. Consequently a larger value of the emitter ballast resistor is required to maintain thermal stability of the device. However, an additional emitter resistance will limit the device performance, such as power gain and cut-off frequency.

4.1 Conclusion

When designing SOI devices one has to consider the thermal effects, especially for high voltage circuits where severe overload conditions can occur. Simulations and measurements of a high voltage SOI bipolar transistor with thick buried insulator show that thermal runaway occurs due to self-heating of the device, because of the low heat conductivity of the buried silicon dioxide.

Based on the time domain measurement and mathematical analysis of DIBJTs, a compact thermal model was implemented to achieve the self heating effects of these devices. The compact thermal model was calibrated from numerical simulation results and compared with these devices measurements. The model offers an efficient alternative to numerical simulations.

The Cadence custom IC design tools and ICCAP were used for measurement and analysis of the devices provided by National Semiconductor Corporation. The Vertical Bipolar Inter Company (VBIC) model, used for characterization of these devices, has a single pole thermal network in its model file. Measurement, analysis and characterization have been done on the devices provided, to optimize better thermal parameter values of the devices. The thermal parameters that were measured and calculated in this thesis, were thermal resistance and thermal capacitance. The thermal resistance is within 5% when compared to the original parameter values provided by National Semiconductor. This thesis provides a more accurate thermal capacitance model which has been calculated for the devices provided.

4.2 Recommendations for future work

The thermal model for the adjacent devices can be explored. The technique used in this thesis also can be used for upcoming technologies like silicon germanium devices. It is also suggested that the thermal model can also have an inductor attached which could take into account the electric field change that could occur when there is a rise in temperature. New technique for extracting the self heating parameter with time delay is developed [14]. Implementation this new approach would provide more accurate time domain estimation.

APPENDIX A

ADDING OF dT NODE TO SPECTRE

In this Section the procedure to add the dT and tl node to Spectre has been has been described.

Adding of the thermal pin in spectreS.

1. Copy the NPN cell-view to your new library.

2. Open the 'Symbol' of the copied NPN
   Add pins 'dt', 'tl' and 'S'.
   - Direction -> 'input-output', type-> 'square'

   b. Add label cdsTerm("dt"), cdsTerm("tl") and cdsTerm("C")
   c. Save

3. Next go to [Design - > Create Cellview From Pin List] and specify the IO pins 'C B E S dt tl', change the view name to 'spectreS' and choose the Tool/Data Type to 'Composer Symbol'. Then click on Ok.
4. Next go to [Design -> Create Cellview From Cellview].
   a. Specify view name -> spectreS
   b. View name -> spectreS
   c. Tool/Data type – 'Composer Symbol'
   A modify/replace window should pop up and check on modify.
   The SpectreS window should pop up and it would contain the additional pins.
   Save
5. Go to Tools at the icfb window menu and open up CDF and click on edit.
   a. CDF type -> base
   b. Add the appropriate library and cell name of the copied npn
   c. Go to the simulation into field and click edit
      i. Choose simulator to be 'spectreS'
      ii. Change the 'termOrder' field to 'C B E S dt tl'
      iii. netlistProcedure -> 'ansSpectreSDevPrim'
      iv. prefix -> 'Q'
   d. Go to the Overall Component Parameter section
      i. modelType – VBIC
      ii. Choose file name example ' N15W0402A1'
      iii. Change the simModel to appropriate name example
      ' N15W0402A1VH' (for vbic models the file should end with VH)
   e. Click on OK

APPENDIX B

APPROXIMATION OF 2-POLE MODEL TO 1-EMEMENT MODEL

This section provides the MATLAB code that is used to convert the 2-pole model to 1-pole model.

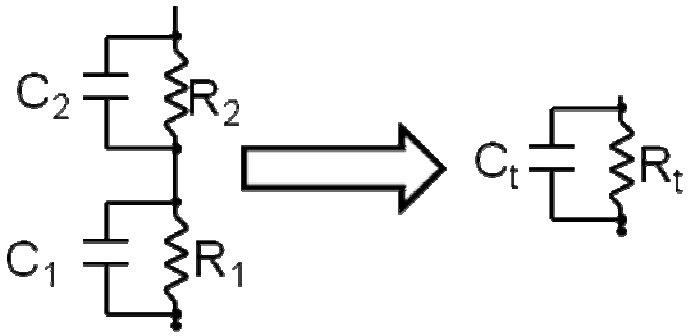


Figure B.1: Approximaiton of 2-pole model to 1-pole.

The Two pole model has to be

$$Z_t(s) = Z_1(s) + Z_2(s) = \frac{R_1}{1 + sR_1C_1} + \frac{R_2}{1 + sR_2C_2}$$

$$Z_{Th} = \frac{(R_1 + R_2)[1 + s\dfrac{C_1R_1R_2 + C_2R_1R_2}{R_1 + R_2}]}{(1 + sR_1C_1)(1 + sR_2C_2)}$$

The One pole model is

$$Z_{Th} = \frac{R_{Th}}{1 + sR_{Th}C_{Th}}$$

$$\left(\frac{d\,20[LogR\ ]}{d\,\omega}\right) = 20$$

$$\Rightarrow \frac{20[Log\ (R_1 + R_2) - Log\ (R_2)]}{Log\ \omega_2 - Log\ \omega_z} = 20$$

$$\Rightarrow Log\ \omega_2 - Log\ \omega_z = Log\ (R_1 + R_2) - Log\ (R_2)$$

$$\omega_z = \frac{R_2 * C_2 * R_2}{R_1 + R_2}$$

```
%MATLAB Conversion of two pole RC circuit to one pole
wmin=1;
wmax=10000000000000;
```

```
w=logspace(log10(wmin),log10(wmax));
%THE 2-pole circuit poles
R1=300;
R2=700;
C1=1*10^-9;
C2=1*10^-6;
%Definiting the dc values, Poles and Zeros
K=R1+R2;
z=1/((R1*C1*R2+R2*C2*R1)./R1+R2);
p1=1/(R1*C1);
p2=1/(R2*C2);
%The representation for the 2-pole circuit
for k=1:length(w)
   ZTH(k)=(R1./(1+j*w(k)/p1))+(R2/(1+j*w(k)/p2));
   mag(k)=abs(ZTH(k));
   phase(k)=angle(ZTH(k));
end
%The conversion of 2-pole to one pole
for k=1:length(w)
   if (log10(R1+R2)< log10((R1+R2)/2)<log10(R2))
   pz=p1;
   elseif (log10(R2)> log10((R1+R2)/2)>0.000001*log10(R2))
        pz = (C2.*R2.*R2)./(R1+R2)
   else
         pz=p2;
   end
   ZTHq(k) = K./(1+j*w(k)/pz);
   magz(k)=abs(ZTHq(k));
   phasez(k)=angle(ZTHq(k));
end
%Values of the single pole model
R3=R1+R2;
C3=R3/pz

subplot(2,2,1), semilogx(w/(2*pi),20*log10(mag))
xlabel('Frequency,Hz'),ylabel('Impedance,dB')
grid
title('2 pole circuit')
subplot(2,2,2), semilogx(w/(2*pi),phase)
grid
xlabel('Frequecy,Hx'), ylabel('Phease,deg')
subplot(2,2,3), semilogx(w/(2*pi),20*log10(magz))
grid
xlabel('Frequency,Hz'),ylabel('Impedance,dB')
title('Single pole Circuit')
subplot(2,2,4), semilogx(w/(2*pi),phasez)
xlabel('Frequecy,Hx'), ylabel('Phease,deg')
grid
```

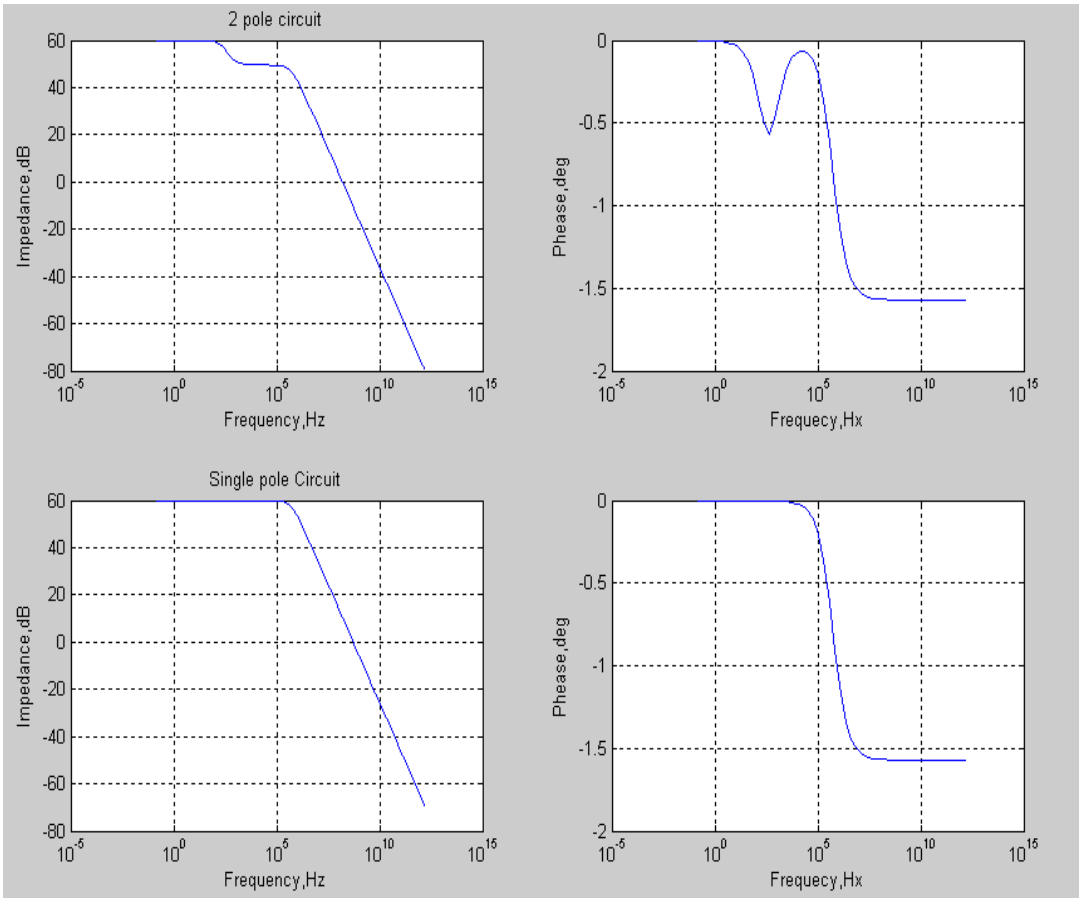


Figure B.2: MathLAB simulation for the approximation of 2-pole to 1-pole network.

APPENDIX C

LAYOUT OF EAGLE 23

In this Section the layout and circuit for adjacent heating devices is represented. Figure C.1 represents the arrangement of the devices in UTA 221,222,223 and 228.

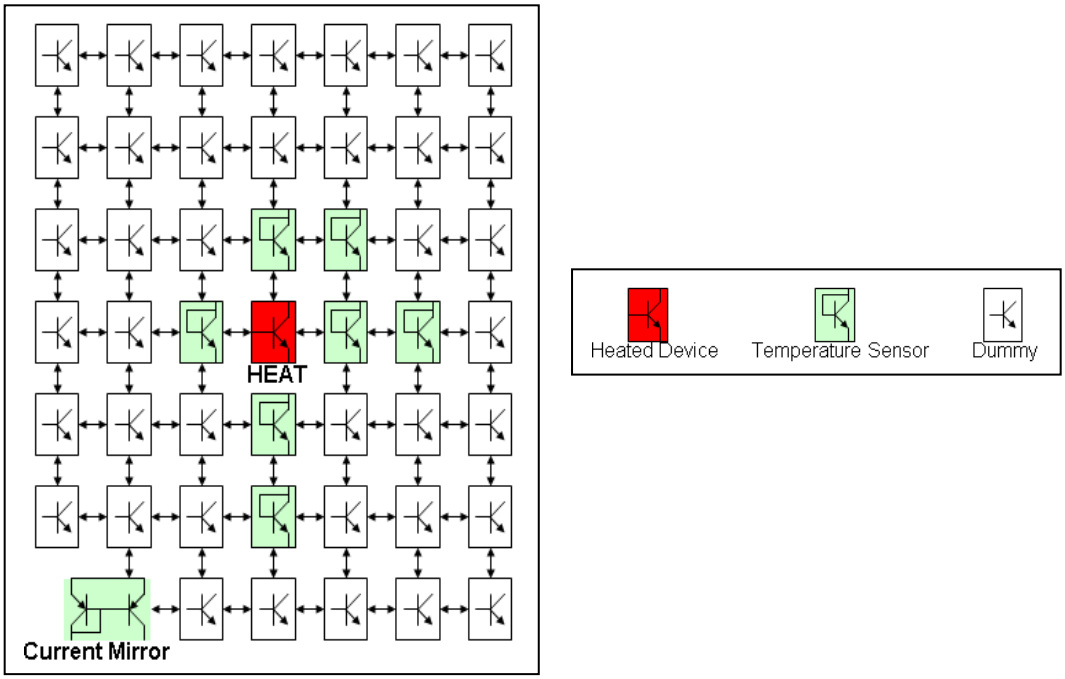


Figure C.1: Schematic for UTA 221,222,223,228.

In Figure C.2, the circuit layout of the UTA 221,222,223 and 228, is represented. Figure C.3-C.6 are the pin-outs of UTA221, 222, 223 and 228 respectively.

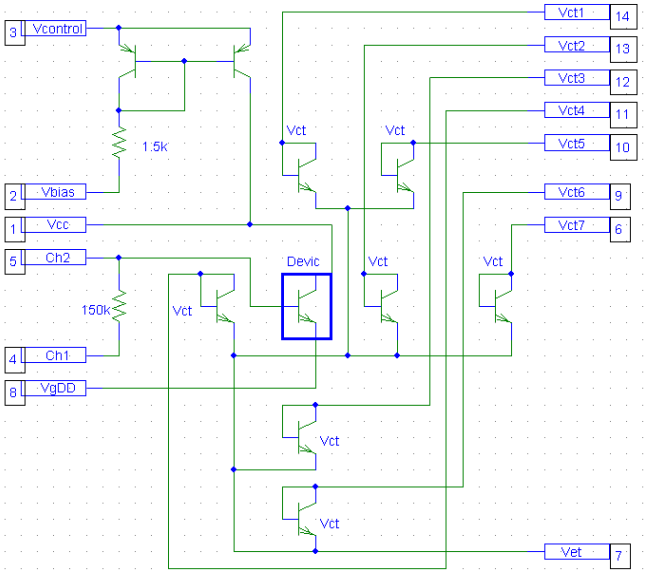


Figure C.2: Closer picture of UTA 221,222,223 and 228.

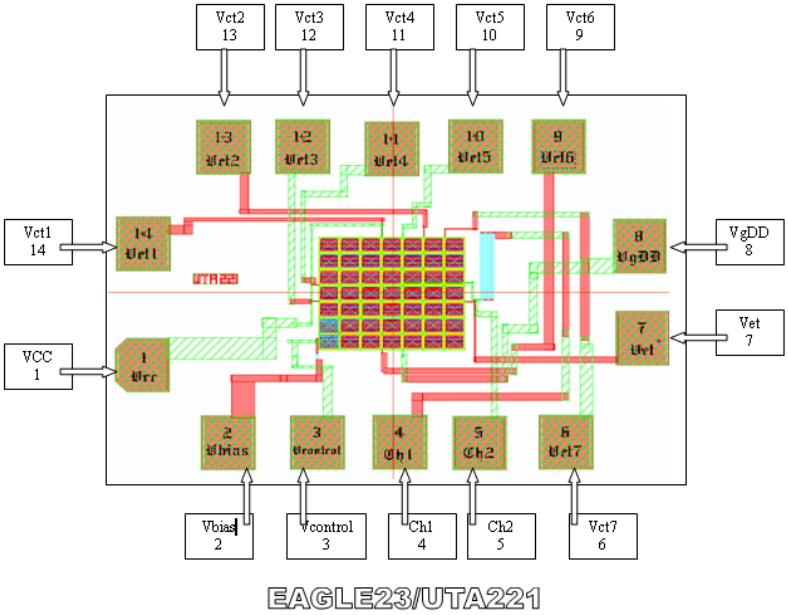


Figure C.3: Pin out for UTA221.

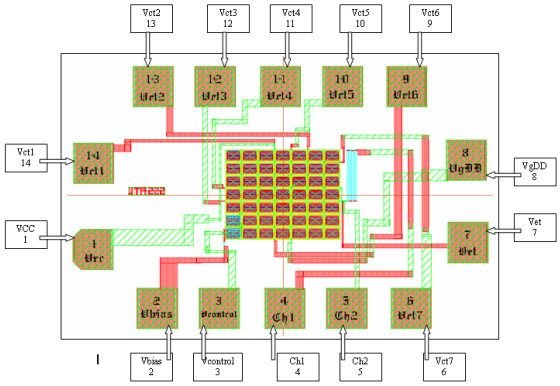


Figure C.4: Pin out for UTA222.

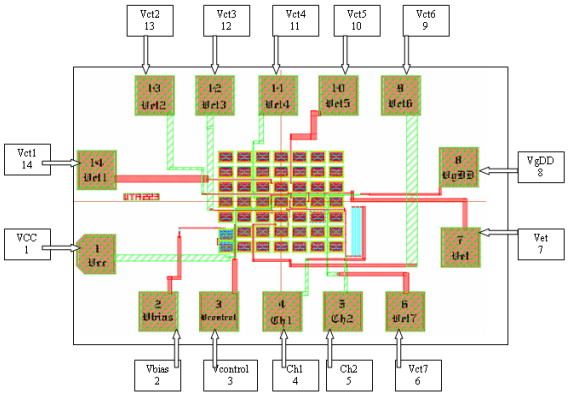
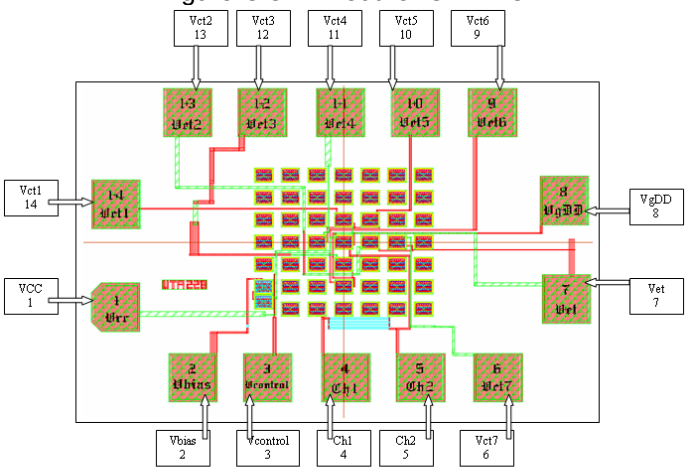


Figure C.5: Pin out for UTA223.



EAGLE23/UTA228

Figure C.6: Pin out for UTA224.

APPENDIX D

LAYOUT FOR UTA 235,236 and 237

The arrangement in Figure D.1 has been designed and fabricated to study the thermal tail current in a current mirror. This designed was used in UTA235, 236 and 237. The distance between each device is 2 micron for UTA 235, 4 micron for UTA236 and 16 micron for UTA 237. Testing and analysis can be done as future work. Figure D.2-D.4 represents the pin-out for UTA235, 236 and 237 respectively.

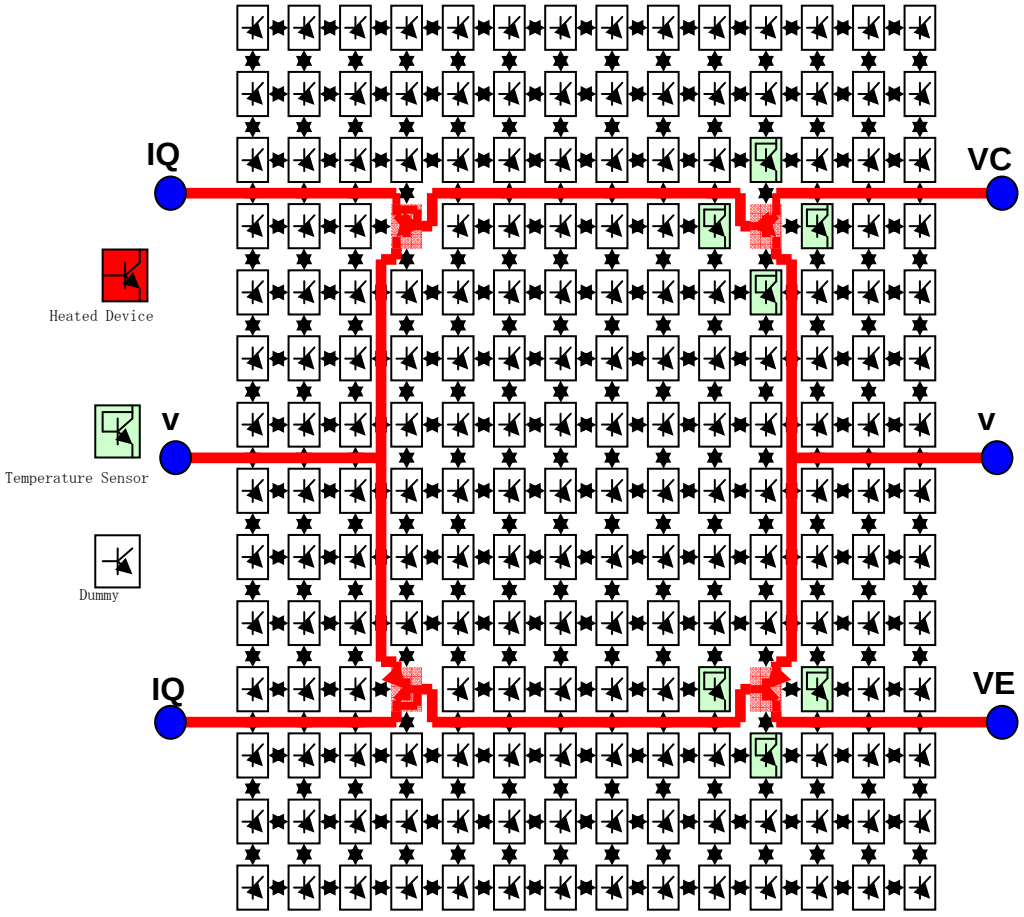


Figure D.1: Circuit layout of UTA 235, 236 and 237.

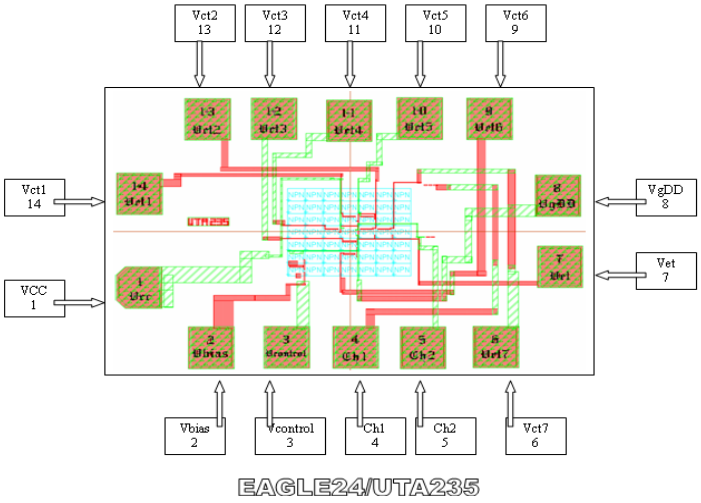


Figure D.2: Pin out for UTA235.

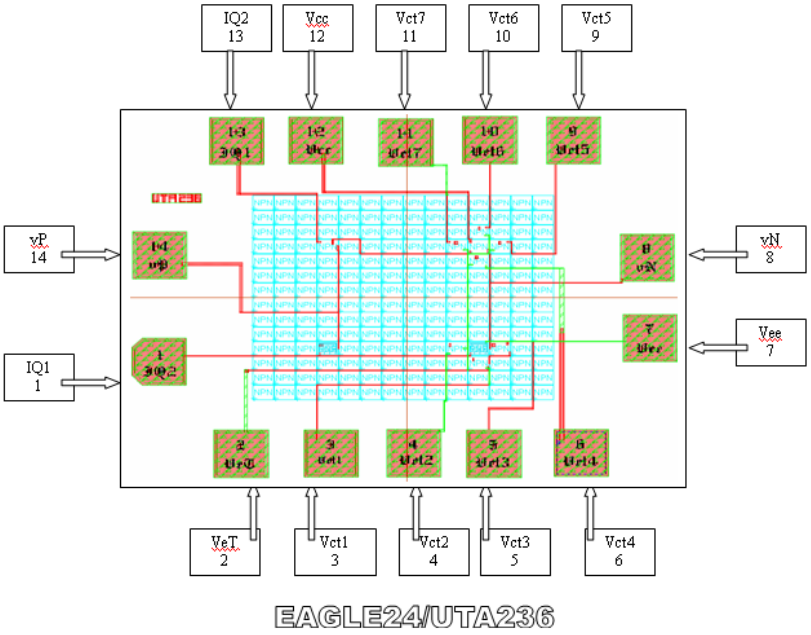


Figure D.3: Pin out for UTA236.

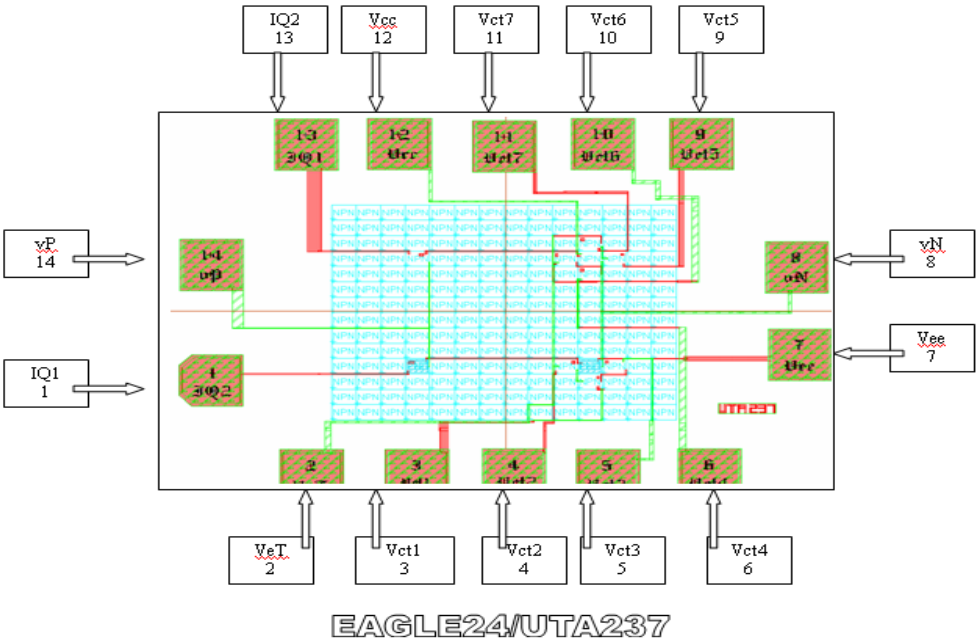


Figure D.4: Pin out for UTA237.

APPENDIX E

LAYOUT OF UTA 246b,c,d AND v

UTA 246b, c, d and v, are special DIBJT devices which had a resistor attached in each individual device. This was done to maintain constant power dissipation in each device. Figure E.1 represents the circuit layout for UTA246b, and c. The spacing between each device is 2 microns for UTA 246b and 4 microns for UTA246c. All the devices in UTAb and c are npn transistors. The same layout is repeated for pnp devices. They are represented in Figure E.2. The pin-out of these devices are in Figure E-3.

UTA 246b,c 2, 4 micron spacing

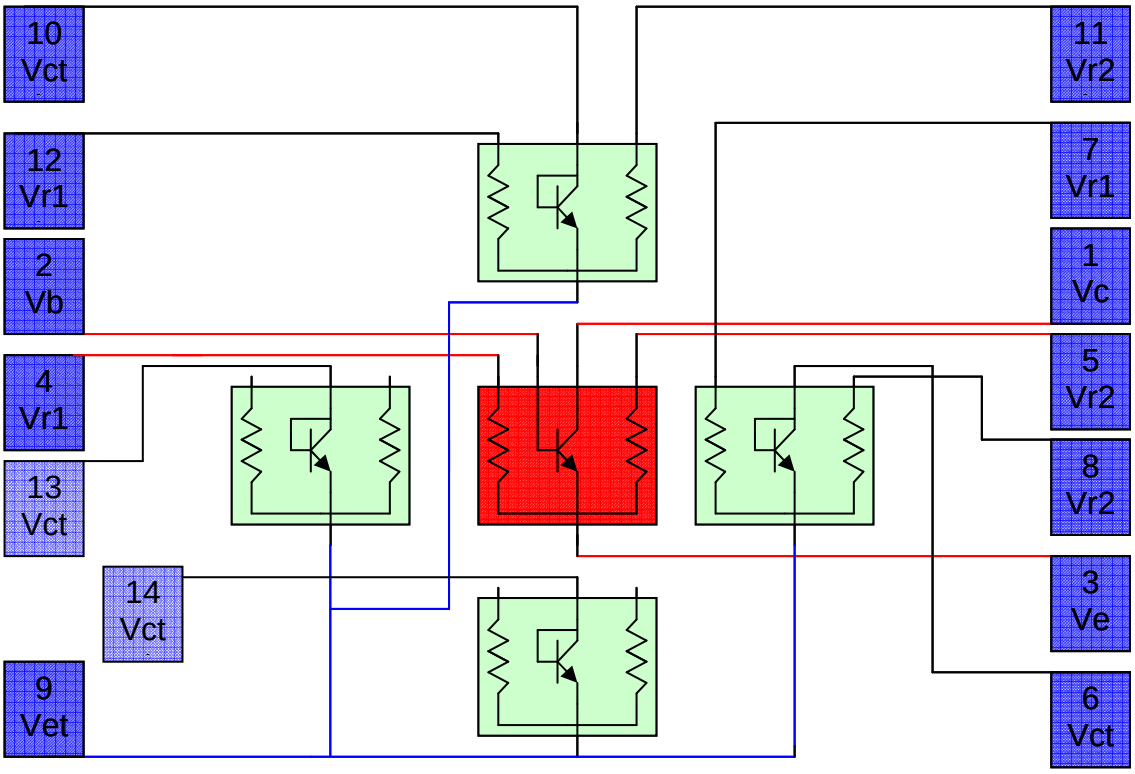


Figure E.1: Setup for UTA246b,c.

UTA 246d,v

2 ,4 micron spacing

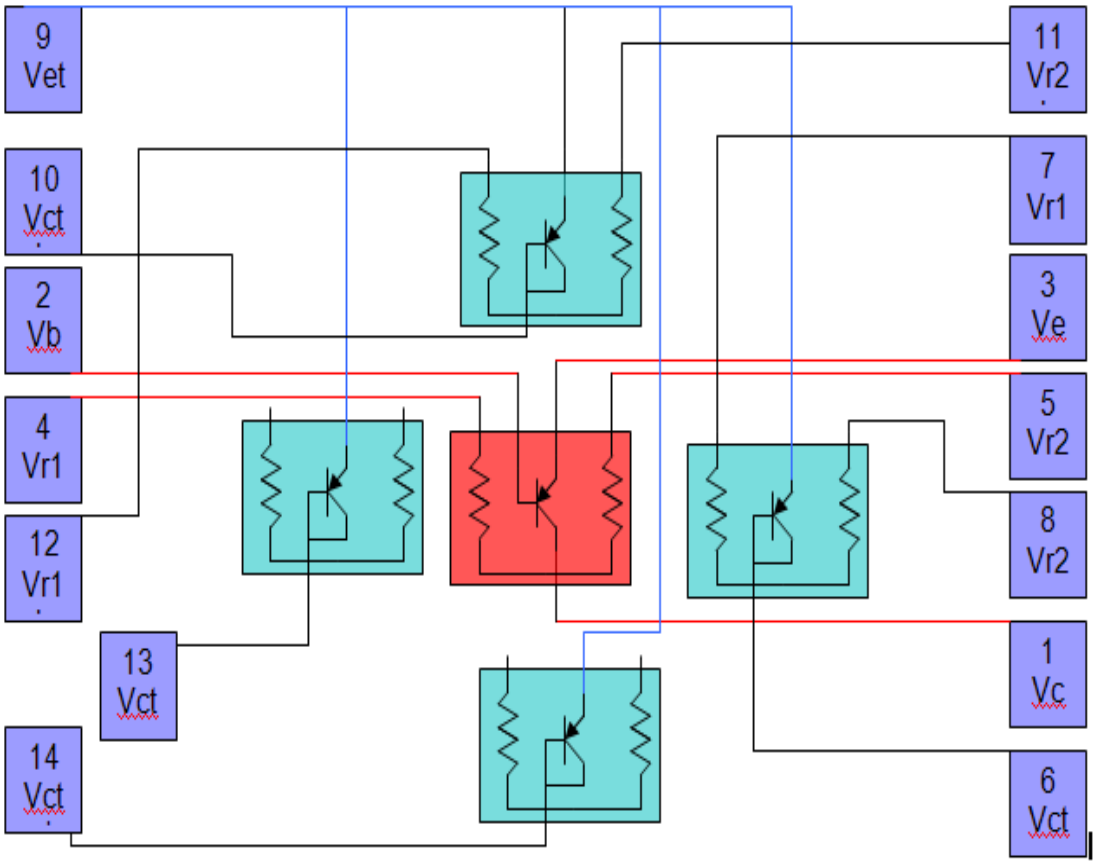


Figure E.2: Setup for UTA246d,v.

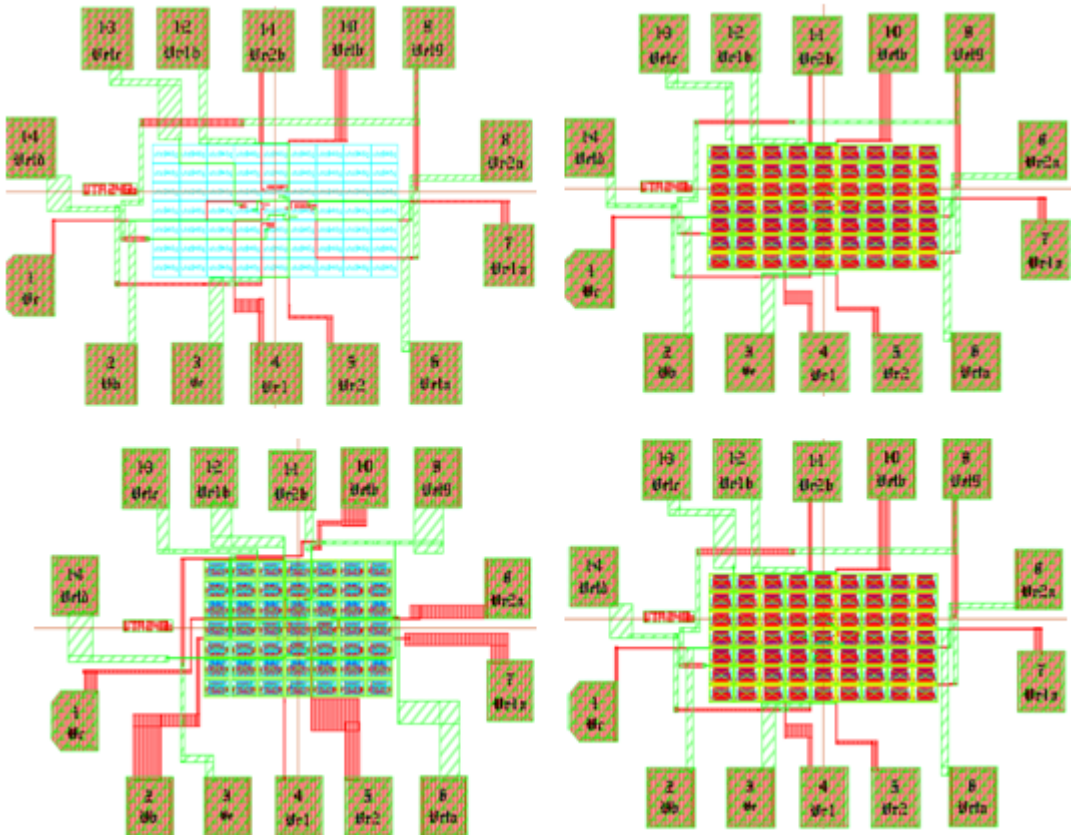


Figure E.3: Setup for UTA 246b,c,d and v.

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BIOGRAPHICAL INFORMATION

Ardasheir Sayek Rahman received his Bachelor of Science degree in Electrical & Electronic Engineering from Michigan Technological University. His undergraduate research was based on the fading effect of monticarlo area scene for mobile vehicles. After finishing his bachelor's degree he started his graduate studies at The University of Texas at Arlington, Texas, United States of America in spring 2006. He started his research in the Analog Integrated Circuits Design Research Laboratory under the guidance of Dr. Ronald L. Carter in 2006. His research interest focuses on the analog circuit design and the thermal effect modeling and characterization. He worked as a graduate research assistant and graduate teaching assistant at UTA from spring 2006 to spring 2008.