RELIABILITY OF ADVANCED DIELECTRICS IN GATE OXIDE AND DEVICE LEVEL

PACKAGING IN MEMS

by

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ABSTRACT

RELIABILITY OF ADVANCED DIELECTRICS IN GATE OXIDE AND DEVICE LEVEL

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The focus of this work is to study the feasibility, reliability and applicability of advanced dielectrics in both Metal Oxide Semiconductor Field Effect Transistor (MOSFET) gate oxide and device level packaging for Microelectromechanical Systems (MEMS). The scaling of silicon based MOSFET is approaching physical limits imposed by atomic structure. This continuous scaling trend of complementary MOSFET technologies introduces new challenges relating to power, heat and device behavior. To overcome the power dissipation and heating problems arising from gate leakage, high dielectric constant (high-k) materials are proposed. Hafnium based high-k dielectric layers and metal gate electrodes have been extensively investigated as alternative gate materials. Successful incorporation of these materials into the MOSFET gate stack with minimum feature size of 45nm has recently been reported.

Here, the low frequency noise characteristics of MOSFETs with differently nitrided HfSiO gate dielectric materials are studied. To evaluate the high-k MOSFET performance using low frequency noise as a characterization tool, the devices were also subjected to different stress induced degradation. Device performance of differently nitrided samples is also compared with

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the control, pure HfSiO MOSFET sample. This work reports, for the first time, the low frequency noise performance of 2nm high-k gate dielectric material for the sub 45nm technology node.

The advantages of the MEMS packaging approach described here compared to other MEMS packaging techniques are that it is a CMOS compatible low temperature method. Different MEMS devices can be used for vacuum encapsulation using this method. It does not require a high temperature deposition and etching of sacrificial materials and is stiction-free. Removal of the sacrificial layer is performed through openings, called trench cuts, and later the openings are sealed for encapsulation.

For the MEMS packaging application, Al_2O_3 (alumina) is chosen as a resonator beam and sealing material. The primary reasons for choosing this material is due to the hard and stiff material property with high Young's modulus. Alumina can also be used in high temperature and under harsh environment. On top of that, packages with optical transparent window can be made with this material. For the first time this work was reported the use of alumina as a packaging material in MEMS.

Extensive RF and reliability measurements were performed on the packaged resonators including evaluation of the package permeability, stress and cavity pressure. Long term and accelerated life testing on the packaged resonators indicated the robustness of the package.

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LIST OF SYMBOLS

C_{EOT}	equivalent oxide capacitance of MOSFET (Fcm^{-2})
C_g	total gate capacitance of MOSFET (Fcm^{-2})
C_{gb}	gate to bulk capacitance of MOSFET (Fcm^{-2})
C_{gc}	gate to channel capacitance of MOSFET (Fcm^{-2})
C_{ox}	gate oxide capacitance of MOSFET (Fcm^{-2})
$C_{overlap}$	overlap capacitance (Fcm^{-2})
D_{it}	interface trap density from sub-threshold measurements ($eV^{-1}cm^{-2}$)
E	energy level (eV)
EOT	equivalent oxide thickness (nm)
E_c	conduction band edge (eV)
E_{fn}	quasi Fermi level (eV)
E_g	energy Gap (eV)
E_i	intrinsic Fermi level (eV)
E_v	valence band edge (eV)
E_x	field along the channel (Vcm^{-1})
f	frequency (Hz)

f_t	trap occupancy function
g_d	Conductance (A V^{-1})
g_m	transconductance (A V^{-1})
h	Planck's constant (eV-s)
I_d	drain current (A)
I_g	gate current (A)
I_{sub}	substrate current (A)
I_s	source current (A)
k	dielectric constant
k	Boltzmann's constant (eV K^{-1})
L	MOSFET channel length (µm)
ΔL	length of pinch-off/velocity saturation region (µm)
m^*	electron effective mass (kg)
N	inversion layer charge density (cm^{-2})
N_0	source end charge density (cm^{-2})
N_f	fixed charge density (cm^{-2})
$N(x)$	inversion layer charge density at distance x from the source (cm^{-2})
N_t	oxide trap density (cm^{-3} eV^{-1})
N_{ot}	occupied traps per unit area (cm^{-2})

N_{tHK0}	trap density at the intrinsic Fermi level, at the high-k dielectric - interfacial layer interface (cm^{-3} eV^{-1})
$N_{tHK}(E_{fn}, z)$	trap density distribution in the high-k layer at the quasi Fermi level (cm^{-3} eV^{-1})
$N_{tIL}(E_{fn}, z)$	trap density distribution in the interfacial layer at the quasi Fermi level (cm^{-3} eV^{-1})
ΔN	inversion charge in the $W\Delta x$ area
ΔN_{ot}	number of occupied traps in the gate oxide ($W\Delta x$ area)
q	electronic charge (C)
Q_{bulk}	bulk charge (Ccm^{-2})
Q_D	depletion charge (Ccm^{-2})
Q_G	gate charge (Ccm^{-2})
Q_{inv}	inversion layer charge (Ccm^{-2})
Q_{it}	interface trap charge (Ccm^{-2})
Q_{sc}	semiconductor charge (Ccm^{-2})
Q_t	oxide trap charge (Ccm^{-2})
R	coupling coefficient between fluctuations in the channel charge and in the gate oxide trapped charge
S	subthreshold slope (V^{-1})
S_I	total current noise power spectral density (A^2 Hz^{-1})
S_{Id}	total drain current noise power spectral density (A^2 Hz^{-1})
$S_{\Delta Id}(x,f)$	power spectral density of the local current fluctuations (A^2 Hz^{-1})

$S_{\Delta Nt}\,(x,\,f)$	power spectral density of the mean square fluctuations in the trapped charge carriers over the area $W\Delta x$ ($\mathrm{Hz^{-1}}$)
S_{V_d}	drain voltage noise power spectral density ($\mathrm{V^2\,Hz^{-1}}$)
T	temperature (K)
t_{CET}	capacitance equivalent thickness (nm)
EOT	equivalent oxide thickness (cm)
T_{HK}	high-k dielectric thickness (cm)
T_{IL}	thickness of interfacial layer (cm)
T_{ox}	thickness of gate oxide (cm)
V_d	drain to source voltage (V)
V_{dsat}	drain to source voltage at pinch-off/velocity saturation point (V)
V_g	gate to source voltage (V)
V_{ox}	potential across gate oxide (V)
V_s	source voltage (V)
V_{sub}	substrate voltage (V)
V_t	threshold voltage (V)
$V(x)$	horizontal channel potential in the channel at a distance x from the source (V)
W	MOSFET channel width of (µm)
x	distance in the channel (cm)
y	distance in the width dimension (cm)
z	distance into the gate dielectric stack (cm)

Δx	infinitesimal length in the gate dielectric (cm)
Δy	infinitesimal width in the gate dielectric (cm)
Δz	infinitesimal thickness in the gate dielectric (cm)
α_H	Hooge's Coefficient
α_{sc}	screened coulomb scattering coefficient (V s)
γ	carrier tunneling coefficient in the gate dielectric (cm^{-1})
γ_{HK}	carrier tunneling coefficient in the high-k gate dielectric (cm^{-1})
ε_0	permittivity of free space (Fcm^{-1})
η_{HK}	fitting parameter that determines the high-k dielectric trap density distribution as a function of z (cm^{-1})
λ_{HK}	fitting parameter that defines the effect of dielectric band-bending on the trap density that the tunneling electron encounters in the high-k dielectric layer (eV^{-1})
μ	surface potential based effective carrier mobility (cm^2/Vs)
μ_{c0}	mobility fitting parameter (cm/Vs)
μ_{eff}	effective carrier mobility (cm^2/Vs)
μ_{imp}	mobility due to impurity scattering (cm^{2}V^{-1}s^{-1})
μ_{latt}	mobility due to lattice scattering (cm^{2}V^{-1}s^{-1})
μ_{others}	mobility due to other scattering phenomena (cm^2/Vs)
μ_{ox}	mobility due to oxide charge scattering (cm^2/Vs)

ξ_{HK} fitting parameter for energy dependence of high-k traps (eV^{-1})

τ (*E, x, y, z*)   trapping time constant in the gate dielectric (s)

τ trapping time constant (s)

τ_o trapping time constant at the Si/SiO_2 interface (s)

σ frequency exponent as in $1/f^{\sigma}$

ω angular frequency (radians/s)

ψ_s surface potential (V)

CHAPTER 1

INTRODUCTION

<u>1.1 Introduction</u>

This dissertation is divided into two sections. In the first section, the low frequency noise performance of Hafnium (Hf) based high dielectric constant (high-k) gate dielectric metal-oxide-semiconductor field effect transistors (MOSFETs) is considered. The second section discusses CMOS process compatible, cost effective, wafer level vacuum packaging of radio frequency (RF) microelectromechanical systems (MEMS) devices.

<u>1.2 Trends in semiconductor industry and device scale</u>

For many decades, the performance of MOSFET has been the main driving force for the growth of the semiconductor industry. This growth is sustained by conventional device scaling. For this reason, the gate length has been reduced from hundreds of micrometers in the 1960s to a few tens of a nanometer today. During 1970s, it was discovered that devices with short gate lengths [1], 1 μm at that time, showed undesired behavior, due to a predicament called short channel effect. Scaling of the threshold voltage also causes an increase in the subthreshold current and leads to high power consumption even when the device is off. On the other hand, gate looses control over the channel as the gate length is scaled down. This leads to a reduced threshold voltage and an increased off-current for devices with a short channel length. However, other technologies to improve device performance were also explored at the same time as traditional downscaling faced difficulties. It was also found that continuous downscaling of device requires introduction of new dielectric materials for the gate oxide. All of these have resulted in the emergence and development of a broad range of alternative CMOS technologies with new materials and novel architectures.

Unfortunately, down-scaling has also resulted in the following undesirable effects [2,3,4]. The carrier mobility has degraded when the doping concentration is increased due to higher effective electric field as well as due to impurity scattering. Moreover, source and drain resistances had to be scaled down in proportion to the channel resistance which is increasingly difficult since the junction depth decreases simultaneously. Reliability and power dissipation became serious problems in the generalized scaling scheme. The tunneling current increased exponentially with the decreasing gate oxide thickness. In addition, the depletion of poly-si gate gave rise to a reduction in the effective oxide capacitance, since the depletion region appears as a capacitance acting in series with the gate oxide capacitance. All these effects together demonstrate the need to find alternative materials and device architectures to enhance the carrier mobility, control the short channel effects, and limit the gate leakage current.

1.2.1 High-k materials and noise modeling

1.2.1.1 Introduction of high-k materials

Improvements in integrated circuit (IC) speed and chip area have been achieved by scaling down the physical thickness of the conventional SiO_2 gate dielectrics and device dimension. Driving technology for modern integrated circuits greatly relies on aggressive down scaling of MOS transistors. Reducing the transistor size not only increases package density but also increases circuit speed and reduces power dissipation [5]. However, SiO_2 has reached its physical limitation due high leakage current and reliability concerns. Continuous scaling down of the MOSFET with the minimum feature size of 90 nm and below would require equivalent oxide thickness (EOT) of 1.5~2nm and below. A 1~1.5 nm of SiO_2 layer corresponds to only around 3~4 monolayers of SiO_2. In this thinner EOT range, SiO_2 suffers from leakage current which is too high to be used for low-power applications. In addition, SiO_2 thickness control across a 12-inch wafer imposes even more serious difficulty in growth of such a thin film. Moreover, in that

thickness, direct tunneling current through the SiO_2 cannot be tolerated anymore. Therefore, it has become necessary to identify alternative high-k gate dielectrics in order to meet the stringent requirements in the leakage gate current and EOT. So far a number of high-k gate materials have been reported such as HfO_2, Al_2O_3, ZrO_2 and their silicates [6,7,8,9]. Among these various high-k gate dielectric materials, Hf-based high-k gate materials and its silicates with moderate high-k value (dielectric constant between 21~25) have been found to be attractive because they have demonstrated enhanced device properties, especially low gate leakage current, improved reliability against induced electrical stress, and better compatibility with poly-silicon as well as metal gate processes [5].

1.2.1.2 Advantages and disadvantages of high-k materials

The scaling of the MOSFET follows the Moore's law, which predicts the increase in number of transistors in IC. However, scaling of conventional gate oxide, SiO_2, beyond 1.5nm is problematic. The leakage current flowing through the gate oxide exceeds well above the specification. Therefore, high-k gate dielectrics have attracted a great deal of attention as the replacement of conventional SiO_2 gate dielectrics. The reason for using higher dielectric constant material is to provide a substantially thicker dielectric material to reduce gate leakage current and to improve the gate capacitance. So far, many materials have been evaluated as a suitable candidate for the gate oxide. Among these materials, Hf-based high-k gate dielectrics appear to be sone of the most promising materials. In fact, Hf-based gate dielectric materials could be scaled down to below EOT of around 1 nm with excellent electrical and physical characteristics. Although high-k gate dielectric materials are necessary to continue the current scaling trends, these materials also have been known to have higher trap density than conventional gate oxide materials [10]. A number of different processing techniques have been reported to improve the characteristics of high-k gate dielectrics [11,12,13,14]. The origin of traps in the high-k gate dielectric materials still remains a question. These pre-existing traps can

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play an important role in the dielectric wear-out as well as device performance. In order to evaluate reliability, it is necessary to pin point the factors that influence the breakdown of the high-k gate dielectric materials.

1.2.1.3 Low Frequency Noise performance

This new high-k gate dielectric technology has several important implications on the MOSFET low frequency noise (LFN) performance. LFN is sensitive to the defects and imperfections in the proximity of the carrier current path. The device quality in terms of defect densities as well as the LFN properties may differ substantially for different materials, manufacturing technologies and device architecture. At the same time as the more complex technologies may lead to the increased LFN, the downsizing of the transistor dimensions certainly causes higher LFN.

1.3 Device level packaging in MEMS

Second part of this proposal discusses design, fabrication, and characterization of wafer level vacuum packaging of MEMS devices. For MEMS products, packaging is one of the stumbling blocks against successful commercialization of the product and is a major portion of the total production cost of virtually every MEMS device. This high cost has made packaging the key point of focus for the industry to reduce cost in order to enhance the competitiveness of the product in the market. Packaging technology vary widely depending between MEMS devices exposed to the environment (pressure sensor) and those isolated from it (RF MEMS and accelerometer). Many MEMS devices require expensive vacuum packaging. MEMS resonator is one example where the quality (Q) factor of the resonator depends on the pressure of the ambient. According to 2007 report on assembly and packaging of International Technology Roadmap for Semiconductors (ITRS) [15], much emphasis has been given to the wafer level vacuum packaging for RF MEMS devices due to its improved electrical performance, low cost,

lower power requirements and smaller size. Providing a controlled micro-environment for isolating MEMS structures may represent an optimal approach for the cost effective production of suspended MEMS devices. By effectively sealing the MEMS at a wafer or die level, it is possible to subject the device to conventional high volume packaging approaches. This work details the design and fabrication of "canopy structure" vacuum packaging of RF MEMS device. The approach is to successfully encapsulate the RF MEMS resonators with the vacuum packages to form self packaged devices and to check the quality of vacuum in the package by measuring the resonator characteristics.

1.3.1 Cost effective RF MEMS packaging

1.3.1.1 Wafer level packaging

Wafer level encapsulation mitigates many of the challenges associated with MEMS packaging such as, dicing, handling, and encapsulation and it represents a challenging and costly task in the manufacturing of MEMS systems [16,17]. On an average, 70% of the cost of a MEMS device is in packaging. The package protects the MEMS device from the detrimental effects of the environment. A vacuum encapsulation is especially required for the operations of MEMS devices such as resonators, Pirani gauges and gyroscopes etc. The package can also provide design specific functions such as RF signal isolation as well as mechanical stability and radiation protection required for sensors.

The main advantage for moving from chip-scale to wafer level is the cost. Moreover, since the wafer level packaging is typically done in clean room environment, there is less chance of contaminating the MEMS device. As a device prototype we have chosen RF MEMS resonators, because the Q-factor and resonance frequency (f_r) of the MEMS resonators are pressure dependent. Therefore, any change in pressure inside the cavity will result in corresponding

change in Q factor and f_r. In this way, we can monitor the vacuum quality inside the encapsulation layer.

1.3.1.2 Review of current MEMS packaging

To ensure the long term reliability, in some cases an open die MEMS device must be hermitically packaged. For MEMS packaging there are generally two approaches. One is chip scale packaging, where sealing is performed on the individual die after dicing; the other one is wafer-level packaging, where sealing is performed in parallel with device fabrication prior to dicing and assembly. Wafer level packaging provides many benefits- two most important being the lowest cost and smallest size.

The wafer level packaging can be classified into wafer bonding and sacrificial layer based encapsulation techniques. The wafer bonding is typically done by bonding a cap wafer on to the MEMS wafer. In the sacrificial layer based technique, the encapsulation can be done on top of a surface micromachined device by depositing a thin film overcoat. Later, the trench cuts are made on top of the packaging layer, followed by removing of the sacrificial layer and finally sealing of the trench cuts by films deposition.

Although wafer bonding results in good life expectancy, it has a number of disadvantages. First of all, the anchor region where the cap seals to the MEMS die must be large to ensure a safe and hermetic seal. This results in a significant increase in die size and consequently in the production cost. And more importantly for RF MEMS there is also an increase in electromagnetic loss. The bonded die is also thicker than the standard IC die. Wafer to wafer bonding requires alignment of the cap to the host MEMS wafer, which can complicate the packaging especially for small packages. On top of all these, the bonding requires very clean

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surfaces. Therefore, packaging of MEMS with rough surfaces may be difficult and may result in a non hermetic seal and yield loss.

A possible solution for all of the above problems is the formation and sealing of surface micromachined layer over the MEMS. The main advantages of this integrated packaging technique would be the reduced thickness and chip area with resultant lower cost batch process. In this dissertation, we have introduced Al_2O_3 (alumina) as a sealing and resonator beam material as part of a low cost, low temperature packaging technique.

1.4 Summary

The contribution of this dissertation is on the contemporary reliability issues arising directly from the semiconductor industry. The first part of this work deals with the low frequency noise characterization and reliability of Hf-based high-k gate dielectric materials. Recently, there have been reports on the LFN performance of various mixed signal circuits with MOSFETS using Hf-based high-k gate dielectric materials [18, 19, 20]. Since LFN is a growing concern for analog and mixed signal CMOS circuitry, it is important to characterize the LFN not only for fresh devices but also during the lifetime of the transistor. By and large, this has been neglected so far. In this work, we present a systematic study of *1/f* noise exhibited by HfSiON gate-dielectric MOSFETs, and its dependence on the nitridation technique. In addition, Hot Carrier Stress (HCS) and Constant Voltage Stress (CVS) induced noise degradation in plasma and thermally nitrided HfSiON and HfSiO devices was investigated. It is shown, for the first time that the nitrogen distribution profile in the gate dielectric due to different nitridation techniques affects the HCS and CVS induced 1/f noise performance of ultra thin HfSiON nMOSFETs.

The second part of the dissertation addresses a very important issue in a fast growing MEMS industry, the packaging. Packaging plays a critical role for microelectromechanical systems. For specific RF applications, where the use of MEMS technology is highly attractive, cost of effective packaging is one of the primary barriers to commercialization. RF MEMS packaging is comparatively new with a variety of approaches being explored to balance the broad range of technological and cost constraints. Many RF MEMS devices require a hermetic or vacuum operation environment. This work presents a post-CMOS compatible method for vacuum packaging of RF MEMS devices by growing an encapsulation layer during the device fabrication. The packaging technique is scalable from device to die to wafer level. The resulting MEMS devices are surrounded by a vacuum or hermetic cavity and can then be placed in a conventional, low cost circuit package. This is a low temperature, area efficient, across wafer, device level encapsulation for MEMS. In this case, RF MEMS resonators in a fixed-fixed beam configuration were used as the test bed for the device level vacuum packaging technique since the quality factor of the resonators can be used as an indirect measure of the package quality and reliability. The encapsulation process started after fabricating the MEMS resonators and is based on a double sacrificial layer surface micromachining technique, used to create a cavity under and above the resonator. Polyimide was used as a sacrificial layer, followed by the deposition of a packaging layer with trench cuts, which facilitate the sacrificial layer removal. The trench cuts were then sealed at a low-pressure environment, thus forming a cavity around the device at the sealant layer deposition pressure. Extensive RF characterization and reliability tests were performed on the packaged resonators. No noticeable degradation in RF characteristics was observed with high temperature and thermal cycling stress, indicating the good reliability of the packages. In addition we report for the first time the use of alumina as resonator beam and packaging material.

A brief outline of the dissertation is presented below.

Chapter 1 presents background, goal and achievements of this work. This chapter also provides a general overview of importance of the work.

Chapter 2 gives information about background as well as various measurement techniques used to evaluate the low frequency noise performance of Hf-based high-k gate dielectric MOSFETs.

Chapter 3 introduces effects of various nitridation techniques on the low frequency noise performance followed by HCS and CVS induced low frequency noise degradation.

Chapter 4 introduces the motivation and approach for cost effective RF MEMS packaging. This chapter also presents the design and fabrication process for the vacuum cavity package and the RF MEMS resonator.

Chapter 5 presents the extensive RF characterization of packaged RF MEMS resonators. A thorough study of different long term and accelerated life testing is also performed.

Chapter 6 is the conclusion of the work done and it also suggests future directions for the present work.

CHAPTER 2

NOISE AND CARRIER MOBILITY MEASUREMENTS

2.1 Introduction

With the immense progress in silicon technology and miniaturization of electronic devices to nanometer sizes, the reliability of gate oxide and its interface has gained importance. Trapped charges, defects and traps both in the oxide and at the high-k/ Si interface play an important role in the gradual degradation of the oxide characteristics. To characterize the defects in the oxide and to predict device reliability due to oxide breakdown, flicker or *1/f* noise has been shown to be a well established diagnostic tool. The measurement of noise is a complex task. The measurement setup must be designed carefully with appropriate shielding and batteries as the power source to avoid disturbances in the measurement setup. The noise measurement is typically performed in the frequency domain by measuring the power spectral density with a spectral analyzer.

This chapter presents the specifications for the MOSFETs used for the noise analysis, describes different measurement methods including DC characteristics, charge density and mobility extraction, low frequency noise as well as different stressing techniques.

2.2 Device specification

The devices used in this work were provided by SEMATECH International, fabricated using the 45 nm technology node [21]. Standard CMOS processing flow was used to fabricate the samples. On HF cleaned wafers, a SiON interface layer was thermally grown. 2nm HfSiO was deposited with an optimized atomic layer deposition (ALD) process using $Hf[N(CH_3)C_2H_5]_4$ (TEMAHf) and $Si[N(CH_3)C2H_5]_4$ (TEMASi) precursors with ozone oxidant . For plasma

nitridation of ALD HfSiO sample, processing time was varied to control the nitrogen content in the film. Other plasma process conditions were kept constant. For thermal nitridation, a similar nitrogen concentration was incorporated in ALD HfSiO film in NH_3 ambient and N content was increased by increasing the temperature of NH_3 anneal. ALD TiN with polysilicon capping was used as the gate electrode. A conventional CMOS process flow that included $1000^{o}C$, five-second activation anneal was used after gate stack formation. Nitrogen content for both plasma and thermally nitrided samples was measured by X-ray photoelectron spectroscopy (XPS) to be 8%. Subsequently TiN was deposited as the gate electrode using ALD. The rest of the CMOS processing was standard. A lot-split containing HfSiO gate dielectric with no nitridation was also included in the investigation as a control sample. Thermally and plasma nitrided samples (HfSiON) and pure HfSiO with no added nitrogen displayed capacitances equivalent to 1.03, 1.06 and 1.17 nm EOT, respectively. The device specification is shown in the following table. The nitrogen method column indicates how nitrogen was incorporated in the gate dielectric and W/L (Width/Length) column indicates device dimensions.

Table 2.1 Device Specifications

Dielectric(HfSiON)	EOT (nm)	Nitridation Method	W/L(µm/µm)
10% SiO_2	1.06	Plasma	10/0.25
10% SiO_2	1.03	Thermal	10/0.25
10% SiO_2	1.17	None (HfSiO)	10/0.25

Semiconductor parameter analyzer Agilent 4155C was used for DC characterization before noise measurements to extract the threshold voltage (V_t), transconductance (g_m), conductance (g_d) and subthreshold slope (S). Split C-V measurements were carried out on 10x10 μm^2 devices to calculate carrier effective mobility and capacitance equivalent thickness (t_{CET}). The reason for using large area MOS devices for C-V measurements is that large area

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capacitors are easier to measure. 10x0.25 μm^2 devices were used for the low-frequency noise measurements. For hot carrier stress and constant voltage stressing conditions 10x0.1 μm^2 devices were used.

<center>2.3 Measurement Setup</center>

The frequency range for low-frequency noise measurements was typically from 1Hz to 100 KHz. The low-frequency noise measurement technique requires sensing very weak signals. Therefore, it is necessary to minimize the internal noise other than *1/f* noise as well as to prevent external interference. By using a battery to bias the device and shielding the device during measurements, we can prevent interference from power lines and other equipment.

The following sets of measurements were performed:

- DC characteristics

- Charge density and mobility extraction

- Low frequency noise

- Stressing

2.3.1 DC characteristics background and measurements:

2.3.1.1 DC characteristics background

Various MOSFET device performance parameters are required for noise analysis. Thus, DC characterization was always done prior to the noise measurements. Additionally, the DC measurements were repeated after the noise measurements to check if there is any change in the device parameters. A typical set of DC curves are shown in Figure 2.1 obtained using HP-4155C semiconductor parameter analyzer on TiN/2nm HfSiON n-channel MOSFET. From

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the I_d-V_d and I_d-V_g curves, parameters like ac conductance (g_d=∂I_d/∂V_d), transconductance (g_m=∂I_d/∂V_g), subthreshold slope (S=∂$log(I_d)$/∂V_g) and the threshold voltage (V_t) were obtained.

2.3.1.2 DC characteristics measurement

The first step in device evaluation was to perform DC characterizations, and measure the terminal currents versus applied voltage. For sensitive and accurate parameter measurements, the Source-Measure Units (SMU) of HP 4155C parameter analyzer is connected to on a shielded 8060 series MicroManipulator probe station with triax cables. Proper grounding of the probe station is ensured before start of the measurments. Precautions were also taken every time to protect the devices from possible voltage spikes or electro-static discharge (ESD).

Basic device parameters such as different terminal currents, drain (I_d), source (I_s), gate (I_g) and substrate (I_{sub}), as well as the terminal voltages were recorded. User defined functions were used to obtain V_{th}, $g_m(A/V) = \dfrac{dI_d}{dV_g}$, $g_d(A/V) = \dfrac{dI_d}{dV_d}$ and $S(Dec/V)$ of the devices.

Different DC characteristic data from 10x0.25 μm^2 HfSiO nMOSFET device are presented in Figures 2.1-2.3
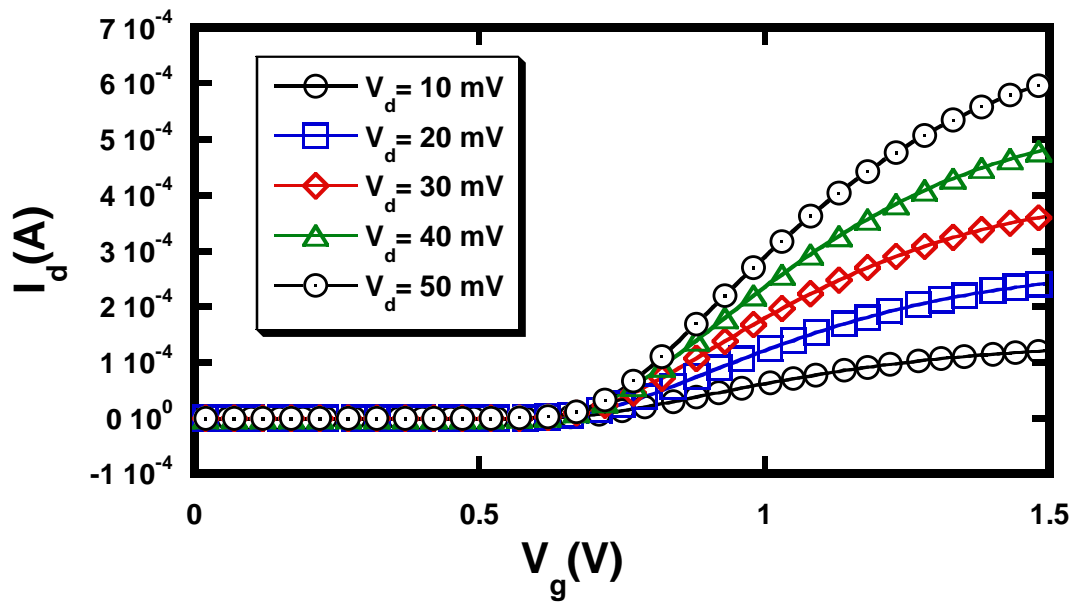
Figure 2.1 Measured drain current as a function of gate voltage at different drain voltages.
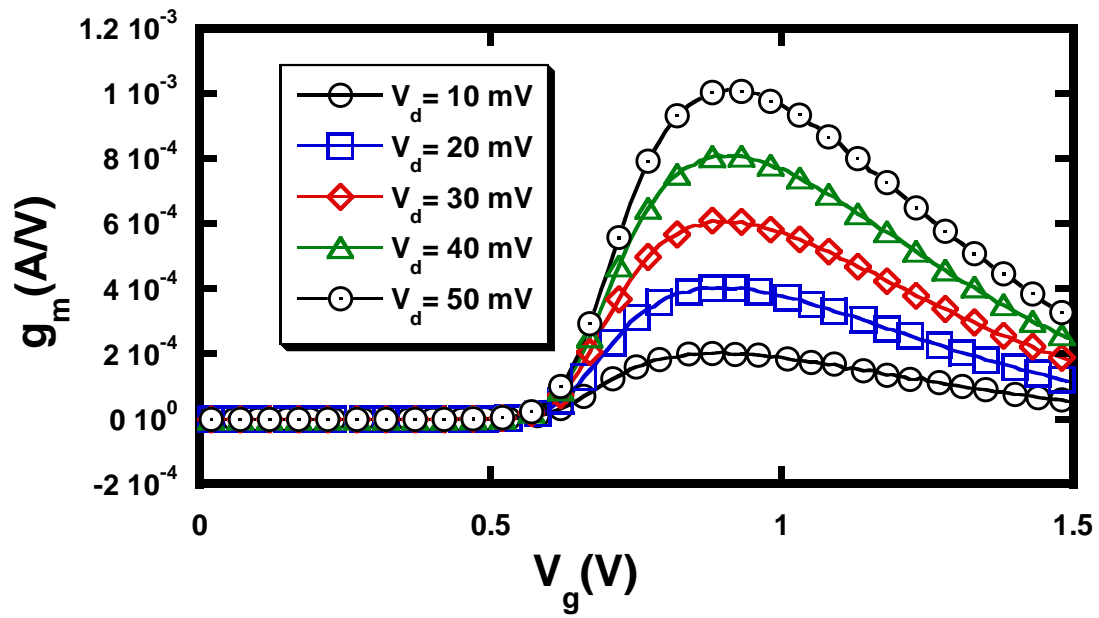
Figure 2.2 Measured transconductance as a function of gate voltage at different drain voltages.
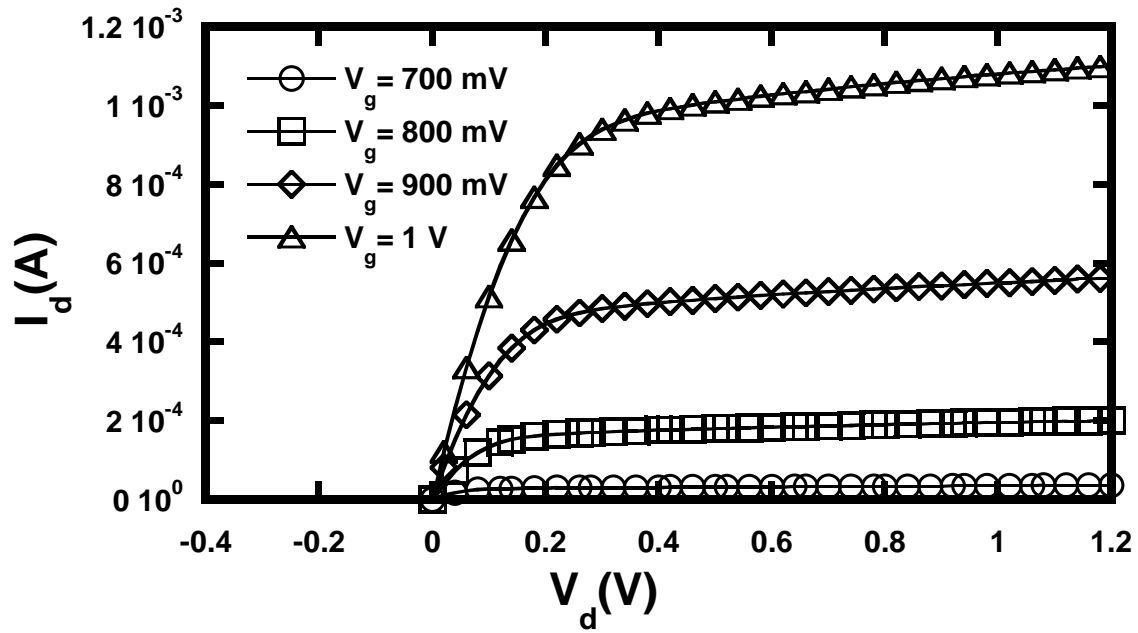
Figure 2.3 Drain current as a function of drain voltage at different gate voltages.

2.3.2 Charge density and mobility extraction:

2.3.2.1 Charge density and mobility extraction background

The inversion layer charge density and mobility values are needed for the noise analysis at different gate bias voltages, as explained in detail in Chapter 3. Mobility can also be extracted from the g_m. However, in ultra thin gate dielectric MOSFET devices, gate leakage current is a prominent phenomenon which leads to errors in the extracted MOSFET device parameters. Therefore, it is important to consider the effect of leakage current. Otherwise the mobility will be underestimated. To accurately determine the MOSFET inversion layer charge density and channel carrier mobility, split C-V measurements were performed. This split C-V measurement technique was originally suggested by Koomen [22].

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The applied voltage at the MOSFET gate terminal is considered as the summation of surface potential (ψ_s) and the potential across the gate oxide (V_{ox}) i.e.,

$$V_g = \psi_s + V_{ox} \qquad \text{or} \qquad V_g = \psi_s + \frac{Q_{sc}}{C_{ox}}$$

$$Q_{sc} = Q_{inv} + Q_{bulk} \qquad\qquad (2.3.1)$$

The device channel charge Q_{sc}, consists of Q_{inv} the inversion layer charge and Q_{bulk} charges in the bulk.

To get the channel capacitance,

$$\frac{d\psi_s}{dV_g} = \frac{C_{ox}}{C_{ox} + \dfrac{dQ_{inv}}{d\psi_s} + \dfrac{dQ_{bulk}}{d\psi_s}} \qquad\qquad (2.3.2)$$

Therefore, gate to channel capacitance is given by,

$$C_{gc} = \frac{dQ_{inv}}{dV_g} = \frac{dQ_{inv}}{d\psi_s}\frac{d\psi_s}{dV_g} = \frac{\dfrac{dQ_{inv}}{d\psi_s}C_{ox}}{C_{ox} + \dfrac{dQ_{inv}}{d\psi_s} + \dfrac{dQ_{bulk}}{d\psi_s}} \qquad\qquad (2.3.3)$$

whereas, the gate to bulk capacitance is given by differentiating the charges in the bulk with respect to gate voltage,

$$C_{gb} = \frac{dQ_{bulk}}{dV_g} = \frac{dQ_{bulk}}{d\psi_s}\frac{d\psi_s}{dV_g} = \frac{\dfrac{dQ_{bulk}}{d\psi_s}C_{ox}}{C_{ox} + \dfrac{dQ_{inv}}{d\psi_s} + \dfrac{dQ_{bulk}}{d\psi_s}} \qquad\qquad (2.3.4)$$

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The final expressions for gate to channel capacitance and gate to bulk capacitance are given by,

$$C_{gc} = \frac{C_{inv} \, C_{ox}}{C_{ox} + C_{inv} + C_{bulk}} \qquad ; \qquad C_{gb} = \frac{C_{bulk} \, C_{ox}}{C_{ox} + C_{inv} + C_{bulk}}$$

and, $C_g = C_{gc} + C_{gb}$

Now, the charge can be found by integrating the capacitance,

$$Q_{inv} = \int_{-\infty}^{V_g} C_{gc}(V_g) \, dV_g \qquad \text{and} \qquad Q_{bulk} = \int_{-V_g}^{\infty} C_{gb}(V_g) \, dV_g$$

The effective mobility can then be expressed in the following way,

$$\mu_{eff} = \frac{g_d}{(W/L) \, Q_{inv}} \tag{2.3.5}$$

For the mobility in the linear region of MOSFET operation, g_d is obtained by biasing the drain end at very low voltage, generally at 10-20 mV.

2.3.2.2 Charge density and mobility extraction measurements

After the completion of the DC parameter extraction, the split C-V measurements were done on 10x10 μm^2 devices using a HP 4284 LCR meter. First, the DUT (Device Under Test) was connected to the LCR meter. To minimize the contribution of the capacitance from interface traps, the operating frequency must be high enough. Parallel circuit mode (Cp-D) was selected from LCR meter because of the small channel capacitance. Before taking C-V measurements, both open and short corrections were performed. The high potential and high current ports as well as low potential and low current ports were shorted together. Furthermore, the length of the

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shorting wires and the distance from the device leads were kept small to minimize the stray capacitance effects as much as possible. As shown in the Fig 2.4, the gate was connected to the high potential, the drain and source terminals were shorted and connected to the low potential ports. The contribution from the bulk charges was reduced by connecting the substrate to the ground terminal. The theory and details of the procedure and measurement setup can be found in a report by Siva Prasad Devireddy [23].

Since high-k gate dielectrics were used here, the gate leakage was at least an order of magnitude lower than the drain current even at the highest gate overdrive. If significant gate leakage currents are observed, appropriate corrections can be made as suggested in [24,25].
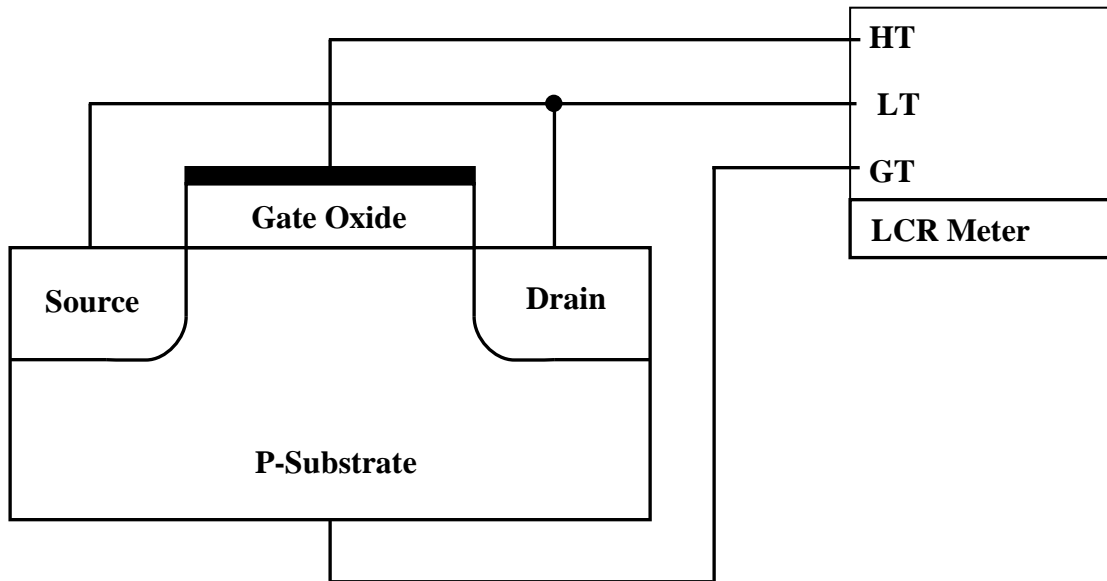
Figure 2.4 Split C-V measurement set up for MOSFET device. HT, LT and GT are high terminal, low terminal and ground terminal respectively [22].

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The C-V measurement set up was controlled by a Lab-VIEW program through GPIB interface with the LCR meter. The gate voltage was varied from -1.5 V to 1.5 V, with 10 mV step increments. As mentioned earlier, higher frequency measurements will eliminate the capacitance contribution from the interface traps. Therefore, 1MHz frequency was chosen. The C-V parameters were extracted as following. From the experimental data, C_{gc} was measured. This was followed by measurement of stray capacitance, $C_{overlap}$ from the sub-threshold region. Finally, the stray capacitance measured from sub-threshold region ($C_{overlap}$) is subtracted from the measured capacitance to get the net channel capacitance C_{gc}. A typical channel capacitance vs. gate voltage curve is shown in Figure 2.5 for an nMOSFET. Later, the inversion charge is calculated by the equation given below,

$$Q_{inv} = \int_0^{V_g} C_{gc}\, dV_g \qquad\qquad (2.3.6)$$

Now, using equation (2.3.5), the effective mobility can be written as,

$$\mu_{eff} = I_d L / W Q_{inv} V_d \qquad\qquad (2.3.7)$$

The above equation can be used to extract the effective mobility in both linear and saturation regions. In addition, t_{CET} can be calculated using the following equation:

$$t_{CET} = (\varepsilon_0 * 3.9) / C_{gc} \qquad\qquad (2.3.8)$$
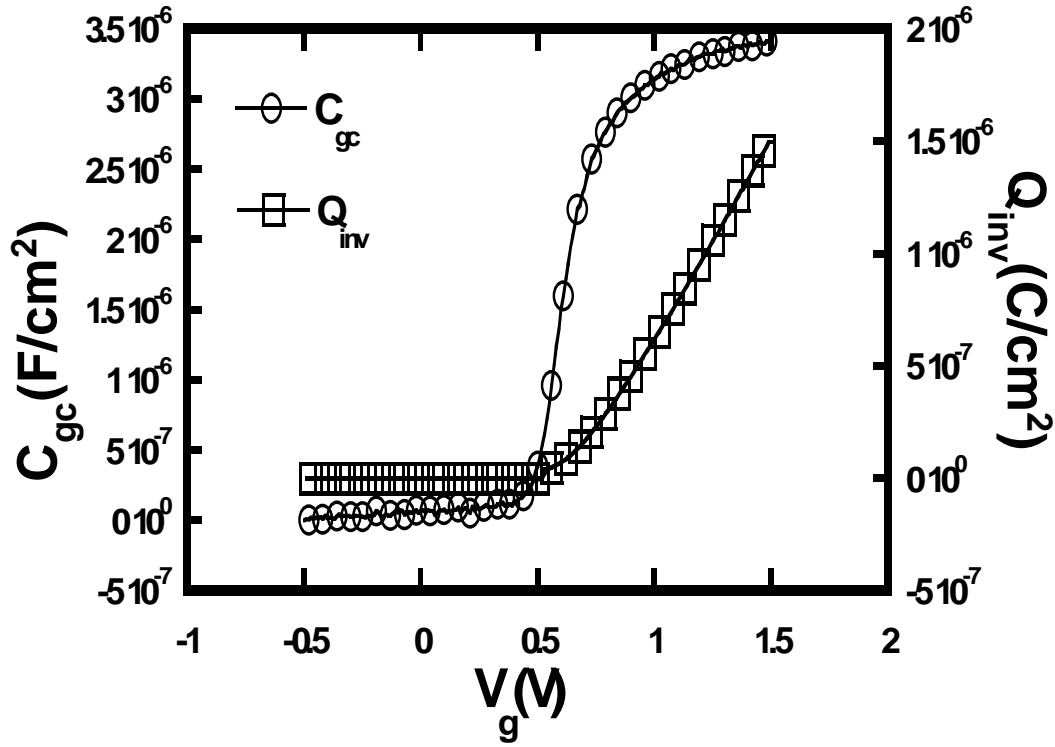
Figure 2.5 Corrected gate to channel capacitance of TiN/HfSiON nMOSFET from split C-V measurement and calculated channel inversion charge are shown here.

2.3.3 Low frequency noise background and measurements:

2.3.3.1 Low frequency noise background

In low frequency noise measurements, the power spectral density is the quantity that is preferably measured instead of noise power, since the spectral shape also provides very important information. Internal noise as well as external interference is needed to be minimized to get the reliable low frequency noise results. Even if the interference can be reduced to an acceptable level, the measurement might not still be accurate. One important thing to remember

is the noise response from the other circuit elements (i.e. bias box, connecting wires, pre-amplifier etc.) in the noise set up must be much lower than the noise response from the DUT. It is, therefore, primarily important to minimize the noise of the other elements in the setup. Appropriate shielding should be used for the part of the setup where the desired signal is sensitive to interference. Rechargeable batteries should be utilized as a power source to avoid noise contribution from the biasing circuitry. A low noise amplifier is used to amplify the weak signal before being fed into the spectrum analyzer. However, the amplifier inevitably adds its own internal noise to the signal. Therefore, the internal noise of the amplifier sets the measurement limit of the system and must be minimized. A spectrum analyzer measures and analyzes the signal in the frequency domain. Modern spectrum analyzers utilize discrete Fast Fourier Transform (FFT) algorithms to convert the measured signal from the time domain to the frequency domain. Most spectral analyzers have several choices of window functions to make the signal periodic in the time record. The most common types of windows are Hanning, rectangular, Gaussian top and flattop windows. Each window has different advantages and disadvantages. The Hanning window provides a good frequency resolution; therefore, it is used for low frequency noise measurements in this work.

2.3.3.2 Low frequency noise measurement

Wafer level low frequency noise measurements were performed at room temperature using an enclosed low noise 8060 series MicroManipulator probe station with proper grounding. The noise measurement set-up includes a DC bias box, an EG&G PAR113 pre-amplifier and a HP 3562A dynamic signal analyzer. Rechargeable Ni-Cd battery was used for DC bias box. Several batteries are connected together to get required bias for drain and gate terminal for the MOSFET. The drain and gate voltage was controlled by a variable resistor. The pre-amplifier, to amplify the drain voltage fluctuation, was battery powered. The frequency range in the pre-

amplifier and voltage gain were set in 0.03 Hz-300 kHz and 1000 respectively with input terminal in AC coupled mode. The output from the pre-amplifier was feed into the HP 3562A dynamic signal analyzer. Averaging must be used for reliable noise measurements. In this work 30 averages were used with 90 % data overlapping. The analyzer was set to evaluate the power spectral density of the voltage noise in V^2/Hz units in 1 Hz- 100 kHz frequency range. Fig. 2.6 shows the overall LFN measurement set up.

Contributions from stray noise sources are minimized by taking above precautions. For MOSFET noise measurements, the source and the substrate terminals are always shorted. Pre-amplifier's inherent noise and channel thermal noise are considered by taking background noise before each noise measurement at a particular gate overdrive. This is done by applying zero voltage at the drain end. Later, this background noise is subtracted from the noise measurement to the net *1/f* noise.

Reliable noise measurements require some knowledge and expertise due to the difficulty in measuring weak noise signals. Therefore, the following steps are suggested for reliable low frequency noise measurements.

- Turn off unused equipment that might disturb the measurement.
- Use preamplifier with low internal noise
- Use metal film resistors and DC batteries in the bias circuitry for lowest noise.
- Sometimes bad contacts due to worn-out probes or too gentle probing force can introduce noise that exceeds noise from DUT.
- Wireless and mobile phones should not be used in the vicinity of the measurement setup.

- Even switching of lights and equipment introduces disturbance in the low frequency range.

2.3.4 Hot carrier stress background and measurements:

2.3.4.1 Hot carrier stress background

Hot carriers (electrons or holes) are of concern in integrated circuits, because electrons and/or holes that gain energy in an electric field can be injected into the oxide to become oxide trapped charge, they can drift through the oxide, causing gate current, they can create interface traps, and they can generate photons [26]. The carrier temperature T and energy E are related through the expression $E = kT$, here k is Boltzman constant. At room temperature, $E \approx 25$ meV for T = 300 K. When carriers gain energy by being accelerated in an electric field, their energy E increases. For example, $T = 1.2 \times 10^4$ K for $E = 1$ eV. Hence the name hot carriers means energetic carriers, not that the entire device is hot. Let us briefly discuss the effects of hot carriers. During hot carrier stressing, some of the electrons in the channel entering the drain space-charge region experience impact ionization. The resulting hot carriers can be injected into the oxide (N_{ot}), can flow through the oxide (I_G), can generate interface traps (D_{it}), flow to the substrate contact as I_{sub}, and create photons [26]. The photons, in turn, can propagate into the device, be absorbed, and create electron-hole pairs. N_{ot} and D_{it} lead to threshold voltage changes and mobility degradation. The substrate current causes a voltage drop in the substrate, forward biasing the source-substrate junction, leading to further impact ionization and possibly snapback breakdown. The device can be viewed as a parasitic bipolar junction transistor (BJT) in parallel with the MOSFET. The BJT has an almost open base and open base BJTs often exhibit snapback breakdown with negative differential resistance. Almost open base means the

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base potential is not well controlled and although the base contact is grounded, the interior base has an ill-defined potential.
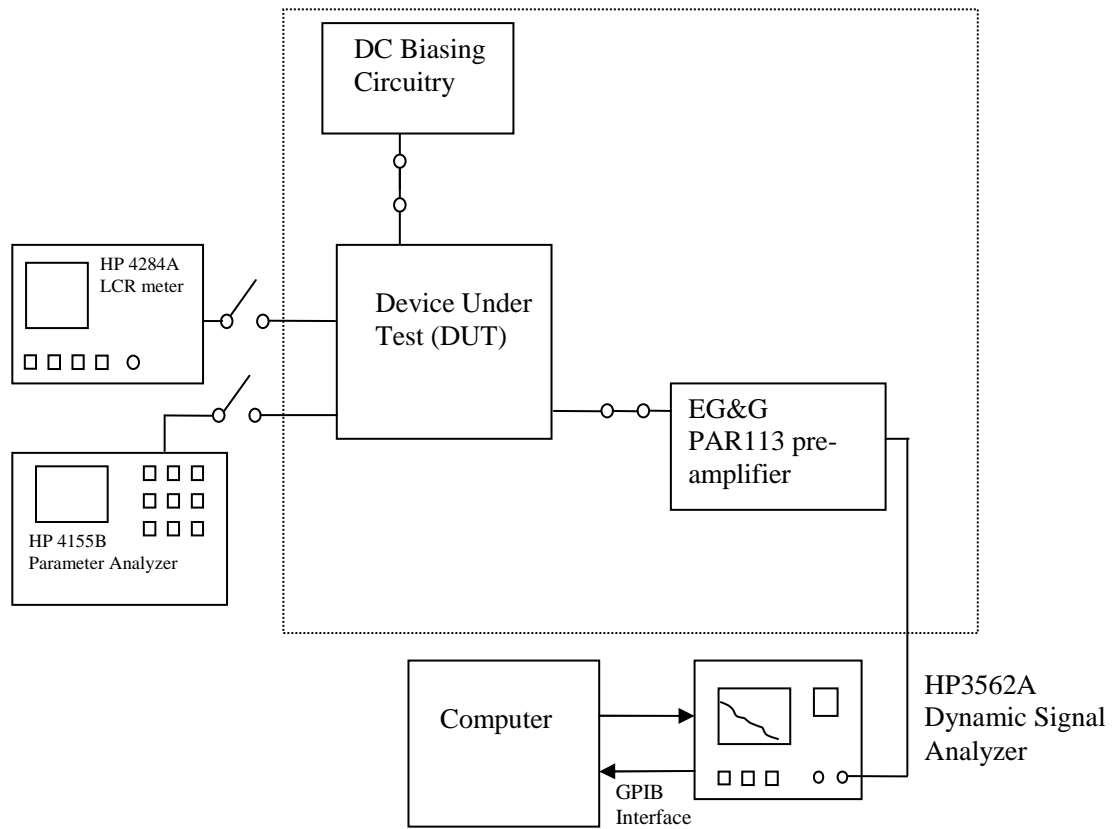
Figure 2.6 An overview of the low frequency noise measurement system.

The popular method to determine hot carrier degradation in conventional SiO_2 based n-channel devices is to bias the device at maximum substrate current. The substrate current depends on the channel lateral electric field. At low V_G, with the device in saturation, the lateral

electric field increases with increasing gate voltage until $V_G \approx V_{D/3} \sim V_{D/2}$. I_{sub} increases to a maximum at that gate voltage for n-channel devices. For higher gate voltages, the device enters its linear region, the lateral electric field decreases as does the substrate current. The device is biased at $I_{sub,max}$ for a certain amount of stressing time and a device parameter, *e.g.*, saturation drain current, threshold voltage, mobility, transconductance, or interface trap density, is measured [27]. This process is repeated until the measured parameter has changed by a predetermined amount (typically 10–20%) for I_{Dsat} . The lifetime corresponds to that time. Next the substrate current is changed by choosing a different gate voltage and the process is repeated and plotted as lifetime versus I_{sub}. The data points, measured over a restricted range, are extrapolated to the IC life, typically ten years, giving the maximum I_{sub} that should not be exceeded during the device operation. The chief degradation mechanism for n-channel MOSFETs is believed to be interface trap generation, and the *substrate* current is a good monitor of such damage. There are, of course, other measurements that can be used, such as interface trap density measurements by charge pumping, for example. Because it is simple to measure, I_{sub} is commonly used. Hot carrier damage can be reduced by reducing the electric field at the drain by, for example, forming lightly doped drains and by using deuterium instead of hydrogen during post-metallization anneal at temperatures around 400–450°C, since the Si-D bond is stronger than the Si-H bond [28,29]. An issue related to hot carriers is *plasma induced damage* during semiconductor processing, where charge in the plasma environment lands on the device. If it lands on MOS gates, the charge produces electric fields which, in turn, can generate insulator leakage currents. However, a different condition was reported to be true for short-channel MOSFETs with high-k dielectric gate oxides. In this work, the worst degradation condition was shown to be at $V_g = V_d$ rather than $I_{sub,max}$.[30]

2.3.4.2 Hot carrier stress measurement

Worst degradation condition ($V_g=V_d$) was chosen for HCS induced low frequency noise degradation in high-k gate oxide [31]. As we mentioned in the preceding paragraph, for MOSFETs with thick gate oxide (>5 nm) and long channel lengths, the substrate current (I_{sub}) is usually taken to monitor the hot carrier damage. In n-MOSFETs, holes generated during HCS due to impact ionization flow out of the substrate contact as I_{sub}, whereas the electrons contribute to the drain current I_d. If the electrons are injected into the oxide, this constitutes the gate current I_g. Since typically the substrate current shows a bell shaped trend with respect to the gate voltage (V_g), with the maximum degradation occurring around $I_{sub,max}$, it is assumed that the maximum HCS damage takes place at V_g for $I_{sub,max}$. [32]. *1/f* noise and dc characteristics were taken before and after applying the stress for 1000 s. Degradation in saturation drain current ($I_{d,sat}$) and maximum transconductance ($g_{m,max}$) was monitored by measuring I_d-V_g characteristics after 1000s of stress. The range of the gate bias was limited to 0-1.5 V to minimize additional stress on the device during I_d-V_g measurements. Both forward and reverse mode measurements (by interchanging drain and source terminal) were taken after hot carrier stress.

2.3.5 Constant voltage stress background and measurements:

2.3.5.1 Constant voltage stress background

The dielectric quality of the gate oxide determines the gate leakage and therefore the ability of the gate to control the MOSFET. For this reason the quality of the gate oxide is very important. It is also very sensitive to damage and can easily degrade. Although the oxide resistivity is on the order of 10^{15} Ohm, it is not infinite. Hence some currents do flow through the

gate oxide for any given gate voltage. However, for moderate gate voltages in conventional gate oxide, typical oxide electric fields $\leq 3 \times 10^6$ V/cm cause negligible gate currents. For higher gate oxide electric fields on the other hand, gate currents increase rapidly with applied voltage. To characterize the lifetime and integrity of gate oxides, voltages higher than operating voltages or temperatures higher than operating temperatures are used with appreciable current flow through the oxide. Many studies have been done on the breakdown mechanism in the ultra-thin gate oxides, in order to improve the reliability of MOSFET devices, as well as to improve the submicron device manufacturing process. In CVS experiment, the quality of the gate oxide is assessed by applying voltage stress at the gate terminal and grounding drain and source terminals. Due to this stress, the Fowler-Nordheim tunneling is the main mechanism for degradation in MOSFET parameters. Therefore this stress is also called FN stress [33]. Fig. 2.7 shows an experimental setup for constant voltage stress. Here the stress is applied at the gate end, with the source, substrate grounded.
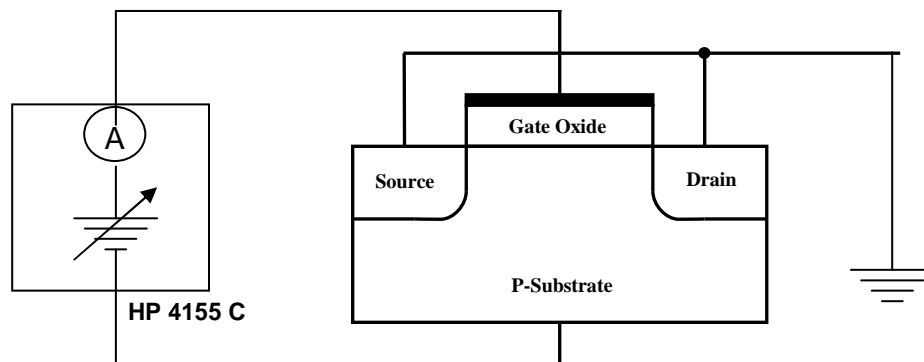
Figure 2.7 An overview of the constant voltage stress measurement setup.

2.3.5.2 Constant voltage stress measurement

Charge trapping in high-k gate dielectrics affects the result of electrical characterization significantly. DC mobility degradation, device threshold voltage instability and *C–V* or *I–V* hysteresis are a few examples. High-k gate materials are expected to have significant charge trapping problems related to structural defects, in particular, oxygen vacancies [34, 35, 36]. The small band gap of high-k gate materials contributes additionally to charge trapping due to enhanced tunneling probability. This charge trapping leads to degradation in carrier mobility and instability in device threshold voltage. The existence of charge trapping is acknowledged as a critical problem for high-k devices and the implications of charge trapping on the low frequency noise reliability have been investigated. For CVS measurements, the vertical electric field was fixed at 10MV/cm to accurately compare samples with different EOT. Here also, *1/f* noise and dc characteristics were taken before and after applying the stress for 1000 s and degradation in $I_{d,sat}$ and $g_{m,max}$ was monitored by measuring I_d-V_g characteristics.

2.4 Summary

A detailed explanation of background and measurement techniques for DC measurement, charge density and mobility extraction, low frequency noise and different stressing measurements are provided. The MOSFET samples used in these measurements were supplied by SEMATECH International. These samples were fabricated using 45 nm technology node and employed high-k gate oxide materials. In later chapters, we have used these samples to validate Multi Stack Unified Noise (MSUN) model. Additionally, these samples were used to study the effect of various nitridation on low frequency noise and different stress induced noise degradation.

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CHAPTER 3

NOISE RESULTS AND DISCUSSION

3.1 Introduction

The rapid development in CMOS technology in the past decades made downscaling possible at an exponential rate in order to follow the Moore's law. The transistor speed and the number of transistors that can be crammed into one chip have greatly increased as a result of the miniaturization of the transistor size. Low $1/f$ noise in the transistors is an important requirement for low noise radio frequency (RF) and analog applications. Therefore, accurate modeling and analysis of noise behavior is very important to CMOS circuit designers and semiconductor manufacturers. The inherent flicker or $1/f$ noise of MOSFET devices is the main subject of this work. According to ITRS [37] updated report of 2008 for DRAM chips, the 45nm technology, which is only possible with high-k/metal gate technology, will be needed by 2010. Among various high-k gate dielectric materials, hafnium based gate dielectrics are the leading candidates to replace the conventional SiO_2 and SiON gate dielectrics. HfO_2 and HfSiO thin films with or without nitrogen are being considered to be the promising. Nitrogen, added through plasma or thermal nitridation, enhances the electrical and physical properties of HfSiO [38,39] mainly due to enhancement of the dielectric constant because of the Hf-N bond. $1/f$ noise exhibited by MOSFETs not only affects the analog and mixed signal applications of these devices, but also can be utilized to evaluate the quality of the gate dielectric and the interfaces in the gate stack. Although extensive studies have been done on ultra-thin (2nm) HfSiON layers to increase carrier mobility, reduce crystallization, decrease charge trapping, improve threshold voltage stability, positive bias temperature instability (PBTI) and compatibility with metal gates,

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studies on the *1/f* noise characteristics have been relatively limited. In this work, LFN characteristics as well as stress induced LFN performance of the HfSiON and HfSiO devices are studied. This chapter starts with a brief overview of noise intrinsic to the MOSFET. Later, noise mechanisms in high-k gate oxide and its difference from conventional gate oxide are discussed. This is followed by validation of the MSUN model and effect of different nitridation techniques on LFN characteristics, as well as LFN behavior due to different stressing. Since different nitridation techniques result in different nitrogen distribution across the gate oxide layers, it is very important to study how this phenomenon affects the *1/f* noise.

3.2 General MOSFET noise theory

Currents and voltages in electronic circuits show random fluctuations around their DC bias values due to fluctuations in the physical processes governing the electronic transport. Several mechanisms exist that generate noise in the semiconductor devices leading to a unique spectral power distribution in the frequency domain. This section will give a brief overview of various noise components in MOSFET devices.

Thermal Noise:

Thermal noise was first discovered experimentally by J. B. Johnson and theoretically explained by H. Nyquist in 1928 [40, 41]. For this reason, this noise is also known as Nyquist or Johnson noise. Thermal noise originates from the random thermal motion of the electrons in the material and exists in thermal equilibrium and non-equilibrium. This type of noise is intrinsic to all resistors and is found in MOSFETs due to its resistive nature of the channel. The thermal noise exists in every resistor and resistive part of a device and no applied bias is needed. If a

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piece of material with resistance R and non zero temperature T is considered then the power spectral density (PSD) of such a noise is given by the the Nyquist theorem as [42]

$$S_V(f) = 4kTR \qquad (3.1)$$

where, R represents the resistance. In MOSFETs, the channel resistance is bias dependent.

Fig. 3.1 depicts white noise in a MOSFET that consists of thermal noise as well as shot noise that is described next.
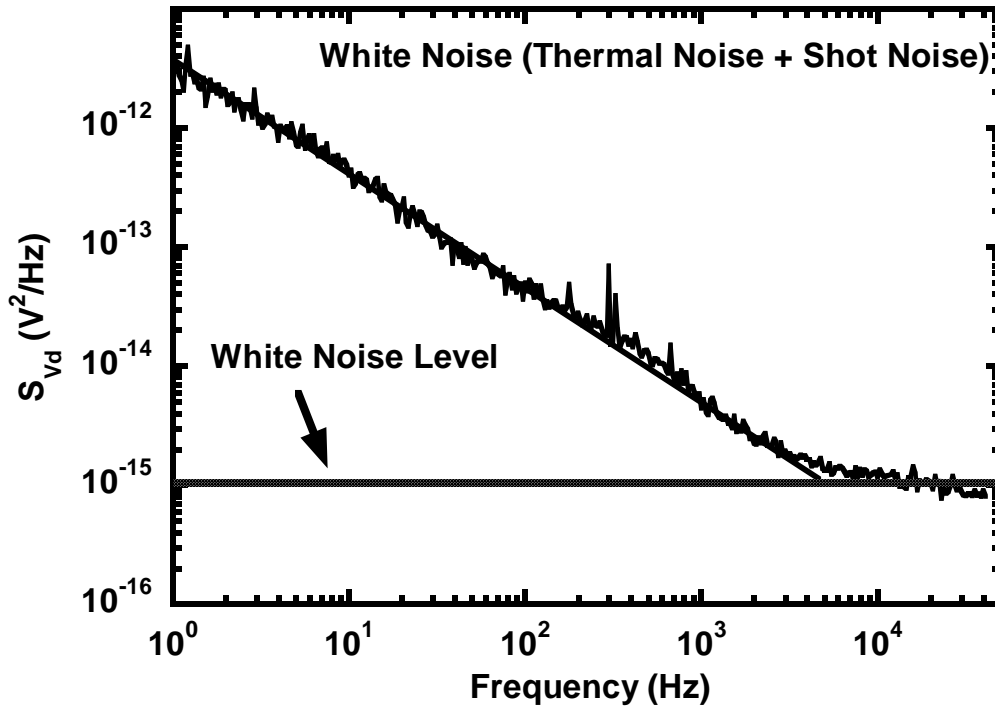
Figure 3.1 Typical MOSFET white noise at high frequencies. The device here is a TiN/HfSiO nMOSFET biased at $V_g = 1.13$ V and $V_d = 0.05$ V.

Shot Noise:

Shot noise current is generated when the electrons cross a potential barrier, like a pn-junction, independently and at random. The current across a barrier is given by the number of carriers, each carrying the charge *q*, flowing through the barrier during a period of time. The current flowing across a potential barrier is not continuous due to the discrete nature of the electronic charge. The expression for shot noise power spectral density takes the following form [43]

$$S_I(f) = 2qI \tag{3.2}$$

where, I is the DC current across the barrier. The physics behind the shot noise is closely related to the thermal noise phenomenon. The source of shot noise in MOSFET is due to the leakage current between the substrate and the channel. In addition, high gate leakage currents in ultra-thin MOSFETs can also be a source of shot noise [44,45,46]. Sometimes the shot noise is indistinguishable from thermal noise because of the flat nature of the frequency spectrum which is shown in Fig. 3.1.

Generation-Recombination Noise:

Generation-recombination (G-R) noise in semiconductors originates from traps that randomly capture and emit carriers. If the carriers are trapped in defects, the trapped charge can also induce fluctuations in the carrier mobility, diffusion coefficient, electric field, barrier height, space charge region etc. Each G-R center can be characterized by a trapping level in the energy band gap and by a relaxation time. The maximum G-R noise occurs for a center with energy at the Fermi level, resulting in equal capture and emission constants, where the noise spectrum becomes [42]

$$S(f) = 4\overline{\Delta N^2} \frac{\tau}{1+(2\pi f\tau)^2} \tag{3.3}$$

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Here, ΔN is the fluctuation in the number of carriers, τ is the characteristic trapping time constant, and f is frequency. The shape of the spectrum of the above equation (3.4) is called a Lorentzian.   G-R noise is only significant when Fermi level is with in a few kT energy close to the trap level. In that case the capture and emission time constant is almost equal, otherwise the traps will be filled or empty most of the time and few transitions occur that produce. Spectrum of a G-R noise component in a MOSFET noise spectrum is shown in Fig. 3.2.
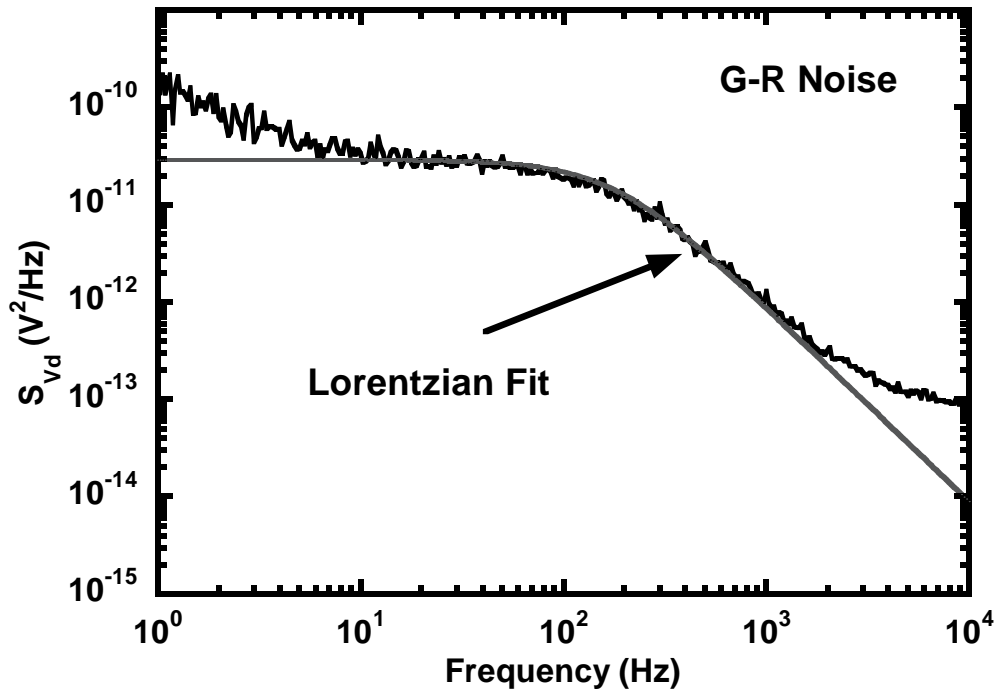
Figure 3.2 G-R noise in TaSiN/HfO$_2$/SiO$_2$ nMOSFET biased at V_g = 0.5 V and V_d = 0.05 V. The Lorentzian approximation is provided for reference [47].

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RTS Noise:

A special case of G-R noise is Random Telegraph Signal (RTS) noise. This noise is also known as burst or popcorn noise and observed in small area devices appearing in time domain as discrete random voltage or current switching events. If only a few traps are involved, the current can switch between two or more states resembling a RTS wave form due to random trapping and detrapping of carriers. For two level pulses with equal height ΔI and Poission distributed time duration $\bar{\tau}_l$ and $\bar{\tau}_h$ in the lower and higher state, the power spectral density of the current fluctuation is derived as [48,49]

$$S_{I_d}(f) = \frac{4(\Delta I)^2}{(\bar{\tau}_l + \bar{\tau}_h)[(1/\bar{\tau}_l + 1/\bar{\tau}_h)^2 + (2\pi f)^2]} \qquad (3.4)$$

Both RTS and G-R noise have a Lorentzian type power spectral density. G-R noise can be viewed as a summation of RTS noise processes from one or more traps with identical time constants, and is only displayed as RTS noise in the time domain. RTS noise is an interesting phenomenon since the random switching event from just one trap can be studied in the time domain. RTS noise can be observed in MOSFETs with small gate area (usually below 1 μm^2) where the gate oxide can have a single defect state causing trapping/de-trapping of a single channel carrier. The Lorentzian spectrum resulted from this trapping/de-trapping is shown in Figure 3.3 [50]. Interesting information about the trap energy, capture and emission kinetics and spatial location of the trap can be acquired from the RTS noise characterization.
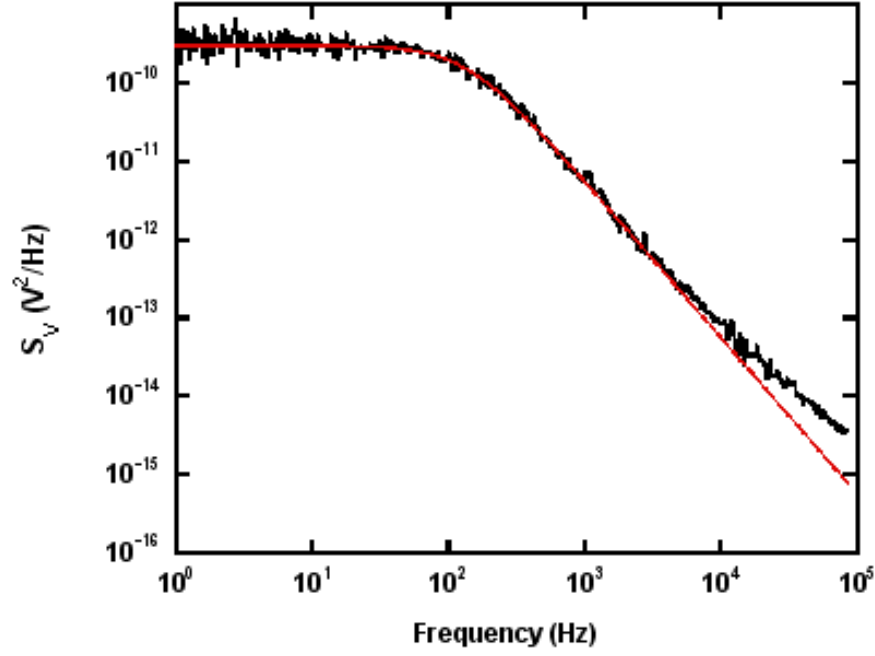
Figure 3.3 Voltage noise power spectrum of small area SiO_2 MOSFET biased at $V_g = 1.3$ V and $V_d = 0.05$ V along with a Lorentzian fitting [50].

Flicker Noise:

Flicker noise, also called as *1/f* noise, is a common name for fluctuations with power spectral density proportional to *1/f$^\sigma$*, with σ usually in the range 0.7~1.3. If I and C are the current flowing through the device and constant typical for the device, respectively, then the flicker noise can be expressed as [42]

$$\frac{S_I(f)}{I^2} = \frac{C}{f^\sigma}$$
(3.5)

Flicker noise is found in almost all electronic materials and semiconductor devices like MOSFETs, BJTs, JFETs, MESFETs and junction diodes [42,51,52].

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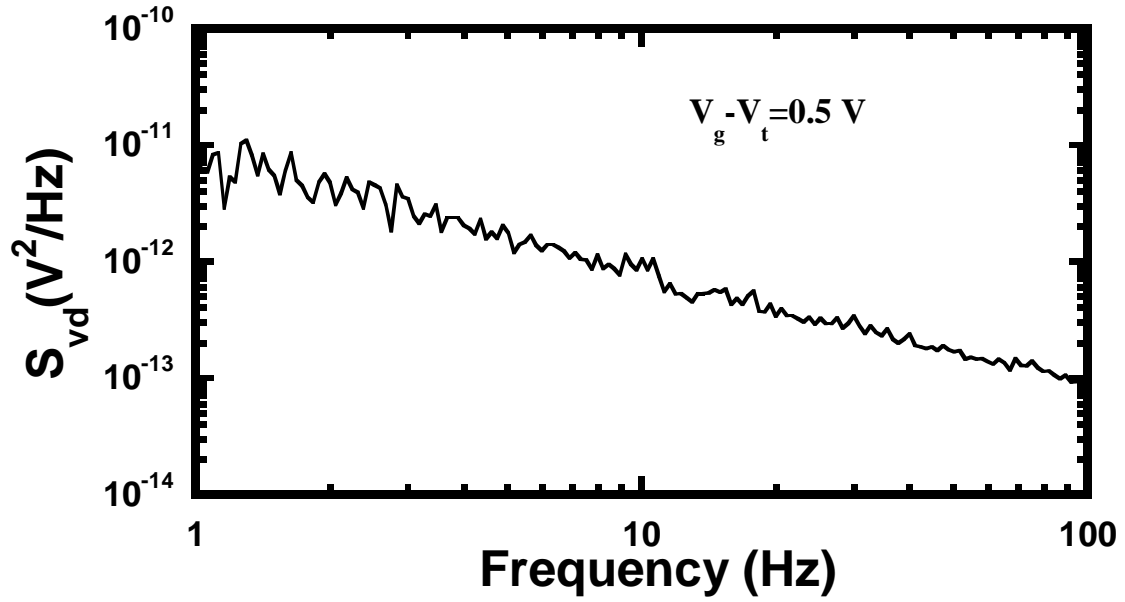
Figure 3.4 *1/f* noise for 10x0.25μm TiN/HfSiON nMOSFET sample with device biased at V_d=50 mV and gate overdrive $(V_g - V_t)$ = 0.5 V.

There are three different commonly accepted theories for flicker noise. They are carrier density fluctuation [53], mobility fluctuation [54] and correlated carrier number and mobility fluctuations models [55]. In the carrier density fluctuation model, the noise is explained by the fluctuation of free channel carriers due to the random capture and emission of carriers by the interface traps in the gate oxide/substrate region. The mobility fluctuation model considers flicker noise to be the result of fluctuations in the charge carrier mobility based on Hooge's empirical relation for the spectral density of the flicker noise in a homogeneous device. The last model, namely the correlated carrier number and mobility fluctuations model is also called the Unified Noise Model. According to the Unified Noise Model, the origin of *1/f* noise due to the trapping and de-trapping of interface traps cause fluctuations in both the carrier number and the mobility.

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3.3 *1/f* Noise Model in MOSFET device

3.3.1 1/f Noise in conventional (SiO₂) gate oxide MOSFET

The low cost integration possibility with logic circuits has made CMOS technology popular for many analog and RF applications. Effective and accurate noise models in circuit simulators are important for analog and RF applications. The possible physical mechanisms for *1/f* noise in MOSFETs have been studied for over a few decades now. In the following section, two most widely used *1/f* noise models for MOSFETS are discussed.

Hooge's Model:

The main mechanism for *1/f* noise according to Hooge's theory is the carrier mobility fluctuations. It has been proposed that the fluctuation of the bulk mobility in MOSFET is induced by the lattice scattering [56,57]. This was first described by Hooge with the following empirical formula [51]

$$\frac{S_{I_d}}{I_d^{\ 2}} = \frac{\alpha_H}{fWLN} \qquad\qquad (3.2.1)$$

Here, S_{Id} is the drain current power spectral density and α_H is Hooge parameter. 1/N results from independent mobility fluctuations by each of the N conducting carriers.

In the original derivation α_H, the dimensionless Hooge parameter was constant and equal to 2×10^{-3}. Later, it was found that crystal quality and phonon scattering affects α_H. Therefore, the following change is introduced in the calculation of α_H [57]

$$\alpha_H = 2 \times 10^{-3} \left(\frac{\mu_{eff}}{\mu_{latt}} \right)^2 \qquad (3.2.2)$$

Here, μ_{latt} is the mobility due to lattice scattering and μ_{eff} is effective mobility. According to Matthiessen's rule,

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{latt}} + \frac{1}{\mu_{imp}} \qquad (3.2.3)$$

In (3.2.3) μ_{imp} is the mobility due to impurity scattering.

Using (3.2.1) the drain current noise power spectral density for MOSFET device can be written as [58]

$$S_{\Delta I_d}(x, f) = \frac{\alpha_H}{fW\Delta x N} I_d^{\ 2} \qquad (3.2.4)$$

where, $\Delta N = NW\Delta x$, total number of carriers for an infinitesimal channel length Δx.

Now, for a MOSFET with a channel length, L, the total current noise spectral density can be obtained by integrating the above equation over the channel length

$$S_{I_d}(f) = \frac{\alpha_H I_d}{fL^2} \int_0^L \left(\frac{I_d}{W\Delta x N} \right) \Delta x dx \qquad (3.2.5)$$

The drain current is given by $I_d = -W\mu_{eff}(qN(x))\dfrac{dV}{dx}$,

Substituting the value of I_d in equation (3.2.5)

$$S_{I_d}(f) = \left(\frac{\alpha_H q \mu_{eff} I_d}{fL^2} \right) \int_0^L dV$$

Simplifying, for a MOSFET, Hooge's expression for the total current noise spectral density is given by,

$$S_{I_d}(f) = \frac{\alpha_H q \mu_{eff} I_d V_d}{fL^2}$$

Unified Noise Model:

The Unified Noise Model was originally proposed by Hung *et al.* [55]. According to this model, a trapped carrier will not only shift the flat-band voltage and thereby cause a fluctuation in the inversion charge density, but it will also affect the mobility. These fluctuations in the mobility are correlated to the fluctuating inversion charge density, both related to the trapping and detrapping of carriers in gate oxide traps as shown in Fig. 3.5. The two-fold effect that is, the fluctuations in the channel carrier number and the fluctuations in the mobility, arises due to the Coulombic interactions between the charged trap sites and the channel carriers. Most modern circuit simulator software packages such as BSIM make use of this model.
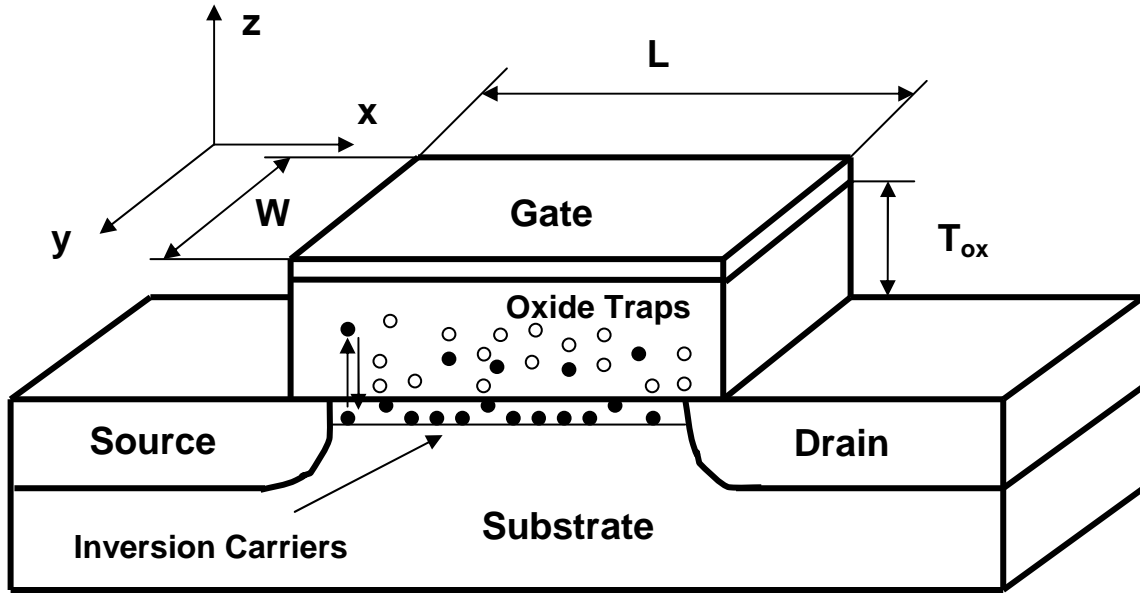
Figure 3.5 Cross section of a typical MOSFET showing trapping/de-trapping of inversion layer carriers by traps in the gate oxide [59].

The coordinate system used in the Unified Noise Model derivation below is as follows. x is along the channel length direction, y is along the channel width direction and z is along the direction of oxide thickness perpendicular to the device plane.

Using the above coordinate system, the drain current in a MOSFET with channel width W is given as,

$$I_d = W\mu_{eff}(qN)E_x \qquad (3.2.8)$$

where q is the electronic charge and E_x is the electric field along the channel.

For a section of channel length Δx in a MOSFET, fluctuations in the amount of trapped interface charge will introduce correlated fluctuations in the channel carrier concentration and mobility. The resulting change in the drain current can be expressed as [55]

$$\frac{\delta I_d}{I_d} = -(\frac{1}{\Delta N}\frac{\delta\Delta N}{\delta\Delta N_{ot}} \pm \frac{1}{\mu_{eff}}\frac{\delta\mu_{eff}}{\delta\Delta N_{ot}})\delta\Delta N_{ot} \qquad (3.2.9)$$

where, $\Delta N = NW\Delta x$ and $\Delta N_{ot} = N_{ot}W\Delta x$, and N_{ot} is the number of occupied traps per unit area. Depending on the type of traps, neutral or charged, the sign in front of the mobility term can be positive and negative. The ratio of the fluctuations in the carrier number to the fluctuations in the occupied trap number, which is defined as $R = \left|\dfrac{\delta\Delta N}{\delta\Delta N_{ot}}\right|$, is close to unity in strong inversion but assumes smaller values at other bias conditions. However, according [60], the expression in the weak inversion can be found by considering the small signal capacitive components. If Q_t is any change in the fluctuation in the trapped charge; the following expression can be written due to the conservation of charges in the MOSFET,

$$\delta Q_G + \delta Q_{it} + \delta Q_D + \delta Q_{inv} + \delta Q_t = 0 \qquad (3.2.10)$$

Where, Q_G, Q_D, Q_{inv} and Q_{it} are the induced fluctuations in the gate, depletion, inversion and interface trap charges, respectively.

Therefore, the ratio between channel charge and charge trapped in the gate oxide can be written as,

$$\frac{\delta\Delta N}{\delta\Delta N_{ot}} = \frac{\delta Q_{inv}}{\delta Q_t} = -\left(\frac{\delta Q_{inv}}{\delta Q_G + \delta Q_{it} + \delta Q_D + \delta Q_{inv}}\right) \qquad (3.2.11)$$

Now, denoting fluctuation in the surface potential as $\delta\psi_s$, the relationship between different charges and corresponding associated capacitances can be expressed as $\delta Q_G = -C_{ox}\delta\psi_s$,

$\delta Q_{it} = -C_{it}\delta\psi_s$, $\delta Q_D = -C_D\delta\psi_s$, $\delta Q_{inv} = -C_{inv}\delta\psi_s$

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Using the above equations, the coupling coefficient between fluctuation in the channel carrier number and the occupied trap number can be simplified as

$$R = \left| \frac{(q/kT)Q_{inv}}{C_{ox} + C_{it} + C_D - (q/kT)Q_{inv}} \right| = \frac{N}{N + N^*} \qquad (3.2.12)$$

where, $N^* = (kT/q^2)(C_{ox} + C_{it} + C_D)$ and $C_{inv} = -(q/kT)Q_{inv}$.

To evaluate $\dfrac{\delta\mu_{eff}}{\delta\Delta N_{ot}}$, the following equation based on Matthiessen's rule is used,

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{others}} + \frac{1}{\mu_{ox}} = \frac{1}{\mu_{others}} + \alpha_{sc}N_{ot} \qquad (3.2.13)$$

Here, μ_{ox} is the mobility due to oxide charge scattering, α_{sc} is the scattering co-efficient and is a function of the local carrier density due to channel charge scattering effect and μ_{others} is the mobility due to other scattering mechanisms.

Differentiating the above equation with respect to the number of occupied traps per unit area and substituting the value in (3.2.9) gives,

$$\frac{\delta\mu_{eff}}{\delta N_{ot}} = \alpha_{sc}\mu_{eff}^{\ 2} \quad \text{or} \quad \frac{\delta\mu_{eff}}{\delta\Delta N_{ot}} = \frac{\alpha_{sc}\mu_{eff}^{\ 2}}{W\Delta x} \qquad (3.2.14)$$

$$\frac{\delta I_d}{I_d} = -(\frac{1}{N} \pm \alpha_{sc}\mu_{eff})\frac{\delta\Delta N_{ot}}{W\Delta x} \qquad (3.2.15)$$

The power spectral density for drain current fluctuations is,

$$S_{\Delta I_d}(x, f) = \left[\frac{I_d}{W\Delta x}(\frac{1}{N} \pm \alpha_{sc}\mu_{eff}) \right]^2 S_{\Delta N_t}(x, f) \qquad (3.2.16)$$

Here, $S_{\Delta N_t}(x, f)$ is the power spectral density of the fluctuations in the number of the occupied traps over the area $W\Delta x$ and given by,

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$$S_{\Delta N_t}(x,f) = \int_{E_v}^{E_c} \int_0^W \int_0^{T_{ox}} 4N_t(E,x,y,z)\Delta x f_t (1-f_t) \frac{\tau(E,x,y,z)}{1+\omega^2\tau^2(E,x,y,z)} dEdydz \qquad (3.2.17)$$

where, $N_t(E,x,y,z)$ is the distribution of traps in the gate oxide and over the energy band, $\tau(E,x,y,z)$ is the trapping time constant in the gate dielectric, $\omega = 2\pi f$ is angular frequency, $f_t = \left[1 \big/ \left(1 + \exp[(E-E_{fn})/kT] \right) \right]$ is the trap occupancy function, E indicates the trap energy level, E_{fn} is the quasi-Fermi level, $E_c - E_v$ is the silicon energy band gap and T_{ox} is the oxide thickness. Since $f_t(1-f_t)$ behaves like a delta function around the quasi-Fermi level, the major contribution to the integral would be from the trap level around E_{fn}.

Now, $(1-f_t)$ in (3.2.17) can be written using the expression for f_t as,

$$(1-f_t) = \left[\frac{\exp[(E-E_{fn})/kT]}{\left[1 + \exp[(E-E_{fn})/kT] \right]} \right] \qquad (3.2.18)$$

Differentiating with respect to *E* gives

$$\frac{df_t}{dE} = -\frac{1}{kT} f_t (1-f_t) \qquad (3.2.19)$$

To evaluate the integral in equation (3.2.17) two assumptions are made. The first one is about the uniform spatial distribution of oxide traps near the gate oxide interface that is $N_t(E,x,y,z) = N_t(E_{Fn})$. The second assumption is that the probability of an electron entering the gate oxide decreases exponentially with distance from the interface. Therefore, the trapping time constant is given by from WKB (Wentzel-Kramer-Brillouin) approximation as [61]

$$\tau = \tau_0 \exp(\gamma z) \qquad (3.2.20)$$

where, τ_0 is the time constant at the oxide substrate interface and the value is 10^{-10} and

$\gamma = \dfrac{4\pi}{h}\sqrt{2m^*\Phi}$ is the attenuation coefficient of the electron wave function in the oxide. m^* is

the effective mass of an electron in the gate oxide and Φ is the barrier height for tunneling

carriers.

For an incremental distance dz in the oxide, the differential time constant $d\tau$ can then be

expressed as,

$$d\tau = \tau_0\gamma\exp(\gamma z)dz \qquad \text{or} \qquad \frac{d\tau}{\gamma\tau} = dz \qquad (3.2.21)$$

Using the expressions (3.2.19) and (3.2.21), the power spectral density of the fluctuations in the

number of the occupied traps can be evaluated as,

$$S_{\Delta N_t}(x, f) = \frac{N_t(E_{f_n})WkT\Delta x}{\gamma f} \qquad (3.2.22)$$

This gives the drain noise power spectral density as,

$$S_{I_d}(f) = \frac{kTI_d^{\,2}}{\gamma f WL^2}\int_0^L (\frac{R}{N(x)} \pm \alpha_{sc}\mu_{eff})^2\, N_t(E_{Fn})dx \qquad (3.2.23)$$

where, $N(x)$ is the local carrier density per unit area at a point x in the channel, and

$N_t(E_{Fn})$ considers the variation of quasi-Fermi level along the channel. Assuming a uniform

carrier distribution along the channel L, and $R=1$ due to strong inversion; equation (3.2.23) can

also be expressed in the following way,

$$S_{I_d}(f) = \frac{kTI_d^{\,2}}{\gamma f WL}(\frac{1}{N} \pm \alpha_{sc}\mu_{eff})^2\, N_t \qquad (3.2.24)$$

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3.3.2 1/f Noise in high-k gate oxide MOSFET

Although the Unified Noise Model [55] is the most successful low frequency 1/f noise model for the conventional SiO_2 gate dielectric devices, the extracted parameter values using this model show noticeable discrepancies when applied to devices using high-k materials as the gate dielectric [62]. Furthermore, significant dependence on the interfacial layer thickness has been observed in the extracted trap density values, although interfacial layer thickness is not a model parameter in the original Unified Model.
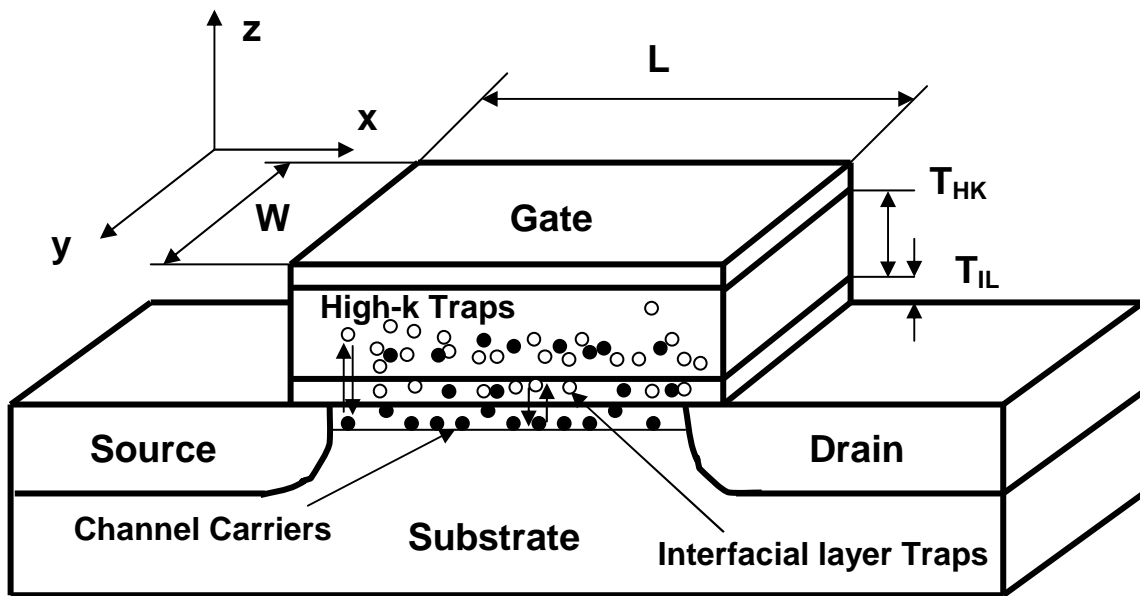
Figure 3.6 Typical structure of MOSFET with high-k/interfacial layer gate stack [59].

The original Unified Model was developed for conventional SiO_2 based MOSFET devices which differ from their high-κ gate stack counter parts both structurally and in material properties. In the former type, a single layer of SiO_2 is used as the gate dielectric material

whereas the high-κ gate stack usually comprises of a single or multiple layers of high-κ materials over a thin interfacial layer (typically of SiO_2). SiO_2 is regarded as an ideal dielectric material with a superior interface with Si substrate that gives lower interfacial trap density as well as a much cleaner dielectric bulk, since it is a mature technology. Compared to that, high-κ materials provide an interface with higher interface trap density [63] and a bulk dielectric with higher number of traps and charges compared with the conventional gate oxide material SiO_2 [64]. A typical structure of MOSFET device with high-k /interfacial layer gate stack is shown in Fig. 3.6.

In order to consider the above mentioned distinctive features for the high-k gate dielectric materials, a new model was developed based on the Unified Noise Model theory. The underlying mechanism affecting the low frequency noise characteristics of high-k MOSFETs used in this work was experimentally verified. The correlated number and surface mobility fluctuation model was determined as the dominant mechanism responsible for the observed noise behavior. The new model is named after the Unified Model as the MSUN (Multi Stack Unified Noise) Model [65].

As was mentioned earlier, for conventional MOSFETs, the main source of *1/f* noise has been shown to be the trapping and detrapping of channel carriers by the gate dielectric traps. According to this model, the noise power spectral density for local current fluctuations can be written in terms of the power spectral density for trapped charge carriers $S_{\Delta N_t}(x, f)$ as in equation (3.2.16). The first and second terms in Eq. (3.2.16) represent the fluctuations in the carrier number and mobility, respectively. In the conventional Unified Noise Model, $S_{\Delta N_t}(x, f)$ is computed assuming a trap center distribution that is spatially uniform in the oxide and also constant with respect to the electronic energy. This assumption is not suitable for high-k gate dielectric materials due to the presence of an interfacial layer (IL) –SiO_2 or SiON- between the

Si substrate and the high-k (HK) dielectric and the increased trapping sites that were shown to exist at the conduction band-edge of the high-k dielectrics [66,67].

According to newly proposed MSUN model [65], $S_{\Delta N_t}(x, f)$ can be represented as the summation of Lorentzians (generation-recombination noise) coming from both interfacial and high-k layers. Just as the original Unified Model, in the MSUN model, the interaction between the traps and the channel carriers occurs through a constant-energy tunneling [67]. However, unlike the original Unified Noise Model, MSUN also takes into account the non-uniformities in the energy and spatial distribution of the dielectric traps. Thus, $S_{\Delta N_t}(x, f)$ can be expressed as the summation of generation-recombination noise components originating from traps N_t located in the IL ($0 \leq z \leq T_{IL}$) and from those located in the high-k gate oxide ($T_{IL} \leq z \leq T_{HK}$) [65,67]

$$S_{\Delta N_t}(x, f) = 4kTW\Delta x \left[\left(\int_0^{T_{IL}} N_{tIL}(E_{fn}, z) \frac{\tau(z)}{1 + \omega^2 \tau^2(z)} dz \right) + \left(\int_{T_{IL}}^{T_{HK}+T_{IL}} N_{tHK}(E_{fn}, z) \frac{\tau(z)}{1 + \omega^2 \tau^2(z)} dz \right) \right]$$ (3.2.2.1)

Here, T_{IL} and T_{HK} are the thicknesses of the IL and HK layer respectively. Since the trap density in high-k materials is reported to be orders of magnitude higher than that for the interfacial layer [67] , *1/f* noise contribution from the interfacial layer can be neglected, thus simplifying Eq. (3.2.2.1) to

$$S_{\Delta N_t}(x, f) = 4kTW\Delta x \left[\left(\int_{T_{IL}}^{T_{IL}+T_{HK}} N_{tHK}(E_{fn}, z) \frac{\tau(z)}{1 + \omega^2 \tau^2(z)} dz \right) \right]$$ (3.2.2.2)

Based on previously reported results on the trap profile in MOS gate dielectrics, the high-k dielectric layer trap density, N_{tHK}, can be written as [68]

$$N_{tHK}(E_{fn}, z) = N_{tHK0} \exp[\xi_{HK}(E_{fn} - E_i) + (q\xi_{HK}(V_g - V(x))/T_{HK})z + \eta_{HK}z] \quad (3.2.2.3)$$

with N_{tHK0} being the mid-gap high-k dielectric trap density at the Si/HK interface.

This high-k gate oxide trap distribution with respect to energy is illustrated in the Fig. 3.7. Density of traps increases exponentially towards both the band edges and this rate of increment are defined by a fitting parameter ξ_{HK}.
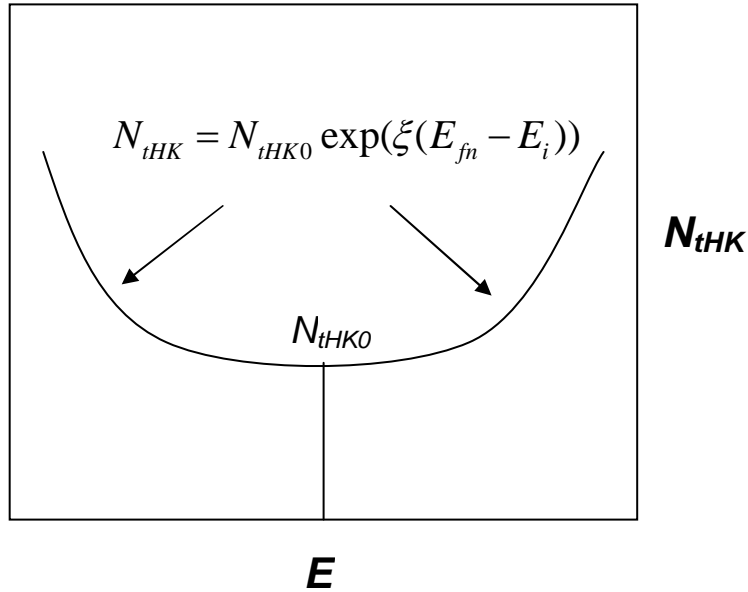
Figure 3.7 Variation of trap density profile with respect to energy in the high-k gate oxide region.

Fig. 3.8 illustrates band diagram of high-k MOSFET with HK and IL layer. Trap density profile in each layer is dependent on the corresponding dielectric layer parameters. The parameter ξ_{HK} represents the energy distribution of the trap density and the variation caused by band bending induced by V_g. The parameter η_{HK} corresponds to the spatial distribution of the high-k dielectric traps. $V(x) = \left(V_d / L\right)x$ is the channel potential due to horizontal field at a distance *x* from the source. E_i is the intrinsic Fermi levels at Si/oxide interface.
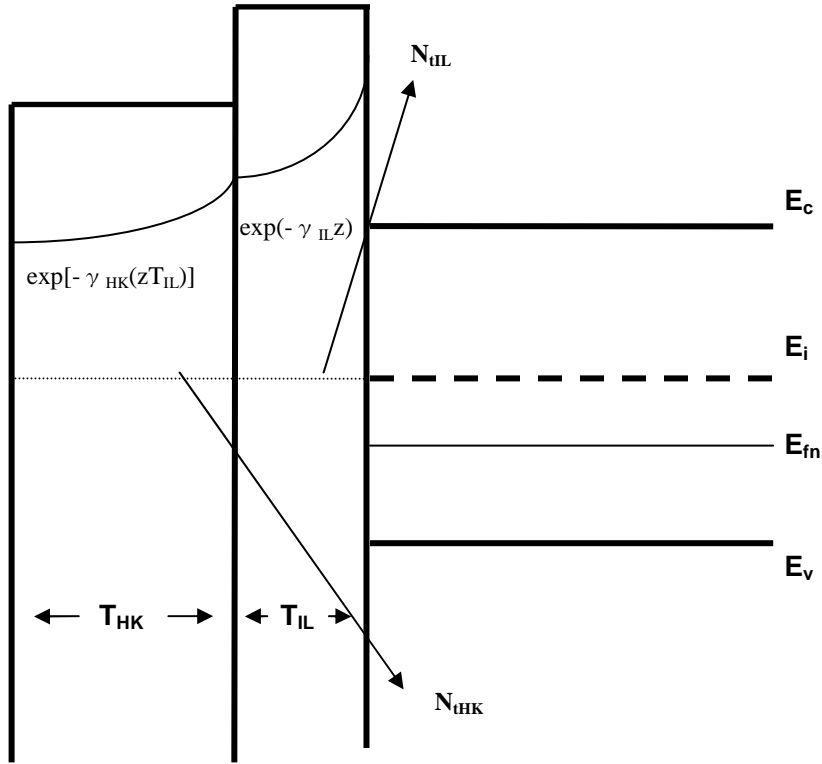
Figure 3.8 High-k MOSFET band diagram with high-k and interfacial layer [69].

According to the WKB approximation, the characteristic time constant for the channel carriers tunneling into the traps located in the gate oxide layer follows the equation (3.2.20). Here we take $\tau_0 = 10^{-10} s$ [70] ,and $\gamma_{HK} = 4\pi\sqrt{2m^*\Phi}/h$ [55]. If we define

$\beta_{HK} \equiv [(q\xi_{HK}(V_g - V(x))/T_{HK}) + \eta_{HK}]$ such that $\exp(\beta_{HK}z) = (\tau/\tau_0)^{\left(\beta_{HK}/\gamma_{HK}\right)}$, rearranging the above equations along with Eqs. (3.2.2.2), (3.2.2.3) and changing the integration variable to $\omega\tau = u$, the expression for $S_{\Delta N_t}(x,f)$ becomes [65]

$$S_{\Delta N_t}(x,f) = \frac{4kTW\Delta x}{\omega}\left[\frac{N_{tHK0}\exp[\xi_{HK}(E_{fn} - E_i)]}{\gamma_{HK}[\omega\tau_0]^{(\beta_{HK}/\gamma_{HK})}}\int_{\omega\tau_0}^{\omega\tau_0\exp(\gamma_{HK}T_{HK})}\frac{u^{(\beta_{HK}/\gamma_{HK})}}{1+u^2}du\right]$$

… … (3.2.2.4)

Since for our case the interfacial layer thickness was negligible, the integral is taken from z=0. It should be noted here that ξ_{HK} and η_{HK} modify the spectral form of the noise from pure 1/f through the $\omega^{\beta_{HK}/\gamma_{HK}}$ in term in (3.2.2.4), which is determined by the trap distribution.

The total drain current noise power spectral density obtained from Eqs. (3.2.16) and (3.2.2.4) is the summation of the fluctuations along the channel:

$$S_{I_d}(f) = \frac{1}{L^2}\int_0^L S_{\Delta I_d}(x,f)\Delta x dx \qquad (3.2.2.5)$$

3.4 Results and Discussion

3.4.1 Effect of nitridation on low frequency noise

Low frequency noise power spectral density was calculated based on MSUN model and

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compared to the data. ξ_{HK} and η_{HK} were extracted from the frequency exponent δ of $1/f^{\delta}$ spectral form, experimentally obtained from the devices in 1 – 100 Hz [68]. Since the main contribution of the total noise comes from the 1-100 Hz region in the high-k layer, ξ_{HK} and η_{HK} can be extracted as a slope and intercept from α versus gate bias plot as shown in Fig. 3.9.
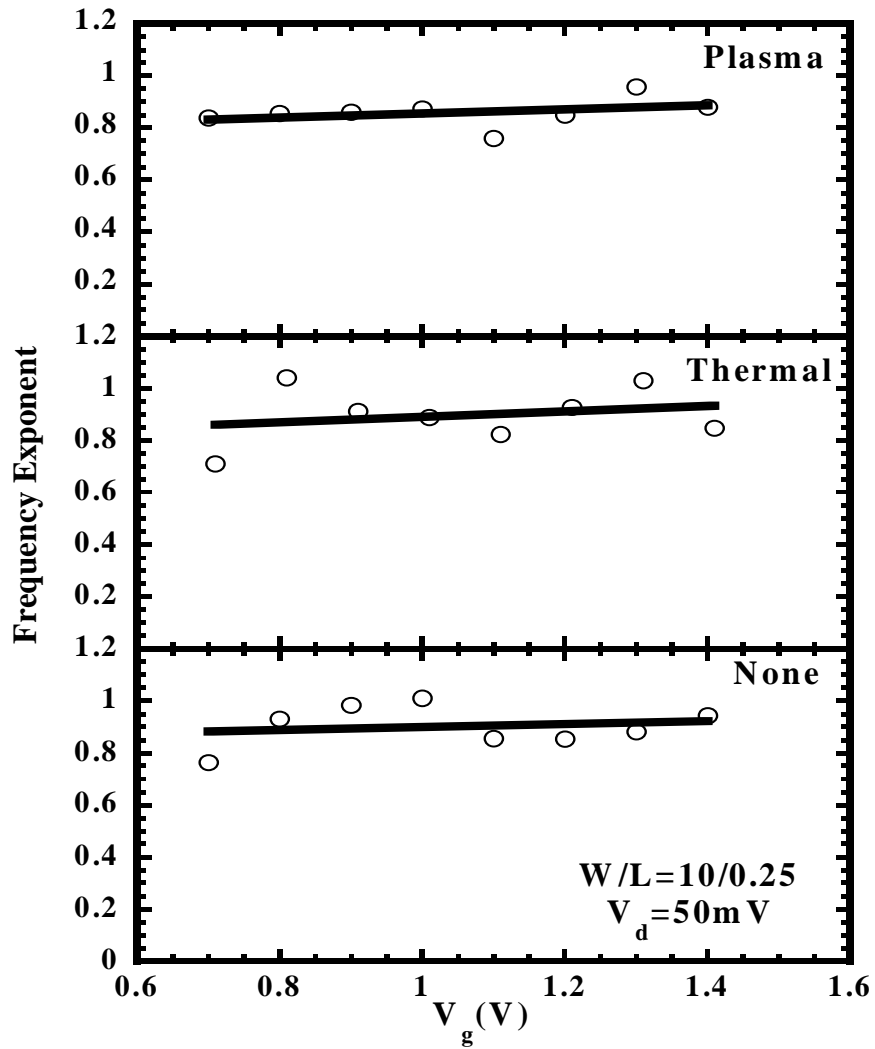
Figure 3.9 Frequency exponent α for 1-100 Hz range is plotted against gate bias to extract the fitting parameters ξ_{HK} and η_{HK}.

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Then, using these parameters, the noise magnitude was fitted in the entire frequency and bias range with a single set of N_{tKH0} and μ_{c0} for each process split [71]. μ_{c0} is a fitting parameter that indicates the effectiveness of the screening by the channel carriers. This is defined as $\alpha_{sc} = \dfrac{1}{\mu_{co}\sqrt{N}}$.

Figure 3.10 shows a typical noise PSD for plasma nitrided sample in 1-100Hz frequency range. A power-fitting is done to get the frequency exponent and the fitted noise value at 1Hz, which is used to obtain S_{ld} at 1 Hz.
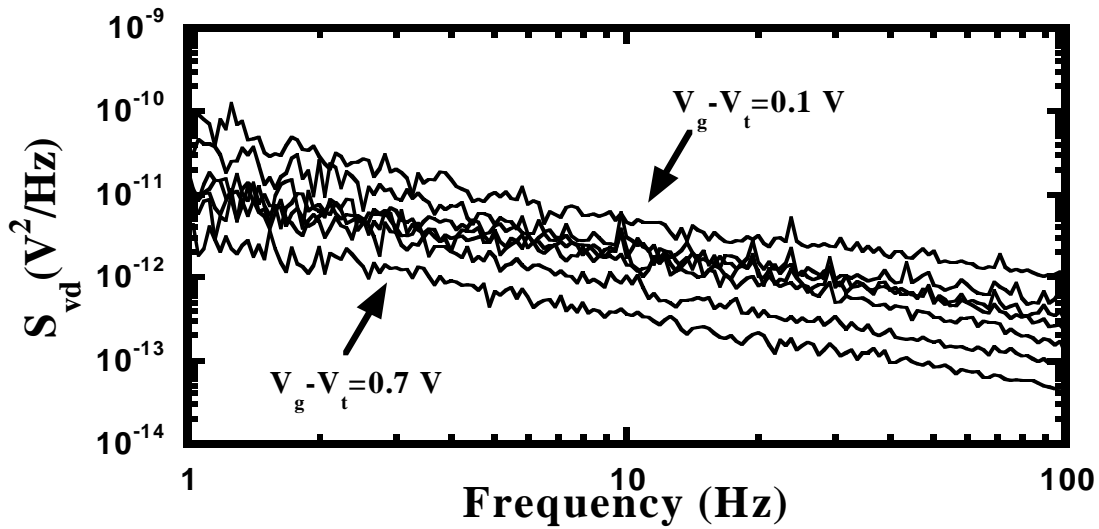
Figure 3.10 Typical drain voltage noise power spectra plot for 10x0.25µm TiN/HfSiON nMOSFET for plasma nitrided sample with device biased at V_d=50 mV and gate overdrive *(V_g-V_t)* varying from 0.1 to 0.7 V.

Validity of number fluctuation model for the observed data can also be evaluated by a simple technique developed by Ghibaudo to differentiate two *1/f* noise mechanisms responsible for the observed noise power spectral density in MOSFETs [72]. If Hooge's theory of bulk mobility fluctuations [73] is responsible for the noise, then the normalized noise S_{ld}/I_d^2 would

follow I_d^{-1}. On the other hand, if correlated number / mobility fluctuations are dominant, as in the case of the Unified Noise Model, then $S_{Id}/I_d^2 \propto (g_m/I_d)^2$. In our case, since S_{Id}/I_d^2 (1 Hz value) follows the same trend as $(g_m/I_d)^2$, carrier number fluctuations are the dominant *1/f* noise mechanism rather than bulk mobility fluctuations. Based on these results, the validity of the MSUN model was explored, which is a variation of the number fluctuations. Figure 3.11 shows the validity of number fluctuation model for the observed data.

The current noise power spectra for $V_g - V_t = 0.3V$ and $V_d = 50mV$ are depicted in Fig. 3.12 along with the fitted line using the MSUN model for all three different process splits. Here, the negative value for η_{HK} indicates a decreasing trap density profile from high-k /Si interface to the bulk of the high-k dielectric. For the parameter ξ_{HK}, positive value represents an increase in the effective trap density the carriers would experience with quasi-Fermi level approaching the conduction bend edge (increasing trap energy).

Figure 3.13 shows the experimental data for the current noise power spectral density at 1 Hz for different gate overdrive voltages as well as the predictions of the model obtained by choosing appropriate values for the fitting parameters [71]. Higher value of μ_{C0} indicates lower contribution to mobility fluctuations from Coulomb scattering sites [74].

The overall *1/f* noise performance is also evaluated for differently nitrided samples. Fig. 3.14 shows the overall *1/f* noise for differently nitrided MOSFETs along with the pure HfSiO sample. Among three different samples, thermaly nitrided samples showed the highest *1/f* noise compared to the plasma and HfSiO samples. Here, in order to compare the inherent noise exhibited by MOSFETs with different I-V characteristics and EOT, the drain voltage noise has

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been first converted to drain current noise PSD [$S_{I_d} = S_{V_d} \cdot (g_d)^2$] then divided by I_d^2 to obtain the noise spectral density in Hz[-1]. According to number fluctuation theory, the noise power is inversely proportional to MOSFET channel area and the square of the gate oxide capacitance [75,76]. Therefore, for MOSFETs with the same channel area, S_{I_d}/I_d^2 was multiplied by C_{EOT}^2 to obtain the device inherent noise.

The highest normalized *1/f* noise (Fig. 3.14) has been attributed to the increased number of Coulomb scattering sites caused by Si-N bonds near the HK/Si interface of thermally nitrided samples due to the higher processing temperatures which drive most of the nitrogen to the interface [71, 65]. The nitrogen profile differences caused by different nitridation techniques seem to play an important role in the observed noise. Better control of the nitrogen profile in the high-k/Si at interface and the bulk of the high-k gate material reduces electron mobility fluctuations leading to lower noise for the plasma nitrided device [77].

In order to find out the effect of different nitridation techniques on the *1/f* noise characteristics, number and mobility fluctuation components are separated in Eq. (3.2.16) using the MSUN model [65]. Figure 3.15 shows the noise components due to number and mobility fluctuations at various gate overdrive voltages for three different samples. From this Figure, it is apparent that the contribution from mobility fluctuations is lower than that of the number fluctuations. The number fluctuations are not influenced by the nitrogen incorporation techniques, whereas the mobility fluctuations are significantly affected. Thermal nitridation shows the highest mobility fluctuation component. This might be explained by the increasing number of Coulomb scattering sites, caused by the Si-N bonds near the interface due to high thermal budget [78] .However better control of N profile over the interface and bulk of high-k gate oxide for the plasma nitrided sample, causes reduced mobility fluctuations [77].
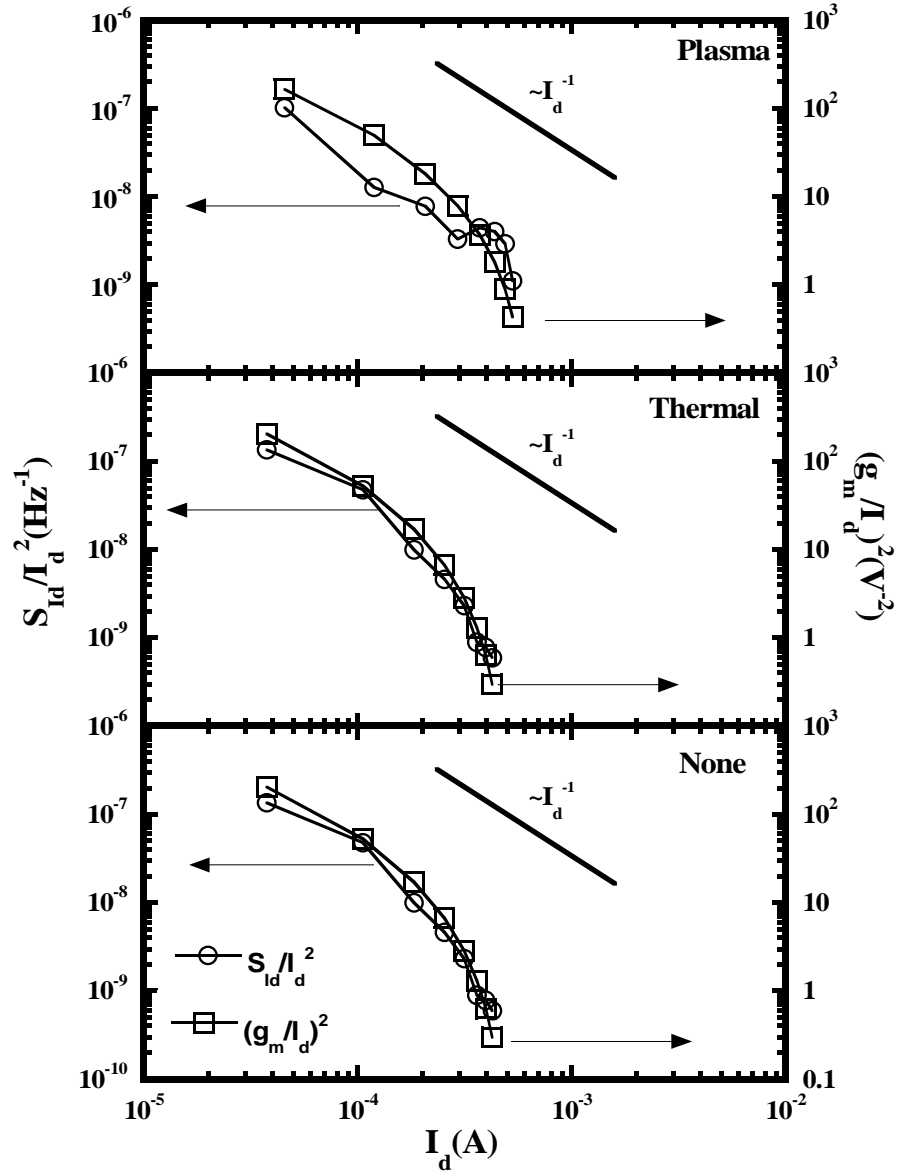
Figure 3.11 S_{Id}/I_d^2 and $(g_m/I_d)^2$ vs. I_d to determine the physical mechanism responsible for 1/f noise (S_{Id} at 1 Hz). Since S_{Id}/I_d^2 and $(g_m/I_d)^2$ follow the same trend, charge carrier number fluctuations are the dominant physical mechanism causing noise.
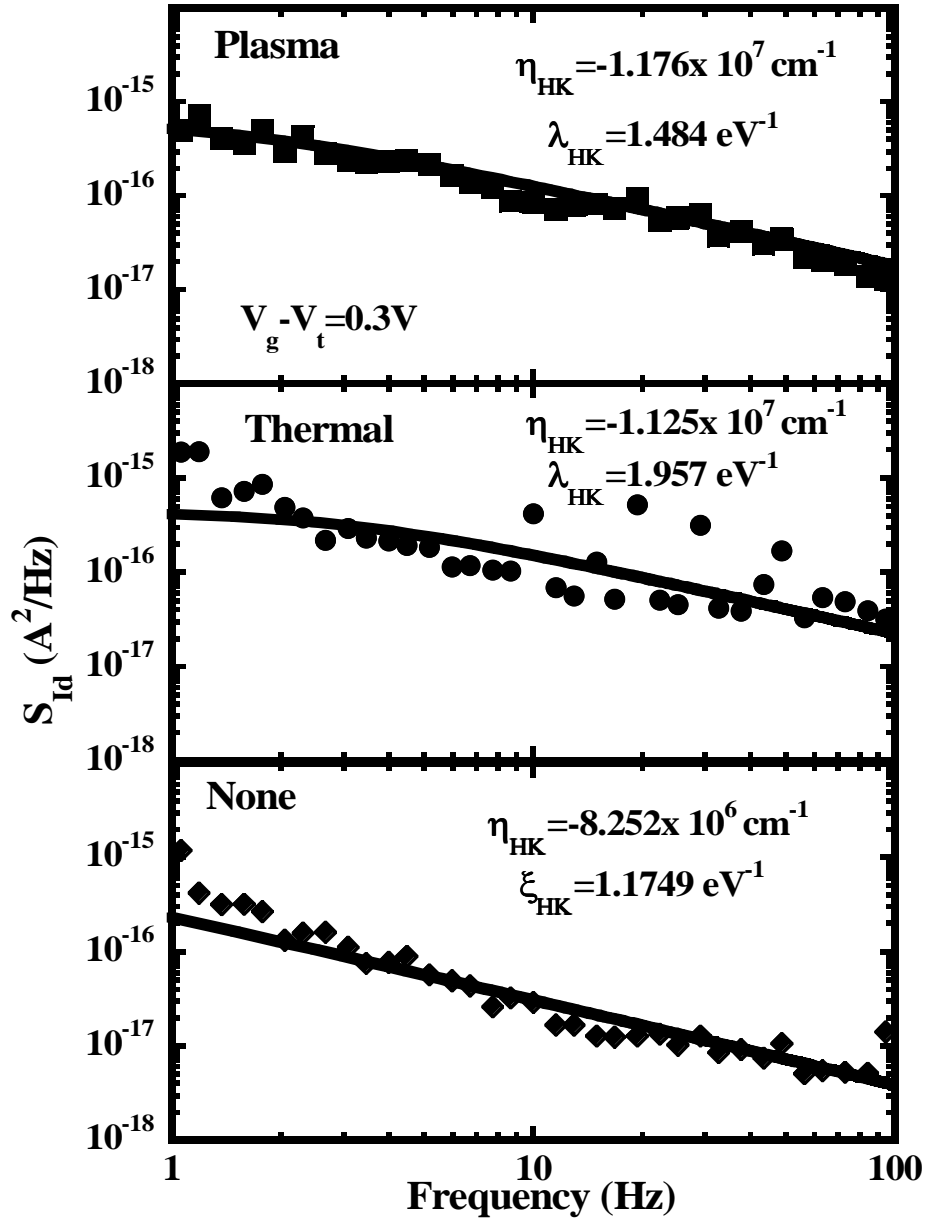
Figure 3.12 Measured noise spectra in the 1-100Hz frequency range for devices biased at V_g-V_t=0.3 V and V_d =50mV along with the MSUN model fitted to the data with the four modeling parameters.

This result is also consistent with the fitting parameter values. Higher N_{tHK0} and ξ_{HK} values mean larger number of traps which in turn increases the noise magnitude. N_{tHK0} and ξ_{HK} values for the thermally nitrided samples are larger than the plasma nitrided and pure HfSiO samples. On the other hand, a lower value of screened Coulomb scattering coefficient α_{sc}, which is defined as $1/\left(\mu_{C0}\sqrt{N}\right)$, means better screening of the trapped-charge Coulomb scattering [74]. This, in turn, reduces the mobility fluctuation component. Thermally nitrided samples showed the least μ_{C0} value compared to the plasma nitrided samples. This indicates less screening of the trapped charge for the thermal nitrided sample than that for the plasma nitrided sample. Highest value of μ_{C0} for HfSiO sample implies the lowest screening of the trapped charges by the channel carriers. These parameters also indicate a decreasing trap profile from the HK/Si interface to the bulk of the gate oxide for plasma and thermally nitride samples. A list of extracted MSUN model parameters are shown in Table 3.3.1

Table 3.1 Extracted MSUN Model Parameters

Sample Spec	μ_{co}(cm/Vs)	N_{tHK0}(cm^{-3} eV^{-1})	ξ_{hk} =λ_{hk}(eV^{-1})	η_{hk}(cm^{-1})
Plasma	1.2×10^{9}	1.3×10^{19}	1.4846	-1.18×10^{7}
Thermal	1.0×10^{9}	2.8×10^{19}	1.957	-1.13×10^{7}
None	5.0×10^{9}	5.0×10^{19}	1.1749	-8.26×10^{6}

3.4.2 Effect of nitridation on HCS and CVS induced low frequency noise degradation

A lot of emphasis has been given to the *1/f* noise performance of various mixed signal circuits with Hf based high-k gate dielectric MOSFETs [79,80,81]. Since low frequency noise is a growing concern for analog and mixed signal CMOS circuit design, it is therefore important to

characterize the *1/f* noise not only for fresh devices but also devices under different stressing conditions. This was the motivation behind studying the effect of different stressing conditions on *1/f* noise performance. The noise degradation was systematically studied in plasma and thermally nitrided HfSiON and HfSiO devices under Hot Carrier (HCS) and Constant Voltage Stress (CVS) conditions.

The so-called worst degradation condition ($V_g=V_d$) was chosen for HCS for these devices [82]. For MOSFETs with thick gate oxide (>5 nm) and long channel lengths, the substrate current (I_{sub}) is usually taken to monitor the hot carrier damage. In n-MOSFETs, holes generated during HCS due to impact ionization flow out of the substrate contact as I_{sub}, whereas the electrons contribute to the drain current I_d. If the electrons are injected into the oxide, this constitutes the gate current I_g. Since typically the substrate current shows a bell shaped trend with respect to the gate voltage (V_g), with the maximum degradation occurring around $I_{sub,max}$, it is assumed that the maximum HCS damage takes place at V_g for $I_{sub,max}$. [83]. A different condition, however, was reported to be true for short-channel MOSFETs with high-k dielectric gate oxides. In this work, the worst degradation condition was shown to be at $V_g=V_d$ rather than $I_{sub,max}$ [84]. In our work, we adopted the latter procedure for HCS. For CVS measurements, the vertical electric field was fixed at 10MV/cm.

1/f noise and dc characteristics were taken before and after applying the stress for 1000 s. Degradation in saturation drain current ($I_{d,sat}$) and maximum transconductance ($g_{m,max}$) was monitored by measuring I_d-V_g characteristics after 1000s of stress. The range of the gate bias was limited to 0-1.5 V to minimize additional stress on the device during I_d-V_g measurements.
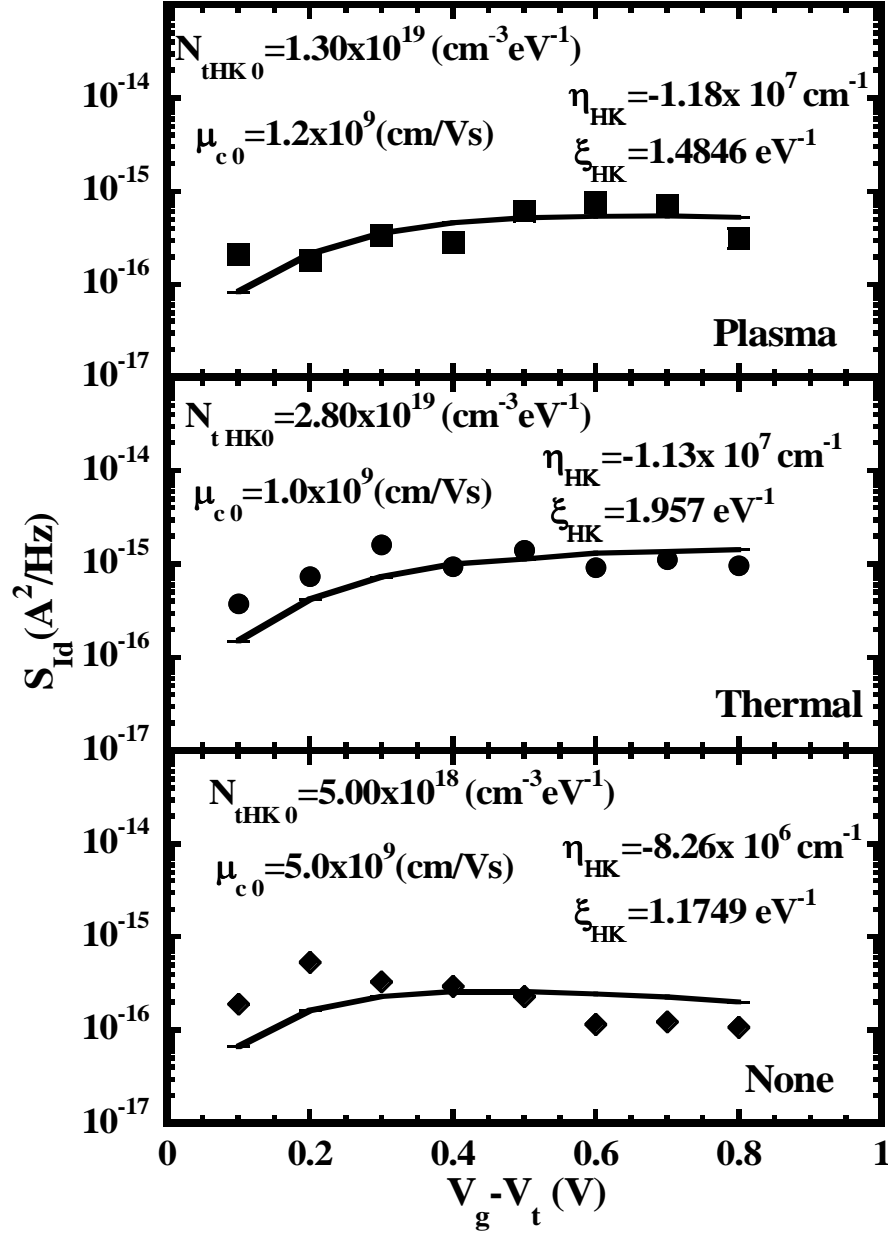
Figure 3.13 Typical fitting obtained between the measured current noise power spectral density at 1 Hz and the model predictions (solid line), using the MSUN model. Plasma and thermally nitrided HfSiON samples are compared to the pure HfSiO sample (none).
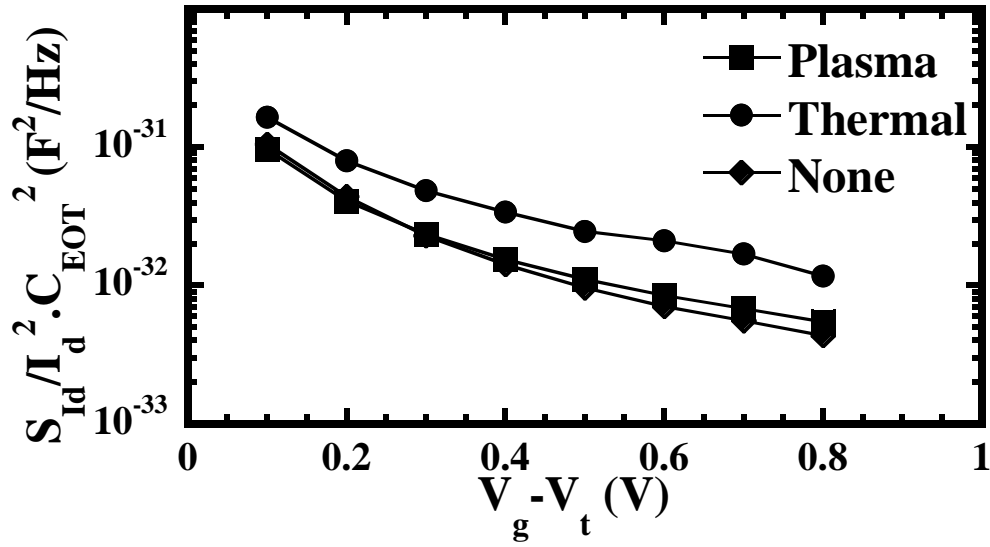
Figure 3.14. Total *1/f* noise for differently nitrided samples along with the pure HfSiO sample
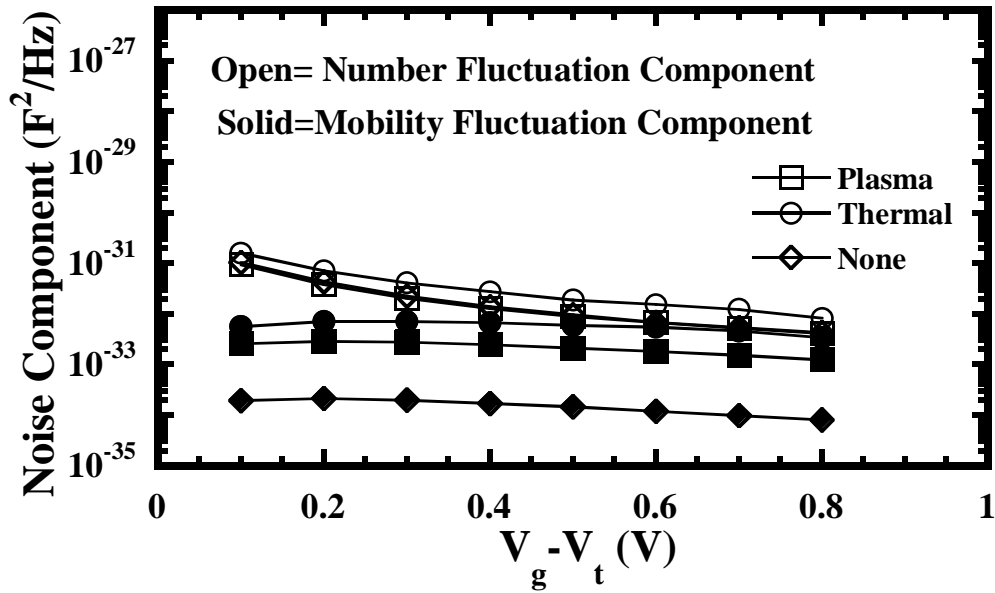
Figure 3.15 Number (Open Symbols) and mobility (Solid Symbols) fluctuation components of the drain current noise power spectral density measured at 1 Hz versus gate overdrive for three different process splits. Thermally nitrided samples show the highest 1/f noise.

3.4.2.1 Effect of HCS and CVS on transconductance and threshold voltage

Among three differently processed samples, thermally nitrided device showed the most degradation in its $_{d,sat}$, $g_{m,max}$ and V_{th} compared to the plasma nitrided and pure HfSiO samples (Table 3.3.2). This higher degradation in thermally and plasma nitrided HfSiON is attributed to the presence of nitrogen. The nitrogen profile in HfON and HfSiON gate dielectric layers has been shown to have a profound effect on the PBTI induced by constant voltage stressing as measured by the amount of shift in V_{th} and $g_{m,max}$ [85,77].

After applying HCS, both forward and reverse mode I-V characteristics were taken (Fig 3.16). If the HCS induced degradation is due to only hot carrier-generated defects in the high-k/Si interface layer, then the damage would be localized primarily in the drain region. Hence, there would be a difference in the drain current between the forward and the reverse measurement modes. None of the samples showed such a difference in their drain current characteristics. Therefore, both hot and cold carriers are responsible for HCS induced dc characteristic degradation for all three different samples. This conclusion is consistent with the results reported by Sim et al. [84] who observed concurrent charging of the bulk dielectric by the cold channel carriers injected into the HfSiON gate dielectric during HCS. They attributed the electron trapping and de-trapping in the bulk of the dielectric with HCS to the high density of structural defects already existing in the high-k dielectric compared to the native oxide.

It is well established that V_{th} shift reflects the bulk property degradation of gate oxide. Hence the highest shift in V_{th} for thermally nitrided sample due to HCS is attributed to the trapping of charges at the bulk of the gate oxide [86]. This is contrary to what is typically observed in short-channel MOSFETs with native gate oxide, where the damage occurs primarily at the Si/SiO_2 interface during HCS. It is, however, consistent with the threshold voltage

instabilities observed by Zafar et al. [87], who explained these through charge trapping by existing bulk traps in the high-k dielectric.

Table 3.2 Stress Induced Degradation for Different of $g_{m,max}$, $I_{d,sat}$, and V_{th} for Different Samples

Type of Stress	Percent Degradation								
	Plasma Nitrided			Thermally Nitrided			No Nitridation		
	$g_{m,max}$	$I_{d,sat}$	V_{th}	$g_{m,max}$	$I_{d,sat}$	V_{th}	$g_{m,max}$	$I_{d,sat}$	V_{th}
Constant Voltage (CVS)	0.27%	1.72%	5.07%	5.54%	10.6%	6.95%	0.62%	3.85%	2.89%
Hot Carrier (HCS)	3.62%	4.19%	7.46%	5.8%	7.31%	10.76%	1.14%	1.69%	2.89%
Hot Carrier – Reverse Mode Measurement (HCSR)	3.8%	4.75%	4.76%	5.1%	6.43%	10.76%	2.18%	2.72%	2.89%

It should be noted from Fig. 3.16 that the transconductance characteristics exhibit a shift with CVS in plasma nitrided and pure HfSiO samples, but no degradation in $g_{m,max}$, very similar to the results reported by Krishnan et al. [77] who concluded that the shift in the I_d-V_g curves is an indicative of increased electron trapping, but not interface defect density increase. Thermally nitrided sample, on the other hand, showed degradation in $g_{m,max}$, due to N pile up and increased Si-N bonds at the interface because of the higher thermal budget [78]. Higher $g_{m,max}$ degradation was observed also by HCS for both thermal and plasma nitrided samples indicating significant interface degradation as well.

3.4.2.2 Effect of HCS and CVS on low frequency noise characteristics

In order to monitor stress induced noise degradation, the low frequency noise characteristics is measured every time after applying stress.

Hot carrier stress induced degradation mechanism in high-k gate dielectric devices is different than that seen in conventional SiO_2 gate dielectric devices due to the relatively high trap density. The total degradation of threshold voltage cannot be explained only by interface trap generation. Significant portion of the degradation might come from cold carrier trapping due to the accumulation nature of the hot and cold carrier at the high-k layer during hot carrier stress [84]. In LFN characteristics, lower frequency corresponds to tunneling to the traps further away from the HK/Si interface and higher frequency corresponds traps near HK/Si interface. For these ultrathin HK gate oxide devices, we are probing the defects close to TiN/High-k interface. Therefore, noise power spectral density can also be used as a tool to evaluate the spatial distribution of traps in the high-k gate oxide after applying stress.

Forward and reverse mode noise behavior after HCS for 1000s is shown in Fig. 3.17. Here, no normalization is required for the measured noise, since the devices are compared before and after stressing conditions. For plasma nitrided sample, the increase in noise in higher frequency range implies that increased trap density close to the high-k/Si interface is more dominant due to HCS than thermally nitrided and pure HfSiO samples, whereas increased noise in the lower frequency range region for the thermal nitrided sample points to the traps further into the dielectric. This is consistent with the observed shift in V_{th} for the thermally nitrided samples – mentioned earlier – with HCS, implying bulk degradation of the dielectric and therefore increased noise at lower frequencies [88].

The MOSFETs were subjected also to constant voltage stress (CVS), applied at the gate terminal for 1000s while source, drain and substrate terminals were grounded. Fig. 3.18 shows the drain voltage noise PSD for $V_g - V_t = 0.3V$ for three different samples. The vertical electric field was fixed at 10MV/cm for all devices. For plasma nitrided HfSiON and HfSiO devices, there is a slight increase in noise. However, the thermally nitrided sample showed an order of magnitude increase in noise. This might be due to the electrons filling the existing traps and increased charge damages created during the CVS. For the thermally nitrided sample, high concentration of nitrogen at the interface as well as damage near HK/metal gate stack due to CVS causes higher noise. Moreover, oxygen vacancies are also likely candidates for intrinsic electron traps in devices and threshold voltage instability [89]. In plasma assisted nitridation, atomic nitrogen is introduced in to the system. This nitrogen incorporation into oxygen vacancy sites results in lowering of the defect level and making them less active as electron traps, Whereas thermal nitridation in NH_3 ambient at high temperatures results in a higher concentration of protons, leading to an increment in positive charge centers [90] and noise due to Coulomb scattering from these centers.

This increase of order of magnitude in noise after CVS measured on thermally nitrided devices throughout the entire frequency range is consistent with the observed highest degradation of $g_{m,max}$ and V_{th} in these MOSFETs, which indicate both interface and bulk oxide degradation are present.
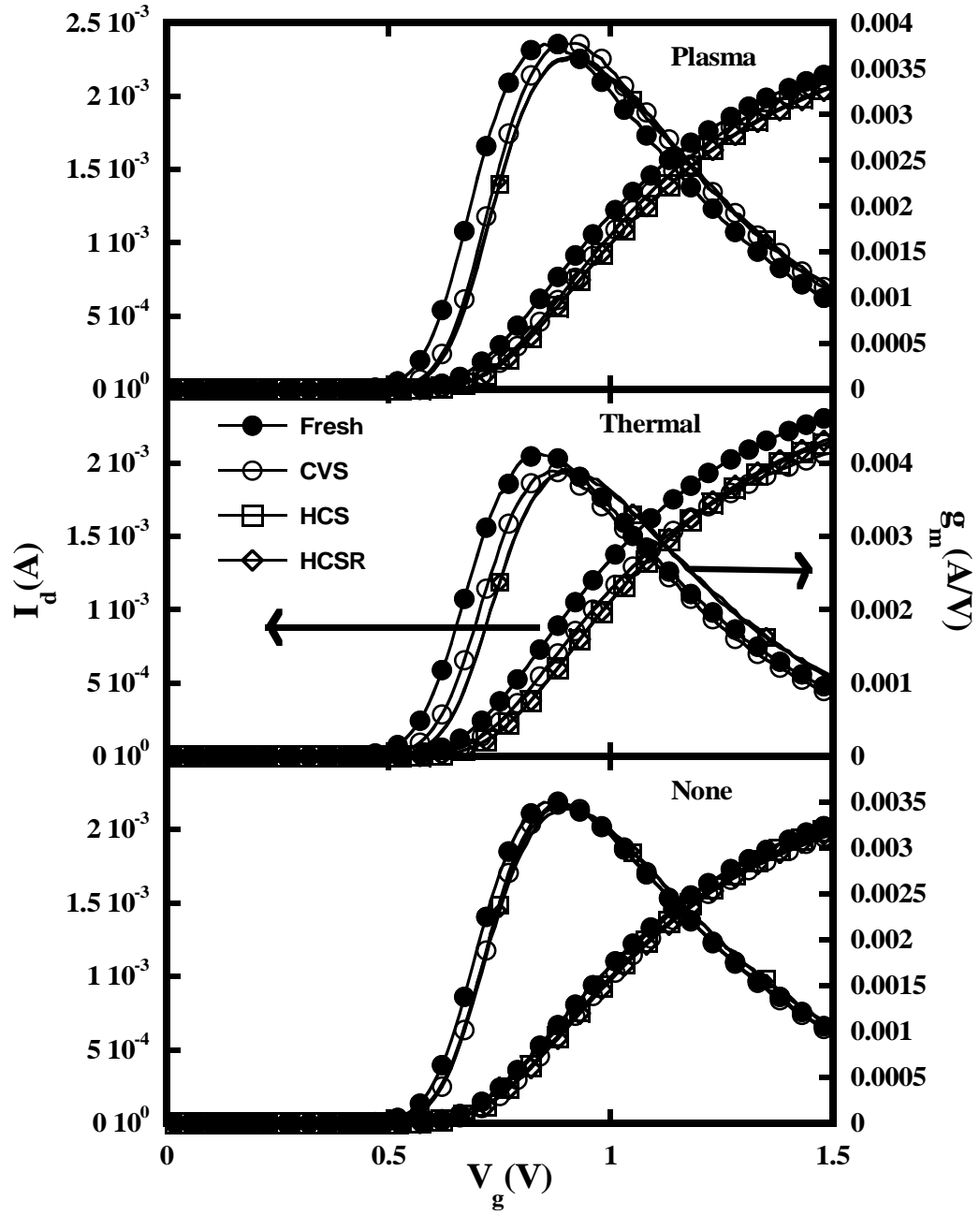
Figure 3.16 Drain current and transconductance characteristics of three different nMOSFETs after hot carrier and constant voltage stress, measured in forward and reverse modes. Gate area is 10 x 0.1 µm^2. Plasma and thermally nitrided gate dielectrics to obtain HfSiON are compared to pure HfSiO (none).
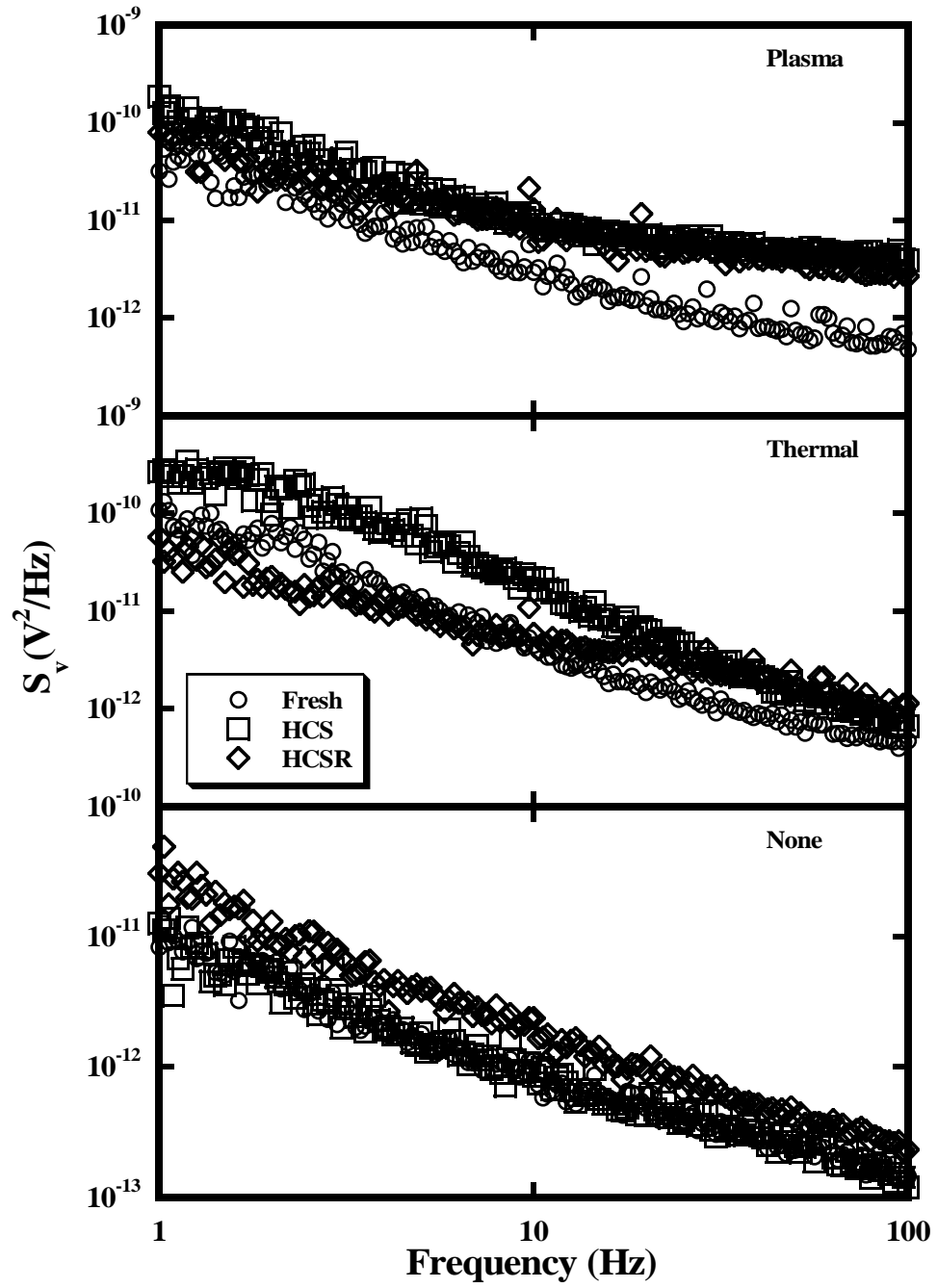
Figure 3.17 Drain voltage noise power spectral density at V_{ds}=50 mV and $(V_g\text{-}V_t)$=0.3 V after applying constant voltage stress at the gate for 1000s on 10 x 0.1µm^2 nMOSFET. HCS: Hot carrier stressing. HCSR: Hot carrier stressing, reverse mode measurement.
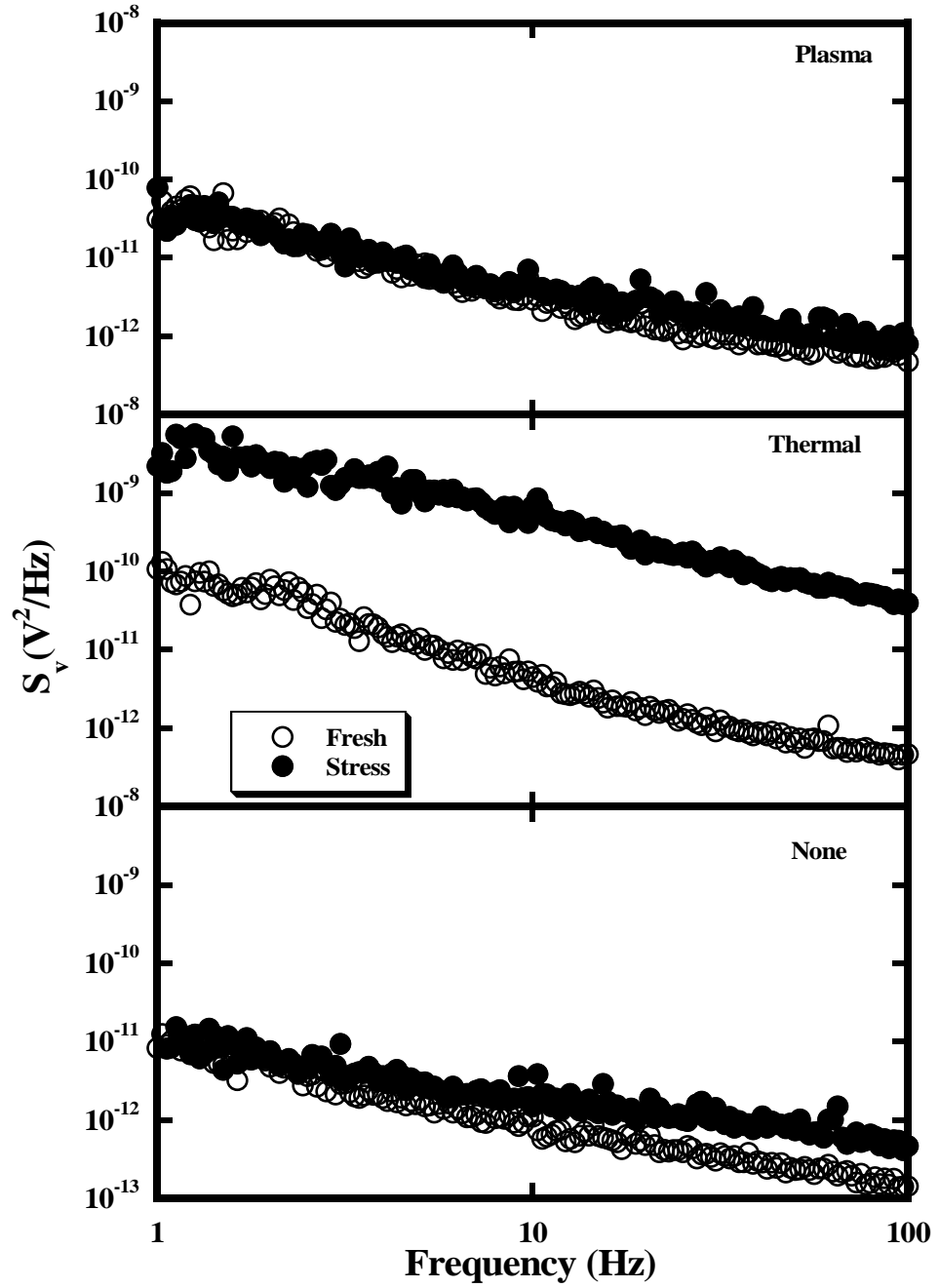
Figure 3.18 Noise characteristics of two differently nitrided HfSiON nMOSFETs along with HfSiO device. V_{ds}=50mV and $(V_g$-$V_t)$=0.3 V. Gate area is 10 x 0.1 µm². Constant voltage stress of 10MV/cm is applied at the gate terminal for 1000s.

3.5 Summary

A comparative study has been provided regarding a new model named MSUN Model for multi layer gate dielectric MOSFETs. In addition, low frequency noise behavior is discussed for differently nitrided HfSiON and HfSiO samples. Thermally nitrided HfSiON shows the highest 1/f noise compared to plasma nitrided and HfSiO samples. Due to different stressing, mainly hot-carrier and constant voltage, increased low frequency noise is observed for nitrided HfSiO gate dielectric MOSFETs. Thermal nitridation of HfSiO to obtain HfSiON using high temperature NH_3 anneal compounded the degradation for both types of stressing, most likely due to the increased dielectric traps in nitrided samples, which get filled during stressing and become channel carrier scattering sites. This problem can be alleviated to an extent by using plasma nitridation done at much lower temperatures. Plasma nitrided devices showed lower *1/f* noise than thermally nitrided devices, even though thermally nitrided devices scaled down the EOT (1.03nm) slightly more than plasma nitrided devices (1.06nm) for the same nitrogen content and initial HfSiO thickness.

CHAPTER 4

DEVELOPMENT OF RF MEMS PACKAGING

4.1 Introduction

MEMS packaging has been more of a challenge than conventional semiconductor devices due to its inherent characteristics. As sensors, MEMS devices are required to be exposed to the agent(s) that they are detecting. As actuators, the geometrically complex moving parts need protection. Moreover, there might be specific requirements such as optical windows, vacuum or hermetic environments. This makes MEMS especially sensitive to damage and contamination during fabrication and packaging process. As MEMS contain fragile movable parts or need to be operated in a specific atmosphere, standard packaging technologies developed for IC cannot be directly used for MEMS devices. Most RF-MEMS devices such as varactors, switches and resonators are devices that respond mechanically to some electrical input signal. Stringent device performance requirements have driven the need for a packaging method that is robust, easily fabricated, tested and manufactured using post-CMOS compatible processes. Since infrared detectors on a conventional silicon wafer have been successfully packaged using aluminum oxide [91] and silicon nitride [92] as an encapsulating layer, vacuum packaging of resonators is also viable using aluminum oxide. We have chosen a resonator as the device to be packaged because responsivity of a resonator is a function of pressure in the package. The goal is to utilize the RF MEMS resonator characteristics to check the quality of vacuum package.

After discussing the motivation behind this work, this chapter details the design and process flow of "canopy structure" vacuum packaging for an RF MEMS device, specifically, a

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resonator. First, the design and the fabrication process flow of the vacuum package and RF MEMS resonator will be briefly discussed, followed by the integration of the resonator with vacuum packaged cavity. The general fabrication steps are described in this chapter. A detailed fabrication process flow is given in the Appendix.

4.2 Motivation and approach

4.2.1 MEMS wafer level packaging technology review

Most MEMS devices are fabricated using techniques that leave the mechanical structures exposed after wafer fabrication is completed. Open-die MEMS devices are easily destroyed if their unprotected mechanical elements come in contact with a physical object. They are also very susceptible to degradation by dust, stiction, and corrosion by water vapor. For instance, RF micromechanical resonators require controlled ambient to operate at a specific resonance frequency. To ensure long-term reliability, an open-die MEMS device must be hermetically packaged. There are two general solutions to MEMS packaging. One approach is to use the existing IC infrastructure, chip-scale ceramic packaging, where release and sealing are performed serially on the individual die after dicing. Figure 4.1 shows a packaged Digital Micromirror Device (DMD) from Texas Instruments [93]. The DMD is adhesively attached to the Al_2O_3 ceramic header and then wire bonded. The optical window is assembled to the ceramic header seal ring. The ceramics have Coefficient of Thermal Expansion (CTE) in the range of 5-9 ppm/°C, which is close to silicon (2.6 ppm/°C). CTE mismatch is more critical when the die size is larger. Because ceramic shrinks during the firing process, the package should be compensated in the design. The challenge in chip-scale packaging is selecting the specific equipment required to seal a die.

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Handling MEMS chips prior to packaging is costly and inefficient from a manufacturing standpoint.
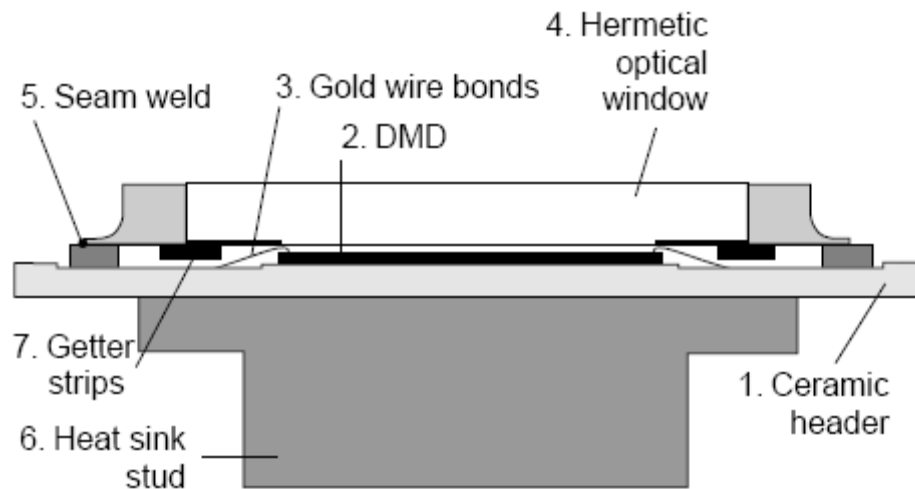

Figure 4.1 Chip scale packaged digital micromirror (DMD^{TM}) from Texas Instruments. Reprinted after J. Faris, T. Kocian, "DMD^{TM} packaging evolution and strategy," Proc. IMAPS 98, pp. 108-113, 1998 by permission of IMAPS.

The other approach is wafer level packaging, in which release and sealing are performed in parallel prior to dicing and assembly. Sealing the dies simultaneously results in a size reduction, time, and cost. Two main approaches have been developed by MEMS engineers for wafer level packaging. The first one is based on wafer bonding. In this technique the micromachined wafer is bonded to a second wafer. This second wafer is generally glass or silicon. Many bonding technologies can be used such as anodic bonding, silicon direct bonding, eutectic bonding, or polymer bonding [94,95,96,97]. These bondings can be hermetic or near hermetic and prevent contamination of MEMS structure during back-end process.

The second technology is the thin film packaging [98,99]. This can be done by surface micromachining to create a thin-film overcoat on top of a sacrificial material, followed by

sacrificial layer removal. In thin film packaging technique, closed cavities are formed above the devices by surface micromachining. A thin capping layer is deposited on top of the sacrificial layer and then perforated to remove sacrificial layer. Finally, a film is deposited on top of the capping layer to seal the holes. Thin film packaging offers lower system cost than wafer bonding packaging because it uses standard IC technology and consumes less die area. Moreover, it does not require wafer to wafer alignment and backside process technologies. There is another hermetic packaging concept developed by Goldsmith *et al.* [100], where a cavity holding the RF MEMS switch and inert gas based upon spin coating technique with a polymer to seal the cavity. There is some question as to whether the package is sufficiently strong to endure the overmolding process. The process used is not compatible with the formation of a vacuum cavity. In addition, it is not compatible with optically transparent sealing.

This work describes a low cost alternative method to conventional die-based, back-end packaging of RF-MEMS. One of the important aspects of this packaging technique is that the RF-MEMS device is self-packaged before leaving the clean room. The packaging can be done on device level, die level or wafer level with the choice of sealing gas and pressure. The encapsulation process is not only CMOS compatible but also cost effective. Furthermore, the process can reduce the temperature effect on the packaged MEMS device and enhance the packaging performance, since it's a low-temperature procedure. This work also reports using Al_2O_3 for the first time as an encapsulation material. In the following sections, the vacuum package design and fabrication process are presented, including the schematics of the vacuum packaged RF MEMS resonator. The fabrication process for the package and an integrated resonator to monitor the pressure inside the package are described. Finally, the RF characterization results and long term reliability data are discussed in Chapter 5.

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4.3 Vacuum cavity package

To check the mechanical integrity, the first set of vacuum-cavity packages were fabricated without the resonators and subjected to an over-molding process. For the overmolding test, the packages were sent to Freescale Semiconductor. Vacuum-cavity packages that can hold resonators ranging from 2 MHz to 100 MHz frequencies were designed. Next, MEMS resonators were built and tested in a vacuum probe station with no packaging. Finally, these two technologies were integrated using surface-micromachining to achieve vacuum packaged MEMS resonators.

4.3.1 Design and fabrication of vacuum package cavity

The mechanical strength of the designed packages was simulated using CoventorWare™ (Fig. 4.2). With pressure applied on top of the package, the deflection and the maximum induced Von Mises stress were computed. The structure was found to withstand up to 103 Atm. The reason for choosing alumina as a packaging material

The fabrication process flow for the vacuum cavity package starts with a deposition of 600 nm silicon dioxide insulation layer by wet oxidation. This is followed by spin coating of 4.0 µm polyimide, PI 2737 from HD Microsystems, sacrificial layer. The polyimide is then cured at 300° C to get a thickness of 2.5~3 µm. For curing a specific temperature vs. time profile was followed. Temperature was increased from 25^oC to 300^oC in 1 hour, curing at 300^oC for 3 hours and finally cooling it down from 300^oC to 25^oC in 1 hour.   Next, 0.8 µm thick aluminum oxide layer is deposited by RF sputtering at 10mT chamber pressure. Trench cuts are made in the
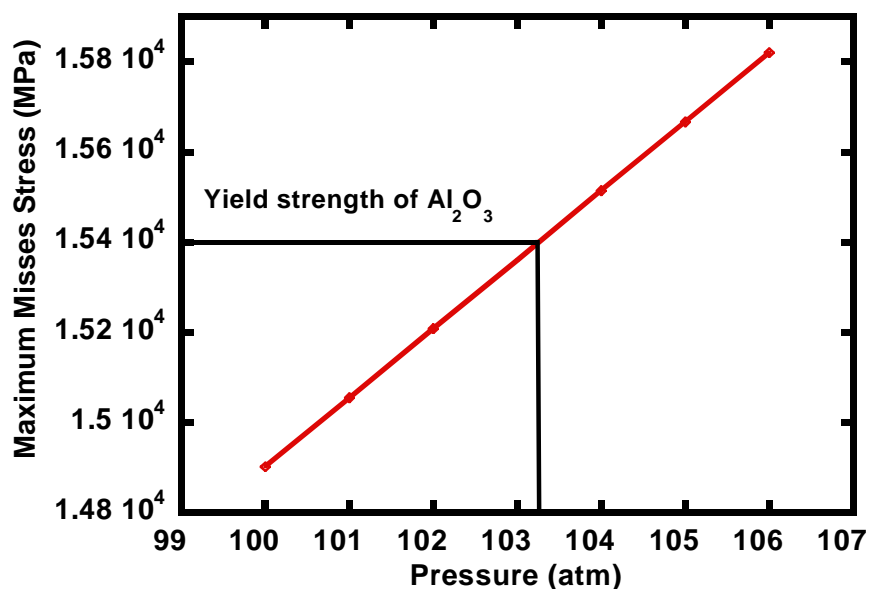
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Figure 4.2 The mechanical strength of the designed packages simulated using CoventorWare™. With pressure applied on top of the package, the deflection and the maximum induced Von Mises stress was computed. The structure was found to withstand up to 103 Atm

aluminum oxide layer to facilitate the removal of sacrificial polyimide layer. The sacrificial layer is removed using an oxygen-based plasma asher and the cavity is sealed by RF sputtering, at 150W power, 4~5 μm thick aluminum oxide sealing layer at 5 mTorr chamber pressure. Since the deposition is done in a low pressure environment (5 mTorr), the packages are vacuum-packaged. Fig.4.3 (a) shows the ConventorWare™ model and SEM image of a completely sealed vacuum cavity, while Fig. 4.3 (b) depicts the FIB cut along the vacuum package to reveal the vacuum cavity.

The reason for using alumina as a beam and sealing material is its attractive physical and optical properties. This is a hard and stiff material with a high Young's modulus. Alumina also has good thermal and chemical stability and firm adhesion to many surfaces. This material

can also be used in high temperatures and under harsh environments. Moreover, alumina possesses high dielectric constant and excellent insulating propserties. Alumina is also transparent over a wide range of wavelengths and can be used as a low refractive index material, which might be important for other applications.
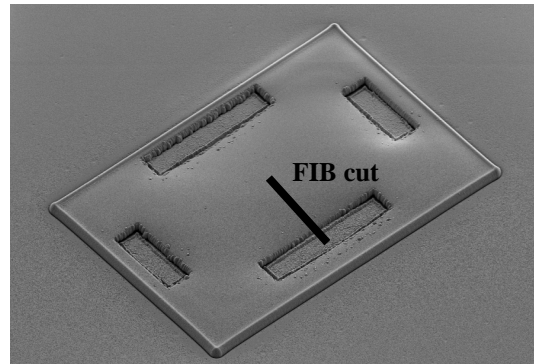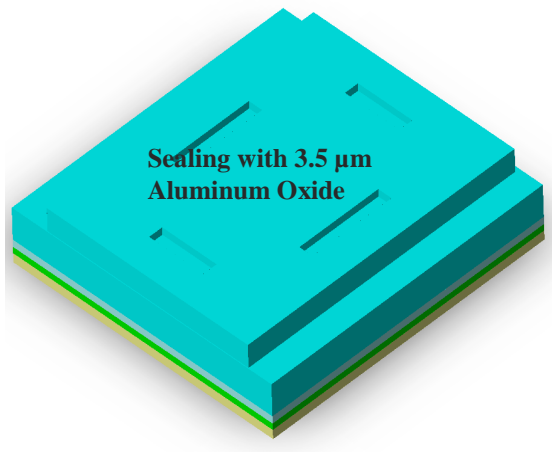
(a)
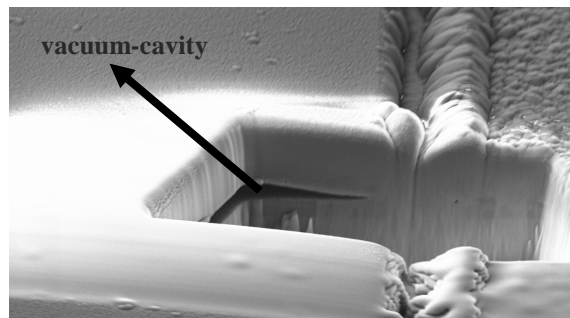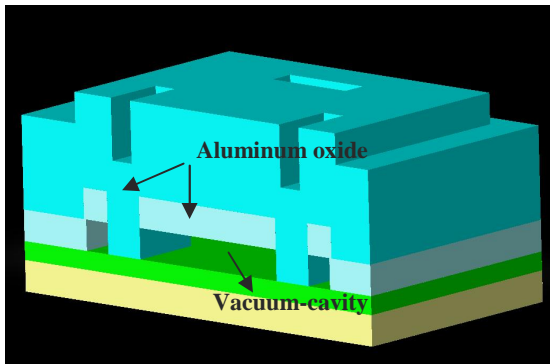
(b)

Figure 4.3 CoventorWare^{TM} model and SEM picture of (a) vacuum-cavity package without the resonator (b) focused ion beam (FIB) cut into the vacuum-package to show the presence of a vacuum-cavity.

<u>4.4 RF MEMS resonator</u>

MEMS resonators are becoming widely used for high frequency (HF, 3-30 MHz), very high frequency (VHF, 30-300 MHz) and even ultra high frequency (UHF, 300 MHz- 3 GHz) systems. They are very promising and could be an alternative to traditional electronic components on the design of multiple RF devices (i.e. mixers, tuneable capacitors, inductors, switches, oscillators etc.). Integration of these elements into a single chip will improve the performance of the RF systems, reducing costs, power consumption and size [101,102]. MEMS resonators also have the potential to integrate all of the analog functions without the problems associated with their counterparts.

4.4.1 Design and fabrication

The designed MEMS resonator is a fixed-fixed beam type wherein the fundamental mode resonance frequency is given by the following equation [103]

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{K_r}{m_r}} = 1.03\sqrt{\frac{E_y}{\rho}}\frac{h}{L_r^2} \qquad (4.1)$$

where K_r is the beam stiffness, m_r is the mass of the beam, E_y is the Young's modulus, ρ is the beam material density, h and L_r are the thickness and length of the beam, respectively. The beams were designed to resonate in the frequency range of 2 – 100 MHz.

The fabrication of vacuum packaged MEMS resonator is based on surface micromachining technique [104]. Fabrication process starts with the deposition of silicon dioxide on a clean silicon wafer serving as an insulating layer followed by 67-nm thick titanium and gold metal layers to form the electrode, anchor and conductors using standard lift-off technique. The 320

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nm thick PI2737 sacrificial layer is then spin coated and cured at 275 ^{o}C for 2 hours 30 minutes to define the critical air-gap height of 200 nm between the resonator beam and the drive electrode. The resonator beam consists of a metal layer and a low stress, aluminum oxide layer. These layers are subsequently deposited by RF sputtering and patterned using the lift-off technique. Thickness of resonator beam is around 1.6 µm. Finally, sacrificial layer is removed with an oxygen-based plasma asher [105,106,107]. CoventorWare^{TM} model of the different fabrication steps is shown in Fig. 4.4.
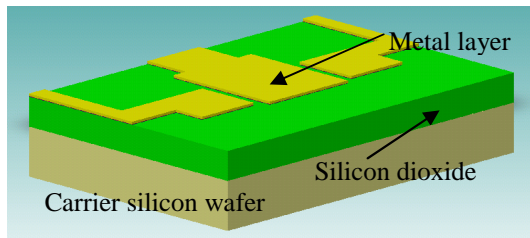
a : Silicon dioxide insulating layer.　　　　　**b :** First Sacrificial layer.
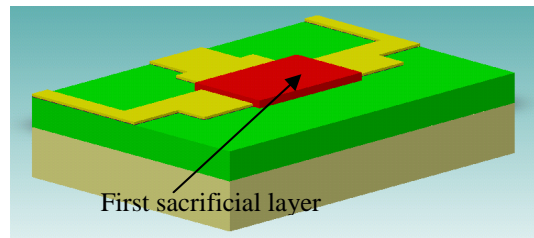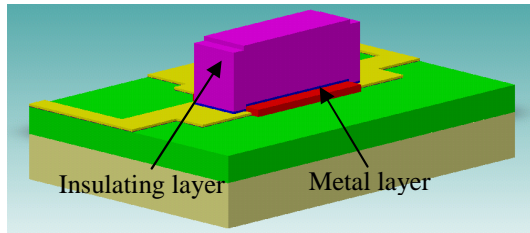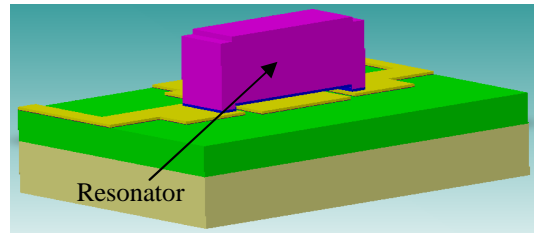
c : Resonator beam.　　　　　**d :** Ash the first sacrificial layer.

Figure 4.4. CoventorWare^{TM} model of RF MEMS resonator fabrication. (a) Insulating layer deposition. (b) Deposition of first sacrificial layer. (c) Deposition of resonator beam. (d) Ashing of first sacrificial layer.

Fig. 4.5 shows optical picture of a released 5 MHz resonator with 40µm beam width and 80 µm beam length after completely removed the first sacrificial layer. Magnified picture of a fully released resonator beam with beam thickness of 1.6 µm and air gap height of 190 nm is

also presented. This photograph also confirms the successful removal of the first sacrificial layer. After fabrication of the resonator Scanning Electron Microscopy (SEM) analysis was done to verify the complete release of resonator beam. Fig. 4.6 is the SEM image of a completely released 5 MHz resonator beam. From this image it is evident that the resonator beam is completely micromachined and also there is no stiction or residue due to ashing of the first sacrificial layer.
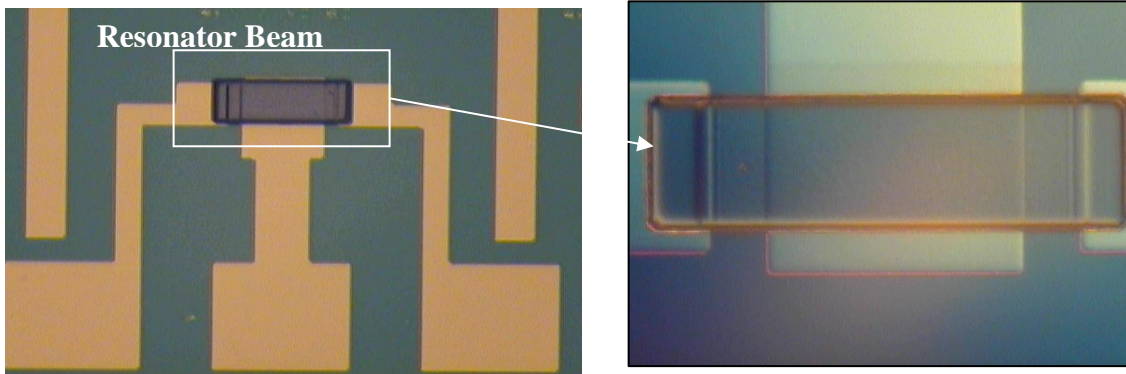

Figure 4.5. Optical picture of a 5 MHz resonator shows the magnified picture of the released resonator beam after ashing the first sacrificial layer.

4.5 Integration of the vacuum package cavity with MEMS resonators

The next step was to integrate the packaging process into the fabrication steps of the MEMS resonators. Vacuum packages are also successfully fabricated and ready to integrate with the resonators. This section describes the step by step integration of resonator to the vacuum package. Fig. 4.7 shows the ConventorWare^{TM} model for thin film encapsulation of a RF MEMS resonator. The sealing process starts with the deposition of approximately 3 μm thick PI 2737 polyimide layer which is spin coated on the released resonator then cured at 300°C for 4 hours. This second sacrificial layer determines the height between the beam and the

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packaging layer. Optical picture of second sacrificial layer after curing and before deposition of the packaging layer is shown in Fig. 4.8. After curing, the thickness of second sacrificial layer becomes 2 µm. This is followed by the deposition of a 0.8 µm thick aluminum oxide as the packaging layer using RF sputtering. Trench cuts are then made to enhance the removal of sacrificial layers by creating more openings to ash the sacrificial layer. Fig.4.9 depicts the packaging layer with trench cuts. We have tried two different ways to release the resonator beam: (1) before depositing the second sacrificial layer (prerelease), (2) after depositing second sacrificial layer and then ashing both layers together (post-release). We observed the former technique to work better than the latter. Fig 4.10 is the magnified picture of the released beam using the prerelease method. DC continuity is again checked after packaging layer deposition to make sure that the beam inside the packaging layer is fully released. Next, the trench cuts are sealed by depositing around 3~4 µm thick aluminum oxide sealing layer. As the deposition is done at 5 mTorr chamber pressure, the resonator is essentially vacuum packaged. This deposition pressure is very important since it determines the ambient inside the cavity.
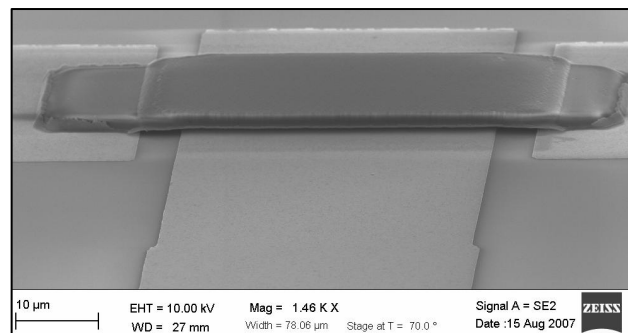

Figure 4.6. SEM image of a micromachined 3.6 MHz MEMS resonator. This image reveals that the resonator beam is completely released after ashing the first sacrificial layer.

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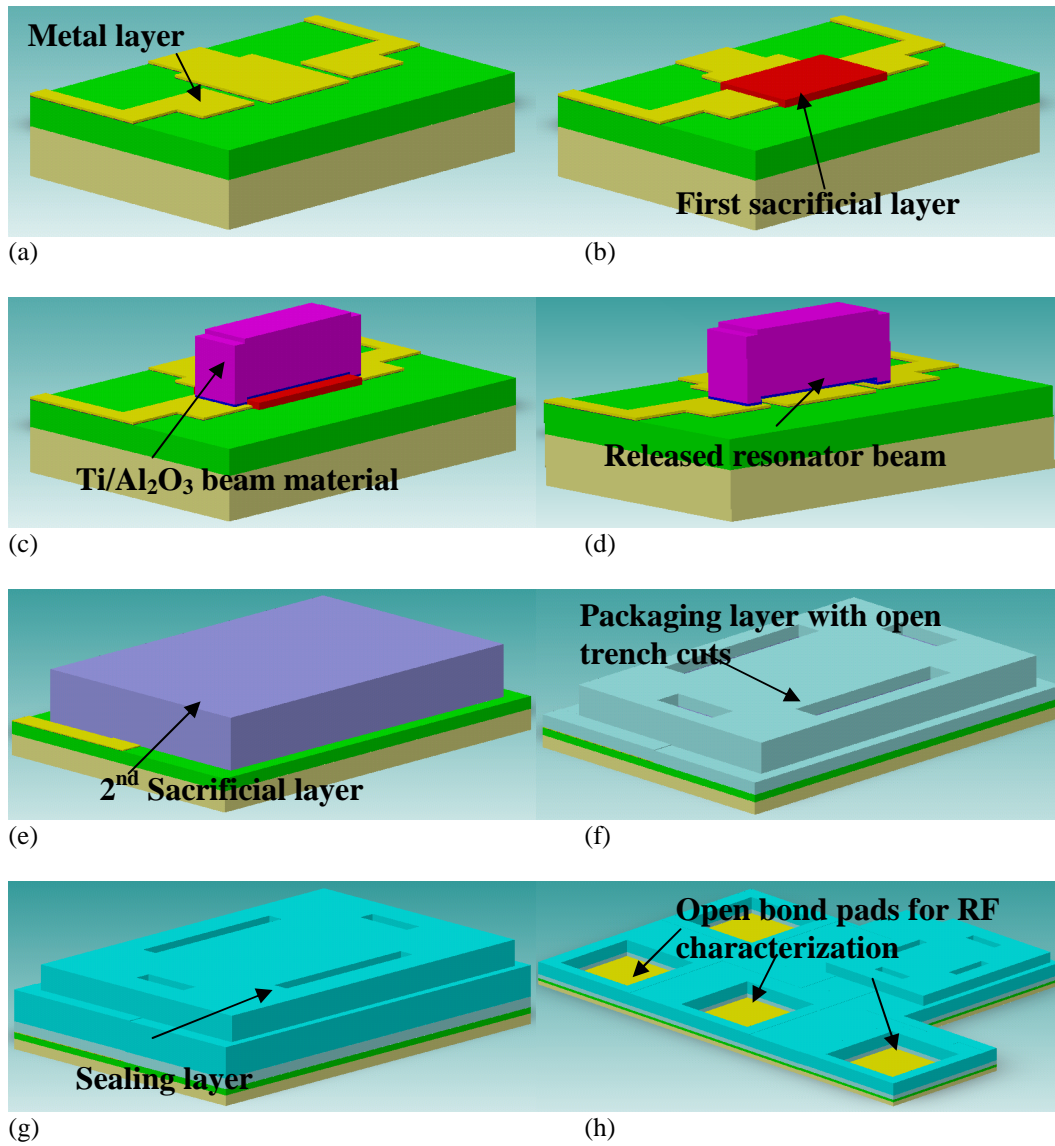
Figure 4.7. Fabrication steps: (a) SiO$_2$ insulating layer and metal layer. (b) Deposition of the first sacrificial layer. (c) Ti/Al$_2$O$_3$ resonator beam deposition. (d) Ashing the first sacrificial layer. (e) Second sacrificial layer. (f) Depositing the packaging layer, forming trenches and ashing second sacrificial layer. (g) Sealing the cavity. (h) Opening bond pads for RF characterization. In (c) and (d), vertical axis is exaggerated by 3 times.

Figure 4.8. Optical image of a pre-released resonator with the second sacrificial layer. Second sacrificial layer determines the height between the beam and the packaging layer.

Figure 4.9. Trench cuts are made before deposition of the sealing layer. The purpose of the trench cut is to ease the process of ashing.
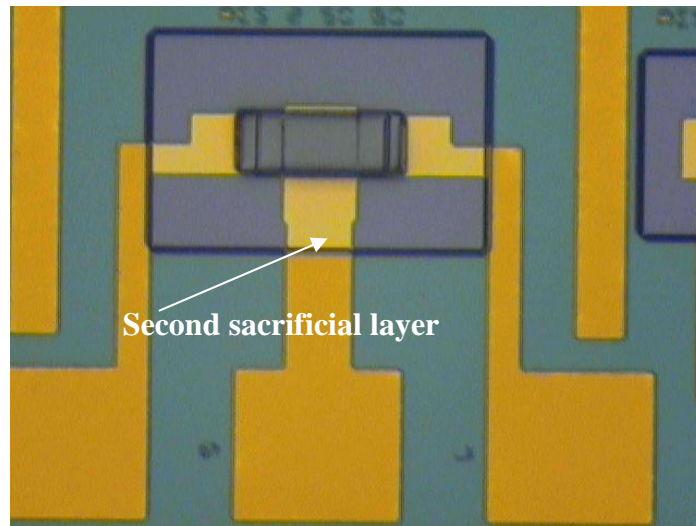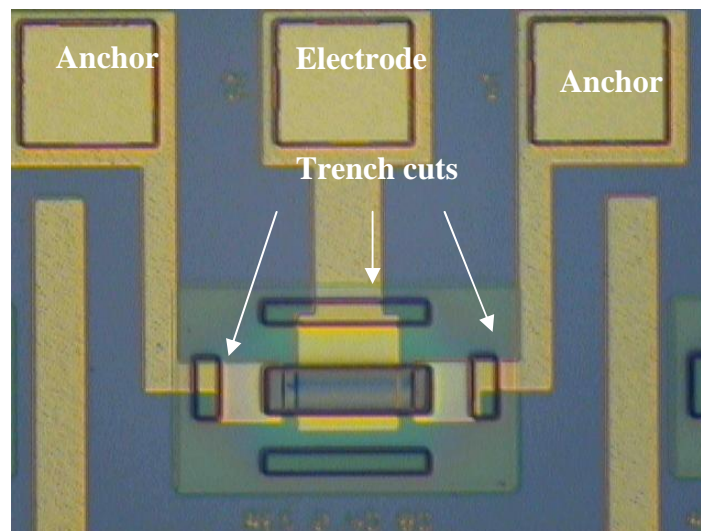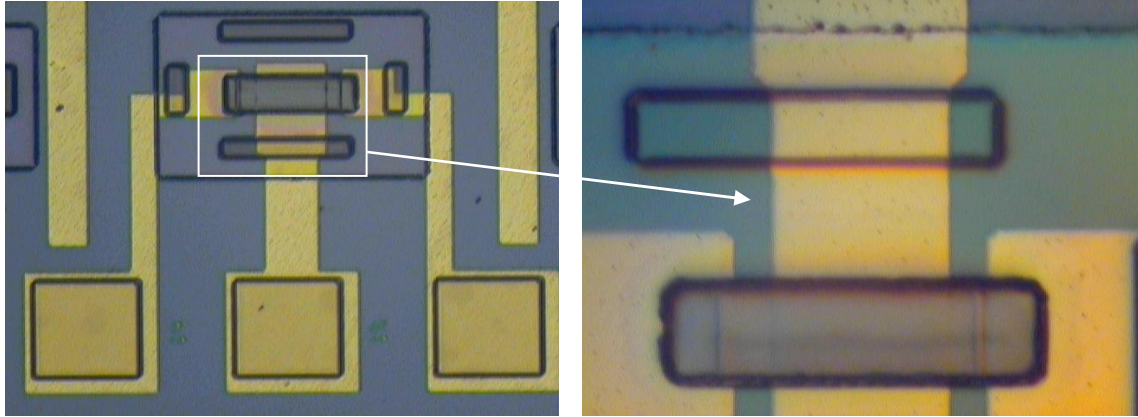
Figure 4.10. Magnified picture after ashing of first (determines the resonator beam height) and second sacrificial layer (determines the height between beam and packaging layer). No trace of sacrificial layer is present.

After successful sealing of packaged resonator, the main challenge is to open the anchor and drive electrode bond pads for device characterization. The main problem in aluminum oxide etching comes from the non planar topography across the wafer. For this reason a relatively thicker photoresist is used and the whole lithography/ etching process is repeated couple of times to make sure that the packages are intact during etching. Fig. 4.11 shows the packaged resonator after opening the bond pads. An SEM image of different packaged resonators is presented in Fig. 3. In order to make sure that the bond pads are opened properly, a profilometer reading is taken across the bond pads. Fig. 4.12 is the bond pad profile data which indicates that the bond pads are opened uniformly. The beam resistance and beam isolation measurements on the packaged resonators are consistent with the corresponding values for the unpackaged counterparts. For example, 20MHz and 25MHz resonators showed beam resistance of 647Ω and 697Ω before packaging and 629Ω and 679Ω after packaging, respectively. Packaged resonators showed tunable capacitive coupling with increasing bias voltage. Resonance was not observed in two samples tested to date. The SEM

images of six different packaged resonators are presented in Fig. 4.13 before and after opening

the bond pads. The packages are seen intact after opening the bond pads.
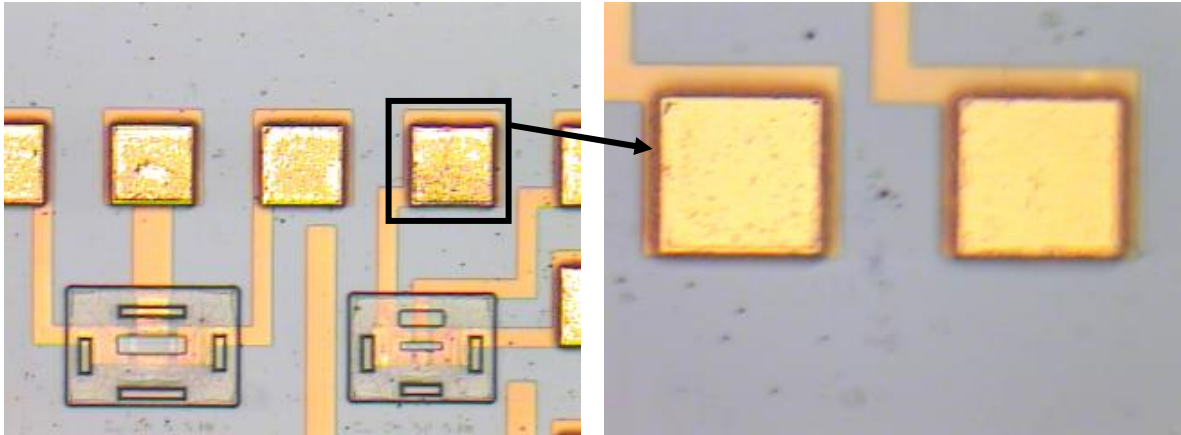
Figure 4.11. Optical image of the packaged resonators after sealing of the ashed holes and opening of the bond pads. Magnified picture of the bond pads shows that these are opened successfully.
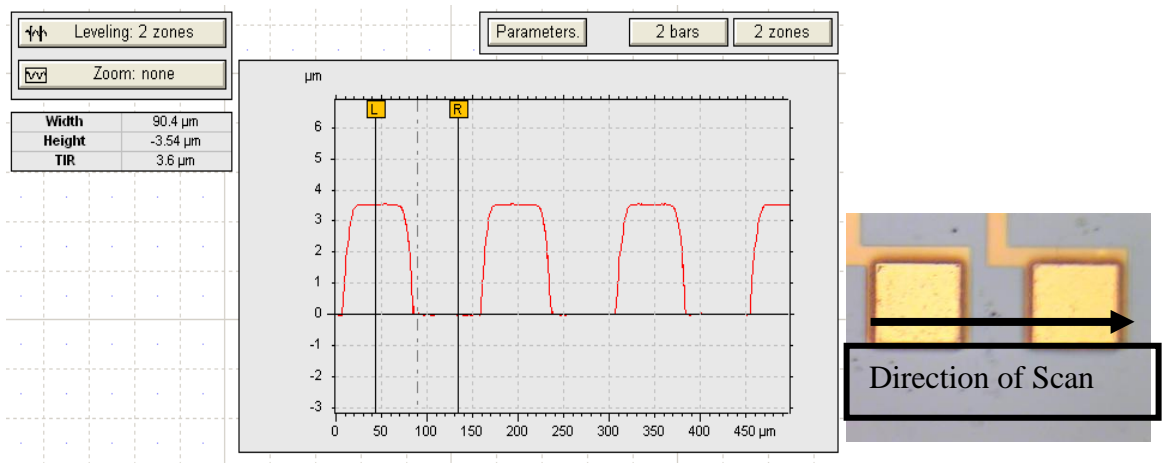
Figure 4.12. Profilometer data shows that the bond pads are opened uniformly.
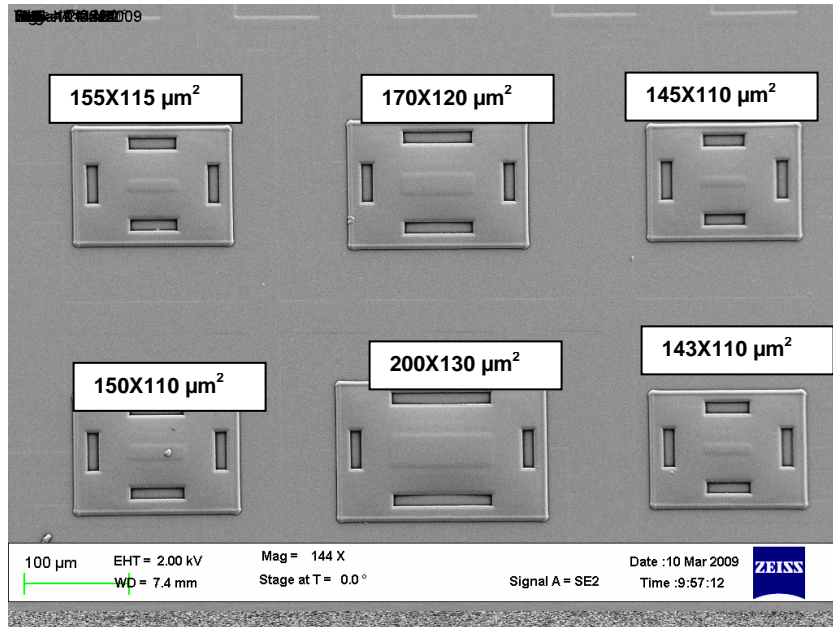
(a)
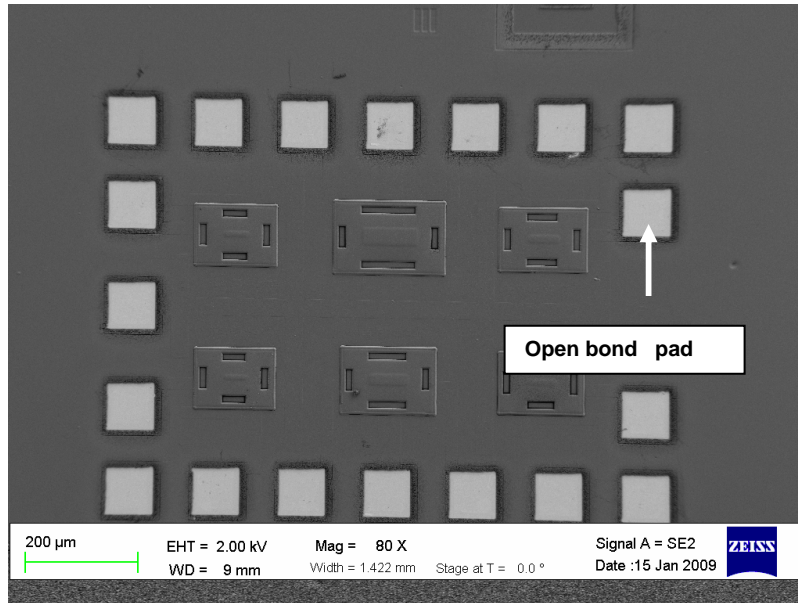
(b)

Figure 4.13. SEM image of completely sealed resonators (a) before and (b) after opening the bond pads. Packages are intact after opening the bond pads. The size of different packages is also given. Width of the trench cut is 15 µm and length is proportional with the package size.

4.6 Summary

Vacuum packaged cavity and MEMS resonators were fabricated separately before integrating together. No process related issues were encountered during integration. After successful integration, the bond pads of the packaged resonator were opened without damaging the package. The suitability of the Al_2O_3 as a packaging and sealing layer was verified using ConventorWare^{TM} based finite element method. Mechanical integrity of the package and extensive RF characteristics of the packaged resonators will be presented in the following chapter.

CHAPTER 5

RF MEMS PACKAGE ASSESSMENT AND DISCUSSION

5.1 Introduction

The packaging technique that we have presented in Chapter 4 is a low cost encapsulation method suitable for a variety of MEMS devices using Al_2O_3 [108]. This method is applicable to surface micromachined structure. A cavity of scalable height is created on top of movable/resonant part of MEMS resonator by processing a sacrificial layer, followed by deposition of thin alumina packaging layer. The packaging layer is patterned to get trench cuts to remove sacrificial layer. Compared with current packaging materials [109,110] used in MEMS packaging, alumina is a hard and stiff material with a high Young's modulus. Ceramic materials are naturally selected as packaging materials because of their superior high temperature chemical and electrical stability. Alumina can also be used in high temperature under harsh environment and it is a low cost material.

The packaging geometry can be changed to tailor different sizes of MEMS devices by scaling the sealed cavity. This technique makes the technology ideal for wide-band packaging of RF MEMS passives and switches as well as Pirani gauges. The low temperature packaging technique is CMOS compatible and does not add any stress to the movable components.

The main advantages of this technique are:

(1) The RF MEMS device is self packaged before leaving the clean room.

(2) This is a low temperature process suitable for MEMS and CMOS devices that is sensitive to high temperature and thermally induced stress.

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(3) The packaging technique is scalable from die to wafer level.

(4) Optically transparent packaging technique is possible.

(5) The enclosure is capable of withstanding the pressures of the surrounding atmosphere and the stresses associated with overmolding the die.

In this chapter, first, we describe the overmolding test results of vacuum package cavity performed at Freescale Semiconductor. Later, extensive RF characteristics and reliability tests were performed on the packaged resonators.

5.2 Overmolding of vacuum cavity package

The fabrication of vacuum-cavity packages without resonators has commenced as a pipe-cleaning lot to identify any processing issues prior to the integration of the MEMS device in the package. The detailed fabrication steps for vacuum-cavity package have already been described in Chapter 4. After the successful fabrication, the vacuum-cavity packages were sent to Freescale Semiconductor for the over-molding process. The over-molding process was done using the appropriate mold material (propreitary). Each vacuum encapsulation packaged six different resonators. Figure 5.1(a) shows six different vacuum-cavity packages after the overmolding process. A cross-section FIB cut was made in the center of the packages as shown by the line in Fig. 5.1(a). Fig. 5.1(b) represents the cross-sectioned image of the packages. From the SEM image, it is apparent that the packages are still intact and have survived the over-molding process. In addition, no major processing issues were encountered during the vacuum-cavity package fabrication process. One of the advantages of using alumina as the beam material and packaging layer is its transparency, so that we can monitor the progress of the ashing of first and second sacrificial layer by visual inspection under the microscope. Figure 5.2 shows the optical image of a packaged resonator with opened bond

pads. From this image, it is apparent that the package is transparent enough to see the resonator beam under the sealing layer.

(a)   **(b)**
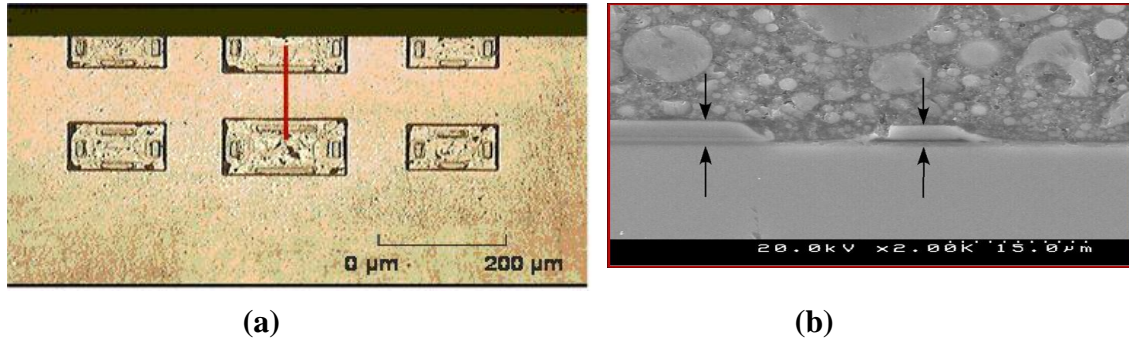
Figure 5.1 (a) Six different vacuum-cavity packages with the substrate removed after the over-molding process. The line depicts the cross-sectional cut made for the SEM. (b) Cross sectioned picture shows that the packages have survived after the over-molding process. The arrows point to the cross-sectioned package cavity. Between the two set of arrows lies the sealed trench-cut.
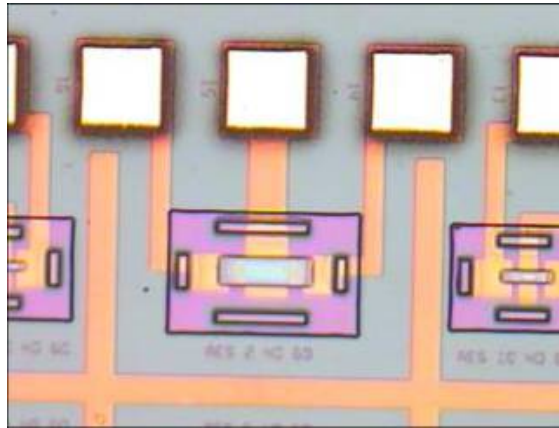

Figure 5.2 Optical image of completely sealed resonator after opening bond pads.

5.3 DC and RF characteristics of MEMS resonators

DC and RF characterizations were performed at different stages of the resonator fabrication and sealing process. DC measurements, which include assessment of beam isolation and resonator beam pull down, were done after micromachining the first and second sacrificial layers and subsequent to sealing of the resonator. The RF characterization was done before and after packaging. Two kinds of measurement setups were used for this purpose. The RF characterization of unpackaged resonators was performed inside a custom built, variable pressure (down to 25 mTorr) vacuum chamber, whereas the vacuum sealed resonators were characterized in a probe station at atmospheric pressure.

5.3.1 DC and RF characterization measurement setup

DC characteristics that includes beam resistance and beam isolation measurement along with pull down voltage is also performed in order to make sure that the resonator beam is fully released. Table 5.1 shows the typical value of beam resistance, isolation and pull down voltage value for different resonators. A custom made vacuum chamber is built to evaluate RF characteristics of the resonator prior to integrating with vacuum package. This chamber enables us to perform RF characterization at different pressure intervals; later on, these results will be compared with the integrated resonator characteristics. The vacuum inside the chamber can be varied from 20 mTorr to 1 atm pressure. This is important because the quality factor and the resonance frequency are pressure dependent. Any change in cavity pressure of packaged resonator will result in corresponding change in the resonance frequency and the quality factor. Figure 5.3 (a) shows the overall RF characterization set up for unpackaged resonators, which include custom made vacuum chamber along with E5071C ENA series network analyzer,

Agilent E3620A power supply and vacuum pump. Figure 5.3 (b) depicts the DUT is attached to a 50 Ω Cu transmission line circuit board and wire-bonded to SMA connectors for RF characterization. Wafer level measurement for packaged resonators was performed inside a probe station at atmospheric pressure. This setup also consists of E5071C ENA series network analyzer and Agilent E3620A power supply. Figure 5.4 shows the wafer level measurement setup for packaged resonators.

Table 5.1 DC continuity check of released resonator

| Resonance Frequency (MHz)	Resonator Beam Width (µm)	Resonator Beam Length (µm)	Measured Beam Resistance (Ω)	Pull down voltage (Volt)
2	40	80	180	11
5	40	80	200	21
10	40	80	230	24
15	40	80	520	25

5.3.2 RF characteristics of packaged and unpackaged resonator

Both input and output RF signals were provided and measured using an Agilent E5071C Network Analyzer. The RF transmission spectrum S21 was used to determine the resonance frequency and the quality factor Q of the device. Figure 5.5 compares the RF response of a 3.6 MHz resonator before and after packaging. The measurements were performed at room temperature with V_{DC}=6.05 V and RF Power= -5 dBm. As expected, no resonance was observed at atmospheric pressure for an unpackaged resonator. However, the S21 characteristics were very similar for an unpackaged resonator probed inside the evacuated chamber and when the same resonator is tested in atmosphere after being vacuum packaged. It is evident from this figure that the resonance is due to the mechanical movement of the beam. In general, the performance of MEMS resonators is assessed by means of two parameters, the

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Q factor and the resonant frequency, f_r. Both are good indicators of the package quality since the pressure inside the package determines the damping parameter which in turn affects Q and f_r. The resonant frequency and Q factor did not change after packaging the device, which ascertains the success of the vacuum-packaging process [108].
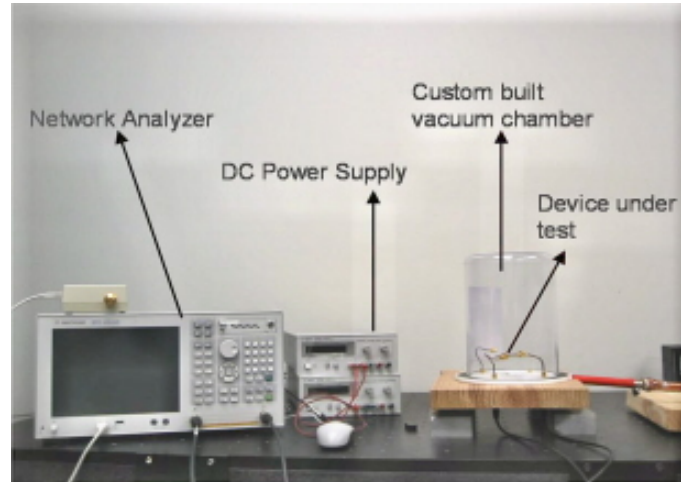
(a)
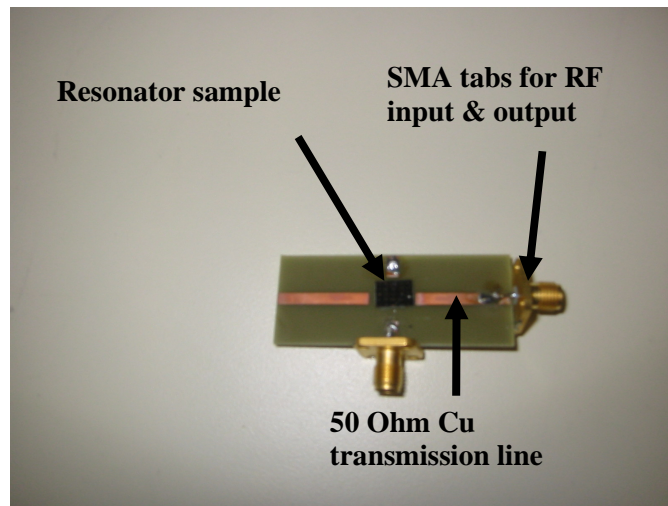
(b)

Figure 5.3 (a) Experimental setup for unpackaged RF MEMS resonators. (b) DUT is glued to circuit board.
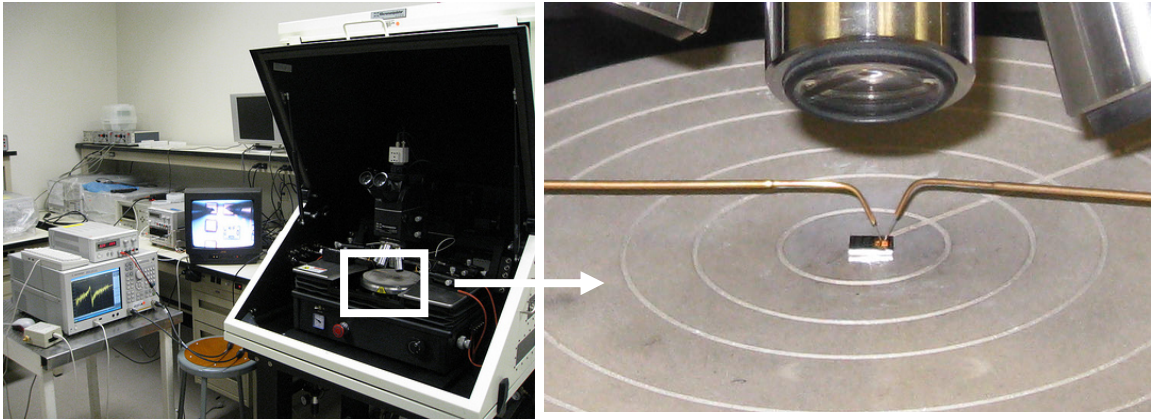
Figure 5.4 Wafer level RF measurement setup at atmospheric pressure inside probe station. Setup includes a E 5071C network analyzer and an Agilent E 3620A power supply.
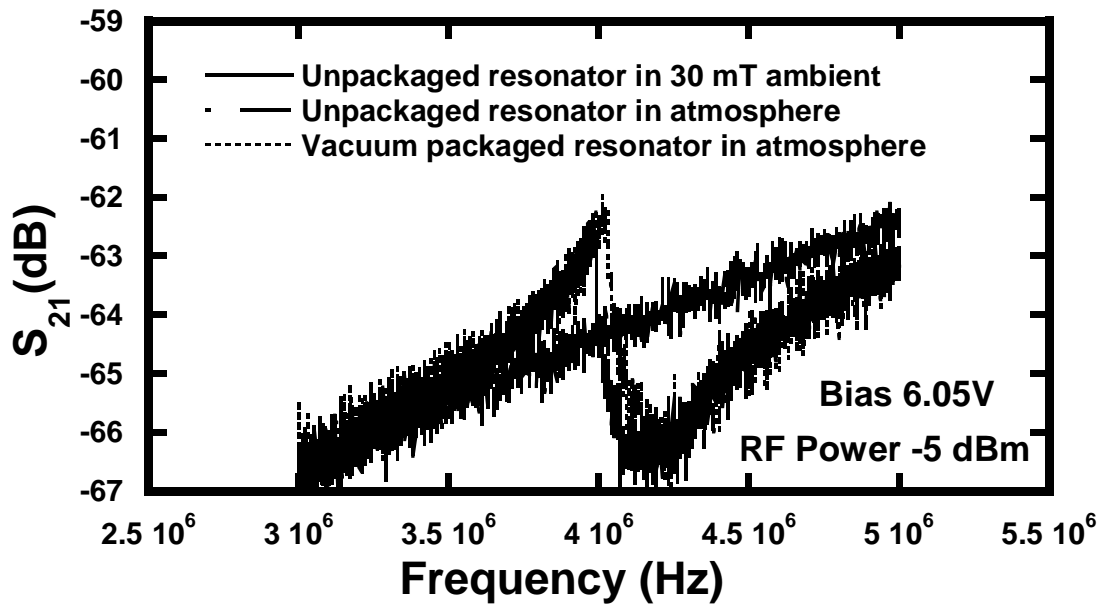

Figure 5.5 Measured RF response of an unpackaged 3.6 MHz resonator showing resonance at 3.65 MHz in vacuum (25 mTorr) and no resonance at atmospheric pressure. Moreover, the vacuum packaged resonator shows resonance at 3.66 MHz inside the probe station at atmospheric pressure.

5.3.3 Integrity of the resonator inside the package

The top dome of a 4 MHz packaged resonator was lifted off to determine the integrity of the device inside. SEM inspection revealed that the resonator inside the package is intact. In addition, as shown in Fig. 5.6 (a) and 5.6 (b) there is no significant spreading of the sputtered alumina, used for sealing the packages through the trench cuts, towards the resonator.

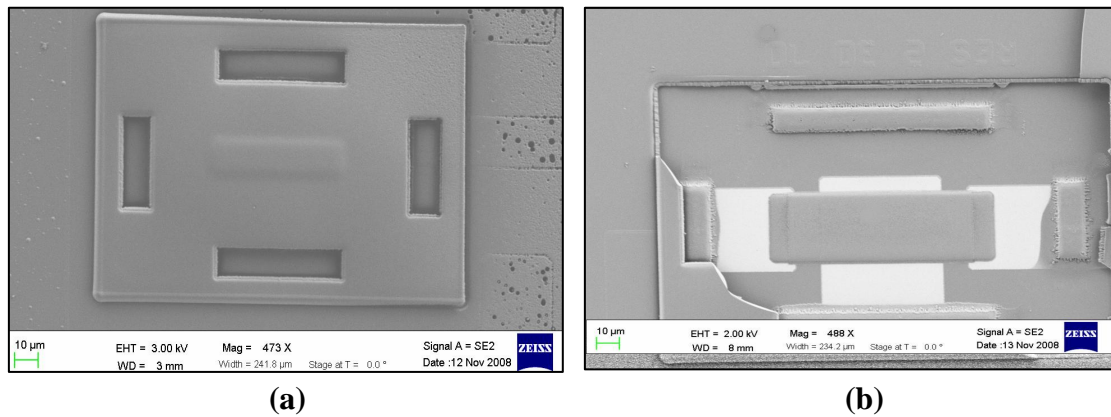**(a)**   **(b)**

Figure 5.6 (a) SEM image of a completely sealed. (b) SEM image of a vacuum-packaged 3.6 MHz resonator where the top layer is intentionally removed to inspect the resonator inside.

5.4 Long term and accelerated life testing

Packaging and reliability remain as some of the major hurdles in getting MEMS devices into commercial markets. Generally reliability depends heavily on the packaging technique. Packaging can be more challenging for released MEMS structures. However, a known and stable package environment is essential for reliable and repeatable performance over a long period of time. This way, MEMS devices are protected from potential contaminants, such as dust particles, moisture, and change in ambient. The importance of a stable pressure

environment is not a new idea, as it has been studied in quartz resonators for many years [111]. In order to assess their reliability, the packaged resonators were also subjected to various other tests, including extended operating life, RF characterization in different pressure ambients, high temperature operating life (HTOL), high temperature storage life (HTSL), temperature cycling and drop tests.

5.4.1 Effect of external pressure on packaged resonator

After successful integration of the resonator with the vacuum cavity and opening the bond pads, the packaged resonators were subjected to RF characterization. In order to characterize the packaged resonators, first the RF response was measured in a 35 mTorr vacuum ambient inside a custom-built vacuum chamber and pressure inside the chamber was varied. No change in the resonance frequency was observed. Fig. 5.7 shows that there is no change in the resonance frequency with respect to chamber pressure variation. Here, the devices are slightly over driven to see the sharp transition in order to precisely determine the difference in different ambient. No change in resonance frequency indicates that the resonator is completely sealed [112], and that the package can withstand such pressure variation.

5.4.2 Extended hour RF characterization

Figure 5.8 illustrates the extended 120 hour RF characterization of a packaged resonator in probe station at atmospheric pressure, held under bias continuously during the duration of the experiment. No change in resonance frequency and Q factor was observed. This indicates the integrity of the package.
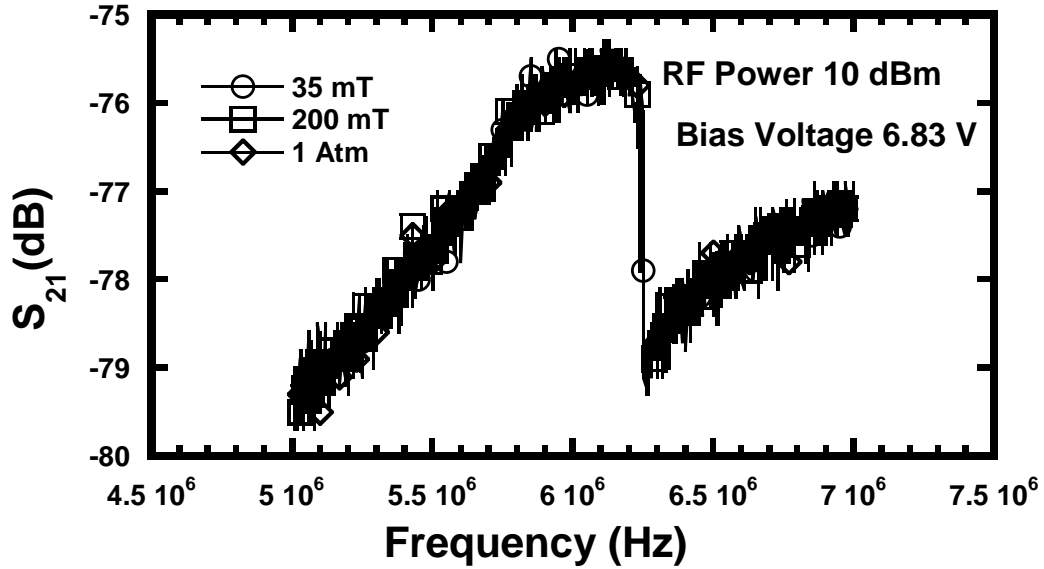
Figure 5.7 Completely sealed RF MEMS resonators showing no change in resonance frequency with chamber pressure variation. Devices are slightly overdriven to get the sharp transition.

5.4.3 High Temperature Operating Life (HTOL) experiment

For HTOL experiment, the packaged resonators were put on a probe station at atmospheric pressure and the measurement was carried by increasing the temperature of the hot chuck. During the entire duration of the experiment, the device was under constant bias and RF response of the device was measured continuously with a network analyzer. Fig. 5.9 shows the HTOL experimental data of a 7 MHz resonator at 70°C. No change in resonance frequency is observed after 144 hours of continuous operation. We also tried HTOL experiment at a higher temperature of 105°C. The minor change (less than 2%) in the resonance frequency, Fig. 5.10, might be attributed to the change in the alumina beam stiffness. However, continuous operation at 105 °C does not cause any change in the RF characteristics. When temperature is returned

to room temperature the RF characteristics returns to room temperature characteristics also. This indicates that the package can operate at this high temperature without any degradation. The difference in the resonance frequency between room and elevated temperature can be explained with the help of equation (4.1). The decrease in resonance frequency with temperature change might be associated with the change in the resonator beam length. The beam length of the resonator used in this experiment was 24.22 μm. Using the linear temperature expansion coefficient for alumina, $\alpha = 3x10^{-6} in/in^0 F$, we can calculate the change in beam length due to the increase in temperature from 27$^{\text{o}}$C to 105$^{\text{o}}$C by the following equation:

$$\Delta L = \alpha L \Delta F \qquad (5.1)$$

where ΔL is the change in beam length due to increase in temperature, L is the original beam length and ΔF is the change in temperature in Fahrenheit. Using the above equation, the change in the beam length between room temperature and 105 $^{\text{o}}$C can be calculated as 0.011 μm. Now using equation (4.1) for two different temperatures and considering the room temperature resonance frequency as 6.98 MHz (from Fig. 5.10), the resonance frequency for the elevated temperature can be calculated as 6.91 MHz. This is very close to the experimental finding of 6.9 MHz at 105 $^{\text{o}}$C. Here we neglected the thermal mismatch based frequency drift because the difference in linear thermal expansion coefficient between alumina and titanium is small. (Thermal expansion co-efficient for titanium is $\alpha = 4.8x10^{-6} in/in^0 F$)
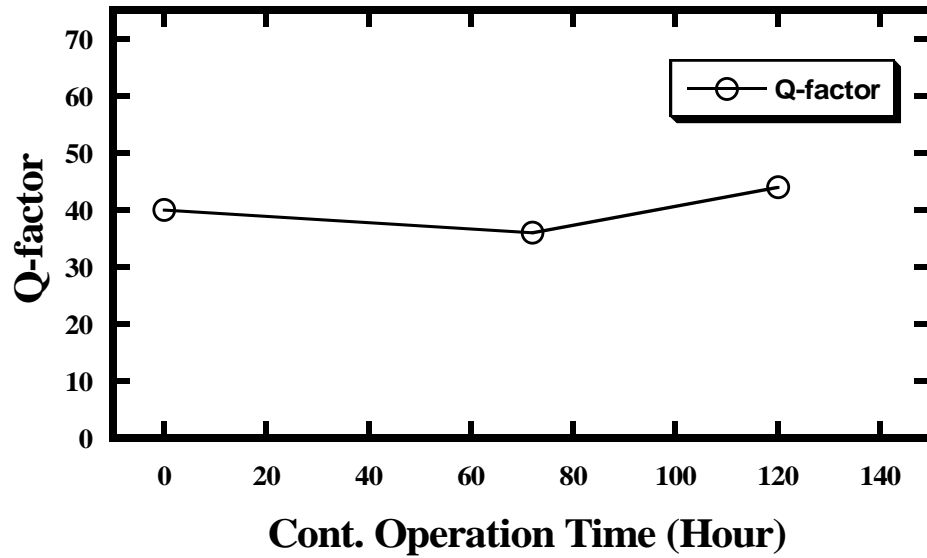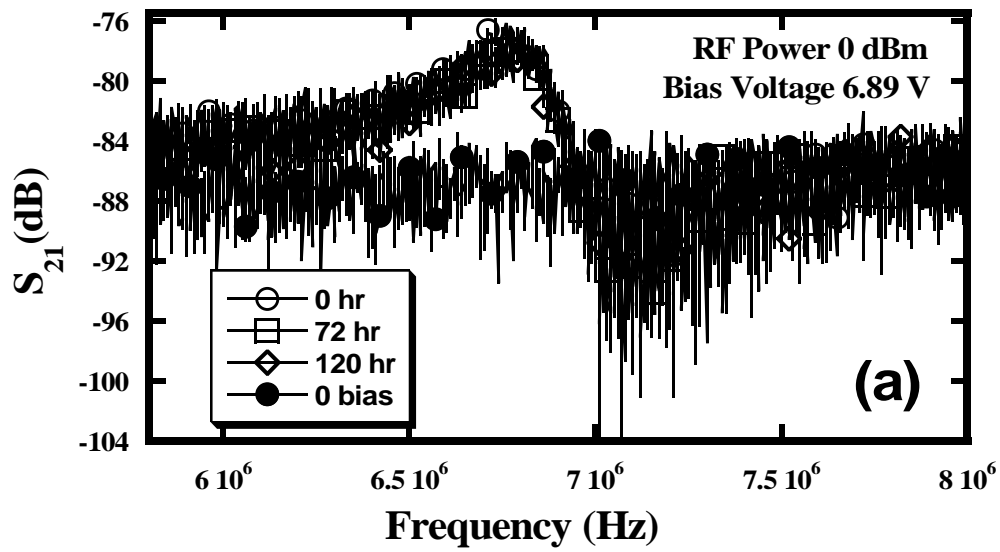
96

Figure 5.8 Extended 120-hour RF characterization with the device held under constant bias during the duration of the experiment. Both (a) resonance frequency and (b) Q factor show no change in their characteristics.
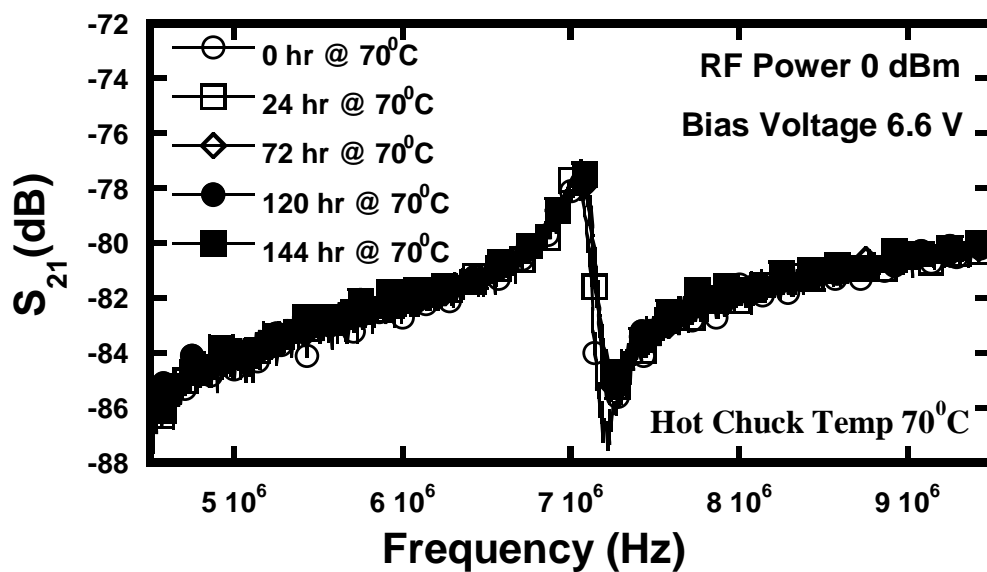
Figure 5.9 High temperature operating life measurements on a completely packaged resonator for 150 hours at 700C. The resonators survived at elevated temperatures.
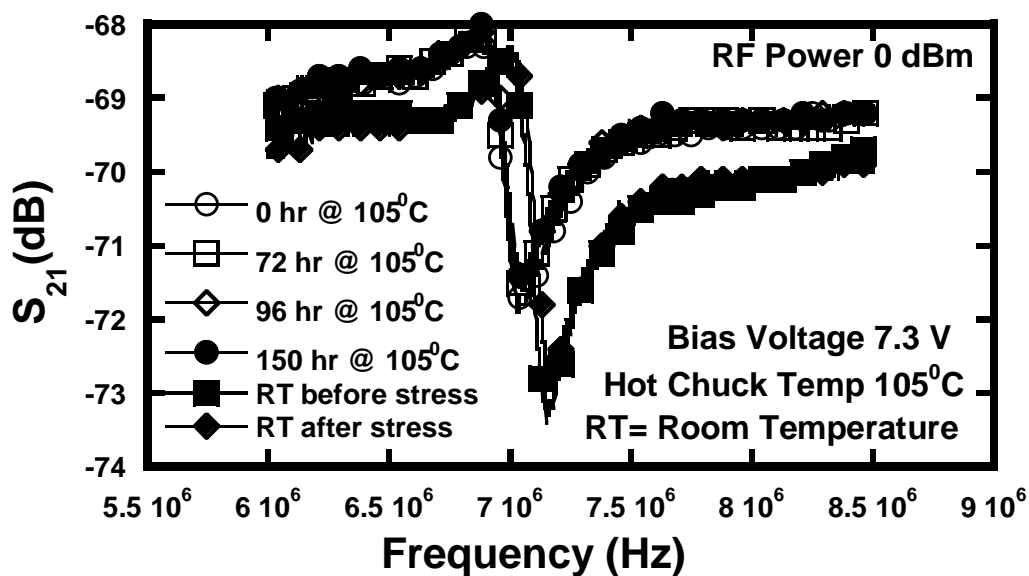

Figure 5.10 RF characteristics of a completely sealed 7 MHz resonator during high temperature operating life (HTOL) experiment performed at 105^oC.

5.4.4 High Temperature Storage Life (HTSL) experiment

To make sure that the vacuum condition inside the cavity is intact, the devices were also subjected to HTSL experiment. In this experiment, the devices were kept inside an oven at 110 ^{0}C, and measurements were taken every 250 hours for a total of 1000 hours. Fig. 5.11 shows the RF characterization data for the HTSL experiment. No change in resonance frequency and Q factor indicates that the vacuum inside the cavity is intact and the test package is robust.
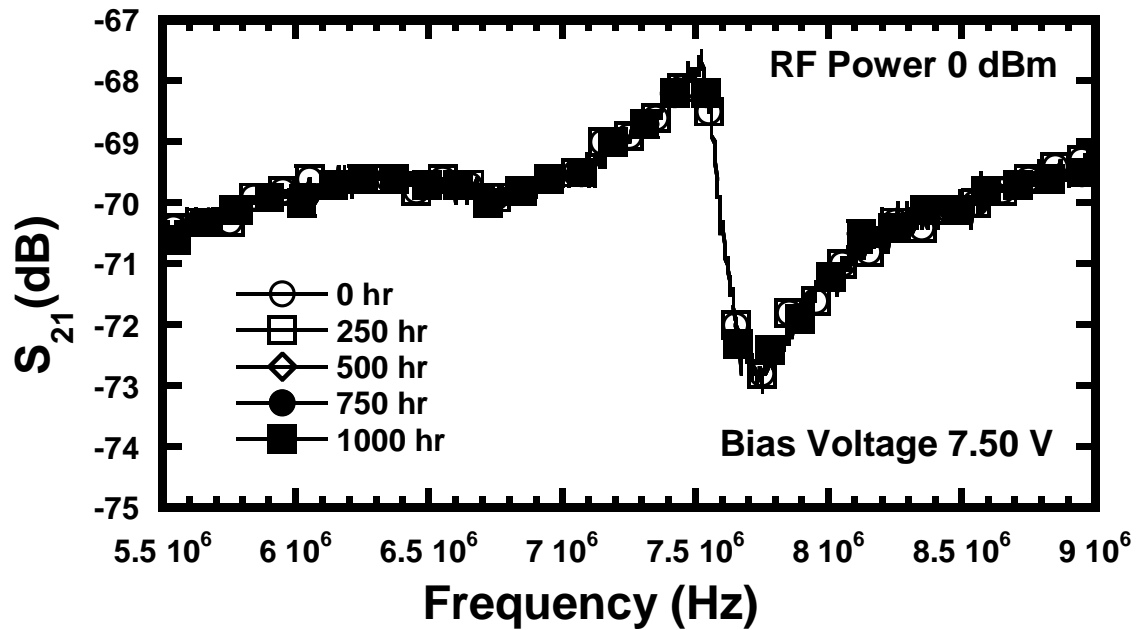

Figure 5.11 RF characteristics of a completely sealed 7.5 MHz resonator during high temperature storage life (HTSL) experiment.

Thermal cycling measurement is a good way to further test the robustness of the package. For thermal cycling, the packaged resonators are kept inside an oven and the temperature in the oven was varied from 27^0C to 120^0C. Each cycle consisted of 12 hours and measurements were taken after every 25 cycles. This cycle was repeated > 100 times. No change in resonance frequency or Q factor could be seen in Fig. 10. This is an evidence that the package is robust and can withstand these temperature changes without compromising the package integrity. It also demonstrates that there is no significant outgassing from the package at these temperatures.
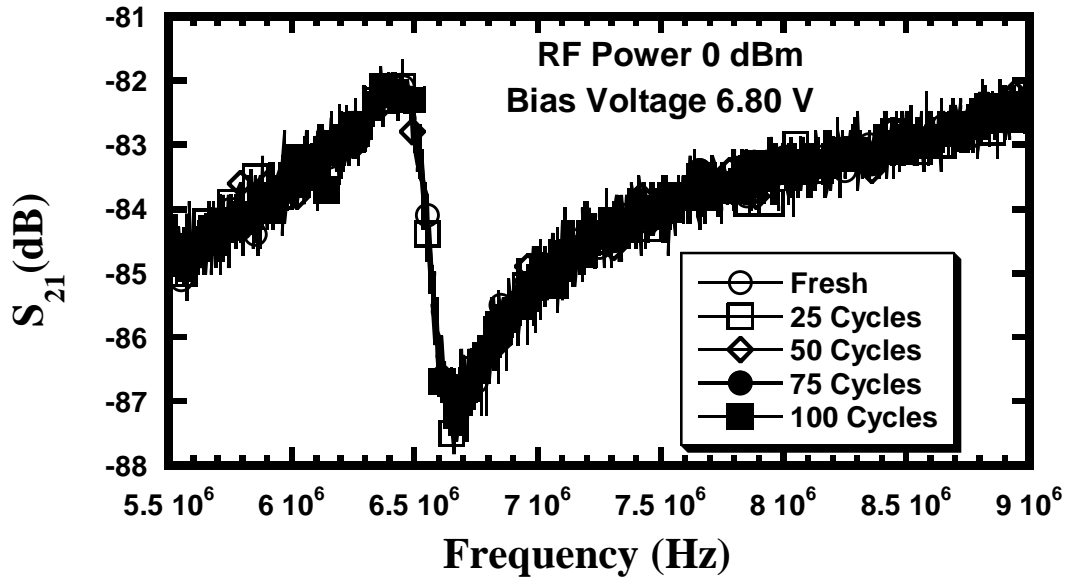

Figure 5.12 Temperature cycling (27^0C to 120^0C) effect on RF characteristics of a 6.5 MHz packaged resonator. Each cycle consists of 12 hours. Measurements were taken every 25 cycles for a total of 100 cycles.

5.4.6 Accelerated humidity and drop test

The integrity of the vacuum inside the package was checked over the course of time by dipping the packaged RF resonators in room temperature water for 241 minutes and taking several measurements in between. The measured resonant frequency was found to be stable with time as shown in Fig. 5.13. This attributes to the sturdiness of the packaged resonators against humidity.

In addition, the capability of the packaged resonator to withstand against physical damage was also checked. In order to determine the ability of the sealing layer to retain and protect the resonator after a free fall, the packaged resonators were subjected to drop tests.
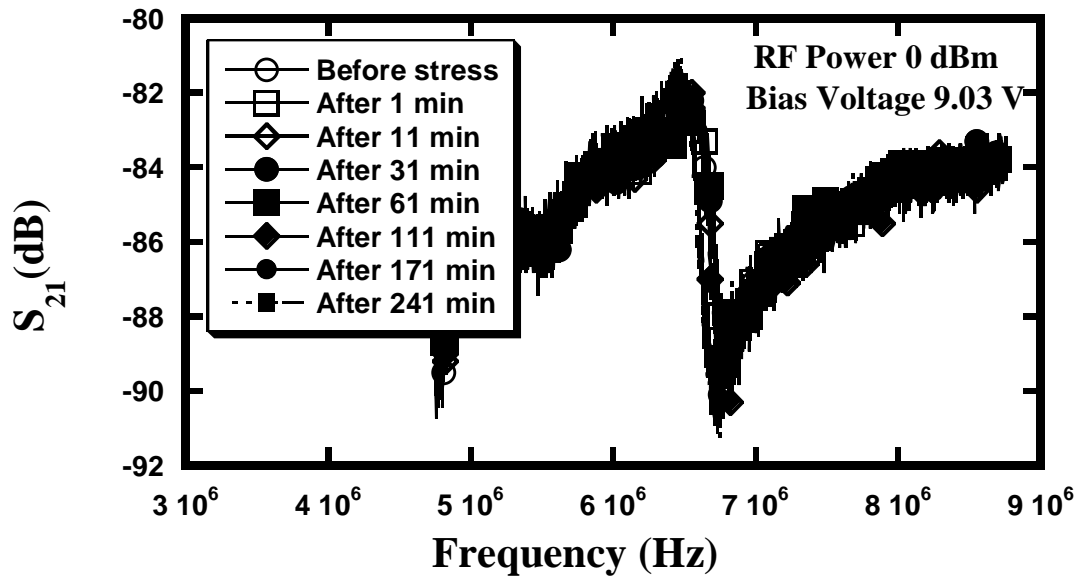

Figure 5.13. Effect of humidity on RF characteristics of a 6.5 MHz packaged resonator is checked by dipping the sample in water at room temperature. No change in resonance frequency is observed.

This test simulates the accidental drops, slips and falls of the package that might be encountered during manual or mechanical handling. For this reason, the die with the packaged resonator was dropped from 36 inches high upside down. After the drop, the sample was cleaned, bonded and characterized. The optical and SEM image of the dropped package resonator in Fig.5.14 shows considerable visual damage (not shown here) on top of the wafer, but package remained intact. The RF characteristics and dc tunability data of dropped packaged resonator in Fig. 5.15 indicates that the package can withstand such free fall. DC voltage tunability of MEMS resonator frequency in Fig. 5.15 (a) is important in order to compensate for manufacturing variations and ambient / operating temperature changes.

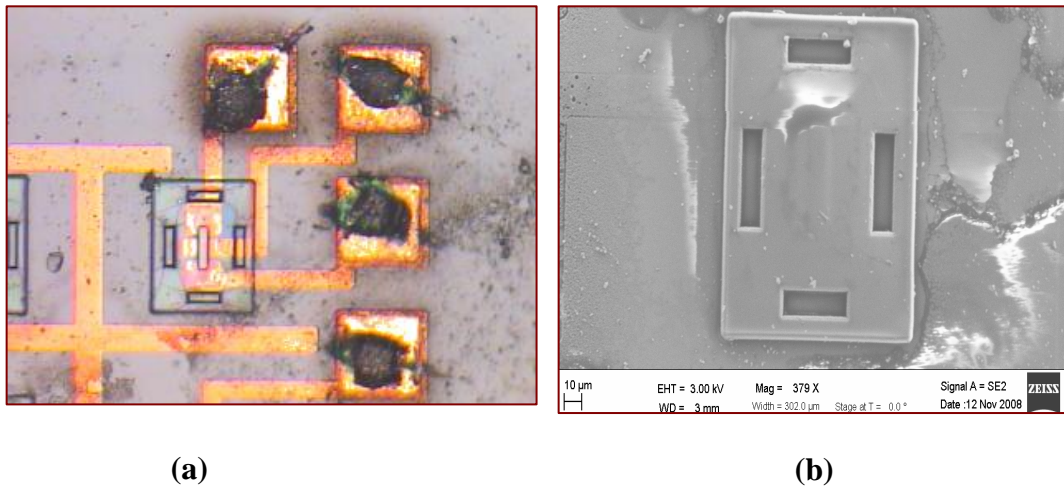**(a)**   **(b)**

Figure 5.14 The (a) optical and (b) SEM image of the dropped package resonator shows considerable visual damage on top of the wafer, but package remains intact.
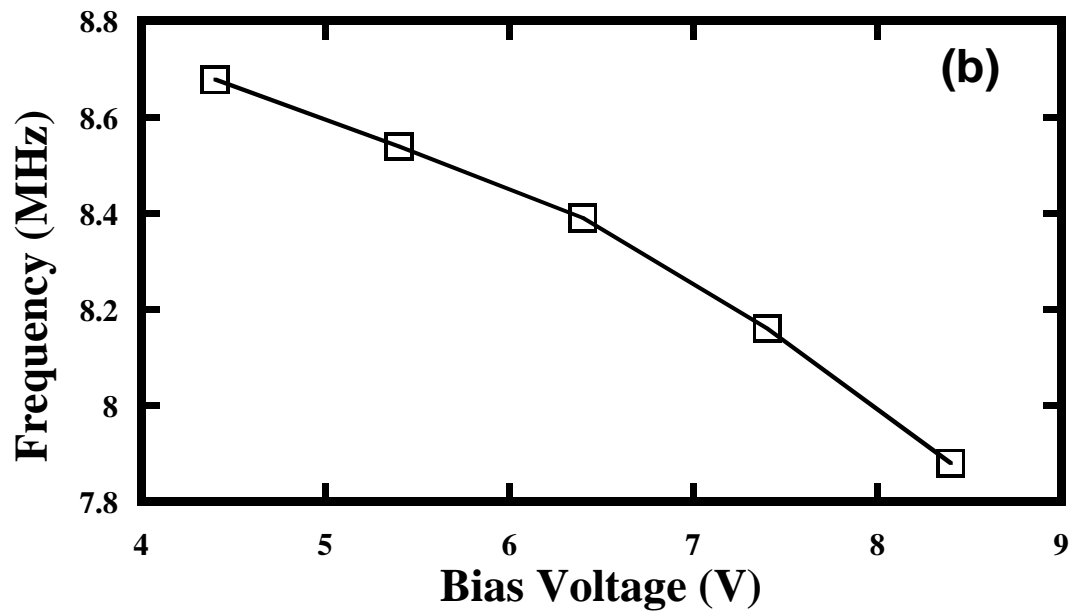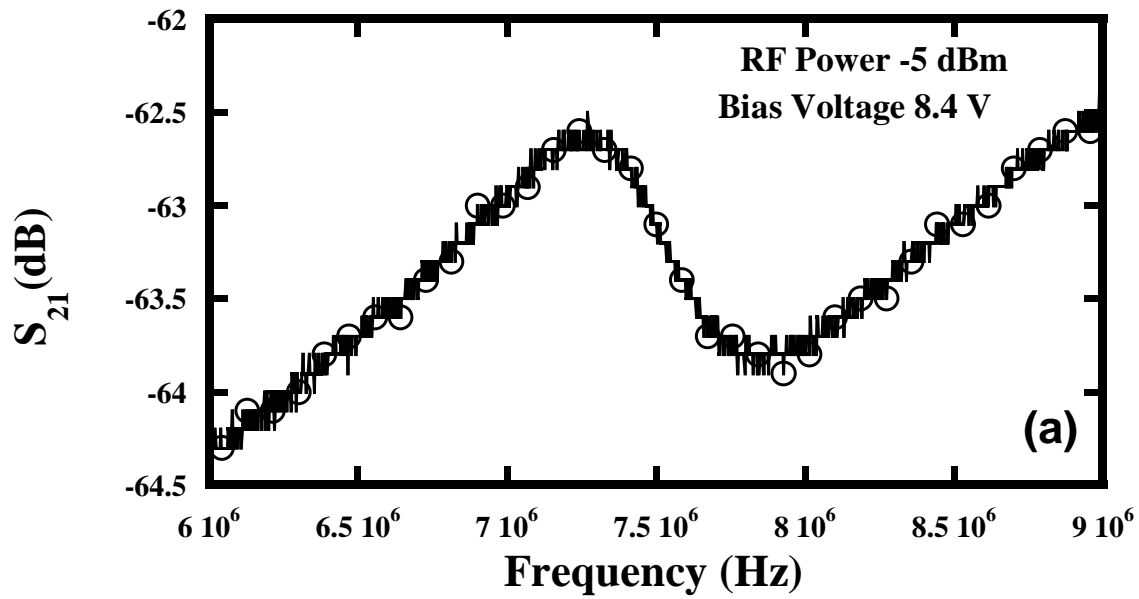
Figure 5.15 (a) RF characteristics and (b) DC tenability of a packaged resonator after drop test. Here the sample fell up side down from three feet height.

5.5 Summary

A device-level vacuum packaging technique has been demonstrated for MEMS devices. Double-layer surface micromachining was utilized in conjunction with an Al_2O_3 capping and sealing layer. To assess the integrity of the package, RF MEMS beam resonators were chosen, since the characteristics of these devices are sensitive to the package vacuum quality. The top layer of the packaged resonator was also removed intentionally to monitor the beam inside the package; no spreading of the sputtered alumina is noticeable through the trench cuts. The packaged resonators were subjected to HTOL, HTSL, and temperature cycling and drop tests and were shown to successfully survive all reliability tests. This packaging technique is offered as a low cost alternative to conventional die-based, back-end packaging of MEMS devices. The very low loss of silicon area due to packaging allows aggressive reduction in die size. By effectively sealing the MEMS devices at the device level across the wafer, it is possible to subject the device to conventional high volume packaging approaches.

CHAPTER 6

SUMMARY AND CONCLUSION

The broad focus of this dissertation is to study the reliability of advanced dielectrics in MOSFET gate oxide and device level packaging in microelectromechanical systems (MEMS). For application of high dielectric constant (high-k) materials in MEMS packaging, we studied the role of alumina (Al_2O_3) in hermetic packaging for radio frequency (RF) MEMS resonators. The quality (Q) -factor and resonance frequency, f_r of a RF MEMS resonator is pressure depended. Any change in cavity pressure will result in corresponding change in Q-factor and f_r. Therefore, we selected RF MEMS resonator as a test device to encapsulate. The focus here is to develop and characterize a new low cost, CMOS compatible hermetic packaging technology for MEMS devices. This technique utilizes surface micromachining to make the cavity. Later alumina film was deposited to provide hermiticity.

The main contribution from this part of the work is to establish a platform for robust packaging of MEMS devices by depositing ceramic material on top of the device using surface micromachining technique. One of the advantages of this encapsulation approach compared to other MEMS packaging techniques is that it is a low temperature process that can be used for packaging a wide variety of MEMS, including Pirani gauges and resonators. Sacrificial layer was removed by plasma ashing through the trench cuts made on top of thin alumina packaging layer. This method also does not require high temperature deposition or etching of sacrificial layer and it is stiction free. The encapsulation geometry can be scaled and tailored to appropriate size.

To evaluate the performance of the package, extensive RF characterization was performed as well as different reliability measurements such as high temperature operating life (HTOL), high temperature storage life (HTSL), temperature cycling, drop test, overmolding test and accelerated humidity test. No noticeable degradation was seen after these reliability experiments. The future direction includes extended hour reliability testing; the hermiticity evaluation comparing with Q of a high-Q resonator before and after packaging, and monitoring Q for a long period of time (approximately 150 hours).

For application of high dielectric constant materials to MOSFET gate oxide, the low frequency noise (LFN) noise performance of hafnium (Hf)-based high-k gate dielectric materials was extensively studied. LFN is a nondestructive way to evaluate the gate oxide quality of MOSFET device and complimentary to the charge pumping method for extending the probing range of traps located in the gate dielectrics. LFN is caused by the interaction of the carriers in the channel with the near interface oxide traps, also called border traps, and the resulting carrier number fluctuations and the correlated mobility fluctuations. For high-k gate dielectric materials, LFN can be attributed to the traps located in the interfacial layer between Si and the dielectric layer and high-k layer or even the top interface between the gate electrode and the high-k layer if the gate stacks are thin enough (< 2nm). With down-scaling of device size, it is difficult to characterize the oxide traps using the traditional capacitance-based and charge pumping techniques because of the lack of sensitivity due to the small capacitance of the devices and/or high leakage current. On the other hand, $1/f$ noise typically scales with $1/WL$, where W and L are the width and length of the device respectively, making it a promising characterization tool for sub-micron devices. Therefore, it has become an important characterization tool for quality and reliability assessment of the high-k gate dielectric materials as a gate dielectric. The investigated dielectrics include HfSiO and differently nitrided HfSiON. The devices used for this part of the work were fabricated by SEMATECH International and Texas Instruments.

The contribution from this part of the work is to study the effect of different nitridation techniques on Hf-based high-k gate dielectric materials. To evaluate the reliability we have chosen LFN measurement as the main tool. Therefore, *1/f* noise characteristics of differently nitrided hafnium silicon oxide samples are discussed. Thermally nitrided samples have the least equivalent oxide thickness (EOT) for the same physical thickness. However they show the largest *1/f* noise compared to plasma nitrided HfSiON and pure HfSiO gate dielectric MOSFETs. This phenomenon might be attributed to the increased number of Coulomb scattering sites caused by Si-N bonds near high-k/Si interface of thermally nitrided samples due to the higher processing temperatures which drive most of the nitrogen to the interface. On the other hand, plasma nitridation allows better control and therefore uniform distribution of the nitrogen across the bulk of the high-k dielectric and high-k/Si interface layer, resulting in reduced *1/f* noise compared to thermally nitrided sample. Moreover, increase in low frequency noise power spectral density with hot-carrier and constant voltage stressing is reported for nitrided HfSiO gate dielectric MOSFETs. Thermal nitridation of HfSiO to obtain HfSiON using high temperature ammonia (NH_3) anneal compounded the degradation for both types of stressing, most likely due to the increased dielectric traps in nitrided samples, which get filled during stressing and become channel carrier scattering sites. This problem can be alleviated to an extent by using plasma nitridation done at much lower temperatures. Plasma nitrided devices showed lower *1/f* noise than thermally nitrided devices, even though thermally nitrided devices scaled down the EOT (1.03nm) slightly more than plasma nitrided devices (1.06nm) for the same nitrogen content and initial HfSiO thickness.

APPENDIX A

SELF PACKAGED MEMS RESONATOR FABRICATION PROCESS FLOW

Self Packaged MEMS Resonator Fabrication Process Flow:

Each fabrication step includes CoventorWare model, optical and SEM image (where available)

1. **Wafer Cleaning**
   Clean silicon wafer with the standard TAMDI de-greasing procedure.

2. **Silicon dioxide deposition**
   Deposit 600 nm of silicon dioxide using wet thermal oxidation process in oxidation furnace.

3. **Titanium and Gold deposition**
   (a) Lithography for Ti and Au:
   - ➢ Spin coat NR9-1500PY at 2500 rpm for 40s.
   - ➢ Pre-bake the photoresist at 150^0C on the hot plate for 60s.
   - ➢ Expose the photoresist under OAI mask aligner for 16s.
   - ➢ Post-bake the photoresist at 100^0C on the hot plate for 60s.
   - ➢ Develop in RD6 for 11s.

   (b) Titanium sputtering
   Titanium was sputtered at 10mT chamber pressure for 1 min at 150W power.

   (c) Gold sputter
   Gold was sputtered at 10mT chamber pressure for 1 min 10s at 100W power.

   *(d) Lift off titanium and gold*
   Place the wafer in 1165 stripper bath floating in the ultrasonic agitation for 4~5 min. Rinse in methanol and DI water. Dry the sample with nitrogen gas.

Metal layer

Silicon dioxide
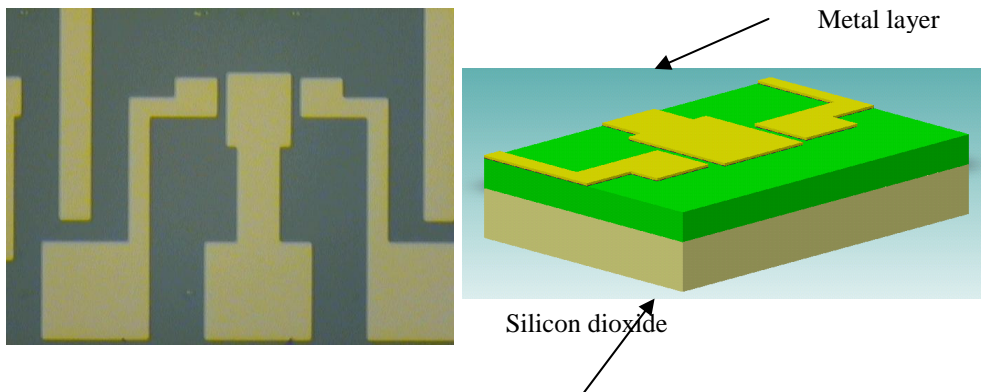
4. First sacrificial layer deposition

(a) Thin the photo definable polyimide PI-2737 by adding 50 grams of thinner T-9039 to 100 grams of PI-2737. Once the PI-2737 is diluted, allow it to stand at room temperature so it can stabilize.

(b) Spin coat diluted PI-2737 at 2000rpm for 60 seconds. Soft bake on hot plate at 70° C for 3 minutes. Hard bake at 100° C for 3 minutes.

(c) Expose for 16 seconds.

(d) Develop in the following sequence in DE 9040 and RI 9180

- Develop in 100 % DE 9040 for 11 seconds.
- Develop in 50% DE 9040 + 50% RI 9180 for 11 seconds.
- Immerse wafer in RI 9180(1st Beaker) for 11 seconds.
- Immerse wafer in RI 9180(2nd Beaker) for 11 seconds.
- Dry the sample with N_2 and check under the microscope for proper developing.

(e) Curing first sacrificial layer

Load the wafer in the oven for curing using the following conditions. Cure it for 1 hr with temperature ramping from 25° C to 300° C followed by curing at 300° C for 3 hours and finally cooling it down from 300° C to 25° C in 1 hour. Thickness of the sacrificial layer before and after curing should be around 430 nm and 240 nm respectively.
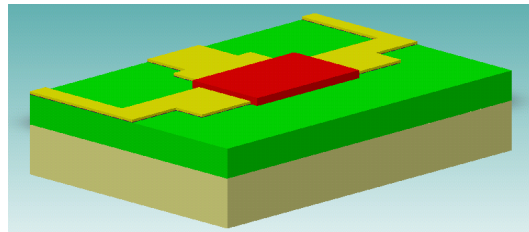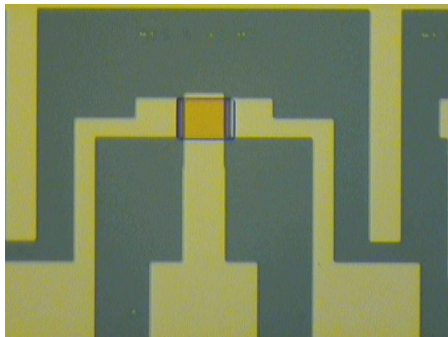
Sacrificial layer 1

5. Resonator beam deposition

(a) Negative lithography for titanium and aluminum oxide beam
  - ➢ Spin coat NR9-1500PY at 2000 rpm for 30s.
  - ➢ Pre-bake the photoresist at 150^0C on the hot plate for 60s.
  - ➢ Expose the photoresist under mask aligner for 16s.
  - ➢ Post-bake the photoresist at 100^0C on the hot plate for 60s.
 - ➢ Develop in RD6 for 12s.

(b) Titanium sputtering
   Titanium was sputtered at 10mT chamber pressure for 5min at 150W power. Ti thickness should be around 50~60 nm.

(c) Aluminum oxide sputtering
   Aluminum oxide was sputtered at 10mT chamber pressure for 20 hrs at 150 W power. Aluminum oxide thickness should be around 1.1~ 1.3 µm.
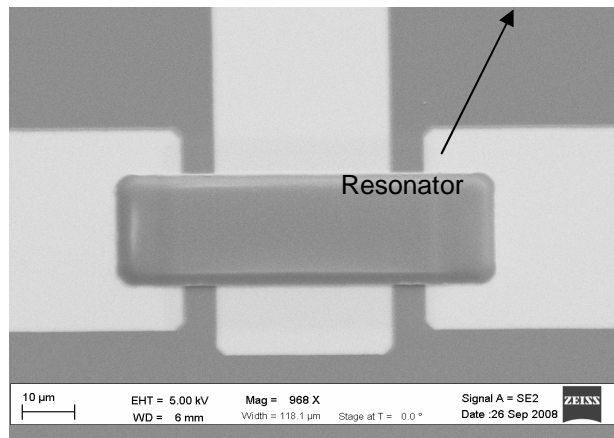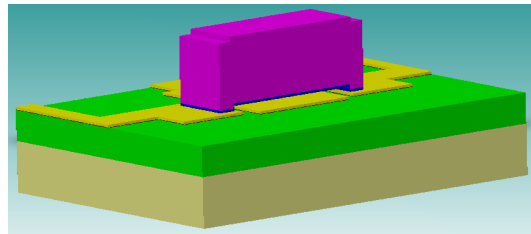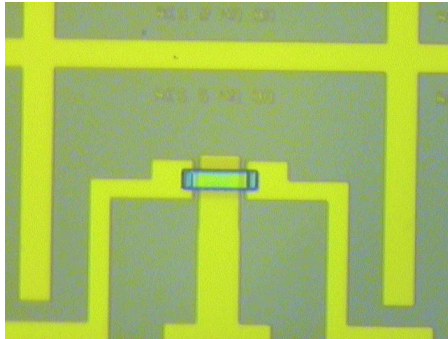
(d) Lift off titanium/aluminum oxide

   Place the wafer in 1165 stripper bath and leave it for 6 hours. Rinse in methanol only and dry the sample with nitrogen gas.
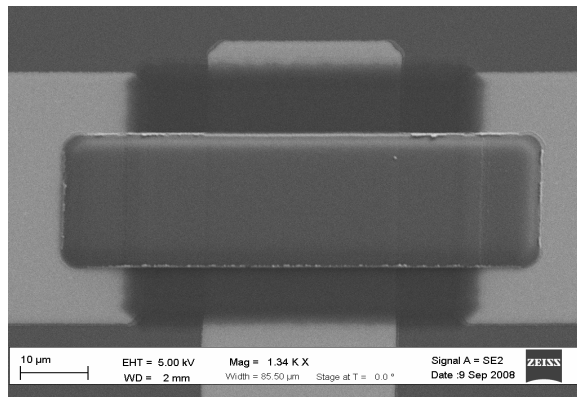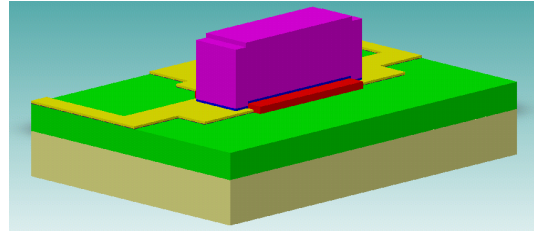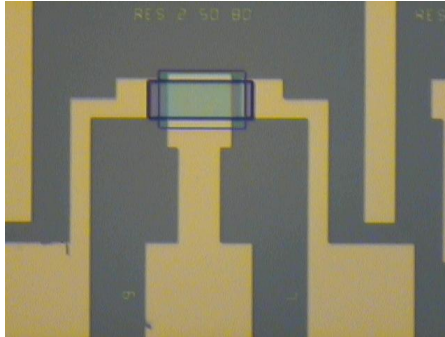
6. Ashing first sacrificial layer

Ash the first sacrificial polyimide at 150 W power and 0.6 mBar chamber pressure using asher to release the resonator beam. Inspect for the complete release of the beam.

7. Second sacrificial layer deposition

(a) Spin coat PI2737 at 1450 rpm for 60 seconds. Soft bake on hot plate at 70° C for 3 minutes. Hard bake at 100° C for 3 minutes. Expose for 16s.

(b) Develop in the following sequence in DE 9040 and RI 9180

- Develop in 100 % DE 9040 for 11 seconds.
- Develop in 50% DE 9040 + 50% RI 9180 for 11 seconds.
- Immerse wafer in RI 9180(1st Beaker) for 11 seconds.
- Immerse wafer in RI 9180(2nd Beaker) for 11 seconds.
- Dry the sample with N_2 and check under the microscope for proper developing.

(c) Load the wafer in the oven for curing using the following conditions. Cure it for 1 hr with temperature ramping from 25° C to 300° C followed by curing at 300° C for 3 hours 45 mins and finally cooling it down from 300° C to 25° C in 1 hour. Thickness of the sacrificial layer before curing 4.5 μm and after curing 3.1 μm.
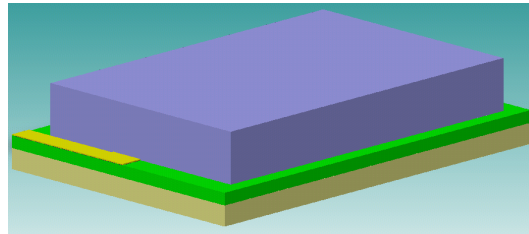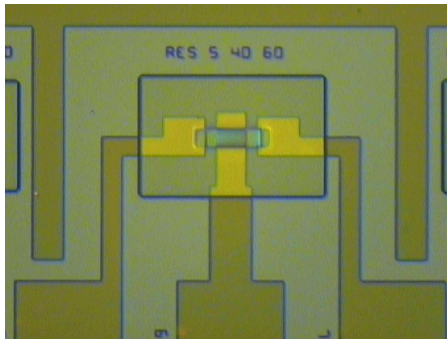
Sacrificial layer 2

8. Packaging layer deposition and opening trench cuts

➢ Spin coat NR9-1500PY at 2500 rpm for 40s.
➢ Pre-bake the photoresist at 150^0C on the hot plate for 60s.
➢ Expose the photoresist under OAI mask aligner for 11s.
➢ Post-bake the photoresist at 100^0C on the hot plate for 60s.
➢ Develop in RD6 for 14s.

Aluminum oxide sputtering

Aluminum oxide was deposited at 5 mT chamber pressure, power 150 W for 12 hrs. Aluminum oxide thickness should be around 0.8 µm. Place the wafer in 1165 stripper bath and leave it for 20 hours. Use ultrasonic agitation if necessary; make sure that every trench cut is open. Rinse in methanol only and dry the sample with nitrogen gas.
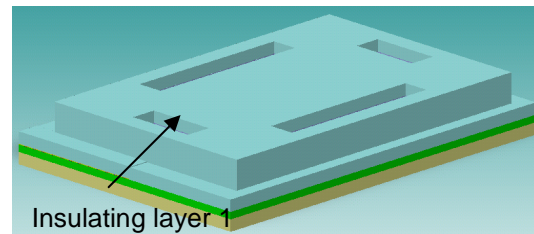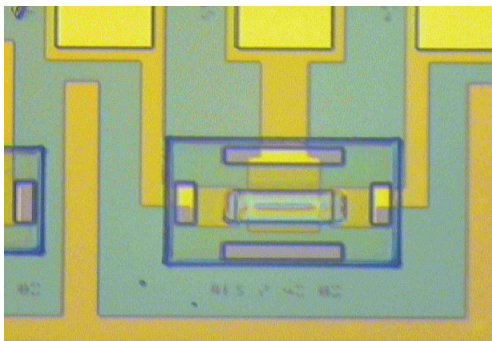
Insulating layer 1

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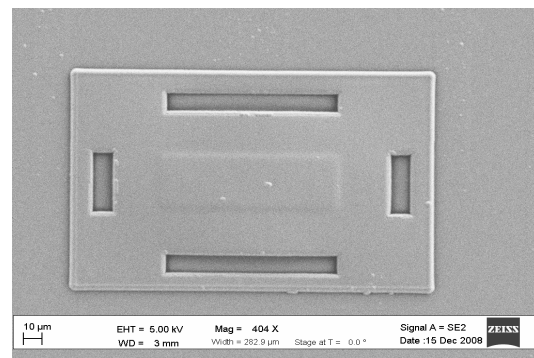
9. Ashing second sacrificial layer

Ash the second sacrificial polyimide at 150 W power and 0.6 mBar chamber pressure using asher. Inspect for the complete removal of the polymide.
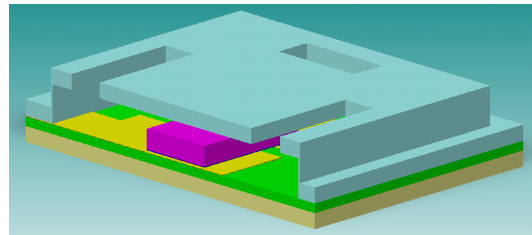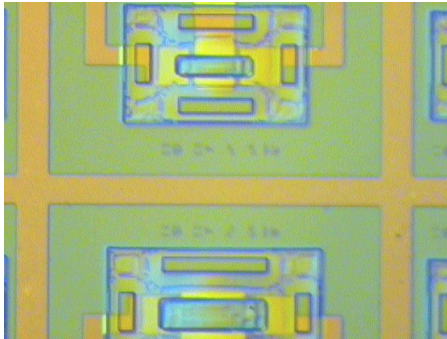
Cross section of a sealed resonator

10. Sealing layer deposition

Aluminum oxide sputtering
Aluminum oxide was deposited at 5 mT chamber pressure for 40 hours at 150 W power. Aluminum oxide thickness should be around 3.5 μm.
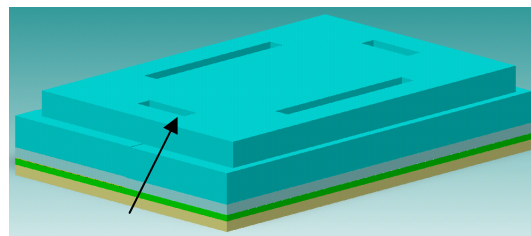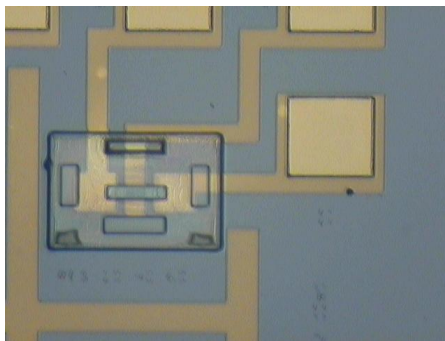
Sealing layer 1

11. Open the bond pads

> ➢ Spin coat PR1-4000A at 2000 rpm for 40s twice.
> ➢ Pre-bake the photoresist at 120^0C on the hot plate for 90s.
> ➢ Expose the photoresist under mask aligner for 20s.
> ➢ Post-bake the photoresist at 120^0C on the hot plate for 12min.
> ➢ Develop in RD6 for 35s.
> ➢ Etch in 49% HF: DI water (500ml: 20ml) for 12 min. Check with the profilometer and probe tip to make sure that the bond pad is opened completely. If not, repeat the open the bond pad procedure again.

RF IN RF OUT DC GROUND packaged resonator

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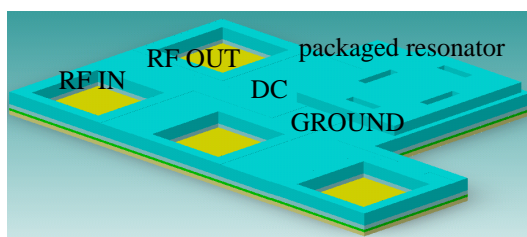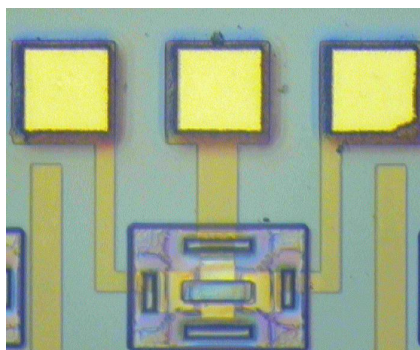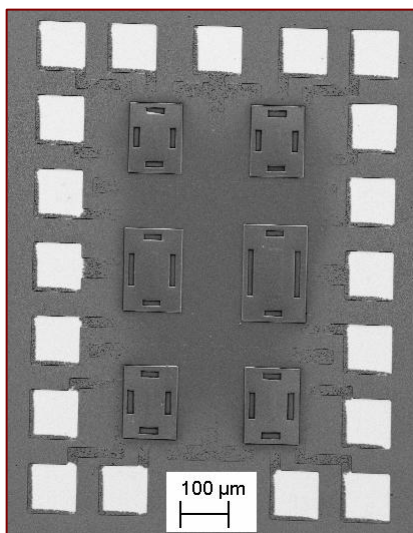
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