THERMAL EFFECTS ON ANALOG INTEGRATED CIRCUIT DESIGN

by

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DEDICATED TO MY MOTHER

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April 17, 2007

ABSTRACT

THERMAL EFFECTS ON ANALOG INTEGRATED

CIRCUIT DESIGN

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Analog Integrated Circuit design (IC) is a big challenge in this modern age. Thermal effect has a substantial role in analog ICs performance. Thermal effects on analog IC design have been investigated in this dissertation project. National Semiconductor Corporation's Vertical Bipolar Inter-Company (VBIC) model of dielectrically isolated bipolar junction transistors (DIBJT) with VIP10 and VIP11 processes have been used for the research. These devices are used for the high speed IC design. Self-heat generated inside these devices is confined within the device and degrades the device performance. In addition, the thermal characteristic of a device

surrounded by the multiple adjacent devices may be different from that of an isolated device because of the thermal coupling effect. These in turn substantially affects the circuit's frequency, dc and time response.

This research explored the modeling, characterization, and extraction of the thermal resistance which accounts for both self-heating and thermal coupling effects. Thermal resistance for the self-heating is analyzed and extracted in both frequency and dc methods. Thermal coupling resistance is extracted in dc method with different spacings among the adjacent devices. A new small signal circuit model of a DIBJT is developed for including the self-heating effect. A five element model of the thermal resistance is studied. This five element thermal resistance includes components of thermal resistances from all sides of a dielectrically isolated bipolar device. This includes adjacent device or thermal coupling effect as well. These elements describe multiple thermal poles. A simple time domain analysis is done to show their existence.

On the other side, the thermal effects have significant impact on the several analog design's performance or parameters. Therefore, several analog circuits are designed and examined the thermal effect. They are current mirrors, V_{be} based bootstrap current source, and high order bandgap reference. Thermal characterization of Y-parameters and output resistance are done as well.

Theory, simulations, and measurement results agree with the modeling, characterization, and designs presented in this dissertation. The simulations and measurements have done primarily with cadence Spectre and HP4395A network

analyzer, Agilent 87511A S-parameter test set, HP4142B Modular DC Source/Monitor, and ICCAP interfaced evaluation system respectively.

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CHAPTER 1

INTRODUCTION

Analog Integrated Circuit design and its issues, in this high technology era, are the most important and critical part for the IC world. The ever increasing growth of the integrated circuit market demand ideal performance of the circuits. On the contrary, in the real world, the perfect behavior of the analog circuits is a dream. There are several issues affecting the performance of circuits. They need to be considered while designing the analog blocks. One of the big issues, thermal effect has significant role in analog integrated circuits performance [1] - [15]. Thermal effects on analog integrated circuit design are investigated in this research work.

It is especially important to consider the thermal effects for the analog circuit designed with the dielectrically isolated complementary bipolar devices [4], [5], [16], and [17]. These devices are used for the high speed IC design [18]. Dielectrically isolated devices are made by a trench isolation process, where a very narrow and comparatively deep trench is etched on all sides of the device. The trench oxide isolation, (SiO_2), has 1% of the thermal conductivity than that of silicon (Table 1.1) [19]. Thus, SiO_2 exhibits high resistance to heat flow due to its negligible thermal conductivity. Heat generated inside the device is confined within the device and degrades the device performance. That in turn substantially affects the complete

circuit's frequency, dc and time response [1] - [3], [16], and [17]. In addition, the thermal characteristic of a device, surrounded by the multiple adjacent devices, may be different from that of an isolated device because of the thermal coupling effect [4]. Moreover due to the explosive growth of the packaging density, thermal effects are becoming more and more important issue in analog circuit design [3].

Table 1.1 Thermal conductivity of Si and SiO_2

	Si	Sio2
Thermal conductivity, k (W/cm-K)	1.412	0.014

Thermal effects in integrated circuits can be categorized as thermal coupling, self-heating and package thermal effect [3]. This research focused on self-heating and thermal coupling. To describe the self-heating and the thermal coupling effect on the semiconductor devices and analog circuits, the in depth knowledge of the modeling and characterization of the thermal resistance must be understood. The analog circuit design must be perceived as well to invent the thermal effect on the circuits.

1.1 The Dielectrically Isolated Device

A dielectrically isolated device from the National Semiconductor's complementary bipolar process, VIP10, is shown in Fig. 1.1 [18]. These devices are complementary NPN and PNP bipolar devices. They offer the best possible performance and features as required by the today's high speed amplifiers. The market demand for high bandwidth is increasing everyday. As a whole, the high performance amplifier need high bandwidth, low power consumption, low supply voltages, large

output swing, high output current and low distortion. All of these can be achieved by using the state of the art designs with these VIP10 devices.

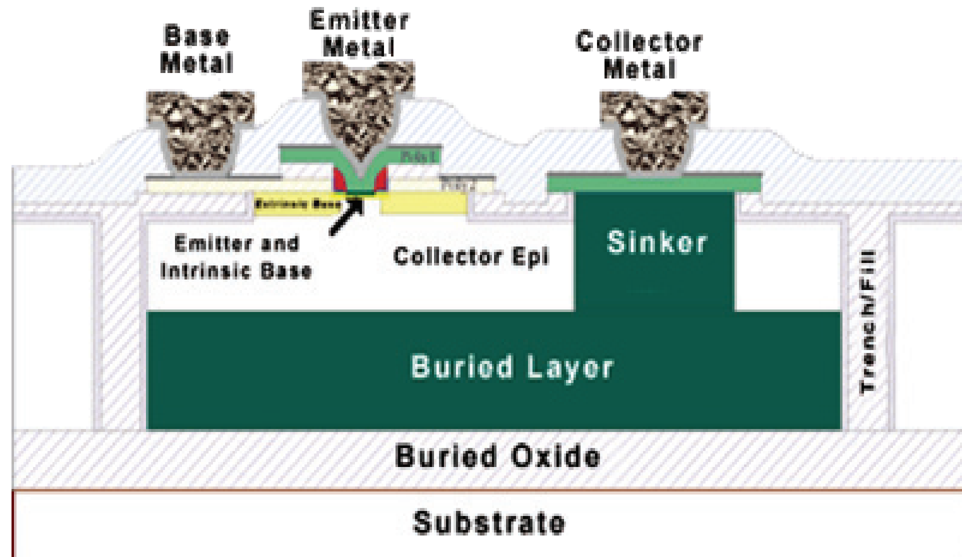


Figure 1.1 Cross section of a DIBJT from VIP10 process [18].

The ICs build by these devices find their applications in high speed DSL and cable modems, set-top boxes, contact image scanners, DVD players and CD-ROMs [18]. In addition, for the portable device (USB, gaming, medical, camera and many others) applications, power consumption must be low. They need single-supply operation with low voltage. In order to meet these market demands, these devices are developed.

The table 1.2 presents some of high profile characteristics for these complementary bipolar processes. It includes the prime parameters for both the NPN and PNP devices. In the table DI stands for dielectrically isolated.

Table 1.2 Important parameters for the DIBJT devices [18]

Devices	F_t GHz	β	V_a	C_{js} fF	Emitter Width μm	Min. Transistor Area μm^2	Max. Supply Voltage V	Isolation
NPN	9	100	120	5	1	300	12	DI
PNP	8	55	40	5	1	300	12	DI

1.2 Organization of the Dissertation

This project involves several research works of thermal effect modeling, characterization, analysis, analog circuit design and thermal effects on the performance of the designs. The thesis is described as follows.

In chapter 2, the dielectrically isolated VBIC bipolar device is characterized. This chapter describes the mechanism of the thermal effect as well. There are several simulations and measurements have done to see the basic characteristics of the device used for the research. They are i) I_c versus V_c, ii) Gummel plot (I_c, I_b versus V_{be}), iii) β versus I_c etc. In addition, various simulations have done to see the temperature effect. They include but not limited to i) I_c vs. V_c at different temperature, ii) thermal transconductances, iii) junction temperature (T_j) versus nominal temperature (T_{nom}), iv) thermal power (P_{th}) versus T_j etc.

In chapter 3, thermal modeling and characterization in dc domain is presented. This has been done for the adjacent device thermal effect. In doing so, a novel procedure for modeling adjacent device heating effects (thermal coupling) has been

developed for the thermal coupling of multiple devices in an integrated circuit. But, part of the procedure is equally applicable to a single device modeling in dc domain.

In this chapter a five element model of the thermal resistance is studied and described. This five element thermal resistance includes components of thermal resistances from all sides of a dielectrically isolated bipolar device of Fig. 1.1. This includes an element for the adjacent device or thermal coupling effect as well. A compact thermal circuit model is developed for the adjacent devices as well. In addition, the thermal resistances for the self-heating and thermal coupling are extracted. This is done in dc method. A set of I_c versus V_c plots at different temperatures are used to extract the thermal resistance. In the I_c versus V_c plots a constant collector current with constant gain and constant junction temperature at different ambient temperatures plays a critical role for the extraction. Several test structures are fabricated and measured to extract the thermal coupling resistance. This extraction is done by heating the adjacent devices and measures the temperature rise of the other adjacent device. The test structures also consider the variable spacings among the adjacent devices.

A time domain analysis for the VBIC dielectrically isolated device is shown in chapter 3 as well to see the thermal behavior. This is done by plotting dt/P_{th} versus time plot. This includes multiple poles simulation by externally adding the extra poles. These poles are associated with the five elements of the thermal resistance.

Chapter 4 explores the frequency dependent modeling and characterization of the thermal effects. A new small signal circuit model of a dielectrically isolated bipolar transistor is developed for including the self-heating effect [2]. Two dependent current

sources are added are included at the collector and base node. They are associated with the thermal transconductances at the base and collector and the temperature increment by the self-heating effect.

The Y parameters are mostly affected by the thermal problem. Thus they are used for the characterization with respect to the frequency. The Y_{22} parameter is the most affected parameter by the self-heating. Thus the Y_{22} parameter versus frequency bode plot is used for the thermal resistance extraction. Initially S parameter simulations and measurements have done and then convert these in to Y parameters. The Y_{22} parameter is characterized and plotted with respect to several device and circuit parameters including thermal resistance, thermal capacitance, saturation current, collector current, bias points while considering self-heating effect. A balanced differential amplifier is used for the simulations and measurement.

An analysis has been done to see the self-heating effect on the small signal open loop gain. A differential amplifier with current mirror active load is designed, simulated and measured to prove the analysis. It is found to be the gain of the amplifier is decreased or distorted at low frequency for the effect of self-heating.

While considering the thermal effects, it is found that, they have significant impact on the several analog circuits' performances. This brings the rest of the research to design several analog circuits and analyze the self-heating and thermal coupling effects on them.

In chapter 5, the thermal effect on the current mirrors performance is investigated and a theory is developed to express the thermal offset of a current mirror.

This research examines the impact of the thermal effect on the output characteristics of the current mirrors. This research has found and emphasized the output resistance decrement with the self-heating effect. In general all the frequently used current mirrors in analog IC design are analyzed, simulated and measured. In a step by step procedure it is shown that the self-heating thermal effect is reduced or can be made negligible for the advanced mirrors; i.e. for the cascode connected and Wilson current mirrors. In addition, thermal coupling effect on a simple current mirror is measured for a couple of separations between the devices. A current feedback operational amplifier's (CFOA) high impedance node (which is comprised of two current mirrors) is simulated with and without self-heating to observe the thermal problem [17]. Analog circuit without current mirror is a kind of impossibility.

In chapter 6, another sub-circuit, the V_{be} based bootstrap (self-bias) current source is designed and measured. The self-heating effects on its sensitivity performance are examined as well. The error due to the self-heating effect is identified and minimized. The minimization is done by using several combinations of NPN and PNP current mirrors and V_{be} referenced current sources in the bootstrap topology. A current source is proposed, which has improved sensitivity and less self-heating effect over the conventional bootstrapped V_{be} referenced current source. This sub-circuit finds many applications as a bias circuit, especially in the input stage of an amplifier.

Chapter 7 presents one of the most important designs in analog domain, a high order curvature corrected bandgap current/voltage reference circuit. A very high performance high order bandgap reference circuit is designed and analyzed its

performance with considering the self-heating effect. Temperature is the most critical parameter for a bandgap reference. The temperature sensitivity for the reference becomes more critical when self-heating increases the devices temperature. This is because the bandgap reference design topology mainly considers and depends on the V_{be} and PTAT current source, which are affected by the temperature increment caused by the thermal effect. It has been established the theory and procedure to compensate the self-heating effect. A designed circuit is fabricated and measured. The design shows improved thermal performance as compared to other published bandgap reference circuits which also minimizes the self-heating effect properly. The proposed design can accommodate a wide range of reference currents/voltages from a few µA to mA and a few mV to a several V range.

Finally, some conclusions have drawn in chapter 8. It has given some future scopes and extensions for this research as well.

CHAPTER 2

THERMAL CHARACTERIZATION OF THE VBIC DIELECTRICALLY ISOLATED DEVICE

2.1 The VBIC Model

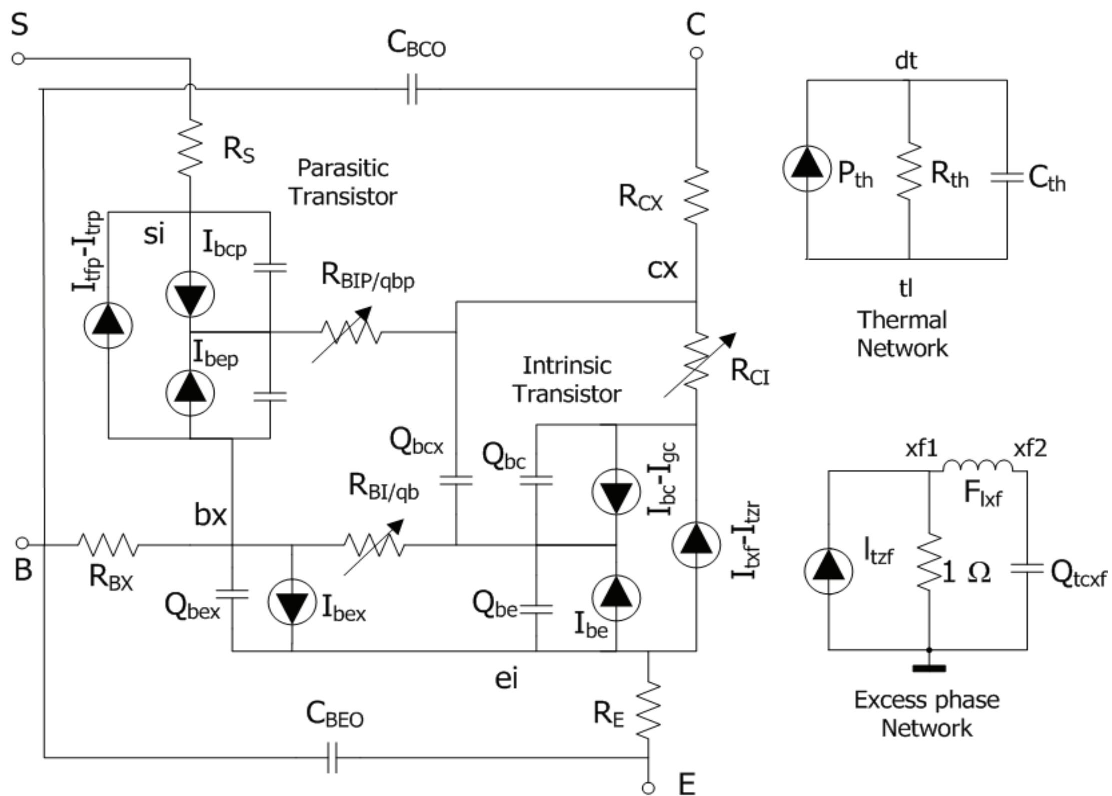


Figure 2.1 VBIC model.

A VBIC model is shown in Fig. 2.1 [9], [20]. The detail about the VBIC model is illustrated in Appendix A. The VBIC model incorporates the thermal nodes of a device. Semiconductor devices are strongly influenced by the thermal effects. When the

device is heated, it raises its local temperature which changes the device's intrinsic parameters. The VBIC model pseudo-code considers the thermal effects on all of the related device parameters for perfect modeling with equations.

2.2 The Thermal Model

In Fig. 2.1 dt and tl are the temperature rise due to self-heating and local temperature nodes respectively. R_{th} and C_{th} are the thermal resistance and capacitance respectively. I_{th} is the thermal power, which can also be represented by P_{th}. The thermal power and the temperature rise 'dt' can be expressed as [2], [4]

$$P_{th} = V_{be} \times I_b + V_{ce} \times I_c \tag{2.1}$$

$$dt = \left(T_j - T_{ambient}\right) = R_{th} P_{th} \tag{2.2}$$

where T_j and $T_{ambient}$ are the junction and ambient temperatures respectively. $T_{ambient}$ is the same as T_{nom} for the simulation in this chapter. T_{nom} is the temperature at which the device parameters are measured.

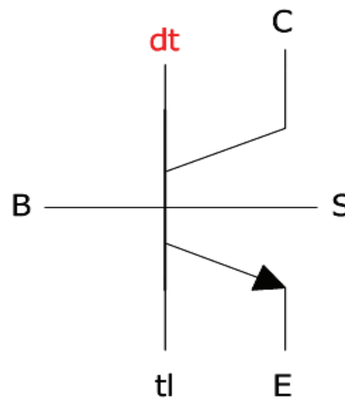


Figure 2.2 A bipolar transistor including local temperature (tl), temperature rise (dt) and substrate (S) nodes.

In (2.2), it is found that, R_{th} is the ratio of the temperature rise and the thermal power (dt/P_{th}). The units for R_{th} and C_{th} are °C/W and F respectively. In the frequency and time domains C_{th} helps determine the thermal time constant since it is the product of the R_{th} and C_{th}. More about the thermal parameters will be described in detail in the following chapters in dc, time and frequency domain.

A five terminal bipolar model including the local temperature (tl), the temperature rise (dt) and the substrate nodes is shown in Fig 2.2. The dt and tl nodes incorporate the R_{th}, C_{th} network with the device.

2.3 The Mechanism of the Thermal Effect on the Saturation Current

The saturation current of an NPN device can be expressed and formulated as follows [21],

$$I_s = \frac{qA\, n_i^2 D_n}{Q_B} \tag{2.3}$$

where, q is the electron charge, A is the cross sectional area of the emitter, n_i is the intrinsic carrier concentration, D_n is the electron diffusion co-efficient and Q_B is the base charge. The electron diffusion co-efficient, intrinsic carrier concentration and the electron mobility can be evaluated as [21]

$$D_n = \mu_n \frac{kT}{q} \tag{2.4}$$

$$n_i^2 = DT^3 \exp\left(\frac{-E_g(0)}{V_t}\right) \tag{2.5}$$

$$\mu_n = CT^{-n} \tag{2.6}$$

in which, k is the Boltzmann constant, μ_n is the electron mobility, T is the temperature, $E_g(0)$ is the band-gap voltage of silicon at 0 °K and V_t (= kT/q)is the thermal voltage.

It can be observed in equations (2.3)-(2.6) that, any temperature rise can affect the D_n, n_i and μ_n. The intrinsic carrier concentration, n_i increases strongly with the temperature. The n_i doubles for every 8 °C temperature increase near room temperature [19]. When the temperature increases, lattice vibrations are larger. Then the collisions between electrons and the lattice vibrations are very important [19]. The theoretical and experimental analyses indicate that the value of n in (2.6) varies from 1.5 to 3 [m&k]. Thus, the mobility decreases with the temperature but less strongly as compared to the intrinsic carrier concentration. Therefore n_i tends to dominate I_c [3]. Including all the effects the expression for the saturation is given by the following equation

$$I_S = \frac{qAk}{Q_B q} CDT^{4-n} \exp\left(\frac{-E_g(0)}{V_t}\right) \tag{2.7}$$

Now, since the self-heating is confined within the device for the dielectrically isolated technology, it raises the device temperature. Thus, as seen from (2.7), I_s would increase when the self-heating is significant. This in turn increases the collector current. Now, the I_s equation with self-heating effect can be proposed as

$$I_S = \frac{qAk}{Q_B q} CD\left(T + dt\right)^{4-n} \exp\left\{\frac{-qE_g(0)}{k(T + dt)}\right\} \tag{2.8}$$

where, dt is the temperature rise due to the self-heating effect. The P_{th} and R_{th} values in (2.1) determine the actual temperature increment of the device due to self-heating.

2.4 Different Temperature and Thermal Simulations

It is very important to know the natural behavior of the device used for design or research. Fig. 2.3 shows pretty good gain and Gummel (I_c, I_b versus V_{be}) characteristics over a wide range of collector current. These devices are robust and used

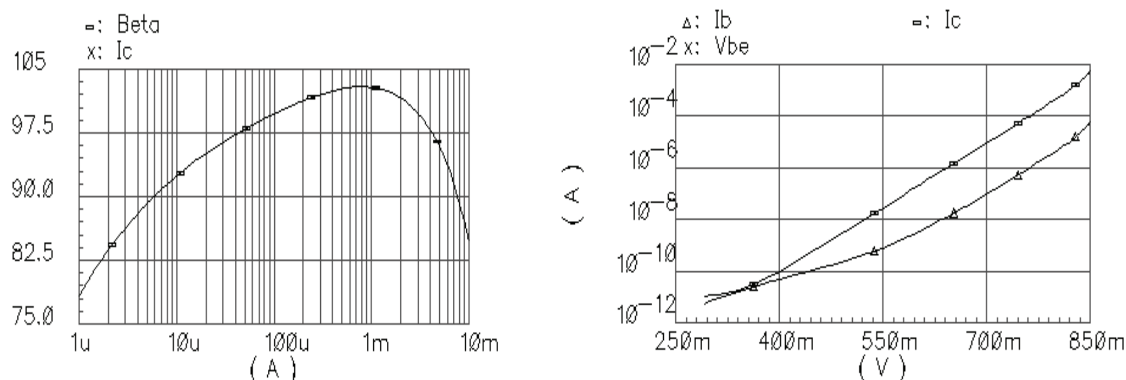


Figure 2.3 Beta versus I_c and I_b, I_c versus V_{be}.

for many analog circuits. In the following sections, several temperature characteristics of the transistor are presented and explained as required. These include simulations and measurements (only for I_c vs. V_c at different temperatures) from the fabricated chip.

2.4.1 Collector Current versus Collector Voltage at Different Temperatures with and without Self-heating

The collector current increases with the temperature in forward active region. There are sixteen I_c graphs at four different temperatures shown in Fig. 2.4. In addition, these plots include early voltage (VEF =100 or 0) and self-heating (selft = 1 or 0) effects. In spice modeling, the early voltage ‘0’ means infinity. Therefore, the four sets of plots correspond to i) T = 27 °C, VEF = 100 or 0, selft = 0 or 1, ii) T = 30 °C, VEF = 100 or 0, selft = 0 or 1, iii) T = 33 °C, VEF = 100 or 0, selft = 0 or 1 and iv) T = 36 °C,

VEF = 100 or 0, selft = 0 or 1.The temperature characteristics of the collector current become steeper when self-heating is on in the device. The measurement result in Fig. 2.5 shows the similar plots. The measurement is done for the lower current. These validate the self-heating theory as expected and derived earlier in this chapter.

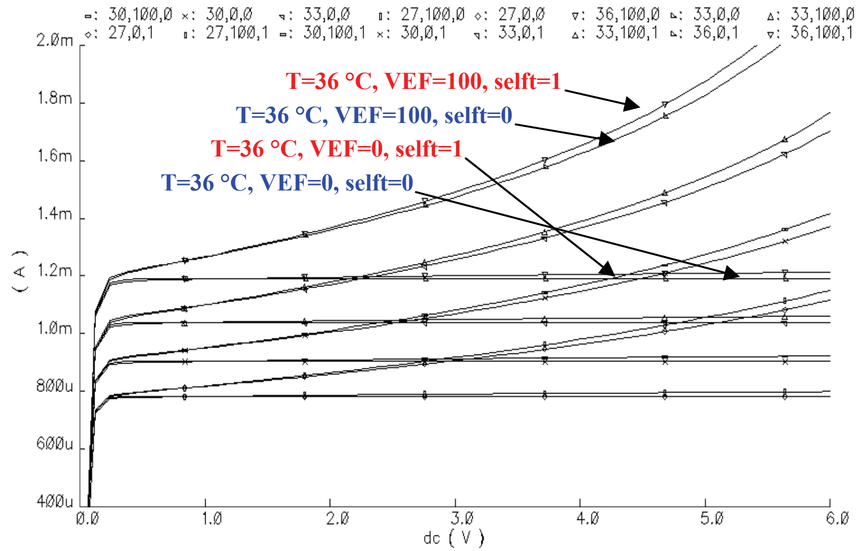


Figure 2.4 I_c vs. V_{ce} at different temperatures with and without self-heating turned off.

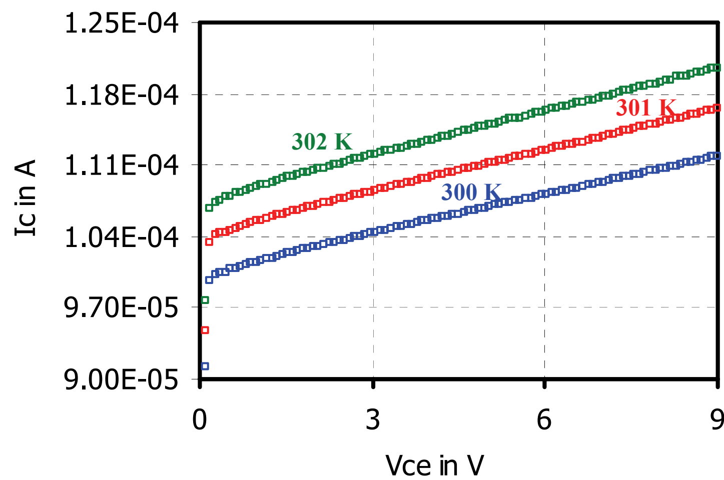


Figure 2.5 Measurement of I_c vs. V_{ce} at different temperatures (part no. UTA208).

2.4.2 Collector Current (I_c) and dI_c / dt versus Temperature

The collector current is simulated with respect to the temperature. The simulated results of the collector current and its temperature derivative versus temperature are shown in Fig. 2.6. The temperature derivative of the collector current is defined as the thermal transconductance (g_{ct}) at the collector [2]. This will be used in chapter 5 for the frequency dependent thermal analysis.

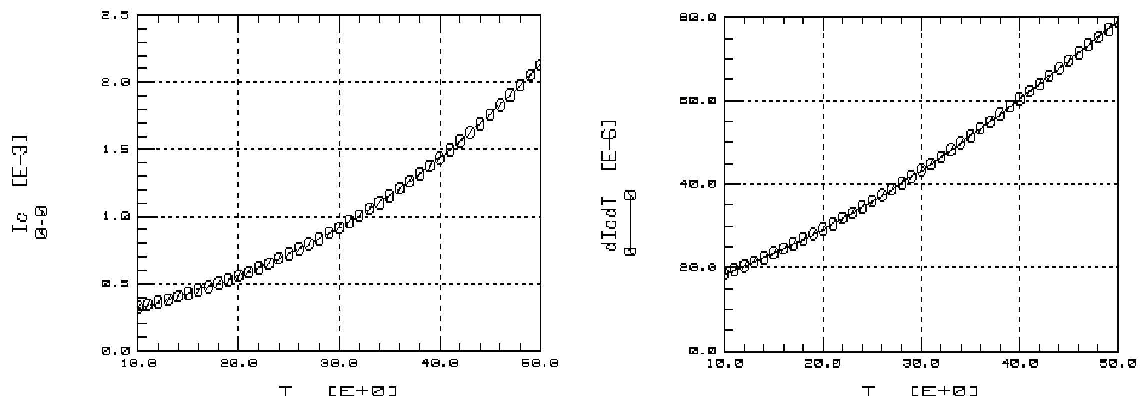


Figure 2.6 I_c and dI_c/dt versus T.

2.4.3 Base Current (I_b) and dI_b / dt versus Temperature

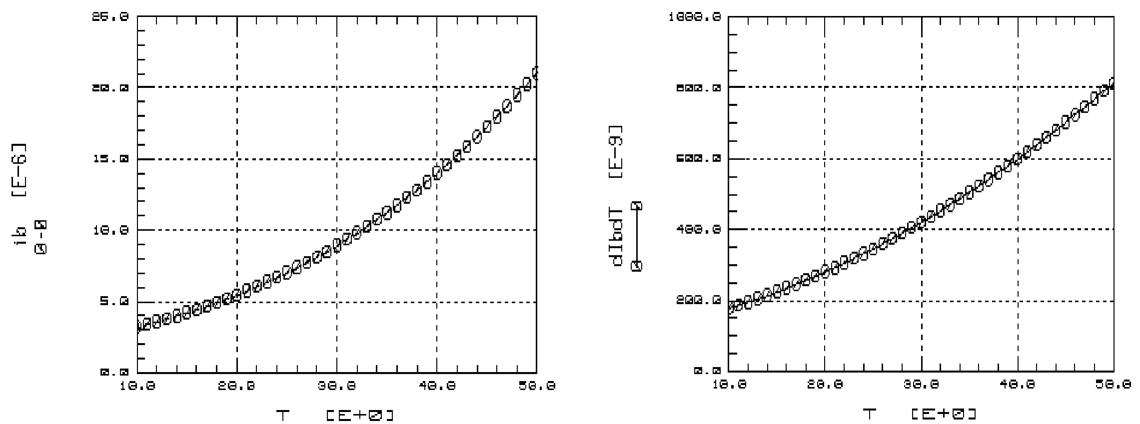


Figure 2.7 I_b and dI_b/dt versus T.

The base current is simulated with respect to the temperature. The simulated results of the base current and its temperature derivative versus temperature are shown in Fig. 2.7. The temperature derivative of the base current is defined as the thermal transconductance (gbt) at the base [2]. This will also be used in chapter 5 for the frequency dependent thermal analysis.

2.4.4 Junction Temperature versus Thermal Power

The junction temperature is plotted with respect to the thermal power. Fig. 2.8 shows how T_j increases with the thermal power, P_{th}. The dT_j/dP_{th} plot is the thermal resistance. The derivative of the (T_j-$T_{ambient}$) or T_j (when, $T_{ambient}$ is constant) is the thermal resistance. This can be found as

$$\frac{dT_j}{dP_{th}} = R_{th} \tag{2.9}$$

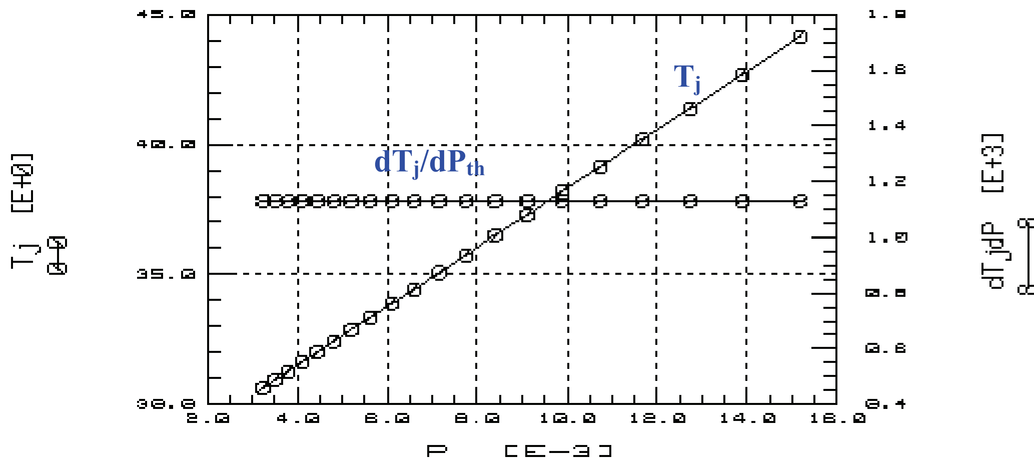


Figure 2.8 T_j and dT_j/dP_{th} versus P_{th}.

2.4.5 Ambient Temperature versus Thermal Power

The ambient temperature can be plotted with respect to the thermal power. The T plot in Fig. 2.9 shows how the ambient temperature rises with increasing the thermal power, P_{th}. The dT/dP_{th} plot in Fig. 2.9 shows how the dT/dP_{th} decreases with increasing the thermal power dP_{th}. The nonlinear characteristics of the plots are expected as the collector and base currents are nonlinear to the temperature variations.

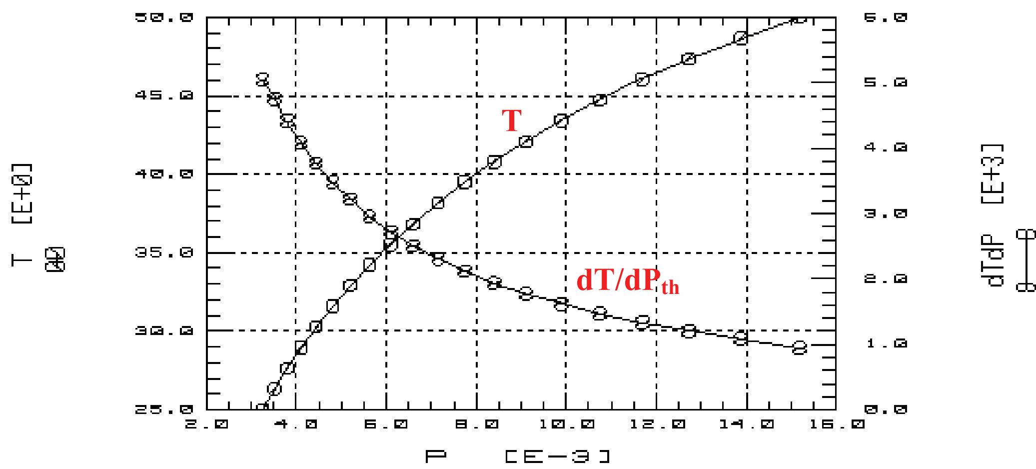


Figure 2.9 T and dT/dP_{th} versus P_{th}.

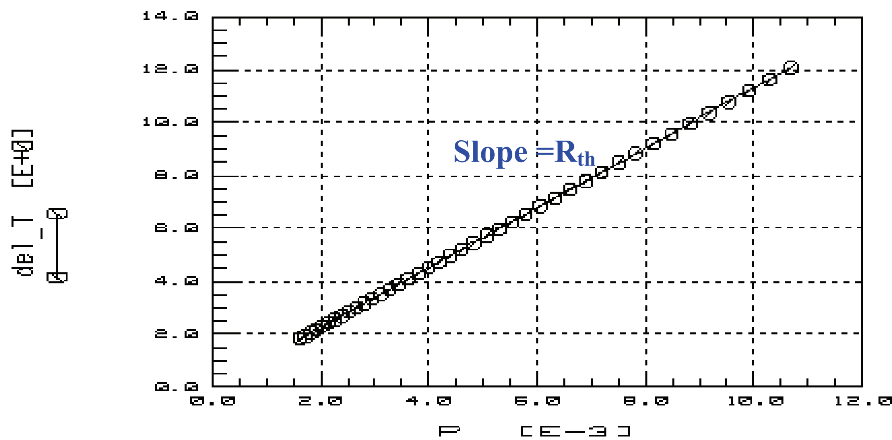


Figure 2.10 dt versus P_{th}.

2.4.6 Temperature Rise versus Thermal Power

Again, the temperature rise, dt (=Tj-Tambient) versus Pth is plotted in Fig. 2.10. So, the slope of the following plot is the thermal resistance as shown in (2.10).

$$\frac{dt}{P_{th}} = R_{th} \tag{2.10}$$

2.5 Temperature Measurement

Temperature measurement is done by using a forward Gummel or a reverse Gummel connected bipolar transistor inside the chip.

2.5.1 Temperature Measurement Using Standard Forward Gummel Connection

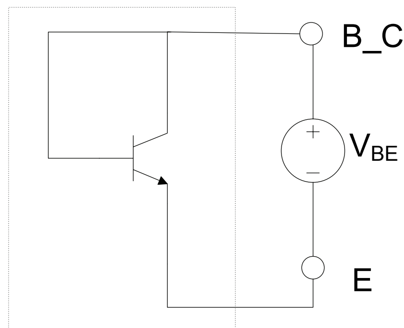


Figure 2.11 Standard forward Gummel set-up for the temperature measurement.

The standard forward Gummel configuration is shown in Fig. 2.11. A linear voltage sweep is applied between the base and the emitter of the BJT. The base and collector terminals are internally shorted in the chip. In this configuration, the variation of collector current as a function of base-emitter voltage is measured. The following equations describe the required voltage-current characteristics.

$$I_c = I_s\left\{\exp\left(\frac{V_{be}}{NF \cdot V_t}\right) - 1\right\} \tag{2.11}$$

$$\ln I_c = \ln I_s + \frac{1}{NF \cdot V_t} V_{be}$$

where the ideality factor (NF) is assumed unity.

$$\frac{\partial \ln I_c}{\partial V_{be}} = \frac{1}{V_t}$$

$$T = \frac{q}{k}\frac{\partial V_{be}}{\partial \ln I_c} \tag{2.12}$$

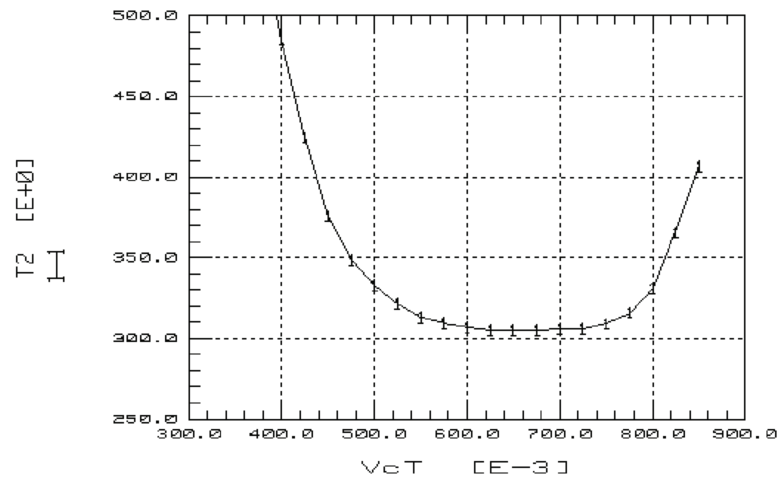


Figure 2.12 Standard forward Gummel set-up for temperature measurement.

A transform function is written in ICCAP By using the equations derived above. The measurement is done by varying V_{be} ($=V_{cT}=V_c$) of Fig. 2.11 and measuring I_c. The measurement is converted to a temperature plot (Fig. 2.12) by using (2.12). The minimum temperature of the T vs. V_{be} plot is the measured temperature of the device [22].

2.5.2 Temperature Measurement Using Standard Reverse Gummel Connection

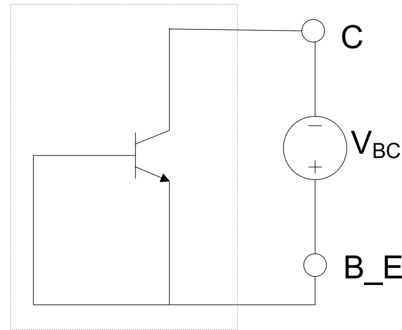


Figure 2.13 Standard reverse Gummel set-up for temperature measurement.

The standard reverse Gummel configuration is shown in Fig. 2.13. A linear voltage sweep is applied between base and collector of the BJT. The base and emitter terminals are internally shorted in the chip. In this configuration, the variation of emitter current as a function of base-collector voltage is measured. The following equations describe the required voltage-current characteristics.

$$I_e = I_s\left\{\exp\left(\frac{V_{bc}}{NR \cdot V_t}\right) - 1\right\} \tag{2.13}$$

$$\ln I_e = \ln I_s + \frac{1}{NR \cdot V_t} V_{bc}$$

$$\frac{\partial \ln I_e}{\partial V_{bc}} = \frac{1}{V_t}$$

$$NR = 1$$

$$T = \frac{q}{k}\frac{\partial V_{bc}}{\partial \ln I_e}$$

If I_b ignored,

$$T = \frac{q}{k}\frac{\partial V_{bc}}{\partial \ln I_c} \qquad (2.14)$$

By using the equations derived above a transform function is written in ICCAP. The measurement is done by varying V_{bc} ($-V_c$) of Fig. 2.13 and measure I_c. The I_c versus $-V_c$ graph for both the simulation and measurement is shown in Fig. 2.14. The measurement is converted to a temperature plot (Fig. 2.15) by using (2.14). The minimum temperature of the T vs. V_{bc} ($-V_c$) plot is the measured temperature of the device [22].

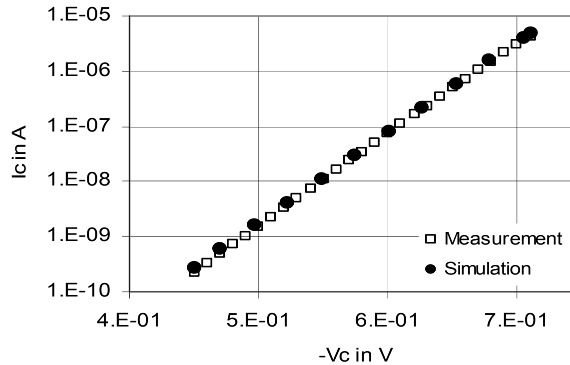


Figure 2.14 I_c vs. $-V_c$ (=V_{bc}), simulation and measurement.

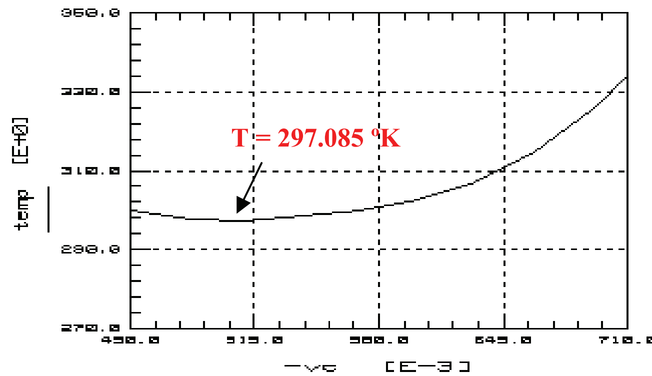


Figure 2.15 Measurement of temperature vs. $-V_c$ (=V_{bc}).

2.6 Conclusion

The VBIC dielectrically isolated device is characterized in this chapter. This is mostly done for the thermal effect. The basic I-V characteristics and the Gummel plot included as well. The thermal resistance is assumed temperature independent in some cases. For the measurement ICCAP and HP4142 measurement setup is used. But, for the measurement, Cadence Spectre and ICCAP Spectre are used.

CHAPTER 3

ADJACENT DEVICE THERMAL EFFECT MODELING AND DC CHARACTERIZATION

A novel procedure for modeling and characterization of adjacent device heating effects (thermal coupling) of dielectrically isolated bipolar junction transistors is presented in this chapter [4]. A new thermal model has been studied and developed for the thermal coupling of multiple devices in an integrated circuit. The spacings among the adjacent devices are considered as well. A new measurement technique is developed to find the self-heating thermal resistance and thermal coupling resistance for that circuit. Multiple test structures have been fabricated and tested to see the thermal coupling effect.

The existing VBIC model for bipolar devices considers the self-heating effect. This includes the R_{th}, C_{th} and P_{th} effects in the modeling by using equations with the Pseudo-codes [appendix B]. But the VBIC modeling techniques do not have parameters to model the adjacent device heating effects. Hence it is essential to make necessary changes in the VBIC model file or develop circuit level modifications to accommodate the adjacent device heating effects. Thermal coupling presents a challenge because of increased device density on a chip. Shelar and Visweswaran show how the current mirror performance varies with the device heating, which is one of the principal circuits in analog design [23].

3.1 Five Element Thermal Resistance Model

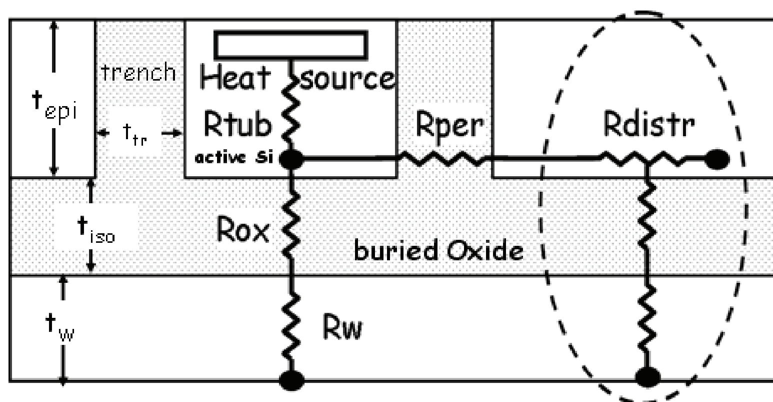


Figure 3.1 Five element thermal resistance model.

Advanced processes are used to fabricate bipolar devices with trench isolation. This technique is suitable for very fine features. In this isolation technique, a very narrow and relatively deep trench is etched around the device to be isolated. The trench is filled with an insulating material like SiO_2. Thus the device is surrounded on all sides by SiO_2, which offers high resistance to heat flow. Consequently, the devices are affected by thermal heating. The maximum heat flow occurs through the interconnecting conductors.

The physical dielectrically isolated bipolar device structure of is shown in Fig. 3.1. Using this physical structure and knowing the properties of the each region, a five element thermal resistance model has been invented and developed previously [5] and [20]. The five components of the thermal resistance of the dielectrically isolated BJT are shown in Fig. 3.1. The five thermal resistance components are, i) R_{tub} for the active region, ii) R_{ox} for the isolation at the bottom of the tub, iii) R_w for the wafer, iv) R_{per} for the peripheral trench oxide, and v) R_{distr} for the inter device and distributed conduction.

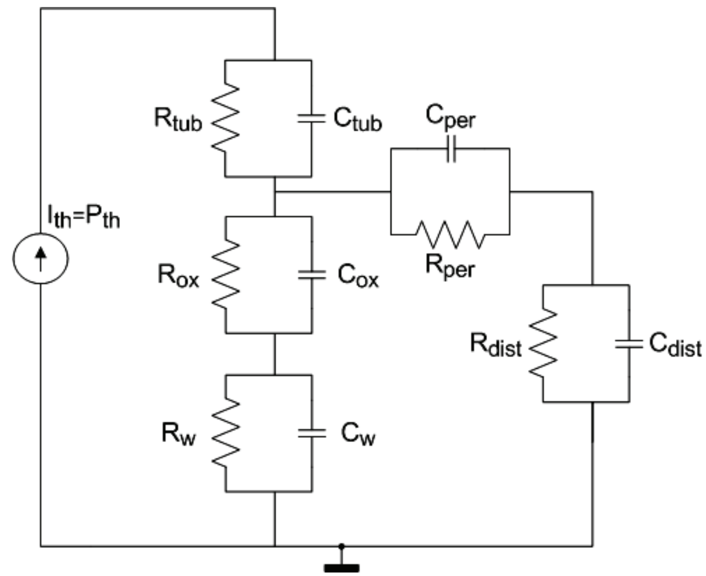
The maximum heat source region is indicated in the figure as a rectangle. The epitexial depth, base diffusion depth, heat source to isolation layer depth, trench oxide thickness, refill oxide depth and isolation oxide thickness etc. are known from the device dimensions.

Thus the individual resistances can be evaluated by knowing the dimensions of each region. The total thermal resistance of the dielectrically isolated device can be computed from these elements as

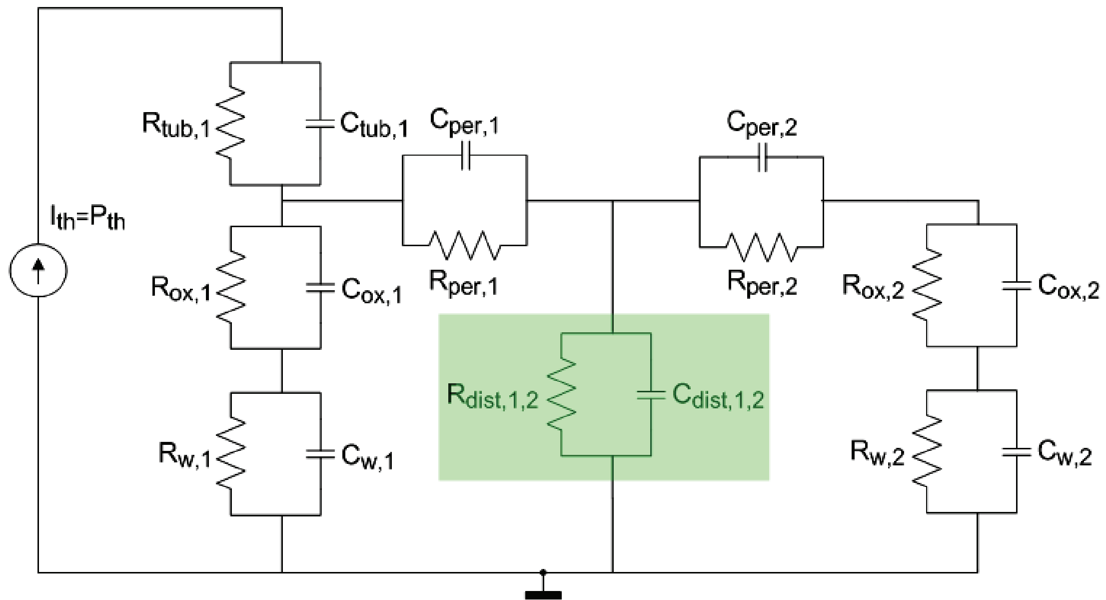
$$R_{th} = R_{tub} + \frac{1}{\left(\frac{1}{R_{ox} + R_{w}}\right) + \left(\frac{1}{R_{per} + R_{dist}}\right)} \tag{3.1}$$

3.2 Adjacent Device Model

The dielectrically isolated devices (Fig. 3.1) are used in the integrated circuit design. Thus they have an inter-device heating effect. A compact thermal circuit model has been developed for the adjacent device heating effect, in which the thermal resistance of each device is divided into five elements. Each of these five resistances represents the thermal resistance of a particular part of the device. They depend upon the geometry and the material properties in that region. This is shown in (3.1). One of the five elements, R_{dist} represents the inter device and distributed thermal resistance, which accounts for the heating effect with the adjacent device.



(a)



(b)

Figure 3.2 Adjacent device coupling parameter circuit model. (a) A single device and (b) Two devices, 'device1' and 'device 2' connected together The common elements $R_{dist,1,2}$ and $C_{dist,1,2}$ are high lighted.

An equivalent compact circuit model is developed using the five elements for a t device as shown in Fig. 3.2(a). coupling of two devices. The equivalent circuit for two adjacent devices, ‘device 1’ and ‘device 2’, is shown in Fig. 3.2(b). The resistance components in Fig. 3.2 accounts for five element thermal resistance. I_{th} (P_{th}) is the thermal power. Each thermal resistance in Fig. 3.2 incorporates a corresponding thermal capacitance to account for the thermal effect delay and thermal frequency response. Thermal capacitances related to the thermal time constants.

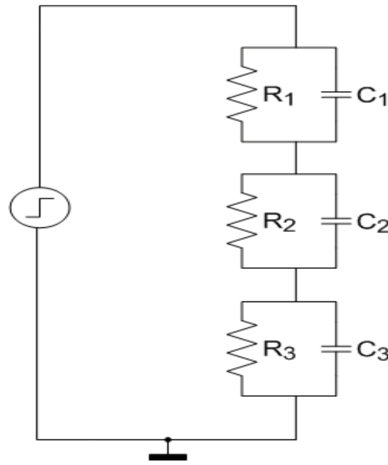
$$R_{th\,x,y} \cdot C_{th\,x,y} = \tau_{th\,x,y} \tag{3.2}$$

where τ_{th} is the thermal time constant while subscript x,y stands for silicon or oxide. This delay is a function of the physical dimension of each part of the thermal circuit.

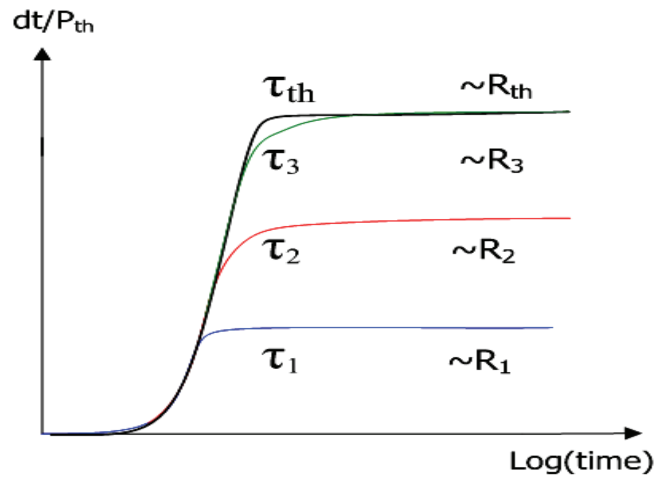
The five element thermal model uses five thermal resistances and capacitances. This brings the idea of multiple pole thermal model. It can be clarified in time domain analysis. It can be understand that, the device has multiple thermal time constants according to the multiple thermal resistance and capacitances. The analysis can be done by plotting dt/P_{th} versus log (time) for the thermal model shown in Fig. 3.3(a). The dt and P_{th} are the temperature rise due to the thermal effect and the thermal power respectively. Actually, by definition dt/P_{th} is the thermal resistance. The symbolic plots in time domain are shown in Fig. 3.3(b). The plot uses three time constants corresponds to R_1C_1, R_2C_2 and R_3C_3 time constants. The three time constants are τ_1, τ_2 and τ_3.

The equation (3.3) shows the relation among the thermal resistance components and the time constants.

$$R_{th} = R_1\left(1 - e^{-t/\tau_1}\right) + R_2\left(1 - e^{-t/\tau_2}\right) + R_3\left(1 - e^{-t/\tau_3}\right) \tag{3.3}$$



(a)

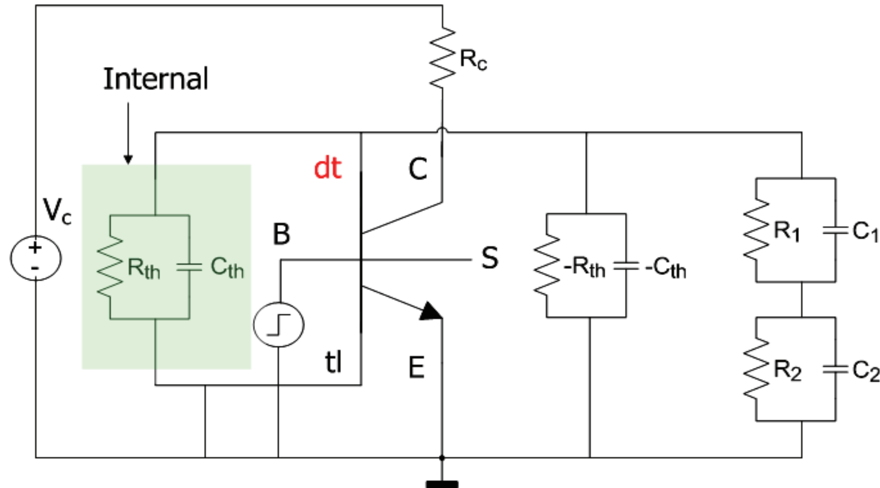


(b)

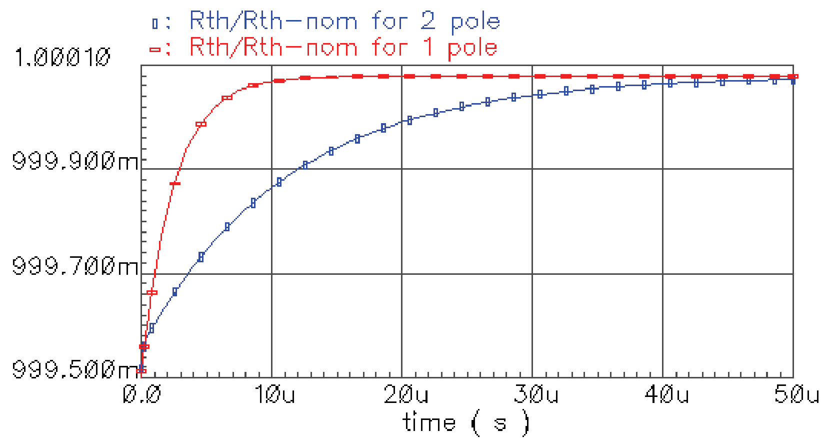
Figure 3.3 A 3 pole thermal model (Fig. a) and its thermal time constants (Fig. b).

It can be observed in (3.3) that, at t = 0, R_{th} = 0 and at t = ∞, $R_{th} = R_1+R_2+R_3$. This idea can be simulated in cadence by using the 6 terminal bipolar model shown in Fig. 2.2. The poles are added externally with the 'dt' node. First, deactivate the internal R_{th}, C_{th} network by adding $-R_{th}$, $-C_{th}$ network externally. The corresponding circuit

diagram and simulations for two pole thermal network are illustrated in Fig. 3.4. In the simulation result $R_{th\text{-}simulated}/R_{th\text{-}nominal}$ is plotted against time.



(a)



(b)

Figure 3.4 Circuit and simulation of thermal time constants for a 2 pole thermal resistance model. (dt/P_{th} (=R_{th}) versus time plot). $R_{th\text{-}simulated}$ is normalized with the default R_{th}.

A procedure can be established to make excellent estimates of the values of each of these components [5] and [20]. The resistance component R_{dist} in (3.1) and Figs.

3.1 and 3.2 is modulated by adjacent devices. The value of this resistance depends upon the number of adjacent devices, amount of epitexial depth, isolation depth, tub perimeter, healing length etc.

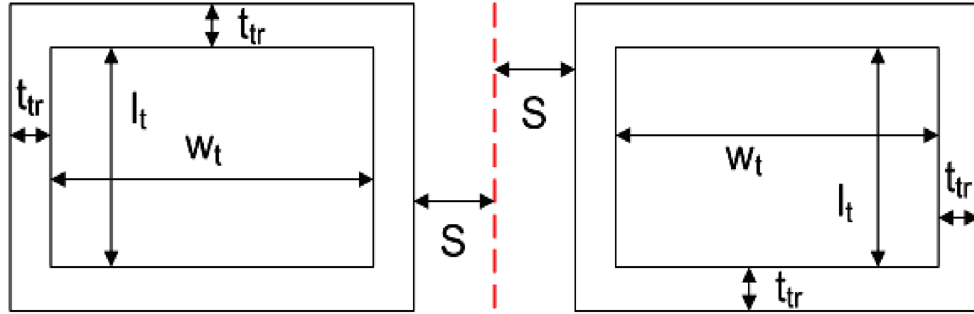


Figure 3.5 Two adjacent devices side by side.

A cross section view of two adjacent devices side by side with a separation 2s is shown in Fig. 3.5. Now, for a device area with trench, $A_{device} = (l_t+2t_{tr})(w_t+2t_{tr})$ in an assembly of devices with inter-device separation, 2s, the fraction of the area useful for heat flow, f(s), and the ratio, r, of device area to total epi area used per device are:

$$f(s) = 1 - r \tag{3.4}$$

$$r = \frac{(l_t + 2t_{tr})(w_t + 2t_{tr})}{(l_t + 2t_{tr} + s)(w_t + 2t_{tr} + s)} \tag{3.5}$$

where l_t and w_t are the inner tub dimensions and t_{tr} is the trench oxide thickness.

The value of R_{distr} can be evaluated as [5]

$$R_{distr} = \frac{1}{2\pi k_{Si} t_{epi} (r_o / r_H + 1)} \propto \frac{C}{f(s)} \tag{3.6.1}$$

where k_{si} is a function of s due to an adjacent device and r_o and r_H are the perimeters of the tub and healing length respectively. C is a constant and t_{epi} is the epitexial depth. The r_o and r_H are defined as [5],

$$r_o = \frac{2(l_t + w_t) + 8t_{tr}}{2\pi} \tag{3.6.2}$$

$$r_H = \sqrt{\frac{k_{Si} t_{epi} t_{ISO}}{k_{Ox}}} \tag{3.6.3}$$

where, k_{si} and k_{ox} are the silicon and oxide thermal conductivity respectively, t_{ISO} is the isolation oxide thickness.

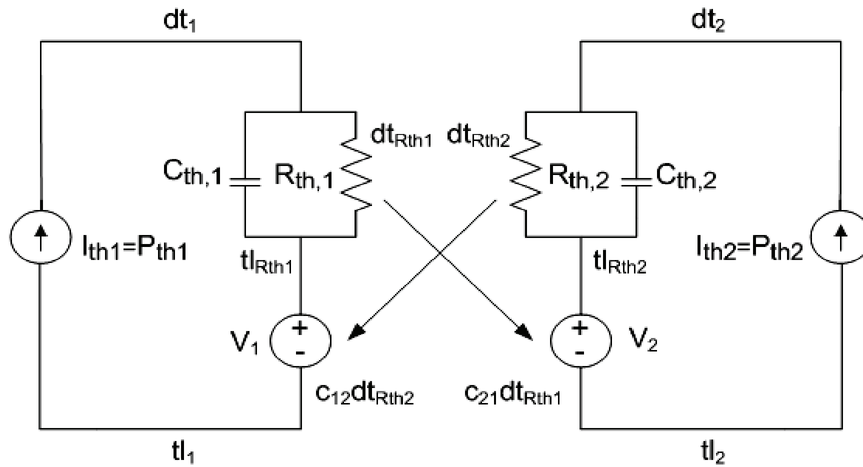


Figure 3.6 VCVS thermal coupling model.

The effect of heating on an adjacent device can be represented in a circuit simulator in the manner shown in Fig. 3.6. A fraction (c_{ij}) of the portion of the temperature increase due to heat generated in the R_{th}, C_{th} dissipation region i is represented as a voltage dependent voltage source in series with the temperature increase in region j. In general, there is a phase shift due to delay of heat diffusion from i to j in addition to reduction in magnitude. As a consequence, c_{ij} is complex with a

magnitude less than 1. In Fig. 3.6, ‘tl’ is the local temperature node and ‘dt’ is the temperature rise node. The voltage V_1 and V_2 correspond to $c_{12}dT_2$ and $c_{21}dT_1$ respectively.

3.3 Measurement of Thermal Resistance

The thermal coupling or adjacent device heating depends on the i) number of adjacent devices, ii) spacing between the devices, iii) nature of shared wall, iv) device dimensions, and v) operating conditions of the adjacent devices [22]. To consider the effect of all these parameters on thermal coupling of DIBJTs various test structures were developed, where all the adjacent devices are the same. The test structures were fabricated and measured. The measured test structure is shown in Fig. 3.7, in which one central device (device under test, DUT) is surrounded by eight adjacent devices. All of the nine devices are dielectrically isolated bipolar junction transistors with the same sizes. Separation between the two devices is S in all sides. One or more of the outer devices may be connected as an active or dummy depending on the test measurement. A dummy device has no collector and base current.

The measurement is done in two parts, i) measurement of thermal resistance (R_{th}) for self-heating, and ii) measurement of thermal resistance ($R_{th\text{-}coupling}$) for adjacent device heating. Hence, all the adjacent devices are made dummy except the central device is ON during the self-heating thermal resistance measurement and all the adjacent transistors are made active during the adjacent device thermal measurement, while the center device used for the temperature measurement.

The temperature of a device is evaluated from the forward Gummel data using equation 3.7.

$$T = \frac{q}{Nk} \frac{\partial V_{be}}{\partial \ln I_c} \quad (3.7)$$

The HP4142B Modular DC Source/Monitor and ICCAP interfaced evaluation system are used for the measurements.

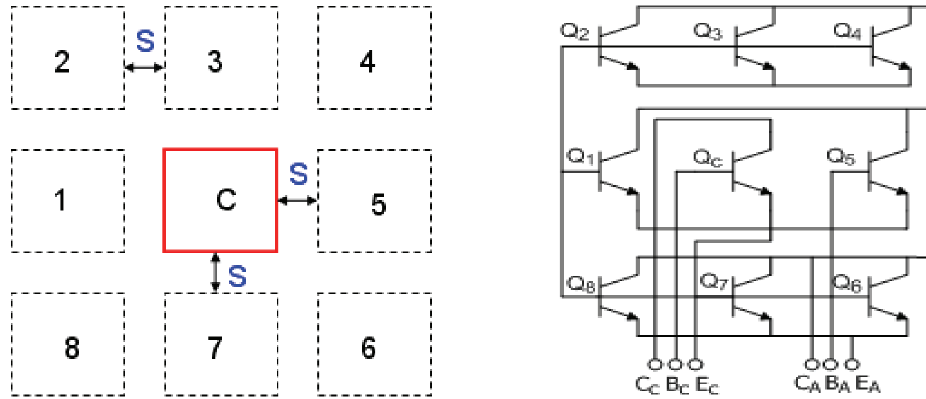


Figure 3.7 Thermal coupling measurement test structure of multiple device (1X: 8X) integrated circuit (S = 2 µm, 4 µm, 8 µm). A device C is at position “C”, the adjacent devices 1 to 8 are at positions “1” to “8”. All the devices are npn 8x5x1 from P10 process.

3.3.1 Measurement of Thermal Resistance (R_{th}) for Self-Heating

To measure the thermal resistance of the central device (DIBJT), a direct extraction technique is employed using collector current (I_c) versus collector emitter voltage (V_{ce}) curves at different temperatures [15]. In Fig. 3.8, the VBIC device shows the characteristics of increasing slopes in I_c-V_{ce} plots for a constant base emitter voltage. It can be easily found from these plots that at each temperature there is a bias point in

each plot where a constant collector current can be measured. At each of these bias points collector currents and base emitter voltages are constant.

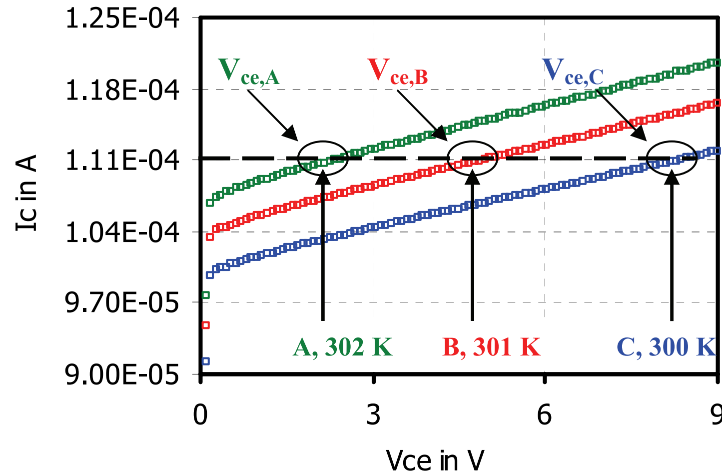


Figure 3.8 Measurement of I_c versus V_{ce} at different temperatures.

Simulation and experimental examination found the constant base current and therefore the current gain. Thus, the average junction temperature is obviously the same at those bias points [15]. Thermal resistance is assumed constant with respect to the minimal temperature change.

The junction temperature can be expressed as

$$T_j = T_{ambient} + R_{th} P_{th} \quad (3.8)$$

$$T_{jA} = T_A + R_{th} P_A \quad (3.9)$$

$$T_{jB} = T_B + R_{th} P_B \quad (3.10)$$

$$T_{jC} = T_C + R_{th} P_C \quad (3.11)$$

where T_A, T_B, and T_C are the ambient temperatures while P_A, P_B, and P_C are the thermal

powers at the bias points A, B, and C. A, B, and C bias points are at the temperatures 302ºK, 301ºK, and 300ºK respectively.

The thermal power can be computed as

$$P_{th} = V_{be} \times I_b + V_{ce} \times I_c \tag{3.12}$$

When the junction temperatures are equal at each bias point, then (3.9) and (3.10) can be solved for the thermal resistance.

$$R_{th} = \frac{T_B - T_A}{P_A - P_B} \tag{3.13.1}$$

When thermal resistance is considered as a function of temperature, then the temperature dependent R_{th} needs to be used in (3.9) – (3.11). In that case the expression for the R_{th} would be changed as well.

The junction temperature can also be evaluated by solving (3.9) – (3.11) [15]. The junction temperature can be expressed as

$$Tj = T_B + \Delta T \left\{ \left(\frac{P_B}{P_A} - \frac{P_B}{P_C} \right) \Big/ \left(\frac{P_B}{P_A} + \frac{P_B}{P_C} - 2 \right) \right\} \tag{3.13.2}$$

3.3.2 Measurement of Thermal Resistance ($R_{th\text{-}coupling}$) for Adjacent Device Heating

Consider the test structure in Fig. 3.7. The distances between the central device and the outer devices are varied as 2 μm, 4 μm and 8 μm. The adjacent outer devices are connected in parallel and are powered up at various power levels with constant base emitter voltage. The temperature of the central device is then measured. The dissipated power of the outer devices can be computed by using (3.12). A set of plots showing the change in apparent temperature of the central device with increasing power on the outer

devices are plotted after measurement. These are presented in the following sections. In this case, the thermal coupling resistance can best be defined as the rate of change of the temperature of the center device with respect to the change of power at the outer devices. This is expressed in (3.14)

$$\frac{dT_i}{dP_j} = R_{th-coupling} \tag{3.14}$$

where T_i is the temperature of the central device and P_j is the power of the outer devices.

The parameter c_{ij} in Fig. 3.6 can now be evaluated as follows.

$$\begin{aligned}
&R_{th-coupling} = \frac{dT_i}{dP_j} \\
&dT_i = R_{th-coupling}\, dP_j \\
&c_{ij}\, dT_{Rth2} = c_{ij} R_{th,j} P_j = dT_i \\
&\Rightarrow c_{ij} = \frac{R_{th-coupling}}{R_{th,j}}
\end{aligned} \tag{3.15}$$

where, $R_{th,j}$ is the nominal model parameter value of the thermal resistance.

The measurement result for the 2 μm spacings in the test structure is shown in Fig. 3.9. The $R_{th-coupling}$ can be evaluated using (3.14). The slope of the trend line indicates the thermal coupling resistance of the central device due to the adjacent device heating effect. It can be normalized with respect to the self heating thermal resistance. This is done in percentage with respect to the R_{th} nominal value using (3.15). This is written as,

$$R_{th\text{ - coupling}} = \frac{dT_i}{dP_j} = c_{ij} R_{th,j} P_j = 72.4 \, {}^{C}\!/\!{}_{W}$$

$$\Rightarrow c_{ij} = 8.04\%$$

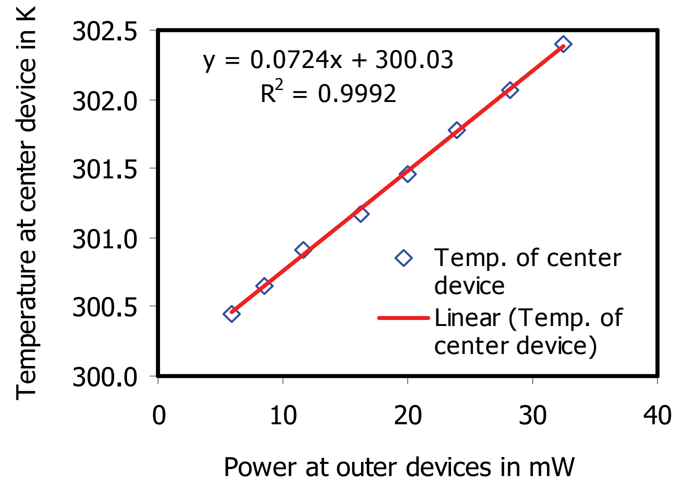


Figure 3.9 Temperature of central device versus power on outer devices (S = 2 µm in Fig. 3.7).

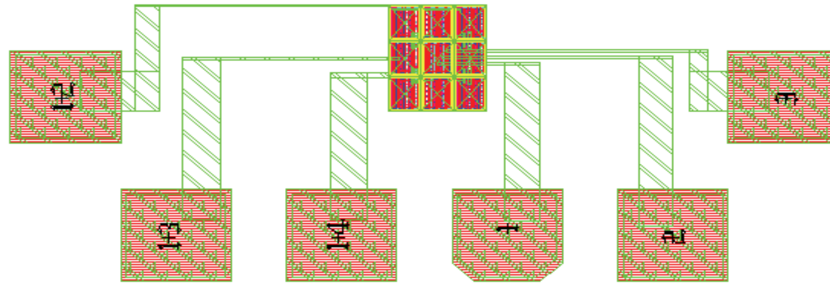


Figure 3.10 Layout of the Adjacent Device Test Structure (Fig. 3.7) for S = 4 µm.

The measurement result for the 4 µm spacings in the test structure is shown in Fig. 3.11. The $R_{th\text{-coupling}}$ can be evaluated using (3.14). The slope of the trend line indicates the thermal coupling resistance of the central device due to the adjacent device heating effect. It can be normalized with respect to the self heating thermal resistance.

This is done in percentage with respect to the R_{th} nominal value using (3.15). This is written as,

$$R_{th\text{ - coupling}} = \frac{dT_i}{dP_j} = c_{ij} R_{th,j} P_j = 59.6 \, C/W$$

$$\Rightarrow c_{ij} = 6.62\%$$

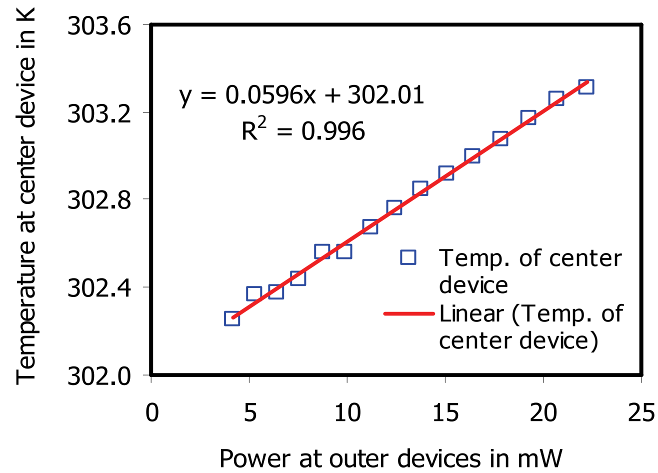


Figure 3.11 Temperature of central device versus power on outer devices (S = 4 μm in Fig. 3.7).

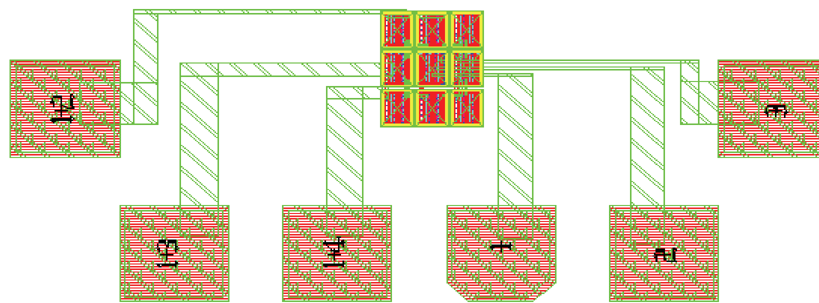


Figure 3.12 Layout of the Adjacent Device Test Structure (Fig. 3.7) for S = 4 μm.

The measurement result for the 8 μm spacings in the test structure is shown in Fig. 3.13. The $R_{th\text{-coupling}}$ can be evaluated using (3.14). The slope of the trend line

indicates the thermal coupling resistance of the central device due to the adjacent device heating effect. It can be normalized with respect to the self heating thermal resistance. This is done in percentage with respect to the R_{th} nominal value using (3.15). This is written as,

$$R_{th\text{ - coupling}} = \frac{dT_i}{dP_j} = c_{ij} R_{th,j} P_j = 26.3\, {}^{C}\!/_{W}$$

$$\Rightarrow c_{ij} = 2.92\%$$

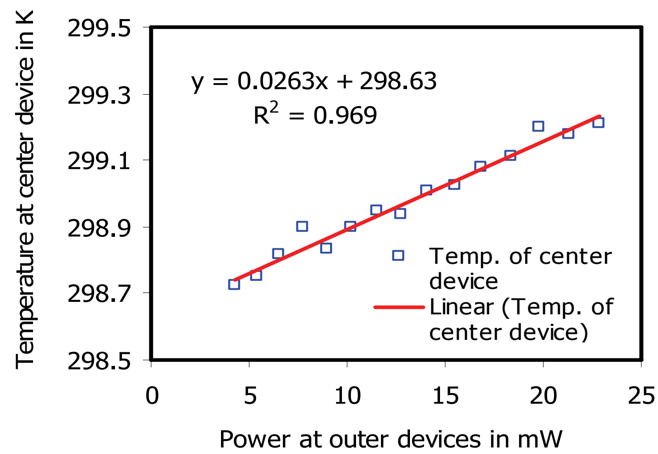


Figure 3.13 Temperature of central device versus power on outer devices (S = 8 μm in Fig. 3.7).

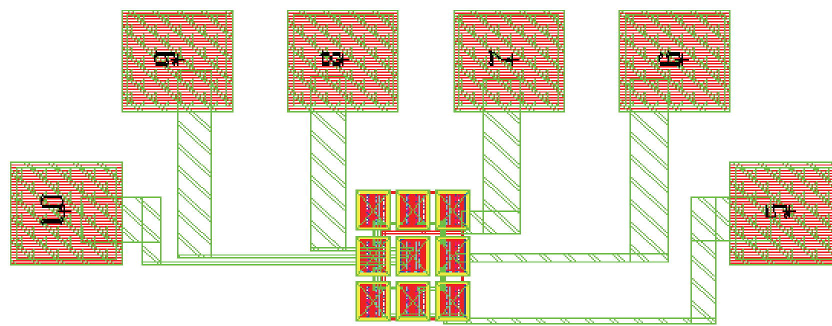


Figure 3.14 Layout of the Adjacent Device Test Structure (Fig. 3.7) for S = 8 μm.

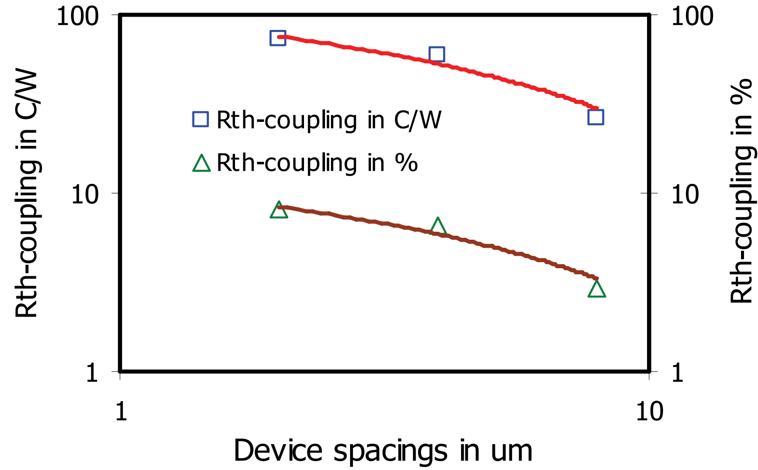


Figure 3.15 Adjacent device coupling space-dependence result.

3.3.3 Overall Measurement Result of the Adjacent Device Heating Effect for the Test Structure

Table 3.1 Overall Results of the Thermal Coupling Measurement

Spacing S	$R_{th\text{-}coupling}$	c_{ij}
μm	C/W	%
2	72.4	8.04
4	59.6	6.62
8	26.3	2.92

The overall measurement results for the $R_{th\text{-}coupling}$ are shown in Fig. 3.15 and Table 3.1. The central device and the outer devices are spaced by 2 μm, 4 μm and 8 μm. The Fig. 3.15 represents the thermal coupling with respect to the space variation among the adjacent devices. This shows decreasing logarithmic characteristics with spacing. The equation (3.6.1) shows the inversely proportional distance characteristics for the

R_{dist}, which is equivalent to $R_{th\text{-}coupling}$. This characteristic has been seen in the measurement as well (Fig. 3.15).

3.4 Conclusion

A new technique for modeling and characterizing of thermal coupling effect is illustrated. The developed compact thermal model for the adjacent device heating provides inclusion of all thermal effects successfully as the sides of the devices are isolated by insulator. Measurement data support the conclusion that the model topology is correct. A macro can be developed to couple to the standard device model to fully incorporate the compact model on the schematic page of the simulator. The VBIC model can be used successfully to improve thermal tail behavior. This research gives an idea how to continue the characterization of coupling coefficients for adjacent device effects for varied spacing. Furthermore it refines the procedures for determining critical points in circuit topologies with regard to thermal effects. This will evaluate the effectiveness of variation in device and circuit layout in reducing thermal effects and coupling.

CHAPTER 4

FREQUENCY DEPENDENT THERMAL EFFECT MODELING AND CHARACTERIZATION

Frequency dependent thermal characterization is very important to understand the thermal behavior of analog circuit characteristics in the frequency domain. The Y (admittance) parameters are significantly affected by the self-heating effect [1], [2], and [24]. The Y parameters can be used to describe the self-heating effect in a transistor [1], [2], [16], and [17] in the frequency domain. The Y_{22} parameter is the most sensitive to self-heating [1] and [2]. R_{th} can be extracted from Y_{22} [2] and the thermal time constant can also be estimated from the Y_{22} versus frequency plot.

4.1 Electro-Thermal Model and Its Small Signal Diagram

The electro thermal model or network for a VBIC self-heating bipolar device is shown in Fig. 4.1 [2], [16], and [17]. P_{th} is the thermal power and can be found as

$$P_{th} = V_{be} \times I_b + V_{ce} \times I_c \quad (4.1)$$

The thermal admittance and impedance Y_{th} and Z_{th} are expressed as,

$$Y_{th} = 1/R_{th} + j\omega C_{th} \quad (4.2)$$

$$Z_{th} = 1/Y_{th} \quad (4.3)$$

where, R_{th} and C_{th} are the thermal resistance and capacitance respectively. $|Y_{th}|$ increases as frequency increases. Thus, it can be concluded by observing (4.2) and (4.3)

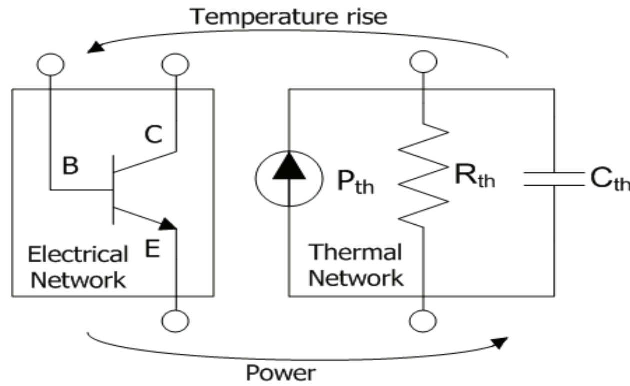


Figure 4.1 Electro thermal network.

that, at high frequencies the thermal impedance is shorted out and has no impact or very little impact on the circuit performance. In reality the device thermal response can not follow the applied electrical bias at high frequency [2], [16], and [17]. It is also found in (4.2) and (4.3) that, at low frequency the thermal impedance is not zero and the device characteristics (temperature) can be changed with the electrical signal.

A five terminal bipolar model including the local temperature (tl), the small signal temperature rise (dt_s) and the substrate nodes is shown in Fig. 4.2 (referred from Fig 2.2).

Now, the temperature rise due to self-heating can be computed as,

$$\left(T_j - T_{ambient}\right) = R_{th} P_{th} \tag{4.4}$$

where, (T_j–$T_{ambient}$) is the temperature rise due to the self-heating. The junction temperature, T_j can be evaluated by the method shown in [15].

The temperature change in a device with thermal resistance 2000 C/W for 1 mW of thermal power is

dt = 2000 C/W ·1mW = 2 ºC

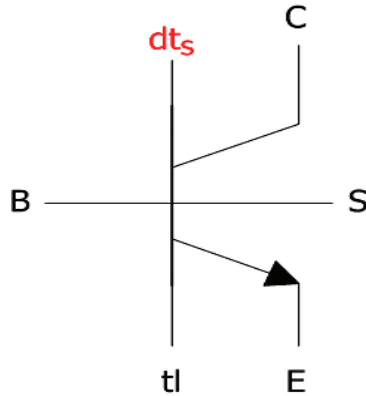


Figure 4.2 A bipolar transistor model including local temperature (tl), small signal temperature rise (dt_s) and substrate (S) nodes.

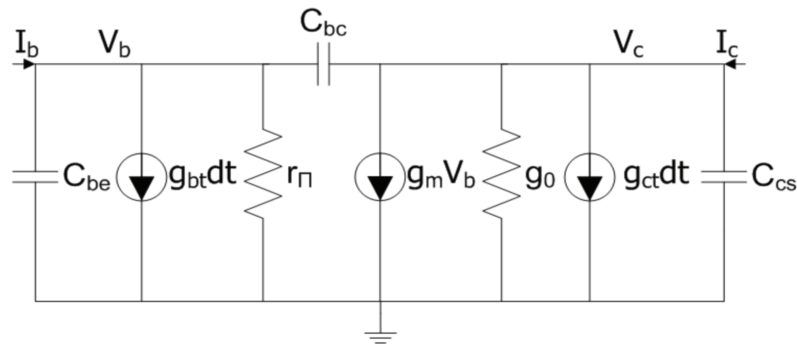


Figure 4.3 Small signal diagram of the electro thermal network in Fig. 4.1.

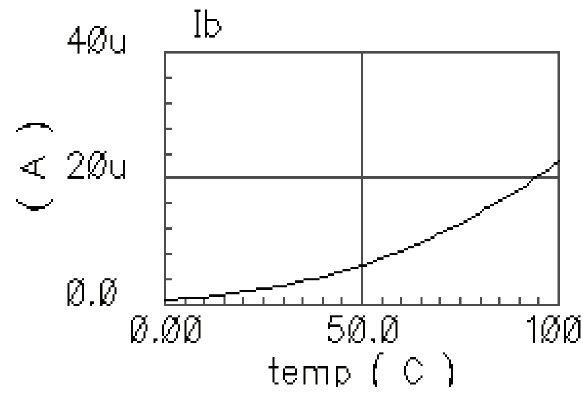
The small signal diagram of the corresponding thermal model is shown in Fig. 4.3 [2], [6], [16], and [17]. The base and the collector currents and voltages are I_b, V_b and I_c, V_c respectively. The capacitances C_{be}, C_{bc} and C_{cs} are the base-emitter, base-collector and collector-substrate capacitances. The ideal output conductance is notated by g_o ($g_o = dI_c/dV_c$). Therefore, the ideal effective output resistance,

$$R_{out} = 1/go \tag{4.5}$$

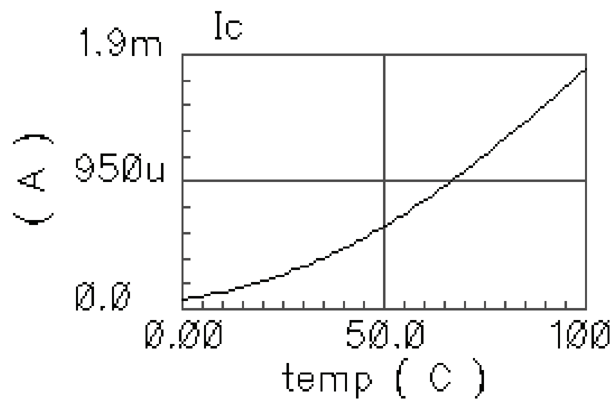
The g_{ct} and g_{bt} are the thermal transconductances at the collector and base of a transistor. They can be measured or calculated by differentiating the base current and the collector current with respect to the temperature [2], [16], and [17]. Thus, the expressions for the g_{ct} and g_{bt} are given by,

$$g_{bt} = \frac{\partial I_b}{\partial T} \tag{4.6}$$

$$g_{ct} = \frac{\partial I_c}{\partial T} \tag{4.7}$$



(a)



(b)

Figure 4.4 The simulations of I_c and I_b versus temperature for a single transistor network.

Thus, $g_{bt}.dt_s$ and $g_{ct}.dt_s$ are the small signal currents at the base and the collector due the self-heating effect [2]. The simulations of the collector and base currents with respect to the temperature can find the thermal transconductances. The simulation results are plotted in Fig. 4.4. The g_{ct} and g_{bt} are plotted (in ICCAP) in Figs. 2.6 and 2.8 as well.

The small signal AC currents at the base and collector terminals in Fig. 4.3 can be written as [2],

$$i_b = \{g_\pi + j\omega(C_{be} + C_{bc})\} v_b - j\omega C_{bc} v_c + g_{bt}\, dt_s \tag{4.8}$$

$$i_c = (g_m - j\omega C_{bc}) v_b + \{g_o + j\omega(C_{bc} + C_{cs})\} v_c + g_{ct}\, dt_s \tag{4.9}$$

The dt_s is the small signal temperature increment for the self-heating effect. The v_c and v_b are the small signal AC voltages at the base and collector. The dt_s can be found by applying the through variable conservation law at the local temperature node [2]. According to the through variable conservation law in a small signal electro thermal diagram, the thermal power at the thermal network is equivalent to the summation of all the powers at the electrical network. Therefore, the product of the small signal temperature and the thermal admittance is given by [2]

$$Y_{th}\, dt_s = (I_c + g_o V_c) v_c + (I_b + g_\pi V_b + g_m V_c) v_b + (g_{ct} V_c + g_{bt} V_b) dt_s \tag{4.10}$$

Now, the small signal temperature rise dt_s can be solved from (4.10)

$$dt_s = \frac{(I_c + g_o V_c) v_c + (I_b + g_\pi V_b + g_m V_c) v_b}{Y_{th} - (g_{ct} V_c + g_{bt} V_b)} \tag{4.11}$$

4.2 The Y Parameters

A symbolic two port network and its Y parameter model showing the input base port and the output collector port is shown in Fig. 4.5. It includes AC voltages and currents (v_b, i_b and v_c, i_c), DC voltages and currents (V_{be}, I_c and V_{ce}, I_b) and the power supplies V_{cc} and V_{ee}.

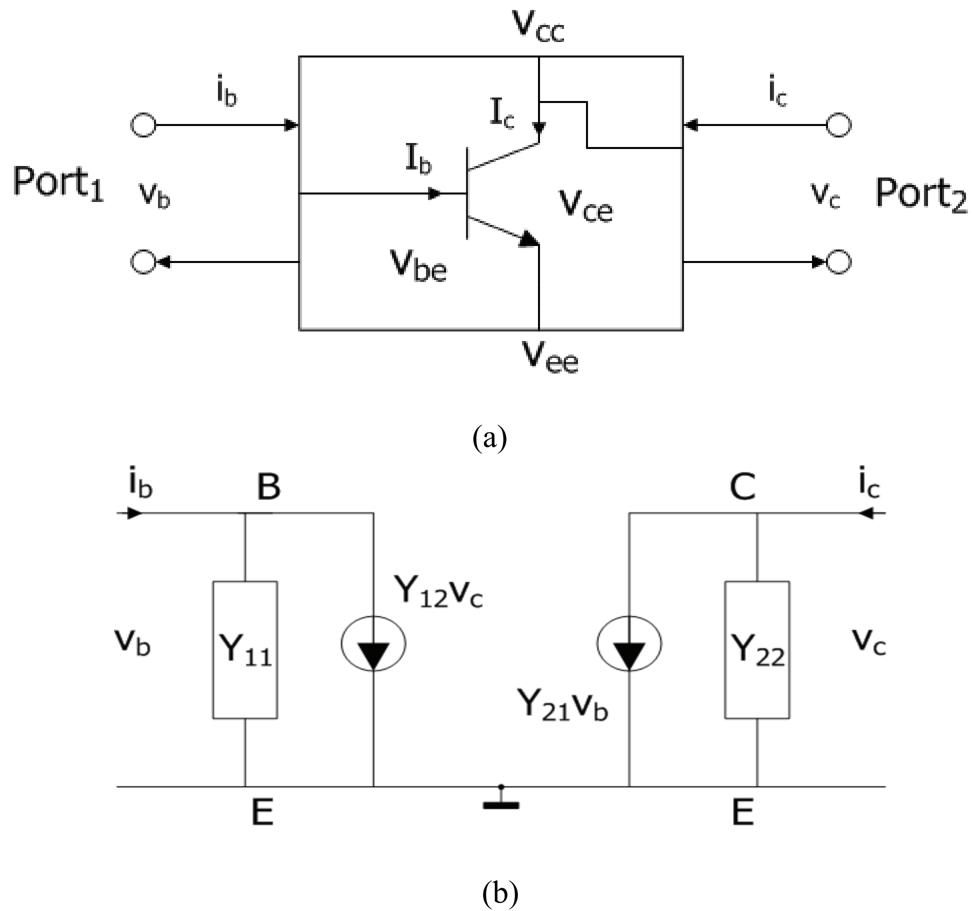


Figure 4.5 (a) A two port network with a bipolar device including all (AC and DC) the voltage and current components, (b) Common-emitter Y parameter model.

By combining the frequency dependent small signal analysis for the electro thermal model in (4.8), (4.9) and (4.11) and the definition of the Y parameters for a 2

port network as shown in Fig. 4.5 (b), the four parameters Y_{11}, Y_{12}, Y_{21} and Y_{22} can be defined and evaluated as [2]

$$Y_{11} = \left.\frac{i_b}{v_b}\right|_{V_c=0} = g_\pi + \frac{g_{bt}(I_b + g_\pi V_b + g_m V_c)}{Y_{th} - (g_{ct}V_c + g_{bt}V_b)} + j\omega(C_{be} + C_{bc}) \tag{4.12}$$

$$Y_{12} = \left.\frac{i_b}{v_c}\right|_{v_b=0} = \frac{g_{bt}(I_c + g_o V_c)}{Y_{th} - (g_{ct}V_c + g_{bt}V_b)} - j\omega C_{bc} \tag{4.13}$$

$$Y_{21} = \left.\frac{i_c}{v_b}\right|_{v_c=0} = g_m + \frac{g_{ct}(I_b + g_\pi V_b + g_m V_c)}{Y_{th} - (g_{ct}V_c + g_{bt}V_b)} - j\omega C_{bc} \tag{4.14}$$

$$Y_{22} = \left.\frac{i_c}{v_c}\right|_{v_b=0} = g_o + \frac{g_{ct}(I_c + g_o V_c)}{Y_{th} - (g_{ct}V_c + g_{bt}V_b)} + j\omega(C_{bc} + C_{cs}) \tag{4.15}$$

Among all the Y parameters Y_{22} is found to be significantly affected by the thermal effect [2], [16], and [17]. The self-heating also causes a considerable change of Y_{12} with respect to frequency and a moderate change with frequency of Y_{11} and Y_{21} [2]. There are several ways to see the self-heating effect on these Y parameters in simulation or measurement. However, to see the simulated and measured data, a balanced resistively loaded differential amplifier is designed, simulated, fabricated and measured.

4.3 Design and Thermal Simulations of the Balanced Differential Amplifier

4.3.1 Design of the Balanced Differential Amplifier

The balanced differential amplifier shown in Fig. 4.6 is designed to simulate and measure the Y parameters. The input transistors Q_1 and Q_2 are biased with the current mirror comprised of Q_3 and Q_4. The resistances R_1 and R_2 work as differential loads. They are 1kΩ each. The bias resistance R_3 is used to vary the circuit current. The circuit operates with ± 3V power supply.

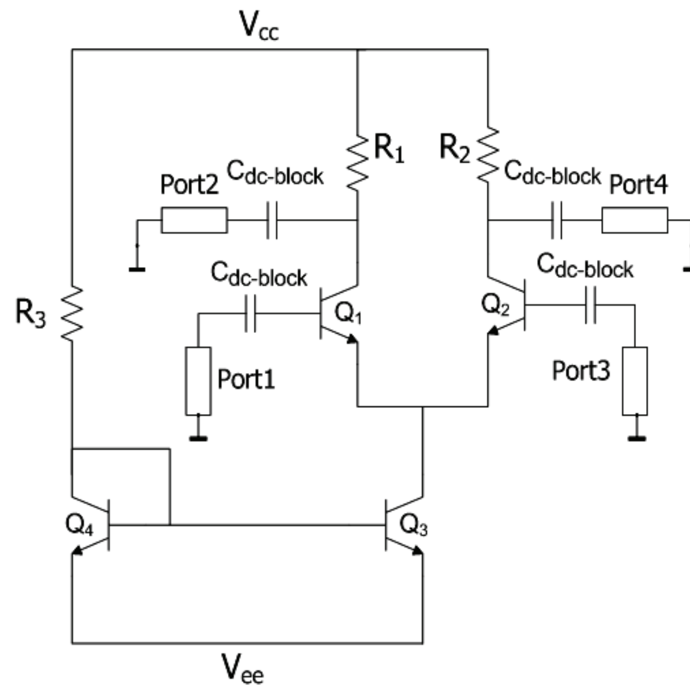


Figure 4.6 A four port network showing the input base ports and the output collector ports.

4.3.2 Thermal Simulations of the Y Parameters

The Y parameters versus frequency are plotted from the S parameter simulations. This can be done with the AC analysis as well. These analyses initially calculate a DC operating point and then linearize the devices about the operating point values. The device needs to be operated in the forward active region.

4.3.2.1 S parameter to Y Parameter Conversion

The S parameter simulation is universal for the frequency domain analysis. But the S parameters can be converted to the Y parameters by using the formulas illustrated below. For a two port network as shown in Fig. 4.5, the conversion formulas are given by

s-parameters in terms of y-parameters	y-parameters in terms of s-parameters
$s_{11} = \frac{(1-y_{11})(1+y_{22})+y_{12}y_{21}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}}$	$y_{11} = \frac{(1+s_{22})(1-s_{11})+s_{12}s_{21}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}}$
$s_{12} = \frac{-2y_{12}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}}$	$y_{12} = \frac{-2s_{12}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}}$
$s_{21} = \frac{-2y_{21}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}}$	$y_{21} = \frac{-2s_{21}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}}$
$s_{22} = \frac{(1+y_{11})(1-y_{22})+y_{12}y_{21}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}}$	$y_{22} = \frac{(1+s_{11})(1-s_{22})+s_{12}s_{21}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}}$

Figure 4.7 S – Y parameter conversion table [25].

4.3.2.2 Simulation of the Y Parameters

The four ports shown in Fig. 4.6 are the S parameters ports. To block the DC the output ports are connected to the AC signal through a capacitor. The capacitor works as a short circuit for the AC signal.

The required capacitance value of the dc blocking capacitor at the ports can be calculated by the following formula. The 10 mS is equivalent to 1/0.1 Ω. The right hand side of (4.16) can be any value that makes a very low resistance path (ideally) for the respective AC signal.

$$2\pi f_{min} C_{block} >> 10 \text{ mS} \quad (4.16)$$

The Spectre S parameter simulation provides the S parameters which are then converted to Y parameters. Several different kinds of simulations have been done. The simulations for a 4 port network (Fig. 4.6) are shown in Fig. 4.8 to Fig.4.12. Only the Y_{22} simulation is shown for a bigger device. The inter-port simulations (Fig. 4.12) Y_{41} and Y_{23} shows the self-heating effect as well. As seen in (4.2), Y_{th} increases with frequency. Thus, the Y parameters in (4.12) – (4.15) should decrease with the frequency until the thermal effects become insignificant. After the thermal effect becomes insignificant, the device capacitance dictates the Y parameters behavior.

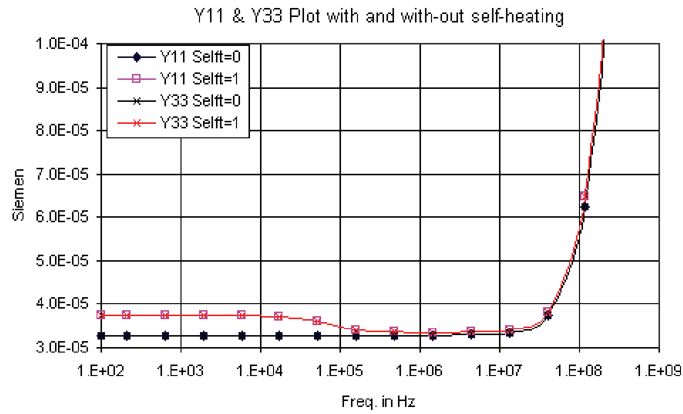


Figure 4.8 Y_{11} and Y_{33} versus frequency with and without self-heating.

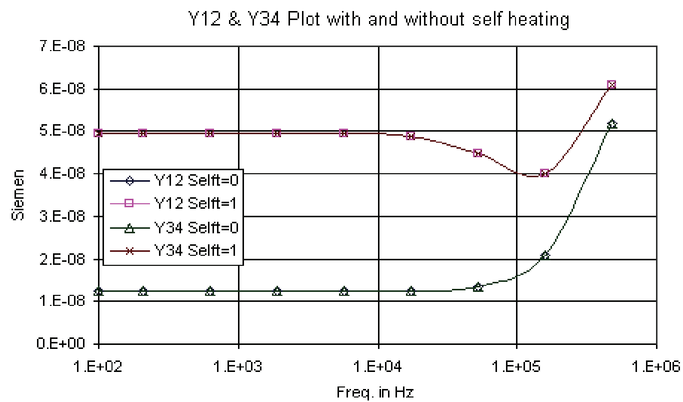


Figure 4.9 Y_{12} and Y_{34} versus frequency with and without self-heating.

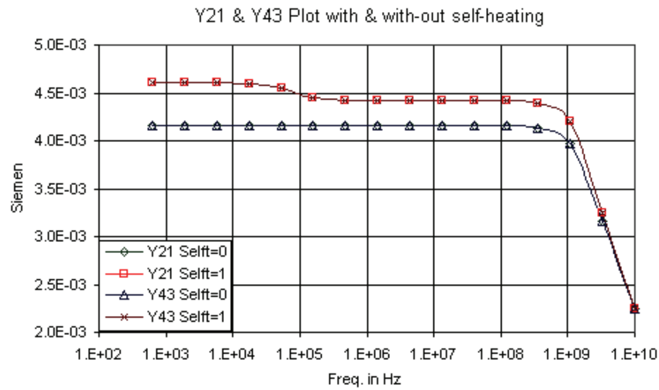


Figure 4.10 Y_{21} and Y_{43} versus frequency with and without self-heating.

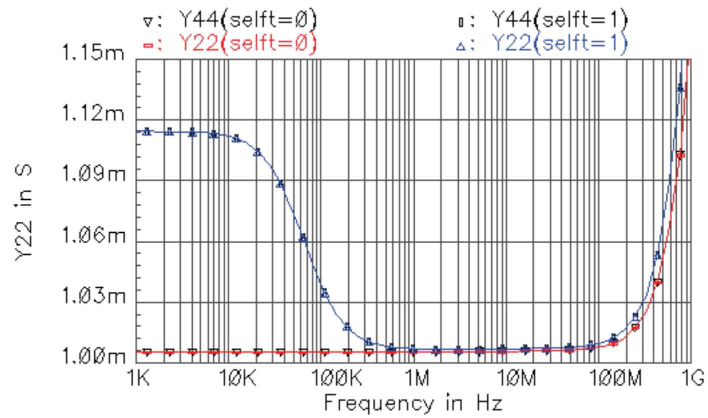


Figure 4.11 Y_{22} and Y_{44} versus frequency with and without self-heating.

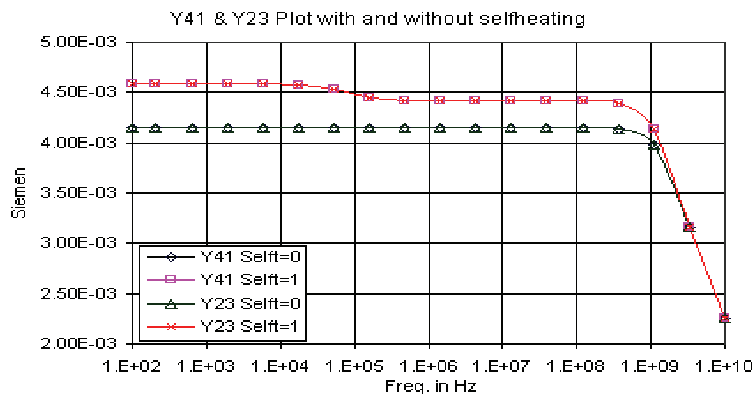


Figure 4.12 Y_{41} and Y_{23} versus frequency with and without self-heating.

4.4 The Y_{22} Parameter

As described earlier, the thermal response cannot follow the high frequency circuit response. Thus at high frequency the output admittance (Y_{22}) is merely the electrical admittance. This can be seen in (4.15). But at low frequency the effective output admittance (Y_{22}) differs from the electrical conductance due to the thermal effect. The thermal behavior of Y_{22} is affected by the bias points, saturation current, and device geometry.

4.4.1 Y_{22} Simulation with Variable Thermal Resistance in the Frequency Domain

The simulations of Y_{22} versus frequency with different R_{th} values are shown in Fig. 4.13. The thermal resistance changes the low frequency magnitudes of the Y_{22} parameter. The higher thermal resistance shows more effect on the Y_{22}. In this simulation, the thermal capacitance is kept constant at its default value.

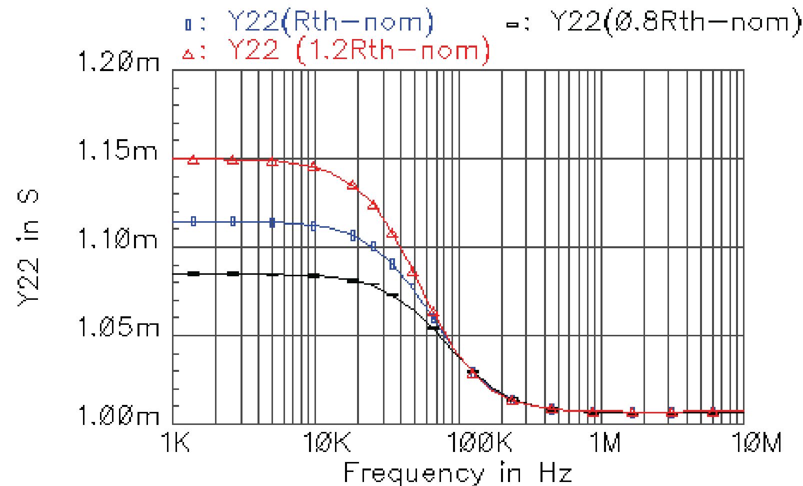


Figure 4.13 Y_{22} versus frequency with different R_{th} values.

4.4.2 Y_{22} Simulation with Variable Thermal Capacitance in the Frequency Domain

The simulations of Y_{22} versus frequency with different C_{th} values are shown in Fig. 4.14.The thermal capacitance moves the low frequency pole. It does not have significant effect on the magnitude of Y_{22}. In this simulation, the thermal resistance is kept constant at its default value.

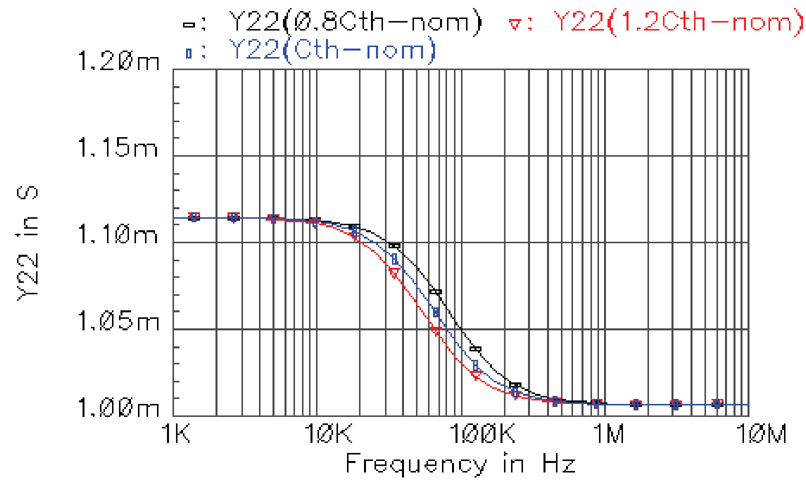


Figure 4.14 Y_{22} versus frequency with different C_{th} values.

4.4.3 Y_{22} Simulation with Variable Thermal Time Constants (variable R_{th} and C_{th}) in the Frequency Domain

The thermal time constant (TC) is defined as the product of the R_{th} and C_{th}. In chapter 3, it was found that multiple thermal TCs are present for the five element thermal resistance in a dielectrically isolated device. Therefore, Y_{22} can be simulated for the multiple thermal TCs. There are three simulations have been done, i) nominal thermal time constant (TC), ii) 1.2 times the nominal thermal time constant, and iii) 0.8

times the nominal thermal time constant. It can be observed that the low frequency pole (corner frequency) of Y_{22} is varied in accordance with the thermal TCs.

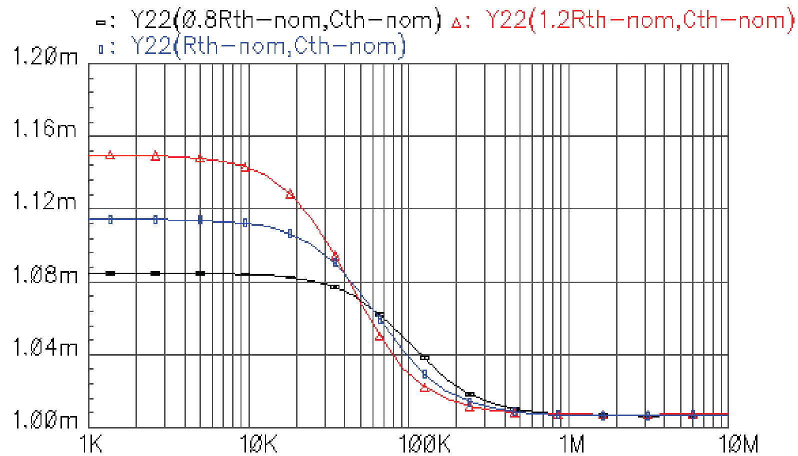


Figure 4.15 Y_{22} versus frequency with different thermal time constants.

4.4.4 Y_{22} Simulation with Variable Bias Current in the Frequency Domain

The expression for Y_{22} in (4.15) shows that, Y_{22} has direct relationship with the collector current. This demonstrates the higher thermal effect for a larger collector current. The plots in Fig. 4.16 show the variation of Y_{22} with respect to the collector current.

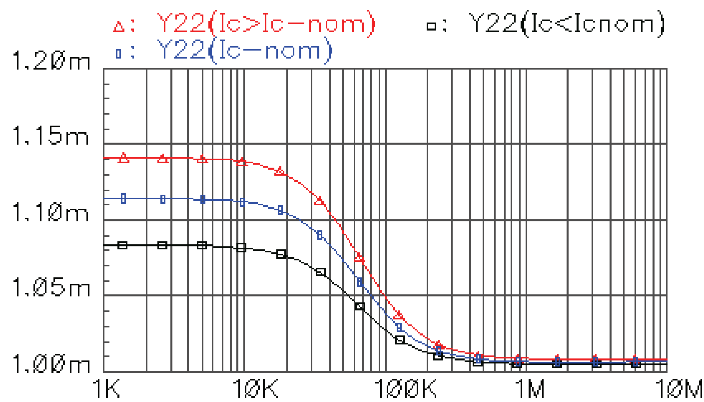


Figure 4.16 Y_{22} versus frequency at different collector currents.

4.5 Thermal Resistance Extraction

4.5.1 Theory

Y_{22} can be used to extract the thermal resistance [2]. Now, Y_{th}, can be evaluated by equations (4.2) and (4.15) as

$$Y_{th} = 1/R_{th} + j\omega C_{th} = \frac{g_{ct}(I_c + g_o V_c)}{Y_{22} - g_o - j\omega(C_{bc} + C_{cs})} + (g_{ct}V_c + g_{bt}V_b) \qquad (4.17)$$

Solving (4.17) for R_{th} gives

$$R_{th} = \frac{Y_{22} - g_o - j\omega(C_{bc} + C_{cs})}{\left[\left\{g_{ct}(I_c + g_o V_c)\right\}\right] + \left[\left\{(g_{ct}V_c + g_{bt}V_b) - j\omega C_{th}\right\}\right]\left[\left\{Y_{22} - g_o - j\omega(C_{bc} + C_{cs})\right\}\right]} \qquad (4.18)$$

Now, R_{th} can be found at dc from (4.18)

$$R_{th} = \frac{Y_{22} - g_o}{\left[\left\{g_{ct}(I_c + g_o V_c)\right\} + \left\{(g_{ct}V_c + g_{bt}V_b)\left(Y_{22} - g_o\right)\right\}\right]} \qquad (4.19)$$

Distributed resistances, which were described as the five element thermal resistance model (chapter 3), give multiple poles in the Y_{22} function. Using the five element thermal resistance model in (3.1), Y_{22} can be revaluated from (4.15)

$$Y_{22} = g_o + \frac{g_{ct}(I_c + g_o V_c)}{\dfrac{1}{\left[R_{tub} + \dfrac{1}{\left(\dfrac{1}{R_{ox} + R_w}\right) + \left(\dfrac{1}{R_{per} + R_{dist}}\right)}\right]} + j\omega C_{th} - (g_{ct}V_c + g_{bt}V_b)} + j\omega(C_{bc} + C_{cs}) \qquad (4.20)$$

where, the five thermal resistance components are, i) R_{tub} for the active region, ii) R_{ox} for the isolation, iii) R_w for the wafer, iv) R_{per} for the peripheral trench oxide, and v) R_{distr} for the inter device and distributed conduction. These are shown in Fig. 3.1.

4.5.2 Layout

The layout of the balanced differential amplifier is shown in Fig. 4.17. There are two similar test designs have been fabricated in the same chip. The current mirror devices (Q_3 and Q_4 in Fig. 4.6) in the differential amplifier are separated far away from the measured devices (Q_1 and Q_2 in Fig. 4.6). So that, the mirror devices does not have any adjacent device heating effect on the Q_1 and Q_2 devices.

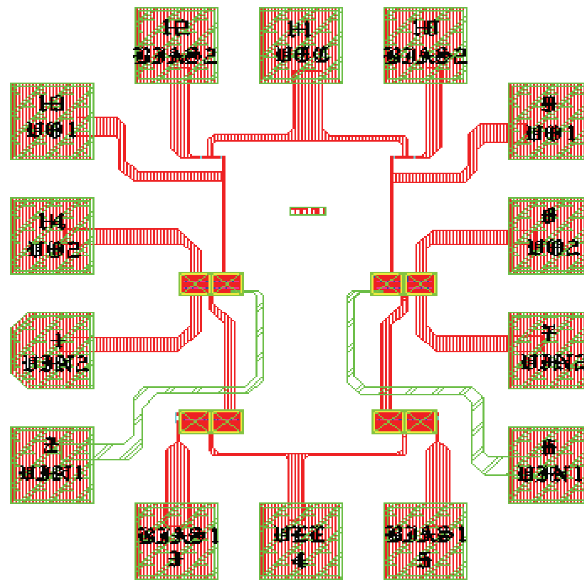


Figure 4.17 The layout of the differential amplifier (UTA214).

4.5.3 Measurement set-up and the Measurement and Simulation Comparison for the Y_{22} parameter

The measurement set-up for the Y_{22} is shown in Fig. 4.18. The S_{22} parameter measurement is done with the HP 4395A network analyzer and Agilent 87511A S-parameter test set. The measurement was done with the one port setup as shown in Fig. 4.18. Before the data is taken, open, short and 50 Ω load calibrations have been completed. The measured S parameter reflection or transmission data is converted to the

equivalent admittance (Y) values. This is not the same as a two-port Y parameter conversion. An S_{11} or S_{22} trace, measured as reflection, can be converted to an equivalent parallel impedance or admittance. The admittance parameter is defined as

$$Y = \frac{1}{Z_0}\frac{(1 - S_{22})}{(1 + S_{22})} \tag{4.21}$$

where, Z_0 is the characteristic impedance.

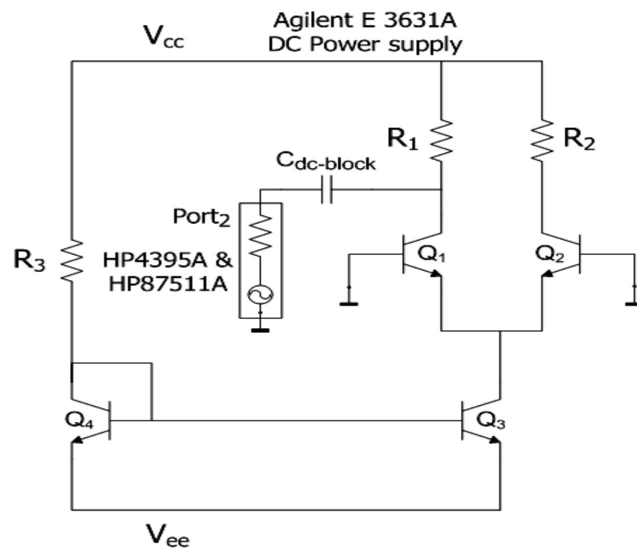


Figure 4.18 Measurement set-up.

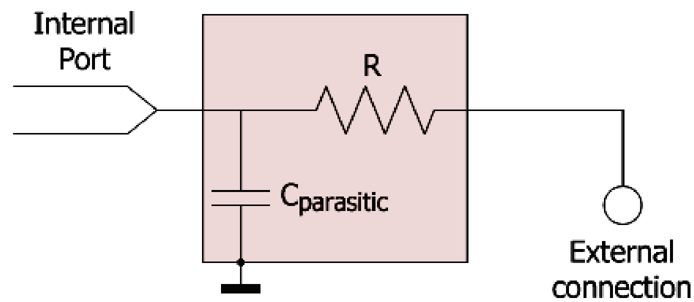


Figure 4.19 The parasitic model that used at each pad.

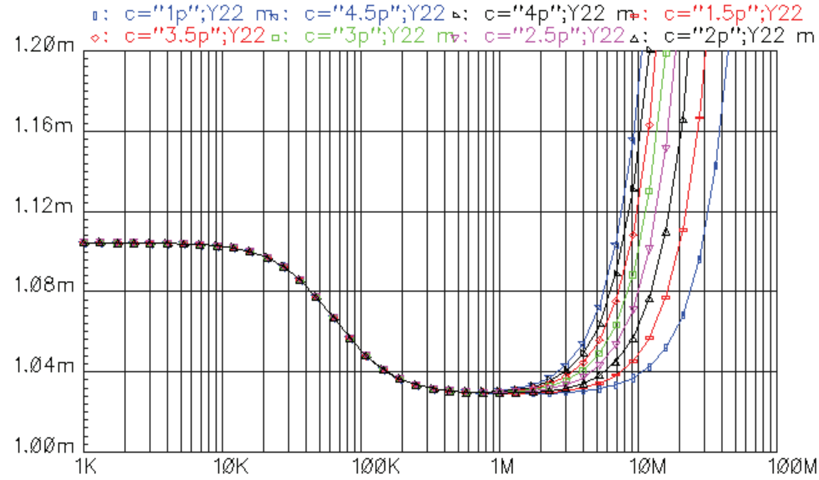


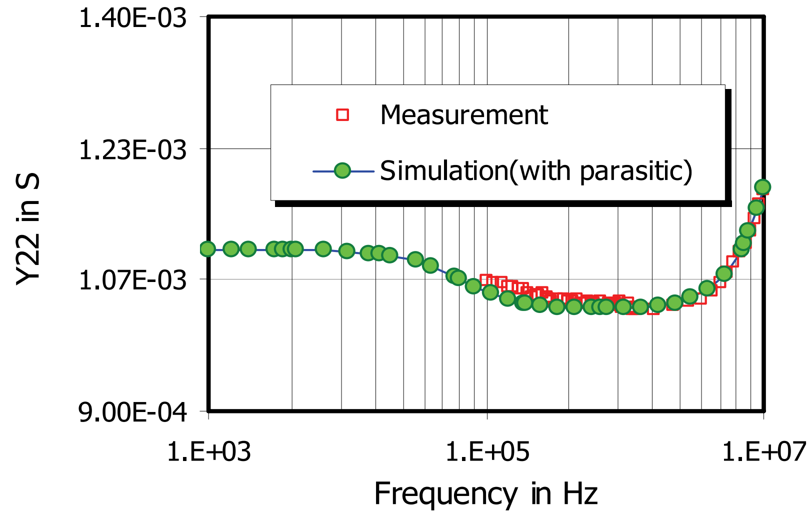
Figure 4.20 The Y_{22} simulation with respect to the parasitic capacitance (Fig. 4.19).

De-embedding is required to get rid of the package, pad, and routing parasitics [26]. This is accomplished in simulation to match the measurement data. A parametric simulation is done by varying $C_{parasitic}$ (Fig. 4.19). By comparing the measured data and simulated results (with parasitic), it is found that, a 4.5 pF parasitic capacitance value matched the simulated and measured data. The expression for the Y_{22} with the parasitic can be written as

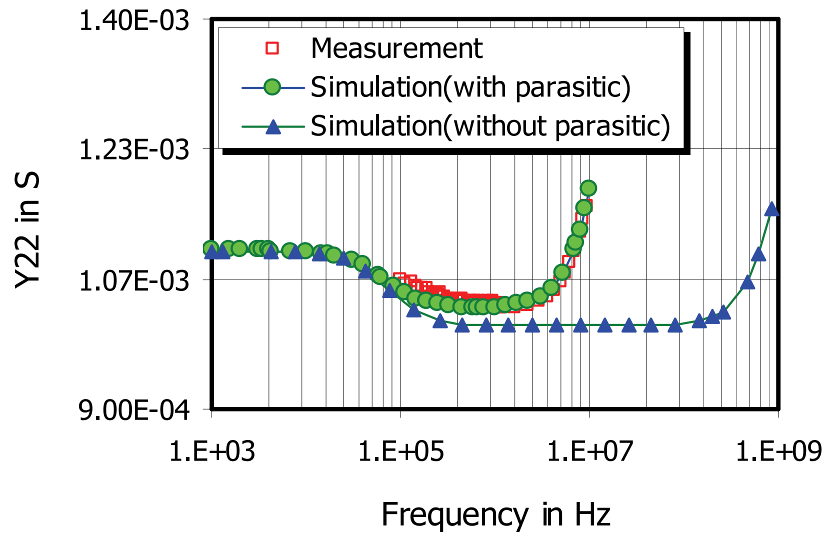
$$Y_{22} = g_o + \frac{g_{ct}(I_c + g_o V_c)}{1/R_{th} + j\omega C_{th} - (g_{ct}V_c + g_{bt}V_b)} + j\omega(C_{bc} + C_{cs} + C_{parasitic}) \quad (4.21)$$

The measurement data and the simulation results (simulation is done using the exactly same one port measurement setup) with and without parasitic capacitance are shown in Fig. 4.20. By comparing and optimizing the plots the thermal resistance can be estimated and extracted. In this measurement, after adding the parasitic capacitance at the ports, it can be observed that, the R_{th} value of the data matched with the default

value of the model R_{th}. In the sense, the simulated and measured Y_{22} matched. In both simulations and measurements S-parameter analyses have done.



(a)



(b)

Figure 4.21 The simulation and data comparison for the Y_{22} parameter. (a) 100 kHz to 10 MHz, (b) 100 kHz to 1 GHz.

4.6 Conclusion

The frequency domain thermal analysis has been done. With the help of a developed small signal thermal circuit, Y parameters are evaluated. The Y parameters are simulated by using a balanced differential amplifier. Y_{22} is simulated by varying thermal parameters and the bias current. It has been observed that, by comparing and optimizing the simulated and measures data, R_{th} can be extracted [2]. The measurement of the admittance parameter was done using one port measurement technique. The measured data is then compared with the simulated (with parasitic capacitance and self-heating turned) data for the same setup.

The theoretical $R_{th}C_{th}$ product estimate is $4.95e\text{-}6(t_{ox}/1.5)^2$, where t_{ox} is the thickness of the isolation oxide in microns [5]. The $R_{th}C_{th}$ is the thermal time constant. The thermal capacitance can be estimated by knowing the thermal time constant and the thermal resistance. The typical value for the thermal time constant is about 2 μs.

The measurement and simulation for the Y_{22} can be done by using a single transistor as well. It requires two 'bias-T's, one end for the dc bias and the other end for the ac signal. This will include actually an inductor through which the dc bias is applied and a capacitor through which the as signal is applied.

CHAPTER 5

THERMAL EFFECTS ON CURRENT MIRROR PERFORMANCE

Thermal effects on current mirror performance are significant. It is especially important to consider the thermal effects for current mirrors designed with dielectrically isolated bipolar devices. This research examines the impact of the self-heating and thermal coupling effect on the output characteristics of a simple current mirror as well as the self-heating effect on the output characteristics of the other frequently used current mirrors in the analog integrated circuit design. The previously developed (chapter 4) new small signal circuit model of a bipolar transistor [2], [6], [16], and [17], which included the self-heating effect, is used to analyze the output characteristics of the current mirrors. The circuits are analyzed using the VBIC model of DIBJTs as usual.

As discussed before, the self-heating is fairly large in dielectrically isolated bipolar technology. This effect has a substantial role in analog integrated circuit performance. Dielectrically isolated devices are made by a trench isolation process, where a very narrow and comparatively deep trench is etched on all sides of the device [4]. SiO_2 exhibits high resistance to heat flow due to its negligible thermal conductivity, so the device is affected by thermal heating. The self-heating effect is typically confined within the heat generating device itself [4]. Self-heating causes a significant change of

output resistance at low frequency or dc [1] and [2]. Such distortion can significantly affect the large signal dc circuits and the frequency response (settling error) of high-gain amplifiers. The self-heating effect in large-signal dc circuits is limited to those precision analog circuits whose characteristics depend on the close matching of the devices [3]. The current mirror circuits demand perfect matching of the shared devices and very high output resistance (ideally infinity). Hence, these circuits are affected by self-heating since their performances are dependent on the output resistance, which is reduced by self-heating induced errors. Munro and Ye [27] show the self-heating effect of a current mirror. Tenbroek *et* al. [28] examines the self-heating and thermal coupling effect for current mirror using silicon on insulator (SOI) complementary metal oxide semiconductor (CMOS) technology. Due to the increasing package density of integrated circuits, thermal effects become more and more important.

5.1 The Output Resistance and the Self-heating Effect

By using the previously developed small signal model and circuit analysis, the output impedance of a simple current mirror with self-heating can be evaluated as [17]

$$Z_{out} = \frac{1}{\left[\left\{ g_o + j\omega\left(C_{bc} + C_{cs}\right) \right\} + \frac{g_{ct}\left(I_c + g_o V_c\right)}{\left\{ Y_{th} - \left(g_{ct} V_c + g_{bt} V_b\right) \right\}} \right]} \tag{5.1}$$

For the large signal dc analysis, the frequency dependent term can be ignored in (5.1). Then the expression of the output resistance is simplified to [16] and [17]

$$Z_{out}\left(f = 0\right) = R_{out} = \frac{1}{g_o + \frac{g_{ct}\left(I_c + g_o V_c\right)}{\frac{1}{R_{th}} - \left(g_{ct} V_c + g_{bt} V_b\right)}} \tag{5.2}$$

Therefore, the magnitude of the output resistance depends on the thermal resistance (R_{th}), thermal capacitance (C_{th}) when frequency is considered, device dimensions, and the operating conditions of the transistor. It is evident from (5.2) that, the output resistance of the current mirror is decreased for the self-heating (R_{th}) effect [16] and [17]. This indicates the reduction of early voltage as well. There are several ways to measure the thermal resistance. Two methods described in the previous chapters 3 and 4 at both dc and over frequency. If no self-heating is considered, then the thermal resistance component can be set to zero in (5.2). Hence, it is simply the inverse of the effective output conductance of the device [2], [16], and [17]. So, the expression for the output resistance can simply be written as

$$R_{out} = \frac{1}{g_o} \tag{5.3}$$

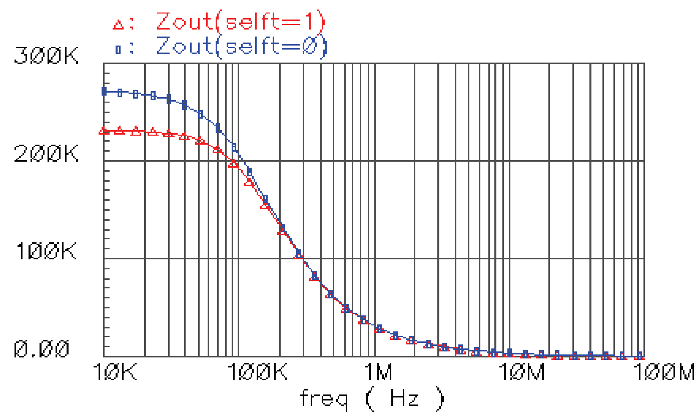


Figure 5.1 Magnitude of the output impedance for a CE single transistor system, as simulated with and without accounting for self-heating.

The Z_{out} or R_{out} expressed in (5.1) – (5.3) did not included any load resistance. These equations clearly show that, the output resistance is reduced by the thermal

effect. At high frequency the thermal network is shorted out and has no effect on the circuit operation. The graph in Fig. 5.1 shows the R_{out} versus frequency of a single transistor common emitter circuit. The V_{be} used is 0.8 V and the V_{ce} used as 3 V. It is observed that at low frequency R_{out} is lower than the normal value of R_{out} when the self-heating is considered. No thermal effect is noticed at high frequency and the effects of the transistors capacitances become significant.

5.2 Current Mirror and Self-heating

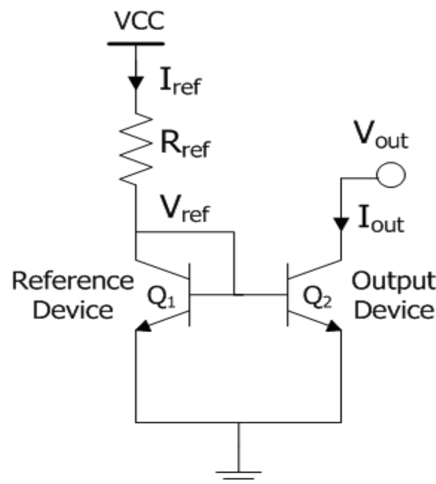


Figure 5.2 A simple current mirror.

A simple current mirror is shown in Fig. 5.2. Assume the two devices, the reference device and the output device are similar with high beta (gain), thus have negligible base current. So, the reference current can be expressed as

$$I_{ref} = I_{c1} = I_{S1}\, e^{\frac{V_{be1}}{V_t}} \left(1 + \frac{V_{ref}}{V_{A1}}\right) \tag{5.4}$$

$$I_{out} = I_{c2} = I_{S2}\, e^{\frac{V_{be2}}{V_t}} \left(1 + \frac{V_{out}}{V_{A2}}\right) \tag{5.5}$$

By subtracting (5.4) from (5.5)

$$I_{out} - I_{ref} = I_S\, e^{\frac{V_{be}}{V_t}} \left(\frac{V_{out} - V_{ref}}{V_A} \right) \tag{5.6}$$

when, $I_{S1} = I_{S2} = I_S,\ V_{be1} = V_{be2} = V_{be},\ V_{A1} = V_{A2} = V_A\ ,\ \eta = 1$

(5.6) can be simplified as

$$I_{out} = I_{ref} + I_c \left(\frac{V_{out} - V_{ref}}{V_A} \right) \tag{5.7}$$

in which, $I_c = I_S\, e^{\frac{V_{be}}{V_t}}$

The output resistance of a current mirror is the reciprocal of the slope of the output characteristic at a given operating point [21]. The output resistance (R_{out}) can also be defined as

$$R_{out} = \frac{VA}{I_c} \tag{5.8}$$

Hence, the relation between the reference current and the output current expressed in (5.7) can be modified as

$$I_{out} = I_{ref} + \left(\frac{V_{out} - V_{ref}}{R_{out}} \right) \tag{5.9}$$

The output current is a function of the output voltage and the reference current is a function of the reference voltage. Thus,

$$I_{out}(V_{out}) = I_{ref}(V_{ref}) + \left(\frac{V_{out} - V_{ref}}{R_{out}} \right) \tag{5.10}$$

For an unbalanced mirror, the reference and output devices are mismatched and

$$V_{out} \neq V_{ref} \tag{5.11}$$

Therefore, the output current is affected by the finite R_{out} (output resistance). For this non ideal condition an additional part ($\Delta I_{finite\text{-}Rout}$) is included to the current mirror equation [16]. This is shown in (5.12)

$$I_{out}(V_{out}) = I_{ref}(V_{ref}) + \Delta I_{finite\ -\ Rout} \tag{5.12}$$

where, $\Delta I_{finite\ -\ Rout} = \dfrac{V_{out}\ -\ V_{ref}}{R_{out}}$ (5.13)

Equation (5.2) proves that the self-heating effect by the thermal resistance (R_{th}) decreases the output resistance. The output and the reference voltages are assumed constant with respect to the other circuit parameters. In the real world the output voltage is not constant and depends on several factors; i.e. base current, gain, early voltage, circuit configuration etc. These effects are not considered here. The inclusion of this thermal effect in (5.10) shows that the non-ideal term increases by a significant amount when self-heating decreases output resistance.

$$I_{out}(V_{out}) = I_{ref}(V_{ref}) + \left[\frac{V_{out}\ -\ V_{ref}}{1 \Big/ \left\{ g_o + \dfrac{g_{ct}(I_c + g_o V_c)}{1/R_{th} - (g_{ct}V_c + g_{bt}V_b)} \right\}} \right] \tag{5.14}$$

where, $R_{out} = 1 \Big/ \left\{ g_o + \dfrac{g_{ct}(I_c + g_o V_c)}{1/R_{th} - (g_{ct}V_c + g_{bt}V_b)} \right\}$

Therefore, the denominator in (5.14) is less than the ideal dc value ($1/g_o$) of the output resistance. If the reduction of R_{out} is expressed by $\Delta R_{out\text{-}self\text{-}heating}$, then (5.14) can be rewritten as

$$I_{out}(V_{out}) = I_{ref}(V_{ref}) + \left(\frac{V_{out}\ -\ V_{ref}}{R_{out}\ -\ \Delta R_{out\ -\ self\ -\ heating}} \right) \tag{5.15}$$

where, $\left(R_{out} - \Delta R_{out - self - heating}\right) = R_{out - self - heating}$ (5.16)

By comparing second term (non ideal part) of (5.15) and (5.10) it can be concluded that,

$$\left(\frac{V_{out} - V_{ref}}{R_{out} - \Delta R_{out - self - heating}}\right) > \left(\frac{V_{out} - V_{ref}}{R_{out}}\right) \quad (5.17)$$

Therefore by using (5.15) and the non equality shown in (5.17) an additional error current, $\Delta I_{self\ heating}$ is included to the current mirror equation (5.12). This is shown in (5.18)

$$I_{out}\left(V_{out}\right) = I_{ref}\left(V_{ref}\right) + \Delta I_{finite - Rout} + \Delta I_{self\ heating} \quad (5.18.1)$$

So, the non-ideal parts are induced because of i) finite output resistance, and ii) the self-heating effect. Hence, the output current consists of three terms as shown in (5.18.1). This can be re-formulated as

$$I_{out} = I_{ref}\left(1 + \delta_{finite - Rout} + \delta_{th - self - heating}\right) \quad (5.18.2)$$

where, $\delta_{finite\text{-}Rout}$ is the current mirror due to finite output resistance and $\delta_{finite\text{-}self\text{-}heating}$ is for the self-heating induced error.

5.3 The Output Characteristics Model of a Simple Current Mirror with and without Self-heating

5.3.1 A Simple Current Mirror's Output Characteristics Model with and without Self-heating

As shown in Fig. 5.2, for a simple current mirror, the output characteristics are affected by the self-heating effect [16] and [17]. The three plots in this figure show different slopes which are explained as follows.

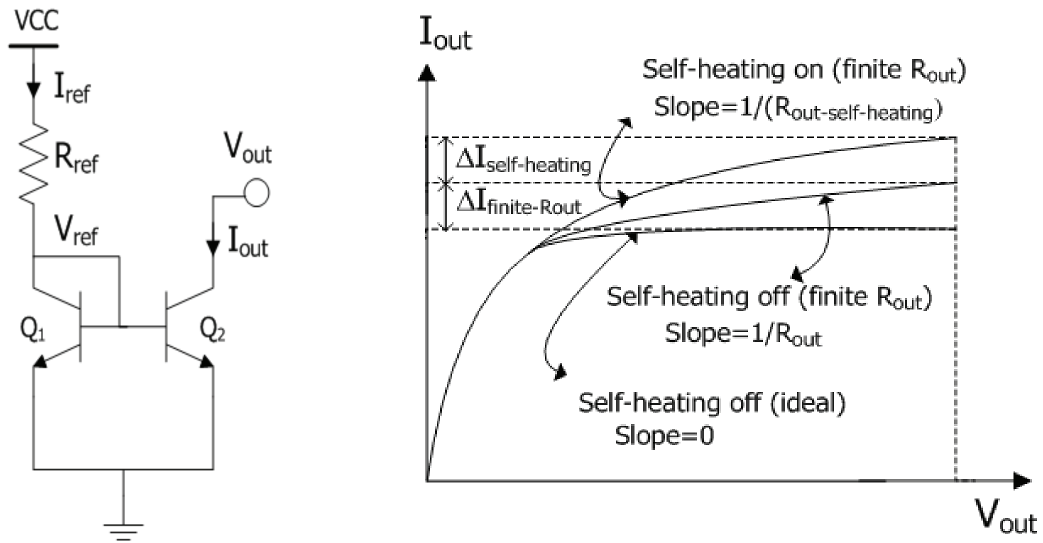


Figure 5.3 A simple current mirror and its output characteristics model with and without self-heating effect.

i) The slope, $dI_{out}/dV_{out} = 0$ is for $g_o = 0$, $R_{th} = 0$ in (5.14). In this case, $I_{out} = I_{ref}$ in (5.14) or (5.18).

ii) The slope $dI_{out}/dV_{out} = 1/R_{out} = g_o$ is for $g_o \neq 0$, $R_{th} = 0$ in (5.14). In this case, $I_{out}(V_{out}) = I_{ref}(V_{ref}) + \Delta I_{finite-Rout}$ as shown in (5.12). The term $\Delta I_{finite-Rout}$ accounts for the finite R_{out} ($g_o \neq 0$) affected increment of the I_{out}.

iii) The slope $dI_{out}/dV_{out} = 1/R_{out-self-heating}$ is for $g_o \neq 0$, $R_{th} \neq 0$ in (5.14). In this case, $I_{out}(V_{out}) = I_{ref}(V_{ref}) + \Delta I_{finite-Rout} + \Delta I_{self\ heating}$ as shown in (5.18.1). The term $\Delta I_{self-heating}$ accounts for the self-heating affected increment of the I_{out}.

5.3.2 Simulation and Measurement Result of a Simple Current Mirror's Output Characteristics with and without Self-heating

Cadence Spectre simulation was done for the current mirror shown in Fig. 5.2 using dielectrically isolated bipolar devices. In order to bias the circuit, the reference

resistance, R_{ref} at the collector node of Q_1 sets to 2 kΩ. The output voltage was varied from 0 to 3 V. The simulation was done for both self-heating on and off conditions. The R_{th}, C_{th} values used according to manufacturing the process. The term “selft” activates the thermal simulation in Spectre when it is set to 1. The simulation result is shown in Fig. 5.4.

A similar circuit has been fabricated with the VIP10 process with 2 µm device spacing between Q_1 and Q_2. The layout is shown in Fig. 5.5. Measurement result has been included in Fig. 5.4 as well. The HP4142B Modular DC Source/Monitor and ICCAP interfaced evaluation system are used for the measurements.

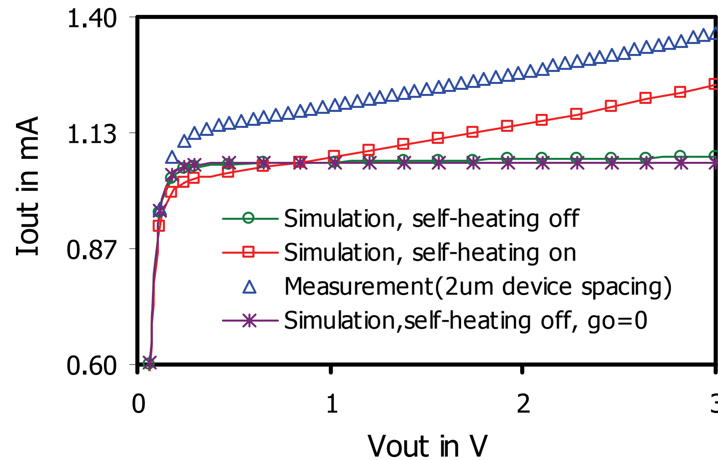


Figure 5.4 Simulation and measurement of a simple current mirror’s output characteristics with considering self-heating effect.

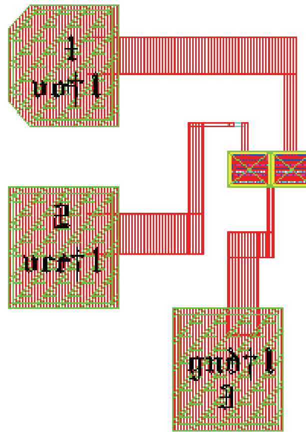


Figure 5.5 Layout a simple current mirror (UTA213).

The following Tables 5.1 shows the comparison chart of the temperature increase at the output device due to the self-heating.

Table 5.1 Simulation and measurement of the simple current mirror's temperature rise at the output device Q_2

Current Mirror Type	Data Type	dt self-heating ON (output device)
Simple Current Mirror	Simulation	3.255 ºC
	Measurement	4.0920 ºC

5.4 Analysis, Simulation, and Measurement of Different Current Mirrors Considering Self Heating Effect

5.4.1 Analysis, Simulation and Measurement Results of the Different Current Mirrors with the Self-heating Effect

The discussions in earlier sections proved that, if the R_{out} can be increased, then the thermal effect is reduced or made negligible. At the circuit design level there are several ways to increase the R_{out}, to reduce the self-heating error. They include i)

emitter degeneration, ii) cascode connection, and iii) Wilson connection. The current mirrors mentioned above can either increase the output resistance or have more feedback to control the output current. In addition to improving the self-heating effect, the high output resistance has several other advantages in analog circuit design.

A simple current mirror with a beta helper (buffer type) has been used in analog circuit designs greatly. Thus, this circuit is analyzed, simulated and measured as well. This mirror improves the base current error but does not increase the output resistance, so, does not found to improve the self-heating effect. All the circuits are shown in Fig. 5.6 to Fig. 5.9.

In order to bias the current mirror circuits shown in Fig. 5.6 through Fig. 5.9, a reference resistance, R_{ref} is connected at each reference node for all the current mirrors. The R_{ref} is set to 2 kΩ for each case. The output voltage (V_{out}) was varied from 0 to 3 V for the emitter degenerated and beta helper current mirrors. For the cascode and Wilson current mirrors V_{out} varies from 0 to 4 V. The simulations and measurements for all the designs are done by the method described in section 5.3.2.

The simulation with and without considering self-heating and the measurement results of the output characteristics for i) emitter degenerated, ii) beta helper (buffer type), iii) cascode, and iv) Wilson current mirrors are shown in from Figs. 5.6-5.9. It is observed that the current level is different and higher than the ideal when self heating is considered. The slope of the I_{out} vs. V_{out} shows the deviation for this thermal effect. It is also observed that as the R_{out} increases for the advanced current mirrors, the slopes are more flat, and thus have less thermal effect.

The small signal output resistances of the current mirrors seen at the collectors of the output transistors are [21]

Beta helper mirror, $R_o \cong r_{o2}$ (5.19)

Emitter degenerated mirror, $R_o \cong r_{o2}(1 + g_m R_{e2})$ (5.20)

Cascode mirror, $R_o \cong \beta_0 r_{o4}$ (5.21)

Wilson mirror, $R_o \cong \beta_0 \frac{r_{o3}}{2}$ (5.22)

The Wilson mirror has the limitation of having less output resistance than the cascode connection. But this limitation can be overcome by introducing a diode connected device between the collector of Q_1 and the base of Q_3 in Fig. 5.9.

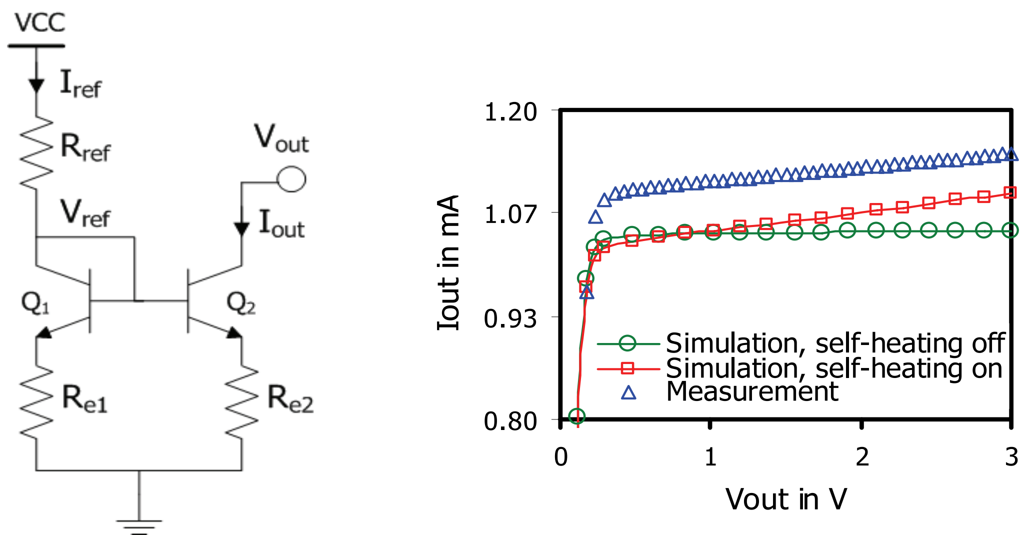


Figure 5.6 A simple current mirror with emitter degeneration (emitter degeneration resistance = 50 ohm) and the simulation and measurement of its output characteristics with considering self-heating effect.

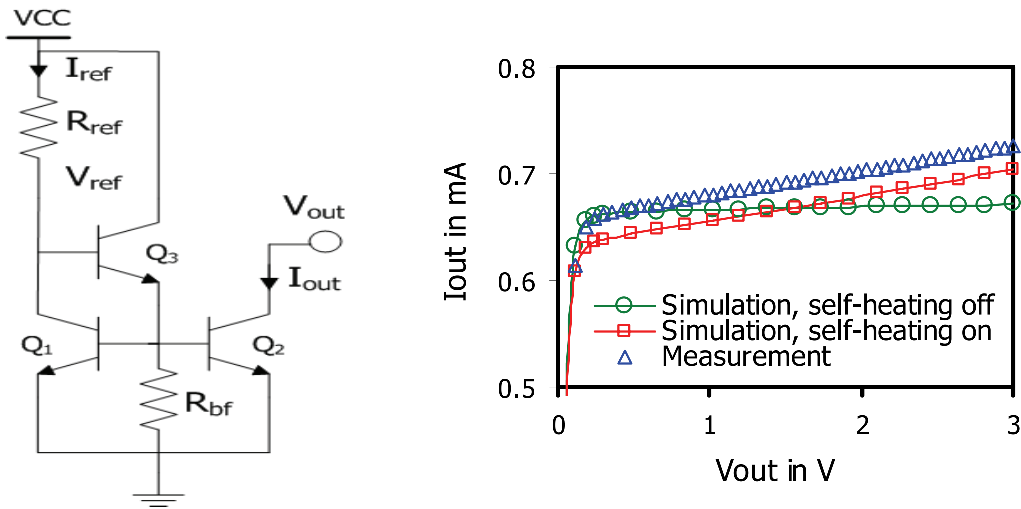


Figure 5.7 A simple current mirror with beta helper (buffer type) and the simulation and measurement its output characteristics with considering self-heating effect.

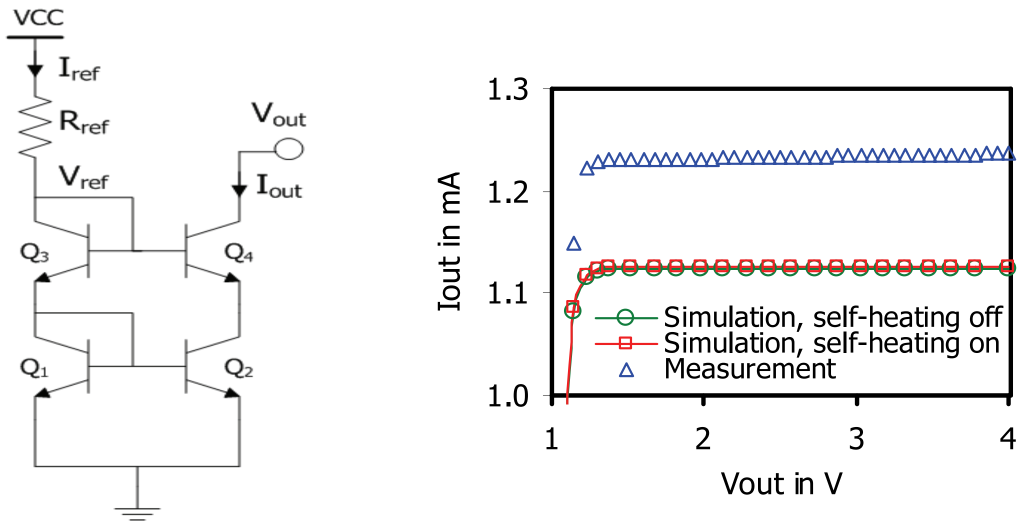


Figure 5.8 A cascode connected current mirror and the simulation and measurement its output characteristics with considering self-heating effect.

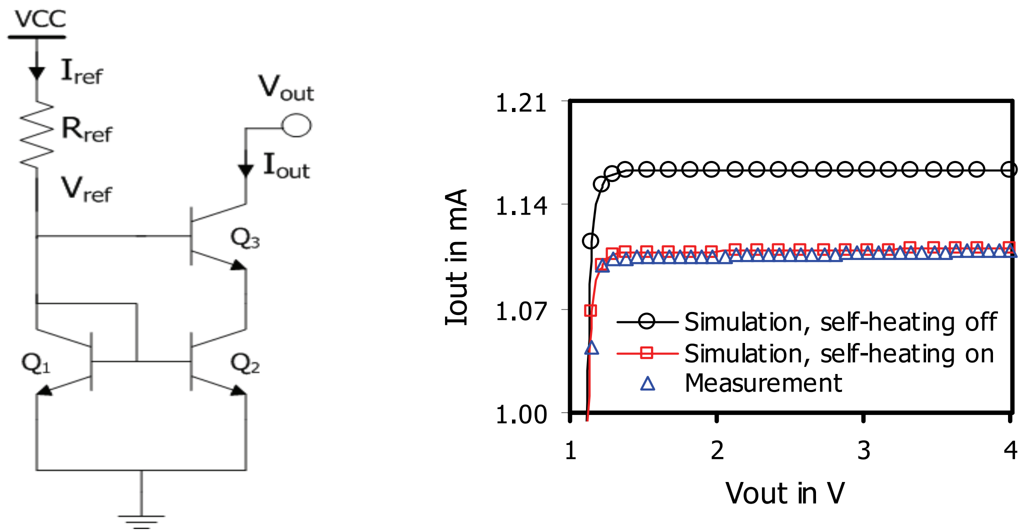


Figure 5.9 A Wilson current mirror and the simulation and measurement its output characteristics with considering self-heating effect.

5.4.2 Layout and Fabrication

The layouts for all the current mirrors are fabricated on the same chip. The chip device ID is UTA 213. A 14 pin DIP package is used. This is illustrated in Fig. 5.10.

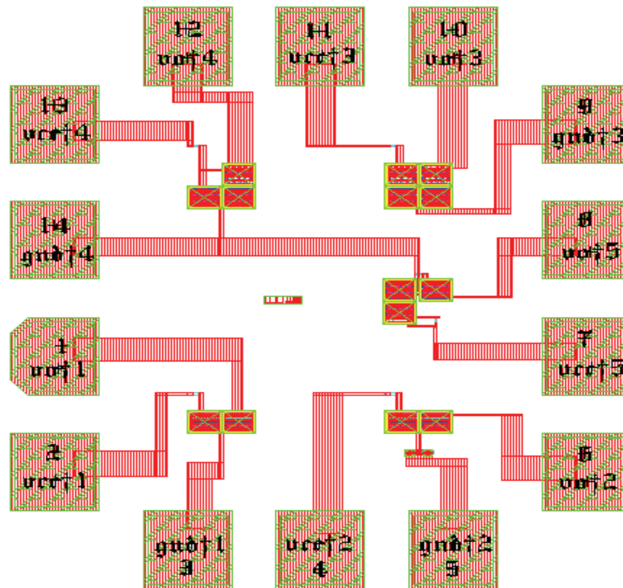


Figure 5.10 Layout of the different current mirrors in a single chip (UTA213).

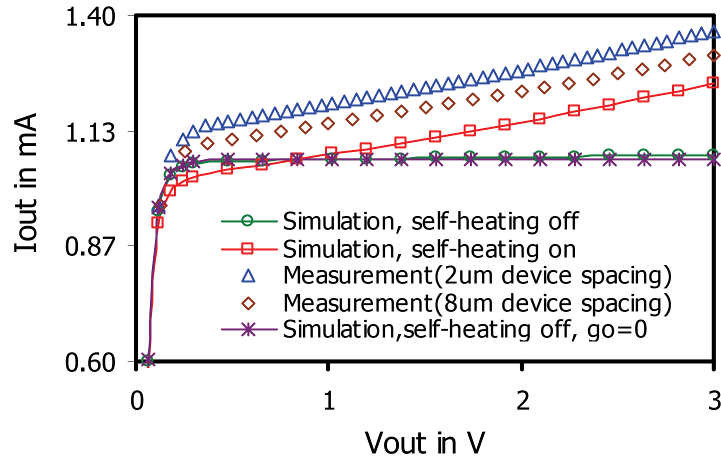
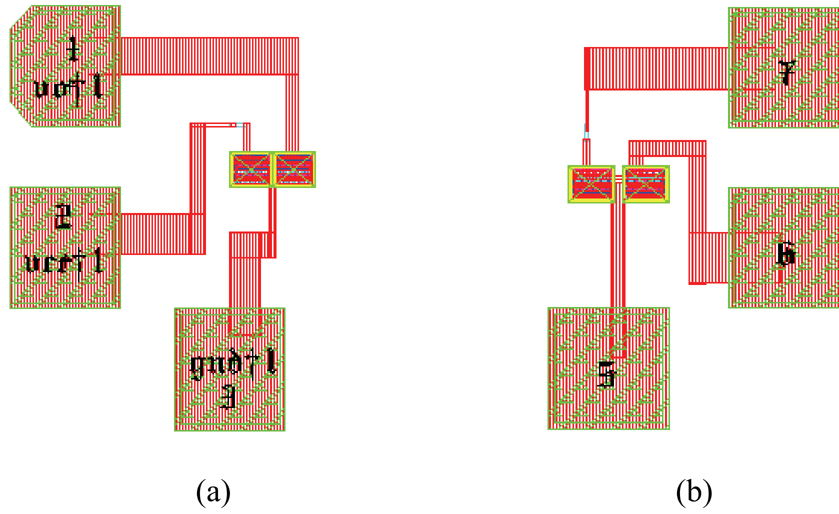


Figure 5.11 Simulation and measurement of a simple current mirror's output characteristics with considering self-heating and thermal coupling effect.

A simple current mirror shown in Fig. 5.2 is laid out and fabricated with different spacing between the reference device, Q_1 and the output device, Q_2. The spacings used for fabrication are 2 µm and 8 µm. It is noticed that for the adjacent device heating effects the current mirror with the larger separation between the devices shows less errors than the current mirror with closer devices. The detailed modeling and characterization analysis of the adjacent device heating effects is described in chapter 3. The R_{distr} part of the five element thermal resistance for both Q_1 and Q_2 are activated for the thermal coupling. The transistor Q_1 is diode connected, so, temperature increase due to the thermal effect is less than the Q_2 transistor. These temperature increments affect each other device and can also be represented in a circuit simulator as a VCVS model with the dt (temperature rise) and tl (local temperature) nodes. Naturally devices spaced far away have less thermal coupling effect. It is shown in chapter 3 that, thermal

coupling decreases logarithmically with the space (distance between the transistors). The thermal coupling effect measurement for the simple current mirror is added in Fig. 5.11. It is observed that, when the devices are more apart, then the output characteristics have less error.



(a) (b)

Figure 5.12 Layout of a simple current mirror with different device spacings (UTA213 and UTA225). (a) 2 µm and (b) 4 µm.

5.6 Current Feedback Amplifier High Impedance Node Simulation with Current Mirrors in the Middle Stage

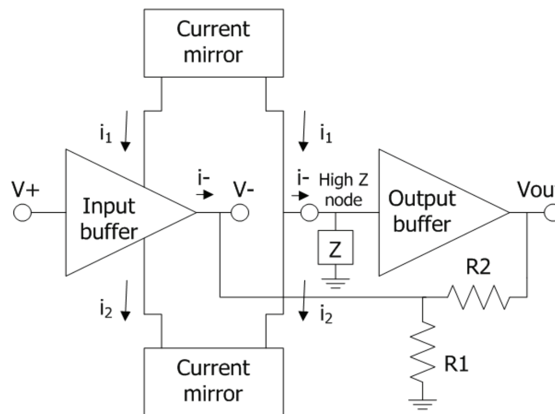


Figure 5.13 Current feedback operational amplifier (CFOA) block.

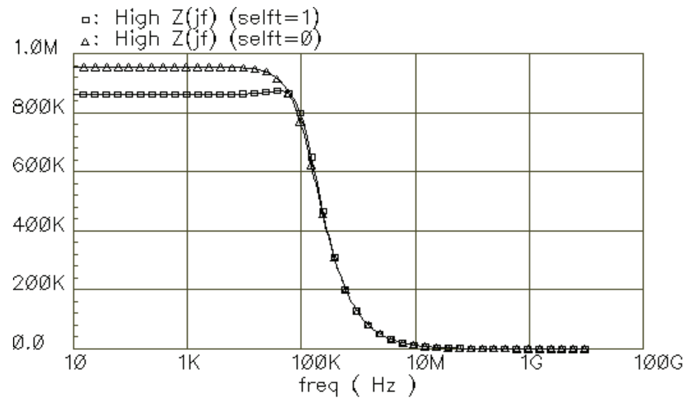


Figure 5.14 Simulation of the CFOA's high impedance node versus frequency.

The high speed CFOA uses the current mirrors as one of its fundamental components. The gain of the CFOA's (Fig. 5.13) depends on the high impedance (high Z) node. The impedance at this node depends directly on the R_{out} of the current mirrors, which is affected by the thermal effect. So, CFOA operation is affected by the thermal effect as well. It is observed that at low frequency the impedance at the high Z node significantly reduced with self-heating (Fig. 5.14), which in turn affects the gain. The gain of a transimpedance CFOA (Fig. 5.13) is expressed by [29]

$$Vout/\, i - = Z(jf) \qquad (5.23)$$

5.7 Conclusion

It is clearly observed that the advanced mirrors have less self-heating effect on their output characteristics than that of the simple mirrors. A current mirror with wide device spacing has reduced thermal coupling effect. The early voltage is also affected by the self-heating effect, as seen from the I_{out} versus V_{out} plots (Figs. 5.6 – 5.9) when considering the self-heating effect. So, by proper design, the transistor's R_{th} can be reduced to get less self-heating. The current mirror error analysis present in this chapter

did not include any other error like process error or saturation current error etc. In addition wide spacing between the transistors, different circuit layout structure may need to be considered to reduce the thermal coupling effect. If a different thermal resistance value is used in the simulation, which may show little difference in the plots. The devices used for the simulation, and fabrication can work in the mA range.

CHAPTER 6

V_{BE} REFERENCED BOOTSTRAP CURRENT SOURCE, SENSITIVITY AND SELF-HEATING EFFECT

This research presents the design of V_{be} based bootstrap (self-bias) current source and self-heating effects on its performance. The performance of this reference circuit is measured by the sensitivity of the output current with respect to the power supply voltage. The self-heating effect on the base emitter voltage is presented as well. In addition, previously discussed output resistance of a device and its dependency on the self-heating effect is used to clarify the design requirements. Based upon the basic principle of the V_{be} referenced bootstrap current source, several combinations of current sources and current mirrors are used for the design to compensate the self-heating effect degraded circuit's sensitivity. Simulation and measurement results validate the design and show that the proposed current source has improved sensitivity and less self-heating effect over the conventional bootstrapped V_{be} referenced current source [30].

Self-heating effects in large-signal dc circuits are limited to those precision analog circuits whose characteristics depend on close matching of devices. The self-biased V_{be} based current source is the other large-signal analog circuits in which the sensitivity is affected by self-heating since V_{be} and output resistance is decreased by self-heating induced errors [1], [17], and [30]. The V_{be} referenced bias circuit is used in both bipolar and CMOS technology for supply insensitive biasing in many analog,

digital and power electronic system designs [31] - [33]. A limited discussion has been reported by Fox regarding the examination of the self-heating effect on the V_{be} based self-bias circuit [1]. This research observed comparable results to the published paper, but intended to discuss more elaborately with respect to comparative studies, simulations and measurement results.

The comparison of the different V_{be} reference bootstrap current source design options to reduce the sensitivity and self-heating effect is presented. The computer optimized design was fabricated. A start-up circuit is also included in the final design to make sure the circuit is not operating in the zero current condition.

6.1 V_{BE} Referenced Current Source and the Bootstrap (self-biasing) Principle

6.1.1 V_{BE} referenced current source

To achieve supply insensitive biasing, a V_{be} referenced current source is used for analog integrated circuit designs [21]. The V_{be} referenced current source is shown in Fig. 6.1. I_{in} and I_{out} are the input and the output currents respectively. For this design, it can be observed that, the output current is dependent on the base emitter voltage not on the supply voltage. By ignoring the effects of I_b, β_F, and V_A the I_{out} can be evaluated as

$$I_{out} = \frac{V_{be1}}{R_2} \cong \frac{V_t}{R_2} \ln\left(\frac{I_{in}}{I_S}\right) \tag{6.1}$$

where, $V_{be1} \cong V_t \ln\left(\frac{I_{in}}{I_S}\right)$ (6.2)

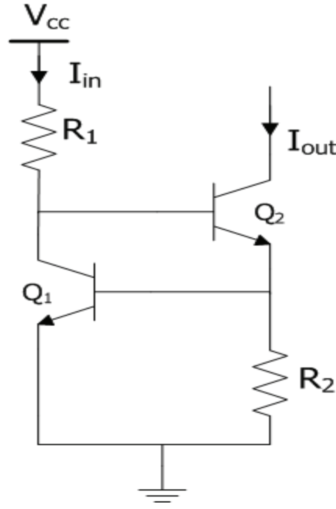


Figure 6.1 V_{be} referenced current source.

The parameter for describing the variation of the output current (y) with the power-supply voltage (x) is the sensitivity S and is defined as [21]

$$S_{x}^{y} = \lim_{x \to 0} \frac{\Delta y/y}{\Delta x/x} = \frac{x}{y}\frac{\partial y}{\partial x} \tag{6.3}$$

If y and x corresponds to I_{out} and V_{cc} respectively, then (6.3) can be re-written as

$$S_{V_{cc}}^{I_{out}} = \frac{V_{cc}}{I_{out}}\frac{\partial I_{out}}{\partial V_{cc}} \tag{6.4}$$

The sensitivity of the V_{BE} referenced current source (Fig.1.) can be simplified by using (6.2) and (6.4) as [21]

$$S_{V_{cc}}^{I_{out}} = \frac{V_t}{I_{out}R_2} S_{V_{cc}}^{I_{in}} = \frac{V_t}{V_{be}} S_{V_{cc}}^{I_{in}} \tag{6.5}$$

in which the expression for I_{in} and the sensitivity of I_{in} to V_{CC} are given by

$$I_{in} = \frac{V_{cc} - 2V_{be}}{R_1} \tag{6.6}$$

$$S_{V_{cc}}^{I_{in}} = \frac{V_{cc}}{I_{in}}\frac{\partial I_{in}}{\partial V_{cc}} \tag{6.7}$$

and the sensitivity of I_{in} to V_{cc} can be set to one if $V_{cc} >> 2V_{be}$. So, using (6.5) – (6.7), the sensitivity of I_{out} to V_{CC} can be re-evaluated as

$$S_{V_{cc}}^{I_{out}} = \frac{V_t}{I_{out} R_2} = \frac{V_t}{V_{be}} \quad (6.8)$$

Hence, the output current sensitivity depends on I_{out} and V_{be} which are affected by the self-heating [2-3].

6.1.2 The Bootstrap (self-biasing) principle

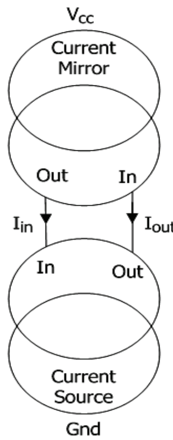


Figure 6.2 Standard bootstrap block diagram [21].

The bootstrap or self-biasing technique is used to minimize the power supply sensitivity to the output current [21]. The block diagram of the bootstrap technique is shown in Fig. 6.2. The input current is not developed by connecting a resistor to the supply. In principle, a current mirror and a current source are connected in such a way that, a feedback loop is generated, where the input current is made dependent on the output current. The current mirror can be any type used in analog design, and the current source in this case is V_{be} referenced.

The input and output current relationships of the current mirror and current source of the bootstrap block are shown in Fig. 6.3. From the standpoint of current source I_{out} is almost independent of I_{in} for a wide range of I_{in}. From the standpoint of the current mirror $I_{in} = I_{out}$ (assume gain = 1). The operating point of the circuit must satisfy a stable condition, and this must be at the intersection of the two characteristics. As a result, point 1 is undesired (because $I_{out} = I_{in} = 0$) and point 2 is desired. Thus, between the two intersected operating points, point 1 is unstable, and point 2 is stable.

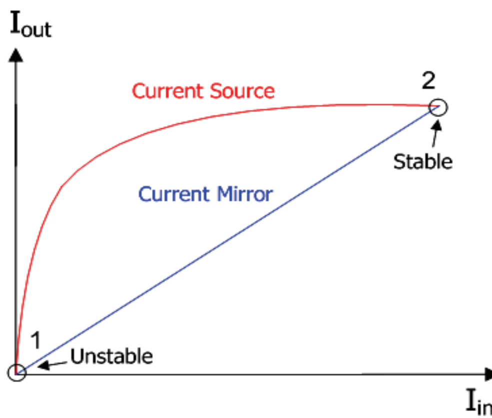


Figure 6.3 Determination of the operating point of the standard bootstrap current source.

The operation of the bootstrap circuit can be described as follows:

Suppose I_{out} increases for any reason → current mirror increases I_{in} (same amount, because gain = 1) → then current source increases I_{out} (depend on the gain of the current source) → so, they form a positive feedback loop. Thus, in Fig. 6.3 point 1 is unstable operating point (zero current and gain > 1). Point 2 is stable operating point (reasonable current and gain < 1, as needed for a stable +ve feedback). The Nyquist criterion can test the stability, which states that a circuit with positive feedback is stable

if the loop gain is less than unity [21]. Actually the loop gain of a self-biased circuit is determined by the gain of the current source, since the gain of the current mirror is usually unity.

Hence, as a whole, the V_{be} referenced bootstrap current source (Fig. 6.2.) may operate in the zero current condition even with non zero supply voltage (Fig. 6.3). A start-up circuit can be used to eliminate this problem.

The current mirror output resistance is extremely important for the current mirror itself and for the whole bootstrap circuit. This requires very high output resistance. Current mismatch between I_{in} and I_{out} increases in the current mirror as the output resistance is decreased by self-heating [17].

6.2 Self-Heating Effect on Base Emitter (V_{be}) Voltage and Output Resistance

6.2.1 Self-Heating on the Base Emitter (V_{be}) Voltage

The expression for the base emitter voltage is given by (6.9) [34]. The details of this equation will be shown in chapter 7 and in the appendix.

$$V_{be}(T) \cong E_g(0) - \{E_g(0) - V_{be}(T_0)\}\left(\frac{T}{T_0}\right) - (XIS - 1) \times V_t(T) \times \ln\left(\frac{T}{T_0}\right) \tag{6.9}$$

where, $E_g(0)$ is the extrapolated bandgap voltage at 0 K, $V_{be}(T_0)$ is the base-emitter voltage at the reference temperature T_0, XIS is the saturation current temperature coefficient and $V_t(T)$ is the thermal voltage at the temperature T.

But, when self-heating occurs, device temperature increases. Thus, the base emitter voltage is reduced by self-heating in (6.9). The relation between the base-emitter voltage and self-heating is [30]

$$V_{be}(T+\Delta T_{SH}) \cong E_g(0) - \{E_g(0) - V_{be}(T_0)\}\left(\frac{T+\Delta T_{SH}}{T_0}\right) - (XIS-1)\times V_t(T+\Delta T_{SH})\times \ln\left(\frac{T+\Delta T_{SH}}{T_0}\right)$$

(6.10)

in which, ΔT_{SH} is the temperature that is increased by self-heating.

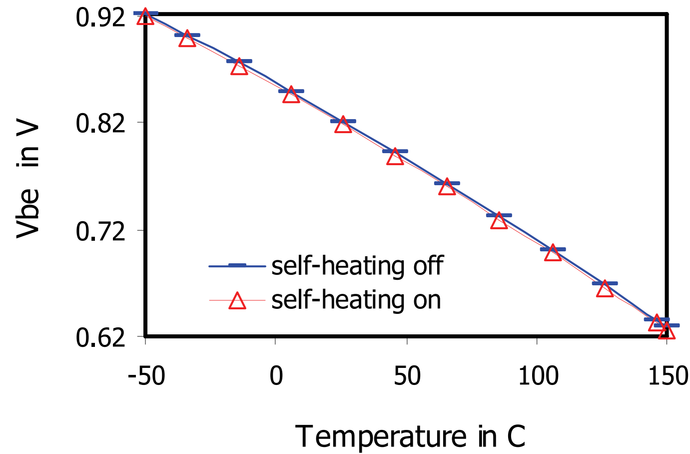


Figure 6.4 Simulation of V_{be} versus temperature (with and without self-heating) for a single transistor system.

Table 6.1 V_{be} and Temperature with and without self-heating effect

Temperature in Centigrade	Self-heating OFF V_{be} in V	Self-heating ON V_{be} in V
-50	0.9212	0.9194
-34	0.9014	0.8994
-14	0.8755	0.8733
6	0.8486	0.8462
26	0.8207	0.8182
46	0.7918	0.7893
66	0.7621	0.7595
86	0.7316	0.7290
106	0.7003	0.6977
126	0.6683	0.6657
146	0.6357	0.6331
150	0.6291	0.6265

The temperature change ΔT_{SH} in (6.10) can be calculated by the methods and formulas shown in chapter 4. The temperature change ΔT_{SH} is actually equivalent to the temperature (Tj-$T_{ambient}$), at the dt node of a device in Spice.

It is found that, self heating causes the base emitter voltage to drop by about -1.80 mV to -2.6 mV at different temperatures as shown in Fig. 6.4 and Table 6.1.

6.2.2 Self-Heating Effect on the Output Resistance

Most of the thermally induced errors in large-signal modeling can be understood by extrapolating from the small-signal behavior [1], [3]. Thus, the detailed small signal and dc analysis of the output resistance and the self-heating effect is presented in chapters 4 and 5.

It is found that the output resistance for a transistor or current mirror is reduced by self-heating at low frequencies. This error is maximum at dc. This is not expected for the bootstrap design where the matching of the input and the output currents of the current mirror is extremely important.

6.3 Simulating Bootstrapped (Self-Biased) V_{be} Referenced Current Source with and without Self-Heating

Current mirrors and current sources can be made with npn and pnp devices. There are several ways to connect BJTs together to make a bootstrapped (self biased) V_{be} based current source. Two examples are shown in Fig. 6.5. In Fig. 6.5(a) the design is made by a pnp current mirror and a npn current source. In Fig. 6.5(b) a npn current mirror and a pnp current source are used.

For both the Figures 6.5 (a) and (b), the current I_{out} is nominally not dependent on V_{cc}. But the finite R_{out} of current mirrors made of Q_3 and Q_4 in Fig. 6.5(a) and Q_1

and Q_2 in Fig. 6.5(b) causes I_{out} sensitive to V_{cc} or any external effect. In addition, self-heating reduces the output resistance. The finite R_{out} values of Q_2 in Fig. 6.5(a) and Q_3 in Fig. 6.5(b) affects the sensitivities as well [1]. The sensitivities for both cases are found by plotting I_{out} vs. V_{cc} and listed in Table 6.2. The sensitivity data in Table 6.2 show that, self-heating deteriorates the sensitivity of the output current with respect to supply voltage. Hence, for proper circuit operation this error must be considered and removed in the design process.

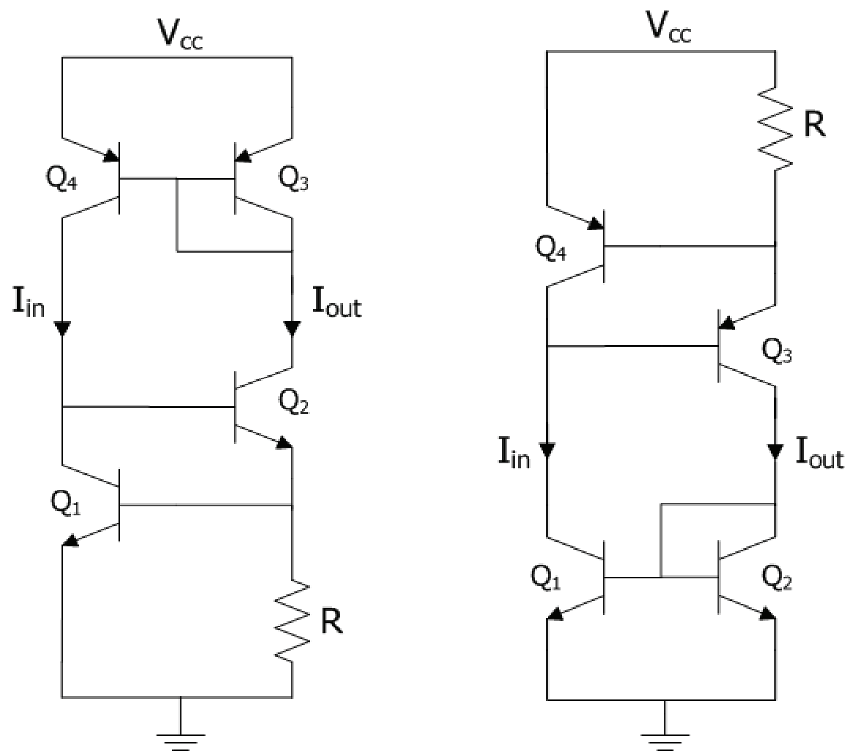


Figure 6.5 Self-biased V_{be} referenced current source made by (a) pnp current mirror and npn current source, (b) npn current mirror and pnp current source.

The VBIC model parameter, 'selft', needs to be set to the value of '1' to turn on self-heating in the circuit.

Table 6.2 Self-heating and Sensitivity Data
for the Figures 6.5 (a) and (b)

	$S_{V_{cc}}^{I_{out}}$	$S_{V_{cc}}^{I_{out}}$
	Fig. 6.5(a)	Fig. 6.5(a)
Self-heating OFF	0.0128	0.01905
Self-heating ON	0.0225	0.0279

6.4 Self-Heating Minimization Techniques

It has been clear from the earlier discussions that, techniques that increase the output resistance of current mirrors can reduce the affect of self-heating [17]. In practice, it has been found that, by increasing the output resistance of a current mirror, better matching between the input and output currents can be achieved as well. So, increasing output resistance not only reduces the difference between the input and output current, it will also reduce the self-heating effect.

There are several ways to increase the output resistance of the current mirrors shown in Fig. 6.5. These include using emitter degeneration, cascode, and Wilson type current mirrors. In addition, the Wilson current mirror has control on current through feedback and gives less sensitivity than others. Fig. 6.6 shows the three improved circuits. In Fig. 6.6(a) the self-biased V_{be} referenced current source uses a pnp emitter degenerated current mirror and npn current source, in Fig. 6.6(b) the pnp cascode current mirror and npn current source are used and the Fig. 6.6(c) a pnp Wilson current mirror and npn current source are used to realize the design. Table 6.3 shows the sensitivity of the improved circuits with self-heating on and off.

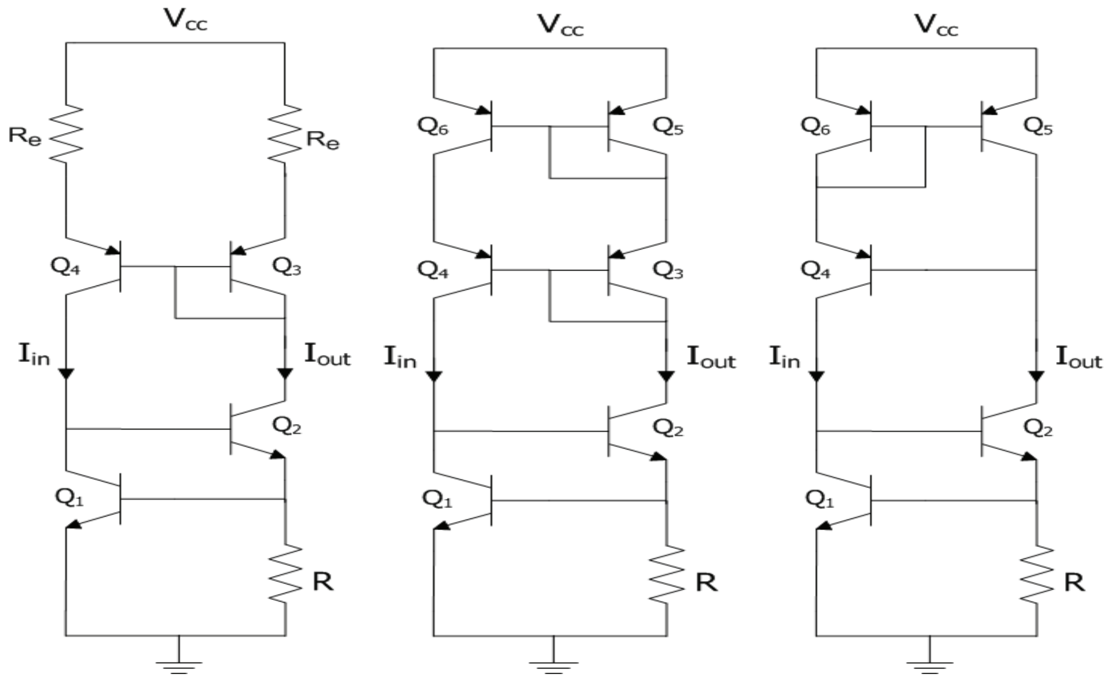


Figure 6.6 Self-biased V_{be} referenced current source made by (a) pnp emitter degenerated current mirror and npn current source, (b) pnp cascode current mirror and npn current source, (c) pnp Wilson current mirror and npn current source (proposed circuit).

Table 6.3 Self-heating and Sensitivity Data of the improved circuits shown in Figs. 6.6 (a), (b) and (c)

	$S_{V_{cc}}^{I_{out}}$	$S_{V_{cc}}^{I_{out}}$	$S_{V_{cc}}^{I_{out}}$
	Fig. 6.6 (a)	Fig. 6.6 (b)	Fig. 6.6 (c)
Self-heating OFF	0.00594	0.00220	0.00 1754
Self-heating ON	0.01254	0.00221	0.001763

It is found that Fig 6.6 (c) has the optimum sensitivity and minimum self-heating effect, which is designed with pnp Wilson current mirror and npn V_{be}

referenced current source. It is also estimated that, the output current error due to base emitter voltage reduction caused by self-heating, is controlled by Wilson mirror feedback. Thus, this circuit is proposed to use when self-heating is significant and considered in dielectrically isolated technology.

6.5 Design and Working Principle of the Self-heating Minimized Bootstrapped V_{be} Referenced Current Source

6.5.1 Design and Working Principle

The sensitivity data in Table 6.3 indicates that, the combination of the Wilson current mirror and a V_{be} based current source provides the minimum sensitivity and the lowest self-heating effect. To operate in a stable condition, this design may need a start-up circuit to remove the zero current condition. Hence a start-up circuit is added with the proposed V_{be} referenced bootstrap circuit [21]. A resistance R_1 is added at the collector of Q_1 to support the stability and biasing of the circuit. The proposed design is shown in Fig. 6.7. The circuit operation is given as follows [21].

- First, assume the circuit is in the undesired zero-current state → V_{be} of Q_1 would be zero → V_{be} of Q_2 would be few milivolts determined by the leakage current → voltage at left side of Q_7 = 4 diode drop → so voltage across R_1 = 3 diode drop → So, a current would flow through R_1 into $Q_1 – Q_2$ combination → this action would cause a current to flow in Q_4, Q_5, and Q_6 → avoiding zero current state.
- The circuit then drives itself toward the desired stable state.
- Start-up circuit must not interfere with the normal operation of the reference once the desired operating is reached.

• Under steady state current condition in $Q_1 \rightarrow V_{ce}$ of Q_1 = 2 diode drop → the voltage drop across R_1 needs to be large enough to reverse bias Q_7 → thus, design $I_{in}R_1 \geq 2$ diode drop → so, voltage drop across $R_1 \geq 4$ diode drop → now, voltage at left side of Q_7 (4 diode drop) ≤ voltage at right side of Q_7 (≥ 4 diode drop) → so, the start-up circuit would be disconnected from the reference circuit and has no impact on the normal circuit operation.

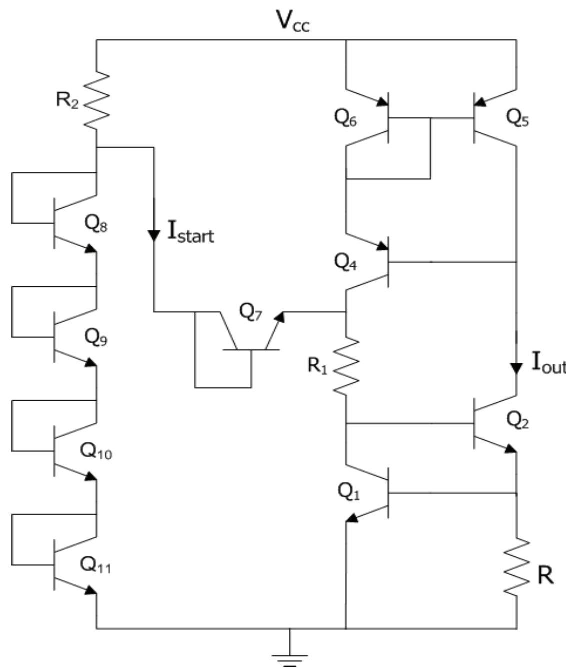


Figure 6.7 Fabricated V_{be} referenced bootstrap circuit with start-up.

6.6 Simulation, Layout, Fabrication and Measurement

The simulation result of the final circuit (Fig. 6.7) is shown in Fig. 6.8. The transient simulation in Fig. 6.9 shows no start-up error. It appears that the self-heating effect is minimized in this design. An 8 pin dual inline packaged chip is fabricated using National Semiconductor's VIP 10 process with dielectrically isolated devices. The

layout is shown in Fig. 6.10. The measurement result of the fabricated circuit is added in Fig. 6.8 as well. The measurement result validates the simulation result. In addition, the simulation is optimized by varying IS to match the measurement result.

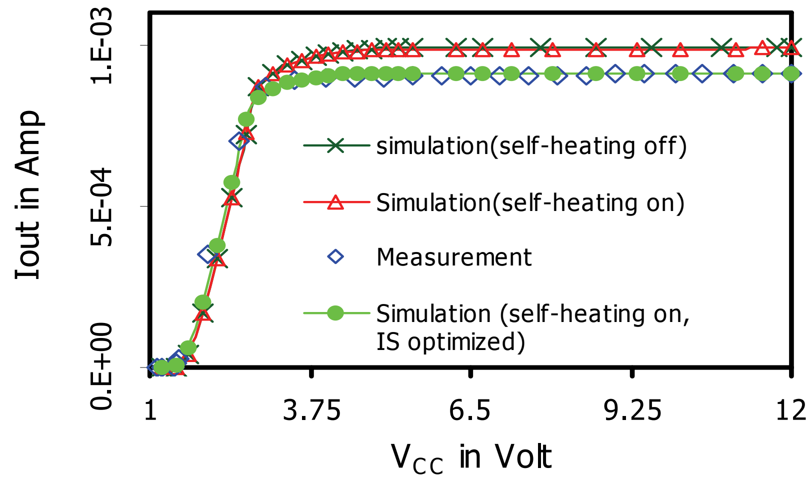


Figure 6.8 Simulation and measurement result of output current versus supply voltage fabricated V_{be} referenced bootstrap circuit.

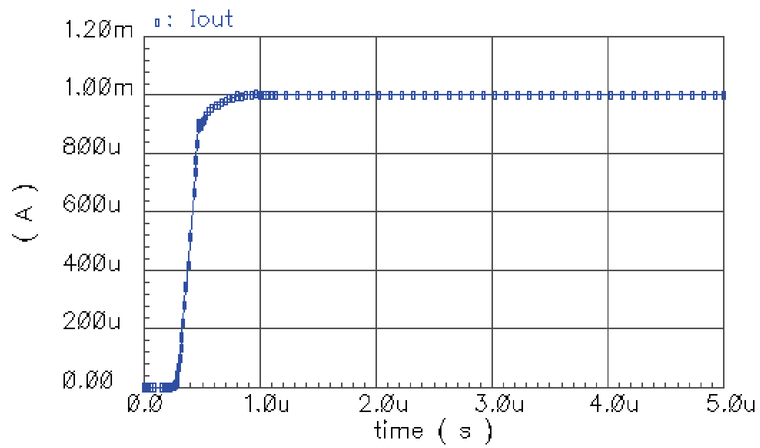


Figure 6.9 Transient simulation of the output current.

The sensitivity of the output current with respect to the supply voltage is 0.001 when simulated, neglecting self-heating and 0.001 with self-heating. The measurement gives a sensitivity of 0.0015 between 5V to 12V.

Table 6.4 Self-heating and Sensitivity Data of
the Fabricated circuit in Measurements

$S_{V_{cc}}^{I_{out}}$	$S_{V_{cc}}^{I_{out}}$	$S_{V_{cc}}^{I_{out}}$
Simulation Self-heating off 5 – 12 V	Simulation Self-heating on 5 – 12 V	Measurement 5 – 12 V
0.001	0.001	0.0015

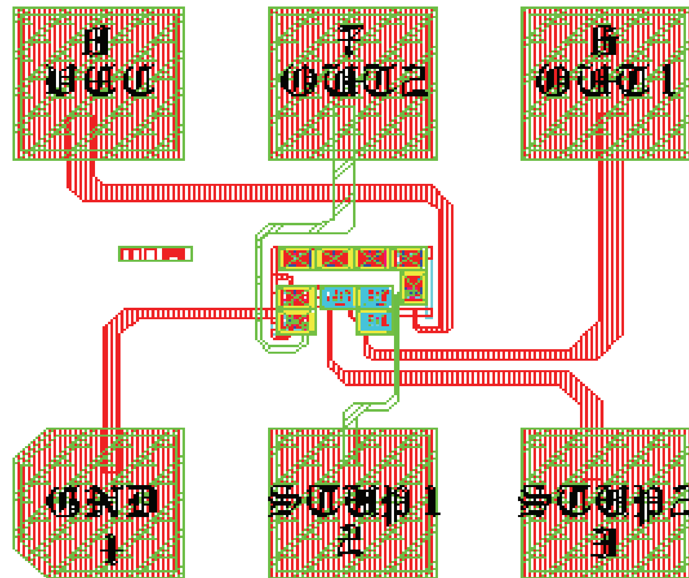


Figure 6.10 Layout of the fabricated circuit (UTA181).

Figure 6.11 Output current for low current operation.

Figure 6.12 Copying current to the external circuit.

6.7 Conclusion

In this chapter the self-heating effect on the base emitter voltage referenced bootstrap current source is simulated and measured. The fabricated circuit includes a

start-up circuit [21], which gives 0.0005 more sensitivity due to the additional circuitry. All the circuits have been designed and simulated by using the VIP10 process of the National Semiconductor Corporation. The designed current source was fabricated to provide ≈1mA current, but it can be reconfigured to work as a very low current source (Fig. 6.11) by changing the resistors R and R_1in the circuit shown in Fig.6.8. The Fig. 6.12 shows an example of the application of the design as a bias circuit.

CHAPTER 7

DESIGN OF HIGH ORDER CURVATURE CORRECTED BANDGAP REFERENCE AND SELF-HEATING

The bandgap reference circuit is one of the key sub-circuits in analog circuit design. This circuit is used in many analog designs for temperature insensitive biasing. For high-performance operation in analog, radio frequency, digital and mixed signal circuits, a high precision, temperature-compensated reference is needed [34]. Power management circuits have a significant role in portable devices. The bandgap reference is the primary component in power management circuits.

Temperature is one of the principal factors for the bandgap reference design, performance, and application. Any temperature change inside or outside the transistors used in a design affects or degrades the performance of any analog circuit. But as a reference, the bandgap reference needs to have stable performance over wide temperature range. Therefore, self-heating is a big factor in bandgap reference design, and needs to be considered in its effect on the design. This research focuses on the high order curvature corrected bandgap reference design and the self heating effects on the design performance. This identifies the errors due to self-heating and a proposed solution for the thermal effect reduction.

For a high precision reference, the temperature drift (working temperature range) should be as high as possible. The temperature variation must include both

negative and positive temperature variation. For constant, stable, and accurate operation, the temperature coefficient should be within a few parts per million per degree centigrade (ppm/ºC) range. The bandgap reference circuit requires highly accurate temperature correction. The design described here works for a very large temperature range and with a smaller temperature coefficient (for the same temperature variation). In addition, the proposed circuit requires small silicon area as well. This design shows improved thermal performance as compared to other published bandgap reference circuits. The design topology works for very low supply voltage as well.

The base emitter voltage is the basis for the bandgap reference. The proposed design first generates a current that is proportional to the base emitter voltage. Then, it generates two other currents, one is proportional to the absolute temperature, and the other one is a nonlinear current (high order curvature corrected current) which has logarithmic temperature characteristics [34] and [43]. The high order curvature compensation of the bandgap reference is done by adding the three currents mentioned above.

Two bandgap reference circuits have been designed and simulated with a similar topology but with different circuit configurations. This includes a self-heating minimized reference as well. One of the circuits is fabricated and measured. The used topology can accommodate a wide range of reference currents/voltages from a few µA to several mA and a few mV to several V [34]. The circuit uses 5V and 1.5 V as the supply voltages for the two designs. The designs use the current mode design technique to establish the reference current or voltage.

7.1 The Bandgap Reference Principle

The basic principle of the bandgap reference is to create a very stable voltage reference in regard to both temperature (self-heating effect included) and power supply variations.

7.1.1 The Base Emitter Voltage

The base emitter voltage, $V_{be}(T)$ of a bipolar device is temperature dependent. This can be expressed as [34]

$$V_{be}(T) \cong E_g(0) - \{E_g(0) - V_{be}(T_0)\}\frac{T}{T_0} - (XIS - n) \times V_t(T) \times \ln\left(\frac{T}{T_0}\right) \quad (7.1.1)$$

where, $E_g(0)$ is the bandgap voltage of silicon at 0 K in V, T_0 is the reference temperature, $V_{be}(T_0)$ is the base emitter voltage at T_0 in V, n is the exponent constant for base region electron mobility that is dependent on the doping level in the base [21], XIS is temperature constant of the saturation current for VBIC model, and $V_t = kT/q$ is the thermal voltage. The detailed analysis and derivation of the base emitter voltage are presented in the appendix B.

The Taylor series expansion (appendix B) of (7.1.1) can be done for the perfect representation of the nonlinear temperature terms associated with the logarithmic term. Hence, (7.1.1) can be rewritten by replacing the 3rd term with a 3rd order Taylor series expansion. This is shown in (7.1.2).

$$V_{be}(T) = Eg(0) - \{Eg(0) - Vbe(T_0)\}\frac{T}{T_0} - (XIS - n)\frac{kT_0}{q}\left\{\frac{1}{3} - \frac{1}{2}\frac{T}{T_0} + T^2 - \frac{1}{6}\left(\frac{T}{T_0}\right)^3\right\} \quad (7.1.2)$$

Thus, (7.1.1) and (7.1.2) show the temperature dependency of the base emitter voltage, $V_{be}(T)$. Essentially, it is observed that $V_{be}(T)$ has a negative temperature coefficient. It roughly decreases -1.25 mV/ºC to -2.5 mV/ºC at room temperature depending on the process type [21]. $V_{be}(T)$ has three components; i) a constant, ii) a linear temperature dependent term contains T, and iii) a nonlinear (log) temperature dependent term that contains T^n (n>1). It is also noticed that, the constant term is independent of the supply voltage. Therefore, the base emitter voltage can be compensated with respect to the temperature and the supply voltage to achieve a constant reference. The compensation can be done in two ways, i) 1st order: this compensate only the 2nd term of the $V_{be}(T)$ in (7.1), ii) high order: this compensate the 2nd and 3rd terms of the $V_{be}(T)$ in (7.1), thus, this method compensates all the temperature dependent terms in $V_{be}(T)$.

Moreover, the proposed relation between the base-emitter voltage and self-heating is expressed in (6.10), repeated here for convenience.

$$\begin{aligned} V_{be}(T + \Delta T_{SH}) \cong E_g(0) - \{E_g(0) - V_{be}(T_0)\}\left(\frac{T + \Delta T_{SH}}{T_0}\right) - \\ (XIS - 1) \times V_t(T + \Delta T_{SH}) \times \ln\left(\frac{T + \Delta T_{SH}}{T_0}\right) \end{aligned} \tag{7.2}$$

where, ΔT_{SH} is the temperature increase for the self-heating. ΔT_{SH} can be evaluated by the method and formula discussed in the previous chapters. Thus, for a precision reference design, both the 1st and high order temperature compensation require the consideration of the thermal effect.

7.1.2 The 1st Order Bandgap Reference Principle

The symbolic diagram in Fig. 7.1 is drawn to show the basic principle of the conventional bandgap reference circuit with the 1st order temperature compensation. To compensate only the linear temperature dependent term of $V_{be}(T)$ (2nd term in 7.1), a thermal voltage, which has a positive temperature coefficient can be generated. This is directly proportional to the absolute temperature (PTAT). This voltage increases at roughly 0.085 mV/ºC at room temperature. Now, $V_{be}(T)$ and $V_t(T)$ have opposite temperature coefficients (TC_F). So, by proper weighting, zero temperature coefficient can be attainable. Thus, multiply V_t by a constant M_2 and summed with the M_1V_{be} to get a constant reference voltage. The reference voltage (Fig. 7.1) can be expressed as

$$V_{ref} = M_1 V_{be} + M_2 V_t \qquad (7.3)$$

The corresponding plots for the V_{be}, V_t, and V_{ref} are shown are shown in Fig. 7.2. The Fig. 7.2(c) is the expected graph for the ideal reference. But for the 1st order design, high order temperature terms are not compensated. Therefore, practically the reference voltage looks like the shape shown in Fig. 7.2(d).

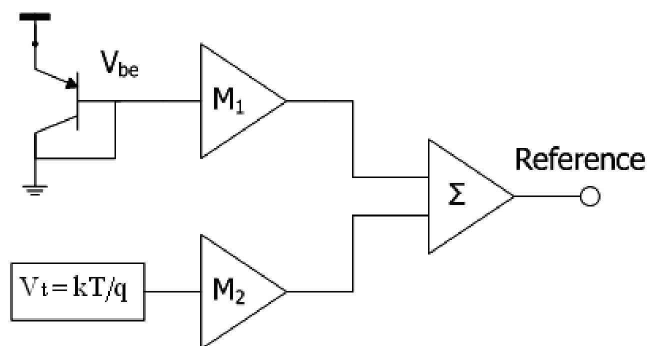


Figure 7.1 The principle of the standard 1st order bandgap reference.

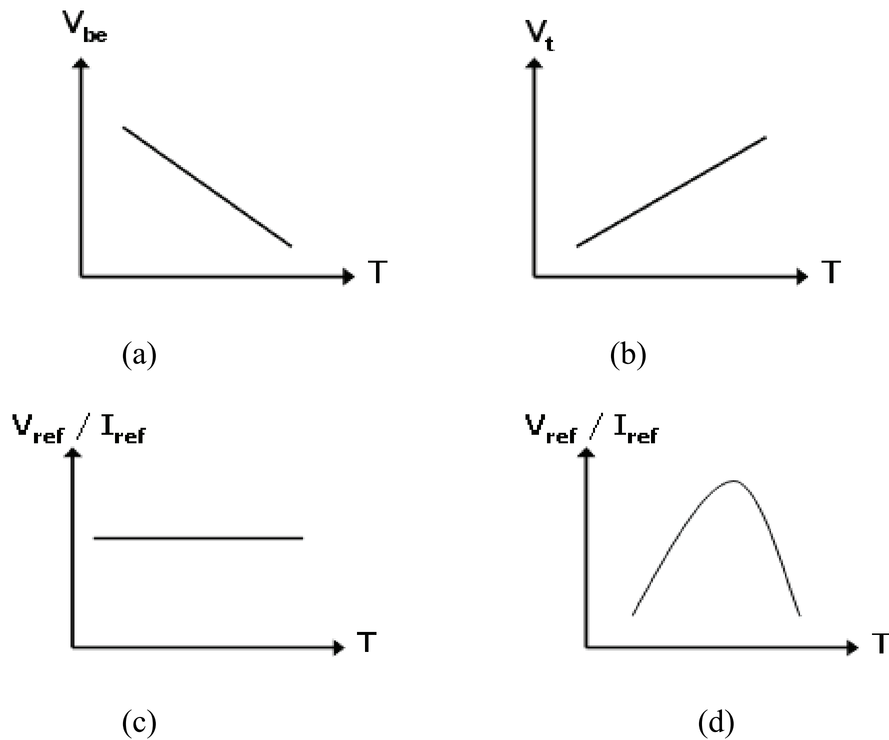


Figure 7.2 Temperature dependence of the different bandgap reference (1st order) components. (a) V_{be} versus temperature, (b) V_t versus temperature, (c) reference voltage/current versus temperature (ideal), and (d) reference voltage/current versus temperature (actual).

7.1.3 The High Order Curvature Corrected Bandgap Reference Principle

In order to design a high order curvature corrected bandgap reference circuit, all the temperature dependent terms in V_{be} (T) must be compensated. Hence, to compensate the proportional to T (temperature) and proportional to T^n (non-linear temperature, $n > 1$) terms, two current or voltage sources, linearly temperature dependent and nonlinearly temperature dependent, can be generated. The symbolic diagram in Fig. 7.3 is drawn to show the proposed bandgap reference operation. Compared to Fig. 7.1, an additional block, T^n, with a multiplier, M_3, is added. The linear (M_2V_t) and nonlinear (M_3T^n) compensating currents or voltages must be positive and added with the M_1V_{be} (T). The

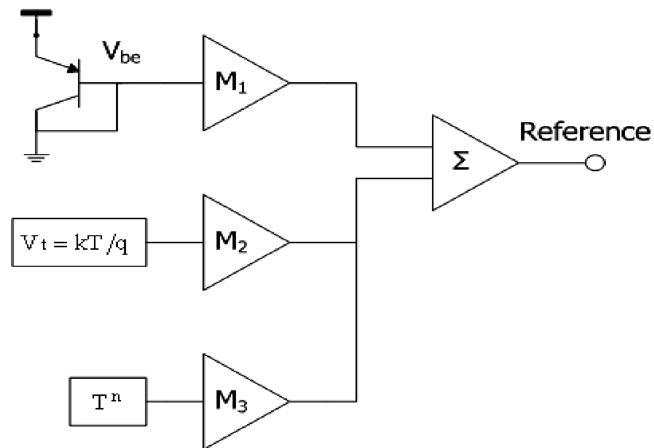


Figure 7.3 The principle of the high order bandgap reference.

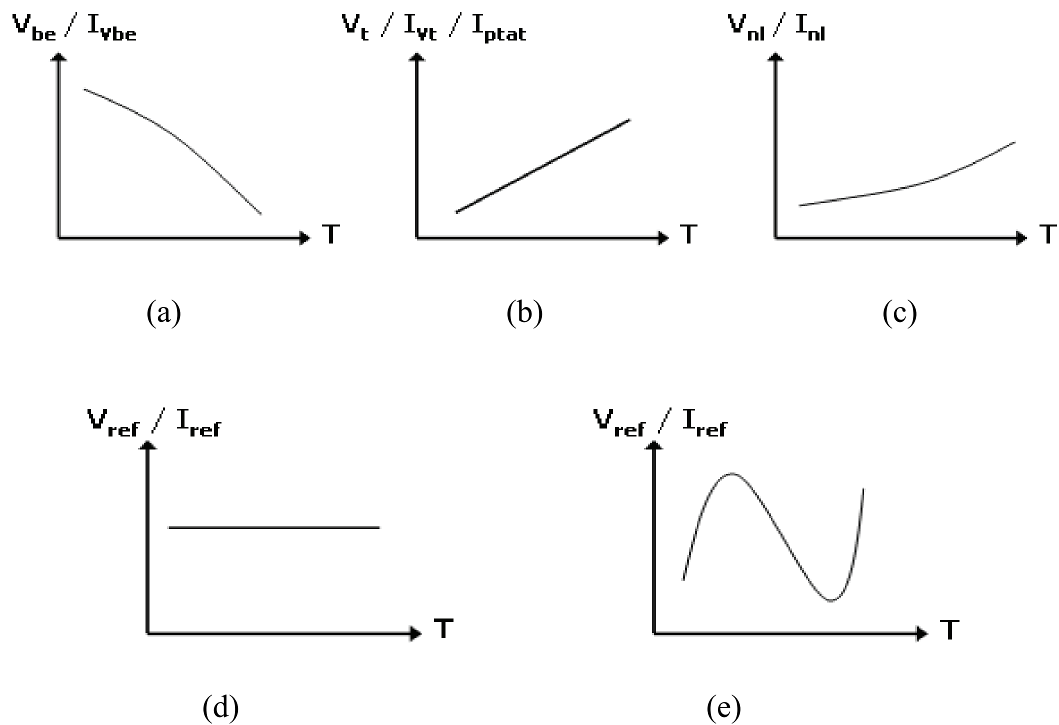


Figure 7.4 Temperature dependence of the different bandgap reference (high order) components. (a) V_{be} versus temperature, (b) V_t versus temperature, (c) V_{nl}/I_{nl} versus temperature, (d) reference voltage/current versus temperature (ideal), and (e) reference voltage/current versus temperature (actual).

M_1 multiplier is applied to set V_{be} to a correct value for optimization. The multiplication can be done by using different area ratios of the transistors. The resistor ratio multiplier in the current mirror can be employed as well. Thus, the reference voltage in (7.3) can be modified to set for a high order compensated reference as

$$V_{ref} = M_1 V_{be} + M_2 V_t + M_3 T^n \quad (7.4)$$

The compensation can be done with respect to the voltages or currents. Thus, the corresponding graphs (not to the scale) for the V_{be}/I_{Vbe}, V_t/I_{PTAT}, V_{NL}/I_{NL} and V_{ref}/I_{ref} are shown in Fig. 7.4. Figure 7.2(d) is the expected graph for the ideal reference. But, practically it looks like the shape shown in Fig. 7.4(e). In this case the temperature coefficient for the reference is extremely small.

7.1.4 The High Order Curvature Corrected Bandgap Reference Output Stage

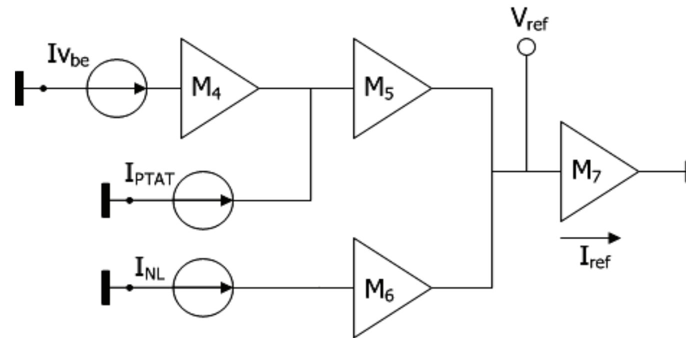


Figure 7.5 The output stage of the high order bandgap reference.

Figure 7.5 represents the output stage of the bandgap reference. Three currents, I_{Vbe}, I_{PTAT}, and I_{NL}, are added through a common branch M_7. The reference current and voltage are shown in the figure. The multipliers M_4, M_5, and M_6 may or may not be related to M_1, M_2, and M_3 of Fig. 7.3. Each of M_4, M_5, and M_6 is one in the proposed designs. Added currents or voltages will give a constant temperature independent

reference. The two temperature dependent negative terms in $V_{be}(T)$ will be compensated by the positive linear and nonlinear temperature dependent currents [34].

7.2 The High Order Curvature Corrected Bandgap Reference Design Procedure

It appears that the compensation can be done by generating the currents to establish the reference voltage or current. In this case, current compensation technique is more effective and flexible when considering high order curvature correction. The current compensation technique will generate three currents, i) a base emitter current, I_{Vbe}, ii) a PTAT current, I_{PTAT}, and iii) a nonlinear current, I_{NL} as shown in Fig. 7.5. This is appropriate for low voltage applications. This topology can accommodate a wide range of reference voltage or current [35]. The generations of the current components are described in the following sections.

7.2.1 The Generation of the Base Emitter Current (I_{Vbe}) Current

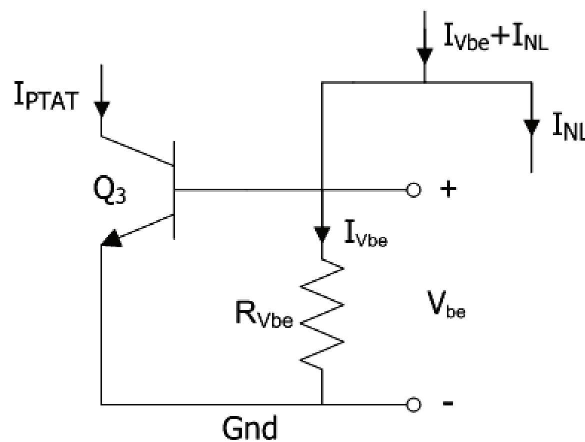


Figure 7.6 Generation of the Base Emitter Current (I_{Vbe}).

A current I_{Vbe}, proportional to V_{be}, can be generated by placing a resistor R_{Vbe} across the base and emitter of bipolar transistor [34]. The corresponding current $I_{Vbe}(T)$

can be expressed as

$$I_{Vbe}(T) \cong \frac{V_{be}(T)}{R_{Vbe}} = \frac{E_g(0)}{R_{Vbe}} - \frac{1}{R_{Vbe}}\{E_g(0) - V_{be}(T_0)\}\frac{T}{T_0} - \frac{1}{R_{Vbe}}(XIS - n) \times V_t(T)T \times \ln\left(\frac{T}{T_0}\right) \tag{7.5}$$

The transistor Q_3 needs to be biased in the forward active region by a pre-specified current. In the proposed design, the collector current for the Q_3 is the PTAT current. The two temperature dependent terms in (7.5) will be compensated by generating the proportional to the absolute temperature (PTAT) current, I_{PTAT} and the nonlinear (NL) current, I_{NL}. Thus, after compensation, the summation of the three currents I_{Vbe}, I_{PTAT}, and I_{NL} must be constant and equivalent to the only constant term, $E_g(0)/R_{Vbe}$ of (7.5). This can be written as,

$$I_{Vbe} + I_{PTAT} + I_{NL} = \text{constant} = \frac{E_g(0)}{R_{Vbe}} \tag{7.6}$$

The simulation of the $I_{Vbe}(T)$ versus temperature is shown in Fig. 7.7.

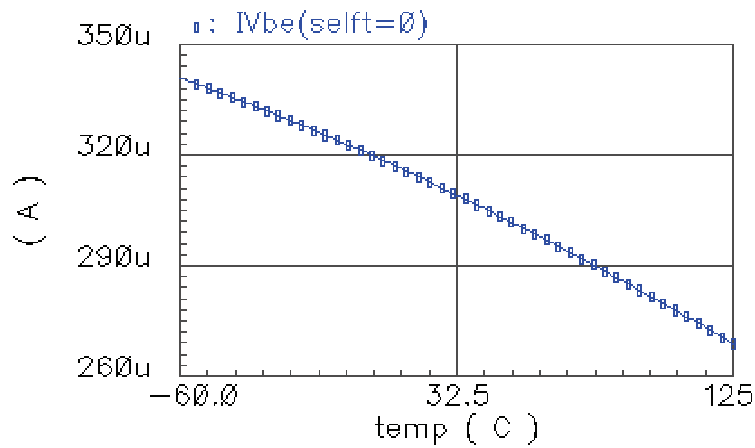


Figure 7.7 Simulation of the Base Emitter Current (I_{Vbe}).

7.2.2 The Generation of the PTAT Voltage (V_{PTAT}) and Current (I_{PTAT})

The PTAT current generates a current that is proportional to the absolute temperature. In principle this can be done in one basic way, but with several different circuit configurations depending on the method used for the bandgap reference design.

7.2.2.1 Generation of the PTAT Voltage

To generate a PTAT voltage, the transistors Q_1 and Q_2 need to be connected as shown in Fig. 7.8 [21]. The transistor Q_1 carries a current of nI with saturation current I_s. The other transistor Q_2 carries a current of I with saturation current mI_s. Therefore, the transistor Q_2 has an area factor of m times that of transistor Q_1.

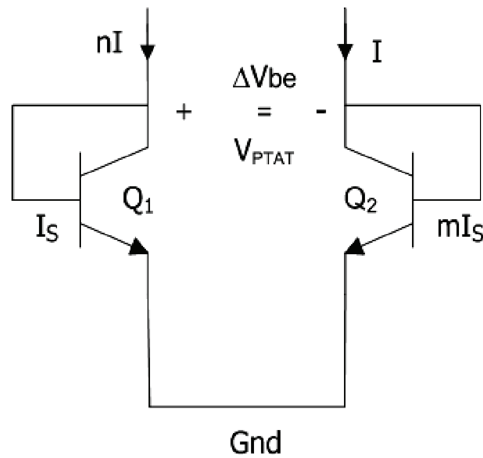


Figure 7.8 Generation of the PTAT voltage.

Neglecting the base current it can be written that,

$$\Delta V_{be} = V_t \ln (nI/I_s) - V_t \ln (I/mI_s)$$

$$= V_t \ln (nm) \quad (7.7)$$

Thus, ΔV_{be} in (7.7) is a PTAT voltage and can be differentiated to see the slope.

$$\frac{\partial \Delta Vbe}{\partial T} = \frac{k}{q} \ln (nm) \tag{7.8}$$

7.2.2.2 Generation of the PTAT Current

By using a similar circuit configuration (Fig. 7.8), a resistance R_{PTAT} can be added to the emitter of Q_2 (Fig. 7.9) to generate the PTAT current. Here, the current I of Fig. 7.8 is replaced by I_{PTAT} in Fig. 7.9. Now, a loop analysis gives,

$$\Delta V_{BE} = I_{PTAT} R_{PTAT} = V_t \ln (nI_{PTAT}/I_s) - V_t \ln (I_{PTAT}/mI_s)$$

$$= V_t \ln (nm)$$

$$I_{PTAT} = \frac{1}{R_{PTAT}} \left\{ \frac{K}{q} \ln(nm) \right\} T \tag{7.9}$$

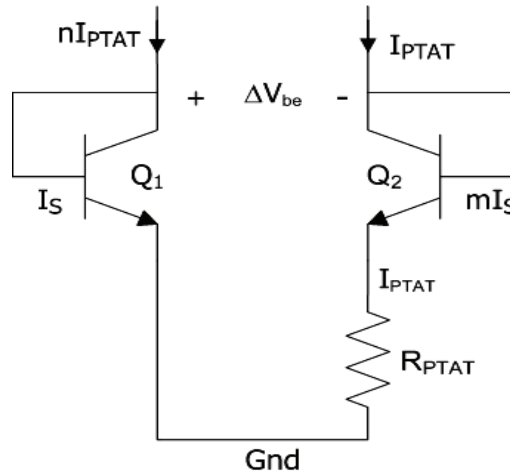


Figure 7.9 Generation of the PTAT Current.

Equation (7.9) shows the required temperature proportionality of the PTAT current. The values of the n and m can be set to the required value. In the proposed design n = 1 and

m = 4 are used. The value of the I_{PTAT} is specified in the design. The simulation of the PTAT current is shown in Fig. 10.

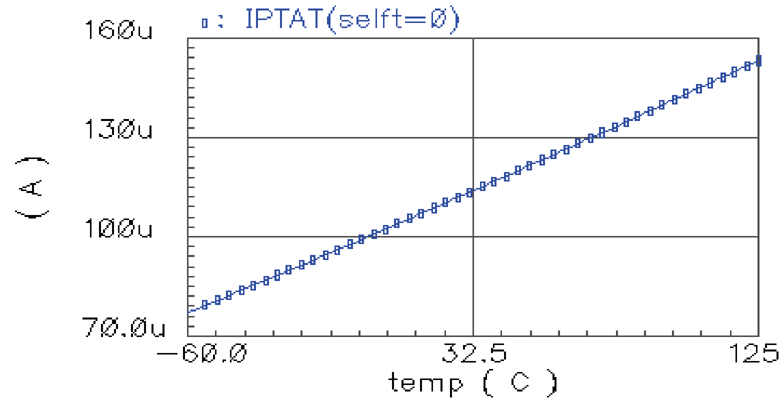


Figure 7.10 Simulation of the PTAT Current.

7.2.3 The Generation of the Nonlinear Current (I_{NL})

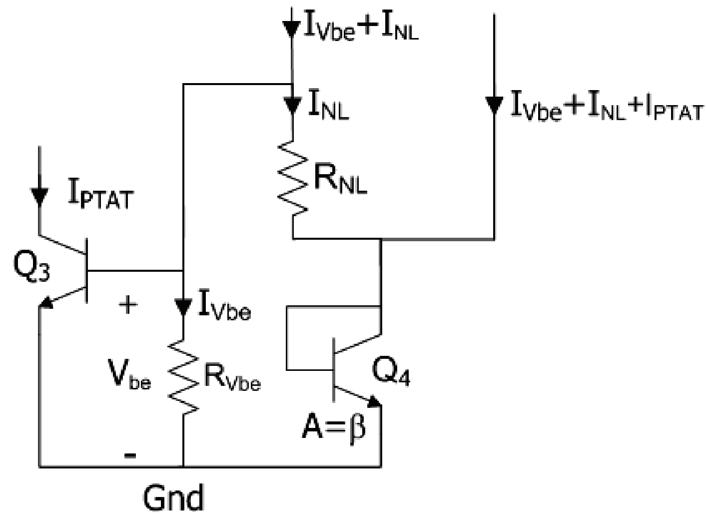


Figure 7.11 Generation of the nonlinear current.

The generation of the nonlinear current for the curvature correction in the bandgap reference can be done by using the circuit configuration shown in Fig. 7.11 [35].The transistors Q_3, Q_4, and a resistor R_{NL} comprise a loop that will generate the nonlinear (logarithmic) current. The transistor Q_4 has an area factor of β compared to the device Q_3. The transistor Q_3 carries a current of I_{PTAT} with saturation current I_s. The other transistor Q_4 carries a current of $(I_{Vbe}+I_{PTAT}+2I_{NL})$ with saturation current βI_s. Due to the inequalities in currents, the base emitter voltages of Q_3 and Q_4 are different. A voltage equivalent to the difference of these two base emitter voltages is the same as the drop across R_{NL}. A loop voltage equation can be written using Kirchhoff's voltage law (KVL) to find the value of R_{NL} and I_{NL}.

$$\Delta V_{be} = V_{be3} - V_{be4} = I_{NL} . R_{NL}$$

So, the nonlinear current can be calculated as

$$I_{NL} = \frac{1}{R_{NL}}\left(V_{be3} - V_{be4}\right)$$

$$= \frac{1}{R_{NL}}\left(V_t \ln \frac{I_{PTAT}}{I_s} - V_t \ln \frac{I_{Vbe} + I_{PTAT} + 2I_{NL}}{\beta I_s}\right)$$

$$I_{NL} = \frac{1}{R_{NL}}\left(V_t \ln \frac{\beta I_{PTAT}}{I_{Vbe} + I_{PTAT} + 2I_{NL}}\right)$$

$$= \frac{1}{R_{NL}} \frac{k}{q} T\left(\ln \frac{\beta I_{PTAT}}{E_g(0)/R_{Vbe} + I_{NL}}\right) \tag{7.10}$$

where, $I_{Vbe} + I_{PTAT} + I_{NL} = E_g(0)/R_{Vbe}$ from (7.6). The expression in (7.10) is the nonlinear current that will compensate the 3rd term of (7.5). The simulation of the nonlinear current is shown in Fig. 7.12.

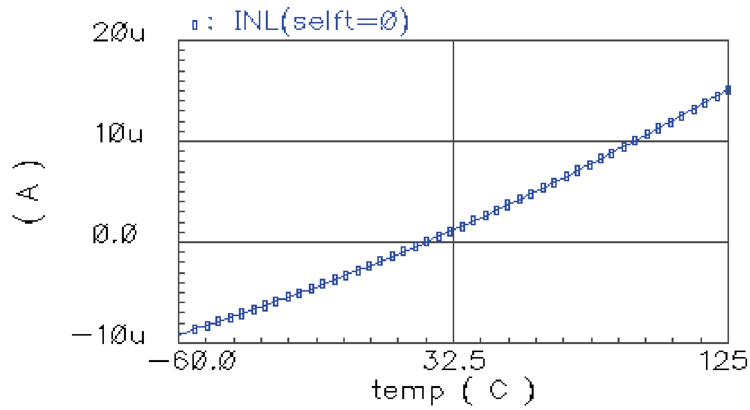


Figure 7.12 Simulation of the Nonlinear Current.

7.2.4 The Design of the High order Bandgap Reference

It is observed that, the curvature correction of a high-order bandgap reference can be practically generated through the use of different temperature-dependent currents and a diode voltage loop [34]. The designed high order curvature corrected bandgap reference is shown in Fig. 7.13. The description of the design as follows.

- The transistors Q_1 and Q_2 generate the PTAT current. Q_2 has an area factor of 4 times that of Q_1. The transistors Q_7 – Q_{10} and Q_{15} bias Q_1 and Q_2 in the forward active region. They use emitter degenerated current mirror topology with a buffer transistor Q_{15}.
- The PTAT current is mirrored to the rest of the circuit (as required) by using the transistors Q_{11}, Q_{12}, and Q_{14}.
- The device Q_3 is for the generation of the base emitter current by using the resistor R_{Vbe}. This is biased with the PTAT current. The transistor Q_{20} make sure that Q_3 is in the active region.

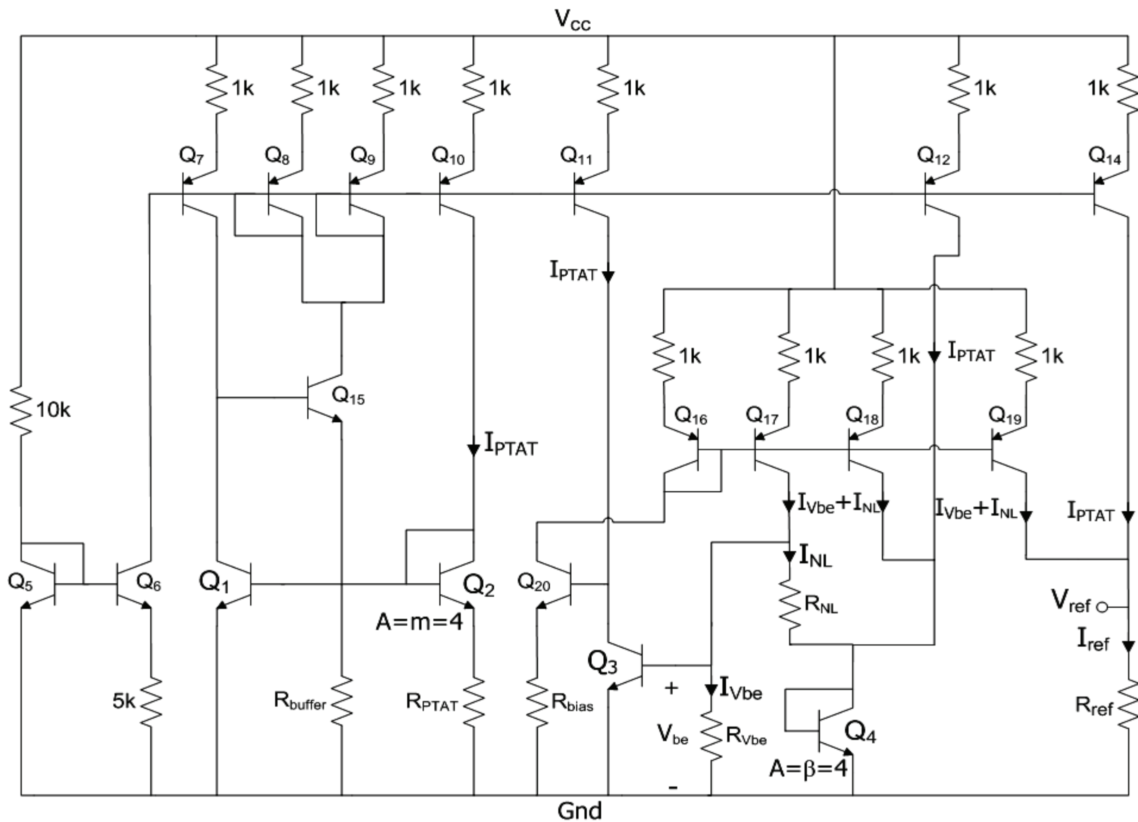


Figure 7.13 The design of the high order curvature corrected bandgap reference [34].

- The transistors $Q_{16} - Q_{19}$ produce $I_{Vbe} + I_{NL}$ to the circuit.
- The loop composed of Q_3, Q_4, and R_{NL} produces the nonlinear current. The device Q_4 has an area factor of 4 times that of Q_3 as required by the design.
- In the output stage, Q_{19} and Q_{14} supply the currents $I_{Vbe} + I_{NL}$ and I_{PTAT} respectively to the resistor, R_{ref}. The reference voltage and current are V_{ref} and I_{ref} respectively.
- The devices Q_5 and Q_6 are work together as a start-up circuit.
- The Vcc used for the design is 5 V.

The compensation is done as the following way. The correction procedures find the values of the R_{PTAT}, R_{Vbe}, R_{NL}, and the area factors, m and β for Q_2 and Q_4 respectively.

7.2.4.1 Finding R_{PTAT}

The I_{PTAT} current is generated using the loop comprised of Q_1, Q_2, and R_{PTAT} (Fig. 7.13) [35]. The method described in 7.2.2.1 can be used to find the R_{PTAT}. Thus, an equation, (7.11) can be written in this loop using KVL.

$$V_{be1} = V_{be2} + I_{PTAT} . R_{PTAT} \qquad (7.11)$$

By using (7.11), R_{PTAT} can be solved as

$$R_{PTAT} = \frac{1}{I_{PTAT}} V_t \left\{ \ln\left(\frac{I_{c1}}{I_{s1}} \frac{m\, I_{s2}}{I_{c2}} \right) \right\} \qquad (7.12)$$

where, V_t is the thermal voltage, I_{c1}, I_{s1} and I_{c2}, I_{s2} are the collector and saturation currents of Q_1 and Q_2 respectively, and m is the area multiplying factor of Q_2. I_{PTAT} needs to be set by design specification. I_{PTAT} can be controlled by R_{PTAT} and m.

In this case, I_{PTAT} = known from specification, m = 4 (chosen), T = 27 ºC, $I_{c1} = I_{c2}$, $I_{s1} = I_{s2} = I_s$. Therefore using (7.12) R_{PTAT} can be solved as

$$R_{PTAT} = \frac{0.025852 * \ln 4}{I_{PTAT}} \qquad (7.13)$$

7.2.4.2 Finding R_{Vbe} and R_{NL} and the High order Curvature Correction

The first order temperature dependent term (2nd term) in (7.5) is compensated by the current which is proportional to the absolute temperature (I_{PTAT}) [35]. Thus the I_{PTAT} current must be equal to the 2nd term in the I_{Vbe} equation shown in (7.5). This will

establish the 1st order temperature compensation. The value of the R_{Vbe} can be solved by equating the I_{PTAT} value and the second term of the I_{Vbe} equation.

$$I_{PTAT} \cong \frac{1}{R_{Vbe}} \{E_g(0) - V_{be}(T_0)\} \frac{T}{T_0} \tag{7.14}$$

$$R_{Vbe} \cong \frac{1}{I_{PTAT}} \{E_g(0) - V_{be}(T_0)\} \frac{T}{T_0} \tag{7.15}$$

Therefore, R_{Vbe} can be evaluated using (7.15). Here, I_{PTAT} is known from the specification, $E_g(0)$ is known from the model parameters, $V_{be}(T_0)$ is the base emitter voltage at the reference temperature T_0, and T is the room temperature.

The higher order nonlinear terms can be compensated by a nonlinear current (I_{NL}). The generation of the nonlinear current using the loop comprised of Q_3, R_{NL}, and Q_4 (Fig. 7.13) is described in section 7.2.2. Hence by equating (7.10) and the nonlinear term (3rd term) of (7.5), R_{NL} and β can be found.

$$I_{NL} = \frac{1}{R_{NL}} \frac{k}{q} T \left\{ \ln \frac{\beta I_{PTAT}}{E_g(0)/R_{Vbe} + I_{NL}} \right\} = \frac{1}{R_{Vbe}} (XIS - n) \times V_t(T) \times \ln\left(\frac{T}{T_0}\right) \tag{7.16}$$

The solution (7.16) provides,

$$R_{NL} = \frac{R_{Vbe}}{(XIS - n)} \tag{7.17}$$

$$\beta = \frac{T}{T_0} \frac{E_g(0)/R_{Vbe}}{I_{PTAT}} = 4 \tag{7.18}$$

where, $E_g(0) >> I_{NL}$. Here, XIS is known from the model, n=1, while R_{Vbe} is already extracted. Therefore, the value of the resistor R_{NL} and the area factor (β) of Q_4 are evaluated.

7.2.4.3 Finding the Reference Voltage, V_{ref}

After compensation, as shown in (7.6), the summation of the currents is the temperature independent reference current and the reference voltage can be generated by letting the currents flow through a reference resistance, R_{ref} (Fig. 7.13). In both the current and voltage reference cases, optimization can be done by varying R_{PTAT}, R_{Vbe}, or R_{NL}. Thus, the reference voltage can be evaluated as

$$V_{ref} = \frac{Eg(0)}{R_{Vbe}} R_{ref} \qquad (7.19)$$

It is observed that, by varying R_{Vbe}, R_{PTAT} and R_{NL}, the compensation can be done. The reference voltage, V_{ref} can be changed by varying R_{ref}. There are two sets of different characteristics shown in the following section, i) one for the 1.25 V reference and ii) the other for the 200 mV reference.

7.3 Computer Simulations

Cadence Spectre simulations have been done using the DIBJTs of National Semiconductor's VIP10 and VIP11 processes. Figs. 7.15 to 7.20 present several different characteristics of the designed bandgap reference.

7.3.1 The Simulations of the Current Components, I_{Vbe}, I_{PTAT}, and I_{NL}

The temperature characteristics of the three principal currents of the design are shown in Fig. 7.14. It can be observed from the figure that, I_{Vbe} and I_{NL} have nonlinear temperature characteristics and I_{PTAT} has linear temperature characteristics. These characteristics were desirable in high order bandgap reference design.

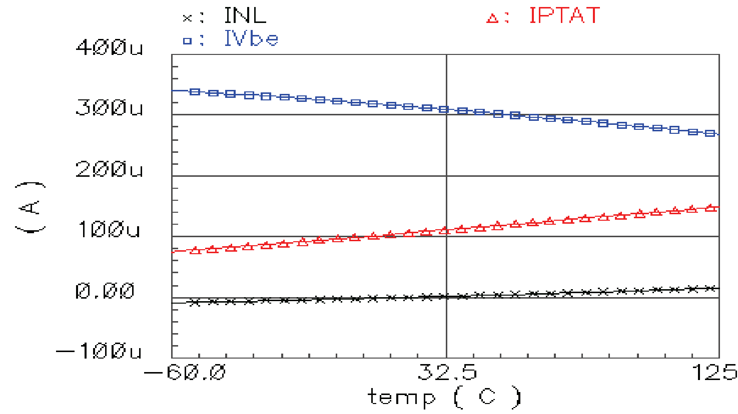


Figure 7.14 Different current components of the proposed bandgap design.

7.3.2 The Simulations of the Reference Voltage, V_{ref} with Temperature

The temperature coefficient of the reference voltage can be found using (7.20).

$$TC_F(V_{ref})[ppm/°C] = \frac{1}{V_{ref}(27\,°C)}\frac{\partial V_{ref}}{\partial T} = \frac{V_{ref}(T_2) - V_{ref}(T_1)}{V_{ref}(27\,°C)(T_2 - T_1)}10^6 \qquad (7.20)$$

where, $TC_F(V_{ref})$ is the temperature co-efficient of the reference voltage in parts per million per degree centigrade (ppm/ºC), $V_{ref}(T_2)$ is the reference voltage at the maximum temperature T_2, $V_{ref}(T_1)$ is the reference voltage at the minimum temperature T_1, and V_{ref} (27 ºC) is the reference voltage at room temperature (27 ºC).

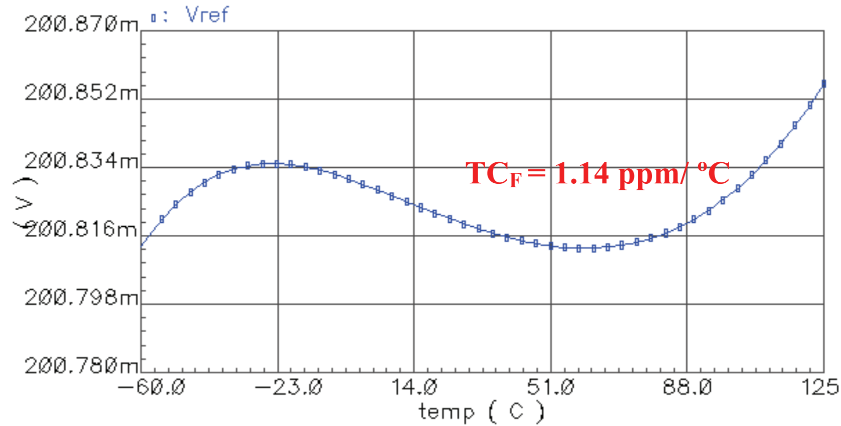


Figure 7.15 Simulation of 200 mV reference of the proposed bandgap design.

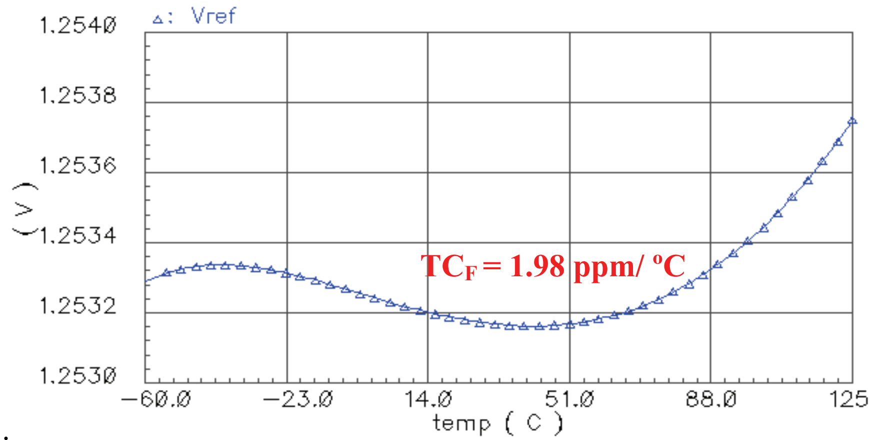


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Figure 7.16 Simulation of 1.25V reference of the proposed bandgap design.

The temperature coefficients and the temperature drifts of the reference are shown in Table 7.1.

Table 7.1 Temperature coefficients for the reference voltage

	1.25 V Reference	200 mV Reference
TC_F	1.98 ppm/ ºC	1.14 ppm/ ºC
Temperature Drift	-60 ºC to 125 ºC	-60 ºC to 125 ºC

7.3.3 The Simulations of the Reference Voltage, V_{ref} with Time (Transient Simulation)

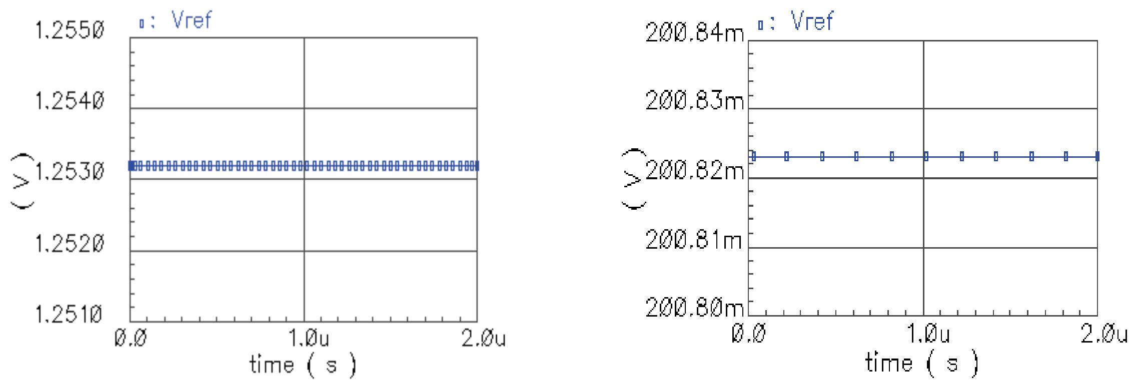

Figure 7.17 Transient simulation of the bandgap reference.

The simulation plot shown in Fig. 7.17 demonstrates the start up problem in the design. Transient simulation was done between 0 to 2 μs to achieve these plots. The plot does not show any start up problem.

7.3.4 The Simulation for the Line Regulation of the Reference Voltage, V_{ref}

The line regulation is another very important property of a bandgap reference. This describes the change in the reference voltage due to a specified change in input supply voltage. The reference voltage should be stable when the supply voltage varies. Figure 7.18 shows the line regulation plot at three different temperatures. The line regulation can be calculated as follows

$$\text{Line regulation} = \frac{V_{ref}(V_{cc,\,max}) - V_{ref}(V_{cc,\,min})}{V_{cc,\,max} - V_{cc,\,min}} \ V/V \qquad (7.21)$$

where, $V_{cc,max}$ and $V_{cc,min}$ refer to the maximum and minimum specified supply.

The line regulation and the working supply voltage range for the designed reference is shown in table 7.2.

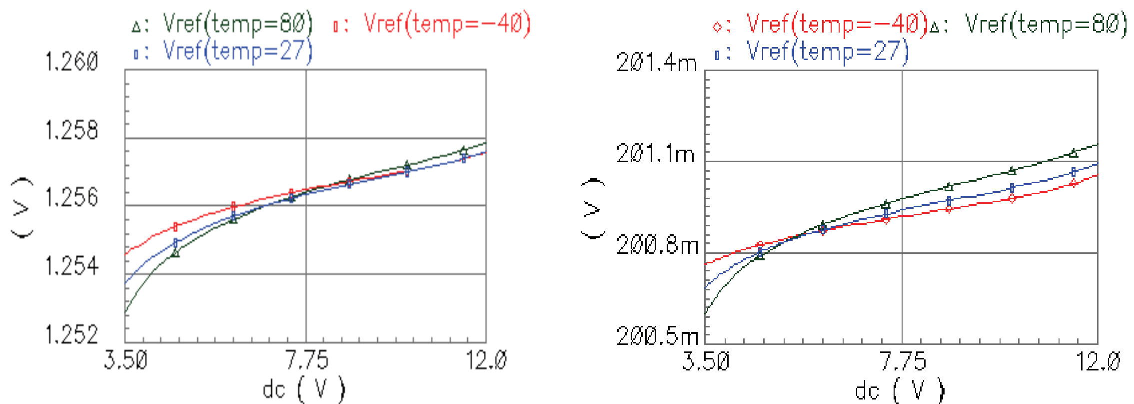

Figure 7.18 Line regulation simulation of the bandgap reference.

Table 7.2 Line regulation and supply voltage range for the reference

	1.25 V Reference	200 mV Reference
Line Regulation	0.59 mV/V	70.6 μV/V
Supply Voltage Range	3.5 V – 12 V	3.5 V – 12 V
Temperature drift	-60 ºC to 125 ºC	-60 ºC to 125 ºC

7.3.5 The Noise Simulation of the Reference Voltage, V_{ref}

The noise simulation of the reference appears very low for the design. The noise simulation has been done for 1 to 10 Hz. This is shown in Fig. 7.19. The noise shown in the figure is at the reference node.

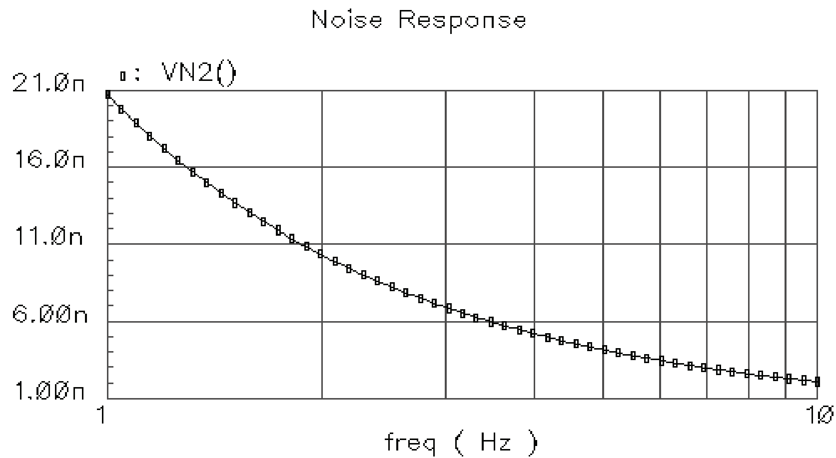

Figure 7.19 Noise simulation of the bandgap reference.

7.4 Self-heating Effect on Bandgap Reference

The self-heating on the bandgap reference design with the dielectrically isolated device is significant. Temperature compensation would not be perfect if self-heating is not considered for the high precision reference. The self-heating affected error

correction in the bandgap reference can be done by analyzing and simulating the three current components (I_{Vbe}, I_{PTAT} and I_{NL}) with and without self-heating. Then by varying and optimizing the three resistor elements (R_{PTAT}, R_{Vbe} and R_{NL}) in Fig. 7.13, optimum high order curvature corrected reference design is possible. The following section analyzes the current components while considering the self-heating effect.

7.4.1 Self-heating on Base Emitter Voltage (V_{BE}) / current (I_{Vbe})

The base emitter voltage and the self-heating relation are expressed in (6.10), (7.2), and Fig.6.4. It is found that V_{be} is reduced by the self-heating effect due to temperature increment by the thermal power and thermal resistance ($\Delta T_{SH} = R_{th} \cdot P_{th}$). I_{Vbe} is produced from V_{be} by dividing by R_{Vbe}. So, I_{Vbe} is reduced due to the self-heating as well. This is shown in Fig. 7.20. The equations (7.22) and (7.23) are written to show the relation between I_{Vbe} and self-heat affected temperature rise by using (7.1.1) and (7.1.2).

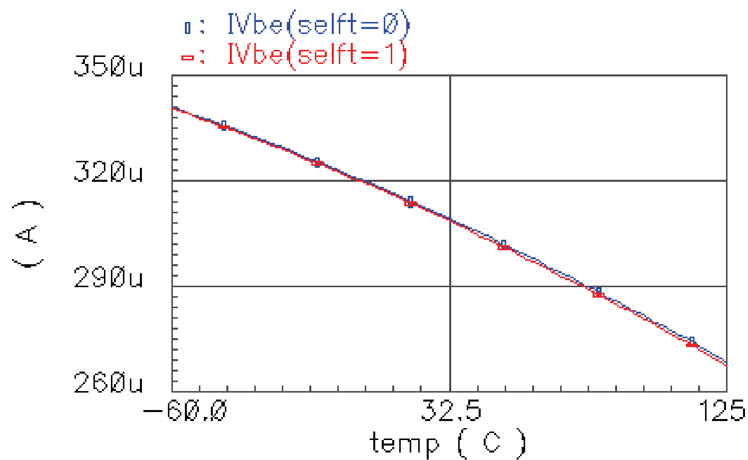

Figure 7.20 Simulation of the Base Emitter Current (I_{Vbe}) with and without self-heating effect.

$$I_{Vbe}(T) \cong \frac{1}{R_{Vbe}} E_g(0) - \frac{1}{R_{Vbe}} \{E_g(0) - V_{be}(T_0)\} \frac{T + \Delta t}{T_0} - \frac{1}{R_{Vbe}} (XIS - n) \times V_t (T + \Delta t) \times \ln\left(\frac{T + \Delta t}{T_0}\right) \quad (7.22)$$

$$I_{Vbe}(T + \Delta t) = \frac{1}{R_{Vbe}} E_g(0) - \frac{1}{R_{Vbe}} \{E_g(0) - V_{be}(T_0)\} \frac{T + \Delta t}{T_0} - \frac{1}{R_{Vbe}} (XIS - n) \times \frac{kT_0}{q} \times \left\{\frac{1}{3} - \frac{1}{2} \frac{T + \Delta t}{T_0} + T^2 - \frac{1}{6}\left(\frac{T + \Delta t}{T0}\right)^3\right\} \quad (7.23)$$

7.4.2 Self-heating Effect on the PTAT Current, I_{PTAT}

The self-heating error on the PTAT current source is significant. If δ_{th} is the error between the collector current of Q_2 and Q_1 in Fig. 7.13 due to the thermal effect, then the relation between the I_{c1} and I_{c2} can be expressed as

$$I_{c2} = I_{c1} (1 + \delta_{th}) \quad (7.\ 24)$$

Combining (7.12) and (7.24) gives

$$I_{PTAT - Thermal - Error} = \frac{1}{R_{PTAT}} V_t \left\{ \ln\left(\frac{I_{c1}}{I_{s1}} \frac{m\, I_{s2}}{I_{c1}(1 + \delta_{th})} \right) \right\}$$

$$I_{PTAT - Thermal - Error} = \frac{V_t}{R_{PTAT}} \ln\left\{ \frac{m}{(1 + \delta_{th})} \right\}$$

$$I_{PTAT - Thermal - Error} = \frac{V_t}{R_{PTAT}} \ln m - \frac{V_t}{R_{PTAT}} \ln (1 + \delta_{th})$$

$$I_{PTAT - Thermal - Error} \approx \frac{V_t}{R_{PTAT}} \ln m - \frac{V_t}{R_{PTAT}} \delta_{th} \quad (7.25)$$

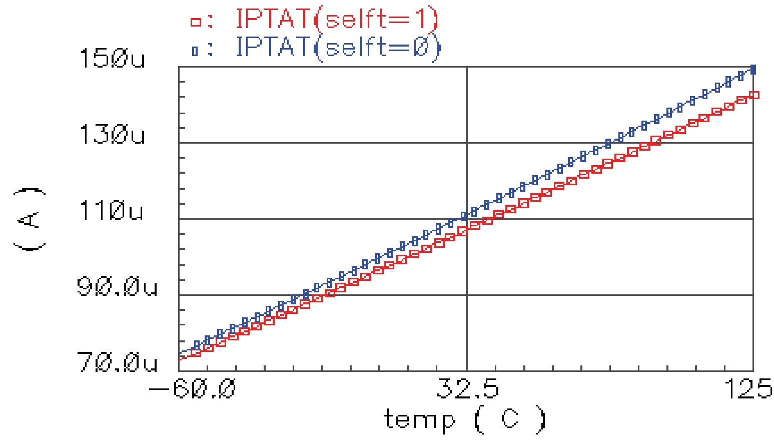

Figure 7.21 Simulation of the PTAT Current (I_{PTAT}) with and without self-heating effect.

So, if the thermal error, δ_{th} in (7.25) becomes zero, then the value of the PTAT current would be ideal. But the PTAT current may still have the error due to the finite output resistances of the transistors. The value of the δ_{th} can be evaluated by the method discussed in chapter 5 (section 5.2).

The error due to the self-heating effect on the PTAT current can be reduced or removed by changing the value of the of the R_{PTAT}. This error can be minimized by reducing the value of the thermal resistance, R_{th} as well. The self-heating effect on the PTAT current is shown in Fig. 7.21.

7.4.3 Self-heating Effect on the Nonlinear Current, I_{NL}

The nonlinear current found in (7.10) can be re-written (when $I_{NL} << E_g(0)/R_{Vbe}$) to see the self-heating effect.

$$I_{NL} \cong \frac{1}{R_{NL}} \frac{k}{q} T \left(\ln \frac{\beta I_{PTAT}}{E_g(0)/R_{Vbe}} \right) \tag{7.26}$$

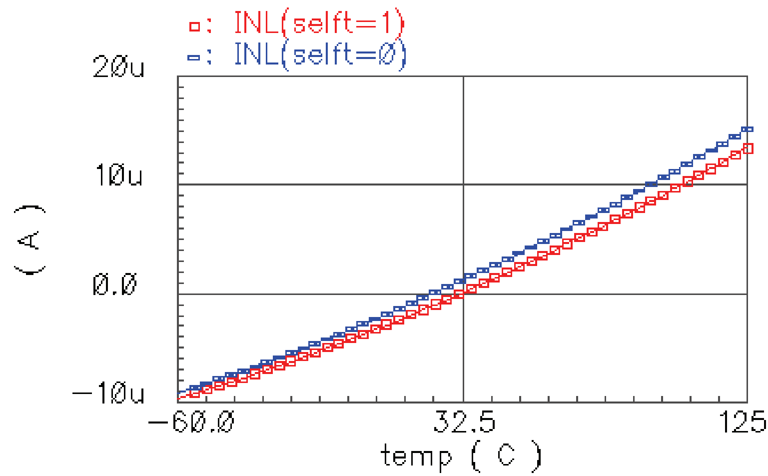

Figure 7.22 Simulation of the nonlinear current (I_{NL}) with and without self-heating effect.

It is seen in section 7.3.2 that IPTAT is reduced by the self-heating effect. Equation (7.26) shows the logarithmic proportionality of the INL on IPTAT. Therefore, INL is reduced due to self-heating as well. The simulation is shown in Fig. 7.22.

7.4.4 Self-heating Effect on the Bandgap Reference Current/Voltage

The self-heating effect on the reference voltage is shown in table 7.3. It appears that, without compensation of the self-heating effect, the temperature co-efficients become worsen.

Table 7.3 Temperature coefficients for the reference with self-heating effect

	1.25 V Reference	200 mV Reference	Temperature drift
TC_F (selft=0)	1.98 ppm/ ºC	1.14 ppm/ ºC	-60 ºC to 125 ºC
TC_F (selft=1)	88 ppm/ ºC	81 ppm/ ºC	

7.5 Design of Bandgap Reference with Different PTAT Current Source

Another bandgap reference is designed with a different PTAT current source. This design followed exactly the same topology as discussed in sections 7.2 and 7.3. This uses a PTAT current source made by PNP devices. In addition this is designed for very low voltage and low current applications. This uses only 1.5 V as a supply voltage with fewer transistors than the design shown in Fig. 7.13. The area factor β (Q_4) is modified to 3 according to the design requirement. The proposed design is shown in Fig. 7.23 [34].

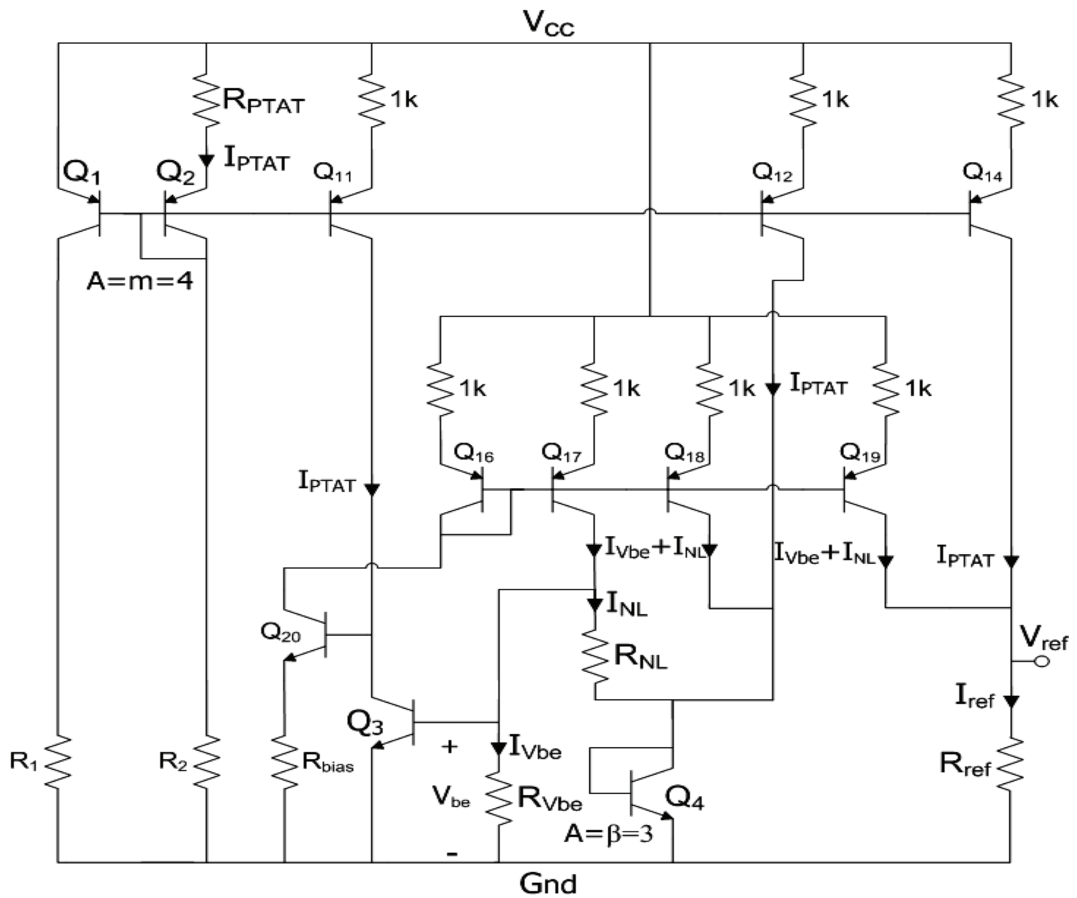

Figure 7.23 Bandgap reference with different PTAT current source (fundamental topology is same as Fig. 7.13).

The temperature coefficients for this design are found to be 2.87 ppm/ºC in the temperature range between -25ºC and 125ºC and 10.144 ppm/ºC in the temperature range between -50ºC and 250ºC without considering self-heating effect.

The design procedure and self-heating effect analyses and discussions proved that the self-heating effect can be minimized by optimizing the resistors R_{Vbe}, R_{PTAT}, and R_{NL}. This is because the currents are controlled by these three resistances. The optimization may include changing the area factor of m (Q_2) and β (Q_4). The self-heating needs to be turned on during the optimization. The parametric analyses have been done using Cadence to optimize the self-heating effect and to achieve minimum temperature coefficient for the reference. It is found that with self-heating (after compensation) the temperature coefficient is 11.17 ppm/ºC between -50 ºC to 250 ºC.

The optimized simulations results for this design including self-heating effect are shown in Figs. 7.24 and 7.25.

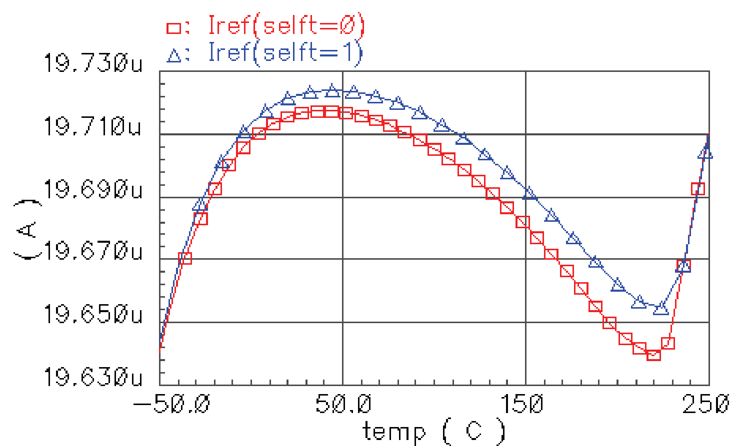

Figure 7.24 Bandgap reference (Fig. 7.23) current at a supply voltage of 1.5 V.

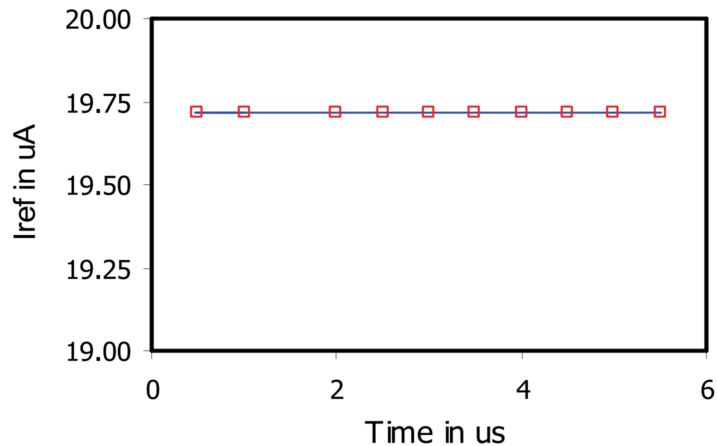

Figure 7.25 Transient simulation of the bandgap reference circuit (Fig. 7.23).

7.6 Fabrication and Measurement

7.6.1 Layout and Fabrication

The design shown in Fig. 7.13 is fabricated. In the design (Fig. 7.13), there are two of the transistors Q_2 (in PTAT block) and Q_4 (in nonlinear current generator block) have the area factor more than one. Thus, multiple transistors are used in parallel to achieve the required higher saturation current or the required area factor. So that, each of the PTAT (Q_2) and the nonlinear (Q_4) blocks uses four transistors in parallel. In the layout, there are several internal test ports have been added to measure and verify the different current elements or voltages. These include the currents I_{Vbe}, I_{PTAT}, I_{NL} etc. To test more points, more external connections are needed. Consequently, a 14 pin dual inline package (DIP) chip is fabricated with the National Semiconductor's VIP10 process with the dielectrically isolated devices. But only 12 pins are used for the

measurement. The device name is UTA198. The layout of the bandgap reference is shown in Fig. 7.26.

To measure an accurate temperature of the chip, a reverse Gummel (RG) connected bipolar transistor is fabricated on-chip with the design. This can be done with a forward Gummel (FG) connected bipolar device as well. The detailed procedures for the temperature measurement with FG or RG connected bipolar transistor are presented in chapter 2. This required writing a transform function and plotting using ICCAP.

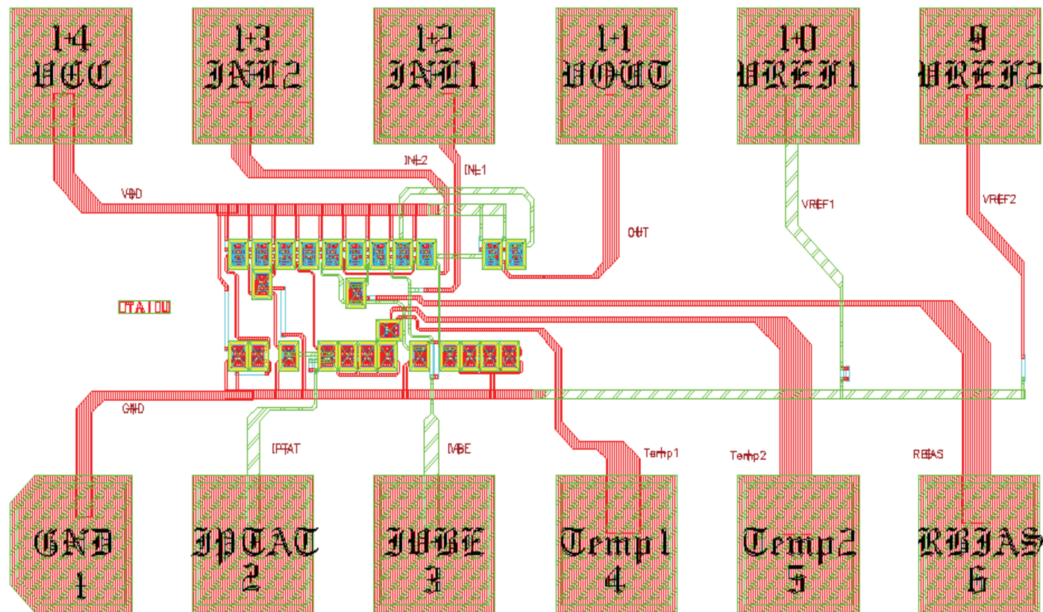

Figure 7.26 Layout of the fabricated bandgap reference (UTA198).

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7.6.2 Measurement for Bandgap Reference Voltage versus Temperature

The measurement setup for the reference voltage measurement versus temperature is shown in Fig. 7.27. The HP4142B Modular DC Source/Monitor and ICCAP interfaced evaluation system are used for the measurements [20], [22].

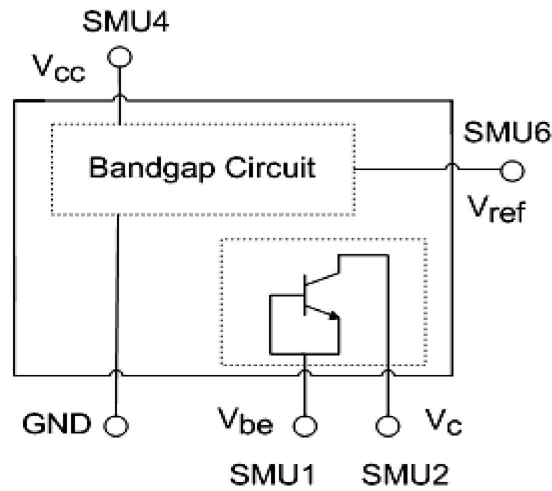

Figure 7.27 Reference voltage and temperature measurement setup.

For the temperature measurement of the chip a reverse Gummel connected bipolar device is fabricated inside the die. For the reference voltage measurement, the 4 SMUs (source monitoring unit) and the ground of the HP4142 are used. The four pins V_{cc}, V_{ref}, V_c and V_{be} are connected to the SMU4, SMU6, SMU2, and SMU1 respectively. The ground of the chip is connected to the ground of the measurement device. The input-output set-up in ICCAP is shown in Fig. 7.28 [20].

Input:	Vcc
Mode:	V
+ Node:	C1
- Node:	GROUND
Unit:	SMU4
Compliance:	50.00m
Sweep Type:	CON
Value:	5.000

Input:	Iref
Mode:	I
To Node:	M
From Node:	GROUND
Unit:	SMU6
Compliance:	50.00m
Sweep Type:	CON
Value:	0.000

Input:	Vbe
Mode:	V
+ Node:	BE
- Node:	GROUND
Unit:	SMU2
Compliance:	20.00m
Sweep Type:	CON
Value:	0.000

Input:	Vc
Mode:	V
+ Node:	C
- Node:	GROUND
Unit:	SMU1
Compliance:	20.00m
Sweep Type:	LIN
Sweep Order:	1
Start:	-900.0m
Stop:	-300.0m
# of Points:	61
Step Size:	10.00m

Output:	Icc
Mode:	I
To Node:	C1
From Node:	GROUND
Unit:	SMU4
Type:	M

Output:	Vref
Mode:	V
+ Node:	M
- Node:	GROUND
Unit:	SMU6
Type:	M

Output:	Ibe
Mode:	V
+ Node:	BE
- Node:	GROUND
Unit:	SMU2
Type:	M

Output:	Ic
Mode:	V
+ Node:	C
- Node:	GROUND
Unit:	SMU1
Type:	M

Figure 7.28 ICCAP input-output set-ups for the reference voltage and temperature measurement.

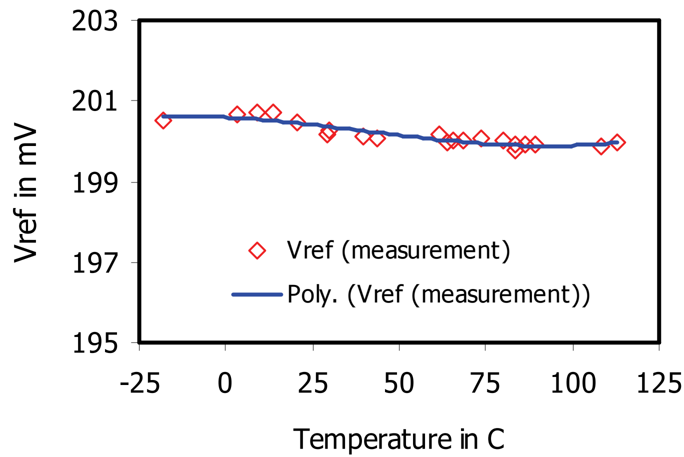

Figure 7.29 The reference voltage measurement with a fabricated chip (-18.31 ºC to +113.09 ºC).

The measurement has been done for the 200 mV reference. The measurement result is shown in Fig. 7.29 and table 7.4.

Table 7.4 Measured Temperature coefficients for the bandgap reference

	200 mV Reference
TC_F	19.465 ppm/ ºC
Temperature drift	-18.31 ºC to +113.09 ºC

7.7 The Effect of Temperature Coefficients of the Resistors in the Design

The temperature performance of the bandgap reference can be affected by the temperature coefficient of the resistors, especially for voltage mode topology. But in a current mode topology, for a voltage reference, the resistors' TC does not degrade the performance of the voltage reference circuit as compared to a voltage mode topology [36]. The TC of the resistors is actually canceled [36].

$$V_{ref} = \left(I_{Vbe} + I_{PTAT} + I_{NL}\right) R_{ref}$$

$$V_{ref} = \left(C_x \frac{V_{be}}{Rx} + C_y \frac{V_t}{Ry} + C_z \frac{V_{NL}}{Rz} \right) R_{ref} \tag{7.27}$$

The temperature co-efficient of a resistor can be expressed as

$$R(T) = R(T_r)\left[1 + A(T - T_r) + B(T - T_r)^2\right] \tag{7.28}$$

C_x, C_y, C_z are temperature independent constants. A and B are the linear and the quadratic temperature coefficients. $R(T_r)$ is the resistance at room temperature.

From the V_{ref} equation,

$$V_{ref} = \left\{ \begin{array}{l} C_x \dfrac{V_{be}}{R_x(T_r)\left[1 + A(T - Tr) + B(T - Tr)^2\right]} + \\ C_y \dfrac{V_t}{R_y(T_r)\left[1 + A(T - Tr) + B(T - Tr)^2\right]} + \\ C_z \dfrac{V_{NL}}{R_z(T_r)\left[1 + A(T - Tr) + B(T - Tr)^2\right]} \end{array} \right\} R_{ref}(T_r)\left[1 + A(T - Tr) + B(T - Tr)^2\right] \tag{7.29}$$

$$= \left\{ C_x \frac{V_{be}}{R_x(T_r)} + C_y \frac{V_t}{R_y(T_r)} + C_z \frac{V_{NL}}{R_z(T_r)} \right\} R_{ref}(T_r)$$

So, as proved in (7.29), if all the resistors are fabricated by the same material, the temperature coefficients of the resistors would cancel out.

7.8 Conclusion

A bandgap reference with wide temperature range (drift), low temperature coefficient (TC), and which can work at a low supply voltage is presented in this research. The origin of the self-heating effect on the current mode high order curvature corrected bandgap is identified. The self-heating effect minimization techniques have been discussed. The self-heating resistor trimming procedures requires very precise and

in some cases very small resistances. Thus, for this topology resistor accuracy is a big factor for self-heating optimization.

The designed bandgap reference has the minimal effect from the thermal coefficient (TC) of resistance [36]. This is expected for the use of current mode output stage [36]. There can be several other effects in the design, which are resistor mismatch, resistor tolerance, early effect, and transistor mismatch, etc. The design shown in Fig. 7.23 may have a resistance temperature coefficient problem. This is because it uses current as the reference, and does not canceling the resistor's temperature coefficients as described in section 7.7. But the corresponding design may be helpful for the future research.

This design topology can also be used for 1st order temperature compensation by removing the nonlinear resistance R_{NL}. But high order temperature compensation is desirable for many analog applications; hence this must be included in the design. The line regulation appears to be very good for this design. The reference voltage/current can be easily adjustable to a different value by varying the R_{PTAT}, R_{Vbe}, and R_{NL} resistor values. A 3rd order Taylor series expansion has been done to prove that, higher order temperature dependent terms have a significant effect on the reference current or voltage.

CHAPTER 8

CONCLUSION AND RECOMMENDATIONS

Thermal modeling and characterization and its effects on analog integrated circuit design are analyzed in this dissertation. This research emphasizes self-heating and thermal coupling of a single device and multiple devices respectively. Modeling and characterization of thermal effect is primarily illustrated in dc and frequency domain. In addition, several analog circuits are designed and thermal effects on their performances have been investigated.

A new dc technique has been developed to extract the thermal resistance for the dielectrically isolated bipolar device. The new method uses I_c-V_{ce} plots at different temperatures to determine the constant collector current data at different temperatures and different collector voltages, when V_{be} was held constant. The extraction of the junction temperature of a dielectrically isolated device using I_c-V_{ce} plots at different temperatures is also discussed.

A novel procedure is developed and for the measurement of thermal coupling effect. The thermal coupling effect was found less than 10% (maximum) of the self-heating effect. The thermal coupling effect is reduced inversely with respect to the device separation.

A five element thermal resistance model is studied and successfully included in cadence simulation. The compact thermal circuit model for a single device and multiple devices are analyzed using the five element thermal resistance. The multiple pole idea of the thermal effect for the DIBJT devices is illustrated in the time domain using the five element model. The delay associated with the multiple pole thermal model is simulated and discussed.

Frequency dependent thermal modeling and characterization have been investigated using Y parameters. This is done with a designed balanced differential amplifier fabricated in a dual inline packaged chip. A 4.5 pF parasitic capacitance (from the package, pad, and routing wires) was found in the frequency domain thermal analysis. The corner frequency for the Y parameters due to thermal effect was found around 10 kHz.

On the other side, several analog circuits have been analyzed, designed, simulated, fabricated, and measured. Then, simultaneously the self-heating effect on these designs has been investigated. The designs include all the frequently used current mirrors, V_{be} based bootstrap current source, and high order bandgap reference.

A theory is developed to show the self-heating effect on the output characteristics of a simple current mirror. It is proved that, the output resistance is reduced by the self-heating effect. This in turn increases the current mismatch in the current mirror. It is shown that, the cascode and Wilson current mirrors have less self-heating effect.

The self-heating affect in the V_{be} referenced bootstrap current source is minimized. The sensitivity of the output current with respect to the supply voltage for this V_{be} referenced bootstrap current source is analyzed incorporating the self-heating effect. The sensitivity of the circuit (with considering self-heating effect) was found to be 0.001 in simulation and 0.0015 in measurement between 5V -12V of the supply voltage.

A high order bandgap reference circuit is designed and fabricated. The self-heating effect on the bandgap reference is analyzed, and this illustrated how to compensate for the self-heating effect. The simulated temperature coefficient for the bandgap reference from -60 °C to 125 °C was found as low as 1.14 ppm/°C. The simulation for the bandgap reference was done for a maximum temperature range between -50 °C to 250 °C with observed TC approximately between 11 ppm/ ºC to 15 ppm/ ºC. The measured TC of the reference was found to be 19.465 ppm/ ºC between -18.31 ºC to 113.09 ºC.

8.1 Recommendations for the Future work

For the frequency domain thermal analysis, a single device with two bias-T's one at the base and the other at the collector can be used. This structure can be used to extract the thermal resistance as well. The 'bias-T' has an inductor at one end and capacitor at the other end. So that, each port can have dc blocking capacitor (work as ac short) and dc short inductor (work as ac block). Therefore, the base and collector can work with both ac and dc. Adjacent device modeling results can be included in the VBIC pseudo code. Adjacent device effect can be included in the circuit simulator as

well. The bandgap reference design topology used in this research can be successfully used for BiCMOS process. VBIC model can be used successfully to improve thermal tail behavior. This research gives the procedures for determining critical points in circuit topologies with regard to thermal effects.

APPENDIX A

THE VBIC MODEL

The VBIC stands for "Vertical Bipolar Inter-Company Model". In 1995, an US industry consortium has developed and proposed a new bipolar model, called VBIC95. It includes better modeling than the G-P model. This model is developed to incorporate the effects of self-heating network, phase network, parasitic transistor, base width modulation, improve capacitance model etc. The parasitic transistor is formed by the substrate, base, and the collector. Now the VBIC95 is called VBIC. The VBIC model is shown in Fig. A.1. The VBIC model parameters are presented in table A.1.

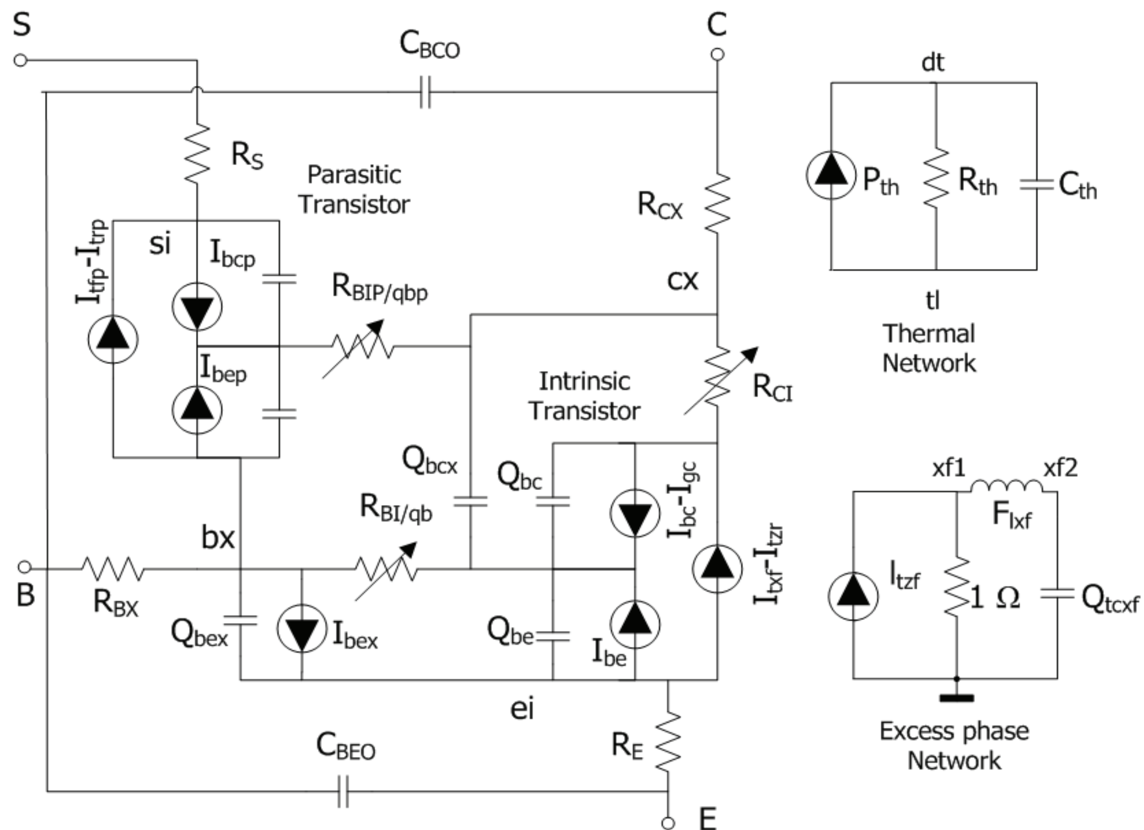

Figure A.1: VBIC Model [20].

Table A.1: Model parameters and their brief explanation [20].

VBIC Parameters	Parameter Definition
IS	Transport saturation current
NF	Forward current emission coefficient
NR	Reverse current emission coefficient
IKF	Forward High level injection current
IKR	Reverse High level injection current
IBEI	Base-Emitter ideal saturation current
NEI	Base-Emitter ideal current co-efficient
IBEN	Base-Emitter non-ideal saturation current
NEN	Base-Emitter non-ideal current co-efficient
WBE	Distributed Base parameter
IBCI	Base-Collector ideal saturation current
NCI	Base-Collector ideal current co-efficient
IBCN	Base-Collector non-ideal saturation current
NEN	Base-Collector non-ideal current co-efficient
VEF	Forward Early Voltage
VER	Reverse Early Voltage
RE	Emitter Resistance
RBI	Current dependent Base Resistance
RBX	Current independent Base Resistance
RCI	Current dependent Collector Resistance
RCX	Current independent Collector Resistance
RTH	Thermal Resistance
CTH	Thermal Capacitance
SELFT	Thermal Network Switch (‘1’ or ‘0’)

APPENDIX B

THE BASE EMITTER VOLTAGE ANALYSIS

The base emitter voltage and the temperature relation can be analyzed as follows.

Now, the base emitter voltage, collector current, and the saturation current are defined as

$$V_{be}(T) = \eta\, V_t(T) \ln\left\{\frac{I_c(T)}{I_s(T)}\right\} \tag{B.1}$$

$$I_c(T) = I_c(T_0)\left(\frac{T}{T_0}\right)^n \tag{B.2}$$

$$I_s(T) = I_s(T_0)\left(\frac{T}{T_0}\right)^{XIS} \exp\left\{\frac{E_g(T_0)}{V_t(T_0)} - \frac{E_g(T)}{V_t(T)}\right\} \tag{B.3}$$

where, ideality factor, η = 1, saturation current temperature coefficient, XIS, bandgap voltage E_g, $E_g(0)$ is the bandgap voltage at 0 K, thermal voltage V_t, and T_0 = 27 ºC. XIS is process dependent parameter. The bandgap voltage at temperature T is defined as

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{B.4}$$

in which, α = 4.73e-4 eV/K, β= 636 ºK.

Thus, (B.1) – (B.3), the base emitter voltage can be recalculated as

$$V_{be}(T) = V_t(T) \ln\left\{\frac{I_c(T_0)\left(\frac{T}{T_0}\right)^n}{I_s(T_0)\left(\frac{T}{T_0}\right)^{XIS} \exp\left\{\frac{E_g(T_0)}{V_t(T_0)} - \frac{E_g(T)}{V_t(T)}\right\}}\right\}$$

$$= V_t(T) \ln \frac{I_c(T_0)}{I_s(T_0)} + \eta\,(n - XIS)\, V_t(T) \ln\left(\frac{T}{T_0}\right) - \eta V_t(T)\left\{\frac{E_g(T_0)}{T_0} - \frac{E_g(T)}{T}\right\}$$

$$= V_t(T)\ln\frac{I_c(T_0)}{I_s(T_0)} + \eta\,(n - XIS)\,V_t(T)\ln\left(\frac{T}{T_0}\right) + \eta V_t(T)\left\{\frac{E_g(T)}{T} - \frac{E_g(T_0)}{T_0}\right\}$$

$$= V_t(T)\times\ln\frac{I_c(T_0)}{I_s(T_0)} + \eta\times(n - XIS)\times V_t(T)\times\ln\left(\frac{T}{T_0}\right) + \eta\times\left(Eg(T) - Eg(T_0)\frac{T}{T_0}\right)$$

$$= \left\{E_g(T) - E_g(T_0)\frac{T}{T_0}\right\} + V_t(T)\times\ln\frac{I_c(T_0)}{I_s(T_0)} - (XIS - n)\times V_t(T)\times\ln\left(\frac{T}{T_0}\right) \quad \text{(B.5)}$$

At $T = T_0$, (B.1) becomes,

$$V_{be}(T_0) = V_t(T_0)\ln\left\{\frac{I_c(T_0)}{I_s(T_0)}\right\}$$

$$= \frac{T}{T}\frac{kT_0}{q}\ln\left\{\frac{I_c(T_0)}{I_s(T_0)}\right\}$$

So, $$V_t(T)\ln\left\{\frac{I_c(T_0)}{I_s(T_0)}\right\} = \frac{T}{T_0}V_{be}(T_0) \quad \text{(B.6)}$$

Using (B.5) and (B.6),

$$V_{be}(T) = \left\{E_g(T) - E_g(T_0)\frac{T}{T_0}\right\} + \frac{T}{T_0}V_{be}(T_0) - (XIS - n)\times V_t(T)\times\ln\left(\frac{T}{T_0}\right) \quad \text{(B.7)}$$

(B.4) and (B.7) gives,

$$V_{be}(T) = \left[Eg(0) - \frac{\alpha T^2}{T+\beta} - \left\{Eg(0) - \frac{\alpha T_0^2}{T_0+\beta}\right\}\frac{T}{T_0}\right] + \frac{T}{T_0}V_{be}(T_0) - (XIS - n)\times V_t(T)\times\ln\left(\frac{T}{T_0}\right)$$

This can be simplified as

$$V_{be}(T) = Eg(0) - \{Eg(0) - V_{be}(T_0)\}\frac{T}{T_0} - (XIS - n)\times V_t(T)\times\ln\left(\frac{T}{T_0}\right) - \frac{\alpha T^2}{T+\beta} + \frac{\alpha T_0 T}{T_0+\beta} \quad \text{(B.8)}$$

So, by canceling the last two terms in (B.8), the base emitter voltage can be written as,

$$V_{be}(T) = Eg(0) - \{Eg(0) - V_{be}(T_0)\}\frac{T}{T_0} - (XIS - n)\times V_t(T)\times\ln\left(\frac{T}{T_0}\right) \quad \text{(B.9)}$$

Now, by differentiating (B.9) $dV_{be}(T)/dT$ can be evaluated,

$$\frac{V_{be}(T)}{dT} = Eg(0) - \{Eg(0) - V_{be}(T_0)\}\frac{1}{T_0} - (XIS - n)\frac{k}{q}\left\{1 + \ln\left(\frac{T}{T_0}\right)\right\} \quad \text{(B.10)}$$

Thus, by using the nominal values of the parameters in (B.10), the rate of change of base emitter voltage with respect to the temperature is found to be around 1.5 mV/°C.

The 3rd logarithmic term of the base emitter voltage in (B.9) has the nonlinear relationship to the temperature. It is useful to develop the Taylor series expansion of the logarithmic term. The purpose is to do more accurate design & cancel the linear as well as the non linear (curvature correcting) components of the bandgap reference.

Now, the Taylor series expansion of the logarithmic term about the reference temperature T_0 is given by

$$-(XIS - n)V_t(T)\ln\left(\frac{T}{T_0}\right)$$

$$= -(XIS - n)\frac{kT_0}{q}\frac{1}{T_0}T\ln\left(\frac{T}{T_0}\right) \quad \text{(B.11)}$$

$$= -(XIS - n)\frac{kT_0}{q}\frac{1}{T_0}\left\{a_0 + a_1\frac{(T - T_0)^1}{1!} + a_2\frac{(T - T0)^2}{2!} + \text{.................} + a_n\frac{(T - T0)^n}{n!}\right\} \quad \text{(B.12)}$$

The coefficients can be expressed as,

$$a_m = \frac{\partial^m}{\partial^m T}\left(T\ln\frac{T}{T_0}\right)\Bigg|_{T=T_0} \quad \text{(B.13)}$$

$$a_0 = \frac{\partial^0}{\partial^0 T}\left(T\ln\frac{T}{T_0}\right)\Bigg|_{T=T_0} = 0 \quad \text{(B.14)}$$

$$a_1 = \frac{\partial^1}{\partial^1 T}\left(T \ln \frac{T}{T_0}\right)\bigg|_{T=T_0} = \left\{T \frac{T_0}{T}\frac{1}{T_0} + \ln\frac{T}{T_0}\right\}\bigg|_{T=T_0} = 1 \tag{B.15}$$

$$a_2 = \frac{\partial^2}{\partial^2 T}\left(T \ln \frac{T}{T_0}\right)\bigg|_{T=T_0} = \frac{\partial^1}{\partial^1 T}\left[1 + \ln\frac{T}{T_0}\right]\bigg|_{T=T_0}$$
$$= \left(\frac{T0}{T}\frac{1}{T0}\right)\bigg|_{T=T_0} = \frac{1}{T_0} \tag{B.16}$$

$$a_3 = \frac{\partial^3}{\partial^3 T}\left(T \ln \frac{T}{T_0}\right)\bigg|_{T=T_0} = \frac{\partial}{\partial T}\left(\frac{1}{T}\right)\bigg|_{T=T_0} = -\frac{1}{T_0^2} \tag{B.17}$$

Now, by using (B.8) and (B.11) – (B.17), the base emitter voltage can be re evaluated as (by considering up to 3rd order temperature dependent terms)

$$V_{be}(T) = Eg(0) - \{Eg(0) - Vbe(T0)\}\frac{T}{T0}$$
$$-(XIS - n)\frac{kT0}{q}\left\{\frac{1}{3} - \frac{1}{2}\frac{T}{T0} + T^2 - \frac{1}{6}\left(\frac{T}{T0}\right)^3\right\} \tag{B.18}$$

REFERENCES

[1] R. M. Fox, S.-G. Lee, D.T. Zweidinger, "The effects of BJT self-heating on circuit behavior," *IEEE Journal of Solid-State Circuits*, Vol. 28, No. 6, pp 678 – 685, June 1993.

[2] Shaikh F. Shams, Colin C. McAndrew, Ik-Sung Lim and Anna Zlotnicka, "SiGe HBT Self-Heating Modeling and Characterization from AC data," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2002, pp. 92-95.

[3] Sang-Gug Lee, "A review of self-heating effects on bipolar circuit," in *Proc. Southcon/94 Conf.*, March 1994, pp. 138 – 142.

[4] Md M. Hossain, Daewoo Kim, Abhijit Chaugule, Dr. W. Alan Davis, Dr. Howard T. Russell Jr., and Dr. Ronald L. Carter, "Adjacent Device Thermal Effects Modeling and Characterization in Dielectrically Isolated Bipolar Technology," *8th ICSICT Conference (CIT and IEEE sponsored)*, October 23-26, 2006.

[5] Dr. Ronald L Carter, Professor, EE Dept., The University of Texas at Arlington.

[6] David T. Zweidinger, Robert NI. Fox, Jonathan S. Brodsky, Taewon Jung, and Sang-Gug Lee, "Thermal Impedance Extraction for Bipolar Transistors," *IEEE Transactions on Electron Devices*, Vol. 43, No. 2, pp. 342-346, February 1996.

[7] S.V. Cherepko, J.C.M. Hwang, and W.R. Curtice, "Effects of bias and load conditions on dynamic self-heating of bipolar transistors," *2004 IEEE MTT-S International Microwave Symposium Digest*, vol. 1, June 6-11, 2004, pp. 47 – 50.

[8] A. Samelis, D. Pavlidis, “Analysis of the large-signal characteristics of power heterojunction bipolar transistors exhibiting self-heating effects,” *IEEE Transactions on Microwave Theory and Techniques*, Vol. 45, Issue 4, pp. 534 – 542, April 1997.

[9] C.C. McAndrew, J.A. Seitchik, D.F. Bowers, M. Dunn, M. Foisy, I. Getreu, M. McSwain, S. Moinian, J. Parker, D.J. Roulston, M. Schroter, P. Van Wijnen, L.F. Wagner, “VBIC95, the vertical bipolar inter-company model ,” *IEEE Journal of Solid-State Circuits*, vol. 31, Issue 10, pp. 1476 – 1483, Oct. 1996.

[10] Wei Ce-Jun, J.M. Gering, and Y.A. Tkachenko, “Enhanced high-current VBIC model,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, Issue 4, Part 1, pp. 1235 – 1243, April 2005.

[11] D.T. Zweidinger, Sang-Gug Lee, R. M. Fox, “Compact Modeling of BJT Self-heating in Circuit Simulation,” *Numerical Modeling of Processes and Devices for Integrated Circuits Workshop*, May 31-June 1, 1992, pp. 219 – 224.

[12] David J. Walkey, Tom J. Smy, Ross G. Dickson, Jonathan S. Brodsky, David T. Zweidinger, and Robert M. Fox, “Equivalent Circuit Modeling of Static Substrate Thermal Coupling Using VCVS Representation,” IEEE Journal Of Solid-State Circuits, Vol. 37, No. 9, pp. 1198-1206, September 2002.

[13] N. Rinaldi, and V. D'Alessandro, “Theory of electrothermal behavior of bipolar transistors: part II-two-finger devices,” *IEEE Transactions Electron Devices*, vol. 52, no. 9, pp. 2022 -2033, Sept. 2005.

[14] S. Bruce, A. Trasser, M. Birk, A. Rydberg, H. Schumacher, "Extraction of thermal time constant in HBTs using small signal measurements," *Electronics Letters*, vol. 33, pp. 165-167, Issue 2, 1997.

[15] S.P. Marsh, "Direct Extraction Technique To Derive the Junction Temperature of HBT's Under High Self-Heating Bias Conditions," *IEEE Transactions on Electron Devices,* vol. 47, pp. 288-291, Feb. 2000.

[16] Md Hossain, W. Alan Davis, Howard T. Russell Jr., and Ronald L. Carter, "Self-Heating Effect on Current Mirror Performance," *9th IEEE Emerging Technologies Conference (ETC 2006),* September 15, 2006.

[17] Md M. Hossain, Ronald L. Carter, W. Alan Davis, M. Peng, and Howard T. Russell Jr., "Thermal Effects on Current Mirrors for High Speed Op Amp in Dielectrically Isolated Technology," *IEEE Region 5 Conference*, AR, April, 2007, accepted.

[18] http://www.national.com/appinfo/amps/vip10.html.

[19] Richard S. Muller and Theodore I. Kamins with Mansun Chan, "Device Electronics for Integrated Circuits," 3rd Ed. John Wiley & Sons, 2003, pp. 52.

[20] Anurag Lakhlani, "Device Characterization and Experimental Determination of Thermal Resistance for Dielectrically Isolated BJTs," MS Thesis, EE Department, UTA.

[21] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis and Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits," 4th Ed. New York: Wiley, 2001, pp. 253-278.

[22] Abhijit Chaugule, "Analysis And Characterization Of Thermal Effects In Analog Circuits," MS Thesis, EE Department, UTA.

[23] Tushar S. Shelar and G. S. Visweswaran, "Inclusion of Thermal Effects in the Simulation of Bipolar Circuits using Circuit Level Behavioral Modeling," Proceedings of the 17th International Conference on VLSI Design (VLSID'04), pp. 821-826.

[24] R. M. Fox and S.-G. Lee, "Scalable Small-Signal Model for BJT Self-Heating," *IEEE Electron Device Letters*, vol. 12, no. 12, pp. 649 – 65, December 1991.

[25] HP Test & Measurement, Application Note 95-1, S-Parameter Techniques.

[26] Troels Emil Kolding, "A Four-Step Method for De-Embedding Gigahertz On-Wafer CMOS Measurements," *IEEE Transactions on Electronic Devices*, Vol. 47, No. 4, April 2000.

[27] Philip C. Munro and Fang-Qiu Ye, "Simulating the Current Mirror with a Self-Heating BJT Model," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 9, pp. 1321–1324, Sept. 1991.

[28] B. M. Tenbroek, W. Redman-White, M. S. L. Lee, R. J. T. Bunyan, M. J. Uren, K.M. Brunson, "Characterization of layout dependent thermal coupling in SOI CMOS current mirrors," *IEEE Transactions on Electron Devices*, vol. 43, Issue 12, pp. 2227-2232, December 1996.

[29] S. Franco, "Design with Operational Amplifiers and Analog Integrated Circuits," 3rd edition, New York: McGraw-Hill, 2002.

[30] Md M Hossain, Ronald L. Carter, W. Alan Davis, and Howard T. Russell Jr., "V_{BE} Referenced Bootstrap Current Source, Sensitivity and Self-Heating Effect," *IEEE Transactions on Circuits and Systems-II: Express Briefs*, to be submitted.

[31] E. M. Camacho-Galeano, C. Galup-Montoro, and M.C. Schneider, "A 2-nW 1.1-V self-biased current reference in CMOS technology," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 2, pp. 61 – 65, Feb 2005.

[32] E. M. Camacho-Galeano, C. Galup-Montoro, and M.C. Schneider, "An ultra-low-power self-biased current reference," *17th Symposium on Integrated Circuits and Systems Design (SBCCI 2004)*, Sept. 7-11, 2004, pp. 147-150.

[33] E. M. Camacho-Galeano, C. Galup-Montoro, and M.C. Schneider, "Design of an ultra-low-power current source," International Symposium on (ISCAS '04), vol. 1, May 23-26, 2004, pp. I333-I336.

[34] Md M Hossain, Ronald L. Carter, W. Alan Davis, and Howard T. Russell Jr., "Design of High Order Bandgap Reference Circuit," *9th IEEE Emerging Technologies Conference (ETC 2006)*, September 15, 2006.

[35] M. Gunawan, G.C.M. Meijer, J. Fonderieand and J.H. Huijsing, "A curvature-corrected low-voltage bandgap reference," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 6, pp. 667 – 670, Jun. 1993.

[36] Gabriel Alfonso Rincon-Mora, "Voltage References: From Diodes to Precision High-Order Bandgap Circuits," Wiley-IEEE press, 2001, pp. 62 - 64.

[37] G. Rincon-Mora, P.E. Allen, "A 1.1-V current-mode and piecewise-linear curvature-corrected bandgap reference, *IEEE Journal of Solid-State Circuits*, vol. 33, Issue 10, pp. 1551 – 1554, Oct. 1998.

[38] Franco Fiori and Pablo Stefano Crovetti, "A new Compact Temperature-Compensated CMOS Current Reference," *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol. 52, no. 11, Nov. 2005.

[39] G.C.M. Meijer, P.C. Schmale, K. Van Zalinge, "A new curvature-corrected bandgap reference," *IEEE Journal of Solid-State Circuits*, vol. 17, pp. 1139-1143, Issue 6, Dec 1982.

[40] C. Popa, "A new curvature-corrected voltage reference based on the weight difference of gate-source voltages for subthreshold-o perated MOS transistors," International Symposium on Signals, Circuits and Systems, 2003 (SCS 2003). vol. 2, 10-11 July 2003, pp. 585 – 588.

[41] Personal communication with Prof. Dr. Ir. Gerard C.M. Meijer, Electronic Instrumentation Laboratory, Fac. EEMCS Delft University of Technology.

[42] Personal communication with Prof. Gabriel A. Rincón-Mora, Georgia Tech Analog and Power IC Design Lab Chairman

[43] Zheng Li, "Power management integrated circuits design, functionality analysis and application" PhD dissertation, EE Department, UTA.

[44] J. M. Audy, "3rd order curvature corrected bandgap cell," Proceedings of the 38th Midwest Symposium on Circuits and Systems, vol.1, pp. 397-400, Aug. 13-16, 1995.

[45] R. Paul, A. Patra, S. Baranwal, K. Dash, "Design of second-order sub-bandgap mixed-mode voltage reference circuit for low voltage applications," 18th International Conference on VLSI Design, pp. 307-312, 2005.

[46] J.P.C. Cajueiro, C.A. Dos Reis Filho, "CMOS bandgap with base-current thermal compensation," Proceedings of the 15th Integrated Circuits and Systems Design Symposium, pp. 345-349, Sept. 9-14, 2002.

[47] O. Salminen, K. Halonen, "The higher order temperature compensation of bandgap voltage references," *IEEE International Symposium on Circuits and Systems Proceedings (ISCAS 92)*, vol. 3, May 3-6, 1992, pp. 388 – 1391.

[48] Chi Yat Leung; Ka Nang Leung; Mok, P.K.T.;" Design of a 1.5-V high-order curvature-compensated CMOS bandgap reference"Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on Volume 1, 23-26 May 2004 Page(s):I - 48-52 Vol.1

[49] A. Van Staveren, C. J. M. Verhoeven, and A.H.M Van Roermund, "The design of low-noise bandgap references," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 43, pp. 290-300, Issue 4, April 1996.

[50] A. Azarkan, A. Van Staveren, and F. Fruett, "A low-noise bandgap reference voltage source with curvature correction," *IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 3, May 26-29, 2002, pp. III-205 - III-208.

[51] A. E. Buck, C. L. McDonald, S. H. Lewis, and T. R. Viswanathan, "A CMOS bandgap reference without resistors," *IEEE Journal of Solid State Circuits*, vol. 37, no. 1, pp. 81-83, Jan. 2002.

[52] Jing Sun, Koh Chin Yeong, Wang Hsin Hsiung, “A low voltage CMOS current source with temperature compensation,” *Southwest Symposium on Mixed-Signal Design*, Feb. 23-25, 2003, pp. 108 – 111.

[53] Xiaobin Ye, and Zhiliang Chen; “Low voltage self-biasing reference circuits,” *Proceedings of the 4th International Conference on ASIC*, Oct. 23-25, 2001, pp. 314 – 317.

[54] Lu Jingmei, Wang Yi, Xu Nuo, Gao Minglun, “Temperature compensation in bootstrapped current reference source,” IEEE Conference on Electron Devices and Solid-State Circuits, Dec. 16-18, 2003, pp. 491 – 494.

[55] A. Q. Khan, S. K. Wadhwa, K. Misri, “Low power startup circuits for voltage and current reference with zero steady state current” Proceedings of the International Symposium on Low Power Electronics and Design, 2003 (ISLPED '03), 25-27 Aug. 2003, pp. 184 – 188.

[56] Md M Hossain, Ronald L. Carter, W. Alan Davis, and Howard T. Russell Jr., “A new BiCMOS High Order Bandgap Reference Circuit,” unpublished.

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