THERMO-MECHANICAL ANALYSIS OF
NANO-IMPRINT LITHOGRAPHY

by

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‘

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To my father Chimanbhai Patel and mother Jyotsnaben Patel who made me and it is all because of their trust and blessings what I am

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Abstract

THERMO-MECHANICAL ANALYSIS OF

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Nanoimprint Lithography is being explored by the semiconductor industries for future high volume fabrication of silicon chips, memory devices and patterned media. Nanolithography and Microlithography has played pivotal role in the field of manufacturing microchips and integrated circuits in semiconductor devices. There is an urge to investigate Nanoimprint lithography, a high-throughput, low-cost and nonconventional lithographic method. Thermal management is a critical area that is necessary to be administrated. As recent advancements are being observed in the field of electronic packaging for thermal optimization, likewise steps are also important in this fabrication process.

This process involves a heat that is generated by various means like UV and high pressure. This heat results in creating a temperature gradient over the silicon wafer. The temperature profile in turn introduces thermal stress in the wafer, as little increase in temperature will have adverse effect on the quality of the product. This proves to be an important factor for aligning a silicon wafer over one another. On a single wafer multiple chips are patterned and thus the heat produced by adjacent chips also adds up to this problem. So we need to discuss various aspects of this heat generation and find a way out to have a optimize solution of this problem. Thus taking inspiration from the above

problems, the simulations were computed to get the desired results. The basic set up comprises of the wafer chuck, wafer, template and template chuck with designated materials. Now a heat source is created in order to resemble the UV exposure on the wafer with the dimensions matching the size of a chip. These set up is used for computing steady state and transient simulation to obtain the temperature profile over the wafer and to get optimal results. The simulations were based on analyzing the temperature dependency on power density while keeping the total dose constant. Based on these temperature results other simulations were carried. The structural analysis to find stress was computed using body temperature as loading. The stress results shows the equivalent (von-Misses) stress in the wafer. Moreover the writing also discusses the optimal pattern in which the exposures should be carried in multi-chip exposure.

Table of Contents

Acknowledgements ... iv

Abstract ... v

List of Illustrations ... ix

List of Table ... xi

Chapter 1 Introduction ... 1

Chapter 2 Background and Literature Review ... 4

2.1 Semiconductor Devices ... 4

2.2 Lithography ... 5

2.3 Nano-imprint Lithography ... 6

2.3.1 Photolithography ... 7

2.3.2 Electron beam Lithography ... 9

2.3.3 Soft lithography and nanoimprint lithography ... 10

2.3.4 Scanning probe lithography ... 13

2.4 Previous Work ... 15

2.5 Ansys ... 16

Chapter 3 Finite Element Method ... 17

3.1 Introduction to Finite Element Method (FEM) ... 17

3.2 Historical Background of FEM ... 17

3.3 Applications of FEM in Engineering ... 18

3.4 Engineering Analysis Discipline ... 18

3.4 Structural Analysis ... 19

3.6 Thermal Analysis ... 20

3.7 FEM Notation ... 20

Chapter 4 Modeling and Simulation 22
4.1 Problem Statement 22
4.2 Validation of Geometry 27
4.3 Transient Thermal Analysis 30
Chapter 5 Modeling and Simulation of Multiple Chip 34
5.1 Exposure of 7-chips at the center of the wafer 36
5.2 Exposure of 9 chips at edge of the wafer 41
Chapter 6 Results and Conclusions 43
6.1 Thermal Results 43
6.2 Structural Results 48
6.3 Future Work 52
References 53
Biographical Information 56

List of Illustrations

Figure 1-1 Semiconductor Wafer 2

Figure 2-1 Semiconductor Chip 4

Figure 2-2 Schematic of Photo-Lithography 7

Figure 2-3 Schematic Illustration of Forms Of Photolithography 8

Figure 2-4 Schematic 0f E-Beam Lithography 9

Figure 2-5 Schematic Illustration of Soft Lithography 11

Figure 2-6 Schematic of UV–Nanoimprint Lithography 12

Figure 2-7 Schematic Drawing for Dip-Pen Nanolithography 14

Figure 4-1 Mesh Geometry 24

Figure 4-2 Meshing for 200K Nodes 25

Figure 4-3 Plot of Temperature Vs. Number Of Nodes 26

Figure 4-4 Meshing for 400k Nodes 26

Figure 4-5 Top View of The Geometry 27

Figure 4-6 Side View of The Geometry 28

Figure 4-7 Temperature Rise Vs. Power Plot 29

Figure 4-8 Temperature Profile 29

Figure 4-9 Temperature Profile at Center 30

Figure 4-10 Temperature Vs. Time 31

Figure 4-11 Convective Heat Transfer Co-Efficient Optimization 32

Figure 5-1 Multiple Chips on Wafer 34

Figure 5-2 Mesh View in Multiple Chip on Wafer 35

Figure 5-3 Sequence for Multichip 1 36

Figure 5-4 Sequence for Multichip 2 37

Figure 5-5 Sequence for Multichip 4 38

Figure 5-6 Sequence for Multichip 3 38

Figure 5-7 Sequence for Multichip 5 39

Figure 5-8 Sequence for Multichip 6 40

Figure 5-9 Sequence for Multichip 7 41

Figure 5-10 Geometry for 9 Exposed Sites 42

Figure 6-1 Temperature Profile for Sequence 7 43

Figure 6-2 Temperature Profile for Sequence 6 44

Figure 6-3 Temperature Profile of Sequence 2 45

Figure 6-4 Temperature Profile of Sequence 4 45

Figure 6-5 Temperature Vs. Displacement Plot 46

Figure 6-6 Temperature Profile for Exposure at The Edge 47

Figure 6-7 Plot for Exposure at The Edge 47

Figure 6-8 Plot of Power Density Vs. Temperature Vs. Stress 48

Figure 6-10 Stress Profile for Exposure at The Edge 49

Figure 6-9 Plot for Exposure at The Edge of The Wafer 49

Figure 6-11 Plot for Exposure at The Center of The Wafer 50

Figure 6-12 Stress Profile for Exposure at The Center 50

List of Table

Table 4-1 Dimensions Of Components 23

Table 4-2 Thermal and Mechanical Properties 24

Table 4-3 Transient Thermal Analysis Condition 31

Table 5-1 Sequence for Exposing 9 Chips 42

Chapter 1

Introduction

The advancement of Nano-sciences (i.e. micro-technology and Nano-technology) depends on the ability to fabricate structures the micro- to the Nano-scale with high precision in a wide variety of materials is of crucial importance. Semiconductor industry is going towards high-precision nano-scale lithography to create ever-smaller transistors and higher-density integrated circuits (ICs). In order to deploy new lithography methodologies for such demanding, industrially relevant processes, several crucial issues like resolution, speed, overlay accuracy and reliability are required to be addressed. On the other hand, less stringent conditions are found in many other areas, for example, photonics, micro- and Nano-fluidics, chip-based sensors, and most biological applications. Several other concepts towards nanostructure fabrication have been exploited in the past 15 years, to avoid the use of expensive tools such as those used in deep-UV projection lithography and electron-beam lithography. Nano-imprinting imprint functional device structure in various polymers leading to a wide range of applications in electronics, photonics, data storage and biotechnology. NIL[1] technique is based on direct mechanical deformation of the resist material hence resolutions beyond the limitations set by light diffraction or beam scattering are achieved.

The implementation of lithography develops a temperature gradient along the silicon wafer. In electronics a wafer is a thin slice of semiconductor material, such as silicon crystal. The wafer is used as a substrate or base to build Integrated Circuits and other micro-devices which undergoes many micro-fabrication process steps such as doping or ion implantation, etching, deposition of various materials and lithographic

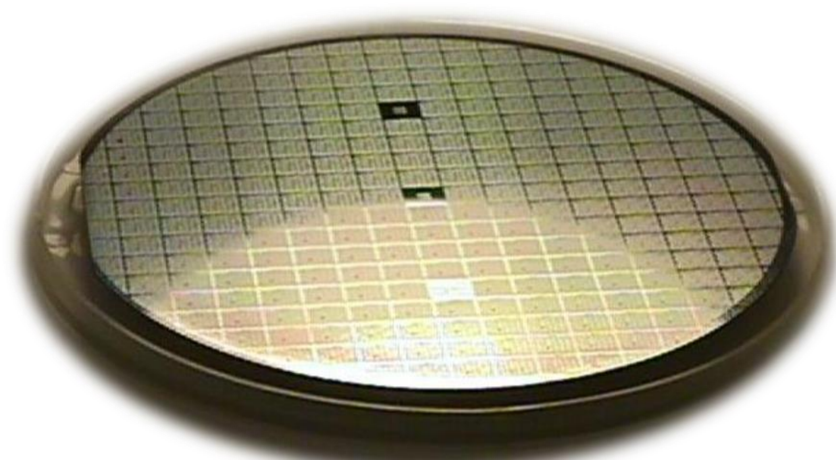


Figure 1-1 Semiconductor Wafer [2]

patterning, figure 1-1 [2] shows such a wafer. Finally the individual microcircuits are separated (dicing) and packaged. The temperature gradient constitute for thermal stresses resulting in miss-match in alignment of stacked wafers. 3-D packaging involves stacking of several wafers to optimize the use of the base area. This packaging does not integrate the chips into a single chip but the chips in the package communicate using off-chip signaling, like as they were mounted in separate packages on a standard circuit board. It is also known as System in Package (SIP) or Chip Stack MCM. Hence the thermal and mechanical analysis of lithography is a critical step in fabrication. As for manufacturing micro-electronics UV nano-imprint lithography is used. In this process the UV rays increase the temperature of the part exposed to it there by creating a temperature gradient. In order to find the temperature profile over the whole wafer, we are required to do thermal analysis of the wafer. Here, we have used Ansys software (CFX Portal) for simulating a model and determine the temperature profile. The temperature gradient hence forth creates thermal stresses over the wafer. Now for examining this stresses mechanical analysis were required, thus thermo-mechanical analysis plays an important role in fabrication of semiconductor devices.

The manufacturing processes involved in fabrication of semiconductor devices are not subjected to only one discipline of engineering. But they involve multi-disciplinary approach to optimize the production. As if we consider only the mechanical or the thermal aspect then it is beneficial to place fewer transistors on the wafer as it will produce less heat and thereby decreasing the amount of the thermal stress. On the other hand electrical engineers will recommend more and more transistors at it increase the electrical efficiency of the system. Thus we need a trade-off between these two approaches to reach an efficient mechanism for fabrication. In my thesis we are gonging to focus on the thermal management with little emphasis on the electrical issue.

The subsequent chapters will give some more information regarding different types of semiconductor fabrication methods, types of nano-imprint lithography, simulation and modeling, results and conclusion. Various types of lithography techniques and a brief introduction about it are discussed in chapter 2. Chapter 3 gives in-depth information of the thesis and methods exploited to calculate various critical parameters arising in fabrication.

Chapter 2

Background and Literature Review

2.1 Semiconductor Devices

Semiconductor Devices are electronic components which use electronic properties of semiconductors chiefly silicon, germanium and gallium. There are also few organic semiconductors which are utilized. Vacuum tubes are replaced by this device in almost all electronic applications. Electronic conduction in solid state is used as compared to gaseous state or thermionic emission in high vacuum.

Semiconductor devices found wide applications because of their reliability, low cost and compactness. They have made their usage in power devices, optical sensors and light emitters including solid-state lasers. Other critical features is their wide range of current capacity ranging from few Nano-ampere(10^{-9} ampere) to more than 5,000 ampere and voltage capacity extending above 100,000 volts More important, semiconductor devices lend themselves to integration into complex but readily manufacturable microelectronic circuit [3].

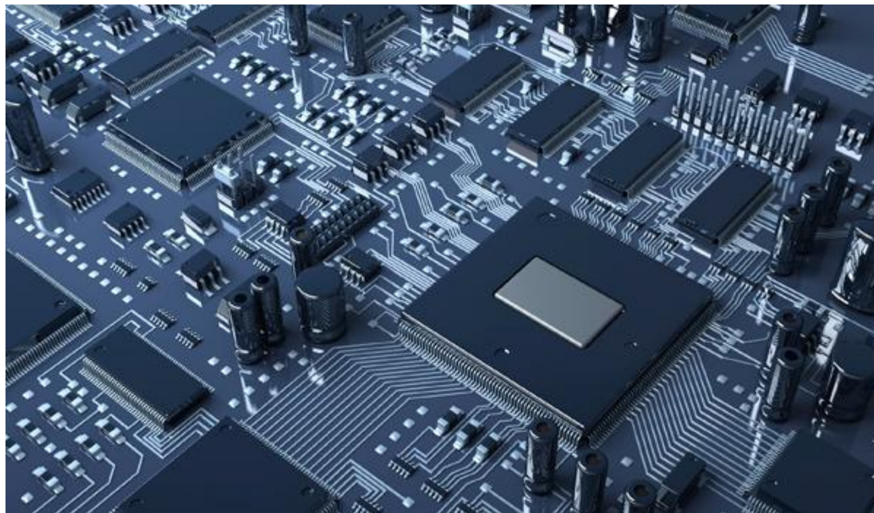


Figure 2-1 Semiconductor Chip [3]

Silicon is the most commonly used semiconductor for manufacturing devices. As silicon does not become dysfunctional because of avalanche breakdown(a process in which an electron avalanche is created by a chain reaction process, producing free electrons and holes by heating which in turn produce more current which delivers more heat) under high temperature and electrical powers. Also silicon becomes insoluble in water due to its insulating oxide which edges it over germanium in certain fabrication techniques [4].

Semiconductor devices are made up of many layers, each with different geometry and specifications and each requiring precise alignment to the previous layers. Lithography has always been an integral part, if not the primary enabler, behind this industry [5].

2.2 Lithography

Lithography uses simple chemical processes to create an image. The basic phenomena can be understood by the following example; the positive part of an image is a hydrophobic substance, while the negative image would be a hydrophilic substance. Thus, when the plate is introduced to a compatible printing ink and water mixture, the ink will adhere to the positive image and the water will clean the negative image. Moreover using a flat print plate, enables much longer and more detailed print than other old physical methods like (letterpress printing, intaglio printing).

The fabrication of an integrated circuit (IC) requires a variety of physical and chemical processes performed on a semiconductor (e.g., silicon) substrate. The fabrication process is categorized into three different processes: film deposition, patterning and semiconductor doping. For changing the conductivity of silicon with the

application of voltage, selective doping is utilized. This different component helps in creating millions of transistors which are wired to form complex circuit of modern microelectronic device. Fundamental to all these processes is lithography, the formation of three-dimension relief images on substrate for subsequent transfer of the pattern to the substrate. The word lithography comes from the Greek *lithos*, meaning stones, and *graphia*, meaning to write. It basically means writing on stones. In the case of semiconductor lithography (also called photolithography), silicon wafer s takes the place of stones and our patterns are written with a light sensitive polymer called a photoresist. The transistors and the number of wires connecting millions of transistors of a circuit make complex structures which are built using lithography. The patterning steps are repeated at least 10 times but generally it is done 20 to 30 times to make one circuit. Each pattern being printed on the wafer is aligned to the previously formed patterns and slowly the conductors, insulators, and selectively doped regions are built up to form the final device.

2.3 Nano-imprint Lithography

The term nanolithography is derived from the Greek words “nanos”, meaning dwarf; “lithos”, meaning rock or stone; and “graphein” meaning to write. Thus it can be comprehended as ‘tiny writing on stone’, but now a days it has been taken as something different whenever this term is associated with nanotech.

Nanolithography is the branch of nanotechnology concerning the study of nanofabrication of nanometer-scale structures and their applications. It means nano-patterning with at least one lateral dimension between the size of an individual atom and approximately 100 nm. Nanolithography is used e.g. during the nanofabrication of leading-edge semiconductor integrated circuits (Nano-circuitry), for nano-electromechanically systems (NEMS) or for almost any other fundamental application

across various scientific disciplines in Nano research. Contrasting to various other nanolithography methods used in nano-research such as

Photolithography

Electron beam Lithography

Soft lithography and nanoimprint lithography

Scanning probe lithography

2.3.1 Photolithography

Photolithography contributes the most in the fabrication of semiconductor and IC industry [6-10]. It is used for pattern generation in manufacturing ICs, microchips and

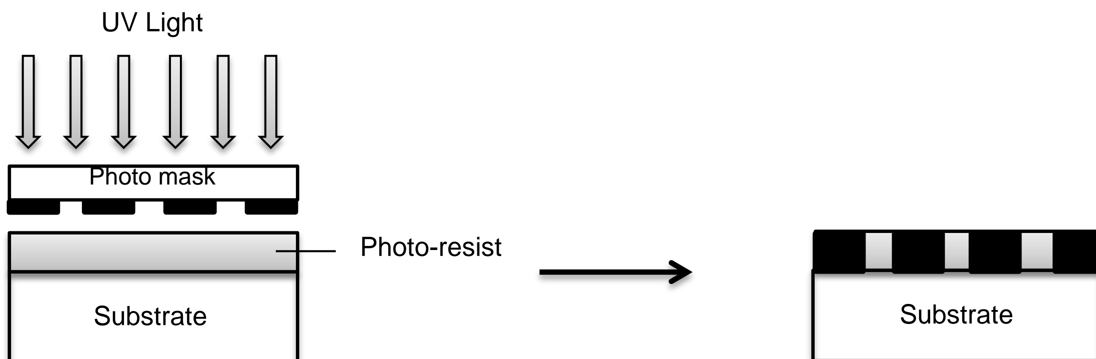


Figure 2-2 Schematic of Photo-lithography

commercial MEMS devices. A desired pattern is defined by exposing a light–sensitive polymer (photo-resist) to ultraviolet (UV) light. Initially, UV light with wavelengths in the range of 193-436 nm is illuminated through a photo mask that consists of opaque features on a transparent substrate (e.g., quartz, glass) to make an exposure on a photo-resist that is coated on a substrate [6,7]. The exposure tends to break the polymer chains of the photo-resist resulting in more soluble in a chemical solution called developer. Subsequently, the exposed photo-resist is removed in a developer to form the desired photo resist pattern. Figure 3 depicts the schematic illustration of the main steps in

photolithography. Moreover, to build topography the patterned photo-resist can be used as a protective layer in subsequent etching or deposition processes on the substrate. Photolithography forms of three different forms: contact printing, proximity printing and projection printing as schematically illustrated in Figure 4 [6, 7]. Contact and proximity as suggested by the name places the printings photo mask in contact with or in a close proximity to the photo-resist. Therefore, contact and proximity printings have the capability of making patterns as small as a few micrometers. Hence, this is traditionally used in the fabrication of moderate-resolution patterns especially in laboratories and

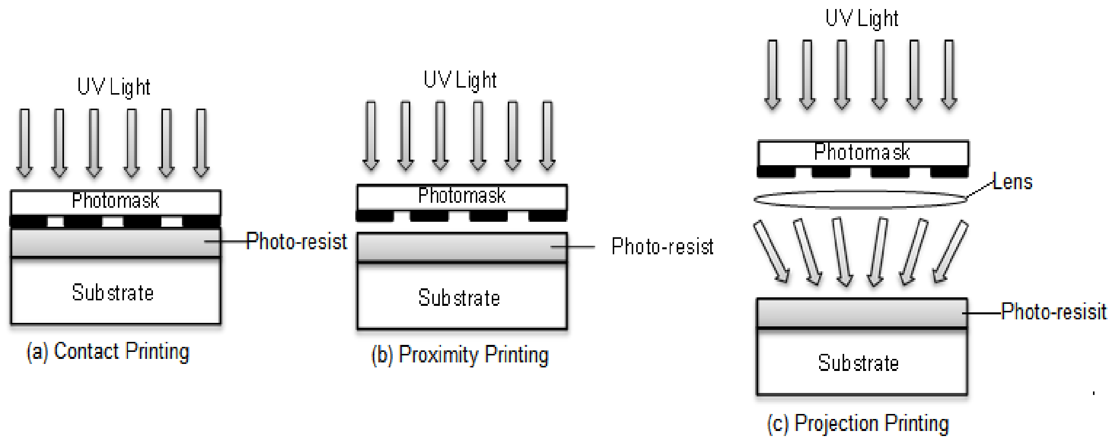


Figure 2-3 Schematic illustration of forms of photolithography

small to medium sized companies. So commonly in research work contact or proximity printings are used. Whereas, a projection printing system also called as ‘stepper’ uses an optical lens system to project a deep UV pattern from an excimer laser (wavelength of 193 or 248 mm) on the photo-resist enabling pattern-size reduction by 2-10 times. The fabrication capability of this type of lithography extends to high resolution patterns as small as a few tens of nanometers (37 nm) [7] at a high throughput (60-80 wafers/hr.) [6]. However, a sophisticated optical –lens system and precise control system of temperature and position makes it a very expensive setup. This limits its utilization in manufacturing of

advanced ICs and CPU chips. In recent years, immersion lithography [9], resolution enhancement technology [6] and extreme-UV lithography [10] have been developed to improve the lithography resolution of projection printing.

2.3.2 Electron beam Lithography

Electron beam and focused ion beam lithographies have been the main techniques for fabricating Nano-scale patterns. Electron beam lithography [11,12] utilizes an accelerated electron beam focusing on an electron-sensitive resist [13] to

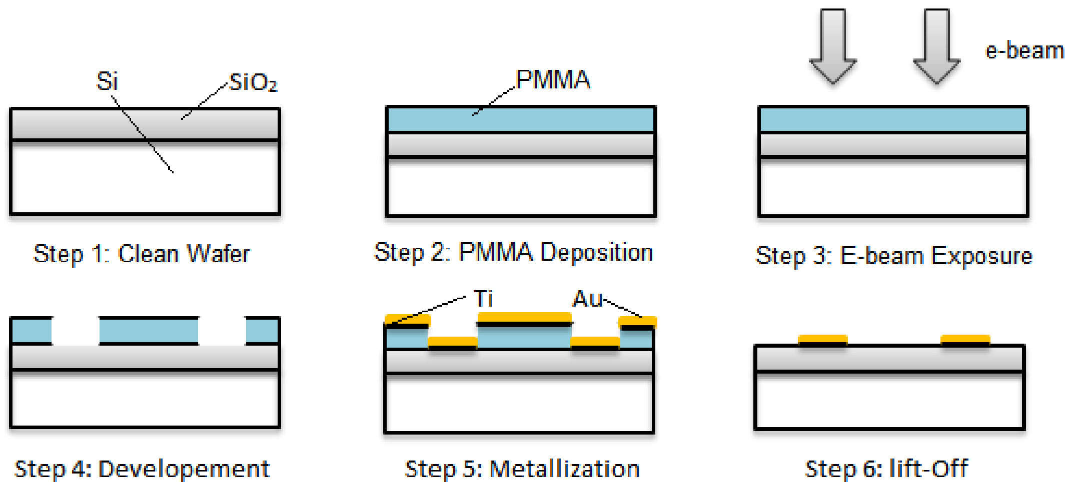


Figure 2-4 Schematic of E-beam Lithography

make an exposure. Thereafter, to create patterns in sequence the electron-beam spot with a diameter as small as a couple of nanometers is scanned on the surface of resist in a dot-by-dot fashion (Figure 5). Whereas, focused-ion beam lithography utilizes an accelerated ion beam (typically gallium ion) instead of the electron beam to directly punch a metallic film on the substrate [14, 18]. The heavy mass of ions compared to that of electrons makes it possible. Moreover, focused ion beam systems also find there usage for depositing materials such as tungsten, platinum, and carbon via ion beam induced

deposition. The process is initiated when a precursor gas such as tungsten hexacarbonyl ($W(CO)_6$) is added into the chamber, the precursor gas is hit by the focused-ion beam leading to gas decomposition which leaves a non-volatile component (tungsten) on the surface [18]. The resolution specifications of electron beam and focused ion beam lithography techniques are of the order of 5 – 20 [6, 12] nm due to ultra-short wavelengths of electron/ion beams in the order of a few nanometers. However, the lack of throughput limits their applications within research and mask fabrication. Thus, these two techniques are normally confounded for fabricating prototypes of nanoscale structures and devices. A multi-axis electron beam lithography [15, 16] has been proposed to increase the throughout. So far, the deployment of this technique in manufacturing process is still limited due to the difficulty in developing practical electron beam sources [7] . Now a day, scanning electron microscopes were able to be equipped with pattern generator modules, whereas in the past, electron beam lithography was very expensive thus limiting the access. This enables the scanning of electron beam spot within desired areas to generate nanoscale patterns as electron beam lithography systems [17]. As a result, this technique has become widely used which greatly contributed to the progress in nanoscience and engineering.

2.3.3 Soft lithography and nanoimprint lithography

Soft lithography is not a new technology but dates back to 1989, when it introduced by Bain and Whitesides [19]. This technique requires inexpensive materials and employs non-specialized equipment. It was initiated by the innovation of using a relatively soft polymer stamp to imprint a solution of molecules (ink) onto a substrate for pattern transferring. This process can divided into two main steps: the fabrication of a

patterned polymer stamp, and the use of this stamp to transfer molecules in geometries defined by the element's relief structure.

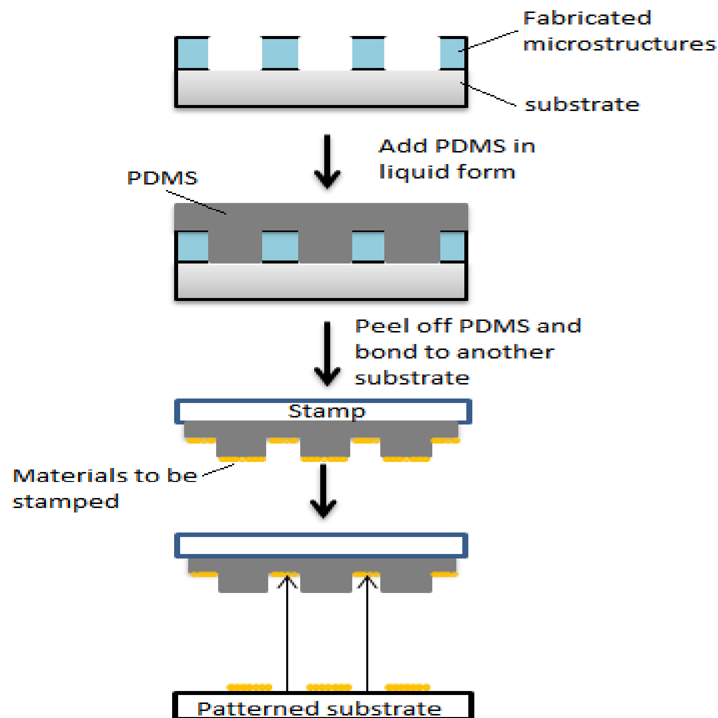


Figure 2-5 Schematic illustration of soft lithography

This lithography utilizes an unique technique allowing conformal contact between the stamp and the substrate with a soft stamp for pattern transferring resulting in a patterning capability on flexible or curved substrates. Unlike soft lithography, nanoimprint lithography utilizes a hard mold to imprint into a polymer film for nanoscale patterning. Nanoimprint lithography has potentially become a strong candidate for next-generation manufacturing methods as it is a surreptitious way to overcome the issues in photolithography, thereby, promising a high-throughput and high-resolution method with a

relatively low cost [6, 7]. S.Y.Chou first introduced nanoimprint lithography as ”hot embossing technique” enabling the definition of features with lateral sizes down to sub-10 nm [20, 21]. The procedure of imprinting lithography is shown in Figure 6. The technique heats thermoplastic polymer above its glass transition temperature enabling material flow, filling the structures of a mold. After that, the mold is cooled bringing down its temperature and the replicated patterns are solidified in place, after which the mold is removed. The most commonly used materials for mold have been quartz and silicon that are kinds of hard material. Traditionally, mold features are patterned by using conventional lithography techniques such as photolithography and electron beam lithography. A hard material offers a number of advantages for nanofabrication like it is thermally stable at high temperature and retains rigidity creating nanoscale features with minimal local deformation.

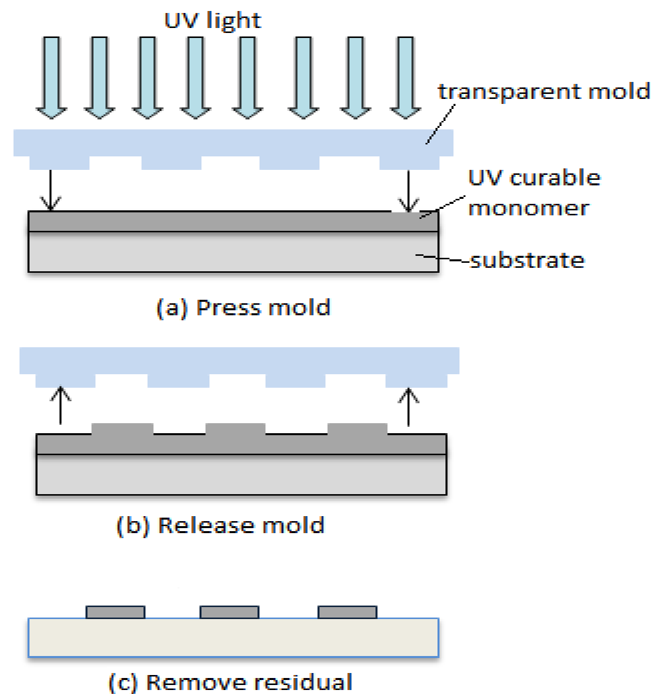


Figure 2-6 Schematic of UV–nanoimprint lithography

Although nanoimprint lithography has made a great progress in a relatively short time, there are few issues to be resolved. The heating/cooling cycles and high pressure, applied during embossing, cause stress and wear on molds making life span of the mold critical. This stress also presents a problem of alignment for multi-layer fabrication and viscosity embossed material is also an important issue. It appears to be a limiting factor for minimizing pattern size and increasing feature density. In 1996, nanoimprint lithography was devised through the introduction of a low-viscosity UV curable monomer as compliant polymer layer in order to enhance fluidity of the embossed material [22].The process is called UV-nanoimprint as schematically shown in Figure 7. After imprinting on a UV-curable monomer layer, broadband UV light radiation directly through the backside of transparent mold causes the monomer crosslink, forming a rigid polymer. It can reduce imprint pressures significantly and avoid time consuming as well as stress induced during high temperature cycle. UV-curable monomers are very important factor for a success of UV-nanoimprint technique. A recent development in this field is the UV-curable Amonil polymer (AMO GmbH, Germany) with a viscosity of about 50 mPas. It found many usage [23-25], with a novel low-viscosity which is about one third that of Amonil and spin ability down to 150 nm thick [26]

2.3.4 Scanning probe lithography

Scanning probe lithography utilizes a sharp probe in an atomic force microscope (AFM) to heat, scratch, oxidize or transfer substances to the surface of a substrate for patterning nanoscale features [27,28]. The approach to deposit nanoparticles or molecules selectively onto a substrate so-called dip-pen nanolithography is the most widely used [29, 30] among all the techniques. One of the advantages of Dip-pen nanolithography is that it can be performed under ambient environment without any large electromagnetic field and shear force involved.

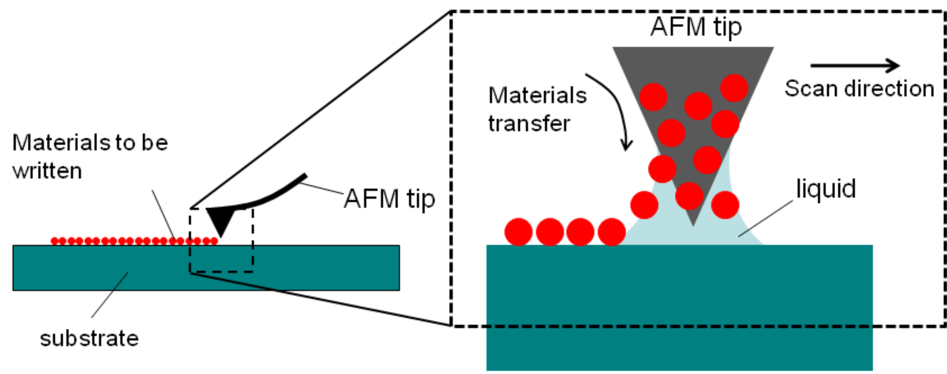


Figure 2-7 Schematic drawing for dip-pen nanolithography [36]

It initially came in for transferring thiol molecules to a freshly prepared gold surface [29]. AFM probe is coated with a thin film of a chemical of interest by immersing the cantilever in a solution or by evaporation. Chemical molecules are deposited onto a substrate surface during the contact between the coated tip and the substrate. The schematic drawing for dip-pen nanolithography is shown in Figure 8 . One limitation of dip-pen technique is the difficulty to scale up that its constructed area Shim et al.[31] propagated an initial array of up to 4,750 silicon probe tips over an area of 1 cm^2 on an elastomer layer attached to a glass slide in 2011. This invention can be used to create arbitrary patterns in a massive parallel fashion without the need for a mask. It was demonstrated that a pattern of holes in a 30 nm PMMA film can be created. Typically hard material such as silicon, silicon nitride, and PDMS elastomer are used to make probe tips while various nanomaterials can be written such as nanoparticles [32] , liquid solution [33] , and organic materials [34]. The characteristics of dip-pen nanolithography from manufacturing aspects including processing rate, tool life, and feature quality have been recently reported [35] .

2.4 Previous Work

In this segment we are going to acknowledge some previous work done in the topic of ‘Thermo-mechanical analysis of Nano-imprint lithography’. Firstly in the year 2005, Eui Kyoon Kim, C. Grant Willson computed simulation on step and flash imprint lithography. They observed that the mismatch between monomer absorbance and the light intensity spectrum and the low loading of photo acid generator and photo radical initiator results in insignificant heat generated by UV absorption. It was about 1% of the heat generated by the polymerization process due UV exposure so it can be neglected. The other important value they mention was for 3 sec exposure at $74mW/cm^2$ was sufficient for completing the polymerization of the acrylate formulation they used. The conclusion made by them was ‘ polymerization reactions of the imprinted materials are rapid, the temperature rise during photo polymerization in this application is very small but sufficient to require the attention of engineers who are designing imprint tools for future device manufacturing’.

The other significant work in this field was an experiment conducted on heat transfer analysis during a curing process for UV nanoimprint lithography by Insoo Park, Si-Hyung Lim, Donghoon Shin. They exposed the chip for 10 minutes but started the UV light after 30 seconds and recorded the temperatures up to 210 seconds. After 210 seconds they turned off the light and recorded the temperature till 600 seconds. They used thermocouple for computing the temperature and performed two sets of experiments. The results of the experiments recorded a maximum temperature rise of 3.5^{o} C and 5°C.

Both previous works were significant development in the field of thermal analysis of Nano-imprint lithography but to have a better understanding of the temperature profile

over the wafer and compute the induced stress because of the temperature gradient the simulation were run. The simulations are computed on Ansys.

2.5 Ansys

In this chapter, we will discuss briefly about the software used for simulating and modeling the thermo-mechanical problem. Ansys provides engineering simulation solution sets in engineering simulation that a design process requires. It is used over a wide variety of industries like automotive, electronics, aerospace and consumer products etc. The tool design a virtual product through a rigorous testing procedure (such as temperature profile of an electronic chip undergoing non-uniform power density or finding various parameters of a fluid flow through a pipe) before it becomes a physical model. Ansys consist of various modules like Ansys CFX, Ansys Fluent, Static and transient thermal as well as structural module. It also has specific modules like the IC engine module which is used to simulate IC engines.

In my thesis I have used Ansys CFX to run my simulations. It provided all the needed tools required to get the desired results. I have also used the static structural module and transient structural module to complete my mechanical analysis. Ansys uses Finite element for solving thermal and structural issues. Finite element analysis provides an efficient means of simulation of generation and dissipation of heat in unique geometries during photo curing. The solution thus obtained consists of 3D thermal elements.

Chapter 3

Finite Element Method

3.1 Introduction to Finite Element Method (FEM)

Finite element method is the most popular and widely used method, among the various numerical methods. Moreover this is also considered as the most sophisticated tool for solving engineering problems. The method basically divides the whole continuum is divided into a finite number of elements of geometrically simple shape. These elements comprises of number of nodes whereas unknown are the displacements of these nodes. The displacement unknowns are described at each point of a polynomial interpolation function. The entire force applied to the structure is replaced by an equivalent system of forces applied to the nodes [40]. The result of the entire displacement of the structure is obtained by assembling the governing equation

$$\{F\} = [K]\{u\}$$,where

{F} = Nodal Load Vector

[K] = Global Stiffness Matrix

{u} = Nodal Displacements

3.2 Historical Background of FEM

- Finite Element Analysis (FEA) was first developed in 1943 by R.Courant who utilize Ritz method of numerical analysis
- The name Finite Element was coined by Clough in the year 1960, who also introduced plane problems in FEA.
- The basic ideas of FEM were presented in the papers of Turner, Clough, Martin & Topp and Argyis And Kelsey.

- By the early 1970's, FEA was limited to expensive mainframe computers generally owned by the aeronautics, automotive, defence and nuclear industries and the scope of analysis were considerably limited.
- People such as Zeinkiewicz & Cheung further enhanced finite element technology during 1970's, when they applied the technology to general problems described by Laplace & Poisson's equations.
- 1971 – First release of ANSYS.
- During 1980's micro computers were employed in the development of Finite Element Method.
- By the early of 1990's FEM is being used for analyzing larger structural systems.
- Now-a-days the Finite Element Method has its roots in many disciplines

3.3 Applications of FEM in Engineering

- Aerospace/Mechanical/Civil/Automobile Engineering
- Structural Analysis(Static/Dynamic/Linear/Non-Linear)
- Thermal/Fluid flows
- Nuclear Engineering
- Electromagnetic
- Biomechanics
- Geomechanics
- Biomedical Engineering
- Hydraulics
- Smart Structure

3.4 Engineering Analysis Discipline

- Structural analysis (Motion of solid bodies, pressure on solid bodies etc.,)
- Thermal Analysis

- Magnetic Analysis
- Electric Analysis
- Fluid Analysis (Motion of gases/fluids)
- Coupled-Field Analysis (Combination of any of the above)

3.4 Structural Analysis

The structural analysis used to compute the deformations, internal forces and stress of a particular object. The basic skeleton to perform a structural analysis consists of the following parameters; we should first determine the structural loads, geometry, support conditions and material properties. The static response of the structure is observed using this type of analysis [39].

Example: Calculation of deformations, internal forces, stresses and strains. The following are the areas in which structural analysis play a major role,

- Static Analysis – Under static loading conditions, determining the displacements and stresses.
- Modal Analysis – For determining the mode shapes and natural frequencies of a structure.
- Harmonic Analysis – Under time varying loads, determining the harmonic response of the structure.
- Transient Dynamic Analysis – Under random time varying loads, determining the response of the structure.
- Spectrum Analysis – Due to a response spectrum or a random vibration input, calculating the stresses and strain of the structure.
- Buckling Analysis – For calculating the buckling loads and determining the buckling load shape.

- Advance Structural Analysis – This examines the dynamic response, stability and nonlinear behavior of the structure.

3.6 Thermal Analysis

Thermal analysis aids in computing the temperature gradients, heat transfer and thermal flux of an object. The three modes of heat transfer; conduction, convection and radiation analysis can be performed on the desired model [40]. The thermal analysis can be performed in two areas:

- Steady State Thermal Analysis – Under static loading conditions they are used to determine the temperature gradient and other thermal quantities.
- Transient Thermal Analysis – Under time varying loading conditions, they are used to determine the temperature gradient and other thermal quantities.

3.7 FEM Notation

Finite element method treats the continuous problem domain as a collection of individual finite elements. The problem parameters are defined at each node of the element. The commonly used definitions of the FEM notation are [40],

- *Dimensionality:* Dimensionality indeed expresses whether the element has 1, 2 or 3 space dimensions.
- *Nodal Points:* Each element is defined by its nodal points. Generally the nodal points are chosen to be the corners of the element. However in case of nonlinear geometries nodal points are also defined on the edges.
- *Geometry:* This term is used to introduce the domain on which finite element discretization needs to be applied.The geometry is defined by the placements of the nodal points.
- *Degrees of Freedom:* The degree of freedom is the number of ways in which the original problem domain can change its state. In the case of the continuous problem

domain, the DOF is infinite, because problem characteristics can be defined in each point on the domain

- *Nodal Forces:* A set of nodal forces (or any other actions depending on the problem) are defined on each nodal point

To summarize in general terms how the finite element method works we list main steps of the finite element solution procedure below :

1. Discretize the continuum - The first step is to divide a solution region into finite elements. The finite element mesh is typically generated by a preprocessor program. The nodal coordinates and element connectivities are of the main arrays which describe the mesh
2. Select interpolation functions - Interpolation functions are used to interpolate the field variables over the element. Typically, polynomials are selected as interpolation function and degree of the polynomial depends on the number of nodes comprising the element.
3. Find the element properties – Establishment of the matrix equation for the finite element, which relates the nodal values of the unknown function to other parameters. This can be done using different approaches, the most convenient are: the variational approach and the Galerkin method.
4. Assemble the element equations – All the element equations must be assembled to find the global equation system for the whole solution region. This means we must combine local element equations for all elements used for discretization. Boundary conditions should be imposed before solution as they are not included in element equation.

Chapter 4

Modeling and Simulation

In this chapter, finite element modeling of the lithography set up is discussed in detail to study the impact of temperature gradient .Finite element method is used because it is the most widely used method to solve the thermo mechanical deformation and stress distributions in semiconductor devices. During the lithography process, when the silicon wafer is exposed to UV rays it heats up and creates temperature gradient over the wafer causing thermo mechanical stress. The entire analysis in this study has been executed in the commercially available code ANSYS Workbench v13.0.

4.1 Problem Statement

In the previous chapters we discussed different form of lithography techniques and implementation of finite element method to perform simulation. Now from the mentioned lithography techniques we selected UV-Nano imprint lithography for our simulation. UV-Nano imprint lithography has made a great progress in a relatively short time; there are few issues to be resolved. The heating/cooling cycles and high pressure, applied during embossing, cause stress and wear on molds making life span of the mold critical. This stress also presents a problem of alignment for multi-layer fabrication and viscosity embossed material is also an important issue. Moreover the thermal properties of the materials involved are also one of the important things to be considered. The cycles involved in the process creates a temperature gradient over the wafer or substrates which are responsible for thermal stresses. Also an increase in temperature during the process results several other problems which includes (a) safety issues related to rapid heating; (b) thermal decomposition results in weak tensile strength and modulus of the imprint.

The following geometry is used for the simulation with the specified dimensions is used for simulation:-

Table 4-1 Dimensions of components

<table>
<tr><th>Component</th><th>Dimension (mm)</th><th>Thickness (mm)</th></tr>
<tr><td>Wafer Chuck</td><td>500 Diameter</td><td>4.5</td></tr>
<tr><td>Wafer</td><td>300 Diameter</td><td>0.8</td></tr>
<tr><td rowspan="2">Template</td><td>15 x 15</td><td>2</td></tr>
<tr><td>100 X 100</td><td>4</td></tr>
<tr><td rowspan="2">Template Chuck</td><td>60 X 60</td><td rowspan="2">6</td></tr>
<tr><td>200 X200</td></tr>
<tr><td>Chip</td><td>10 X 10</td><td>0.8</td></tr>
</table>

A wafer have multiple chips fabricated on it, first we are going to predict the temperature and corresponding stresses related to a single chip and later on multi-chip system. The design of experiment is performed to predict the temperature profile over the wafer. The first step was to model geometry of a lithography method, for this purpose we considered the photolithography technique from the nanoimprint technique. The geometry bellow was used for simulation having wafer chuck, wafer, template and template chuck. The dimensions of all of them are mentioned in Table 1 and Figure 9 shows the meshed geometry. Meshing is an important part of the simulations therefore we carried out a nodal analysis. Nodal analysis showed the minimum number of elements required for having a consistent result. The plot shown in Figure 10 represents the relation between number of nodes and temperature increase. The geometry used for this purpose is exactly the same as used for actual simulations for the purpose of consistency. For

carrying out this analysis we have done a steady state thermal analysis using the following thermal properties [41, 42] and boundary conditions.

Table 4-2 Thermal and Mechanical Properties

Components	Wafer Chuck	Wafer	Template	Template Chuck
Material	Cooper	Silicon	Silica	Aluminum
Thickness [mm]	5	0.8	6	6
Thermal Conductivity (K) [W/m K]	401	148	1.38	237
Specific Heat (Cp) [J/Kg K]	390	710	670	910
Density (ρ) [g/cm^3]	8.96	2.33	2.65	2.702
Young's modulus [MPa]	1.15 X 10^5	1.5 X 10^5	7.3 X 10^4	7 X 10^4
Poisson's Ratio	0.34	0.17	0.70	0.35
CTE [^{o}C^{-1}]	1.65 X 10^{-5}	2.6 x 10^{-6}	4.5 X 10^{-7}	2.31 X 10^{-5}

The boundary conditions for the simulation consist of the power on the chip due to UV radiation and the convective heat transfer co-efficient on template chuck and wafer chuck. The heat transfer co-efficient on the outer surface of wafer chuck was 5000

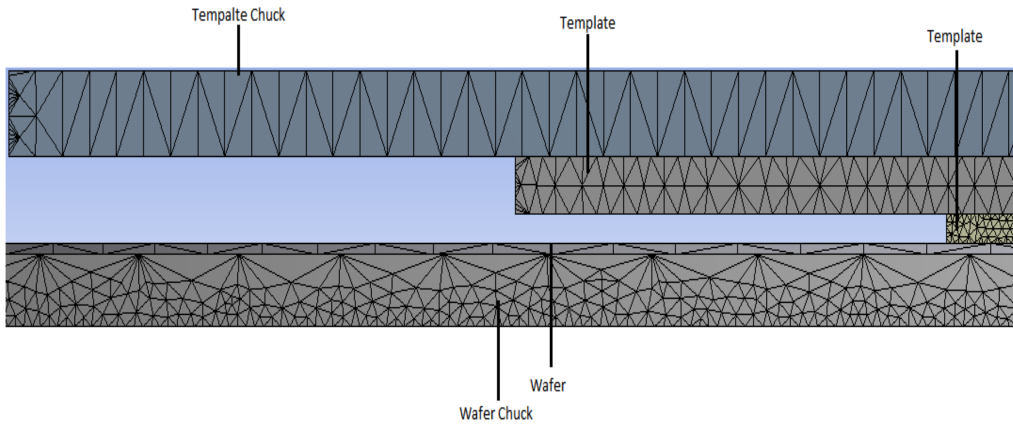


Figure 4-1 Mesh Geometry

W/m^{2}K, whereas on the template chuck it is 1000 W/m^{2}K. Also a power source intensity of 5 W was considered on the chip because of the radiation.

The mesh structures shown in Figure 4-2 are for approx. 200K nodes and in Figure 4-3 it is approx. 400K. The number of nodes was selected from 200,000 to 120,00,00. The results showed that we got consistent result number of nodes ranging between 800,000 to 120, 00, 00. The exact number of nodes which provides consistency are 984,581 nodes but it took longer duration for the results in the structural analysis hence around 200K nodes were used. The plot shown below explains the result of the simulations.

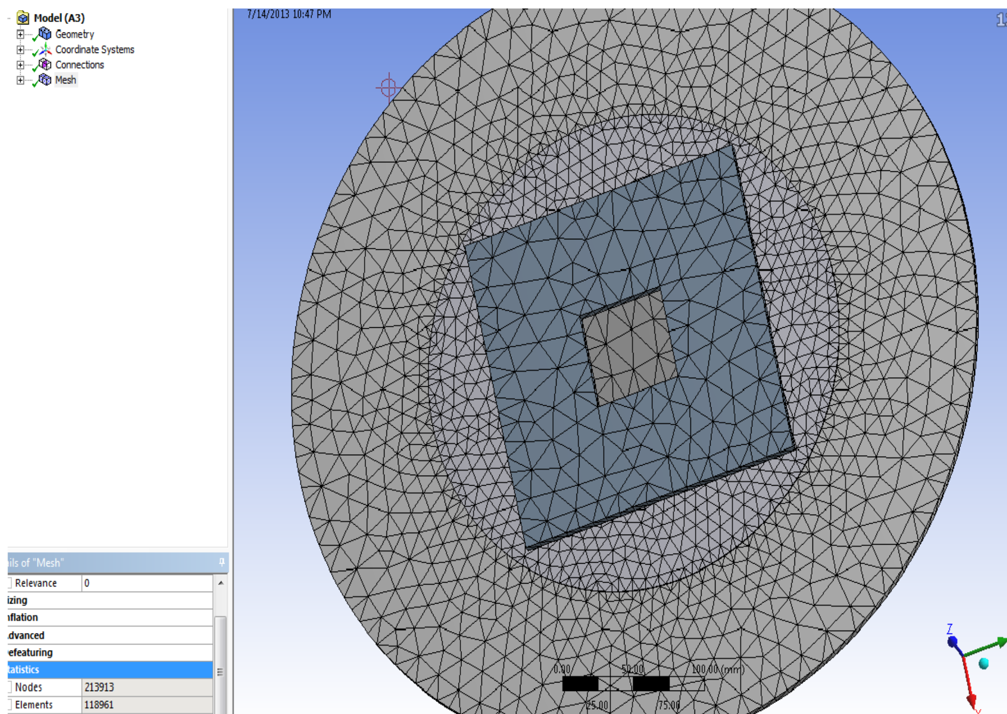


Figure 4-2 Meshing for 200K Nodes

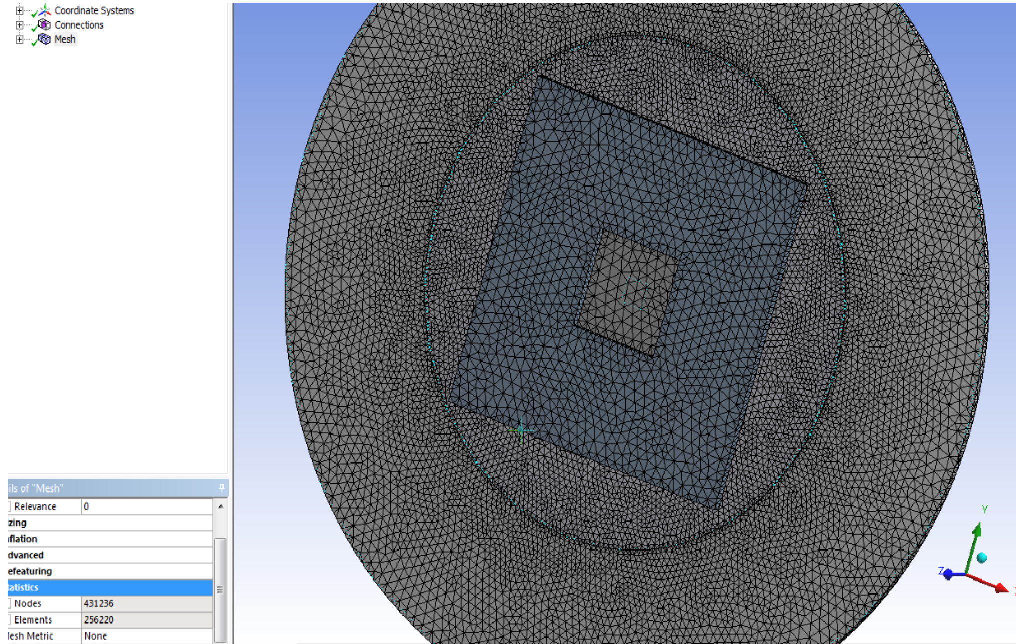


Figure 4-4 Meshing for 400K Nodes

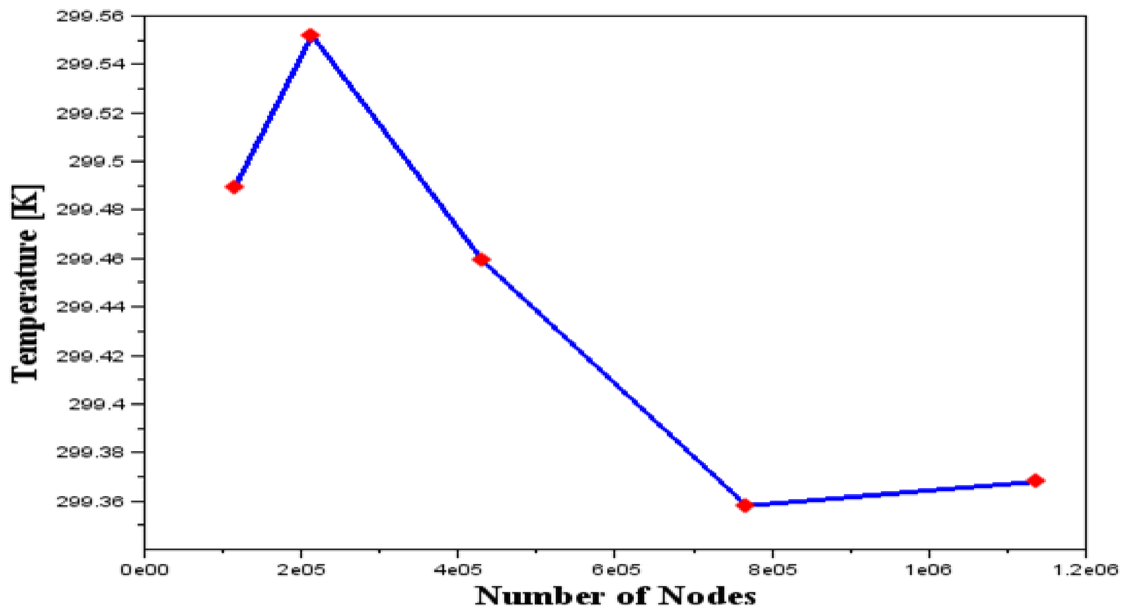


Figure 4-3 Plot of Temperature vs. Number of Nodes

4.2 Validation of Geometry

In this section, a steady state analysis is discussed for the purpose of validation of the geometry. The geometry of the model is critical in the analysis as it affects the results. For this reason we validated the geometry with a steady state analysis with a power xsource of 1 W over the chip having dimesions10mm x 10mm. The boundary condition over the surface of wafer chuck and template chuck were same as used for the nodal analysis. The top view of the model is shown in figure 4-5, whereas side view of the

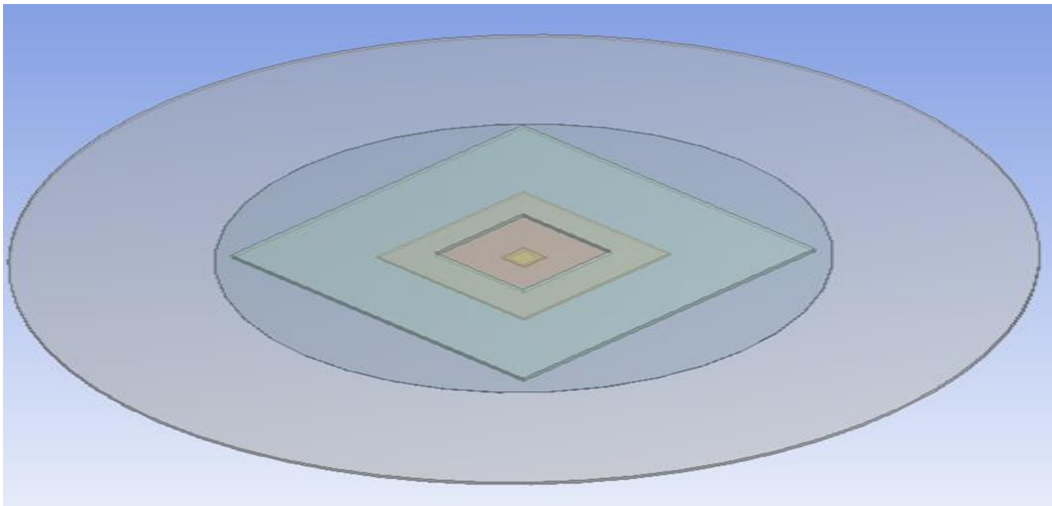
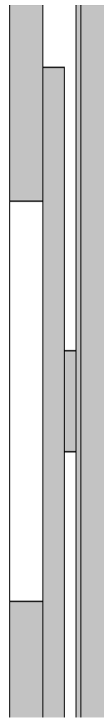


Figure 4-5 Top View of the Geometry

model is shown in Figure 4-6. In the side view we can see a square cavity of 60mm x 60mm in the template chuck which allows the UV rays to directly fall on the template. The geometry was then used to run a steady state analysis with increasing values of power to validate the model.



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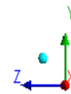


Figure 4-6 Side View of the geometry

The steady state analysis was carried out by giving wattage of 0.01 watt (W) to the chip and going up to 200 W to a single chip. According to the general heat equation heat generated or power supplied is directly proportional to the change in temperature. The proportionality equation is shown below

$$Q \propto \Delta T$$

Q = Heat generated or Power supplied

ΔT = Change in temperature

The results from the simulation converse to this equation. So by the means of this simulation we were able to validate the geometry. The plot shown in the figure 4-7 explains the results of the simulation. Also in the figure 4-8, we can see the temperature

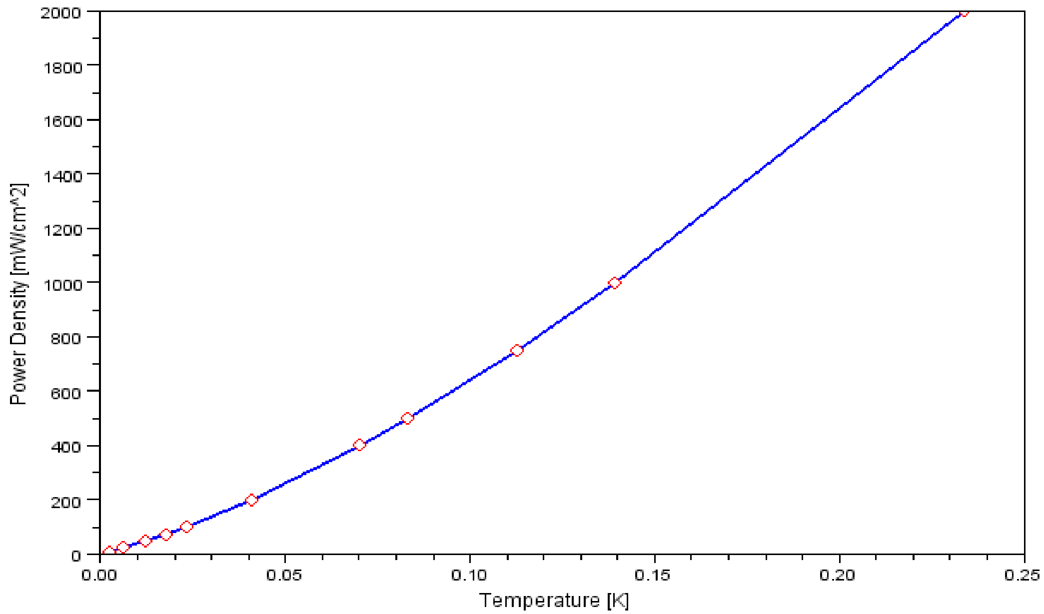


Figure 4-7 Temperature rise vs. Power plot

profile of the system. Moreover the figure 4-9 shows the zoom in temperature profile of the model using a plane which passes through the center of the chip.

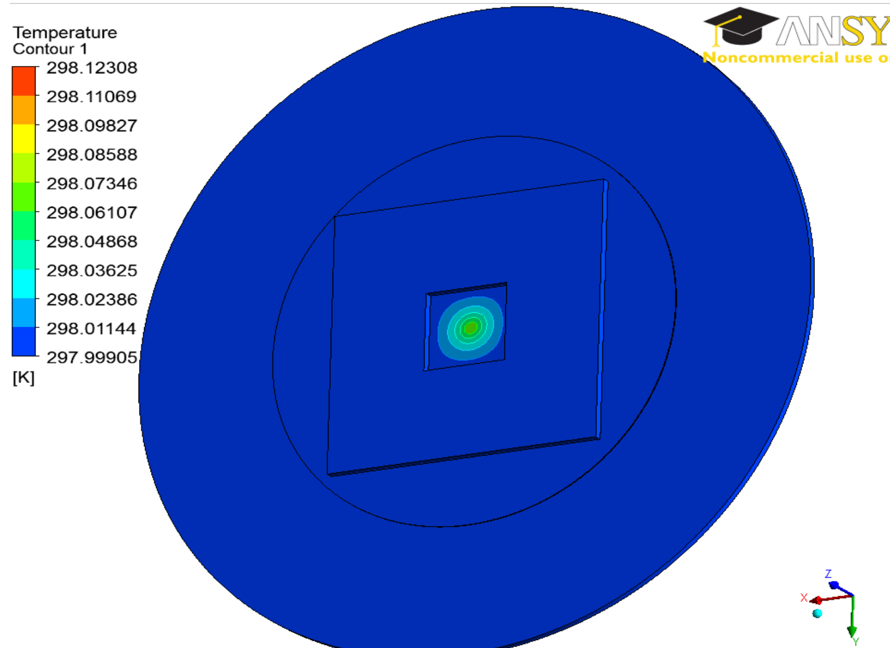
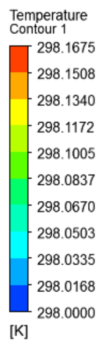


Figure 4-8 Temperature Profile



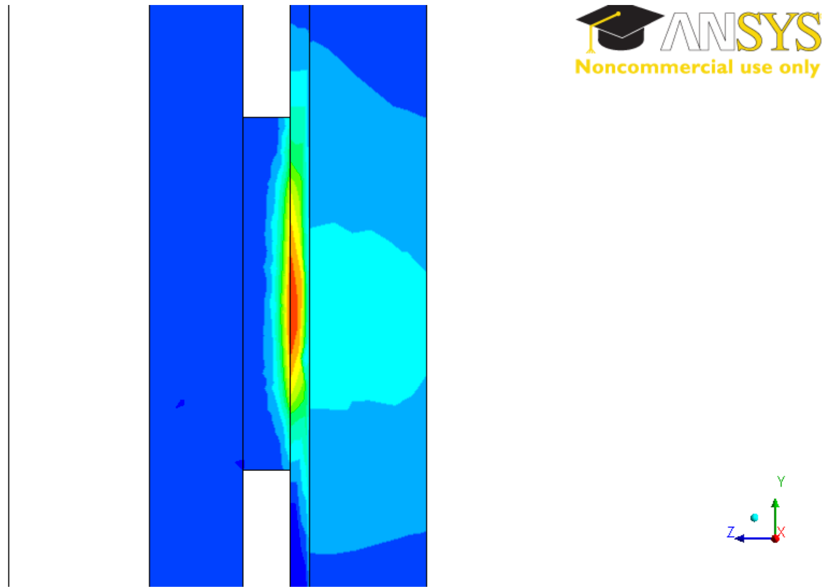


Figure 4-9 Temperature profile at center

In the next section the transient thermal simulation of the model is done to determine the best possible time and power source, the wafer should be exposed for minimum temperature rise.

4.3 Transient Thermal Analysis

The transient thermal analysis is carried out by exposing a square part of the wafer resembling chip of size 10mm x 10mm for varying time and varying power. The main aim is to determine the combination of time and power which gives a minimum temperature rise. The simulation were not only conducted to get the least temperature rise but to get an optimal solution. An optimal solution means the combination of low temperature rise and less exposure time. The exposure time is directly proportional to the productivity of the product as less exposure time means we can have more chips exposed to the UV rays in a specified time. Whereas temperature rise induces thermal

stresses over the wafer which is undesirable. The table indicates the boundary conditions and the initial conditions used for the simulation.

Table 4-3 Transient Thermal Analysis Condition

Time [sec]	Power Intensify [mW/cm^2]	Dose [mJ/cm^2]
30	10	300
12	25	300
6	50	300
4	75	300
3	100	300
1.5	200	300
0.75	400	300
0.60	500	300
0.40	750	300
0.30	1000	300

The series of experiments showed that exposed time of about 3 sec for power intensity of 100 mW/cm^2 has the optimum result. While it doesn't have a high increase in temperature also takes less time. In the above plot the optimal solution will a point which is near to the origin as it has both low temperature rise and low exposure time which occurs at a value of 100 mW/cm^2 power intensity

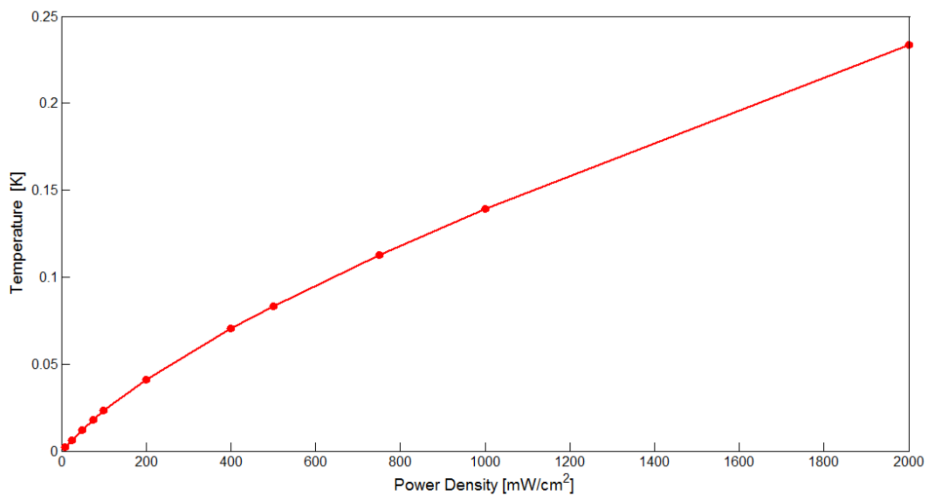


Figure 4-10 Power density vs. Temperature

In this segment, design of experiments was simulated to obtain minimum temperature rise for high power exposure. This can be done either by changing the thermal conductivity which is a material property or changing the co-efficient of convective heat transfer. We cannot change the material as silicon is the heart of the fabrication process hence we thought we changing the heat transfer co-efficient. The below table shows the results calculated by the simulation. The simulation depicted that changing the heat transfer co-efficient is not a feasible alternative, as a large increment in the value of heat transfer co-efficient is needed to get the desired value of temperature. The figure bellow shows the computed convective heat transfer co-efficient value for 1200 mW/cm^2 which is needed for getting a temperature rise equal to that of 100 mW/cm^2.

The optimization results showed that to decrease the temperature rise from 0.2159 K to 0.18927 K we need to increase the convective heat transfer co-efficient from 5000 W/m^{2}K to 106603 W/m^{2}K. So it means for a decrease of approx. 0.025 K

Table of Schematic P4: Optimization

	A	B	C	D	E
1		P3 - convectionwc (W m^-2 K^-1)	P2 - tmax (K)	P4 - tmax (K)	P6 - tmax (K)
2	Optimization Study				
3	Objective	No Objective	No Objective	Seek Target	No Objective
4	Target Value			0.18927	
5	Importance	Default	Default	Higher	Default
6	Candidate Points				
7	Candidate A	1.0663E+05	0.24189	0.18929	0.2665
8	Candidate B	1.5605E+05	0.24189	0.18183	0.2665
9	Candidate C	2.0548E+05	0.24189	0.17648	0.2665

Figure 4-11 Convective Heat transfer co-efficient optimization

temperatures we need to increase the convective heat transfer co-efficient about 20 times. Hence this optimization was insignificant.

Chapter 5

Modeling and Simulation of Multiple Chip

In this previous chapter modeling of a single chip over a wafer is discussed but in industry multiple chips are fabricated over a single wafer. In order to understand the basic temperature profile of the wafer while fabrication, the previous simulations were conducted. This chapter discusses the various simulation conducted with multiple chip being exposed over a period of time with the understanding of the previous chapter. The material properties and materials used for the various components of the process are same as in the prior simulations.

The basic geometry which is used is similar to the one shown in figure 4-5 with the exception of multiple chips on the wafer. The detailed view is shown in figure 5-1 with the chips on the wafer. The geometry is formed by making a grid structure resembling

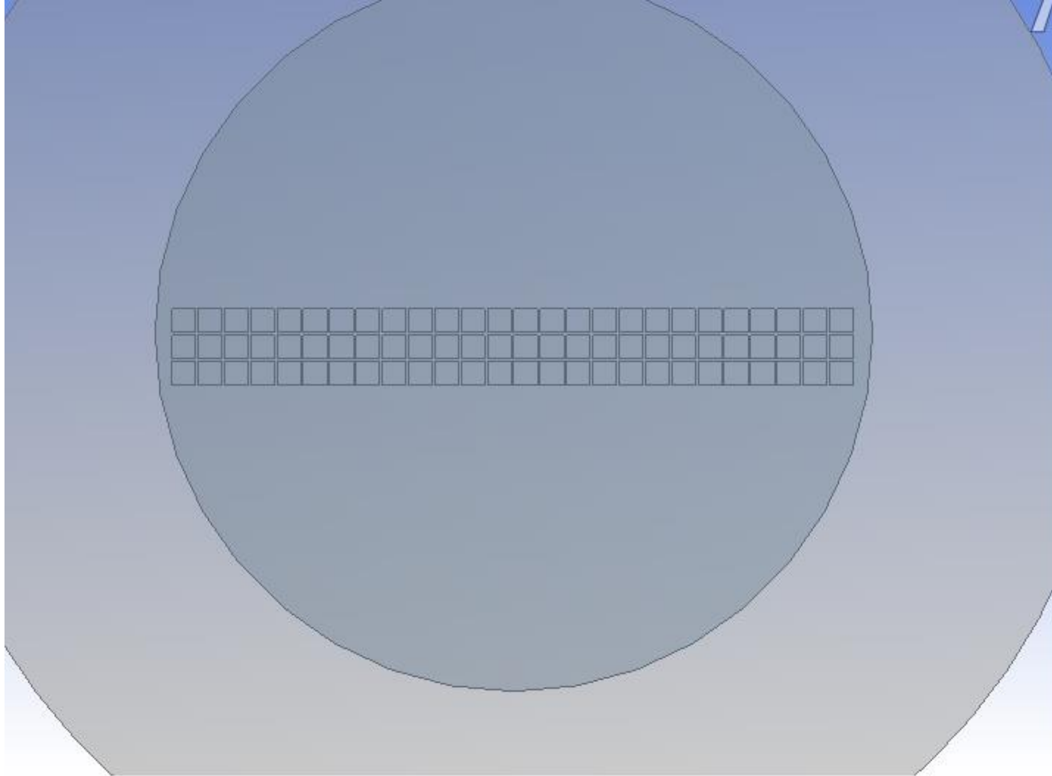


Figure 5-1 Multiple chips on Wafer

chips to be patterned on the wafer. The dimension of the chips is 10mm x 10mm and they are 1mm apart. For a better view the template and the template chuck is not shown.

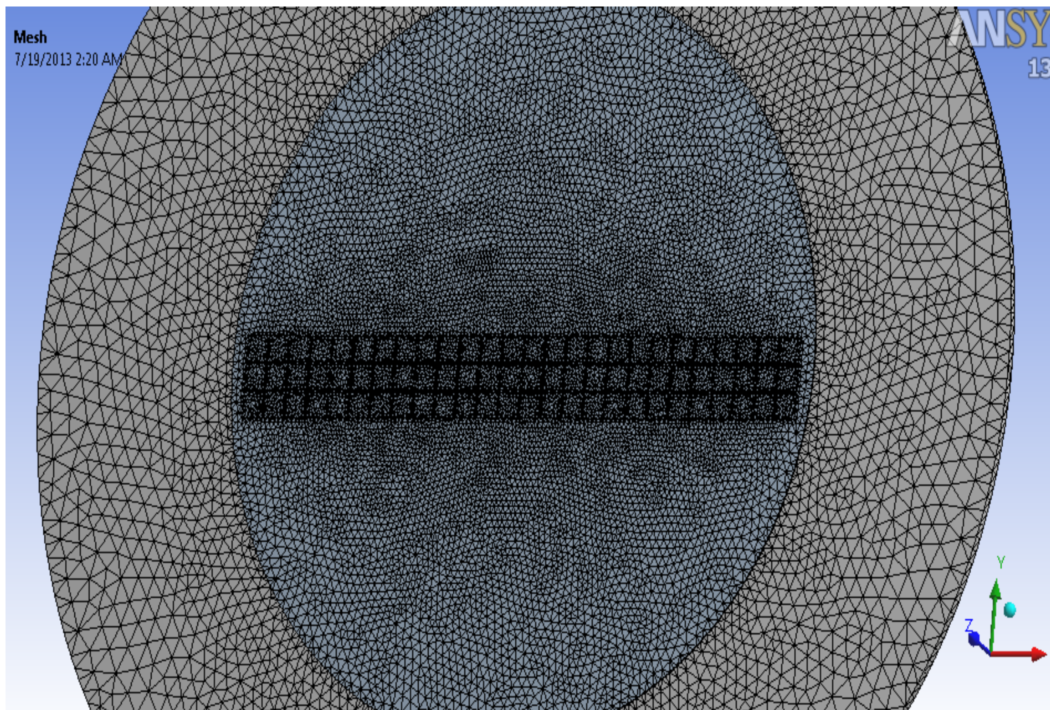


Figure 5-2 Mesh view in Multiple chip on wafer

The experiments were design in order to get a sequence of exposing which trade-off between the path travelled and the rise in temperature. From the figure shown above, it can be seen that the, if we expose the chips in horizontal or vertical straight way it will be the least displacement path. But the same thing cannot be said for the temperature rise will not be a linear function of exposure time only but the exposure of the adjacent chip will also affect in this case. Now, for the understanding of the temperature profile while exposing multiple chips over a wafer, the simulation is performed with two different setups. The various setups are discussed in the later section of this chapter.

5.1 Exposure of 7-chips at the center of the wafer

In this section , the simulation based on considering seven chips out of the grid as shown in figure 5-1 are discussed. . The goal of performing the simulation considering seven chips is to understand the effect of power intensity of adjacent chips to the temperature rise. The results of tis experiments are then validated in the following experiments. The exposure time and the power intensity for all of the seven chips are same so that there is a consistency in the experiment.

The order for exposing the seven chips is done with nine different ways; all the various ways are shown in the following nine figures. The sequence is also specified in the figure. The chip with number 1 means it is the first one to be exposed with the UV

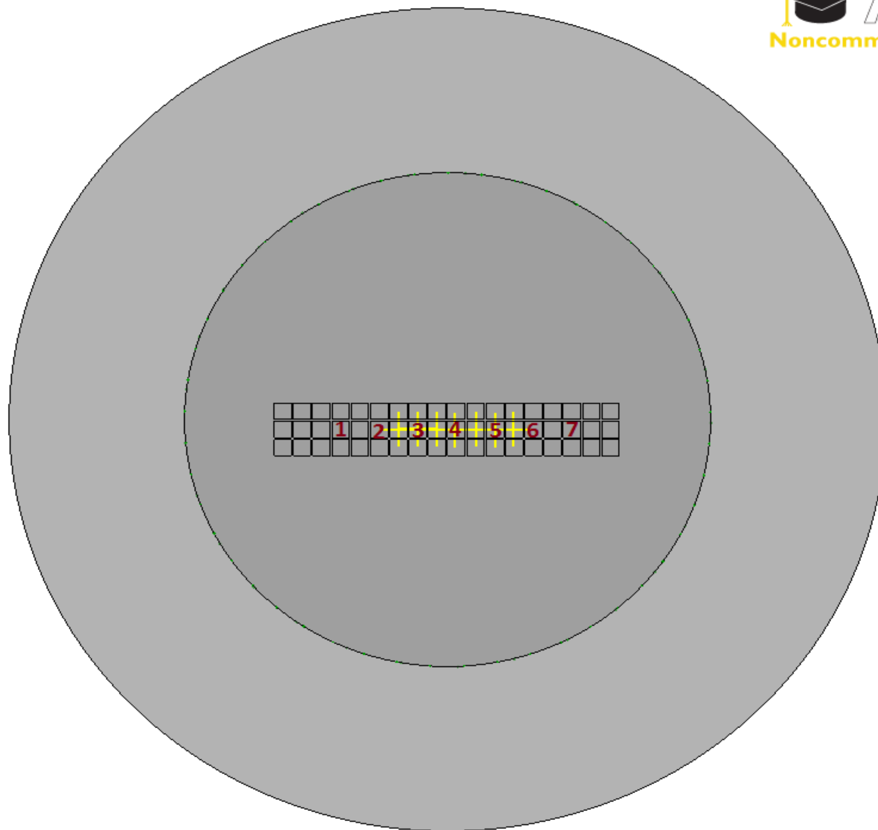


Figure 5-3 Sequence for multichip 1

rays for the lithography process and follows in chronological order up to number 7.

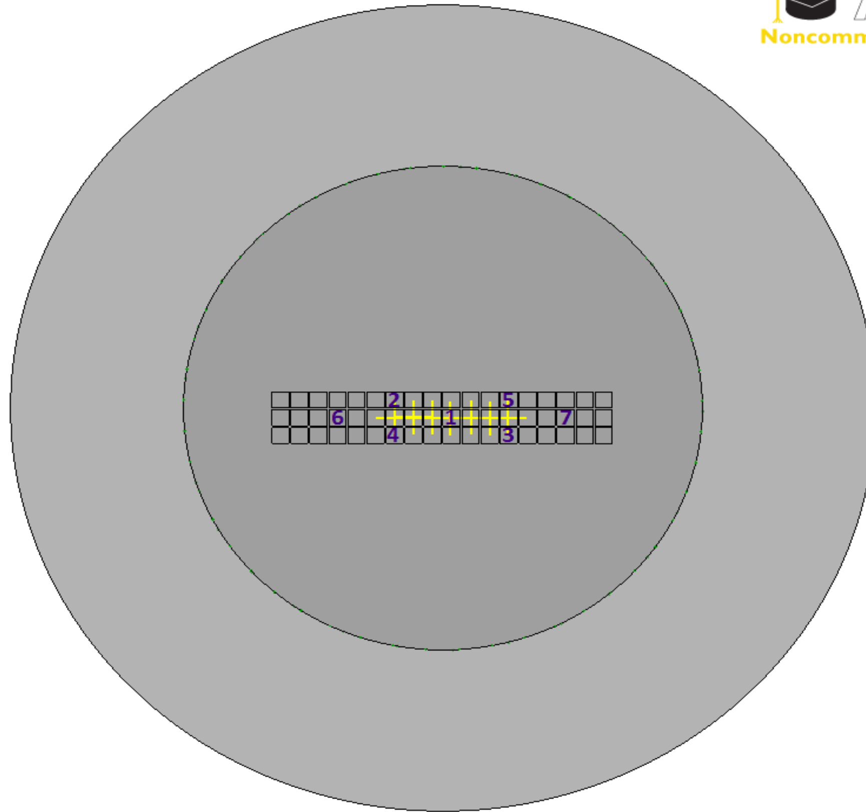


Figure 5-4 Sequence for multichip 2

The figure 5-3 shows the sequence used for exposing the chips. In this the chips are exposed by skipping the adjacent chip. The sequences are randomly chosen to find the relation between the path travelled and temperature rise which is discussed in the next chapter. Also figure 5-4 explains the second type of sequence which is used. In this design the chips are exposed far apart which increases the path travelled by the beam which is used to bombard the UV rays on the chips.

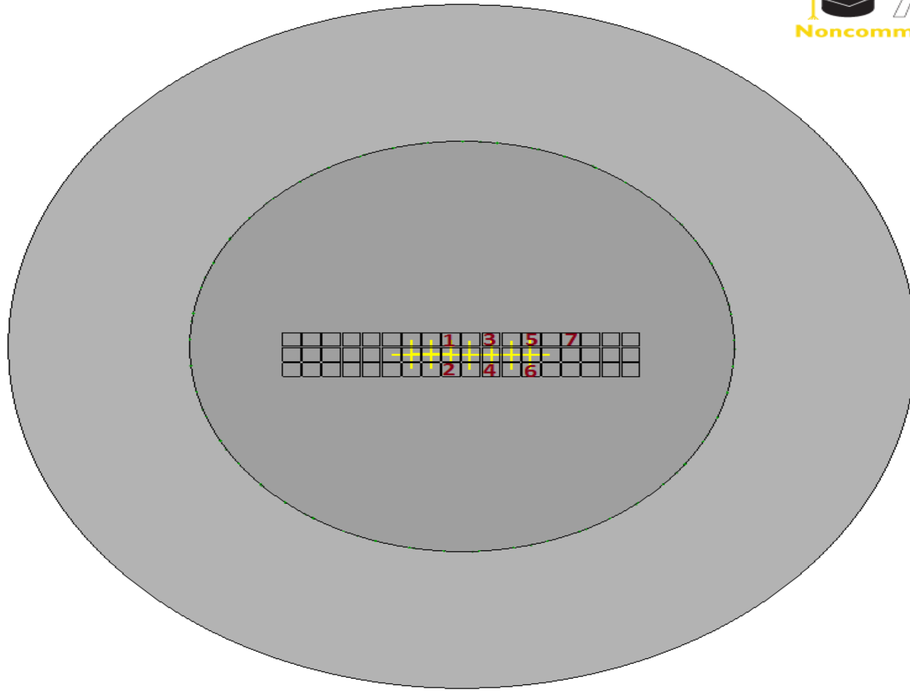


Figure 5-5 Sequence for multichip 3

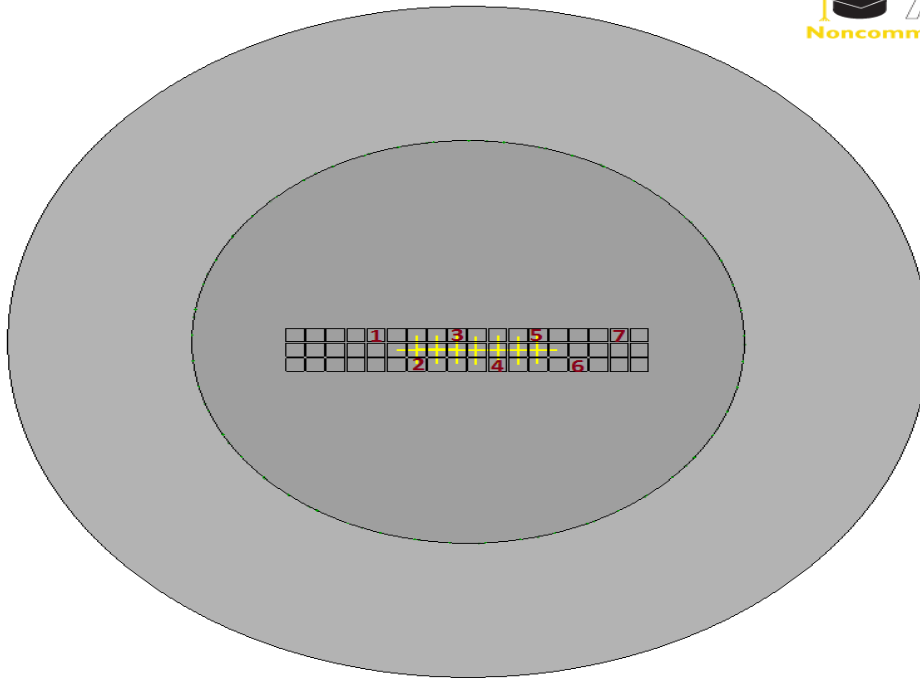


Figure 5-6 Sequence for multichip 4

Similarly the third sequence is shown in figure 5-5 which is at the top of the previous page. In the next figure the chips are exposed diagonally to each other just to get a different value of the path travelled.

Whereas in figure 5-6 a linear sequence is used but the exposure of the chips is not done in chronological order a random sequence is used for the purpose of experimenting to calculate the temperature variation if the exposing sequence is changed.

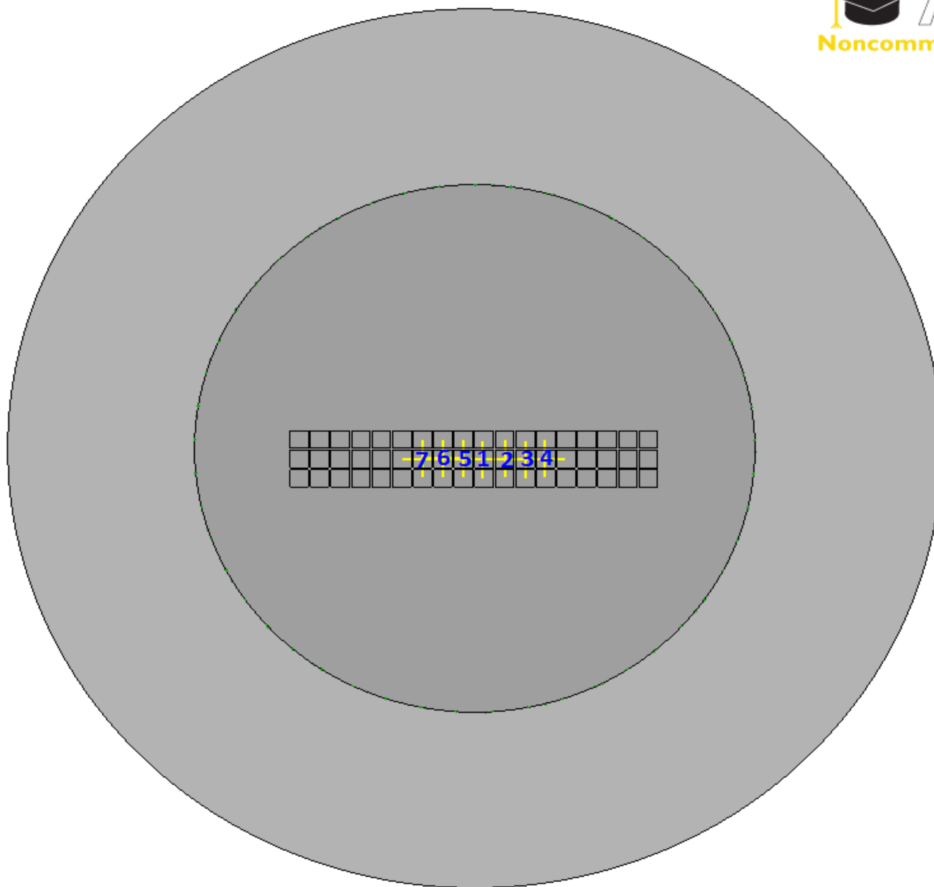


Figure 5-5 Sequence for multichip 5

Noncommerc

Figure 5-6 Sequence for multichip 6

The figure 5-8 shows that the chips are closely packed and are exposed one after other, though the path travelled in both figure 5-8 and 6-9 will be same but in figure 5-8 the temperature of adjacent chip will have more effect than the sequence shown in figure 5-9. In figure 5-9 the exposure is done in a linear pattern unlike the cluster type set uo in the above figure. The figure 5-9 is shown in the next page.

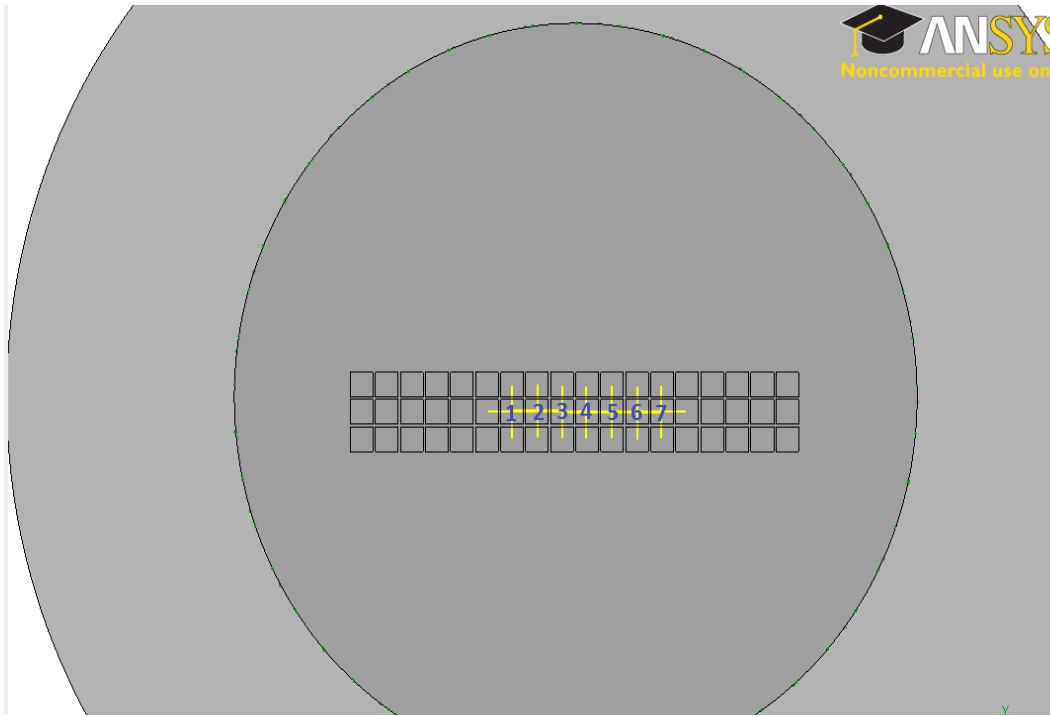


Figure 5-7 Sequence for multichip 7

5.2 Exposure of 9 chips at edge of the wafer

In this segment after concentrating only at the center part of the wafer , this part deals with the comparison of temperature profile if the exposure is done at the edge of the wafer. The exposure is done in 6 different patterns. The patterns were created using random sequence generator function in MS Excel. The sequences which are used are shown below in the table. The exposing sites were numbered from 1 to 9 and then were exposed according to the sequence. Moreover Figure 5-10 shows the basic geometry used for computing the simulations.

Table 5-1 Sequence for Exposing 9 chips

Serial No.	Sequence	Displacement [mm]
1	9-1-6-8-3-7-5-4-2	319
2	1-7-4-8-6-5-9-3-2	297
3	3-7-6-2-8-5-4-1-9	308
4	6-5-7-1-3-8-9-2-4	286
5	4-9-3-5-6-2-8-1-7	407
6	1-2-3-4-5-6-7-8-9	88

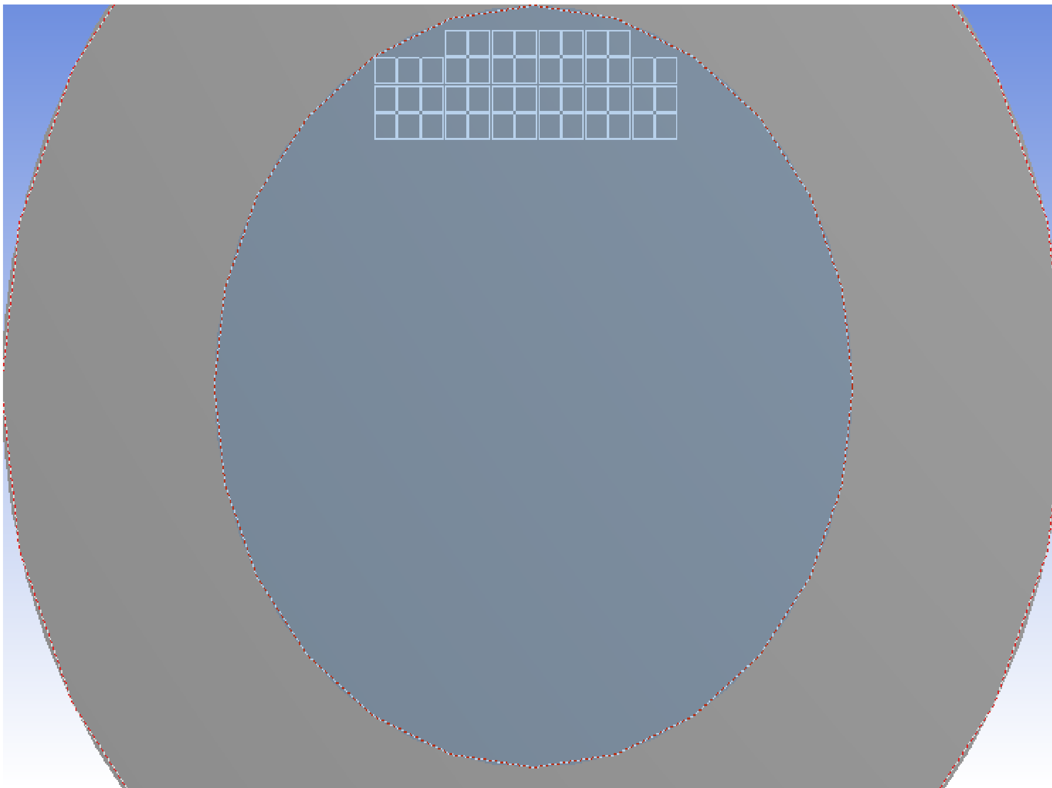


Figure 5-8 Geometry for 9 exposed sites

Chapter 6

Results and Conclusions

6.1 Thermal Results

In this chapter the results of the simulations are discussed and conclusions are drawn. The thermo-mechanical simulations are completed using different ste ups to understand the temperature profile. The figure 6-1 shows the results of the multichip sequence 7, it can be seen that the hot spot is only at the chip which is exposed but it has a effect on the adjacent chip also.

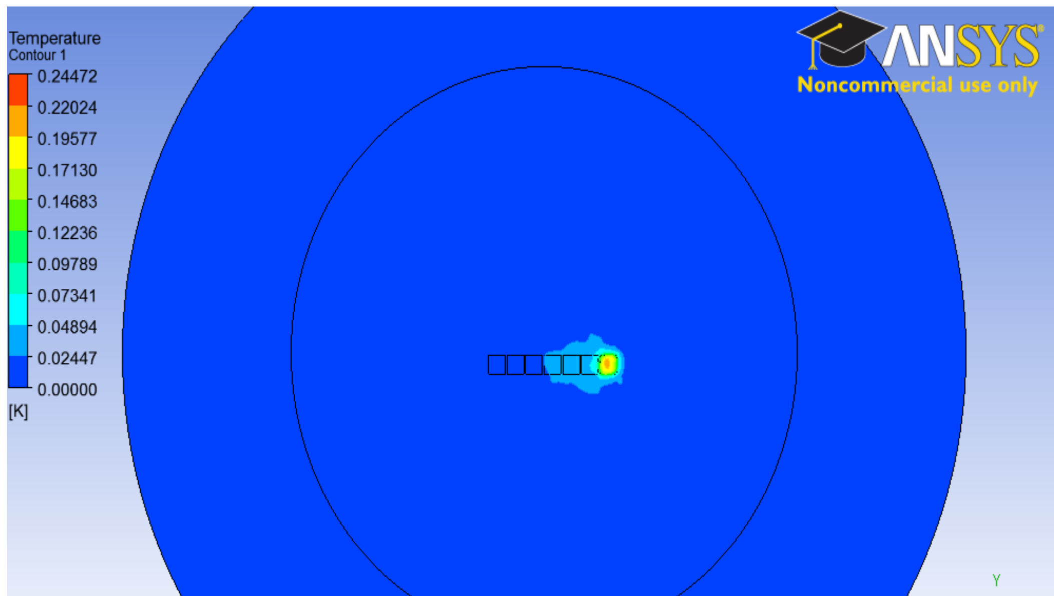


Figure 6-1 Temperature Profile for sequence 7

It can be seen from the figure how the temperature profile spreads over the wafer. Though the chips adjacent to the one with the hot spot are not exposed but due to the heating of this chip there is a temperature gradient in them. This temperature gradient induces thermal stresses. The temperature profile for the exposure sequence 6 is shown below.

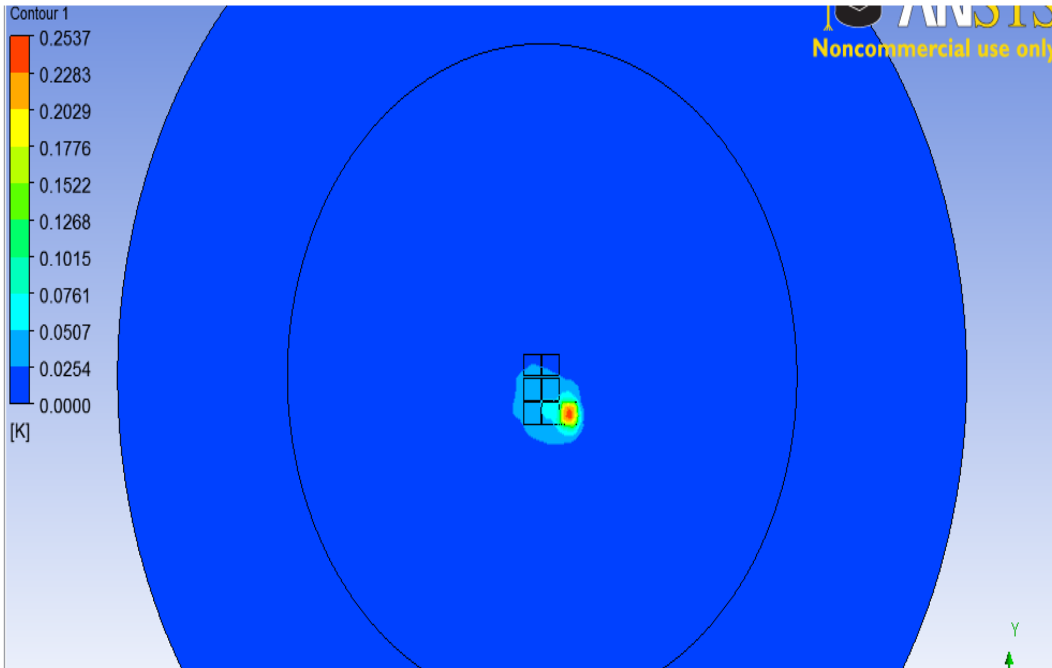


Figure 6-2 Temperature Profile for sequence 6

The temperature profile for this is spread over a larger area of the wafer than in figure 6-1. The displacement for both sequence 6 and sequence 7 is same but the temperature profile is different. Moreover the rise in temperature is also greater in sequence 6 as the effect of adjacent chip is prominent in the sequence 6.

The figure 6-3 is of sequence 2 in which the exposure of the chip far apart is done. The temperature profile is similar to that of exposing a single chip as the chips are so much apart that there is no effect of the adjacent chips. Hence the temperature rise is also the least among all other sequence. The figure 6-4 shows the temperature profile of sequence 4 which has displacement between the sequence 6 and sequence 2.The comparison of all the sequence is also done and an optimal point can be observed in the plot below.

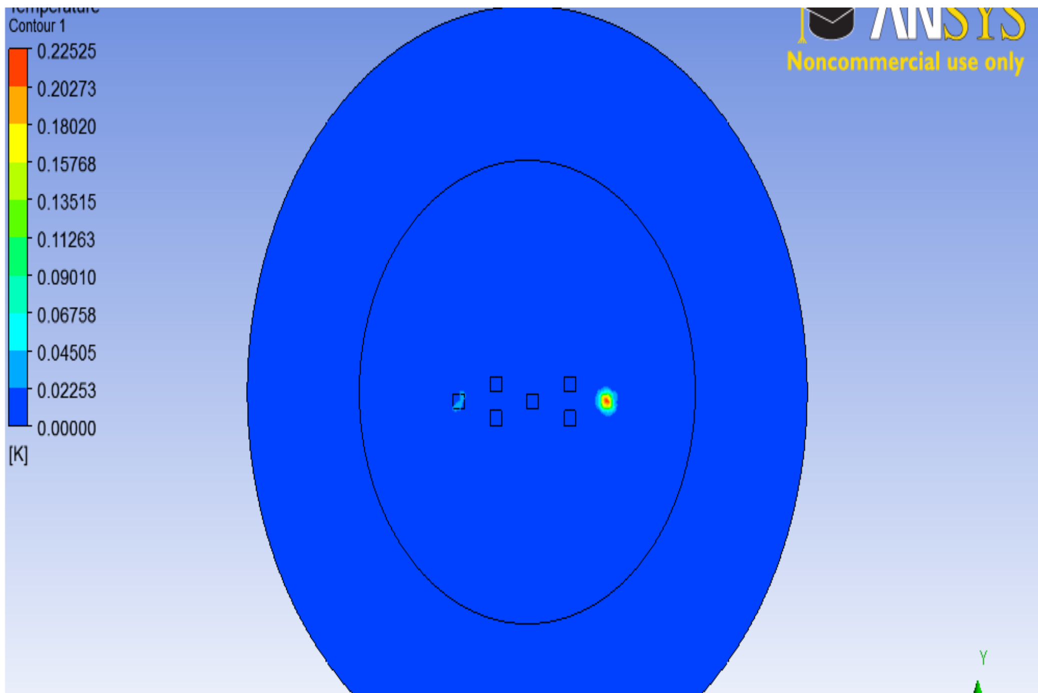


Figure 6-3 Temperature Profile of sequence 2

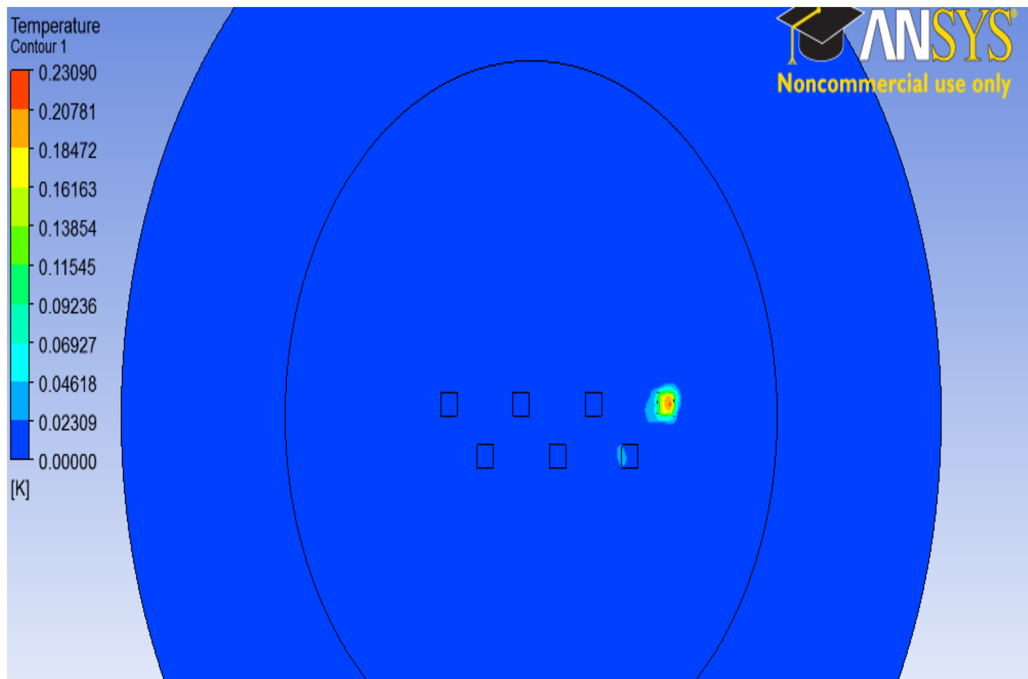


Figure 6-4 Temperature Profile of sequence 4

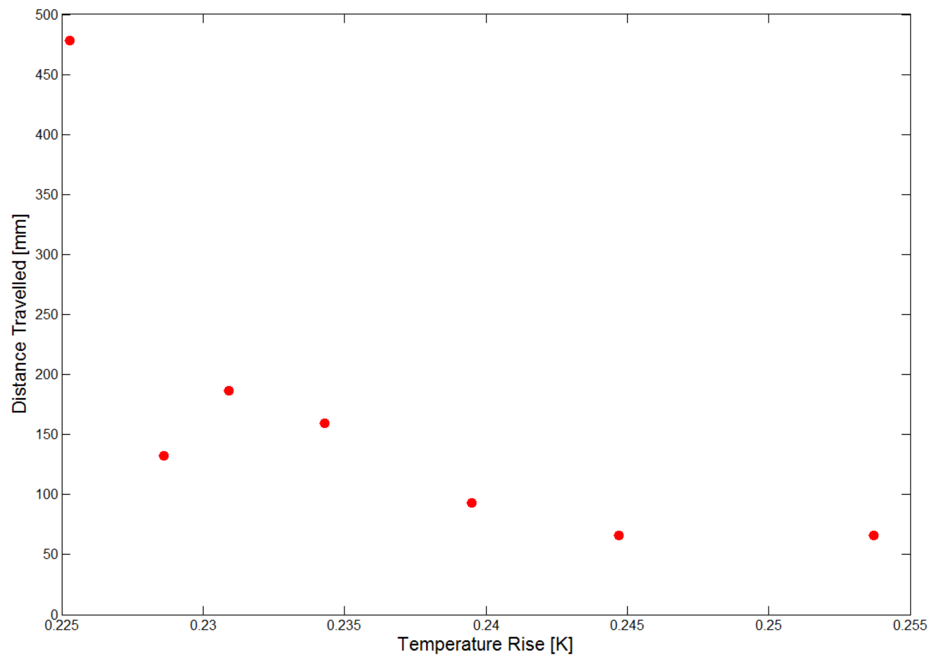


Figure 6-5 Temperature vs. Displacement plot

From the plot it is observed that as the displacement increases the temperature rise decrease. But the optimal point is the one with less displacement having less temperature rise. The optimal point on the ploy refers to the one which is at the bottom left. This point is refers to sequence 1.

In this section the temperature plot of the simulation computed using exposure at the edge is explained. The exposure at edge provides the similar temperature profile over the wafer which is shown in figure 6-7. The plot in figure 6-6 explains the nature of relation between the total displacement of the template chuck and the temperature rise of the wafer. From the plot it was observed the best sequence among the simulated one was the linear sequence as it is shown by the point near to the origin.

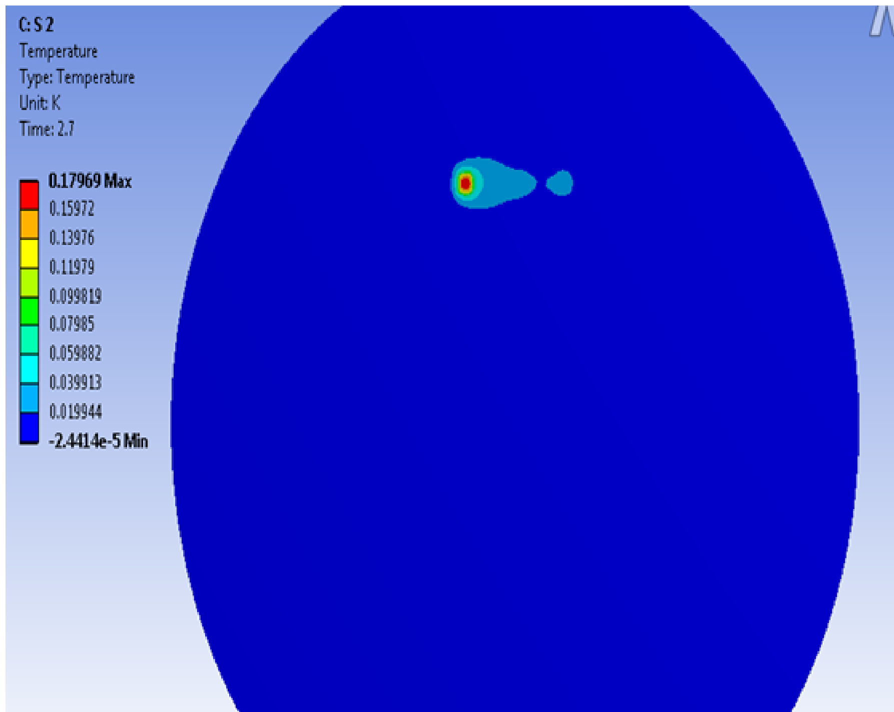


Figure 6-7 Temperature Profile for exposure at the edge

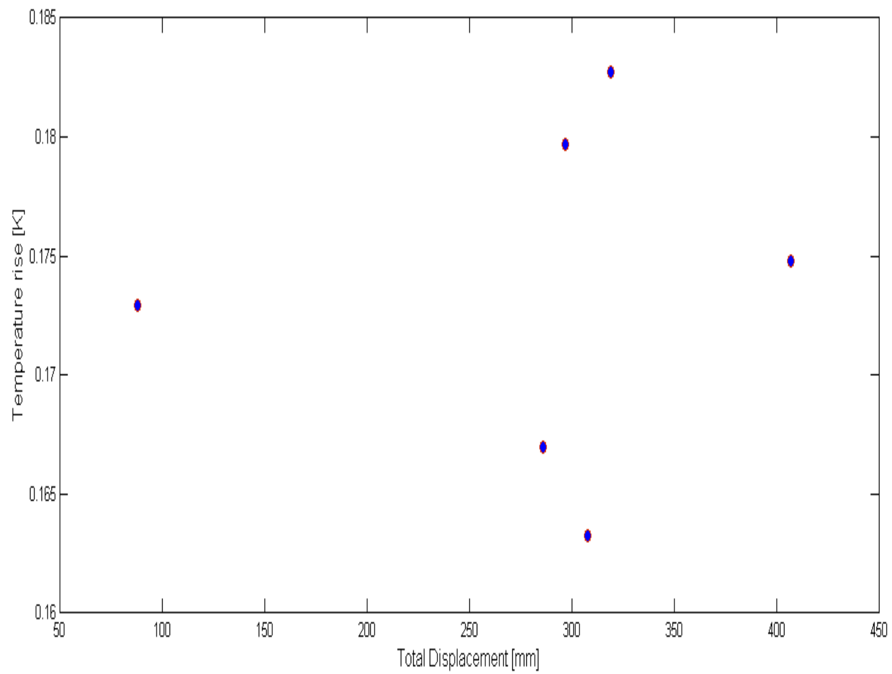


Figure 6-6 Plot for exposure at the edge

6.2 Structural Results

In this section the structural results are discussed obtained using the temperature loading obtained from the thermal simulations. The plot below shows the relation between the stresses, temperature and power intensity for a single chip. The plot shows a linear relation between the thermal stresses and the temperature rise. So it can be concluded that as temperature increase the stresses also increase.

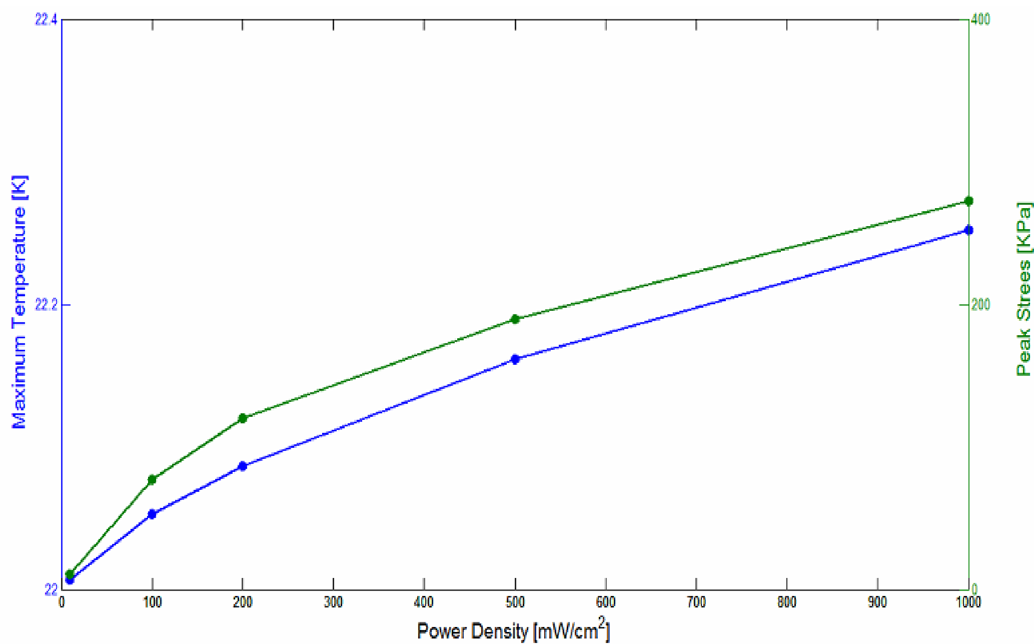


Figure 6-8 Plot of Power density vs. Temperature vs. Stress

Unlike the single chip exposure we did not obtained linear plots for the multichip exposure. The plots have different nature and have optimum points which were our goal at the beginning. The stress profile is also been shown in figure. The point which is closes to the origin is selected as the best candidate based on the criteria having least displacement and minimum stress value.

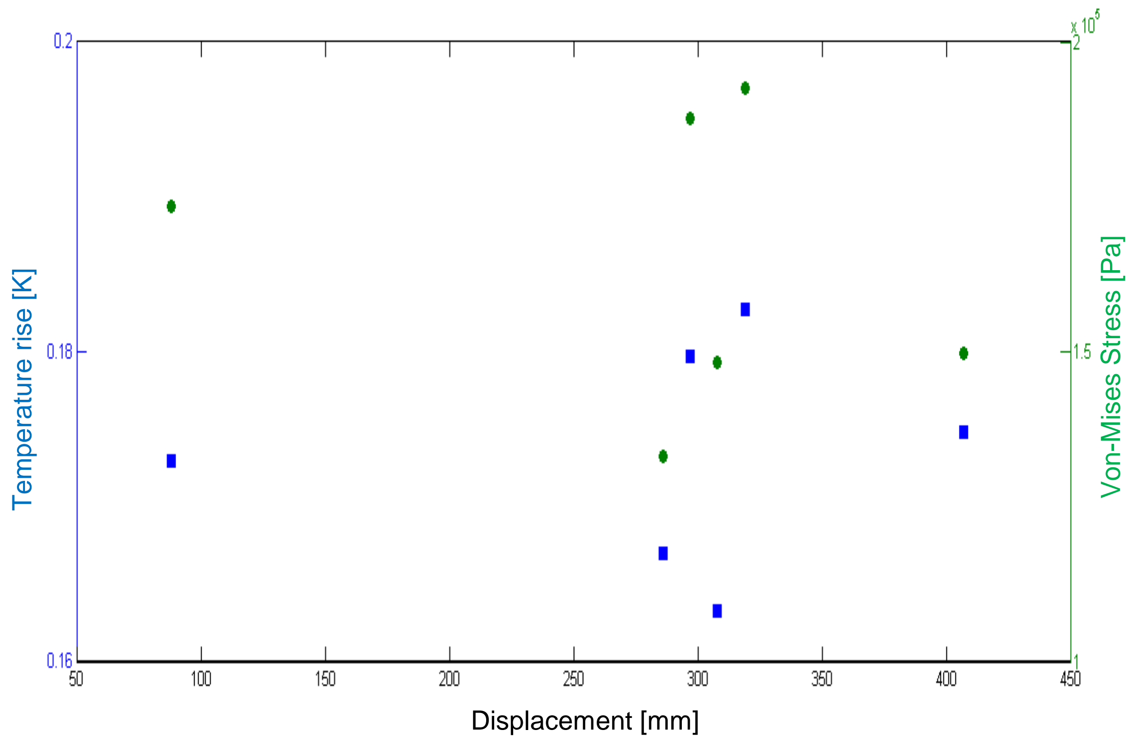


Figure 6-10 Plot for exposure at the edge of the wafer

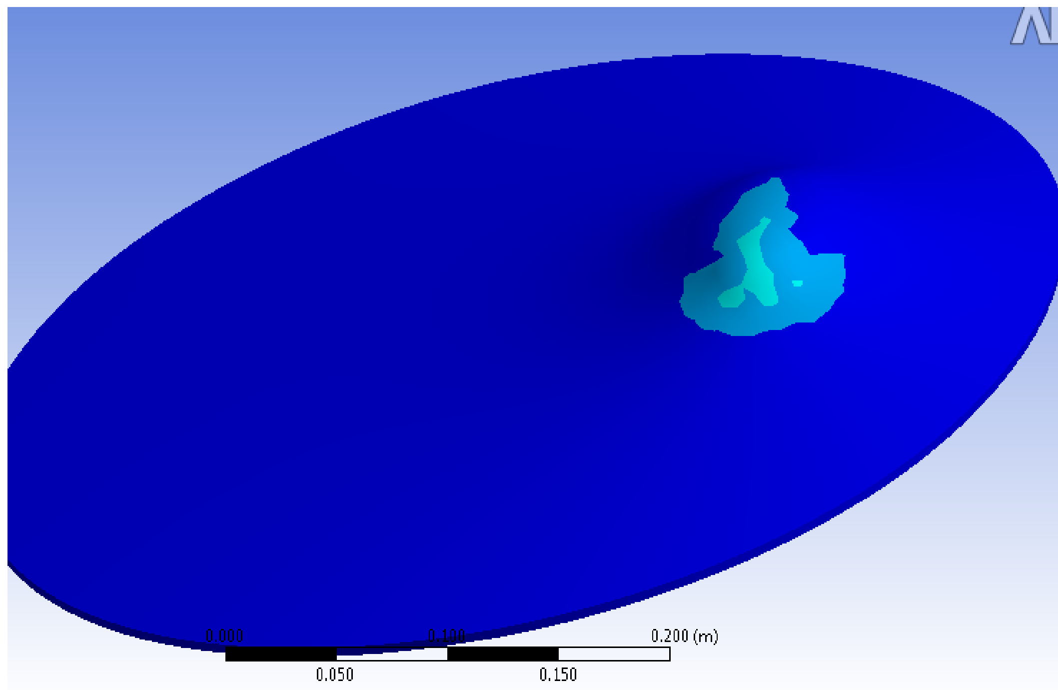


Figure 6-9 Stress profile for exposure at the edge

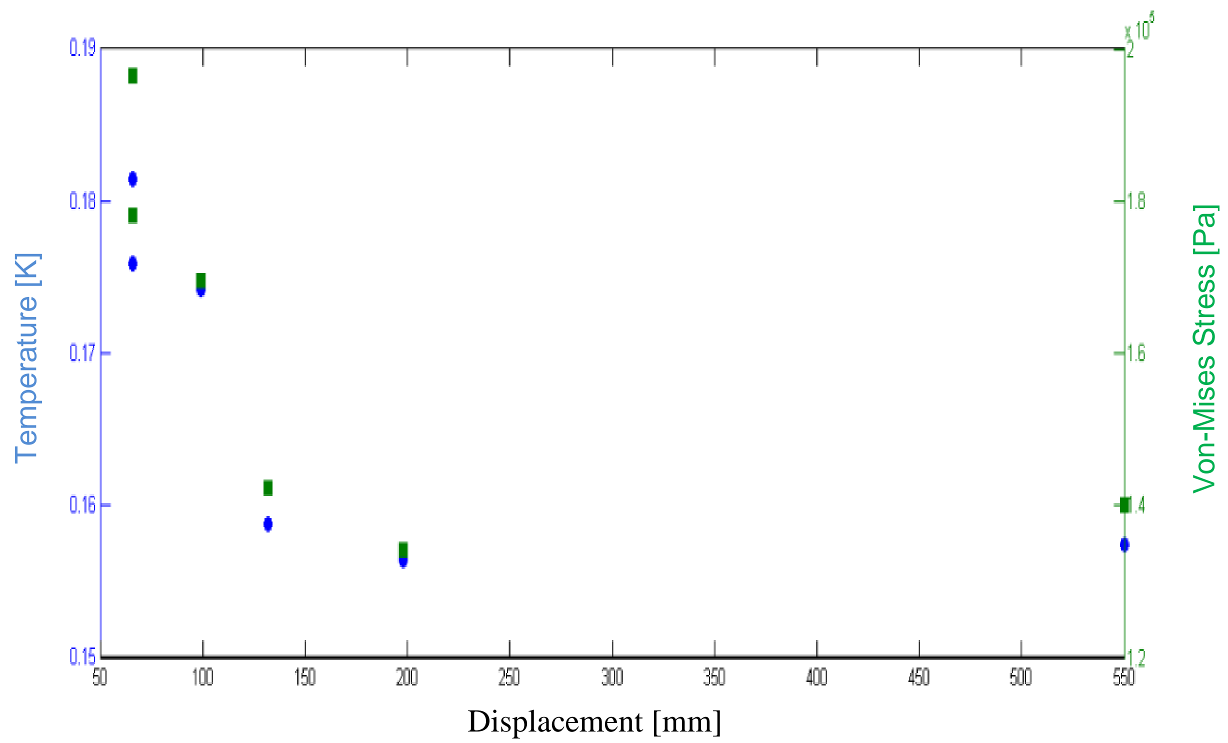


Figure 6-11 Plot for exposure at the center of the wafer

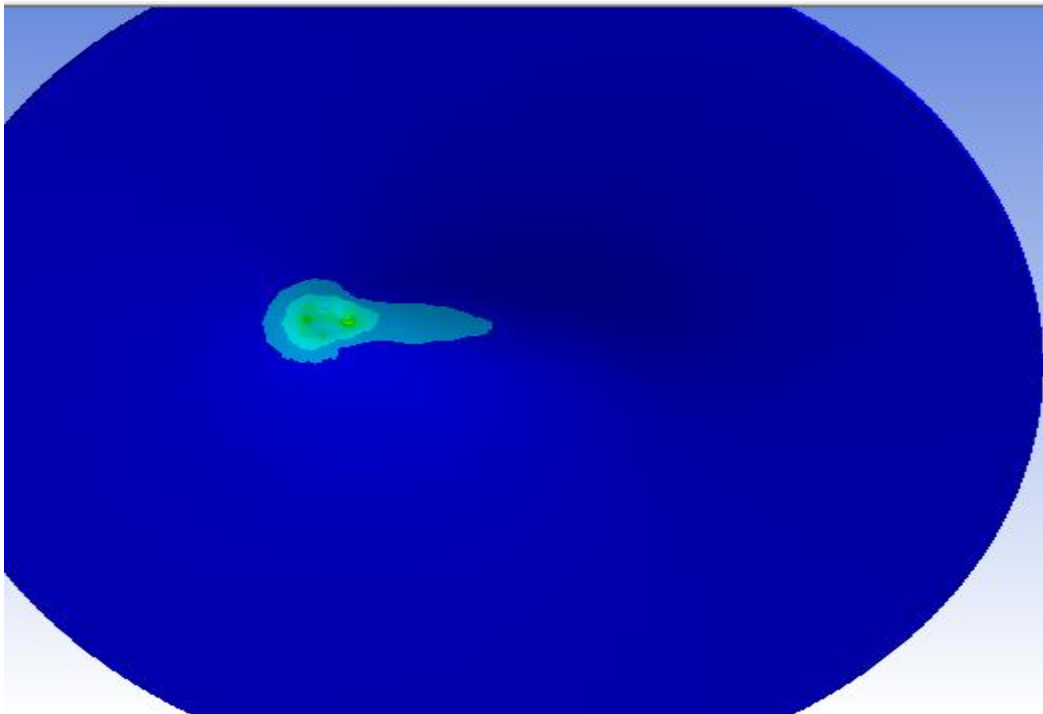


Figure 6-12 Stress profile for exposure at the center

In this section the final results and conclusion are mentioned, the sequence which satisfy the criteria for optimal solution are as follows

- The optimal sequence for the chips exposed at center

  1-0-2-0-3-0-4-0-5-0-6-0-7

- The optimal sequence for the chips at the edge

  Linear sequence

6.3 Future Work

This section provides the information about the future work that can be expanded based on the results obtained from the completed simulations. The results obtained for the muti-chip exposure are based on 7 and 9 chips being exposed, which can be further expanded for the whole wafer full of chips. This way it will provide us more detailed information regarding the temperature profile and stresses induced on the wafer. The computational of the induced stresses can be used to predict the life of the chip considering other factors.

Moreover while considering the power intensity the monomer absorption of the wafer template is not considered. So this can be considered, as if there is a miss-match the procedure will not have any fruitful results. Experimental validation will also be a challenge to perform but will be an important development towards the optimization of the process.

Moreover the melting time and molten depth are not considered. The melting time where means the time required for the monomer to melt in order to replicate the pattern on the mold or template. Molten depth is the depth required on the pattern that is created on the wafer to put transistors and other electronics devices. The molten depth does not play significant role in the simulation as the whole set is stationary but the melting time will provide the exact time for the simulations to be computed. The above work will provide a better understanding of the optimization process required in Nano-imprint Lithography.

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