NANOMEMBRANE SURFACE EMITTING LIGHT SOURCES

by

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ABSTRACT

NANOMEMBRANE SURFACE EMITTING LIGHT SOURCES

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Crystalline semiconductor nanomembranes (NM), which are transferable, stackable, bondable and manufacturable, offer unprecedented opportunities for unique electronic and photonic devices for vertically stacked high density photonic/electronic integration, high performance flexible electronics and flexible photonics. High quality single crystalline silicon NMs (Si NM) have been transferred onto various foreign substrates, such as glass and flexible Polyethylene terephthalate (PET) plastics, based on low temperature transfer and stacking processes, developed by various groups. In the last few years, significant progress has been made by Ma's group on record high-speed flexible electronics, and high performance flexible Germanium (Ge) photodetectors, based on transferable Si/SiGe NMs. Many excellent results have also been reported by Lagally and Rogers's group on the unique electronic, photonic and thermoelectronic, and mechanical properties associated with this new class of inorganic flexible semiconductor membrane material systems. In this thesis, the design, fabrication and characterization of these following unique photonic devices, with focus on the NM broadband reflectors both on SOI and glass substrates, flexible crystalline InP NM LEDs arrays on PET substrate, and membrane reflector vertical cavity surface emitting lasers (MR-VCSELs) on silicon substrate, will be investigated in detail.

The single crystalline silicon membrane reflectors (MR) based on Fano resonance or guided mode resonance (GMR) effect have been designed, fabricated, characterized, and compared their measured results with calculated ones and all of them agreed very well. Importantly, all of these MRs will be employed to replace distributed Bragg reflectors (DBRs) in the conventional InP-based VCSEL and provide a very compact resonant cavity for MR-VCSELs which will be discussed later.

The flexible crystalline InP NM LEDs arrays for high performance flexible electronics and photonics have been experimentally demonstrated, transferred onto PET substrate based on low temperature transfer and stacking processes including frame-assisted membrane transfer process (FAMT), and both optically and electrically characterized.

The III-V based VCSELs on Si substrate by transfer printing technique have been designed, fabricated, and characterized. The InGaAsP quantum wells embedded in a Si-MR cavity have been performed. Unlike the conventional DBR-based VCSEL, the ultra-thin DBR-free MR-VCSELs can be bonded or transferred onto Si substrate after finishing laser fabrication that offers a very simple and agile approach to large scale photonic heterogeneous integration. Unlocked constraints in lattice mismatches and thermal mismatches, moving forward to a wide range of applications in optoelectronic and photonic devices, and integrated systems.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

In the last decade, most major breakthroughs in scientific semiconductor have focused on silicon as a photonic platform. The main reasons for integration in electronic integrated circuits and photonic integrated circuits (PICs) are performance and cost of devices. It is very well known that silicon is an indirect band gap material, and not efficient to emit light compared to other direct band gap materials such as gallium arsenide (GaAs). Many efforts tried to grow the efficiency light source materials directly onto silicon substrate, however the results of reliability still a problem due to lattice mismatch and thermal expansion mismatch of those materials and silicon [1]. Recently, by low temperature wafer-bonding III-V materials to silicon, hybrid silicon lasers have been made [2]. Another approach to integrate III-V materials to silicon is transfer printing technique developed by [3-5]. A lot of impressive devices have been successfully fabricated with this method [6-9]. Also, It provide an easy and effective way to make a large-scale integration of III-V lasers on silicon [10]. By employing well developed transfer printing technique, our target is that we would like to demonstrate the ultra-compact surface emitting lasers integrated on silicon-on-insulator (SOI) substrate. To make them compact, the top and bottom mirrors are made by only single layer of crystalline silicon based on Fano resonance phenomenon called “Silicon nanomembrane reflector”.

1.2 Photonic Crystals

A photonic crystal is a medium with different dielectric constants periodically modulated in one, two, or three-dimensional structures [11-13] as shown in Fig 1.1(a) - (c), respectively. For one dimensional photonic crystals, the materials are alternating only in one direction in this case from Fig. 1.1 along z direction shown in Fig 1.1(a), for example a distributed Bragg

reflector that is used in the conventional vertical cavity surface emitting lasers (VCSELs). For two-dimensional photonic crystals, the materials are modulating in two directions in this case along z and y directions, but do not change in x direction shown in Fig 1.1(b). One of the examples of two-dimensional photonic crystals can be imagined as square lattice of dielectric rods with infinite extent. In three-dimensional photonic crystals, the materials are modulating in all three directions such as an inverse opal structure and spheres in a diamond lattice shown in Fig 1.1(c).

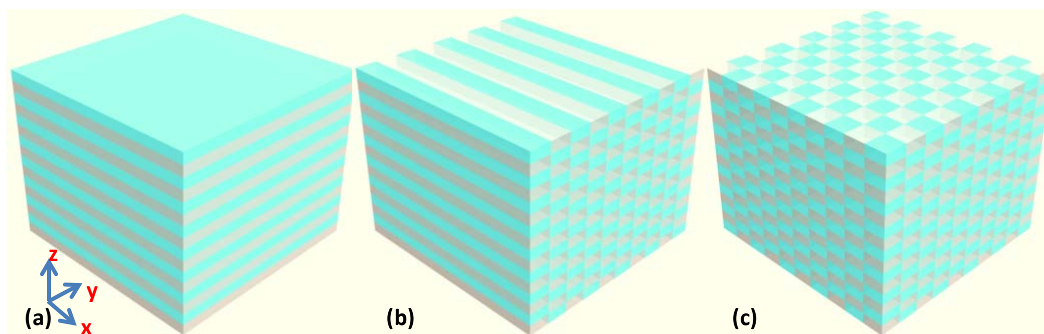

Figure 1.1 A schematic illustration of (a) one dimensional photonic crystal, (b) two-dimensional photonic crystal, and (c) three-dimensional photonic crystal.

1.2.1 Photonic Band Gap

Originated in 1987, photonic band gap (PBG) was proposed to make lasers more efficient by suppressing the waste as spontaneous light emission [14] and to create what is known as light localization by random refractive index variation [15]. In 1991, man-made three-dimensional photonic crystal (3D PC) with a complete photonic band gap was first invented by using a variant of the diamond structure called Yablonovite [16]. Owing to the challenge of fabricating nanometer scale structures at that time, it was intentionally fabricated on millimeter scales for measurements of microwave frequencies since there is no fundamental length scale in photonic crystals (PC). Like electronic band gap comprising the conduction and the valence band, PBG consists of the air band analogous to the conduction band and the dielectric band analogous to the valence band in semiconductors. Nature is always amazing. There are various

natural photonic crystals such as gem opal, butterfly's colorful wings, beetle wings, and peacock feathers. All of them have been investigated to take advantage of the potential of photonic crystals. Nowadays, the terminology "photonic crystal" is very well known for all researchers in this area nevertheless, many useful devices related to photonic crystal still need to be discovered.

1.2.2 Two-Dimensional Photonic Crystal Slab

Two-dimensional photonic crystal slab (2D PCS) is the finite thickness structure with two-dimensional periodicity shown in Fig. 1.2(a). Practically, this structure is most preferable to fabricate using electron beam lithography for nanometer scale features and it will plays an important role in our research project. Fig.1.2(b) shows the dispersion plot or band diagram of 2D PCS. The shaded region represents the continuum radiation modes above the light line which is the boundary between those two regions. The white region represents the discrete guided mode below the light. The GMRs are represented by ω1 and ω2.

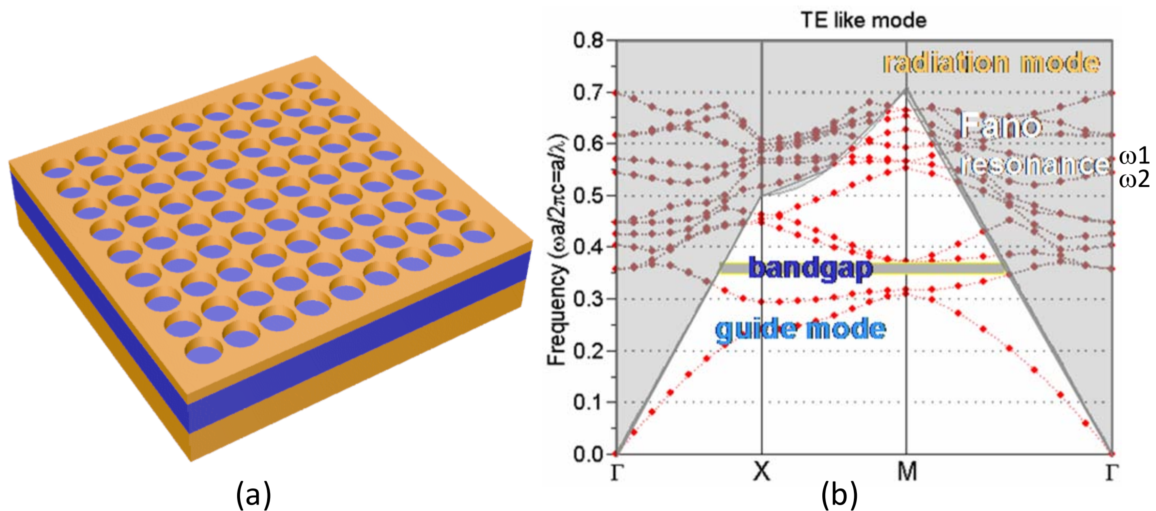

Figure 1.2 (a) Schematic illustration of schematic illustration of two-dimensional photonic crystal slab (2D PCS) fabricated on SOI wafer where top layer is single crystalline silicon and bottom is silicon substrate (brown in color) and middle layer is buried oxide (BOX) layer. (b) Dispersion relation of 2D PCS shown in (a) for the case of an infinite number of air holes. The gray region corresponds to the continuum radiation modes. The red dots correspond to TE-like guided modes.

1.2.3 Guided Mode Resonances in Photonic Crystal Slab

In 2D PCS, the in-plane discrete guided modes (TE-like or TM like) will be completely confined within the slab because the in-plane wave vector is conserved, however the out-of-plane continuum modes or radiation modes are leaky modes that can couple to external radiation so that they can provide an efficiency way to channel light from within the slab to the external environment and vise versa [16-20]. To clarify this phenomenon, as the incident wave impinge on 2D PCS, the diffracted wave can couple to the leaky modes supported by periodically modulated structure and it excites the guided mode resonances (GMR) that causes sharp variations, or broad spectrum in the wavelengths.

1.3 Photonic Crystal Slab for Si-Based Reflectors

Fano resonance effect in PC structures has been employed to fabricate membrane reflectors and these devices can be transferred onto glass and flexible PET substrates. By properly choosing the key design parameters, broadband reflectors can also be realized. it is possible to achieve >99% of reflection over 250nm spectral band and a broad spectrum cover 1550nm can be obtained owing to the GMR effect which never exist in a uniform dielectric slab.

1.4 Photonic Crystal Based Vertical Cavity Surface Emitting Lasers

In the last few years, several significant improvements in semiconductor lasers have been reported. Specifically, VCSELs which have many advantages compared to other types of lasers such as edge-emitter lasers will play an important role in the upcoming optical communication systems. The VCSEL technology can provide several benefits such as cost effective large wafer-scale fabrication and package, high coupling efficiency due to a circular laser beam directly coupled to optical fibers, and compatible integration with Si platform and much more [21], however there are many issues needed to be investigated for long-wavelength VCSELs. Although VCSEL was initially demonstrated for more than three decades ago [22], the mirror reflector is still one of the key challenges of the development of this laser. Because of high-reflectivity (> 99.5%) DBR required by lasing condition, material systems to form high

refractive index contrast alternating layers of quarter wave DBR and lattice matched to InP substrate are very rare so that it is required that a number of DBR pairs be more than 40 pairs or even higher [23]. Another problem is that the thermal conductivities of the InGaAsP / InP systems in long wavelength VCSELs is poor compared to those of the GaAs / AlGaAs or AlAs systems in short wavelength ones. Many papers have been reported to improve the thermal performance and reduce the number of required DBR pairs for long wavelength VCSEL using wafer bonding technique [24, 25] to integrate the new top and bottom DBR with the InGaAsP / InP active region. At that time, significant advance in long wavelength VCSEL has been demonstrated mostly due to the fusion-bonding technology and the improvements in the epitaxial growth techniques.

The new idea of replacing Bragg mirrors with 1D guided mode resonant (GMR) mirrors in vertical cavity lasers to increase the laser efficiency and reduce the threshold mirror reflectance needed for lasing has been proposed [26]. Recently, the first 850 nm surface emitting laser incorporating a GMR mirror called high-index-contrast subwavelength grating (SWG or HCG) has been experimentally demonstrated [27]. By effectively replacing a thick top DBR (~30 pairs) with a combination of a single layer of HCG and the rest four pairs of top DBR, the device strikingly exhibits excellent performance in terms of lower lasing threshold and higher output power compared to that of standard epitaxial growth VCSELs from the same company. It is worth to mention that this device emits only one polarization and suppresses another one because the HCG is polarization-dependent. The main reason for leaving some pairs of top DBR is to protect the active region during fabrication and from the simulation, it is confirmed that only four pairs of top DBR are not enough to provide high reflectivity for lasing. It was shown that only single layer of HCG is much better than the whole thick top DBR in terms of giving very high reflectivity exceed 99.5%. With this work, the novel VCSEL device no longer needs to rely on the thick DBR like the conventional VCSELs such that the device fabrication, the optical and thermal properties, and the stringently required the thickness of both top and

bottom DBR can be relaxed. In the same year, the compact 1.55 μm optically pumped VCSEL at room temperature using a single layer photonic crystal mirror (PCM) also has been experimentally reported [28]. Similar to a previous device, the single layer PCM is employed to replace the entire top DBR so that the compactness of the device can be realized. More recently, further work about the CMOS compatible ultra compact 1.55 μm VCSEL using double photonic crystal mirrors has been experimentally demonstrated [29]. The bottom PCM was fabricated onto SOI substrate and bonded to the active region InGaAsP quantum wells and then the top PCM was deposited.

By using the new approach for heterogeneous integration based on elastomeric stamp transfer printing developed by [3-5], we will demonstrate the novel device 1.55 μm membrane reflector vertical cavity surface emitting lasers (MR-VCSELs) by integrating III-V materials onto Si substrate [30]. With the same technology, many research publications also have been experimentally demonstrated [10, 31]. There are two major keys technologies that offer the possibility of this new device. One is the ultra compact silicon membrane reflectors (SiMR) based on Fano resonance principles in 2D photonic crystal slab (PCS) and another one is the heterogeneous integration of III-V materials with Si based on transfer printing technique. The device structure consists of GaInAaP QWs gain region sandwiched in between thin single layer of SiMR so that the device is very compact with the total thickness of 1.6 μm [30] compared to that of the conventional VCSELs which is more than 10 μm. The device has the capability to tune the lasing wavelength because of the high reflection bands of SiMRs broadly covered the emission spectrum of gain medium.

1.5 Thesis Outline

Chapter 2 introduces the SiMRs based on Fano resonance or guided mode resonance (GMR) fabricated onto SOI substrate also exhibits the capability of spectral tuning by depositing the buffer oxide layer on top of SiMR and then transfer printing technique was discussed in detail to transfer SiMR onto a foreign substrate such as glass or plastic substrate. Chapter 3

shows the crystalline InP LED arrays transferred onto flexible PET substrate including to characterization of devices under bending conditions. To demonstrate the MR-VCSELs for the first time, Chapter 4 exhibits the design, fabrication, and characterization of these novel devices in detail. Finally, concluding remarks and future research direction are presented in Chapter 5.

CHAPTER 2

MEMBRANE REFLECTORS BASED ON SILICON PHOTONIC CRYSTALS

2.1 Introduction

Surface-normal ultra-compact broadband reflectors (BBRs) are the indispensable elements of many photonics and optoelectronics device applications, such as lasers, microcavities, solar cells, photodetectors, sensors, and reconfigurable photonics, etc [32]. Two-dimensional photonic crystal slab (2D PCS) is an alternative to the conventional multi-layer distributed Bragg reflectors (DBRs) [33] ,and single layer of high contrast grating or sub-wavelength grating (HCG or SWG) structures [34, 35] that can be used as ultra-compact broadband reflectors hold great promises for a wide range of electronic and photonic device applications. However, basic one-dimensional SWG structures are intrinsically polarization-dependent. Recently, the complicated reflectors based on periodic multilayer with a multi-subpart profile grating combining with the particle swarm optimization (PSO) method [36] have been proposed for polarization independent reflectors [37]. Two-dimensional photonic crystal slab (2D PCS) structures, on the other hand, can be used to realize both polarization dependent and independent operations, with proper dispersion engineering and structural optimizations. Based on Fano resonance principles in 2D PCS, both high-Q narrow band filters and low-Q broadband reflectors can be realized for surface normal operations [17]. In recent years, devices based on Fano resonances such as narrowband filters [38-40] and broadband reflectors [41, 42] have been experimentally reported. Recently, 2D PCS based broadband reflectors on silicon-insulator (SOI) substrates has been demonstrated and reported a post-process technique for spectral-trimming of reflection band [43]. Employing a modified polydimethylsiloxane (PDMS) stamp transfer technique, the single-layer broadband membrane reflectors can be transferred onto the new host substrates, based on transferred crystalline

silicon nanomembranes (SiNM) [44]. Polarization independent reflection properties were also both theoretically and experimentally realized. In what follows, firstly, the computational methods for Fano BBRs on SOI are introduced. Secondly, the device fabrication will be discussed in detail. We consider the impact of superstrate of Fano BBRs, for spectral red-shift, by effectively increasing the refractive index above Si membrane layer. Subsequently, the device characterizations will be performed. Finally, a conclusion is given.

2.2 Computational Methods for Si-Based Membrane Reflectors

The numerical methods for the calculation of transmission and reflection spectra of membrane reflectors are based on rigorous coupled wave analysis (RCWA) [45] and finite difference time domain (FDTD) [46, 47] methods. Both techniques are very well-known for computationally solving Maxwell's equations in electromagnetic problems. On the one hand, RCWA method is applied to solve scattered fields from periodic dielectric membrane reflectors. The incident field can be a single plane wave and the diffracted fields which consist of reflected and transmitted fields will be a superposition of plane wave Fourier expansion forms or spatial harmonics. The computational solution is solved by eliminating the fields at each of the intervals between the stratums until the fields at both top and bottom of the structure can be obtained. On the other hand, FDTD method is employed to determine the response functions of the nanomembrane reflectors. Fig. 2.1 shows unit cell of dielectric material for 2D PCS. To compute the transmission spectrum from 2D PCS, the Gaussian pulse source was placed at the top of the structure just in front of the PML [48]. We calculate the flux spectrum of the Fourier-transformed electric and magnetic fields at the second monitors as shown in Fig. 2.1(a) for every point in the flux plane via summation over the recorded discrete time steps [49]. The transmitted flux through 2D PCS needs to be normalized by the incident flux without scattering structure to get the transmission spectrum. Next, computing the reflection spectrum is not straightforward since we need to separate the incident and reflected flux by subtracting the Fourier-transformed incident electric and magnetic fields to get the exact reflected flux. The simulation must be run

twice, once without and once with 2D PCS, and subtracted the Fourier-transforms in the reflected plane before computing the flux. Similarly, after the reflected power is computed, it will be normalized by the incident power to get the reflection spectrum.

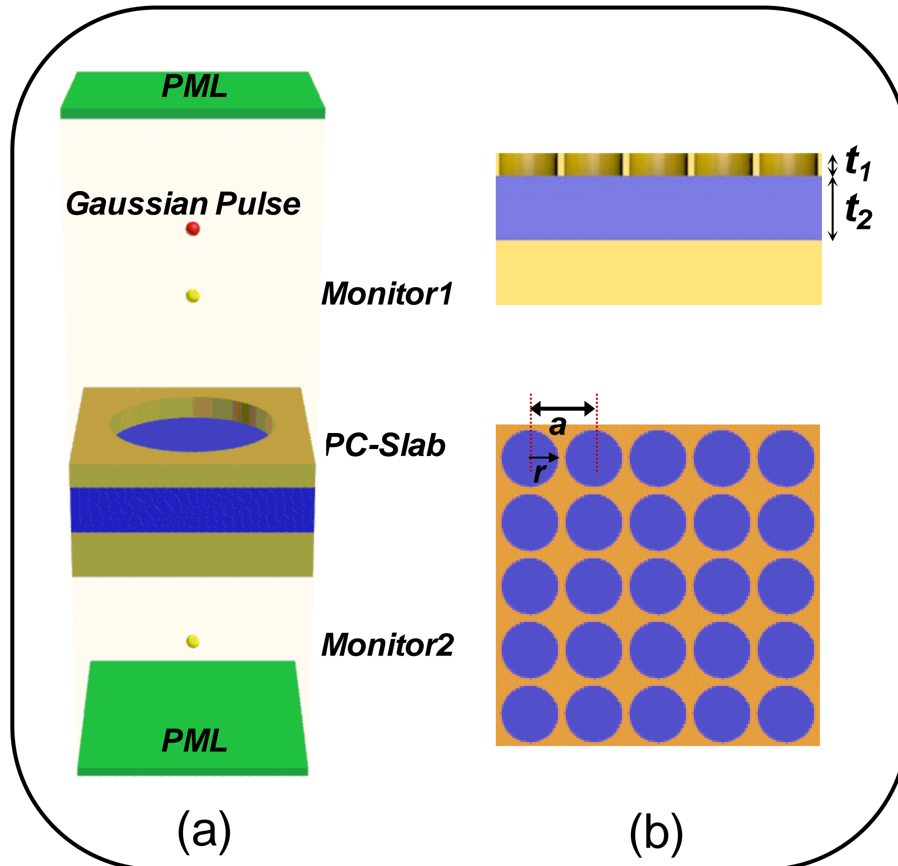

Figure 2.1 The computational unit cell of dielectric material for 2D PCS is shown in (a) top and bottom surfaces of the unit cell are perfectly matched layer (PML) as absorbing material and four sides perpendicular to the unit cell are imposed by Bloch periodic boundary condition (PBC). Design parameters of 2D PCS are shown in (b) a is the center-to-center spacing of the air holes; r is the radius of air holes; t_1 and t_2 are the thickness of top silicon (Si) layer and the thickness of buried oxide layer respectively.

By applying guided-mode resonance (GMR) or Fano-resonance effect [16, 17, 50] in periodically modulated index structures in single thin layer of dielectric medium, many useful applications can be realized such as narrow band filters, wideband polarizer, tunable filters, optical sensors, modified absorption property in solar cells and photodetectors, display pixels,

broadband reflectors and others. In this chapter, compact broadband reflectors can be fabricated with only single crystalline layer of Si with two-dimensional periodicity on Silicon On Insulator (SOI) wafer. The top layer of membrane reflector of 340 nm thick has two parts consisting of Si with the index of refractive taken to be 3.48 and air hole with the index of refractive of 1.0 and underneath layer is buried oxide of 2 μm with the index of refractive of 1.48. For simplicity, it is assumed that membrane reflectors are infinitely periodic lattice dielectric, and materials are non-dispersive (frequency independence) and lossless (non-absorption) [51] in our infrared region of interest. The key design parameters of our 2D PCS square lattice of air holes in dielectric consists of refractive index and slab thickness of considering material, lattice constant, and radius of air holes. By optimizing these design parameters, it is possible to achieve >99% of reflection over 250nm spectral band and a broad spectrum cover 1550nm can be obtained owing to the GMR effect which never exist in a uniform dielectric slab [17, 52]. In our experiment, the refractive indices of Si and SiO2 are constant as mentioned earlier and slab thicknesses of top Si and buried oxide layers also have been fixed in our case. Therefore, the remaining two parameters which are lattice constant and radius of air holes will play the important roles in designing the broadband membrane reflectors. There are two major sets of design parameters for our 2D PCS. The first configuration is classified as relatively large air hole design which has lattice constant varied from 0.85 μm to 0.90 μm and ratio of air hole radius to lattice constant (r/a) varied from 0.42 to 0.47. Another one is defined as relatively small air hole design which has lattice constant starting from 0.97 μm to 1.03 μm and r/a changing from 0.26 to 0.31 as schematically illustrated in Fig 2.1 (b).

2.3 Fabrication of Membrane Reflectors

The membrane reflector was fabricated on an SOI wafer with top silicon and buried oxide layer thickness of 340 nm and 2 μm, respectively. Because of the high resistance to dry etching, the resist thickness of 400 nm at spin speed 2600 rpm for 1 minute is enough to protect the top layer during dry etching. Pattern was defined in positive electron beam resist ZEP520A

using electron beam lithography (EBL; Joel JBX6000 system), and directly transferred into top silicon layer using chemistry reactive ion etching (RIE; Plasma-Therm's 790 series, 180-200 W RIE power, pressure 58 mTorr, 25.4 sccm gas flow rate Hbr, 4.0 sccm gas flow rate Cl_2; etching time 8 minutes).

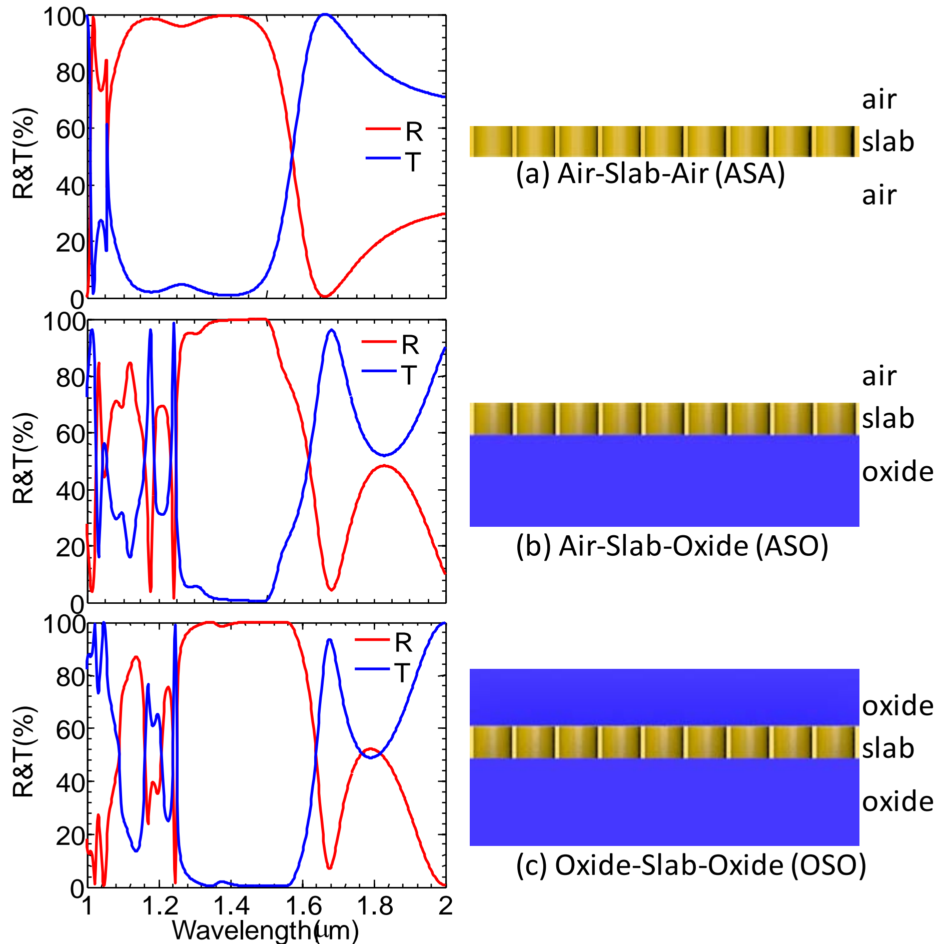

Figure 2.2 Simulated reflection and transmission spectra for different slab structures assuming incident light is perpendicular to the slab and lattice constant=0.86 μm, radius of air hole equals 0.404 μm, and slab thickness=0.34 μm for (a) air-slab-air (b) air-slab-oxide (c) oxide-slab-oxide.

Schematic illustration of different types of slab configurations is depicted in Fig. 2.2. The reflection spectral peak shifts toward shorter wavelengths by ~50 nm after the buried oxide layer (BOX) is completely removed ("ASA" shown in Fig. 2.2(a)). The spectral trimming (blue-

shift) can be obtained by chemical selectively wet etching the underlying BOX layer. On the other hand, the reflection spectral peak can be controlled toward longer wavelengths by ~50 nm after a thin oxide layer with thickness of 400 nm is placed on top surface of the SiNM ("OSO" shown in Fig. 2.2(c)). The spectral trimming (red-shift) can be achieved with either plasma-enhanced chemical vapor deposition (PECVD) of oxide, or spin-on-glass (SOG) backfilling of air region above, and inside the air holes of patterned SiNM. The reflection and transmission spectra of SiNM fabricated on SOI substrate with the lattice constant=0.86 μm, radius of air hole equals 0.404 μm, and slab thickness=0.34 μm also show ("ASO" shown in Fig. 2.2(b)).

Fig. 2.3 illustrates the transfer printing process with the elastomeric stamp. In the first instance (Fig. 2.3(a)), the small thickness of Si nanomembrane reflector on an SOI substrate has been fabricated by using electron beam lithography (EBL) and then reactive ion etching (RIE). Fig 2.3 (b) shows the selective wet etching of buried oxide layer by using the solution of a concentrated aqueous hydrofluoric acid (49% HF) and de-ionized (DI) water, at a HF:H_2O volume ratio of about 1:3 for up to about 3 hours at room temperature. After the underlying buried oxide layer has been completely etched away so that the top Si nanomembrane fell down and attached on the Si handling substrate by weak van de Waals force [5]. Contacting a soft PDMS stamp against top free-standing Si membrane leads to conformal contact. Quickly pulling the stamp away from the SOI substrate and then lifting it away from the substrate. Now, the stamp with Si membrane is brought into contact with a new host substrate. Slowly removing the stamp (Fig 2.3 (c)) causes the Si membrane to adhere to the receiving substrate and separate from the stamp. The optical image of Si nanomembrane was transferred to a new glass substrate, where it will flatten and bond as shown in Fig 2.3 (d) [5, 53, 54].

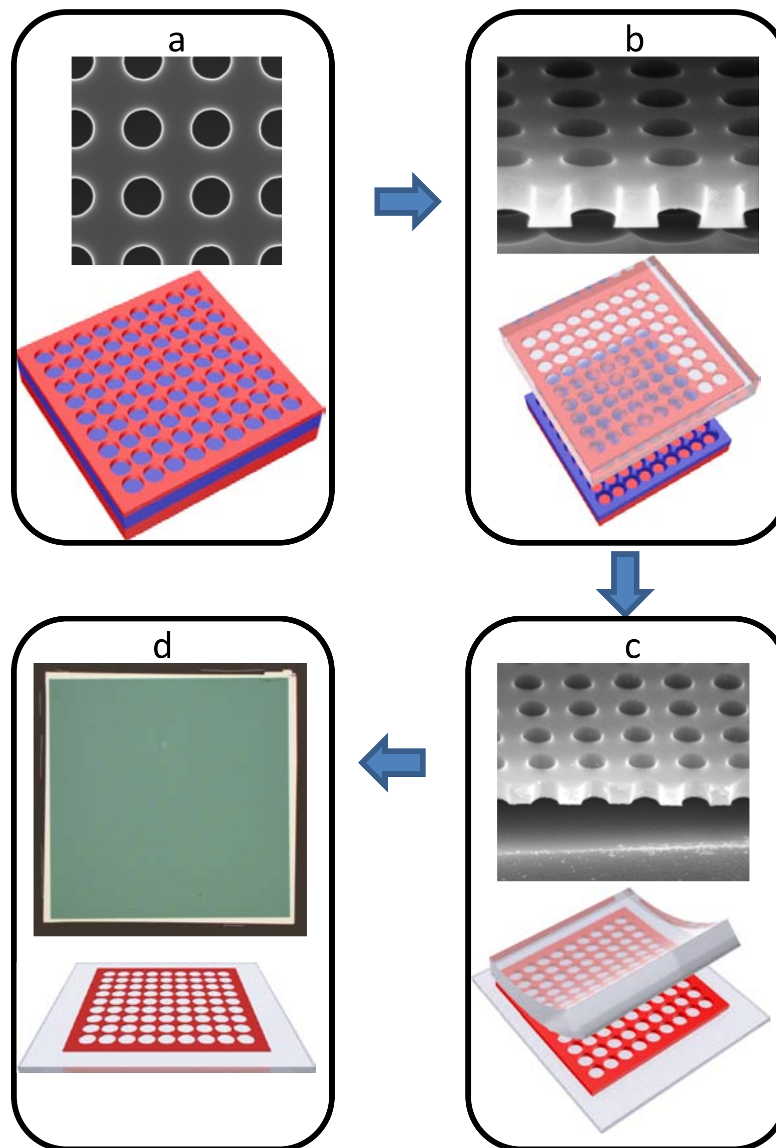

Figure 2.3 Schematic illustration of the process flow for transfer printing Si membrane including microscope and SEM images for each step. (a) Si membrane was fabricated on SOI substrate using electron beam lithography (EBL) and then reactive ion etching (RIE) for subsequent pattern transfer to top Si layer. (b) Sacrificial buried oxide layer was selectively etched away to release top membrane from a Si substrate after that laminating PDMS stamp against a substrate and then quickly peeling it away and pulling the Si membrane from the substrate onto the PDMS stamp. (c) Contacting the stamp to new host substrate and then slowly peeling it away transfers the membrane from the stamp to the receiver. (d) The Si membrane was successfully transferred to a new foreign substrate.

The 2D PCS with lattice constant equal to 0.98 μm, radius of air hole=0.28 μm, and slab thickness=0.34 μm is shown in Fig. 2.4(a) where blue curve shows the simulated result (S) and red curve exhibits the measured result (M). Both results agree very well and show the center peak at ~1510 nm. The red-shift of 2D PCS with the same key parameters is shown in Fig. 2.4(b). The center of spectral peak shifts to 1550 nm after the depositing a thin oxide layer with the thickness of 377 nm on top of 2D PCS surface as shown in Fig. 2.4(b). The measured result (M) also agrees well with the simulated result (S). The simulation results are based on RCWA simulation technique.

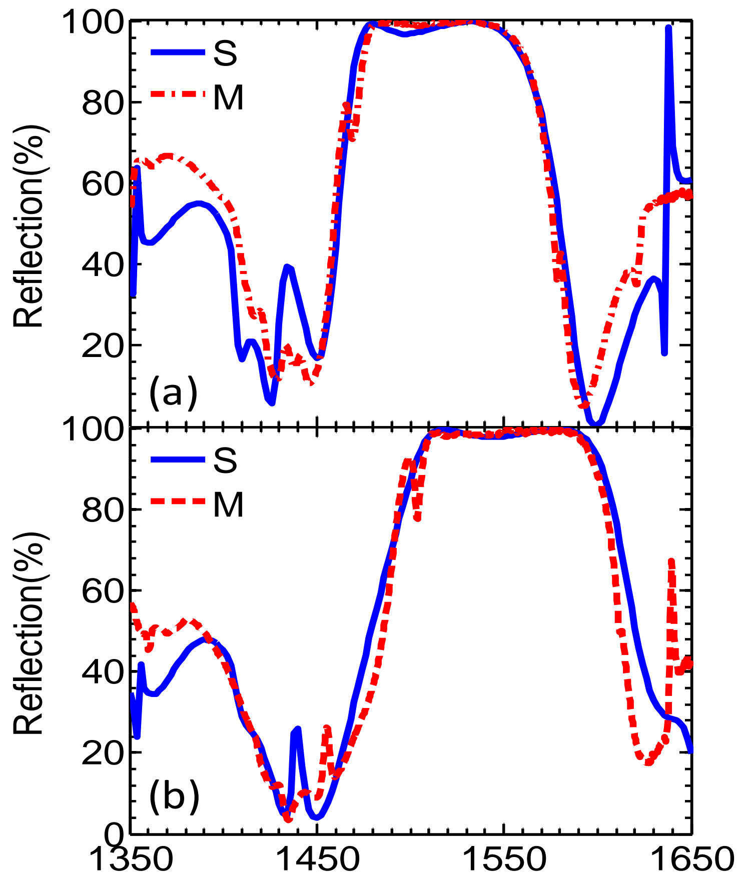

Figure 2.4 Controlled resonance of membrane reflector. Simulated (S) and measured (M) reflection spectra of surface normal 2D PCS with lattice constant=0.98 μm, radius of air hole=0.28 μm, and slab thickness=0.34 μm for (a) as fabricated on SOI substrate (b) after depositing SiO_2 with thickness of 377 nm on its top surface.

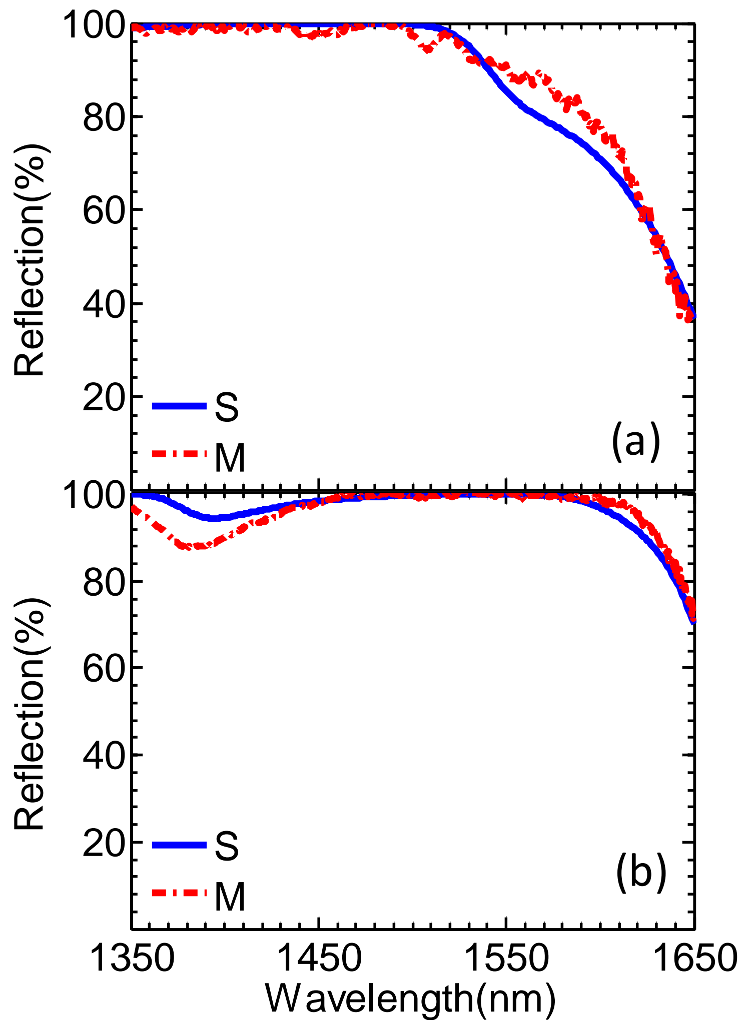

Figure 2.5 Controlled resonance of membrane reflector. Simulated (S) and measured (M) reflection spectra of surface normal 2D PCS with lattice constant=0.88 μm, radius of air hole=0.465 μm, and slab thickness=0.34 μm for (a) as fabricated on SOI substrate (b) after depositing SiO_2 with thickness of 400 nm on its top surface.

The 2D PCS with lattice constant equal to 0.88 μm, radius of air hole=0.465 μm, and slab thickness=0.34 μm is shown in Fig. 2.5(a) where blue curve shows the simulated result (S) and red curve exhibits the measured result (M). Both results are in close agreement with each other. The red-shift of 2D PCS with the same key parameters is shown in Fig. 2.4(b). The spectral peak shifts toward longer wavelengths by ~90 nm after the deposition of a thin oxide

layer with the thickness of 400 nm on top of 2D PCS surface as shown in Fig. 2.5(b). It is very obvious that after PECVD deposition on top surface of this sample compared to the previous one the spectral peak of current sample shifts longer than that of previous one. The main reason is that this sample is deposited thicker oxide during PECVD process and inside its air holes also filled more due to the relative larger radius of air holes compared to the previous one. The measured result (M) also agrees well with the simulated result (S). These results demonstrate practical post-process means for Fano resonance engineering broadband reflectors.

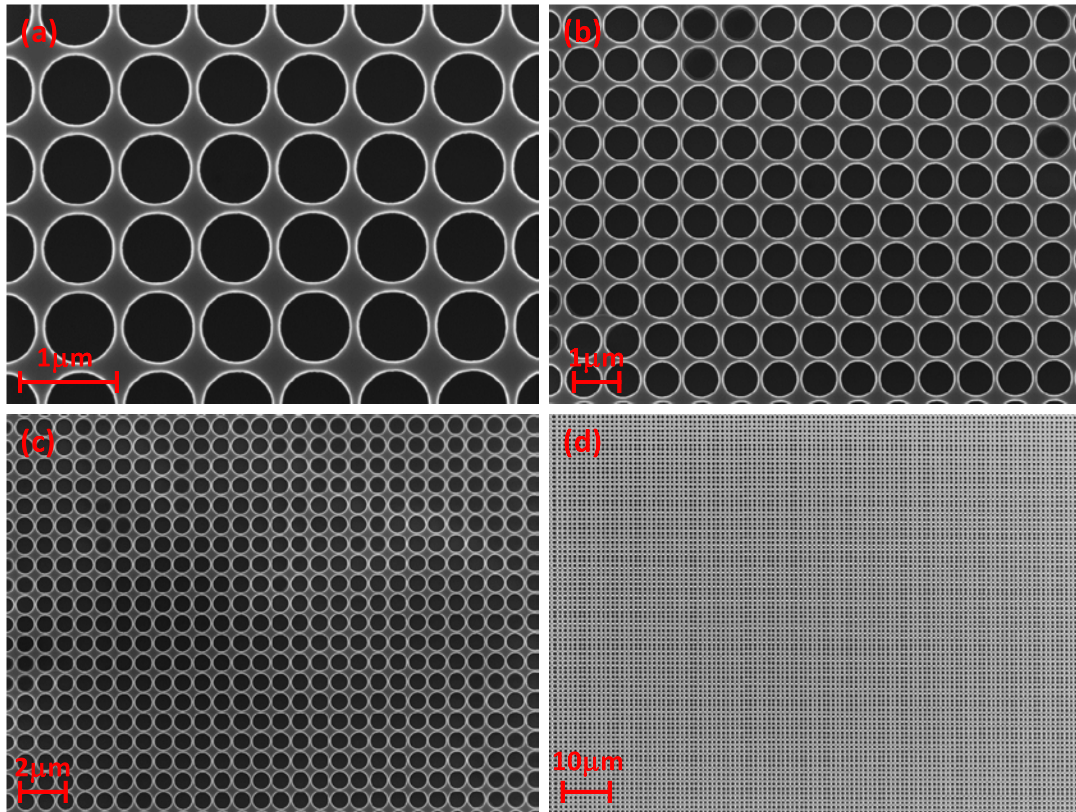

Figure 2.6 The scanning electron microscope images with different magnifications (a-d) of a fabricated nanomembrane reflector with square lattice of air holes in a single crystalline Si with lattice constant=0.86 μm, radius of air hole=0.404 μm, and slab thickness=0.34 μm

Fig 2.6 shows the SEM images of top view of SiNM fabricated on SOI substrate with the high quality patterning and etching which play an important role in achieving the very good reflection performance as we expected from the simulation. With these design parameters, the reflection bandwidth should be very broad covered wavelength of 1550 nm after PECVD has been done as shown in Fig 2.5(b).

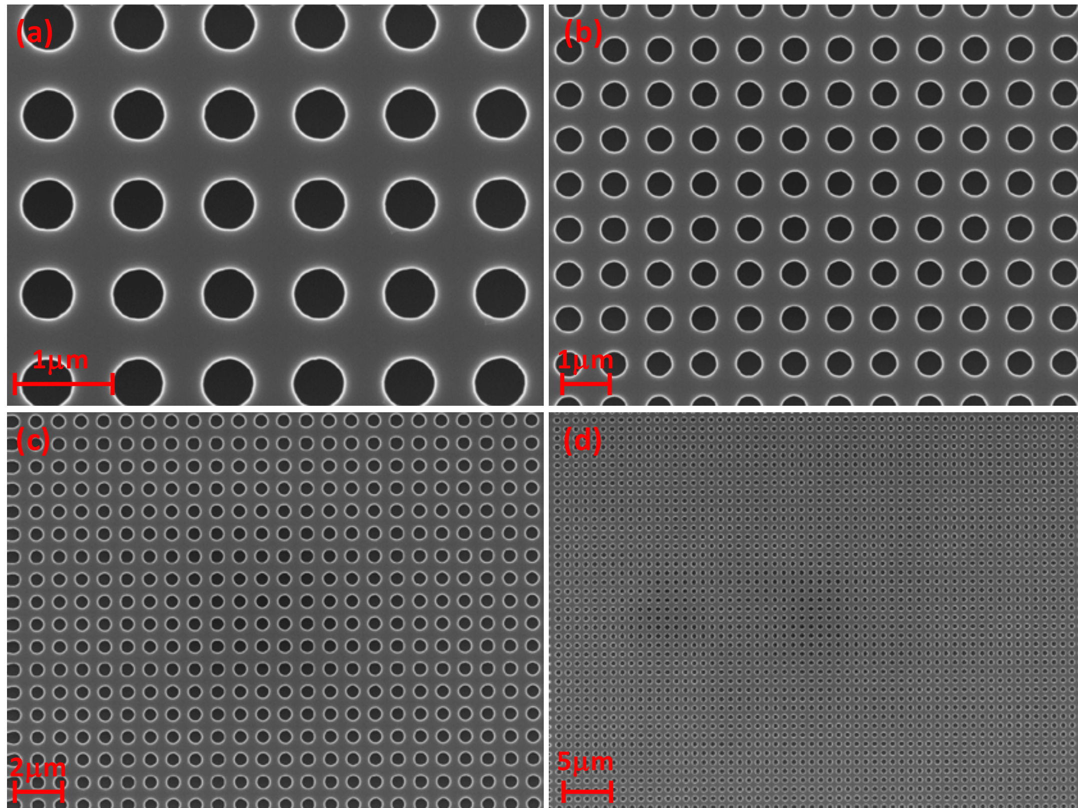

Figure 2.7 The scanning electron microscope images with different magnifications (a-d) of a fabricated nanomembrane reflector with square lattice of air holes in a single crystalline Si with lattice constant=0.98 μm, radius of air hole=0.265 μm, and slab thickness=0.34 μm

Fig 2.7 illustrates the SEM images of top view of SiNM fabricated on SOI substrate with square lattice of air holes in a single crystalline Si with lattice constant=0.98 μm, radius of air hole=0.265 μm, and slab thickness=0.34 μm. From the SEM images, the same high quality EBL patterning and highly anisotropic RIE etching through the slab is accomplished. After it was

characterized, the device exhibits very good reflection performance. The simulated and measured results match very well.

2.4 Characterization of Membrane Reflectors

Fig. 2.8 shows the schematic of reflection measurement setup where an unpolarized broadband tungsten halogen light sources was collimated and focused into a small spot size with an objective lens. By precisely controlling the sample holder, we can perform the reflection measurement. The reflected light was detected by optical spectrum analyzer (OSA) and processed by LABVIEW software.

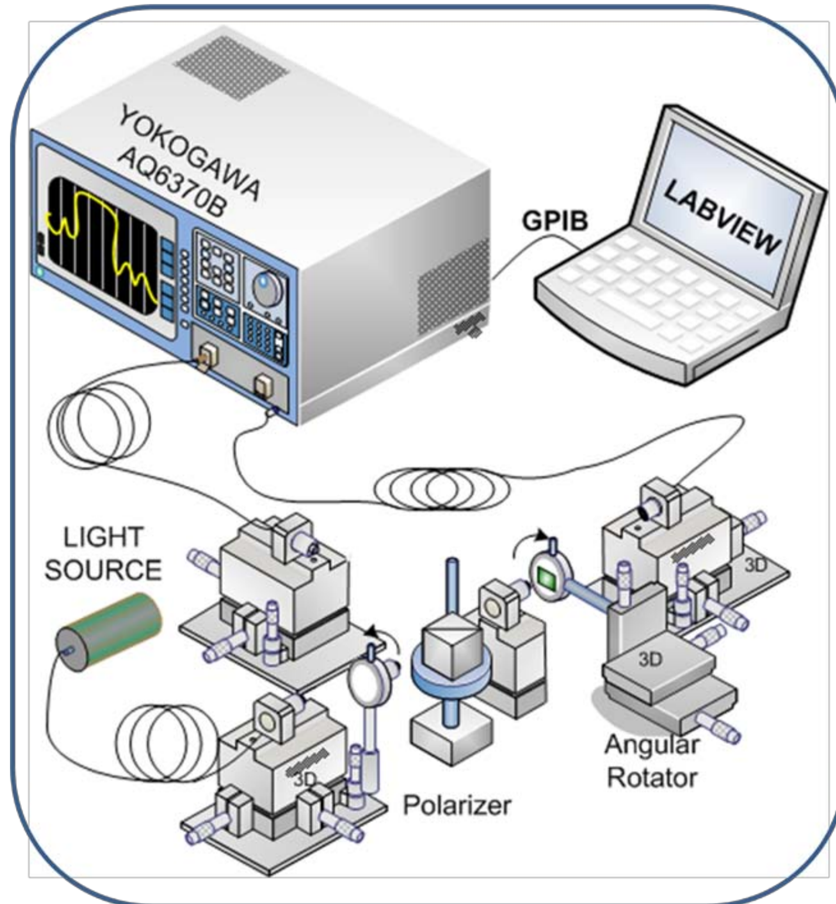

Figure 2.8 Reflection and transmission measurement setup for nanomembrane reflector characterizations. Broadband light source is employed as the incident light which is detected by optical spectrum analyzer controlling by labview computer.

The measured (denoted as “M” in Fig. 2.9) and simulated (“S”) reflection spectra are shown in Fig. 2.9, for reflectors before transfer (on SOI) and after transfer (on glass), respectively. The measured spectra agree well with the simulated results. Some degradation is evident in the measured reflection spectra at the shorter wavelengths band, mostly due to certain fabrication non-uniformity associated with the large area photonic crystal structure on SOI substrate. Spectral blue-shift is also observed after the membrane reflector is transferred from the original SOI substrate to the glass substrate, mostly due to the relatively lower refractive index of glass substrate and slightly larger air hole radius due to BHF undercut etching in SiNM transfer process. More importantly, the reflector peak reflection and the reflection band do not degrade after being transferred onto glass substrates. This indicates the uniform, high quality large area patterned transferred NMs, owing to the excellent PDMS transfer process.

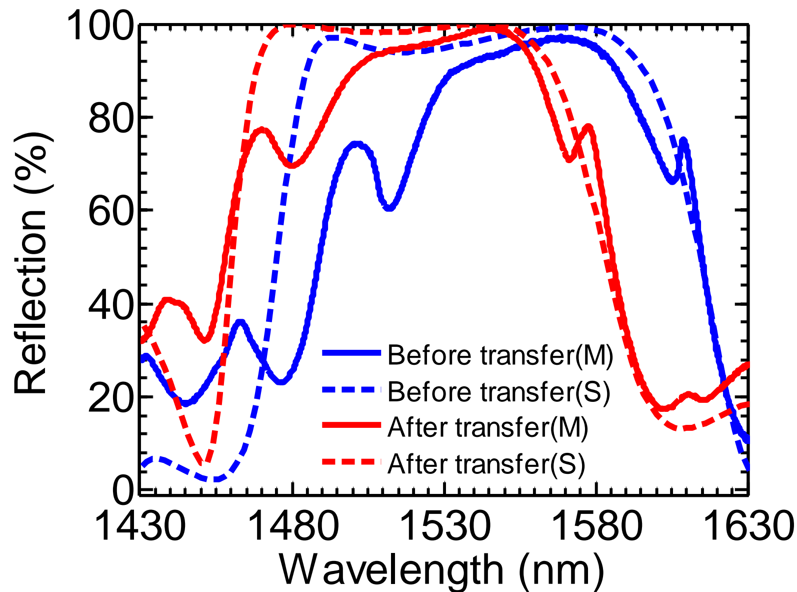

Figure 2.9 Measured (M) and simulated (S) reflection spectra of Si membrane reflector on SOI (before transfer) and on glass substrate (after transfer).

Shown in Fig. 2.10(a, b) are optical microscope images of a 2mm × 2mm sized membrane reflector, transferred to a glass substrate. With optimized elastomeric PDMS stamp printing transfer process, high quality NMs have been successfully transferred without any visible defects. Also shown in Fig. 2.10(c-d) are scanning electron microscope (SEM) images of the transferred membrane reflector on glass substrate, with different zoom levels. It is also worth noting that such high quality transfer of large area crystalline semiconductor nanomembranes is essential in maintaining high reflectivity performance for the transferred reflectors on glass substrates.

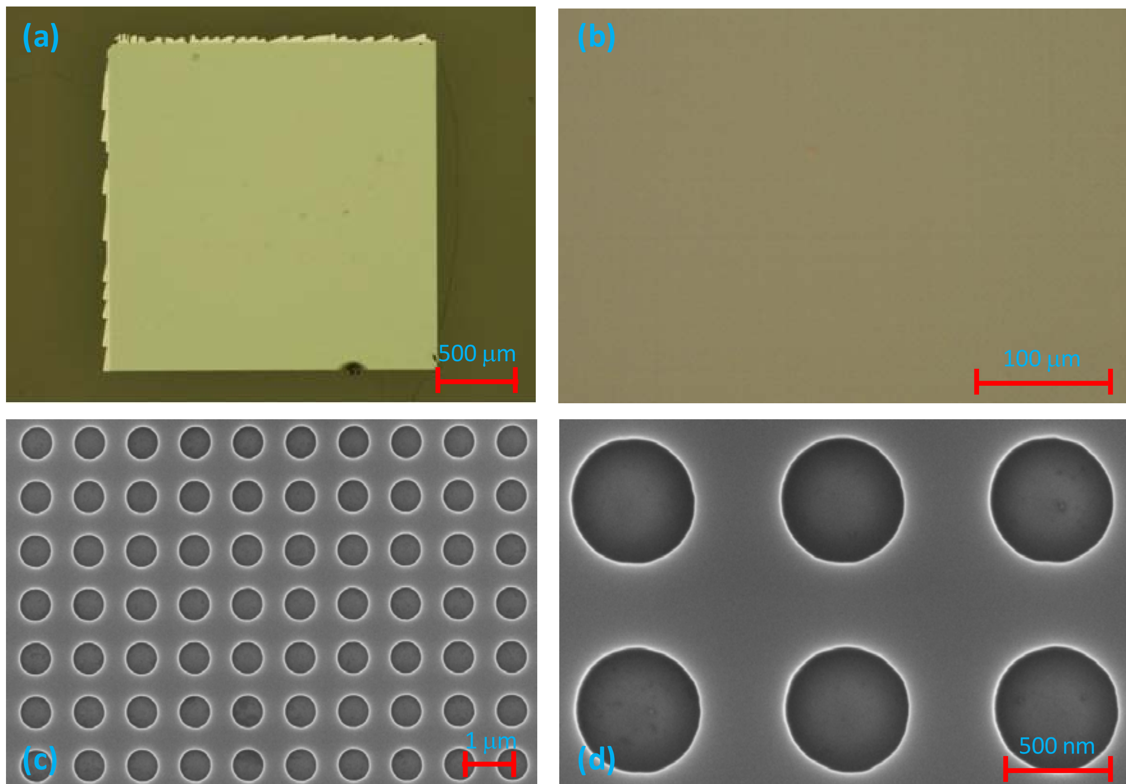

Figure 2.10 (a) and (b) are microscope images. (c) and (d) are scanning electron microscope images of a membrane reflector that was transferred onto glass substrate using transfer printing process.

To further investigate the polarization property, we utilize a Newport precision linear polarizer in our test setup to control the incident beam polarization angle. By controlling the

polarization angle, the measured, along with the simulated, reflection spectra are shown in Fig. 2.11. The incident beam polarization was swept from ϕ = 0° (as defined in Fig. 2.11(a)), for TM polarized beam, which has electric field parallel to ΓX direction of PC pattern, to ϕ = 90° for TE polarized beam, which has a perpendicular electric field to ΓX direction. The measured reflection spectra overlap with each other under normal incident condition. The simulated polarization dependent reflection spectra are shown in Fig. 2.11(b). The polarization independent feature is also expected for such square lattice photonic crystal membrane reflectors, owing to the high symmetric properties of the square lattice structure. It is also worth mentioning that polarization dependent reflectors can also be engineered, by the control of the lattice structure (e.g., rectangular lattice, hexagonal lattice, etc.), and the change of air hole shape (e.g. elliptical or rectangular shapes, etc.).

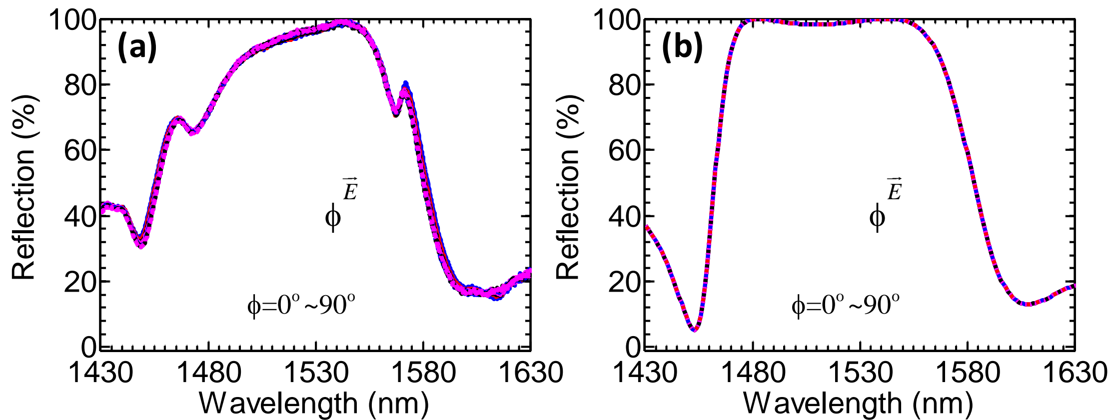

Figure 2.11 (a) Measured and (b) simulated polarization-dependent reflection spectra for the fabricated membrane reflector on glass substrate. Notice the spectra overlaps with each other for different polarization angles.

The reflection spectral of a membrane reflector for surface normal measurement were also investigated to observe the dip location at wavelength of 1510 nm because the simulation does not show the reflection obviously dropped at this location. After fining adjustment the incident beam, we found that the dip came from the effects of small angle of incident light impinging onto the sample. To minimize the angle of incidence, the sample was moved far

away from focusing position by precisely controlled sample holder and at that position the accurate reflection can be obtained. Fig 2.12 shows the simulated and measured reflection results of the membrane reflector. The measured results can be obtained by two approaches and both results are very similar, however one is without dip after adjust incident angle similar to the simulation result and another one with very profound dip at wavelength of 1510 nm measured without adjusting incident beam.

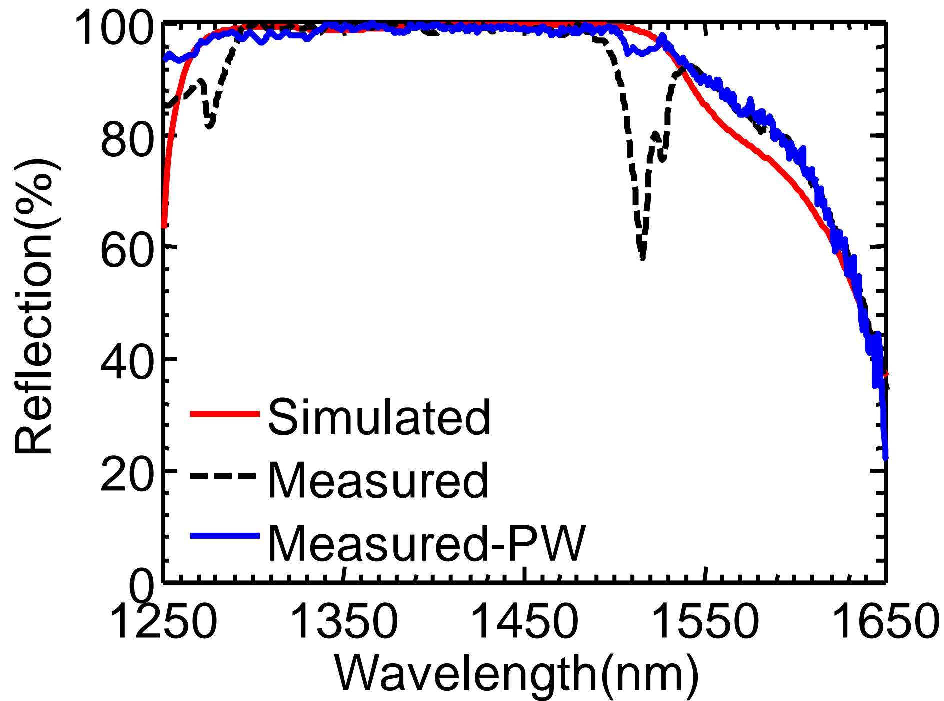

Figure 2.12 Investigation of simulated and measured reflection spectra of surface normal 2D PCS with lattice constant=0.88 μm, radius of air hole=0.465 μm, and slab thickness=0.34 μm to achieve the exact measured result match with simulated result.

2.5 Summary

Nanomembrane reflectors were fabricated on SOI substrate with different key design parameters, transferred onto glass substrate, and characterized before and after transferred. With the high resolution of EBL patterning and highly anisotropic RIE etching, the reflections of both simulation and experiment close agree with each other. The fabricated membrane

reflectors can be selectively controlled center of reflection spectral band to the target wavelength. Devices were transferred based on PDMS transfer process still give very high reflection. The measured and simulated results of devices fabricated on an SOI substrate are in very good agreement ,and the measured reflections of devices are very closed to 100% over 100~220 nm in the desired infrared wavelengths

CHAPTER 3

FLEXIBLE CRYSTALLINE INP NANOMEMBRANE LED ARRAYS

3.1 Introduction

A rigid material becomes bendable and flexible if we make it thin to make it flexible. It could be very useful for many applications that would be impossible if an electronic device was fabricated on a brittle and rigid substrate, for example, sensors, light emitting diodes (LEDs), and solar cells [55-57]. From thick rigid substrate to thin flexible substrate, we report here flexible LEDs arrays based on transferred inorganic crystalline InP nanomembranes. Flexible electronics and optoelectronics structures which can be stretched, folded, and manipulated electronic and photonic devices are of great scientific and engineering importance. Such devices have their applications ranging from flexible imaging/displays, sensors, solar cells and conformal electronic/photonic integrated systems to potential integration into artificial muscles or biological sensors. Most flexible electronics research so far is based on organic, polymer, and/or amorphous semiconductor material systems. Crystalline semiconductor nanomembranes (NMs), which are conformable, patternable, transferable, stackable, and manufacturable, offer unprecedented opportunities for unique electronic and photonic devices for vertically stacked high density photonic/electronic integration, high performance flexible electronics, and flexible photonics. High quality single-layer silicon NMs (SiNM) have been transferred onto various foreign substrates, such as glass, flexible PET (polyethyleneterephthalate) plastics, etc., based on low temperature transfer and stacking processes [3, 4, 6, 58, 59]. Very high performance electronics based on transferable Si/SiGe NMs and flexible Ge photodetectors were already reported [3, 4, 6, 60]. We have also reported various photonic devices based on Fano resonances on Si, glass and flexible PET substrates [39, 40, 61]. In addition to Group IV materials (Si, Ge, etc), nanomembranes based on III-V

(GaAs, InP, etc.) and other material systems are also being developed for heterogeneous integration (membrane stacking) on Si and other foreign substrates, with high potential electronic and photonic for a wide range of applications.

3.2 Device Fabrication

The starting wafer is InGaAsP QW Cavity wafer comprising of the device layers (top and bottom contact layers, cladding and spacer layers on top and bottom, and quantum well (QW) structures in the middle) grown on top of the sacrificial layers (e.g., InP and InGaAs for the InP material system). The top rings are first patterned into various diameter sizes of mesas with 5 μm-wide, using optical lithography. The top ring metal contacts are defined by electron-beam evaporation (Pd/Zn/Pd/Au: 10/10/20/200 nm) on top surface of source wafer and then liftoff. Next, an alignment pattern to protect metal contacts is patterned before the regions between the metal contacts of active layer are selectively etched down to the bottom contact layer with wet chemical etching. In our case, the InGaAs and InGaAsP QW layers are selectively etched away by the chemical mix of $HF/H_2O_2/H_2O$ (1:1:10) solution and The InP layer is selectively etched away by the chemical mix of HCl/H_3PO_4 (1:4). The bottom contact patterns are formed into stripes by photolithography and subsequent evaporation of metals (Ni/Ge/Au/Ti/Au: 15/20/30/10/100 nm) at the bottom of the etched regions and then liftoff. The thin PECVD SiO_2 layer with total thickness of 600 nm was universally deposited to passivate all devices. The devices are patterned and access holes of both top and bottom contacts are formed by photolithography and passivated layer is etched by using the RIE-etching. Finally, the interconnect layer was patterned to connect all of the devices together forming the device arrays. A completed flexible InP LED arrays were formed, with top and bottom contacts (Fig. 3.1(a) (b)). The SEM image of top ring contact and interconnect line connecting to the stripe to form the arrays and laying on the SiO_2 passivation layer is shown in Fig. 3.1(c). The InP LED was transferred onto flexible PET substrate as shown in Fig. 3.1(d). In Fig. 3.1(e) shows the

device was under probing test and Fig. 3.2(f) illustrates the device was transferred onto gold coated PET substrate.

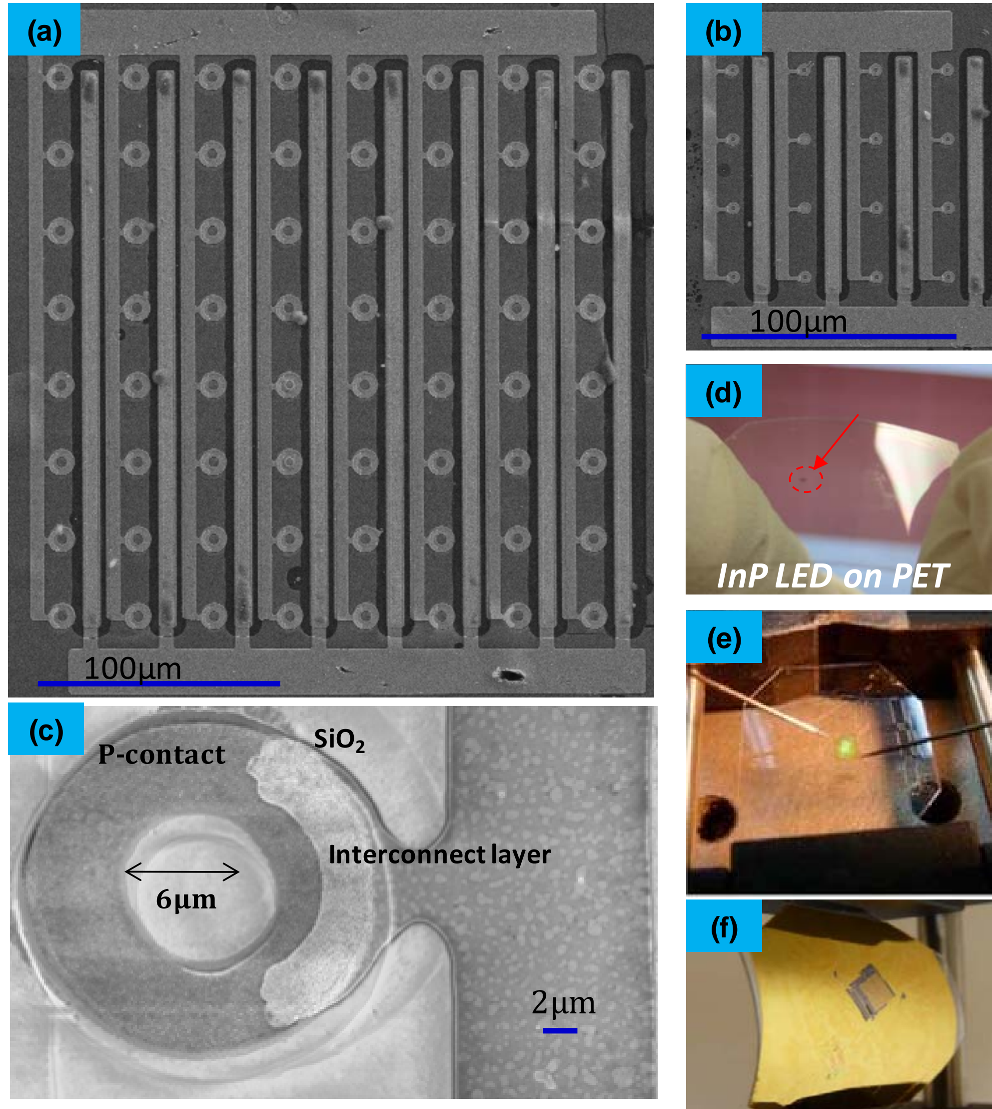

Figure 3.1 Demonstration of flexible LEDs based on InGaAsP QW NM transferred onto PET substrates. (a) (b) SEM images of 8 by 8 and 4 by 4 devices on PET substrate after testing. (c) SEM image of top ring contact linked by interconnect layer and passivated by thin layer of SiO_2. (d) Image of devices transferred onto PET substrate. (e) Image of devices under probing test. (f) Image of fabricated devices on Au coated PET substrate.

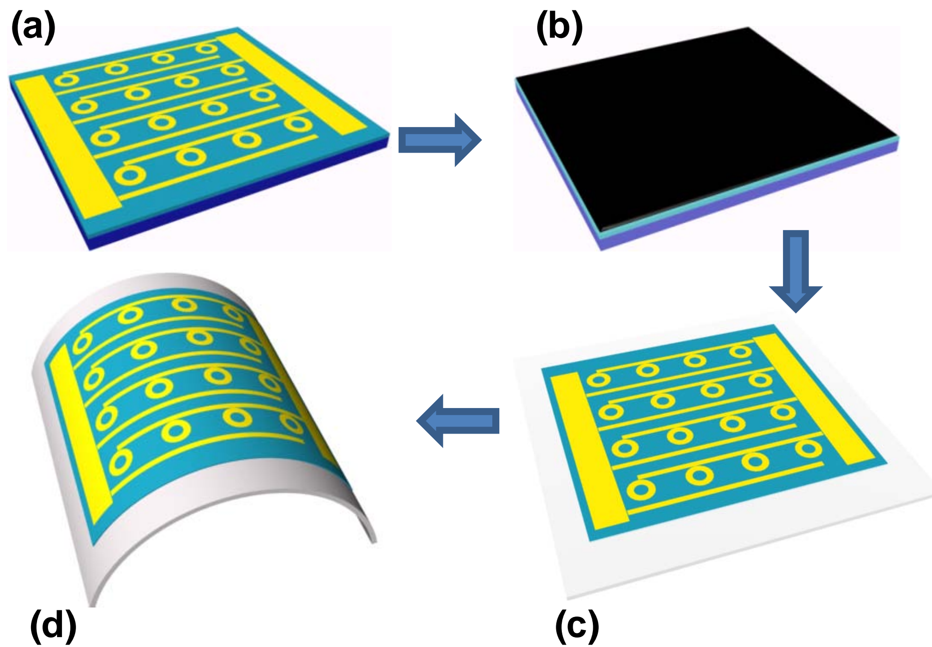

Figure 3.2 The crystalline InP LED arrays are fabricated on InP substrate as depicted in (a). (b) The top surface of the devices is protected by Apiezone wax before putting it into chemical wet selective etching to release devices from handling substrate. (c) The devices are transferred onto a new PET substrate after Apiezone wax was cleaned with Trichloroethylene (TCE). (d) The flexible crystalline InP LED arrays on PET substrate.

Fig. 3.2 shows schematically illustrates the key processing steps for fabricating the device. The device was fabricated on InP handling substrate and all P contacts were connected together to form an array at one side whereas all N contacts were connected to another side as shown in Fig. 3.2(a). The top surface of the device was coated with a thin layer of Apiezone wax mixing with TCE as shown in Fig. 3.2(b) and it was baked at 120 °C for 10 minutes to consolidate the wax. The device with coated wax was immerged into the chemical wet selective etching to release the device from the sacrificial layers and handling InP substrate as mentioned earlier before placing it onto new host substrate and keeping it under pressure for 24 hours. Either InGaAs or InP etch stop/sacrificial layers were used for the release of top InGaAsP QW active region. After completely etching the substrate, gently removing wax with

TCE as shown in Fig. 3.2(c), then the device will be successfully transferred onto new flexible substrate shown in Fig. 3.2(d).

3.3 Device Characterization

Different mesa sizes of device arrays were formed based on InGaAsP QW NM transfer process. Notice here both top and bottom contacts were formed before transferring and placed on one side of the NM. The flexible InP LED array devices show excellent electrical and optical performance with low turn-on voltage, low series resistance, and the spherical optical beam profile.

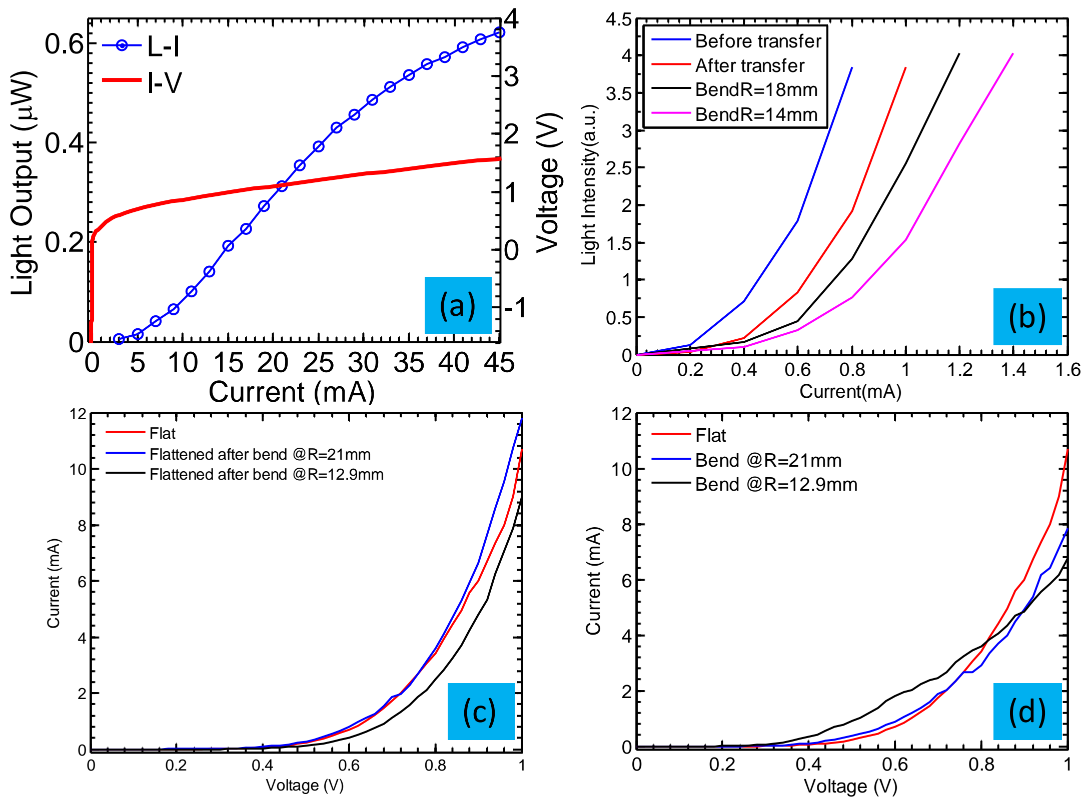

Figure 3.3 Optical and electrical characteristics of flexible crystalline InP LED arrays are measured. (a) L-I-V curves of the devices. (b) L-I curves of the devices before and after transferred with different bending radii. (c) I-V characteristics of the devices that have been backed to the flat state after different bending radii. (d) I-V characteristics of the devices during different bending radii.

Fig. 3.3(a) shows the typical voltage versus current (VI) and the optical output powers as a function of input currents (LI) characteristics for a crystalline InP LED array. The device has an output power of >0.6 μW and operation voltage is still below 1.6 V. The VI curves are shown in Fig. 3.3(b) for before and after transferring device onto flexible substrate also at different bending radii. The currents are slightly reduced after bending from the bending radius of 21 mm down to 12.9 mm possibly caused by the strain-induced in the metal–InGaAs contacts. However, the VI curves of the device obtained when the PET substrate was returned to its unbent condition after different bending radii of 18.0 mm and 14.0 mm, showing the contacts can be back to the stable condition as shown in Fig 3.3(c) (d). When devices were bended at a smaller radius, peak intensities also reduce possibly came from some devices out of focusing because of substrate bending. These results indicate that the flexible InP LED array will work even the bending radius is at about 12.9 mm.

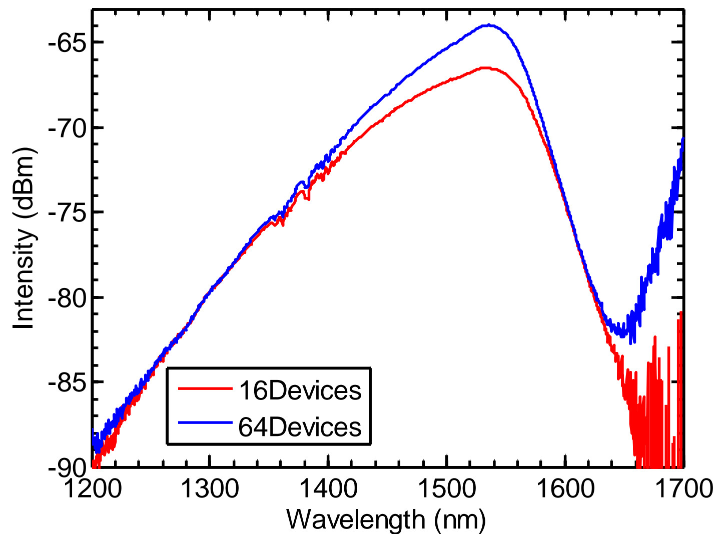

Figure 3.4 The emission spectra of flexible crystalline InP LED arrays for both 4x4 and 8x8 devices are characterized by coupled light to the fiber and monitored by optical spectrum analyzer.

Fig. 3.4 shows the output emission spectra of both large (64 devices) and small (16 devices) arrays of InP LEDs as a function of wavelengths with emission peak at 1540 nm at the

input current of 60 mA. Fig. 3.5 shows the far- field images of large and small flexible devices using beam profiler. Both sizes of flexible devices exhibits the uniform emission spectra where the large array was forward biased at 0.5 mA and the small array was forward biased at 0.7 mA. We also analyzed the InP LED light beam by using beam profilers during the bending substrate testing. Typical far-field intensity distribution of flexible crystalline InP LED arrays was experimentally investigated at room temperature with different focusing points shown in Fig 3.6. Fig 3.6(a)-(d) shows the beam profiler focused with objective lens during the bending of radius 12.9 mm at point a, b, c, and d, respectively.

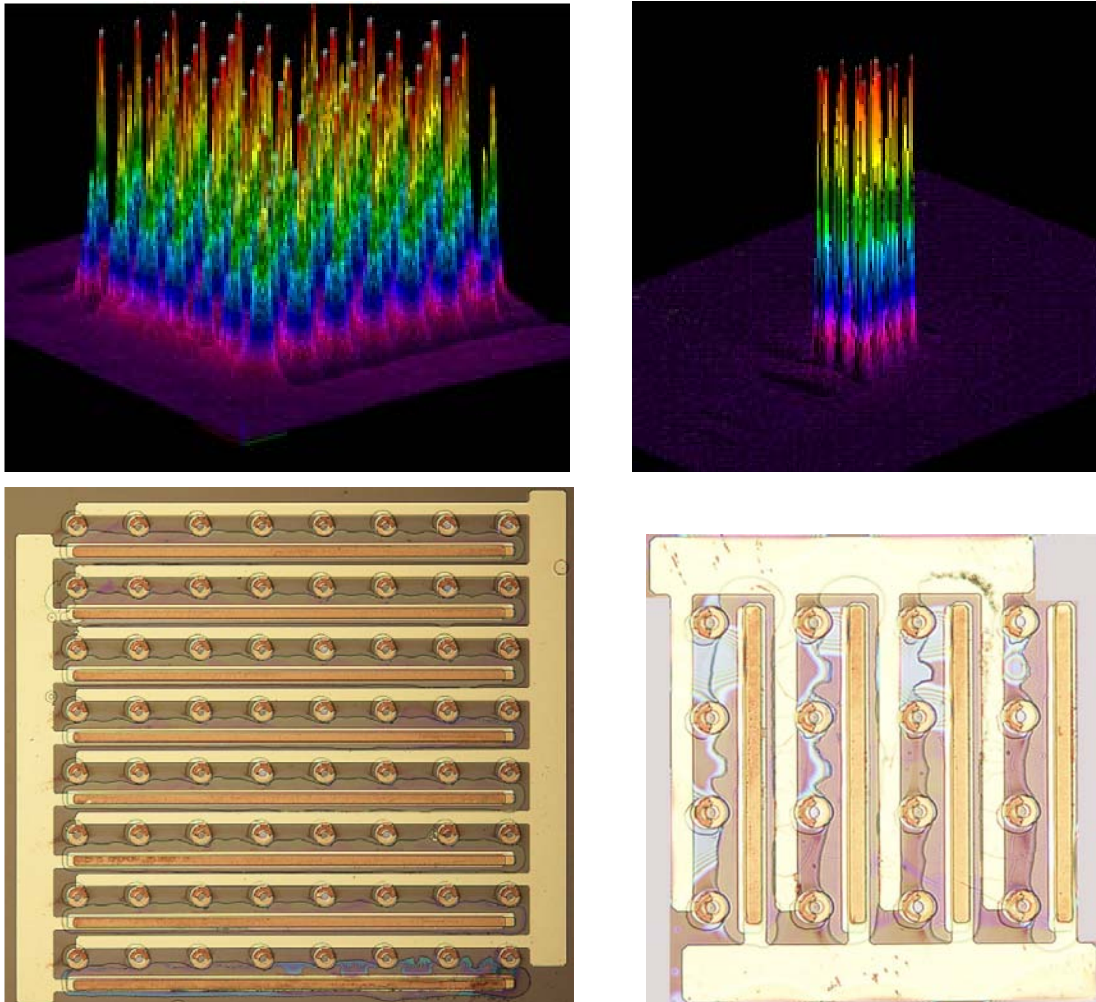

Figure 3.5 The far-field images and optical microscope images of flexible crystalline InP LED arrays for both 4x4 and 8x8 devices are shown.

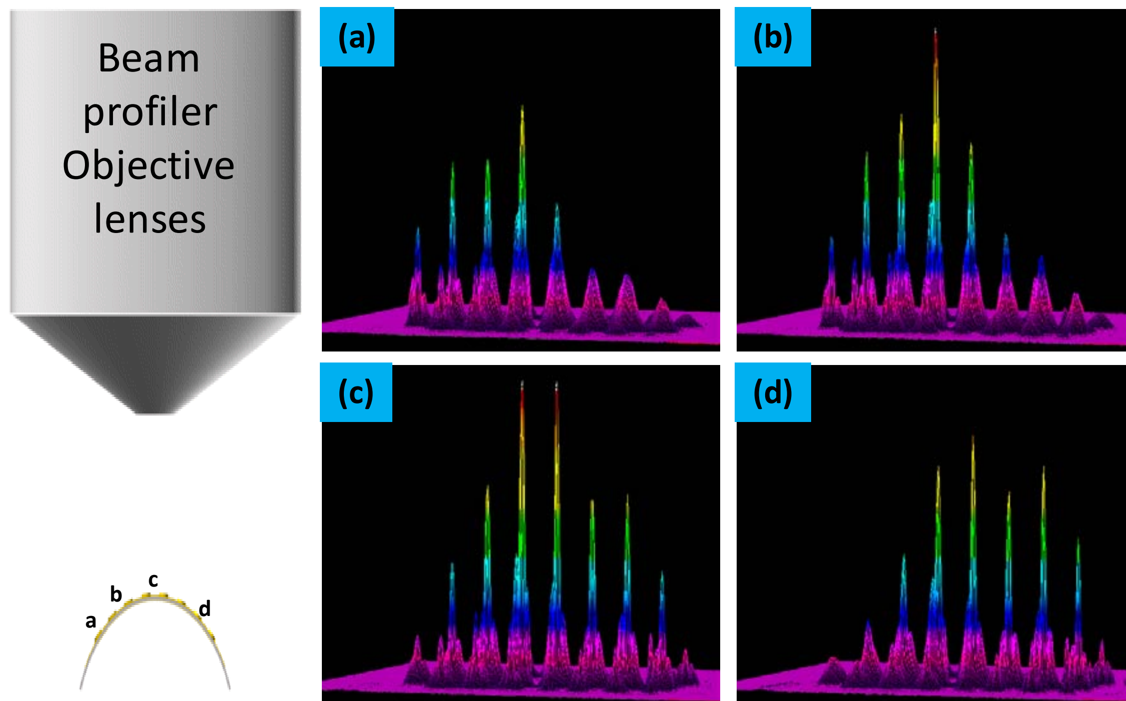

Figure 3.6 The far-field images of flexible crystalline InP nanomembrane LED arrays characterized with beam profiler at different focusing locations of the devices to demonstrate that the substrate was bended during testing as shown in (a) to (d).

3.4 Summary

Flexible crystalline InP nanomembrane LED array have been experimentally demonstrated. The devices were fabricated and characterized before and after transferring onto PET substrate based on low temperature transfer and stacking processes. High performance flexible InP LED arrays were optically and electrically characterized, and investigated typical far-field intensity distributions by beam profiler. To enhance the mechanical strength of crystalline InP nanomembrane during transferring, we also employed the FAMT process and it drastically improved transferring quality of fragile III-V materials not only a small piece of InP but also a very large piece of flexible InP can be successfully transferred. Finally, the transferred devices were optically and electrically characterized to compare the performance during

substrate has been bended and flat and it shown that the high performance devices worked very well even though they were bended at a very small radius. The flexible InP LED arrays perform well although the bending radius is smaller than 13.0 mm.

CHAPTER 4

MEMBRANE REFLECTOR VERTICAL CAVITY SURFACE EMITTING LASERS

4.1 Introduction

The creation of silicon based light sources has been a major research and development effort world-wide. The availability of a practical on-silicon lasers will enable a new generation integrated photonic and electronic components and systems, which will be more cost-effective, of higher performance and more energy efficient [62, 63]. Among various approaches to Si-based light sources reported thus far, the hybrid gain-medium approach (especially integrated with group III-V materials) [64]. seems to be the most promising one (toward practical use) due to its higher efficiencies than any others. Lasers on Si, mostly edge emitting lasers, with good performances have been reported, via heterogeneous integration of III-V and Si, based on direct growth on Si [65-67] or direct wafer bonding to silicon [64-68]. We report here a membrane reflector surface-emitting laser on Si, based on multi-layer semiconductor nanomembrane stacking via a stamp-assisted transfer printing process [5, 9]. This type of near-infrared ultra-compact lasers on silicon consists of a transferred III-V InGaAsP quantum well heterostructure that is sandwiched in between two thin single-layer silicon photonic crystal Fano resonance membrane reflectors [69-71]. High finesse single or multi-wavelength vertical lasing cavities can be formed with two Si membrane reflectors, either on a Si substrate or print-transferred to a glass or a flexible host. Unlocking the constraints of material incompatibility, including both lattice mismatch and thermal mismatch that are typically encountered in the current heterogeneous approach, the multi-layer integrated laser structure via transfer printing offers a viable approach to heterogeneously integrated lasers and other photonic and electronic devices at any wavelengths on any types of substrates. Since its invention 50 years ago, semiconductor lasers [72] mostly based on compound semiconductor heterostructures, have

made a tremendous impact on modern science and technology, with widespread applications in the areas of communications, imaging, displays, medicine and optical physics, etc. However, the creation of practical light sources on elementary silicon substrates, the so-called "bread-and-butter" material of the electronic industry, has proven to be a major roadblock toward large volume, low cost integrated photonics and electronics on Si substrates [73]. Various approaches have been taken to make light sources based on light emission from Si material itself, including engineered Si or Ge structures, [73, 74] and stimulated Raman scattering in Si ,etc [75, 76]. However, these lasers have extremely low efficiencies, owning to the inefficient light emission from Si, an indirect band gap semiconductor material. Lasing on Si has also been pursued based on heterogeneous integration of Si with compound semiconductor materials, where emission comes from efficient direct band gap (e.g. group III-V) materials. These Si based lasers have been reported with promising performances, either based on direct growth of III-V materials on Si [66, 67] or direct wafer bonding to Si [64, 77, 78]. However, challenges remain for these hybrid approaches as well [79]. Direct (molecular) wafer bonding or wafer fusion has stringent bonding interface requirements [64, 80]though such requirement can be relaxed with adhesive-assisted wafer bonding technique [81]. Direct growth of III-V on Si is, on the other hand, limited by the lattice mismatches between different material systems, as well as the incompatibility of different material growth conditions. Additionally, most on-Si lasers reported thus far are edge-emitting lasers. For these edge-emitting lasers, inherent challenges exist in forming cleaved mirror facets, in CMOS compatible on-chip testing, and in forming large and dense laser arrays. We report here an optically pumped ultra-compact Si membrane reflector vertical-cavity surface-emitting laser (MR-VCSEL), which can be easily built with low temperature processes on CMOS compatible Si substrates and on any other low cost substrates. The lasing cavity consists of a transferred III-V InGaAsP quantum well (QW) heterostructure active region, sandwiched in between two single-layer Si photonic crystal (PC) Fano resonance membrane reflectors (MRs). These two MRs essentially replace the two multi-

layer quarter wavelength DBR (distributed Bragg reflector) mirrors that are commonly used in conventional VCSELs.

4.2 MR-VCSEL Cavity Design

To achieve lasing with a low threshold current, it is highly desirable to design MR-VCSEL cavities with the following characteristics: (1) The cavity mode should spectrally match well with that of the QW peak; (2) The cavity mode should have an optimal field distribution for spatial matching with the QW active region; (3) The cavity mode optical confinement factor should be maximized to enable low gain threshold requirements; and (4) The cavity should be designed such that the waveguide mode should be spectrally separated from the cavity mode. Fig. 4.1(a) shows the schematic of MR-VCSEL cavity under investigation. The cavity consists of six different layers (t_1 to t_6), sitting on top of the SOI substrate with SiO_2 BOX layer thickness of t_0. Using the InGaAsP QW cavity and the top and the bottom MRs fabricated from the Soitec SOI structure, the following parameters are fixed in our design: t_0 = 2 μm with an index of refraction of 1.48, $t_1 = t_5$ = 340 nm with refractive index of 3.48, and t_3 =465 nm with detail shown in table 4.1. The photonic crystal (PC) square lattice parameters of the top and the bottom MRs are optimized during the MR design. For the cavity case shown in Fig. 4.1, the square lattice PC structures have a lattice constant a = 0.86 μm for both the top and the bottom MRs. However, different air hole radii are used, with r/a = 0.46 and r/a = 0.45, for the top and the bottom MR, respectively. Considering the partial filling of oxide inside the air holes using a PECVD SiO_2 deposition process, an effective index of n_f is taken to be 1.2, which offers the best matching between the measured and simulated reflection spectra [52, 69]. The low refractive index oxide buried layer thicknesses t_2 and t_4 were optimized through our design. Glass substrate was also incorporated in the design (layer t_6). Both infinite (in-plane) and finite (vertical) structures were numerically calculated using Finite Difference Time Domain (FDTD) method [47, 49] and we imposed periodic boundary condition (PBC) and Perfect Matched Layer (PML) absorbing boundary conditions [48]. Shown in Fig. 4.1(b) are the demonstrations of the

reflection characteristics of the top and bottom MRs, where high reflection (>98%) covers a wavelength range from 1420 to 1530 nm. Two different techniques were employed here to identify the cavity mode. The first one is the calculation of the reflection of the whole cavity structure. From the reflection dip located at the high reflection band range, we can find the cavity mode according to its resonant transmission property. The reflection of MR-VCSEL structure with t_2 = t_4= 400 nm is plotted in Fig. 4.1(c) (the blue line), which is computed using Rigorous Coupled-Wave Analysis (RCWA) technique [45]. The reflection dip is located at 1478 nm. To confirm this cavity mode, the other method was employed based on the phase resonant condition (total phase change of one round-trip in cavity is equal to integer times of 2π). The phase calculation details can be found in [82, 83]. After obtaining the reflection phase change (ϕ) of the top and bottom MR, the resonant cavity mode can be decided. The phase of the mode in the cavity is shown in Fig. 4.1(c), plotted in red dash dotted line. One can find that the mode located at 1478 nm has a 2π phase change.

Table 4.1 Key Design Parameters of InGaAsP QW Cavity on InP Substrate.

Layer	Description	Material	Thickness (nm)	Dopant	Doping (cm^{-3})	Optical index	Optical thickness
23	Contact layer	InGaAs	40	Zn	1e19	3.444	0.0889
22	Cladding layer	InP	50	Zn	2e18	3.172	0.1023
21	Spacer layer	InP	81.5	Undoped (UID)		3.172	0.16679
20	Barrier (0.9% ts)	$Ga_{0.515}In_{0.485}As_{0.83}P_{0.17}$	7.5	Undoped (UID)		3.4	0.0165
5…19	QWs (1% cs)(x8)	$Ga_{0.24}In_{0.76}As_{0.83}P_{0.17}$	7.5	Undoped (UID)		3.5	0.1355
4…18	Barrier (0.9% ts)(x8)	$Ga_{0.515}In_{0.485}As_{0.83}P_{0.17}$	7.5	Undoped (UID)		3.4	0.1316
3	Spacer layer	InP	81.5	Undoped (UID)		3.172	0.16679
2	Cladding layer	InP	50	Si	2e18	3.172	0.1023
1	Contact layer	InGaAs	40	Si	1e19	3.444	0.0889
	Sacrificial layer	InP	100	Si	5e18		
	Sacrificial layer	InGaAs	500	Si	5e18		
InP Substrate (n+)							

Finally, we investigated the properties of quality factor and field distribution of this cavity mode. By employing FDTD technique [47, 49], a short temporal Gaussian pulse is used to excite the cavity mode. The quality factor (Q) of the cavity mode at 1478 nm is calculated to be 4,300 defined by $Q=\mathrm{Re}(\omega)/-2\mathrm{Im}(\omega)$. Then a longer temporal Gaussian pulse is used to excite only this cavity mode and the stable field is recorded after the source is turned off for a long time. The electric field of the standing wave distribution is demonstrated in Fig. 4.1(d), where the cavity index profile is also plotted. The confinement factor is calculated to be Γ = 5.6%. This value is comparable to the confinement factor of conventional DBR-based VCSEL structures.

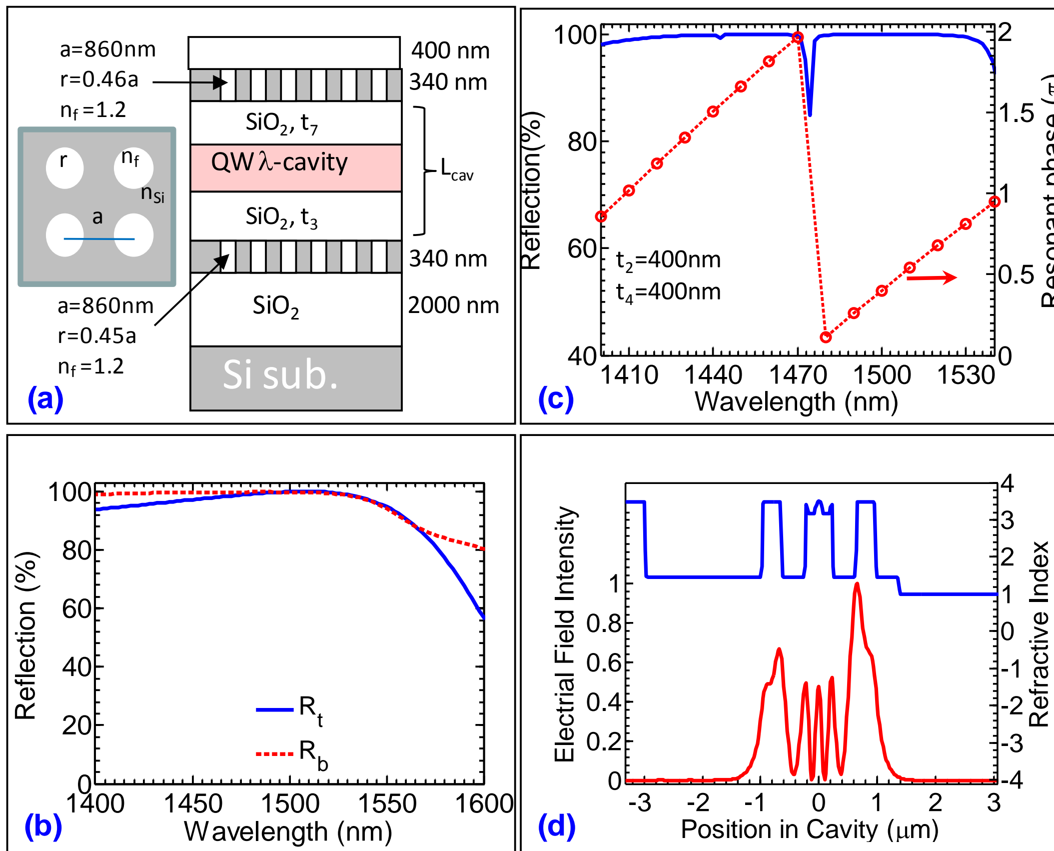

Figure 4.1 Characteristics of the designed MR-VCSEL cavity. (a) MR-VCSEL cavity structure configuration, where t_0 = 2μm, t_1 = t_5 = 340 nm, t_3 = 465 nm, t_2 = t_4 = 400 nm, and glass substrate t_6. (b) Simulated reflection spectra for top (R_t) and bottom (R_b) MRs. (c) Calculated cavity resonance mode based on cavity reflection (solid blue line) and phase resonant conditions (dashed red line). (d) Field distribution of cavity mode (red), along with index profile in the cavity (blue).

4.3 Fabrication of MR-VCSEL Devices

The MR-VCSEL devices were constructed on Si substrates with transfer-printing stacked multiple layers by sandwiching an InGaAsP QW active layer in between two single layer Si membrane reflectors (top and bottom MRs). The fabrication process of MR-VCSEL is illustrated in Fig. 4.2 schematically. High quality patterned photonic crystal Si reflectors were fabricated via e-beam lithography and reactive ion etching (RIE) process on SOI substrates purchased from Soitec®, with 340 nm Si template layer and 2 μm buried oxide (BOX) SiO_2 layer. A low-index PECVD SiO_2 layer was then deposited on the top of the patterned Si to form the bottom MR. The PDMS stamp based transfer printing process is used and optimized for inking and printing patterned photonic crystal Si NMs with high hole-to-neck ratios. The PDMS stamp is made of SYLGARD® 184 silicone elastomer with an optimized mixing ratio between base and curing agents. The agents are supplied in two parts: lot-matched base and curing agents. After thoroughly mixing the base and the curing agents, the air introduced during the mixing step is reduced by gentle agitation. After pouring the mixture into a pre-cleaned mold container, a vacuum de-airing process is applied. A final PDMS stamp is then formed after a two-hour curing step in an oven at about 70 °C. Previous studies have been carried out in detail to understand the kinetics of peeling an elastomer layer (PDMS stamp) off a rigid substrate (NMs) [5, 84]. Employing the PDMS stamp based transfer printing process, various types of crystalline semiconductor materials have been successfully transferred onto foreign substrates [4, 9, 44, 85]. Here we used our PDMS stamps to transfer InGaAsP QW active layer and disks to the SiO_2 layer on top of the bottom Si MR. Notice that a relatively low temperature (~1100C for 30 min) bonding process may improve the as-stacked bonding interface between InGaAsP QW active layer and low index SiO_2 layer, devices reported here did not apply this low temperature bonding process.

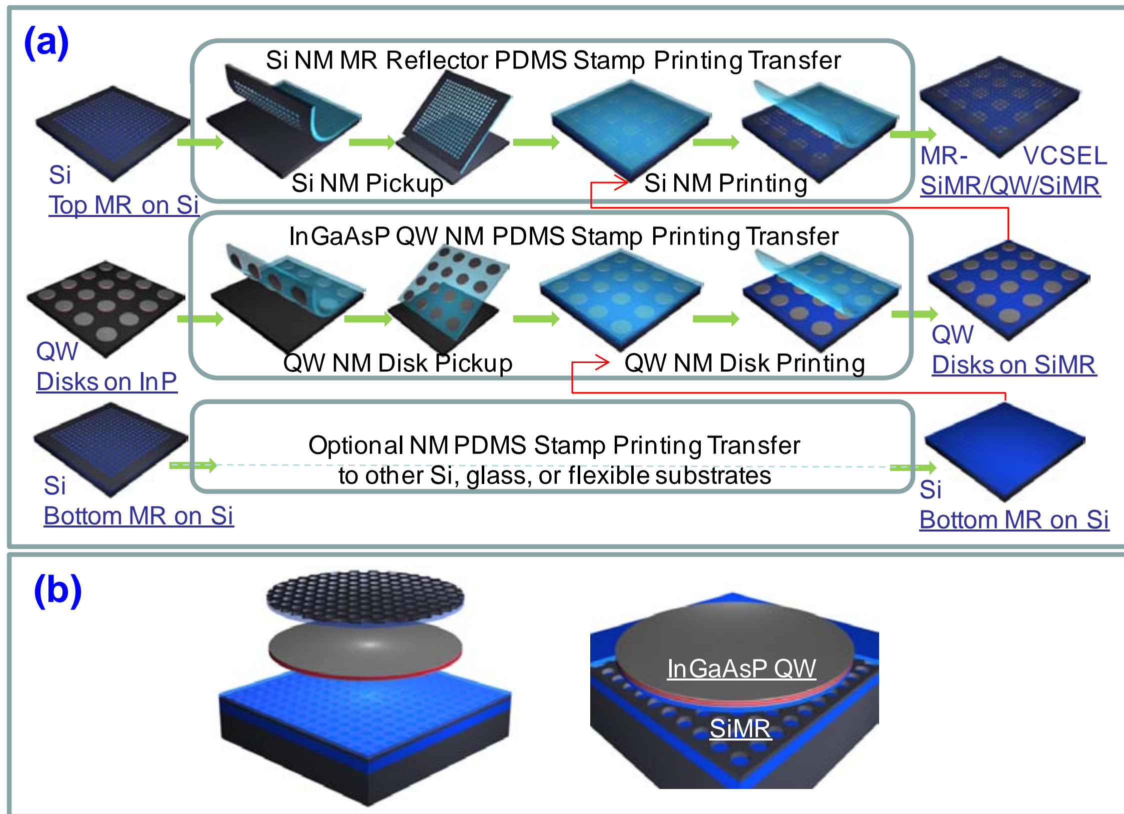

Figure 4.2 MR-VCSEL fabrication based on nanomembrane (NM) PDMS stamp printing process. (a) Schematic illustration of multi-layer PDMS printing process for the formation of a MR-VCSEL array. (b) Schematic of a complete, individual MR-VCSEL device.

The top MR was patterned and released from SOI substrates. Using the PDMS stamp printing transfer process, the top MR was transfer printed to a transparent glass substrate. The top Si MR attached to the glass substrate was then transferred on the top of the InGaAsP QW disks to complete the MR-VCSEL device fabrication. Both the top MR and the bottom MR are in the form of a single piece, while the InGaAsP disks are separated from each other, forming an array of disks. It is worth to note that the transfer printing method that was employed in this work is readily scalable to full wafer size. As shown schematically in Fig. 4.2(a), the lasing cavity consists of a transferred III-V InGaAsP quantum well (QW) heterostructure active region, sandwiched in between two single-layer Si photonic crystal (PC) Fano resonance membrane

reflectors (MRs). These two MRs essentially replace the two multi-layer quarter wavelength DBR (distributed Bragg reflector) mirrors that are commonly used in conventional VCSELs. Fig 4.2(b) schematically illustrates that the quantum well was transfer printed onto the prepared bottom membrane reflector and subsequently integrated top membrane reflector on top of it.

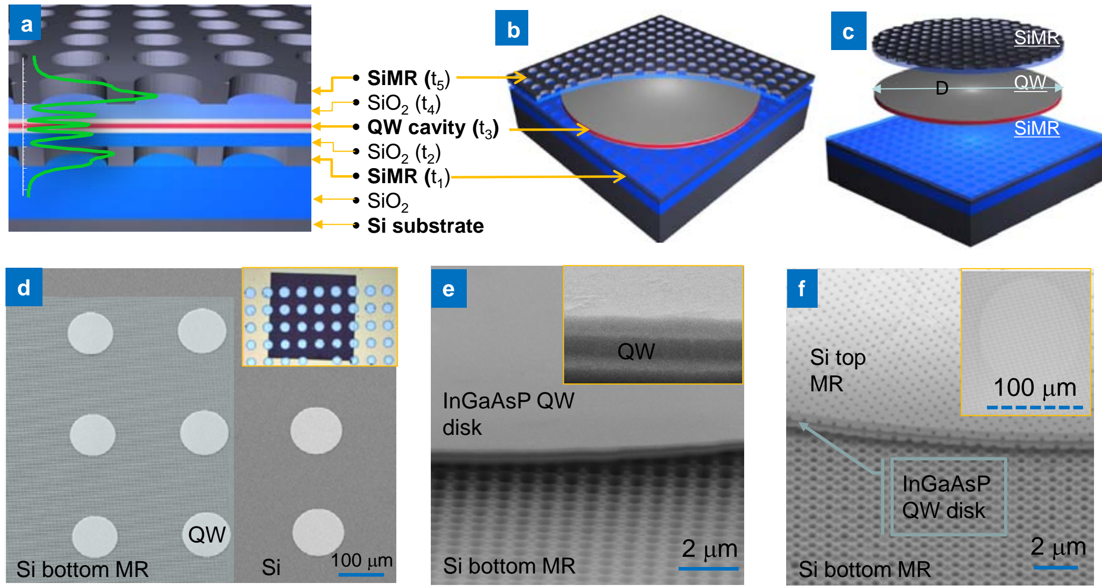

Figure 4.3 Membrane reflector VCSEL (MR-VCSEL) schematic and SEM images are shown in (a) Schematic of a MR-VCSEL lasing cavity, which consists of five layers (t_1-t_5), with total thickness of 1-2 wavelengths. An InGaAsP QW cavity sandwiched in between two single-layer Si Fano resonance photonic crystal membrane reflectors (Si-MR), stacked on a Si substrate. Low index buffer layers are inserted to ensure high reflection MRs. Also shown is a simulated electrical field distribution in the cavity for a lasing mode at 1527 nm, with a confinement factor of 6%. (b) A cut-out view of the complete MR-VCSEL device. (c) Illustration of multi-layer printing process for the formation of MR-VCSEL. The diameter of active area is D. (d) SEM image of InGaAsP QW disks/mesas transferred onto a bottom MR with Si substrate. An optical image is shown in the inset, where the central dark region represents the 1x1 mm2 bottom MRs (photonic crystal patterned area). (e) Zoom-in view of one InGaAsP QW disk on bottom MRs, with the inset shown InGaAsP QW heterostructure. (f) An SEM image of a complete MR-VCSEL device, showing the InGaAsP QW disk sandwiched in between top and bottom Si-MRs. Also shown in the inset is a SEM top view of InGaAsP QW disk underneath large top Si-MR layer.

The use of membrane reflectors results in the lasers to be directly built on Si substrates with much reduced laser size (height), leading to a complete near infrared (NIR) MR-VCSEL cavity thickness to be less than 2 μm (for a total of five layers t_1 to t_5 as defined in Fig. 4.3(a)).

The unique laser features not only enable high performance lasers on Si, but also enable a planar cavity structure allowing much simpler integration schemes with CMOS electronics. Also shown in Fig. 4.3(a) is the simulated optical electric field distribution profile for the designed lasing cavity mode at 1527 nm. A confinement factor of 6% was obtained, which is similar to the values obtained from conventional DBR based VCSELs [86, 87]. Such an ultra-thin cavity also has a much tighter field distribution than DBR based VCSELs, with significantly reduced energy penetration depth and reduced cavity lengths [82, 83]. By further reducing the lateral cavity size down to a few micrometers, such MR-VCSEL can have greatly reduced power consumption, improved power efficiency and higher modulation speed [86, 87].

The multi-layer Si-MR/QW/Si-MR MR-VCSEL cavity (Fig. 4.3(b)) is formed with a semiconductor nanomembrane (NM) transfer printing process [5]. A polydimethylsiloxane (PDMS) stamp is developed and optimized for ultra-thin and large hole-to-neck ratio photonic crystal NM pick-up and transfer, from a source substrate to a foreign destination substrate. The PDMS transfer printing has been applied to a wide range of material systems, with demonstrations of various electronic, optoelectronic, and photonic devices [3, 5, 9, 44, 84, 88]. For the first time, we demonstrated here a multi-layer stacked laser cavity on Si, based on a two-step NM transfer printing process (Fig. 4.3(c)). The high quality active region of the laser cavity, which consists of an undoped strain-compensated InGaAsP QW active region and doped p- and n-InP cladding layers, is obtained via releasing as a membrane from a source InP substrate. To do this, a sacrificial InGaAs layer is first grown on an InP substrate before the growth of the InGaAsP QW active region. The InGaAsP QW active region is released from the InP substrate by selective wet-etching process. The metal organic chemical vapor deposition (MOCVD) grown QW λ-cavity consists of 8 strain-compensated $In_{0.76}Ga_{0.24}As_{0.83}P_{0.17}$ /$In_{0.485}Ga_{0.515}As_{0.83}P_{0.17}$ QWs, with room temperature center emission wavelength at ~1527 nm [89]. To form a complete MR-VCSEL cavity, InGaAsP QW heterostructure was first released and transferred onto the bottom Si-MR, followed by another PDMS transfer of a top Si-MR on

the top of the transferred InGaAsP QW NM. As reported here, despite the stringent requirements in mirror reflectivities (R) and high cavity quality factors (Q), multi-layer high quality PDMS transfer printing is feasible for the construction of MR-VCSEL cavities with high-finesse. Further information on fabrication process can be found in the online Supplementary Information (SI) section.

A scanning electron micrograph (SEM) image is shown in Fig. 4.3(d), for the InGaAsP QW disks transferred onto the bottom Si-MR. Shown here are six QW disks already transferred onto a patterned bottom Si-MR region (another two other QW disks were laid onto the unpatterned Si region). The diameter D of these QW disks (i.e., the active area of the MR-VCSELs) is 100 μm. Shown in the inset of Fig. 4.3(d) is a micrograph of fabricated device top view, with QW disks transferred onto a bottom Si-MR (the square shaped dark color region). A zoom-in view of an InGaAsP QW disk on bottom Si-MR is shown in Fig. 4.3(e), along with a zoom-in view of InGaAsP QW heterostructure λ-cavity shown in the inset of Fig. 4.3(e). A complete MR-VCSEL structure is shown in Fig. 4.3(f), where both the top and the bottom Si-MRs are visible, with an inset showing a single QW disk underneath the top Si-MR layer.

4.4 Characterization of MR-VCSEL Devices

The design and measurement results of the top and the bottom MRs for MR-VCSEL operating at room temperature (RT) summarized in Fig. 4.4. As an alternative to the conventional multi-layer DBRs, single layer, high index-contrast grating (HCG), or guided-mode resonance (GMR) grating and two-dimensional photonic crystal slab (2D PCS) Fano resonance structures that can be used as ultra-compact broadband reflectors hold great promises for a wide range of device applications [27, 34, 69-71] As shown in Fig. 4.4(a), a fabricated 2D PCS with square lattice of air holes on SOI is used for MRs. The key design parameters are lattice constant (a), radius of air holes (r), and thickness of Si-MR (t_{si}). For all the MRs reported here, the Si layer thickness is 340 nm. The design and configuration are applied here for MR-VCSEL cavities with cavity resonance, operating at room temperature, as shown in Fig. 4.4(b-d). For

the top MR used in this lasers reported here, we first transfer the fabricated Si-MR on a transparent glass substrate, and then transfer the glass substrate holding the Si-MR onto the top of the InGaAsP QW disks. The simulated and measured reflection spectra are shown in Fig. 4.4(b), for the top Si-MR with its spectral band centered about 1550 nm so as to match the InGaAsP QW emission wavelength at room temperature. The bottom Si-MR, on the other hand, is directly fabricated on a SOI substrate, followed by a plasma-enhanced chemical vapor deposition (PECVD) of a thin SiO_2 film on top of it, with SiO_2 layer thickness t_2 ~ 350-400 nm as an intermediate lower refractive index layer, depending on the desired cavity resonance spectral location. Notice that other low refractive index materials such as Al_2O_3, or diamond can also be used, for improving thermal conductivity. A cross-sectional SEM image is shown in Fig. 4.4(c), where the high index patterned Si-MR layer is embedded in between the top and the bottom lower index oxide layers. Shown in Fig. 4.4(d) is shown the simulated and measured reflection spectra for the bottom Si-MRs with a top SiO2 thickness t_2 of 365 nm for the purpose of spectrally tuning [43] the reflection band to a centered wavelength of 1550 nm. The SEM images without and with the top SiO_2 layer are also shown in the insets of Fig. 4.4(d). Notice that due to different vertical index profiles for the top and the bottom MRs, different sets of design parameters (a, r) are used in order to have the reflection spectral band cover the designed wavelengths. All the reflectors designed and demonstrated here have peak reflection values >99%, with different high reflection bands.

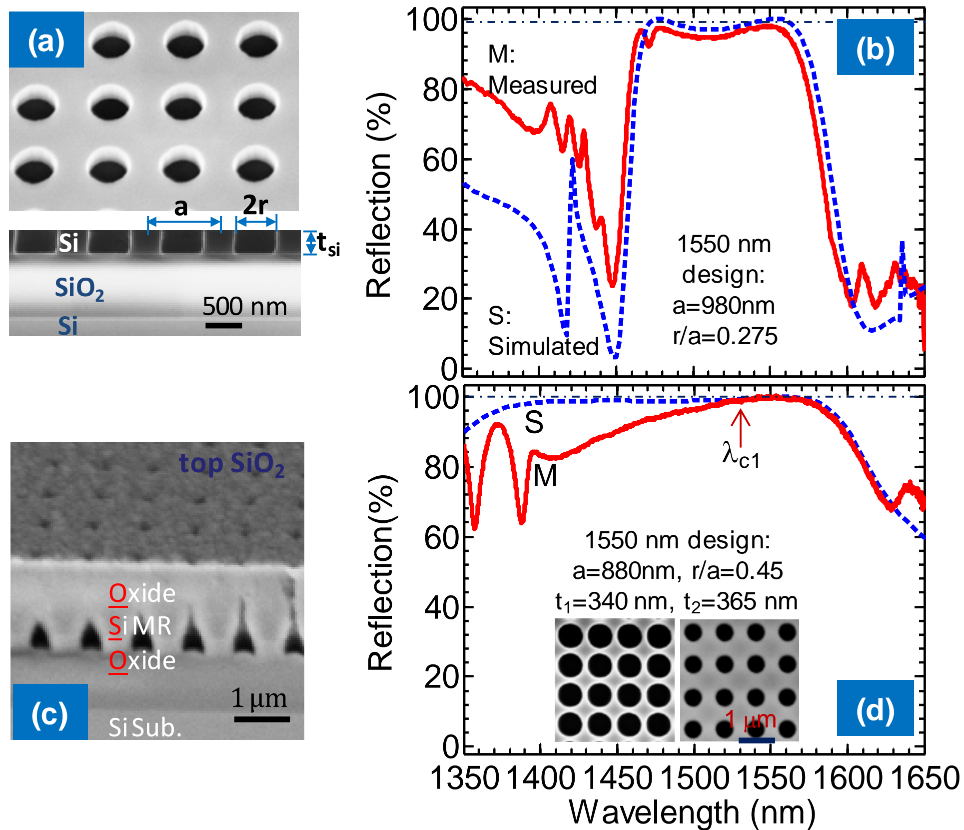

Figure 4.4 (a) Scanning electron microscope (SEM) image of top and cross-sectional zoom-in views of a fabricated Si-MR sample on SOI substrate. Key design parameters for the square lattice air hole Si photonic crystal structure are also shown, including lattice constant a, air hole radius r, and membrane thickness t_{si}. (b) Simulated (S) and Measured (M) reflection spectra of top Si-MR on glass substrate designed for 1550 nm spectral band for operating at room temperature. (c) an SEM image of a fabricated bottom MR sample on SOI substrate, with SiO_2 low index buffer layer (t_2) deposited on top of it. (d) Simulated (S) and Measured (M) reflection spectra for bottom Si-MR (with SiO_2 t_2 layer on top) designed for 1550 nm spectral bands. Shown in insets are SEM top view images of bottom Si-MR before and after SiO_2 (t_2) layer deposition.

Fig. 4.5(a) shows a micrograph image of the transferred Si-MR onto glass. The design parameters of MRs for MR-VCSEL resonance cavities are employed here for operating at low temperature (LT), as shown in Fig. 4.5(b-d). The simulated and measured reflection spectra of the top Si-MRs on glass substrate with its center wavelength of approximately 1450 nm in order to match the InGaAsP QW spontaneous emission wavelength at low temperature are shown in

Fig. 4.5(b) including, the design parameters of top Si-MR. The inset shows the SEM top view image of top Si-MR transferring onto glass substrate. A micrograph image is also shown in Fig. 4.5(c) for a fabricated 1x1 mm^2 bottom Si-MR on the SOI substrate. Fig. 4.5(d) shows the simulated and measured reflection spectra for the bottom Si-MR which is deposited a lower refractive index SiO_2 on top with thickness t_2 of 383 nm in an attempt to match the spectral band centered about 1450 nm. The insets of Fig. 4.5(d) show the SEM images without and with the top SiO_2.

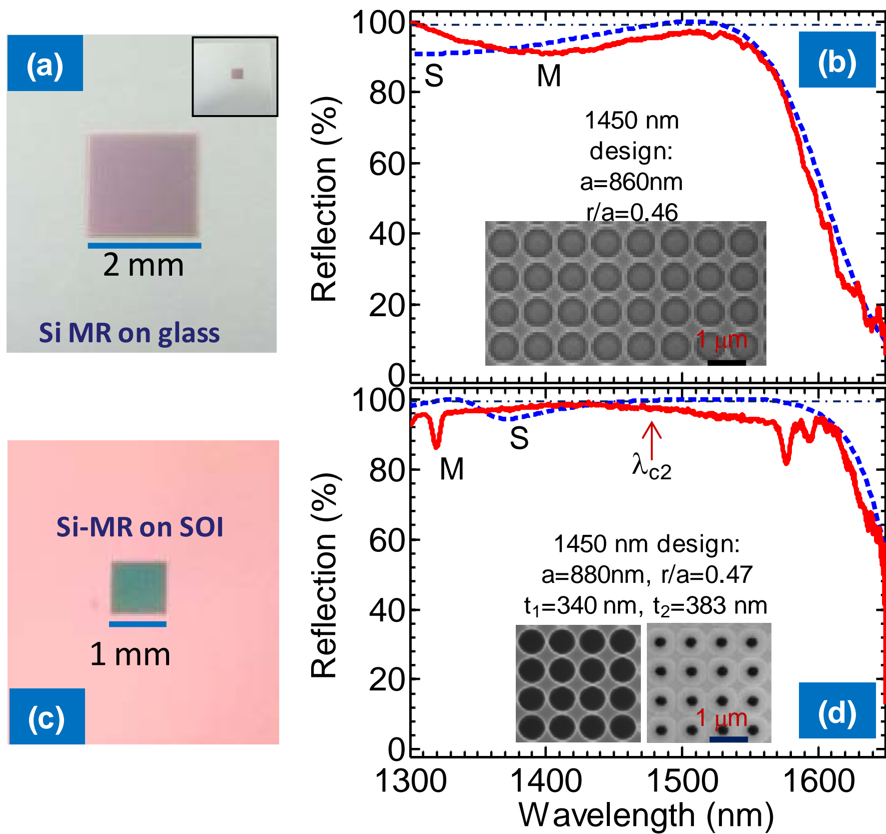

Figure 4.5 (a) A micrograph image of a fabricated Si-MR which is transferred onto glass substrate, serving as the top MR of MR-VCSEL cavity. (b) Simulated (S) and Measured (M) reflection spectra for top MR (Si-MR on glass) designed for 1450 nm spectral band for operating at low temperature, with the inset showing a zoom-in SEM image of a 2x2 mm^2 sized top Si-MR on glass. (c) A micrograph image of a fabricated Si-MR on an SOI substrate, serving as the bottom MR of MR-VCSEL cavity. (d) Simulated (S) and Measured (M) reflection spectra for bottom Si-MR (with SiO_2 t_2 layer on top) designed for 1450 nm spectral bands. Shown in insets are SEM top view images of bottom Si-MR before and after SiO_2 (t_2) layer deposition.

Lasing cavity design was carried out carefully to understand the lasing cavity properties. Great care was taken to design and separate the competing lasing cavity modes from the waveguide modes within the InGaAsP QW λ-cavity region. Due to drastically different phase differences, and different reflection mechanisms, the cavity resonance modes, along with the field distribution profiles, are quite dissimilar to the lasing cavities formed by two conventional DBRs [82]. Despite the relatively large field concentration in the high index Si-MR layer, the lasing mode field confinement factor or the longitudinal confinement factor (i.e., the overlap between the standing wave field distribution and the QW active region) is about 6% for MR-VCSELs, which is comparable to DBR-based VCSELs.

$$\Gamma_{\mathrm{z}} = \frac{\int_{thickness\ of\ QWs} E^2(z)dz}{\int_L E^2(z)dz} \approx \frac{d}{L}\Gamma_{\mathrm{r}} ,$$

where Γ_{z} is the longitudinal confinement factor, L is the resonant cavity length, d is total thickness of QW, and Γ_{r} is defined as relative confinement factor. In our case, d is 0.060 μm, L is roughly equal to 2 μm, and Γ_{r} is just about 2 [87]. Such high confinement factor may be a result of the much reduced lasing cavity length and stronger cavity confinement, due to the reduced field penetration depths [90], and MR large index contrasts. Si-MR Two types of MR-VCSEL devices were fabricated for low temperature (LT) and room temperature (RT) operations. Shown in Fig. 4.6 - 4.7 are the measured characteristics of the MR-VCSEL fabricated based on the LT and RT designs that are shown in Fig. 4.4 - 4.5. Notice that the total vertical cavity thickness is only 2.4 μm. All tests were carried out based on monochromater based optically pumped micro-photoluminescence (μPL) setup, with the sample placed inside a cryostat as depicted in Fig. 4.8. The optically pumped MR-VCSELs were characterized with a 320 nm focal length monochromater based μPL setup and mounted inside a cryostat for ambient temperature control from T=10K to T=300K. A continuous wave green laser at a wavelength of 532 nm was launched perpendicularly onto the MR-VCSEL via a long working distance objective lens, with a chopper and lock-in amplifier for data acquisition. Spectrally

resolved lasing output was detected with a TE-cooled InGaAs photodetector. Notice that the optically pumped power was calibrated as the incident power onto MR-VCSEL, assuming the lasing beam size is similar or smaller than the MR-VCSEL lateral dimension of 100 μm. The actual power absorbed by the lasing cavity may be smaller, considering top mirror reflection, and QW absorption layer thickness. The use of 532 nm CW laser as the pump laser source also induces excessive energy loss (heat) on MR-VCSEL cavity region, which leads to increased lasing threshold and reduced light power efficiency of MR-VCSEL. Light emitted from the MR-VCSEL was collected via the same long working distance objective lens and separated with a cold mirror (which passes 1550 nm infrared signal and reflects 532 nm pump signals). Light output spectra were collected for different pumped power levels at different ambient temperatures. Output power was taken as the lasing peak power. In order to estimate the output power levels, a 1550 nm commercial DFB laser source was placed at the sample location and have the output power launched into the PL setup, with exactly the same optical configuration as the MR-VCSEL light collection scheme. By correlating the lock-in amplifier readout and the actual lasing power based on the1550 nm DFB laser, we estimated the MR-VCSEL output power, based on the lock-in amplifier output.

The L-L plot (light output for different pumped light input powers) and the corresponding spectral linewidths are shown in Fig. 4.6(a) for a LT design of MR-VCSEL device. The threshold pumped power is just about 8 mW, or 0.32 kW/cm^2. The measured spectral linewidths reduce from 30 nm below threshold to 0.6 - 0.8 nm above threshold. The measured spectral outputs are shown in Fig. 4.6(b), for pumped powers below, at, and above thresholds (points i, ii, iii, and iv at L-L curve). For better visibility, the below-threshold spectrum is magnified and shown in the left inset of Fig. 4.6(b). The lasing spectral linewidth is 8 Å, which is limited by the measurable resolution of monochromater. Also, right inset is a measured far-field image for the MR-VCSEL biased above threshold (point (iv) at L-L curve), with collimated circular single mode output. The relative peak location shift shown in Fig. 4.6(b) from bias levels (ii) and (iii, iv)

is mostly related to mode hopping and temperature rise inside the active region at higher pumped input power levels. The peak shift is also evident in Fig. 4.6(c), where the lasing peak locations shift towards longer wavelengths with the increase of temperature, at a rate ($d\lambda_c/dT$) close to the simulated 0.088 nm/K. There is a mode hopping occurred below and above the operation temperature of 80 K. MR-VCSEL device was characterized at different temperatures up to 120 K, which is mainly limited by the MR reflector bandwidth. For reference, also shown in Fig. 4.6(c) is the measured temperature dependent emission peak from as-grown QW sample. The QW emission peak has a red-shift at a rate of 0.43 nm/K as temperature rises. For this set of low temperature MR-VCSEL samples, the measured temperature dependent lasing threshold is shown in Fig. 4.6(d), where the extracted characteristic temperature is 125 K.

A different set of MR-VCSELs was also fabricated for quasi- continuous wave mode lasing at RT, with reflection spectra of both top and bottom MRs centered at the 1550 nm band (RT design). The optical characteristic results are shown in Fig. 4.7(a). The pumped threshold is 18 mW, very similar to the low temperature threshold at 120 K (Fig. 4.6(d)). The lasing spectral linewidth is ~0.9 nm. Currently this MR-VCSEL thermal performance is limited by the use of low index SiO_2 layer, which has very poor thermal conductivity about 1.4 $Wm^{-1}K$ comparing to thermal conductivity of diamond about 2200 $Wm^{-1}K$.

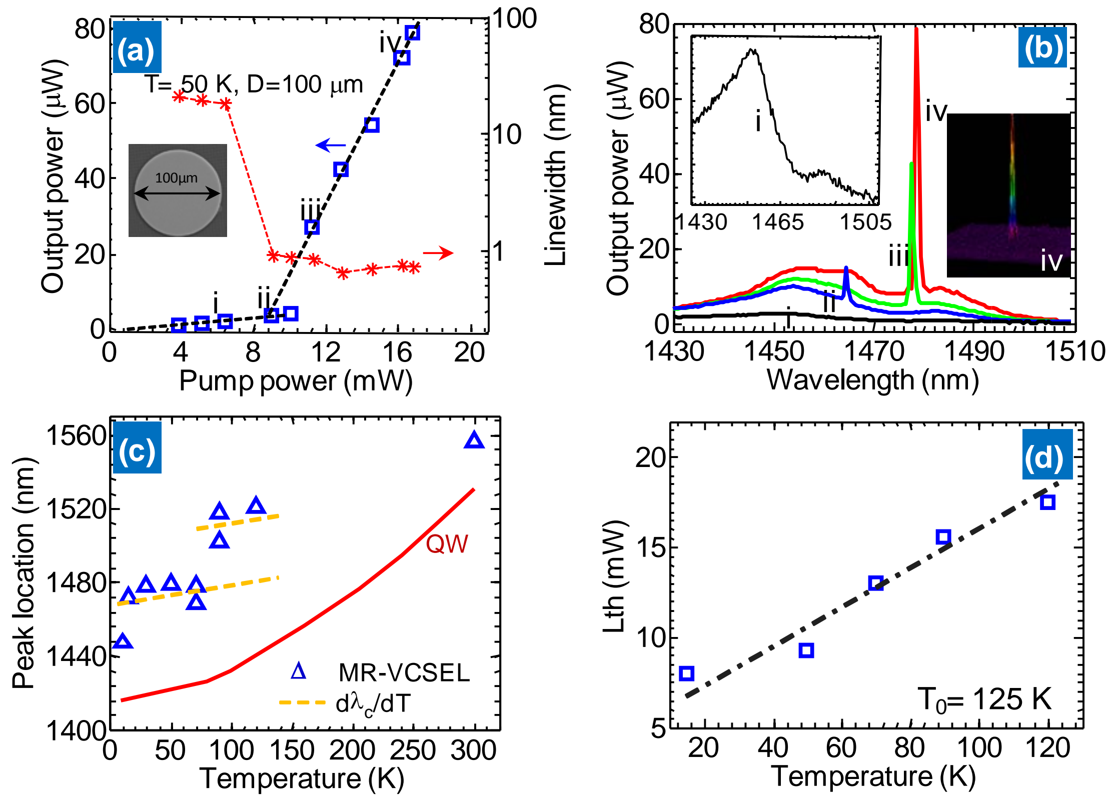

Figure 4.6 Low temperature MR-VCSEL performances with low temperature design MRs. (a) Laser output power at the lasing wavelength and lasing linewidth versus the input pumped power. The sample was cooled at temperature = 50 K and pumped with a chopped continuous wave (CW) green laser. The lateral lasing cavity diameter is D = 100 μm (inset), with a total vertical cavity thickness ~ 2.4μm. (b) Measured spectral output of the MR-VCSEL at three pumped power levels, below threshold (i), at threshold (ii) and above thresholds (iii, iv). The spontaneous emission below threshold (at pumped power point i) is shown in the left inset. Also shown in the right inset is the far-field (FF) image above threshold (point iv). (c) Measured MR-VCSEL lasing peak locations, along with the calculated cavity resonance shift ($d\lambda_c/dT$=0.088 nm/K), at different temperature for both low and room temperature (LT and RT) designs. Also shown is the measured as-grown QW emission spectral shift with temperature. (d) Measured lasing threshold power for different temperatures. A characteristic temperature T_0 is extracted to be 125 K.

Multi-wavelength MR-VCSEL arrays can be further realized by simply varying the photonic crystal MR lattice parameters. Here we show the different lasing wavelengths in Fig. 4.7(b) based on MRs with the LT design and the RT design. For the LT design cavity, lasing wavelengths of 1448 nm (at 10 K), 1478 nm (at 50 K), and 1520 nm (at 120 K) were obtained at

different setting temperatures. For the RT design cavity, lasing wavelength of 1556 nm was obtained. These lasing wavelengths match well with the cavity resonances based on the different designs.

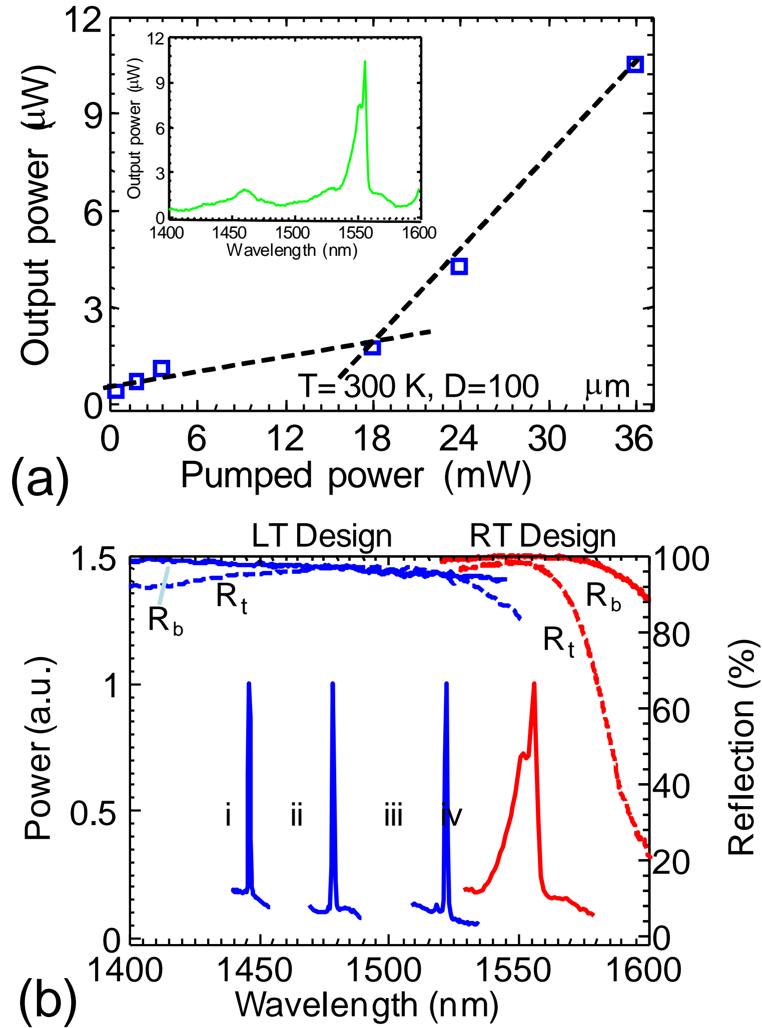

Figure 4.7 RT Design MR-VCSELs and multi-spectral lasing. (a) Laser L-L curve at room temperature for the RT Design MR-VCSEL device. Shown in the inset is the measured spectral output above threshold at pumped power 36mW. (b) Measured MR-VCSEL spectral outputs at different temperatures for both LT and RT Designs: (i) T = 10 K; (ii) T = 50 K; (iii) T = 120 K; and (iv) T = 300 K. Portions of measured top (R_t, dash lines) and bottom (R_b, solid lines) reflection spectra are also shown for both LT and RT designs.

It can be clearly seen that the MR-VCSEL device suffers from the thermal dissipation when it was pumped with 532 nm laser and operated at room temperature (Fig. 4.7(a)). The drastic increase of light threshold of MR-VCSELs to 18 mW operated at T=300K mainly because of the heat inside the active region generated by pump laser excitation. To utilize the pumped power efficiently and achieve the low light threshold, the 980 nm pump laser was used instead of 532 nm laser so that the heat in the active region can be decreased. Fig 4.8(a) shows the emission peak output of MR-VCSEL device as a function of pumped power input for both 980 nm and 532 nm lasers. The pumped threshold is significantly reduced to 1.9 mW as the 980 nm laser was employed at 15K as shown in the inset of Fig. 4.8(a). With the same device, the pumped threshold increase to 10 mW when MR-VCSEL device was pumped with 532 nm laser as shown in same Fig 4.8(a). The measured MR-VCSEL spectral outputs at T=15K with 980 nm laser was shown in Fig. 4.8(b) with lasing peak at wavelength of 1450 nm. Similarly, the measured MR-VCSEL spectral outputs at T=15K with 532 nm laser was also shown in Fig. 4.8(b) with lasing peak at wavelength of 1480 nm. Fig. 4.8(b) confirmed that the lasing wavelength of MR-VCSEL device shifts due to the 532 nm pump laser creating heat inside the active region compared to another one. The reflections of top and bottom membrane reflectors for MR-VCSELs are also shown.

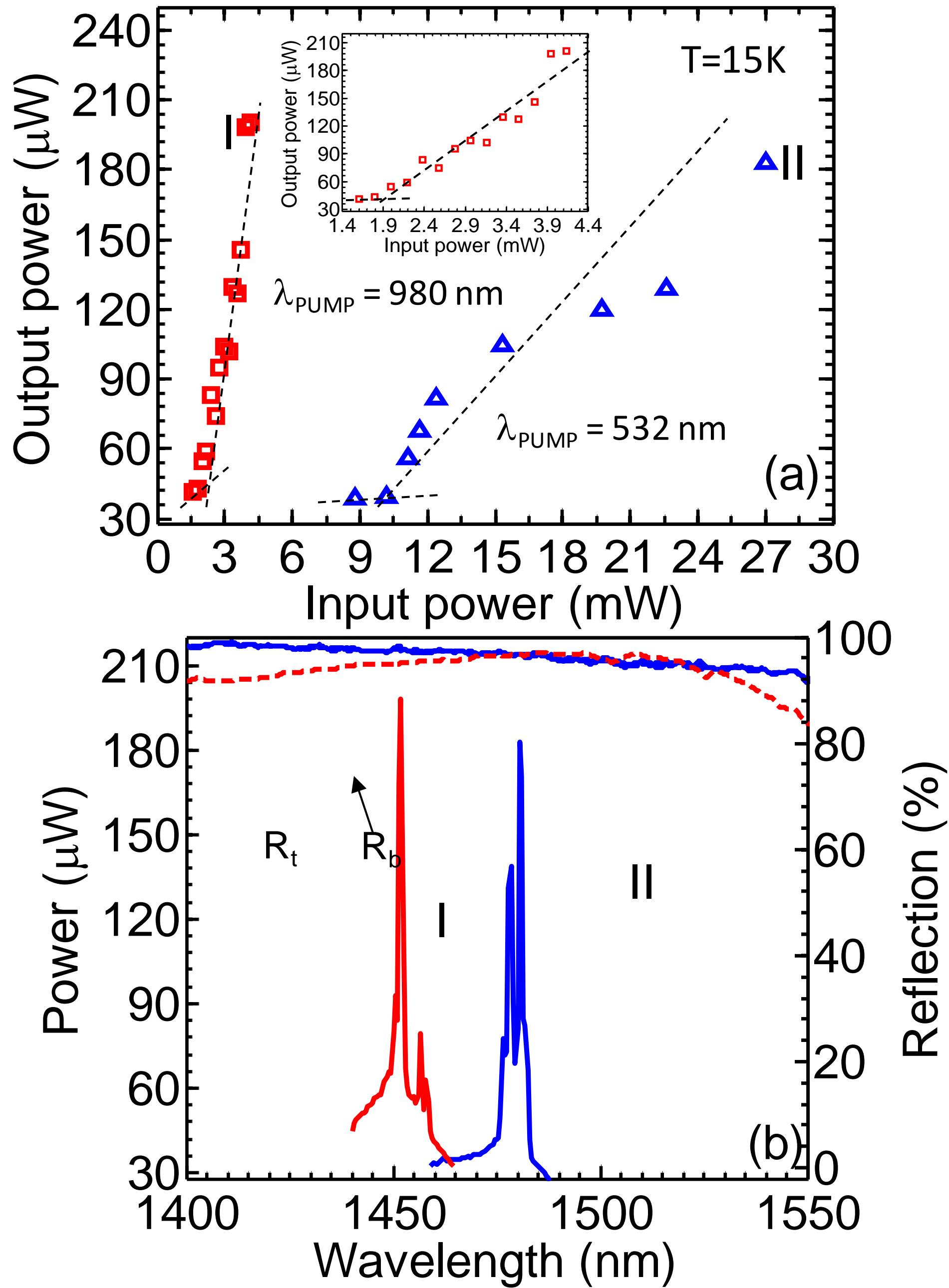

Figure 4.8 Different pumping schemes to reduce light threshold of MR-VCSELs. (a) Laser L-L curve at T=15K with either 980 nm or 532 nm pump laser. (b) Measured MR-VCSEL spectral outputs at T=15K with pump laser both 980 nm and 532 nm: (i) pump laser 980 nm; (ii) pump laser 532 nm. Measured top (R_t, dash red lines) and bottom (R_b, solid blue lines) reflection spectra are also shown.

Figure 4.9 Schematic of optically pumped micro-photoluminescence (μPL) setup based on monochromater TRIAX320 spectrograph both for LT and RT measurements and a 300mW green laser (532nm) are employed as a pump laser.

4.5 Toward Electrically Pumped MR-VCSEL Devices

The samples were fabricated on InP substrate with multiple quantum wells as the active region. The active region is formed by eight compressively strained quantum wells separated by quaternary barriers with tensile strain, leading to an overall strain-compensated structure. Molecular beam epitaxy has been used for growth of InGaAsP/InP QW cavity to exhibit precisely control thickness of the layers structure since the wavelength of operation of VCSELs is directly related to the layer thickness of QW structure. A simply epitaxial structure grown on InP substrate (n+) as employed for these devices shown in Fig. 4.10.

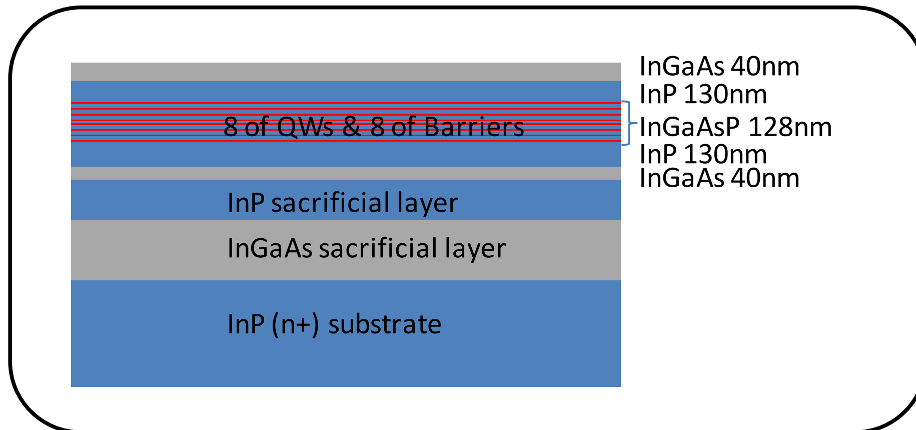

Figure 4.10 A typical epitaxial structure grown on InP substrate as used for electrically pumped devices.

The electrically pumped device fabrication process is depicted schematically in Fig. 4.11. The first step requires the standard photolithography, O_2 plasma treatment, metal deposition and a liftoff process. For this p-ring mask, a negative resist (AZ-5214) layer is transferred onto the starting epitaxial wafer to create a resist undercut which is easy for liftoff process. To remove residue of unwanted resist after developing, plasma processing is efficient method of surface cleaning. For the metal rings forming the p-ring top contacts with layer sequence of Pd/Zn/Pd/Au (10/10/20/200 nm) on InGaAsP/InP wafer to avoid surface damage due to subsequent steps and defining next masks for the later p-mesa etching is deposited using AJA electron beam evaporation. Then the sample is immerged into AZ-300T stripper at 80° C for 10 to 30 minutes for liftoff process as shown in Fig. 4.11(a). Second, the photolithography using positive resist (AZ-1813) with p-mesa mask and wet etching are needed. After p-mesa pattern is perfectly aligned, transferred on top of the p-ring contacts, and baked to harden the photoresist at 130°C for 60 sec, wet etching is employed to etch through the cladding, barrier, and QW layers until reaching N-contact layer. The p-mesa is formed using selective chemical wet etching solutions consisting of $HF:H_2O_2:H_2O$ (1:1:10) to etch InGaAs at etching rate 7nm/sec and InGaAsP at etching rate 6.5nm/sec and HCl : H_3PO_4 (1:4) to etch InP at etching

rate 5.5nm/sec under stirring hotplate at 50 rpm. This step is very crucial since resist has to be strong enough to protect devices during multiple times of wet etching as shown in Fig. 4.11(b). After finishing wet etching, cleaning resist with AZ-300T stripper at 80°C for 10 minutes and following by rinsing with acetone/isopropanal. Third, this step is similar to the first one except that metal rings forming the n-ring bottom contacts with layer sequence of Ni/Ge/Au/Ti/Au (12/20/30/10/200 nm) on InGaAs contact is deposited using AJA electron beam evaporation and performing standard photolithography with n-ring mask. Then liftoff and cleaning sample by using AZ-300T stripper at 80°C for 10 to 30 minutes and acetone/isopropanol respectively as shown in Fig. 4.11(c). Rapid thermal annealing (RTA) in N_2 ambient is required to make the good ohmic contacts. It is worth to note that RTA is very critical for our devices. Therefore, in our case we use well calibrated annealing recipe at 200/300/200°C for 30/120/30 sec following by checking I-V characteristics of devices before and after RTA. Then photolithography using n-mesa mask for n-mesa etching is employed to etch away opening area of bottom contact. Since this step requires only wet etching for InGaAs bottom contact, hard bake photoresist (AZ-1813) at 130°C for 60 sec is needed before selective wet etching following by cleaning resist with acetone/isopropanal as shown in Fig. 4.11(d). Next step is SiO_2 deposition to passivate the devices. The mesas are now covered by thin layer of SiO_2 with thickness of 400 nm. Then photolithography using SiO_2-mesa mask is transferred pattern to the whole surface of sample. The combination of selective wet etching and RIE etching can be employed to etch away opening area of thin SiO_2 layer. Since this step requires both wet etching and dry etching to etch away SiO_2 passivation layer, hard bake photoresist (AZ-1813) is uncritical. In our case, RIE etching (power=150 watts; pressure=130 mtorr; gas CF_4=15 sccm; etching rate=50 nm/min) has been using to etch about 90% of total thickness of SiO_2 and other 10% of the remaining SiO_2 will be etched by selective wet etching solution of HF(49%):H_2O (1:10) with etching rate of SiO2 about 100 nm/min. After finishing this step, removing resist with AZ-300T stripper at 80°C for 10 minutes then rinsing sample with acetone/isopropanol. For opening

contacts using an open-hole mask, a negative resist (AZ-5214) layer is transferred onto the top surface of devices. Similarly, plasma processing can be employed to remove unclean patterning area after developing. In this step, only RIE etching is preferred following the recipe mentioning earlier. The opening area can be over etched in this case to make sure that all required contacts are fully uncovered then cleaning resist with AZ-300T and acetone/isopropanal respectively as shown in Fig. 4.11(e). The standard photolithography is employed to transfer an interconnection pattern from an interconnect layer mask to AZ-5214 resist onto both p-ring and n-ring contacts. Then O_2 plasma is applied to remove the residue of resist after developing. Finally, the last step is transferring devices onto prepared bottom mirror which has been deposited SiO2 thickness of 400 nm to tune reflection spectral matching with spontaneous emission of QWs. From the last previous step, sample is covered by Apiezone wax (mixture of Aapiezone wax and TCE) and left in the air at least 6 hours or waiting until wax harden enough for substrate removal. The selective chemical wet etching solutions consist of HCl : H_3PO_4 (1:1) to etch InP substrate at etching rate 42nm/sec, HF:H_2O_2:H_2O (1:1:10) to etch InGaAs sacrificial layer at etching rate 7nm/sec, and HCl : H_3PO_4 (1:4) to etch InP sacrificial layer at etching rate 5.5nm/sec under stirring hotplate at 50 rpm for all of them. After finishing substrate removal, putting one drop of clean DI water on top of prepared bottom mirror, placing sample (devices) and adjusting the position of sample (devices) to match with an area of prepared bottom mirror. If satisfied with the position of sample, at this point you have to remove an excess of DI water with small wipe paper by gently absorbing it. Typically, sample must be left under pressure p=0.2 N/mm^2 more or less using metal weight and cleanroom swap placing on top of sample for more than 24 hours or even longer since a surface of prepared bottom mirror is not smooth enough to form good Van der Waals bonding between QWs thin film and prepared bottom mirror. To improve the bonding quality, chemical mechanical polishing (CMP) process can be performed to smooth surface of prepared bottom mirror before bonding. Gently removing metal weight and cleanroom swap, and slowly cleaning Apiezone wax with TCE. After

wax is cleaned completely, O_2 plasma treatment (RIE power=100 watts; pressure=100 mtorr; gas O_2=100 sccm; time=30 sec) is employed to remove residue of remaining TCE from the sample. Immediately, loading sample into load lock chamber of electron beam evaporator and waiting for an hour to minimize the pressure difference between main chamber and load lock chamber.

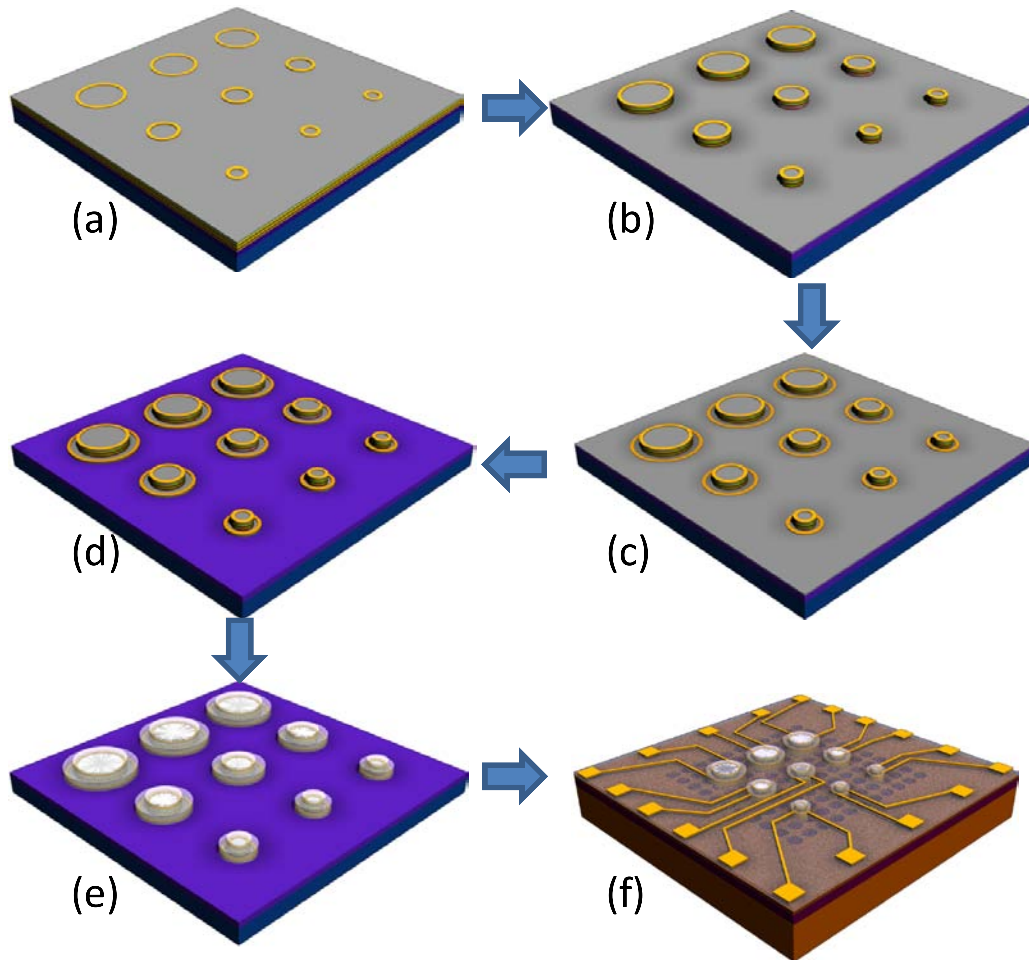

Figure 4.11 Fabrication processes of electrically pumped devices. (a) P-ring metallization; (b) P-mesa etching; (c) N-ring metallization; (d) N-mesa etching; (e) SiO2 mesa etching and open-holes etching; (f) Metallization after removing wax with TCE.

Then contact metallization with layer sequence of Ti/Au (12/200 nm) is evaporated at slow deposition rate. After finishing metallization, left sample inside the vacuum chamber for an hour

before taking it out for better bonding adhesion. Then sample is immerged in AZ-300T stripper at 80° C for 30 minutes for liftoff process before it is gently cleaned with acetone/isopropanol as shown in Fig. 4.11 (f). Fig. 4.12(a) shows the microscope image of sample after finishing sacrificial layers and substrate removal including the resist pattern and Fig. 4.12(b) shows microscope image of sample after finishing Ti/Au metallization.

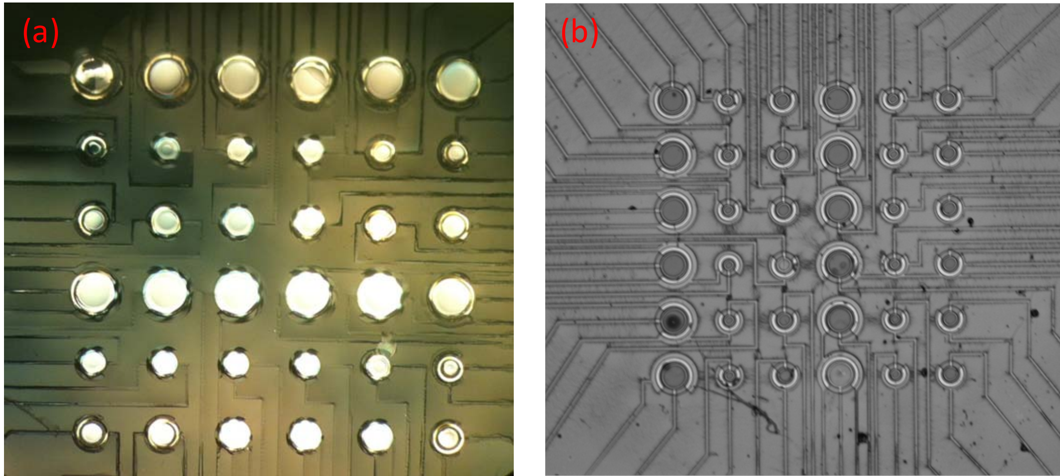

Figure 4.12 (a) Sample after finishing substrate removal; (b) Sample after finishing metallization.

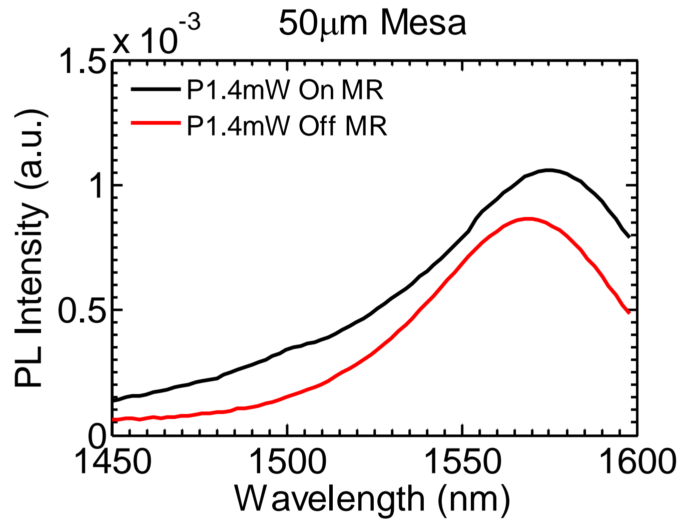

Figure 4.13 Photoluminescence of device size 50 μm mesa comparing between device on MR and off MR.

After sample is immerged into AZ-300T stripper at 80° C for 30 minutes for last liftoff process, it is rinsed with acetone/isopropanol and naturally dried.

Fig. 4.13 shows photoluminescence of fabricated devices with 980 nm CW laser as the pump laser source for the same 50 μm mesa sizes comparing between device on MR and off MR. As we can see that the peak photoluminescence intensity at the wavelength of 1580 nm on MR is higher than that off MR because of the effect of higher reflection on the area of MR.

Fig. 4.14(a) to (d) show L-I characteristics of transferred devices and devices on InP substrate comparing with the same devices before and after transferring. It can be clearly seen that all devices on SiO_2/SOI substrate show electroluminescence intensity at wavelength of 1580 nm more than those on InP substrate about four times at least. All devices have been investigated varying from 10 μm to 100 μm mesa sizes.

Fig. 4.15(a) confirms that all results are reasonable since the reflection square of SiO2/SOI substrate is higher than that of InP substrate by about five times. Fig. 4.15 (b) shows microscope image of transferred devices.

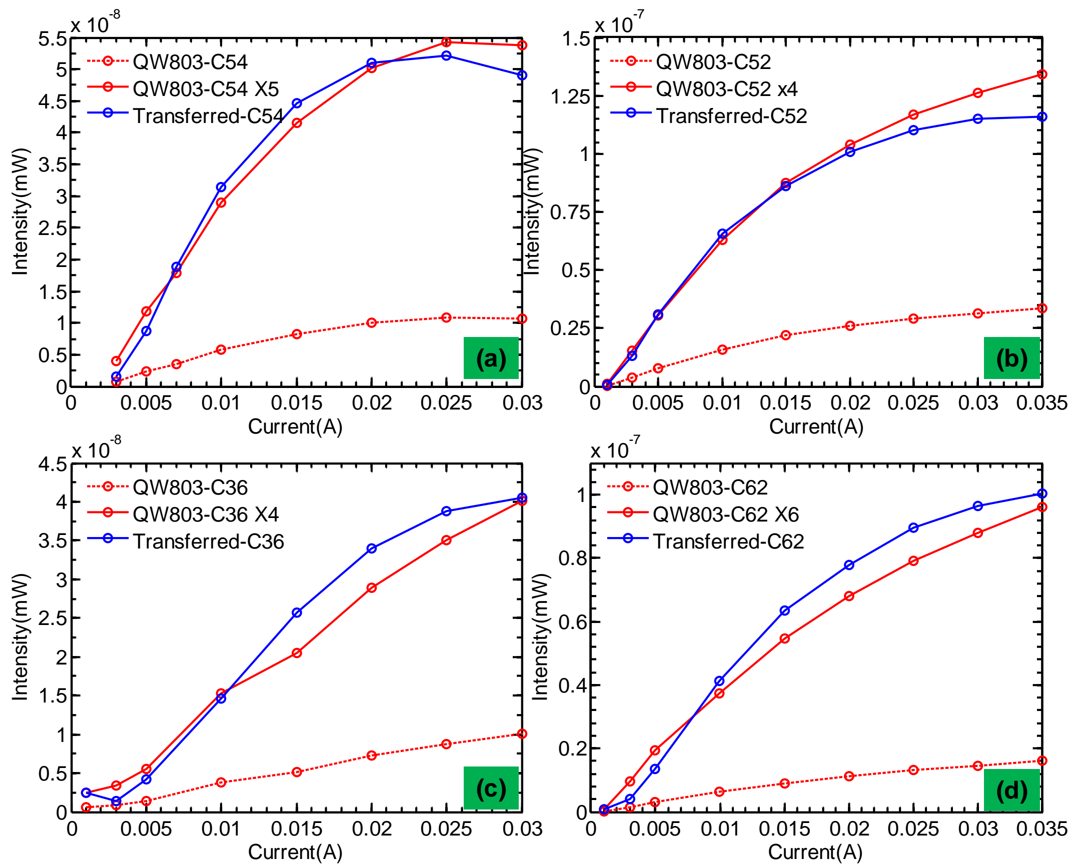

Figure 4.14 L-I characteristics of transferred devices on SiO_2/SOI substrate comparing to those on InP substrate.

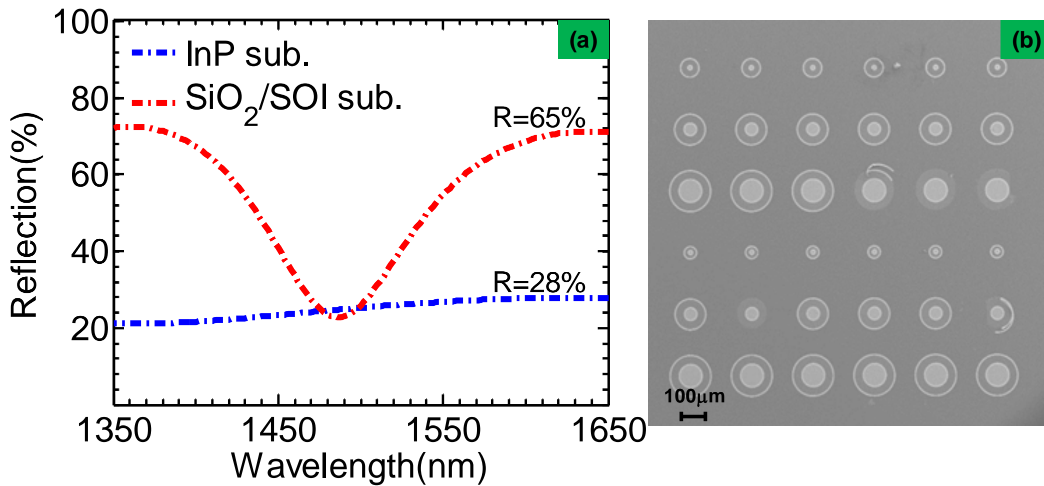

Figure 4.15 (a) Simulated reflection of InP substrate and SiO2/SOI substrate. (b) SEM image of transferred devices onto SiO2/SOI substrate.

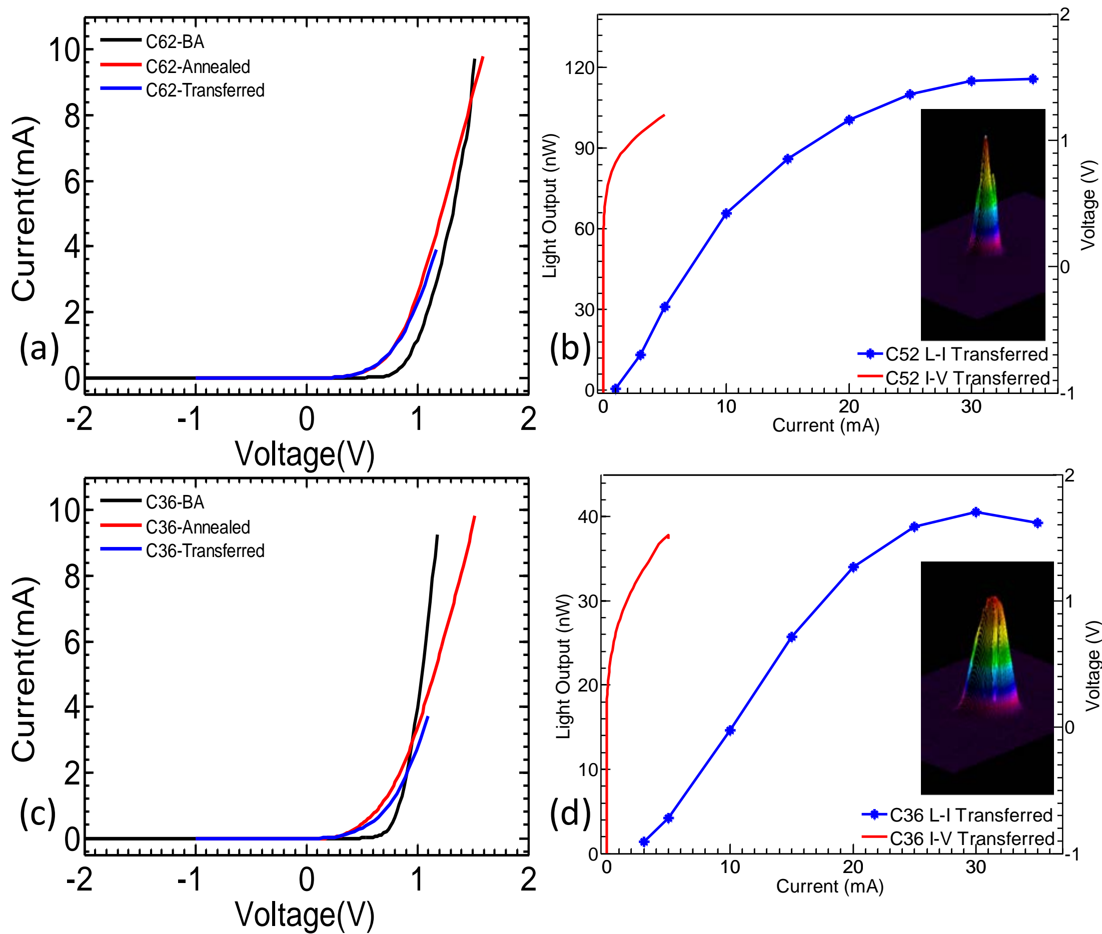

Figure 4.16 I-V characteristics of devices (a) 50 μm mesa (c) 100 μm mesa before and after transferring. L-I-V characteristics of transferred devices (b) 50 μm mesa (d) 100 μm mesa on SiO_2/SOI and insets show far-field images at maximum intensities.

All devices also have been characterized in terms of I-V characteristics as shown in Fig. 4.16 (a) and (c) where same devices before and after annealing are plotted together a long with same devices after transferring. It can be clearly seen that I-V characteristics of devices after annealing increase because RTA process reduces the ohmic contact resistance considerably. In addition to that, I-V characteristics of transferred devices are the same as those of devices on InP substrate. Remarkably, it is shown that the transfer quality is very good and does not degrade the performance of all devices in terms of I-V curves after using

photoresist pattern to help mesas firmly adhere to new substrate. Also L-I-V characteristics of transferred devices with different mesa sizes of 50 μm and 100 μm have been investigated as shown in Fig. 4.16(b) and (d) respectively. Insets of Fig. 4.16(b) and (d)show far-field images of both 50 μm and 100 μm mesa sizes biased at 30 mA measured by beam profiler.

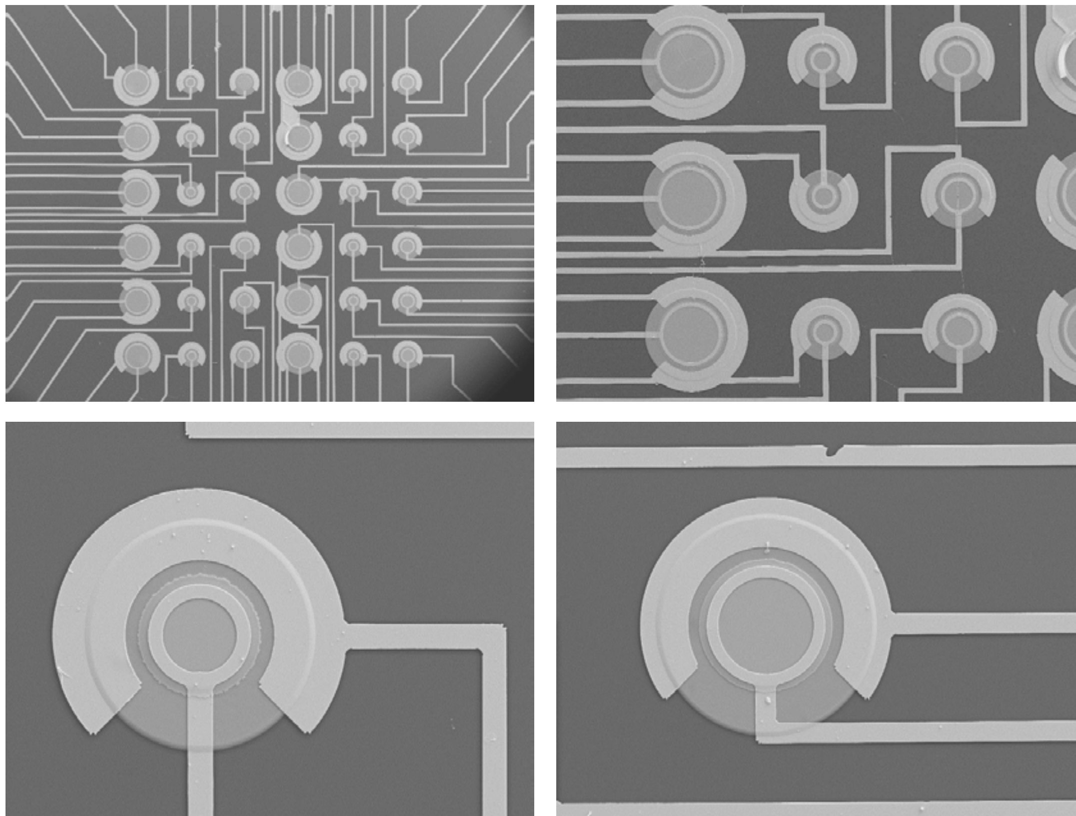

Figure 4.17 SEM images of transferred devices onto SiO_2/SOI.

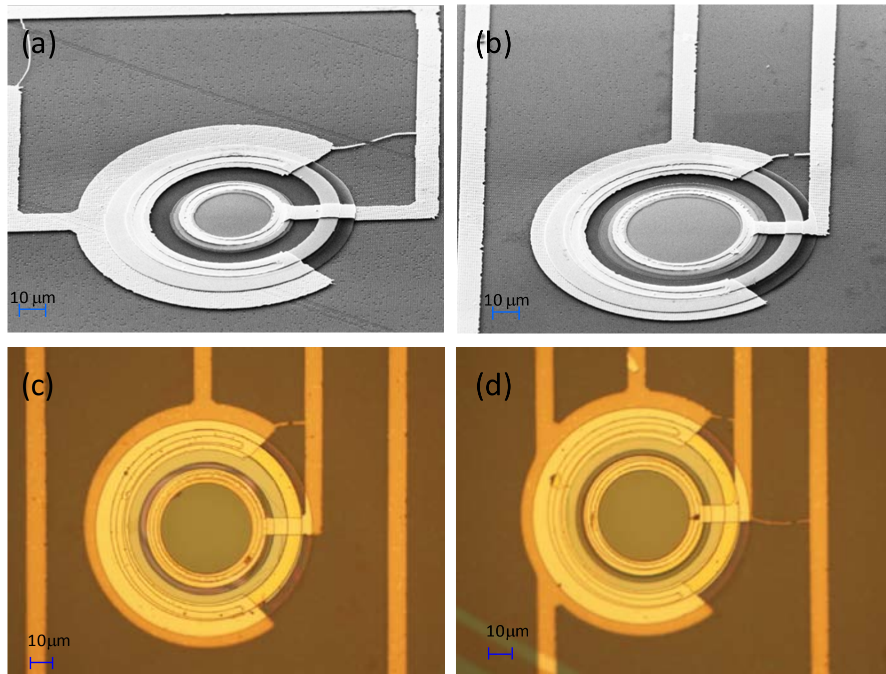

Figure 4.18 SEM images of transferred devices onto SiMR.(a) SEM image of 50 μm mesa at tilt angle (b) SEM image of 70 μm mesa at tilt angle (c) and (d) Top view of microscope images of 70 μm mesa.

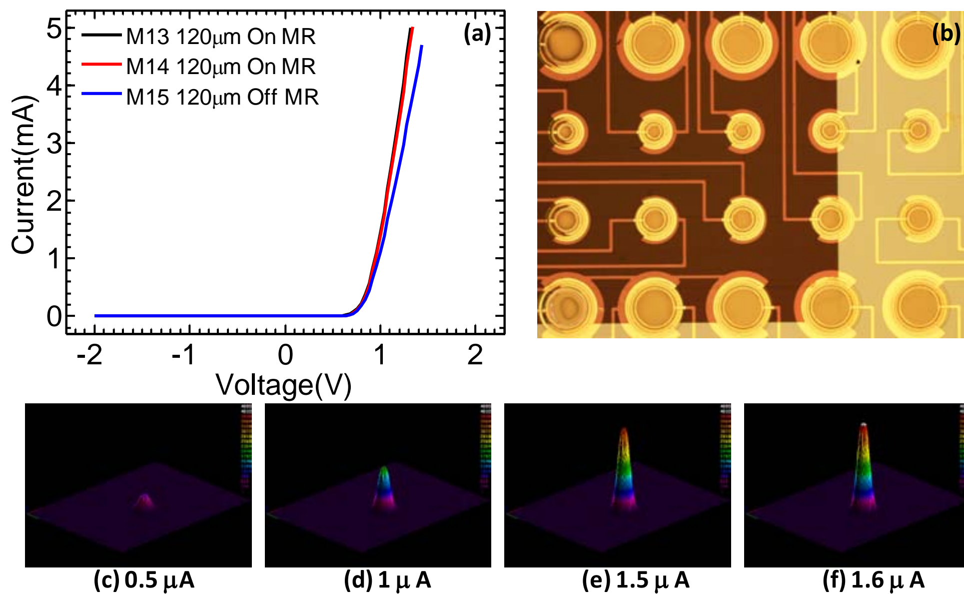

Figure 4.19 (a) Comparison of I-V characteristics of devices between on MR and off MR (b) Microscope image of devices successfully transferred onto bottom mirror (c) (d) (e), and (f) Far-field images of 50 μm mesa device with different biased currents varying from 0.5 μA to 1.6μA.

Fig 4.17 show SEM images of transferred devices on SiO_2/SOI substrate using resist pattern to hold mesas during bonding process. By using the same method, electrically pumped devices with different mesa sizes of 50 μm and 70 μm are successfully transferred onto prepared bottom mirror as shown in Fig. 4.18(a) and (b) respectively. A thin layer of SiO_2 is deposited on top of n-ring so that p and n contacts are isolated from each other. Fig. 4.18(c) and (d) show microscope images of devices with the same mesa size of 70 μm transferred onto bottom mirror. The I-V curves of the same mesa size comparing between on MR and off MR as shown in Fig 4.19(a). A microscope image of transferred devices onto bottom mirror (darker area) and outside bottom mirror (lighter area) is depicted in Fig. 4.19(b). Far-field images at different bias current are illustrated in Fig. 4.19(c) to (f) as you can see that the intensity already saturated at very small input bias current of 1.6 μA and most devices are similar in terms of performances because of high quality transfer process.

4.6 Summary

We demonstrated an ultra-thin DBR-free MR-VCSEL on Si, based on transfer printed InGaAsP QW cavities sandwiched in between two single layer Si-MRs. The complete lasing cavity was built using low temperature processes on CMOS compatible Si substrates. Different from the conventional DBR-based VCSEL that may be bonded/transferred onto Si substrates after complete laser fabrication, the multi-layer membrane transfer printing process offers a very simple and agile approach to large scale photonic integration. Also different from the direct wafer-fusing/bonding approaches, the transfer printed multi-layer membranes can have different types of interface control and engineering measures, allowing better thermal mismatch tolerance between dissimilar materials. With this demonstrated approach to lasers on Si, different material systems can be further integrated together, with unlocked constraints in lattice mismatches and thermal mismatches, opening doors towards a wide range of applications in optoelectronic and photonic devices, and integrated systems thereof. The ultra-compact high finesse Fabry-Perot cavity, based on two parallel single layers of Si-MRs, offers a simple

solution to VCSELs on Si and on any other substrates. The approach also renders wavelength scalability and tunability. Electrical injection is also feasible with the incorporation of the intra-cavity contacts. Notably, the MR-VCSEL devices can be further integrated with different functional photonic NM layers for modulation, beam focusing and routing, and 3D photonic/electronic integration. Lastly, the MR-VCSEL devices can be built and transferred onto any other rigid glass or flexible plastic substrates, making them even more attractive for applications in consumer electronics and bio-photonics, etc.

CHAPTER 5

CONCLUDING REMARKS AND FUTURE RESEARCH DIRECTIONS

5.1 Concluding Remarks

In this thesis, various kinds of photonic and electronic devices have been experimentally demonstrated. The membrane reflectors based on guided mode resonance (GMR) have been designed, fabricated, and characterized. Different designs of membrane reflectors on an SOI substrate can be selectively controlled center of reflection spectral band to the target wavelength. The measured and simulated results of devices fabricated on an SOI substrate are in very good agreement ,and the measured reflections of devices are very closed to 100% over 100~220 nm in the desired infrared wavelengths. Moreover, the resonant control reflections can be realized by depositing a thin layer of SiO_2 on top surface of the devices and all measured results agreed very well with calculated results for this post-process [43]. Also red-shift of reflection spectra were demonstrated with a tuning range of 50 nm and 90 nm for the center wavelength of 1550 nm for relatively small and large air hole radius, respectively. With carefully controlled thickness of low refractive index SiO_2 on top surface of membrane reflectors, we can tailor the reflection band of devices to our need, or control the reflection band of those devices in a typical useful ways. To further characterized a membrane reflector on a foreign substrate, the transfer printing with a PDMS stamp was used to transfer a top membrane layer onto a glass substrate or any preferred substrate after it completely released from the silicon handling substrate by selectively wet etching underlying sacrificial buried oxide layer [5, 53, 70]. The measured results agreed well with the calculated ones. The effects of the degradation of reflection spectra is discernible especially at the shorter wavelength band, mostly owing to a non-uniformity of fabricated air hole pattern associated with the very large area of photonic crystal structure on an SOI substrate. The polarization properties of broadband

membrane reflectors on glass substrate were optically characterized by using linear polarizer to control the polarization angle of incident light. Under normal incident both TE and TM polarized light, the simulated and measured reflection spectra overlap with each other as expect owing to the symmetry of the square lattice of dielectric structure. The spectral blue-shift of reflection can be clearly noticed after the membrane reflector was transferred onto the glass substrate. By comparing the effective refractive index of the SOI substrate to only the new glass substrate, the effects of spectral blue-shift in the transferred membrane reflector can be apparently understood unlike the case of spectral red-shift. Nevertheless, the reflection band and peak of the reflector do not degrade after being transferred onto the glass substrate. This shown the uniform, high quality of transfer printing technique for large area transferred patterned NMs. The capability and compatibility of this approach with semiconductor and other micro/nanometer scale structures could offer the easy ways to fabricate the devices in photonics, electronics, and other areas of interest.

The crystalline InP nanomembrane LED arrays have been fabricated on InP substrate and successfully transferred onto flexible PET substrate based on low temperature transfer and stacking processes. High performance flexible InP LED arrays were successfully achieved. The devices were optically and electrically characterized, and investigated typical far-field intensity distributions of the devices by beam profiler. The flexible devices were both optically and electrically characterized to compare the performance during substrate has been bended and flat and it clearly shown that the high performance devices worked very well even though they were at a very small radius of bending. The flexible InP LED arrays perform well although the bending radius is smaller than 13.0 mm.

The ultra-compact DBR-free membrane reflector vertical cavity surface emitting lasers were successfully fabricated on Si substrate, for the first time based on transfer printing technology. The active region III-V materials were sandwiched in between top and bottom single silicon crystalline membrane reflectors to form the novel devices. By getting rid of DBRs,

making the devices very compact only the total thickness of 1.6 μm resonant cavity. The threshold pumped power is just about 8 mW, or 0.32 kW/cm^2. The measured spectral linewidths reduce from 30 nm below threshold to 0.6 - 0.8 nm above threshold at low temperature measurement. For the room temperature measurement, the measured spectral linewidths reduce from > 100 nm below threshold to ~4 nm above threshold at wavelength of 1545 nm unfortunately, the linewidth a little bit large due to the relatively low reflection of top membrane reflector at this wavelength.

5.2 Future Research Directions

5.2.1 Wafer-Scale Integration of Inorganic LEDs on Flexible Substrates

The transfer printing technology can be applied to a large wafer-scale integration of visible or infrared LEDs on flexible substrate. To satisfy the commercial market, hopefully, we can develop the process for making the flexible monitor for flexible cell phone screens, flexible television monitors, and thin flexible electronic books.

5.2.2 Wafer-Scale Integration of MR-VCSELs on Flexible Substrates

While silicon is an attractive integration platform due to its capabilities in both electronics and photonics, the indirect band gap of silicon precludes its use for efficient optical emission. One possible approach to enable high performance optoelectronics on low-cost silicon platform is to heterogeneously integrate III-V photonics with silicon to include high efficient III-V optical emitters and other photonic devices with the silicon electronic and photonic platform. By integrating III-V materials high efficient light sources with Si platform which we have been successfully demonstrated, the large wafer-scale effective heterogeneous integration can be obtained by transfer printing technology to provide the high performance lasers embedded in Si chip. These devices will support the upcoming optical communication systems needed a very high capacity bandwidth and very high speed.

5.2.3 Electrically Pumped MR-VCSELs on Flexible Substrates

The main purpose of MR- VCSELs is to achieve high efficiency electrically pumped MR-VCSELs with the smallest cavity such that it can be integrated into Si chip plus on flexible substrate that could be used for medical applications in the near future. To improve the efficiency of electrically pumped MR-VCSELs, diamond can be deposited directly onto bottom mirror instead of SiO_2 which has considerably low thermal conductivity such that heat dissipation inside gain medium can be reduced significantly during current injection.

APPENDIX A

ABBREVIATION LIST

2D PCS	Two-dimensional photonic crystal slab
BBRs	Broadband reflectors
BOX	Buried oxide layer
CMOS	Complementary metal–oxide–semiconductor
DBRs	Distributed Bragg reflectors
EBL	Electron beam lithography
EL	Electroluminescence
FAMT	Frame-assisted membrane transfer
FDTD	Finite-difference time-domain
GMR	Guided mode resonance
HCG	High-contrast grating
LED	Light emitting diode
LT	Low temperature
MOCVD	Metal organic chemical vapor deposition
MRs	Membrane reflectors
MR-VCSELs	Membrane reflector vertical cavity surface emitting lasers
NIR	Near infrared
NMs	Nanomembranes
OSA	Optical spectrum analyzer
PBC	Periodic boundary condition
PBG	Photonic band gap
PCS	Photonic crystal slab
PDMS	Polydimethylsiloxane
PECVD	Plasma-enhanced chemical vapor deposition
PET	Polyethylene terephthalate
PC	Photonic crystals
PCM	Photonic crystal mirror
PICs	Photonic integrated circuits
PL	Photoluminescence
PML	Perfectly matched layers
PSO	Particle swarm optimization
Q	Quality factor
QW	Quantum well
RCWA	Rigorous coupled-wave analysis
RIE	Reactive ion etching

RT	Room temperature
SEM	Scanning electron micrograph
Si-MR	Silicon membrane reflector
SiNM	Silicon nanomembrane
SOI	Silicon-on-insulator
SWG	Sub-wavelength grating
TCE	Trichloroethylene
VCSELs	Vertical cavity surface emitting lasers

APPENDIX B

RELATED PUBLICATIONS

Journal papers

1 Q. Zexuan, Y. Hongjun, S. Chuwongin, Z. Deyin, M. Zhenqiang, and Z. Weidong, "Design of Fano Broadband Reflectors on SOI," Photonics Technology Letters, IEEE, vol. 22, pp. 1108-1110, 2010.

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BIOGRAPHICAL INFORMATION

Santhad Chuwongin was born in Chainat, Thailand, in 1972. He received his B.Eng (1995) in telecommunication engineering from King Mongkut's Institute of Technology Ladkrabang (KMITL), Bangkok, Thailand, and received his M.Sc. and PhD degree both in electrical engineering from the University of Texas at Arlington, in 2009 and 2012 respectively. His research focused on design, fabrication and characterization of Silicon-based membrane reflector vertical cavity surface emitting lasers (MR-VCSELs) both optically pumped and electrically pumped MR-VCSELs, III-V materials flexible crystalline LED arrays, and Silicon-based nanomembrane reflectors on SOI and on foreign substrates by applying transfer printing technique.