INVESTIGATION OF DEGRADATION IN ADVANCED

ANALOG MOS TECHNOLOGIES

by

MD. IQBAL MAHMUD

Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

THE UNIVERSITY OF TEXAS AT ARLINGTON

December 2013

Acknowledgements

December 9, 2013

Abstract

INVESTIGATION OF DEGRADATION IN ADVANCED

ANALOG MOS TECHNOLOGIES

Md. Iqbal Mahmud, PhD

The University of Texas at Arlington, 2013

Supervising Professor: Zeynep Çelik-Butler

The focus of this work is to study the noise and degradation in advanced high and low voltage analog Metal Oxide Semiconductor Field Effect Transistors (MOSFET). Medium and high voltage transistors, especially lateral double diffused MOS (LDMOS) FETs are known as the workhorse for present day RF and analog mixed signal smart power applications. In presence of multiple in-plane Si-SiO$_2$ interfaces in asymmetric LDMOS devices, additional defects are created in those interfaces. The trapping-detrapping of charge carriers by these traps lead to increased low frequency noise (LFN) degradation in LDMOS compared to CMOS transistors. Hence, LFN sets a performance limit and increases the reliability concern in LDMOS devices. The majority of applications of LDMOS devices are in high frequency analog circuits and equipment, for example, in cellular communications, whereas *1/f* noise is generally known to be important for frequencies up to 10 kHz. However, when the spectrum is up-converted to higher frequencies, noise gets amplified as well due to different nonlinearities in the system. This in effect, increases the phase noise in communication system and other reliability concerns during device operation. This can result in significant performance degradation of the system itself at the operational frequencies. This is why the study of *1/f* noise degradation in medium and high voltage LDMOS is vital from the industry point of view.

iv

On the lower voltage side, analog submicron transistors are extensively utilized for obtaining high gain and bandwidth, while consuming low on-state power in analog to digital (and vice-versa) interfaces, in communication systems and in industrial electronics. Continuous downscaling of advanced submicron area low voltage analog MOSFETs requires rigorous in-depth study of the gate-oxide reliability. As compared to their high-voltage counterparts, these smaller devices have the oxide thickness of a few nanometers. This makes them vulnerable to individual defects in the Si-SiO$_2$ interfaces more severely than the high-voltage devices. Hence, it is necessary to identify, quantify, individually characterize and accurately model electrically active defects (charge trapping and scattering centers) in scaled analog and mixed signal (AMS) devices. In this regard, random telegraph signal (RTS) noise measurement to characterize single charge carrier switching events in time domain, is of significant importance in present-day submicron device technologies, because of its versatility and inherent non-destructiveness to devices, as far as the device degradation is concerned.

For LDMOS, the DC stress induced degradation characteristics of differently processed devices are studied in this work along with the noise performance. It is illustrated in this work that modeling the DC degradation alone cannot fully explain the physical mechanisms for LDMOS degradation. Hence, *1/f* noise was utilized as a non-destructive characterization tool to quantitatively evaluate the device reliability and degradation at time-zero and after they were subjected to stress-induced degradation. Correlation has been established between low frequency noise and DC stress-induced degradation. From that, a simple but well-defined approach has been delineated to separate the individual resistance and noise components in different regions of these devices. The effect of extended drain drift region scaling on *1/f* noise performance is

studied for different foundry-fabricated devices. An early lifetime prediction method for LDMOS is also reported here using *1/f* noise measurements.

This work represents the first ever physics-based *1/f* noise model for LDMOS devices, and demonstrates that the developed model can correctly predict the experimentally observed noise behavior in the linear region of operation in fresh devices as well as in stressed devices. The model is based upon the correlated carrier number and mobility fluctuation theory known as the Unified *1/f* Noise Model, but has been modified to account for the fluctuations in the extended drain as well as the channel. Unlike the Unified *1/f* Noise Model, non-uniform trap distribution has been taken into account with respect to the position in the gate oxide and in the band-gap energy.

In case of low voltage analog CMOS, we have demonstrated the RTS noise measurement and analysis technique to isolate each individual physical defect, and to characterize the trap properties both quantitatively and qualitatively. Multiple level RTS have been observed in submicron NMOS transistors at room temperature. From our analysis, we could ascertain the presence of two active traps, which are found to be responsible for four level RTS generation. Two different types of active traps- donor and acceptor, responsible for RTS generation, have been identified simultaneously for the first time in the same NMOS transistors at room temperature. A numerical computation method has been developed to separate fluctuations due to each trap, and to calculate the trap properties such as the mean capture and emission times, trap energy, capture cross-section and the distance into the oxide from the interface.

Table of Contents

List of Illustrations

xvii

List of Tables

LIST OF SYMBOLS

C_{gc} gate to channel capacitance of MOSFET (Fcm^{-2})

C_{ox} gate oxide capacitance of MOSFET (Fcm^{-2})

E any energy level (eV)

E_C energy at the conduction band edge (eV)

E_{fov} quasi Fermi energy for electron in the gate-overlap region (eV)

$E_{f\max}$ energy at the effective maximum spatial distribution of active traps (eV)

E_g bandgap energy (eV)

E_i intrinsic Fermi level energy (eV)

E_T trap energy level (eV)

E_F Fermi energy level for electron (eV)

E_V valence band edge (eV)

E_x electric field along the channel (Vcm^{-1})

ΔE_B barrier energy for capture by a trap (eV)

ΔE_{CT} trap binding energy (eV)

$E_{C_{ox}}$ oxide conduction band energy (eV)

f frequency (Hz)

f_t trap occupancy function

g_D conductance of the LDMOS channel ($A\,V^{-1}$)

$g_{D_{eff}}$ LDMOS effective device conductance ($A\,V^{-1}$)

g_m	transconductance (A V^{-1})
$g_{m\,\mathrm{max}}$	transconductance in the MOSFET linear operation region (A V^{-1})
h	Planck's constant (eV-s)
I_d	drain current (A)
I_{dlin}	drain current in the MOSFET linear operation region (A)
ΔI_d	drain current fluctuations (V)
I_g	gate current (A)
I_R	current in a DNWell resistor (A)
κ	dielectric constant
k_B	Boltzmann's constant (eV K^{-1})
L_c	MOSFET channel length (μm)
L_D	Debye length (cm)
L_{ov}	length of the gate oxide-overlap region (μm)
$L_{ED_{FO}}$	length of the field oxide region (μm)
n	inversion charge carrier concentration (cm^{-3})
N	charge carrier density in semiconductor device (cm^{-2})
N_c	inversion carrier charge density in the channel (cm^{-2})
$N_{it_{ov}}$	active interface trap density at the gate-overlap region Si-SiO$_2$ interface (cm^{-2})
N_{ov}	charge carrier density in accumulation in the gate-overlap region (cm^{-2})

N_{ot_c}	number of occupied traps per unit area in the gate oxide in the channel region (cm^{-2})
$N_{ot_{ov}}$	number of occupied traps per unit area in the gate-overlap region oxide (cm^{-2})
N_{t_c}	oxide trap density in the channel (cm^{-3} eV^{-1})
$N_{t_{ov}}$	oxide trap density in the gate-overlap region (cm^{-3} eV^{-1})
$N_{t0_{ov}}$	mid band-gap trap density at the interface (z=0) (cm^{-3}eV^{-1})
$N(x)$	inversion layer charge carrier density at distance x from the source (cm^{-2})
ΔN_c	charge carrier density in the channel within $W\Delta x_c$ area (cm^{-2})
ΔN_{ov}	charge carrier density in the gate-overlap region within $W\Delta x_{ov}$ area (cm^{-2})
ΔN_{ot_c}	number of occupied traps in the channel in $W\Delta x_c$ area
$\Delta N_{ot_{ov}}$	number of occupied traps in the gate oxide in $W\Delta x_{ov}$ area
q	elementary electronic charge (C)
Q_{ot_c}	insulator trap charge per unit area in the channel (Ccm^{-2})
R_{ch}	LDMOS channel resistance (Ω)
R_{GO}	resistance of the standalone DNWell resistor having a gate oxide (Ω)
R_{FO}	resistance of the standalone DNWell resistor having a field oxide (Ω)
R_{on}	on-resistance of LDMOS (Ω)
$R_{ED_{GO}}$	bulk resistance in the extended drain under the gate oxide (Ω)

$R_{ED_{FO}}$	bulk resistance in the extended drain under the field oxide (Ω)
R_{over}	bulk resistance in the extended drain under the gate oxide (Ω)
R_{sp}	spreading resistance (Ω)
S_s	subthreshold slope (V^{-1})
S	Huang-Rhys parameter
S_I	drain current noise power spectral density ($A^2\ Hz^{-1}$)
S_{I_d}	current noise power spectral density generated at the Si-SiO$_2$ interface in the channel and in the gate-overlap region ($A^2\ Hz^{-1}$)
$S_{\Delta I_{d_c}}(x,f)$	power spectral density of the local current fluctuations in the channel ($A^2\ Hz^{-1}$)
$S_{\Delta I_{d_{ov}}}(x,f)$	power spectral density of the local current fluctuations in the gate oxide-overlap ($A^2\ Hz^{-1}$)
$S_{\Delta I_{d_{FO}}}(x,f)$	power spectral density of the local current fluctuations in the field oxide region ($A^2\ Hz^{-1}$)
$S_{\Delta N_{t_c}}(x,f)$	power spectral density of the mean square fluctuations in the trapped charge carriers over the area $W\Delta x_c$ (Hz^{-1})
$S_{\Delta N_{t_{ov}}}(x,f)$	power spectral density of the fluctuations in the number of the occupied traps over the area $W\Delta x_o$ in the gate-overlap region (Hz^{-1})
$S_{R_{ED_{GO}}}$	bulk resistance fluctuation under the gate oxide in the extended drain ($\Omega^2 Hz^{-1}$)

$S_{R_{ED_{FO}}}$	bulk resistance fluctuation under the field oxide in the extended drain $(\Omega^2 Hz^{-1})$
$S_{R_{FO}}$	bulk resistance fluctuation in the standalone DNWell resistor under the field oxide $(\Omega^2 Hz^{-1})$
$S_{R_{GO}}$	bulk resistance fluctuation in the standalone DNWell resistor under the gate oxide $(\Omega^2 Hz^{-1})$
S_V	drain voltage noise power spectral density $(V^2\ Hz^{-1})$
S_{V_c}	voltage noise power spectral density from the channel $(V^2\ Hz^{-1})$
$S_{V_{fb}}$	noise power spectral density for flat-band voltage fluctuations $(V^2\ Hz^{-1})$
$S_{V_{R_{ED_{FO}}}}$	voltage noise power spectral density from the extended drain under the field oxide region $(V^2\ Hz^{-1})$
$S_{V_{R_{ED_{GO}}}}$	voltage noise power spectral density from the extended drain under the gate oxide region $(V^2\ Hz^{-1})$
t_{inv}	inversion layer thickness (nm)
T	temperature (K)
T_{ox}	thickness of gate oxide (nm)
V_{ch}	voltage drop across the channel (V)
V_d	drain to source voltage (V)
ΔV_d	magnitude of the drain voltage fluctuation (V)
V_{FB}	flat-band voltage (V)
V_g	gate to source voltage (V)

V_t	threshold voltage (V)
ΔV_t	threshold voltage fluctuation (V)
v_{th}	average thermal velocity for channel carriers (cms^{-1})
W	MOSFET device width (µm)
x_c	distance from the source toward the drain in the channel (cm)
x_{ov}	distance from the channel/drain junction in the gate-overlap region (cm)
$x_{ED_{FO}}$	distance from the bird's beak in the extended drain toward the drain contact (cm)
Δx_c	infinitesimal distance from the source toward the drain in the channel (cm)
Δx_{ov}	infinitesimal distance from the channel/drain junction in the gate-overlap region (cm)
$\Delta x_{ED_{FO}}$	infinitesimal distance from the bird's beak in the extended drain toward the drain contact (cm)
x	distance along the channel (cm)
x_T	trap distance into the gate oxide from the Si-SiO$_2$ interface (nm)
y	distance in the width dimension (cm)
z	distance into the gate dielectric (cm)
z_{max}	maximum spatial distribution of the active traps (nm)
α_H	Hooge's coefficient
α_c	screened Coulomb scattering coefficient for the channel (Vs)

α_{ov}	screened Coulomb scattering coefficient for the gate-overlap region (Vs)
δ	frequency exponent as in $1/f^{\delta}$
ϕ_0	electron affinity difference between Si and SiO_2 (eV)
γ	carrier tunneling coefficient in the gate dielectric (cm^{-1})
ε_0	permittivity of free space (Fcm^{-1})
ε_{Si}	permittivity of Si (Fcm^{-1})
η_{ov}	fitting parameter that determines dielectric trap density distribution as a function of z (cm^{-1})
λ_{ov}	fitting parameter that defines the effect of dielectric band-bending on the trap density that the tunneling electron encounters in the dielectric layer (eV^{-1})
ξ_{ov}	fitting parameter for energy dependence of traps (eV^{-1})
μ_c	effective channel carrier mobility ($cm^2V^{-1}s^{-1}$)
$\mu_{c0_{ov}}$	mobility fluctuation fitting parameter for the gate-overlap region ($cmV^{-1}s^{-1}$)
μ_{eff}	effective carrier mobility ($cm^2V^{-1}s^{-1}$)
μ_{latt}	mobility due to lattice scattering ($cm^2V^{-1}s^{-1}$)
μ_{others}	mobility due to other scattering phenomena ($cm^2V^{-1}s^{-1}$)
μ_{ov}	effective carrier mobility in the gate-overlap region ($cm^2V^{-1}s^{-1}$)
μ_{ox}	mobility due to oxide charge scattering ($cm^2V^{-1}s^{-1}$)
σ	capture cross-section (cm^2)
σ_0	capture cross-section pre-factor (cm^2)

τ	trapping time constant in the gate dielectric (s)
$\overline{\tau}_c$	mean capture time (s)
$\overline{\tau}_e$	mean emission time (s)
τ_o	trapping time constant at the Si-SiO$_2$ interface (s)
ψ	Si surface potential at any position in the channel (V)
ψ_s	Si surface potential at the SiO$_2$ interface (V)
ω	angular frequency (radians s^{-1})

Chapter 1

Introduction

1.1 Preface and Motivation

This dissertation consists of two distinct sections. The first section is on the investigation of degradation in medium and high voltage lateral-double-diffused metal oxide semiconductor field-effect transistors (LDMOSFET) or the LDMOS. The second section discusses individual characterization of semiconductor/gate dielectric defects using multilevel random telegraph signal (RTS) noise in analog MOS transistors.

Carrier fluctuation leading to low frequency noise (LFN) degradation with electrical stressing can be a major reliability concern in integrated power devices [1], affecting the Si/SiO_2 interface and gate oxide reliability, and possibly impacting the device lifetime. In analog and mixed signal (AMS) applications, low frequency noise, also known as *1/f* noise or flicker noise, serves as a figure-of-merit for the reliability as it often sets the sensitivity limit for the transistor or even for the circuit itself. It will be evident in this dissertation that LFN measurement is a powerful diagnostic tool because of its versatility, i.e can be applied to devices with smaller (submicron) to long channel dimensions or even to advanced high power devices, e.g. LDMOS. Although a lot of research is being carried out on the LDMOS breakdown voltage improvement, hot carrier degradation, safe operating area (SOA) and on-resistance optimization [2, 3], there had been no comprehensive study on LDMOS low frequency noise characteristics.

In this work, we investigated the LFN behavior of different voltage-rated reduced surface field (RESURF) LDMOS devices. We separated the individual resistance and *1/f* noise components in different regions in this asymmetric device from the study of DC stress induced degradation. Although *1/f* noise theory is well established and understood for conventional enhancement MOSFETs, there has been no such model proposed for

the *1/f* noise in LDMOS transistors. Hence, a physics-based LDMOS noise model could be an essential addendum for analog integrated smart power circuit design. Such a model should accurately predict the LFN behavior for the devices before stress as well as after stress. Moreover, the model has to be generalized, i.e. applicable for LDMOS with different physical structure and design layout. This dissertation reports on our developed novel, physics-based *1/f* noise model, which incorporates the trapping–detrapping of carriers in the proximity of Si/SiO_2 interfaces of the channel and the extended drain to account for the charge carrier number and mobility fluctuations. Stressing time dependence of the measured noise and individual noise components is described. The accuracy of the model is verified with respect to stressing time. Finally, we show that our model can predict the oxide trap density of LDMOS transistors and stress time dependence of the active traps.

Second part of this dissertation discusses methodology towards a measurement-driven RTS noise characterization to explore individual charge carrier capture/emission at the semiconductor/gate dielectric interface and in the dielectric that incorporates the effects of multiple traps/defects and their interaction. The goal/objective is to (1) devise a methodology for individually identifying and characterizing electrically active defects (traps), specifically carrier trapping and scattering states, in MOS structures; (2) extract each trap location, capture and emission time constants, capture cross-section, screened scattering coefficient and type (acceptor/donor); (3) develop analysis strategy for the above properties associated with the traps; and (4) find the physical origin of creation and activation of these defects as charge carrier traps. We obtained a four level RTS as a function of gate bias in different analog NMOS devices and developed a methodology to extract the number of traps along with the required trap properties.

1.2 Degradation in Scaled Down Analog MOSFETs

Amidst the quest for alternative technology, device and materials, semiconductor industry is still primarily dependent on conventional MOSFET performance and dimension scaling to enhance integrated circuit performance at a reduced operation cost. Since Moore's law was introduced in 1965, semiconductor industry is continuously increasing the transistor density by reducing the device dimensions (typically the gate length reduction). From the decade of 1960's, the gate length has been shrunk from hundreds of micrometers to less than 45 nm in modern day technology [4]. However, MOS technology was immediately associated with the limitations of short channel effects, right from the beginning of scaling [5]. Since then, device degradation has been observed in the form of, for example, increase in the subthreshold conduction, increase in source-drain resistance leading to decreased mobility, exponential increase in gate leakage current (tunneling) and off-state power consumption. To overcome this predicament, several alternative materials like high-κ gate stack technology, use of III-V materials instead of Si as the substrate etc. have been explored to improve the device performance. However, amongst all of these alternatives, Si-SiO$_2$ substrate-dielectric technology has still sustained throughout the decades due to lower manufacturing cost and excellent device performance. Moreover, scaling in Si based technology is still possible by implementing novel architectures and by having proper reliability studies, especially in analog technologies. Reliability and degradation study is therefore, is of utmost importance in the arena of integrated scaled-down devices.

1.2.1 Scalability and Applications of High Voltage and Low Voltage Analog MOSFETs

In high power analog operations, for example in RF amplifiers (used in wireless radio base stations, aerospace or in defense broadcast), LDMOS is the most prevailing device technology, extensively utilized for frequencies ranging approximately from 10

MHz to 3.8 GHz [6]. From the industry point of view, LDMOS has significant advantages over Si bipolar transistors and devices made of alternative material (e.g. GaN) based high power amplifiers because of ruggedness, outstanding efficiency and high gain. On the other hand, necessity of low voltage analog transistors is realized in innumerable real life applications because of their continuous time operation and gain. For example, any digital to analog (D/A) or analog to digital (A/D) conversion to interface with outside world is fundamentally analog. The superiority of analog devices is evident in signal processing compared to their digital device counterpart, because of lower on-chip power consumption and the gain [7]. Hence, low voltage analog MOSFETs are incorporated with the integrated CMOS processes in semiconductor industries. It should be apparent that analog design and scalability is sometimes more challenging and difficult compared to well-defined lithography-driven digital processes, because of numerous complex fabrication processes as well as introduction of several alternate substrate materials involved in analog process to achieve the desired device performance. In addition to that, scaling of digital transistor significantly impacts analog device performance and analog device scalability as well in the long run [8]. This is because, with the same expected device performance constraint from analog devices after scaling, when the power supply voltage is scaled down for digital applications, threshold voltage for the analog devices does not scale down complementarily. A possible reason is the DIBL (drain induced barrier leakage) effect, which impacts directly on the gain and useful bandwidth of the output signal. Hence, it is well known in industry that "if you can do it in digital - don't do analog" [9].

1.2.2   Degradation Study Techniques in Analog Transistors

So far we have discussed the scalability issues with high and low voltage analog MOSFETs. Due to the operating conditions of devices and ICs, devices are stressed or wear out over time, which results in various short term and long term performance and reliability problems. Some of the degradation effects are irreversible like dielectric breakdown, while some are recoverable (to some extent) in the off-state. Degradation due to dielectric breakdown can be instantaneous and catastrophic like electrostatic discharge (ESD) failure or can be due to trap build up in the oxide bulk or at the Si-SiO$_2$ interface over time, known as time dependent dielectric breakdown (TDDB). The defects cause gate leakage current through the dielectric, which either results in threshold voltage shift or in the permanent device failure because of dielectric breakdown. It should be apparent that the study of TDDB or ESD stress in MOSFETs is for most part, a destructive measurement approach. Charge pumping [10] is a well-known degradation analysis technique, by which spatial distribution of interface traps can be investigated. However, it entails prior knowledge of MOSFET doping and potential profiles, which may not be always accessible. Moreover, this experimental technique is usually unable to probe the damaged region deeper into the oxide and remains useful only in identifying shallow traps (close to the Si-oxide interface) in the middle of Si band gap [11]. This technique is not suitable in SOI devices, where there is usually no available contact from the bulk [12]. Since the device size will continue to shrink, the charge pumping current, which is proportional to gate area, will be difficult to measure. Negative and positive bias temperature instability (NBTI and PBTI) are other important degradation metrics for PMOS and NMOS, respectively in VLSI circuits. The electrical PBTI or NBTI stress (for example in V_g <0 in NBTI stress) on the transistor, generates traps at the Si−SiO$_2$ interface, which increases V_t, degrades channel mobility and increases parasitic

5

capacitances. However, the shortcoming of NBTI (or PBTI to some extent) is again not being a fully non-destructive approach, since the damage due to interface traps can sometimes be partially alleviated when the stress is reduced/ released [13].

Hot carrier injection (HCI), is another severe degradation mechanism that causes defect generation in the dielectric and also at the Si−SiO$_2$ interface near the drain side due to carrier heating resulting into impact ionization. Unlike NBTI/PBTI stress, HCI causes faster degradation in the form of V_t shift, impedes high frequency switching and reduces the device performance drastically and more importantly, the recovery in HCI is sometimes impossible. Therefore, an alternative technique is essential to investigate the analog device degradation in a non-destructive approach.

1.3   Noise in Semiconductor Devices

Electronic 'noise' in solid state devices refers to the random voltage, current or resistance fluctuations. This is a stochastic process where the metric or characteristic under observation changes randomly over time. An example is the low frequency noise, whose mean value and the standard deviation are constant when calculated at different time intervals (hence LFN is a stochastic 'stationary' phenomena). Generally, it occurs due to the presence of localized defects in microstructures (whether it is a MOSFET, BJT or diode etc.), regardless of the device dimensions, albeit electrical noise does not necessitate the presence of physical defects in a solid state device. In the following subsections, four most significant noise sources in electronic devices will be addressed. Among them, *1/f* noise and RTS noise are the topics of discussion in this dissertation.

1.3.1 Dominant Low Frequency Noise Sources: RTS Noise, G-R Noise and 1/f Noise

RTS noise in solid state devices are observed in small area transistors when the charge transport is governed by the charging and discharging of defects resulting in discrete random voltage or current fluctuations with time. This is sometimes referred to as popcorn or burst noise (a term used before 1980's). If only an active trap is present around the Fermi level (within about $3k_BT$ to be precise), a simple two level RTS will evolve. This is mostly observed by authors in submicron MOSFETs at room temperature and at lower temperatures [14-16]. It is also likely to have several trapping centers to be active at the same time to generate multi-level RTS, which is the superposition of the random fluctuations from all of the traps. Systematic analysis of RTS can provide important information about the properties of each defect like trap type, physical location and capture cross-section. With RTS measurement, it is possible to identify both process-induced traps and those introduced after the device is stressed. RTS noise due to process-induced traps was first observed by Kandiah and Whiting in 1978 [17]. They are generated from the imperfections during device fabrication, and are therefore, dependent on the foundry processing. Hot carrier stress induced trap was reported to be more effective in trapping-detrapping compared to process induced traps by Fang *et al.* in 1991 [18]. With the aggressive downsizing of MOS technology, RTS noise is expected to dominate as a device design concern; not only for analog devices, but also in digital memory devices like Static Random Access Memory (SRAM), Ferroelectric RAM (FRAM) or Dynamic RAM (DRAM) devices. According to [4], at 22-nm SRAM technology node and beyond, RTS noise will be large enough to increase the variability of noise sources above the minimum supply voltage limitation of scaling. This might then make the future design margin or scaling probability to be negative for SRAM [4].

Generation-recombination (G-R) noise has distinct similarity to RTS noise as both of them show Lorentzian power spectral density (PSD) in frequency domain. In semiconductors, it originates due to random capture and emission of charge carriers from conduction or valence band to the defect state, analogous to RTS noise case. This G-R noise therefore, can be observed as a superposition of several RTS noise from one or more traps with identical time constants. In relatively large devices, RTS noise can be part of G-R noise, which would be indistinguishable from G-R noise and also *1/f* noise component will be observed at the same time in real time domain measurement [11]. Just like RTS noise, G-R noise is also bias and temperature sensitive [11]. The maximum G-R noise occurs for a defect center with energy at the Fermi level, resulting in equal capture and emission time constants, and the noise spectrum becomes [19]:

$$S_V(f) = 4\overline{\Delta N^2} \frac{\tau^2}{1+\left(2\pi f \tau\right)^2} \tag{1.1}$$

where N is the charge carrier density and τ is the characteristic time constant for the charges. This reveals that the G-R noise is constant at low frequencies and falls off after the corner frequency (*f*) at *1/f²* rate. There is also another noise source, known as *1/f²* noise, whose frequency exponent is close to 2 (in fact in the range of 1.8–2.2) and the physical mechanism for this type of noise is different than that for *1/f* noise [20]. An example is the electromigration in metal lines.

On the other hand, if the number of active traps is high, the superposition of the random telegraph signals (Lorentzian's) from individual defect states in the gate-oxide will result in *1/f* noise. This means that both *1/f* noise and RTS noise have the same physical origin in MOSFETs [15]. However, *1/f* noise is more universal i.e. can be observed in any metal, semimetal, BJT, diode or even in organic systems (of course, the physical origin

8

will be different in those systems). As the name suggests, *1/f* noise has a power spectral density of $1/f^\delta$ with δ is typically unity or ranges from 0.7-1.4. At low frequencies in relatively larger area devices, *1/f* noise has the most significant impact in generating device electrical noise. By means of LFN measurements, localized defects can be probed more sensitively than using other electrical characterization tools [12]. Nevertheless, RTS and *1/f* noise are the two most significant noise sources in transistors and hence, we will focus on these two topics in the subsequent parts of this dissertation.

1.3.2 Other Noise Sources: Thermal Noise and Shot Noise

In any electronic device, there are two sources of electrical noise: intrinsic noise and extrinsic noise [12]. Thermal noise and shot noise are the most important examples of intrinsic noise in electron devices. This kind of noise can be observed within a device even without the presence of defects or any traps [12]. On the other hand, extrinsic noise sources need the electrical conduction mechanism by the charge carriers to have communication with physical defects. Generation recombination noise, RTS and *1/f* noise are the examples of such noise sources, as discussed above.

Thermal noise

Thermal noise, also known as Johnson noise or Nyquist noise is present in any conducting material (metal or semiconductor) operating at above absolute zero temperature. This is generated due to thermal agitation of charge carriers, even without the presence of external bias. The power spectral density for thermal noise is defined as:

$$S_V(f) = 4k_B TR \tag{1.2}$$

where R is the device resistance. Thermal noise is generally independent of frequencies, except at extremely high frequencies, where a quantum correction factor restricts the thermal noise power from becoming theoretically infinite [11], and the thermal noise is then expressed as:

$$S_V(f) = 4\frac{hf}{e^{hf/k_BT}-1}R \qquad (1.3)$$

where h is the Planck's constant and f is the frequency. In the typical frequency range for noise measurement $hf \ll k_BT$, and we can simply consider Equation (1.2) to be applicable. Thermal noise therefore, appears as a plateau in the power spectrum.

Shot noise

Shot noise is described as the drift in the charge carriers upon application of electric field. It occurs randomly when the carriers cross a potential barrier, for example, in a p-n junction. Due to the discrete nature of the electronic charges, not all the charges flow continuously while crossing across the barrier and creates the shot noise. This is also an intrinsic noise, just like the thermal noise. In MOSFETs at high temperatures (above room temperature), leakage current in between the substrate and the channel generates shot noise and is reflected in the power spectral density (PSD) as:

$$S_I(f) = 2qI\beta \qquad (1.4)$$

where β is a shot noise suppression factor which is typically less than 1 [21]. Sometimes, high gate leakage currents in ultra-thin MOSFETs can also generate this

kind of noise [22]. Please note that power spectrum for both the thermal noise and shot noise are independent of frequency.

1.4 *1/f* noise in Medium and High Voltage LDMOS Transistors

1.4.1 Introduction to LDMOS

Integrated smart power and mixed signal applications entail medium and high voltage (20-200V) transistors to be compatible for integration with modern BiCMOS power technology (BPT) processes [2, 3, 23, 24]. With the ramping up of voltage capability requirement in automotive industry, RF and cellular communication, display devices and power electronics applications, lateral double diffused MOS transistors have become the workhorse because of their superior on-resistance and breakdown voltage trade-off. Unlike conventional CMOS, these devices are asymmetrical with respect to lateral geometry (Figure 1-1). For the typical analog smart power applications, (1-5 A and 20-200 V), there are primarily two distinct architectures that are employed: one is the interleaved Si/STI (shallow trench isolation) fingers with lateral field plates [25] and another one is the reduced surface field LDMOS devices [26].

These drain extended MOSFETs are asymmetric in nature. The thick oxide in the drift region decreases gate to drain capacitance for low resistance sinkers, making RESURF LDMOS transistors ideal for high speed switching over their STI based counterparts [27] in smart power technologies. The LDMOS devices contain an extended drain consisting of a medium doped resistive region under the gate oxide (overlap region), which works as "current funnel" transition between the channel and the drift region [28]; as well as a lateral drift region under a bird's beak shaped LOCOS (local oxidation of silicon) field oxide to reduce electric field crowding (Kirk effect) [29]. The channel is formed in the highly doped p-body region by the lateral diffusion difference

11

(out-diffusion) between the source and the N-Well. The gradual doping concentration gradient in the channel ensures improved conductivity for relatively longer channel lengths and protects from the punch-through effects [27]. The high carrier concentration in the source side determines the threshold voltage [30]. The extended drain with its bird's beak shaped FOX drift region is formed in an NWell epi-layer, which ensures double RESURF effect from both the p-body/NWell junction and the N+ buried layer/NWell junction to overcome the very high electric field near the drain junction [31]. This also prevents drain side degeneration due to hot carrier effects.
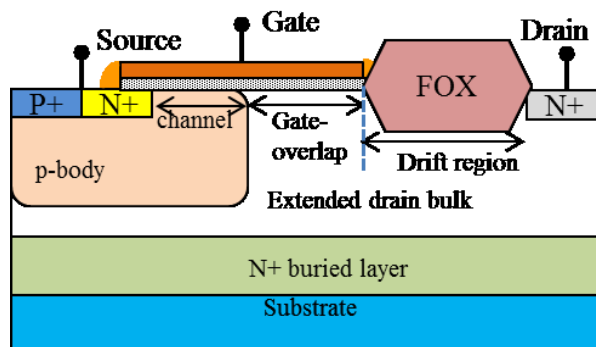
Figure 1-1 Cross-sectional schematic for an LDMOS showing the channel, gate oxide overlap region and the extended drain drift regions.

1.4.2   Sources of 1/f Noise in LDMOS

Although the LDMOS concept dates back some years, low frequency noise characteristics of these devices have attracted attention only recently, due to the booming of important analog applications as explained above. *1/f* noise can cause a severe impact in System-on-Chip (SOC) applications when the transistor is coupled with other devices or circuits through the substrate or in oscillators, gate drives and analog voltage converters [32]. In RESURF LDMOSs, current flows near the bulk Si-oxide

interfaces and therefore the devices are more susceptible to high current densities and strong electric fields, severe hot carrier injection, on-resistance degradation, fast interface trap generation [1, 3, 27, 33, 34], and carrier trapping-detrapping leading to considerable low frequency noise degradation. Due to large applied voltage, LDMOS devices are typically susceptible to high current densities [35]. When the carriers are exposed to additional dielectric/Si interfaces in the extended drain, this high density increases the drain current fluctuations through further carrier trapping-detrapping, leading to trap-induced interface and dielectric degradation. Therefore, these phenomena have to be investigated simultaneously with DC parameter degradation such as drain current (I_d) or on-resitance (R_{on}) [36]. The *1/f* noise characteristics in LDMOS differ significantly from conventional CMOS devices due to the additional fluctuations prevailing in the extended drain region. Since LDMOS contains an active channel in series with a drift region resistance and an extended drain, where accumulation of majority carriers take place (in the gate overlap region) [30], it has been found experimentally that LDMOS does not follow any conventional noise models which are originally developed for CMOS devices.

1.4.3   *1/f Noise Measurement as a Non-Destructive Degradation Analysis Technique*

Low frequency noise measurements are regarded as a nondestructive diagnostic tool that provides information about defect/trap density, location, trap energy, and interface quality [37, 38]. Conventional characterization techniques are mainly based on degradation tests under accelerated stress conditions. For a given number of devices, these tests provide adequate statistical information on the projected lifetime and different physical parameter degradation. However, in many cases, it is not possible to get sufficient evaluation of degradation processes and to predict the lifetime in early stages,

13

which could be important for the semiconductor industries. Accelerated stress sometimes results in device failure i.e. the device is already wasted [12].

The LFN measurement offers an alternative characterization tool to study the 'quality' of unstressed as well as stressed devices, for example as a probe for assessing the effects of hot-electron degradation or, radiation-induced damage on the microstructure [12]. A device with high levels of low frequency noise is not reliable as it is prone to defect formation. Therefore, LFN study can qualitatively assess a material under investigation. LFN measurement is not only useful in degradation study in MOSFETs but also in other microelectronic materials and devices as well for its sensitivity to localized defects and of course, since this is non-destructive to devices. It also requires no special procedures for sample preparation, except some device level packaging for measurement at low temperature if a cryostat is used as part of a cryogenic measurement system [14].

Recent studies on identification of degradation with stressing in LDMOS utilized relatively complex charge pumping and simulation-based techniques [34, 39, 40]. However, as the degradation of LDMOS is a function of bias voltages as well as the device process and layout parameters [34], the worst degradation condition and corresponding mechanism in each LDMOS device have to be investigated separately. Due to this, and partially due to the lack of a known universal degradation mechanism, no single nondestructive technique has emerged to date to assess the level of degradation in these devices. Our experimental results and analyses based on *1/f* noise measurements present a simple diagnostic methodology to identify the damage location in LDMOS induced due to DC voltage stressing. We showed that LFN characterization can give better insight about the damage in different regions of LDMOS [11], the effect of

different process technologies on device reliability, trap kinetics and also provides information about scattering. Details are provided in Chapter 4 in this dissertation.

1.5 RTS Noise in Low Voltage Analog Transistors

Aggressive downscaling of the gate dielectric thickness in MOSFET increases trap assisted tunneling through the oxide. This results in increased on-state power consumption, reduction in output signal to noise ratio and eventually, lower device reliability. Researchers have shown that the variability of RTS noise from device to device increases more drastically than Random Dopant Fluctuation (RDF)-induced variation in devices, as the technology scales below 22 nm [41]. Therefore, accurate RTS characterization is of utmost importance in present day low voltage analog MOSFETs. The Fourier transform of the time domain RTS theoretically should turn out to be a Lorentzian (plateau before the knee frequency and $1/f^2$ at high frequencies). However, as shown in Figure 1-2, the slope at high frequencies does not always exhibit $1/f^2$ dependence.

Unlike $1/f$ noise, which is continuous and has Gaussian (normal) distributed amplitudes in time domain according to central limit theorem for large number of random fluctuations [42], RTS noise shows discrete waveform of several magnitude levels (two levels or more). As will be discussed in later chapters, RTS noise can have tremendous impact in submicron analog device operation, particularly in low power designs, in presence of single and multiple active defects. A number of device properties can be extracted using RTS noise measurement quite accurately, and the fluctuations can be observed in real time domain instead of frequency domain. From RTS noise measurement we can individually scrutinize the traps which is not possible with ensemble averaging of frequency domain $1/f$ noise measurements.
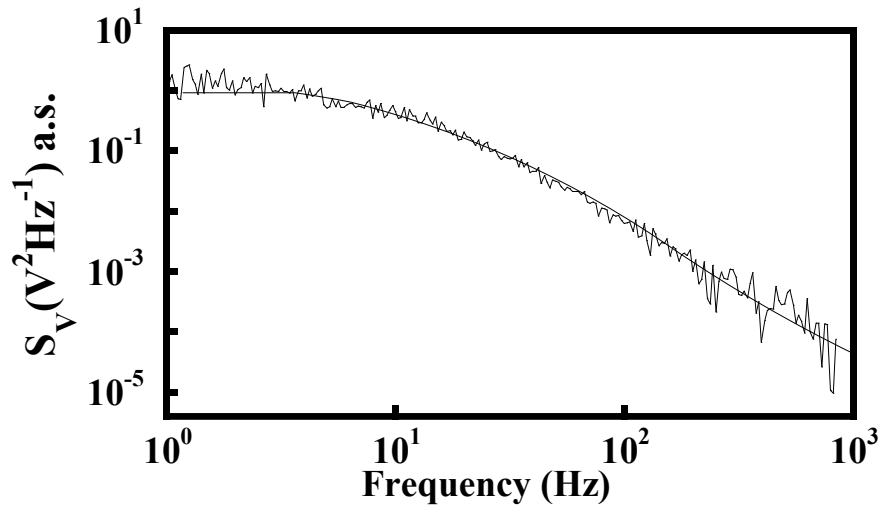
Figure 1-2 A typical noise spectra in frequency domain with a Lorentzian fitting. The y-axis is arbitrarily scaled to a higher magnitude than the actual device noise.

1.6   Summary

The significance of this dissertation lies in the fact that it is the first ever *1/f* noise modeling in analog medium and high voltage LDMOS transistors and also first evidence of presence of two different types of traps (acceptors and donors) in the same device by means of RTS noise measurement and analysis. The research on noise is of great interest to semiconductor industries in recent years. In this work, we dealt with reliability and degradation study in advanced analog MOSFET technologies, like that of RESURF and double RESURF technologies, using *1/f* noise measurements. The analysis provided in this work is generalized by combining the measurement results from different foundry-fabricated LDMOS device technologies. The technical compilations and the developed physics-based theoretical model are supported with a large amount of experimental results.

The dissertation is organized in the following way. This chapter provides the background, motivation and goals of this work and a general overview of degradation study techniques in analog devices. The importance of this research has been briefly highlighted for scaled MOS devices (both high and low voltage devices).

Chapter 2 provides the details of the experimental setup, device specifications and measurement procedures used for LDMOS characterization. We also focused on why we needed to do noise measurement in standalone DNWell resistors along with measurements in regular LDMOS transistors.

Chapter 3 comprises the results of DC stress induced degradation in LDMOS transistors. A technique to separate the contribution of the resistances as well as *1/f* noise from different regions of the devices has been elaborated. Finally, a method for predicting the lifetime of the LDMOS devices is discussed.

In Chapter 4, the step by step development procedure of the proposed LDMOS noise model is described in terms of correlated carrier number and mobility fluctuation model (also known as unified *1/f* noise model). We discussed the source of deviation from original unified noise model in LDMOS transistors and incorporated the effect of extended drain in noise behavior in the developed model. Then the dominant noise mechanism has been explored.

Chapter 5 is dedicated to the measurement and analysis procedure for multilevel RTS in submicron analog low voltage MOSFETs. A literature review is presented to discuss the necessity of multilevel RTS study in analog devices along with current analysis methods.

Chapter 6 discusses the measurement results in details for the multilevel RTS noise observed in the investigated devices. Then a detailed algorithm is proposed for extracting RTS amplitude, mean capture and emission times for each active oxide trap.

This is then followed by determination of several important trap properties: capture cross-section, energy and trap depth. A possible description for the physical mechanism for multilevel RTS generation is then presented, which is the carrier number and mobility fluctuation.

The summary of this work is presented in Chapter 7 with future research direction for both the degradation studies in medium and high voltage LDMOS, and RTS noise in low voltage CMOS for next generation technologies.

Chapter 2

Electrical Stressing and Noise Measurement

2.1 Introduction

In the previous chapter, a brief overview of the importance *1/f* noise measurement as a non-destructive probing technique in the study of LDMOS degradation was provided. To analyze the impact of the physical defects in the gate dielectric on MOS characteristics, precise measurement of noise is crucial. This chapter presents a heuristic step by step approach towards the different measurement methods including DC measurement, stressing at predefined intervals, and measurement of LFN in LDMOS as well as in standalone DNWell resistors, which laid the foundation towards the development of a new *1/f* noise model for LDMOS. Unless the measurement setup for LDMOS is designed carefully, electromagnetic interference and disturbances from DC battery itself or other electronic equipment or from the measurement environment will severely impact the extracted signals. The frequency domain noise is obtained by measuring the power spectral density of the very small signal (of the order of μV) using a dynamic signal analyzer, which is applicable to low voltage analog devices as well. However, some extra precautions have to be followed for time domain RTS measurements in analog devices which will be discussed in Chapter 5. Please note that, random fluctuations from a large number of traps are instantaneous, and the time average of them becomes zero if integrated over a long period. Instead, ensemble average of large number of fluctuations can be considered to have Gaussian (normal) distribution, according to central limit theorem, and mean squared values for the random fluctuations (also known as the power spectral density, PSD) are analyzed in frequency domain when a large number of traps are involved in the trapping-detrapping process. Hence, RTS noise was not possible to measure in our specific LDMOS devices; we

measured *1/f* noise instead.   In the process of developing the *1/f* noise model for LDMOS, a significantly large volume of statistical noise data was acquired to support the proposed noise model through careful experimentation.

2.2 Device Specifications

We studied different voltage-rated NLDMOS transistors at room temperature in their linear operation region. The channel lengths varied from 0.3 to 0.7 *µ*m with a channel width of 5–250 *µ*m. The gate overlap regions (Figure 1-1) were within the range of 0.5–1.5 *µ*m. The 20 V, 30 V, 40 V and 50 V LDMOS devices reported here were fabricated at Texas Instruments Inc., USA and Freescale Semiconductor Inc., USA. Although their physical dimensions, design and processing were different, all had a lightly doped extended drain formed in an NWell epitaxial layer over the Si substrate and the double-diffused channel formed in the highly doped p-body (PWell) to ensure enhanced on-resistance characteristics. The n-type buried layer (NBL) implant ensures the RESURF effect regarding the breakdown voltage driving the carriers away from the interface and therefore, thus improving the bias temperature stability (BTI) of lateral power devices [27]. During the measurements, source and p-body were connected together to form back-gate and to prevent the leakage current flow. The gate-bias controlled accumulation layer (gate overlap region) of the extended drain, in effect, is in parallel with the bulk resistance $R_{ED_{GO}}$ (extended drain bulk in Figure 1-1) and can be considered as distributed devices [33]. However, the two dimensional effect has been simplified to a single accumulation layer resistance fluctuation model, since it has been found that the majority carriers cause much higher degradation in the form of trapping-detrapping in the proximity of Si/SiO$_2$ interface in the gate overlap layer compared to the 'bias independent' bulk fluctuation. Eventually, the equivalent on-resistance model

20

reduces to a simple intrinsic MOSFET which controls the gain (p-body) with a bias dependent series resistor R_{over} responsible for RESURF to prevent thermal runaway, and another bias independent (due to the isolation by the thick field oxide from vertical field) drift region resistor $R_{ED_{FO}}$ that supports high applied voltages [29].

2.3 Noise Measurement Procedure

1/f noise in semiconductor devices and transistors are typically observed in the frequency range of 1 Hz to 1 MHz [11]. The typical measurement set up that we implemented in our laboratory is schematically represented in Figure 2-1. The noise measurement setup includes a low noise voltage preamplifier, a dynamic signal analyzer and a custom-designed DC biasing circuitry which is illustrated in Figure 2-2. For both the gate and drain terminals, we used 100 kΩ potentiometers. The series resistor R_S was properly adjusted based on the device type and voltage rating to make sure only the device noise gets amplified. LFN characteristics were obtained with the gate overdrive voltages ($V_g - V_t$), extending over subthreshold to linear region of operation at a constant drain voltage of 0.3 V. It is preferable to measure noise in a shielded area, for example, in a shielded probe station to minimize the interference from extraneous sources. Since the measured device noise has a small magnitude, it can easily get corrupted by the signals coming from the laboratory environment, for example, other circuits or equipment running in close proximity, electromagnetic signal from cell phone and other transmitters, and even the ambient light can cause disturbance. Another possible source of external disturbance is the line frequency (60 Hz) interference. Therefore, we used battery operated power supplies and a dedicated external grounding for the noise measuring AC equipment, which is completely isolated from the laboratory building ground. The *1/f*

21

noise measurement is so sensitive to 60 Hz line frequency interference that the AC equipment like multimeters, if connected to the power line, can impact with a large 60 Hz peak and its odd numbered harmonics in the measured PSD even with the equipment turned off during the measurement. Hence, multimeters have to be disconnected completely from the power line ground before starting a noise measurement. Moreover, the weak signal from the device under test (DUT) can get corrupted before it is fed to the dynamic signal analyzer (D.S.A.) and hence, a low noise preamplifier is required. We used an EG&G PAR 113 voltage preamplifier for our RTS and *1/f* noise measurements. In the case of strong inversion in linear operation region, input current noise increases proportionally with the decrease in device resistance when the bias is increased [11]. This will cause distortion in the output signal due to lower input impedance and hence, we chose a voltage preamplifier over a current preamplifier in our measurements. The use of preamplifier also improves the sensitivity of the D.S.A., which does the fast Fourier transform (FFT) of the time domain signal and analyzes the signal in frequency domain. The setting for the preamplifier was: frequency range 0.03-300 KHz, typical gain 1000 for *1/f* noise and 10000 for RTS noise measurement in AC coupling mode. Since the stochastic ergodic signal is often not periodic due to the signal randomness, a Hanning window function (for its better frequency resolution) is used to limit the spectral broadening of the FFT signal [11]. Other sources of disturbances like the device thermal noise, noise from the preamplifier itself and those external sources mentioned above, all constitute what is known as the 'background noise'. This noise can be measured by keeping the gate bias on and turning off the drain bias immediately after 'actual device noise' measurement at each gate bias. The background noise PSD is subtracted from that measured noise PSD with the drain bias 'ON', to obtain the net device noise PSD at that particular gate bias. Figure 2-3 shows the drain-source voltage *1/f* noise PSD, S_V for

22

a 30 V device before stress. For each measured spectrum, a power fitting was done to find $S_V(1Hz)$. Then, $S_I(1Hz)$ was computed through $S_I(1Hz) = S_V(1Hz) \cdot g_{D_{eff}}^2$ where $g_{D_{eff}}$ is the effective conductance of the LDMOS (including the conductance from the channel and the extended drain).
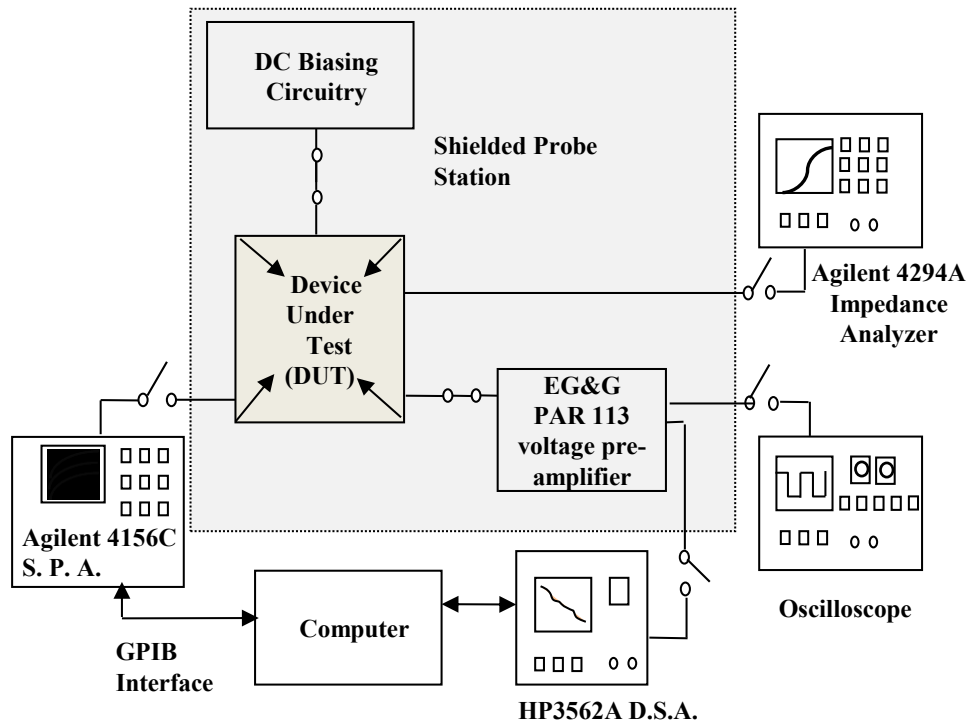
Figure 2-1 A schematic representation showing the setup for *1/f* noise, RTS noise, DC characteristics and C-V characteristics measurement.
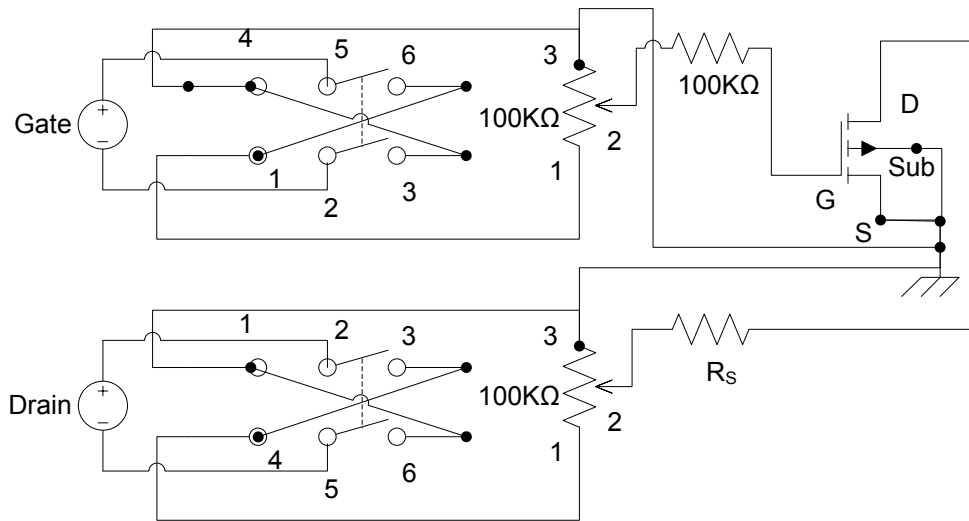
Figure 2-2 A schematic representation of the DC biasing circuitry used in the experimentation for both *1/f* noise measurements in LDMOS, and RTS noise in low voltage submicron analog transistors.
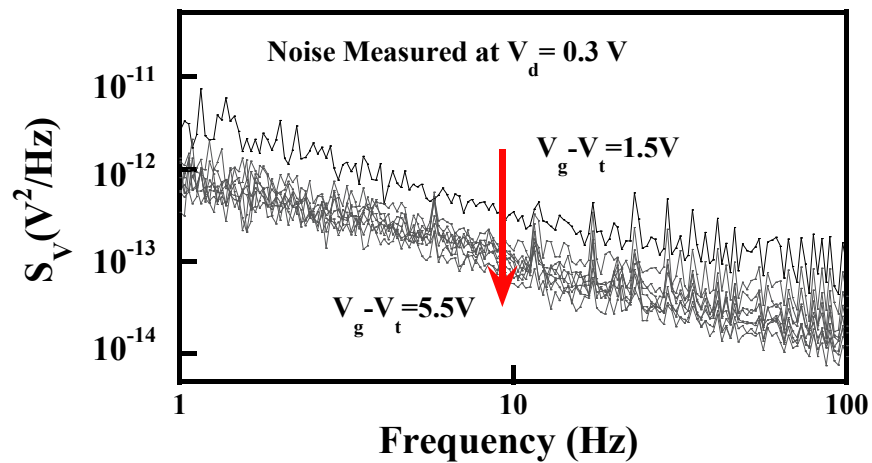
Figure 2-3 Measured drain-source voltage noise power spectral density for a 30 V rated LDMOS at gate overdrive voltages of 1.5-5.5 V before stress.
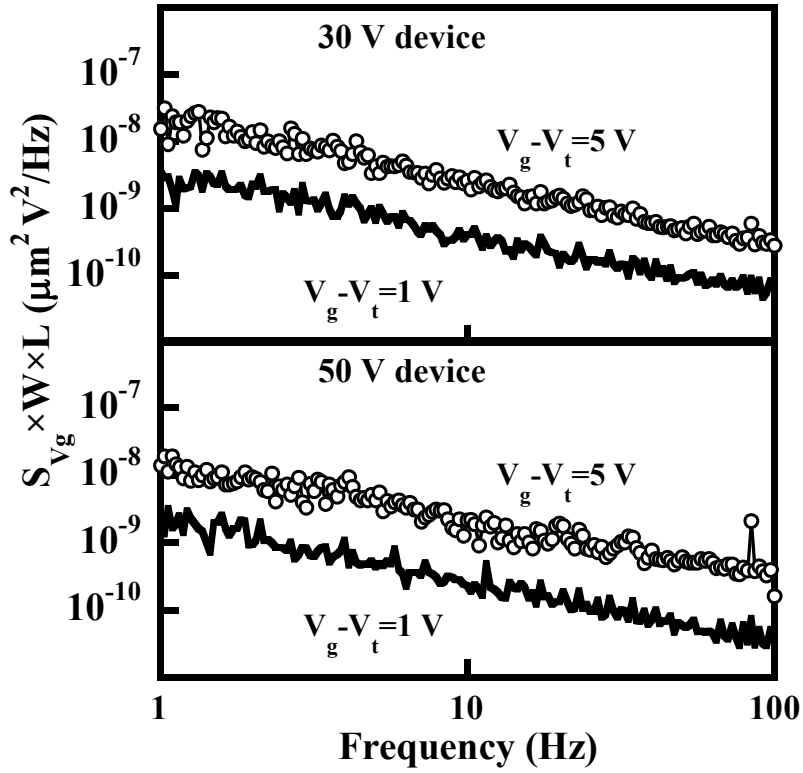
Figure 2-4 Input referred noise for different LDMOS devices at V_d =0.3 V before

stressing. The noise measurements were done for several more decades of frequencies

which are not shown here.

The input-referred noise PSD, S_{V_g} is shown in Figure 2-4 for a 30 V and a 50 V

devices which have the same channel length and width. The input referred noise is

calculated from: $S_{Vg} = S_I / g_m^2$ where S_I (A²/Hz) is the drain current noise spectral density

and g_m (A/V) is the device transconductance. The normalized flicker noise is comparable

to the results of Dikshit *et al.* [43] in case of both LDMOS and in standard CMOS

transistors.
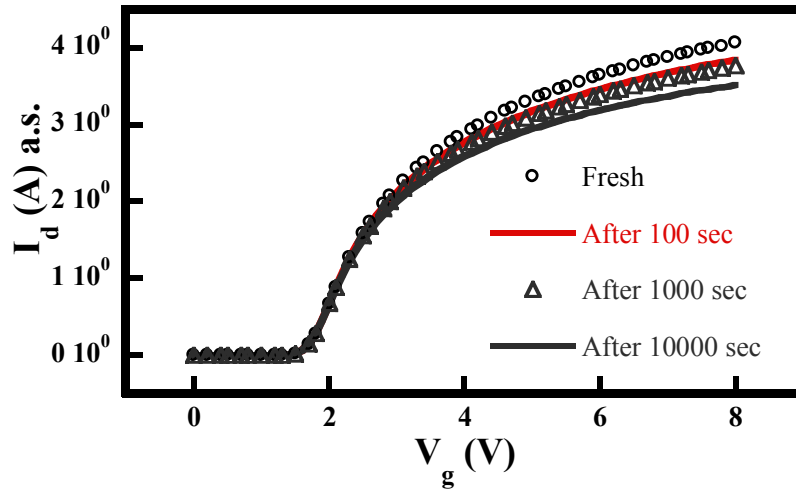
(a)
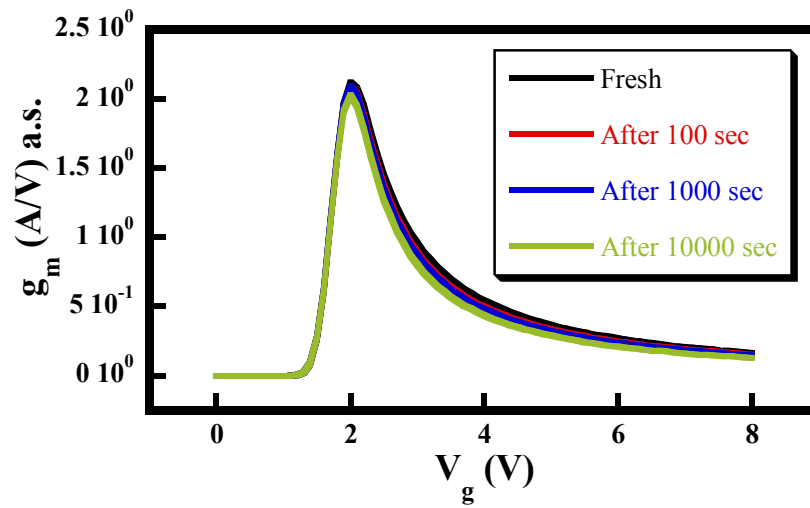
(b)

Figure 2-5 (a) Measured drain current (b) transconductance as a function of gate voltage

after different stressing times for a 40 V-rated device stressed at V_d =40 V and V_g =4 V.

2.4 Stressing and DC Measurements

Before performing a noise measurement, DC characterizations are to be done on the devices. All the DC and LFN measurements on LDMOS were performed at V_d = 0.3 V before and after applying cumulative stress at the worst DC degradation (i.e. drain current in linear region, I_{dlin} and on-resistance, R_{on} degradation) condition.

In the Kelvin measurement system, the force and sense terminals of the semiconductor parameter analyzer (S.P.A.) Agilent 4156C were always shorted before connecting to the device itself to minimize the possibility of formation of any potential difference across the device terminals. The device parameters that we measured were the gate (I_g) and drain (I_d) currents, subthreshold swing $\left(S_s = \dfrac{dV_g}{d\left(\log I_d\right)} \right)$ and the threshold voltage V_t, which can be found from the intercept of the slope of square root of drain current $\left(\sqrt{I_d} \right)$ at the point where the differentiation of that term with respect to gate bias $\left(d\sqrt{I_d}/dV_g \right)$ is at maximum. A representative transfer characteristics and transconductance $\left(g_m = \dfrac{dI_d}{dV_g} \right)$ plots are shown in Figure 2-5. A typical output characteristics (I_d-V_g) curve is shown in Figure 2-6 and then, a procedure for threshold voltage extraction for LDMOS is illustrated in Figure 2-7.
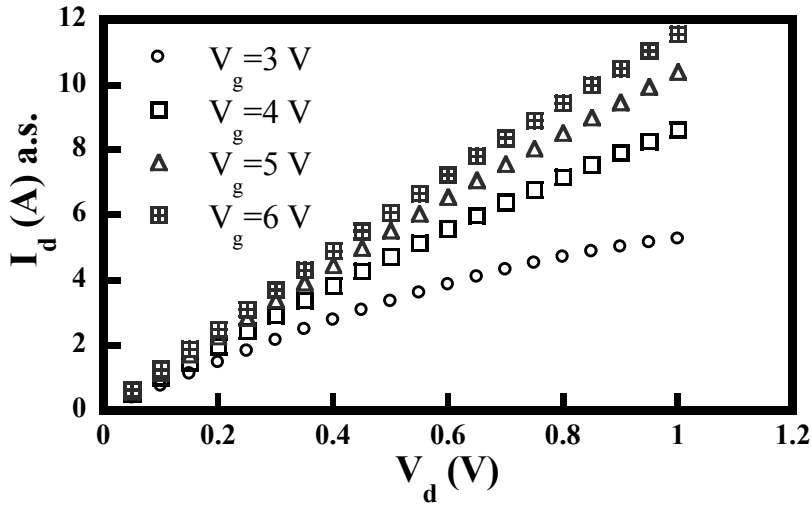
Figure 2-6 A typical output characteristics for a 40 V NLDMOS device at room

temperature. Only linear region measurement results are shown at different gate biases.
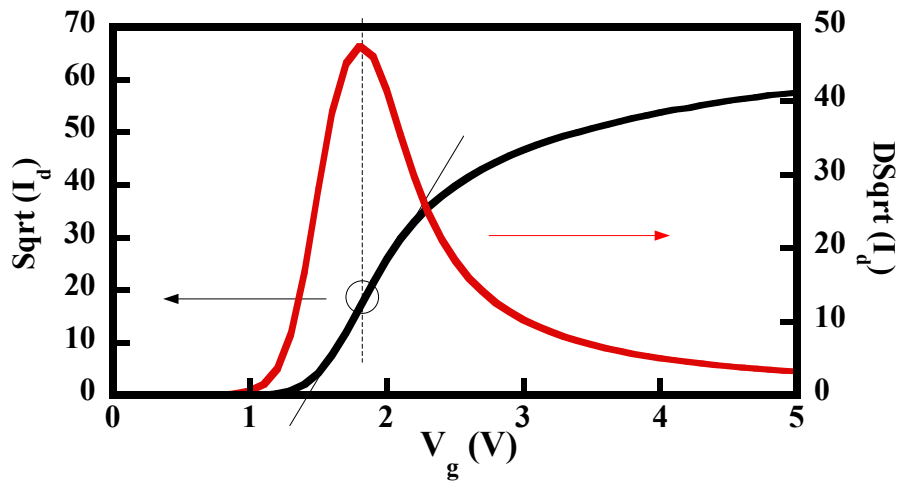
Figure 2-7 An example of threshold voltage extraction method, which is applicable for

both LDMOS and low voltage CMOS. A tangent is drawn on the *Sqrt (I_d)* curve i.e. on

$\left(\sqrt{I_d} \right)$ at the gate voltage where DSqrt (I_d) i.e $\left(d\sqrt{I_d} \big/ dV_g \right)$ is at maximum, as

highlighted by the circle on the vertical line. The intercept of the tangent on the x-axis

identifies the threshold voltage. Y axes are arbitrary here.

DC stressing was accomplished starting by applying the rated voltages at the gate and drain, respectively. Then, other stressing conditions were tested with reduced DC gate stress voltage while the drain remained at the rated voltage. After that, the drain voltage was either kept at the rated value or slightly higher than the rating, depending on the device degradation rate. This accelerated stress condition at higher drain voltages was required in some of the devices to ensure sufficient impact ionization of charge carriers (due to Kirk effect) to take place in the p-body/NWell junction, which could result in a measurable degradation in the LDMOS output characteristics. Five to seven different stressing conditions were tested to evaluate the worst degradation condition, each time in a fresh (unstressed) device. The on-resistance (R_{on}) was measured at V_d = 0.3 V and V_g = 4.5 V. All the stress experiments were carried out on wafer level at a constant ambient temperature of 25°C in a shielded probe station. The selected stressing conditions are summarized in Table 2-1.

Table 2-1 Stressing Conditions for Different LDMOS Devices, Corresponding to Their Worst Degradation Condition, Respectively

Device drain voltage rating	Stress voltage for worst degradation	
	V_d (V) during stress	V_g (V) during stress
20 V	22	5
30 V	30	5
40 V	40	4
50 V	53	4

2.5 Standalone DNWell Resistor Noise Measurements

As explained in detail in Chapter 3, it was necessary to measure the *1/f* noise in standalone DNWell resistors to evaluate their equivalent noise contribution to the LDMOS. The bulk resistance fluctuation in the extended drain under the field oxide ($S_{R_{ED_{FO}}}$) and that under the gate oxide ($S_{R_{ED_{GO}}}$), were estimated by doing separate noise measurements on standalone DNWell resistors with a gate oxide and field oxide over them, located on the same wafers. The concept of separate DNWell resistors is depicted in Figure 2-8. The details of the fabrication process for the standalone DNWell resistors (with length bigger than the width) can be found in [44]. The *1/f* noise in these resistors are measured by considering these as two terminal devices and applying high bias in one contact and low bias in another contact. The contact at low potential is also connected to the substrate during measurement to avoid any junction formation between the NWell and the substrate.

Figure 2-9 shows the normalized noise PSD at 1 Hz at different bias currents for standalone DNWell resistors under gate oxide and field oxide, respectively. Then, the equivalent noise in the extended drain region under the gate oxide and in the field oxide bulk are calculated from the average noise data from the DNWell resistors by using

$$\frac{S_{R_{GO}}}{R_{GO}{}^2} = \frac{S_{R_{ED_{GO}}}}{R_{ED_{GO}}{}^2} \tag{2.1}$$

and
$$\frac{S_{R_{FO}}}{R_{FO}{}^2} = \frac{S_{R_{ED_{FO}}}}{R_{ED_{FO}}{}^2} \tag{2.2}$$
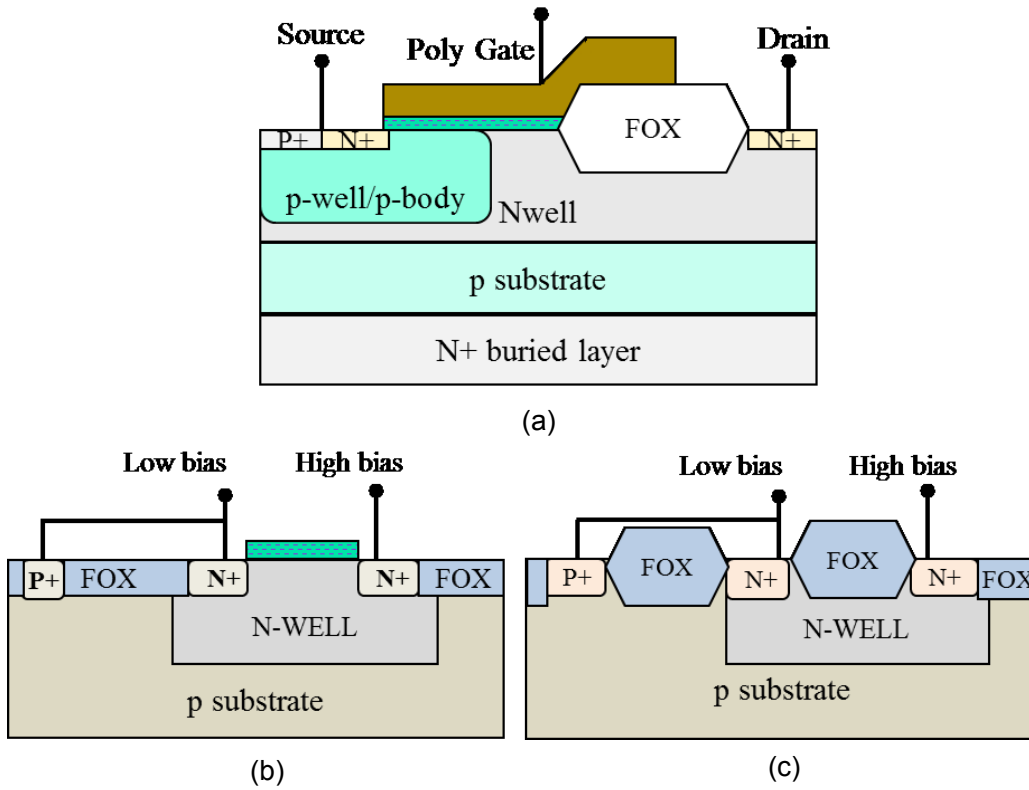
Figure 2-8 Explaining the standalone DNWell resistors concept from an LDMOS. (a) The LDMOS itself. DNWell resistors are shown in (b) under the gate oxide, and in (c) under the field oxide.

where $S_{R_{GO}}$ and $S_{R_{FO}}$ are the measured resistor noise and R_{GO} and R_{FO} are the resistances of the standalone resistors with gate and field oxides, respectively. The obtained noise results from DNWell resistors were extrapolated to estimate the equivalent low frequency noise in the extended drain under the gate and field oxides with the scaling expressions in (2.1) and (2.2).
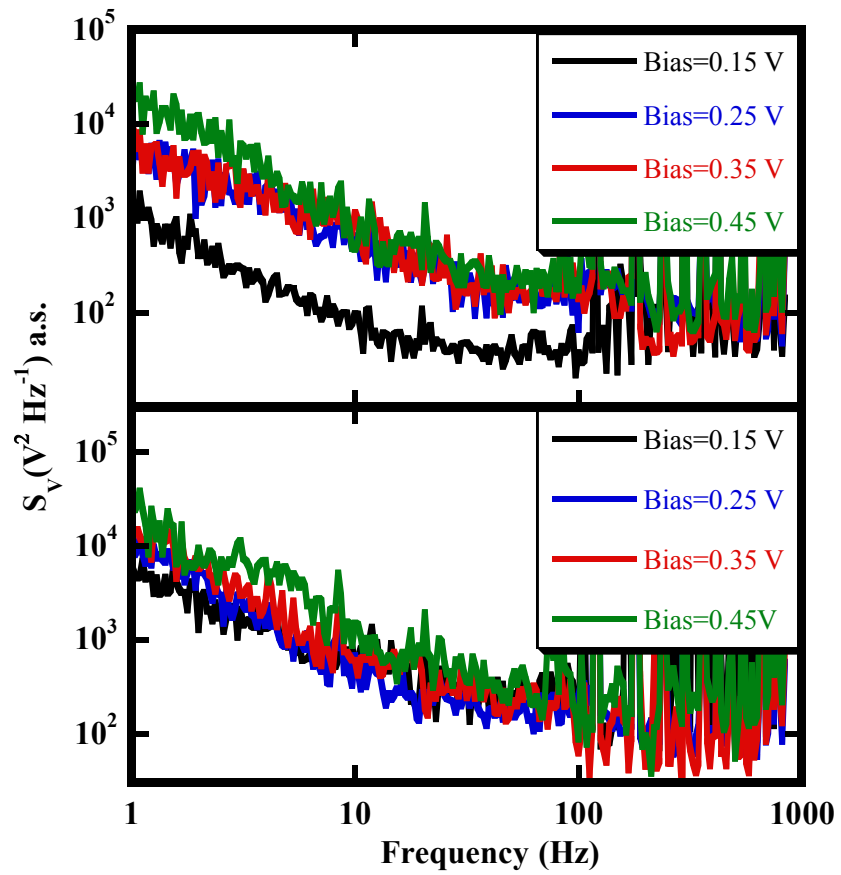
Figure 2-9 Bulk resistance fluctuations in the form of PSD in a standalone DNWell resistor under the gate oxide (top) and that under the field oxide (bottom). Y axis is arbitrarily scaled.
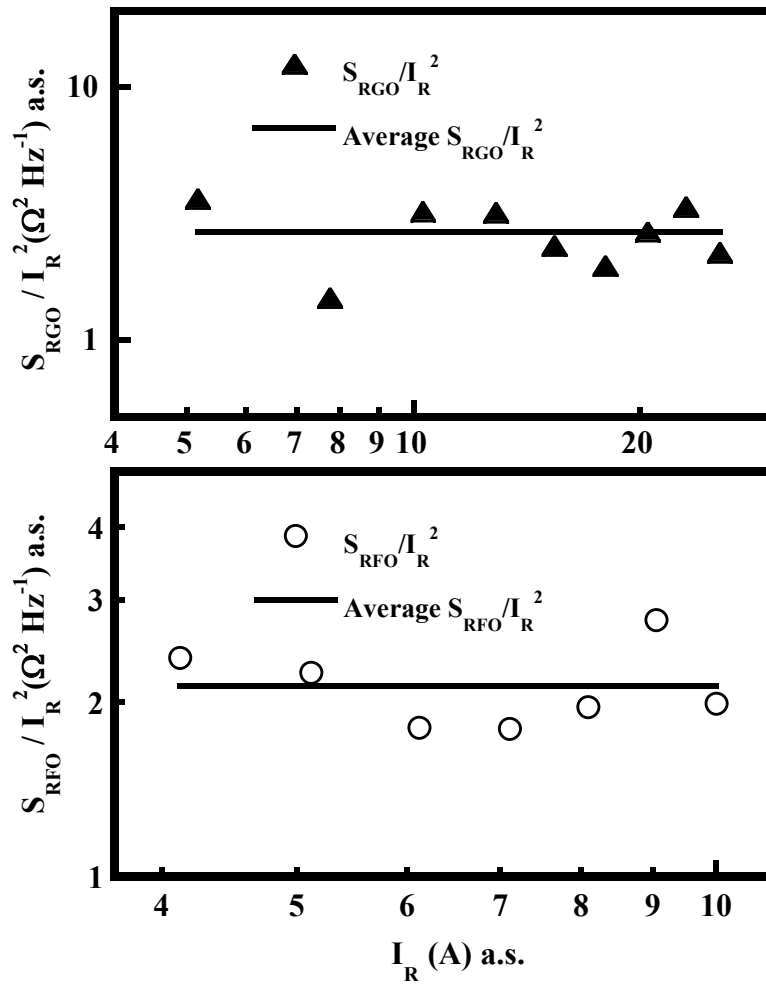
Figure 2-10 Measured (top) $S_{R_{GO}}$ and (bottom) $S_{R_{FO}}$ as a function of resistor current (I_R)

are shown after normalization with the current which were then arbitrarily scaled.

2.6 Summary

In this chapter, the details of the noise measurement, DC measurement, stressing technique, and additional measurement procedure for DNWell resistors are provided. Mathematical formulation for conversion from DNWell resistor noise towards LDMOS device noise measurement is delineated. Setting up the measurement system, designing of the bias box and necessary precautions to be taken during and before measurement are also highlighted. Results from these measurements laid the foundation for analyzing the specifics of LDMOS degradation from a microscopic point of view in Chapter 3 and for developing the *1/f* noise model in Chapter 4.

Chapter 3

Analysis of Stress Induced Degradation in LDMOS

3.1 Introduction

Medium and high voltage LDMOS transistors, with voltage-rating of 20-600 V, need to maintain stringent reliability requirement during operation, for example, when these are part of automotive and medical appliances, or utilized in military radio. As such, accelerated device degradation evaluation is needed in power semiconductor devices to ascertain the reliability of the device performance. In this chapter, we describe the degradation behavior of *1/f* noise with varying stressing time, in three distinct regions of LDMOS under the worst degradation condition. The DC stressing was interrupted after each predetermined interval, and DC and noise measurements were done before resuming stressing again. The LDMOS field oxide (FOX) dimension optimization remains a critical challenge for circuit designers, which is addressed here in terms of the device noise performance. The contribution of drain current fluctuations from the dielectric traps is evaluated as a function of stressing time. Finally, the increase in *1/f* noise was found to emerge earlier and in a more pronounced manner in the noise components compared to degradation observed in DC parameters. The analyses reported here are measurement-driven, in addition to computer modeling, which provide better insight to the actual device degradation.

3.2 Effect of Stress on DC and Noise Characteristics

Cumulative DC stressing up to 10,000 sec was performed on 20-50 V transistors at the worst degradation condition (maximum I_{dlin} and g_{mlin} reduction), and I-V and *1/f* noise along with background noise measurements were done after 10 sec, 100 sec, 200 sec, 500 sec, 1000 sec, 2000 sec, 3000 sec, 5000 sec and 10000 sec by interrupting the

continuous stressing. Unlike [1], we did not observe any reduction in R_{on} for short stressing time, which eliminates the possibility of hot-hole injection near the bird's beak at low gate voltage stressing. Due to the worst hot carrier stress occurring at low to moderate V_g, the interface trap generation takes place in the extended drain accumulation region near the source side bird's beak and in the accumulation region [1]. At high gate biases, the critical electric field and therefore, the degraded region moves near the drain side bird's beak which is subdued by the field oxide isolation. At low gate bias voltages, overall resistance is predominantly the channel resistance, which is mostly unaffected by the applied stress (Figure 3-1). However, the percentage of resistance degradation increases, as an example, from 2% towards ~11% at high gate biases, when measured at high gate overdrive ($V_g - V_t$) voltages. Please note that $1/g_{D_{eff}}$ is plotted instead of the conductance itself, to illustrate the degradation better.

The typical DC components, $I_{dlinmax}$, g_{mmax} and R_{on} show (Figure 3-2) a sharp increase in degradation for relatively low stressing time (0-500 sec) due to increased carrier scattering and interface state generation [33] as well as an increase in the series resistance of the gate-overlap region. For higher stressing time, the device degradation tends to saturate. According to [45], this is due to the induced interface traps forming a potential barrier that prohibit subsequent hot carriers from causing further damage and therefore the device degradation saturates.
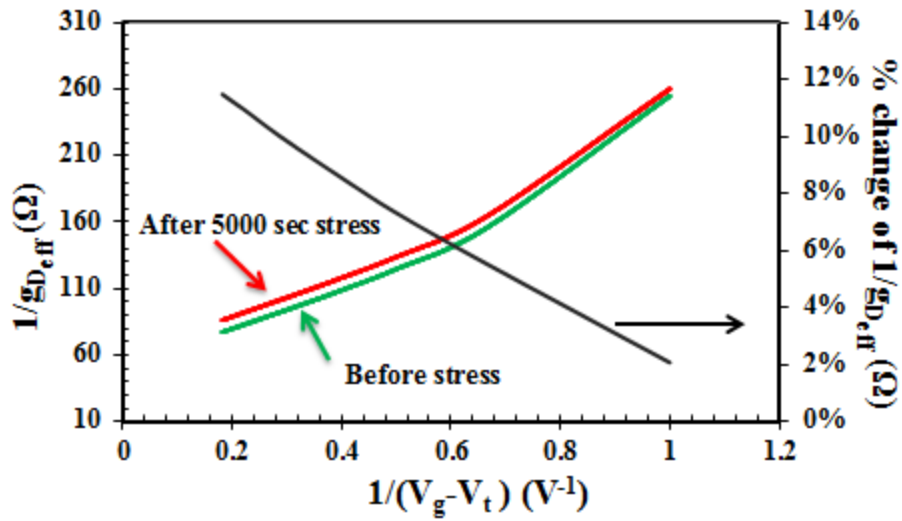
Figure 3-1 Measured LDMOS resistance as a function of gate bias before and after 5,000 sec stress. The device was a 40 V transistor, which was stressed at V_g =4 V and V_d =40 V. The effective channel resistance seems to remain unchanged with stress at low gate bias voltages. Percentage increase in degradation is shown on the secondary axis.

We have hitherto discussed DC degradation in LDMOS. Now, let us switch our focus to the *1/f* noise behavior. For each of the 20 V, 30 V, 40 V and 50 V-rated devices at low gate voltages, the channel noise dominates, and the overall measured noise was found not to change notably with stress. However, at relatively higher gate biases, where the extended drain region becomes the dominant noise source over the channel, the noise exhibits an increase with stress [35, 46]. This is illustrated in Figure 3-3 for three different voltage rated devices.
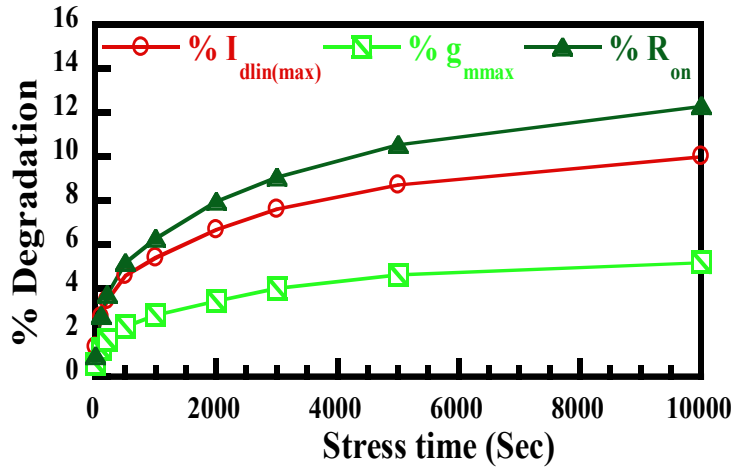
Figure 3-2 DC degradation behavior for a 30 V device stressed at V_g =5 V and V_d =30 V

up to 10,000 sec. R_{on} measured at V_g =4.5 V and V_d =0.3 V. The rate of initial

degradation (up to 500 sec) is very sharp, and tends to behave sub-linearly thereafter.

All measured noise spectra exhibited $1/f^{\delta}$ behavior with $0.7 \leq \delta \leq 1.4$. Once a

numerical least square fitting is done for each of the measured drain-source voltage *1/f*

noise PSD in Figure 3-3, S_V (V^2/Hz) at 1 Hz can be extracted, and then was plotted as a

function of gate overdrive voltages (Figure 3-4). S_V was then converted to drain current

noise PSD S_I using the overall measured channel conductance as was explained in

Chapter 2. Fig. 3-5 shows overall measured noise S_I (1Hz) normalized with drain

current, as a function of gate bias for all the different rated devices.
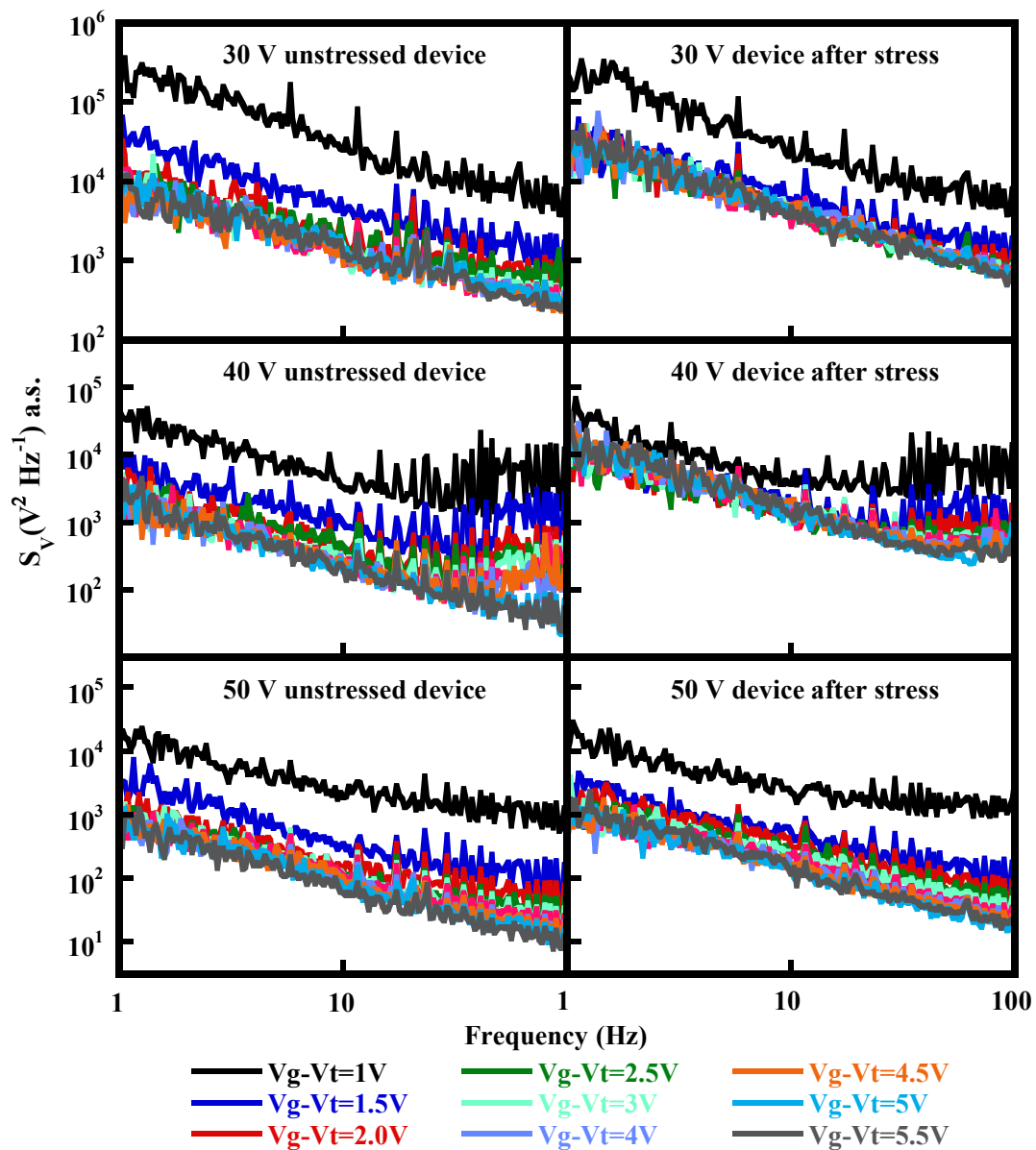
Figure 3-3 Noise power spectra for 30 V, 40 V and 50 V devices before and after 5,000 sec stress. Stress conditions were: for 30 V device V_g =5 V and V_d =30 V; for 40 V device V_g =4 V and V_d =40 V and for 50 V device V_g =5 V and V_d =53 V.
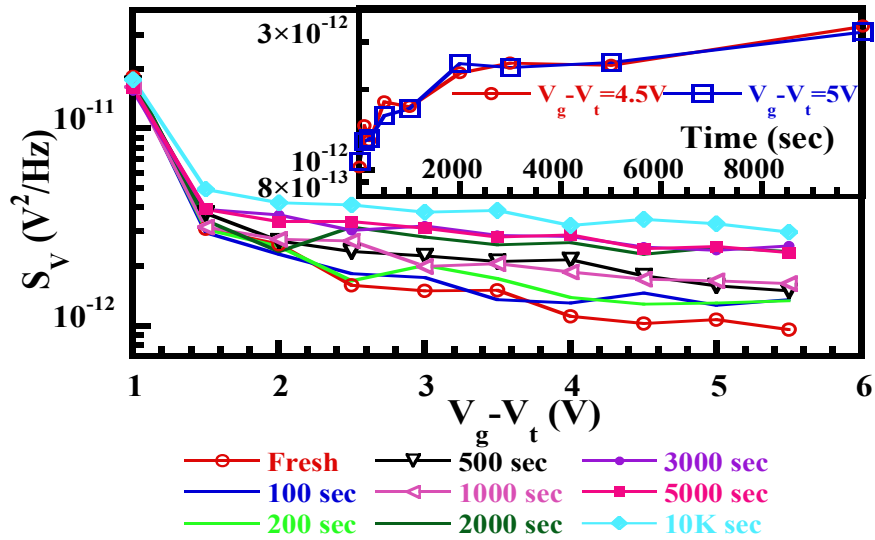
Figure 3-4 Measured noise PSD, S_V at 1 Hz for a 30 V device at different gate overdrive voltages, from fresh (unstressed) condition up to 10,000 sec stress in eight steps. The stressing condition was V_g =5 V and V_d =30 V. The inset shows S_V at 1 Hz as a function of stressing time.

Since noise is a stochastic random process, a crucial question about repeatability of the observations needs to be clarified at this point. As evident from Figure 3-6, the variation in exhibited *1/f* noise from device to device was indeed found negligible. Such a consistency was observed in other different voltage rated devices as well.
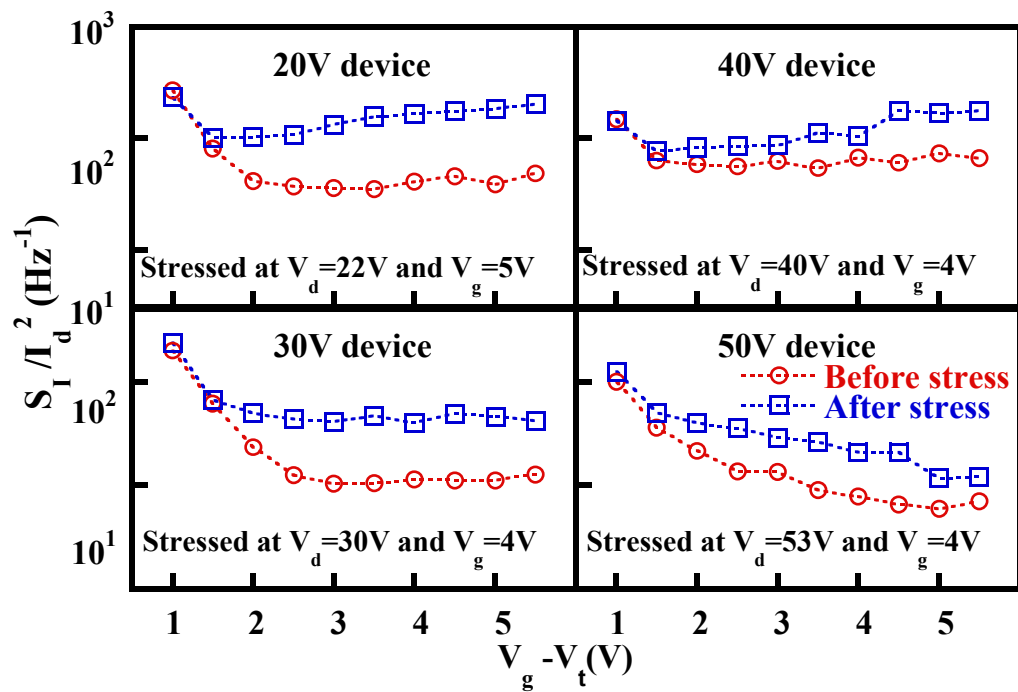
Figure 3-5 Increase in drain current normalized noise magnitude after 5,000 sec stress. Y

scale is arbitrary. At low V_g, where the channel noise is dominant, degradation with

stress is minimal. However, at relatively high V_g where the extended drain region plays

an important role, severe degradation occurs due to trapped carrier fluctuations in the

NWell-SiO$_2$ interface.
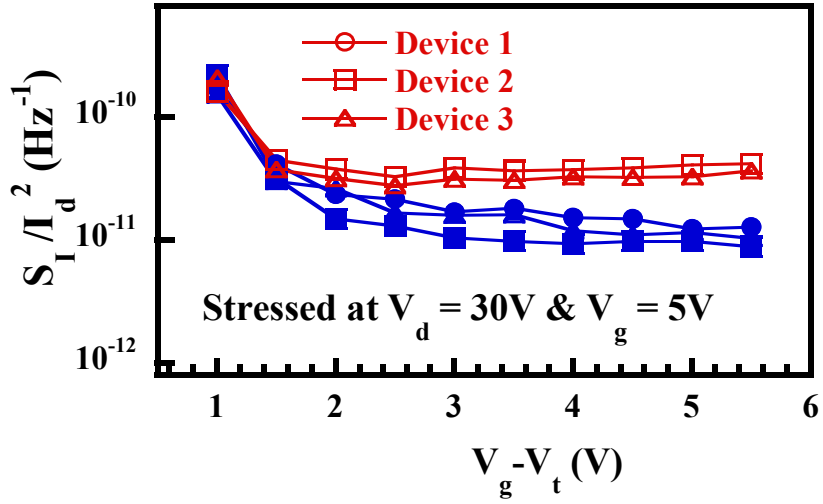
Figure 3-6 Drain current normalized *1/f* noise at 1 Hz for three 30 V rated devices. Blue colored symbols represent devices before stress and red colored symbols are for the corresponding devices after 5,000 sec stress.

3.3 Separation of Resistance Components

For the linear operation region, the effective, measured drain to source resistance can be expressed as a summation of the channel resistance $1/g_D$, the drain overlap resistance R_{over} and the extended drain region resistance under the field oxide $R_{ED_{FO}}$ using:

$$\frac{1}{g_{D_{eff}}} \approx \frac{1}{g_D} + R_{over} + R_{ED_{FO}} \tag{3.1}$$

These resistance components are shown in Figure 3-7. Here, g_D is the channel-only conductance. The gate bias dependent channel resistance is calculated by using low field mobility approximations from the measured I-V characteristics. Please note that R_{over} is
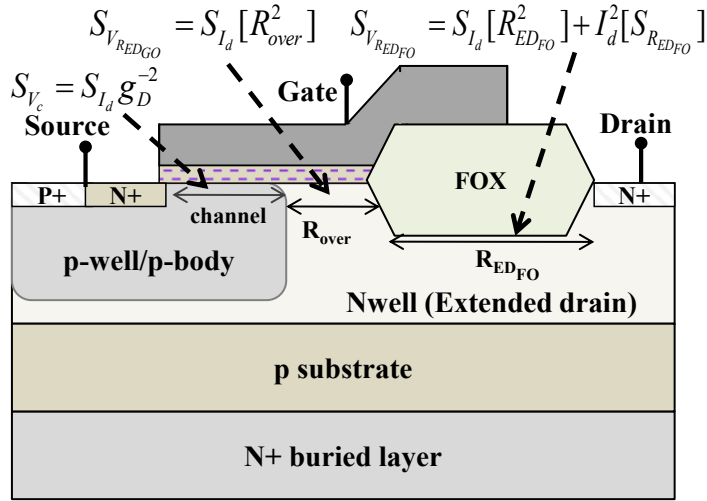
Figure 3-7 Cross-sectional schematic for an LDMOS with all the resistance and noise components shown.

the resistance under the gate–overlap in the extended-drain, which is in accumulation and therefore much less than the bulk resistance $R_{ED_{GO}}$ (Figure 2-8) of the same region. The effect of spreading resistance in DNWell near the bird's beak and the contact resistances of the source and drain are considered negligible for the fabrication process technology utilized here. No notable shift in threshold voltage was found, while I_{dlin}, and maximum transconductance $g_{m\max}$ changed considerably due to stressing. $R_{ED_{FO}}$ was obtained using stand-alone DNWell resistor structures on the same die as the measured LDMOS (discussed in Chapter 2). Then, from the measured $R_{ED_{FO}}$, $g_{D_{eff}}$ and using the calculated g_D, R_{over} was determined for each bias condition. Since the extended drain resistance under the field oxide does not degrade due to stressing at worst degradation condition, we can consider $R_{ED_{FO}(\text{stressed})} \approx R_{ED_{FO}(\text{fresh})}$ [39, 40]. Again, since no

43

degradation was observed in the channel, we approximate that $g_{D(\text{stressed})} \approx g_{D(\text{fresh})}$. As depicted in Figure 3-8, the channel does not exhibit degradation due to applied stress because of the double RESURF effect in the extended drain and the N$^+$ buried layer [47]. Then, the drain overlap resistance after stress $R_{over(\text{stressed})}$ can be found from the measured effective drain-source resistance after stress $g_{D_{eff}(\text{stressed})}$ using:

$$R_{over(\text{stressed})} = \frac{1}{g_{D_{eff}(\text{stressed})}} - \frac{1}{g_{D_{eff}(\text{fresh})}} + R_{over(\text{fresh})} \qquad (3.2)$$
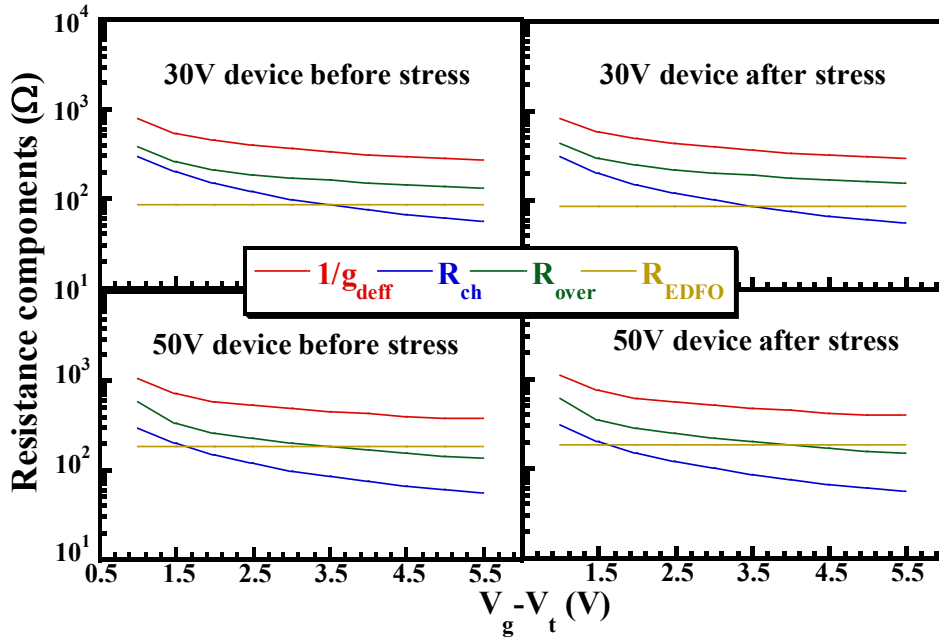
Figure 3-8 Different resistance components as a function of gate voltage before and after 5,000 sec stress. 30 V device was stressed at V_g =5 V and V_d =30 V while 50 V device was at V_g =5 V and V_d =53 V.

At low gate voltages, overall resistance is predominantly the channel resistance, which is almost unaffected by the applied stress (Figure 3-8). The channel resistance ($R_{ch} = 1/g_D$), and the resistance of the drift region, $R_{ED_{FO}}$ were found to remain unaffected with stressing, while the extended drain region resistance under the gate oxide-overlap R_{over} increased considerably with stress [35].

3.4 Separation of Noise Components

The total voltage noise PSD can be written, by summing the contributions from the channel ($S_{V_c} = S_{I_d} g_D^{-2}$), the extended drain regions under the gate oxide (ED_{GO}) ($S_{V_{R_{ED_{GO}}}}$), and the field oxide (ED_{FO}) ($S_{V_{R_{ED_{FO}}}}$) as [11, 48]:

$$S_V = S_{V_c} + S_{V_{R_{ED_{GO}}}} + S_{V_{R_{ED_{FO}}}} \tag{3.3}$$

The different noise components were shown in Figure 3-7. S_{I_d} (A^2/Hz) is the PSD of drain current fluctuations originating at the Si-SiO$_2$ interfaces in the channel and gate-oxide overlap region. Since the majority of the current is at the interface in ED_{GO} due to accumulation, the noise PSD is dominated by the interface fluctuations $S_{I_d} R_{over}^2$, and not by the bulk resistance fluctuation $I_d^2 S_{R_{ED_{GO}}}$ [35, 46]. Here, we approximated noise in the ED_{GO} region as: $S_{V_{R_{ED_{GO}}}} = S_{I_d} R_{over}^2 + I_d^2 S_{R_{ED_{GO}}} \approx S_{I_d} R_{over}^2$. In the ED_{FO} region, however, the current spreads, requiring both bulk and interface components to be considered $\left(S_{V_{R_{ED_{FO}}}} = S_{I_d} R_{ED_{FO}}^2 + I_d^2 S_{R_{ED_{FO}}} \right)$. Summing the components and rearranging the terms:

$$S_V = [S_{I_d} g_D^{-2} + S_{I_d} R_{over}^2 + S_{I_d} R_{ED_{FO}}^2] + I_d^2 S_{R_{ED_{FO}}} \tag{3.4}$$

Equation (3.4) can be interpreted as two independent fluctuation sources: S_{I_d}

and $S_{R_{ED_{FO}}}$. The former makes up the first three terms in Eq. (3.4) and is due to trapping

and detrapping of charge carriers at the gate dielectric/channel interface (in inversion), in

the gate dielectric/overlap region interface R_{over} (in accumulation), and in the

dielectric/drift region (under the field oxide) interface. The second source is the bulk

resistance fluctuations $S_{R_{ED_{FO}}}$ (Ω^2/Hz) from $R_{ED_{FO}}$ the extended drain NWell bulk

resistance under the field-oxide. This is the last term in Equation (3.4). S_{I_d} in unstressed

devices can be calculated by knowing the resistance components and by using the

equivalent $S_{R_{ED_{FO}}}$ from DNWell resistor noise measurement (refer to Chapter 2).

Following the unified flicker noise model [49], developed for CMOS, the drain

current fluctuations can be attributed to the trapping and detrapping of charge carriers by

the traps in the gate dielectric and at the Si-SiO$_2$ interface. For the LDMOS case,

however, not only the gate dielectric/channel interface (in inversion), but also the gate

dielectric/drain overlap region interface (in accumulation) contributes. Since the bulk

resistance under extended drain field oxide does not degrade with low gate voltage

stress, $S_{R_{ED_{FO}}}$ remains unaffected with stressing. Hence, S_{I_d} after stress can be

calculated by:

$$S_{I_{d_{stress}}} = \frac{S_{v_{stress}} - I_{d_{stress}}^2 S_{R_{ED_{FO_{fresh}}}}}{g_{D_{fresh}}^{-2} + R_{ED_{FO_{fresh}}}^2 + R_{over_{stress}}^2} \tag{3.5}$$

With the knowledge of each of the resistance components and $S_{R_{EDFO}}$ through the aforementioned analyses for fresh and stressed conditions, the noise components in Eq. (3.4) before stress and in Eq. (3.5) after stress can be individually evaluated as depicted in Figure 3-9. Here, $I_d^2 S_{R_{EDFO}}$ contribution to overall noise is insignificant and shows a negligible increase with stress because of I_d degradation. However, the channel voltage noise, $S_{I_d} g_D^{-2}$ and all other noise components display an increase with stress as S_{I_d} increases, with the maximum increase being in $S_{I_d} R_{over}^2$ component, because of simultaneous degradation effect from R_{over} and S_{I_d} (Table 3.1). This confirms that additional traps are mostly generated in the gate oxide-overlap region due to stress, which are responsible for enhanced trapped carrier fluctuations and further attribute to the worst degradation in that region irrespective of the field oxide LOCOS layer size.
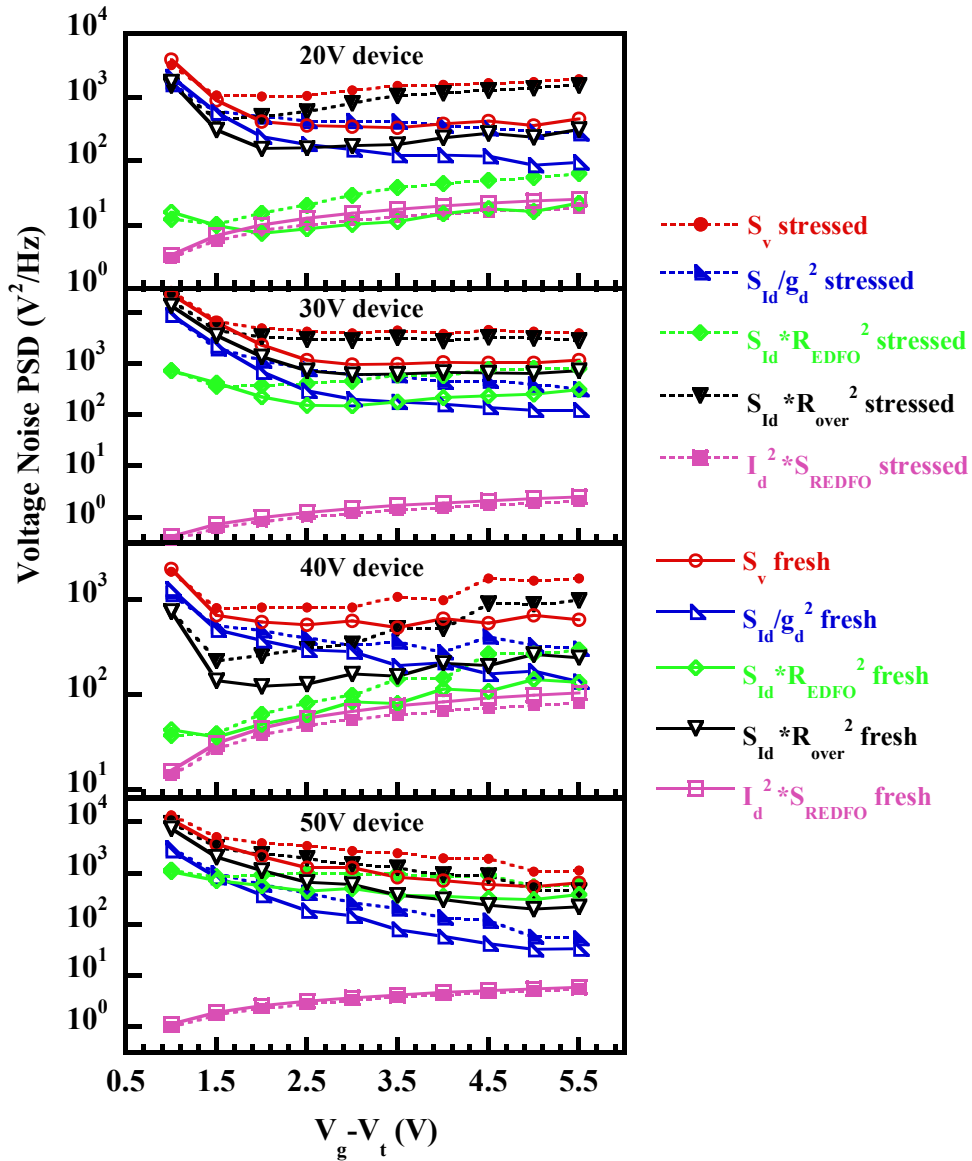
Figure 3-9 Different noise components contributing to the measured noise, before and after 5,000 sec stress. Open symbols-solid lines are for fresh devices and closed symbols-dotted lines are for stressed devices. The bulk fluctuation component $I_d^2 S_{R_{ED_{FO}}}$ is the lowest contributor. Y scale is arbitrary.

Table 3-1 Percentage Increase of Parameters at High Gate Biases after Stress. All the

Data are for the Measurements at $V_g - V_t$ =5.5 V and V_d =0.3 V.

Parameter	Explanation	Device Rating	
		30 V	50 V
$I_{d\,(lin)}$ (A)	Drain to source current	-7.9%	-2.8%
$g_{m\,(lin)}$ (A/V)	Device transconductance	-5.5%	-0.7%
$1/g_{Deff}$ (Ω)	LDMOS overall resistance	8.8%	3.0%
R_{over} (Ω)	Accumulation resistance under the gate oxide overlap region	18.3%	8.3%
S_V (V^2/Hz)	LDMOS $1/f$ noise (at 1Hz)	233.1%	101.8%
$S_{Id}*g_D^{-2}$ (V^2/Hz)	Fluctuation generated in the channel region (at1Hz)	167.1%	91.7%
$S_{Id}*R_{over}^{2}$ (V^2/Hz)	Fluctuation generated under the gate oxide overlap (at1Hz)	280.5%	124.8%
$S_{Id}*R_{EDFO}^{2}$ (V^2/Hz)	Fluctuation induced in extended drain under the field oxide (at1Hz)	167.1%	91.7%
$I_d^2 S_{REDFO}$ (V^2/Hz)	Bulk resistance fluctuation under the field oxide region (at1Hz)	-15.1%	-5.6%

3.5 Stress Duration Dependence of $1/f$ noise

In RESURF or in STI LDMOS, possible origin of charge carrier trapping and detrapping leading to fluctuations are the dielectric/Si interfaces in the channel, in the gate-overlap and in the drift region. As evident in Figure 3-10, the normalized drain current fluctuation increases significantly with stressing. This is because, the accumulated charges in the overlap region (analogous to a depletion-type MOSFET) undergo increased trapping-detrapping at the interface, especially when noise is measured at high gate biases [43, 50].

The drain current fluctuation S_{I_d} is originated at the interface of both the channel and the gate-overlap region which is responsible for causing 'induced' fluctuations in the drift region. For devices having identical channel and gate-overlap regions, this fluctuation increases with the drift region physical dimension. The LDMOS channel noise,
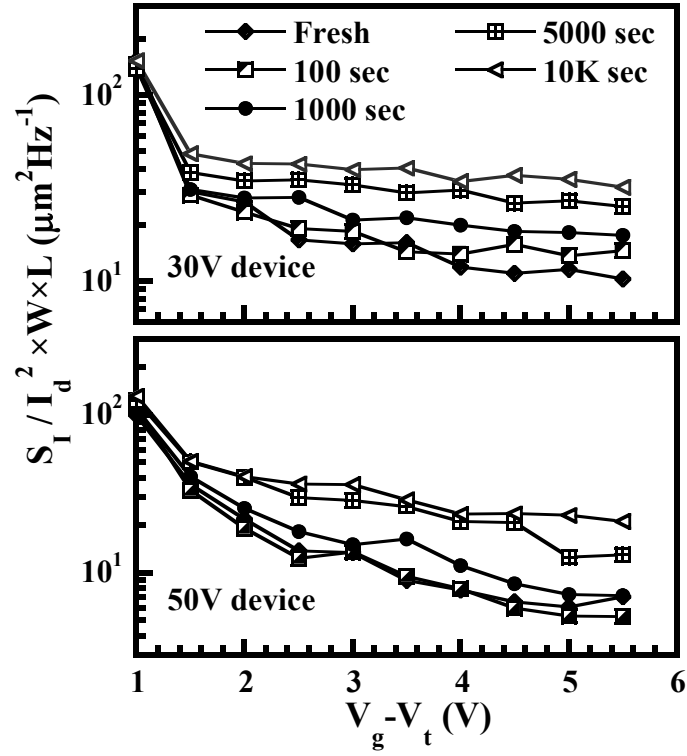
Figure 3-10 Drain-current normalized S_I as a function of gate bias in different rated devices at V_d =0.3 V. Stressing conditions are: for 30 V device V_g =5 V and V_d =30 V and for 50 V device V_g =4 V and V_d =53 V. Y axes are scaled to arbitrary magnitude levels.

$S_{V_C} = S_{I_d} g_D^{-2}$ does not exhibit any stress duration dependence within the breakdown limit (Figure 3-11a). Figures 3-11(b) and 3-11(c) display an increase in noise with stressing time due to increased S_{I_d}. Due to the series resistance increase in R_{over} and greater oxide trap formation in the overlap region leading to additional current fluctuation (S_{I_d}) with stress, $S_{I_d} R_{over}^2$ shows the worst degradation when measured at relatively higher
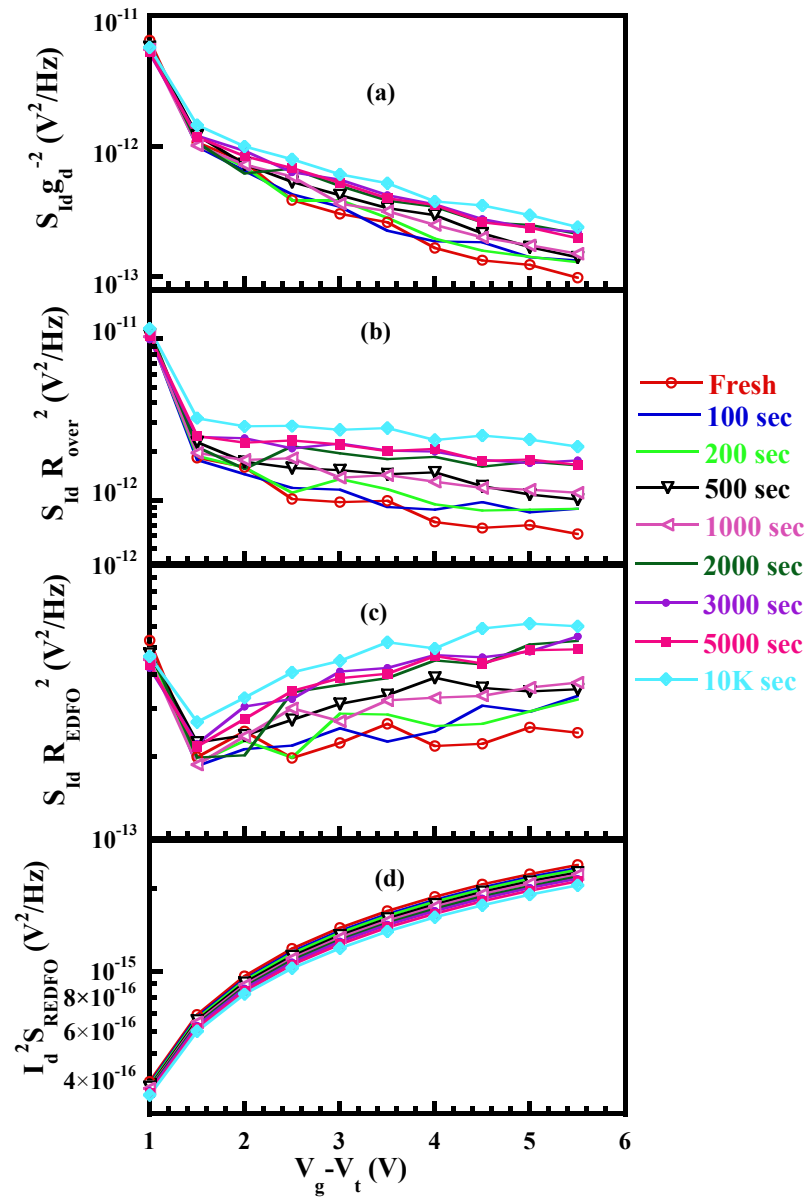
Figure 3-11 Individual voltage noise components contributing to the measured noise in Fig. 3. Voltage noise PSD (a) in the channel, (b) in the extended drain under the gate oxide-overlap region (in accumulation), (c) due to fluctuation in the extended drain under the field oxide induced by S_{I_d}, (d) due to bulk resistance fluctuations inherent in the extended drain under the field oxide of the LDMOS.

gate biases. In presence of the field oxide, bulk fluctuation in the drift region $I_d^2 S_{R_{ED_{FO}}}$ has

a lower impact in degrading the devices [35] and that conclusion is found to be valid for

all the different voltage rated devices that were tested in this study (Figure 3-11d).
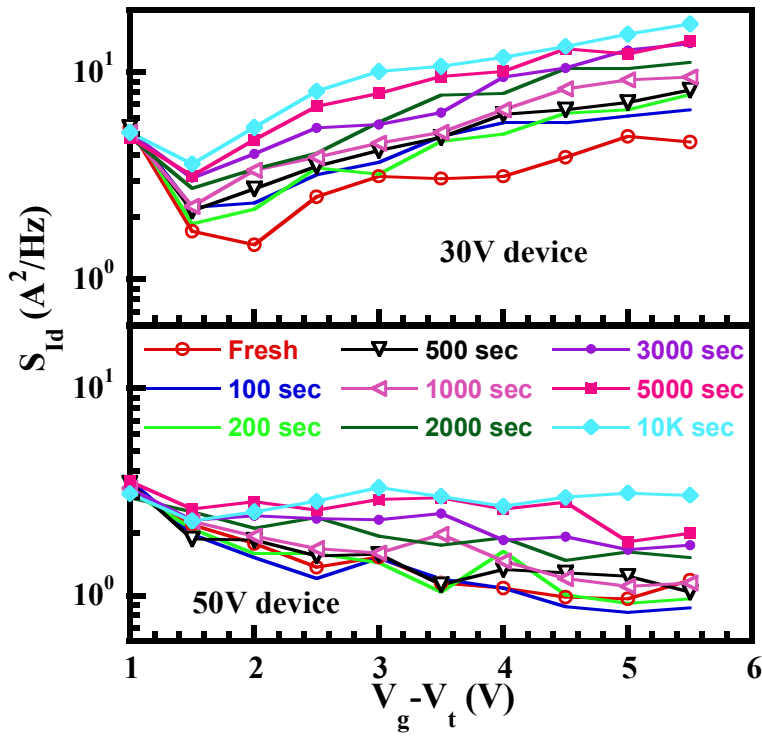
Figure 3-12 Extracted drain current noise PSD at 1 Hz for 30 V and 50 V devices from

fresh (unstressed) condition up to 10,000 sec stress in steps. Y axis is arbitrarily scaled

to the same magnitude level in both the devices. A trend of increase in noise is found at

high gate biases.

This impact of stressing can be far more conceivable if we analyze Figure 3-12,

where the most important parameter associated with LDMOS oxide reliability and

degradation is portrayed. This clearly suggests that a simple resistance degradation

model as depicted by many authors [1, 3, 25, 27], alone cannot be sufficient to investigate the complete degradation behavior of LDMOS devices, especially because of the gate oxide-overlap region, for which one needs to incorporate the impact of trap-assisted drain current fluctuations in the gate oxide.

3.6 A Quantitative Analysis on the Dominant Noise Sources in LDMOS

To derive a comprehensive yet physical model for LDMOS *1/f* noise, we need to first quantify and analyze the dominant noise sources in the device. The measured *1/f* noise is separated into individual noise components as was depicted in Figure 3-11. Since $R_{ED_{FO}}$ does not degrade with stress [35], it is reasonable to assume that the increase in $S_{I_d} R_{ED_{FO}}^2$ component in Fig. 3-11(c) with stress is entirely due to the induced degradation in S_{I_d}. Since, both R_{over} and S_{I_d} degrade with stress, gate-oxide overlap region becomes the worst degraded area in RESURF LDMOS devices. At relatively high gate biases, the degradation is more severe in the extended drain side than the channel side which is consistent with other reports [24, 34]. Finally, the contribution of $S_{R_{ED_{FO}}}$ noise component (Figure 3-11d) to the overall measured noise is found to be a few orders of magnitude less than other noise components and we did not observe any noticeable change in this component in spite of very long stressing time in any device. We reported earlier in this chapter that the $S_{R_{ED_{FO}}}$ does not degrade due to stress. It, therefore, follows that the degradation in $I_d^2 S_{R_{ED_{FO}}}$ component is only due to drain current degradation with stress. As stressing is continued, a small monotonous increase in noise is noticeable at relatively high gate biases.
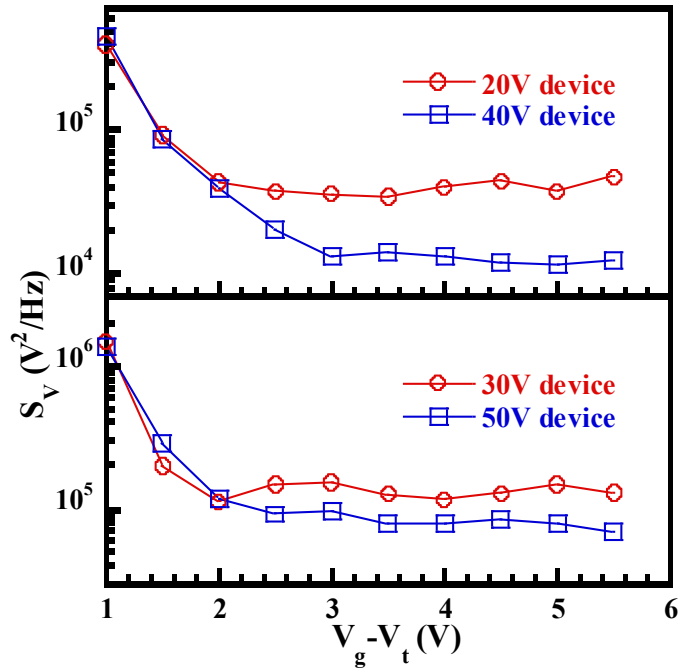
Figure 3-13 Effect of FOX size scaling on noise behavior in different LDMOS at their respective unstressed conditions. For two identical devices with the same channel and overlap length, increase in the FOX length improves noise performance (lowers the noise magnitude). The noise magnitude is arbitrarily normalized.

3.7 Scaling of *1/f* Noise in LDMOS

As the device dimensions will continue to shrink according to ITRS (International Technology Roadmap for Semiconductors) roadmap [51], analysis of aggressive downscaling issues bears significant impact on device reliability and circuit operation viewpoint. Scaling issues can be explored in three perspectives, by varying the length of either the channel, extended drain gate-overlap or the drift length (FOX size) while keeping the rest of the dimensions unchanged. Here, we investigated the effect of variable FOX length. 20 V and 40 V rated devices had the same channel and gate-

overlap dimension while 30 V and 50 V rated counterparts shared the same dimensions. From Figure 3-13, it is identifiable that the device with longer FOX has lower *1/f* noise. Since larger FOX provides more extent for the carriers underneath the field oxide to spread out towards the NWell bulk, the high current density and the corresponding carrier fluctuations near the bird's beak are reduced.
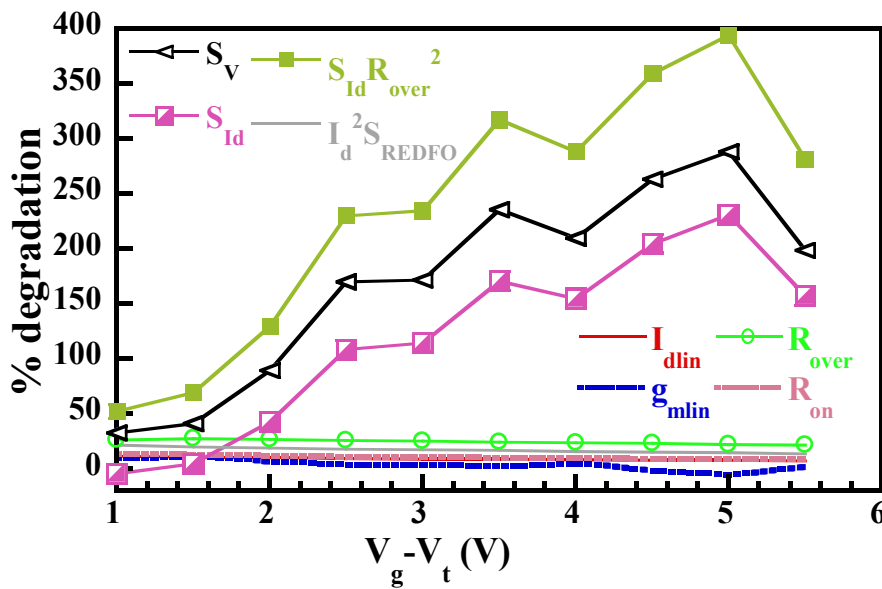
Figure 3-14 Percentage DC and noise parameter degradation comparison after 10,000 sec stress in a 50 V device at V_g =4 V and V_d =53 V. S_V and S_{REDFO} represent measured actual device noise and bulk resistance fluctuation under the field oxide, respectively.

3.8   Early Lifetime Prediction of LDMOS Devices

Another important observation is that we can predict the lifetime of LDMOS devices from the measured *1/f* noise data. Figure 3-14 shows that at relatively high gate effective voltages $(V_g - V_t)$, the degradation in DC components like I_{dlin}, g_m, R_{on} and

R_{over} are exceeded by the degradation in the noise components. In addition to that, the degradation in the noise components shows a sharp increase at quite early stages of DC stressing (Figure 3-15). The advantage of lifetime prediction using LFN data is that the degradation is very high compared to I_{dlin} or R_{on} degradation and the effect is so pronounced that it is manifested within a few hundreds of seconds of stressing.
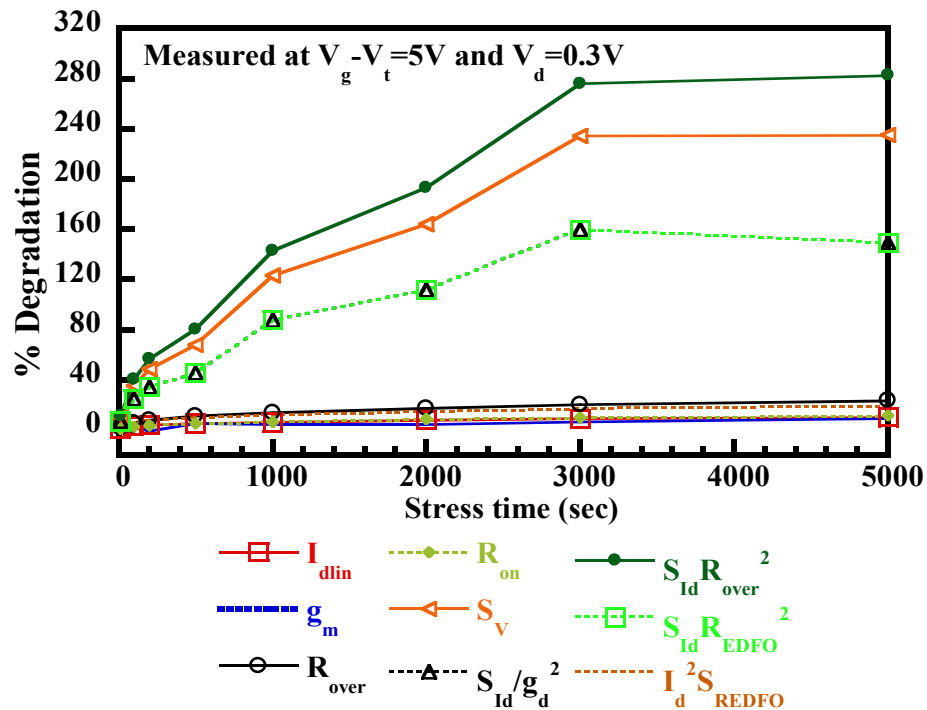
Figure 3-15 Early degradation of noise parameters compared to the DC parameters. The 30 V device was stressed at V_g =4 V and V_d =30 V. All the noise components except $I_d^2 S_{R_{ED_{FO}}}$ show much higher degradation and this effect is reflected right from the beginning of stressing. Highest degradation is in $S_{I_d} R_{over}^2$ component. Similar results were obtained on other different-rated LDMOS devices.

As shown in Figure 3-15, for a 30 V device stressed at V_g =4 V and V_d =30 V, once we know the standard failure criterion, which is typically taken as 10% R_{on} degradation, we can extrapolate the lifetime from % R_{on} degradation curve. From that lifetime, we can do a power fitting for % S_V degradation curve at very low stressing times (10-1000 sec). Any other 30 V devices can be predicted as to eventually fail if that device shows % S_V degradation with a steeper slope than the benchmarked device for low stressing time. In other words, if the percentage noise degradation of the tested device exceeds this safe limit determined from the benchmarked device, it cannot be accepted as reliable. This early failure analysis procedure can be very effective as it is fast and nondestructive [52].

3.9 Conclusion

A systematic experimental study on the low frequency noise characteristics of RESURF LDMOS devices with different voltage rating has been performed. A unique method to distinguish the noise contributors and their effects in LDMOS has been explored and explained. A simple diagnostic tool of *1/f* noise measurements is implemented to assess the location and mechanism for degradation due to DC stressing in RESURF LDMOS devices. Significant trapped carrier fluctuations at the Si-SiO$_2$ interface are found in both the channel and gate-oxide overlap region. When measured at higher transverse fields, the experimental results point to more pronounced *1/f* noise degradation in the overlap region rather than the channel side. The bulk resistance fluctuation under the field oxide is found to be much lower than the gate overlap region. We also have shown that the relative percentage of degradation with stressing time in *1/f* noise is much higher and occurs much earlier than that for the DC parameters.

57

Chapter 4

LDMOS Low Frequency Noise Modeling

4.1 Introduction

1/f noise observed on differently processed high power, RESURF LDMOS transistors has been correlated with degradation in the drain current and transconductance induced by DC stressing. It has been found that the LDMOS does not follow conventional CMOS noise models due to asymmetric extended drain. Therefore, a physics-based model has been implemented to describe the low-frequency noise behavior in differently processed LDMOS devices. The developed model is based upon correlated carrier number and mobility fluctuation theory, also known as the Unified *1/f* Noise Model (UNM), which has been modified to account for the fluctuations in the extended drain and the channel. Unlike the Unified *1/f* Noise Model, non-uniform trap distribution has been taken into account with respect to position in the gate oxide and band-gap energy. The model is experimentally verified to identify the physical mechanisms for degradation due to stressing. Interface trap density as well as effective oxide trap density was calculated from the developed model. Observations from some recent approaches on LDMOS noise modeling are also highlighted here. Although the investigation is limited to linear region of operation, a discussion is provided at the end, on the findings of noise behavior in the saturation region.

4.2 *1/f* Noise Theories for Conventional MOS Devices

The origin of *1/f* noise has been a question for debate over the years. The first noise theory was developed by McWhorter in 1956, which was based on carrier number fluctuation due to capture and emission of charge carriers by oxide traps [53, 54]. Then another school of thought came into light in 1978 by F. N. Hooge *et. al.* [54], who

described noise as an outcome of bulk mobility fluctuation due to Coulombic scattering. Later on, a more widely accepted noise model for conventional MOSFETs was developed by K. Hung *et. al.* [49], which showed a correlation of carrier number fluctuation with the mobility fluctuation. This theory is known as the Unified *1/f* Noise Model.

According to Hooge's theory, lattice scattering is responsible for mobility fluctuations, leading to the drain current PSD for *1/f* noise (S_{I_d}) expressed as:

$$\frac{S_{I_d}}{I_d{}^2} = \frac{\alpha_H}{fWL_c N_c} \tag{4.1}$$

where α_H is known as the Hooge parameter, L_c is the channel length, W is the device width and N_c is the inversion carrier density per unit area in the channel. In the original derivation, α_H was found to be a fixed number (2×10^{-3}). This was then modified to take the effect of crystal quality and phonon scattering using:

$$\alpha_H = 2 \times 10^{-3} \left(\frac{\mu_c}{\mu_{latt}} \right)^2 \tag{4.2}$$

where, lattice scattering-limited mobility is defined as μ_{latt} and effective channel mobility is expressed as μ_c. A simplified expression for the Hooge's model is:

$$S_{I_d}(f) = \frac{\alpha_H q \mu_{eff} I_d V_d}{fL_c{}^2} \tag{4.3}$$

This expression reveals that the noise is severely impacted by the channel length reduction (inversely proportional to $L_c{}^2$), as well as increase in the drain current. Hooge's

model is known to be mainly applicable in case of noise in PMOS devices or in metals and bulk materials [55]. Since we modeled *1/f* noise in LDMOS with the context of the Unified *1/f* Noise Model, this theory is explained in detail in the next subsection.

4.3 The Unified *1/f* Noise Model

The general drain current formulation in a conventional MOSFET, which does not have an extended drain, can be written as:

$$I_d = W\mu_c(qN_c)E_x \tag{4.4}$$

where E_x is the electric field along the lateral direction. Then the resulting drain current fluctuation in the channel can be expressed, as was developed in the original Unified *1/f* Noise Model [49]:

$$\frac{\delta I_d}{I_d} = -\left[\left(\frac{1}{\Delta N_c}\frac{\delta\Delta N_c}{\delta\Delta N_{ot_c}} \pm \frac{1}{\mu_c}\frac{\delta\mu_c}{\delta\Delta N_{ot_c}}\right)\delta\Delta N_{ot_c}\right] \tag{4.5}$$

where, $\Delta N_c = N_c W \Delta x_c$ and, $\Delta N_{ot_c} = N_{ot_c} W \Delta x_c$. N_c is the channel carrier density and N_{ot_c} is the number of occupied traps per unit area. The ± sign in front of the mobility fluctuation term depends on the type of traps, whether donor or acceptor. A positive sign is applied, if the traps are charged after they capture electrons. The opposite sign applies if the traps become neutral after capturing charge carriers. Since, all our measurements were done in strong inversion region, the ratio of fluctuations in the number of carriers to that in the number of occupied traps in the gate oxide above the channel can be considered to be unity. Then to find out $\delta\mu_c/\delta\Delta N_{ot_c}$ term, the following expression is utilized [49]:

$$\frac{1}{\mu_c} = \frac{1}{\mu_{others}} + \frac{1}{\mu_{ox}} = \frac{1}{\mu_{others}} + \alpha_c N_{ot_c} \qquad (4.6)$$

where, α_c is the screened scattering coefficient, which is a bias dependent parameter, is μ_{ox} the mobility due to oxide charge scattering, and μ_{others} is the mobility due to other scattering effects associated in the carrier transport. The rate of change for the channel mobility can be expressed as: $\delta\mu_c / \delta N_{ot_c} = \alpha_c \mu_c^2$ and the Equation (4.5) becomes:

$$\frac{\delta I_{d_c}}{I_d} = -\left(\frac{1}{N_c} \pm \alpha_c \mu_c \right) \frac{\delta \Delta N_{ot_c}}{W \Delta x_c} \qquad (4.7)$$

Therefore, for an unstressed (fresh) device, the power spectral density for the localized channel carrier (in inversion) fluctuations can then be expressed from Equation (4.7) as:

$$S_{\Delta I_{d_c}}(x, f) = \left[\frac{I_d}{W \Delta x_c} \left(\frac{1}{N_c} \pm \alpha_c \mu_c \right) \right]^2 S_{\Delta N_{t_c}}(x, f) \qquad (4.8)$$

where, $S_{\Delta N_{t_c}}(x, f)$ is the PSD of the fluctuations in the number of the occupied traps over the area $W \Delta x_c$ in the channel. From a different perspective, the normalized drain current PSD (S_{I_d}) can also be written in terms of flat-band voltage fluctuations ($S_{V_{fb}}$). The fluctuations in the flat-band voltage can be expressed as [56]:

$$\delta V_{fb} = \frac{\delta Q_t}{W L_c C_{ox}} \qquad (4.9)$$

where Q_t is the oxide trap charge. The drain current fluctuation can then be written, when mobility fluctuation is considered along with the flat-band voltage fluctuation, as [56]:

61

$$\delta I_d = \delta V_{fb} \left. \frac{\partial I_d}{\partial V_{fb}} \right|_{\mu_c = \text{const}} + \delta \mu_c \left. \frac{\partial I_d}{\partial \mu_c} \right|_{V_{fb} = \text{const}} \tag{4.10}$$

Now, we express the channel mobility as: $1/\mu_c = \alpha_c Q_t + 1/\mu_{c0}$, where μ_{c0} is a fitting parameter, which can either be a constant or can be dependent on the N_c, electric field, or V_g [56]. Then, we can write the mobility fluctuations as: $\delta \mu_c = -\alpha \mu_c^2 \delta Q_t$. Therefore, from the linear region drain current expression: $I_d = (W/L_c)\mu_c C_{ox}(V_g - V_t)V_d$ and considering $\partial I_d / \partial V_{fb} = -\partial I_d / \partial V_g$, the drain current fluctuation can be written as:

$$\delta I_d = -g_m \delta V_{fb} \pm \alpha_c I_d \mu_c \delta Q_t \tag{4.11}$$

The normalized drain current fluctuation is then written by combining equations (4.9)-(4.11) as:

$$\frac{\delta I_d}{I_d} = -\left[1 \pm \alpha_c \mu_c \frac{\delta Q_t}{\delta V_{fb}} \frac{I_d}{g_m} \right] \left(\frac{g_m}{I_d} \right) \delta V_{fb} \tag{4.12}$$

Hence, the normalized spectral density of the drain current can be expressed as:

$$\frac{S_{I_d}}{I_d^2} = \left[1 \pm \alpha_c \mu_c C_{ox} \frac{I_d}{g_m} \right]^2 \left(\frac{I_d}{g_m} \right)^2 S_{V_{fb}} \tag{4.13}$$

According to the above expression, the drain current normalized *1/f* noise near the gate oxide-Si interface (S_{I_d}/I_d^2), should follow $(g_m/I_d)^2$ for all $V_g - V_t$ in linear operation for the Unified *1/f* Noise Model to be applicable.
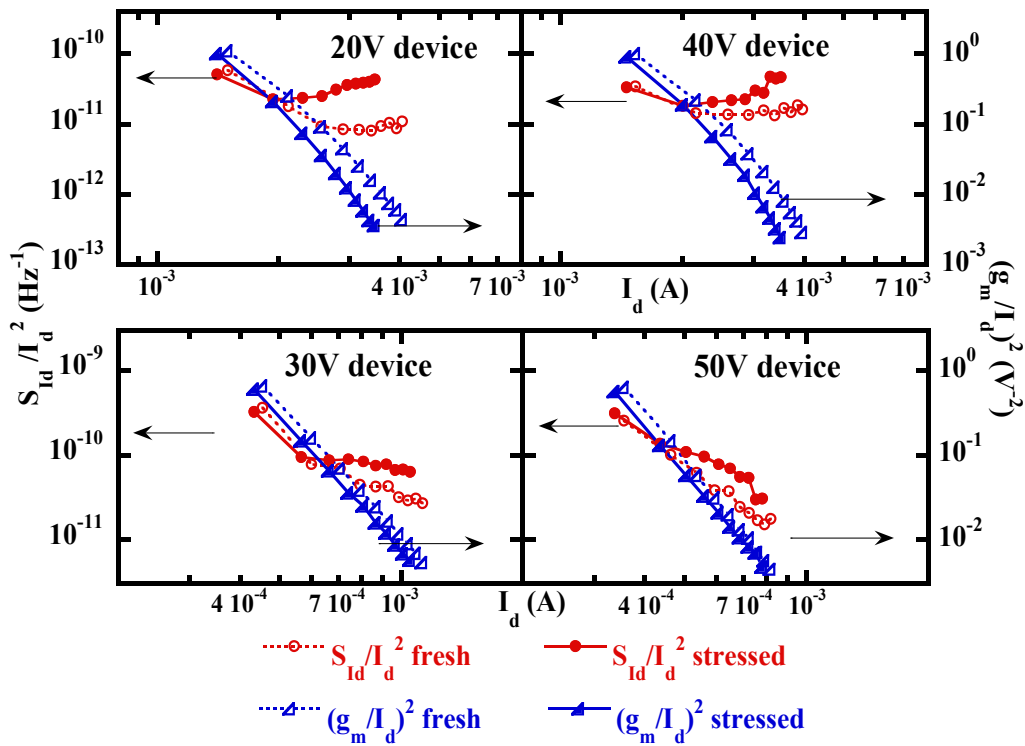
Figure 4-1 Drain-current normalized S_{I_d} vs. drain-current normalized transconductance to verify the Unified *1/f* Noise Model in different rated devices. Stress conditions are: for 20 V device V_g =5 V and V_d =22 V; for 30 V device V_g =5 V and V_d =30 V; for 40 V device V_g =4 V and V_d =40 V and for 50 V device V_g =4 V and V_d =53 V.

4.4   Unified *1/f* Noise Model Verification for LDMOS

For conventional CMOS, correlated carrier number and surface mobility fluctuation theory has been the most successful model. It is based on trapping-detrapping of free carriers in the channel by gate-dielectric traps as the main source of current fluctuations. However, as depicted in Figure 4-1, none of the devices before or after hot

carrier stress follows the model exactly. For low gate biases, S_{I_d}/I_d^2 is consistent with this behavior, but deviates from $(g_m/I_d)^2$ at high gate biases, as the extended drain gate-overlap region fluctuations become dominant over those coming from the channel. Therefore, the conventional Unified Model is not able to account for the observed noise in LDMOS, and the fluctuations in the extended drain also need to be taken into account. The Hooge's model also does not apply here, as S_{I_d}/I_d^2 does not follow $(1/I_d)$ characteristics [57-59].

4.5 Origin of Deviation from the Unified *1/f* Noise Model

When the Unified *1/f* Noise Model is applied to asymmetrical LDMOS devices, noticeable discrepancies are found as shown in the preceding section. The extended drain has been observed to be very instrumental in causing trap-assisted degradation and eventually the worst degradation is found in the gate-overlap region in the extended drain where accumulation of majority carriers takes place. This impact of stressing can be more conceivable if we analyze Figure 4-2, where the most important parameter associated with LDMOS oxide reliability and degradation is portrayed.

This clearly suggests that a simple resistance degradation model as depicted by many authors [1, 3, 25, 27], alone will not be sufficient to investigate the complete degradation behavior of LDMOS devices, especially because of the gate oxide-overlap region, for which one needs to incorporate the impact of trap assisted drain current fluctuations in the gate oxide. Therefore, we have completely modeled the current fluctuation (S_{I_d}) from weak accumulation (dominated by channel noise) to strong accumulation (gate overlap fluctuation dominated region) before and after stress using

modified Unified *1/f* Noise Model approach. Unlike the original model, in this theoretical

framework, we considered nonlinear trap distribution along the oxide with respect to

energy, band bending and distance into the oxide [60].
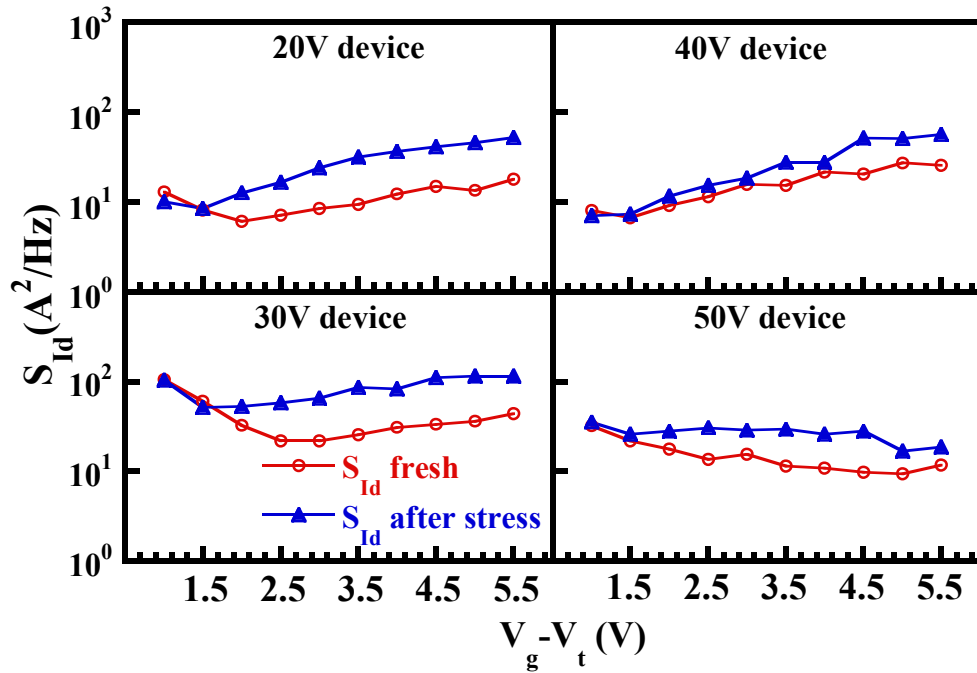
Figure 4-2 The trend of S_{I_d} fluctuation is highlighted before and after 5,000 sec stress. In

each case, S_{I_d} does not show any degradation with stress at low gate voltages, where

the fluctuations of carriers at the channel Si-SiO$_2$ interface dominate. At higher gate

overdrives, where the fluctuations at the Si-SiO$_2$ interface of the extended drain gate-

overlap region dominate, considerable increase in noise is observed due to stress. Once

again the vertical scale is arbitrarily chosen.

4.6   Development of New LDMOS Noise Model

Aforementioned analysis corroborates that the LDMOS channel plays less important role in determining the device degradation in linear region operation. It should be apparent by the discussions in the previous chapter that LDMOS lifetime is mostly dependent on the degradation of gate-overlap region and is related to increase in current fluctuation (due to oxide trap formation) with stress. Since these two effects are complimentary, their correlation can be modeled as follows.

The total current fluctuation S_{I_d} can be considered as the summation of the local carrier fluctuations from the channel $S_{\Delta I_{d_c}}$, the extended drain under the gate-oxide overlap $S_{\Delta I_{d_{ov}}}$ and that under the field oxide $S_{\Delta I_{d_{FO}}}$ as:

$$S_{I_d}(x,f) = \frac{1}{L_c^2}\int_0^{L_c} S_{\Delta I_{d_c}}(x,f)\Delta x_c dx_c + \frac{1}{L_{ov}^2}\int_0^{L_{ov}} S_{\Delta I_{d_{ov}}}(x,f)\Delta x_{ov} dx_{ov}$$
$$+ \frac{1}{L_{ED_{FO}}^2}\int_0^{L_{ED_{FO}}} S_{\Delta I_{d_{FO}}}(x,f)\Delta x_{ED_{FO}} dx_{ED_{FO}}$$

(4.14)

where, L_c, L_{ov} and $L_{ED_{FO}}$ are the length of channel, gate-overlap and field oxide region respectively. x_c is the distance from the source to the channel, and x_{ov} is from the channel/drain junction to the gate-overlap region, and $x_{ED_{FO}}$ is that from the bird's beak to the drain contact. The carriers flow close to the interface in the channel and in the gate overlap, which then spreads out under the field oxide region by RESURF or double RESURF action [31] and thus, increase the device voltage handling capability. Therefore, no significant gate-bias induced fluctuation can occur in presence of the thick bird's beak shaped field oxide, which provides isolation from gate controlled carrier trapping-

detrapping at the Si-SiO$_2$ interface. The generated fluctuations due to $S_{\Delta I_{d_c}}$ and $S_{\Delta I_{d_{ov}}}$ contribute to additional induced voltage fluctuations under the field oxide ($S_{I_d} R^2_{ED_{FO}}$). Therefore, we neglected the contribution of the last term in Equation (4.14). Then, we consider that the fluctuations in the channel and the overlap region are not correlated as their relative Fermi level positions are different, as shown in Figure 4-3.
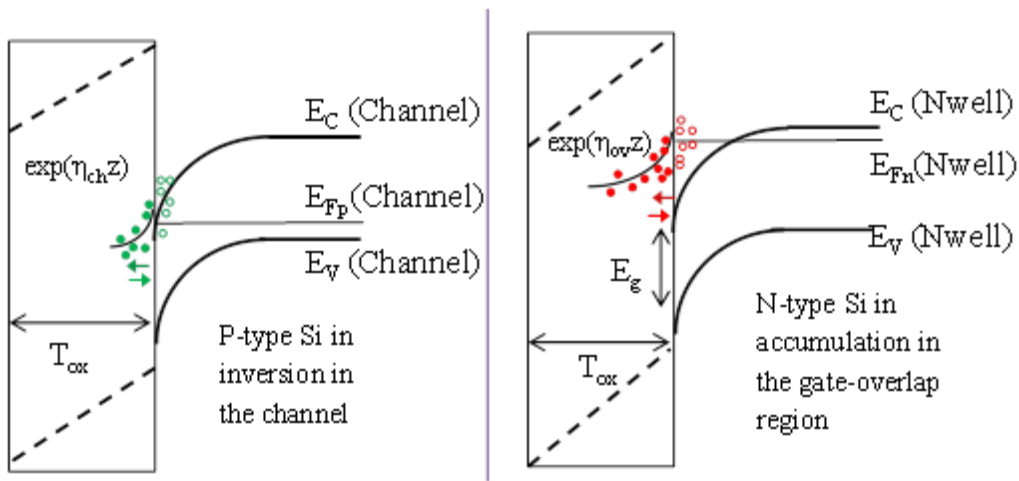
Figure 4-3 Energy-band diagrams for the channel at inversion and for the gate-overlap at strong accumulation, respectively. Only the traps within the quasi-Fermi level in each region are active to contribute to trapping-detrapping of charge carriers from the surface.

4.6.1 1/f Noise in the Channel

For conventional MOSFETs or in advanced high-κ devices, hot-carrier induced interface state generation is known to be the dominant source of degradation with stress [57-59]. The channel noise dominated part of the normalized noise PSD has been shown to follow the Unified *1/f* Noise Model at low gate voltages in Figure 4-1. However, we did not look into the dominant noise mechanisms when channel noise is the highest

contributor, as this noise component does not degrade over time with stressing (as was shown in Figures 3-11 and 3-12). It has been reported by other researchers that carrier number fluctuation dominates over mobility fluctuation in this case [32]. Nevertheless, although LDMOS contains a double diffused channel, as discussed above the degradation in the gate overlap region of the extended drain exceeds that in the channel. Hence, we concentrated primarily on modeling of noise and degradation in the extended drain gate-overlap region in the following subsection.

4.6.2 1/f noise in the Gate-Overlap Region

Since we assumed that oxide trap occupancy fluctuation is primarily due to the carrier number and surface mobility fluctuations, and the fluctuations in the channel and in the extended drain are independent (the fluctuation terms can be added linearly), a similar expression to that of Equation (4.5) can be written for the fluctuations in the overlap region:

$$\frac{\delta I_d}{I_d} = -\left(\frac{1}{N_{ov}} \pm \alpha_{ov}\mu_{ov} \right) \frac{\delta \Delta N_{ot_{ov}}}{W \Delta x_{ov}}$$

(4.15)

Here, $\Delta N_{ov} = N_{ov}W\Delta x_{ov}$ and $\Delta N_{ot_{ov}} = N_{ot_{ov}}W\Delta x_{ov}$. N_{ov} is the accumulation carrier density in the gate-overlap region and $N_{ot_{ov}}$ is the number of occupied traps per unit area in the gate oxide above that region. Adopting the same physical explanations and assumptions that were made while developing the expression (4.7), an identical formulation to that of Equation (4.7) for the gate overlap region can be written as:

$$\frac{\delta I_d}{I_d} = -\left[\left(\frac{1}{\Delta N_{ov}} \frac{\delta \Delta N_{ov}}{\delta \Delta N_{ot_{ov}}} \pm \frac{1}{\mu_{ov}} \frac{\delta \mu_{ov}}{\delta \Delta N_{ot_{ov}}} \right) \delta \Delta N_{ot_{ov}} \right]$$

(4.16)

At high $(V_g - V_t)$'s, the overlap region is in strong accumulation and the trapped carrier fluctuation can be considered to be equal to fluctuations of the free carriers in the overlap region, just like in the case of channel noise. Following the Mattheisen's rule, as was described by Equation (4.6), we can write: $\delta\mu_{ov}/\delta N_{ot_{ov}} = \alpha_{ov}\mu_{ov}^2$ for the overlap region, where α_{ov} is the screened scattering coefficient for the overlap region. From [61, 62] and [62], we can take $\alpha_{ov} = 1/\mu_{c0_{ov}}\sqrt{N_{ov}}$ for NWell overlap region (in strong accumulation), with $\mu_{c0_{ov}}$ being the mobility fluctuation fitting parameter. Then, for an unstressed device, we write the power spectral density for the localized majority carrier (in accumulation) fluctuations, by following the Equation (4.8) as [49]:

$$S_{\Delta I_{d_{ov}}}(x,f) = \left[\frac{I_d}{W\Delta x_{ov}}\left(\frac{1}{N_{ov}} \pm \alpha_{ov}\mu_{ov}\right)\right]^2 S_{\Delta N_{t_{ov}}}(x,f) \qquad (4.17)$$

where, $S_{\Delta N_{t_{ov}}}(x,f)$ is the PSD of the fluctuations in the number of the occupied traps over the area $W\Delta x_{ov}$ in the gate-overlap region $S_{\Delta N_{t_{ov}}}(x,f)$ can be expressed as the summation of all the Lorentzian spectra (generation-recombination noise) generated at the Si-SiO$_2$ interface as [49]:

$$S_{\Delta N_{t_{ov}}}(x,f) = \int_{E_V}^{E_C}\int_0^W\int_0^{T_{ox}} 4N_{t_{ov}}(E,x,y,z)(1-f_t)f_t\Delta x_{ov}\frac{\tau(E,x,y,z)}{1+\omega^2\tau^2(E,x,y,z)}dEdydz \quad (4.18)$$

Here, $f_t = \left[1/\left(1+\exp[(E-E_{f_{ov}})/kT]\right)\right]$ is the trap occupancy function in the overlap region with $E_{f_{ov}}$ (eV) as the quasi-Fermi level for electrons. $\tau(E,x,y,z)$ is the trapping time constant in the gate dielectric for a trap located at x, y, z coordinates and at

energy E. Considering constant energy tunneling of the accumulated carriers analogous to channel carriers as in the case for CMOS [49, 57-59], we can take $\tau = \tau_0 \exp(\gamma z)$, where $\tau_0 = 10^{-10}$ sec is the characteristic time constant and $\gamma = 1 \times 10^8$ cm^{-1} is the tunneling coefficient for SiO$_2$ gate dielectric. Since the fluctuations near the quasi-Fermi level for electrons contribute most to the fluctuations due to the delta-function-like behavior of $(1-f_t)f_t$, the energy integral can be approximated as:

$$\int_{E_V}^{E_C} N_{t_{ov}}(E,x,y,z)(1-f_t)f_t \ dE \approx k_B T N_{t_{ov}}(E_{f_{ov}},z) \qquad (4.19)$$

We can now simplify Equation (4.18) by approximating that the fluctuations along the device width remain unchanged:

$$S_{\Delta N_{t_{ov}}}(x,f) = 4k_B TW \int_0^{T_{ox}} N_{t_{ov}}\left(E_{f_{ov}},x,z\right)\Delta x_{ov} \frac{\tau(E_{f_{ov}},x,z)}{1+\omega^2\tau^2(E_{f_{ov}},x,z)} dz \qquad (4.20)$$

The above expression is based upon the assumption that the trap density is uniform throughout the gate dielectric, as described in the original UNM.

4.6.3 Modification to the Existing Unified Noise Model

The conventional Unified *1/f* Noise Model assumes traps to be spatially uniformly distributed and constant with respect to energy. A modification to this concept was then suggested in [60] to account for a more realistic distribution, where non-linearity due to energy, band-bending and spatial variation is taken into account. This modified approach was shown to accurately describe the trap characteristics in conventional as well as in high-κ MOSFETs [57-59]. Therefore, we adopted the modified approach of Unified *1/f*

Noise Model in our analysis to extract the effective oxide trap density in the gate-overlap area as:

$$N_{t_{ov}}(E_{f_{ov}}, z) = N_{t0_{ov}} \exp[\xi_{ov}(E_{f_{ov}} - E_i) + \eta_{ov}z +$$
$$(q\lambda_{ov}(V_g - V_{ch} - V_{ov}x_{ov}/L_{ov})/T_{ox})z]$$

(4.21)

where ξ_{ov} (eV^{-1}), η_{ov} (cm^{-1}) and λ_{ov} (eV^{-1}) are process dependent fitting parameters that represent the energy distribution of the trap density, spatial variation and the modification caused by energy band bending respectively [60]. A typical energy distribution plot by using Equation (4.21) is shown in Figure 4-4. $N_{t0_{ov}}$ is the mid band-gap trap density at the interface (z =0), E_i is the midgap energy, and V_{ch} is the voltage drop across the channel measured from the source. The mid-gap trap density, $N_{t0_{ov}}$ can be either due to family of dangling bond centers (P_b centers) protruding into the mid-energy gap region or because of U-shaped energy continuum of band-edge states [63, 64]. Since the traps at mid-gap are not active, and do not contribute to the trapping-detrapping, $N_{t0_{ov}}$ is nothing more than a process and technology dependent fitting parameter. The exponential energy distribution parameter is ξ_{ov}. The second term in (4.21) defines the distance into the oxide, up to where the traps are effective in contributing to the fluctuations. Under strong accumulation, energy bands of both NWell Si and SiO$_2$ bend to compensate for the vertical field. This is accounted by the last term in Equation (4.21).
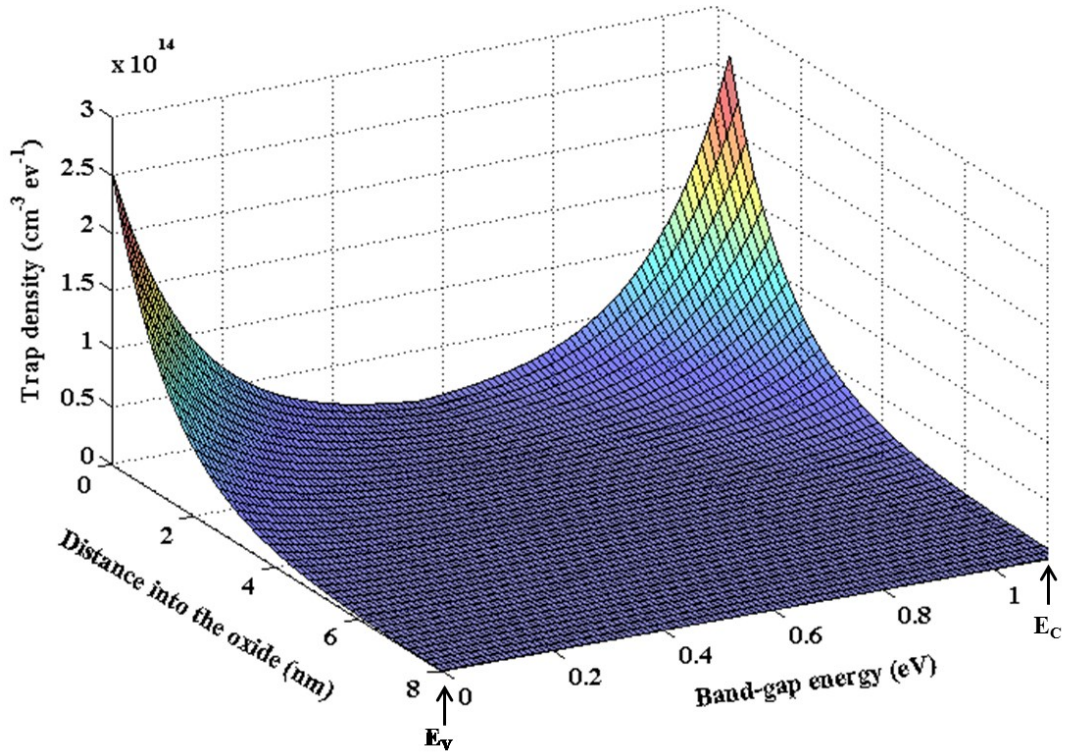
Figure 4-4 A 3-D representation of the oxide trap density for the overlap region plotted as
a function of energy and distance into the oxide using Equation (4.21). Energy is
measured from the valence band (E =0 at E_V of Si). $N_{ot_{ov}}$, η_{ov} , λ_{ov} ,and ξ_{ov} are chosen
as 6.1x10^{12} (cm^{-3} eV^{-1}), -1.91x10^{7} cm^{-1}, 7.3 eV^{-1} and 7.3 eV^{-1}, respectively for this plot.

4.6.4 Proposed Functional Form of LDMOS Noise Model

Defining $\beta_{ov} = q\lambda_{ov} / T_{ox}$ and $V'_{ov} = V_g - V_{ch} - V_{ov}x_{ov} / L_{ov}$, and then applying the
terms in Equation (4.21) to Equation (4.20) we get:

$$S_{\Delta N_{t_{ov}}}(x,f) = 4k_B TW\Delta x_{ov}\left[\begin{array}{c} N_{to_{ov}}\exp[\xi_{ov}(E_{f_{ov}}-E_i)] \\ \times\displaystyle\int_0^{T_{ox}}\dfrac{\exp\left\{\left(\beta_{ov}V_{ov}'+\eta_{ov}\right)z\right\}\tau}{1+\omega^2\tau^2}dz \end{array}\right] \qquad (4.22)$$

By defining the corresponding parameters and appropriate symbols, we can derive a similar kind of expression for the fluctuation in the channel. For simplicity, we are not showing that derivation. Since the same gate oxide extents over the channel and the overlap region, τ_0 and γ will remain the same for the LDMOS channel. The total drain current noise PSD (S_{I_d}) at high gate biases is derived from Equation (4.14) using the above trap density and tunneling considerations in Equations (4.20) and (4.21) and by putting $\omega\tau = u$ and $\exp\left(\beta_{ov}V_{ov}'z+\eta_{ov}z\right) = \left(\tau/\tau_0\right)^{\left(\beta_{ov}V_{ov}'+\eta_{ov}\right)/\gamma}$ for the integral in Equation (4.22), for the high gate bias portion of the operation as:

$$S_{I_d}(x,f) = \dfrac{4k_B TI_d^{\,2}}{W}\left[\left\{\begin{array}{c}\displaystyle\int_0^{L_{ov}}\dfrac{N_{t0_{ov}}\exp[\xi_{ov}(E_{f_{ov}}-E_i)]}{L_{ov}^{\,2}\gamma(\tau_0)^{\left(\beta_{ov}V_{ov}'+\eta_{ov}\right)/\gamma}(\omega)^{\left(\beta_{ov}V_{ov}'+\eta_{ov}\right)/\gamma+1}} \\[4mm] \left(\dfrac{1}{N_{ov}}+\alpha_{ov}\mu_{ov}\right)^2\displaystyle\int_{\omega\tau_0}^{\omega\tau_0\exp(\gamma T_{ox})}\dfrac{u^{\left(\beta_{ov}V_{ov}'+\eta_{ov}\right)/\gamma}}{1+u^2}du\end{array}\right\}dx_{ov}\right] \qquad (4.23)$$

where $\delta = \left(\beta_{ov}V_{ov}'+\eta_{ov}\right)/\gamma+1$, which accounts for the gate bias dependence of the frequency exponent due to non-uniform trap distribution and hence, modifies *1/f* noise PSD into *1/f $^\delta$* spectrum. The final functional form for *1/f* noise, considering all the noise sources including all the individual regions, thus becomes:

$$S_{I_d}(x,f) = \frac{4kTI_d^{\ 2}}{W} \left[\begin{array}{c} \left\{ \begin{array}{c} \displaystyle\int_0^{L_c} \frac{N_{t0_c}\exp[\xi_c(E_{f_c}-E_i)]}{L_c^{\ 2}\gamma(\tau_0)^{\left\{\left(\beta_c V_c'+\eta_c\right)/\gamma\right\}}(\omega)^{\left(\beta_c V_c'+\eta_c\right)/\gamma+1}} \\ \left(\frac{1}{N_c}+\alpha_c\mu_c\right)^2 \displaystyle\int_{\omega\tau_0}^{\omega\tau_0\exp(\gamma T_{ox})} \frac{u^{\left(\beta_c V_c'+\eta_c\right)/\gamma}}{1+u^2}du \end{array} \right\} dx_c + \\[4em] \left\{ \begin{array}{c} \displaystyle\int_0^{L_{ov}} \frac{N_{t0_{ov}}\exp[\xi_{ov}(E_{f_{ov}}-E_i)]}{L_{ov}^{\ 2}\gamma(\tau_0)^{\left(\beta_{ov}V_{ov}'+\eta_{ov}\right)/\gamma}(\omega)^{\left(\beta_{ov}V_{ov}'+\eta_{ov}\right)/\gamma+1}} \\ \left(\frac{1}{N_{ov}}+\alpha_{ov}\mu_{ov}\right)^2 \displaystyle\int_{\omega\tau_0}^{\omega\tau_0\exp(\gamma T_{ox})} \frac{u^{\left(\beta_{ov}V_{ov}'+\eta_{ov}\right)/\gamma}}{1+u^2}du \end{array} \right\} dx_{ov} \end{array} \right] \qquad (4.24)$$

For low gate bias, the first term (channel noise) in Equation (4.24) will dominate. For modeling the noise dominated by the gate-overlap portion, we can simply consider the expression in (4.23), when the vertical electric field is higher.

4.7   LDMOS Noise Model Implementation and Verification

4.7.1 Extraction of Noise Model Parameters

The developed model for drain current fluctuations in the overlap region is significantly different from the original Unified *1/f* Noise Model as we incorporated bias dependence and spatial variation of traps. By knowing the channel voltage drop (V_{ch}) from DC I-V characteristics at low drain biases, accumulation layer carrier density (N_{ov}) in the overlap region was approximated using $qN_{ov} \approx C_{ox}(V_g - V_{ch})$. λ_{ov} and η_{ov} were

extracted by plotting the frequency exponent (δ) vs. $V_g - V_{ch}$ in the frequency range of 1 –

100 Hz for different stressing times as shown in Figure 4-5. Then, using these

parameters, the noise magnitude $S_{I_d}(1Hz)$ was fitted with the experimental results by

varying the rest of the fitting parameters $N_{t0_{ov}}$, ξ_{ov} and $\mu_{c0_{ov}}$ (Figure 4-6). Excellent

agreement has been obtained between the model predictions and the experimental

values for all the LDMOS devices before stress and with the progression of stressing

time. It should be noted that η_{ov} was always found to be negative in all unstressed and

stressed devices suggesting effective trap density to decrease exponentially into the

oxide, as is the case in conventional and high-κ devices [57-60]. The positive sign of ξ_{ov}

confirms that the trap energy and consequently the trap density increases as the quasi-

Fermi level for electrons approaches towards the conduction band edge of NWell (Si).

Finally, the positive sign for λ_{ov} irrespective of the stressing time implies that the

accumulation layer carriers tunneling at a constant energy into the dielectric experience

greater trap density, which is the consequence of band-bending due to gate bias.

For low gate biases, $S_{I_d}(1Hz)$ is in agreement with the original Unified *1/f* Noise

Model as was already depicted in Figure 4-1. Therefore, the model in Equation (4.24)

completely describes the noise behavior of RESURF LDMOS devices regardless of the

processing variation and the operation voltage.
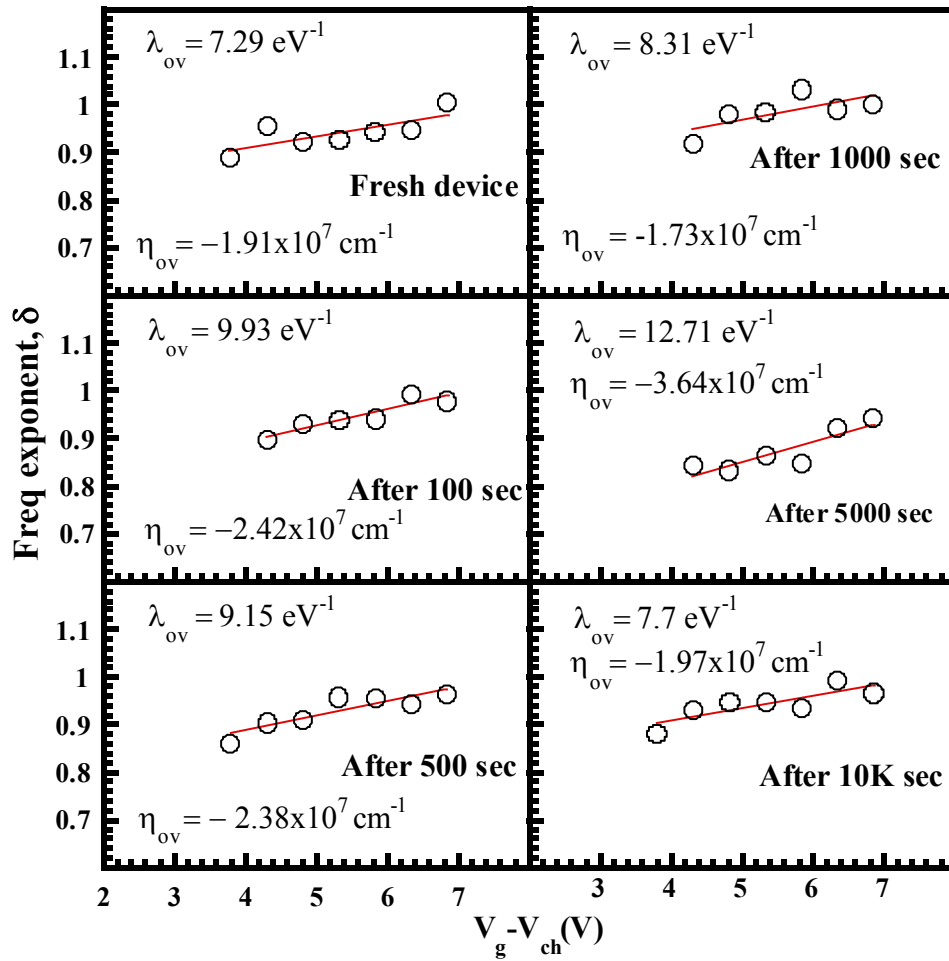
Figure 4-5 The experimental values of frequency exponent δ plotted as a function of gate

bias. The device was stressed at V_g =4 V and V_d =40 V for 10,000 sec. From a linear

fitting for each different stress time, λ_{ov} and η_{ov} parameters are obtained.
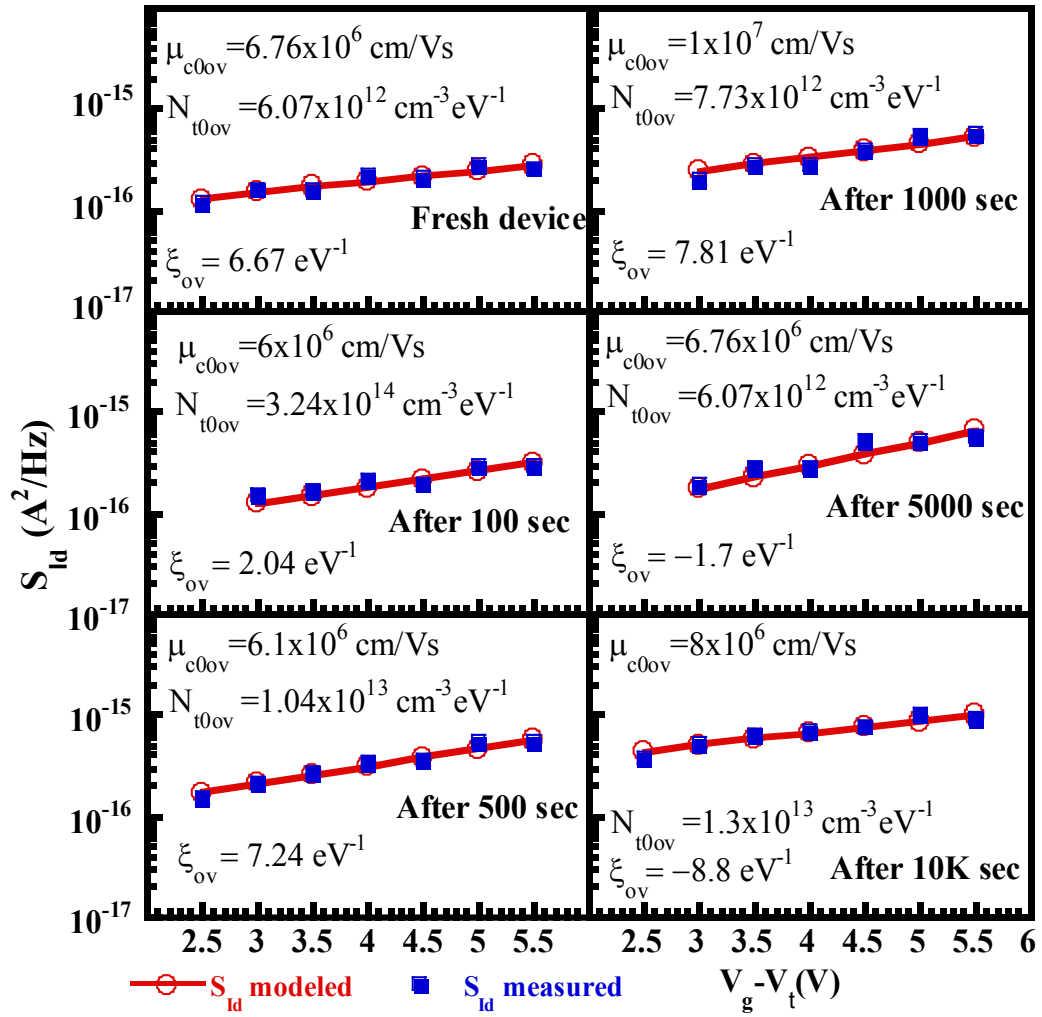
Figure 4-6 Verification of the proposed noise model at high gate biases with the S_{I_d} at 1 Hz obtained experimentally. The data fitting presented here are for the same 40V device stressed at V_g =4 V and V_d =40 V as in Figure 4-5. Other devices also showed similar behavior.

4.7.2 Number of Fitting Parameters in Noise Modeling

Although it might appear as if there are too many fitting parameters, making the fitting procedure somewhat arbitrary, this is not the case. Here, the measured frequency exponent as well as the noise magnitude is used as data in obtaining the fitting parameters. Typically only the measured noise magnitude is utilized, assuming pure *1/f* noise (δ =1), and two fitting parameters are employed, one related to number fluctuations (such as number of traps) and another one related to correlated mobility fluctuations (such as the screened scattering coefficient). In addition to the noise magnitude, here we use also the measured frequency exponent and its change with respect to the gate bias and stressing time. This gives us two more independent parameters to fit. This is the main reason why we can obtain such detailed information about the location, energy and the stressing behavior of the dielectric traps.

4.7.3 Comparison with Other Existing LDMOS Noise Models

Langevelde *et al.* [50] investigated the *1/f* noise in the saturation region of p-channel DMOS. Mobility fluctuation [54, 65, 66] was reported as the mechanism for *1/f* noise when channel noise dominates at low V_g. When the so-called depletion mode transistor, which we call the overlap region here, dominates, the carrier number fluctuations become important. Our results are restricted to the latter region of operation, and are in line with their conclusions. There are, however, substantial differences in the device geometry and type. The concept of DMOS in Langevelde's paper is similar to our LDMOS. However, our LDMOS is RESURF. We operate our devices in the linear region, while theirs is in saturation. Therefore, although our results corroborate theirs, a direct comparison is not meaningful.
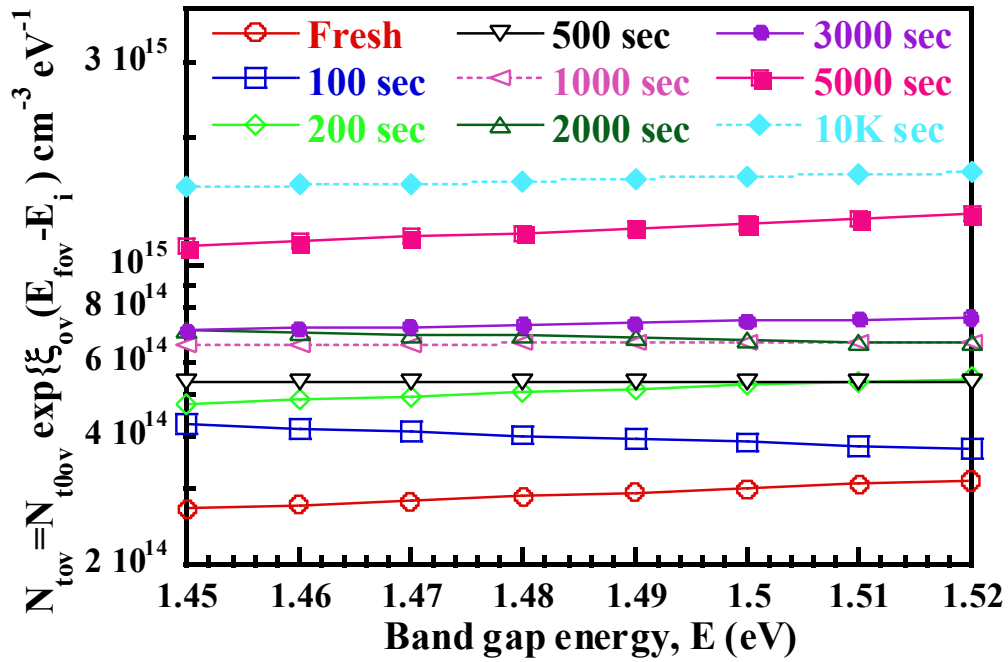
Figure 4-7 Extracted trap density distribution at the Si-SiO$_2$ interface in the gate overlap obtained from the developed LDMOS noise model in a 30 V device stressed at V_g =5 V and V_d =30 V. The quasi-Fermi level sweeps from 1.47~1.50 eV range above the valence band-edge and active traps are located within this range for this device in the experimental conditions.

4.8 Effective Oxide Trap Density Variation with Stressing Time

Figure 4-7 depicts the Si-SiO$_2$ interface (z =0) trap density variation in the gate-overlap region with increase in stressing duration versus band gap energy measured from E_V (Si). Within the quasi-Fermi level sweep range at different gate biases, we observed at least one to two orders of magnitude increase in the active oxide trap density after 10,000 sec of stress. This observation corroborates our findings that the worst

carrier degradation occurs in the overlap region due to increased dielectric trap formation. Nevertheless, the trap density is process and layout dependent. The extracted effective oxide trap density of 1×10^{15} ~1×10^{17} $cm^{-3}eV^{-1}$ for our RESURF LDMOS devices from virgin devices to aged devices is about two orders of magnitude lower than that found (for the active channel) in conventional or high-κ MOSFETs [49, 57-59, 67]. It should be noted, however, a direct comparison is not meaningful between the trap density values extracted for an inverted p-type silicon making up the NMOS channel and the trap density values extracted for a n-type silicon in accumulation, as is the case here, for the gate overlap region.

Figure 4-8 is the 3D graph of the trap density as a function of the electron tunneling distance into the gate oxide in the overlap region and silicon band-gap energy measured from the valence band-edge. There is a clear trend of increase in the oxide trap density at the interface with duration of stress with diminishing effect further in the oxide.

Assuming equi-energy tunneling of carriers into the defect states in the dielectric, ensemble averaging of these microscopic entities gives rise to distribution of wide range of time constants and consequently generates $1/f$ noise in LDMOS. However, one can probe only active traps within $3k_BT$ in energy band around the quasi-Fermi level for electrons, since the traps above or below are either empty or full, respectively and therefore, are mostly ineffective. Figure 4-3 demonstrated the difference of the positions for minority channel carrier Fermi energy level within the band-gap and that for the majority carriers (electron) flowing in the gate-overlap region, which is in accumulation.
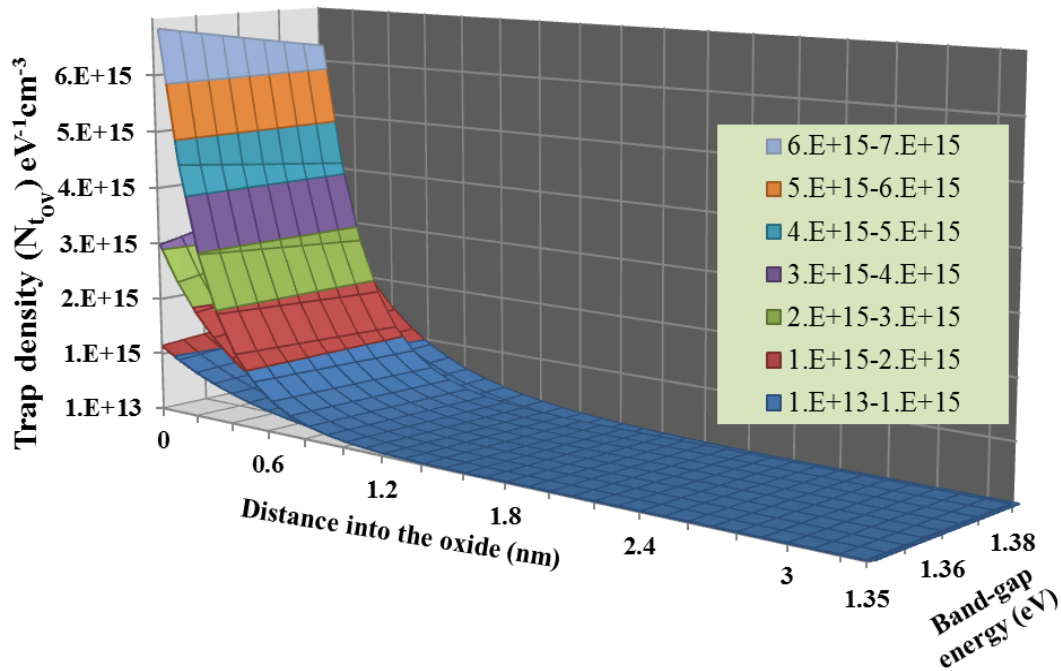
Figure 4-8 The extracted oxide trap density for a 40 V device stressed at V_g =4 V and V_d =40 V before stress and after 500 sec and 3,000 sec stress within the measured frequency range of 1-100 Hz. Horizontal axis shows the distance into the oxide and depth axis shows the corresponding band-gap energy with respect to the valence-band edge. Trap density increases with stressing time for different-rated LDMOS devices. For simplicity, the trap distribution after other stress times are not shown.

A simplified two dimensional view for the effective oxide trap density is portrayed in Figure 4-9 for particular energy (1.471 eV). No noticeable variation in the effective oxide trap density is found at the overlap region Si-oxide interface between the similarly processed devices (30 V and 50 V devices are shown here for example). This is reasonable as they both have the same channel and gate-overlap length (differ in the field oxide size) and are fabricated using the same technology.
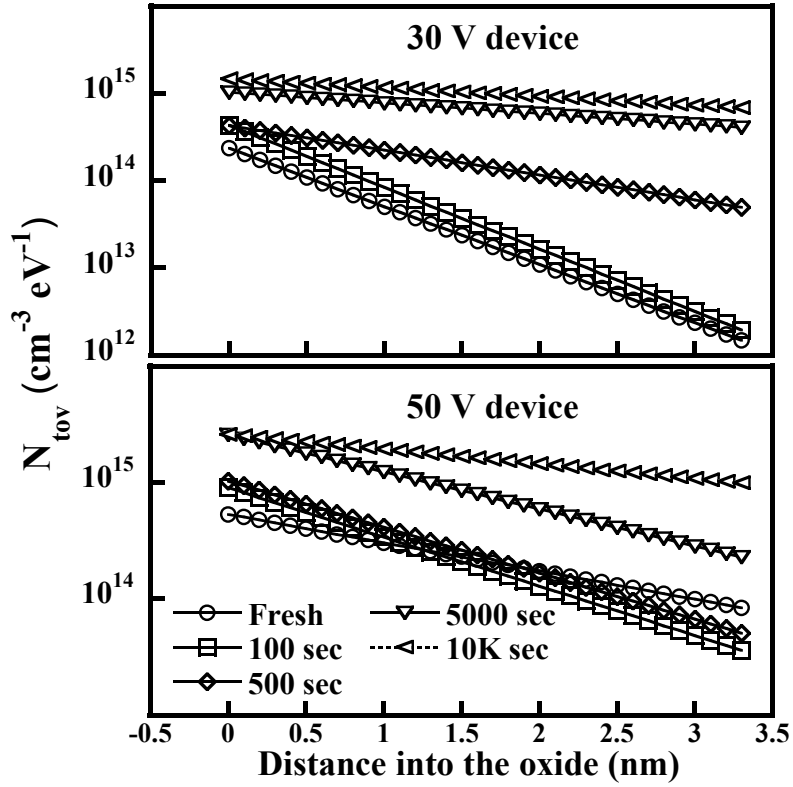
Figure 4-9 Overlap region active oxide trap density at a constant energy of 1.471 eV from

the Si valence band edge for two different devices. Stress conditions are mentioned in

Table 3-1.

4.9 Determination of Interface Trap Density

We can extrapolate the active trap density $N_{it_{ov}}$ at the overlap region oxide-Si

interface by using:

$$N_{it_{ov}} = N_{t0_{ov}} \int_0^{z_{max}} \exp(\eta_{ov} z) dz \int_0^{E_{f max}} \exp\left[\xi_{ov}\left(E_{f_{ov}} - E_i\right)\right] dE \qquad (4.25)$$

where, $z_{\max}$ and $E_{f\max}$ are the maximum spatial distribution of active traps and corresponding energy into the oxide, respectively. Assuming the active traps are within $3k_BT$ around the quasi-Fermi level, we can obtain $N_{it_{ov}}$ to be 8×10^6 cm^{-2} before stress, and that increases to 1×10^8 cm^{-2} after the same device is stressed for 10,000 sec (Figure 4-10). The obtained trap density after stress is at least 2 orders of magnitude lower than the reported trap densities in different LDMOSFETs [30, 64, 68].
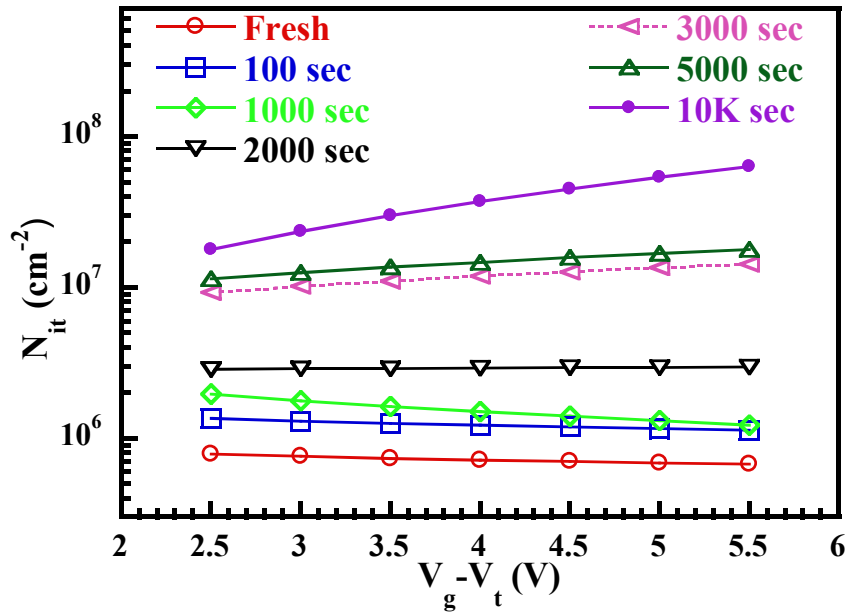
Figure 4-10 Increasing trend of interface trap density with stressing time for a 30 V device stressed at V_g =5 V and V_d =30 V. Other devices also showed similar tendency of trap variation.

4.10   Dominant *1/f* Fluctuation Mechanism

From Equation (4.23), if the carrier number fluctuation is the dominant noise mechanism, S_{I_d} will be varying as N_{ov}^{-1} and will dominate over the surface mobility

fluctuation (which is proportional to $\alpha_{ov}\mu_{ov}$). Figure 4-11 shows the separation of number and mobility fluctuations in four different unstressed devices (20-50 V rating) at various gate overdrive voltages. In each case, mobility fluctuation surpasses carrier number fluctuation by several orders of magnitude, and this conclusion is not influenced by process variations. This is contrary to the conventional symmetric NMOS, where carrier number fluctuation is typically known to be the dominant source of noise [58, 69]. The magnitude of the screened scattering coefficient, α_{ov} (7.5×10^{-14}~2×10^{-13} Vs) is at least an order of magnitude higher than that in NMOS (~1×10^{-15}) [69]. Although, a general trend for the mobility fluctuation fitting parameter $\mu_{c0_{ov}}$ was not obtained, its magnitudes are lower in general, compared to the conventional and high-κ MOSFETs [58, 69].

In LDMOS, there is no depletion region underneath the gate-overlap accumulation layer. The fluctuations from the bulk traps in the NWell can be considered to be negligible [67]. The observed high mobility fluctuations are then due to the increased number of Coulomb scattering sites at the Si-SiO$_2$ interface and in the gate-oxide bulk. Therefore, mobility fluctuation due to remote Coulomb scattering is found as the dominant noise mechanism for flicker noise in LDMOS. Figure 4-12 shows the dependence of stressing duration on the carrier number fluctuation, mobility fluctuation, and correlated carrier number and mobility fluctuation terms at different gate biases. At V_g =2.5 V, the extended drain noise starts to dominate over the channel noise. We observed a noticeable difference in magnitude of the mobility fluctuation term after 5000 sec stressing, compared to that after 1000 sec stressing at that gate bias. The difference, however, reduces as we measure the noise at higher gate biases. At V_g =5.5 V, the increase in mobility fluctuation term with stressing time is more gradual. On the other hand, the number fluctuation term does not show any discernible stressing time
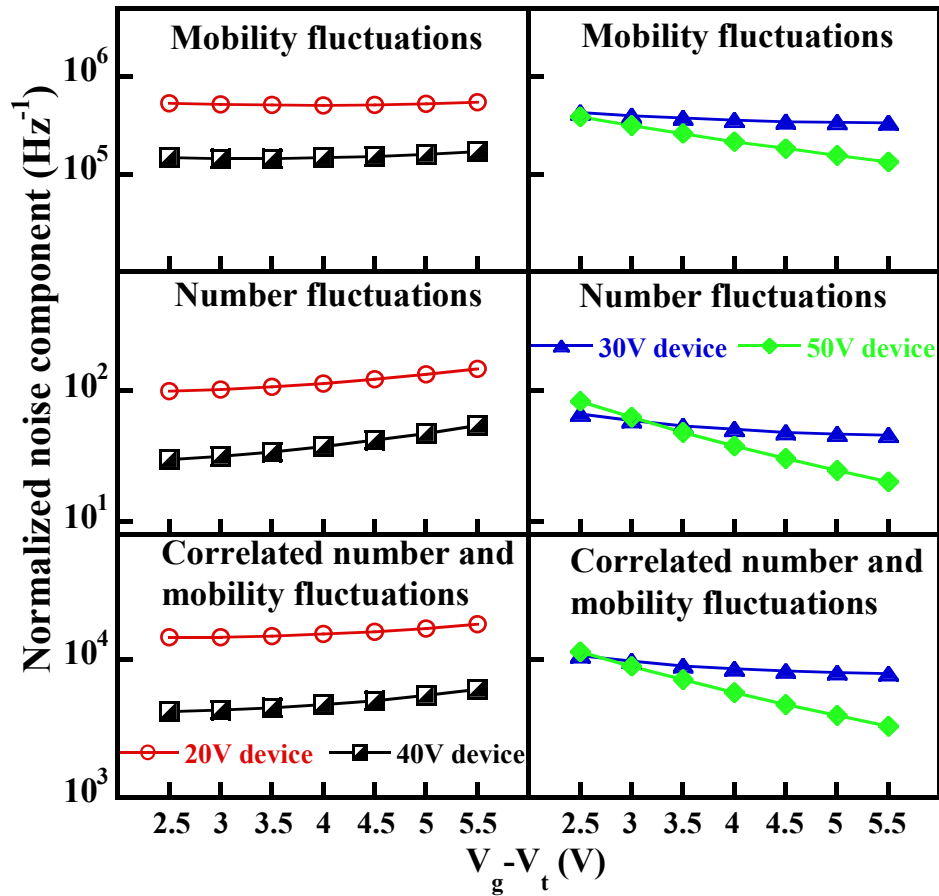
Figure 4-11 Drain current normalized *1/f* noise components of the measured drain current power spectral density as a function of gate overdrive voltages for fresh devices. Y axis is arbitrarily scaled.

dependence at any gate bias. An increase in the number fluctuation term is observed at V_g =4V and above, if the device is stressed up to 500 sec. However, a decreasing tendency is observed for further increase in the stressing times at those gate biases. Finally, for the correlated carrier number and mobility fluctuation term, a dramatic increase is found after 1000 sec stress compared to after 500 sec stress, when

measured at V_g=2.5 V. However, at V_g=5.5 V, the catastrophic increase in this

fluctuation term, occurs later at 5000 sec stressing. The physical reason for this behavior

is not known at this moment.
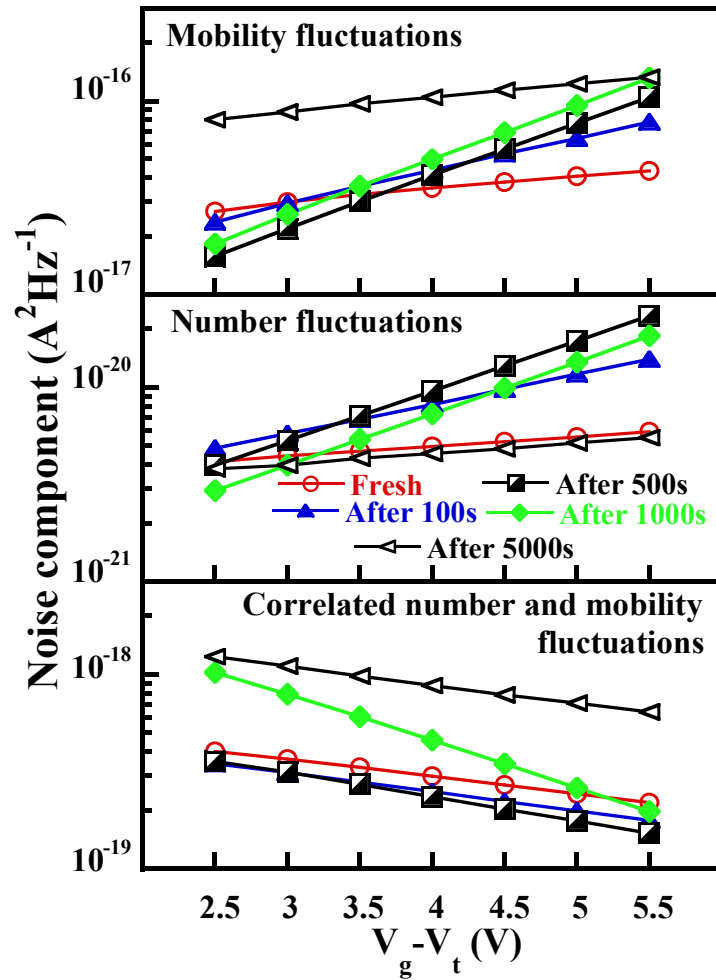
Figure 4-12 Effect of stress on different noise components of the drain current fluctuation

in a 30 V device stressed at V_g=5 V and V_d=30 V.

A critical observation is the correlated number and mobility fluctuation term in Equation (4.23) to have significant contribution to *1/f* noise in LDMOS, which typically does have lower or sometimes negligible contribution in conventional and high-κ MOSFETs [63, 69, 70]. We found that this noise component is at least an order of magnitude higher than carrier number fluctuations in all the devices before stress, and also regardless of stressing time (Figure 4-11).

4.11 Origin of Lifetime Degradation in LDMOS

From the developed noise model, we can identify the extent of physical location of the active traps and their spatial variation with DC stress as well as with gate bias. From the upper-bound of the integral term $(\omega\tau)^{\left(\beta_{ov}V'_{ov}+\eta_{ov}\right)/\gamma+1}\Big/\left[1+(\omega\tau)^2\right]$ in Equation (4.23), which is $\omega\tau_0\exp(\gamma T_{ox})$, the extent of the active traps in the oxide are listed in Table 4-1 for one of the LDMOS devices. Since stressing degrades the Si-SiO$_2$ interface, the effect of traps at the interface contributing to fluctuations increases compared to those deeper in the oxide, thus moving the extent of active trap density effectively closer to the interface [25]. This is also consistent with the observation in Figure 4-8. Therefore, the stress induced interface states are responsible to a further extent for LDMOS lifetime degradation than the deeper oxide traps.

Table 4-1 Spatial Distribution of Traps into the Oxide

V_g-V_t (V)	Before stress		After stress	
	Trap density $N_{t_{ov}}$ (cm^{-3}eV^{-1})	Distance into the oxide (nm)	Trap density $N_{t_{ov}}$ (cm^{-3}eV^{-1})	Distance into the oxide (nm)
2.5	2.82×10^{14}	3.20	1.57×10^{15}	3.18
3	2.86×10^{14}	3.21	1.58×10^{15}	3.18
3.5	2.90×10^{14}	3.21	1.59×10^{15}	3.18
4	2.94×10^{14}	3.21	1.60×10^{15}	3.18
4.5	2.97×10^{14}	3.22	1.61×10^{15}	3.19
5	2.99×10^{14}	3.22	1.62×10^{15}	3.19
5.5	3.02×10^{14}	3.23	1.63×10^{15}	3.19

4.12 Deviation from U-Shaped Oxide Trap Energy Distribution

Because of the gate-bias induced strong surface energy band-bending of the amorphous oxide above the NWell overlap region, the quasi-Fermi level position there is found at about E_c + 0.26 eV to E_c + 0.4 eV depending on device rating (Figure 4-7). This means, the active traps are located above the conduction band edge of Si. A recent report also confirms that available defect states (within the quantum confinement of carriers) are extended beyond the band edges [63].

We showed that the deeper oxide traps, which are found above E_c, have a significant impact on *1/f* fluctuations in LDMOS [29, 71]. It is well-known that the traps follow a U-shaped energy distribution from the mid-gap towards the band-edges in the Si-SiO$_2$ interface [72-74]. However, some authors have shown [64, 75] that the interface trap density follows the U-shaped distribution within E_V + 0.2 eV to E_V + 0.9 eV of Si. In

the developed *1/f* noise model, we accounted for such an energy continuum to exist in the gate-overlap oxide trap distribution (Figure 4-13) [49].
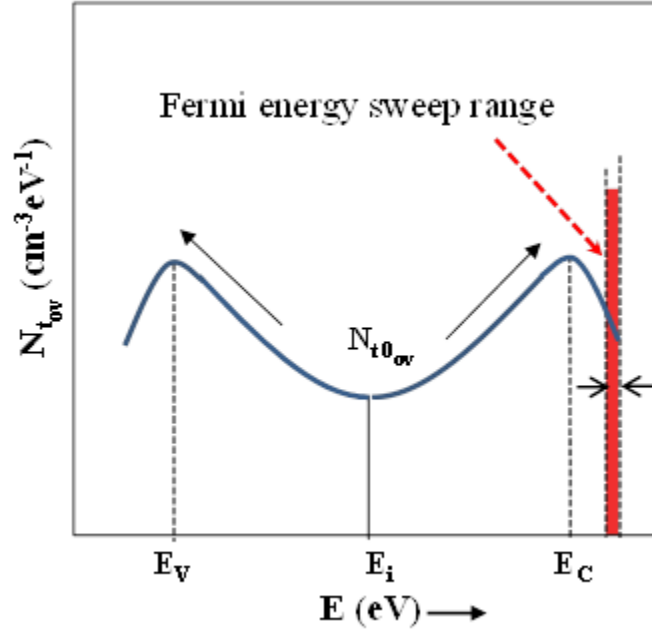
Figure 4-13 Exponential trap distribution profile at the Si-SiO$_2$ interface of gate-overlap region. Due to strong accumulation, position of Fermi level and therefore the active traps are above the conduction band edge of Si. $N_{t0_{ov}}$ is the mid-gap trap density and ξ_{ov} defines the energy dependence of the traps (eV^{-1}): $N_{t_{ov}} = N_{t0_{ov}} \exp\left[\zeta_{ov}\left(E_{f_{ov}} - E_i\right)\right]$.

Now to compare with the existing results, typical effective oxide trap density in poly-Si gated conventional NMOS devices is found as ~1×10^{17} cm^{-3}eV^{-1} [59]. High-κ devices show even higher trap density [57]. Our LDMOS transistors, however, show at least 2-3 orders of lower magnitude, as discussed above. Since the channel and gate-overlap regions have the same native oxide, we can assume a typical trap density of

1×10^{17} cm^{-3}eV^{-1} exists at the conduction band edge of Si. As we obtained active traps to be located above E_C, and that trap density quantitatively is lower than that at E_C, the extracted trap density can be said to contradict the conventional U-shaped energy continuum for trap distribution above the conduction band edge. Our observation can be supported with a recent report (although not in the case of LDMOS) that the U-shape energy continuum of the band-edge states does not hold true in case of high-quality Si-SiO$_2$ interfaces [63]. Therefore, deviation from U-shape trap energy density continuum is not unlikely. Hence, it is not surprising that the effective trap density will also vary from the conduction band edge all the way to the quasi-Fermi level position depending on device type and processing. Nevertheless, the trap distribution within the probed energy levels may not be an accurate reflection of actual trap profile in the gate-oxide below and beyond that probed energies, as the experimental data is valid for active trap fluctuations around the quasi-Fermi level only.

4.13   Noise in Saturation Region

Our investigations have been limited to the linear region of operation. There have been reports also for the saturation region. Unlike our results, these studies demonstrated that in saturation region, the channel noise is dominant due higher lateral electric field swiping the carriers away from the interface and also partially due to quasi-saturation effect [32, 43]. The effect of drift region is reported to be dominant in n-channel devices compared to p-channel LDMOS [32]. The drift region impacts not only in linear region but also when the channel is short and device is in saturation [43]. However, as the channel length increases, corresponding channel flicker noise decreases, and drift region becomes insensitive to gate bias in saturation [32]. It has been proposed that optimized *1/f* noise performance can be obtained when LDMOS is operated at higher

drain bias to saturate the channel to avoid the onset of quasi-saturation, although this conclusion has not been verified on noise performance upon applying high voltage stress. A time-dependent degradation based noise analysis would be interesting as far as device reliability is concerned.

4.14 Discussion and Summary

Conventional techniques like *C-V* measurements, electron paramagnetic resonance (EPR) [75], conductance method and the popular charge-pumping method are limited to calculating interface traps, typically well within the Si band-gap. Several authors have determined the 'fast' interface trap density in LDMOS devices from charge-pumping method and other high-frequency techniques [24, 30, 68], albeit our results suggest that the slow interface states are responsible for increased *1/f* noise degradation with stress.

Active oxide trap density is characterized spatially and for the first time up-to ~0.4 eV above E_C of Si in the extended-drain NWell. We mentioned above that our observation contradicts the well-known U-shaped trap energy distribution. Surface mobility fluctuation due to increase in the number of Coulomb scattering events is identified as the dominant physical mechanism for LDMOS *1/f* fluctuation irrespective of process technology.

We showed the channel noise follows the Unified *1/f* Noise Model in Figure 4-1. However, we did not look into the dominant noise mechanisms when channel noise is the highest contributor as this noise component does not degrade over time with stressing. It has been reported that carrier number fluctuation dominates over mobility fluctuation in this case [32].

Finally since V_t did not degrade significantly with stress in any device, which would have suggested preexisting oxide bulk defects [76], it is perceivable that additional

traps are generated in the interface of gate-overlap region upon stressing which are responsible for LDMOS lifetime degradation.

4.15 Conclusion

A new model for low frequency noise in RESURF LDMOS is implemented based on the Unified *1/f* Noise Model. The developed model has been experimentally verified for different LDMOS technologies for varying hot-carrier stressing times up to 10,000 sec. The dominant *1/f* noise mechanism has been found to be the charge carrier number and mobility fluctuations due to dielectric traps in the gate overlap region of the extended drain. As this region was found to degrade the most in noise characteristics with stressing, it was possible to extract the increase in the dielectric trap density with stressing as a function of position in the gate dielectric and with respect to band-gap energy, using the developed model.

Chapter 5

RTS Noise in Submicron Analog Devices

5.1 Introduction

Over the last three decades, random telegraph signals have drawn the attention of researchers as a non-destructive characterization technique for investigation of individual trap behavior, specifically in small area MOSFETs. With advanced submicron device area scaling, RTS issue has become even more of a growing concern for both analog and digital devices, especially as the CMOS channel length has shrunk to 45 nm or even below [4, 14, 15, 77]. Researchers have found electronic noise in the form of RTS with magnitude as high as 30% of the drain bias in deep submicron MOSFETs [78] due to random dopant atomic density fluctuations, dominating over other random thermal capture-emission processes, especially if there is inhomogeneous carrier concentration present due to local surface potential minima (in weak inversion). If a defect is in such a strategic position, it may completely prevent the channel carriers to conduct and therefore, can generate very high RTS signal [79]. Other researchers found low frequency noise magnitude greater than 60% as well [80, 81]. If this situation deteriorates further, such a significant discrete drain current fluctuation could lead to scaling limit for device miniaturization [82]. Therefore, RTS amplitude for the traps is an important indicator from device design and reliability point of view.

An RTS event is created when the electron transition occurs from Si conduction band to a defect state (with energy within a few $K_B T$ of surface Fermi level) in the oxide or in the oxide-Si interface by capture and returns to the channel by an emission process. This is a stochastic, non-radiative process, where excess energy during capture and emission of the free channel carriers is dissipated to give out multiple phonons [83]. Before an electron capture event, the defect undergoes thermal vibration with respect to

its equilibrium position which is above the energy bandgap of Si in strong inversion for a repulsive trap. If the lattice displacements between free and bound electronic state is high enough and at large lattice vibrations, the equilibrium position of trap state can cross the conduction band of Si to capture electron(s) and then relocate to a new equilibrium position in the energy gap and relaxes or damps down by giving up energy in the form of phonons. The relaxation energy is known as semi-Franck-Condon energy shift $S\hbar\omega$ (S phonons of energy $\hbar\omega$ each) where S is the Huang-Rhys parameter which is a measure of the strength of phonon-electron coupling [83, 84]. Typically, electron capture occurs from the ground energy level and from the first energy level of the channel [83]. Other subbands do not significantly contribute to this process. Cascade-capture and Auger-assisted trapping mechanisms are ignored as suggested in [85]. Please note that, this is the most accepted physical origin of RTS noise which is however, not applicable to all operating regions of MOSFETs [14, 80]. A universal RTS theory is not available till date.

RTS noise analysis in the following sections will be based on several assumptions made in other literatures as well [15, 16, 86-90]:

a) Active traps are located within the tunneling distance from the interface to the dielectric (within 2 nm) of electrons. However, this can vary depending on oxide thickness.

b) Each defect site is capable of capturing only a single charge carrier at a time. Kirton and Uren [15] showed that multi-electron trapping in the same site is not possible unless the traps are located in the bulk Si.

c) Excess energy changes during capture and emission processes are reflected in the trap enthalpy and entropy changes, which can be explored if temperature dependence of the trap parameters is studied, which is however not covered in this dissertation.

d) Image charge effect (Coulomb blockade) is considered negligible in linear region operation in strong inversion [15, 79, 90, 91].

e) Trap distribution in the dielectric does not have to be uniform, as explained in the previous chapters.

f) Room temperature RTS analysis for capture and emission of traps refers to lattice temperature only, which is independent of electron temperature. Electron temperature can be made different than lattice temperature upon applying a high drain bias, especially at lower temperatures [15]. However, capture energy depends only on the lowest electronic energy level.

g) For simplicity, RTS amplitude is considered not to depend on the trap position along the channel; it only depends on the depth of the trap into the oxide.

5.2 Motivation for Investigation of Multilevel RTS in Analog Devices

So far, most published RTS analyses are based on simple two-level drain-current fluctuations, measured in the linear region of MOSFET operation. Moreover, most studies are applicable to submicron devices having few active traps [4, 15, 80, 92]. In many instances, multilevel RTS are observed because of the higher number of active traps and their mutual interactions. According to [77, 93], RTS in the form of threshold voltage fluctuation (the difference of threshold voltage before and after capture of a channel carrier) is inversely proportional to the device dimension:

$$\Delta V_t = -q / WL_c C_{ox} \tag{5.1}$$

where C_{ox} is the oxide capacitance per unit area and WL_c is the effective device area. This intuitive relationship holds for both analog and digital transistors, suggesting that

RTS will become even more of reliability concern in future technologies in implementing the ITRS roadmap [4, 80]. The situation worsens in case of multilevel or complex RTS cases, where RTS magnitude is larger compared to two level RTS [77]. This dissertation presents a study of multilevel RTS measurement and analysis in 1.5 V submicron analog transistors (with active area <0.03 μm^2) at room temperature and emphasizes on a particular RTS switching behavior. As will be evident later in this chapter, the observed switching events have a superposition of two different RTS waveforms (similar to Figure 5-1) with identical amplitudes. This was found in 33% of the NMOS devices that were investigated. We then developed a new algorithm to identify the RTS amplitudes, and mean capture and emission times for each trap. Our analysis demonstrates the existence of two different types of traps (acceptor and donor) in the same device at room temperature, which are not in the same physical location, unlike reported results [15, 94, 95].
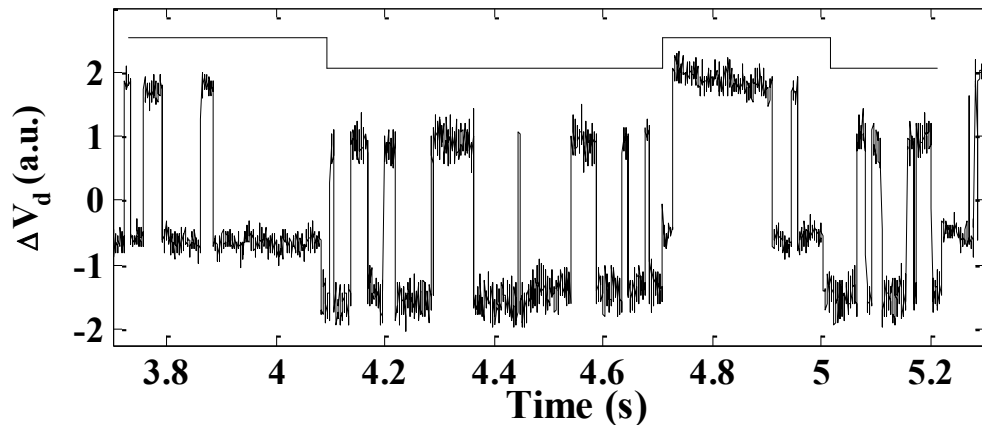
Figure 5-1 A small window of typical four level RTS obtained from a 1.5 V NMOS, which showed multilevel RTS. The RTS magnitudes are shown as the drain voltage fluctuation (ΔV_d) in arbitrary units. The trend of the envelope switching is shown on the top.

5.3 Literature Review on Multilevel RTS

Researchers have shown that multilevel RTS with four independent levels can be obtained in NMOS transistors originating due to three independent trap fluctuations [14]. There has been a report of a complex three level RTS due to sequential two electron capture by a single defect which shows metastability i.e. electronic reconfiguration towards two metastable states, and one electron affects the occupancy of another one by Coulombic effect [15]. Another report illustrated that multilevel threshold voltage fluctuations can be possible due to two active traps, which are present at the same location [77]. Two level and multilevel RTS were analyzed by Nagumo *et al.* [96] using a time lag plot (TLP) to find the threshold voltage shift and to extract the number of active traps. Then the analysis methodology was extended for finding trap positions [97]. Miki *et al.* [98] assumed RTS is a two state Markov process and developed a hidden Markov model (HMM) for extracting RTS mean capture and emission time constants. A similar method was adopted by Realov *et al.* [99]. However, according to [100], all these methods suffer from severe limitations. For example, RTS magnitude and time constants were analyzed independently without finding the relationship between these two parameters, which might cause inaccurate trap parameter extraction. Another limitation is that those methods were applied to devices that have a single dominant trap. However, details were not provided for applicability to multi-traps. In multiple trap case, each trap is responsible for drain voltage shifts (or equivalently drain current shift) and a superposition of all these drain voltage fluctuations is what one observes in time domain. Hence, in order to investigate the activities of each trap, decomposition of multi-trap activity is required. A general consensus for the physical mechanism for multilevel RTS switching events has not been reached till date due to random fluctuations varying from device to device, and it is not easily predictable to identify which devices will show multilevel RTS.

5.4 RTS Analysis Methods

Random telegraph signals can be analyzed in time domain, where there is no averaging of real time signal is done and no fast Fourier transform is taken. When a single or a few traps are present, realistic switching events can be observed in time domain, and each trap properties can be quantitatively and qualitatively studied. On the other hand, in frequency domain, we can have Lorentzians due to the presence of a single or multiple traps, and individual capture/emission processes cannot be observed. If the traps are uncorrelated (independent), significant Lorentzians should be observed in the synthesized spectra, with the number of Lorentzians corresponding to each independent trap [101]. However, if a number of traps are present, the ensemble average of them will lead to *1/f* noise spectra instead. An overview of Lorentzian spectrum observed in frequency domain was provided in Chapter 1. In a typical CMOS, dominant RTS are found either (i) after a dielectric breakdown near the breakdown spot (due to current filamentation effect), where gate leakage current induces significant capture and emission of charge carriers leading to RTS fluctuation [102] or (ii) if the device size is small. We have not studied the former case in this work.

5.4.1 Time Domain Analysis

Time domain measurement of RTS is done with an Agilent 54832B oscilloscope. In the simplest case of two level RTS, it is somewhat easier to come up with upper and lower limits for each of the levels (Figure 5-2a). Using Poisson distribution, we can calculate mean time at each level. For example, the total duration in the top level is subdivided into small time intervals (Figure 5-2b) and the number of occurrences is counted that have the time width that spreads into each small interval. Then, the plot of frequency of occurrences for each time interval will follow Poisson fitting, $a_0 e^{-t_0(t)}$.
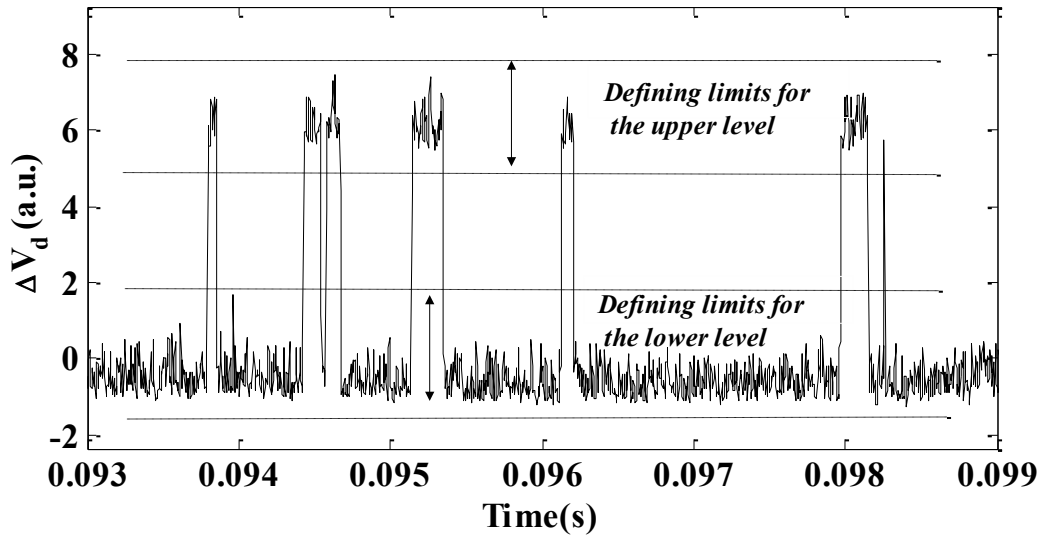
(a)
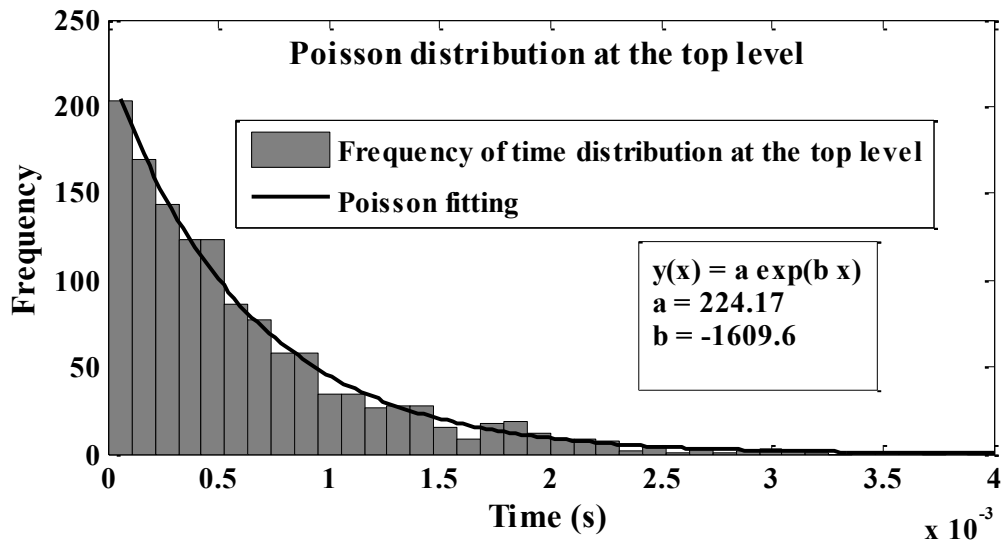
(b)

Figure 5-2 (a) Defining voltage limits for the top and bottom levels of the RTS. (b) Time distribution of the top level along with a Poisson fitting. The RTS was measured at V_g =0.702 V and V_d =0.2 V.
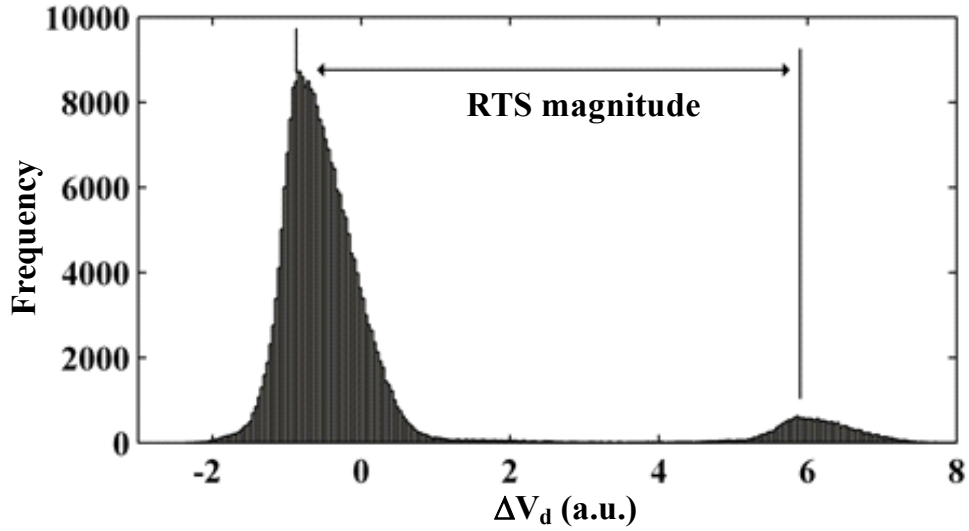
Figure 5-3 Histogram for the amplitudes of the time domain RTS in Figure 5-2. Extraction method for the RTS magnitude is also shown as the difference of two maxima.

The mean time at that transition level is calculated using:

$$\tau_0 = \frac{\sum_i (t_i) a_0 e^{-t_0(t_i)}}{\sum_i a_0 e^{-t_0(t_i)}} \tag{5.2}$$

where a_0 and t_0 are fitting parameters. In an ideal measurement result, this mean time from Poisson distribution should correspond to that extracted from time distribution analysis. However, in practice, especially in case of multilevel RTS, a deviation should be expected when there are data overlapping in between the levels as shown in Figure 5-1. This issue will be discussed in detail in the next Chapter. Once a histogram is plotted for the RTS amplitudes as shown in Figure 5-3, the RTS magnitude will be the difference between the two maxima, each corresponding to the top and bottom levels.

We have adopted $\Delta V_d / V_d$ ratio to measure the relative magnitude of RTS in analog devices. Please note that it is also possible to consider $\Delta I_d / I_d$ parameter as shown by other researchers [103], which can then be converted to measure threshold voltage fluctuation (ΔV_t) by:

$$\Delta V_t = \frac{\Delta I_d}{g_m} \qquad (5.3)$$

Physically, the parameter ΔV_t means the change in threshold voltage before and after a charge carrier is captured by a trap [93]. However, it was convenient for our measurement system to extract ΔV_d, in a constant current supply condition. Since, the transconductance (g_m) needs to be measured using a semiconductor parameter analyzer, simultaneous determination of ΔI_d and g_m was not possible without error due to 60 Hz line frequency interference and interference in between two AC equipment. Therefore, the DC and C-V measurements were done separately from the RTS measurement. Nevertheless, RTS analysis in time domain is useful in determination of three trap properties: capture time, emission time and the RTS magnitude.

5.4.1.1 Mean Capture and Emission Times

Capture time is the duration spent by a trap before capture of an electron from the channel to become full, and emission time is how long it takes for the full trap to become empty again. Since RTS is a stochastic process, it is therefore conventional to use mean capture ($\overline{\tau}_c$) and mean emission time ($\overline{\tau}_e$) to explain the macroscopic capture and emission times. According Shockley-Read-Hall (SRH) statistics [104], these

quantities are related to barrier energy (ΔE_B) and trap binding energy (ΔE_{CT}) as [14, 15, 80]:

$$\overline{\tau}_c = \frac{\exp\left(\Delta E_B / k_B T\right)}{n \sigma_0 v_{th}}$$ (5.4)

$$\overline{\tau}_e = \frac{\exp\left[\left(\Delta E_B + \Delta E_{CT}\right) / k_B T\right]}{n \sigma_0 v_{th}}$$ (5.5)

Here, σ_0 is the capture cross-section pre-factor and n is the inversion carrier concentration. Both σ_0 and ΔE_{CT} are gate bias dependent, while in general, barrier energy is independent of gate or drain bias [15, 80]. Please note that, σ_0 and ΔE_{CT} can be found as fitting parameters, by doing a bias and temperature dependence study since they are independent parameters [80]. Since we did not study variable temperature RTS behavior, to calculate mean capture and emission time at room temperature, we used the following relationships based on carrier thermal activation [105]:

$$\overline{\tau}_c = \frac{1}{n \sigma v_{th}}$$ (5.6)

$$\overline{\tau}_e = \frac{\overline{\tau}_c}{g} \exp\left(-\frac{E_T - E_F}{kT}\right)$$ (5.7)

where $\sigma = \sigma_0 \exp\left(-\Delta E_B / k_B T\right)$ is the capture cross-section. The trap degeneracy factor (g) [106] is usually taken as 1, when the defect is in the oxide [14, 15]. $E_T - E_F$ is the energy difference in between the trap energy and electron Fermi

level. Now, the mean capture time is related to the channel carrier concentration (n). In the linear region of MOSFET operation, n is expressed as:

$$n = \left(\frac{L_{eff}}{W_{eff}}\right)\left(\frac{I_d}{q\mu V_d t_{inv}}\right) \tag{5.8}$$

where μ is the channel carrier mobility and t_{inv} is the inversion layer thickness. Using charge sheet model approximation, the carrier concentration can be found anywhere in the channel [80]:

$$n(0,y) = \left(\frac{n_i^2}{N_a}\right)\exp\left[\frac{q\left(\psi(0)-V(y)\right)}{k_B T}\right] \tag{5.9}$$

where surface potential is taken at the interface and $V(y)$ is the potential at a distance y from the source to the drain. Using a gradual channel approximation in the linear region operation, n can be calculated using:

$$n = \frac{C_{ox}\left(V_g - V_t - V_c\right)}{q t_{inv}} \tag{5.10}$$

where V_c is the channel potential $\left(V_c \approx yV_d/L\right)$ at a distance y from the source. To simplify the analysis, t_{inv} is considered not to change with drain bias. So, n decreases with drain bias, which consequently increases $\overline{\tau}_c$.

5.4.1.2. Determination of Trap Type and Distance from the Interface

The trap type can be found from time domain analysis using the schematic diagram in Figure 5-4. The bottom level in Figure 5-4 (a) shows the state where the single trap is neutral (state 0), and the upper level (state 1) is where the trap is full (either

103

negatively or positively charged). For an n-channel MOSFET, if a trap is negatively charged when in state 1 i.e. when it is full with channel carrier, and stays at state 0 when devoid of electron, the trap is called acceptor or repulsive type. To the contrary, if a trap is positively charged in its empty state (in state 1), and goes to state 0 when it captures an electron to become neutral, the trap is called a donor or attractive type. Typically, acceptor trap is due to a non-bridging oxygen atom [94] while its antagonist, the donor trap is due to Si bond vacancy.
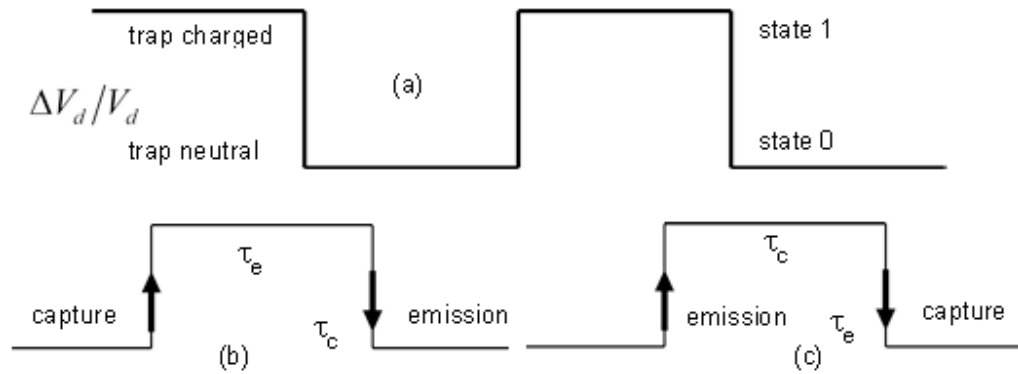
Figure 5-4 Schematic identification of donor and acceptor traps for electron trapping-detrapping. (a) State 0 is where the trap is neutral and state 1 is after the trap is charged. Capture and emission process and corresponding mean capture and emission times are shown for an (b) acceptor trap and (c) donor type trap.

Mean capture and emission times are related to trap occupancy function as:

$$\frac{\overline{\tau}_c}{\overline{\tau}_e} = \frac{1-f_t}{f_t} \qquad (5.11)$$

Increasing gate bias will increase the trap occupancy (f_t) which in turn decreases mean capture time (and increases capture probability) for an electron. The emission time typically remains the same or increases under certain cases [90]. If low current state (or equivalently, the high voltage state) is dominant with increased V_g, the trap is expected to be ionized [107] as an acceptor trap and the low state defines the capture time. The upper state then determines the emission time. The opposite is true for the donor trap case, and also for the case of hole trapping/detrapping.

From the capture and emission time statistics, we can calculate several other trap properties. From the principle of detailed balance, capture and emission time ratio is related to trap energy, E_T with respect to the oxide conduction band energy, $E_{C_{ox}}$ and trap distance x_T through [14]:

$$\ln \frac{\overline{\tau_c}}{\overline{\tau_e}} = -\frac{1}{k_B T}\left[\left(E_{C_{ox}} - E_T\right) - \left(E_C - E_F\right) - \phi_0 + q\psi_s + q\frac{z_T}{T_{ox}}\left(V_g - V_{FB} - \psi_s\right)\right] \quad (5.12)$$

where, ϕ_0 is the electron affinity difference between the Si and SiO$_2$, ψ_s is the surface potential, T_{ox} is the oxide thickness, and V_{FB} is the flat-band voltage. This relationship is however, not always applicable, especially when the trap is located near the drain side as drain bias dependence is neglected in this relationship. In most cases, active traps causing RTS are found near the mid-channel region albeit dominant trap near the source side is also reported [108]. Nevertheless, the relationship above is widely accepted and used for low drain voltages to find the trap energy. The location of the trap into the oxide then can be found from:

$$\frac{d\left(\ln \bar{\tau}_c / \bar{\tau}_e\right)}{dV_g} = -\frac{q}{k_B T}\frac{z_T}{T_{ox}} \tag{5.13}$$

Please note that, the chemical properties of these trap species are beyond the scope of this work as a temperature dependence study was not done. However, we can find the macroscopic nature of the trap (attractive or repulsive type impurity) from the RTS switching behavior.

5.4.1.3 RTS Amplitude

RTS amplitude provides vital information about trap properties. As explained above, from the time domain RTS measurement, a histogram is plotted and RTS magnitude is found from the difference between two maxima in case of a simple two level RTS. Typically, if an acceptor trap is close to interface, it generates higher RTS magnitude due to proportional increase in Coulomb scattering which bolsters the RTS magnitude, as compared to the trap further inside the dielectric [94]. For donor type traps, scattering decreases with gate bias and corresponding RTS amplitude also decreases. RTS magnitude also depends on MOSFET operation regime. In weak inversion, scattering does not change noticeably, so $\Delta V_d / V_d$ remains constant, whereas in strong inversion the magnitude decreases with gate bias [94]. In multilevel RTS case, if the traps are uncorrelated and independent i.e. if there is (n-1) traps for n maxima [14], the same methodology of finding the difference between consecutive maxima applies to calculate RTS magnitude. However, RTS magnitude extraction is sometimes quite complex, as in the case of Figure 5-1. This will be discussed in the next chapter.

5.4.2 Frequency Domain Analysis

The probability of electron capture by a trap is defined by:

$$p_c(t) = \frac{1}{\overline{\tau}_c} \exp\left(-\frac{t}{\overline{\tau}_c}\right)$$ (5.14)

and the probability that the full trap releases that electron:

$$p_e(t) = \frac{1}{\overline{\tau}_c} \exp\left(-\frac{t}{\overline{\tau}_e}\right)$$ (5.15)

Capture and emission probabilities are normalized such that: $\int_0^\infty p_c(t)dt = 1$ and

$\int_0^\infty p_e(t)dt = 1$. Therefore, the transition time from each level can be determined as:

$$t = \overline{\tau}_{c/e} \ln\left(p(t)\right)$$ (5.16)

Hence, the mean capture and emission times are exponentially distributed. Once the time domain RTS is converted to frequency domain, a Lorentzian shape appears in the power spectrum. Let, electron captured state has amplitude $x_c=0$ and after emission the state goes to $x_e = \Delta V_d$. Then at any time, capture rate is $1/\overline{\tau}_c$ and probability that the electron is in captured state is $\overline{\tau}_c/(\overline{\tau}_c + \overline{\tau}_e)$. Following the derivation by Machlup, as shown in [15], it can be shown that the power spectral density of the RTS in frequency domain is:

$$S_V(f) = \frac{4\left(\Delta V_d\right)^2}{\left(\overline{\tau}_c + \overline{\tau}_e\right)\left[\left(1/\overline{\tau}_c + 1/\overline{\tau}_e\right)^2 + \left(2\pi f\right)^2\right]}$$ (5.17)

The total power from the generated RTS can be obtained by integrating Eq. (5.17) over all the frequencies as:

$$P = \frac{\left(\Delta V_d\right)^2}{\left(\overline{\tau}_c + \overline{\tau}_e\right)\left(1/\overline{\tau}_c + 1/\overline{\tau}_e\right)} \tag{5.18}$$

The maximum noise power can be obtained when $\overline{\tau}_c = \overline{\tau}_e$, which is $P = \frac{1}{2}\left(\Delta V_d\right)^2$. The mean characteristic time ($\overline{\tau}$) is defined as: $1/\overline{\tau} = 1/\overline{\tau}_c + 1/\overline{\tau}_e$ and characteristic frequency is defined as:

$$f_0 = 1/2\pi\overline{\tau} \tag{5.19}$$

Now, let the magnitude of the power spectral density: $k = \dfrac{4\left(\Delta V_d\overline{\tau}\right)^2}{\left(\overline{\tau}_c + \overline{\tau}_e\right)}$. Therefore, we get:

$$\overline{\tau}_{c/e} = \frac{2\left(\Delta V_d\overline{\tau}\right)^2}{k}\left[1 \pm \sqrt{1 - \frac{k}{\Delta V_d^2\overline{\tau}}}\right] \tag{5.20}$$

Depending on the trap type (acceptor or donor), an appropriate sign is put here for mean capture or emission time. Following the above analysis, Eq. (5.17) can be rewritten for multiple traps as [14]:

$$S_V(f) = \sum_i \frac{k_i}{\left(1 + f/f_{0i}\right)^2} \tag{5.21}$$

Where f_{0i} and k_i are applicable for i^{th} trap in the oxide. For each characteristic frequency (f_{0i}) and spectral magnitude (k_i), we can calculate mean capture and emission times for the trap, if we can obtain ΔV_d from time domain analysis. From

108

equations (5.6) and (5.19), we can find the dependence of f_0 with capture cross-section. The typical value of $\bar{\tau}$ ranges from 10^{-5}~10^{2} sec [109, 110].

5.5 Experimental Setup

The experimental procedure includes first a DC measurement to extract threshold voltage, $I_d - V_g$ transfer characteristics and output characteristics ($I_d - V_d$). This is followed by a time domain noise measurement, and then a frequency domain noise measurement. For obtaining surface mobility and inversion charge density (N_c), a split C-V measurement is done in relatively larger area devices. All the measurements were done several times to ensure the obtained data are repeatable.

5.5.1 Device Specifications and Sample Preparation

In this work, we studied 1.5 V NMOS transistors at room temperature and in linear operation region under strong inversion. In the subthreshold operation region, image charge effect and partial screening of the charge carriers from the gate and substrate charges are observed [15, 79, 90]. On the other hand, high lateral electric field causes surface mobility scattering and charge carrier velocity saturation because of the pinch-off condition for a MOSFET operating in saturation region. All the measurements here were performed in linear region (strong inversion). In such a case, the channel can be considered to be homogeneous in the linear operation region due to invariability of inversion charge density at low drain biases [90]. Since the channel is not pinched-off, active traps can be located anywhere along the channel. The test wafers were provided by Texas Instruments Inc. The effective device area was less than 0.03 µm^2 in all the tested devices with a gate oxide thickness below 3.5 nm. To control the threshold voltage

and to prevent drain induced barrier leakage or the punchthrough effect [111], a halo implant was made near the source and drain side during device fabrication. In case of split C-V measurements, larger devices were used with typical dimensions of 0.5x70 μm^2 (LxW), so that the capacitance is measurable. Prior to RTS noise and C-V measurements, each device has to be tested to make sure they are operational by doing DC characteristics measurement ($I_d - V_g$ and $I_d - V_d$). Because the devices are highly scaled, extra precaution was taken during and outside measurement. The procedure starts with finding the desired devices on the test wafer. Before touching the probe tips on the contact pads, all the probe holders are shorted together outside the probe station. After that the pads are probed. Shorting of the gate, drain, source and substrate input leads altogether minimizes the probability of charge buildup across the gate oxide which might generate high electric field resulting in leakage current, or dielectric breakdown in the worst case scenario. After probing the pads, the shorts are removed and measurements can be done. While switching from DC measurement to noise or C-V measurements, the device inputs again need to be shorted to avoid any charge build up or physical contact. Devices might still fail due to electrostatic discharge event (ESD) due to triboelectric charge formation on semiconductor devices from the operator's physical movement, measurement environment change and due to other unavoidable charge build up events. Therefore, electrostatic gloves and a wrist strap must be put on which is connected to ground, during any physical contact with the probe station or the probes.

5.5.2 Time Domain Measurement

Time domain RTS measurements were obtained using an Agilent 54832B 4-channel oscilloscope which can capture up to 200 sec time trace and has a sampling rate of 4 GSa/sec. All the RTS measurements were done at a sampling frequency of 50

KSa/sec to 250 KSa/sec depending on the device characteristic time, so that we can capture all the slower transitions. This sampling rate varies with the measurement system as well as device properties. For example, a slow sampling rate of 60 Sa/sec was reported in the case of SRAM RTS characterization [112], due to long characteristic time constants involved for those particular devices. In selecting the oscilloscope measurement condition, care should be taken not to miss any transition (enough resolution) as well as to ensure sufficient number of transitions. Kirton and Uren [15] mentioned that at least 200 transitions are needed in 20,000 data points to have less than 10% transition detection error for a two level RTS. Since we did multilevel RTS measurement, it was necessary to take several time traces to ensure enough transitions to and from each level, and then the traces were stitched together. It was assumed that consecutive measurements thus taken without changing the measurement condition will not cause significant change in the analysis results. Since multilevel RTS is not easily obtained on all devices and also not observed at every bias condition, it is essential to test a number of devices and need to vary the bias conditions before confirming any noticeable multilevel time trace.

5.5.3 Frequency Domain Measurement

After RTS measurement, the frequency domain measurement to obtain Lorentzian spectrum was done in the submicron analog transistors at different bias conditions. The detail of this measurement system was already described in Chapter 2. These measurements can confirm the findings from some of the time domain RTS results, for example, the existence of the dominant traps in the Lorentzian spectra and the characteristic time constant for each trap.

5.5.4 C-V Measurements

The C-V measurements are taken using an Agilent 4294A precision impedance analyzer after the completion of DC parameter extraction (Figure 5-5). Before disconnecting the semiconductor parameter analyzer, a short is placed for all the terminals of a MOSFET outside the probe station and an additional T-connector in each terminal is kept as provision for C-V measurement. After connecting the device to 4294A, the shorting cables in the T-connector ports are removed. An AC small signal of 10 mV is applied with an operating frequency of 1 MHz which is high enough for minority carriers not to follow the signal. To minimize the stray capacitance effect, shielded two-terminal (2T) configuration of connecting the probes to the device was chosen [113]. Parallel circuit mode (Cp-Q) was chosen as the measurement technique of the 4294A due to very low MOSFET channel capacitance. Open, short, phase and load corrections are done prior to any C-V measurement. Since Kelvin measurement system was not possible on the devices, the low potential port was connected to low current terminal of 4294A, while the high potential and high current ports were also shorted to each other. For gate-channel capacitance measurement, gate is connected to the high terminals (shorted), while the source and drain are connected to the low terminal ports. The substrate terminal of the MOSFET is connected to the guard terminal plate of the 4294A. This ensures that the bulk charges do not interfere the gate-channel capacitance. The 'stray capacitance' is estimated from the MOSFET sub-threshold region capacitance and is subtracted from measured inversion capacitance to get the net channel capacitance C_{gc}. Then it is integrated over the inversion region gate bias to obtain the actual inversion charge density as:

$$Q_{inv} = \int_{0}^{V_{gs}} C_{gc}(V_g)dV_g \qquad (5.22)$$

A sample result of inversion carrier density extraction from C_{gc} measurement is shown in Figure 5-6.
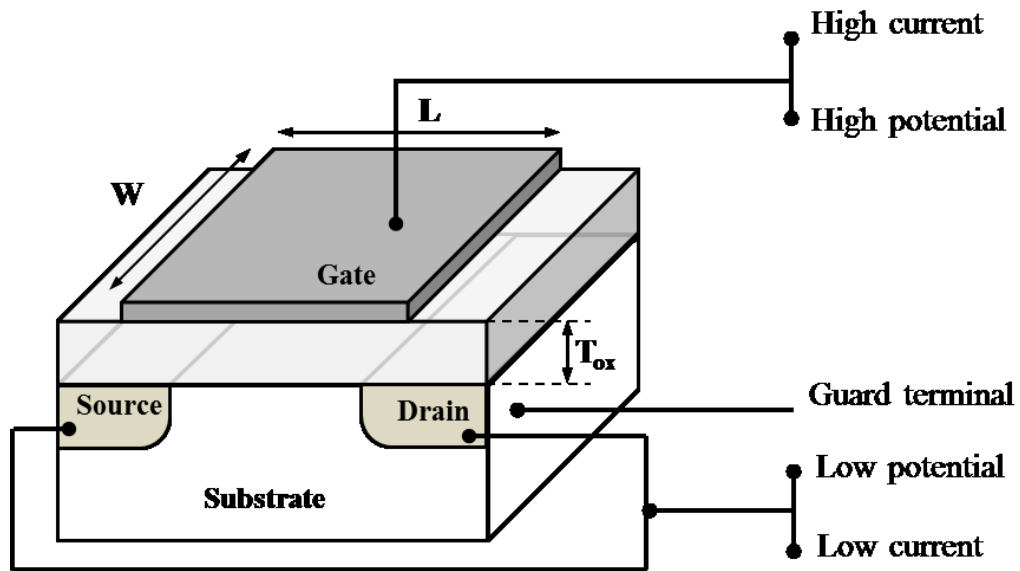
Figure 5-5 Split C-V measurement set up schematic diagram.
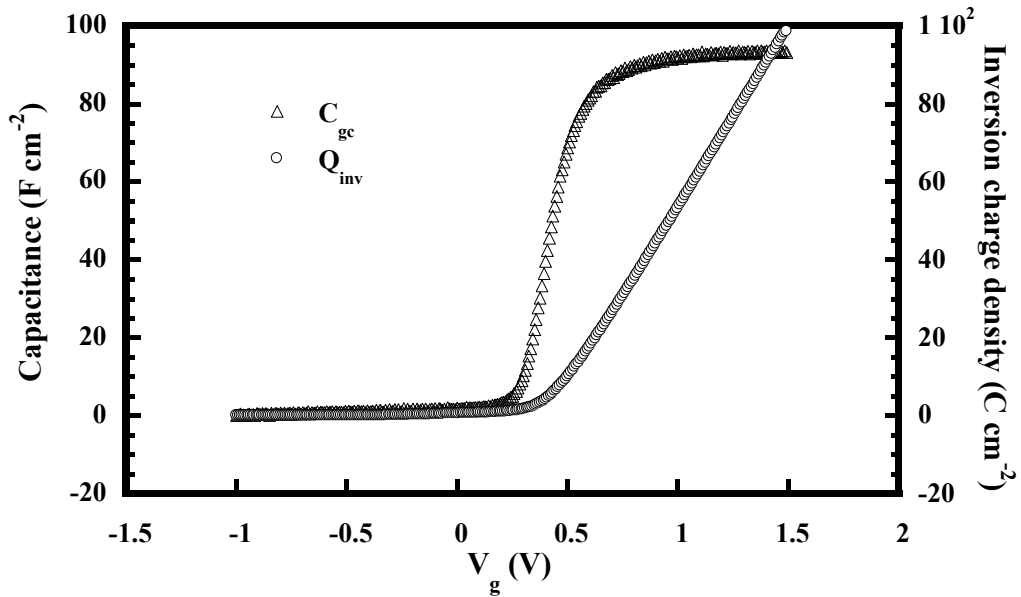
Figure 5-6 C-V measurement result from an NMOS. The left axis shows the measured

C_{gc} capacitance (after correcting for stray capacitance) and the right axis shows the

calculated inversion carrier density. Both the axes are scaled by an equal number.

5.6 Summary

In this chapter, details of the RTS noise measurement and analysis procedure along with literature review on some recent multilevel RTS analysis techniques are discussed. In addition, C-V measurement procedure and some sample results are shown. Since submicron devices are very sensitive to operator handling, specifics for device handling are discussed. DC and frequency domain measurement systems were already presented in Chapter 2, so these are not repeated here.

Chapter 6

RTS Analysis and Extraction of Trap Properties

6.1 Introduction

In this chapter, the detailed results and analysis of multilevel RTS will be presented. Depending on the bias condition, the same device can show two level or more than two level RTS, which we call as 'multilevel RTS'. This is because at low biases, some of the traps are above the quasi-Fermi level for electrons and remain empty. With increase of gate bias, traps are energetically located within a few $k_B T$ range around the Fermi level, and become active for capture and release of channel carriers. With further increase in gate bias, additional band-bending causes the traps to become inactive again by remaining full with the trapped channel carriers (away from the Fermi position). Another observation was that not all the devices having the same dimension showed RTS, due to the random location of traps. This means that the variability of trap characteristics is quite high from MOSFET to MOSFET. The observed RTS behavior is first compared to the existing reports in the literature, and then the analysis strategy from these reports are summarized. This is followed by the algorithm developed for analyzing four level RTS. A new method for identifying the multilevel RTS amplitudes will be discussed. Finally, extraction of other trap properties like trap distance into the oxide, energy, capture cross-section and screened scattering coefficient is addressed with numerical results. To the best of our knowledge, this report is the first evidence of locating two different types of traps (acceptor and donor) at room temperature.

6.2 Development of an Algorithm for Multilevel RTS Analysis

In 33% of the devices that showed multilevel RTS, we observed a four level RTS. However, the transitions among the levels were not alike. In the first type of multilevel

RTS, independent switching within the odd numbered and even numbered levels are caused by the same first trap, trap A (this will be proven later with more details). In Figure 6-1, the RTS amplitude between levels 1 and 3 has the same magnitude as the amplitude between levels 2 and 4. We define the switching events between levels 1 and 3 as the switching within the 'lower envelope', and those between levels 2 and 4 are identified as switching events within the 'upper envelope'. Modulation of the upper envelope towards the lower envelope and vice versa, is caused by the presence of a second trap that we define as trap B. We will call this type of transistors as opposite trap (OT) devices for nomenclature purpose. There is a second category, which we identify as similar trap (ST) devices. These are typically longer than the OT type devices. Unlike OT type devices, trap A now switches within consecutive bottom two levels (1 and 2) and top two levels (3 and 4), and a second trap creates the envelope modulation (Figure 6-2), which we define as trap C. Gate bias dependence of RTS was studied for both types of devices, while drain bias was kept constant. The mean times in the upper and lower levels, t_{high} and t_{low} respectively, for each trap were found to be faster for the ST type devices. Both traps are found to be acceptor type (negative when full and neutral when empty) in ST devices. The reported results for devices with four level RTS so far have found similar-type trap interaction (STTI), as in our ST devices case [114-116]. However, trap A is found to be acceptor, while trap B is determined as donor type (neutral when full and positive when empty) in OT devices, because of opposite type-trap interaction (OTTI). An interesting observation for trap A is that, the switching inside lower envelope dominates over that in upper envelope at comparatively low gate biases, which then reverses (more transitions in upper envelope) with increased transverse field (Figure 6-1). This was found for all the multi-trap devices that were investigated.
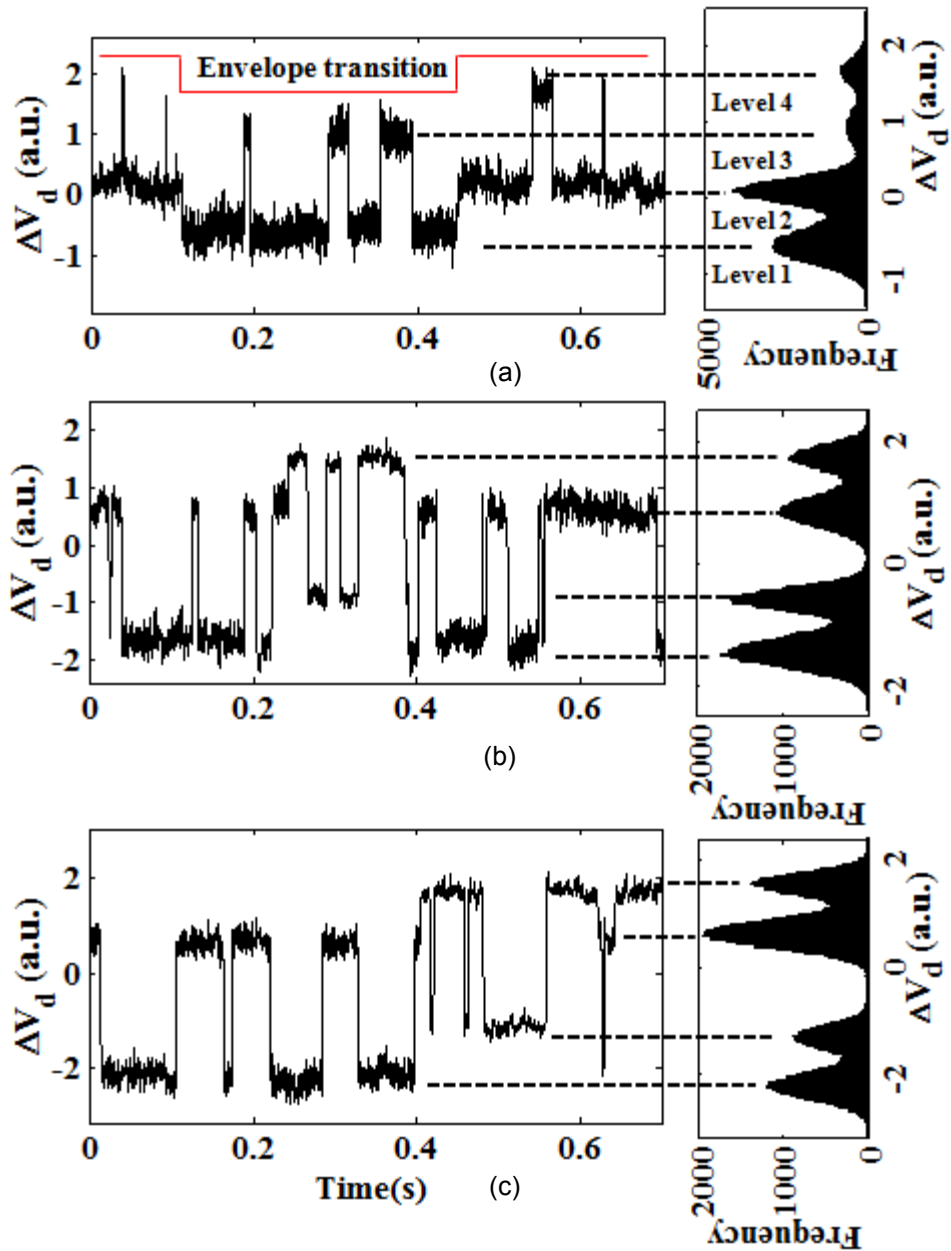
Figure 6-1 Gate bias dependence of RTS in an OT type device. RTS magnitudes are arbitrarily scaled. A small window of RTS are shown which were measured at V_d =0.4 V and (a) V_g =0.7 V, (b) V_g =0.8 V and (c) V_g =0.9 V. For each time domain signal, the corresponding amplitude distribution is shown on the right as histograms.
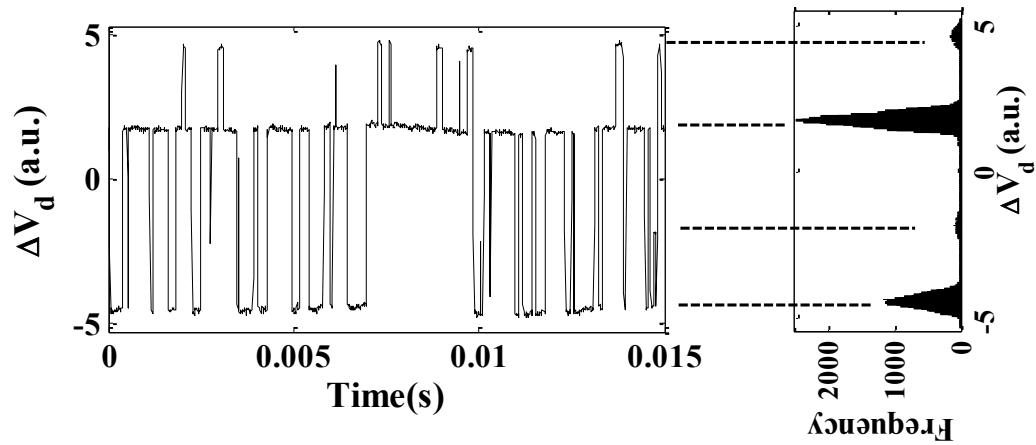
Figure 6-2 A portion of RTS trace found in an ST type device. RTS magnitudes are arbitrarily scaled. RTS measured at V_d =0.2 V and V_g =0.682 V and the corresponding amplitude distribution is shown on the right as histogram.

In the next subsections, we are going to describe the developed strategy to resolve the multilevel RTS waveforms. By merging the transition levels (level 1 with 3 while 2 with 4 in case of OT device, and level 1 with 2 and 3 with level 4 for ST device), the mean times at the top and bottom 'merged' levels are calculated. Then, mean time at the upper and lower envelope levels are calculated for the second trap. Capture and emission time for each trap is determined from their respective gate bias dependence [14, 15]. The time distribution for each level was found to follow a Poisson distribution. Due to overlapping RTS from two traps and their strong gate bias dependence, many exploratory runs were acquired during experimentation. The upper and lower limits for each level (as was shown in Figure 5-2a) were adjusted properly, and to obtain optimized mean times in each of the levels, the number of bins was varied in the time distribution plot to closely follow the Poisson fitting (Figure 5-2b).

6.2.1 Comparison with Existing Analysis Techniques for Multilevel RTS

Uncorrelated complex switching similar to Figure 6-1 or Figure 6-2, found in the NMOS devices, were described in literature [79, 114] as the sum of several transients owing to several independent traps, without providing much insight to the gate bias dependence of the RTS. The physical mechanism has not been described in detail for the amplitude shift from upper to lower envelope and vice versa. It was assumed that the same type of traps would be present in the oxide (just like the trap A and trap C in our ST devices) with two different RTS amplitudes. The novelty of our work lies in the fact that we found the second trap can be either donor or acceptor type in different devices with OTTI or STTI with trap A. Therefore, a simple overview of superposition of two uncorrelated trap does not provide any detail into the trap behavior.

We eliminated the probability of coupled switching [79], where switching of one trap would depend on the state of the second trap. In such a case, the traps would be located in close proximity [114] and in a more complex scenario; two or more electrons could be captured at the same defect location [15]. Since our devices showed that the second trap (trap B), which causes the envelope switching, can be of donor or acceptor type, competition between two different time constants of same type of traps cannot fully explain the general RTS behavior.

Another feature of the obtained RTS characteristics is that, the signal time record is not strictly Gaussian distributed at each distinctive level. The overlaps in the amplitude histograms are caused by other background noise generating sources and the measurement system, which cannot be completely eliminated [42]. For a non-overlapping RTS signal case, each distinct level will exhibit a clear Gaussian distribution with the standard deviation being equal to the mean value of the exponential distribution [15] and ratio of RTS amplitude to background noise would be high [117]. However, in practice, all

119

the random signals are observed with smaller ratio of RTS to background noise which makes the direct determination of individual non-Gaussian mean switching times almost impossible. A method to separate individual time domain dominant transition levels was proposed based on isolating time domain and background noise components from the measured signal [42]. This is based on an ad-hoc assumption that RTS is a Marcovian process of random switching in between two states and the background noise is perfectly Gaussian. This method works for two level overlapping signals which require cumbersome statistical analysis and data redistribution, and mean capture and emission times are considered as fitting parameters in the iterations. Another method to find minimum jump-threshold among different RTS levels by separating *1/f* noise component in each run was described in [102]. This requires a number of iterations to find the plateau in the jump threshold vs. *1/f* noise measurements. Several other methods for detecting and analyzing four level RTS from histograms have been proposed [42]. However, all of them require statistical analysis or much iteration, and based on four independent level analyses, which is not applicable to our RTS data.

6.2.2 Proposed Algorithm for Analyzing Multilevel RTS with Envelope Transitions

Here, we proposed a simple method for analyzing multilevel RTS which does not require a long iterative procedure. The flow chart is shown in Figure 6-3. The analysis starts with plotting the RTS histogram and by identifying the top and bottom limits for each level to make each level as perfect bell shaped as possible. So, for four level RTS, we should observe four dominant bell shapes with some data overlaps. Then the data points are refined or filtered such that any data point in between the bottom level's maxima and the consecutive top level's minima is taken back (refined) to that bottom level with a RTS magnitude assigned as equal to the last good data point in that

particular bottom level. In this way, all data points will be assigned to designated levels, and data overlaps in successive levels are now eliminated. Of course, we made sure that the number of refined points does not exceed 2% of the total measured data points.
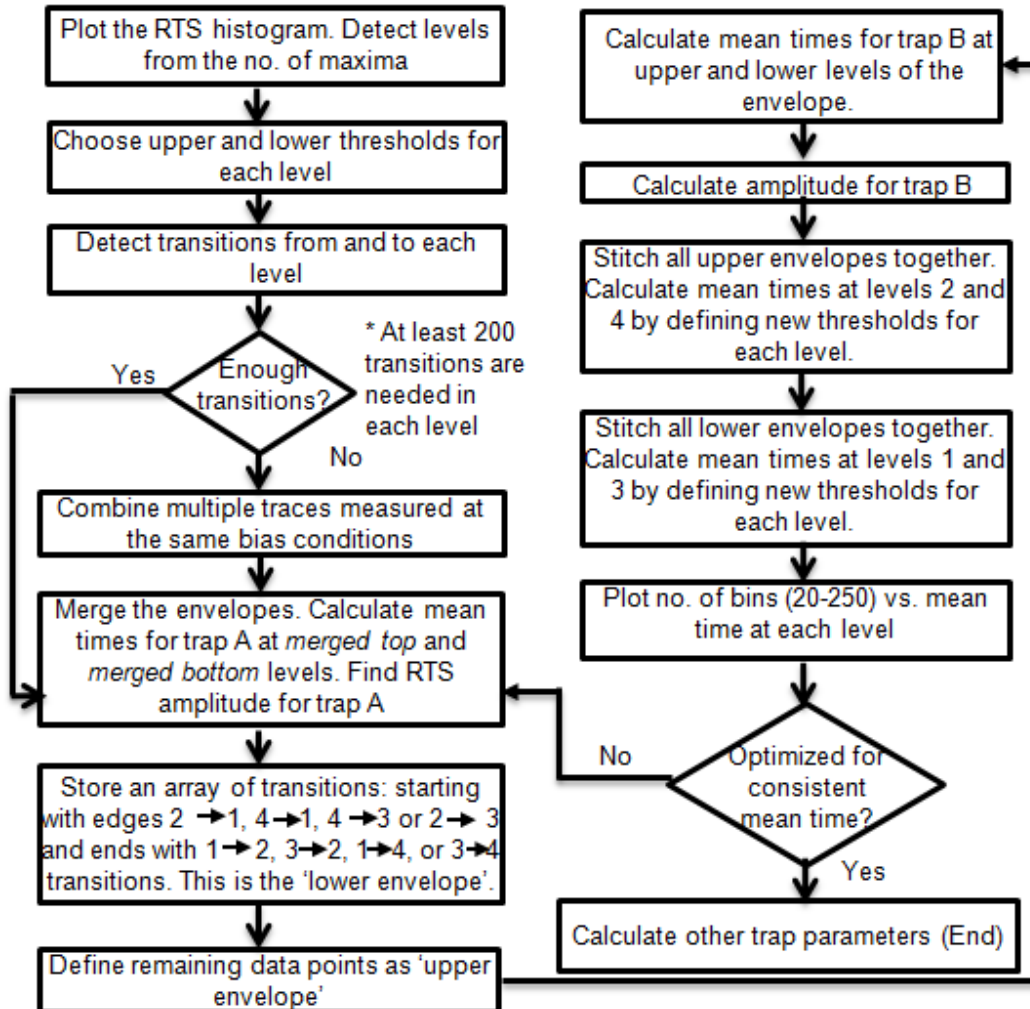
Figure 6-3 Flow chart of the proposed algorithm

The next step is to determine the number of transitions from and to each level. Due to instrument's limitation of acquiring data for longer time, several RTS traces of switching events might be needed to be combined and analyzed at the same bias condition. We assume that since the measurement condition was identical, several consecutive traces can be stitched together without introducing large error. Next step is to merge the fluctuation levels (as mentioned above, for OT and ST type devices), that are caused by trap A. To calculate mean times for trap A at 'merged top' and 'merged bottom' levels in Figures 6-4(a) and 6-4(b), we define new thresholds for each merged level's top and bottom cut-off limit. This step is succeeded by plotting a histogram of time distribution for each level and also doing a Poisson distribution fitting (as was discussed in chapter 5). Thus, we obtain the mean time in each merged level. This is shown in Figures 6-4(c) and 6-4(d).

Meanwhile, optimization of the Poisson distribution is vital, as this can mislead to erroneous mean time extraction. The mean times at each of the levels discussed so far are plotted as a function of number of histogram bins (Fig. 6-5). From the plateau in the mean times plot, we can easily determine the appropriate number of bins for each level to get exponential time dependency in that level to be in agreement with the corresponding Poisson distribution.
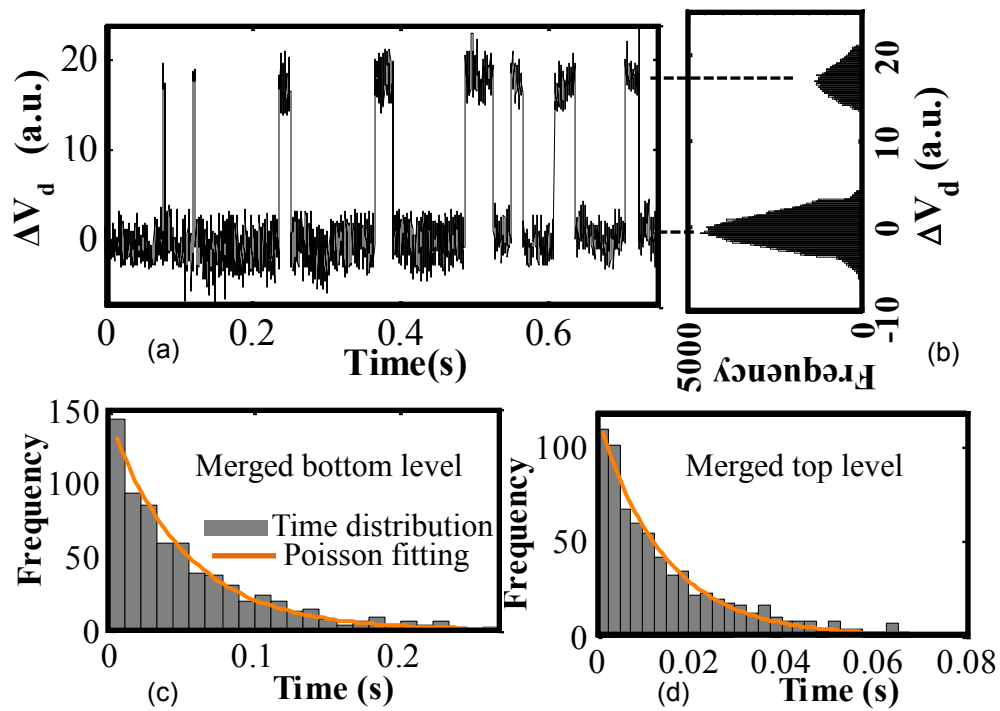
Figure 6-4 (a) A small window of time domain signal after levels 1 and 2 are merged, and levels 3 and 4 are merged. (b) The corresponding histogram after merging the levels. From the merged levels, time distribution and Poisson fitting is shown for (c) merged bottom level and (d) merged top level. RTS was measured at V_d=0.4 V and V_g=0.72 V. RTS magnitudes are arbitrarily scaled.
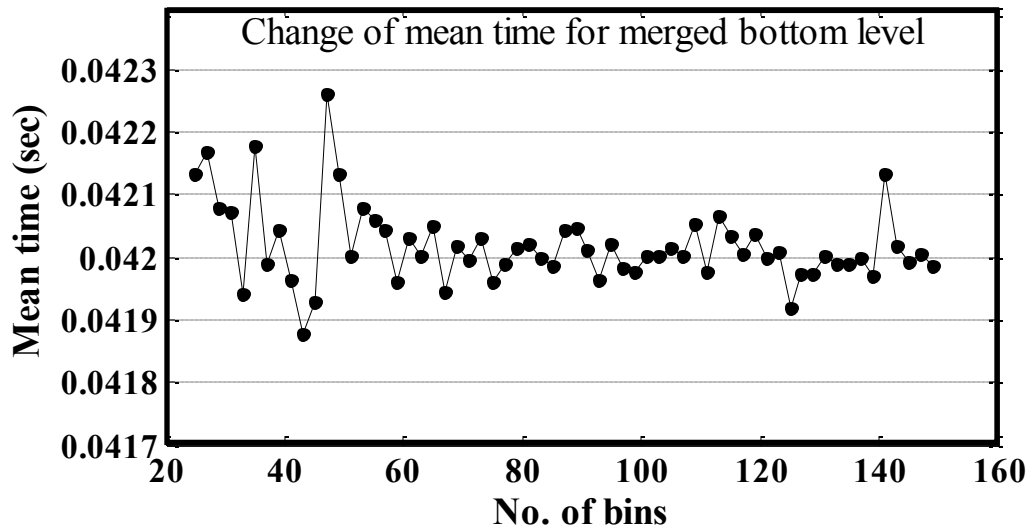
Figure 6-5 Optimization for the number of bins of time distribution in the merged lower level of Figure 6-4. Selecting 51 bins in this case, matches most accurately with the Poisson distribution fitting as was shown in Figure 6-4c. Mean time due to selecting different number of bins in this case, can vary from 0.0419 sec to 0.0422 sec. This introduces about 0.72% error if 20-50 bins are used. For higher number of bins, the error margin reduces to 0.23%.

We have observed that the RTS amplitudes for trap A in the top switching levels (within upper envelope) and in the bottom switching levels (within lower envelope) appear to be the same for both types of devices (Figures 6-6 and 6-7). In Figure 6-6, for OT devices, RTS magnitude between levels 1 and 3 coincides with that between levels 2 and 4. This also matches with the RTS amplitude obtained from the merged histogram, which was shown in Figure 6-4(b). Similar result is observed in Figure 6-7, where RTS amplitude between 1 and 2 matches with that between levels 3 and 4 for ST type devices. This quantitatively means that the transitions within each envelope are due to the capture and emission of charge carriers by the same trap (trap A).
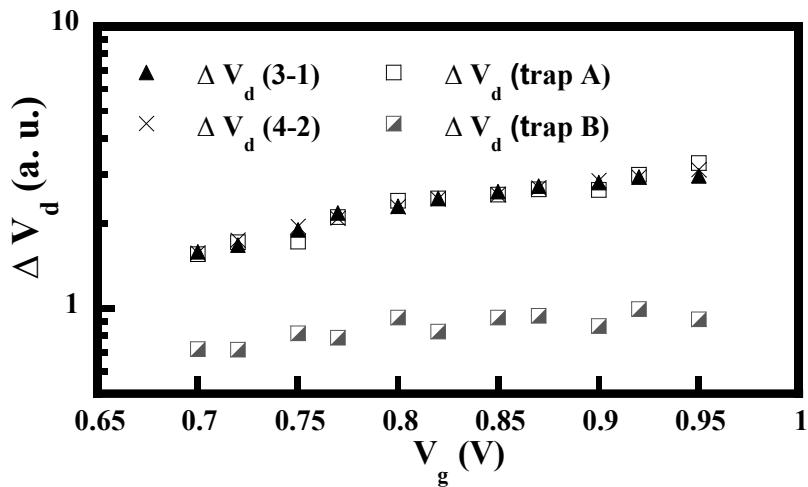
Figure 6-6 RTS magnitudes as a function of gate bias (V_d=0.4 V) for the OT type

device in Figure 6-1. RTS magnitudes obtained between levels 1 and 3 coincide with

those in between levels 2 and 4, which also show similar trend as merged amplitude

of trap A. Trap B has a lower RTS amplitude. Y axis is arbitrarily scaled.
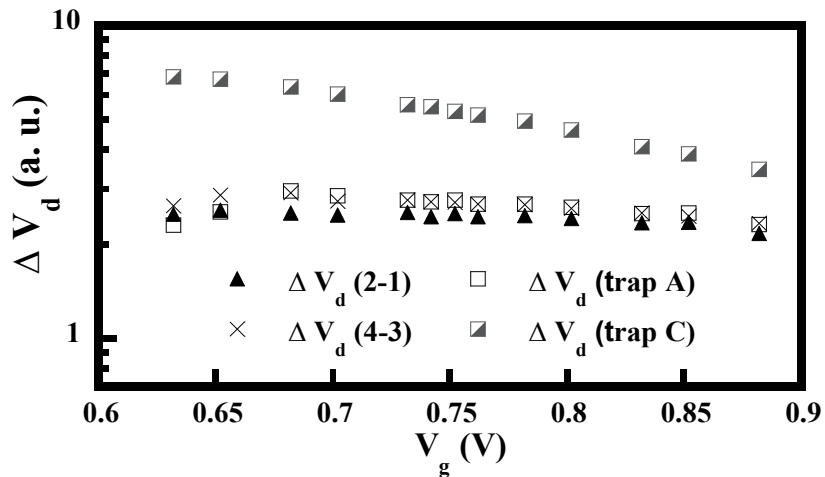
Fig. 6-7 RTS magnitudes as a function of gate bias (V_d=0.2 V) for the ST type transistor

as was shown in Figure 6-2. Y axis is arbitrarily scaled. Trap A has lower amplitude than

trap C in this case.
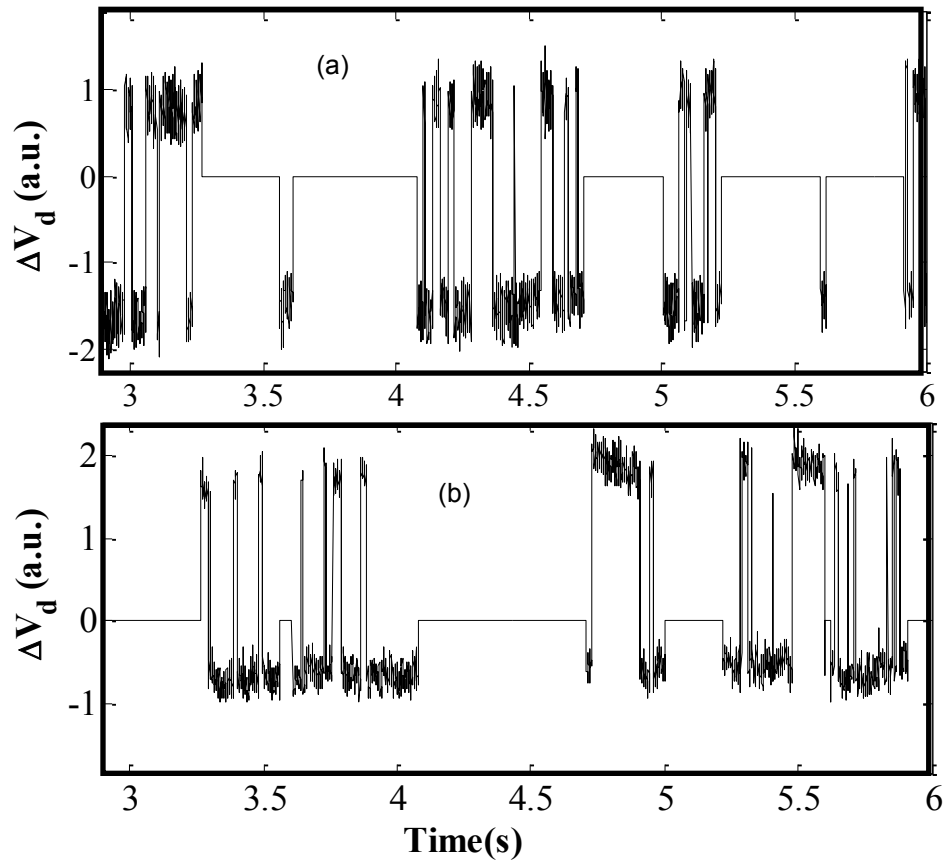
Figure 6-8 Method of envelope separation. (a) Switching within the lower envelope and

(b) switching within the upper envelope only for the OT device. RTS was measured at V_d

=0.4 V and V_g =0.82 V.

However, the mean time in each individual level might not be equal to its counterpart

equivalent level in the merged level analysis, in most instances. To explain that

observation, we first separated the upper and lower envelopes. The mean time in each

individual level is calculated by separating the lower envelope transitions from Figure 6-1,

to keep only those data points which belong to the transitions occurring between levels 1

and 3 (Figure 6-8a). In the numerical program, this is done by identifying the indices of

126

the positions from where the desired transitions occur. The mean time at level 1 and at level 3 are separately calculated by defining top and bottom limits for each of these levels and then doing time distribution analysis again with Poisson fitting. The remaining data points in the measured signal after removing the data points in lower envelope are kept in another array, which now contains only the data in the upper envelope (Figure 8b). The mean time at level 1 is found to follow the trend of mean time in level 2 (Figures 6-9a); however, they are not exactly the same. Same is the case with levels 3 and 4 in Figure 6-9b. Hence, finding the mean capture and emission times for trap A is accomplished by a statistically robust procedure i.e. from the time distribution after merging the respective levels of RTS for either type of devices (Figure 6-9c). Comparing Figure 6-9a and 6-9b with Figure 6-9c, it can be observed that mean time at the merged bottom level shows almost the identical mean time to that at level 1 and at level 2, at different gate biases. This confirms the viability of our 'merged level' analysis.

Next, we need to analyze the mean times for the second trap. This is accomplished by a straightforward Poisson distribution fitting to the time spent at each of these upper and lower envelopes of Fig. 6-8. The extracted mean times for trap B are shown in Figure 6-10 for the OT device. Following the same methodology, the gate bias dependence of the mean times at levels 1 and 2 are shown in Figure 6-11a, and at levels 3 and 4 in Figure 6-11b. Although the mean time characteristics in ST devices is similar to OT devices for trap A (Figure 6-11c), discrepancy is observed in the mean times for the second trap (trap C) causing envelope transitions. This is shown in Figure 6-12 for the ST device. In this case, the mean time for trap C at the lower envelope decreases, while that for the upper envelope increases, unlike for trap B in OT devices.

127
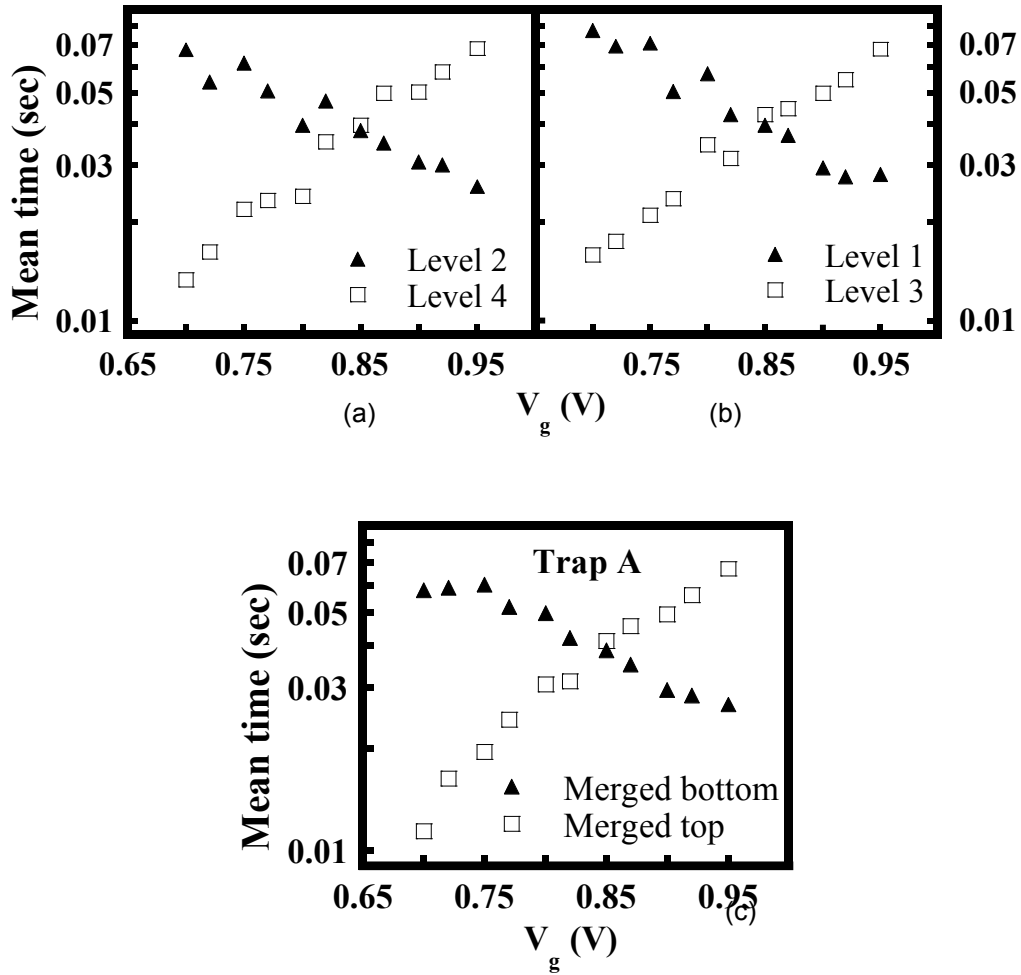
Figure 6-9 After the envelopes are separated by the method as illustrated in Figure 6-8, mean times are shown (a) for levels 2 and 4 in the upper envelope and (b) for levels 1 and 3 in the lower envelope.(c) Mean times for trap A for the OT device as a function of gate bias. All the measurements were done at V_d =0.4 V.
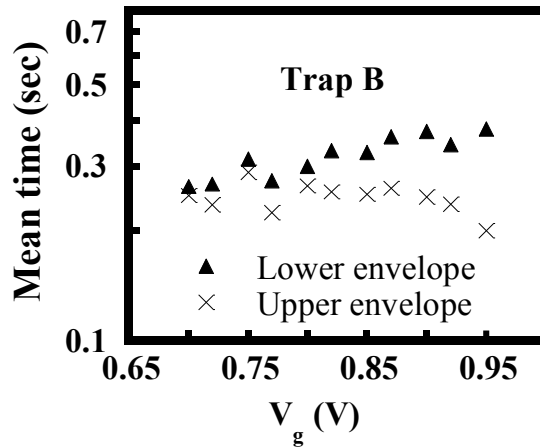
Figure 6-10 Mean times for trap B for the OT device as a function of gate bias. RTS were

measured at V_d =0.4 V.

Since trap B and C modulate the switching from upper envelope to lower envelope in their respective devices, the RTS magnitude calculation for these traps is not straightforward. Since the RTS magnitude for switching between levels 1 and 3 is identical in OT devices, the amplitude for trap B is calculated as follows. First we averaged the RTS magnitudes at which the frequencies of occurrences for levels 1 and 3 are at their respective maximum (as shown in the histograms in Figure 6-1). Then we calculated the average in case of levels 2 and 4. Finally, we subtracted the former average from the latter average (Figure 6-6). For ST type devices, fast switching occurs within levels 1 and 2, which is shifted to fast switching between levels 3 and 4 and vice versa. Hence, in this case, RTS amplitude for trap C was extracted by averaging the maxima of levels 1 and 2, and subtracting that from the average of the maxima of levels 3 and 4 (Figure 6-7).
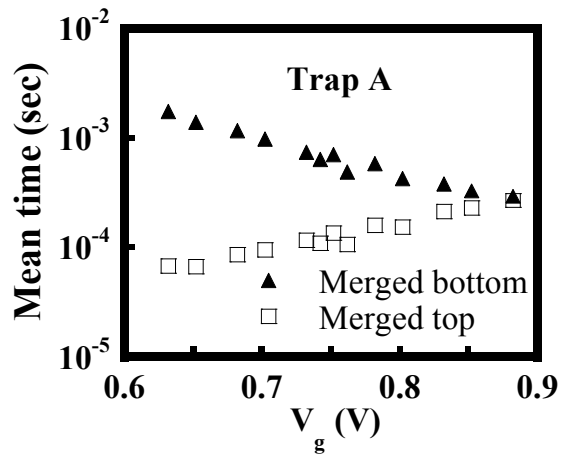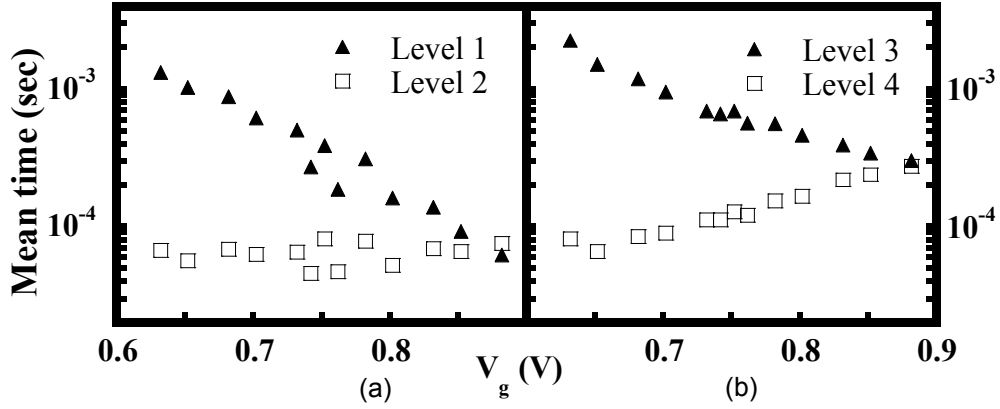
Figure 6-11 Mean times as a function of gate bias (a) for levels 1 and 2 in the lower

envelope and (b) for levels 3 and 4 in the upper envelope. (c) Mean times for trap A for

the ST device as a function of gate bias. RTS were measured at V_d =0.2 V.
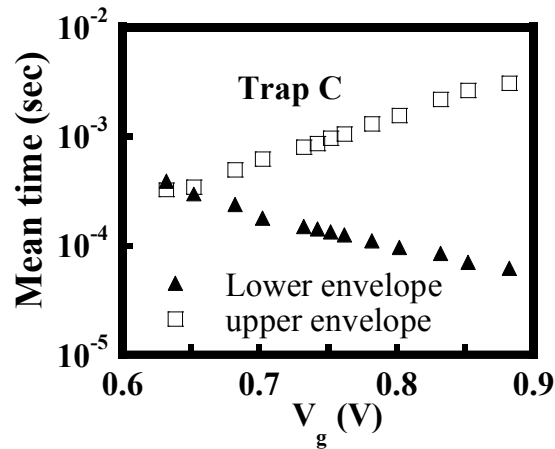
Figure 6-12 Mean times for trap C for the ST device as was shown in Figure 6-2. RTS

were measured at V_d =0.2 V.

6.2.3 Applicability and Limitations of the Proposed Analysis Technique

The methodology described so far has been applied to all the four level RTS waveforms that we obtained in the tested devices. We did not observe independent switching like [14], where all the transitions would be from level 2. It was also shown that the fast switching can be possible either in between two consecutive levels (ST devices), or within the odd numbered and even numbered levels (OT devices). We observed that the transitions from levels 1 to 4 (and vice versa) are negligible in any device. Obviously, this method of RTS analysis based on envelope analysis will not work if the RTS magnitude between corresponding levels in each envelope were not the same (for example, if $\Delta V_{N1-3} \neq \Delta V_{N2-4}$ in OT devices). Typically, more than four level RTS is rarely seen in literature, as *1/f* noise will be more observable if several traps are present. Please note that, if the measured signal is such that the fluctuation in-between levels dominates over the RTS and the levels are overlapping in histogram, then data refinement before merged levels analysis will result in erroneous mean time extraction. This high in-

131

between level fluctuation is a strong limitation in other reported methodologies as well [102, 117]. Our developed methodology, will also work for simple two level RTS, where there is no need for envelope analysis.

6.3 Extraction of Other Trap Properties

From the RTS analysis in time domain, we have shown the method to extract mean times in different levels and how to calculate the RTS amplitude. There are several other trap properties that can be determined from the aforementioned analysis. These are capture and emission time, trap type, trap energy and location, capture cross-section and screened scattering coefficient. However, chemical nature of the traps and trap binding energy cannot be identified merely from room temperature RTS measurements.

6.3.1 Determination of Mean Capture and Emission Times

Once we plot the mean times at each level as a function of gate bias, we can identify which level belongs to capture time and which one defines mean emission time. This methodology was described in Chapter 5 in detail and the results are shown here. In Figures 6-9c and 6-11c, the mean time at the merged bottom level decreases, while that for merged top level increases with gate bias. According to Equations (5-6) and (5-11), increasing the gate bias decreases the mean capture time. Hence, merged bottom level defines mean capture time in both type of devices, and merged top level is responsible for the mean emission time for trap A. However, for the second trap, we found dissimilar results. For the OT devices, mean time at lower envelope increases, which enables us to identify that as the emission time (Figure 6-10), while for ST devices, the lower envelope determines mean capture time (Figure 6-12).

6.3.2 Determination of Trap Type

Referring to Section 5.4, for an electron capture, a repulsive trap is identified when the mean time in the lower level for an RTS decreases with increased gate bias. This is because, a proportional increase in the capture rate and trap occupancy results in a decrease in the mean capture time. Therefore, trap A is acceptor type in both ST and OT type devices, where mean time for the merged lower level always decreases. In case of ST type devices, the similar result holds for trap C as well (Figure 6-12), since the mean time at lower envelope decreases with gate bias. However, trap B in OT devices shows the opposite behavior; the mean time at upper envelope decreases, suggesting it to be a donor type trap. This is supported by the extracted RTS amplitude in Figure 6-6, where the magnitude of RTS for trap B is found to be smaller than that for trap A. This means that the carrier mobility fluctuation and scattering events counteract with carrier density fluctuation at increased gate biases, and this leads to lowering of RTS amplitude [80]. This is explained in more detail in section 6.3.5. Reports have shown that donor traps are typically observed below 70K [94, 95], whereas we obtained two different type of traps in the same device at room temperature. This is explained more in terms of trap energy in the next subsection. From the mean time characteristics, both traps are found to be independent of each other, as occupancy of one trap does not impact on the average capture or emission time for another trap, and hence, they plausibly communicate independently with the channel.
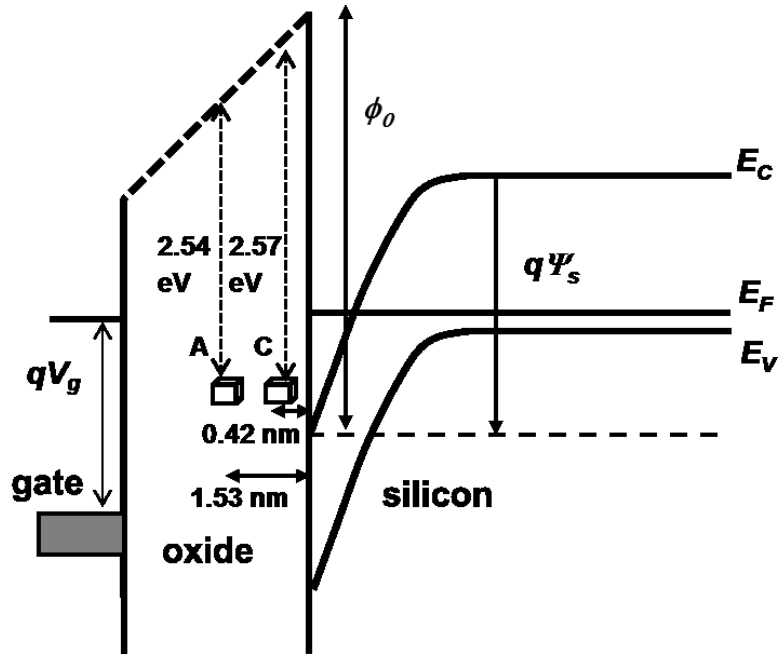
Figure 6-13 Energy band diagram at the source end of the channel showing the position and energy for each trap for the ST type device. Both trap A and trap C are above the conduction band edge of Si in this case.

6.3.3 Computation of Trap Energy and Distance

Trap energy is calculated with respect to the conduction band edge of SiO$_2$ by using Equation (5.12). For both the traps in ST type devices, trap energy is found such that the traps are above E_C (Si). $\left(E_{C_{ox}} - E_T \right)$ for trap A is found as 2.54 eV and for trap C is 2.57 eV; both are lower than electron affinity, ϕ_0 (3.1 eV). This indicates that both traps are repulsive centers, as the interface states within or above E_C can only be acceptor traps [118]. The corresponding approximate energy band diagram is shown in Figure 6-13. In a typical OT type device, trap A has energy of 2.86 eV, which is again above E_C of Si. For trap B, the energy is found to be 4.1 eV, which puts it near the valence band

134

edge (as shown in Figure 6-14). According to [118, 119], interface states below the conduction band are only donor states. In other words, acceptor states are either completely absent or can be merely found at a lower energy level than the donor states, near and above the valence band. Therefore, trap B is not an acceptor trap. Since the traps are energetically apart, OTT or STT interaction between them does not cause the mean time for trap A to change in presence of trap B, only the envelope shifts to upper and lower levels.
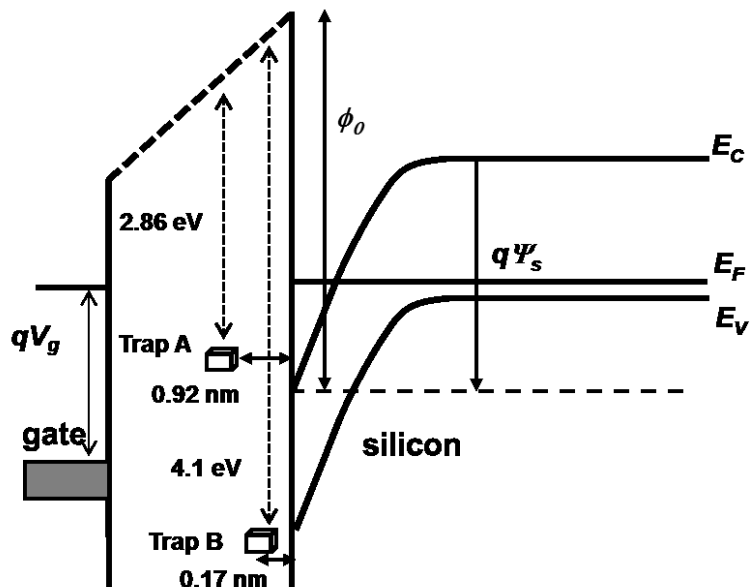
Figure 6-14 Energy band diagram at the source end of the channel for the OT type device. Trap A is located above the conduction band edge and trap B is near the valence band edge of Si.
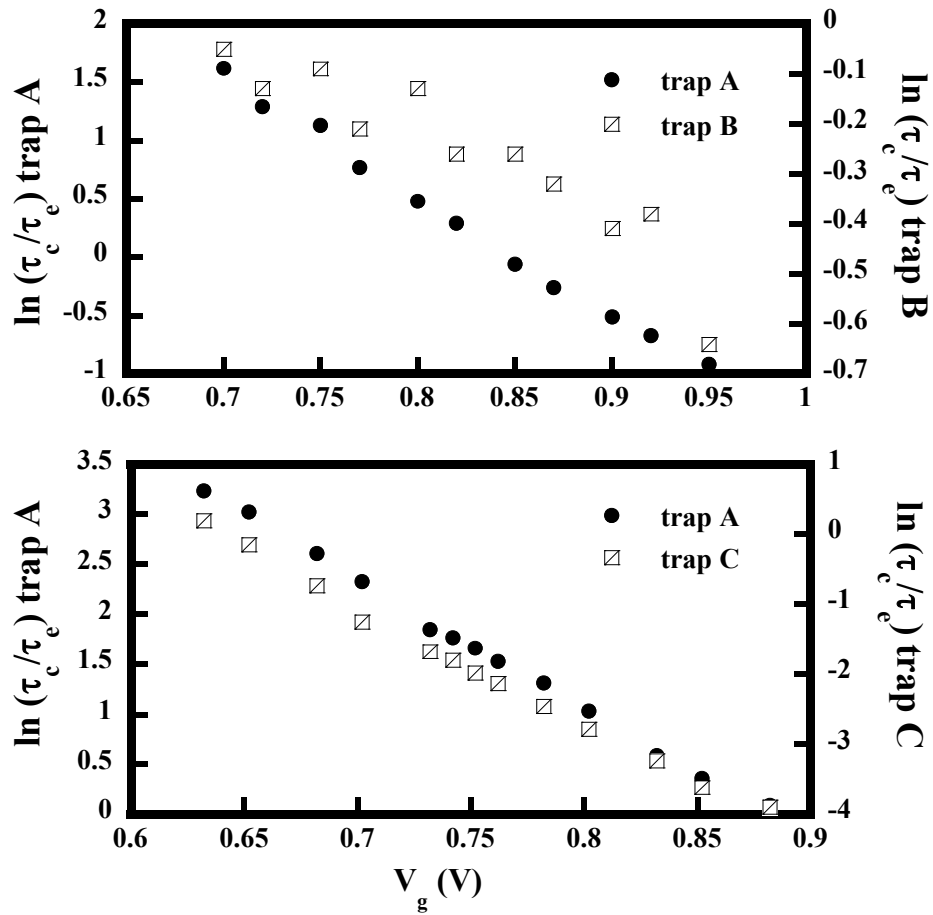
Figure 6-15 Determination of trap location into the oxide from capture to emission time ratio for (a) traps A and B in case of OT device (RTS measured at V_d =0.4 V) and (b) traps A and C in case of ST type device (RTS measured at V_d =0.2 V). The slope from each line gives the trap distance into the oxide.

The trap distance into the oxide from the interface can be obtained from Equation (5.13), by obtaining a slope for $\ln \bar{\tau}_c / \bar{\tau}_e$ vs. V_g plot for each trap. This is shown in Figure 6-15 for both ST and OT type devices. Trap A is found to be deeper (0.92 nm) in OT

device, which is an attractive center, compared to the donor trap B (0.17 nm). A question may arise, why the amplitude for trap B is lower in the OT devices although it is closer to the interface? The reason lies in the types of the embodiments. As explained so far, donor trap will have lower RTS magnitude, reinforced by lowering of scattering when such a trap is occupied [94]. Hence, both trap A and B are strongly affected by scattering i.e. carrier screening at strong inversion, albeit the consequence of scattering is dissimilar. To the contrary, both the traps are acceptors in ST device, and nearer trap C (0.42 nm) from interface has larger RTS magnitude compared to the distant trap A (1.53 nm), as expected (shown in Figure 6-7).

6.3.4 Capture Cross-Sections

At room temperature, capture cross-section can be calculated by using Equation (5.6). For the OT device, we obtained σ to be 2.5×10^{-26} cm^2 for trap A and 3.5×10^{-27} cm^2 for trap B. Larger capture cross-sections are obtained in ST devices; 1×10^{-23} cm^2 for trap A while 7×10^{-24} cm^2 for trap C. This can be realized from Equation (5-6) and by comparing Figures 6-9, 6-10, 6-11 and 6-12. Since the thermal velocity is assumed to be constant in strong inversion, change in capture time has a profound effect on determining capture cross-sections.

Since the transitions in OT type device are much slower than those in ST devices, the capture cross-section is correspondingly lower for OT type interaction devices. The traps are physically apart, and the capture cross-sections in the same device differ by an order of magnitude for the two traps. The extracted capture cross-sections agree well with the reported results, where it is mentioned that the capture cross-section ranges from 10^{-22} -10^{-26} cm^2 [15]. Lower σ values, as low as 10^{-29} cm^2, are also obtained in case of traps in NMOS transistors [120]. Hence, four orders of difference

in the obtained cross-sections in two opposite type trap interaction devices is not unusual [120], and suggests variability of σ from device to device. A point worth mentioning here is that such low capture cross-sections are consistent with the fact that these defects have reduced capture probability compared to a bulk trap and hence, are located physically inside the oxide; not in the bulk Si [91].

6.3.5 Screened Scattering Coefficient and Physical Origin of Multilevel RTS

In case of *1/f* noise in LDMOS, we have demonstrated that the physical origin of noise is due to correlated carrier number and mobility fluctuation. Since *1/f* noise and RTS noise have the same physical origin [15], a similar model has been applied for submicron devices [16]. Following that procedure, we can express RTS amplitude as the summation of carrier number and mobility fluctuations as [14-16, 94]

$$\frac{\Delta I_d}{I_d} = \frac{\Delta N_c}{N_c} \pm \frac{\Delta \mu_c}{\mu_c} = -\frac{1}{WL_c}\left[\frac{1}{N_c} \pm \alpha_c \mu_c\right] \tag{6.1}$$

Here, α_c is the screened scattering coefficient and we can approximate $\Delta I_d/I_d \approx \Delta V_d/V_d$ in strong inversion [14]. The ± sign symbolizes whether the trap is acceptor or donor type as was discussed in Chapter 3. The first term in Equation (6.1) represents the number fluctuation term, which determines the carrier screening by the traps in the oxide [94]. In the MOSFET linear region operation, when the drain bias is very low, $\Delta V_d/V_d$ is expected to decrease with increased gate bias (increased channel carrier screening) for a simple two level RTS in presence of an acceptor trap. However, a deviation is observed from the expected behavior in case of OT type interaction, when two opposite type traps are present. The ST devices have two acceptor type traps, and both traps have similar energy with respect to the oxide conduction band edge. At higher

transverse electric field and fixed low drain bias (in linear region), average carrier mobility increases due to reduced Coulomb scattering (higher screening). Therefore, except for the anomalous behavior at relatively low gate biases for trap A in Figure 6-7, RTS amplitudes for the traps in these devices decrease with increased gate bias, similar to the observations in the published reports [14-16, 94]. To the contrary, OT devices have one acceptor (trap A) and another donor trap (trap B), located away from each other in terms of energy (one near conduction band and another near valence band edge). The traps are separated in terms of physical position as well, and both trap amplitudes remain unaffected or show a little increase with gate bias (Figure 6-6). The physical reason is not known for such a phenomenon at this moment.

The importance of mobility fluctuation in the RTS noise generation mechanism can be explained to some extent, by analyzing the drain bias dependence of the RTS amplitudes. When V_d is increased, keeping the gate bias constant, the inversion charge carrier density, N_c can be considered to have negligible variation [78]. In that case, the normalized drain voltage or current fluctuations should vary with $\alpha_c \mu_c$ according to Equation (6.1). In Figure 6-16, we verified this by comparing normalized drain voltage fluctuations for both traps (A and C) with average inversion carrier mobility (μ_c), which was normalized with respect to the low field mobility (μ_0). At high V_d, lateral electric field causes mobility degradation with respect to low field mobility, which is not the case at relatively low drain biases [78, 121]. As illustrated in Figure 6-16, both normalized RTS magnitude and mobility degradation follows the identical trend with respect to the drain bias. Since mobility fluctuation term ($\Delta\mu_c / \mu_c$) is equal to $\alpha_c \mu_c$, this result shows that a significant contribution to measured drain current fluctuation comes from the surface

mobility fluctuations in submicron analog transistors, similar to the observation in [78]. It was also concluded in [78] that the normalized voltage fluctuations and mobility fluctuations will also follow the same decreasing tendency when V_d is varied, while V_g is kept constant at other different fixed gate voltages. However, we did not verify that observation in our devices.
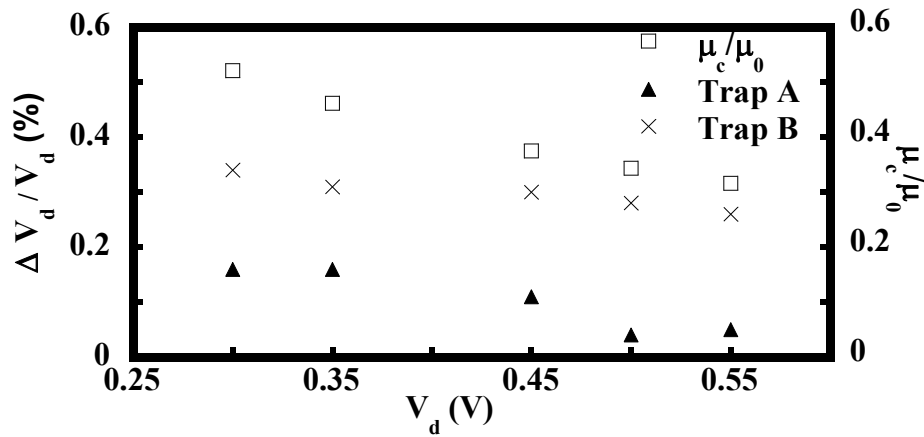
Figure 6-16 Relative surface electron mobility and drain voltage fluctuations for both the traps plotted as a function of drain bias for the ST device. Measurements were taken at V_g =0.702 V).

The magnitudes of α for each trap are shown in case of OT and ST devices in Figure 6-17 as a function of gate biases. It is found that α for all the devices follow the empirical equation [14, 16]: $\alpha = K_1 + K_2 \ln(N)$, where K_1 and K_2 are two constants. According to K. Hung *et al.* [49], this is consistent with the Conwell-Weisskopt formula applicable for a screened Coulomb scattering center.
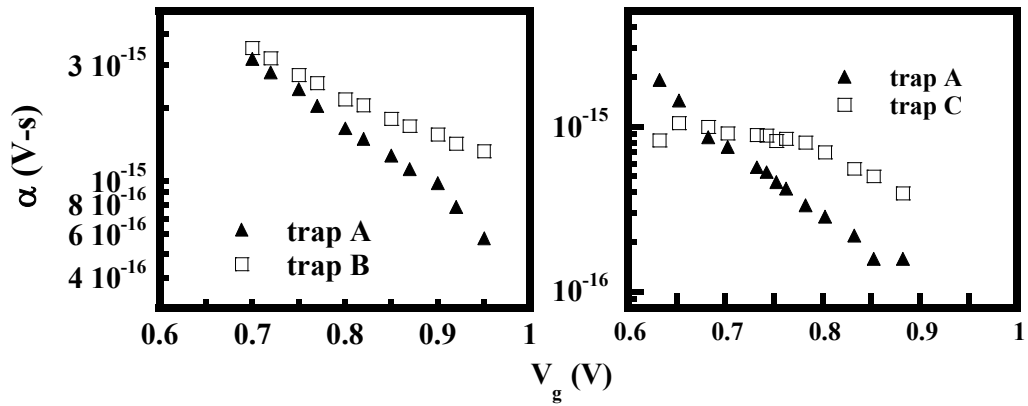
Figure 6-17 Dependence of screened Coulomb scattering coefficient on gate bias for the

(a) OT type device (RTS measured at V_d =0.4 V) and (b) ST type device (RTS measured

at V_d =0.2 V).

Table 6-1 Summary of the Trap Properties for ST and OT Type Devices.

Device type	Trap	Trap type	$\left(E_{C_{ox}} - E_T\right)$ eV	x_T (nm)	σ (cm^2)
ST	A	acceptor	2.54	0.42	1.0×10^{-23}
	C	acceptor	2.57	1.53	7.0×10^{-24}
OT	A	acceptor	2.86	0.92	2.5×10^{-26}
	B	donor	4.10	0.17	3.5×10^{-27}

The values of α are consistent with reported results as well [14, 15, 120]. Godoy

et al. [78] found α to be 3.5×10^{-15} - 5.5×10^{-15} (V-s), while Nuditha et al. [14] found higher

magnitudes of 1×10^{-14} - 6×10^{-14} (V-s), depending on the gate bias, although a direct

comparison might not be meaningful, as the measured voltage and voltage rating of the

devices are dissimilar. Nevertheless, Coulomb scattering mechanism dominates in the scattering process [49], and is mainly responsible for surface mobility fluctuation in the analog NMOS devices. The summary of the results obtained for different traps is presented in Table 6-1.

6.4 Discussion and Summary

The mean capture time for a trap is known to vary exponentially with gate bias [122], while mean emission time depends on capture time as well as the difference between the trap energy and Fermi energy. The increase in the emission time for all the traps in the investigated devices is possibly due to increase in the activation energy (not measured in this work) with increase in channel carrier density, which overcomes the Coulomb energy [91]. For trap A in OT devices, we observed that capture and emission time intersects (Figure 6-9c). Theoretically, this intersection can be attributed to 50% trap occupation probability, which in effect indicates the crossing of trap energy level with Fermi energy [107]. Another interesting feature of the RTS is that the envelope switching is slower in OT devices, while faster capture-emission processes goes on for trap A (trap A is faster). On the other hand, mean times are of comparable magnitude for the ST devices. We did not observe any radical change in the mean capture time or emission time characteristics for any of the traps, as was observed by Schulz [91].

The trap position is found by researchers in a wide range from 0.45 nm [123], or 0.5 nm [95] up to 3.7 nm [94] from the interface (z_T =0) for acceptor type trap centers in submicron transistors. We obtained acceptor traps from 0.9 nm towards 1.53 nm deeper, which is well supported by the references. We can also conclude that these traps are process induced. In general, process induced traps are deeper than stress induced traps (i.e. hot carrier stress induced traps) [18]. On the other hand, donor type traps are usually

142

shallower than acceptor counterparts [95]. Therefore, it is not unusual to obtain donor traps at as low as 0.17 nm from the interface. In present day process technologies, where the gate oxide thickness has shrunk to a few nanometers, trap position should be within a reasonable distance (within a few monolayers) into the oxide. Please note that the trap position along the channel has not been accounted for this dissertation.

The capture cross-section is a strong function of lattice relaxation energy. To have a trap center to be large in a non-radiative multiphonon emission process, the equilibrium trap energy level should be near E_C of Si and after capture it should relax to near E_V, to make sure a substantial energy relaxation [124]. In our devices, the capture cross-sections were obtained to be very low, so the capture probability is low, which is another indication that the traps are in the oxide; not in the bulk Si [80, 124].

The discrepancies in trap activation energy from different energy subbands due to quantum-mechanical effects [122, 125] are ignored in this work, since we performed the measurements at room temperature only. Typically energy band quantization is observed in highly doped NMOS transistors, where the conduction band energy is discretized into different energies in strong inversion. Similar to the observation of Nuditha *et al.* [126], we did not observe the inverse of capture time to be dependent on n/t_{inv}, rather it does follow Equation (5.6). Therefore, the classical SRH statistics is sufficient to explain the RTS behavior.

Finally, we focused on RTS amplitude obtained from OT and ST devices. There have been reports that anomalously large RTS could be obtained due to sequential trapping of two electrons at the same location, and most likely the traps exhibit several metastable energy states due to electronic reconfiguration [88, 127]. Another proposition is that some traps can be strategically positioned in the inhomogeneous channel to block

143

the channel conduction completely after capturing the charge carriers, which can result in large RTS magnitudes [95, 103, 128, 129]. However, in all of the investigated devices, we found RTS amplitude to be less than 0.4 % of the drain bias, and RTS signal was never ceased to stay at any level. We can therefore, eliminate the possibility of multi-electron trapping in the same location and the chances of trap metastability in our NMOS transistors.

6.5 Conclusion

In this chapter, we have demonstrated a methodology that was developed to analyze multilevel RTS having envelope transitions. Identification of effective number of traps, their positions in the oxide, trap energy with respect to the oxide conduction band and trap type has been accomplished through analysis of the experimental results. The physical origin of RTS has been explored from the context of number and mobility fluctuation theory, and corresponding screened scattering coefficients for each trap have been calculated. Same kind of trap embodiment (both acceptors) is found in one type of NMOS, while two different types of traps have been identified in another type of device. Acceptor type traps are close to the conduction band-edge of Si and donor type trap is near the valence band edge of Si. The defect properties are found to be consistent with their trap nature/type.

Chapter 7

Conclusions and Summary

In summary, we have demonstrated non-destructive methods of *1/f* noise measurements in frequency domain and RTS noise measurements in time domain to investigate the degradation in state-of-the-art high voltage transistors and analog submicron CMOS devices, respectively. In the first part of this dissertation, we discussed about the investigation of DC stress-induced degradation in LDMOS transistors. Here, a systematic procedure for *1/f* noise measurement in LDMOS is elaborated, and details of the noise analysis and modeling approach are provided. Individual resistance and noise components in the channel and in the extended drain regions under the gate and field oxides are evaluated as a function of stressing duration. The relative contribution of fluctuations from the channel, from the extended drain region under the gate oxide and from that under the field oxide is highlighted. Since the channel noise dominates at low gate biases, the increased drain current noise degradation at relatively higher biases points to more degradation in the oxide-NWell side (overlap region) than the channel-oxide counterpart. Because of the additional fluctuations from this region, we reported here that at relatively higher gate biases, the *1/f* noise behavior deviates from that predicted by conventional noise models. The noise contribution from the extended drain under the field oxide is found to be negligible compared to the other two regions. From *1/f* noise study, we were able to determine the active oxide trap density up to 30% above the band-gap energy. In LDMOS, no other technique explored active oxide traps to that energy level above the conduction band edge of Si reported to date.

Our study is an all-encompassing approach to find the variation of the effective oxide trap density, extent of the traps in the oxide, and characteristics of these dielectric traps at time-zero and as a function of stressing time. Here, we did *1/f* noise modeling

based on experimental results. Following the original Unified *1/f* Noise Model, we took the influence of the oxide traps on the drain current fluctuations as two-fold. Trap occupancy changes the carrier number and charged trap affects the local carrier mobility. In addition to that, we considered non-uniform distribution of the traps, which is more realistic than considering the traps to be uniform throughout the oxide, as is the case in the Unified *1/f* Noise Model. From the developed model, we were able to extract the oxide trap densities before stress, and with the progression of stressing time. We also showed that carrier mobility fluctuation remains the dominant source of low frequency noise in LDMOS devices even with stressing. Finally, an early lifetime prediction method, by using *1/f* noise measurement results, was delineated.

In the second part of this dissertation, we provided the details of RTS measurement system and analysis techniques. Here, we restricted our analysis to multilevel RTS noise only, although two level RTS was also observed at different bias conditions in the investigated devices. From the RTS measurements, we showed that two opposite type of traps can be simultaneously present in a device at room temperature. We named these NMOS devices as opposite trap (OT) type interaction devices. The presence of donor and acceptor type traps in the same device has been justified by their position with respect to the band-gap energy of Si. To our knowledge, presence of two opposite type traps simultaneously active at room temperature has not been reported to date. In other NMOS devices, we found both traps to be acceptors, and we named them as similar trap (ST) type interaction devices. We analyzed the RTS mean capture time, emission time as well as the RTS amplitudes in each case. A data analysis technique is developed for characterizing the RTS, which is based on experimental results. Our method takes into account for the cut-off limits of each of the distinguishable levels in the observed RTS, and shows a simple yet innovative procedure to do signal envelope

analysis and merging of appropriate RTS levels to extract different trap properties. The advantage of our developed numerical method is that it does not involve long iteration steps, as was suggested by some other authors for analyzing multilevel RTS. From the gate bias dependence of mean capture to emission time ratio, we were then able to locate the trap position from the Si-SiO$_2$ interface in the dielectric. We also calculated the trap energy with respect to the conduction band edge of SiO$_2$. Finally, we computed the capture cross-section and screened scattering coefficient for each trap. As a future work, statistical models need to be developed in order to study the RTS noise variability in analog devices. The models need to incorporate the effect of gate and drain bias dependence, as well as the effect of variable temperatures on RTS noise characteristics.

Appendix A

Mathcad Implementation of LDMOS Surface Potential

Mathcad implementation of surface potential calculation (A sample calculation is shown. The substrate doping concentration and carrier density values do not belong to any LDMOS device)

$\varepsilon Si := 11.8 \cdot 8.854 \cdot 10^{-14}$ Permittivity of Si (Fcm^{-1})

$kB := 1.38 \cdot 10^{-23}$ Boltzman constant (JK^{-1})

$Temp := 300$ Temperature (K)

$q := 1.602 \cdot 10^{-19}$ Elementary electron charge (C)

$Nd := 1 \cdot 10^{16}$ Substrate doping concentration (cm^{-3})

$LD := \sqrt{\dfrac{\varepsilon Si \cdot kB \cdot Temp}{q^2 \cdot Nd}}$ Debye length (cm)

$LD = 4.105 \times 10^{-8}$

$vt := kB \dfrac{Temp}{q}$ Thermal velocity (cms^{-1})

$vt := .026$

$ni := 1.38 \cdot 10^{10}$ Intrinsic carrier concentration (cm^{-3})

$Nov := 2.62 \cdot 10^{12}$ Gate-overlap region carrier density (cm^{-2})

$f(\psi s) := 2^{0.5} \cdot \varepsilon Si \cdot \left(\dfrac{vt}{q \cdot LD}\right) \cdot \left[\left[\left(\dfrac{\psi s}{vt} + \exp\left(\dfrac{-\psi s}{vt}\right) - 1\right) + \left(\dfrac{Nd}{ni}\right)^2 \cdot \left(\exp\left(\dfrac{\psi s}{vt}\right) - \dfrac{\psi s}{vt} - 1\right)\right]^{0.5} - Nov\right]$

$\psi s := .56$ Initial test value for surface potential

$\psi ss := root(f(\psi s), \psi s)$

$\psi ss = 0.5625194$ Calculated surface potential

Appendix B

Matlab Program Code for Multilevel RTS Analysis

%% The following program is written in Matlab® for opposite trap (OT) type devices. By changing the levels accordingly, the program can be used for the analysis of RTS in similar trap (ST) type devices. Each part of the program is explained with comments. Initially, limits for different levels are defined, and then merged level analysis is done, followed by envelope analysis. After that, the envelopes are separated, and upper and lower envelopes are analyzed individually. The histograms are plotted for each level, which are not shown in each step to avoid repetition of some of the lines in the following program. The program is written according to the algorithm shown in Chapter 6 (Figure 6-3). This program uses two functions: one is mean_time_func and another one is timehist function. The functions are separately shown in the end.

```
Time=RTS_file(:,1); % RTS_file is the output file created by the oscilloscope, which has two
columns: time and voltage

v_meas=RTS_file(:,2);
actual_sampling_rate= length(v_meas)/(max(Time)-min(Time));

Gain=10000;
v_actual=v_meas/Gain;
resolution=Time(2,1)-Time(1,1);

bins_for_amp=300; % defining histogram bins
nrows=length(v_actual);

%% Define limits for each level. Magnitudes are for representation purpose only.
low_1=-2.53;
high_1=-1.1;
low_2=-9.84;
high_2=-5.98;
low_3=3.18;
high_3=1.37;
low_4=1.44;
high_4=2.4;

%% Putting each datum in individual level according to the limits as defined above

new_v_array=v_actual;
new_t_array=Time;
total_refined=0;

for i=2:nrows
```

```matlab
    if (v_actual(i,1)>= low_1&& v_actual(i,1)<= high_1) || (v_actual(i,1)>=low_2 &&
            v_actual(i,1)<=high_2)...            ||(v_actual(i,1)>=low_3&&v_actual(i,1)<=high_3||
            v_actual(i,1)>=low_4&& v_actual(i,1)<=high_4)
        new_v_array(i,1)=v_actual(i,1);
    else
            new_v_array(i,1)=new_v_array(i-1,1);
            total_refined=total_refined+1;
    end
end

state=zeros(nrows,1);

% Defining state or level (1, 2, 3 or 4) of the first data point only
if new_v_array(1,1)>=low_1 && new_v_array(1,1)<=high_1
        state (1,1)=1;
elseif new_v_array(1,1)>=low_2 && new_v_array(1,1)<=high_2
        state (1,1)=+2;
elseif new_v_array(1,1)>=low_3 && new_v_array(1,1)<=high_3
        state (1,1)=+3;
elseif new_v_array(1,1)>=low_4 && new_v_array(1,1)<=high_4
        state (1,1)=+4;
end

 % Defining state for all the other data points
for i=2:nrows
   if (new_v_array(i,1)>=low_1&& new_v_array(i,1)<=high_1)
      state(i,1)=1;
   end
   if (new_v_array(i,1)>=low_2&& new_v_array(i,1)<=high_2)
      state(i,1)=2;
   end
   if (new_v_array(i,1)>=low_3&& new_v_array(i,1)<=high_3)
      state(i,1)=3;
   end
   if (new_v_array(i,1)>=low_4&& new_v_array(i,1)<=high_4)
      state(i,1)=4;
   end
end
refined_state=state;

% Count transitions
transition_12=zeros(nrows,1);
transition_21=zeros(nrows,1);
transition_23=zeros(nrows,1);
transition_32=zeros(nrows,1);
transition_13=zeros(nrows,1);
transition_31=zeros(nrows,1);
transition_14=zeros(nrows,1);
transition_41=zeros(nrows,1);
transition_24=zeros(nrows,1);
transition_42=zeros(nrows,1);
```

```matlab
transition_34=zeros(nrows,1);
transition_43=zeros(nrows,1);

for i=2:nrows
    if refined_state(i-1,1)==1 && refined_state(i,1)==2
        transition_12(i,1)=1;
    end
    if refined_state(i-1,1)==2 && refined_state(i,1)==1
        transition_21(i,1)=1;
    end
    if refined_state(i-1,1)==1 && refined_state(i,1)==3
        transition_13(i,1)=1;
    end
    if refined_state(i-1,1)==3 && refined_state(i,1)==1
        transition_31(i,1)=1;
    end
    if refined_state(i-1,1)==2 && refined_state(i,1)==3
        transition_23(i,1)=1;
    end
    if refined_state(i-1,1)==3 && refined_state(i,1)==2
        transition_32(i,1)=1;
    end
    if refined_state(i-1,1)==4 && refined_state(i,1)==1
        transition_41(i,1)=1;
    end
    if refined_state(i-1,1)==1 && refined_state(i,1)==4
        transition_14(i,1)=1;
    end
    if refined_state(i-1,1)==4 && refined_state(i,1)==2
        transition_42(i,1)=1;
    end
    if refined_state(i-1,1)==2 && refined_state(i,1)==4
        transition_24(i,1)=1;
    end
    if refined_state(i-1,1)==4 && refined_state(i,1)==3
        transition_43(i,1)=1;
    end
    if refined_state(i-1,1)==3 && refined_state(i,1)==4
        transition_34(i,1)=1;
    end
end

total_transition_12=sum(transition_12);
total_transition_21=sum(transition_21);
total_transition_23=sum(transition_23);
total_transition_32=sum(transition_32);
total_transition_13=sum(transition_13);
total_transition_31=sum(transition_31);
total_transition_41=sum(transition_41);
total_transition_42=sum(transition_42);
total_transition_43=sum(transition_43);
```

```
total_transition_14=sum(transition_14);
total_transition_24=sum(transition_24);
total_transition_34=sum(transition_34);

total_transition=sum(transition_12)+sum(transition_21)+sum(transition_23)+sum(transition_32)
+sum(transition_13)+sum(transition_31)+sum(transition_41)+sum(transition_42)+sum(transition
_43)+sum(transition_14)+sum(transition_24)+sum(transition_34);

time_state=refined_state;

%% Merged level analysis
v_lifted=refined_v;
t_lifted=Time;
avg_level_1=mean(v_actual(state==1));
avg_level_2=mean(v_actual(state==2));
avg_level_3=mean(v_actual(state==3));
avg_level_4=mean(v_actual(state==4));

for i=1:nrows
    if refined_v(i,1)<high_1
        v_lifted(i,1)=refined_v(i,1)+avg_level_2-avg_level_1;
    end
    if (refined_v(i,1)>=low_3 && refined_v(i,1)<=high_3)
        v_lifted(i,1)=refined_v(i,1)+avg_level_4-avg_level_3;
    end
end

nonzero_v_lifted=v_lifted;

boundary_lifted=input('Where you want to put the bottom_boundary line in lifted plot? = ');
lifted_state=zeros(length(nonzero_v_lifted),1);

for i=1:length(nonzero_v_lifted)
    if nonzero_v_lifted(i,1)>boundary_lifted
        lifted_state(i,1)=1;
    else lifted_state(i,1)=0;
    end
end

dura_bottom=zeros(length(nonzero_v_lifted),1);
dura_upperr=zeros(length(nonzero_v_lifted),1);
for k=1:length(nonzero_v_lifted)
    if lifted_state(k,1)==1
        dura_upperr(k,1)=resolution;
    else
        dura_bottom(k,1)=resolution;
    end
end

% plotting Poisson distribution
```

```matlab
bins_bottom=input('Number of bins for bottom level?=');
bins_upperr=input('Number of bins for top level?=');

% for the merged bottom level
level=1;
[mean_time,total_time_bottom,bin_array_bottom,nonzero_level_bottom,
frequencies_of_bottom_levels_in_bins] = mean_time_func(dura_bottom,
level,bins_bottom, sampling_rate);

mean_time_lifted_bottom=mean_time;
total_time_at_bottom=total_time_bottom;
bin_array_at_bottom=bin_array_bottom;
frequencies_of_merged_bottom_in_bins=frequencies_of_bottom_levels_in_bins;

% for the merged top level
level=2;
[mean_time,total_time_upperr,bin_array_upperr,nonzero_level_upperr,frequencies_of_upperr_l
evels_in_bins] = mean_time_func(dura_upperr, level,bins_upperr,sampling_rate);
mean_time_lifted_upper=mean_time;
total_time_at_upperr=total_time_upperr;
bin_array_at_upperr=bin_array_upperr;
frequencies_of_merged_upper_in_bins=frequencies_of_upperr_levels_in_bins;

%% Envelope analysis
prime_v=zeros(nrows,1); % Prime_v is the array of transitions between levels 1 and 3
m=2;
while m<nrows
    if transition_21(m,1)==1 || transition_31(m,1)==1 || transition_43(m,1)==1 ||...
        transition_23(m,1)==1|| transition_41(m,1)==1

        k=m;
        while k<nrows-1
            if (transition_12(k+1,1)==1 ||transition_24(k+1,1)==1 || transition_42(k+1,1)==1 ||
transition_34(k+1,1)==1 || transition_14(k+1,1)==1)|| transition_32(k+1,1)==1
                prime_v(k,1)=refined_v(k,1);
                break
            end
            prime_v(k,1)=refined_v(k,1);
            k=k+1;
        end
        m=k;
    end
    m=m+1;
end

v_normal=zeros(nrows,1); % v_normal is the transitions between levels 2 and 4
for i=1:nrows
    if prime_v(i,1)==0
        v_normal(i,1)=refined_v(i,1);
    end
end
```

```matlab
plot (Time, prime_v);
title ('RTS for lower envelope levels (1 and 3)');

prime_lower_time=zeros(nrows,1);
prime_upper_time=zeros(nrows,1);
for k=1:nrows
    if prime_v(k,1)~=0
        prime_lower_time(k,1)=resolution;
    else
        prime_upper_time(k,1)=resolution;
    end
end

%% separation of levels 1 and 3 from the lower envelope
v_separated_13=prime_v(prime_v~=0);
t_lower=zeros(length(v_separated_13),1);

for i=2:length(v_separated_13)
    t_lower(i,1)=t_lower(i-1,1)+resolution;
end

boundary_13=input ('Where you want to put the boundary line? ');
lower_state=zeros(length(v_separated_13),1);
for i=1:length(v_separated_13)
    if v_separated_13(i,1)>boundary_13
        lower_state(i,1)=1;
    else lower_state(i,1)=0;
    end
end

plot (t_lower,v_separated_13);
title ('RTS lower levels stitched (levels 1 and 3)');

dura_1=zeros(length(v_separated_13),1);
dura_3=zeros(length(v_separated_13),1);
for k=1:length(v_separated_13)
    if lower_state(k,1)==1
        dura_3(k,1)=resolution;
    else
        dura_1(k,1)=resolution;
    end
end

%% separation of levels 2 and 4
v_separated_24=v_normal (v_normal~=0);
t_upper=zeros (length(v_separated_24),1);

for i=2:length (v_separated_24)
    t_upper(i,1)= t_upper(i-1,1)+resolution;
end
```

```matlab
boundary_24=input ('Where you want to put the boundary line? ');

upper_state=zeros (length(v_separated_24),1);
for i=1:length(v_separated_24)
    if v_separated_24(i,1)>boundary_24
        upper_state(i,1)=1;
    else upper_state(i,1)=0;
    end
end

plot (t_upper,v_separated_24);
title ('RTS upper levels stitched (level 2 and 4)');

dura_2=zeros(length(v_separated_24),1);
dura_4=zeros(length(v_separated_24),1);
for k=1:length(v_separated_24)
    if upper_state(k,1)==1
        dura_4(k,1)=resolution;
    else
        dura_2(k,1)=resolution;
    end
end

End of program
```

▪▪

```matlab
%% explanation of mean_time_func function

function
[mean_time,total_time_1,bin_array_1,nonzero_level_1,frequencies_of_1_levels_in_bins] =
mean_time_func(duration_1, level,bins_1,sampling_rate)

Number_of_bin=bins_1;
cumulative_level_1=timehist(duration_1)';
sorted_cum_level_1=sort(cumulative_level_1,'descend');
nonzero_level_1=sorted_cum_level_1(sorted_cum_level_1~=0);
[freq_1,bin_1]=hist(nonzero_level_1,Number_of_bin);
frequencies_of_1_levels_in_bins=freq_1';
bin_array_1=bin_1';

total_1_pulses=sum(level==1);
total_time_1=total_1_pulses/sampling_rate;
rows_sorted_level_1=length(bin_array_1);
time_and_freq_1=zeros(length(bin_array_1),1);

for r=1:rows_sorted_level_1
    time_and_freq_1(r,1)=bin_array_1(r,1)*frequencies_of_1_levels_in_bins(r,1);
end;

mean_time=sum(time_and_freq_1)/sum(frequencies_of_1_levels_in_bins);
end;
```

```matlab
%% explanation of timehist function

function [ summary ] = timehist( input )

    summary = zeros(1,length(input));
    chunks = [];
    n=length(input);
    start = -1;
    stop = -1;

  for(i=1:n)
      if (input(i) >0 && start < 0 && stop < 0 )
            %we found a new chunk
            start = i;
            stop = i;
      elseif (input(i) > 0 && start > 0)
          %we are in the middle of a chunk
          stop = i
      elseif (input(i) == 0 && stop > 0)
          %we have come to the end of the chunk, add last chunk to chunks
          %database
          chunks = [chunks ; [start stop]];
          start = -1;
          stop = -1;
      else
          disp('Error, we should never get here')
      end
  end

    %add last chunk
    if(start > 0)
        chunks = [chunks ; [start stop]];
    end

    % this is the important calculation to populate the summary vector
    disp('debug');
    size(chunks);
    disp(chunks);

    s=size(chunks);
    l_chunks = s(1); %this is how many elements (rows) there are in the chunks data structure
    for i=1:l_chunks
        chunk = chunks(i,:);
        summary(chunk(2)) = sum(input(chunk(1):chunk(2)));
    end

end
```

References

[1] P. Moens, J. Mertens, F. Bauwens, P. Joris, W. De Ceuninck and M. Tack, "A comprehensive model for hot carrier degradation in LDMOS transistors," in *Proc. IEEE International Reliability Physics Symposium*, pp. 492-497, 2007.

[2] K. Benaissa, G. Baldwin, S. Liu, P. Srinivasan, F. Hou, B. Obradovic, S. Yu, H. Yang, R. McMullan and V. Reddy, "New cost-effective integration schemes enabling analog and high-voltage design in advanced CMOS SOC technologies," in *Proc. VLSI Technology (VLSIT), Symposium,* pp. 221-222, 2010.

[3] J. F. Chen, S. Chen, K. Wu, J. Shih and K. Wu, "Convergence of hot-carrier-induced saturation region drain current and on-resistance degradation in drain extended MOS transistors," *IEEE Transactions on Electron Devices,* vol. 56, issue 11*,* pp. 2843-2847, 2009.

[4] K. V. Aadithya, A. Demir, S. Venugopalan and J. Roychowdhury, "Accurate prediction of random telegraph noise effects in SRAMs and DRAMs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 32, issue 1, pp. 73-86, 2013.

[5] H. C. Pao and C. Sah, "Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors" *Solid-State Electronics,* vol. 9, issue 10, pp. 927-937, 1966.

[6] A. Bindra and M. Valentine, "GaN power transistors poised for growth, LDMOS promises to maintain lead," *RF DESIGN,* vol. 30, issue 1, p. 18, 2007.

[7] E. Vittoz, "Present and future industrial applications of bio-inspired VLSI systems," *Analog Integrated Circuits and Signal Processing,* vol. 30, issue 2*,* pp. 173-184, 2002.

[8] A. Annema, "Analog circuit performance and process scaling," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing,* vol. 46, issue 6, pp. 711-725, 1999.

[9] P. E. Allen and D. R. Holberg, "*CMOS Analog Circuit Design,"* Elsevier, 2011.

[10] J. S. Brugler and P. G. Jespers, "Charge pumping in MOS devices," *IEEE Transactions on Electron Devices,* vol. 16, issue 3, pp. 297-302, 1969.

[11] M. Von Haartman and M. Östling, "*Low-Frequency Noise in Advanced MOS Device,"* Springer, 2007.

[12] C. Ciofi and B. Neri, "Low-frequency noise measurements as a characterization tool for degradation phenomena in solid-state devices," *Journal of Physics D,* vol. 33, issue 21*,* p. R199, 2000.

[13] G. I. Wirth, "Modeling and Simulation of Device Variability and Reliability at the Electrical Level," PhD dissertation, Universidade Federal Do Rio Grande Do Sul, 2011.

[14] N. V. Amarasinghe, Z. Çelik-Butler, A. Zlotnicka and F. Wang, "Model for random telegraph signals in sub-micron MOSFETS," *Solid-State Electronics*, vol. 47, issue 9, pp. 1443-1449, 2003.

[15] M. Kirton and M. Uren, "Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency ($1/f$) noise," *Advances in Physics,* vol. 38, issue 4, pp. 367-468, 1989.

[16] K. K. Hung, P. K. Ko, C. Hu and Y. C. Cheng, "Random telegraph noise of deep-submicrometer MOSFETs," *IEEE Electron Device Letters*, vol. 11, issue 2, pp. 90-92, 1990.

[17] K. Kandiah and F. Whiting, "Low frequency noise in junction field effect transistors. *Solid-State Electronics,*" vol. 21, issue 8, pp. 1079-1088, 1978.

[18] P. Fang, K. K. Hung, P. Ko and C. Hu, "Hot-electron-induced traps studied through the random telegraph noise," *IEEE Electron Device Letters,* vol. 12, issue 6, pp. 273-275, 1991.

[19] A. Van der Ziel, A. Van der Ziel and A. Van der Ziel, "*Noise in Solid State Devices and Circuits,*" New York: Wiley, 1986.

[20] A. Diligenti, B. Neri, P. Bagnoli, A. Barsanti and M. Rizzo, "Electromigration detection by means of low-frequency noise measurements in thin-film interconnections," *IEEE Electron Device Letters,* vol. 6, issue 11, pp. 606-608, 1985.

[21] A. Van Der Ziel, "Noise in solid-state devices and lasers," *Proceedings of IEEE,* vol. 58, issue 8, pp. 1178-1206, 1970.

[22] J. Lee, G. Bosman, K. R. Green and D. Ladwig, "Noise model of gate-leakage current in ultrathin oxide MOSFETs," *IEEE Transactions on Electron Devices,* vol. 50, issue 12, pp. 2499-2506, 2003.

[23] R. Bianchi, F. Monsieur, F. Blanchet, C. Raynaud and O. Noblanc, "High voltage devices integration into advanced CMOS technologies," in *Proc. IEEE Electron Devices Meeting*, pp. 1-4, 2008.

[24] P. Moens, C. De Keukeleire, R. Degraeve, M. Tack and G. Groeseneken, "Hot hole degradation effects in lateral nDMOS transistors," *IEEE Transactions on Electron Devices,* vol. 51, issue 10, pp. 1704-1710, 2004.

[25] S. Reggiani, S. Poli, E. Gnani, A. Gnudi, G. Baccarani, M. Denison, S. Pendharkar, R. Wise and S. Seetharaman, "Analysis of HCS in STI-based LDMOS transistors," in *Proc. IEEE Reliability Physics Symposium,* pp. 881-886, 2010.

[26] T. Khan, V. Khemka, R. Zhu, W. Huang, X. Cheng, P. Hui, M. Ger, B. Grote and P. Rodriquez, "Combined lateral vertical RESURF (CLAVER) LDMOS structure," in *Proc. International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 13-16, 2009.

[27] P. Moens, "Reliability assessment of integrated power transistors: Lateral DMOS versus vertical DMOS," *Microelectronics Reliability,* vol. 48, issue 8, pp. 1300-1305, 2008.

[28] T. R. Efland, C. Tsai and S. Pendharkar, "Lateral thinking about power devices (LDMOS)," in *Proc. IEEE Electron Devices Meeting,* pp. 679-682,1998.

[29] M. I. Mahmud, Z. Çelik-Butler, P. Hao, P. Srinivasan, F. Hou, X. Cheng, B. L. Amey and S. Pendharkar, "A physics based analytical *1/f* noise model for RESURF LDMOS transistors," vol. 60, issue 2, pp. 677 - 683, 2013.

[30] T. Nigam, A. Shibib, S. Xu, H. Safar and L. Steinberg, "Nature and location of interface traps in RF LDMOS due to hot carriers," *Microelectronic Engineering,* vol. 72, issue 1, pp. 71-75, 2004.

[31] V. Khemka, V. Parthasarathy, R. Zhu and A. Bose, "A floating RESURF (FRESURF) LD-MOSFET device concept," *IEEE Electron Device Letters,* vol. 24, issue 10, pp. 664-666, 2003.

[32] N. Mavredakis, M. Bucher, R. Friedrich, A. Bazigos, F. Krummenacher, J. Sallese, T. Gneiting, W. Pflanzl and E. Seebacher, "Measurement and compact modeling of *1/f* noise in HV-MOSFETs," *IEEE Transactions on Electron Devices*, vol. 60, issue 2, pp. 670 - 676, 2013.

[33] S. Sun and J. D. Plummer, "Modeling of the on-resistance of LDMOS, VDMOS, and VMOS power transistors," *IEEE Transactions on Electron Devices,* vol. 27, issue 2, pp. 356-367, 1980.

[34] E. Riedlberger, C. Jungemann, A. Spitzer, M. Stecher and W. Gustin. "Comprehensive analysis of the degradation of a lateral DMOS due to hot carrier stress," in *IEEE International Integrated Reliability Workshop Final Report (IRW'09),* pp. 77-81, 2009.

[35] M. Mahmud, Z. Celik-Butler, P. Hao, P. Srinivasan, F. Hou, B. Amey and S. Pendharkar, "Effect of stress-induced degradation in LDMOS *1/f* noise characteristics," *IEEE Electron Device Letters,* vol. 33, issue 1*,* pp. 107-109, 2012.

[36] M. I. Mahmud, Z. Celik-Butler, X. Cheng, W. Huang, P. Hao, P. Srinivasan, F. Hou, B. L. Amey and S. Pendharkar, "Experimental analysis of DC and noise parameter degradation in n-channel reduced surface field (RESURF) LDMOS transistors," in *Proc. International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 311-314, 2012.

[37] C. Claeys and E. Simoen, "Noise as a diagnostic tool for semiconductor material and device characterization," *Journal of Electrochemical Society,* vol. 145, issue 6, pp. 2058-2067, 1998.

[38] L. Vandamme, "Noise as a diagnostic tool for quality and reliability of electronic devices," *IEEE Transactions on Electron Devices,* vol. 41, issue 11, pp. 2176-2187, 1994.

[39] J. F. Chen, J. Lee, K. Wu, T. Huang and C. Liu, "Effect of drift-region concentration on hot-carrier-induced ron degradation in nLDMOS transistors," *IEEE Electron Device Letters,* vol. 29, issue 7*,* pp. 771-774, 2008.

[40] P. Moens, G. Van den Bosch and G. Groeseneken, "Competing hot carrier degradation mechanisms in lateral n-type DMOS transistors," in *Proc. IEEE Reliability Physics Symposium,* pp. 214-221, 2003.

[41] N. Tega, H. Miki, Z. Ren, C. D'Emic, Y. Zhu, D. Frank, J. Cai, M. Guillorn, D. Park and W. Haensch, "Reduction of random telegraph noise in high-κ/metal-gate stacks for 22 nm generation FETs," in *Proc. IEEE Electron Devices Meeting,* pp. 1-4, 2009.

[42] Y. Yuzhelevski, M. Yuzhelevski and G. Jung, "Random telegraph noise analysis in time domain," *Review of Scientific Instruments*, vol. 71, issue 4, pp. 1681-1688, 2000.

[43] A. Dikshit, V. Subramanian, S. Pandharpure, S. Sirohi and T. Letavic, "Influence of drift region on the *1/f* noise in LDMOS," in *Proc. International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 315-318, 2012.

[44] P. Srinivasan, W. Xiong and S. Zhao, "Low-frequency noise in integrated N-WELL resistors," *IEEE Electron Device Letters,* vol. 31, issue 12, pp. 1476-1478, 2010.

[45] R. Dreesen, K. Croes, J. Manca, W. De Ceuninck, L. De Schepper, A. Pergoot and G. Groeseneken, "Modelling hot-carrier degradation of LDD NMOSFETs by using a high-resolution measurement technique," *Microelectronics Reliability,* vol. 39, issue 6, pp. 785-790, 1999.

[46] M. Mahmud, Z. Çelik-Butler, P. Hao, F. Hou, B. Amey, T. Khan and W. Huang, "Low-frequency noise and stress-induced degradation in LDMOS," in *Proc. 21st International Conf. Noise and Fluctuations (ICNF)*, pp. 352-355, 2011.

[47] B. Duan, B. Zhang and Z. Li, "A new reduced bulk field (REBULF) high-voltage LDMOS with N -floating layer," in *Proc. International Conf. Communications, Circuits and Systems*, pp. 2709-12, 2006.

[48] W. B. Davenport and W. L. Root, "*An Introduction to the Theory of Random Signals and Noise*," IEEE press, 1986.

[49] K. K. Hung, P. K. Ko, C. Hu and Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Transactions on Electron Devices,* vol. 37, issue 3, pp. 654-665, 1990.

[50] R. Van Langevelde, S. Blieck and L. Vandamme, "Noise in DMOS transistors in a BICMOS-technology," *IEEE Transactions on Electron Devices,* vol. 43, issue 8, pp. 1243-1250, 1996.

[51] www.itrs.net.

[52] R. Brederlow, W. Weber, D. Schmitt-Landsiedel and R. Thewes, "Hot-carrier degradation of the low-frequency noise in MOS transistors under analog and RF operating conditions," *IEEE Transactions on Electron Devices,* vol. 49, issue 9, pp. 1588-1596, 2002.

[53] A. McWhorter, "*1/f* noise and germanium surface properties," *Semiconductor Surface Physics,* pp. 207-228, 1957.

[54] F. Hooge and L. Vandamme. Lattice scattering causes $1/f$ noise," *Physics Letters A,* vol. 66, issue 4, pp. 315-316, 1978.

[55] F. Hooge, T. Kleinpenning and L. Vandamme, "Experimental studies on *1/f* noise," *Reports on Progress in Physics,* vol. 44, issue 5, p. 479, 1981.

[56] G. Ghibaudo, O. Roux, C. Nguyen-Duc, F. Balestra and J. Brini, "Improved analysis of low frequency noise in Field-Effect MOS transistors," *Physica Status Solidi (a),* vol. 124, issue 2, pp. 571-581, 1991.

[57] T. H. Morshed, S. P. Devireddy, Z. Celik-Butler, A. Shanware, K. Green, J. Chambers, M. Visokay and L. Colombo, "Physics-based *1/f* noise model for MOSFETs with nitrided high-κ gate dielectrics," *Solid-State Electronics,* vol. 52, issue 5, pp. 711-724, 2008.

[58] M. S. Rahman, T. Morshed, S. Devireddy, Z. Çelik-Butler, M. Quevedo-Lopez, A. Shanware and L. Colombo, "Effect of nitrogen incorporation on *1/f* noise performance of metal-oxide-semiconductor field effect transistors with HfSiON dielectric," *Journal of Applied Physics,* vol. 103, issue 3, pp. 033706-033706-5, 2008.

[59] B. Min, S. P. Devireddy, Z. Çelik-Butler, F. Wang, A. Zlotnicka, H. Tseng and P. J. Tobin, "Low-frequency noise in submicrometer MOSFETs with HfO_2, HfO_2/Al_2O_3 and $HfAlO_x$ gate stacks," *IEEE Transactions on Electron Devices,* vol. 51, issue 8, pp. 1315-1322, 2004.

[60] Z. Celik-Butler and T. Hsiang, "Spectral dependence of $1/f^{\gamma}$ noise on gate bias in nMOSFETS," *Solid-State Electronics,* vol. 30, issue 4, pp. 419-423, 1987.

[61] J. Koga, S. Takagi and A. Toriumi, "A comprehensive study of MOSFET electron mobility in both weak and strong inversion regimes," in *Proc. IEEE Electron Devices Meeting,* pp. 475-478, 1994.

[62] E. P. Vandamme and L. K. Vandamme, "Critical discussion on unified *1/f* noise models for MOSFETs," *IEEE Transactions on Electron Devices*, vol. 47, issue 11, pp. 2146-2152, 2000.

[63] J. Ryan, R. Southwick, J. Campbell, K. Cheung, C. Young and J. Suehle, "On the "U-shaped" continuum of band edge states at the Si/SiO_2 interface," *Applied Physics Letters,* vol. 99, issue 22, pp. 223516-8, 2011.

[64] E. Poindexter, G. Gerardi, M. Rueckel, P. Caplan, N. Johnson and D. Biegelsen, "Electronic traps and P_b centers at the Si/SiO_2 interface: Band-gap energy distribution," *Journal of Applied Physics,* vol. 56, issue 10, pp. 2844-2849, 1984.

[65] L. K. Vandamme, "Bulk and surface *1/f* noise," *IEEE Transactions on Electron Devices,* vol. 36, issue 5, pp. 987-992, 1989.

[66] L. Vandamme, X. Li and D. Rigaud, "*1/f* noise in MOS devices, mobility or number fluctuations?," *IEEE Transactions on Electron Devices,* vol. 41, issue 11, pp. 1936-1945, 1994.

[67] Z. Celik-Butler and T. Hsiang, "Determination of Si-SiO$_2$ interface trap density by *1/f* noise measurements," *IEEE Transactions on Electron Devices,* vol. 35, issue 10, pp. 1651-1655, 1988.

[68] C. Cheng, K. Tu, T. Wang, T. Hsieh, J. Tzeng, Y. Jong, R. Liou, S. C. Pan and S. Hsu, "Investigation of hot carrier degradation modes in LDMOS by using a novel three-region charge pumping technique," in *Proc. IEEE Reliability Physics Symposium,* pp. 334 - 337, 2006.

[69] K. Uchida, J. Koga, and S.-I. Takagi, "Experimental study on carrier transport mechanisms in double-and single-gate ultrathin-body MOSFETs-coulomb scattering, volume inversion, and δT$_{SOI}$-induced scattering," in *Proc. IEEE Electron Devices Meeting*, pp. 33.5.1 - 33.5.4, 2003.

[70] B. Min, S. P. Devireddy, Z. Çelik-Butler, A. Shanware, K. Green, J. Chambers, M. Visokay and L. Colombo, "Low-frequency noise characteristics of HfSiON gate-dielectric metal-oxide-semiconductor-field-effect transistors," *Applied Physics Letters,* vol. 86, issue 8, pp. 082102-3, 2005.

[71] M. I. Mahmud, Z. Celik-Butler, P. Hao, P. Srinivasan, F. Hou, B. L. Amey, S. Pendharkar, X. Cheng and W. Huang, "Correlation of 1/f noise and high-voltage-stress-induced degradation in LDMOS," in *Proc. IEEE Reliability Physics Symposium,* pp. XT.4.1 - XT.4.6, 2012.

[72] T. Sakurai and T. Sugano, "Theory of continuously distributed trap states at Si-SiO$_2$ interfaces," *Journal of Applied Physics,* vol. 52, issue 4, pp. 2889-2896, 1981.

[73] R. Laughlin, J. Joannopoulos and D. Chadi, "Theory of the electronic structure of the Si-SiO$_2$ interface," *Physical Review B,* vol. 21, issue 12, p. 5733, 1980.

[74] Y. Wang and K. Cheung, "Carrier capture at the SiO$_2$–Si interface: A physical model," *Applied Physics Letters,* vol. 91, issue 11, pp. 113509-3, 2007.

[75] R. Black, P. Restle and M. Weissman, "Hall effect, anisotropy, and temperature-dependence measurements of *1/f* noise in silicon on sapphire," *Physical Review B,* vol. 28, issue 4, p. 1935, 1983.

[76] M. S. Rahman, T. H. Morshed, Z. Celik-Butler, M. Quevedo-Lopez, A. Shanware and L. Colombo, "Hot-carrier-and constant-voltage-stress-induced low-frequency noise in nitrided high-dielectric MOSFETs," *IEEE Transactions on Device and Materials Reliability,* vol. 9, issue 2, pp. 203-220, 2009.

[77] N. Tega, H. Miki, F. Pagette, D. Frank, A. Ray, M. Rooks, W. Haensch and K. Torii, "Increasing threshold voltage variation due to random telegraph noise in FETs as gate lengths scale to 20 nm," in *Proc. VLSI Technology (VLSIT) Symposium,* pp. 50-51, 2009.

[78] A. Godoy, F. Gámiz, A. Palma, J. Jiménez-Tejada, J. Banqueri and J. López-Villanueva, "Influence of mobility fluctuations on random telegraph signal amplitude in n-channel metal–

oxide–semiconductor field-effect transistors," *Journal of Applied Physics,* vol. 82, issue 9, pp. 4621-4628, 1997.

[79] H. Mueller and M. Schulz, "Individual interface traps at the Si—SiO$_2$ interface," *Journal of Material Science: Materials in Electronics,* vol. 6, issue 2, pp. 65-74, 1995.

[80] N. H. Hamid, A. F. Murray and S. Roy, "Time-domain modeling of low-frequency noise in deep-submicrometer MOSFET," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 55, issue 1, pp. 245-257, 2008.

[81] H. Bu, Y. Shi, X. Yuan, Y. Zheng, S. Gu, H. Majima, H. Ishikuro and T. Hiramoto, "Impact of the device scaling on the low-frequency noise in n-MOSFETs," *Applied Physics A,* vol. 71, issue 2, pp. 133-136. 2000.

[82] G. Ghibaudo and O. Roux-dit-Buisson, "Low frequency fluctuations in scaled down silicon CMOS devices status and trends," in *Proc. 24th European Solid-State Device Research (ESSDERC)*, pp. 693-700, 1994.

[83] A. Palma, A. Godoy, J. Jimenez-Tejada, J. Carceller and J. Lopez-Villanueva, "Quantum two-dimensional calculation of time constants of random telegraph signals in metal-oxide–semiconductor structures," *Physical Review B,* vol. 56, issue 15, p. 9565, 1997.

[84] S. Yoo, Y. Son and H. Shin, "Capture cross section of traps causing random telegraph noise in gate-induced drain leakage current," *IEEE Transactions on Electron Devices,* vol. 60, issue 3, pp. 1268 - 1271, 2013.

[85] J. Salfi, N. Paradiso, S. Roddaro, S. Heun, S. V. Nair, I. G. Savelyev, M. Blumin, F. Beltram and H. E. Ruda, "Probing the gate− voltage-dependent surface potential of individual InAs nanowires using random telegraph signals," *ACS Nano,* vol. 5, issue 3, pp. 2191-2199, 2011.

[86] A. Asenov, R. Balasubramaniam, A. R. Brown and J. H. Davies, "RTS amplitudes in decananometer MOSFETs: 3-D simulation study," *IEEE Transactions on Electron Devices,* vol. 50, issue 3, pp. 839-845, 2003.

[87] E. Simoen, B. Dierickx, C. L. Claeys and G. J. Declerck, "Explaining the amplitude of RTS noise in submicrometer MOSFETs," *IEEE Transactions on Electron Devices,* vol. 39, issue 2, pp. 422-429, 1992.

[88] M. Uren, M. Kirton and S. Collins, "Anomalous telegraph noise in small-area silicon metal-oxide-semiconductor field-effect transistors," *Physical Review B,* vol. 37, issue 14, pp. 8346–8350, 1988.

[89] O. Roux dit Buisson, G. Ghibaudo and J. Brini, "Model for drain current RTS amplitude in small-area MOS transistors," *Solid-State Electronics,* vol. 35, issue 9, pp. 1273-1276, 1992.

[90] E. Simoen and C. Claeys, "Random telegraph signal: a local probe for single point defect studies in solid-state devices," *Materials Science and Engineering: B 91,* pp. 136-143, 2002.

[91] M. Schulz, "Coulomb energy of traps in semiconductor space-charge regions," *Journal of Applied Physics,* vol. 74, issue 4, pp. 2649-2657, 1993.

[92] G. I. Wirth, J. Koh, R. da Silva, R. Thewes and R. Brederlow, "Modeling of statistical low-frequency noise of deep-submicrometer MOSFETs," *IEEE Transactions on Electron Devices,* vol. 52, issue 7*,* pp. 1576-1588, 2005.

[93] K. Sonoda, K. Ishikawa, T. Eimori and O. Tsuchiya, "Discrete dopant effects on statistical variation of random telegraph signal magnitude," *IEEE Transactions on Electron Devices*, vol. 54, issue 8, pp. 1918-1925, 2007.

[94] Z. Shi, J. Mieville and M. Dutoit, "Random telegraph signals in deep submicron nMOSFET's," *IEEE Transactions on Electron Devices,* vol. 41, issue 7, pp. 1161-1168, 1994.

[95] K. Ralls, W. Skocpol, L. Jackel, R. Howard, L. Fetter, R. Epworth and D. Tennant, "Discrete resistance switching in submicrometer silicon inversion layers: Individual interface traps and low-frequency (*1/f*) noise," *Physical Review Letters,* vol. 52 pp. 228-231, 1984.

[96] T. Nagumo, K. Takeuchi, S. Yokogawa, K. Imai and Y. Hayashi, "New analysis methods for comprehensive understanding of random telegraph noise," in *Proc. IEEE Electron Devices Meeting*, pp. 1-4, 2009.

[97] T. Nagumo, K. Takeuchi, T. Hase and Y. Hayashi, "Statistical characterization of trap position, energy, amplitude and time constants by RTN measurement of multiple individual traps," in *Proc. IEEE Electron Devices Meeting*, pp. 28.3.1 - 28.3.4, 2010.

[98] H. Miki, M. Yamaoka, N. Tega, Z. Ren, M. Kobayashi, C. D'Emic, Y. Zhu, D. Frank, M. Guillorn and D. Park, "Understanding short-term BTI behavior through comprehensive observation of gate-voltage dependence of RTN in highly scaled high-κ/metal-gate pFETs," in *Proc. VLSI Technology (VLSIT) Symposium,* pp. 148-149, 2011.

[99] S. Realov and K. L. Shepard, "Random telegraph noise in 45-nm CMOS: Analysis using an on-chip test and measurement system," in *Proc. IEEE Electron Devices Meeting*, pp. 28.2.1 - 28.2.4, 2010.

[100] H. Awano, H. Tsutsui, H. Ochi and T. Sato. Multi-trap RTN parameter extraction based on bayesian inference," in *Proc. International Symposium on Quality Electronic Design (ISQED),* pp. 597-602, 2013.

[101] N. V. Amarasinghe, "Random Telegraph Signals in Submicron MOSFETS," PhD Dissertation, Southern Methodist University, 2001.

[102] G. Giusi, F. Crupi and C. Pace, "An algorithm for separating multilevel random telegraph signal from *1/f* noise," *Review of Scientific Instruments,* vol. 79, issue 2*,* pp. 024701-5, 2008.

[103] L. Vandamme, D. Sodini and Z. Gingl, "On the anomalous behavior of the relative amplitude of RTS noise," *Solid-State Electronics,* vol. 42, issue 6*,* pp. 901-905, 1998.

[104] W. Shockley and W. Read Jr., "Statistics of the recombinations of holes and electrons," *Physical Review,* vol. 87, issue 5, p. 835, 1952.

[105] M. Schulz and N. Johnson, "Evidence for multiphonon emission from interface states in MOS structures," *Solid State Communications,* vol. 25, issue 7*,* pp. 481-484, 1978.

[106] R. Pierret, and G. W. Neudeck, "*Advanced semiconductor fundamentals*," vol. 6, Reading, Massachusetts: Addison-Wesley, 1987.

[107] C. Leyris, F. Martinez, M. Valenza, A. Hoffmann and J. Vildeuil, "Random telegraph signal: A sensitive and nondestructive tool for gate oxide single trap characterization," *Microelectronics Reliability,* vol. 47, issue 4, pp. 573-576, 2007.

[108] N. Ashraf, D. Vasileska, G. Wirth and P. Srinivasan, "Accurate model for the threshold voltage fluctuation estimation in 45-nm channel length MOSFET devices in the presence of random traps and random dopants," *IEEE Electron Device Letters,* vol. 32, issue 8, pp. 1044-1046, 2011.

[109] J. Campbell, J. Qin, K. Cheung, L. Yu, J. Suehle, A. Oates and K. Sheng, "Random telegraph noise in highly scaled nMOSFETs," in *Proc. IEEE Reliability Physics Symposium,* pp. 382-388, 2009.

[110] S. Li, W. McMahon, Y. Lu and Y. Lee, "RTS noise characterization in flash cells," *IEEE Electron Device Letters,* vol. 29, issue 1, pp. 106-108, 2008.

[111] B. G. Streetman and S. Banerjee, "*Solid State Electronic Devices,"* vol. 4, New Jersey: Prentice Hall, 2000.

[112] S. O. Toh, Y. Tsukamoto, Z. Guo, L. Jones, T. K. Liu and B. Nikolic, "Impact of random telegraph signals on V_{min} in 45nm SRAM," in *Proc. IEEE Electron Devices Meeting*, pp. 1-4, 2009.

[113] http://www.home.agilent.com/~The Impedance Measurement Handbook-4th Edition - Application Note.

[114] K. Kandiah, M. Deighton and F. Whiting, "A physical model for random telegraph signal currents in semiconductor devices," *Journal of Applied Physics,* vol. 66, issue 2, pp. 937-948, 1989.

[115] N. Tega, H. Miki, T. Osabe, A. Kotabe, K. Otsuga, H. Kurata, S. Kamohara, K. Tokami, Y. Ikeda and R. Yamada, "Anomalously large threshold voltage fluctuation by complex random telegraph signal in floating gate flash memory," in *Proc. IEEE Electron Devices Meeting*, pp. 1-4, 2006.

[116] H. Miki, "Method of extracting a time constant from complex random telegraph signals," U.S. Patent 8,155,905, April 10, 2012.

[117] J. Kolhatkar, L. Vandamme, C. Salm and H. Wallinga, "Separation of random telegraph signals from *1/f* noise in MOSFETs under constant and switched bias conditions," in *Proc. 33rd European Solid-State Device Research (ESSDERC)*, pp. 549-552, 2003.

[118] K. Ziegler, "Distinction between donor and acceptor character of surface states in the Si-SiO$_2$ interface," *Applied Physics Letters,* vol. 32, issue 4, pp. 249-251, 1978.

[119] P. Lenahan and P. Dressendorfer, "Hole traps and trivalent silicon centers in metal/oxide/silicon devices," *Journal of Applied Physics,* vol. 55, issue 10, pp. 3495-3499, 1984.

[120] N. Tega, H. Miki, M. Yamaoka, H. Kume, T. Mine, T. Ishida, Y. Mori, R. Yamada and K. Torii, "Impact of threshold voltage fluctuation due to random telegraph noise on scaled-down SRAM," in *Proc. IEEE Reliability Physics Symposium,* pp. 541-546, 2008.

[121] J. Roldán, F. Gámiz, J. López-Villanueva, J. Carceller and P. Cartujo, "The dependence of the electron mobility on the longitudinal electric field in MOSFETs," *Semiconductor Science and Technology,* vol. 12, issue 3*,* p. 321, 1997.

[122] M. Schulz and A. Karmann, "Single, individual traps in MOSFETs," *Physica Scripta,* vol. T35*,* p. 273, 1991.

[123] F. Adamu-Lema, C. Monzio Compagnoni, S. M. Amoroso, N. Castellani, L. Gerrer, S. Markov, A. S. Spinelli, A. L. Lacaita and A. Asenov, "Accuracy and issues of the spectroscopic analysis of RTN traps in nanoscale MOSFETs," *IEEE Transactions on Electron Devices,* vol. 60, issue 2*,* pp. 833 - 839, 2013.

[124] C. Henry and D. V. Lang, "Nonradiative capture and recombination by multiphonon emission in GaAs and GaP," *Physical Review B,* vol. 15, issue 2*,* pp. 989–1016, 1977.

[125] T. Ando, A. B. Fowler and F. Stern, "Electronic properties of two-dimensional systems," *Reviews of Modern Physics,* vol. 54, pp. 437-672, 1982.

[126] N. V. Amarasinghe, Z. Çelik-Butler and A. Keshavarz, "Extraction of oxide trap properties using temperature dependence of random telegraph signals in submicron metal–oxide–semiconductor field-effect transistors," *Journal of Applied Physics* vol. 89, issue 10, pp. 5526-5532, 2001.

[127] H. Nakamura, N. Yasuda, K. Taniguchi, C. Hamaguchi and A. Toriumi, "Existence of double-charged oxide traps in submicron MOSFET's," *Japanese Journal of Applied Physics 28 (part 2),* pp. 2057-2060, 1989.

[128] M. Uren, D. Day and M. Kirton, "*1/f* and random telegraph noise in silicon metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters,* vol. 47, issue 11, pp. 1195-1197, 1985.

[129] H. Mueller and M. Schulz, "Random telegraph signal: An atomic probe of the local current in field-effect transistors," *Journal of Applied Physics,* vol. 83, issue 3, pp. 1734-1741, 1998.

Biographical Information

Md. Iqbal Mahmud started his BS to PhD study in EE in University of Texas at Arlington, USA in Fall 2009. He received the B.Sc. degree in EEE from Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh in 2006. He was the winner of the "UTArlington Nanofab Best Graduate Student" award, 2013 and was a runner-up for the "Dr. N. M. Stelmakh Outstanding Research Student" award, 2013 in UTArlington. In 2012, he did a summer internship in analog technology development (ATD) group in Texas Instruments Inc., Dallas, USA as a power transistor engineer. He is enthusiastic to continue working on modeling, characterization and reliability issues of state-of-the-art semiconductor devices.