MULTIPORT DC ENERGY CONVERSION SYSTEMS

by

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Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

THE UNIVERSITY OF TEXAS AT ARLINGTON

December 2013

ACKNOWLEDGEMENTS

First, I should thank God for giving me the strength to *pursue the happiness*, and my parents for their unconditional support.

My sincere appreciation goes to my academic advisor, Dr. Ali Davoudi, for his support and guidance during my Ph.D. studies. I would like to thank Dr. Frank Lewis, Dr. Wei-Jen Lee, Dr. David Wetz, and Dr. Kambiz Alavi for their agreement to be on my committee and their valuable suggestions and comments. My special thanks go to Dr. Jonathan Bredow and Dr. Rasool Kenarangui for their guidance and mentoring throughout the course of my Ph.D. work at the University of Texas at Arlington.

My gratitude goes to the members of the Renewable Energy and Vehicular Technology Laboratory at the University of Texas at Arlington, especially Mr. Lei Niu, for being supportive over the past few years.

Finally, I would like to thank my lovely fiancé, Kristina, to whom I dedicate this dissertation.

November 18, 2013

ABSTRACT

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The University of Texas at Arlington, 2013

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Sustainable energy sources and power electronic systems for utilizing such energy sources are becoming indispensible components of the modern power grid. The ability of multiport converters to mitigate the intermittency issues associated with these energy sources have made them attractive candidates for renewable energy conversion systems. Two single-stage multiport dc-dc converters, with independent and series outputs, are proposed in this dissertation. The advantages and applications of the proposed topologies are discussed. The ability of the proposed converters to regulate the input powers, coming from different energy sources, in addition to regulating the output voltages stands out. Specific switching schemes are presented for the proposed converters and the dynamic models of the converters are developed based on the designated switching scheme. Appropriate control algorithms are presented for regulating the input powers and output voltages.

Proper design and development of digital controllers for multiport dc energy conversion systems requires exact discrete-time modeling of such systems. An exact discrete-time modeling framework is set forth for direct digital-control design of multiport dc-dc converters. The proposed modeling technique addresses the peculiar aspects of multiport dc-dc converters, which make the use of conventional continuous-time modeling for such converters prone to failure. Time-multiplexing switching schemes are accommodated by considering multiple propagation paths during each switching period. Sampling effects, modulator effects, and the propagation delays due to multiple propagation paths are included. The proposed model can accommodate both leading and trailing edge PWM schemes. The approximations inherent in the averaging techniques are avoided by using Floquet theory.

A cooperative control method is also proposed for multiphase dc-dc converters. The proposed cooperative control scheme enjoys structural modularity, plug-and-play capability, fault tolerance against random failures in the converters and/or communication links, and satisfactory dynamic performance. A general analytical framework is provided to study modular dc-dc converters with an arbitrary communication graph. Hence, the designer has the freedom to choose among the various types of graphs based on the available communication resources and the desired level of reliability and fault tolerance. The dynamic model of the cooperative multi-phase converter system is developed and analyzed.

Semiconductor switches are, arguably, among the reliability bottlenecks in power electronic converters and, especially, multiport converters. Redundant switch structures are proposed for reliability improvement in such systems. Parallel and standby configurations are applied to semiconductor switches to this aim. The reliability models of both configurations are developed based on Markov process. Mean Time to Failure (MTTF) of each configuration is derived in terms of the underlying parameters. It is demonstrated that there is a boundary condition in which both configurations have the same MTTF. This boundary condition is expressed in terms of the junction temperature of the semiconductor switch in the steady state. The temperature range in which the parallel configuration is more reliable is formulated for different types of power semiconductor switches.

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NOMENCALTURE

SISO	Single Input Single Output	JTAG	Joint Test Action Group
MISO	Multiple Input Single Output	ADC	Analog to Digital Converter
SIMO	Single Input Multiple Output	MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MIMO	Multiple Input Multiple Output	SCR	Silicon Controlled Rectifier
FCBB	Forward Conducting Bidirectional Blocking	TRIAC	Triode for Alternating Current
CCM	Continuous Conduction Mode	BJT	Bipolar Junction Transistor
DCM	Discontinuous Conduction Mode	DDM	Direct Design Method
EDC	Effective Duty Cycle	IDM	Indirect Design Method
SSA	State Space Averaging	IPOP	Input Parallel Output Parallel
CA	Circuit Averaging	ISOP	Input Series Output Parallel
GSSA	Generalized State Space Averaging	IPOS	Input Parallel Output Series
MTTF	Mean Time To Failure	ISOS	Input Series Output Series
FDIR	Fault Detection Isolation and Reconfiguration	PWM	Pulse Width Modulation
DSP	Digital Signal Processor	PI	Proportional Integral
USB	Universal Serial Bus	PID	Proportional Integral Derivative

CHAPTER 1

INTRODUCTION

Depletion of fossil fuel resources has become one of the major concerns of the new century and attracted much attention to the renewable energy sources, as alternatives. However, several challenges are yet to be overcome in the way of large-scale utilization of the renewable energy sources, among which intermittent characteristic of such energy sources (e.g. solar, wind) is the major concern. The ability of multi-port power electronic converters to diversify the energy sources, and consequently, mitigate the inherent intermittency of renewable energy sources has made them attractive candidates to be used in renewable energy systems.

Figure 1.1 depicts the schematic of a general multiport dc energy conversion system. Such energy conversion system can feed several loads and accommodate several sources, simultaneously. The voltage/current characteristics of the input and output ports are not necessarily identical. For instance, the input ports can be connected to photovoltaic panel, fuel cell, battery, rectified wind, etc.. Some ports can act as both input and output, e.g., those connected to rechargeable batteries.

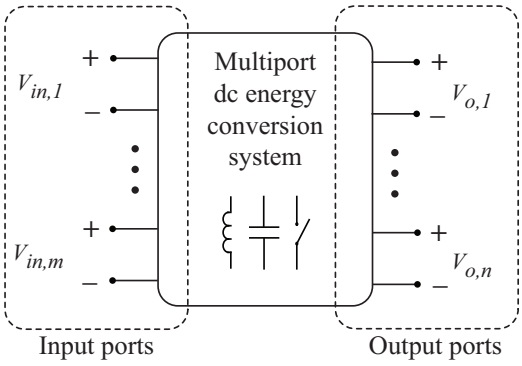

Figure 1.1 A general multiport dc energy conversion system

The multiport dc energy conversion system is essentially a power-electronics based system. Multiport converters can be synthesized using two different approaches, namely, the modular approach, and the single-stage approach. In modular approach, several SISO converters are connected to a common

dc bus to realize a multiport system, as seen in Figure 1.2. Such modular configuration enjoys improved reliability through structural redundancy, easing the thermal management, reducing the component stress, reducing the manufacturing cost by standardization of system components, and re-configurability. However, the modular approach results in a complex structure and high cost. Besides, the control complexity and stability issues associated with the modular system make the single-stage multiport converters more attractive alternatives, especially in cost-effective applications. In single-stage approach, the power processing takes place in one converter stage. Thus, the efficiency is expected to improve due to the reduction in the total number of the components and the resulting power loss reduction. Reduction in the total number of components also results in reduction in cost and size of the system.

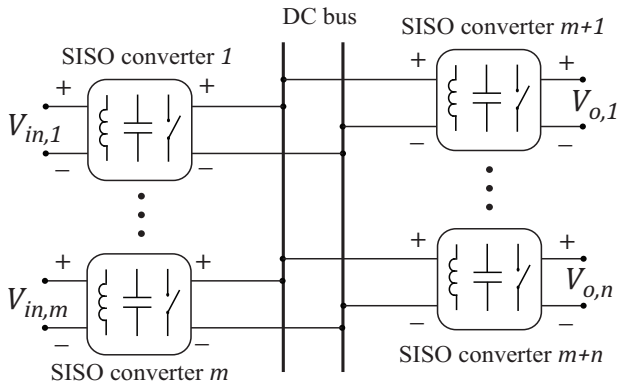

Figure 1.2 Modular realization of multiport dc energy conversion system.

Chapter 2 proposes a single-stage multiport dc-dc converter topology with independent outputs. The advantages and applications of the proposed topology are also discussed in chapter 2. The ability of the proposed converter to regulate the input powers, coming from different energy sources, in addition to regulating the output voltages stands out. A specific switching scheme is presented for the proposed multiport converter and the dynamic model of the converter is developed based on the designated switching scheme. An appropriate control algorithm is also presented, based on which the input powers and output voltages are regulated.

Chapter 3 proposes another single-stage multiport dc-dc topology that provides series outputs. The proposed series-output multiport converter, as discussed in chapter 3, is a good candidate for interfacing between the diversified energy sources and grid-tied multilevel inverters. The steady-state and dynamic characteristics of the proposed converter are analyzed. A controller scheme is proposed that allows budgeting of the input powers coming from different energy sources, in addition to regulating the output voltages. Loss and efficiency modeling as well as sensitivity analysis to the underlying parameters are performed.

Digital controllers are widely used in modern power electronic systems, including multiport converters, due to their salient features. These features include immunity to parameter variations, less electromagnetic-interference, and ability to handle complex control algorithms. Proper design and development of digital controller for the multiport converters requires exact discrete-time modeling of such systems. In chapter 4, an exact discrete-time modeling framework is set forth for direct digital-control design of multiport dc-dc converters (including those proposed in Chapters 2 and 3). The proposed modeling technique addresses the peculiar aspects of multiport dc-dc converters, which make the use of conventional continuous-time modeling for such converters prone to failure. Time-multiplexing switching schemes are accommodated by considering multiple propagation paths during each switching period. Sampling effects, modulator effects, and the propagation delays due to multiple propagation paths are included. The proposed model can accommodate both leading and trailing edge PWM schemes. The approximations inherent in the averaging techniques are avoided by using Floquet theory.

The so-called ‘multiphase’ dc-dc converters can be considered as modular multiport converters, as shown in Figure 1.2, with all the input and output ports connected together. By doing so, a new SISO converter can be synthesized where one of its ports is the dc bus in the antecedent configuration (see Figure 1.2). Chapter 5 proposes a discrete-time modeling method that is suitable for direct digital-control design for multiphase dc-dc converters.

In chapter 6, a cooperative control method is proposed for multiphase converters. The proposed cooperative control scheme enjoys structural modularity, plug-and-play capability, fault tolerance against random failures in the converters and/or communication links, and satisfactory dynamic performance. Chapter 6 provides a general analytical framework to study modular dc-dc converters with an arbitrary communication graph. Hence, the designer has the freedom to choose among the various types of graphs based on the available communication resources and the desired level of reliability and fault tolerance. The dynamic model of the cooperative multiphase converter system is developed and analyzed.

One of the shortcomings of the single-stage multiport systems, compared to their modular counterparts, is less reliability since the single-stage configurations have minimum redundancy. Semiconductor switches are, arguably, among the reliability bottlenecks in power electronic converters, in general, and single-stage multiport converters, specifically. Chapter 7 proposes redundant switch structures for reliability improvement in such systems. Parallel and standby configurations are applied to semiconductor switches to this aim. The reliability models of both configurations are developed based on Markov process. MTTF of each configuration is derived in terms of the underlying parameters. It is demonstrated that there is a boundary condition in which both configurations have the same MTTF. This boundary condition is expressed in terms of the junction temperature of the semiconductor switch in the steady state. The temperature range in which the parallel configuration is more reliable is formulated for different types of power semiconductor switches.

CHAPTER 2

MULTIPORT DC-DC CONVERTER WITH INDEPENDENT OUTPUTS

Multi-port converters can be synthesized by connecting several SISO converters to a common dc bus. This configuration, even though prevalent in conventional renewable energy systems, is not cost- or size-effective. Besides, control and stability issues associated with the negative input impedance of the SISO converters further degrade the performance of such systems and make a unified, single-stage, multi-port converter a more attractive alternative. Single-stage multi-port converters can be categorized as MISO, SIMO, and MIMO converters.

MISO and SIMO dc-dc converters have been well studied in the literature. Several MISO topologies are derived from the basic SISO converters, namely, buck [1, 2], boost [3, 4], buck-boost [5-7], H-bridge [8-10], flyback, and forward [11, 12] converters. Assumptions, restrictions, and conditions for expanding basic SISO converters to their MISO versions are discussed in [13]. Systematic approaches to synthesize MISO converters are studied in [14]. SIMO converters can be categorized into isolated- and non-isolated topologies. In isolated topologies, a multiple-winding transformer is employed to provide multiple output ports. Usually, the output port that is connected to the heaviest load has a tight closed-loop control while the other output voltages are determined by the conversion ratios of the secondary windings and, thus, make independent regulation of output voltages challenging [15]. The non-isolated SIMO converters can be further categorized into independent- and series-output configurations. In independent-output configuration [16, 17], all outputs share the same ground whereas in series-output configuration [18, 19], different outputs are connected in a series fashion. Series-output SIMO converters are mostly used for balancing the dc-link voltages of diode-clamped multilevel inverters [19, 20].

Unlike MISO and SIMO converters, less attention has been paid to MIMO DC-DC converters in the literature to date. A MIMO converter is presented in [21] for energy harvesting in wireless sensor networks. High power operation of such converter would be challenging since it is designated to operate in discontinuous conduction mode, which means, inductor current cannot exceed above a certain limit.

Another MIMO converter is proposed in [22] to interface between a Li-ion battery, a fuel cell, and a passive load. Even though only one passive load can be supplied, this topology is considered as a MIMO converter since it allows the battery to supply and sink the current, and hence, act as both "source" and "load". This chapter introduces a MIMO converter topology with independent outputs and "power budgeting capability" [23, 24]. Power budgeting capability can be defined as the ability of the converter to regulate the input powers coming from different energy sources in addition to regulating the output voltages.

The fundamental features of the proposed converter can be summarized as follows.

- Employing multiple energy sources and supplying multiple loads
- Power budgeting capability
- Employing a single inductor, which in turn, can reduce the size and cost of the converter, and simplify current sensing [6] (given the switching signals of the active switches, all input and output currents can be determined by only sensing the inductor current.)

The rest of this chapter is organized as follows. The operational principles of the converter are discussed in section 2.1. Section 2.2 presents average value modeling and dynamic characterization for the converter. The control algorithm for power budgeting is developed in Section 2.3. Section 2.4 presents several case studies to verify analytical derivations and evaluate the performance of the proposed multiport converter.

2.1 Operational Principles

Figure 2.1 illustrates the proposed converter topology. This topology, in general, is capable of employing arbitrary number of input energy resources, $V_{\text{in},1}, V_{\text{in},2}$, ..., $V_{\text{in},m}$, while regulating arbitrary number of output voltages, $V_{\text{o},1}, V_{\text{o},2}$, ..., $V_{\text{o},n}$. Without loss of generality, the input voltage sources are assumingly arranged such that $V_{\text{in},1} > V_{\text{in},2} > \cdots > V_{\text{in},m}$. The output voltages are assumed to be regulated

such that $V_{o,1} > V_{o,2} > \cdots > V_{o,n}$. It can be shown that the output voltage arrangement is achievable using the proposed switching scheme.

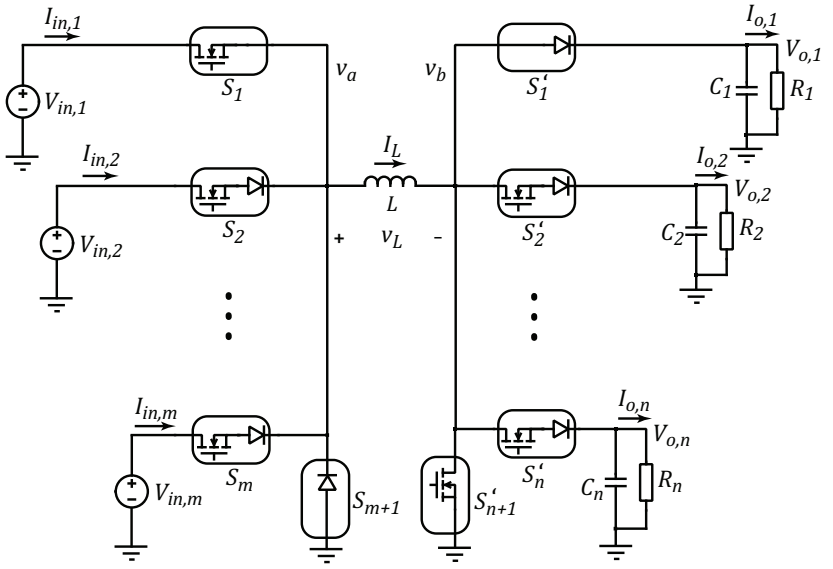

Figure 2.1 The proposed independent-output MIMO topology: a general *m*-input *n*-output converter**.**

The input and output switches are denoted by S_k and S_k' for the k^{th} input and output ports, respectively. All switches are FCBB except for S_1, S_{m+1}, S_1', and S_{n+1}'. The FCBB switches are realized by a series connection of a MOSFET and a diode here. Switches S_1 and S_{n+1}' are single MOSFETs whereas S_{m+1} and S_1' are single diodes. Even though FCBB switches imply unidirectional power flow, they are prevalent in MISO and SIMO converters to avoid simultaneous parallel connection of different dc sources [5-7]. Moreover, unidirectional multi-port converters are preferred in applications with unidirectional inputs (e.g. solar cells, fuel cells, primary batteries) or loads.

The proposed switching scheme for the converter is depicted in Figure 2.2. Switching commands are denoted by $q_1, q_2, \ldots, q_m$ and $q_2', q_3', \ldots, q_{n+1}'$ for the input and output MOSFETs, respectively. As shown in Figure 2.2, the leading edges of the switching commands coincide but the trailing edges do not necessarily coincide. The average-values of switching commands are the input and

output duty cycles, $d_1, d_2, \ldots, d_m$ and $\alpha_2, \alpha_3, \ldots, \alpha_{n+1}$, respectively. The switching command of S_m and S'_{n+1} are the same, i.e., $d_m = \alpha_{n+1}$. Since S_{m+1} and S'_1 are diodes, they do not require switching commands. However, to simplify model formulation, on-state switching commands are assigned, i.e., $d_{m+1} = \alpha_1 = 1$, as shown in Figure 2.2.

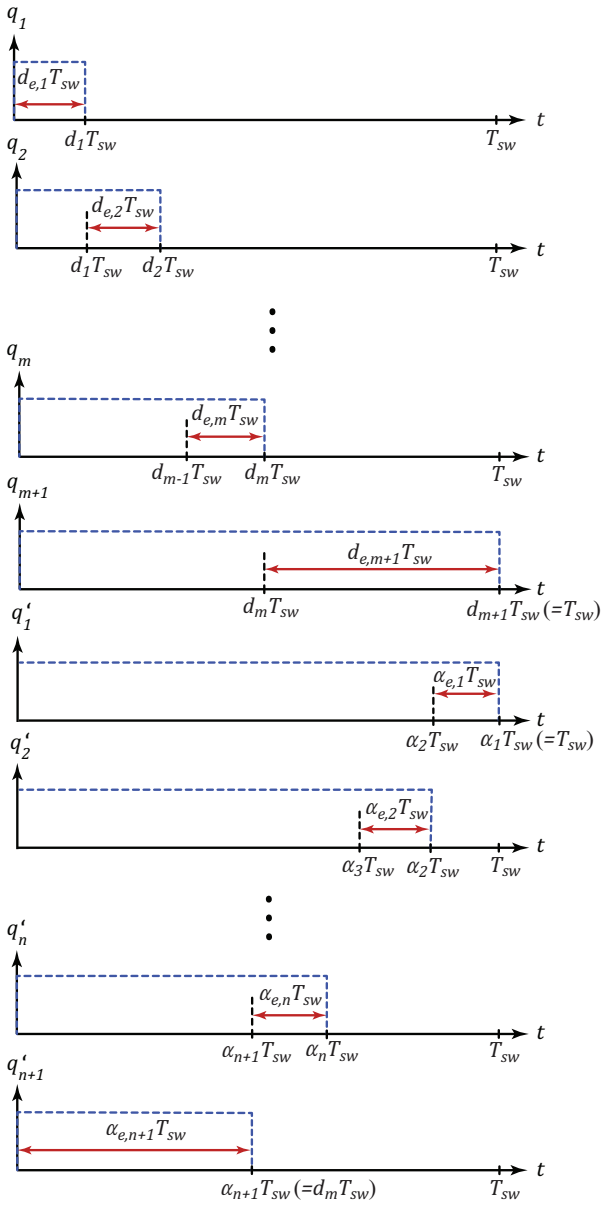

Figure 2.2 The designated switching scheme for the independent-output MIMO converter.

If two or more input switches are turned on, only the one connected to the highest input voltage conducts. This is the input switch with the lowest index. Likewise, if two or more output switches are turned on, only the one connected to the lowest output voltage conducts. This is the commanded output switch with the highest index. This property of the FCBB switches enables defining the concept of effective duty cycles for both input and output switches. A similar notion of the effective duty cycles for FCBB switches is defined in [6, 7] for MISO converters.

The effective duty cycles of input and output switches are denoted by $d_{e,1}, d_{e,2}, \dots, d_{e,m+1}$ and $\alpha_{e,1}, \alpha_{e,2}, \dots, \alpha_{e,n+1}$, respectively. These effective duty cycles are shown in Figure 2.2. The effective duty cycles of input switches, $d_{e,i}$, can be expressed in terms of commanded input duty cycles, d_i, as

$$d_{e,i} = \begin{cases} 0 & ,d_i < \sum_{k=1}^{i-1} d_{e,k} \\ d_i - \sum_{k=1}^{i-1} d_{e,k} & ,d_i \geq \sum_{k=1}^{i-1} d_{e,k} \end{cases} \tag{2.1}$$

where $i = 2, \dots, m+1$ and $d_{e,1} = d_1$. Similarly, the effective output duty cycles, $\alpha_{e,j}$, can be expressed in terms of the commanded output duty cycles, α_j, as

$$\alpha_{e,j} = \begin{cases} 0 & ,\alpha_j < \sum_{k=j+1}^{n+1} \alpha_{e,k} \\ \alpha_j - \sum_{k=j+1}^{n+1} \alpha_{e,k} & ,\alpha_j \geq \sum_{k=j+1}^{n+1} \alpha_{e,k} \end{cases} \tag{2.2}$$

where $j = 1,2, \dots, n$ and $\alpha_{e,n+1} = \alpha_{n+1}$. On the other hand, given a set of effective input and output duty cycles, $d_{e,i}$ and $\alpha_{e,j}$, the commanded duty cycles, d_i and α_j, can be calculated to be used by the modulation circuitry as follows.

$$d_i = \sum_{k=1}^{i} d_{e,k} \quad ,i = 1, \dots, m+1 \tag{2.3}$$

$$\alpha_j = \sum_{k=j}^{n+1} \alpha_{e,k} \quad ,j = 1,...,n+1. \tag{2.4}$$

In each sequential switching state, either one source is utilized or one load is powered. This time multiplexing method is prevalent in MISO dc-dc converters [5-7, 25]. Pulsating input currents is one of the inherent characteristics of this method, which can be justified by simplicity and compactness of the converter structure. Moreover, additional input current filters can be employed for those input sources that are unable to tolerate pulsating currents.

2.2 Dynamic Characterization

Dynamic characterization is an indispensable part of analyzing PWM converters. Proper controller design and stability analysis require extracting the dynamic model of the converter around the designated operating point (equilibrium point). Several dynamic characterization methods have been well studied in the literature including SSA, CA, and GSSA [26, 27]; among which SSA is the most well-established method; it is considered here.

First, the SSA model for a general m-input n-output converter is developed. Then, using the general model, the equivalent small-signal circuit for a two-input two-output converter is derived and different input to output transfer functions are obtained.

2.2.1 SSA for a General m-input n-output Converter

2.2.1.1 Average Model

SSA is based on the state-space description of the converter in each switching state. Assuming a m-input n-output converter, the state-space description of the converter in each switching state can be expressed as

$$\begin{cases} \mathbf{K}\dfrac{d\mathbf{x}(t)}{dt} = \mathbf{A}_i\mathbf{x}(t) + \mathbf{B}_i\mathbf{u}(t) \\ \mathbf{y}(t) = \mathbf{C}_i\mathbf{x}(t) + \mathbf{D}_i\mathbf{u}(t) \end{cases} \quad ,i = 1,\cdots,m+n, \tag{2.5}$$

where $\mathbf{x}(t)$, $\mathbf{u}(t)$, and $\mathbf{y}(t)$ are state, input, and output vectors:

$$\mathbf{x}(t)=\begin{bmatrix} v_{C_1} \\ \vdots \\ v_{C_n} \\ i_L \end{bmatrix}_{n+1}, \mathbf{u}(t)=\begin{bmatrix} v_{in,1} \\ \vdots \\ v_{in,m} \end{bmatrix}_{m}, \mathbf{y}(t)=\begin{bmatrix} i_{in,1} \\ \vdots \\ i_{in,m} \end{bmatrix}_{m}. \tag{2.6}$$

The outputs are arbitrarily chosen to be the input currents, $i_{in,1},\dots,i_{in,m}$. This assumption will simplify the derivation of equivalent small-signal circuit. Matrices $\mathbf{A}_i$, $\mathbf{B}_i$, $\mathbf{C}_i$, and $\mathbf{D}_i$ are state matrix, input matrix, output matrix, and feed-forward matrix, respectively. Matrix $\mathbf{K}$ depends on the inductance and capacitance values of the energy storage components and remains constant during all switching states. The first m switching states ($i=1,\dots,m$) pertain to the charging subinterval of the inductor whereas the last n switching states ($i=m+1,\dots,m+n$) pertain to its discharging subinterval.

The basic principle of SSA states that the average of the product of a switching function (e.g. q_i) and one of the system vectors (e.g. $\mathbf{x}(t)$) can be approximated by the product of their averages over a switching period, T_s. In other words,

$$\left\langle q_i\mathbf{x}(t)\right\rangle_{T_s}=\left\langle q_i\right\rangle_{T_s}\left\langle \mathbf{x}(t)\right\rangle_{T_s}=d_i\left\langle \mathbf{x}(t)\right\rangle_{T_s} \tag{2.7}$$

where $\langle\,\rangle_{T_s}$ denotes the moving average of a signal over a switching period, T_s.

In order to apply the basic principle of SSA to MIMO converters, two modifications should be applied to (2.7). First, since the effective duty cycles are involved rather than commanded duty cycles, $d_{e,i}$ should be used in (2.7) instead of d_i. Second, for output switches, q_i' and $\alpha_{e,i}$ should be considered. Applying SSA to the state-space description of the converter (2.5), results in

$$\begin{cases} \mathbf{K}\dfrac{d\left\langle \mathbf{x}(t)\right\rangle_{T_s}}{dt}=\overline{\mathbf{A}}\left\langle \mathbf{x}(t)\right\rangle_{T_s}+\overline{\mathbf{B}}\left\langle \mathbf{u}(t)\right\rangle_{T_s} \\ \left\langle \mathbf{y}(t)\right\rangle_{T_s}=\overline{\mathbf{C}}\left\langle \mathbf{x}(t)\right\rangle_{T_s}+\overline{\mathbf{D}}\left\langle \mathbf{u}(t)\right\rangle_{T_s} \end{cases} \tag{2.8}$$

where

$$\left\langle \mathbf{x}(t)\right\rangle_{T_s}=\begin{bmatrix}\left\langle v_{C_1}\right\rangle_{T_s}\\ \vdots \\ \left\langle v_{C_n}\right\rangle_{T_s}\\ \left\langle i_L\right\rangle_{T_s}\end{bmatrix},\left\langle \mathbf{u}(t)\right\rangle_{T_s}=\begin{bmatrix}\left\langle v_{in,1}\right\rangle_{T_s}\\ \vdots \\ \left\langle v_{in,m}\right\rangle_{T_s}\end{bmatrix},\left\langle \mathbf{y}(t)\right\rangle_{T_s}=\begin{bmatrix}\left\langle i_{in,1}\right\rangle_{T_s}\\ \vdots \\ \left\langle i_{in,m}\right\rangle_{T_s}\end{bmatrix} \tag{2.9}$$

The average state, $\overline{\mathbf{A}}$, input, $\overline{\mathbf{B}}$, output, $\overline{\mathbf{C}}$, and feedforward, $\overline{\mathbf{D}}$, matrices can be found as follows.

$$\begin{cases}\overline{\mathbf{A}}=\sum_{i=1}^{m}d_{e,i}(t)\mathbf{A}_i+\sum_{j=1}^{n}\alpha_{e,j}(t)\mathbf{A}_{m+n-j+1}\\ \overline{\mathbf{B}}=\sum_{i=1}^{m}d_{e,i}(t)\mathbf{B}_i+\sum_{j=1}^{n}\alpha_{e,j}(t)\mathbf{B}_{m+n-j+1}\\ \overline{\mathbf{C}}=\sum_{i=1}^{m}d_{e,i}(t)\mathbf{C}_i+\sum_{j=1}^{n}\alpha_{e,j}(t)\mathbf{C}_{m+n-j+1}\\ \overline{\mathbf{D}}=\sum_{i=1}^{m}d_{e,i}(t)\mathbf{D}_i+\sum_{j=1}^{n}\alpha_{e,j}(t)\mathbf{D}_{m+n-j+1}\end{cases} \tag{2.10}$$

It should be noted that the first output's effective duty cycles, $\alpha_{e,1}(t)$, is uncontrollable since it belongs to a diode, D_1'. This duty cycle is internally determined such that the summation of all effective duty cycles will be 1. Hence, it can be expressed in terms of the other effective duty cycles as

$$\alpha_{e,1}(t)=1-\sum_{i=1}^{m}d_{e,i}(t)-\sum_{j=2}^{n}\alpha_{e,j}(t). \tag{2.11}$$

Considering (2.11), (2.10) can be modified as follows.

$$\begin{aligned}\overline{\mathbf{A}}&=\mathbf{A}_{m+n}+\sum_{i=1}^{m}d_{e,i}(t)\left(\mathbf{A}_i-\mathbf{A}_{m+n}\right)+\sum_{j=2}^{n}\alpha_{e,j}(t)\left(\mathbf{A}_{m+n-j+1}-\mathbf{A}_{m+n}\right).\\ \overline{\mathbf{B}}&=\mathbf{B}_{m+n}+\sum_{i=1}^{m}d_{e,i}(t)\left(\mathbf{B}_i-\mathbf{B}_{m+n}\right)+\sum_{j=2}^{n}\alpha_{e,j}(t)\left(\mathbf{B}_{m+n-j+1}-\mathbf{B}_{m+n}\right).\\ \overline{\mathbf{C}}&=\mathbf{C}_{m+n}+\sum_{i=1}^{m}d_{e,i}(t)\left(\mathbf{C}_i-\mathbf{C}_{m+n}\right)+\sum_{j=2}^{n}\alpha_{e,j}(t)\left(\mathbf{C}_{m+n-j+1}-\mathbf{C}_{m+n}\right).\\ \overline{\mathbf{D}}&=\mathbf{D}_{m+n}+\sum_{i=1}^{m}d_{e,i}(t)\left(\mathbf{D}_i-\mathbf{D}_{m+n}\right)+\sum_{j=2}^{n}\alpha_{e,j}(t)\left(\mathbf{D}_{m+n-j+1}-\mathbf{D}_{m+n}\right).\end{aligned} \tag{2.12}$$

2.2.1.2 Linearization and Equilibrium Point

In steady-state, the averaged state variables, $\langle \mathbf{x}(t) \rangle_{T_s}$, inputs, $\langle \mathbf{u}(t) \rangle_{T_s}$, and outputs, $\langle \mathbf{y}(t) \rangle_{T_s}$, are supposed to be settled at a desired equilibrium point. They can be expressed in terms of their steady-state values (at the equilibrium point) and perturbations around it:

$$\begin{cases} \left\langle \mathbf{x}(t) \right\rangle_{T_s} = \mathbf{X} + \left\langle \hat{\mathbf{x}}(t) \right\rangle_{T_s} \\ \left\langle \mathbf{u}(t) \right\rangle_{T_s} = \mathbf{U} + \left\langle \hat{\mathbf{u}}(t) \right\rangle_{T_s} \\ \left\langle \mathbf{y}(t) \right\rangle_{T_s} = \mathbf{Y} + \left\langle \hat{\mathbf{y}}(t) \right\rangle_{T_s} \end{cases} \tag{2.13}$$

where **X**, **U**, **Y** represent the equilibrium point for state variables, inputs, and outputs, respectively; $\langle \hat{\mathbf{x}}(t) \rangle_{T_s}$, $\langle \hat{\mathbf{u}}(t) \rangle_{T_s}$, and $\langle \hat{\mathbf{y}}(t) \rangle_{T_s}$, denote the corresponding perturbations around the equilibrium point. The input and output duty cycles can be similarly expressed in terms of their values at the equilibrium point and perturbations around them:

$$\begin{cases} d_{e,i}(t) = D_{e,i} + \hat{d}_{e,i}(t) \\ \alpha_{e,j}(t) = A_{e,j} + \hat{\alpha}_{e,j}(t) \end{cases} \tag{2.14}$$

where $D_{e,i}$ and $A_{e,j}$ denote the equilibrium point values of $d_{e,i}(t)$ and $\alpha_{e,j}(t)$, respectively.

Substituting (2.13) and (2.14) into (2.8) and discarding the perturbation terms, one may find the basic algebraic equations that govern the steady state operation of the converter:

$$\begin{cases} \mathbf{0} = \mathbf{AX} + \mathbf{BU} \\ \mathbf{Y} = \mathbf{CX} + \mathbf{DU} \end{cases} \tag{2.15}$$

where

$$\begin{cases} \mathbf{A} = \sum_{i=1}^{m} D_{e,i}\mathbf{A}_i + \sum_{j=1}^{n} A_{e,j}\mathbf{A}_{m+n-j+1} \\ \mathbf{B} = \sum_{i=1}^{m} D_{e,i}\mathbf{B}_i + \sum_{j=1}^{n} A_{e,j}\mathbf{B}_{m+n-j+1} \\ \mathbf{C} = \sum_{i=1}^{m} D_{e,i}\mathbf{C}_i + \sum_{j=1}^{n} A_{e,j}\mathbf{C}_{m+n-j+1} \\ \mathbf{D} = \sum_{i=1}^{m} D_{e,i}\mathbf{D}_i + \sum_{j=1}^{n} A_{e,j}\mathbf{D}_{m+n-j+1} \end{cases} . \tag{2.16}$$

Thus, the steady-state values of state variables, **X**, and outputs, **Y**, (i.e. equilibrium point) can be found as follows.

$$\begin{cases} \mathbf{X} = -\mathbf{A}^{-1}\mathbf{B}\mathbf{U} \\ \mathbf{Y} = \left(\mathbf{D} - \mathbf{C}\mathbf{A}^{-1}\mathbf{B}\right)\mathbf{U} \end{cases} \tag{2.17}$$

Equation (2.17) is used to design a proper equilibrium point for the converter, i.e., determining the required $D_{e,i}$ and $A_{e,j}$ to achieve the desired **X** and **Y**.

Substituting (2.13) and (2.14) into (2.8) and (2.12), one can find the SSA model for a general m-input n-output converter. In order to linearize the obtained model, the higher order terms that pertain to multiplication of two perturbation signals (e.g. $\hat{d}_{e,i}\langle\hat{\mathbf{x}}(t)\rangle_{T_s}$), should be discarded. The resulted linearized SSA model can be found as follows.

$$\begin{cases} \mathbf{K}\dfrac{d\left\langle\hat{\mathbf{x}}(t)\right\rangle_{T_s}}{dt} = \mathbf{A}\left\langle\hat{\mathbf{x}}(t)\right\rangle_{T_s} + \mathbf{B}\left\langle\hat{\mathbf{u}}(t)\right\rangle_{T_s} + \sum_{i=1}^{m}\mathbf{F}_i\hat{d}_{e,i}(t) + \sum_{j=2}^{n}\mathbf{G}_j\hat{\alpha}_{e,j}(t) . \\ \left\langle\hat{\mathbf{y}}(t)\right\rangle_{T_s} = \mathbf{C}\left\langle\hat{\mathbf{x}}(t)\right\rangle_{T_s} + \mathbf{D}\left\langle\hat{\mathbf{u}}(t)\right\rangle_{T_s} + \sum_{i=1}^{m}\mathbf{L}_i\hat{d}_{e,i}(t) + \sum_{j=2}^{n}\mathbf{M}_j\hat{\alpha}_{e,j}(t) . \end{cases} \tag{2.18}$$

where

$$\begin{cases} \mathbf{F}_i = \left(\mathbf{A}_i - \mathbf{A}_{m+n}\right)\mathbf{X} + \left(\mathbf{B}_i - \mathbf{B}_{m+n}\right)\mathbf{U} \\ \mathbf{G}_j = \left(\mathbf{A}_{m+n-j+1} - \mathbf{A}_{m+n}\right)\mathbf{X} + \left(\mathbf{B}_{m+n-j+1} - \mathbf{B}_{m+n}\right)\mathbf{U} \\ \mathbf{L}_i = \left(\mathbf{C}_i - \mathbf{C}_{m+n}\right)\mathbf{X} + \left(\mathbf{D}_i - \mathbf{D}_{m+n}\right)\mathbf{U} \\ \mathbf{M}_j = \left(\mathbf{C}_{m+n-j+1} - \mathbf{C}_{m+n}\right)\mathbf{X} + \left(\mathbf{D}_{m+n-j+1} - \mathbf{D}_{m+n}\right)\mathbf{U} \end{cases}. \tag{2.19}$$

As suggested by (2.18), matrices $\mathbf{F}_i$, $\mathbf{G}_j$, $\mathbf{L}_i$, and $\mathbf{M}_j$ determine the effect of the effective input and output duty cycles, $\hat{d}_{e,i}$ and $\hat{\alpha}_{e,j}$, on the state-space equations of the linearized SSA model.

2.2.2 Model Development for a Two-input Two-output Converter

2.2.2.1 Average Model

According to (2.6), the state, $\mathbf{x}(t)$, input, $\mathbf{u}(t)$, and output, $\mathbf{y}(t)$, vectors for a two-input two-output converter are

$$\mathbf{x}(t) = \begin{bmatrix} v_{C_1} \\ v_{C_2} \\ i_L \end{bmatrix}, \quad \mathbf{u}(t) = \begin{bmatrix} v_{in,1} \\ v_{in,2} \end{bmatrix}, \quad \mathbf{y}(t) = \begin{bmatrix} i_{in,1} \\ i_{in,2} \end{bmatrix}. \tag{2.20}$$

Since two inputs and two outputs are considered, four switching states exist. The state-space description of the two-input two-output converter in these switching states can be written in a lumped format as follows.

$$\begin{cases} C_1 \dfrac{dv_{C_1}}{dt} = -\dfrac{v_{C_1}}{R_1} + (q_1' - q_2')i_L \\ C_2 \dfrac{dv_{C_2}}{dt} = -\dfrac{v_{C_2}}{R_2} + (q_2' - q_3')i_L \\ L\dfrac{di_L}{dt} = (q_2' - q_1')v_{C_1} + (q_3' - q_2')v_{C_2} + q_1 v_{in,1} + q_2 v_{in,2} \end{cases}, \tag{2.21}$$

$$\begin{cases} i_{in,1} = q_1 i_L \\ i_{in,2} = (q_2 - q_1)i_L \end{cases}.$$

The state, input, output, and feedforward matrices pertaining to each switching state, $\mathbf{A}_i$, $\mathbf{B}_i$, $\mathbf{C}_i$, and $\mathbf{D}_i$, can be extracted from the state-space equation in (2.21). This step is skipped here for conciseness.

2.2.2.2 Equilibrium Point

Considering (2.16) and the system matrices pertaining to each switching state, $\mathbf{A}_i$, $\mathbf{B}_i$, $\mathbf{C}_i$, and $\mathbf{D}_i$, the averaged system matrices in equilibrium point, **A**, **B**, **C**, and **D**, can be obtained as follows.

$$\mathbf{A}=\begin{bmatrix} \frac{-1}{R_1} & 0 & A_{e,1} \\ 0 & \frac{-1}{R_2} & A_{e,2} \\ -A_{e,1} & -A_{e,2} & 0 \end{bmatrix}, \mathbf{B}=\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ D_{e,1} & D_{e,2} \end{bmatrix}, \mathbf{C}=\begin{bmatrix} 0 & 0 & D_{e,1} \\ 0 & 0 & D_{e,2} \end{bmatrix}, \mathbf{D}=\mathbf{0}_{2\times 2}. \tag{2.22}$$

Thus, the equilibrium values (steady-state values) of the state variables, **X**, and outputs, **Y**, can be found using (2.17) and (2.22):

$$\mathbf{X}=\begin{bmatrix} V_{C_1} \\ V_{C_2} \\ I_L \end{bmatrix}=\begin{bmatrix} \frac{R_1 A_{e,1}(V_{in,1}D_{e,1}+V_{in,2}D_{e,2})}{R_1 A_{e,1}^2+R_2 A_{e,2}^2} \\ \frac{R_2 A_{e,2}(V_{in,1}D_{e,1}+V_{in,2}D_{e,2})}{R_1 A_{e,1}^2+R_2 A_{e,2}^2} \\ \frac{V_{in,1}D_{e,1}+V_{in,2}D_{e,2}}{R_1 A_{e,1}^2+R_2 A_{e,2}^2} \end{bmatrix}, \mathbf{Y}=\begin{bmatrix} I_{in,1} \\ I_{in,2} \end{bmatrix}=\begin{bmatrix} \frac{D_{e,1}(V_{in,1}D_{e,1}+V_{in,2}D_{e,2})}{R_1 A_{e,1}^2+R_2 A_{e,2}^2} \\ \frac{D_{e,2}(V_{in,1}D_{e,1}+V_{in,2}D_{e,2})}{R_1 A_{e,1}^2+R_2 A_{e,2}^2} \end{bmatrix} \tag{2.23}$$

It should be noted that assuming an ideal converter, the capacitors' voltages in (2.23) are the same as output voltages. Thus, the first two rows of vector **X** in (2.23) are the steady-state conversion ratios of the converter from $V_{in,1}$ and $V_{in,2}$ to $V_{o,1}$ and $V_{o,2}$. Using the same method, it can be shown in general that the conversion ratios for a general m-input n-output converter have the same form:

$$V_{o,j}=\frac{A_{e,j}\sum_{i=1}^{m}V_{in,i}D_{e,i}}{\sum_{k=1}^{n}n_{k,j}A_{e,k}^2},\ n_{k,j}=\frac{R_k}{R_j},\quad j=1,\cdots,n, \tag{2.24}$$

Similarly, the inductor average current, I_L, and average input currents, $I_{in,i}$, for a general m-input n-output converter have the same form as those of two-input two-output converter in (2.23):

$$I_L = \frac{\sum_{i=1}^{m} V_{in,i} D_{e,i}}{\sum_{j=1}^{n} R_j A_{e,j}^2}, \quad I_{in,i} = \frac{D_{e,i} \sum_{k=1}^{m} V_{in,k} D_{e,k}}{\sum_{j=1}^{n} R_j A_{e,j}^2}, \quad i = 1, \cdots, m. \tag{2.25}$$

2.2.2.3 Linearization and Small-signal Model Extraction

Applying the general linearized SSA model in (2.18) and (2.19) to the two-input two-output converter with the switching states described in (2.21) results in (2.26). Equations (2.26) describes the linearized small-signal SSA model for the two-input two-output converter. This model can be used to construct the equivalent small-signal circuit for a two-input two-output converter.

$$\underbrace{\begin{bmatrix} C_1 & 0 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & L \end{bmatrix}}_{\mathbf{K}} \frac{d}{dt} \underbrace{\begin{bmatrix} \hat{\langle} v_{C_1}(t) \hat{\rangle}_{T_s} \\ \hat{\langle} v_{C_2}(t) \hat{\rangle}_{T_s} \\ \hat{\langle} i_L(t) \hat{\rangle}_{T_s} \end{bmatrix}}_{\hat{\langle} \mathbf{x}(t) \hat{\rangle}_{T_s}} = \underbrace{\begin{bmatrix} \frac{-1}{R_1} & 0 & A_{e,1} \\ 0 & \frac{-1}{R_2} & A_{e,2} \\ -A_{e,1} & -A_{e,2} & 0 \end{bmatrix}}_{\mathbf{A}} \underbrace{\begin{bmatrix} \hat{\langle} v_{C_1}(t) \hat{\rangle}_{T_s} \\ \hat{\langle} v_{C_2}(t) \hat{\rangle}_{T_s} \\ \hat{\langle} i_L(t) \hat{\rangle}_{T_s} \end{bmatrix}}_{\hat{\langle} \mathbf{x}(t) \hat{\rangle}_{T_s}}$$

$$+ \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ D_{e,1} & D_{e,2} \end{bmatrix}}_{\mathbf{B}} \underbrace{\begin{bmatrix} \hat{\langle} v_{in,1}(t) \hat{\rangle}_{T_s} \\ \hat{\langle} v_{in,2}(t) \hat{\rangle}_{T_s} \end{bmatrix}}_{\hat{\langle} \mathbf{u}(t) \hat{\rangle}_{T_s}} + \underbrace{\begin{bmatrix} -I_L \\ 0 \\ V_{C_1} + V_{in,1} \end{bmatrix}}_{\mathbf{F}_1} \hat{d}_{e,1}(t) + \underbrace{\begin{bmatrix} -I_L \\ 0 \\ V_{C_1} + V_{in,2} \end{bmatrix}}_{\mathbf{F}_2} \hat{d}_{e,2}(t) + \underbrace{\begin{bmatrix} -I_L \\ I_L \\ V_{C_1} - V_{C_2} \end{bmatrix}}_{\mathbf{G}_2} \hat{\alpha}_{e,2}(t),$$

$$\underbrace{\begin{bmatrix} \hat{\langle} i_{in,1}(t) \hat{\rangle}_{T_s} \\ \hat{\langle} i_{in,2}(t) \hat{\rangle}_{T_s} \end{bmatrix}}_{\hat{\langle} \mathbf{y}(t) \hat{\rangle}_{T_s}} = \underbrace{\begin{bmatrix} 0 & 0 & D_{e,1} \\ 0 & 0 & D_{e,2} \end{bmatrix}}_{\mathbf{C}} \begin{bmatrix} \hat{\langle} v_{C_1}(t) \hat{\rangle}_{T_s} \\ \hat{\langle} v_{C_2}(t) \hat{\rangle}_{T_s} \\ \hat{\langle} i_L(t) \hat{\rangle}_{T_s} \end{bmatrix} + \underbrace{\begin{bmatrix} I_L \\ 0 \end{bmatrix}}_{\mathbf{L}_1} \hat{d}_{e,1}(t) + \underbrace{\begin{bmatrix} 0 \\ I_L \end{bmatrix}}_{\mathbf{L}_2} \hat{d}_{e,2}(t). \tag{2.26}$$

2.2.2.4 Equivalent Small-signal Circuit

An equivalent small-signal circuit can be constructed from the linearized small-signal SSA model in (2.26). This equivalent circuit helps to better understand the dynamics of the converter. Moreover, extracting the input-to-output transfer functions is more straightforward using this equivalent circuit rather than inspecting (2.26).

Figure 2.3(a and b) depict the equivalent small-signal circuits corresponding to the first and second row of the algebraic equations in (2.26), pertaining to $\langle i_{in,1}\hat{(t)}\rangle_{T_s}$ and $\langle i_{in,2}\hat{(t)}\rangle_{T_s}$, respectively. These sub-circuits illustrate the dynamics of the input ports of the converter. Similarly, Figure 2.3(c, d, and e) pertain to the first, second, and third rows of the differential equations in (2.26), pertaining to $\langle v_{C_1}\hat{(t)}\rangle_{T_s}$, $\langle v_{C_2}\hat{(t)}\rangle_{T_s}$, and $\langle i_L\hat{(t)}\rangle_{T_s}$, respectively. These sub-circuits illustrate the dynamics of the inductor and the output ports of the converter.

The dependent current source $D_{e,1}\langle i_L\hat{(t)}\rangle_{T_s}$ in the sub-circuit shown in Figure 2.3(a) and the dependent voltage source $D_{e,1}\langle \hat{v}_{in,1}(t)\rangle_{T_s}$ in the sub-circuit shown in Figure 2.3(e) imply the presence of a transformer between these sub-circuits. The turn-ratio of this transformer is $1: D_{e,1}$. Similarly, other coupled dependent voltage and current sources can be identified in Figure 2.3(a-e). These coupled dependent sources are depicted in squares whereas the independent sources are shown in circles. Replacing the coupled dependent current and voltage sources by the equivalent transformers, all sub-circuits in Figure 2.3(a-e) can be combined together and a lumped equivalent circuit can be constructed. Figure 2.4 depicts the lumped equivalent small-signal circuit.

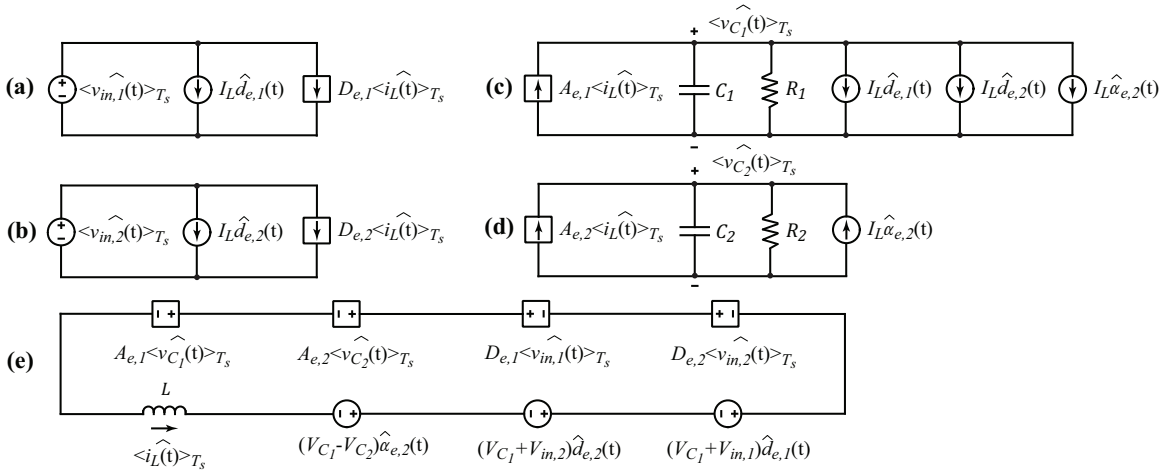

Figure 2.3 The equivalent small-signal circuits describing the converter's dynamics.

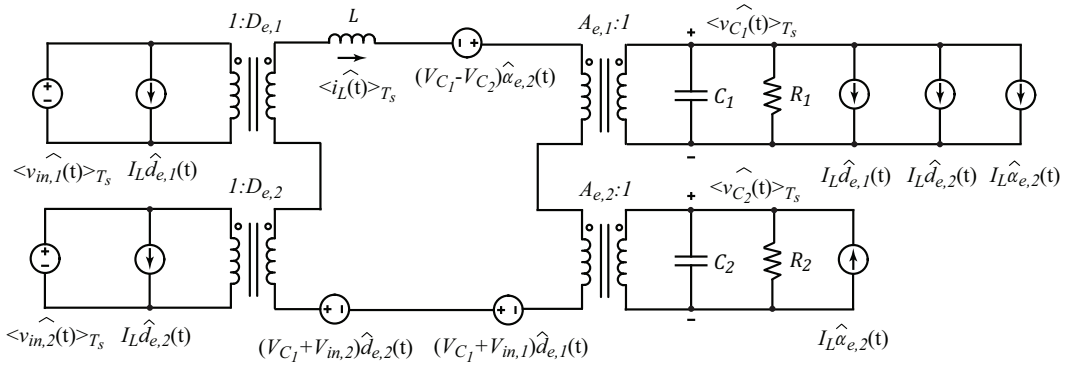

Figure 2.4 The lumped equivalent small-signal circuit describing converter's dynamics.

2.2.2.5 Input-to-output Transfer Functions

Using the lumped equivalent small-signal circuit in Figure 2.4, different input-to-output transfer functions can be derived. To this point, the outputs have been defined as the input currents, $i_{in,1}$ and $i_{in,2}$ in (2.20). This assumption was made to simplify development of the equivalent small-signal circuit. Now that the small-signal circuit is found, the outputs of the system can be defined as the output voltages (capacitors' voltages) since they need to be tightly regulated. In addition, the inputs of the system are comprised of three categories: the input voltages, $\langle \hat{v}_{in,1}(t) \rangle_{T_s}$, the effective input duty cycles, $\hat{d}_{e,i}$, and the

effective output duty cycles, $\hat{\alpha}_{e,i}$. Thus, three types of input-to-output transfer functions can be identified as illustrated in Figure 2.5. The transfer function matrix, $\mathbf{H}(s)$, can be defined, elements of which are the input-to-output transfer functions

$$\mathbf{H}(s) = [\mathbf{H}^d(s) \mid \mathbf{H}^\alpha(s) \mid \mathbf{H}^v(s)], \tag{2.27}$$

$$\begin{aligned}
\mathbf{H}^d(s) &= \begin{bmatrix} H_{11}^d(s) & \cdots & H_{m1}^d(s) \\ H_{12}^d(s) & \cdots & H_{m2}^d(s) \\ \vdots & \ddots & \vdots \\ H_{1n}^d(s) & \cdots & H_{mn}^d(s) \end{bmatrix}, \mathbf{H}^\alpha(s) = \begin{bmatrix} H_{21}^\alpha(s) & \cdots & H_{n1}^\alpha(s) \\ H_{22}^\alpha(s) & \cdots & H_{n2}^\alpha(s) \\ \vdots & \ddots & \vdots \\ H_{2n}^\alpha(s) & \cdots & H_{nn}^\alpha(s) \end{bmatrix}, \\
\mathbf{H}^v(s) &= \begin{bmatrix} H_{11}^v(s) & \cdots & H_{m1}^v(s) \\ H_{12}^v(s) & \cdots & H_{m2}^v(s) \\ \vdots & \ddots & \vdots \\ H_{1n}^v(s) & \cdots & H_{mn}^v(s) \end{bmatrix}.
\end{aligned} \tag{2.28}$$

Thus,

$$\begin{bmatrix} \hat{\langle v_{o,1} \rangle}_{T_s}(s) \\ \hat{\langle v_{o,2} \rangle}_{T_s}(s) \\ \vdots \\ \hat{\langle v_{o,n} \rangle}_{T_s}(s) \end{bmatrix} = \mathbf{H}(s) \times \begin{bmatrix} \hat{\mathbf{d}}_e(s) \\ \hat{\boldsymbol{\alpha}}_e(s) \\ \hat{\langle \mathbf{v}_{in} \rangle}_{T_s}(s) \end{bmatrix}, \hat{\mathbf{d}}_e(s) = \begin{bmatrix} \hat{d}_{e,1}(s) \\ \vdots \\ \hat{d}_{e,m}(s) \end{bmatrix}, \hat{\boldsymbol{\alpha}}_e(s) = \begin{bmatrix} \hat{\alpha}_{e,2}(s) \\ \vdots \\ \hat{\alpha}_{e,n}(s) \end{bmatrix}, \hat{\langle \mathbf{v}_{in} \rangle}_{T_s}(s) = \begin{bmatrix} \hat{\langle v_{in,1} \rangle}_{T_s}(s) \\ \vdots \\ \hat{\langle v_{in,m} \rangle}_{T_s}(s) \end{bmatrix}. \tag{2.29}$$

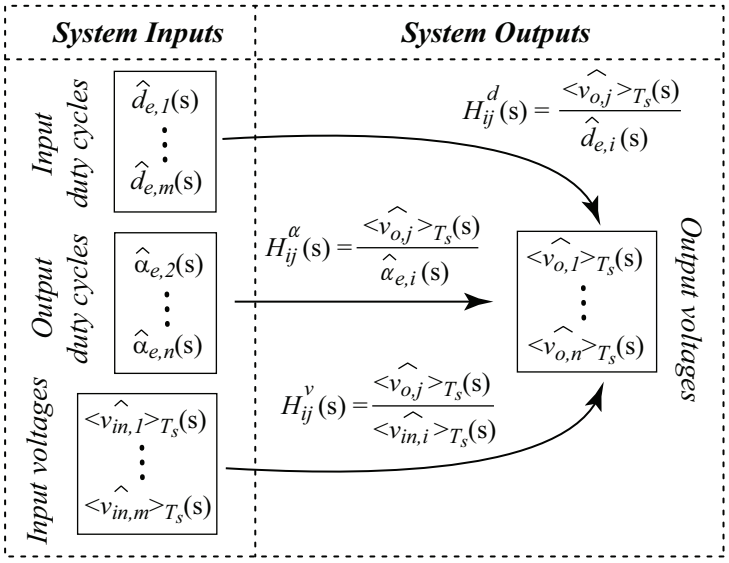

Figure 2.5 Definition of the system inputs, outputs, and input-to-output transfer functions.

For a two-input two-output converter, the dimensions of $\mathbf{H}(s)$ is 2×5; ten transfer functions can be identified. Here, the transfer function $H_{11}^{d}(s)$ is derived in terms of the circuit parameters:

$$H_{11}^{d}(s)=\frac{\beta_2^{d11}s^2+\beta_1^{d11}s+\beta_0^{d11}}{\mu_3 s^3+\mu_2 s^2+\mu_1 s+\mu_0} \tag{2.30}$$

This transfer functions will be used in the case studies section (section 2.4). The numerator and denominator coefficients of this transfer functions are given as follows.

$$\begin{cases}\mu_0 = R_1A_{e,1}^2+R_2A_{e,2}^2\\ \mu_1 = L+R_1R_2(C_2A_{e,1}^2+C_1A_{e,2}^2)\\ \mu_2 = (R_1C_1+R_2C_2)L\\ \mu_3 = R_1R_2LC_1C_2\end{cases}$$
$$\begin{cases}\beta_0^{d11} = (V_{C_1}+V_{in,1})A_{e,1}R_1-R_1R_2I_LA_{e,2}^2\\ \beta_1^{d11} = (V_{C_1}+V_{in,1})A_{e,1}R_1R_2C_2-LR_1I_L\\ \beta_2^{d11} = -R_1R_2C_2I_LL\end{cases} \tag{2.31}$$

Other input-to-output transfer functions can be similarly found by inspecting the lumped equivalent small-signal circuit (Figure 2.4).

2.3 Power Budgeting

The objective of this section is to design and analyze a MIMO controller that is able to regulate the input powers and output voltages at the same time. It should be noted that, assuming an ideal converter, the conservation of power principle implies that

$$\sum_{i=1}^{m} P_{in,i} = \sum_{j=1}^{n} \frac{V_{o,j}^2}{R_j}. \tag{2.32}$$

Hence, it is not possible to regulate all the input powers and output voltages at the same time; one of the inputs should be relaxed to supply arbitrary power. For the two-input two-output converter considered here, $P_{in,2}$ is relaxed.

Before designing the controller to regulate the output voltages and input powers, it is necessary to analyze the regulation problem in equilibrium point (steady-state). Then, a closed-loop MIMO controller can be designed around this equilibrium point. Using (2.25), for a m-input n-output converter, the input powers coming from diversified sources can be found as

$$P_{in,i} = V_{in,i} I_{in,i} = \frac{V_{in,i} D_{e,i} \sum_{k=1}^{m} V_{in,k} D_{e,k}}{\sum_{j=1}^{n} R_j A_{e,j}^2}, \quad i = 1,\ldots,m \tag{2.33}$$

in steady-state. Besides, proper output voltage regulation in steady-state requires that (2.24) is satisfied. Equation (2.24) and (2.33) form a set of $m+n$ nonlinear equations to be solved for the steady-state values of duty cycles, $D_{e,1}, \ldots, D_{e,m}, A_{e,2}, \ldots, A_{e,n}$. Only $m+n-1$ of these equations are independent since conservation of power must be satisfied (2.32). Besides, $A_{e,1}$ is not controllable since S_1' is a single diode; thus, there are $m+n-1$ unknown variables to solve for (the number of equations and unknown variables are equal). Once the steady-state values of $D_{e,1}, \ldots, D_{e,m}, A_{e,2}, \ldots, A_{e,n}$ are calculated, a MIMO controller can be designed around the corresponding equilibrium point.

2.3.1 Feedback Loop Design

The state-space description of the converter's small-signal model is needed for designing the controller. The small-signal SSA model developed in (2.26) can be used with two modifications. First, since the input voltage perturbations are not concerned when designing the controller, $\langle \hat{v}_{in,1}(t) \rangle_{T_s}$ and $\langle \hat{v}_{in,2}(t) \rangle_{T_s}$ in (2.26) can be neglected (set to zero). Then, by arranging the effective duty cycles as the input vector of the system, **u**, one can find

$$\frac{d}{dt}\begin{bmatrix} \hat{\langle i_L(t) \rangle}_{T_s} \\ \hat{\langle v_{C_1}(t) \rangle}_{T_s} \\ \hat{\langle v_{C_2}(t) \rangle}_{T_s} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & \frac{-A_{e,1}}{L} & \frac{-A_{e,2}}{L} \\ \frac{A_{e,1}}{C_1} & \frac{-1}{R_1 C_1} & 0 \\ \frac{A_{e,2}}{C_2} & 0 & \frac{-1}{R_2 C_2} \end{bmatrix}}_{\mathbf{A}_{ol}} \underbrace{\begin{bmatrix} \hat{\langle i_L(t) \rangle}_{T_s} \\ \hat{\langle v_{C_1}(t) \rangle}_{T_s} \\ \hat{\langle v_{C_2}(t) \rangle}_{T_s} \end{bmatrix}}_{\mathbf{x}} + \underbrace{\begin{bmatrix} \frac{V_{C_1}+V_{in,1}}{L} & \frac{V_{C_1}+V_{in,2}}{L} & \frac{V_{C_1}-V_{C_2}}{L} \\ \frac{-I_L}{C_1} & \frac{-I_L}{C_1} & \frac{-I_L}{C_1} \\ 0 & 0 & \frac{I_L}{C_2} \end{bmatrix}}_{\mathbf{B}_{ol}} \underbrace{\begin{bmatrix} \hat{d}_{e,1}(t) \\ \hat{d}_{e,2}(t) \\ \hat{\alpha}_{e,2}(t) \end{bmatrix}}_{\mathbf{u}}, \tag{2.34}$$

where **x**, $\mathbf{A}_{ol}$, and $\mathbf{B}_{ol}$ are the state vector, open-loop state matrix, and open-loop input matrix. In (2.20), system outputs were defined to be the input currents, to simplify derivation of the small-signal equivalent circuit. However, the outputs of the system for the purpose of controller design should be defined as the input powers and output voltages. The average power delivered by the first input source, $p_{in,1}(t)$, can be expressed as

$$\langle p_{in,1}(t) \rangle_{T_s} = V_{in,1} d_{e,1}(t) \langle i_L(t) \rangle_{T_s}. \tag{2.35}$$

Linearizing (2.35) around the equilibrium point, one may find

$$\hat{\langle p_{in,1}(t) \rangle}_{T_s} = V_{in,1} D_{e,1} \hat{\langle i_L(t) \rangle}_{T_s} + V_{in,1} I_L \hat{d}_{e,1}(t). \tag{2.36}$$

Thus, the system output equation can be written as

$$\underbrace{\begin{bmatrix} \hat{\langle p_{in,1}(t)\rangle}_{T_s} \\ \hat{\langle v_{o,1}(t)\rangle}_{T_s} \\ \hat{\langle v_{o,2}(t)\rangle}_{T_s} \end{bmatrix}}_{\mathbf{y}} = \underbrace{\begin{bmatrix} V_{in,1}D_{e,1} & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}}_{\mathbf{C}_{ol}} \underbrace{\begin{bmatrix} \hat{\langle i_L(t)\rangle}_{T_s} \\ \hat{\langle v_{C_1}(t)\rangle}_{T_s} \\ \hat{\langle v_{C_2}(t)\rangle}_{T_s} \end{bmatrix}}_{\mathbf{x}} + \underbrace{\begin{bmatrix} V_{in,1}I_L & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}}_{\mathbf{D}_{ol}} \underbrace{\begin{bmatrix} \hat{d}_{e,1}(t) \\ \hat{d}_{e,2}(t) \\ \hat{\alpha}_{e,2}(t) \end{bmatrix}}_{\mathbf{u}} \tag{2.37}$$

where $\mathbf{y}$, $\mathbf{C}_{ol}$, and $\mathbf{D}_{ol}$ are the output vector, output matrix, and feedforward matrix.

Equations (2.34) and (2.37) form the state-space description of the converter's small-signal model or simply the "plant" model. A closed-loop control scheme can be constructed around the plant model to regulate the outputs, $p_{in,1}(t)$, $v_{o,1}(t)$, and $v_{o,2}(t)$. Figure 2.6 illustrates such closed-loop control scheme using a MIMO PI controller. The integral and proportional terms, $\mathbf{K}_i$ and $\mathbf{K}_p$, of a MIMO PI controller are matrices as opposed to conventional PI controllers, where they are real numbers. The integrator part, $\mathbf{K}_i/s$, of the controller ensures eliminating the steady-state error between the output vector, $\mathbf{y}$, and reference vector, $\mathbf{r}$.

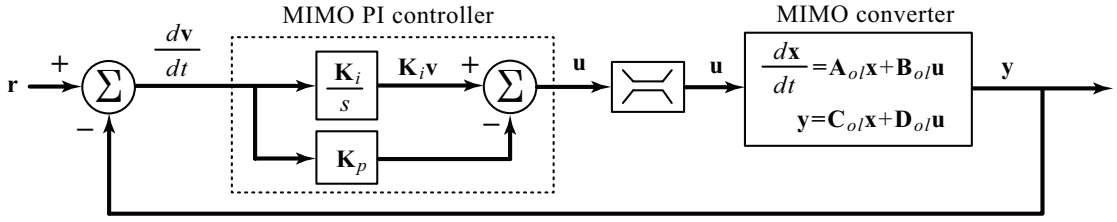

Figure 2.6 The closed-loop block diagram of the converter and controller.

Employing the MIMO PI controller introduces new state variables to the system, $\mathbf{v}$. In order to analyze the stability and dynamic performance of the closed-loop system, it is necessary to develop a new state-space description for the system that takes account of $\mathbf{v}$ as a part of the state vector. The differential equations governing the system block diagram in Figure 2.6 are

$$\begin{cases} \dfrac{d\mathbf{x}}{dt} = \mathbf{A}_{ol}\mathbf{x} + \mathbf{B}_{ol}\mathbf{u} \\ \mathbf{y} = \mathbf{C}_{ol}\mathbf{x} + \mathbf{D}_{ol}\mathbf{u} \\ \dfrac{d\mathbf{v}}{dt} = \mathbf{r} - \mathbf{y} \\ \mathbf{u} = \mathbf{K}_i\mathbf{v} + \mathbf{K}_p\dfrac{d\mathbf{v}}{dt} \end{cases} . \tag{2.38}$$

These equations can be manipulated to obtain the state space description of the closed-loop system as follows.

$$\begin{cases} \dfrac{d}{dt}\begin{bmatrix}\mathbf{x}\\ \mathbf{v}\end{bmatrix} = \mathbf{A}_{cl}\begin{bmatrix}\mathbf{x}\\ \mathbf{v}\end{bmatrix} + \mathbf{B}_{cl}\mathbf{r} \\ \mathbf{y} = \mathbf{C}_{cl}\begin{bmatrix}\mathbf{x}\\ \mathbf{v}\end{bmatrix} + \mathbf{D}_{cl}\mathbf{r} \end{cases} \tag{2.39}$$

where

$$\begin{aligned} \mathbf{A}_{cl} &= \begin{bmatrix} \mathbf{A}_{ol} - \mathbf{B}_{ol}\mathbf{K}_p(\mathbf{I}+\mathbf{D}_{ol}\mathbf{K}_p)^{-1}\mathbf{C}_{ol} & \mathbf{B}_{ol}(\mathbf{I}-\mathbf{K}_p(\mathbf{I}+\mathbf{D}_{ol}\mathbf{K}_p)^{-1}\mathbf{D}_{ol})\mathbf{K}_i \\ -(\mathbf{I}+\mathbf{D}_{ol}\mathbf{K}_p)^{-1}\mathbf{C}_{ol} & -(\mathbf{I}+\mathbf{D}_{ol}\mathbf{K}_p)^{-1}\mathbf{D}_{ol}\mathbf{K}_i \end{bmatrix} \\ \mathbf{B}_{cl} &= \begin{bmatrix} \mathbf{B}_{ol}\mathbf{K}_p(\mathbf{I}+\mathbf{D}_{ol}\mathbf{K}_p)^{-1} \\ (\mathbf{I}+\mathbf{D}_{ol}\mathbf{K}_p)^{-1} \end{bmatrix} \\ \mathbf{C}_{cl} &= [(\mathbf{I}+\mathbf{D}_{ol}\mathbf{K}_p)^{-1}\mathbf{C}_{ol} \quad (\mathbf{I}+\mathbf{D}_{ol}\mathbf{K}_p)^{-1}\mathbf{D}_{ol}\mathbf{K}_i] \\ \mathbf{D}_{cl} &= [(\mathbf{I}+\mathbf{D}_{ol}\mathbf{K}_p)^{-1}\mathbf{D}_{ol}\mathbf{K}_p] \end{aligned} \tag{2.40}$$

and $\mathbf{A}_{cl}$, $\mathbf{B}_{cl}$, $\mathbf{C}_{cl}$, and $\mathbf{D}_{cl}$ are the state, input, output, and feedthrough matrices of the closed-loop system.

2.3.2 Stability Analysis

In order for the designed closed-loop system to be stable, the eigenvalues of the closed-loop state matrix, $\mathbf{A}_{cl}$, must lie on the left-hand complex plane. In other words, the real part of the eigenvalues must be negative:

$$\begin{cases} \det(\lambda_i\mathbf{I} - \mathbf{A}_{cl}) = 0 \\ \forall\lambda_i : \quad \mathrm{Re}\{\lambda_i\} < 0 \end{cases} \quad ,i = 1,\cdots,2n+1 \tag{2.41}$$

2.4 Case Studies

2.4.1 Hardware Setup

A two-input two-output laboratory-scale prototype is built to evaluate the performance of the proposed topology. The hardware setup is shown in Figure 2.7. The circuit parameters of the implemented prototype are as follows. $V_{in,1} = 25\text{V}$, $V_{in,2} = 20\text{V}$, $L = 250\mu\text{H}$, $R_1 = 24\Omega$, $R_2 = 13\Omega$, $C_1 = 2200\mu\text{F}$, $C_2 = 2200\mu\text{F}$, $V_{o,1} = 22\text{V}$, and $V_{o,2} = 11\text{V}$. The controller algorithm is implemented in ezDSP-F2808 DSP board (target computer). The target computer is connected to a laptop (host computer) via USB JTAG emulation connector for real-time monitoring purposes. The first input's voltage and current, $v_{in,1}$ and $i_{in,1}$ are measured and fed to the target computer to compute the first input's power, $p_{in,1}$. The output voltages, $v_{o,1}$ and $v_{o,2}$ are also sampled by the target computer. Since the input current $i_{in,1}$ is pulsating, it goes through a second order analog Butterworth filter before being sampled by ADCs of the target computer. All other measured variables, $v_{in,1}$, $v_{o,1}$, and $v_{o,2}$, also go through the same analog filters to filter high-frequency components and avoid aliasing. The switching frequency and the cut-off frequencies of all Butterworth filters are 40kHz and 400Hz, respectively.

2.4.2 Converter Operation in Steady-state

Figure 2.8 illustrates the measured circuit waveforms in steady-state. The switching signals, q_1, q_2, q_2', corresponding to the active switches, S_1, S_2, and S_2', are depicted in Figure 2.8 for two switching cycles. As seen in Figure 2.8, the commanded duty cycles, d_1, d_2, α_2, are not the same as effective duty cycles, $d_{e,1}$, $d_{e,2}$, $\alpha_{e,2}$. In fact, the effective duty cycles, $d_{e,1}$, $d_{e,2}$, $\alpha_{e,2}$, and $\alpha_{e,1}$, determine the portions of the switching period that different input and output voltages, $V_{in,1}$, $V_{in,2}$, $V_{o,2}$, and $V_{o,1}$, are applied across the inductor, respectively. The measured voltages of the left and right sides of the inductor, v_a and v_b in Figure 2.1, and the inductor voltage, $v_L = v_a - v_b$, are also shown in Figure 2.8. As seen in Figure 2.8, the input and output voltages are applied to the inductor according to the pattern $V_{in,1}$, $V_{in,2}$, $-V_{o,2}$, $-V_{o,1}$, ..., and cause the inductor current to increase and decrease sequentially. The steady-state duty

cycles for regulation of output voltages and the first input power, $v_{o,1}$, $v_{o,2}$, and $p_{in,1}$, are measured to be $D_1 \approx 0.3$, $D_2 \approx 0.5$, $A_2 \approx 0.7$, which verify the steady-state characterizations in (2.24) and (2.25).

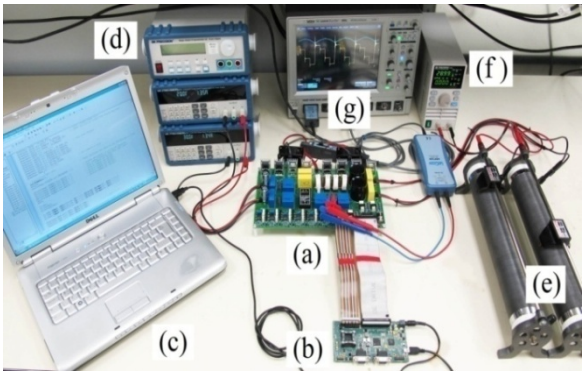

Figure 2.7 The hardware setup: (a) The converter prototype, (b) target computer (ezDSP-F2808 board), (c) host computer (laptop), (d) input voltage sources, (e) output static loads, (f) dynamic load, (g) oscilloscope.

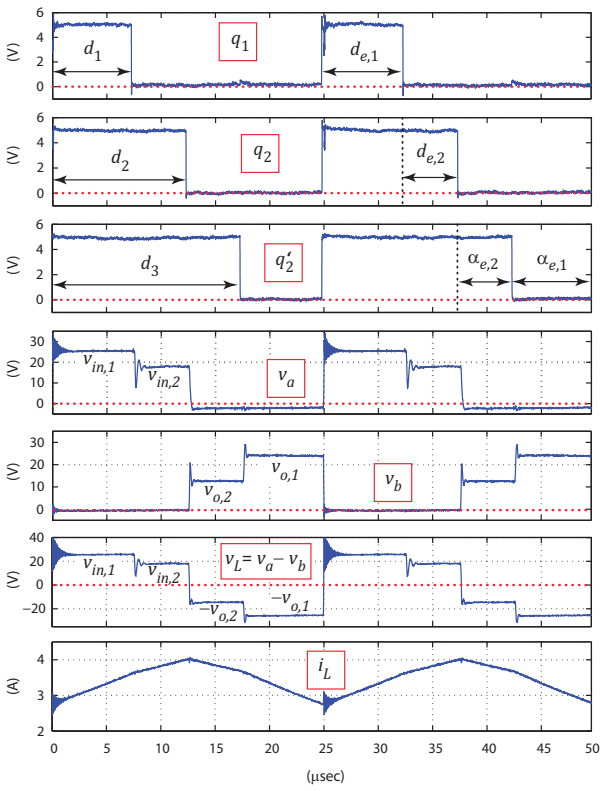

Figure 2.8 The measured circuit waveforms in steady state: q_1 , q_2 , q_2' , v_a , v_b , v_L and i_L .

2.4.3 Small-signal Model Verification

According to (2.27) and (2.28), for the two-input two-output converter prototype, 10 input to output transfer functions can be considered, one of which are illustrated in Figure 2.9 as an example. The considered transfer function, $H_{11}^{d}(s)$, is analytically derived in (2.30) and (2.31), and plotted in Figure 2.9. Measurement and simulation data are also incorporated in Figure 2.9 to verify the analytical derivations. Numerical simulations are conducted using SIMULINK in MATLAB [28].

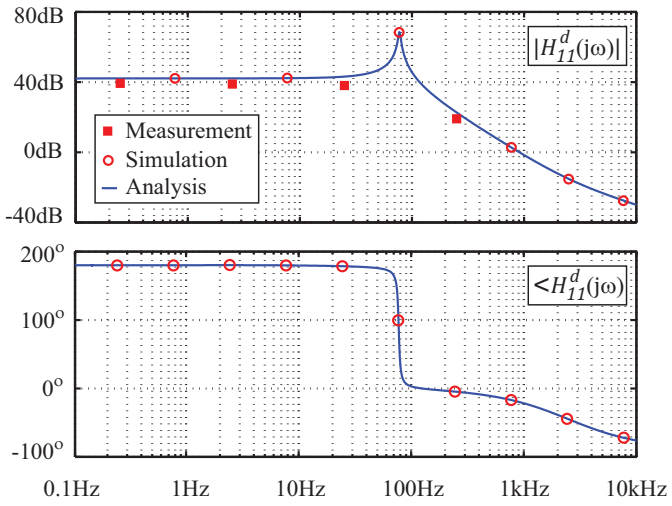

Figure 2.9 The input-to-output transfer function $H_{d}^{11}(s)$.

2.4.4 Controller Performance

Employing the proposed control scheme in section 2.3, the converter is able to regulate the output voltages, $v_{o,1}$ and $v_{o,2}$, as well as the first input power, $p_{in,1}$. The second input power, $p_{in,2}$ is relaxed to enable proper output voltages regulation, according to (2.32). It should be noted that the controller coefficients are not tuned for optimal performance since optimal controller design is not within the scope of this dissertation. However, the designed controller shows good dynamic performance; Using the given controller coefficient, all eigenvalues of the resulting closed-loop state matrix will be located on the left side of the complex plane, i.e., the closed-loop system is stable.

Besides, the integrator term in the control rule, $\mathbf{K}_i/s$, ensures zero steady-state error, which means all output voltages and input power will be regulated at the desired levels in steady-states.

2.4.4.1 Line Regulation

Figure 2.10 illustrates the measured line-regulation performance of the converter. The output voltages and the first input power, $v_{o,1}$, $v_{o,2}$, and $p_{in,1}$, are set at 22V, 11V, and 35W, respectively. As seen in Figure 2.10, once the step change in the first input voltage, $v_{in,1}$, occurs, the controller adjusts the input and output duty cycles to decrease the average current coming from the first input, $\langle i_{in,1} \rangle$, in order to keep $p_{in,1}$ at the desired setpoint ($p_{in,1} = 35$W). Moreover, the output voltages regulation is also achieved at the same time.

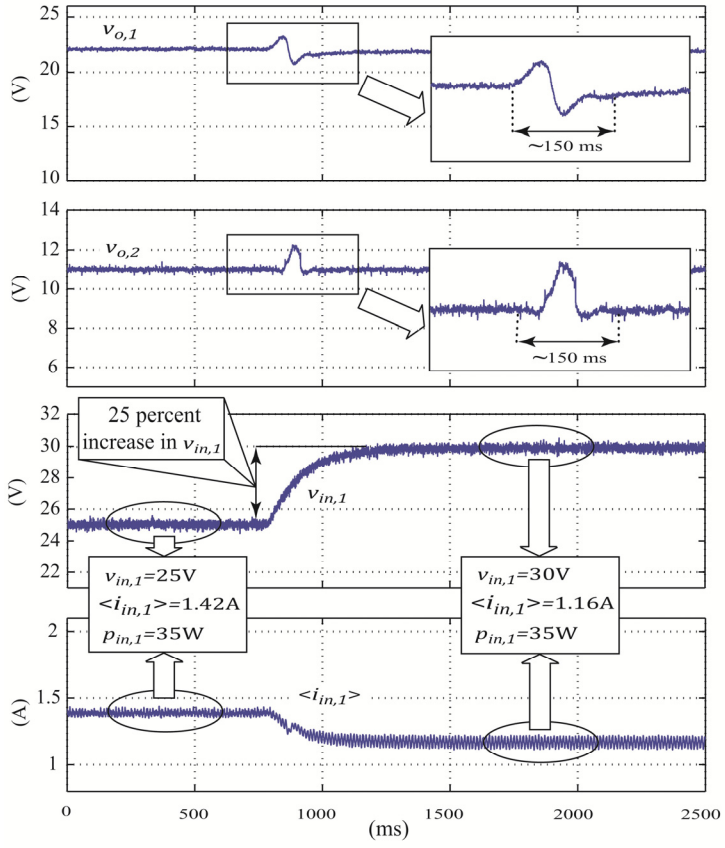

Figure 2.10 The measured line-regulation performance of the converter (25% increase in $v_{in,1}$).

2.4.4.2 Load Regulation

Figure 2.11 depicts the measured load-regulation performance of the converter prototype. A 230% step change in the first output load, $i_{o,1}$, is applied at the marked instance in Figure 2.11. Since the first input voltage, $v_{in,1}$, does not vary, regulation of the first input power, $p_{in,1}$, is equivalent to keeping $\langle i_{in,1} \rangle$ at the constant level. As shown in Figure 2.11, the controller adjusts the input and output duty cycles to keep $\langle i_{in,1} \rangle$ at the constant level ($\langle i_{in,1} \rangle = 1.4\text{A}$) and consequently, regulate the first input power, $p_{in,1}$. The output voltages, $v_{o,1}$ and $v_{o,2}$, are also properly regulated as seen in Figure 2.11.

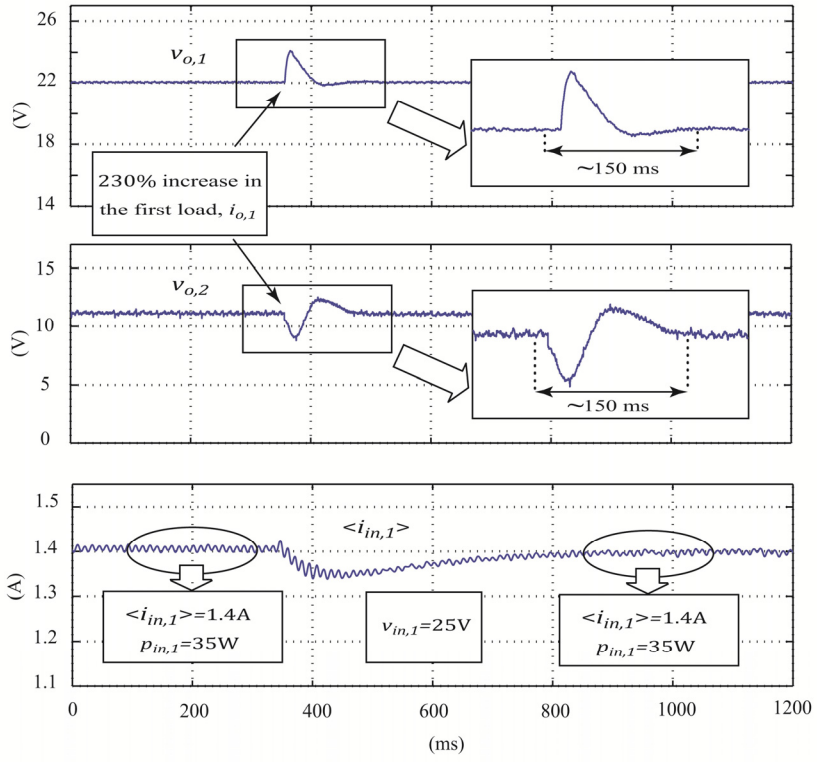

Figure 2.11 The measured load-regulation performance of the converter (230% increase in $i_{o,1}$).

The next chapter proposes another type of MIMO dc-dc converter with series outputs.

CHAPTER 3

MULTIPORT DC-DC CONVERTER WITH SERIES OUTPUTS

Single-stage multiport converters, as discussed in chapter 2, can be categorized into MISO, SIMO, and MIMO topologies. MISO converters have been well established in the literature. Early MISO converters were constructed by connecting the input voltage sources in series to obtain a multiple-input topology [29]. In such configurations, if one input source is diminished, the output voltage regulation will be challenging. An alternative approach is to put the input voltage sources in parallel with the input port of a SISO converter [7]. To prevent the input voltage sources from being shorted together, an active switch must be connected in series with each input source. Thus, only one input source can transfer energy to the load at a time. The operation of this family of MISO converters is based on time-multiplexing scheme [25]. Such scheme has been applied to buck, boost [3], buck-boost [5, 6], H-bridge [8, 9], flyback and forward [11, 12] converters and the resulting MISO converters have been studied. On the other hand, a number of MISO converter are able to transfer power to the load simultaneously [4, 10, 30], thus overcoming the shortcoming of time-multiplexing scheme. Assumptions, restrictions, and conditions for expanding SISO converters to their MISO versions are studied in [13] and systematic approaches to synthesize MISO converter are presented in [14].

SIMO converters can be categorized into isolated and non-isolated configurations. In isolated topologies, a transformer with multiple secondary windings interfaces between the input and output ports. Only one output voltage (usually the one with the heaviest load) is regulated while the others are determined by the turn ratios of the secondary windings. Hence, independent output voltage regulation is not straightforward [15]. The non-isolated SIMO topologies can be further categorized into independent- and series-output configurations. In independent-output configuration [16, 17], all output ports share the same ground whereas in series-output configuration [18, 19], different outputs are constructed in a series fashion. Series-output SIMO converters are suggested as efficient solutions to balance the dc-link voltages of diode-clamped multilevel inverters [20].

To date, MIMO converters have not received as much attention as MISO or SIMO converters. They are potentially able to combine the advantages of both MISO and SIMO topologies and provide a more cost-effective solution. A MIMO converter is proposed in [21] for energy harvesting applications (e.g. wireless sensor networks). This converter is designed to operate in DCM, which limits the maximum inductor current and inhibits the high power operation of such converter. Another MIMO power charger-supply is proposed in [22], whereby a fuel-cell and a Li-ion battery power a passive load. The Li-ion battery is considered as both load and source since it can be charged or discharged, respectively. However, only one output voltage can be regulated and this converter cannot supply more than one passive load.

In this chapter, a MIMO dc-dc converter topology with series outputs is proposed. The salient features of the proposed topology are as follows.

- An arbitrary number of inputs dc sources and passive loads can be accommodated.
- It can operate in both CCM and DCM.
- The input powers delivered by different dc sources can be individually regulated; thus, power budgeting between input energy sources can be accommodated.
- It only employs a single inductor, which can reduce complexity and cost of the system as well as simplifying the current sensing [6]. By sensing the inductor current and monitoring the switching signals of the switches, the input and output currents can be determined without employing additional current sensing circuitry.
- The output voltages can be, individually, higher than the maximum input voltage or lower than the minimum input voltage.

The rest of this chapter is organized as follows. Section 3.1 presents the converter topology and its operational principle. The steady-state operation of the converter is analyzed in section 3.2. Dynamic characterization and subsequent controller design are performed in sections 3.3 and 3.4, respectively. Section 3.5 presents loss and efficiency modeling. Sensitivity analysis studies are presented in section

3.6. Section 3.7 includes several case studies to verify the analytical characterizations and evaluate the performance of the converter.

3.1 Converter Topology and Operation Principles

The schematic of the proposed converter is illustrated in Figure 3.1. The input and output switches are denoted by $S_1, \dots, S_{m+1}$ and $S_1', \dots, S_{n+1}'$, respectively. All switches are FCBB except for S_1, S_{m+1}, S_1', and S_{n+1}'. FCBB switches can be realized by a series connection of a MOSFET and a diode, as shown in Figure 3.1. They prevent parallel connection of the input voltage sources [3, 6], however, imply unidirectional power flow. Unidirectional dc-dc converters are of interest in applications with unidirectional energy sources (e.g. solar array, primary battery, and fuel cell) or loads.

The converter provides non-isolated output voltages that are constructed in a series fashion. Non-isolated converters are prevalent in multiport dc systems that allow common ground such as those in [1, 5]. In such systems, replacing a bulky multiple-winding transformer with a single inductor, which sacrifices isolation, leads to significant reduction in complexity, size, and cost of the converter.

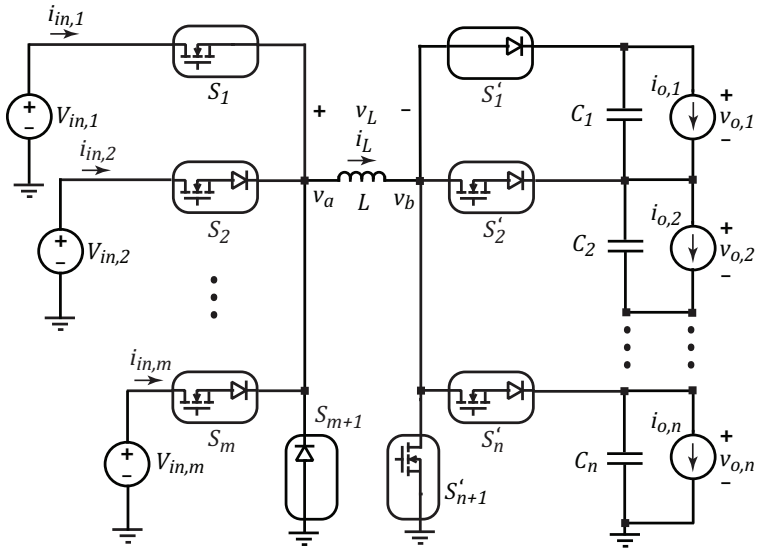

Figure 3.1 The proposed MIMO converter with series outputs.

The designated switching scheme for the converter is depicted in Figure 3.2. The gating signals of $S_1, \dots, S_{m+1}$ and $S'_1, \dots, S'_{n+1}$ are denoted by $q_1, \dots, q_{m+1}$ and $q'_1, \dots, q'_{n+1}$, respectively. The respective duty cycles are denoted by $d_1, \dots, d_{m+1}$ and $\alpha_1, \dots, \alpha_{n+1}$. Although S_{m+1} and S'_1 are uncontrollable (they are diodes), abstract gating signals, q_{m+1} and q'_1, are still considered for them to simplify the converter analysis. As expected, the duty cycles of these abstract gating signals are always one ($d_{m+1} = \alpha_1 = 1$). It should be noted that the proposed switching scheme requires the same gating signals for S_m and S'_{n+1} i.e. $d_m = \alpha_{n+1}$, as shown in Figure 3.2.

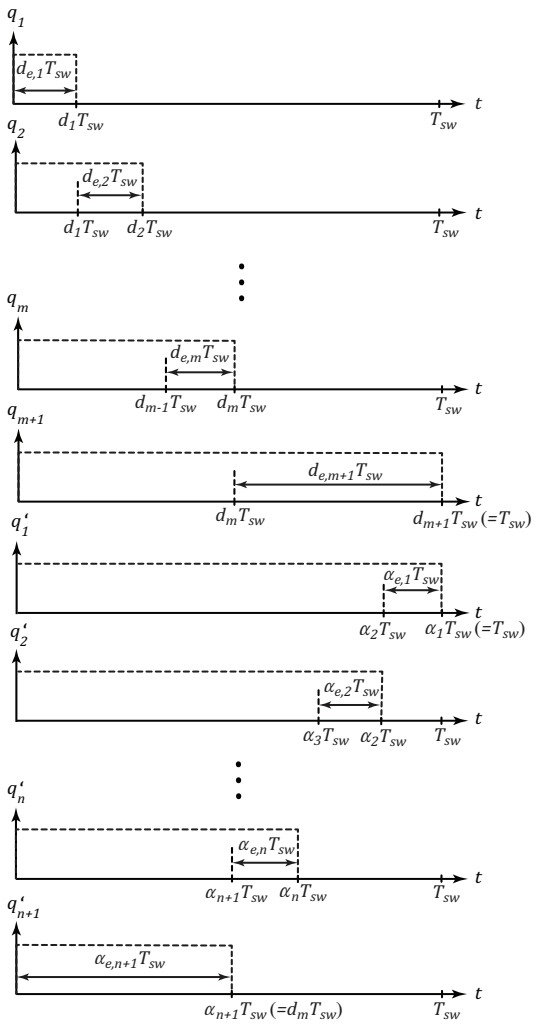

Figure 3.2 The switching scheme for the input and output switches.

Without loss of generality, the input voltage sources are arbitrarily arranged such that $V_{\text{in},1} > V_{\text{in},2} > \cdots > V_{\text{in},m}$. This arrangement simplifies the analysis of the converter operation as follows. If two or more input switches are commanded to turn on, only the one connected to the highest input voltage conducts and the rests are reverse-biased. Since the input voltages are arranged in a descending order, when gating signals overlap, the switch with the lower index conducts. This property of the converter enables defining the concept of effective duty cycles, similar to [3, 6, 7]. The effective duty cycle of the k^{th} input switch, $d_{e,k}$, can be defined as the portion of the switching period that S_k conducts, which is not necessarily the same as its commanded duty cycle, d_k. A similar discussion is applied to the output duty cycles. The effective input and output duty cycles, $d_{e,k}$ and $\alpha_{e,k}$, are depicted in Figure 3.2. They can be expressed in terms of their corresponding commanded duty cycles, d_i and α_j as follows.

$$d_{e,i} = \begin{cases} 0 & ,d_i < d_{i-1} \\ d_i - d_{i-1} & ,d_i \geq d_{i-1} \end{cases}, \qquad i = 2, \cdots, m+1, \tag{3.1}$$

$$\alpha_{e,j} = \begin{cases} 0 & ,\alpha_j < \alpha_{j+1} \\ \alpha_j - \alpha_{j+1} & ,\alpha_j \geq \alpha_{j+1} \end{cases}, \qquad j = 1, \cdots, n. \tag{3.2}$$

where $d_{e,1} = d_1$ and $\alpha_{e,n+1} = \alpha_{n+1}$. Alternatively, the commanded duty cycles, d_i and α_j, can be constructed from a given set of effective duty cycles, $d_{e,i}$ and $\alpha_{e,j}$, to be used by the modulation circuitry:

$$d_i = \sum_{k=1}^{i} d_{e,k}, \qquad i = 1, \cdots, m+1, \tag{3.3}$$

$$\alpha_j = \sum_{k=j}^{n+1} \alpha_{e,k}, \qquad j = 1, \ldots, n+1. \tag{3.4}$$

The sequential switching states of the converter are illustrated in Figure 3.3. In the first m switching states, $V_{\text{in},1}, \ldots, V_{\text{in},m}$ charge the inductor, sequentially. Then, S_m and S'_{n+1} turn off and the inductor current flows through S_{m+1} and S'_n. Thus, the last output capacitor, C_n, starts charging and the inductor current starts decreasing. Likewise, other output capacitors, $C_{n-1}, \ldots, C_1$, are charged sequentially in the next switching states. The sequential operation of the converter is based on time multiplexing

method, which has been widely used in MISO and SIMO converters [6, 18]. One of the inherent shortcomings of this method is pulsating input currents, which can be justified by the compactness of the converter when compared with multi-converter topologies [14]. Moreover, additional current filtering can be used for those inputs that cannot tolerate pulsating currents.

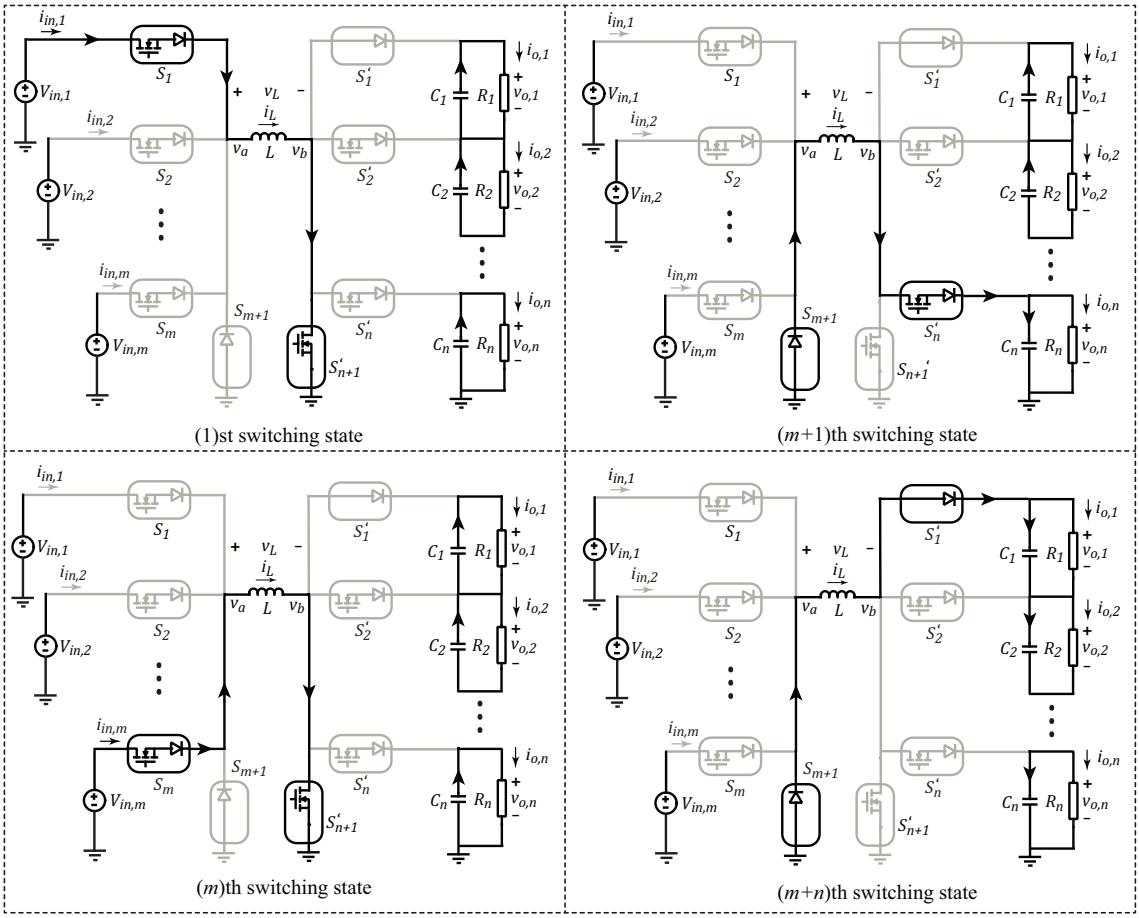

Figure 3.3 The sequential switching states of the converter.

3.2 Steady-state Characterization

In the following derivations, capital letters denote the average-values whereas the lowercase letters denote the instantaneous values.

3.2.1 CCM

3.2.1.1 Average Output Voltages and Inductor Current

Inductor volt-second balance principle implies that the average inductor voltage over a switching interval, V_L, is zero, in steady state. Assuming an ideal converter, the inductor volt-second balance in CCM can be written as

$$V_L = \sum_{i=1}^{m}\left(D_{e,i}V_{in,i}\right) - \sum_{j=1}^{n}\left(A_{e,j}\sum_{k=j}^{n}V_{o,k}\right) = 0. \tag{3.5}$$

Moreover, capacitor charge-balance principle implies that

$$A_{e,j}I_L = \begin{cases} \dfrac{V_{o,1}}{R_1} & , j = 1 \\ \dfrac{V_{o,j}}{R_j} - \dfrac{V_{o,j-1}}{R_{j-1}} & , j = 2,\cdots,n \end{cases}. \tag{3.6}$$

The derivations in (3.5) and (3.6) form a set of $n+1$ equations that can be explicitly solved for the average inductor current, I_L, and average output voltages, $V_{o,1}, \ldots, V_{o,n}$:

$$I_L = \frac{\sum_{i=1}^{m}V_{in,i}D_{e,i}}{\sum_{j=1}^{n}R_j\left(\sum_{k=1}^{j}A_{e,k}\right)^2}, \tag{3.7}$$

$$V_{o,j} = \frac{\left(\sum_{k=1}^{j}A_{e,k}\right)\left(\sum_{i=1}^{m}V_{in,i}D_{e,i}\right)}{\sum_{k=1}^{n}n_{k,j}\left(\sum_{l=1}^{k}A_{e,l}\right)^2}, \quad j = 1,\cdots,n. \tag{3.8}$$

where $n_{k,j}$ is defined as

$$n_{k,j} = \frac{R_k}{R_j}. \tag{3.9}$$

According to (3.8), the output voltages, $V_{o,j}$, depend on the ratio of the loads, $n_{k,j}$. The load dependency of the output voltages is common in SIMO converters [18, 19]. The controller, however, regulates the output voltages and compensates for the load dependency in such converters.

To obtain a desired operating point, the steady-state values of effective input and output duty cycles, $D_{e,i}$ and $A_{e,j}$, must satisfy the output voltage equations in (3.8). Since (3.8) dictates n number of constraints but $m+n$ number of variables are to be determined, $D_{e,1}, \dots, D_{e,m}$, $A_{e,1}, \dots, A_{e,n}$, designer has m degree of freedom. This freedom in determining the duty cycles can be used to regulate the input powers in addition to the output voltages, as will be discussed in section 3.4.

3.2.1.2 Ripple Analysis

The inductor current profile has a piecewise linear shape (assuming that the switching frequency, f_{sw}, is much faster than the inductor dynamics). Thus, the inductor current ripple for an ideal converter can be expressed as

$$\left|\Delta i_L\right| = \frac{1}{L f_{sw}} \sum_{i=1}^{m} V_{in,i} D_{e,i}. \tag{3.10}$$

According to (3.10), to obtain a inductor current ripple that is less than a desired maximum value, $|\Delta i_{\mathrm{L}}|_{\max}$, L should satisfy the following inequality:

$$L \geq \frac{1}{\left|\Delta i_L\right|_{\max} f_{sw}} \sum_{i=1}^{m} V_{in,i} D_{e,i}. \tag{3.11}$$

The discharging subinterval of the j^{th} output capacitor, $\left(A_{e,j+1} + \cdots + A_{e,n+1}\right)T_{sw}$, can be considered to find the output voltages ripples for an ideal converter:

$$\left|\Delta v_{o,j}\right| = \frac{\left(\sum_{k=1}^{j} A_{e,k}\right)\left(\sum_{k=j+1}^{n+1} A_{e,k}\right)\left(\sum_{i=1}^{m} V_{in,i} D_{e,i}\right)}{\left(C_j f_{sw}\right)\sum_{k=1}^{n} R_k \left(\sum_{l=1}^{k} A_{e,l}\right)^2}, j = 1,\ldots,n. \tag{3.12}$$

Thus, in order to obtain small enough output voltage ripples, $\left|\Delta v_{o,j}\right|_{\max}$, the output capacitors should satisfy the following inequalities:

$$C_j \geq \frac{\left(\sum_{k=1}^{j} A_{e,k}\right)\left(\sum_{k=j+1}^{n+1} A_{e,k}\right)\left(\sum_{i=1}^{m} V_{in,i} D_{e,i}\right)}{\left|\Delta v_{o,j}\right|_{\max} f_{sw}\sum_{k=1}^{n} R_k \left(\sum_{l=1}^{k} A_{e,l}\right)^2}, \quad j = 1,\cdots,n. \tag{3.13}$$

3.2.2 DCM

3.2.2.1 Definition of h-th DCM Mode

For an m-input n-output converter, n distinct DCM modes can be identified. As an example, a three-input two-output converter in the second DCM mode is considered. A sample inductor voltage and current profiles for this converter are illustrated in Figure 3.4. The input voltages, $V_{\text{in},1}$, $V_{\text{in},2}$, and $V_{\text{in},3}$, are applied to the inductor in subsequent charging intervals, $D_{e,1}T_{sw}$, $D_{e,2}T_{sw}$, and $D_{e,3}T_{sw}$, and cause the inductor current to increase piecewise linearly. Then, in the first discharging subinterval ($A_{e,2}T_{sw}$), $-V_{\text{o},2}$ is applied to the inductor and reduces the inductor current to $i_{p,4}$. In the second discharging subinterval ($A_{e,1}T_{sw}$), $-\left(V_{\text{o},1} + V_{\text{o},2}\right)$ is applied to the inductor and reduces the inductor current to zero at t_f. Since the inductor current reaches zero in the second discharging subinterval, this converter is defined to be operating in the second DCM mode.

In general, for an m-input n-output converter, n discharging subintervals exist, $A_{e,n}T_{sw}, \ldots, A_{e,1}T_{sw}$. The converter is defined to be operating in the h^{th} DCM mode if the inductor current becomes zero in the h^{th} discharging subinterval, $A_{e,n-h+1}T_{sw}$.

It should be noted that for a converter operating in the h^{th} DCM mode, the effective duty cycle of the last conducting switch, S'_{n-h+1}, is no longer $A_{e,n-h+1}$. This is because S'_{n-h+1} does not conduct current for the whole duration of $A_{e,n-h+1}T_{sw}$. For instance, in the converter considered in Figure 3.4, S'_1 does not conduct the current for the whole duration of $A_{e,1}T_{sw}$. Therefore, the actual effective duty cycle of the last conducting switch, $A'_{e,n-h+1}$, is always less than or equal to $A_{e,n-h+1}$. This new effective duty cycle, $A'_{e,n-h+1}$, is determined by the inductor volt-second balance:

$$A'_{e,n-h+1} = \frac{\sum_{i=1}^{m} V_{in,i} D_{e,i} - \sum_{j=n-h+2}^{n} A_{e,j} \left(\sum_{k=j}^{n} V_{o,k} \right)}{\sum_{j=n-h+1}^{n} V_{o,j}}. \tag{3.14}$$

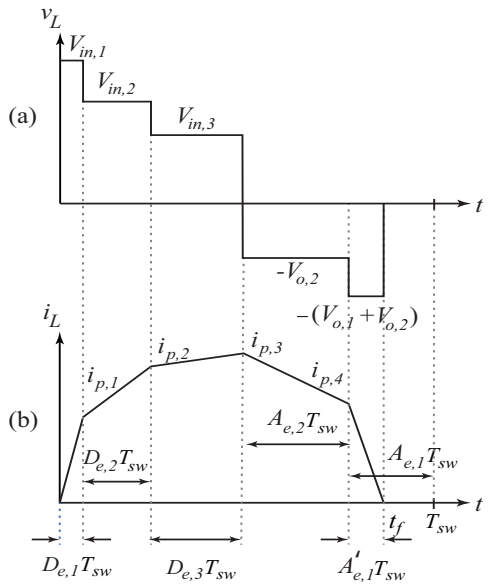

Figure 3.4 A three-input two-output converter operating in the second DCM mode: (a) inductor voltage, v_L, and (b) inductor current, i_L.

3.2.2.2 Determining the DCM Mode

An m-input n-output converter is operating in boundary condition between CCM and DCM if

$$A'_{e,1} = A_{e,1}. \tag{3.15}$$

Moreover, the boundary condition between h^{th} and $(h+1)^{\text{th}}$ DCM modes, can be characterized as

$$A'_{e,n-h+1} = A_{e,n-h+1}. \tag{3.16}$$

It should be noted that considering $h = n$ in (3.16), gives the same result as (3.15); thus, CCM can be treated as the $(n+1)$th DCM mode when determining the operating mode of the converter.

3.2.2.3 Average Output Voltages and Inductor Current

In DCM, the inductor current after k^{th} subinterval, $i_{p,k}$, can be expressed as

$$i_{p,k} = \begin{cases} i_{p,k-1} + \dfrac{V_{in,k} D_{e,k}}{L f_{sw}}, & ,k = 1,2,...,m \\ i_{p,k-1} - \dfrac{\sum_{j=n+m-k+1}^{n} V_{o,j}}{L f_{sw}} A_{e,n+m-k+1} & ,k = m+1,...,m+h-1 \end{cases} \tag{3.17}$$

where $i_{p,0} = 0$. The average inductor current, I_L, can be expressed in terms of $i_{p,k}$'s as

$$I_L = \sum_{k=1}^{m} \frac{i_{p,k-1} + i_{p,k}}{2} D_{e,k} + \sum_{k=m+1}^{m+h-1} \frac{i_{p,k-1} + i_{p,k}}{2} A_{e,n+m-k+1} + \frac{i_{p,m+h-1}}{2} A'_{e,n-h+1} \tag{3.18}$$

in the h^{th} DCM mode. The average output voltages, $V_{o,1}, \ldots, V_{o,n}$, can also be found in terms of $i_{p,k}$'s as

$$V_{o,j} = \begin{cases} 0 & j = 1,\cdots,n-h \\ A'_{e,j} \dfrac{i_{p,m+n-j}}{2} & j = n-h+1 \\ A_{e,j} \dfrac{i_{p,m+n-j} + i_{p,m+n-j+1}}{2} & j = n-h+2,\cdots,n \end{cases}. \tag{3.19}$$

It should be noted only h output ports have nonzero voltage in the h^{th} DCM mode i.e. $V_{o,1} = V_{o,2} = \cdots = V_{o,n-h} = 0$, as stated in (3.19).

For a two-input two-output converter, (3.17)-(3.19) can be explicitly solved to find the output voltages in terms of input voltages and effective duty cycles. The explicit solution of (3.17)-(3.19) for a two-input two-output converter are given in (3.20) and (3.21) to be used in section 3.7.

$$V_{o,1} = \frac{\left(k_2 + \frac{A_{e,2}^2}{2}\right)V_{o,2} - A_{e,2}\sum_{i=1}^{2} D_{e,i}V_{in,i}}{k_1} \tag{3.20}$$

$$V_{o,2} = \frac{2A_{e,2}(A_{e,2}^2 + 2k_2) + \sqrt{8k_1k_2(k_1 + k_2 - A_{e,2}^2) + 2k_1A_{e,2}^4}}{(A_{e,2}^2 + 2k_2)^2 + 4k_1k_2}\sum_{i=1}^{2} D_{e,i}V_{in,i} \tag{3.21}$$

The term k_i in (3.20) and (3.21) is defined as

$$k_j = L/(R_jT_{sw}). \tag{3.22}$$

3.2.2.4 Ripple Analysis

The inductor current ripple in DCM is the same as its peak value, $i_{p,m}$:

$$\left|\Delta i_L\right| = i_{p,m} = \frac{1}{Lf_{sw}}\sum_{i=1}^{m} D_{e,i}V_{in,i}. \tag{3.23}$$

The output voltage ripples in DCM can be found by considering the discharging subintervals of the output capacitors as follows:

$$|\Delta v_{o,j}| = \begin{cases} 0 & , j = 1,\ldots,\ n-h \\ \frac{1}{C_jf_{sw}}\left(\frac{V_{o,j}}{R_j}\right)\left(\sum_{k=j+1}^{n+1} A_{e,k}\right) & , j = n-h+1,\ldots,\ n \end{cases}. \tag{3.24}$$

3.3 Dynamic Characterization

Dynamic characterization of the converter is essential for controller design and stability assessment. Several dynamic characterization methods have been well established in the literature for the power electronic converters, among which SSA is a well-known technique [26]. The SSA model of a two-input, two-output MIMO converter is developed in this section. This model can easily be extended to the general case where a *m*-input *n*-output converter is considered.

3.3.1 Average Value Model

SSA is based on the state-space description of the converter in each switching subinterval. In order to determine the state-space description, the input, $\mathbf{u}(t)$, output, $\mathbf{y}(t)$, and state, $\mathbf{x}(t)$, vectors are defined as:

$$\mathbf{x}(t)=\begin{bmatrix} v_{C_1} \\ v_{C_2} \\ i_L \end{bmatrix}, \quad \mathbf{u}(t)=\begin{bmatrix} v_{in,1} \\ v_{in,2} \end{bmatrix}, \quad \mathbf{y}(t)=\begin{bmatrix} i_{in,1} \\ i_{in,2} \end{bmatrix}. \tag{3.25}$$

Here, the input currents, $i_{in,1}$ and $i_{in,1}$, are chosen as the output variables to simplify small-signal model development. Once the small-signal equivalent circuit is developed, the transfer function from any input to any output can be easily extracted.

By inspecting the converter topology, one can find the following state-space-description, which represents all switching subintervals in a compact form:

$$\begin{cases} C_1 \dfrac{dv_{C_1}}{dt} = -\dfrac{v_{C_1}}{R_1} + (q_1' - q_2')i_L \\ C_2 \dfrac{dv_{C_2}}{dt} = -\dfrac{v_{C_2}}{R_2} + (q_1' - q_3')i_L \\ L\dfrac{di_L}{dt} = q_1 v_{in,1} + (q_2 - q_1)v_{in,2} - (q_1' - q_2')v_{C_1} - (q_1' - q_3')v_{C_2} \\ i_{in,1} = q_1 i_L \\ i_{in,2} = (q_2 - q_1)i_L \end{cases} \tag{3.26}$$

The switching functions of input and output switches, q_i and q'_j, are illustrated in Figure 3.2. The state-space description given in (3.26) is time variant because it includes the switching functions, q_i and q'_j. It can be converted to a time-invariant model by applying SSA. The average of a signal, $x(t)$, over the switching period, T_s, is defined as

$$\langle x \rangle_{T_s}(t) = \frac{1}{T_s}\int_t^{t+T_s} x(t)dt. \tag{3.27}$$

SSA states that the average of the product of a switching function, e.g. $q(t)$, and a converter's variable, e.g. $x(t)$, can be approximated by the product of their averages, i.e.

$$\langle q(t)x(t)\rangle_{T_s} = \langle q(t)\rangle_{T_s}\langle x(t)\rangle_{T_s} = d(t)\langle x(t)\rangle_{T_s} \tag{3.28}$$

where $d(t)$ is the duty cycle of $q(t)$. Applying SSA to (3.26) yields to (3.29). The model described by (3.29) is time invariant, yet, nonlinear since it includes multiplication of different signals (e.g. $\alpha_{e,1}$ and $\langle i_L \rangle_{T_s}$). To obtain a linear time invariant model, (3.29) should be linearized around a specific equilibrium point.

$$\begin{cases} C_1 \dfrac{d\langle v_{C_1}\rangle_{T_s}}{dt} = -\dfrac{\langle v_{C_1}\rangle_{T_s}}{R_1} + \alpha_{e,1}\langle i_L\rangle_{T_s} \\ C_2 \dfrac{d\langle v_{C_2}\rangle_{T_s}}{dt} = -\dfrac{\langle v_{C_2}\rangle_{T_s}}{R_2} + (\alpha_{e,1}+\alpha_{e,2})\langle i_L\rangle_{T_s} \\ L\dfrac{d\langle i_L\rangle_{T_s}}{dt} = d_{e,1}\langle v_{in,1}\rangle_{T_s} + d_{e,2}\langle v_{in,2}\rangle_{T_s} - \alpha_{e,1}\langle v_{C_1}\rangle_{T_s} - (\alpha_{e,1}+\alpha_{e,2})\langle v_{C_2}\rangle_{T_s} \\ \langle i_{in,1}\rangle_{T_s} = d_{e,1}\langle i_L\rangle_{T_s} \\ \langle i_{in,2}\rangle_{T_s} = d_{e,2}\langle i_L\rangle_{T_s} \end{cases} . \tag{3.29}$$

3.3.2 Equilibrium Point

The equilibrium point of the converter can be determined by equating the derivative terms of (3.29) to zero. Eliminating the derivative terms yields a set of algebraic equations that can be solved to find V_{C_1}, V_{C_2}, I_L, $I_{in,1}$ and $I_{in,2}$. The equilibrium point values of V_{C_1}, V_{C_2},and I_L are, in fact, the same as the

steady-state values calculated in (3.7) and (3.8); they are not repeated here for brevity. The equilibrium point values of $I_{in,1}$ and $I_{in,2}$ are

$$\begin{bmatrix} I_{in,1} \\ I_{in,2} \end{bmatrix} = \begin{bmatrix} \dfrac{D_{e,1}(V_{in,1}D_{e,1} + V_{in,2}D_{e,2})}{R_1 A_{e,1}^2 + R_2 (A_{e,1} + A_{e,2})^2} \\ \dfrac{D_{e,2}(V_{in,1}D_{e,1} + V_{in,2}D_{e,2})}{R_1 A_{e,1}^2 + R_2 (A_{e,1} + A_{e,2})^2} \end{bmatrix}. \tag{3.30}$$

3.3.3 Linearization and Small-signal Modeling

The average model described in (3.29) can be linearized considering small perturbations around the equilibrium point represented by (3.31). In general, all average variables ($\langle v_{C_1} \rangle$, $\langle v_{C_2} \rangle$, $\langle i_L \rangle$, etc.) can be expressed as

$$\langle x \rangle_{T_s} = X + \hat{x} \tag{3.31}$$

where X and $\hat{x}$ denote the equilibrium value and perturbation of the signal $\langle x \rangle_{T_s}$. Similarly, some perturbations can be applied around the equilibrium values of input and output duty cycles as follows

$$\begin{cases} d_{e,i} = D_{e,i} + \hat{d}_{e,i} \\ \alpha_{e,j} = A_{e,j} + \hat{\alpha}_{e,j} \end{cases} \tag{3.32}$$

where $\hat{d}_{e,i}$ and $\hat{\alpha}_{e,j}$ denote the perturbations around $D_{e,i}$ and $A_{e,j}$, respectively.

Considering the discussed perturbations, one can linearize (3.29) as follows.

$$\begin{bmatrix} C_1 & 0 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \hat{v}_{C_1} \\ \hat{v}_{C_2} \\ \hat{i}_L \end{bmatrix} = \begin{bmatrix} \frac{-1}{R_1} & 0 & A_{e,1} \\ 0 & \frac{-1}{R_2} & A_{e,1} + A_{e,2} \\ -A_{e,1} & -A_{e,1} - A_{e,2} & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{C_1} \\ \hat{v}_{C_2} \\ \hat{i}_L \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ D_{e,1} & D_{e,2} \end{bmatrix} \begin{bmatrix} \hat{v}_{in,1} \\ \hat{v}_{in,2} \end{bmatrix} +$$

$$\begin{bmatrix} -I_L \\ -I_L \\ V_{in,1} + V_{C_1} + V_{C_2} \end{bmatrix} \hat{d}_{e,1} + \begin{bmatrix} -I_L \\ -I_L \\ V_{in,2} + V_{C_1} + V_{C_2} \end{bmatrix} \hat{d}_{e,2} + \begin{bmatrix} -I_L \\ 0 \\ V_{C_1} \end{bmatrix} \hat{\alpha}_{e,2} \tag{3.33}$$

$$\begin{bmatrix} \hat{i}_{in,1} \\ \hat{i}_{in,2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & D_{e,1} \\ 0 & 0 & D_{e,2} \end{bmatrix} \begin{bmatrix} \hat{v}_{C_1} \\ \hat{v}_{C_2} \\ \hat{i}_L \end{bmatrix} + I_L \begin{bmatrix} \hat{d}_{e,1} \\ \hat{d}_{e,2} \end{bmatrix}$$

3.3.4 Equivalent Small-signal Circuit

An equivalent small-signal circuit can be developed to represent the dynamic behavior of the converter and extract the transfer functions from any arbitrary input (e.g. duty cycles) to any arbitrary output (e.g. output voltages). This small-signal circuit is based on the linearized SSA model given in (3.33). Each row of the differential-algebraic equations in (3.33) corresponds to an equivalent subcircuit. Figure 3.5 illustrates these equivalent subcircuits. The first and second rows of the algebraic equations in (3.33), pertaining to $\hat{\imath}_{in,1}$ and $\hat{\imath}_{in,2}$, correspond to the subcircuits shown in Figure 3.5(a and b), respectively. Likewise, the first, second, and third rows of the differential equations in (3.33), pertaining to $\hat{v}_{C_1}$, $\hat{v}_{C_2}$, and $\hat{\imath}_L$, correspond to the subcircuits depicted in Figure 3.5(c, d, and e), respectively.

In Figure 3.5, the independent voltage or current sources are shown in circles whereas the dependent sources are shown in squares. The dependent voltage and current sources can be combined together to obtain a lumped small-signal equivalent circuit, shown in Figure 3.6. As demonstrated by Figure 3.6, the MIMO converter operation is equivalent to a circuit comprising of multiple transformers with conversion ratios equal to the input and output effective duty cycles. Figure 3.6 can autonomously describe the dynamic behavior of the converter.

3.3.5 Input-to-output Transfer Functions

Three types of inputs can be recognized for the converter: input voltages, $v_{in,i}$, input duty cycles, $d_{e,i}$, and output duty cycles, $\alpha_{e,i}$. System outputs are defined as the output voltages (capacitor voltages). Figure 3.7 illustrates the input/output assignments. Therefore, three types of input-to-output transfer function can be identified, namely, input-voltage to output-voltage ($H_{ij}^{v}(s)$), input-duty-cycle to output-voltage ($H_{ij}^{d}(s)$), and output-duty-cycle to output voltage ($H_{ij}^{\alpha}(s)$) transfer functions.

The input-to-output transfer function can be found by inspecting the lumped equivalent small-signal circuit of the converter (Figure 3.6). Here, the transfer functions from the first input voltage to the second output voltage ($H_{12}^{v}(s)$), and from the first input duty cycle to the first output voltage $H_{11}^{d}(s)$ are calculated as an example:

$$\begin{cases} H_{12}^{v}(s) = \dfrac{\beta_1^{v12}s + \beta_0^{v12}}{\mu_3 s^3 + \mu_2 s^2 + \mu_1 s + \mu_0} \\ H_{11}^{d}(s) = \dfrac{\beta_2^{d11}s^2 + \beta_1^{d11}s + \beta_0^{d11}}{\mu_3 s^3 + \mu_2 s^2 + \mu_1 s + \mu_0} \end{cases} \tag{3.34}$$

where

$$\begin{cases} \mu_0 = R_1 A_{e,1}^2 + R_2 (A_{e,1} + A_{e,2})^2 \\ \mu_1 = L + R_1 R_2 \left(C_2 A_{e,1}^2 + C_1 (A_{e,1} + A_{e,2})^2 \right) \\ \mu_2 = (R_1 C_1 + R_2 C_2) L \\ \mu_3 = R_1 R_2 C_1 C_2 L \end{cases}$$

$$\begin{cases} \beta_0^{v12} = R_2 D_{e,1} (A_{e,1} + A_{e,2}) \\ \beta_1^{v12} = R_1 R_2 C_1 D_{e,1} (A_{e,1} + A_{e,2}) \end{cases} \tag{3.35}$$

$$\begin{cases} \beta_0^{d11} = R_1 A_{e,1} (V_{C_1} + V_{C_2} + V_{in,1}) - R_1 R_2 A_{e,2} (A_{e,1} + A_{e,2}) I_L \\ \beta_1^{d11} = R_1 R_2 C_2 A_{e,1} (V_{in,1} + V_{C_1} + V_{C_2}) - R_1 L I_L \\ \beta_2^{d11} = -R_1 R_2 C_2 L I_L \end{cases}$$

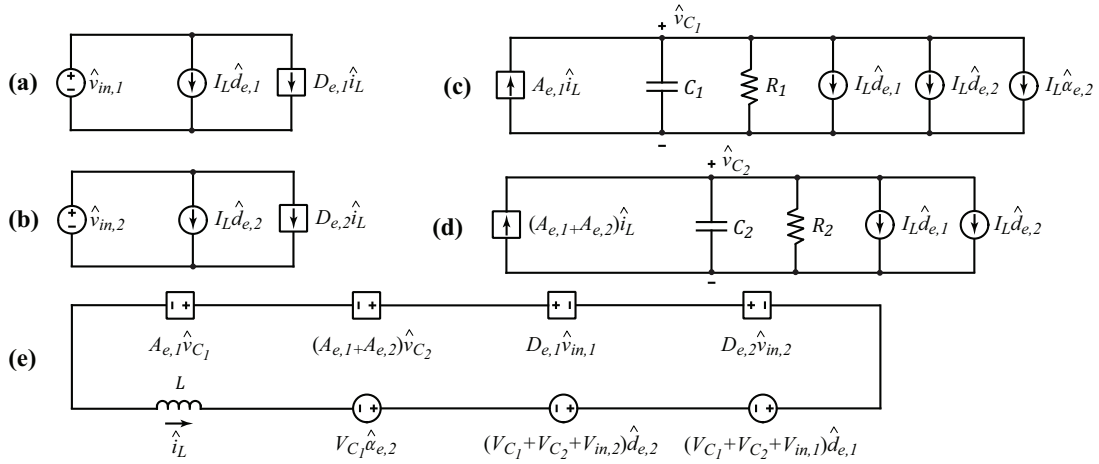

Figure 3.5 The equivalent small-signal subcircuits of the converter.

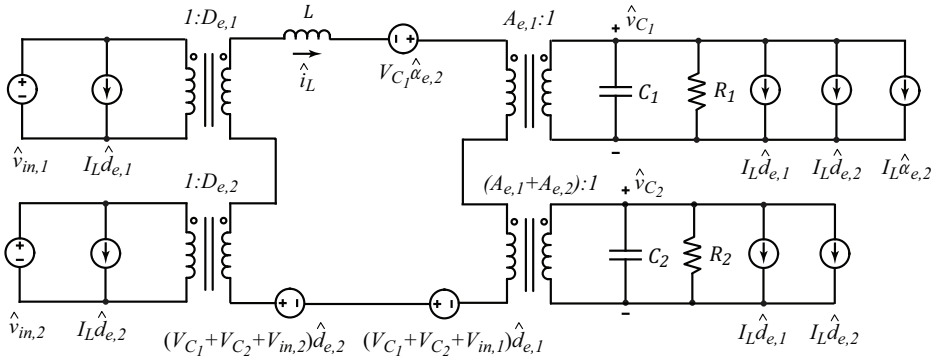

Figure 3.6 The lumped equivalent small-signal circuit of the converter.

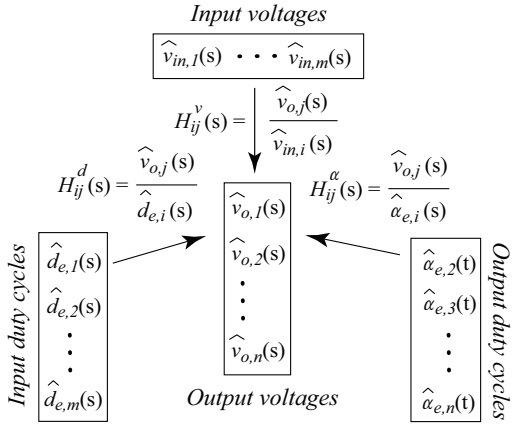

Figure 3.7 Definition of system inputs, outputs, and input-to-output transfer functions.

3.4 Controller Design

A m-input n-output MIMO converter has $m+n$ active switches. Thus, a controller must adjust $m+n$ duty cycles, $d_{e,1},\dots,d_{e,m},\alpha_{e,1},\dots,\alpha_{e,n}$, to regulate n output voltages and m input powers. Assuming an ideal converter, the conservation of power principle states that

$$\sum_{i=1}^{m} P_{in,i} = \sum_{j=1}^{n} \frac{V_{o,j}^2}{R_j}. \tag{3.36}$$

Equation (3.36) implies that one of the input powers should be relaxed in order to achieve proper regulation for output voltages. In other words, for a m-input n-output converter, with output voltage regulation, only $(m-1)$ input powers can be regulated.

In equilibrium (steady state), the input powers coming from each energy source can be expressed as

$$P_{in,i} = V_{in,i} I_{in,i} = \frac{V_{in,i} D_{e,i} \sum_{k=1}^{m} V_{in,k} D_{e,k}}{\sum_{j=1}^{n} R_j A_{e,j}^2}, \quad i = 1,\dots,m. \tag{3.37}$$

For proper output voltage and input power regulation, (3.8) and (3.37) should be satisfied in steady state. Therefore, the set of nonlinear algebraic equations formed by (3.8) and (3.37) can be simultaneously solved to determine the equilibrium values of input and output duty cycles, $D_{e,i}$ and $A_{e,j}$, respectively. Then, a MIMO controller can be designed around this equilibrium point.

For a two-input two-output converter considered in section 3.7, $p_{in,1}$, $v_{o,1}$, and $v_{o,2}$ are the designated output variables to be regulated. The average value of $p_{in,1}$ can be expressed as

$$\left\langle p_{in,1} \right\rangle_{T_s} = V_{in,1} d_{e,1} \left\langle i_L \right\rangle_{T_s}. \tag{3.38}$$

Thus, perturbations in $p_{in,1}$ can be expanded as

$$\hat{p}_{in,1} = V_{in,1} D_{e,1} \hat{i}_L + V_{in,1} I_L \hat{d}_{e,1}. \tag{3.39}$$

Considering the small-signal behavior of $p_{in,1}$ in (3.39), the dynamic model of the plant (converter) can be developed as follows.

$$\underbrace{\frac{d}{dt}\begin{bmatrix}\hat{i}_L\\ \hat{v}_{C_1}\\ \hat{v}_{C_2}\end{bmatrix}}_{\frac{d\mathbf{x}}{dt}} = \underbrace{\begin{bmatrix}0 & \frac{-A_{e,1}}{L} & \frac{-A_{e,1}-A_{e,2}}{L}\\ \frac{A_{e,1}}{C_1} & \frac{-1}{R_1C_1} & 0\\ \frac{A_{e,1}+A_{e,2}}{C_2} & 0 & \frac{-1}{R_2C_2}\end{bmatrix}}_{\mathbf{A}_{ol}} \underbrace{\begin{bmatrix}\hat{i}_L\\ \hat{v}_{C_1}\\ \hat{v}_{C_2}\end{bmatrix}}_{\mathbf{x}} + \underbrace{\begin{bmatrix}\frac{V_{C_1}+V_{C_2}+V_{in,1}}{L} & \frac{V_{C_1}+V_{C_2}+V_{in,1}}{L} & \frac{V_{C_1}}{L}\\ \frac{-I_L}{C_1} & \frac{-I_L}{C_1} & \frac{-I_L}{C_1}\\ \frac{-I_L}{C_2} & \frac{-I_L}{C_2} & 0\end{bmatrix}}_{\mathbf{B}_{ol}} \underbrace{\begin{bmatrix}\hat{d}_{e,1}(t)\\ \hat{d}_{e,2}(t)\\ \hat{\alpha}_{e,2}(t)\end{bmatrix}}_{\mathbf{u}} \tag{3.40}$$

$$\underbrace{\begin{bmatrix}\hat{p}_{in,1}\\ \hat{v}_{o,1}\\ \hat{v}_{o,2}\end{bmatrix}}_{\mathbf{y}} = \underbrace{\begin{bmatrix}V_{in,1}D_{e,1} & 0 & 0\\ 0 & 1 & 0\\ 0 & 0 & 1\end{bmatrix}}_{\mathbf{C}_{ol}} \underbrace{\begin{bmatrix}\hat{i}_L\\ \hat{v}_{C_1}\\ \hat{v}_{C_2}\end{bmatrix}}_{\mathbf{x}} + \underbrace{\begin{bmatrix}V_{in,1}I_L & 0 & 0\\ 0 & 0 & 0\\ 0 & 0 & 0\end{bmatrix}}_{\mathbf{D}_{ol}} \underbrace{\begin{bmatrix}\hat{d}_{e,1}\\ \hat{d}_{e,2}\\ \hat{\alpha}_{e,2}\end{bmatrix}}_{\mathbf{u}} \tag{3.41}$$

where $\mathbf{A}_{ol}$, $\mathbf{B}_{ol}$, $\mathbf{C}_{ol}$, and $\mathbf{D}_{ol}$ are the open-loop state, input, output, and feed through matrices, respectively. The state, input, and output vectors are denoted by **x**, **u**, and **y**, respectively.

3.4.1 Multi-variable Feedback Loop

A multi-variable PI controller is implemented here. In order to regulate the output vector, **y**, including $p_{in,1}$, $v_{o,1}$, and $v_{o,2}$, one strategy is to measure **y**, subtract it from a reference vector, **r**, and feed it through an integrator to ensure zero steady-state error. Figure 3.8 illustrates the proposed control scheme. The error vector is multiplied by a integrator-gain matrix, $\mathbf{K}_i$, to enable fine-tuning of the controller. A proportional term ($\mathbf{K}_p$) is also implemented to enhance the transient performance.

3.4.2 System Stability

To examine the stability of the resulting linear, time-invariant system, one can study the location of the system poles. All system poles must lie on the left side of the imaginary axis to achieve a stable system. The poles of the closed-loop system are eigen-values of the closed-loop state matrix, $\mathbf{A}_{cl}$. The

closed-loop state matrix, $\mathbf{A}_{cl}$, can be found by adding vector $\mathbf{v}$ (shown in Figure 3.8) to the state vector $\mathbf{x}$, and determining the state-space description of the new system. The dynamics of the closed-loop system is governed by

$$\begin{cases} \dfrac{d\mathbf{x}}{dt} = \mathbf{A}_{ol}\mathbf{x} + \mathbf{B}_{ol}\mathbf{u} \\ \mathbf{y} = \mathbf{C}_{ol}\mathbf{x} + \mathbf{D}_{ol}\mathbf{u} \\ \dfrac{d\mathbf{v}}{dt} = \mathbf{r} - \mathbf{y} \\ \mathbf{u} = \mathbf{K}_i\mathbf{v} + \mathbf{K}_p\dfrac{d\mathbf{v}}{dt} \end{cases}. \tag{3.42}$$

The closed-loop system matrix, $\mathbf{A}_{cl}$, can be derived by inspecting (3.42) as follows

$$\mathbf{A}_{cl} = \begin{bmatrix} \mathbf{A}_{ol} - \mathbf{B}_{ol}\mathbf{K}_p(\mathbf{I} + \mathbf{D}_{ol}\mathbf{K}_p)^{-1}\mathbf{C}_{ol} & \mathbf{B}_{ol}(\mathbf{I} - \mathbf{K}_p(\mathbf{I} + \mathbf{D}_{ol}\mathbf{K}_p)^{-1}\mathbf{D}_{ol})\mathbf{K}_i \\ -(\mathbf{I} + \mathbf{D}_{ol}\mathbf{K}_p)^{-1}\mathbf{C}_{ol} & -(\mathbf{I} + \mathbf{D}_{ol}\mathbf{K}_p)^{-1}\mathbf{D}_{ol}\mathbf{K}_i \end{bmatrix} \tag{3.43}$$

The closed-loop system is stable if and only if the eigen-values of $\mathbf{A}_{cl}$ lie on the left side of the imaginary axis, i.e.,

$$\begin{cases} \det(\lambda_i\mathbf{I} - \mathbf{A}_{cl}) = 0 \\ \forall\lambda_i : \quad \mathrm{Re}\{\lambda_i\} < 0 \end{cases} \quad ,i = 1, \cdots, N. \tag{3.44}$$

where N is the number of the eigen-values of $\mathbf{A}_{cl}$.

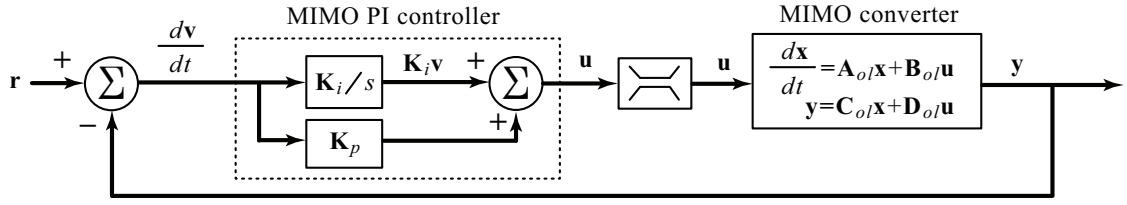

Figure 3.8 Closed-loop system block diagram.

3.5 Loss Modeling

3.5.1 Steady-state Operation

The parasitic elements of the converter components, including on-state input and output switches' resistances, $r_{on,i}$ and $r'_{on,j}$, on-state input and output switches' voltage-drops, $V_{on,i}$ and $V'_{on,j}$, and the inductor resistance, r_L, decrease the steady-state output voltages and inductor current. Considering the parasitic elements for (3.5) and (3.6), it can be shown that the steady-state inductor current, I_L, and output voltages, $V_{o,j}$, of a non-ideal converter are

$$I_L = \frac{V_{in,\text{eff}}}{r_{L,\text{eff}} + \sum_{j=1}^{n} R_j \left(\sum_{k=1}^{j} A_{e,k} \right)^2}, \tag{3.45}$$

and

$$V_{o,j} = \frac{\left(\sum_{k=1}^{j} A_{e,k} \right) V_{in,\text{eff}}}{\left(\frac{r_{L,\text{eff}}}{R_j} \right) + \sum_{k=1}^{n} n_{k,j} \left(\sum_{l=1}^{k} A_{e,l} \right)^2}, \quad j = 1, \cdots, n, \tag{3.46}$$

where

$$r_{L,\text{eff}} = r_L + \sum_{i=1}^{m+1} r_{on,i} D_{e,i} + \sum_{j=1}^{n+1} r'_{on,j} A_{e,j}, \tag{3.47}$$

and

$$V_{\text{in,eff}} = \sum_{i=1}^{m} V_{\text{in},i} D_{e,i} - \sum_{i=1}^{m+1} V_{on,i} D_{e,i} - \sum_{j=1}^{n+1} V'_{on,j} A_{e,j}. \tag{3.48}$$

It can be concluded from (3.47) that the on-state resistances of the input and output switches, $r_{\text{on},i}$ and $r'_{\text{on},j}$, can be reflected to the inductor side, if they are multiplied by the corresponding effective duty cycles, $D_{e,i}$ and $A_{e,j}$, respectively. Upon reflection, they can be lumped together with the inductor's resistance (3.47). The same conclusion applies to on-state voltage drops as demonstrated by (3.48).

3.5.2 Efficiency Analysis

The conduction losses and non-idealities of the converter components undermine the converter efficiency. The dominating converter losses are considered as follows.

$$P_{loss} = P_L + P_{S_i,cond} + P_{S_i,sw} + P_{S_i',cond} + P_{S_i',sw} \tag{3.49}$$

where P_L, $P_{S_i,cond}$, $P_{S_i',cond}$, $P_{S_i,sw}$, and $P_{S_i',sw}$ are inductor power loss, input and output switches' conduction loss, and input and output switching loss, respectively. All terms of (3.49), except for the switching losses, can be approximated using the inductor current in the steady state (3.45):

$$P_L = r_L I_L^2 \tag{3.50}$$

$$P_{S_i,cond} = I_L \sum_{i=1}^{m} (V_{on,i} D_{e,i}) + I_L^2 \sum_{i=1}^{m} (r_{on,i} D_{e,i}) \tag{3.51}$$

$$P_{S_i',cond} = I_L \sum_{j=1}^{n} (V'_{on,i} A_{e,j}) + I_L^2 \sum_{j=1}^{n} (V'_{on,i} A_{e,j}) \tag{3.52}$$

The switching losses should be determined by precisely measuring the voltage and current profiles of the switches in the implemented converter. The output powers, assuming ripple-free output voltages, can be approximated as

$$P_o = \frac{V_{o,1}^2}{R_1} + \cdots + \frac{V_{o,n}^2}{R_n}. \tag{3.53}$$

The converter's efficiency is

$$\eta = \frac{P_o}{P_o + P_{loss}}. \tag{3.54}$$

3.6 Sensitivity Analysis

Sensitivity of the output voltages with respect to the duty cycles, $D_{e,i}$ and $A_{e,i}$, and input voltages, $V_{in,i}$, determines how significant the effect of these variables on changing the equilibrium point

of the converter is. Sensitivity of variable y with respect to variable x is defined as the ratio of the percentage change in y (dependent variable) caused by that in x (independent variable), i.e.,

$$S_x^y = \frac{dy/y}{dx/x} = \frac{dy}{dx} \cdot \frac{x}{y} \tag{3.55}$$

Here, the sensitivity of output voltages to the variation in input voltage as well as input and output duty cycles are found.

3.6.1 Sensitivity to Input-voltage Variations

The sensitivity of output voltages to input voltages can be found using (3.55) and (3.8) as

$$S_{V_{in,i}}^{V_{o,j}} = \frac{dV_{o,j}}{dV_{in,i}} \cdot \frac{V_{in,i}}{V_{o,j}} = \frac{D_{e,i}V_{in,i}}{\sum_{k=1}^{m} V_{in,k}D_{e,k}}. \tag{3.56}$$

3.6.2 Sensitivity to Variations in Input Duty Cycles

The last effective output duty cycle, $A_{e,1}$, depends on other effective duty cycles since S_1 is not controllable, i.e.,

$$A_{e,1} = 1 - \sum_{k=1}^{m} D_{e,k} - \sum_{k=2}^{n} A_{e,k}. \tag{3.57}$$

Equation (3.57) implies that

$$\frac{\partial A_{e,1}}{\partial D_{e,i}} = -1 \qquad ,i = 1, \cdots, m. \tag{3.58}$$

Moreover, the output voltages are functions of all effective input and output duty cycles, including $A_{e,1}$. Thus,

$$S_{D_{e,i}}^{V_{o,j}} = \frac{dV_{o,j}(D_{e,i}, A_{e,1})}{dD_{e,i}} \cdot \frac{D_{e,i}}{I_L} = \left(\frac{\partial V_{o,j}}{\partial D_{e,i}} \cdot \frac{\partial D_{e,i}}{\partial D_{e,i}} + \frac{\partial V_{o,j}}{\partial A_{e,1}} \cdot \frac{\partial A_{e,1}}{\partial D_{e,i}} \right) \cdot \frac{D_{e,i}}{I_L}. \tag{3.59}$$

Using (3.58), (3.59), and (3.8), the sensitivity of output voltages with respect to the effective input duty cycles can be found as

$$S_{D_{e,i}}^{V_{o,j}} = \frac{D_{e,i}V_{in,i}}{\sum_{k=1}^{m} V_{in,k}D_{e,k}} - \frac{D_{e,i}}{\sum_{k=1}^{j} A_{e,k}} + \frac{2D_{e,i}\sum_{k=1}^{n} n_{k,j}\left(\sum_{l=1}^{k} A_{e,l}\right)}{\sum_{k=1}^{n} n_{k,j}\left(\sum_{l=1}^{k} A_{e,l}\right)^2}. \tag{3.60}$$

3.6.3 Sensitivity to Variations in Output Duty Cycles

Similar to (3.60), the sensitivity of output voltages to the output duty cycles can be found using partial differentiation:

$$S_{A_{e,i}}^{V_{o,j}} = \begin{cases} \dfrac{2A_{e,i}\sum_{k=1}^{i-1} n_{k,j}\left(\sum_{l=1}^{k} A_{e,l}\right)}{\sum_{k=1}^{n} n_{k,j}\left(\sum_{l=1}^{k} A_{e,l}\right)^2} & , 1 \le i \le j \\ -\dfrac{A_{e,i}}{\sum_{k=1}^{j} A_{e,k}} + \dfrac{2A_{e,i}\sum_{k=1}^{i-1} n_{k,j}\left(\sum_{l=1}^{k} A_{e,l}\right)}{\sum_{k=1}^{n} n_{k,j}\left(\sum_{l=1}^{k} A_{e,l}\right)^2} & , j < i \le n \end{cases} \tag{3.61}$$

3.7 Case Studies

3.7.1 Steady-state Operation

A laboratory-scale prototype with three inputs and two outputs is built to evaluate the steady-state characterizations in both CCM and DCM. Since steady-state operation is intended, no closed-loop feedback scheme is employed in this converter. The circuit parameters pertaining to this converter are as follows. $V_{in,1} = 12V$, $V_{in,2} = 9V$, $V_{in,3} = 5V$, $L = 1.2mH$, $C_1 = 22\mu F$, $C_2 = 68\mu F$, $r_L = 0.44\Omega$, $r_{C,1} = 0.1\Omega$, $r_{C,2} = 0.2\Omega$, $r_{on,diode} = 0.014\Omega$, $V_{on,diode} = 0.4V$, $r_{on,MOSFET} = 0.07\Omega$, and $f_{sw} = 10KHz$. The output loads in CCM and DCM are $\{R_1 = 46.7\Omega,\ R_2 = 12.0\Omega\}$ and $\{R_1 = 440\Omega,\ R_2 = 120\Omega\}$, respectively.

3.7.1.1 CCM

The output voltages, $V_{o,1}$ and $V_{o,2}$, are functions of $D_{e,1}$, $D_{e,2}$, $D_{e,3}$, and $A_{e,2}$; note that $A_{e,1}$ is uncontrollable since S_1' is a single diode. First, $D_{e,2}$ and $D_{e,3}$ are kept constant ($D_{e,2} = 0.1$ and $D_{e,3} = 0.3$) while $D_{e,1}$ and $A_{e,2}$ can change. The output voltages found by (3.46) are plotted in Figure 3.9. The corresponding plot obtained by detailed switch-level simulation is illustrated in Figure 3.10. The detailed switch-level simulation is conducted using the PLECS toolbox in MATLAB/SIMULINK [28]. A good match between the analytical derivations, Figure 3.9, and detailed switch-level simulations, Figure 3.10, can be observed.

Next, $D_{e,1}$ is also kept constant ($D_{e,1} = 0.2$, $D_{e,2} = 0.1$ and $D_{e,3} = 0.3$). The highlighted curves in Figure 3.9(c,f) and Figure 3.10(c,f) correspond to this condition. These curves are plotted in two dimensions in Figure 3.11. Measurement data are also included in Figure 3.11 to further verify the analytical model.

If $D_{e,2}$, $D_{e,3}$, and $A_{e,2}$ are kept constant ($D_{e,2} = 0.1$, $D_{e,3} = 0.3$, $A_{e,2} = 0.2$), the output voltages will be only functions of $D_{e,1}$. The highlighted curves in Figure 3.9(b,e) and Figure 3.10(b,e) correspond to this condition. These curves are plotted together with the measurement data in Figure 3.12. A good match between the analytical derivations, detailed switch-level simulations, and measurement data can be observed in Figure 3.12.

Next, all effective input and output duty cycles are kept constant ($D_{e,1} = 0.2$, $D_{e,2} = 0.1$, $D_{e,3} = 0.3$, $A_{e,2} = 0.2$). Circuit waveforms obtained by simulation and hardware measurement for this operating point are depicted in Figure 3.13 and Figure 3.14, respectively. A good match between simulation and measurement can be observed from Figure 3.13 and Figure 3.14.

3.7.1.2 DCM

The converter operation in the second DCM mode is considered. Similar to CCM, the output voltages are functions of effective input and output duty cycles, $D_{e,1}, D_{e,2}, D_{e,3}, A_{e,2}$. First, $D_{e,2}$ and $D_{e,3}$

are set at 0.1 and 0.3, respectively. Therefore, the output voltages are functions of only $D_{e,1}$ and $A_{e,2}$. The calculated and simulated output voltages in this condition are illustrated in Figure 3.15 and Figure 3.16, respectively.

Setting $A_{e,2}$ at 0.2, the highlighted curves in Figure 3.15(c,f) and Figure 3.16(c,f) are resulted. These curves are plotted in Figure 3.17 along with the measurement data. A good match can be observed between analytical derivations, detailed switch-level simulations, and measurements.

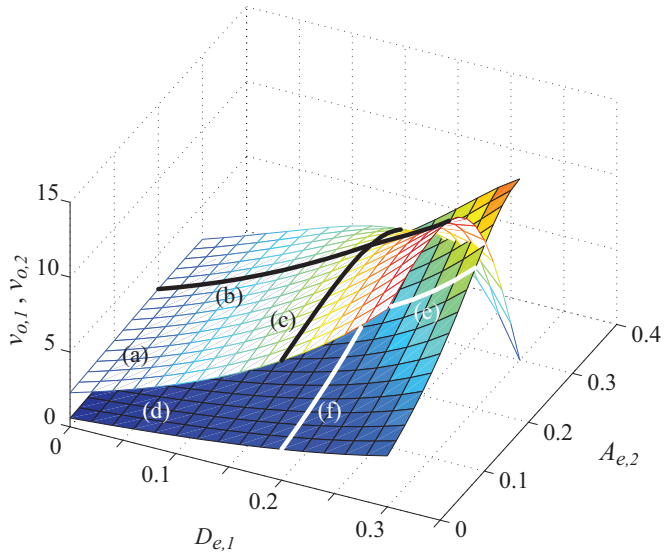

Figure 3.9 The output voltages obtained by analytical derivations, (3.46), in CCM ($D_{e,2} = 0.1$ and $D_{e,3} = 0.3$): (a) $v_{o,1}$ surface, (b) $v_{o,1}$ curve when $A_{e,2} = 0.2$, (c) $v_{o,1}$ curve when $D_{e,1} = 0.2$, (d) $v_{o,2}$ surface, (e) $v_{o,2}$ curve when $A_{e,2} = 0.2$, (f) $v_{o,2}$ curve when $D_{e,1} = 0.2$.

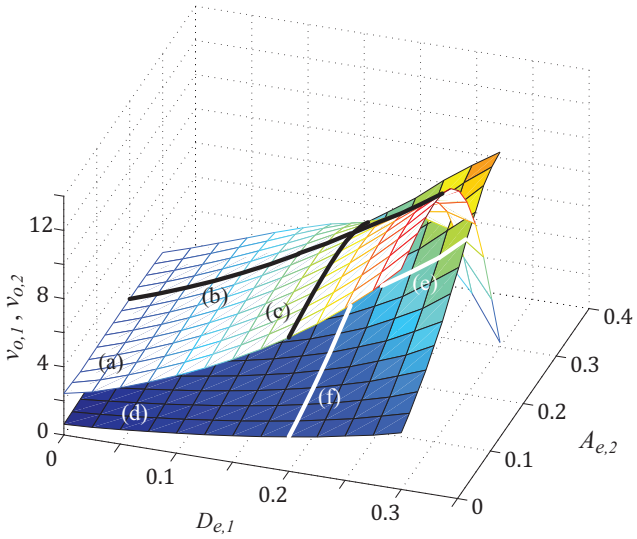

Figure 3.10 The output voltages obtained by detailed switch-level simulations in CCM ($D_{e,2} = 0.1$ and $D_{e,3} = 0.3$): (a) $v_{o,1}$ surface, (b) $v_{o,1}$ curve when $A_{e,2} = 0.2$, (c) $v_{o,1}$ curve when $D_{e,1} = 0.2$, (d) $v_{o,2}$ surface, (e) $v_{o,2}$ curve when $A_{e,2} = 0.2$, (f) $v_{o,2}$ curve when $D_{e,1} = 0.2$.

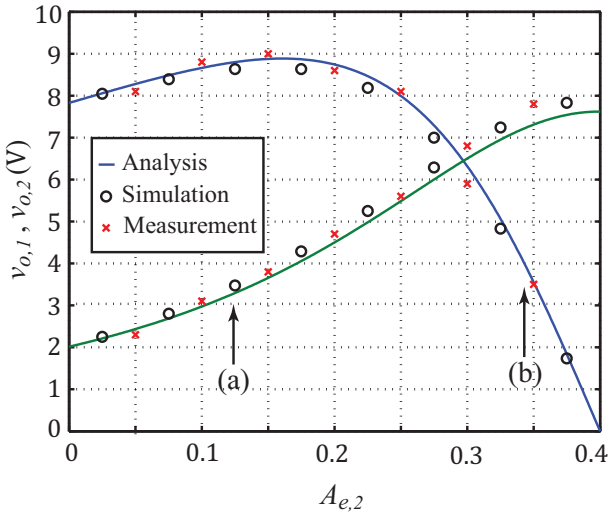

Figure 3.11 The calculated, simulated, and measured output voltages in CCM ($D_{e,1} = 0.2$, $D_{e,2} = 0.1$ and $D_{e,3} = 0.3$): (a) $v_{o,2}$, and (b) $v_{o,1}$.

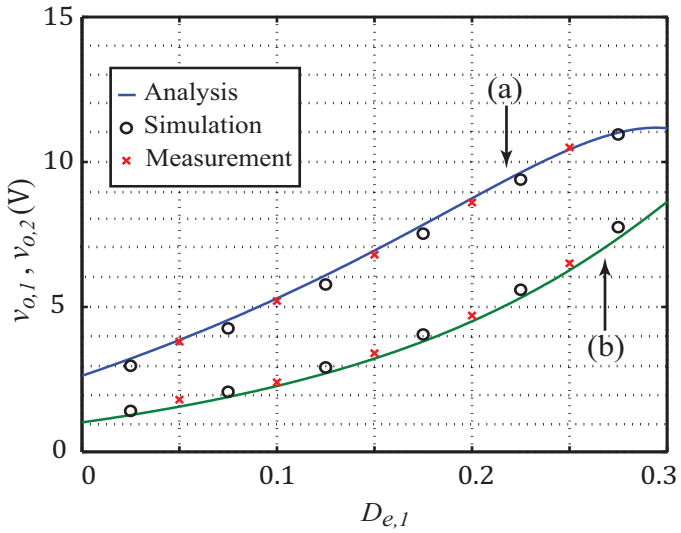

Figure 3.12 The calculated, simulated, and measured output voltages in CCM ($D_{e,2} = 0.1$, $D_{e,3} = 0.3$, and $A_{e,2} = 0.2$): (a) $v_{o,1}$, and (b) $v_{o,2}$.

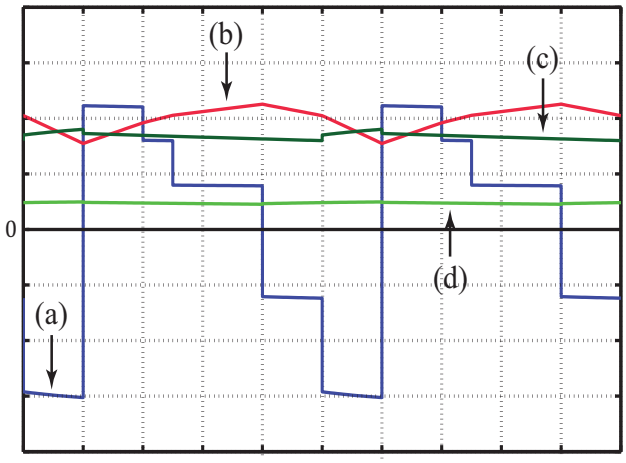

Figure 3.13 The circuit waveforms obtained by simulations in CCM ($D_{e,1} = 0.2$, $D_{e,2} = 0.1$, $D_{e,3} = 0.3$, and $A_{e,2} = 0.2$): (a) v_L (5V/div), (b) i_L (500mA/div), (c) $v_{o,1}$ (5V/div), and (d) $v_{o,2}$ (10V/div), (time scale: 20μs/div).

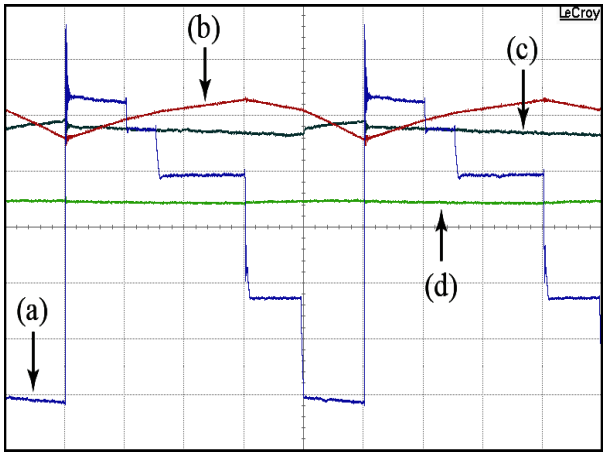

Figure 3.14 The circuit waveforms obtained by hardware measurements in CCM ($D_{e,1} = 0.2$, $D_{e,2} = 0.1$, $D_{e,3} = 0.3$, and $A_{e,2} = 0.2$): (a) v_L (5V/div), (b) i_L (500mA/div), (c) $v_{o,1}$ (5V/div), and (d) $v_{o,2}$ (10V/div), (time scale: 20µs/div).

If $D_{e,1}$ is also kept constant and $A_{e,2}$ is relaxed ($D_{e,1} = 0.1$, $D_{e,2} = 0.1$, $D_{e,3} = 0.3$), the output voltages will be functions of only $A_{e,2}$. The highlighted curves in Figure 3.15(b,e) and Figure 3.16(b,e) correspond to this condition. These curves are plotted in Figure 3.18 together with the measurement results. A good match between analytical derivations, detailed switch-level simulation, and hardware measurements is reported.

The simulated circuit waveforms for an specific operating point are shown in Figure 3.19. In this operating point, $D_{e,1} = 0.1$, $D_{e,2} = 0.2$, $D_{e,3} = 0.1$, and $A_{e,2} = 0.2$. The corresponding measured waveforms are depicted in Figure 3.20. A good match can be observed between simulation and measurement from Figure 3.19 and Figure 3.20. The oscillation of the inductor current in Figure 3.20(b), once it touches zero, is due to the parasitic capacitances of the MOSFETs and reverse recovery effects of the diodes. This oscillation is negligible and does change the equilibrium point.

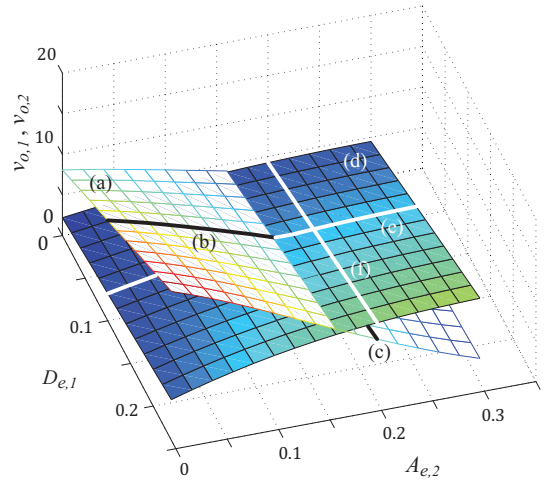

Figure 3.15 The output voltages obtained by analytical derivations, in DCM ($D_{e,2} = 0.1$ and $D_{e,3} = 0.3$): (a) $v_{o,1}$ surface, (b) $v_{o,1}$ curve when $D_{e,1} = 0.1$, (c) $v_{o,1}$ curve when $A_{e,2} = 0.2$, (d) $v_{o,2}$ surface, (e) $v_{o,2}$ curve when $D_{e,1} = 0.1$, (f) $v_{o,2}$ curve when $A_{e,2} = 0.2$.

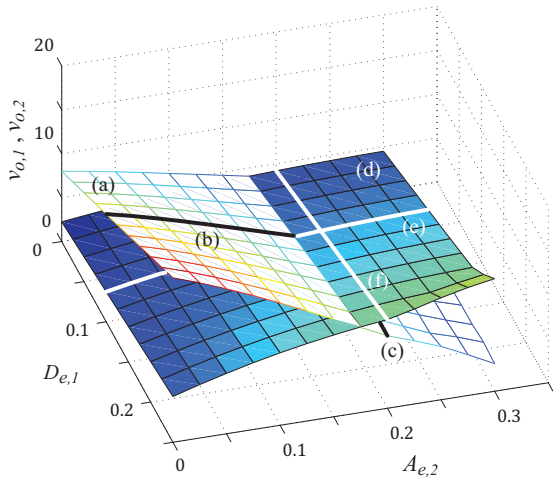

Figure 3.16 The output voltages obtained by detailed switch-level simulations in DCM ($D_{e,2} = 0.1$ and $D_{e,3} = 0.3$): (a) $v_{o,1}$ surface, (b) $v_{o,1}$ curve when $D_{e,1} = 0.1$, (c) $v_{o,1}$ curve when $A_{e,2} = 0.2$, (d) $v_{o,2}$ surface, (e) $v_{o,2}$ curve when $D_{e,1} = 0.1$, (f) $v_{o,2}$ curve when $A_{e,2} = 0.2$.

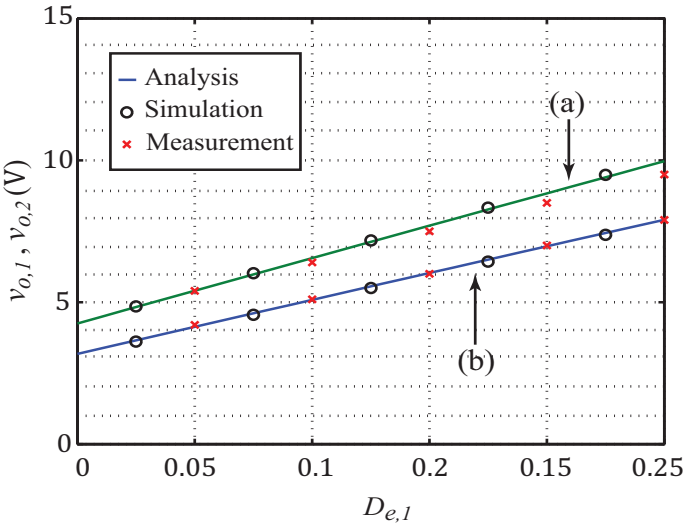

Figure 3.17 The calculated, simulated, and measured output voltages in DCM, ($D_{e,2} = 0.1$, $D_{e,3} = 0.3$, $A_{e,2} = 0.2$): (a) $v_{o,2}$, and (b) $v_{o,1}$.

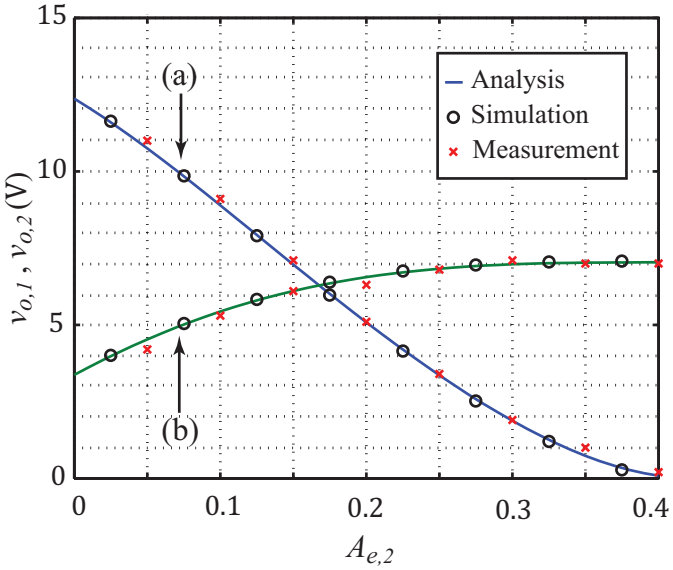

Figure 3.18 The calculated, simulated, and measured output voltages in DCM, when $D_{e,1} = 0.1$, $D_{e,2} = 0.1$ and $D_{e,3} = 0.3$: (a) $v_{o,1}$, and (b) $v_{o,2}$.

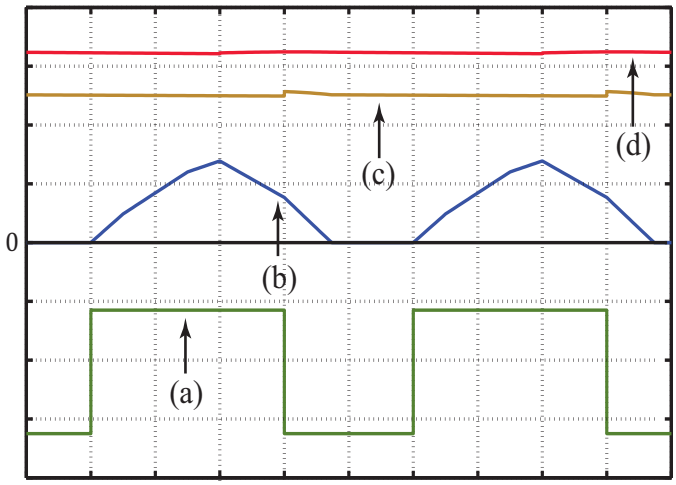

Figure 3.19 The circuit waveforms obtained by simulations in DCM ($D_{e,1} = 0.1$, $D_{e,2} = 0.2$, $D_{e,3} = 0.1$, and $A_{e,2} = 0.2$): (a) q_2' , (b) i_L (200mA/div), (c) $v_{o,1}$ (2V/div), and (d) $v_{o,2}$ (2V/div), (time scale: 20μs/div).

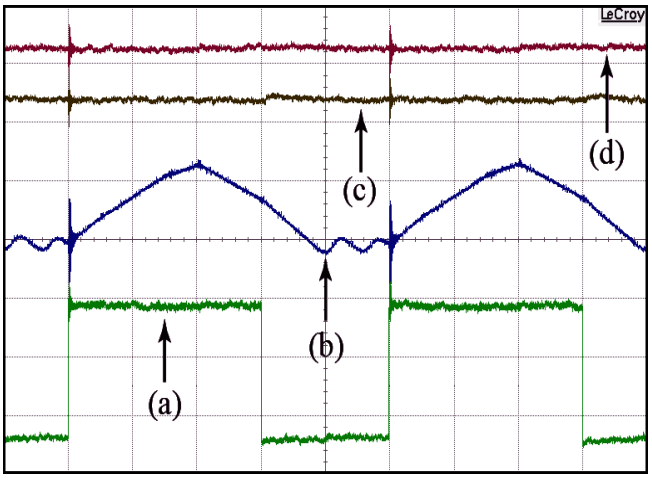

Figure 3.20 The circuit waveforms obtained by hardware measurements in DCM ($D_{e,1} = 0.1$, $D_{e,2} = 0.2$, $D_{e,3} = 0.1$, and $A_{e,2} = 0.2$): (a) q_2' , (b) i_L (200mA/div), (c) $v_{o,1}$ (2V/div), and (d) $v_{o,2}$ (2V/div), (time scale: 20μs/div).

3.7.2 Dynamic Performance

A two-input, two-output prototype, and corresponding closed-loop controller, are considered to evaluate the dynamic performance of the converter; Figure 3.21 shows the hardware setup. The circuit parameters for this converter are as follows: $V_{in,1} = 30V$, $V_{in,2} = 20V$, $P_{in,1} = 25W$, $V_{o,1} = 21V$, $V_{o,2} = 8V$, $L = 250\mu H$, $C_1 = 2200\mu F$, $C_2 = 2200\mu F$, $R_1 = 25\Omega$, $R_2 = 6\Omega$, and $f_{sw} = 40KHz$.

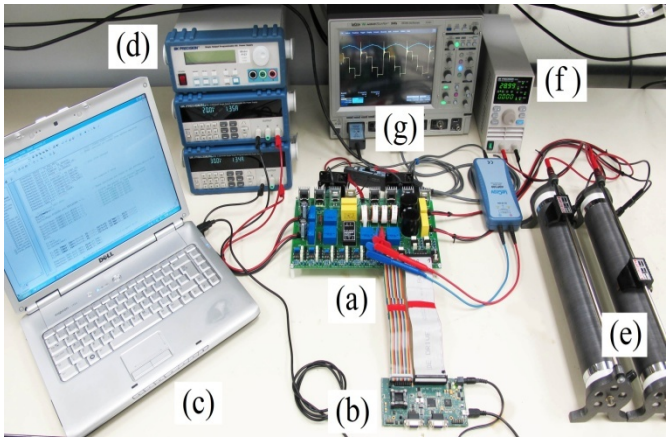

Figure 3.21 The hardware setup: (a) MIMO converter, (b) target computer (ezDSP TMS320F2808 board), (c) host computer (laptop), (d) input sources, (e) static output loads (rheostats), (f) dynamic output load, (g) oscilloscope.

3.7.2.1 Input-to-output Transfer Functions

According to Figure 3.7, ten input-to-output transfer functions can be identified for this converter, four of which relate the input voltages, $v_{in,1}$ and $v_{in,2}$, to the output voltages, $v_{o,1}$ and $v_{o,2}$. The other six transfer functions relate the effective duty cycles, d_{e1}, $d_{e,2}$, and $\alpha_{e,2}$, to the output voltages, $v_{o,1}$ and $v_{o,2}$. Here, two of these input-to-output transfer functions are considered for brevity, namely, H_{11}^{d} and H_{22}^{d}. Figure 3.22 illustrates the model prediction, numerical simulation, and measurement data pertaining to these transfer functions. Numerical simulations are conducted using MATLAB/SIMULINK. A good match can be observed between the model, simulation, and measurement in Figure 3.22.

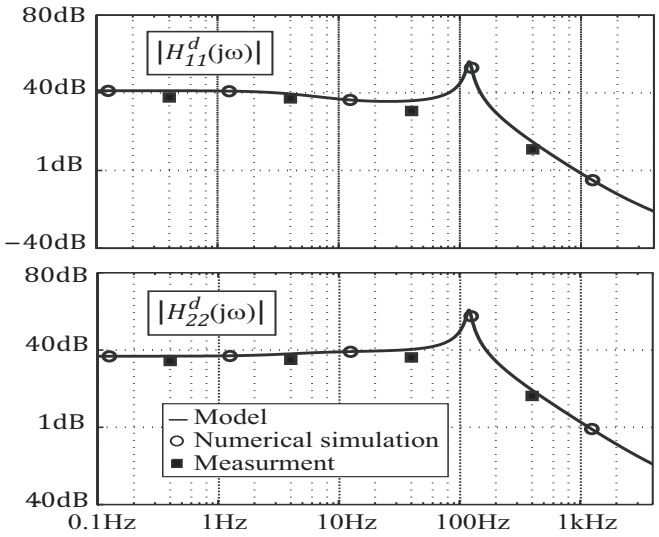

Figure 3.22 The input to output transfer functions $H_{11}^d(s)$ and $H_{22}^d(s)$.

3.7.2.2 Line Regulation

The controller scheme described in section 3.4 is implemented on a ezDSP TMS320F2808 board (target computer). The DSP board is connected to the host computer (laptop) via a USB JTAG emulation connector. Optimum controller design for the converter requires optimal tuning of the $\mathbf{K}_i$ and $\mathbf{K}_p$ matrices, each of which has 3×3 entries. Optimum multivariable controller design is not within the scope of the discussion here. Thus, without the loss of generality, $\mathbf{K}_p$ is set to zero for simplicity. Matrix $\mathbf{K}_i$ is tuned to stabilize the system using (3.43) and (3.44). Figure 3.23 shows the dynamic response of the system to a step change in the first input voltage. As depicted in Figure 3.23, the first input power, $p_{in,1}$, is also regulated in addition to the output voltages. Once the step change occurs in first input voltage, $v_{in,1}$, the controller adjusts the duty cycles to change $\langle i_{in,1} \rangle$ accordingly, such that $p_{in,1}$ remains constant.

3.7.2.3 Load Regulation

The controller's response to a 40% step change in the first load, R_1, is shown in Figure 3.24. Since the first input voltage, $v_{in,1}$, does not change, regulating $p_{in,1}$ is equivalent to keeping $\langle i_{in,1} \rangle$

constant in this case. The d_1, d_2, and α_2 traces in Figure 3.24 show how the controller adjusts the duty cycles to regulate $\langle i_{in,1} \rangle$ in addition to $v_{o,1}$ and $v_{o,2}$.

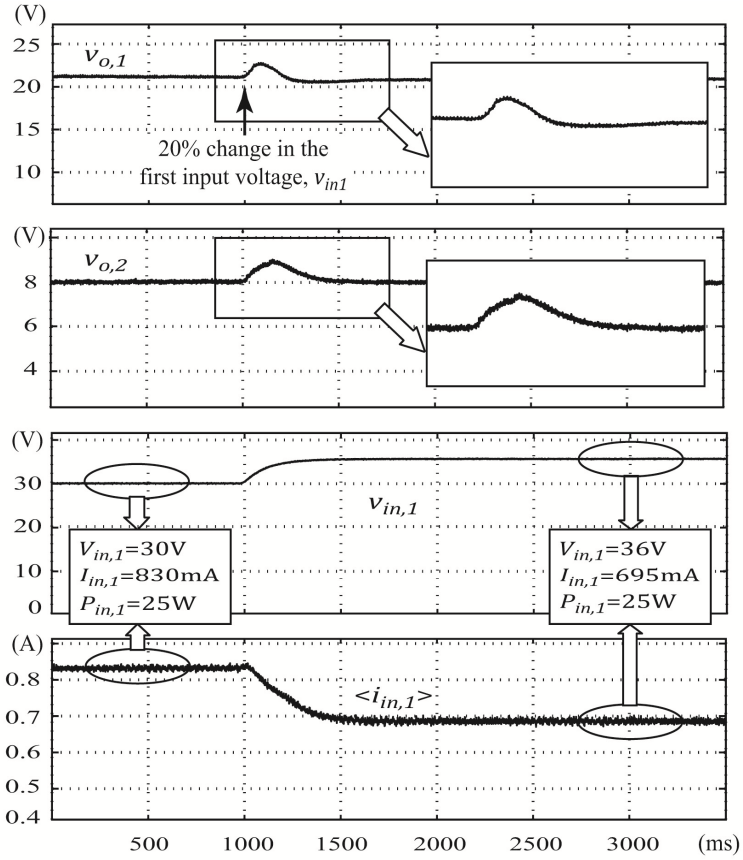

Figure 3.23 Line regulation: measured converter response to step change in $v_{in,1}$

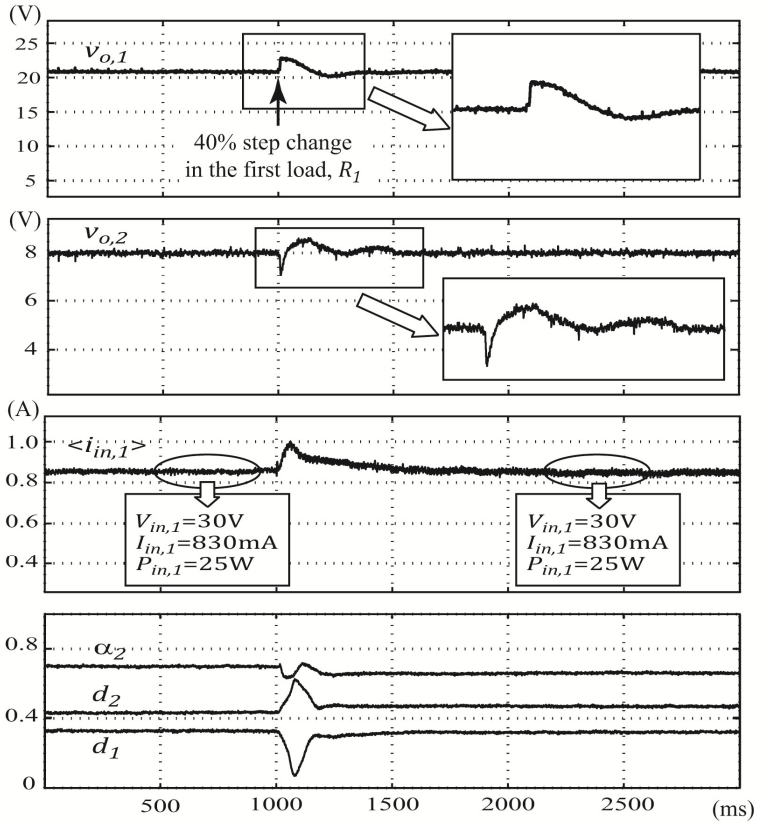

Figure 3.24 Load regulation: the converter's response to step change in R_1.

3.7.3 Efficiency

Figure 3.25 shows the efficiency of the converter versus the total output power. The output powers are equal in Figure 3.25, i.e., each load consumes half of the total output power. The measurement results show 86% efficiency for the laboratory-scale prototype in the designated operating point. It should be noted that MOSFETs and diodes are overdesigned in the laboratory-scale prototype; they have relatively high forward voltage drop and on-state resistance and, consequently, undermine the efficiency of the prototype. However, in general, since multiport topologies share the components among different sources and loads, they have fewer components compared to their multi-converter counterparts. Thus, one can expect the proposed topology to be more efficient than its conventional multi-converter counterparts with the same number of inputs and output ports.

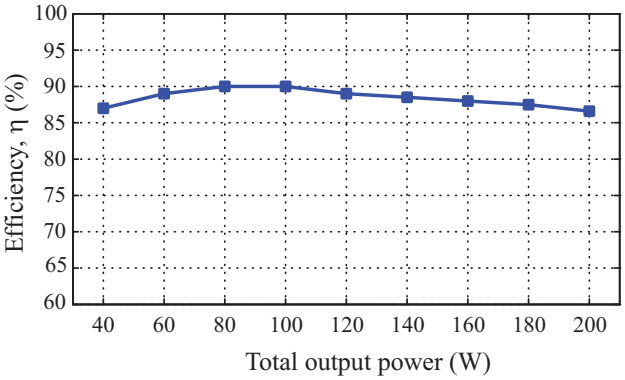

Figure 3.25 The converter efficiency versus total output power.

The discrete-time model of the proposed MIMO converters will be presented in the next chapter.

CHAPTER 4

DISCRETE-TIME MODELING OF MULTIPORT DC-DC CONVERTERS

Multiport dc-dc converters, as discussed in chapters 2 and 3, have recently received great attention due to their desired characteristics including cost effectiveness, compact design, and diversification of energy sources with complementary natures [8, 13, 14, 31, 32]. Digital controllers are widely used in PWM converters due to their salient features, namely, immunity to parameter variations, passive component elimination, less electromagnetic-interference susceptibility, and ability to handle complex control algorithms [33, 34]. Automated system identification and self-tuning techniques, which are very difficult to realize using analog controllers, can be easily integrated in digital controllers [35, 36]. Therefore, digital controllers are becoming prevalent in multiport converters [16, 37, 38].

Digital design tools described in current literature can be categorized into IDM and DDM [39]. In IDM, the power-stage model (called "plant model" hereafter) is developed using conventional averaging methods [40-43]. The resulting continuous-time plant model is converted to the discrete-time domain using z-transform techniques and the digital controller is designed based on the resulting discrete-time model. Although straightforward, IDM have several drawbacks. The selection of the discretization method and the sampling rate can lead to models that are unable to accurately predict the stability of the closed-loop system [39]. Moreover, IDM models inherit the intrinsic shortcomings of averaging techniques, such as discrepancy at high frequencies and inaccuracy in predicting the closed-loop stability [27, 44]. In DDM models [45-47], the plant model is characterized directly in the discrete-time domain, which leads to a high-fidelity model. A DDM-based model that involves computation of matrix exponentials is proposed in [47-49] for SISO dc-dc converters. A similar approach is presented in [50] based on truncating the matrix exponentials in a bilinear fashion. Another DDM-based model is developed in [51] based on the transition of the spectral coefficients of the state variables. The state-variable sensitivity method is employed in [52] to develop a DDM-based model for AC/DC converters. The distinction between IDM and DDM is sometimes blurred in methods that combine the state-space

averaging and DDM to obtain a simplified discrete-time model, e.g., [53]. In general, direct digital controller design for multiport converters requires an accurate discrete-time modeling framework.

Multiport dc-dc converters can be modeled as continuous MIMO systems using conventional averaging methods [9, 54]. In multiple-output converters, cross regulation issues make the tight regulation of the output voltages challenging [18, 19]. Another aspect of multiport dc-dc converters, that employ time-multiplexing switching schemes, is the concept of EDCs [3, 6, 7, 31]. It will be shown that EDCs will cause multiple signal propagation paths throughout the switching period, which makes the precise dynamic modeling of such systems more mathematically involved. In this chapter, a general high-fidelity discrete-time modeling framework is set forth that extends the direct digital design methods in [47] to multiport converters. The salient features of this proposed technique can be summarized as follows.

- It accommodates the time-multiplexing switching schemes seen in the multiport dc-dc converters by accounting for the corresponding multiple propagation paths in each switching period.
- It avoids assumptions involved in averaging techniques (e.g., small state-variable ripples) by using the Floquet theory [55], while the final model is still simple enough for design purposes.
- It is able to model the sampling effect, modulator effect, and the propagation delays. The results can be extended to both leading- and trailing- edge PWM schemes.

Multiport dc-dc converters include MISO, SIMO, and MIMO converters. The most general case, MIMO converters, is considered. Figure 4.1 depicts the proposed MIMO converter in chapter 2, which utilizes a single inductor and time-multiplexing switching schemes [54]. As discussed in chapters 2 and 3, the EDCs of the input and output switches are not necessarily the same as their commanded duty cycles. An ideal discrete-time modeling framework should consider the effective duty cycles and time multiplexing properties of multiport converters.

The two-input two-output converter considered in chapter 2 is shown again in Figure 4.1. The converter has four active switches (MOSFETs), S_1, S_2, S_2', and S_3'. Figure 4.2 depicts the switching

commands of the active switches; q_1 is the switching command of S_1, q_2 is the switching command of both S_2 and S_3', and q_3 is the switching command of S_2'. The duty cycles of q_1, q_2, and q_3 are denoted by d_1, d_2, and d_3, respectively. In the first switching subinterval ($0 \leq t < d_1 T_s$), all S_1, S_2, S_2', and S_3' are commanded on; however, only S_1 and S_3' conduct the current. In the second subinterval ($d_1 T_s \leq t < d_2 T_s$), S_1 is off and the inductor current flows through S_2 and S_3'. In the third subinterval ($d_2 T_s \leq t < d_3 T_s$), S_2 and S_3' are off and the inductor current flows through the S_3 and S_2'. In the fourth subinterval ($d_3 T_s \leq t < T_s$), all switches are off and the inductor current flows through the diodes S_3 and S_1'.

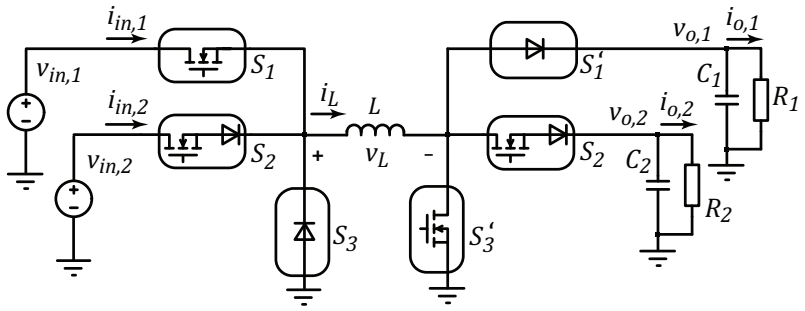

Figure 4.1 The buck-boost-type MIMO dc-dc converter proposed in [54].

4.1 Discrete-time Model

The discrete-time model is developed based on the piecewise linear model of the converter in the different topological instances of a prototypical switching interval. There are $M+N$ topological instances for the M-input N-output MIMO converter employing the time-multiplexing scheme. The converter linear model during each topological instance can be expressed in a canonical state-space format as

$$\begin{cases} \dfrac{d\mathbf{x}}{dt} = \mathbf{A}_k \mathbf{x} + \mathbf{b}_k \\ \mathbf{y} = \mathbf{C}_k \mathbf{x} + \mathbf{d}_k \end{cases}, \qquad k = 1, \cdots, M+N \tag{4.1}$$

where $\mathbf{A}_k$, $\mathbf{b}_k$, $\mathbf{C}_k$, and $\mathbf{d}_k$ are the system matrix, input vector, output matrix, and feed-through vector in the k^{th} topological instance, respectively. The duration of each subinterval is determined by the

corresponding effective duty cycle. A single ADC sampling per switching period is considered. The desired small-signal discrete-time model should be of the form

$$\begin{cases} {}^{(N+1)\times 1}\hat{\mathbf{x}}[n] = {}^{(N+1)\times(N+1)}\mathbf{\Phi}\hat{\mathbf{x}}[n-1] + {}^{(N+1)\times(M+N-1)}\mathbf{\Gamma}\hat{\mathbf{d}}_e[n-1] \\ {}^{M\times 1}\hat{\mathbf{y}}[n] = {}^{M\times(N+1)}\mathbf{C}_1\hat{\mathbf{x}}[n] \end{cases} \tag{4.2}$$

where $\hat{\mathbf{x}}[n]$, $\hat{\mathbf{d}}_e[n]$, and $\hat{\mathbf{y}}[n]$ are the perturbations in the state vector, effective duty-cycle vector, and output vector, respectively; and n is the index term (not to be confused with the number of the output ports, N). Matrices $\mathbf{\Phi}$, $\mathbf{\Gamma}$, and $\mathbf{C}_1$ form the discrete-time model. Without loss of generality, the sampling is assumed to take place at the beginning of each switching cycle; therefore, the matrix $\mathbf{C}_1$, pertaining to the first topological instance in (4.1), determines the state-to-output relationship. Matrices $\mathbf{\Phi}$ and $\mathbf{\Gamma}$ are needed to finalize the model formulation.

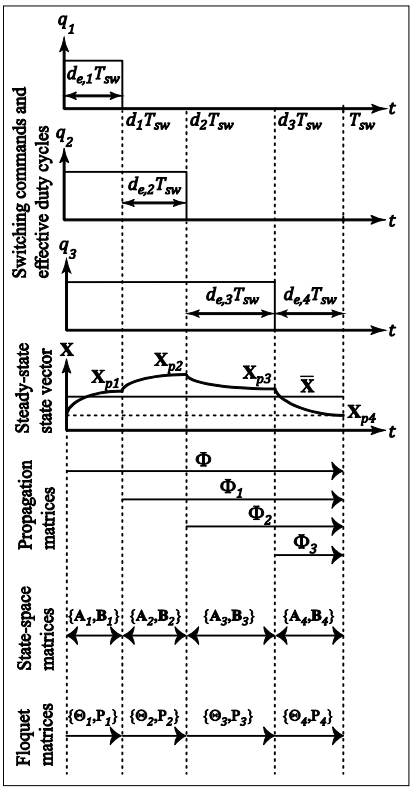

Figure 4.2 Switching commands, effective duty cycles, state-vector evolution in steady state, propagation matrices, state-space matrices, and Floquet matrices for the MIMO converter in Figure 4.1 (two inputs/two outputs).

Although there are $M+N$ effective duty cycles, only $M+N-1$ of those are independent. The perturbation in the last effective duty cycle, $\hat{d}_{e,M+N}[n]$, can be expressed in terms of those in the other effective duty cycles as

$$\hat{d}_{e,M+N}[n] = 1 - \sum_{k=1}^{M+N-1} \hat{d}_{e,k}[n]. \tag{4.3}$$

Consequently, vector $\hat{\mathbf{d}}_e[n]$ is of the length $M+N-1$,

$$\hat{\mathbf{d}}_e[n-1] = [\hat{d}_{e,1}[n-1] \quad \cdots \quad \hat{d}_{e,M+N-1}[n-1]]^T \tag{4.4}$$

and matrix $\mathbf{\Gamma}$ has $N+1$ rows and $M+N-1$ columns,

$$\mathbf{\Gamma} = [\boldsymbol{\gamma}_1 \,|\, \boldsymbol{\gamma}_2 \,|\, \cdots \,|\, \boldsymbol{\gamma}_{M+N-1}] \tag{4.5}$$

Each column, $\boldsymbol{\gamma}_k$, is determined separately and, then, they will be all aggregated to the matrix $\mathbf{\Gamma}$. The column $\boldsymbol{\gamma}_k$ describes the effect of perturbation in the effective duty cycle $\hat{d}_{e,k}[n-1]$ on the state vector at the end of the switching period, $\hat{\mathbf{x}}[n]$. To find $\boldsymbol{\gamma}_k$, the state-space description of the converter in the k^{th} and $(k+1)^{\text{th}}$ consecutive topological instances are considered as follows

$$\begin{cases} \sum_{i=0}^{k-1} d_{e,i}T_s \le t < \sum_{i=0}^{k} d_{e,i}T_s \\ \dfrac{d\mathbf{x}}{dt} = \mathbf{A}_k\mathbf{x} + \mathbf{b}_k \\ \mathbf{y} = \mathbf{C}_k\mathbf{x} + \mathbf{d}_k \end{cases} \text{(I)}, \quad \begin{cases} \sum_{i=0}^{k} d_{e,i}T_s \le t < \sum_{i=0}^{k+1} d_{e,i}T_s \\ \dfrac{d\mathbf{x}}{dt} = \mathbf{A}_{k+1}\mathbf{x} + \mathbf{b}_{k+1} \\ \mathbf{y} = \mathbf{C}_{k+1}\mathbf{x} + \mathbf{d}_{k+1} \end{cases} \text{(II)} \tag{4.6}$$

It is assumed that the steady-state state vector at the switching instant between the two consecutive topological instances is $\mathbf{X}_{p,k}$. With a small-signal perturbation in $d_{e,k}$, the portion of the time spent in (4.6)-(I) is increased by $\hat{d}_{e,k}T_s$ while the portion of the time spent in (4.6)-(II) is decreased by $\hat{d}_{e,k}T_s$. Therefore, perturbation in $\hat{d}_{e,k}$ will cause a perturbation in the state vector at the switching instant between the two consecutive topological instances. This instantaneous state perturbation, $\hat{\mathbf{x}}_d$, can be found by considering the difference between the time spent in (4.6)-(I) and (4.6)-(II) ($\hat{d}_{e,k}T_s$) as follows.

$$\hat{\mathbf{x}}_d = [(\mathbf{A}_k - \mathbf{A}_{k+1})\mathbf{X}_{p,k} + (\mathbf{b}_k - \mathbf{b}_{k+1})]T_s\hat{d}_{e,k} \tag{4.7}$$

The instantaneous perturbation in the state vector, $\hat{\mathbf{x}}_d$, will then propagate throughout the rest of the switching period and causes a perturbation in the state vector at the next sampling instance, i.e., $\hat{\mathbf{x}}[n]$. The propagation effect is considered using different propagation matrices, $\mathbf{\Phi}_k$, depending on when $\hat{\mathbf{x}}_d$ happens during the switching period (see Figure 4.2). According to Figure 4.2, the perturbations occurring at the trailing edges of q_1, q_2, and q_3 will propagate through propagation matrices $\mathbf{\Phi}_1$, $\mathbf{\Phi}_2$, and $\mathbf{\Phi}_3$, respectively.

It should be noted that perturbations in $\hat{d}_{e,1}$, while keeping other $d_{e,k}$s constant, will cause three different instantaneous perturbations in the state vector at the trailing edges of q_1, q_2, and q_3 (see Figure 4.2). Similarly, perturbations in $\hat{d}_{e,2}$, while keeping other $d_{e,k}$s constant, will cause two different instantaneous perturbations in the state vector at the trailing edges of q_2 and q_3. Since q_3 is the last switching command, perturbations in $\hat{d}_{e,3}$ causes only a single instantaneous perturbation in the state vector at the trailing edge of q_3. These instantaneous state perturbations travel through the switching period with different propagation matrices, $\mathbf{\Phi}_k$, depending on their relative location in the switching cycle. Consequently, one may find $\boldsymbol{\gamma}_k$s ($k = 1,2,3$) as follows

$$\begin{cases} \boldsymbol{\gamma}_1 = \mathbf{\Phi}_1[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X}_{p1} + (\mathbf{b}_1 - \mathbf{b}_2)]T_s + \mathbf{\Phi}_2[(\mathbf{A}_2 - \mathbf{A}_3)\mathbf{X}_{p2} + (\mathbf{b}_2 - \mathbf{b}_3)]T_s + \mathbf{\Phi}_3[(\mathbf{A}_3 - \mathbf{A}_4)\mathbf{X}_{p3} + (\mathbf{b}_3 - \mathbf{b}_4)]T_s \\ \boldsymbol{\gamma}_2 = \mathbf{\Phi}_2[(\mathbf{A}_2 - \mathbf{A}_3)\mathbf{X}_{p2} + (\mathbf{b}_2 - \mathbf{b}_3)]T_s + \mathbf{\Phi}_3[(\mathbf{A}_3 - \mathbf{A}_4)\mathbf{X}_{p3} + (\mathbf{b}_3 - \mathbf{b}_4)]T_s \\ \boldsymbol{\gamma}_3 = \mathbf{\Phi}_3[(\mathbf{A}_3 - \mathbf{A}_4)\mathbf{X}_{p3} + (\mathbf{b}_3 - \mathbf{b}_4)]T_s \end{cases}$$

(4.8)

Given the steady-state state vectors at the trailing edges of the switching commands, $\mathbf{X}_{p,k}$, and the propagation matrices, $\mathbf{\Phi}_k$, (4.8) can be used to find the input matrix $\mathbf{\Gamma}$ in (4.5). $\mathbf{X}_{p,k}$ can be approximated by the average steady-state state vector, $\overline{\mathbf{X}}$ [26]; however, exact calculation of $\mathbf{X}_{p,k}$ using Floquet theory [55] results in models with better accuracy.

Considering the canonical state-space description in each topological instance (4.6), $\mathbf{X}_{p,i}$ can be expressed in terms of the previous $\mathbf{X}_{p,i-1}$ as follows.

$$\mathbf{X}_{p,i} = e^{\mathbf{A}_i D_{e,i} T_s} \mathbf{X}_{p,i-1} + \int_0^{D_{e,i}T_s} e^{\mathbf{A}_i (D_{e,i}T_s - \tau)} \mathbf{b}_i d\tau = \mathbf{\Theta}_i \mathbf{X}_{p,i} + \mathbf{P}_i \tag{4.9}$$

where $D_{e,i}$ is the steady-state value of $d_{e,i}$ and $\mathbf{\Theta}_i$ and $\mathbf{P}_i$ are constant matrices pertaining to the i^{th} topological instance (see Figure 4.2), given by

$$\begin{cases} \mathbf{\Theta}_i = e^{\mathbf{A}_i D_{e,i} T_s} \\ \mathbf{P}_i = \int_0^{D_{e,i}T_s} e^{\mathbf{A}_i (D_{e,i}T_s - \tau)} \mathbf{b}_i d\tau = (e^{\mathbf{A}_i D_{e,i} T_s} - \mathbf{I}) \mathbf{A}_i^{-1} \mathbf{b}_i = (\mathbf{\Theta}_i - \mathbf{I}) \mathbf{A}_i^{-1} \mathbf{b}_i \end{cases}. \tag{4.10}$$

Thus, $\mathbf{X}_{p,i}$ can be determined recursively as

$$\mathbf{X}_{p,i} = \mathbf{\Theta}_i \mathbf{X}_{p,i-1} + \mathbf{P}_i = \mathbf{\Theta}_i \left(\mathbf{\Theta}_{i-1} \mathbf{X}_{p,i-2} + \mathbf{P}_{i-1} \right) + \mathbf{P}_i = \cdots \tag{4.11}$$

$$\Rightarrow \mathbf{X}_{p,i} = \mathbf{\Theta}_i \mathbf{\Theta}_{i-1} \cdots \mathbf{\Theta}_1 \mathbf{X}_{p,0} + \mathbf{\Theta}_i \mathbf{\Theta}_{i-1} \cdots \mathbf{\Theta}_2 \mathbf{P}_1 + \cdots + \mathbf{\Theta}_i \mathbf{P}_{i-1} + \mathbf{P}_i. \tag{4.12}$$

In other words,

$$\mathbf{X}_{p,i} = \left(\prod_{k=1}^{i} \mathbf{\Theta}_k \right) \mathbf{X}_{p,0} + \sum_{j=1}^{i} \left(\prod_{k=j+1}^{i} \mathbf{\Theta}_k \right) \mathbf{P}_j \tag{4.13}$$

where the sequence product operator, $\Pi(\cdot)$, is defined such that the matrices are multiplied from the left as

$$\prod_{k=i}^{j} \mathbf{\Theta}_k = \mathbf{\Theta}_j \mathbf{\Theta}_{j-1} \cdots \mathbf{\Theta}_{i+1} \mathbf{\Theta}_i. \tag{4.14}$$

Additionally, in the steady state, $\mathbf{X}_{p,N}$ and $\mathbf{X}_{p,0}$ must be identical (see Figure 4.2), i.e.,

$$\mathbf{X}_{p,N} = \mathbf{X}_{p,0}. \tag{4.15}$$

Hence, $\mathbf{X}_{p,0}$, can be found as

$$\mathbf{X}_{p,0} = \left(\mathbf{I} - \prod_{k=1}^{N} \mathbf{\Theta}_k \right)^{-1} \left(\sum_{j=1}^{N} \left(\prod_{k=j+1}^{N} \mathbf{\Theta}_k \right) \mathbf{P}_j \right) = (\mathbf{I} - \mathbf{\Theta}_{tot})^{-1} \mathbf{P}_{tot}, \tag{4.16}$$

where matrices $\mathbf{\Theta}_{tot}$ and $\mathbf{P}_{tot}$ are constant predetermined matrices defined as

$$\begin{cases} \boldsymbol{\Theta}_{tot} = \prod_{k=1}^{N} \boldsymbol{\Theta}_k \\ \mathbf{P}_{tot} = \sum_{j=1}^{N} \left(\prod_{k=j+1}^{N} \boldsymbol{\Theta}_k \right) \mathbf{P}_j \end{cases}. \tag{4.17}$$

Once $\mathbf{X}_{p,0}$ is found, other $\mathbf{X}_{p,i}$s can be determined recursively as

$$\begin{cases} \mathbf{X}_{p,1} = \boldsymbol{\Theta}_1 \mathbf{X}_{p,0} + \mathbf{P}_1 \\ \mathbf{X}_{p,2} = \boldsymbol{\Theta}_2 \mathbf{X}_{p,1} + \mathbf{P}_2 \\ \quad \vdots \\ \mathbf{X}_{p,k} = \boldsymbol{\Theta}_k \mathbf{X}_{p,k-1} + \mathbf{P}_k \end{cases} \tag{4.18}$$

The propagation matrices, $\boldsymbol{\Phi}_k$, and the system matrix, $\boldsymbol{\Phi}$ in (4.2), can be found considering the evolution of the state vector in each topological instance as

$$\begin{cases} \boldsymbol{\Phi} = e^{\mathbf{A}_4 D_{e,4} T_s} e^{\mathbf{A}_3 D_{e,3} T_s} e^{\mathbf{A}_2 D_{e,2} T_s} e^{\mathbf{A}_1 D_{e,1} T_s} \\ \boldsymbol{\Phi}_1 = e^{\mathbf{A}_3 D_{e,3} T_s} e^{\mathbf{A}_2 D_{e,2} T_s} e^{\mathbf{A}_1 D_{e,1} T_s} \\ \boldsymbol{\Phi}_2 = e^{\mathbf{A}_2 D_{e,2} T_s} e^{\mathbf{A}_1 D_{e,1} T_s} \\ \boldsymbol{\Phi}_3 = e^{\mathbf{A}_1 D_{e,1} T_s} \end{cases} \tag{4.19}$$

Equation (4.19) reveals the close relationship between the propagation matrices, $\boldsymbol{\Phi}_k$, and the Floquet matrices, $\boldsymbol{\Theta}_k$ in (4.10). This relationship can be expressed as

$$\begin{cases} \boldsymbol{\Phi} = \boldsymbol{\Theta}_4 \boldsymbol{\Theta}_3 \boldsymbol{\Theta}_2 \boldsymbol{\Theta}_1 \\ \boldsymbol{\Phi}_1 = \boldsymbol{\Theta}_4 \boldsymbol{\Theta}_3 \boldsymbol{\Theta}_2 \\ \boldsymbol{\Phi}_2 = \boldsymbol{\Theta}_4 \boldsymbol{\Theta}_3 \\ \boldsymbol{\Phi}_3 = \boldsymbol{\Theta}_4 \end{cases} \tag{4.20}$$

It should be noted that the matrix exponential, $e^{\mathbf{A}_i D_{e,i} T_s}$, can be expressed in Taylor series format similar to scalar exponentials as

$$\boldsymbol{\Theta}_i = e^{\mathbf{A}_i D_{e,i} T_s} = \mathbf{I} + \mathbf{A}_i D_{e,i} T_s + \frac{\left(\mathbf{A}_i D_{e,i} T_s \right)^2}{2} + \frac{\left(\mathbf{A}_i D_{e,i} T_s \right)^3}{3!} + \cdots \tag{4.21}$$

Considering the first two terms of the matrix exponential in (4.21) results in an approximate discrete-time model.

This discrete-time modeling framework is general and can be readily applied to any multiport converter in three steps. First, the state-space matrices in each topological instance are determined ($\mathbf{A}_k$, $\mathbf{b}_k$, $\mathbf{C}_k$, and $\mathbf{d}_k$). Then, steady-state state vectors, $\mathbf{X}_{p,i}$, the propagation matrices, $\mathbf{\Phi}_k$, and the discrete-time system matrix, $\mathbf{\Phi}$, are computed using (4.18) and (4.20), respectively. Finally, the columns of the discrete-time input matrix, $\mathbf{\Gamma}$, are computed using (4.8). The resulting system matrices, $\mathbf{\Phi}$, $\mathbf{\Gamma}$, and $\mathbf{C}_1$ in (4.2) are constant and computed prior to digital-control design. Subsequently, one can find the z-domain MIMO transfer function as

$$\hat{\mathbf{Y}}(z) = \underbrace{\left(\mathbf{C}_1(z\mathbf{I}-\mathbf{\Phi})^{-1}\mathbf{\Gamma}\right)}_{\mathbf{H}(z)}\hat{\mathbf{d}}_e(z). \tag{4.22}$$

4.2 Case Studies

A two-input two-output MIMO converter shown in Figure 4.1 is considered. The circuit parameters of the MIMO converter are $V_{in,1} = 24\text{V}$, $V_{in,2} = 18\text{V}$, $D_{e,1} = 0.2$, $D_{e,2} = 0.4$, $D_{e,3} = 0.2$, $D_{\text{e},4} = 0.2$, $L = 247\mu\text{H}$, $r_L = 0.6\Omega$, $C_1 = 1201\mu\text{F}$, $r_{C_1} = 0.01\Omega$, $C_2 = 1200\mu\text{F}$, $r_{C_2} = 0.02\Omega$, $R_1 = 50\Omega$, $R_2 = 25\Omega$, $f_s = 40\text{kHz}$, $V_F(\text{diode}) = 1.1\text{V}$, $r_F(\text{diode}) = 0.03\Omega$, and $r_F(\text{MOSFET}) = 0.07\Omega$. Figure 4.3 illustrates the hardware setup. A digital signal processor (TMS320F2808), called the target computer, is employed to apply the small-signal perturbation in different effective duty cycles and sample the output voltages and the inductor current. The target computer is connected to the host computer (laptop) via a USB JTAG emulator for data acquisition and processing purposes.

Figure 4.4 illustrates the frequency responses of i_L, $v_{o,1}$, and $v_{o,2}$ to small-signal perturbations in $d_{e,1}$, predicted by the discrete-time model as well as those identified through switching-level simulations and measurements. The switching-level simulations are performed using the PLECS toolbox in MATLAB; where Fourier analysis is applied to the time-domain waveforms for each examined frequency point. The same perturbation injection and frequency sweep method is used to obtain the measured

transfer functions. A close match between the discrete-time model, switching-level simulations, and the measurement data can be seen in Figure 4.4.

The frequency responses of i_L, $v_{o,1}$, and $v_{o,2}$ to small-signal perturbations in $d_{e,2}$ and $d_{e,3}$ are considered. The proposed discrete-time model is compared with the conventional state-space average model in Figure 4.5. As seen in Figure 4.5, both discrete-time model and the average model offer acceptable results in predicting the frequency responses due to perturbations in $d_{e,2}$; however, the average model fails to accurately predict the frequency responses of magnitude, $|i_L|$, $|v_{o,1}|$, and phase, $< v_{o,1}$, due to perturbations in $d_{e,3}$. The reason that the average model cannot predict accurate results in all cases can be explained as follows.

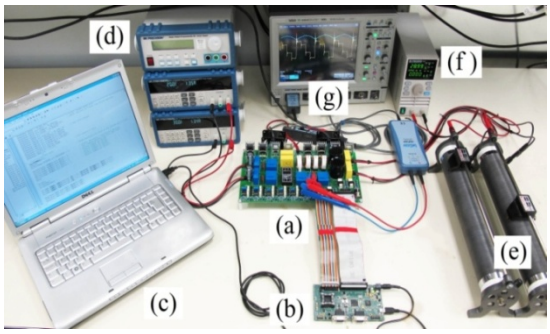

Figure 4.3 The hardware setup: (a) MIMO DC-DC converter, (b) target computer (TMS320F2808 digital signal processor), (c) host computer (laptop), (d) input sources, (e) output static loads, (f) output dynamic load, (g) oscilloscope.

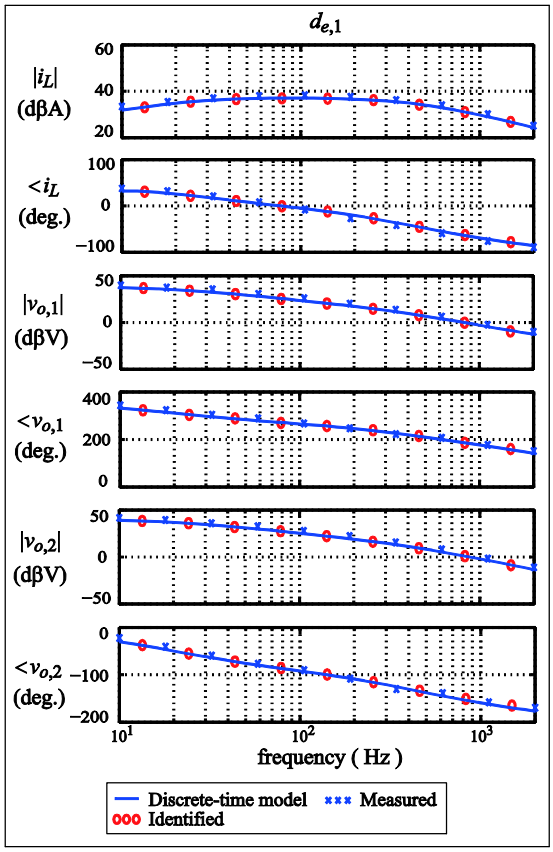

Figure 4.4 The frequency responses obtained by hardware measurements, switching-level simulations, and the discrete-time average model.

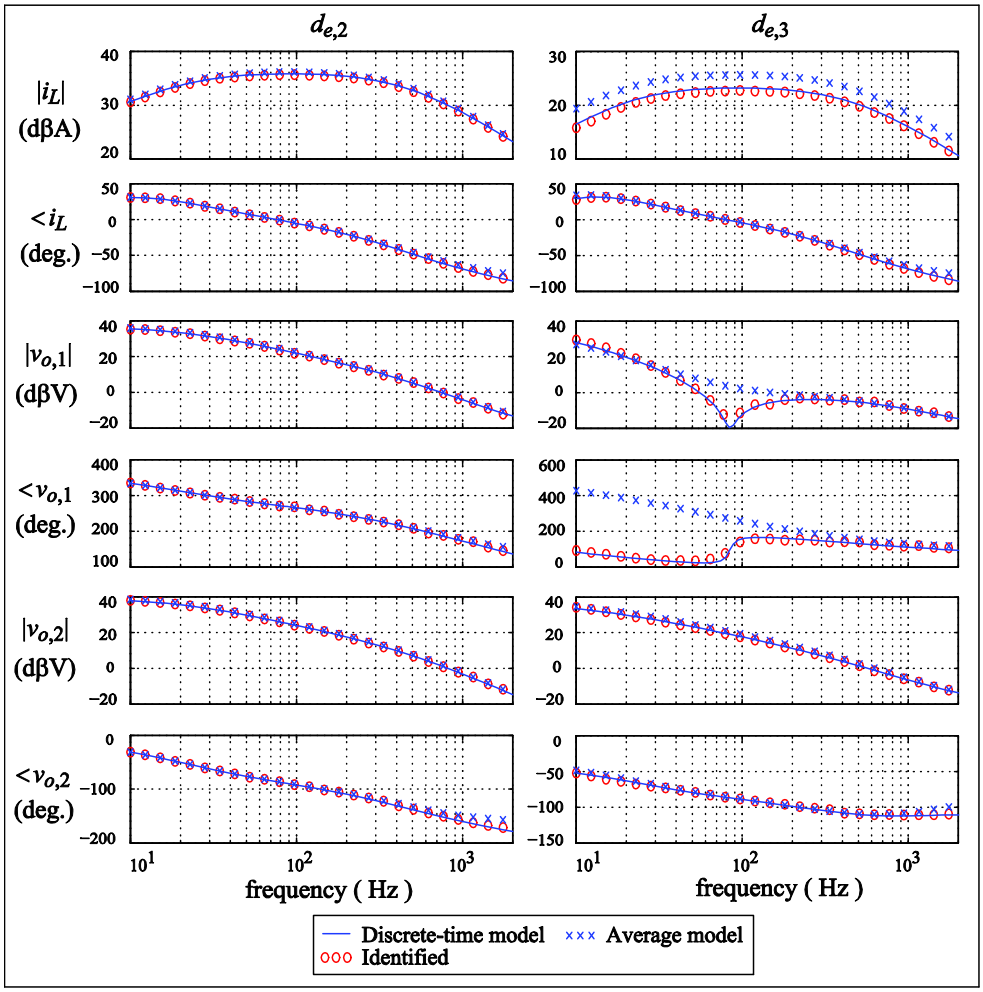

Figure 4.5 The frequency responses due to perturbations in $d_{e,2}$ and $d_{e,3}$, obtained by the discrete-time model, switching-level simulations, and the conventional average model.

In state-space averaging, the overall system matrix, $\bar{\mathbf{A}}$, is defined as the average of the system matrices pertaining to the different topological instances as follows.

$$\bar{\mathbf{A}} = d_{e,1}\mathbf{A}_1 + d_{e,2}\mathbf{A}_2 + d_{e,3}\mathbf{A}_3 + d_{e,4}\mathbf{A}_4 \tag{4.23}$$

Therefore, the system transition matrix, $\mathbf{\Phi}_{SSA}$, in one switching cycle, T_s, will be

$$\mathbf{\Phi}_{SSA} = e^{\bar{\mathbf{A}}T_s} = e^{(d_{e,1}\mathbf{A}_1 + d_{e,2}\mathbf{A}_2 + d_{e,3}\mathbf{A}_3 + d_{e,4}\mathbf{A}_4)T_s} \tag{4.24}$$

However, the exact system transition matrix, as suggested by (4.19) is

$$\mathbf{\Phi}_{DT} = e^{d_{e,4}\mathbf{A}_4 T_s} e^{d_{e,3}\mathbf{A}_3 T_s} e^{d_{e,2}\mathbf{A}_2 T_s} e^{d_{e,1}\mathbf{A}_1 T_s} \tag{4.25}$$

As opposed to the scalar exponential operator, the matrix exponential operator, $e^{(\cdot)}$, does not have the distributive property, i.e.,

$$\mathbf{\Phi}_{DT} = e^{d_{e,4}\mathbf{A}_4 T_s} e^{d_{e,3}\mathbf{A}_3 T_s} e^{d_{e,2}\mathbf{A}_2 T_s} e^{d_{e,1}\mathbf{A}_1 T_s} \neq e^{(d_{e,1}\mathbf{A}_1 + d_{e,2}\mathbf{A}_2 + d_{e,3}\mathbf{A}_3 + d_{e,4}\mathbf{A}_4)T_s} = \mathbf{\Phi}_{SSA} \tag{4.26}$$

The only case that the matrix exponential operator shows the distributed property is when

$$\mathbf{XY} = \mathbf{YX} \Rightarrow e^{\mathbf{X}+\mathbf{Y}} = e^{\mathbf{X}} e^{\mathbf{Y}} = e^{\mathbf{Y}} e^{\mathbf{X}}. \tag{4.27}$$

However, if the norm of the topological system matrices, $\{\|d_{e,1}\mathbf{A}_1 T_s\|, \|d_{e,2}\mathbf{A}_2 T_s\|, \cdots\}$, are small enough, then the system transition matrix, $\mathbf{\Phi}$, can be approximated using the Taylor series as

$$\begin{aligned} &\mathbf{\Phi}_{DT} = e^{d_{e,4}\mathbf{A}_4 T_s} e^{d_{e,3}\mathbf{A}_3 T_s} e^{d_{e,2}\mathbf{A}_2 T_s} e^{d_{e,1}\mathbf{A}_1 T_s} = \\ &\left(\mathbf{I} + d_{e,4}\mathbf{A}_4 T_s + \cdots\right)\left(\mathbf{I} + d_{e,3}\mathbf{A}_3 T_s + \cdots\right)\left(\mathbf{I} + d_{e,2}\mathbf{A}_2 T_s + \cdots\right)\left(\mathbf{I} + d_{e,1}\mathbf{A}_1 T_s + \cdots\right) \approx \\ &\mathbf{I} + \left(d_{e,1}\mathbf{A}_1 + d_{e,2}\mathbf{A}_2 + d_{e,3}\mathbf{A}_3 + d_{e,4}\mathbf{A}_4\right) \approx e^{(d_{e,1}\mathbf{A}_1 + d_{e,2}\mathbf{A}_2 + d_{e,3}\mathbf{A}_3 + d_{e,4}\mathbf{A}_4)T_s} = \mathbf{\Phi}_{SSA} \end{aligned} \tag{4.28}$$

Therefore, the state-space average model is expected to give acceptable results only when T_s is relatively small compared to the eigen values of matrices $\{d_{e,1}\mathbf{A}_1,\ d_{e,2}\mathbf{A}_2,\ d_{e,3}\mathbf{A}_3,\ d_{e,4}\mathbf{A}_4\}$, although it is not guaranteed in all cases.

The next chapter is dedicated to discrete-time model development for multiphase converters.

CHAPTER 5

DISCRETE-TIME MODELING OF MULTIPHASE CONVERTERS

Interleaved, multi-phase dc-dc converters are vastly used in microprocessor power supplies that require tight voltage regulation in the presence of drastic load transients. Digital controllers are preferred due to their less susceptibility to the noise and parameter variations, low power consumption, passive components elimination, system diagnostic, and programmability. Dynamic characterization of multiphase converters is required to extract small-signal models prior to the controller synthesis. Small-signal discrete-time models, that include time-delay effects of analog-to-digital converters and digital PWM generators, are presented in [47]. A bilinear mathematical method for discrete-time modeling of converters is studied in [42], where a new approximation of matrix exponential is used to further simplify the result. However, existing models are only suitable for single-phase converters, and there is no discrete-time model for multi-phase dc-dc converters despite their prevalent use in microprocessors power supplies. In this chapter, an accurate discrete-time model for multiphase dc-dc converters is presented.

5.1 Discrete-time Model Development

A multiphase digitally-controlled dc-dc buck converter is shown in Figure 5.1. The proposed methodology is general and applicable to all types of converters. The converter operates in continuous conduction mode with constant switching frequency and a single sampling per cycle. State-space equations describing circuit dynamics are

$$\begin{cases} \dfrac{d\mathbf{x}}{dt} = \mathbf{A}_k + \mathbf{b}_k v_{in} \\ y = \mathbf{C}_k \mathbf{x} \end{cases} \qquad k = 1, 2, \cdots, m \tag{5.1}$$

where $\mathbf{x}$ is the state vector constituting of inductor currents and capacitor voltages, $(\mathbf{A}_k,\ \mathbf{b}_k, \mathbf{C}_k)$ are system matrices corresponding to the k^{th} switching subinterval, m is the number of topologies encountered in a switching interval, and y is the output vector (considered as the output voltage here).

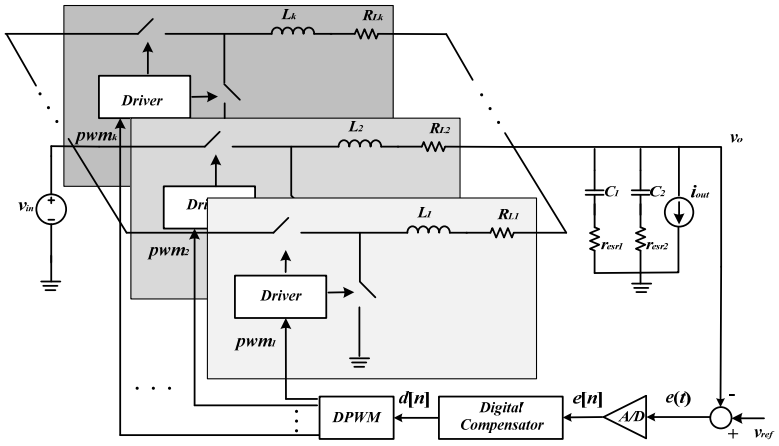

Figure 5.1 A digitally-controlled, multiphase dc-dc buck converter

The exact small-signal model is found by perturbing the state vector, $\mathbf{x}$, and duty cycles for each phase, and propagating the resulted perturbations through converter topological instances, as illustrated in Figure 5.2. The final small-signal discrete-time models should have the following form [48]

$$\begin{aligned}\hat{\mathbf{x}}[n] &= \mathbf{\Phi}\hat{\mathbf{x}}[n-1] + \boldsymbol{\gamma}\hat{d}[n-1] \\ \hat{y}[n] &= \mathbf{C}\hat{\mathbf{x}}[n]\end{aligned} \tag{5.2}$$

where $\mathbf{C}$ is the state-to-output system matrix in the first subinterval where the ADC sampling occurs. In order to extract the matrix and vector coefficients, $(\mathbf{\Phi}, \boldsymbol{\gamma})$, one can consider the effect of state and duty perturbations separately. The perturbation in previous state sample, $\hat{\mathbf{x}}[n-1]$, propagates through all topological instances in an *n*-phase converter with dynamics shown in (5.2). Thus, the matrix coefficient, $\mathbf{\Phi}$, is the product of all state transition matrices corresponding to each switching subinterval

$$\mathbf{\Phi} = e^{\mathbf{A}_1 DT_s} e^{\mathbf{A}_2 DT_s} \cdots e^{\mathbf{A}_n DT_s} e^{\bar{\mathbf{A}}(1-nD)T_s} \tag{5.3}$$

where, $(\mathbf{A}_1, \ldots, \mathbf{A}_n)$, are system matrices when the corresponding switches , $(\mathbf{q}_1, \ldots, \mathbf{q}_n)$, are on, and $\bar{\mathbf{A}}$ is the system matrix when all of the switches are off.

The perturbation in duty cycle, $\hat{d}[n-1]$, leads to a perturbation in state vector, $\hat{\mathbf{x}}_{d,k}$, at the modulation edge of the switching function at each phase, q_k, as shown in Figure 5.2. This perturbation in

state vector, $\hat{\mathbf{x}}_{d,k}$, can be calculated using linear combination of previous and current switching dynamics as

$$\begin{cases} \hat{\mathbf{x}}_{d,k} = \boldsymbol{\alpha}_k \hat{d}[n-1]T_s \\ \boldsymbol{\alpha}_k = \left(\mathbf{A}_k - \bar{\mathbf{A}}\right)\mathbf{X}_{p,k} + \left(\mathbf{b}_k - \bar{\mathbf{b}}\right)V_{in} \end{cases} \tag{5.4}$$

where, $\mathbf{X}_{p,k}$, is state vector at the falling edge of k^{th} switching function, $\mathbf{q}_k$. The resulting state perturbation in k^{th} phase, $\hat{\mathbf{x}}_{d,k}$, then propagates through remaining $(n-k)$ switching subintervals. Once this process is repeated for all n phases, one can find the vector coefficient in (5.2), $\boldsymbol{\gamma}$, as

$$\begin{cases} \boldsymbol{\gamma} = \sum_{k=1}^{n} \boldsymbol{\Phi}_k \boldsymbol{\alpha}_k T_s \\ \boldsymbol{\Phi}_k = e^{\mathbf{A}_{k+1}DT_s} e^{\mathbf{A}_{k+2}DT_s} \cdots e^{\mathbf{A}_n DT_s} e^{\bar{\mathbf{A}}\left[\frac{n-k+1}{n} - (n-k)D\right]T_s} e^{-\bar{\mathbf{A}}t_d} \end{cases} \tag{5.5}$$

where t_d is the total delay introduced by the digital controller consisting of ADC time, computational delays, and modulation delays. The final model is obtained by applying *z*-transform to (5.2).

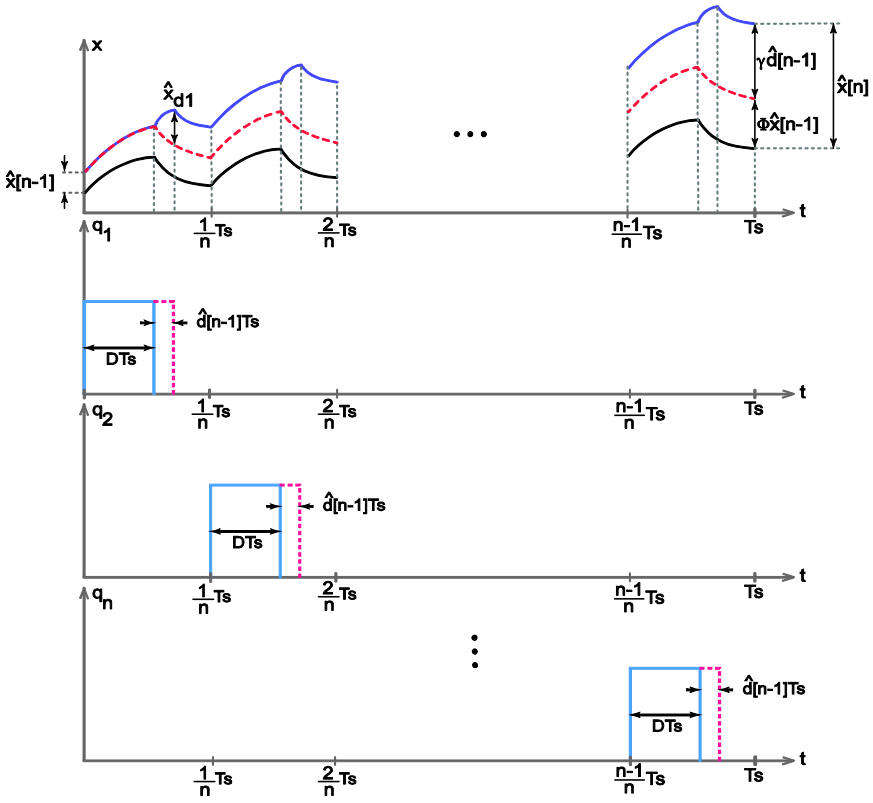

Figure 5.2 The state vector trajectory due to perturbation in duty cycle, $\hat{d}[n-1]$, and initial state vector, $\hat{\mathbf{x}}[n-1]$.

5.2 Case Studies

The proposed methodology is applied to a dual-phase, digitally-controlled buck converter with the following parameters. $V_{in} = 10\text{V}$, $V_{\text{ref}} = 1.8\text{V}$, $f_{sw} = 300\text{KHz}$, $L_1 = L_2 = 650\text{nH}$, , $R_{L_1} = R_{L_2} = 2.6\text{m}\Omega$, $C_1 = 672\mu\text{F}$, $C_2 = 2 \times 47\mu\text{F}$, $R_{C_1} = 14.4\text{m}\Omega$, $R_{C_2} = 18.0\text{m}\Omega$, $L_{C_1} = 6.5\text{nH}$, $L_{C_2} = 3.0\text{nH}$, $R_{load} = 0.225\Omega$, $R_{on} = 4.3\text{m}\Omega$, and $t_d = 450\text{ns}$. For accurate representation of the power stage, equivalent series resistors and stray inductances are obtained from the hardware prototype and considered in numerical simulation. The open loop, control-to-output transfer-function predicted by the proposed discrete-time model and conventional average-value model are shown in Figure 5.3. A satisfactory

agreement between two models is reported; however, conventional average-value model deviates at higher frequency as it does not include delay effects of digital controllers.

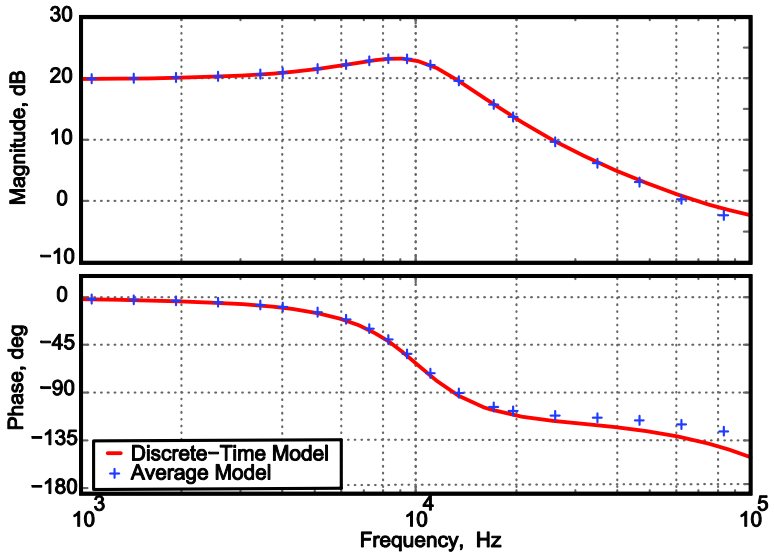

Figure 5.3 Open loop, control-to-output transfer functions predicted by the average-value model and the proposed discrete-time model.

Next, a digital PID controller, with $k_{dc} = 3500$, $f_p = 90$KHz, and $f_z = 1.2$KHz, is used to close the control loop. The loop-gain transfer-function is extracted from the experimental setup using a network analyzer. The closed-loop transfer function predicted by the proposed discrete-time model matches the experimental results, as shown in Figure 5.4, verifying model accuracy.

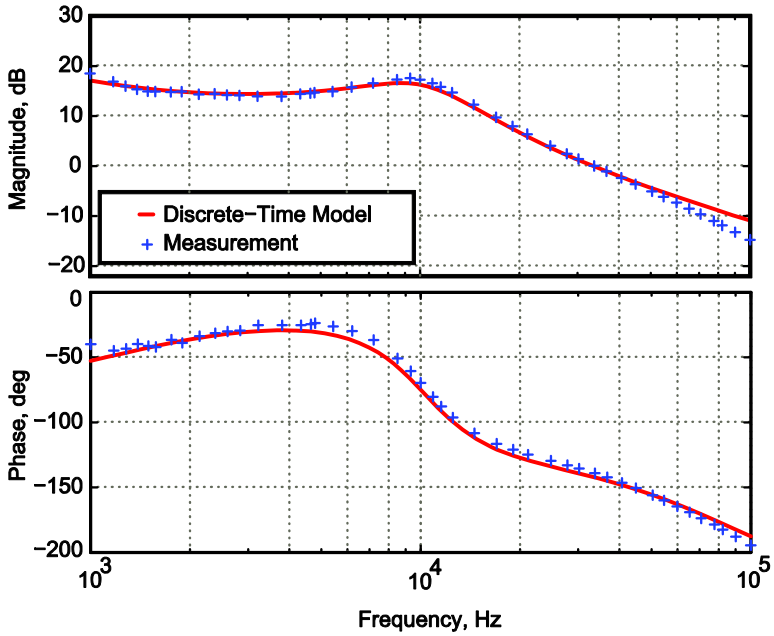

Figure 5.4 Loop-gain transfer functions predicted by the proposed model and obtained by hardware measurements

A cooperative control scheme based on distributed control of multi-agent systems is proposed for multiphase converters in the next chapter.

CHAPTER 6

COOPERATIVE CONTROL OF MULTIPHASE CONVERTERS

Modular dc-dc converters are prevalent in both front-end and point-of-load power processing units due to their numerous advantages. System wise, these advantages include increasing the reliability through structural redundancy, easing the thermal management, reducing the component stress, reducing the manufacturing cost by standardization of system components, re-configurability, and modularity. Performance wise, modular dc-dc systems allow for reducing the output voltage ripple through interleaving of the switching patterns, relaxing the requirements for input and output filters, higher efficiency, and better dynamic performance due to operation at higher frequencies.

Modular dc-dc converters can be categorized into IPOP, ISOP, IPOS, and ISOS systems [56]. The series port of the IPOS or ISOP converter is used at the high-voltage low-current side whereas the parallel port is connected to the low-voltage high-current side. IPOP or ISOS converters are useful for applications where both input and output ports are high-current or high-voltage, respectively. IPOP (or multiphase) converters are also prevalent in voltage regulators powering the modern microprocessors, where the output voltage is very low (1.1V-3.3V) and the load current is high (30A-50A) with substantial slew rates [57].

A critical challenge in multi-converter systems is balancing the stress among the constituent converters by proper current sharing at the parallel port and/or proper voltage sharing at the series port. Unbalanced voltages or currents lead to the need to overdesign the circuit elements and might even cause premature failure due to the thermal runaway in overloaded converters. If all converters are exactly identical, their currents and voltages are naturally balanced. In practice, however, these converters might not be identical due to the manufacturing tolerance of the electronic components and the inevitable parasitic elements in the circuit. Current and voltage sharing methods aim to compensate the effects of such non-idealities and ensure proper current/voltage balance among the constituent converters in the multi-module systems.

Several current and voltage sharing methods have been proposed in the literature. The current sharing methods can be categorized to droop and active-sharing schemes. In droop methods [58-61], the output voltage of individual converters droops as the load current increases. By selecting proper no-load voltage and droop slope for each converter, all converters can reach consensus on their output currents. Dc-dc converters, however, naturally have ideal voltage-source characteristics. Thus, the droop method requires implementation of a current-sharing controller that mimics the behavior of a non-ideal voltage source. Therefore, droop methods might exhibit poor voltage regulation [62]. The most well-known active-sharing methods include master-slave configuration [63-67], common duty-ratio control [68-70], digital resistive current control [71], sensorless current control [72-74], peak current-mode control [75], and cross-feedback control [76]. In master-slave configuration, the master converter regulates the output voltage while other converters try to synchronize their currents with the master. The master converter and its communication links to the slave converters are critical for proper operation of such scheme, i.e., they can be the single points of failure in the system. Therefore, master-slave configuration, although useful, undermines the system reliability. Besides, master-slave structure loses the modularity advantage because the master converter cannot be taken out. In common duty-ratio control, the same duty cycle is applied to all converters, and proper current balancing is achieved using the inherent characteristics of the employed converters. In such scheme, the resulting phase currents are different to the extent that parameters of the constituent converters are different [77]; thus, perfect current balance cannot be obtained in practice. In digital resistive current control, equal current sharing is achieved through converting the input characteristics of the converters from a negative resistance to a positive resistive load sink [71]. In sensorless current control approach, the current of each phase is estimated from the input voltage ripple information [78]. Both digital-resistive and sensorless current control schemes, although effective, are computationally intensive. In [79], the output voltage regulator is decoupled from the current sharing controller by applying elementary transformations to the Jacobian matrix of the average model. Such method gives the designer the freedom to design the output voltage regulation and current sharing loops

independently. A decentralized scheme is proposed in [80-82], where an 'active consumer agent' determines the total current reference for constituent converters, and the converters share this total current reference such that a prescribed cost function is minimized. This cost function could be, e.g., the power loss of each converter. The active consumer agent is a critical point of failure in such scheme. A general circuit theoretic classification and comparative studies of different current sharing schemes are presented in [83].

In ISOP converters, if the output currents are balanced, the input voltages will be automatically balanced (and vice versa) since the input and output powers of the constituent converters must be identical [84]. Due to such a close relationship between the input voltage and output current sharing, the distinction between the voltage and current controllers is sometimes blurred, especially in methods that obtain both through the same control strategy. A charge control method with input voltage feed forward is proposed for voltage sharing in [85]. The arithmetic average of the input voltages is used as the voltage reference in [86] to obtain proper voltage sharing. A three-loop control scheme, consisting of an output-voltage regulation loop, an input-voltage sharing loop, and a current sharing loop is proposed for ISOP inverters in [86, 87].

Although several control strategies have been proposed for stress sharing (i.e., current sharing) in modular dc-dc converters, not much attention has been given to how the choice of the communication structure among converters can affect the stability and the performance measures of such systems (e.g. fault tolerance, plug and play ability, etc.). In this chapter, the problem of stress sharing is approached from the point of view of cooperative control in multi-agent systems, where each converter represents a node (agent) on a directed communication graph that represents the information flow among the converters. The concept of cooperative multi-agent systems is inspired by the synchronization phenomena observed in the nature (e.g., flocking in birds, swarming in insects, and schooling in fish), where each agent is only allowed to exchange information with some neighbor agents according to a prescribed communication graph [88-91]. In this chapter, IPOP converters are considered for the purpose

of the discussion. The proposed approach, however, is general and can be applied to ISOP, IPOS, and ISOS converters as well. The contributions of this chapter can be summarized as follows.

- The proposed cooperative control method is truly modular and can realize a plug-and-play environment in both cyber and physical domains, where any converter can be added to or removed from an existing structure without disrupting the system operation.
- System reliability is greatly improved. As opposed to the master-slave configuration where the master converter and its communication links with the slave converters are the reliability bottlenecks, there is no single point-of-failure in this cooperative framework. For example, even if a communication link or a converter fails, the cooperative system can still balance the currents through other links as long as the communication graph has certain basic properties. Such properties are identified and studied.
- Using the cooperative control scheme, the designer is free to choose the proper communication graph (e.g. star, linear, gossip-ring). Each graph has specific fault-tolerance characteristics and requires certain communication resources. For instance, gossip rings require minimum communication resources but are the most vulnerable to failure. On the other hand, complete graphs have the highest reliability since they have the most number of edges, but they require maximum communication resources. The effects of the choice of the communication graph on the system reliability and stability are discussed.

The rest of this chapter is organized as follows. Section 6.1 describes the preliminaries of graph theory and multi-agent systems. Section 6.2 describes the proposed cooperative multi-agent control scheme. Several case studies are presented in section 6.3 to verify the performance of the proposed method.

6.1 Dynamic Systems on Graphs

Each converter can be considered as a node in a directed communication graph (digraph). This communication graph determines the information flow among converters [92, 93]. Node i can receive the information from node j if there is a directed edge from node j to i. Assuming N nodes, the

communication graph can be represented by an adjacency matrix, $\mathbf{A}_{N\times N} = [a_{ij}]$, with $a_{ij} = 1$ if there is a directed edge from node j to i, otherwise, $a_{ij} = 0$. The edge weights (a_{ij}) are assumed to be either 0 or 1 for simplicity; however, they can be any nonnegative real number in general. The in-degree of the node i, d_i, is defined as the number of the edges having node i at the receiving end. The neighbor nodes set of node i, N_i, is defined as the set of all nodes that pin to node i. The graph in-degree matrix, $\mathbf{D}_{N\times N}$, is a diagonal matrix whose diagonal entries are the in-degrees of the corresponding nodes in the communication graph. The sum of the entries of the kth row in matrix $\mathbf{A}$ equals to the number of edges having node k as a head. Therefore, the in-degree of each node is equal to the corresponding row sum in matrix $\mathbf{A}$. The graph Laplacian matrix is defined as $\mathbf{L}_{N\times N} = \mathbf{D}_{N\times N} - \mathbf{A}_{N\times N}$.

Figure 6.1(a-c) illustrates a few possible communication graphs for the modular converter system. It is customary to remove the arrows of the bidirectional edges. A digraph is said to be connected if there is at least one directed path between every two arbitrary nodes. A spanning tree is a tree that includes all the nodes in the digraph. Each node can obtain the information from a few neighbor nodes. If the communication graph has a spanning tree, such information can be shown to be sufficient to reach consensus among all the converters. In other words, there is no need for a centralized controller that has access to the information of all nodes.

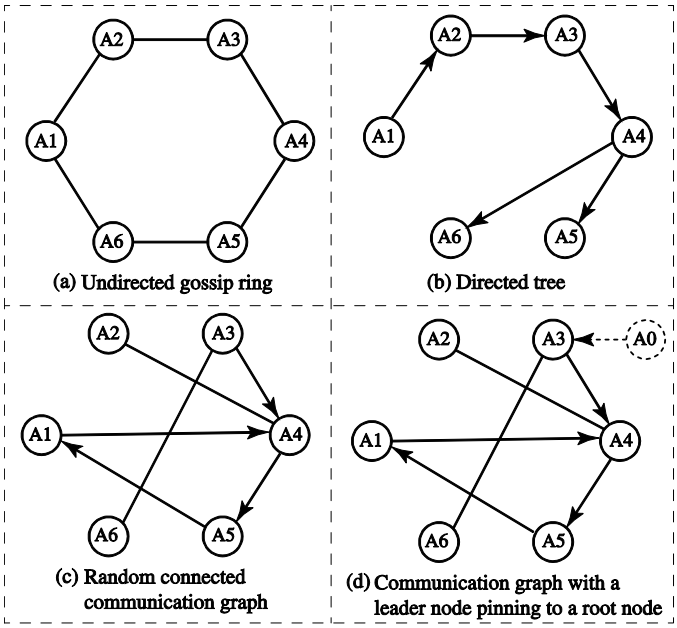

Figure 6.1 Modular converters on communication graphs: (a) an undirected gossip ring, (b) a directed tree, (c) a random graph, and (d) a connected graph with a leader node.

In cooperative tracking, an abstract leader node is considered that, as opposed to the other nodes, does not correspond to a physical converter. The leader node pins to a few nodes in the communication graph and has independent dynamics. The leader node is not a reliability bottleneck since it is not a physical converter. For instance, the leader node can simply be the reference output voltage information, which some follower nodes know. Node i is called a root node if the communication graph has a spanning tree whose root node is node i. Figure 6.1(d) depicts a connected communication graph with a leader node, A0, pinning to a root node, A3. It can be shown that if the leader node pins to a root node, all nodes will be synchronized with the leader node's dynamics in steady state [94, 95]. The pinning gains matrix, $\mathbf{G}_{N\times N}$, is a diagonal matrix defined as $\mathbf{G}$ =diag$\{g_i\}$ where g_i is the weight of the pinning edge from the leader node to node i. Considering that the leader node does not need to pin to all the follower nodes to reach consensus, the pinning gain matrix, $\mathbf{G}$, is usually a sparse diagonal matrix.

6.2 Cooperative Current Synchronization

IPOP converters are considered here for the purpose of the discussion, although the proposed control method is general and can be applied to ISOP, IPOS, and ISOS converters as well. Figure 6.2 depicts the schematic of a IPOP system in a cyber-physical structure. The physical layer represents the converters and their dynamics whereas the cyber layer determines the information flow among the converters. The leader node in the cyber layer, A0, represents the voltage reference information, which some of the converters know. All converter units share the same output capacitor. The objective is to obtain a control scheme that balances the currents of all converters, regulates the output voltage, does not need a centralized controller, and is able to operate uninterruptedly whenever a converter is taken out or brought into the system. Upon failure of a converter, it can be automatically isolated and other converters can compensate for the lost current capacity by supplying more current. Of course, the maximum current handling capability of the converters should be taken into account in such cases.

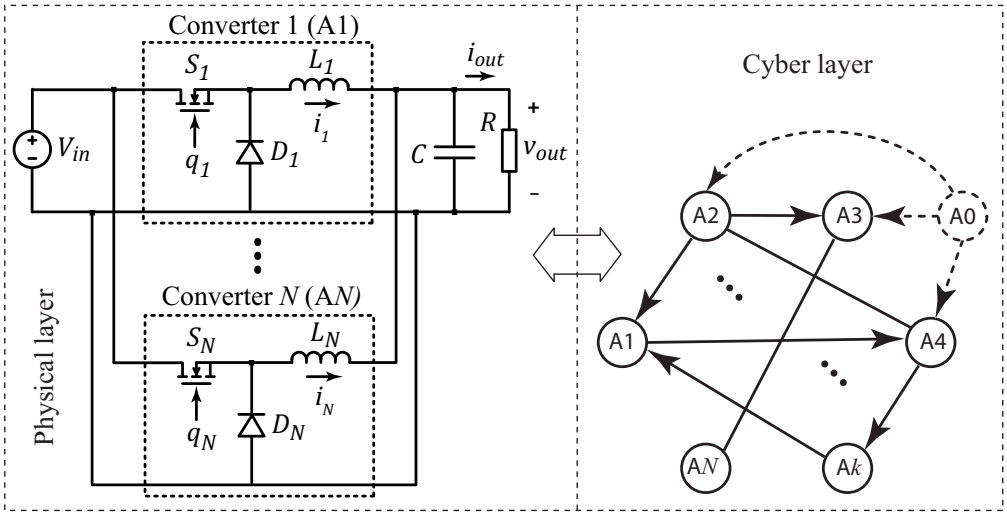

Figure 6.2 IPOP buck converters in a cyber-physical structure.

6.2.1 Average Model

The time-invariant dynamic model of the IPOP system is required to design the cooperative controller; such model can be found using the conventional SSA techniques as follows [96].

$$\begin{cases} L_k \dfrac{d\langle i_k \rangle}{dt} = V_{in}\mu_k - \langle v_o \rangle, \quad k = 1, \cdots, N \\ C \dfrac{d\langle v_{out} \rangle}{dt} = -\dfrac{\langle v_{out} \rangle}{R} + \langle i_1 \rangle + \langle i_2 \rangle + \cdots + \langle i_N \rangle \end{cases} \tag{6.1}$$

where L_k, C, R, and V_{in} are the circuit parameters shown in Figure 6.2, $\langle \cdot \rangle$ is the moving-average operator, and μ_k is the duty cycle of the kth converter. The switching frequency is assumed to be much faster than the converter dynamics for the average model to be accurate. The moving-average operator, $\langle \cdot \rangle$, is dropped hereafter for brevity; all the variables denote their averages over a switching cycle.

6.2.2 Agent Dynamics

Figure 6.3 illustrates the block diagrams of the control schemes embedded in the microcontrollers of the agents. Those agents that are connected to the leader node participate in the voltage regulation (Figure 6.3(a)); they are called group I hereafter. Those agents that are not connected to the leader node only try to synchronize their currents with the other agents (Figure 6.3(b)); they are called group II hereafter. The agents in group II do not need voltage sensor, which can reduce the cost of the system. The voltage PID controller, $H_1(s)$, employed in the control schemes of the agents in group I, can be described as

$$i_{\text{ref}} = k_{p1}\left(V_{\text{ref}} - v_{out}\right) + k_{i1}\int_0^t \left(V_{\text{ref}} - v_{out}\right) dt + k_{d1}\frac{d}{dt}\left(V_{\text{ref}} - v_{out}\right). \tag{6.2}$$

where k_{p1}, k_{i1}, and k_{d1} are the corresponding proportional, integral, and derivative coefficients of $H_1(s)$, respectively.

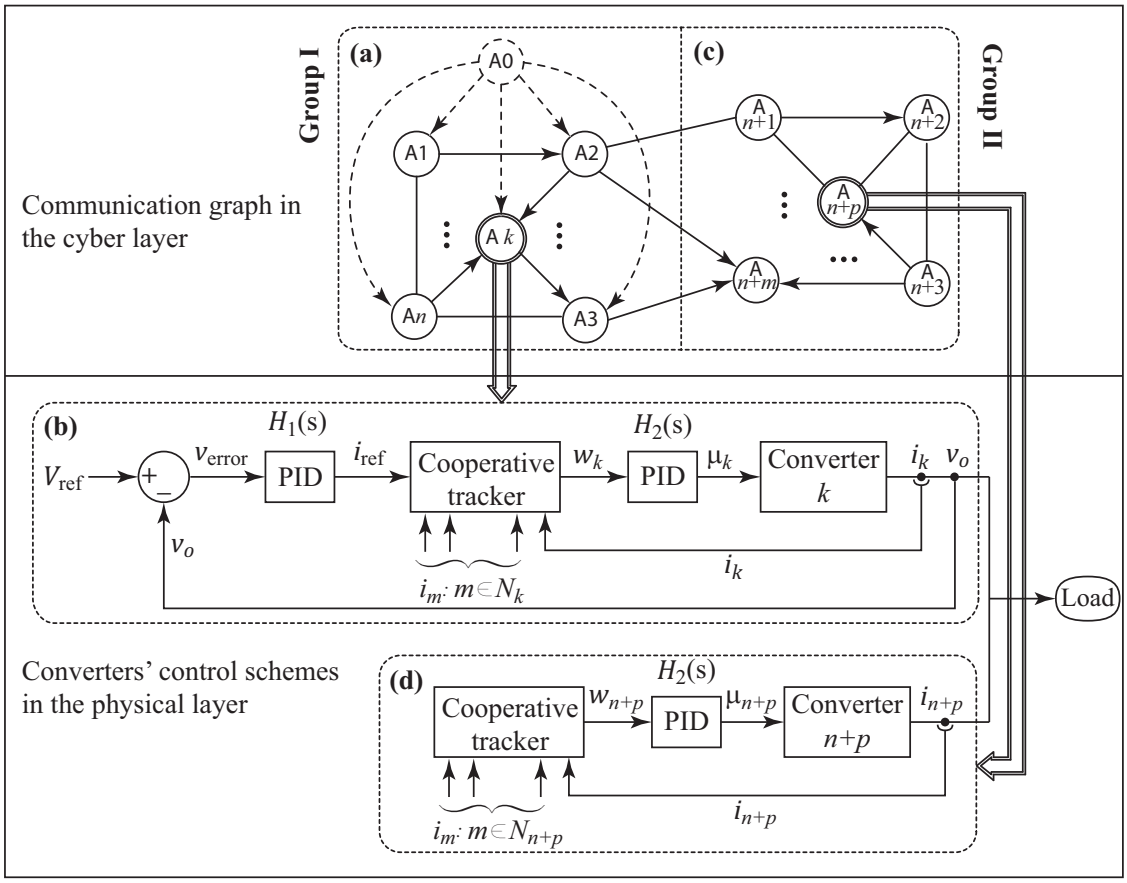

Figure 6.3 The proposed cyber-physical structure for the IPOP system: (a) the converters that know the voltage reference, (b) their control schemes, (c) the converters that do not know the voltage reference, and (d) their control schemes.

The output of the PID voltage controller, $H_1(s)$, is the reference current, i_{ref}, to which the kth converter is desired to synchronize. This reference current is fed to the cooperative tracker block governed by the following democratic voting protocol.

$$w_k = \sum_{m \in N_k} a_{km}\left(i_m - i_k\right) + g_k\left(i_{\text{ref}} - i_k\right) \tag{6.3}$$

where a_{km}s are the entries of the adjacency matrix of the communication graph, $\mathbf{A}$, g_ks are the pinning gains which are the diagonal entries of the graph pinning gain matrix, $\mathbf{G}$, and N_k is the set of the neighbor nodes of the node k. According to the voting protocol in (6.3), each node tries to synchronize its current

with those of the neighbor nodes and the leader (i_{ref}). For the nodes in group I, $g_k = 1$, whereas $g_k = 0$ for the nodes in group II. The cooperative control protocol described in (6.3) can be expressed as

$$w_k = -i_k \sum_{m \in N_k} a_{km} + \sum_{m \in N_k} a_{km} i_m + g_k i_{\text{ref}} - g_k i_k . \tag{6.4}$$

The term $\sum_{m \in N_k} a_{km}$ is the row sum of the kth row in the graph adjacency matrix, $\mathbf{A}$, which is equal to the in-degree of node k, d_k. Hence,

$$w_k = -\left(d_k + g_k\right) i_k + g_k i_{\text{ref}} + \sum_{m \in N_k} a_{km} i_m \tag{6.5}$$

As demonstrated by (6.5), only the information of the neighbor nodes of each node, N_k, is required in the proposed scheme, and the information flow is determined by the communication graph through a_{km} $\{m \in N_k\}$.

Equation (6.5) can be expressed in the matrix format by aggregating all currents to a single current vector as

$$\mathbf{I} = [i_1 \quad i_2 \quad \cdots \quad i_N]^T . \tag{6.6}$$

Considering (6.6), it can be shown that (6.5) is equivalent to

$$\mathbf{W} = -(\mathbf{D} + \mathbf{G})\mathbf{I} + \mathbf{G}\mathbf{I}_{\text{ref}} + \mathbf{A}\mathbf{I} \tag{6.7}$$

where $\mathbf{I}_{\text{ref}} = [i_{\text{ref}} \quad \cdots \quad i_{\text{ref}}]^T$. Therefore,

$$\mathbf{W} = -(\mathbf{D} - \mathbf{A})\mathbf{I} + \mathbf{G}(\mathbf{I}_{\text{ref}} - \mathbf{I}) = -\mathbf{L}\mathbf{I} + \mathbf{G}(\mathbf{I}_{\text{ref}} - \mathbf{I}) \tag{6.8}$$

where $\mathbf{L}$ is the graph Laplacian matrix defined in section 6.1. Since the summation of the entries in each row of $\mathbf{A}$ is equals to the corresponding diagonal entry in $\mathbf{D}$ and, $\mathbf{L} = \mathbf{D} - \mathbf{A}$, the row sum of $\mathbf{L}$ is always zero. In other words,

$$\mathbf{L}\begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}^T = \mathbf{0} \rightarrow \mathbf{L}\mathbf{I}_{\text{ref}} = \mathbf{0} \tag{6.9}$$

Hence, one can express (6.8) as

$$\mathbf{W} = \mathbf{L}\mathbf{I}_{\text{ref}} - \mathbf{L}\mathbf{I} + \mathbf{G}(\mathbf{I}_{\text{ref}} - \mathbf{I}) = (\mathbf{L} + \mathbf{G})(\mathbf{I}_{\text{ref}} - \mathbf{I}). \tag{6.10}$$

The output of the cooperative tracker, w_k, goes to the current controller, $H_2(s)$, to generate the required duty cycle, μ_k:

$$\mu_k = k_{p2} w_k + k_{i2} \int_0^t w_k dt + k_{d2} \frac{dw_k}{dt} \tag{6.11}$$

6.2.3 Global Dynamics

To evaluate the stability and dynamic performance of the proposed cooperative control scheme, the global dynamic model of the system should be determined. It is desired that the steady-state value of the output voltage, v_{out}, be the same as the reference voltage, V_{ref}. Besides, the current of all converters, i_ks, must be identical in the steady state. The differential equation governing the PID voltage and current controllers, $H_1(s)$ and $H_2(s)$, can be expressed in the general form of

$$y = k_p x + k_i \int_0^t x dt + k_d \frac{dx}{dt} \tag{6.12}$$

where x and y are the input and output of the PID controller, respectively. Assuming that the system is stable, (6.12) forces the steady-state value of x, denoted by X, to be zero ($X = 0$). If $X \neq 0$ in the steady state, the integral term in (6.12) keeps integrating x and, thus, y changes. Change in y means that the steady-state condition has not been reached yet. Thus, the input of both PID controllers should be zero in the steady state.

Setting the input of the PID voltage controller (6.2) to zero in the steady state, one may find

$$V_{\text{error}} = 0 \rightarrow V_{\text{out}} = V_{\text{ref}} \tag{6.13}$$

Thus, the output voltage is properly regulated, provided that the system is stable. Similarly, setting the input of the PID current controller, $H_2(s)$, to zero in (6.11), one may find

$$\mathbf{W} = \mathbf{0} \rightarrow (\mathbf{L} + \mathbf{G})(\mathbf{I}_{\text{ref}} - \mathbf{I}) = \mathbf{0} \tag{6.14}$$

It can be shown that the matrix $(\mathbf{L} + \mathbf{G})$ is invertible if the corresponding communication graph has a spanning tree and the leader node pins to the root node of that tree [91, 94]. It should be noted that

since the row sum of $\mathbf{L}$ is zero, its null space is all the vectors of the form $r[1 \quad \cdots \quad 1]^T$, where r is a real number. Since the null space of $\mathbf{L}$ is nonzero, $\mathbf{L}$ is not invertible; however, the null space of $(\mathbf{L}+\mathbf{G})$ is always zero if the graph has a spanning tree and the leader pins to the root node of that spanning tree. In such cases, all currents will be identical and equal to the reference current in the steady state since

$$\left(\mathbf{I}_{\text{ref}} - \mathbf{I}\right) = \left(\mathbf{L}+\mathbf{G}\right)^{-1}\mathbf{0} = \mathbf{0} \rightarrow \mathbf{I} = \mathbf{I}_{\text{ref}} \rightarrow i_k = i_{\text{ref}}. \tag{6.15}$$

To construct the global dynamic model, the transfer function matrix from the duty cycles to the converter currents, $\mathbf{G}_{id}(s)$, and the transfer function vector from the duty cycles to the output voltage, $\mathbf{G}_{vd}(s)$, are required. Taking Laplace transform of (6.1), one may find

$$\begin{cases} sL_k I_k(s) = V_{in}M_k(s) - V_{out}(s) \\ sCV_{out}(s) = -\dfrac{V_{out}(s)}{R} + I_1(s) + I_2(s) + \cdots + I_N(s) \end{cases}. \tag{6.16}$$

where $M_k(s)$ is the Laplace transform of $\mu_k(t)$, the duty cycle. Equation (6.16) describes a system of $N+1$ coupled differential equations with the $M_k(s)$ as the system inputs and $I_1(s), \cdots, I_N(s)$, $V_{out}(s)$ as the outputs. The Kron reduction technique [97] can be used to eliminate the row corresponding to $V_{out}(s)$. The result would be

$$\mathbf{\Gamma}\underbrace{\begin{bmatrix} I_1(s) \\ I_2(s) \\ \vdots \\ I_N(s) \end{bmatrix}}_{\mathbf{I}(s)} = \underbrace{\begin{bmatrix} M_1(s) \\ M_2(s) \\ \vdots \\ M_N(s) \end{bmatrix}}_{\mathbf{M}(s)} V_{in} \tag{6.17}$$

where

$$\mathbf{\Gamma} = \begin{bmatrix} sL_1 + \dfrac{R}{1+RCs} & \dfrac{R}{1+RCs} & \cdots & \dfrac{R}{1+RCs} \\ \dfrac{R}{1+RCs} & sL_2 + \dfrac{R}{1+RCs} & \cdots & \dfrac{R}{1+RCs} \\ \vdots & \ddots & \ddots & \vdots \\ \dfrac{R}{1+RCs} & \dfrac{R}{1+RCs} & \cdots & sL_N + \dfrac{R}{1+RCs} \end{bmatrix}. \tag{6.18}$$

Therefore,

$$\mathbf{I}(s) = \mathbf{\Gamma}^{-1} V_{in} \mathbf{M}(s) = \mathbf{G}_{id}(s)\mathbf{M}(s) \rightarrow \mathbf{G}_{id}(s) = \mathbf{\Gamma}^{-1} V_{in}. \tag{6.19}$$

The transfer function vector $\mathbf{G}_{vd}(s)$ can then be found using (6.16) as follows.

$$\begin{aligned} V_{out}(s) &= \frac{R}{1+RCs}\left(I_1(s) + \cdots + I_N(s)\right) = \\ &\frac{R}{1+RCs}\left(\begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix} \cdot \mathbf{I}(s)\right) = \\ &\frac{R}{1+RCs}\left(\begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix} \cdot \mathbf{G}_{id}(s)\mathbf{M}(s)\right) \end{aligned} \tag{6.20}$$

Hence,

$$\mathbf{G}_{vd}(s) = \frac{R}{1+RCs}\begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}\mathbf{G}_{id}(s) = \frac{R}{1+RCs}\begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}\mathbf{\Gamma}^{-1} V_{in} \tag{6.21}$$

The block diagram of the global dynamic model is depicted in Figure 6.4 for a general communication graph with graph adjacency matrix $\mathbf{A}$ and pinning gain matrix $\mathbf{G}$. There are two control loops, namely, the inner current control loop and the outer voltage control loop. Both loops should be stable. The inductor current of a buck converter is usually a fast state variable whereas the output capacitor voltage is the slow state variable. Thus, designing the cascaded loops, such that the inner loop regulates the inductor currents while the outer loop regulates the output voltage, is preferred. The inner loop can be modeled as a transfer function matrix $\mathbf{H}_c(s)$, where

$$\mathbf{M}(s) = \mathbf{H}_c(s)\mathbf{I}_{\text{ref}} \tag{6.22}$$

Considering the system block diagram in Figure 6.4, $\mathbf{H}_c(s)$ can be expressed as

$$\mathbf{H}_c(s) = \left(\mathbf{I} + \underbrace{H_2(s)\left(\mathbf{L}+\mathbf{G}\right)\mathbf{G}_{id}(s)}_{\mathbf{G}_{L1}(s)}\right)^{-1} H_2(s)\left(\mathbf{L}+\mathbf{G}\right). \tag{6.23}$$

Therefore, the loop gain of the inner current control loop, denoted by $\mathbf{G}_{L1}(s)$ is

$$\mathbf{G}_{L1}(s) = H_2(s)\left(\mathbf{L}+\mathbf{G}\right)\mathbf{G}_{id}(s). \tag{6.24}$$

By proper tuning of the PID current controller, $H_2(s)$, and assigning the proper communication graph, $\mathbf{L}+\mathbf{G}$, the bandwidth of the inner current control loop, with the loop gain $\mathbf{G}_{L1}(s)$, can be tuned. This bandwidth, as mentioned, should be high enough to ensure fast response of the current control loop.

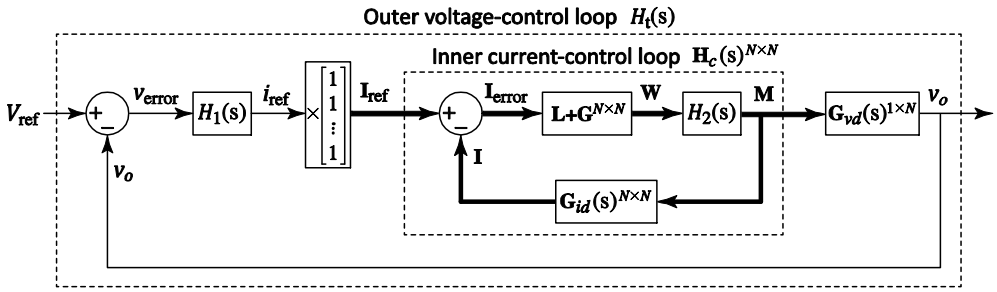

Figure 6.4 Global dynamic model for an arbitrary graph with adjacency matrix, **L**, and pinning gain matrix, **G**.

Similarly, the outer voltage control loop can be described by the scalar transfer function $H_t(s)$, where

$$V_{out}(s) = H_t(s)V_{\text{ref}}. \tag{6.25}$$

Considering the block diagram of the system in Figure 6.4, $H_t(s)$ can be expressed as

$$H_t(s) = \left(\underbrace{1 + \mathbf{G}_{vd}(s)\mathbf{H}_c(s)\begin{bmatrix}1\\ \vdots \\ 1\end{bmatrix} H_1(s)}_{\mathbf{G}_{L2}(s)} \right)^{-1} \times \left(\mathbf{G}_{vd}(s)\mathbf{H}_c(s)\begin{bmatrix}1\\ \vdots \\ 1\end{bmatrix} H_1(s) \right) \tag{6.26}$$

Therefore, the loop gain of the outer voltage control loop, $G_{L2}(s)$, would be

$$G_{L2}(s) = \mathbf{G}_{vd}(s)^{1\times N}\mathbf{H}_c(s)^{N\times N}\begin{bmatrix}1\\ \vdots \\ 1\end{bmatrix} H_1(s) \tag{6.27}$$

By proper tuning of the PID voltage controller, $H_1(s)$, the bandwidth of the outer voltage-control loop can be properly adjusted to be lower than that of the inner current control loop. Stability of the system can

be assessed using the well-known linear system methods (e.g., the root locus method ([98]) for $G_{L1}(s)$ and $G_{L2}(s)$.

6.3 Case Studies

6.3.1 Hardware Setup

Three laboratory-scale buck converters are implemented in an IPOP configuration. Figure 6.5 depicts the hardware setup. Interleaved switching patterns are used to reduce the output voltage ripple. The circuit parameters are as follows. $V_{\text{in}} = 24\text{V}$, $V_{\text{out}} = 18\text{V}$, $L_1 = L_2 = L_3 = 100\mu\text{H}$, $C = 2200\mu\text{F}$, $f_{sw} = 40\text{kHz}$, $R = 2\Omega$. The bandwidths of the inner and outer loops are 2kHz and 100Hz, respectively. Without loss of modularity, the control algorithms of all converters are embedded in a single DSP to simplify the development of the hardware prototype. The employed DSP is TMS320F2808, which has 16 channels of ADC and 12-bit built-in ADCs. The ultra-fast ADCs (80ns conversion time) of this DSP keep the combined conversion and computation times for all converters below one switching cycle (25μs for f_{sw}=40kHz). Therefore, the controller delay is limited to 25μs, which results in a better resemblance between the developed analytical model and the implemented hardware. The DSP (target computer) is connected to the host computer (laptop) for programming and monitoring purposes. As a default, the converters communicate through a gossip ring and they all participate in the output voltage regulation (they are all connected to the leader), unless otherwise specified.

6.3.2 Startup Response and Steady-state Operation

Figure 6.6 illustrates the measured startup response of the IPOP converter. As seen in Figure 6.6(a and b), the current averages are not equal in the beginning due to the mismatch between the actual circuit parameters of the individual converters; however, the cooperative control algorithm manages to balance the currents and regulate the output voltage, simultaneously. The output voltage, v_{out}, rises smoothly and does not overshoot. The steady-state current waveforms of all converters are shown in Figure 6.6(c). The measured i_1 in Figure 6.6(c) has more high-frequency noise content compared to i_2

and i_3 since the nominal current rating of the current probe used for measuring i_1 is 150A, which is much higher than the actual measured current (3A). The current ratings of the current probes used for measuring i_2 and i_3 are both 30A; they show less noise content as seen in Figure 6.6(c).

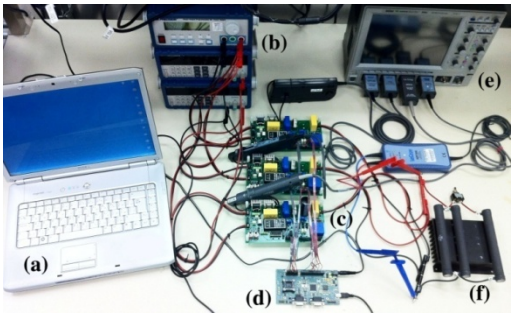

Figure 6.5 Hardware setup: (a) host computer (laptop), (b) power supplies, (c) parallel converters, (d) target computer (TMSF2808 DSP), (e) oscilloscope, (f) output loads.

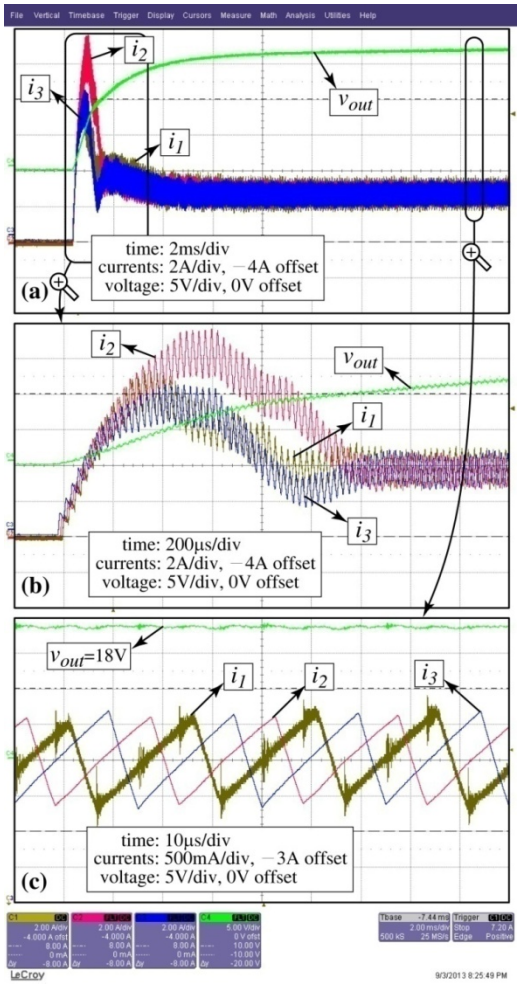

Figure 6.6 Startup response and steady-state waveforms of the IPOP converter: (a) Startup response, (b) zoomed-in view of the startup response, (c) steady-state waveforms.

6.3.3 Fault Tolerance

Two different fault categories can be considered, namely, converter failure and communication link failure. The former pertains to the faults in the physical layer whereas the latter pertains to the cyber-layer faults. When a converter fails, the FDIR mechanism [99] isolates the failed converter and reconfigures the communication graph, if necessary, based on the existing communication resources. When a communication link fails, the system can operate uninterruptedly if the new graph is still connected and has at least one spanning tree with the leader node spinning to the root node of that tree.

Otherwise, the system loses the current synchronization, although output voltage regulation remains intact. To ensure fault-tolerant operation of the system, existence of the FDIR mechanism is necessary in the case of a converter failure but not required in the case of communication link failure. The output load is set at 3Ω for the following fault tolerance studies.

6.3.3.1 Converter Failure

Figure 6.7 depicts the system performance in the case of failure in converter 1. The failure is simulated through the DSP code by disabling the PWM generator module pertaining to converter 1. The remaining converters are simultaneously put in a gossip ring by the FDIR mechanism. As seen in Figure 6.7, the cooperative control scheme manages to compensate for the failure of converter 1 by increasing the reference current of the remaining converters, while maintaining proper output voltage regulation.

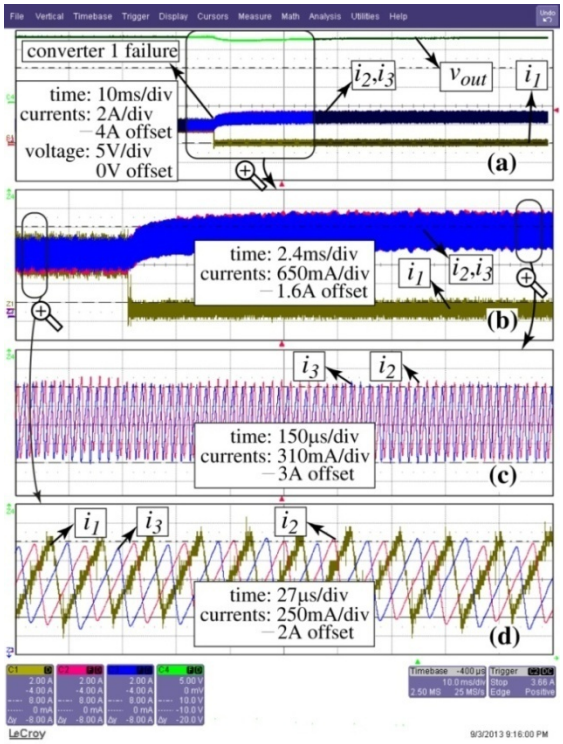

Figure 6.7 System response to the failure of converter 1: (a) converter waveforms, (b) zoomed-in view of current waveforms, (c) currents waveforms after failure, (d) current waveforms before failure.

6.3.3.2 Communication Link Failure

After failure of one or more communication links, the system can operate uninterruptedly if the remaining graph still has a spanning tree with the leader node pinning to the root of that tree. For instance, consider directed and undirected gossip rings as shown in Figure 6.8(a and b), respectively. The leader, first, second, and third agents are denoted by A0, A1, A2, and A3, respectively. In the directed ring, if the link e_{31} fails, there is still one spanning tree, but, the leader node does not pin to the root node of that spanning tree (A1). Therefore, the current synchronization is lost since the information of the leader node cannot propagate to A1 and A2. As a result, the current of both A1 and A2 will drop to zero while A3 catches the total load current. On the other hand, in the undirected graph in Figure 6.8(b), even if e_{31} fails, there is still a spanning tree with the root node A3, to which the leader node pins. Hence, the system is fault tolerant and continues normal operation. Obviously, improved fault tolerance comes at the price of increasing the communication resources since each converter should have two receivers and two transmitters in the undirected graph whereas only one transmitter and one receiver is needed for each converter in the directed graph.

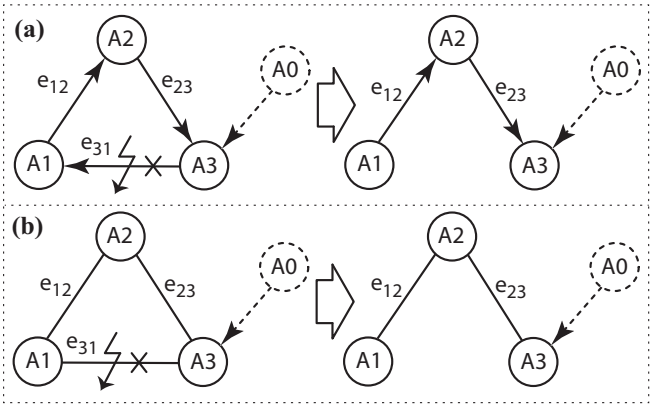

Figure 6.8 Failure of the link e_{31} in a gossip ring with the leader node pinning to the third agent (A3): (a) directed gossip ring, (b) undirected gossip ring.

Existence of a directed edge from the leader to an agent implies that that agent participates in the output voltage regulation, i.e., that agent is in group I (see Figure 6.3). However, it is not necessary that

all of the converters participate in the output voltage regulation (being connected to the leader). In the converters of group II, the control scheme only has a cooperative current sharing loop depicted in Figure 6.3(d). The system can reach consensus if at least one root node participates in the output voltage regulation, for instance A3 in Figure 6.8(b).

Figure 6.9 illustrates the measured response of the cooperative control scheme employing the undirected gossip ring (Figure 6.8(b)) to the failure in communication link e_{31}. As shown in Figure 6.9, no significant transients are seen after the failure and the system maintains its current synchronization as well as output voltage regulation.

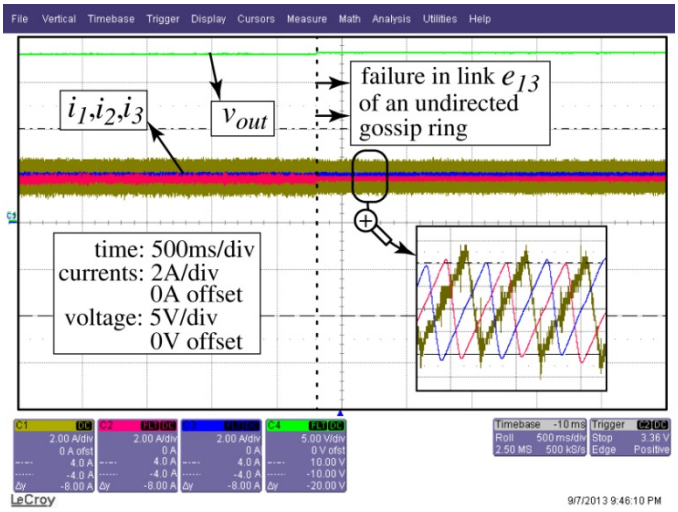

Figure 6.9 System response to the failure of communication link e_{31} using an undirected gossip ring with the leader node pinning to the third agent (Figure 6.8(b)).

Figure 6.10, on the other hand, depicts the system response when the directed gossip ring (Figure 6.8(a)) is employed. As seen in Figure 6.10, the converters lose their consensus on the current; the currents of converters 1 and 2 drops to zero, and converter 3 carries the total current instead. Significant voltage transients are also reported as seen in Figure 6.10.

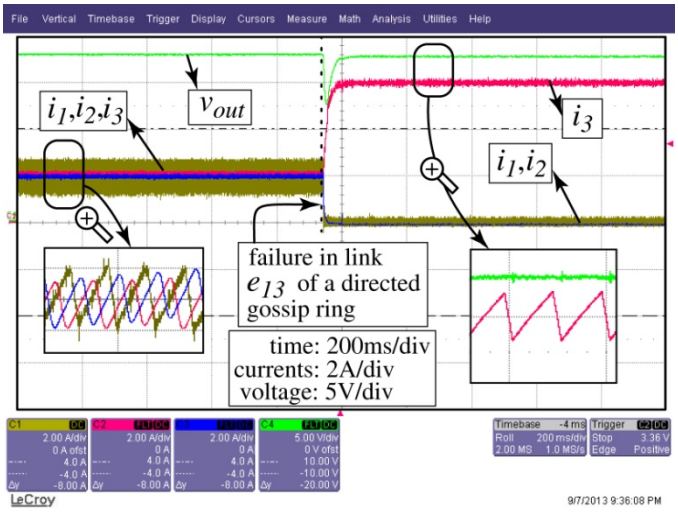

Figure 6.10 System response to the failure of communication link e_{31} using a directed gossip ring with the leader node pinning to the third agent (Figure 6.8(a)).

6.3.4 Plug-and-play Capability

The proposed cooperative control scheme can accommodate a plug and play environment so that new converters can be augmented to the system and become automatically synchronized with the other converters. For instance, the new converter can get the information from only one of the existing converters. Obviously, if the existing graph has a spanning tree, by adding another directed edge from one of its nodes to the new converter's node, it will still have a spanning tree. Besides, since the leader node was already pinning to a root node of the old graph before adding the new converter, there is no need for the leader node to pin to the new node. Another way of adding the new node, to a gossip ring for example, is to bring that node in the ring such that it can get the information from the previous node and give the information to the next node in the ring. This method is employed here. Figure 6.11 illustrates the response of the parallel converter system to the augmentation of converter 1. The total output load is set at 3Ω; the total output current should be $18\text{V}/3\Omega = 6\text{A}$. As seen in Figure 6.11, the total current that was shared between converters 1 and 2 ($2 \times 3\text{A} = 6\text{A}$), is now shared among all three converters after the augmentation ($3 \times 2\text{A} = 6\text{A}$). The output voltage is also regulated simultaneously.

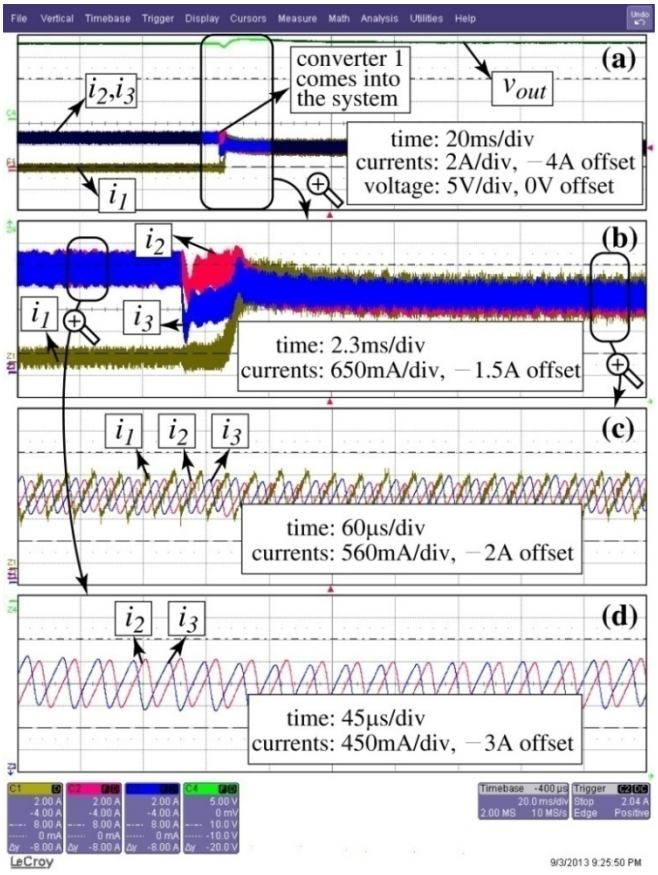

Figure 6.11 Plug and play feature: (a) system response to the augmentation of a new converter (converter 1), (b) zoomed-in view of the current transients, (c) current waveforms after the augmentation, and (d) current waveforms before the augmentation.

6.3.5 Audio Susceptibility

Audio susceptibility or line-regulation capability determines the ability of the parallel converter system to reject the random disturbances in the input voltage. Figure 6.12 depicts the line-regulation performance of the system when the input voltage suddenly drops from 24V to 20V. The output load is set at 3Ω. As seen in Figure 6.12(a-c), the proposed control scheme manages to maintain the output voltage regulation while keeping the current averages equal. The inductor current ripples depend on the difference between the input and output voltages; thus, decreasing the input voltage decreases the inductor current ripples as seen in Figure 6.12(b) and Figure 6.12(c). The average of the current

waveforms, however, does not change since they depend on the reference output voltage and the output load ($I_{\text{out}} = V_{\text{out}}/R$), both of which do not change by changing the input voltage. This explains why noticeable transients are not seen in the average currents in Figure 6.12.

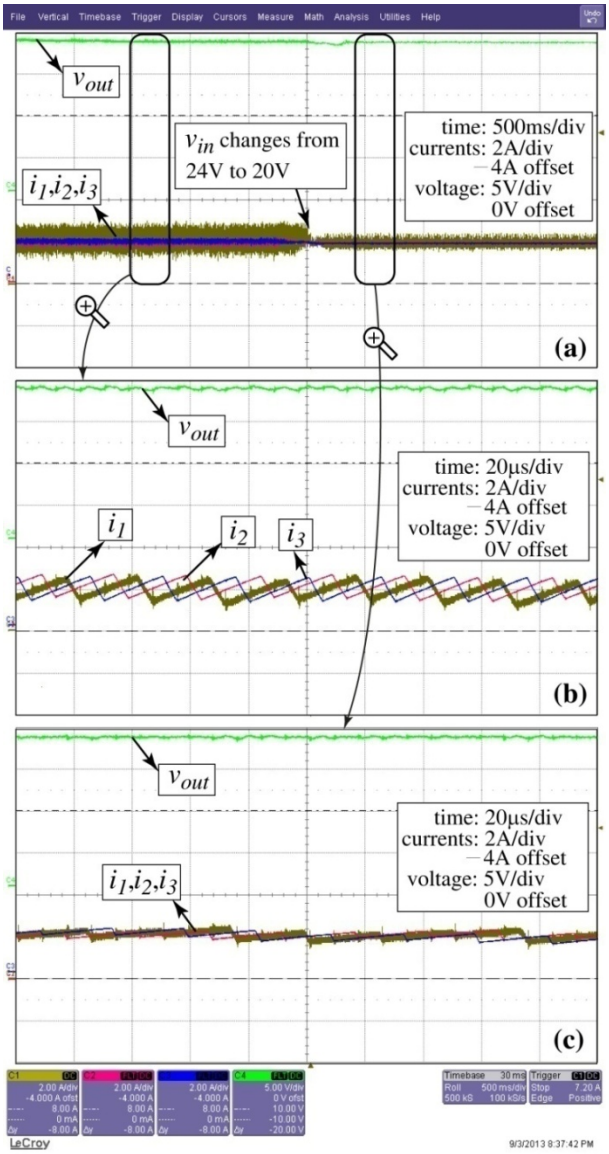

Figure 6.12 Audio susceptibility: (a) system response to the sudden decrease of the output voltage from 24V to 20V, (b) current waveforms before the step change in the input voltage, and (c) current waveforms after the step change.

6.3.6 Load Regulation

Load-regulation capability determines the ability of the parallel converter system to reject the random disturbances in the output load. Figure 6.13 illustrates the load-regulation performance of the proposed cooperative control scheme. The load is consecutively changed from 2Ω to 3Ω and vice versa. As seen in Figure 6.13(a), the current synchronization is maintained among the converters while the output voltage regulation is retained simultaneously. The average currents change from 3A to 2A in response to the step changes in the load from 2Ω to 3Ω, respectively. As seen in Figure 6.13, the cooperative control scheme manages to change the average currents and regulate the output voltage without introducing any significant transients.

Two redundant switch structures are studied and compared for reliability improvement in multiport converters.

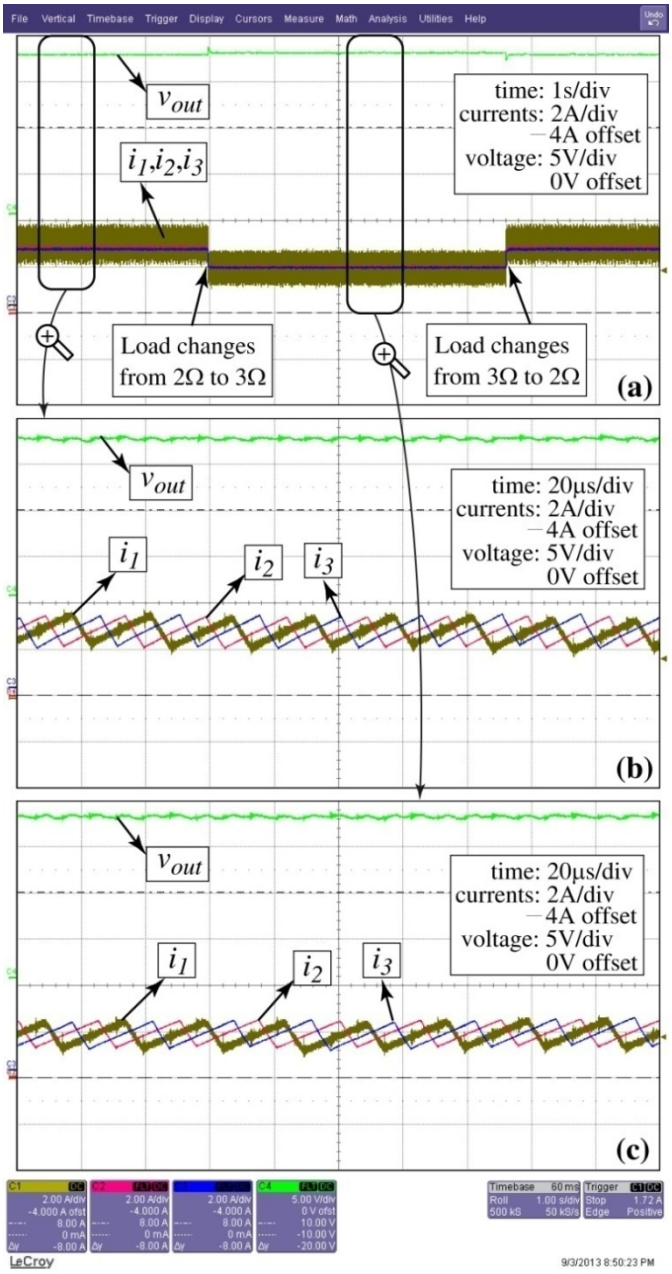

Figure 6.13 Load regulation performance: (a) system response to the sudden change in the output load from 2Ω to 3Ω and vice versa, (b) current waveforms at 2Ω output load, and (c) current waveforms at 3Ω output load.

CHAPTER 7

RELIABILITY ANALYSIS

Power electronic converters, including multiport dc-dc converters, are widely used as power processing units in mission-critical applications such as military, aerospace industry, communication infrastructures, and smart grids. Reliability of the converter is a critical concern in these applications. Fault-tolerant power electronic converters are able to adapt and compensate random faults that might occur during their expected lifetimes. Fault-tolerant operation is conventionally achieved using different control strategies [100-106] or structural redundancy [107-114]. Structural redundancy, in general, is the duplication of critical components in order to have a backup in the case of fault occurrence.

Various redundant structures have been introduced in the literature for different power electronic converters, e.g., inverters [115-117], matrix converters [105-108], multilevel converters [118-120], motor drive [121-124], dc-dc converters [69, 125], and power factor correction rectifiers [126, 127]. These structures usually employ a redundant sub-circuit comprised of several components. For instance, an additional leg is augmented to a three-leg, diode-clamped multilevel inverter in [109].

Structural redundancy can also be considered at a component level as opposed to sub-circuit level. The advantages of the component-level redundancy are simplicity of the fault management and cost effectiveness. Power semiconductor switches are, arguably, among the least reliable components in power electronics converters [128, 129]. Two well-known redundant structures, namely parallel and standby configurations [130], can be considered to improve the reliability of system components. They can also be applied to semiconductor switches. Reliability analysis framework and selection criteria for the parallel and standby switch configurations have not been investigated to date. This chapter performs a comparative reliability analysis between these configurations and provides the following contributions:

- Reliability models of parallel and standby switch configurations are developed based on Markov process. The MTTF of each configuration is derived and formulated.

- A boundary curve is identified and parameterized, where both redundant configurations have equal MTTFs, i.e., similar reliability characteristics. The key parameter of the boundary curve is found to be the switch-junction temperatures in steady state according to MIL-HDBK-217F handbook [131].
- The junction temperature range in which the parallel switch configuration is more reliable is determined for different high-power semiconductor switches including MOSFETs, BJTs, SCRs, TRIACs, regular diodes, and Schottky diodes.
- The effects of ambient temperature, converter's power level, and utilization of heat sink on the reliabilities of parallel and standby configurations are analyzed. It is shown that, for high-power converters operating at regular ambient temperature, the parallel configuration is likely to be more reliable. This is in direct contrast to the conventional reliability wisdom that the standby configuration is always more reliable than the parallel configuration. On the other hand, for low-power converters operating in high ambient temperature, standby configuration is likely to be the more reliable option.

The rest of this chapter is organized as follows: Section 7.1 introduces the parallel and standby switch configurations. Markov-process based reliability models of both configurations are developed in section 7.2. A comparative reliability analysis between the two configurations is presented in section 7.3. Section 7.4 discusses the effect of the junction temperature on the relative lifetime of these configurations. The influences of converter's power level and ambient temperature on the relative reliability of parallel and standby configurations are analyzed in section 7.5. Section 7.6 presents thermal studies and reliability analysis for a laboratory-scale buck converter. A discussion about how utilization of heat sinks can affect the experimental results is provided in section 7.7. The detailed derivations of the boundary curve, where both configurations have equal MTTFs, is given in section 7.8.

7.1 Redundant Switch Structures

Two widely-accepted redundant switch structures are standby and parallel configurations, shown in Figure 7.1(a) and Figure 7.1(b), respectively. Two groups of switches are considered: auxiliary switches, $S_1', \dots, S_n'$, and main switches, $S_1, \dots, S_n$. The auxiliary switches enable the FDIR mechanism to

appropriately manage the faults [132]. They can be realized using low-frequency electromechanical relays. The main switches are the semiconductor switches (e.g., MOSFET or BJT) operating in high frequency ranges.

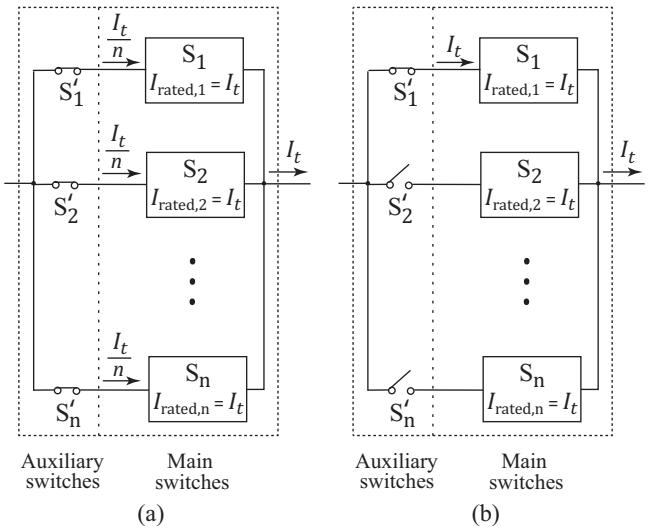

Figure 7.1 Redundant switch structures: (a) parallel configuration; (b) standby configuration.

In the parallel configuration (Figure 7.1(a)) all auxiliary switches, S_i', are initially closed. Once a main switch, S_i, fails, the FDIR mechanism opens the corresponding auxiliary switch, S_i', and the total current, I_t, is shared between the rest of the main switches. Proper current balancing between the main switches is assumed [133-137]. When all switches are healthy, each one should carry I_t/n. However, in the case that all but one switch fail, the remaining switch should be able to conduct the total load current, I_t. Thus, the current rating of each main switch, $I_{\text{rated},i}$, should be the same as that of the overall switch network, I_t. In other words, all main switches are overrated to avoid overloading.

In the standby configuration, illustrated in Figure 7.1(b), only the first auxiliary switch, S_1', is initially closed. Once the main switch, S_1, fails, the FDIR mechanism isolates S_1 by opening its corresponding auxiliary switch, S_1'. The next healthy switch, S_2, replaces the failed switch by closing S_2'. The system proceeds until all main switches fail, where the overall system fails. Similar to the parallel

configuration, the current rating of each main switch, $I_{\text{rated},i}$, is the same as that of the overall switch network, I_t.

The fault isolation mechanism (e.g. mechanical relays) can be embedded in semiconductor switch modules. Especially, with the recent introduction of on-chip mechanical relays [138], new redundant switch modules can be potentially developed that have integrated isolation mechanism. Besides, integrated current or temperature sensors can also be employed in these switch modules to enable fault detection. These switch modules will be able to detect the random faults, isolate them, and reconfigure their circuit (FDIR) based on a user-defined redundant structure (e.g. parallel or standby configurations). Enhanced reliability and prolonged lifetime will be the potential advantages of these switch modules over their conventional counterparts.

7.2 Markov Reliability Model Development

A Markov chain is a special type of stochastic process, $X(t)$. A stochastic process $X(t)$ is called a Markov chain if it is memoryless, i.e.,

$$\Pr\{X(t_k) = s_k \mid X(t_{k-1}) = s_{k-1}, \cdots, X(t_1) = s_1\} = \Pr\{X(t_k) = s_k \mid X(t_{k-1}) = s_{k-1}\} \tag{7.1}$$

where s_k is the state of Markov chain at time t_k. When the number of states is finite, a natural number, $\{1, \ldots, N\}$, can be assigned to each state. The probability that Markov chain is in the i^{th} state at time t, $P_i(t)$, is given by the following set of linear differential equations [130]:

$$\frac{dP_i(t)}{dt} = -\sum_{i \neq j} \lambda_{ij} P_i(t) + \sum_{j \neq i} \lambda_{ji} P_j(t) \tag{7.2}$$

where $1 \leq i, j \leq N$, and λ_{ij} denotes the rate at which the chain transitions from the state i to state j. The matrix format of (7.2) is more convenient for the analysis purpose:

$$\frac{d\ \mathbf{P}(t)}{dt} = \mathbf{A}\mathbf{P}(t) \tag{7.3}$$

where $\mathbf{P}(t) = [P_1 \ldots P_N]^T$, and $\mathbf{A}$ is the transition matrix. Assuming that the first state is where the chain begins, the initial condition of (7.3) is

$$\mathbf{P}(0) = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 \end{bmatrix}^T \tag{7.4}$$

The final state, N, is assumed to be the state in which the whole system has failed. Thus, the reliability of the system is

$$R(t) = 1 - P_N(t) \tag{7.5}$$

MTTF is a metric that determines the expected lifetime of the system [130], and is given by

$$MTTF = \int_0^\infty R(t)dt \tag{7.6}$$

The Markov reliability models of parallel and standby configurations are developed in the following. A two-switch redundant structure is considered. The procedure, however, is general and can accommodate arbitrary numbers of switches.

7.2.1 Parallel Configuration

Figure 7.2 illustrates the Markov chain diagram for a parallel configuration with two main switches. Hereafter, the term "switch" refers to the main switches. Four states can be identified: the state in which both switches are healthy (state 11); the state in which the first switch failed, was detected, and isolated but the second one is still healthy (state 01); the state in which the second switch failed, was detected, and isolated but the first one is still healthy (state 10); and the final state in which the whole configuration failed (state 00). These states and their occupational probabilities, $P_1, \ldots, P_4$, are shown in Figure 7.2. In the case of fault occurrence, the probability that the FDIR mechanism can manage the fault is denoted by P_p^c (fault coverage), where the subscript "p" denotes the parallel configuration.

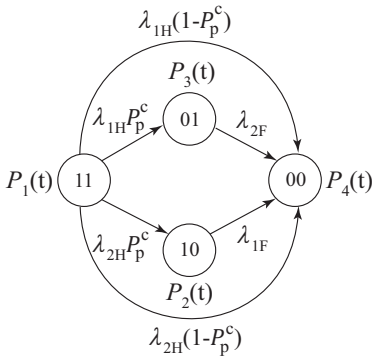

Figure 7.2 The Markov chain diagram of two switches operating in the parallel configuration.

When both switches are healthy, each carries half of the load current. Here, this condition is referred to as the half-load operation mode. The failure rates of the k^{th} switch, S_k, in half load and full load conditions are denoted by λ_{kH} and λ_{kF}, respectively. The rate at which the first switch fails when both switches are healthy is λ_{1H}. Besides, the probability that the FDIR mechanism can manage the fault is P_p^c. Therefore, the rate at which the Markov chain transitions from state 11 to state 01 is $\lambda_{1H}P_p^c$. The probability that the FDIR mechanism fails to manage the fault is $\left(1-P_p^c\right)$. Therefore, the rate at which the Markov chain transitions from state 11 to state 00 is $\lambda_{1H}\left(1-P_p^c\right)$. If the first switch fails and the FDIR mechanism manages the fault, the second switch should carry the total current. Thus, the rate at which the Markov chain transitions from state 01 to state 00 is λ_{2F}. Likewise, the rates at which the chain transitions from state 11 to state 10 and from state 10 to state 00 are $\lambda_{2H}P_p^c$ and λ_{1F}, respectively. According to (7.2)-(7.3) and Figure 7.2, the evolution of the occupational probabilities is governed by

$$\frac{d}{dt}\begin{bmatrix} P_1(t) \\ P_2(t) \\ P_3(t) \\ P_4(t) \end{bmatrix} = \begin{bmatrix} -\lambda_{1H}-\lambda_{2H} & 0 & 0 & 0 \\ \lambda_{2H}P_p^c & -\lambda_{1F} & 0 & 0 \\ \lambda_{1H}P_p^c & 0 & -\lambda_{2F} & 0 \\ \left(1-P_p^c\right)\left(\lambda_{1H}+\lambda_{2H}\right) & \lambda_{1F} & \lambda_{2F} & 0 \end{bmatrix}\begin{bmatrix} P_1(t) \\ P_2(t) \\ P_3(t) \\ P_4(t) \end{bmatrix}. \tag{7.7}$$

Considering the initial condition in (7.4), one can find the reliability function of the parallel configuration:

$$R_p(t) = \left[1 - \frac{\lambda_{1H} P_p^c}{\lambda_{1H} + \lambda_{2H} - \lambda_{2F}} - \frac{\lambda_{2H} P_p^c}{\lambda_{1H} + \lambda_{2H} - \lambda_{1F}}\right] e^{-(\lambda_{1h} + \lambda_{2h})t} + \frac{\lambda_{1H} P_p^c}{\lambda_{1H} + \lambda_{2H} - \lambda_{2F}} e^{-\lambda_{2F} t} + \frac{\lambda_{2H} P_p^c}{\lambda_{1H} + \lambda_{2H} - \lambda_{1F}} e^{-\lambda_{1F} t}. \quad (7.8)$$

7.2.2 Standby Configuration

In this configuration, the probability that FDIR mechanism can detect the faulty switch, isolate it, and replace it with the healthy one is denoted by P_{sb}^c (fault coverage). The subscript "sb" in P_{sb}^c denotes the standby structure. Figure 7.3 depicts the corresponding Markov chain diagram. State 11 represents the state in which both switches are healthy, but only the first switch carries the total current. State 01 represents the state in which the first switch failed, was detected, isolated, and replaced with the second one. State 00 represents the state in which the whole configuration failed.

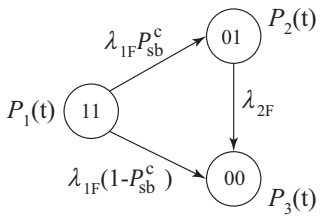

Figure 7.3 The Markov chain diagram of two switches operating in the standby configuration.

The first switch, S_1, conducts the total current until it fails; its failure rate is λ_{1F}. Besides, the probability that FDIR mechanism can manage the fault is P_{sb}^c. Therefore, the rate at which the transitions occur from state 11 to state 01 is $\lambda_{1F}P_{sb}^c$. If the FDIR mechanism cannot detect the fault, isolate it, or replace the second switch, the whole configuration fails. Thus, the rate at which the Markov chain transitions from state 11 to state 00 is $\lambda_{1F}(1 - P_{sb}^c)$. In the case that the first switch is already failed and the second switch is operational, state 01, the system will fail if the second switch also fails. Thus, the rate at which the Markov chain transitions from state 01 to state 00 is λ_{2F}.

The evolution of occupational probabilities for this configuration is governed by

$$\frac{d}{dt}\begin{bmatrix} P_1(t) \\ P_2(t) \\ P_3(t) \end{bmatrix} = \begin{bmatrix} -\lambda_{1F} & 0 & 0 \\ \lambda_{1F} P_{sb}^c & -\lambda_{2F} & 0 \\ \lambda_{1F}(1-P_{sb}^c) & \lambda_{2F} & 0 \end{bmatrix} \begin{bmatrix} P_1(t) \\ P_2(t) \\ P_3(t) \end{bmatrix}. \tag{7.9}$$

Using (7.4)-(7.5), the reliability function of the standby configuration can be derived as

$$R_{sb}(t) = e^{-\lambda_{1F}t} + \frac{\lambda_{1F}}{\lambda_{1F}-\lambda_{2F}} P_{sb}^c \left[e^{-\lambda_{2F}t} - e^{-\lambda_{1F}t} \right]. \tag{7.10}$$

7.3 Comparative Reliability Analysis

The MTTFs of parallel and standby configurations determine the expected lifetime of the corresponding switch networks. Thus, they can be good measures to compare the reliabilities of parallel and standby configurations. Conventionally, the failure rates are assumed to be constant in parallel and standby configurations constructed from independent modules [130]. According to [130], this assumption leads to the following derivations for MTTFs of parallel and standby configurations, $MTTF_p$ and $MTTF_{sb}$ respectively,

$$MTTF_p = \frac{1}{\lambda_1} + \frac{1}{\lambda_2} - \frac{1}{\lambda_1 + \lambda_2} \tag{7.11}$$

$$MTTF_{sb} = \frac{1}{\lambda_1} + \frac{1}{\lambda_2} \tag{7.12}$$

where λ_1 and λ_2 are the constant failure rates of the first and second modules for their entire lifetime, respectively. Comparing (7.11) and (7.12), one might conclude that the standby configuration is always more reliable. However, the failure rates of power semiconductors depend on their operating current; they cannot be assumed constant. Thus, the Markov models developed in section 7.2 should be used to compare the reliabilities of these switch configurations since they can tackle variant failure rates.

Using (7.6), (7.8), and (7.10), one can express the MTTFs of both configurations in terms of λ_{1H}, λ_{2H}, λ_{1F}, and λ_{2F}:

$$MTTF_p = \frac{1+\left(\lambda_{1H}/\lambda_{2F} + \lambda_{2H}/\lambda_{1F}\right)P_p^c}{\lambda_{1H}+\lambda_{2H}}, \tag{7.13}$$

$$MTTF_{sb} = \frac{\lambda_{2F} + \lambda_{1F}P_{sb}^c}{\lambda_{1F}\lambda_{2F}} \tag{7.14}$$

Since both switches operate at the same voltage and current levels, they can be identical. Employing identical semiconductors also helps balance the current between them [128]. Thus,

$$\begin{cases} \lambda_{1H} = \lambda_{2H} = \lambda_H \\ \lambda_{1F} = \lambda_{2F} = \lambda_F \end{cases} \tag{7.15}$$

This assumption can simplify the MTTF expressions. Using (7.13)-(7.15), the ratio of MTTFs can be calculated to determine the relative lifetime of these configurations

$$\frac{MTTF_p}{MTTF_{sb}} = \frac{2KP_p^c + 1}{2K(P_{sb}^c + 1)} \tag{7.16}$$

where K is defined as the ratio of half-load to full-load failure rate of the switches:

$$K = \frac{\lambda_H}{\lambda_F}. \tag{7.17}$$

The boundary condition is defined as the condition in which both parallel and standby configurations have the same MTTF. The boundary condition can be found in terms of K by equating (7.16) to one:

$$K = \frac{1}{2(1+P_{sb}^c - P_p^c)}. \tag{7.18}$$

It can be seen that the parallel configuration is more reliable if

$$K < \frac{1}{2(1+P_{sb}^c - P_p^c)}. \tag{7.19}$$

Besides, because the current stress of a switch in half load is less than that in full-load, half-load failure rate is always less than the full-load failure rate, i.e., $K \leq 1$. Thus, if the right hand side of (7.19) is

greater than one; (7.19) is satisfied regardless of the value of K. Thus, the parallel configuration is more reliable than the standby configuration if

$$\frac{1}{2(1+P_{sb}^{c}-P_{p}^{c})}>1, \tag{7.20}$$

which implies

$$P_{p}^{c}-P_{sb}^{c}>0.5. \tag{7.21}$$

Proper FDIR operation in standby configuration requires opening the first auxiliary switch, S_1', and closing the second one, S_2'. On the other hand, proper FDIR operation in parallel structure only requires opening one auxiliary switch, S_1' or S_2'. Thus, the fault coverage in parallel configuration is usually easier than the standby configuration, i.e., $P_p^c > P_{sb}^c$. According to (7.21), if the difference between P_p^c and P_{sb}^c is more than 50%, then the parallel configuration is more reliable regardless of the half-load and full-load failure rates. If the difference is less than 50%, then the ratio of the half-load to full-load failure rate, K, determines the more reliable configuration.

Figure 7.4 illustrates the MTTFs of parallel and standby configurations versus half-load and full-load failure rates assuming 100% fault coverage in both cases ($P_p^c = P_{sb}^c$=1). The intersection of the two surfaces, Figure 7.4(c), represents the boundary condition. As (7.18) suggests, the spatial location of the boundary condition depends on the difference between the fault coverage capabilities of the FDIR mechanisms, $P_p^c - P_{sb}^c$. The boundary conditions are plotted in two dimensions in Figure 7.5 for different values of $P_p^c - P_{sb}^c$.

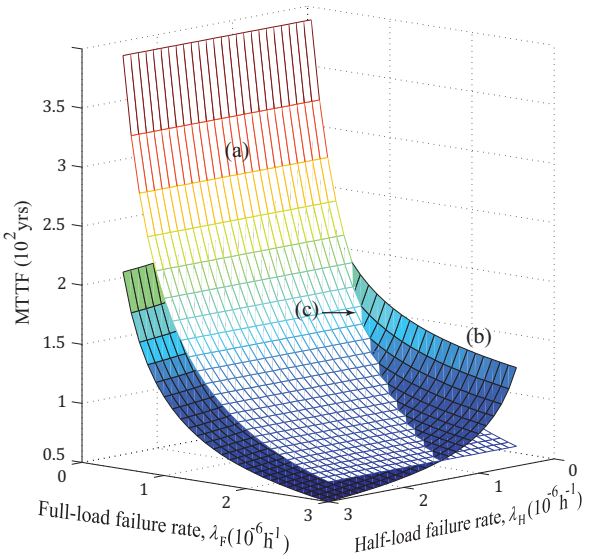

Figure 7.4 (a) MTTF of the standby configuration, $MTTF_{sb}$; (b) MTTF of the parallel configuration, $MTTF_p$; (c) the boundary condition, ($P_{sb}^c = P_p^c$).

Since half-load failure rate, λ_H, is always less than its full-load failure rate, λ_F, the region in which $\lambda_H > \lambda_F$ is infeasible (the upper triangle shown darker in Figure 7.5). The boundary line divides the feasible area into two subareas: (a) the region in which parallel configuration is more reliable, (b) the region in which standby configuration is more reliable. One can see from Figure 7.5 that region (a) is a wider than region (b) for all different values of $P_p^c - P_{sb}^c$ except for $P_p^c - P_{sb}^c = 0$, where two regions have equal areas. In other words, the parallel configuration is more reliable for wider range of half-load to full-load failure ratios. The boundary line lies on the infeasible region if $\left(P_p^c - P_{sb}^c\right) > 0.5$ as expected; the parallel configuration is always more reliable if $\left(P_p^c - P_{sb}^c\right) > 0.5$.

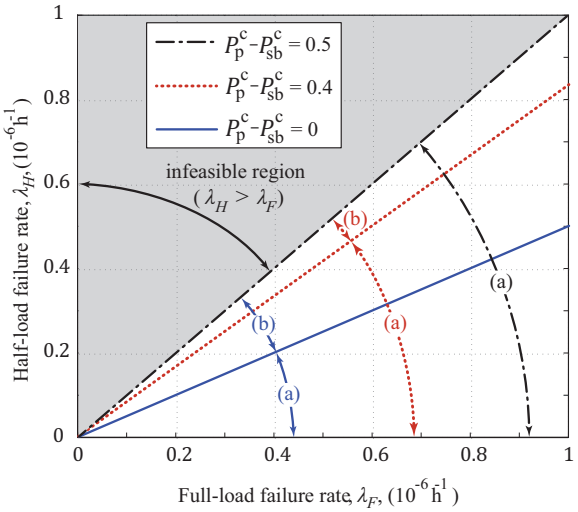

Figure 7.5 The boundary conditions corresponding to different values of ($P_p^c - P_{sb}^c$): (a) the region in which the parallel configuration is more reliable; (b) the region in which the standby configuration is more reliable.

7.4 Junction Temperature Effect

If the difference between fault coverage capacities in parallel and standby configurations is less than 50%, i.e., $P_p^c - P_{sb}^c < 0.5$, then the ratio of the half-load to full-load failure rate, K, determines the more reliable configuration. The half-load and full-load failure rates of the switches depend on their junction temperatures in these operating modes [131]. Thus, reformulating of (7.16) and (7.17) in terms of junction temperatures helps determine the operating temperature range where the parallel configuration is more reliable. The type of the semiconductor switch must be specified in this regard. A power MOSFET will be considered first. A similar discussion can be extended to other types of power semiconductor switches.

The failure rate of a power MOSFET is given according to the well-known MIL-HDBK-217F [131]:

$$\lambda = \lambda_b \pi_T \pi_A \pi_Q \pi_E \tag{7.22}$$

where λ_b, π_T, π_A, π_Q, and π_E are base failure rate, temperature factor, application factor, quality factor, and environmental factor, respectively. Since λ_b, π_A, π_Q and π_E are equal in half-load and full-load operation modes [131], K is simplified to

$$K = \frac{\lambda_H}{\lambda_F} = \frac{\pi_{T,H}}{\pi_{T,F}} \tag{7.23}$$

where $\pi_{T,H}$ and $\pi_{T,F}$ are temperature factors in half-load and full-load, respectively. In addition, $\pi_{T,H}$ and $\pi_{T,F}$ depend on the junction temperature of the MOSFET [131]:

$$\pi_T = e^{-1925\left(\frac{1}{T_j+273}-\frac{1}{298}\right)}. \tag{7.24}$$

To ensure a fair comparison between the two configurations, their fault coverage capacities are assumed to be equal i.e. $P_p^c = P_{sb}^c$. By this assumption and using (7.18), (7.23), and (7.24), the boundary condition can be expressed in terms of the junction temperature of the MOSFETs:

$$T_{jH} = \frac{0.893 \times T_{jF} - 32.0°\text{C}}{3.6 \times 10^{-4} T_{jF} + 1.107} \tag{7.25}$$

where T_{jH} and T_{jF} denote the junction temperature of the MOSFETs in half-load and full-load, respectively. The first term in the denominator of (7.25) is negligible compared to the second term. Therefore the condition in which the parallel structure is more reliable can be approximated as

$$T_{jH} < 0.806 \times T_{jF} - 28.9°\text{C} \tag{7.26}$$

The derivation details of (7.25) and (7.26) are provided in section 7.8. Figure 7.6 depicts the spatial location of the boundary condition for a power MOSFET. Figure 7.6(a) is the K surface and Figure 7.6(b) is a flat surface corresponding to the boundary condition, $k = 1/\left[2\left(1 + P_{sb}^c - P_p^c\right)\right]$. As suggested by (7.19), the parallel configuration is more reliable if $k < 1/\left[2\left(1 + P_{sb}^c - P_p^c\right)\right]$. Thus, the intersection of the surfaces in Figure 7.6(a) and Figure 7.6(b) determines the boundary condition. It should be noted that half of the area in Figure 7.6 is infeasible because junction temperature at half-load cannot exceed the junction temperature at the full-load ($T_{j,H} \leq T_{j,F}$).

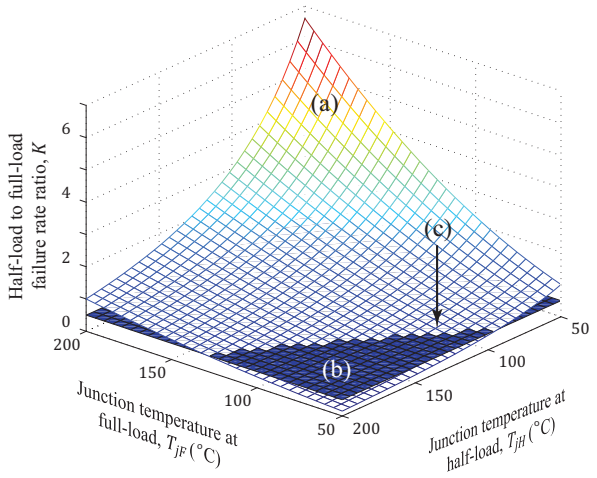

Figure 7.6 (a) The ratio of half-load failure rate to full-load failure rate, K, for power MOSFETs; (b) $K = 0.5/(1 + P_{sb}^{c} - P_{p}^{c})$ plane; (c) the boundary condition, $(P_{sb}^{c} = P_{p}^{c})$.

The same procedure is followed for other types of semiconductor switches according to MIL-HDBK-217F, [131], and results are reported in Table I.

Table 7.1 The junction temperature range in which the parallel configuration is more reliable for different types of power semiconductors

Power semiconductor type	The junction temperature range in which parallel configuration is more reliable
Power diode	$T_{jH} < 0.874T_{jF} - 18.7\,^{\circ}\mathrm{C}$
Schottky diode	$T_{jH} < 0.820T_{jF} - 26.7\,^{\circ}\mathrm{C}$
Power BJT	$T_{jH} < 0.905T_{jF} - 15.9\,^{\circ}\mathrm{C}$
Power MOSFET	$T_{jH} < 0.806T_{jF} - 28.9\,^{\circ}\mathrm{C}$
Thyrisor, SCR, TRIAC	$T_{jH} < 0.874T_{jF} - 18.7\,^{\circ}\mathrm{C}$

7.5 Effects of Ambient Temperature and Converter's Power Level

The effect of junction temperature, T_j, on the relative reliability of parallel and standby configurations was studied in the previous section. The junction temperature, however, depends on two

other parameters, namely, power loss of the semiconductor switch and ambient temperature. The objective of this section is to clarify how these parameters affect the junction temperature and, consequently, the relative reliability of parallel and standby configurations.

The junction temperature of a switch, T_j, can be expressed in terms of its power loss, P_{loss}, and case temperature, T_c, as

$$T_j = T_c + R_{\text{th,jc}} P_{\text{loss}}. \tag{7.27}$$

where $R_{\text{th,jc}}$ is the thermal resistance between the junction and case of the semiconductor switch. In addition, the thermal resistance between the semiconductor's case and ambient determines the case temperature, T_c. If a heat sink is used, this thermal resistance will be the thermal resistance of the heat sink, which is much less than the thermal resistance between case and ambient when no heat sink is used. Similar to (7.27), the case temperature can be expressed as

$$T_c = T_a + R_{\text{th,ca}} P_{\text{loss}}. \tag{7.28}$$

where T_a is ambient temperature and $R_{\text{th,ca}}$ is either the thermal resistance of the heat sink or the normal thermal resistance between the case and ambient. The equivalent thermal circuit of the switch is illustrated in Figure 7.7. Since the steady-state value of T_j is of interest, the effect of C_{th} in the thermal circuit is neglected. Using (7.27) and (7.28), the junction temperature in half-load and full-load operation modes, T_{jH} and T_{jF}, can be expressed as

$$\begin{cases} T_{jH} = T_a + \left(R_{\text{th,jc}} + R_{\text{th,ca}}\right) P_{\text{loss},H} \\ T_{jF} = T_a + \left(R_{\text{th,jc}} + R_{\text{th,ca}}\right) P_{\text{loss},F} \end{cases}. \tag{7.29}$$

where $P_{loss,H}$ and $P_{loss,F}$ denote the power loss of the switch in half-load and full-load operation modes, respectively.

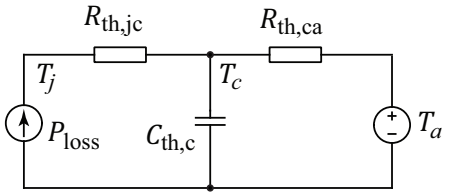

Figure 7.7 The thermal equivalent circuit of power semiconductor switches.

The inequalities given in Table I describe the necessary and sufficient conditions for the parallel configuration to be more reliable than its standby counterpart. These inequalities, in general, can be expressed in the form of

$$T_{jH} < k_1 T_{jF} - k_2 \tag{7.30}$$

where k_1 and k_2 are constants that depend on the type of the power semiconductor. Using (7.29) and (7.30), one can find the following condition for the parallel configuration to be more reliable:

$$\frac{\left(1-k_1\right)\ T_a + k_2}{R_{\text{th,jc}} + R_{\text{th,ca}}} < \left(k_1 P_{\text{loss},F} - P_{\text{loss},H}\right)\ . \tag{7.31}$$

It should be noted that the values of k_1 are very close for different types of semiconductors. The average and standard deviation of k_1 are 0.856 and 0.041, respectively. Since the standard deviation of k_1 is small, it can be substituted by its average value in (7.31):

$$\frac{0.144\times T_a + k_2}{R_{\text{th,jc}} + R_{\text{th,ca}}} < \left(0.856\times P_{\text{loss},F} - P_{\text{loss},H}\right)\ . \tag{7.32}$$

Increasing the ambient temperature, T_a, increases the left side of (7.32), and consequently, (7.32) is less likely to be satisfied. In other words, the higher the ambient temperature, the more likely that standby configuration is more reliable. On the other hand, increasing the power level of the converter leads to higher switch voltage and current. Consequently, the power loss of the switches increase, and the difference between the power loss in half-load and full-load operation modes increases as well. This means that the right side of (7.32) increases; i.e., (7.32) is more likely to be satisfied. Thus, the parallel configuration becomes the more reliable configuration.

One can conclude that the parallel configuration is more suitable for the converters with low ambient temperature and high power level. On the other hand, standby configuration, is more suitable for the converters with high ambient temperature and low power level. For heavy-duty converters that operate at high power levels and in high ambient temperatures, (7.32) should be examined to exactly determine which configuration is more reliable.

7.6 Case Studies

The objective of this section is to examine (7.26) for a laboratory-scale buck converter operating in room temperature. A 70W buck converter with a single MOSFET is built to determine the junction temperature in full-load, T_{jF}. Another similar 70W buck converter with two MOSFETs is also built to determine the junction temperature in half-load, T_{jH}. Every other aspect of these two converters is identical. The circuit parameters are as follows: $V_{\text{in}} = 20\text{V}$, $V_{\text{out}} = 15\text{V}$, $P = 68\text{W}$, $L = 1.2\text{mH}$, $C = 4400\mu\text{F}$, $R_{\text{on,MOSFET}} = 0.07\Omega$, $R_{\text{th,jc}} = 0.32^{\circ}\text{C/W}$, $R_{\text{th,ca}} = 62^{\circ}\text{C/W}$, and $R_{\text{th,heatsink}} = 12^{\circ}\text{C/W}$. Figure 7.8 and Figure 7.9 show the converters' schematics and the experimental setup, respectively.

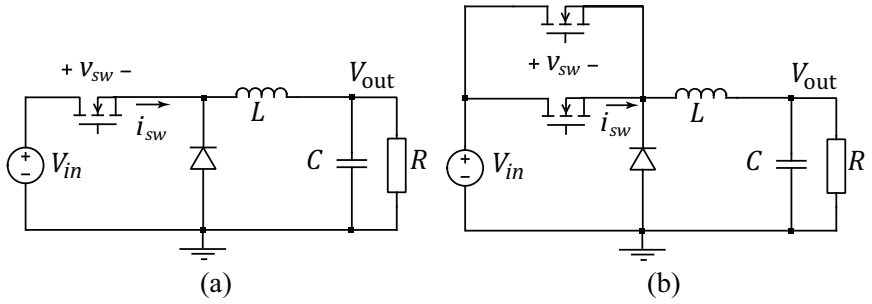

Figure 7.8 The schematics of a buck converter with (a) full-loaded MOSFET, and (b) half-loaded MOSFETs.

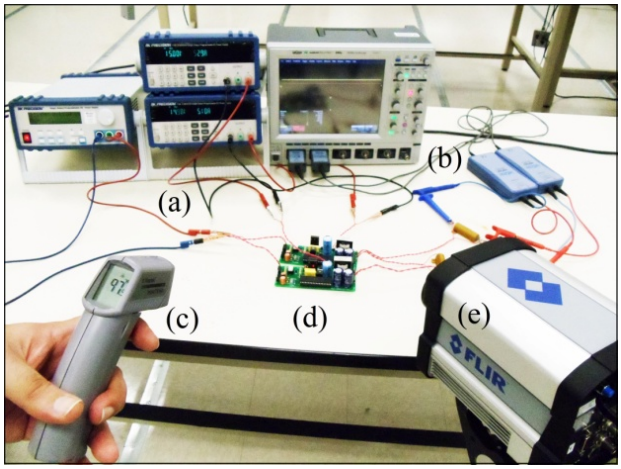

Figure 7.9 The hardware setup: (a) power supplies, (b) oscilloscope, (c) laser thermometer, (d) converters, (e) thermal camera.

The following procedure is used to accurately determine the half-load and full-load junction temperatures:

- The MOSFETs' power losses are precisely determined by measuring their voltage and current waveforms, v_{sw} and i_{sw}, respectively. Figure 7.10(a, b, and c) show the measured current, voltage, and instantaneous power loss of the half-loaded MOSFETs in two switching cycles, respectively. As seen in Figure 7.10(c), the instantaneous power loss of the MOSFETs has a considerable peak at the turn-off moment, whereas, its peak at the turn-on moment is negligible ($E_{\text{on}} \ll E_{\text{off}}$). The voltage and current profiles of the MOSFETs explain why E_{on} is negligible. As seen in Figure 7.10(a and b), during turn-on transition, the switches' voltages become approximately zero before their currents start to rise. Moreover, since Schottky diodes (V40100C) are used, there is no significant diode reverse recovery current to affect the power loss of the MOSETs during turn-on transition. The magnified voltage, current, and instantaneous power loss waveforms during turn-off transition are shown in Figure 7.11 and Figure 7.12, respectively. Likewise, the corresponding waveforms of the other buck converter with the full-loaded MOSFET are shown in Figure 7.13, Figure 7.14, and Figure 7.15. The average power loss of each MOSFET in both cases is given by

$$P_{\text{loss}} = \left(E_{\text{on}} + E_{\text{off}}\right) f_{sw} + P_{\text{cond}} \tag{7.33}$$

where E_{off}, and f_{sw} are the energy loss during the turn off subinterval and the switching frequency, respectively. The energy loss during turn off subinterval, E_{off}, can be found by determining the area under the waveforms of Figure 7.12 and Figure 7.15. The conduction power loss, P_{cond}, is

$$P_{\text{cond}} = f_{sw} \int_{T_{\text{cond}}} v_{on} i_{on} dt \tag{7.34}$$

where T_{cond} is the conduction subinterval of the MOSFET. The conduction power losses are determined by considering the forward resistances of the MOSFETs and their operating current. The switching energy loss, conduction power loss, and average power loss of the MOSFETs are listed in Table II for both cases.

Table 7.2 The switching loss, conduction loss, average power loss, and junction temperature of the MOSFETs in full-load and half-load operation modes

	$E_{\text{on}} + E_{\text{off}}$ (μJ)	P_{cond}(W)	P_{loss}(W)	T_j(°C)
Full-load	92	1.31	2.23	97
Half-load	68	0.24	0.92	36

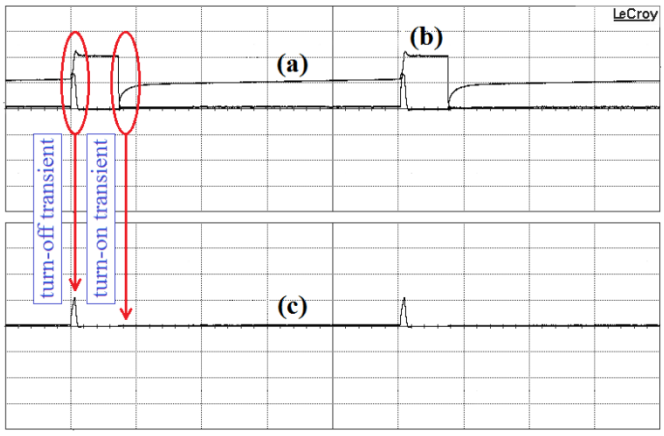

Figure 7.10 The measured current, (b) voltage, and (c) instantaneous power loss of the half-loaded MOSFETs. (2A/div, 10V/div, 50W/div, 20μs/div)

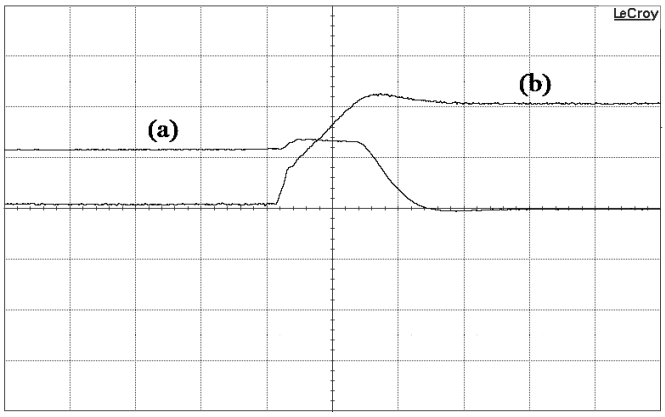

Figure 7.11 The magnified (a) current, and (b) voltage of the half-loaded MOSFETs during the turn off transients. (2A/div, 10V/div, 1μs/div)

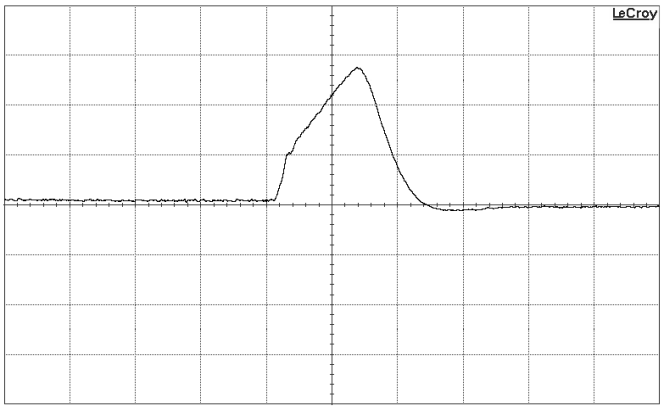

Figure 7.12 The magnified instantaneous power loss of the half-loaded MOSFETs during the turn off transients. (20W/div, 1μs/div)

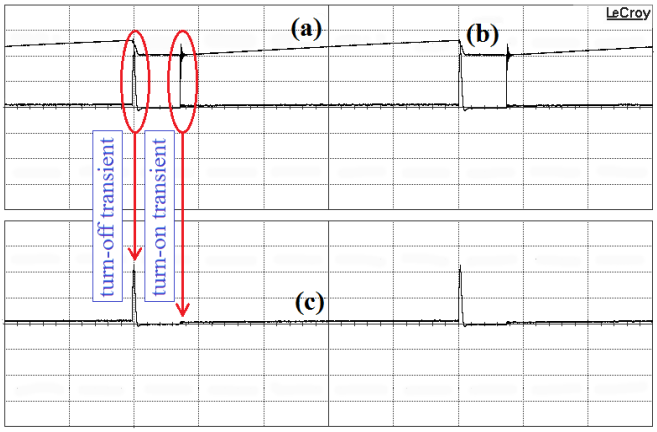

Figure 7.13 (a) The measured current, (b) voltage, and (c) instantaneous power loss of the full-loaded MOSFET. (2A/div, 10V/div, 50W/div, 20μs/div)

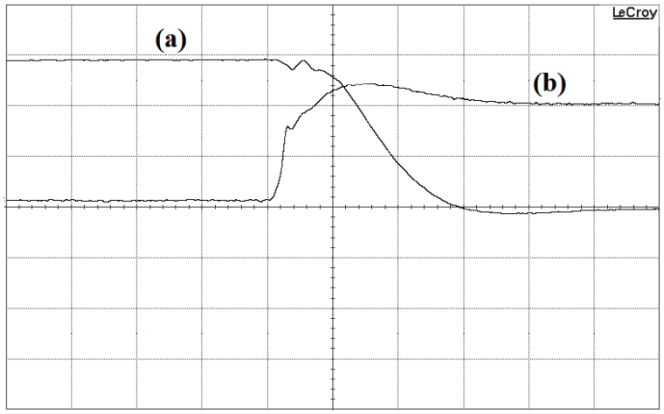

Figure 7.14 The magnified (a) current, and (b) voltage of the full-loaded MOSFET during the turn off transients. (2A/div, 10V/div, 1μs/div)

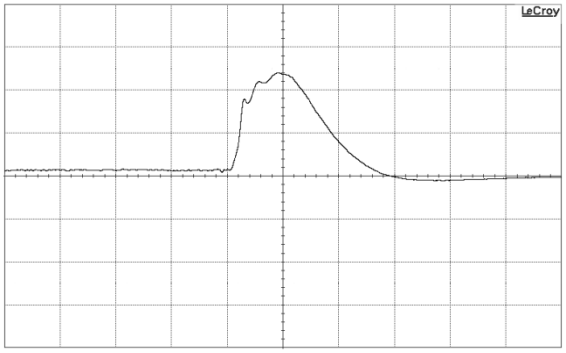

Figure 7.15 The magnified instantaneous power loss of the full-loaded MOSFET during the turn off transients. (50W/div, 1μs/div).

- The case temperature of each MOSFET in steady state is precisely measured by a thermal camera. The two converter prototypes are shown in Figure 7.16. Their thermal pictures when both are on are illustrated in Figure 7.17. Given the case temperature and average power loss of each MOSFET, T_{jH} and T_{jF} are calculated using (7.27), and reported in Table II.

The reported $T_{j,H}$ and $T_{j,F}$ values in Table II satisfy the inequality in (7.26), i.e., the parallel configuration is more reliable for a buck converter with the given properties. The failure rate of a semiconductor switch depends on the junction temperature according to MIL-HDBK-217F [131]. This temperature dependency of the failure rates and the temperature difference in Figure 7.17 intuitively explains why the parallel configuration is more reliable in this case.

Figure 7.16 (a) The buck converter with full-loaded MOSFET, (b) the buck converter with half-loaded MOSFETs.

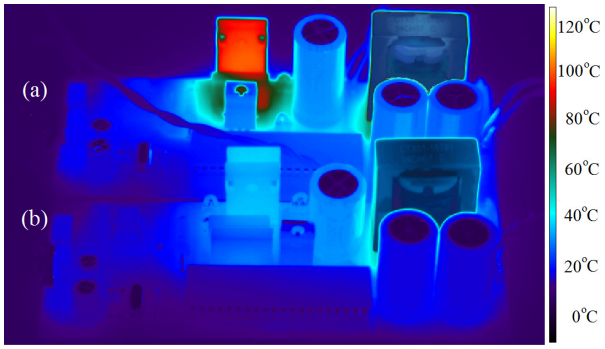

Figure 7.17 The thermal image of the converters when both are on and the case temperatures of the MOSFETs reached their steady state values: (a) the buck converter with full-loaded MOSFET, (b) the buck converter with half-loaded MOSFETs.

7.7 Discussion on Heat Sinks

In the previous section, it was concluded that the parallel configuration is the more reliable option for the studied prototype. This conclusion was drawn based on the measured $P_{\text{loss},H}$ and $P_{\text{loss},F}$ values. It should be noted that this conclusion is not very sensitive to some tolerance in measuring $P_{\text{loss},H}$ and $P_{\text{loss},F}$. For instance, using (7.31), it can be demonstrated that ±35% variations in the measured $P_{\text{loss},H}$ or ±18% variations in the measured $P_{\text{loss},F}$ does not change the result. The relatively low sensitivity of (7.31) with respect to $P_{\text{loss},F}$ and $P_{\text{loss},H}$ implies that variation in the operating point of the converter, which can be caused by the load variation, does not necessarily change the conclusion. The sensitivity to the ambient temperature, T_a, is even much less. According to (7.31), ±430% variation in the ambient temperature does not change the result as well.

However, the final conclusion is considerably sensitive to $R_{\text{th,ca}}$. Thus, one can expect the relative reliability ranking of parallel and standby configurations to change by utilization of a heat sink. For instance, a typical heat sink with the thermal resistance of 12˚C/W is considered here. Assuming the same operating point for the converters, the half-load and full-load power losses of the MOSFETs are the same as those given in Table II. All variables in (7.31) remain the same except for $R_{\text{th,ca}}$, which is the thermal resistance of the heat sink. One can observe that by changing $R_{\text{th,ca}}$ from 62˚C/W (without heat

sink) to 12˚C/W (with heat sink), (7.31) will no longer be satisfied. In other words, using this specific heat sink makes the standby configuration more reliable than parallel configuration.

However, if a different heat sink with the thermal resistance of 45˚C/W is used, the parallel configuration stays as the more reliable option. For the given values of $P_{\text{loss},F}$, $P_{\text{loss},H}$, and T_a, the critical $R_{\text{th,ca}}$, for which the parallel and standby configurations have the same MTTF, is 38˚C/W. For every heat sink with higher $R_{\text{th,ca}}$, the parallel configuration is more reliable, whereas, using a heat sink with $R_{\text{th,ca}}$ less than 38˚C/W makes the standby configuration the more reliable option.

In general, for a specific power semiconductor with known k_1, k_2, $R_{th,jc}$, ambient temperature T_a, half-load power loss $P_{loss,H}$, and full-load power loss $P_{loss,F}$, the critical heat sink thermal resistance, $R_{th,ca}^{\text{critical}}$, for which parallel and standby configurations are equally reliable can be found using (7.31):

$$R_{th,ca}^{\text{critical}} = \frac{(1-k_1)\ T_a + k_2}{k_1 P_{\text{loss},F} - P_{\text{loss},H}} - R_{th,jc}. \tag{7.35}$$

For any heat sink with thermal resistance higher than $R_{th,ca}^{\text{critical}}$, the parallel configuration is more reliable, whereas, for the heat sinks with thermal resistance less than $R_{th,ca}^{\text{critical}}$, standby configuration is the more reliable option.

7.8 Detailed Derivation of the Boundary Condition

The boundary condition, where parallel and standby configurations have the same MTTF, is given by (7.18). The coefficient K of (7.18) has been expressed in terms of $\pi_{T,H}$ and $\pi_{T,F}$ in (7.23). Equating (7.18) and (7.23), one may find

$$\frac{\pi_{T,H}}{\pi_{T,F}} = \frac{1}{2(1+P_{sb}^c - P_p^c)}. \tag{7.36}$$

To ensure a fair comparison between parallel and standby configurations, the same fault coverage capability is assumed for both configurations ($P_p^c = P_{sb}^c$). This assumption simplifies the right side of (7.36) to $1/2$.

The temperature factor, π_T, of power MOSFETs is given in (7.24) according to MIL-HDBK-217F [131]. The temperature factors of the other semiconductor types are also given in [131]; They all have the general form of

$$\pi_T = e^{-a\left(\frac{1}{T_j+b}-\frac{1}{c}\right)} \tag{7.37}$$

where a, b, and c are constants that depend on the type of the power semiconductor. Using (7.36) and (7.37), the boundary condition can be expressed as

$$\frac{e^{-a\left(\frac{1}{T_{jH}+b}-\frac{1}{c}\right)}}{e^{-a\left(\frac{1}{T_{jF}+b}-\frac{1}{c}\right)}} = \frac{1}{2}. \tag{7.38}$$

Manipulating (7.38) leads to

$$\frac{1}{T_{jH}+b} - \frac{1}{T_{jF}+b} = \frac{\ln 2}{a}. \tag{7.39}$$

Equation (7.39) can be rearranged in terms of T_{jH} as

$$T_{jH} = \frac{\left(1-\frac{b}{a}\ln 2\right)T_{jF} - \frac{b^2}{a}\ln 2}{\frac{\ln 2}{a}T_{jF} + \left(1+\frac{b}{a}\ln 2\right)}. \tag{7.40}$$

Replacing a, b, and c in (7.40) by their corresponding values for MOSFETs results in (7.25). For a MOSFET, the first term in the denominator of (7.40), $(\ln 2)T_{jF}/a$, is $3.6 \times 10^{-4}T_{jF}$, whereas the second term, $1 + (b/a)\ln 2$, is 1.1. Thus, the first term, $(\ln 2)T_{jF}/a$, can be safely neglected. The same conclusion is valid for other a, b, and c values belonging to other power semiconductor types. Thus, the boundary condition in (7.40) can be approximated as

$$T_{jH} = \left(\frac{a-b\ln 2}{a+b\ln 2}\right)T_{jF} - \left(\frac{b^2\ln 2}{a+b\ln 2}\right). \tag{7.41}$$

Replacing a, b, and c in (7.41) by their corresponding values for MOSFETs results in (7.26). Similarly, replacing them by their corresponding values for the other types of semiconductors gives the boundary conditions described in Table I. The linear shape of boundary curve in Figure 7.6(c) also verifies the validity of the approximation that led to the linear relationship in (7.41).

CHAPTER 8

CONCLUSIONS

8.1 Conclusion

Two new multiple-input multiple-output dc-dc converter topologies, which can be used in multiple-source multiple-load energy systems, have been proposed in chapters 2 and 3. Specific switching strategies have been presented for the converters and their operational principles have been analyzed based on the proposed switching schemes. The state-space average models of the converters have been developed based on the proposed switching schemes. Dynamic characterization, loss and efficiency modeling, and sensitivity analysis studies are performed. The models have been linearized and different input-to-output transfer functions have been derived. Proper control strategies have been proposed that enable regulating the input powers, coming from diversified energy sources, in addition to the output voltages. The performances of the converters have been evaluated by different hardware measurements as well as numerical simulations.

A discrete-time modeling framework has been proposed for multiport and multiphase dc-dc converters in chapter 4 and 5, respectively. This modeling technique considers salient aspects of such converters that make the use of conventional continuous-time modeling prone to failure. The approximations imposed by the use of averaging techniques have been avoided by using the Floquet theory. The influence of effective duty cycles has been modeled by considering the multiple propagation paths during each switching period in multiport converters. The proposed model has been verified through switching-level simulations and hardware measurements. It has been shown that the developed model can properly predict the frequency responses whereas the conventional continuous-time average model fails in several cases.

A flexible current sharing method, based on the concept of cooperative control in multi-agent systems, has been proposed for multiphase dc-dc converters in chapter 6. The effects of the communication graph on the stability and fault-tolerance of the multiphase systems have been analyzed.

Using the proposed control method, a plug-and-play environment has been realized. A systematic framework has been proposed to analyze the stability and performance measures of the system using any desired communication graph. Hardware measurements have verified the modularity, plug-and-play ability, fault tolerance, and dynamic performance of the proposed control method.

To improve the reliability of multiport dc-dc converters, two redundant switch structures, namely parallel and standby configurations, have been examined for power semiconductor switches in chapter 7. Analytical models have been developed to compare the reliabilities of parallel and standby switch configurations. It has been shown that the junction temperature of the semiconductor switches in steady state is a key element in determining the more reliable configuration. The expected lifetime of each configuration has been expressed in terms of the junction temperature of the switches in half-load and full-load operation modes. The junction temperature range in which the parallel configuration is more reliable has been determined for different types of power semiconductor switches. The effects of converter's power level and ambient temperature on the junction temperature and, consequently, on determining the more reliable configuration have been discussed. The sensitivity of the results with respect to the underlying parameters has been analyzed. It has been shown that the thermal resistance of heat sink is a critical factor in determining the more reliable configuration. It is demonstrated that, for high-power converters in regular ambient conditions, the parallel configuration is likely to be more reliable than its standby counterpart. This is in direct contrast to the conventional reliability wisdom that the standby configuration is always more reliable. On the other hand, it is shown that for low-power converters operating at high ambient temperatures, the standby configuration is likely to be more reliable. A necessary and sufficient condition is presented to determine which configuration is more reliable for a converter with arbitrary parameters (e.g. ambient temperature, power level).

8.2 Future works

Future works can have three main directions, namely, topology synthesis, controller design, and reliability improvement for multiport dc energy conversion systems. Synthesizing new multiport

converters with enhanced performance, based on the proposed topologies, can be of paramount value (for instance, adding maximum power point tracking feature for one input source that is connected to a PV panel). Developing more robust control strategies for the multiport and multiphase converters can also be subjects of future works. The proposed cooperative control for multiphase dc-dc converters can be employed for current and phase synchronization in modular rectifiers or inverters. From the reliability perspective, future works can address more complex redundant structures of power semiconductor switches for reliability improvement purposes. Development of redundant switch modules with integrated fault detection and isolation mechanism can also be another interesting subject for future works. Such new switch modules will be able to provide high reliability and prolonged lifetime for mission-critical applications.

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BIOGRAPHICAL INFORMATION

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