FABRICATION AND CHARACTERIZATION OF SINGLE ELECTRON DEVICE AND STUDY OF ENERGY FILTERING IN SINGLE ELECTRON TRANSPORT

by

LIANG-CHIEH MA

Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

THE UNIVERSITY OF TEXAS AT ARLINGTON

December 2013

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Acknowledgements

First, I want to thank my advisor, Dr. Seong Jin Koh, for his guidance in my pursuit of a PhD. His support in all aspects of the process allowed me to focus on my research without worrying about other problems. I also want to thank my group members: Pradeep, Manouchehr, Derek and Vinay who encouraged me and actively helped support my projects almost every day.

I would also like to thank the people who helped me while I worked in the clean room at Nanofab. Dennis and Kevin offered immense help in the utilization of the tools used in this study.

My parents inspired me to begin this journey to pursue my Doctoral degree. I would not have ever completed my degree without their support and encouragement. Thank you.

Most of all, I thank Mei-Lin Wu, my fiancée, for waiting such a long time while I studied in the US. In the most difficult of times when nothing seemed to work, she always found a way to encourage me with the motivation to carry on. I cannot even express my appreciation to her with words.

This study was supported by the Office of Naval Research under Grant No. N00014-05-1-0030 and N00014-12-1-0492, by the National Science Foundation under Grant No. ECS-0449958 and ECCS-0925997, by the US Army Research Office under Grant No. W911NF-12-1-0071, and by the Texas Higher Education Coordinating Board under Grant No. 003656-0014-2006

November 25, 2013

Abstract

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Liang-Chieh Ma, PhD

The University of Texas at Arlington, 2013

Supervising Professor: Seong Jin Koh

Single electron devices, in which transport of single electrons is precisely controlled, hold a great promise as important components of future electronic devices and sensors. However, technical challenges have prevented their implementations to practical electronic and sensing systems. First of all, the fabrication of single electron devices requires their components to be defined and arranged in nanoscale precision, a great challenge for a large-scale fabrication. Secondly, for room temperature operation, the single-electron charging energy should be much larger than the room-temperature thermal energy, ~25 meV, requiring use of extremely small Coulomb island, which is difficult to control. This has limited the operation of most single-electron devices to low temperatures, requiring liquid N_2 or liquid He cooling, a great obstacle for practical applications. In this thesis, I present systematic study to address these critical problems. First, I demonstrate a method which allows large scale fabrication of single electron devices using CMOS compatible processing technology. Second, I demonstrate a method that suppresses the thermal excitation of electrons and cools down electron temperature, enabling room-temperature operation of single electron devices.

By analyzing the single electron device from statistical thermodynamics point of view, a model was constructed to describe single-electron tunneling events. In this

model, the free energy change associated with a single tunneling event was formulated, from which the tunneling rates were calculated using the Fermi Golden rule. The I-V characteristics calculated from this model were in exact match with the widely used single electron device simulator SIMON.

A new vertically aligned electrode structure of single electron device was designed and fabricated. CMOS-compatible fabrication process allowed a large scale fabrication of single electron devices. The source and drain were stacked vertically and separated by a thin dielectric layer (~10 nm). The deposition of dielectric layers was well controlled using PECVD (plasma-enhanced chemical vapor deposition) or ALD. (atomic layer deposition). Gold nanoparticles serving as Coulomb islands were attached on the exposed sidewall of the dielectric layer. Most importantly, a quantum well structure was formed between the source and tunneling barrier. The discrete energy state of the quantum well was utilized as an energy filter, serving as a key component for room-temperature operation of single electron devices.

Clear Coulomb blockade, Coulomb staircase and Coulomb oscillation were demonstrated at room temperature by the fabricated single electron devices. I-V measurements done at different temperatures showed suppression in Fermi-Dirac thermal smearing. This was attributed to the electron energy filtering through the discrete energy level of the quantum well. When electron tunnels between the quantum well and Coulomb island, the energy distribution of electrons is squeezed. Through this energy filtering effect, cold electrons whose temperature is as low as ~45K can be created and transported at room temperature without physically cooling the device.

Since the tunnel junctions play an important role for the single electron transport, a new structure of single electron device was proposed in order to gain more control in manipulating the tunnel junctions. A structure of silicon nanopillar single electron device

was proposed and its fabrication procedure was designed. Cr nanopillars were fabricated to demonstrate the feasibility of the proposed nanopillar single electron device.

In fabricating nanoscale devices, precise placement of nanoscale objects (e.g. nanoparticles) onto targeted substrate positions is critical. A new method for precise placement of nanoparticles, electrostatic funneling, was developed. In this method, the electrostatic guiding structure formed using self-assembled monolayers of organic molecules guides charged nanoparticles onto desired target positions with nanoscale precision. This electrostatic funneling method could be used to increase the yield of single electron device fabrication.

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Chapter 1

Introduction

1.1 Overview

The first observation of the Coulomb blockade phenomena was carried out by *Goreter* [1] back in 1951. The observation was conducted through a granular thin film with a suppressed conductivity. In 1969, Lambe and Jaklevic [2] investigated charge quantization in a single-electron, box like structure. However the research in single electron devices was not very active until mid-1980 when, the single electron transistors were introduced by Averin and Likharve [3]. All the research in single electron devices were limited to a very low operation temperature due to the insufficient ability to make nanoscale objects at that time.

Recently, due to the demand from the microelectronic industry, there is a continuous evolution of fabrication tools, materials, and processes to keep up with the need of increasing device density. By the advance of nanofabrication processes and technology, fabrications of nanoscaled objects are becoming feasible. A large amount of researches is focused on developing and fabricating nanoscale devices with smaller size, faster speed and lower power consumption. Single electron devices have been intensively studied because of it’s unique multifunctionality with ultra-low power consumption and scalability down to nanometer range [4, 5].

1.2 Single Electron Devices

Single electron devices control the transport of individual electrons by way of the charging energy. It is composed of a source, drain, and tunnel junction with a Coulomb island in between. The tunnel junctions are insulators which separate the source, Coulomb island and drain. Electron transport in the device is via tunneling sequentially to each of the components. Currents in the single electron device are considered not continuous since the charging energy of the Coulomb island only allows the tunneling of one electron at a time.

The single electron device has attracting features over other devices including its ultra-low power consumption, scalability down to the nanometer range [6, 7], and it's high sensitivity to a small amount of charge [8-13]. However, a critical requirement for fabricating single electron device lies in the manipulation of its components in the right positions. Although several methods were proposed for this issue such as e-beam lithography [14], shadow mask evaporation [15], electromigrations [12, 16, 17], mechanically controlled break junctions [18, 19], electrodeposition [20, 21], nanoscale oxidation [22, 23], and scanning tunneling microscopy [13, 24], the fabrication is still limited to a small number of devices that can be made at a time. This is limits the practical applications for single electron device. Therefore a parallel process which allows the large scale fabrication of single electron device is still in demand.

1.3 Organization of This Thesis

The main objective of this study is to fabricate single electron devices which can be operated at room temperature. The fabrication process needs to be in parallel process; therefore large scale of fabrication is possible. In addition, to manipulate the thermal excitation and electron temperature in our device is also important goal.

In chapter 2, a basic structure of double junction single electron device will first be introduced with the arrangement for each component in this structure and their functions. An equivalent circuit will be presented to explain the electron transport through these components.

In chapter 3, since transportation of electron through these components are reflected from the change of charge and energy stored in each component, equations that describe and govern the transportation of electrons will be derived and explained in the aspect of energy through the assisting of energy diagram. Derivation is started from the fundamentals of statistical thermal dynamics then applies it to the system of our single electron device. After the derivations, the featured phenomena of single electron transport will be demonstrated and explained. Finally, a model describing the behavior of electron transport in single electron device will be built.

In Chapter 4, detailed fabrication process of single electron device will be carried. All the fabrication process and techniques used are compatible with current CMOS technology. Starting on a 4 inch silicon wafer, fabrication process are composed of thermal oxidation, optical lithography, E-beam evaporation, plasma enhanced chemical vapor deposition (PECVD), formation of self-assembled monolayer, RF sputtering, and reactive ion etch (RIE).

In chapter 5, electrical characterization of the fabricated single electron devices will be carried at both low and high temperatures. Due to the features of our fabrication process, fabricated device can have varied configurations thus demonstrate different I-V characteristic for the behavior of single electron transport. Various I-V characteristic of single electron device will be presented and followed with the explanation of how the configuration of the device corresponds to the observed I-V. Single electron transport was found in our device both at low and room temperatures. While comparing our observation with theoretical calculations at various temperatures, it was revealed that there is an energy filtering effect in our fabricated device. Since this effect can have cold electron transporting at room temperature, it may hold a great promise for wide applications in fabrication of quantum device.

After demonstration and discussion of the single electron behavior in fabricated device at different temperatures, a nanopillar single electron device was proposed and fabricated for a different direction of investigation of tunnel junctions. Silicon nanopillar single electron devices are fabricated for this purpose. The detailed structure and fabrication process will be presented in Chapter 7. In addition, the actual fabricated nanopillar with a diameter of 50 nm will also be shown in the SEM image.

Chapter 8 will focus on placing the nanoparticle with nanoscale precision. Experimental procedure of this method and the application of gold nanoparticle placement will be presented. Following with the result showing the effectiveness, a model will be created to assist in the understanding of this electrostatic funneling effect for precise nanoparticle placement.

Chapter 2

Overview of Single Electron Device

2.1 Introduction

The working principle of single electron device will be discussed and explained with fundamentals in this chapter. The electron transportation in between the components of the single electron device was represented in an equivalent circuit in order to establish the relation between the free energy and device parameters such as capacitance and external bias. The outline of this chapter is described as follows:

- Structure of the single electron device
- Tunnel junction
- Double barrier tunnel junction (equivalent circuit)

2.2 Structure of Single Electron Device

The basic structure of SED is composed of source, drain, two tunnel junctions and a coulomb island as shown in Figure 2.1. Source, drain and Coulomb Island are conductors and they are separated by two tunnel junctions which are insulators. When an external bias is applied, the electrons will tunnel from source to drain by tunneling through the tunnel junctions.

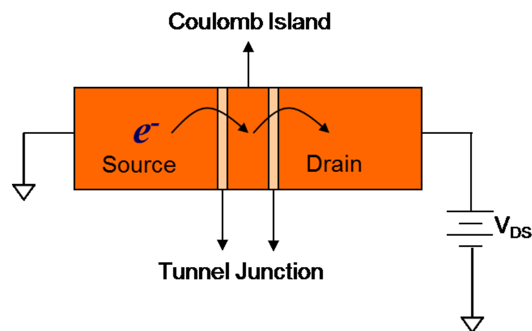

Figure 2.1 Basic structure of single electron device. Electron tunnels through tunnel junctions from source to Coulomb Island then drain.

The tunneling current is governed by the tunneling rate between the two tunneling junctions and the Coulomb island.

2.3 Tunnel Junction

Tunnel junctions are made by a thin layer of dielectric material which isolates the source and coulomb island. Electrons can only be transported through the tunnel junction by tunneling because they are blocked by the potential barrier from the tunnel junction. The potential barrier is determined by the difference of the work function between the source and junction materials. The tunneling current will drop exponentially with the barrier width. The thickness of the tunnel junction will be less than 5 nm in order to observe the tunnel current. Since the tunnel junction is a dielectric between two conductors, the concept of parallel plate capacitor could be applied. In Figure 2.2, an equivalent circuit of tunnel junction is represented by a capacitor and a resistor connected in parallel. C and R in the equivalent circuit are the capacitance and tunneling resistance of the tunnel junction. It should be notice here that tunneling resistance is different from the Ohmic resistance where the current was described as a continuous charge flow and obey the Ohm's law. In a single electron device, the electron transportation is discrete. The tunneling resistance is governed by the tunneling rate across the tunnel junction.

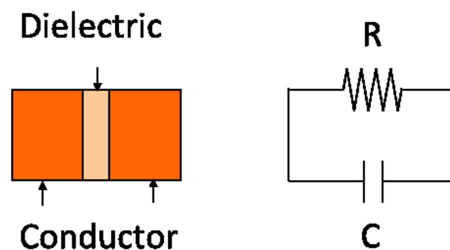

Figure 2.2 Tunnel junction and its equivalent circuit. Capacitance and tunneling resistance are represented by C and R, respectively.

2.4 Double Junction Single Electron Device

A structure of double junction SED and its equivalent circuit are illustrated in Figure 2.3 (a) and (b). The Coulomb Island, which is a quantum dot (nanoparticle), is isolated by two tunnel junctions between a source and a drain. From the equivalent circuit in Figure 2.3 (b), two tunnel junctions and a quantum dot are considered to be connected with each other in series. Source and drain electrode are just represented by the voltage source V_S, and V_D, respectively.

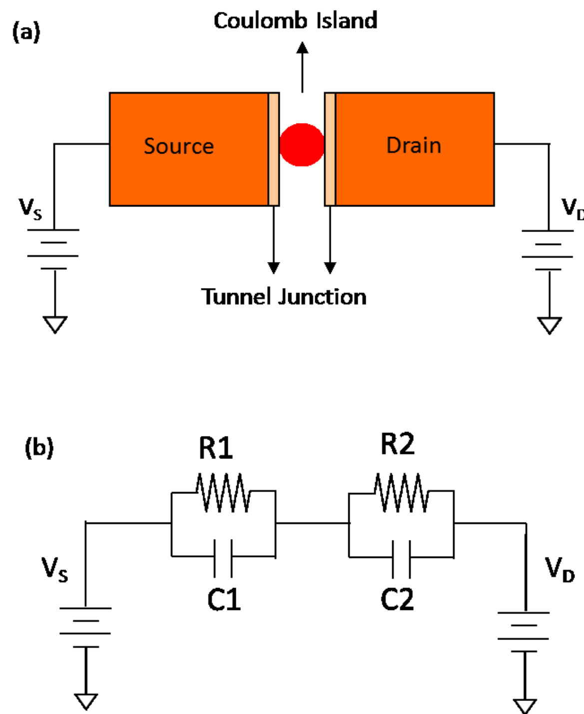

Figure 2.3 (a) Structure of double junction single electron device. (b) Equivalent circuit of the double junction single electron device.

2.4.1 Charges and Energy Stored in the Double Junction Single Electron Device

In the equivalent circuit, tunnel junctions are considered as a parallel plate capacitor [6]. When connected with an external source drain bias, the tunnel junctions will be charged and charges will be accumulated in the junctions. An internal electric field will

build up due to the accumulated charges and thus resists further charging of the tunnel junction. The energy required to further charge the tunnel junction to reach a charge value Q can be consider as the energy stored at the tunnel junction when a tunnel junction caries a charge of Q.

In Figure 2.4, the charges Q_S and Q_D carried by the double junctions T_S and T_D can be represented by the capacitance C_S and C_D and the voltage drop across T_S and T_D. Consider in a parallel plate capacitor, a charge q is the obtained by the product of the capacitance C and voltage V across the parallel plate.

$$q = C.V \tag{2.1}$$

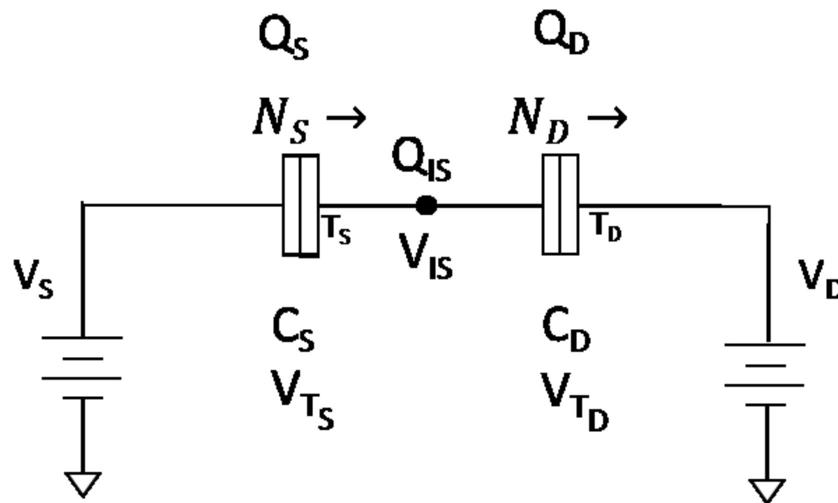

Figure 2.4 Equivalent circuit of the double junction single electron device with a coulomb island. The source and drain bias V_S andV_D are applied to the tunnel junctions T_S and T_D, respectively. The voltage drop across T_S and T_D are V_{T_S} and V_{T_D}. The coulomb island is represented by the black dot and a voltage drop across is V_{IS}. Capacitive charges accumulated in the tunnel junctions T_S and T_D are Q_S and Q_D, respectively. Junction capacitances are C_S and C_D for T_S and T_D, respectively. N_S and N_D are integer numbers of electrons which are tunnel in and out of the coulomb island, respectively. Net charge in the coulomb island is represented by Q_{IS}.

When the source and drain connect with bias V_S and V_D, the voltage drop across the quantum dot can be defined as V_{IS}. Then the voltage drop across T_S and T_D are:

$$V_{T_S} = V_{IS} - V_S \tag{2.2}$$

$$V_{T_D} = V_D - V_{IS} \tag{2.3}$$

The charges Q_S and Q_D stored in the tunnel junctions T_S and T_D are:

$$Q_s = C_S V_{T_S} \tag{2.4}$$

$$Q_D = C_D V_{T_D} \tag{2.5}$$

Now let us consider the net charges Q_{IS} in the. Before an external bias applied, there are fractional electron charges already reside on the coulomb island. It is referred to the background charges Q_0 [25]. It could be induced by the work function difference between the electrodes and impurities charges located on the tunnel junctions [6, 26].The net charges Q_{IS} is the sum of the background charges and the charges from excess electrons accumulated on the coulomb island through tunneling.

$$Q_{IS} = -Ne + Q_0 \tag{2.6}$$

where N is the number of excess electrons in the coulomb island. N can be obtained from the number of electrons, N_S, tunneled into the coulomb island from source, substrates the number of electrons, N_D, tunneled out from the coulomb island to drain.

$$N = N_S - N_D \tag{2.7}$$

The net charges accumulated on the coulomb island can also be represented by equation (2.6),

$$Q_{IS} = Q_s - Q_D \tag{2.8}$$

Substituting Q_{IS} with equation (2.6) and Q_S, Q_D with equation (2.4), (2.5), we can obtain V_{IS} by:

$$-Ne + Q_0 = C_S(V_{IS} - V_S) - C_D(V_D - V_{IS})$$

$$\Rightarrow -Ne + Q_0 = C_S V_{IS} - C_S V_S - C_D V_D + C_D V_{IS}$$

$$\Rightarrow -Ne + Q_0 = V_{IS}(C_S + C_D) - C_S V_S - C_D V_D$$

$$\therefore V_{IS} = \frac{C_S V_S + C_D V_D - (Ne - Q_0)}{C_S + C_D} \tag{2.9}$$

Since $C_S + C_D$ represent the total capacitance of the single electron device, we can define C_{TOT} as:

$$C_{TOT} \equiv C_s + C_D$$

$$\therefore \mathrm{V}_{IS} = \frac{C_S V_S + C_D \mathrm{V}_D - (Ne - Q_0)}{C_{TOT}} \tag{2.10}$$

As the V_{IS} was obtained, the voltage drop V_{T_S} and V_{T_D}across the tunnel junction in equation (2.2) and (2.3) can be rewrite by replacing V_{IS} from equation (2.10),

$$\Rightarrow V_{T_\mathrm{S}} = \frac{C_S V_S + C_D \mathrm{V}_D - (Ne - Q_0)}{C_{TOT}} - V_S$$

$$\Rightarrow V_{T_\mathrm{S}} = \frac{C_S V_S + C_D \mathrm{V}_D - (Ne - Q_0) - C_s V_S - C_D V_S}{C_{TOT}}$$

$$\Rightarrow V_{T_\mathrm{S}} = \frac{C_D \mathrm{V}_D - C_D V_S - (Ne - Q_0)}{C_{TOT}}$$

$$\Rightarrow V_{T_\mathrm{S}} = \frac{C_D (\mathrm{V}_D - V_S) - (Ne - Q_0)}{C_{TOT}}$$

$$\therefore V_{T_\mathrm{S}} = \frac{C_D \mathrm{V}_{DS} - (Ne - Q_0)}{C_{TOT}} \tag{2.11}$$

where $V_{DS} \equiv V_D - V_S$. Similarly, V_{T_D} can be rewrite as:

$$\Rightarrow V_{T_\mathrm{D}} = V_D - \frac{C_S V_S + C_D \mathrm{V}_D - (Ne - Q_0)}{C_{TOT}}$$

$$\Rightarrow V_{T_\mathrm{D}} = \frac{C_s V_D + C_D V_D - C_S V_S - C_D \mathrm{V}_D + (Ne - Q_0)}{C_{TOT}}$$

$$\Rightarrow V_{T_\mathrm{D}} = \frac{C_S (V_D - V_S) + (Ne - Q_0)}{C_{TOT}}$$

$$\therefore V_{T_\mathrm{D}} = \frac{C_S V_{DS} + (Ne - Q_0)}{C_{TOT}} \tag{2.12}$$

The total electrostatic energy due to the capacitive charges in the system of double junction SED can be obtained from adding up the energy stored at two tunnel junctions. The electrostatic energy stored at a parallel capacitor is:

$$E = \int_0^Q \frac{q}{C} dq = \frac{Q^2}{2C} \tag{2.13}$$

where C is the capacitance and Q is the charges in the capacitor.

For the double junction single electron device, total electrostatic energy is the sum of the energy stored at each junction, thus we have:

$$E_{TOT} = \frac{{Q_S}^2}{2C_s} + \frac{{Q_D}^2}{2C_D} \tag{2.14}$$

Insert the Q_S and Q_D from equation (2.4) and (2.5), E_{TOT} becomes:

$$E_{TOT} = \frac{{C_S}^2{V_{T_S}}^2}{2C_s} + \frac{{C_D}^2{V_{T_D}}^2}{2C_D}$$

$$\Rightarrow E_{TOT} = \frac{1}{2}\left(C_s{V_{T_S}}^2 + C_D{V_{T_D}}^2\right)$$

Replace the V_{T_S} and V_{T_D} from equation (2.11) and (2.12), respectively; the total electrostatic energy is then expressed as:

$$\Rightarrow E_{TOT} = \frac{1}{2}C_s\left[\frac{C_D V_{DS} - (Ne - Q_0)}{C_{TOT}}\right]^2 + \frac{1}{2}C_D\left[\frac{C_S V_{DS} + (Ne - Q_0)}{C_{TOT}}\right]^2$$

$$\Rightarrow E_{TOT} = \frac{C_s}{2{C_{TOT}}^2}\left[C_D V_{DS} - (Ne - Q_0)\right]^2 + \frac{C_D}{2{C_{TOT}}^2}\left[C_S V_{DS} + (Ne - Q_0)\right]^2$$

$$\Rightarrow E_{TOT} = \frac{1}{2{C_{TOT}}^2}\left[C_s{C_D}^2{V_{DS}}^2 + C_s(Ne - Q_0)^2 - 2C_sC_DV_{DS}(Ne - Q_0) + C_D{C_S}^2{V_{DS}}^2 + C_D(Ne - Q_0)^2 + 2C_DC_SV_{DS}(Ne - Q_0)\right]$$

$$\Rightarrow E_{TOT} = \frac{1}{2{C_{TOT}}^2}\left[C_sC_D{V_{DS}}^2(C_S + C_D) + (Ne - Q_0)^2(C_S + C_D)\right]$$

$$\therefore E_{TOT} = \frac{1}{2C_{TOT}}\left[C_sC_D{V_{DS}}^2 + (Ne - Q_0)^2\right] \tag{2.15}$$

The total electrostatic energy E_{TOT} will change if one electron is added or removed from the coulomb island. The excess number of electrons in coulomb island, N, will be $N + 1$ for addition and $N - 1$ for subtraction of one electron on the coulomb island. The change of total electrostatic energy $\triangle E_{TOT}$ can be obtained by:

$$\pm E_{TOT} = \frac{1}{2C_{TOT}}\left\{C_sC_D{V_{DS}}^2 + [(N+1)e - Q_0]^2\right\} - \frac{1}{2C_{TOT}}\left[C_sC_D{V_{DS}}^2 + (Ne - Q_0)^2\right] \Rightarrow \pm E_{TOT} = \frac{1}{2C_{TOT}}\{[(N+1)e - Q_0]^2 - (Ne - Q_0)^2\}$$

$$\Rightarrow \pm E_{TOT} = \frac{1}{2C_{TOT}}\{(N+1)e - Q_0 + (Ne - Q_0)\}\{(N+1)e - Q_0 - (Ne - Q_0)\}$$

$$\Rightarrow \pm E_{TOT} = \frac{1}{2C_{TOT}}(2Ne - 2Q_0 + e)(e)$$

$$\Rightarrow \pm E_{TOT} = \frac{e}{C_{TOT}}\left[\frac{e}{2} + (Ne - Q_0)\right] \tag{2.16}$$

where positive and negative sign indicates the addition and subtraction of an electron on the coulomb island, respectively.

Chapter 3

Study of Single Electron Transport from Statistical Thermodynamics Point of view

3.1 Free Energy Change in Single Electron System

We consider a system $\mathcal{s}$ is in contact with a thermal and particle reservoir $\mathcal{R}$, as showing in Figure 3.1.

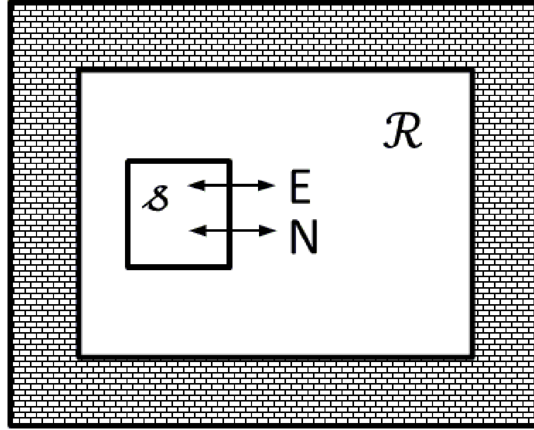

Figure 3.1 A closed system in which a system is in contact with a thermal reservoir and particle reservoir.

The system $\mathcal{s}$ can exchange energy E and particles N with its reservoir $\mathcal{R}$ within the wall. No energy and particles exchange allowed through the insulated wall. The total energy E_{TOT} and total number of particles N_{TOT} for the entire system inside the wall are constant. The entropy S is defined as:

$$S \equiv k \ln \mathcal{g} \tag{3.1}$$

where k is Boltzmann constant and $\mathcal{g}$ is the number of accessible states. $\mathcal{g}$ can be expressed as:

$$\mathcal{g} = \exp\left(\frac{S}{k}\right) \tag{3.2}$$

We can define the probability $P(j)$ and $P(k)$ for the system $\mathcal{s}$ at state j and k with the energies $\mathcal{E}_j$, and $\mathcal{E}_k$, respectively. Then the ratio of $P(j)$ to $P(k)$ can be written as:

$$\frac{P(j)}{P(k)} = \frac{g_{res}(E_{TOT} - \mathcal{E}_j)}{g_{res}(E_{TOT} - \mathcal{E}_k)} \tag{3.3}$$

where $g_{res}(E_{TOT} - \mathcal{E}_j)$ is the number of accessible states for the reservoir with energy $E_{TOT} - \mathcal{E}_j$.

The probability of the system in a state is described by the number of accessible states in the reservoir can be understand since the system was fixed at a state, the number of accessible state is 1 for the system. The reservoir can have number of accessible states g_{res} while the system is at a fixed state. Then the total number of the accessible states for the entire system (system $\mathcal{s}$ and reservoir $\mathcal{R}$) is $1 \times g_{res} = g_{res}$. For the system in the state j with energy $\mathcal{E}_j$, total number of accessible states is $1 \times g_{res}(E_{TOT} - \mathcal{E}_j) = g_{res}(E_{TOT} - \mathcal{E}_j)$. Inserting the equation (2.18) in to (2.19), we can have:

$$\frac{P(j)}{P(k)} = \frac{exp\left[\frac{S_{res}(E_{TOT} - \mathcal{E}_j, N_{TOT} - N_j)}{k}\right]}{exp\left[\frac{S_{res}(E_{TOT} - \mathcal{E}_k, N_{TOT} - N_k)}{k}\right]} \tag{3.4}$$

where $S_{res}(E_{TOT} - \mathcal{E}_j, N_{TOT} - N_j)$ and $S_{res}(E_{TOT} - \mathcal{E}_k, N_{TOT} - N_k)$ is the entropy of the reservoir when system is in state j and k, respectively. S is a function of energy and number of the particles thus it is described as $S(E, N)$.

In equation (2.19), $S_{res}(E_{TOT} - \mathcal{E}_j, N_{TOT} - N_j)$ can be described in the form of partial differentiation as:

$$S_{res}(E_{TOT} - \mathcal{E}_j, N_{TOT} - N_j) = S_{res}(E_{TOT}, N_{TOT}) + \left(\frac{\partial S_{res}}{\partial E_{res}}\right)_{N_{res}} .(-\mathcal{E}_j) + \left(\frac{\partial S_{res}}{\partial N_{res}}\right)_{E_{res}} .(-N_j) \tag{3.5}$$

From the definition of entropy in thermal dynamics, we know

$$\left(\frac{\partial S_{res}}{\partial E_{res}}\right)_{N_{res}} = \frac{1}{T_{res}} = \frac{1}{T} \tag{3.6}$$

where T_{res} and T is the temperature of the reservoir and system, respectively. Because there is no heat transferred, system and its reservoir are in the same temperature for $T = T_{res}$.

From the partial derivative of entropy, one can obtain

$$\left(\frac{\partial S_{res}}{\partial N_{res}}\right)_{E_{res}} = -\frac{\left(\frac{\partial E_{res}}{\partial N_{res}}\right)_{S_{res}}}{\left(\frac{\partial E_{res}}{\partial S_{res}}\right)_{N_{res}}} = -\frac{\mu}{T} \tag{3.7}$$

where μ is chemical potential. Substitute the terms $\left(\frac{\partial S_{res}}{\partial E_{res}}\right)_{N_{res}}$ and $\left(\frac{\partial S_{res}}{\partial N_{res}}\right)_{E_{res}}$ in equation (2.20) with (2.21) and (2.22),

$$S_{res}\left(E_{TOT} - \mathcal{E}_j, N_{TOT} - N_j\right) = S_{res}(E_{TOT}, N_{TOT}) - \frac{\mathcal{E}_j}{T} + \frac{\mu}{T} N_j \tag{3.8}$$

The term S_{res} in the equation (2.19) now can be replaced with (2.20) to become:

$$\frac{P(j)}{P(k)} = \frac{exp\left[\frac{S_{res}(E_{TOT}, N_{TOT}) - \frac{\mathcal{E}_j}{T} + \frac{\mu}{T} N_j}{k}\right]}{exp\left[\frac{S_{res}(E_{TOT}, N_{TOT}) - \frac{\mathcal{E}_k}{T} + \frac{\mu}{T} N_k}{k}\right]}$$

$$\Rightarrow \frac{P(j)}{P(k)} = \frac{exp\left[\frac{S_{res}(E_{TOT}, N_{TOT})}{k}\right] . \, exp\left[\frac{1}{k}\left(-\frac{\mathcal{E}_j}{T} + \frac{\mu}{T} N_j\right)\right]}{exp\left[\frac{S_{res}(E_{TOT}, N_{TOT})}{k}\right] . \, exp\left[\frac{1}{k}\left(-\frac{\mathcal{E}_j}{T} + \frac{\mu}{T} N_j\right)\right]}$$

$$\Rightarrow \frac{P(j)}{P(k)} = \frac{exp\left[\frac{1}{k}\left(-\frac{\mathcal{E}_j}{T} + \frac{\mu}{T} N_j\right)\right]}{exp\left[\frac{1}{k}\left(-\frac{\mathcal{E}_j}{T} + \frac{\mu}{T} N_j\right)\right]}$$

$$\Rightarrow \frac{P(j)}{P(k)} = \frac{exp \frac{-1}{kT}\left(\mathcal{E}_j + \mu N_j\right)}{exp \frac{-1}{kT}\left(\mathcal{E}_k + \mu N_k\right)} \tag{3.9}$$

The grand partition function, Z, can be defined as:

$$Z = \sum_{l} exp \frac{-1}{kT}\left(\mathcal{E}_l - \mu N_l\right) \tag{3.10}$$

where l is the total number for all possible states in the system.

If the probability for a system being in a state is added up for all possible states, the sum of the probability should be equal to the unity 1. It can be represented as $\sum_l P(l)$ in equation (2.21),

$$\frac{P(j)}{\sum_l P(l)} = \frac{exp\frac{-1}{kT}(\mathcal{E}_j + \mu N_j)}{\sum_l exp\frac{-1}{kT}(\mathcal{E}_l - \mu N_l)}$$

$$\Rightarrow \frac{P(j)}{1} = \frac{exp\frac{-1}{kT}(\mathcal{E}_j + \mu N_j)}{Z}$$

$$\Rightarrow P(j) = \frac{1}{Z} exp\frac{-1}{kT}(\mathcal{E}_j + \mu N_j) \tag{3.11}$$

Now consider three reservoir A, B and C are connected to the system $\mathcal{s}$. When system is in state j, with energy $\mathcal{E}_l$, as shown in Figure 3.2. We can describe the condition for the system as follows.

Total number of particles in the entire isolated system is N_{TOT}, and the number of particles in the system is N. Therefore,

$$N = N_{Aj} + N_{Bj} + N_{Cj}$$

where N_{Aj}, N_{Bj}, and N_{Cj} are number of particles transferred from the reservoir A,B, and C, respectively, to the system $\mathcal{s}$.

$$N_{TOT} = N + N_A + N_B + N_C$$

where N_A, N_B, and N_C are the number of particles in the reservoir A, B, and C, respectively. When $N = 0$, let us define the number of number of particles N_A^0, N_B^0, and N_C^0 in the reservoir A,B and C, respectively.

$$N_{TOT} = N_A^0 + N_B^0 + N_C^0$$

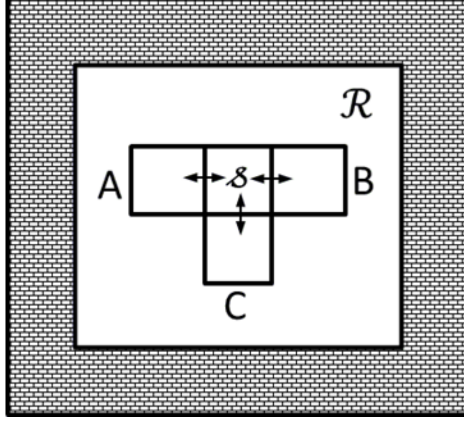

Figure 3.2 Three particles reservoir A, B, and C are connected to a system $\mathcal{S}$. Entire system is isolated by the wall from outside environment.

In order to obtain $P(j)$, we can go to the similar process as mentioned for the case of single reservoir. Starting with S_{res}, we have:

$$S_{res}\left(E_{TOT}-\mathcal{E}_j, N_A^0-N_{Aj}, N_B^0-N_{Bj}, N_C^0-N_{Cj}\right)$$

$$= S_{res}(E_{TOT}, N_A^0, N_B^0, N_C^0) + \left(\frac{\partial S_{res}}{\partial E_{res}}\right)_{\substack{N_A\\N_B\\N_C}} .\left(-\mathcal{E}_j\right) + \left(\frac{\partial S_{res}}{\partial N_{res}}\right)_{\substack{E_{res}\\N_B\\N_C}} .\left(-N_{Aj}\right)$$

$$+\left(\frac{\partial S_{res}}{\partial N_{res}}\right)_{\substack{E_{res}\\N_A\\N_C}} .\left(-N_{Bj}\right) + \left(\frac{\partial S_{res}}{\partial N_{res}}\right)_{\substack{E_{res}\\N_A\\N_B}} .\left(-N_{Cj}\right) \tag{3.12}$$

From equation (2.21) and (2.22), we can get:

$$\Rightarrow S_{res}\left(E_{TOT}-\mathcal{E}_j, N_A^0-N_{Aj}, N_B^0-N_{Bj}, N_C^0-N_{Cj}\right)$$

$$= S_{res}(E_{TOT}, N_A^0, N_B^0, N_C^0) - \frac{\mathcal{E}_j}{T} + \frac{\mu_A}{T}N_{Aj} + \frac{\mu_B}{T}N_{Bj} + \frac{\mu_C}{T}N_{Cj} \tag{3.13}$$

Similar to equation (2.23), we have:

$$P(j) = \frac{1}{Z} exp \frac{-1}{kT}\left(\mathcal{E}_j - \mu_A N_{Aj} - \mu_B N_{Bj} - \mu_C N_{Cj}\right) \tag{3.14}$$

where Z is grand partition function. Similar to equation (2.22), Z can be defined as:

$$Z = \sum_l exp \frac{-1}{kT}\left(\mathcal{E}_j - \mu_A N_{Aj} - \mu_B N_{Bj} - \mu_C N_{Cj}\right) \tag{3.15}$$

We may define the free energy $F(l)$ for the system at state l as:

$$F(l) \equiv \mathcal{E}_j - \mu_A N_{Aj} - \mu_B N_{Bj} - \mu_C N_{Cj} \tag{3.16}$$

Insert equation (2.28) to (2.26), $P(j)$ become:

$$P(j) = \frac{1}{Z} exp \frac{-F(l)}{kT} \tag{3.17}$$

Now we can consider the analogy to an electrical system. The particles can now be concerned as charge carriers, for example, electrons. The particle reservoir now becomes a charge reservoir. The charges can be obtained from the number of particles multiply by the unite electron charge e, therefore,

$$Q_A = N_A . e$$

Replacing all the term N with Q in equation (2.24), the entropy of reservoir S_{res} became:

$$S_{res}\left(E_{TOT} - \mathcal{E}_j, Q_A^0 - Q_{Aj}, Q_B^0 - Q_{Bj}, Q_C^0 - Q_{Cj}\right)$$
$$= S_{res}(E_{TOT}, Q_A^0, Q_B^0, Q_C^0) + \left(\frac{\partial S_{res}}{\partial E_{res}}\right)_{\substack{N_A \\ N_B \\ N_C}} . \left(-\mathcal{E}_j\right) + \left(\frac{\partial S_{res}}{\partial Q_{res}}\right)_{\substack{E_{res} \\ Q_B \\ Q_C}} . \left(-Q_{Aj}\right)$$
$$+ \left(\frac{\partial S_{res}}{\partial Q_{res}}\right)_{\substack{E_{res} \\ Q_A \\ Q_C}} . \left(-Q_{Bj}\right) + \left(\frac{\partial S_{res}}{\partial Q_{res}}\right)_{\substack{E_{res} \\ Q_A \\ Q_B}} . \left(-Q_{Cj}\right) \tag{3.18}$$

Since the electrostatic energy E accumulated by charges Q with potential V has the relation $E = Q.V$, the partial derivative of energy E_{res} at charges Q is:

$$\frac{\partial E_{res}}{\partial Q_A} = V_A \tag{3.19}$$

$$\frac{\partial E_{res}}{\partial Q_B} = V_B \tag{3.20}$$

$$\frac{\partial E_{res}}{\partial Q_C} = V_C \tag{3.21}$$

The term of partial derivative $\frac{\partial S_{res}}{\partial Q_{res}}$ can be transformed to:

$$\frac{\partial S_{res}}{\partial Q_{res}} = -\left(\frac{S_{res}}{E_{res}}\right) . \left(\frac{E_{res}}{Q_{res}}\right) \tag{3.22}$$

Insert the result from equation (2.21) and (2.31) to (2.33) into (2.34), we have:

$$\left(\frac{\partial S_{res}}{\partial Q_{res}}\right)_{\substack{E_{res} \\ Q_B \\ Q_C}} = -\frac{1}{T} . V_A \tag{3.23}$$

$$\left(\frac{\partial S_{res}}{\partial Q_{res}}\right)_{\substack{E_{res}\\Q_A\\Q_C}} = -\frac{1}{T}.V_B \tag{3.24}$$

$$\left(\frac{\partial S_{res}}{\partial Q_{res}}\right)_{\substack{E_{res}\\Q_A\\Q_B}} = -\frac{1}{T}.V_C \tag{3.25}$$

The equation (3.18) with the replacement of result from (3.9), (3.23), (3.24), and (3.25) is then

$$S_{res}\left(E_{TOT} - \mathcal{E}_j, N_A^0 - N_{Aj}, N_B^0 - N_{Bj}, N_C^0 - N_{Cj}\right)$$

$$= S_{res}(E_{TOT}, Q_A^0, Q_B^0, Q_C^0) - \frac{\mathcal{E}_j}{T} + \frac{Q_{Aj}}{T}V_A + \frac{Q_{Bj}}{T}V_B + \frac{Q_{Cj}}{T}V_C \tag{3.26}$$

Similar to equation (2.27), we can have the grand partition function Z as

$$Z = \sum_l exp\frac{-1}{kT}(\mathcal{E}_l - Q_A V_{Al} - Q_B V_{Bl} - Q_C V_{Cl}) \tag{3.15}$$

Thus the free energy of the electric system in state$l$ can be defined as:

$$F(l) \equiv \mathcal{E}_l - Q_{Al}V_{Al} - Q_{Bl}V_{Bl} - Q_C V_{C_j} \tag{3.27}$$

If the system changes from an initial state i to a final state j, the free energy change, $\Delta F(i \to f)$ is

$$\Delta F = F(f) - F(i)$$

$$= \left(\mathcal{E}_f + Q_{Af}V_A + Q_{Bf}V_B + Q_C V_{C_f}\right) - \left(\mathcal{E}_i + Q_{Ai}V_A + Q_{Bi}V_B + Q_C V_{C_i}\right)$$

$$\therefore \Delta F = \Delta\mathcal{E} - \Delta Q_A V_A - \Delta Q_B V_B - \Delta Q_C V_C \tag{3.28}$$

where $\Delta\mathcal{E} = \mathcal{E}(f) - \mathcal{E}(i)$, and

$$\Delta Q_A = \Delta Q_{Af} - \Delta Q_{Ai} \tag{3.29}$$

$$\Delta Q_B = \Delta Q_{Bf} - \Delta Q_{Bi} \tag{3.30}$$

$$\Delta Q_C = \Delta Q_{Bf} - \Delta Q_{Bi} \tag{3.31}$$

Considering a single electron transistor, the schematic equivalent circuit and its charge reservoir are represented in Figure 3.3

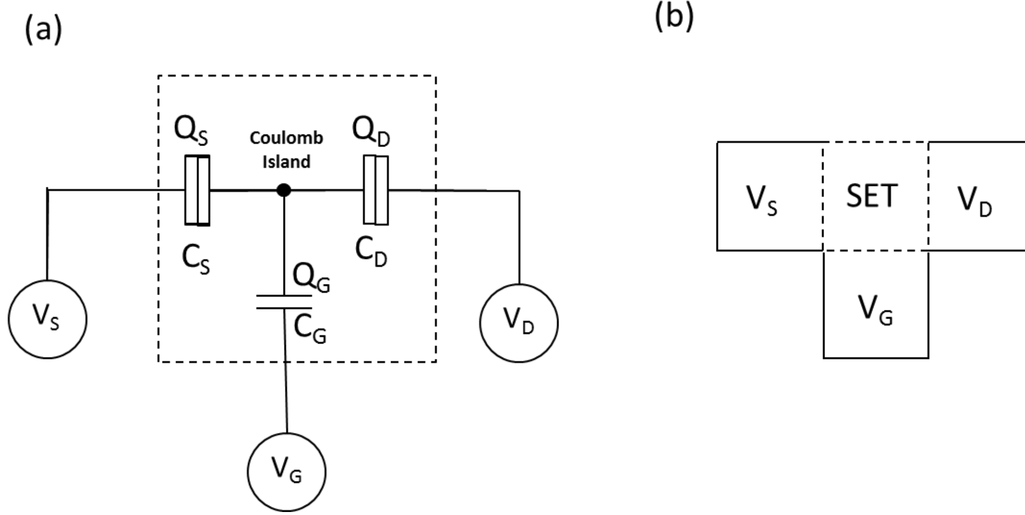

Figure 3.3 (a) Equivalent circuit of single electron transistor and (b) its charge reservoir. In (a), the charges Q_S, Q_D and Q_G are capacitive charges stored on tunnel junctions and gate, which are induced by external bias V_S, V_D, and gate bias V_G, respectively. C_S and C_D are the capacitance of tunnel junctions connected with source, drain, respectively. C_G is the gate capacitance. The dotted square indicat the system SET considered to be connected with three charge reservoirs as V_S, V_D, and V_G, which are represented in (b).

Now, we can discuss the free energy change ΔF in the condition where an electron added or removed from the coulomb island. According to the equation (2.40), the free energy change in a single electron transistor system is expressed as:

$$\Delta F = \Delta \mathcal{E} - \Delta Q_S V_S - \Delta Q_D V_D - \Delta Q_G V_G \tag{3.32}$$

Assuming the system has N electrons as an initial state and $N-1$ or $N+1$ at the final state. The energy change $\Delta \mathcal{E}$ of the system can be obtained from equation (2.16) as

$$\Delta \mathcal{E}^{\pm} = \frac{e}{C_{TOT}}\left[\frac{e}{2} \pm (Ne - Q_0)\right] \tag{3.33}$$

Positive and negative signs for $\Delta \mathcal{E}$ indicate either an electron in the SET system is added or subtracted at the final state. C_{TOT} is the total capacitance of the SET system and $C_{TOT} = C_S + C_D + C_G$.

The change of charge, ΔQ, due to the SET system with number of excess electrons changes from N to $N+1$ or $N-1$, can be expressed by ΔQ_S, ΔQ_D, and ΔQ_G. According to equation (3.29) (3.30) and (3.31),

$$\Delta Q_S^{N\pm1,N} = Q_S^{N\pm1} - Q_S^N \tag{3.34}$$

$$\Delta Q_D^{N\pm1,N} = Q_D^{N\pm1} - Q_D^N \tag{3.35}$$

$$\Delta Q_G^{N\pm1,N} = Q_G^{N\pm1} - Q_G^N \tag{3.36}$$

From equation (2.4), Q_s is obtained from $Q_s = C_S V_{T_S}$, where V_{T_S} is voltage drop across tunnel junction T_s and defined as $V_{T_S} = V_{IS} - V_S$ for a single electron device. However, concerning of the single electron transistors, we define this voltage drop as $V_{T_s}^*$ where $V_{T_s}^* = V_S - V_{IS}$ for the ease of defining voltage drop across gate as V_{T_G} where $V_{T_G} = V_G - V_{IS}$. Thus

$$V_{T_s}^* = V_S - V_{IS} = -V_{T_S} \tag{3.37}$$

From equation (2.4), the charges Q_s stored in tunnel junction T_s can be obtained by:

$$Q_S = C_S \mathrm{V}_{T_S}^* = -C_S V_{T_S} \tag{3.38}$$

Insert the result of V_{T_S} form equation (2.11) into (3.38)

$$\mathrm{Q_S} = -C_S \frac{C_D \mathrm{V}_{DS} - (Ne - Q_0)}{C_{TOT}} \tag{3.39}$$

Insert $\mathrm{Q_S}$ in equation (3.39) into (3.34), we get the change of charge ΔQ_s by adding one extra electron on coulomb island as:

$$\Delta Q_S^{N\pm1,N} = \left[(-C_S)\frac{C_D \mathrm{V}_{DS} - [(N\pm1)e - Q_0]}{C_{TOT}}\right] - \left[(-C_S)\frac{C_D \mathrm{V}_{DS} - (Ne - Q_0)}{C_{TOT}}\right]$$

$$\Rightarrow \Delta Q_S^{N\pm1,N} = -C_S \frac{C_D \mathrm{V}_{DS} - [(N\pm1)e - Q_0]}{C_{TOT}} + C_S \frac{C_D \mathrm{V}_{DS} - (Ne - Q_0)}{C_{TOT}}$$

$$\Rightarrow \Delta Q_S^{N\pm1,N} = \frac{C_S}{C_{TOT}}\{(-C_D \mathrm{V}_{DS}) + [(N\pm1)e - Q_0] + C_D \mathrm{V}_{DS} - (Ne - Q_0)\}$$

$$\Rightarrow \Delta Q_S^{N\pm1,N} == \frac{C_S}{C_{TOT}}(N\pm1)e - Q_0 - Ne + Q_0$$

$$\therefore \Delta Q_S^{N\pm1,N} = \pm\frac{C_S}{C_{TOT}} e \tag{3.40}$$

where the positive and negative sign indicates that the Coulomb island gains or losses one excess electron, Similarly, from equation (3.35) and (3.36), we can get:

$$\Delta Q_D^{N\pm1,N} = \pm\frac{C_D}{C_{TOT}}e \tag{3.41}$$

$$\Delta Q_G^{N\pm1,N} = \pm\frac{C_G}{C_{TOT}}e \tag{3.42}$$

Summarizing the situation that one excess electron is added or removed on the coulomb island, the free energy change can be written as:

$$\Delta F = \Delta\mathcal{E}^{\pm} - \Delta Q_S^{N\pm1,N}V_S - \Delta Q_D^{N\pm1,N}V_D - \Delta Q_G^{N\pm1,N}V_G \tag{3.43}$$

From equation (3.43), we can discuss the free energy change ΔF in the following situation:

1. An electron is tunneled from the source, to the Coulomb island, and the excess number of electrons is $N+1$ for the SET system.
2. An electron is tunneled from the Coulomb island to the source,and the excess number of electrons is $N-1$ for the SET system.
3. An electron tunnels from drain to Coulomb island, thus excess number of electrons is $N+1$ for SET system.
4. An electron tunnels from Coulomb island to drain, thus excess number of electrons is $N-1$ for SET system.

For situation 1, excess number of electrons is $N+1$ on coulomb island, ΔF can be obtained from equation (3.43) as:

$$\Delta F_S^{+} = \Delta\mathcal{E}^{+} - \left(\Delta Q_S^{N+1,N} - e\right)V_S - \Delta Q_D^{N+1,N}V_D - \Delta Q_G^{N+1,N}V_G \tag{3.44}$$

where the foot notes S in ΔF_S^{+} indicates that the electron is tunneled from source and the positive sign indicates the coulomb island gains one excess electron. Since one electron leaves from the tunnel junction which is connected with the source to coulomb island, one electron charge needs to be subtracted from Q_S^{N+1} as the final state for $\Delta Q_S^{N+1,N}$. Insert the result from equation (3.40) to (3.42) and (3.33) into equation (3.44), we have:

$$\Delta F_S^+ = \frac{e}{C_{TOT}}\left[\frac{e}{2} + (Ne - Q_0)\right] - \left(\frac{C_S}{C_{TOT}}e - e\right)V_S - \left(\frac{C_D}{C_{TOT}}e\right)V_D - \left(\frac{C_G}{C_{TOT}}e\right)V_G$$

$$= \frac{e}{C_{TOT}}\left[\frac{e}{2} + (Ne - Q_0)\right] - \frac{e}{C_{TOT}}[C_S V_S - (C_S + C_D + C_G)V_S + C_D V_D + C_G V_G]$$

$$= \frac{e}{C_{TOT}}\left[\frac{e}{2} + (Ne - Q_0)\right] - \frac{e}{C_{TOT}}[C_D(V_D - V_S) + C_G(V_G - V_S)]$$

$$\therefore \Delta F_S^+ = \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} + (Ne - Q_0)\right] - [C_D(V_D - V_S) + C_G(V_G - V_S)]\right\} \tag{3.45}$$

Similarly, for situation 2, excess number of electrons is $N-1$ on the Coulomb island, ΔF can be obtained from equation (3.44) as:

$$\Delta F_S^- = \Delta \mathcal{E}^- - \left(\Delta Q_S^{N-1,N} + e\right)V_S - \Delta Q_D^{N-1,N}V_D - \Delta Q_G^{N-1,N}V_G \tag{3.46}$$

where the foot notes S in ΔF_S^- indicates that the electron tunnels to source and the negative sign indicates the coulomb island losses one excess electron. Since one electron tunnels to the source through the tunnel junction connected with the source, one electron charge needs to be added to Q_S^{N-1} as the final state for $\Delta Q_S^{N-1,N}$. Insert the result from equation (3.40) to (3.42) and (3.33) into equation (3.46), we have:

$$\Delta F_S^- = \frac{e}{C_{TOT}}\left[\frac{e}{2} - (Ne - Q_0)\right] - \left(\frac{-C_S}{C_{TOT}}e + e\right)V_S - \left(\frac{-C_D}{C_{TOT}}e\right)V_D - \left(\frac{-C_G}{C_{TOT}}e\right)V_G$$

$$= \frac{e}{C_{TOT}}\left[\frac{e}{2} - (Ne - Q_0)\right] - \frac{e}{C_{TOT}}[-C_S V_S + (C_S + C_D + C_G)V_S - C_D V_D - C_G V_G]$$

$$= \frac{e}{C_{TOT}}\left[\frac{e}{2} - (Ne - Q_0)\right] - \frac{e}{C_{TOT}}[C_D(V_S - V_D) + C_G(V_S - V_G)]$$

$$= \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} - (Ne - Q_0)\right] - C_D(V_S - V_D) - C_G(V_S - V_G)\right\}$$

$$\therefore \Delta F_S^- = \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} - (Ne - Q_0)\right] + [C_D(V_D - V_S) + C_G(V_G - V_S)]\right\} \tag{3.47}$$

Summarizing with equation (3.45) and (3.47), the free energy change ΔF due to an electron tunnels through tunnel junction from the source side is obtained:

$$\boxed{\Delta F_S^\pm = \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} \pm (Ne - Q_0)\right] \mp [C_D(V_D - V_S) + C_G(V_G - V_S)]\right\}} \tag{3.48}$$

For situation 3, excess number of electrons is $N+1$ on coulomb island, ΔF can be obtained from equation (3.43) as:

$$\Delta F_D^+ = \Delta \mathcal{E}^+ - \Delta Q_S^{N+1,N} V_S - \left(\Delta Q_D^{N+1,N} - e\right) V_D - \Delta Q_G^{N+1,N} V_G \tag{3.49}$$

where the foot notes D in ΔF_D^+ indicates that the electron tunnels from drain and the positive sign indicates the coulomb island gains one excess electron. Since one electron leaves from the tunnel junction which is connected with the drain to coulomb island, one electron charge needs to be subtracted from Q_D^{N+1} as the final state for $\Delta Q_D^{N+1,N}$. Insert the result from equation (3.40) to (3.42) and (3.33) into equation (3.49), we have:

$$\Delta F_D^+ = \frac{e}{C_{TOT}}\left[\frac{e}{2} + (Ne - Q_0)\right] - \frac{C_S}{C_{TOT}} e V_S - \left(\frac{C_D}{C_{TOT}} e - e\right) V_D - \left(\frac{C_G}{C_{TOT}} e\right) V_G$$

$$= \frac{e}{C_{TOT}}\left[\frac{e}{2} + (Ne - Q_0)\right] - \frac{e}{C_{TOT}}\left[C_S V_S + C_D V_D - (C_S + C_D + C_G) V_D + C_G V_G\right]$$

$$= \frac{e}{C_{TOT}}\left[\frac{e}{2} + (Ne - Q_0)\right] - \frac{e}{C_{TOT}}\left[C_S (V_S - V_D) + C_G (V_G - V_D)\right]$$

$$\therefore \Delta F_D^+ = \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} + (Ne - Q_0)\right] - \left[C_S (V_S - V_D) + C_G (V_G - V_D)\right]\right\} \tag{3.50}$$

For situation 4, excess number of electrons is $N-1$ on coulomb island, ΔF can be obtained from equation (3.43) as:

$$\Delta F_D^- = \Delta \mathcal{E}^- - \Delta Q_S^{N+1,N} V_S - \left(\Delta Q_D^{N+1,N} + e\right) V_D - \Delta Q_G^{N+1,N} V_G \tag{3.51}$$

where the foot notes D in ΔF_D^- indicates that the electron is tunneled to drain and the negative sign indicates the coulomb island losses one excess electron. Since one electron tunnels to the drain through the tunnel junction connected with the drain, one electron charge needs to be added to Q_D^{N+1} as the final state for $\Delta Q_D^{N+1,N}$. Insert the result from equation (3.40) to (3.42) and (3.33) into equation (3.51), we have:

$$\Delta F_D^- = \frac{e}{C_{TOT}}\left[\frac{e}{2} - (Ne - Q_0)\right] - \frac{-C_S}{C_{TOT}} e V_S - \left(\frac{-C_D}{C_{TOT}} e + e\right) V_D - \left(\frac{-C_G}{C_{TOT}} e\right) V_G$$

$$= \frac{e}{C_{TOT}}\left[\frac{e}{2} - (Ne - Q_0)\right] - \frac{e}{C_{TOT}}\left[-C_S V_S - C_D V_D + (C_S + C_D + C_G) V_D - C_G V_G\right]$$

$$= \frac{e}{C_{TOT}}\left[\frac{e}{2} - (Ne - Q_0)\right] - \frac{e}{C_{TOT}}\left[C_S (V_D - V_S) + C_G (V_D - V_G)\right]$$

$$\therefore \Delta F_D^- = \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} - (Ne - Q_0)\right] + \left[C_S (V_S - V_D) + C_G (V_G - V_D)\right]\right\} \tag{3.52}$$

Summarizing with equation (3.50) and (3.52), the free energy change ΔF due to an electron tunnels through the tunnel junction from the drain side is:

$$\Delta F_D^{\pm} = \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} \pm (Ne - Q_0)\right] \mp [C_D(V_S - V_D) + C_G(V_G - V_D)]\right\} \tag{3.53}$$

3.2 Stability Diagram of the Single Electron Transistor

After obtaining the free energy change for the single electron transistor with an electron tunneling at four junctions, we can discuss certain conditions that the tunneling event will not occur if the free energy change for that condition is less than 0 ($\Delta F < 0$).

From equation (3.45), the free energy change ΔF_S^+ for the condition that an electron tunnels from source to the Coulomb island is obtained. If we have $V_S = 0$, which is the case when we measure our SET device, ΔF_S^+ can be rewritten as:

$$\Delta F_S^+ = \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} + (Ne - Q_0)\right] - [C_D(V_D - 0) + C_G(V_G - 0)]\right\}$$

$$= \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} + (Ne - Q_0)\right] - (C_D V_D + C_G V_G)\right\}$$

For $\Delta F_S^+ = 0$, we get:

$$0 = \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} + (Ne - Q_0)\right] - (C_D V_D + C_G V_G)\right\}$$

$$C_D V_D = -C_G V_G + \left[\frac{e}{2} + (Ne - Q_0)\right]$$

$$\therefore V_D = \frac{-C_G}{C_D} V_G + \frac{1}{C_D}\left[\frac{e}{2} + (Ne - Q_0)\right] \tag{3.54}$$

Similarly, from equation (3.46), the free energy change ΔF_S^- can be rewritten as:

$$\Delta F_S^- = \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} - (Ne - Q_0)\right] + [C_D(V_D - 0) + C_G(V_G - 0)]\right\}$$

$$= \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} - (Ne - Q_0)\right] + (C_D V_D + C_G V_G)\right\}$$

For $\Delta F_S^- = 0$, we get:

$$0 = \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} - (Ne - Q_0)\right] + (C_D V_D + C_G V_G)\right\}$$

$$C_D V_D = -C_G V_G - \left[\frac{e}{2} - (Ne - Q_0)\right]$$

$$\therefore V_D = \frac{-C_G}{C_D} V_G - \frac{1}{C_D}\left[\frac{e}{2} - (Ne - Q_0)\right] \tag{3.55}$$

Equation (3.54) and (3.55) can be plotted as a function of $V_D = f(V_G)$, showing Figure 3.4.

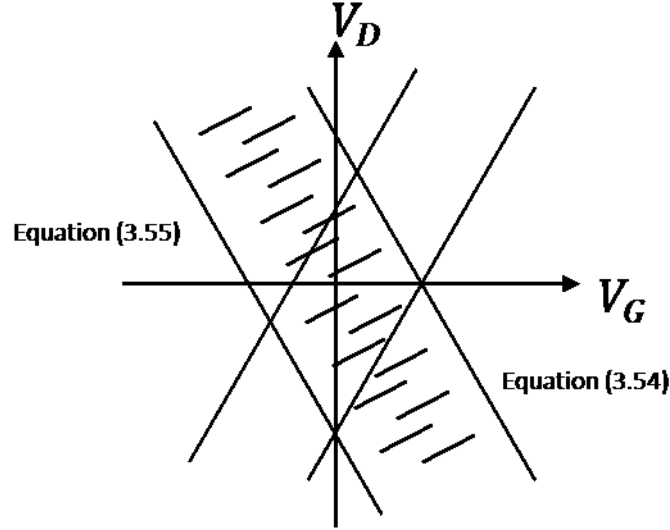

Figure 3.4 V_D vs V_G for the free energy change $\Delta F_S^{\pm} = 0$. Equation (3.54) and (3.55) is obtained as $\Delta F_S^{+} = 0$ and $\Delta F_S^{-} = 0$, respectively. Shaded area between equation (3.54) and (3.55) are the zone for $\Delta F_S^{\pm} > 0$, thus the tunneling is prohibited within this area.

At absolute zero temperature, if the change of free energy is larger than zero, $\Delta F_S^{+} > 0$, the tunneling of an electron from source to coulomb island is prohibited. The V_D in equation (3.54) then is expressed as:

$$V_D < \frac{-C_G}{C_D} V_G + \frac{1}{C_D}\left[\frac{e}{2} + (Ne - Q_0)\right] \tag{3.56}$$

This inequality can be represented by the area on the left side of the line of equation (3.55) in Figure 3.4.

Similarly, at absolute zero temperature, when $\Delta F_S^- > 0$, the tunneling of an electron from coulomb island to source is prohibited, the V_D in equation (3.55) is expressed as:

$$V_D > \frac{-C_G}{C_D} V_G - \frac{1}{C_D}\left[\frac{e}{2} - (Ne - Q_0)\right] \tag{3.57}$$

This inequality $V_D$is represented by the area on the right side of the line of equation (3.55). Thus the area in between these two inequalities has a free energy change larger than zero, $\Delta F_S^{\pm} > 0$, inducing coulomb blockage prohibiting any tunneling events from occurring between the source and Coulomb island.

Now, let us consider the tunneling between drain and Coulomb island. The free energy change of an electron tunneling in between drain and coulomb island is expressed as $\Delta F_D^{\pm}$. From equation (3.50), the free energy change ΔF_D^+ for an electron to tunnel from drain to Coulomb island can be rewritten when $V_S = 0$.

$$\Delta F_D^+ = \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} + (Ne - Q_0)\right] - [C_S(0 - V_D) + C_G(V_G - V_D)]\right\} \tag{3.50}$$

$$= \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} + (Ne - Q_0)\right] - [-C_S V_D + C_G V_G - C_G V_D]\right\}$$

$$\therefore \Delta F_D^+ = \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} + (Ne - Q_0)\right] - [-(C_S + C_G)V_D + C_G V_G]\right\}$$

For $\Delta F_D^+ = 0,\ V_D$ can be obtained by:

$$0 = \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} + (Ne - Q_0)\right] - [-(C_S + C_G)V_D + C_G V_G]\right\}$$

$$(C_S + C_G)V_D = C_G V_G - \left[\frac{e}{2} + (Ne - Q_0)\right]$$

$$\therefore V_D = \frac{C_G}{C_S + C_G} V_G - \frac{1}{C_S + C_G}\left[\frac{e}{2} + (Ne - Q_0)\right] \tag{3.58}$$

Similarly, from equation (3.52), the free energy change ΔF_D^- for an electron to tunnel from Coulomb island to drain can be rewritten when $V_S = 0$

$$\therefore \Delta F_D^- = \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} - (Ne - Q_0)\right] + [C_S(0 - V_D) + C_G(V_G - V_D)]\right\} \tag{3.52}$$

$$= \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} - (Ne - Q_0)\right] + (-C_S V_D + C_G V_G - C_G V_D)\right\}$$

$$= \frac{e}{C_{TOT}}\left[\frac{e}{2} - (Ne - Q_0)\right] + [-(C_S + C_G)V_D + C_G V_G]$$

For $\Delta F_D^- = 0$, we get:

$$0 = \frac{e}{C_{TOT}}\left[\frac{e}{2} - (Ne - Q_0)\right] + [-(C_S + C_G)V_D + C_G V_G]$$

$$(C_S + C_G)V_D = \left[\frac{e}{2} - (Ne - Q_0)\right] + C_G V_G$$

$$\therefore V_D = \frac{C_G}{C_S + C_G} V_G + \frac{1}{C_S + C_G}\left[\frac{e}{2} - (Ne - Q_0)\right] \quad (3.59)$$

Equation (3.58) and (3.59) are plotted as a function of $V_D = f(V_G)$ in Figure 3.5.

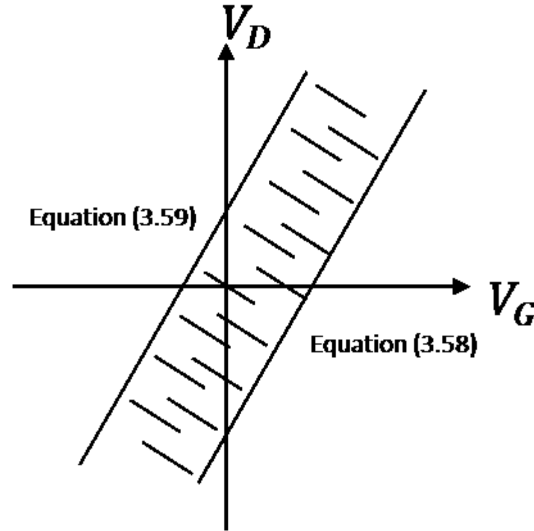

Figure 3.5 V_D vs V_G for the free energy change $\Delta F_D^{\pm} = 0$. Equation (3.58) and (3.59) is obtained as $\Delta F_D^+ = 0$ and $\Delta F_D^- = 0$, respectively. The shaded area between equation (3.58) and (3.59) is the zone where $\Delta F_D^{\pm} > 0$, thus tunneling is prohibited within this area.

At absolute zero temperature, if the change of free energy is larger than zero, $\Delta F_D^+ > 0$, the tunneling of an electron from drain to coulomb island is prohibited. The V_D in equation (3.58) then is expressed as:

$$V_D > \frac{C_G}{C_S + C_G} V_G - \frac{1}{C_S + C_G} \left[\frac{e}{2} + (Ne - Q_0) \right] \quad (3.60\ )$$

This inequality can be represented by the area on the left side of the line of equation (3.58) in Figure 3.5.

Similarly, at absolute zero temperature, when $\Delta F_D^- > 0$, the tunneling of an electron from coulomb island to drain is prohibited, the V_D in equation (3.58) is expressed as:

$$V_D < \frac{C_G}{C_S + C_G} V_G + \frac{1}{C_S + C_G} \left[\frac{e}{2} - (Ne - Q_0) \right] \quad (3.61)$$

This inequality $V_D$is represented by the area on the right side of the line of equation (3.59).

Thus the area in between these two inequalities has free energy change larger than zero, $\Delta F_D^{\pm} > 0$, which constructs the regime of coulomb blockage prohibiting any tunneling event occurred between drain and coulomb island.

Summarized from the four conditions discussed above, the stability diagram of a single electron transistor can be constructed. In Figure 3.6, the centered shaded area is constructed by combing equation (3.54), (3.55), (3.58), and (3.59). In this area, the tunneling of an electron is prohibited in all four conditions through either junctions, for the coulomb island with no excess electrons (N=0) as an initial state before tunneling. This is the coulomb blockade regime for single electron transistor. The shaded trapezoids adjacent with the number for N=1 and N=-1 represent the tunneling is prohibited for the coulomb island with different state of N but have same coulomb blockage regime. It can be seen that with a constant V_D, increase the gate bias V_G can turn on and off the electron tunneling causing the transition of a state from N to N+1. This is the coulomb oscillation for the single electron transistor.

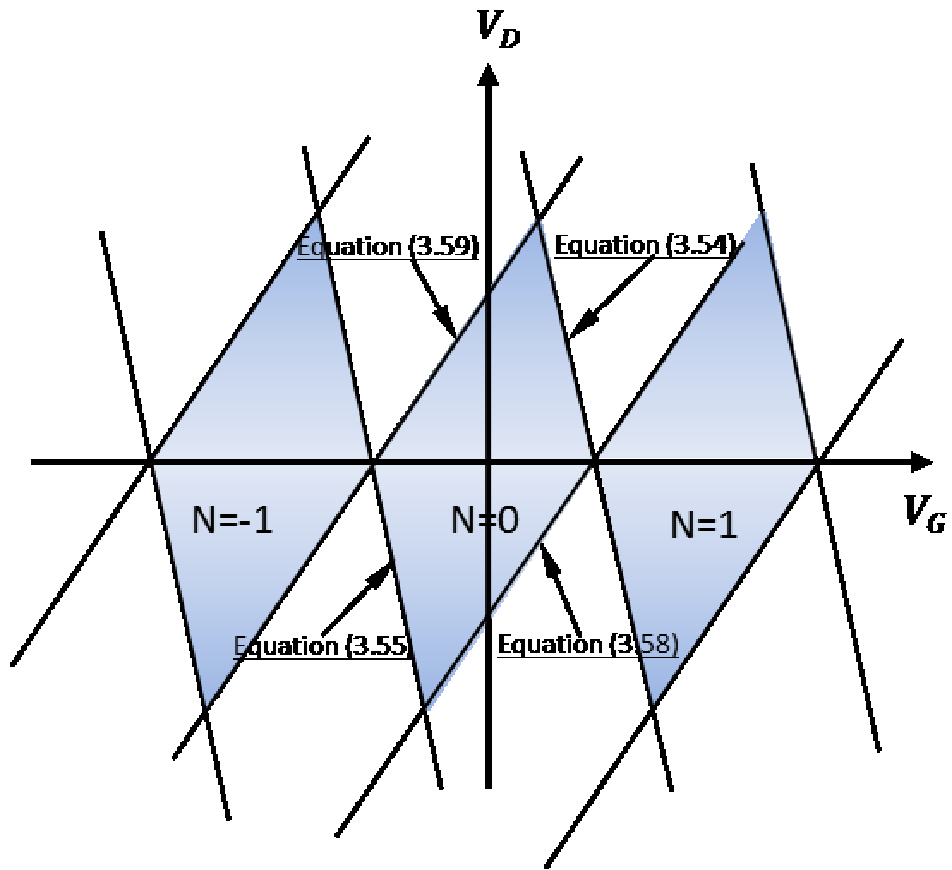

Figure 3.6 Stability diagram of single electron transistor. Shaded trapezoids represent the coulomb blockage regime. N is the excess number of electrons on the coulomb island before tunneling.

3.3 Energy Diagram

The energy diagram of a single electron transistor can be constructed from the free energy change discussed in the previous section. Consider the situation that an electron tunnels from source to coulomb island, as shown in Figure 3.7, the free energy change ΔF_S^+ is obtained from equation (3.44):

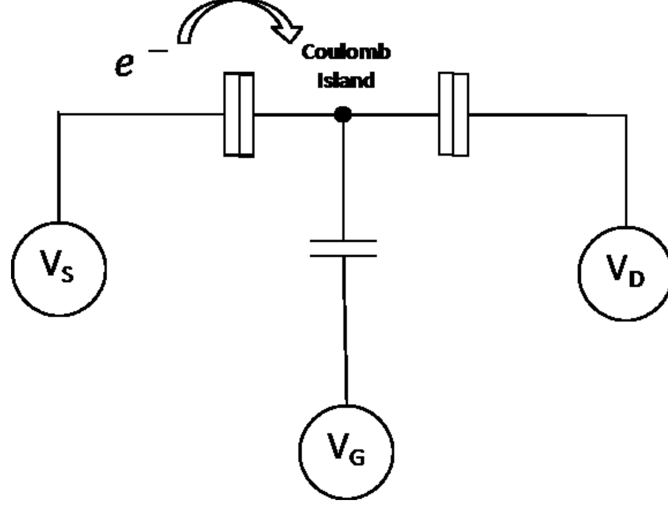

Figure 3.7 Equivalent circuit for single electron transistor.

$$
\begin{aligned}
\Delta F_S^+ &= \Delta \mathcal{E}_S^{\pm\left(\Delta Q_S^{N+1,N}-e\right)V} - \Delta Q_D^{N+1,N} V_D - \Delta Q_G^{N+1,N} V_G \qquad (3.44)\\
&= \frac{e}{C_{TOT}}\left[\frac{e}{2} + (Ne - Q_0)\right] - \left(\frac{C_S}{C_{TOT}}e - e\right)V_S - \left(\frac{C_D}{C_{TOT}}e\right)V_D - \left(\frac{C_G}{C_{TOT}}e\right)V_G\\
&= \frac{e^2}{2C_{TOT}} + \frac{e}{C_{TOT}}(Ne - Q_0) - \frac{e}{C_{TOT}}C_S V_S + eV_S - \frac{e}{C_{TOT}}C_D V_D - \frac{e}{C_{TOT}}C_G V_G\\
&= \frac{e^2}{2C_{TOT}} + eV_S + \frac{e}{C_{TOT}}\left[(Ne - Q_0) - C_S V_S - C_D V_D - C_G V_G\right]\\
&= eV_S + \frac{e^2}{2C_{TOT}} - \frac{e}{C_{TOT}}\left[C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0)\right]\\
&= eV_S + \frac{e^2}{2C_{TOT}} - e\left[\frac{C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0)}{C_{TOT}}\right] \qquad (3.62)
\end{aligned}
$$

The last term $\frac{C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0)}{C_{TOT}}$ in the equation presents the electrostatic potential of the Coulomb island, $\varphi_{IS}(N)$. Thus we have:

$$\Delta F_S^+ = eV_S + \frac{e^2}{2C_{TOT}} - e\varphi_{IS}(N) \qquad (3.63)$$

If we consider the free energy change is the sum of energy for taking one electron from source and adding it to the Coulomb island, the ΔF_S^+ can be expressed as

$$\Delta F_S^+ = (-g_s) + g_{IS} \qquad (3.64)$$

where g_s is the energy to add one electron to source and g_{IS} is the energy to add one electron to coulomb island.

Before an electron tunnels from source to coulomb island under an external bias V_s and V_D connected to source and drain, respectively, the highest occupied energy level of the source and drain can be represented as $-eV_s$ and $-eV_D$, respectively. The highest energy level occupied by N electrons in the coulomb island can be described by the electrostatic potential $\varphi_{IS}(N)$. Combining these components, an energy diagram can be constructed. It is schematically represented in Figure 3.8.

The first available energy level in coulomb island for an electron from source to tunnel to can be obtained by adding the free energy change ΔF_S^+ to the source energy level $-eV_s$, thus we have:

$$-eV_S + \Delta F_S^+ = -eV_S + eV_S + \frac{e^2}{2C_{TOT}} - e\varphi_{IS}(N)$$

$$\therefore -eV_S + \Delta F_S^+ = \frac{e^2}{2C_{TOT}} - e\varphi_{IS}(N)$$

From equation (3.65), the energy for adding an electron to the source is g_s, thus the energy to remove an electron from source is $-g_s$. This energy can be obtained since the source is having the highest energy level $-eV_S$. To remove an electron from this energy level, the energy required is eV_S. We can write this term as:

$$-g_s = eV_S$$

From equation (3.65), we can rewrite the g_{IS} as $g_{IS} = \Delta F_S^+ - (-g_s)$. Insert $-g_s = eV_S$ and ΔF_S^+ from equation (3.64), we can have

$$g_{IS} = eV_S + \frac{e^2}{2C_{TOT}} - e\varphi_{IS}(N) - eV_S$$

$$\therefore g_{IS} = \frac{e^2}{2C_{TOT}} - e\varphi_{IS}(N) \qquad (3.65)$$

This is the free energy required to add one electron to Coulomb island. We can found that it is the same as the first available energy level on the Coulomb island as we calculated before. The first empty energy level represented by g_{IS} is shown in Figure 3.8.

Since $-g_s = eV_S$, $g_s = -eV_S$ can represent the highest energy level occupied in source. From equation (3.64), $\Delta F_S^+ = g_{IS} - g_s$. Then the energy diagram can be simplified as in Figure 3.9.

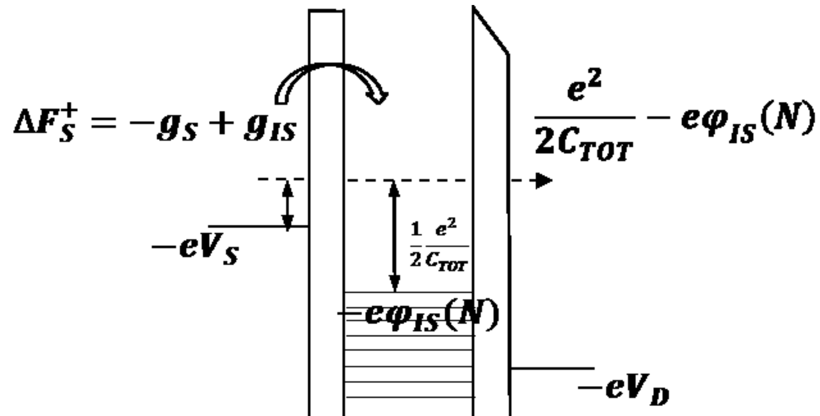

Figure 3.8 Schematic energy diagram for an electron tunneling from source. V_S and V_D is the bias applied to source and drain respectively. The electrostatic potential of the coulomb island is represented by $\varphi_{IS}(N)$ with N excess electrons on it. ΔF_S^+ represents the free energy change for an electron tunnel from source to coulomb island and is composed by the sum of free energy of taking one electron out from source, $-g_S$, and the free energy to add one electron to coulomb island, g_{IS}.

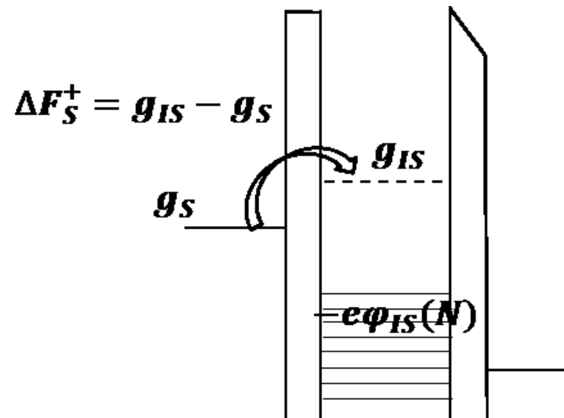

Figure 3.9 Simplified energy diagram. Simply use g_S and g_{IS} representing the energy level of the source and coulomb island.

3.4 Charging Energy

The charging energy $\mathrm{E_C}$ of coulomb island in the single electron transistor can be defined as the difference of the electrochemical potential in the coulomb island with states of $\mathrm{N+1}$ and N. From energy diagram in Figure 3.9, $\mathrm{E_C}$ is defined as:

$$\mathrm{E_C} \equiv g_{IS}(N+1) - g_{IS}(N) \tag{3.66}$$

where $g_{IS}(N+1)$ and $g_{IS}(N)$ is the energy level of the state with $N+1$ and N electrons in the coulomb island. From equation (3.65), the $g_{IS}(N)$ can be expressed as:

$$g_{IS} = \frac{e^2}{2C_{TOT}} - e\varphi_{IS}(N) \tag{3.65}$$

where $e\varphi_{IS}(N)$ is the electrochemical potential for the coulomb island.

From equation (3.62) and (3.63), the electrostatic potential $\varphi_{IS}(N)$ is:

$$\varphi_{IS}(N) = \frac{C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0)}{C_{TOT}} \tag{3.67}$$

Thus $g_{IS}(N+1) - g_{IS}(N)$ is

$$g_{IS}(N+1) - g_{IS}(N) = \left[\frac{e^2}{2C_{TOT}} - e\varphi_{IS}(N+1)\right] - \left[\frac{e^2}{2C_{TOT}} - e\varphi_{IS}(N)\right]$$

$$= e\varphi_{IS}(N) - e\varphi_{IS}(N+1)$$

$$= e\frac{C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0)}{C_{TOT}} - e\frac{C_S V_S + C_D V_D + C_G V_G - [(N+1)e - Q_0]}{C_{TOT}}$$

$$= e\frac{[(N+1)e - Q_0] - (Ne - Q_0)}{C_{TOT}}$$

$$= \frac{e^2}{C_{TOT}}$$

$$\therefore \mathrm{E_C} = \frac{e^2}{C_{TOT}} \tag{3.68}$$

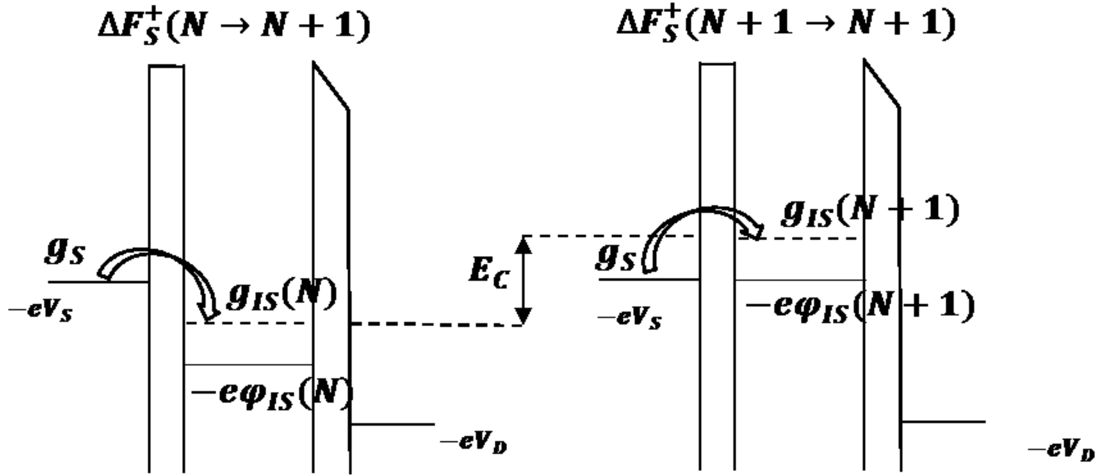

Figure 3.10 Schematic Energy diagram for state transition of N to N+1, and N+1 to N+2. Charging Energy is defined as the difference of the electrochemical potential of the Coulomb island before and after addition of one electron.

Now considering the condition when an electron tunnelsfrom drain to Coulomb island. The free energy change ΔF_D^+ is obtained from equation (3.49):

$$\Delta F_D^+ = \Delta\mathcal{E}^+ - \Delta Q_S^{N+1,N} V_S - \left(\Delta Q_D^{N+1,N} - e\right)V_D - \Delta Q_G^{N+1,N} V_G \tag{2.60}$$

$$= \frac{e}{C_{TOT}}\left[\frac{e}{2} + (Ne - Q_0)\right] - \frac{C_S}{C_{TOT}} eV_S - \left(\frac{C_D}{C_{TOT}} e - e\right) V_D - \left(\frac{C_G}{C_{TOT}} e\right) V_G$$

$$= \frac{e^2}{2C_{TOT}} + \frac{e}{C_{TOT}}(Ne - Q_0) - \frac{e}{C_{TOT}}(C_S V_S + C_S V_D + C_G V_G) - (-eV_D)$$

$$= \frac{e^2}{2C_{TOT}} - \frac{e}{C_{TOT}}[C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0)] - (-eV_D)$$

$$= \frac{e^2}{2C_{TOT}} - e\frac{C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0)}{C_{TOT}} - (-eV_D)$$

$$= \frac{e^2}{2C_{TOT}} - e\varphi_{IS}(N) - (-eV_D)$$

$$\therefore \Delta F_D^+ = g_{IS}(N) - g_D \tag{3.69}$$

where g_D is the electrochemical potential of the drain when biased with V_D.

The free energy diagram constructed for the condition that an electron is tunneled from drain to Coulomb island is schematically illustrated in Figure 3.11.

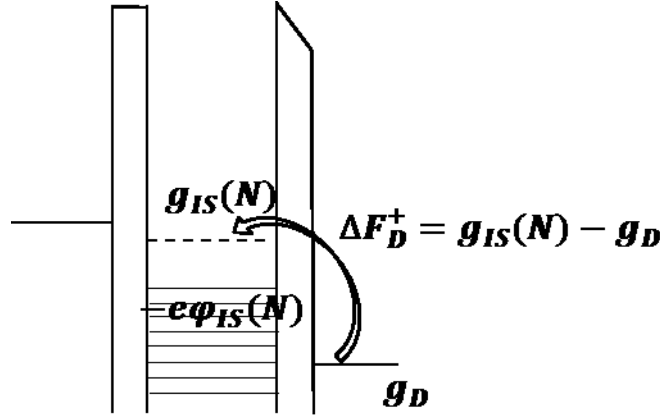

Figure 3.11 Free energy diagram for an electron tunneled from drain to source.

Similary, the charging energy E_C can be obtained from equation (3.66)

$$\mathrm{E_C} \equiv g_{IS}(N+1) - g_{IS}(N) \qquad (3.66)$$

$$g_{IS}(N+1) - g_{IS}(N) = \left[\frac{e^2}{2C_{TOT}} - e\varphi_{IS}(N+1)\right] - \left[\frac{e^2}{2C_{TOT}} - e\varphi_{IS}(N)\right]$$

$$= e\varphi_{IS}(N) - \ e\varphi_{IS}(N+1)$$

$$\therefore E_C = \frac{e^2}{C_{TOT}} \qquad (3.70)$$

The charging energy obtained from equation (3.70) for the condition that an electron tunnels from the drain to coulomb island is identical to that obtained from equation (3.68). This means that the charging energy is independent of the location where the electron tunnels from.

The charging energy is also demonstrated in free energy diagram for the Coulomb island with a state of $g_{IS}(N)$ and $g_{IS}(N+1)$ in Figure 3.12.

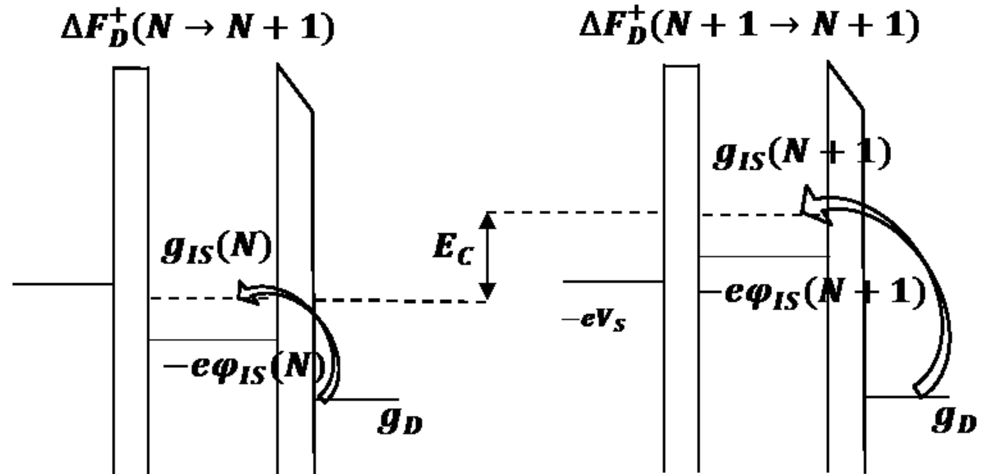

Figure 3.12 Charging energy for the Coulomb island with a state of $g_{IS}(N)$ and $g_{IS}(N+1)$.

In summary, the charging energy is defined as the difference of electrochemical potential in coulomb island resulting from the addition of an electron on it. It is independent of where the electron is added from. Since $E_C = \frac{e^2}{C_{TOT}}$, it is also independent of the number of excess electrons N in the coulomb island.

3.5 Single Electron Behavior

3.5 1 Coulomb Blockade

The coulomb blockade is the most import phenomena in single electron devices. Coulomb blockade is observed as an IV characteristic presented by a flat region with a constant source drain current with increasing bias for the single electron device.

The Coulomb blockage can be understood qualitatively by the energy diagrams indicating the change of free energy and electrochemical potential while an electron is tunneled through the tunnel junctions. Figure 3.13 illustrates the process of an electron tunnels from the source to drain. As discussed before, the free energy change ΔF of the SED system determines the occurring of Coulomb blockade. It will be an indicator in etch of the transition state in the energy diagrams.

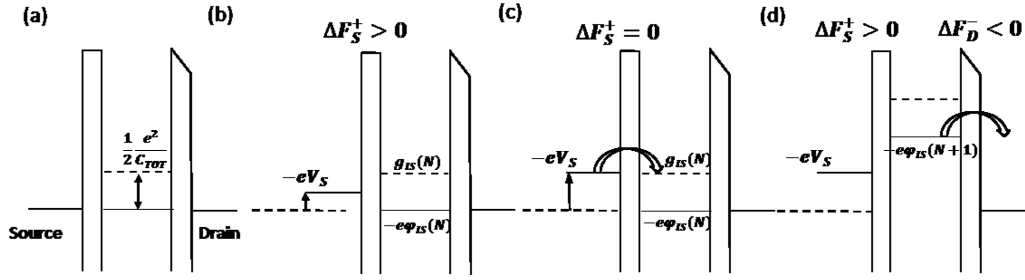

Figure 3.13 Schematic energy diagram for the process of electron transportation in single electron device. (a) No bias applied. (b) Small source bias V_S applied. Since $\Delta F_S^+ > 0$, Coulomb blockade occurs and electron is prohibited to tunnel from source to the coulomb island. (c). Sufficient source bias V_S is applied such that $\Delta F_S^+ = 0$. One electron can be tunneled to coulomb island. (d) Addition of one electron in the coulomb island causes the raise of electrochemical potential and $\Delta F_D^+ < 0$. Thus one electron can be tunneled to drain.

Consider a single electron device with double barrier tunnel junction as showing in Figure 3.13. Before any external bias is applied, the Fermi level of the source and drain are aligned as shown in Figure 3.13 (a). An unoccupied energy state in the Coulomb island is indicated by the daished line. The electrochemical potential difference between this state and the occupied state is obtained by the free energy change discussed in previous sections. In previous section we define the unoccupied state is $g_{IS}(N)$ and occupied state is $e\varphi_{IS}(N)$ thus from Equation (3.65) the energy difference obtained as $\frac{e^2}{2C_{TOT}}$. If a small source bias V_{DS} is applied, the source Fermi level raises. Before the source Fermi level aligned with the energy state $g_{IS}(N)$, free energy change $\Delta F_S^+ < 0$, electron cannot tunnel from source to coulomb island and device is under the regime of coulomb blockade. An interpretation of the coulomb blockade can be considered that source bias is not providing enough energy to put one electron to the available energy state $g_{IS}(N)$ on the Coulomb island, or simply saying, V_S is not sufficient to charge the coulomb island by one electron. As V_S is increased to a certain value that the Fermi level

of source is aligned with the unoccupied energy state $g_{IS}(N)$ therefore $\Delta F_S^+ = 0$, tunneling is allowed for one electron from source to coulomb island. This is shown in Figure 3.13 (b). After one electron is added to the Coulomb island, the electrochemical potential rises up due to the occupancy of this extra electron in coulomb island. This causes the free energy change of an electron tunneling from island to drain become larger than zero, $\Delta F_D^+ > 0$, resulting the simultaneous tunneling of an electron to drain as shown in Figure 3.13 (d). One electron tunneling out of the coulomb island drops down the electrochemical potential and turns the system back to the state of Figure 3.13 (c). Thus the tunneling current obtained from single electron device is composed by repeating the state of coulomb island with excess number of electron from N to $N+1$ to N.

Now we can further obtained the width of the coulomb blockade ΔV_{DS} based on the free energy change ΔF in four conditions of coulomb blockade discussed in previous section.

The four conditions of coulomb blockade resulting from $\Delta F > 0$ are described by the drain bias V_D from Inequality (3.56), (3.57), (3.60), and (3.61).

$$V_D < \frac{-C_G}{C_D} V_G + \frac{1}{C_D}\left[\frac{e}{2} + (Ne - Q_0)\right] \tag{3.56}$$

$$V_D > \frac{-C_G}{C_D} V_G - \frac{1}{C_D}\left[\frac{e}{2} - (Ne - Q_0)\right] \tag{3.57}$$

$$V_D > \frac{C_G}{C_S + C_G} V_G - \frac{1}{C_S + C_G}\left[\frac{e}{2} + (Ne - Q_0)\right] \tag{3.60}$$

$$V_D < \frac{C_G}{C_S + C_G} V_G + \frac{1}{C_S + C_G}\left[\frac{e}{2} - (Ne - Q_0)\right] \tag{3.61}$$

By combinding the inequalities above, the range of drain bias for coulomb blockade can be defined in four different conditions. For the simplicity, we can first focus on the case of the single electron device with no gate. The gate bias $V_G = 0$ and gate capacitance $C_G = 0$ are applied to the inequalities above. Furthermore, consider the condition when excess number of electron N is zero, $N = 0$. This is true when initially source drain bias is increased from 0 to a higher value during the measurement.

According to the conditions above, inequalities (3.56), (3.57), (3.60), and (3.61) are reduced as:

$$V_D < \frac{\frac{e}{2} - Q_0}{C_D} \tag{3.71}$$

$$V_D > \frac{-\frac{e}{2} - Q_0}{C_D} \tag{3.72}$$

$$V_D > \frac{-\frac{e}{2} + Q_0}{C_S} \tag{3.73 }$$

$$V_D < \frac{\frac{e}{2} + Q_0}{C_S} \tag{3.74}$$

Comparing the inequality (3.71) an (3.74), the upper limit of the V_D is obtained as $V_D < \frac{\frac{e}{2}-Q_0}{C_D}$ or $V_D < \frac{\frac{e}{2}+Q_0}{C_S}$. Similarly, from inequality (3.72) an (3.73), the lower limit of V_D is obtained as $V_D > \frac{-\frac{e}{2}-Q_0}{C_D}$ or $V_D > \frac{-\frac{e}{2}+Q_0}{C_S}$. By these two upper limits and two lower limits, we can have four ranges of V_D based on the conditions described below:

A. If the two lower limits are compared as:

$$\frac{-\frac{e}{2} - Q_0}{C_D} < \frac{-\frac{e}{2} + Q_0}{C_S} \tag{3.75}$$

And if the two lower upper limits are compared as:

$$\frac{\frac{e}{2} - Q_0}{C_D} < \frac{\frac{e}{2} + Q_0}{C_S} \tag{3.76}$$

then V_D is limited in the range as

$$\frac{-\frac{e}{2} + Q_0}{C_S} < V_D < \frac{\frac{e}{2} - Q_0}{C_D} \tag{3.77}$$

Thus the width of the coulomb blockade ΔV_D can be obtained from equation (3.78) as:

$$\Delta V_D = \frac{\frac{e}{2} - Q_0}{C_D} - \frac{-\frac{e}{2} + Q_0}{C_S}$$

$$= \frac{C_S\left(\frac{e}{2} - Q_0\right) - C_D\left(-\frac{e}{2} + Q_0\right)}{C_D C_S}$$

$$= \frac{C_S\left(\frac{e}{2} - Q_0\right) + C_D\left(\frac{e}{2} - Q_0\right)}{C_D C_S}$$

$$= \frac{C_S + C_D}{C_D C_S}\left(\frac{e}{2} - Q_0\right)$$

$$\therefore \Delta V_D = \frac{C_\Sigma}{C_D C_S}\left(\frac{e}{2} - Q_0\right) \tag{3.78}$$

The inequalities (3.75) and (3.76) that we used to set the range of ΔV_D can be written as:

$$\frac{-\frac{e}{2} - Q_0}{C_D} < \frac{-\frac{e}{2} + Q_0}{C_S} \tag{3.75}$$

$$\frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0} > \frac{C_D}{C_S} \qquad (3.75)(a)$$

It need to be noted that $|Q_0| < \frac{1}{2}$, so $-\frac{e}{2} + Q_0 > 0$ and $-\frac{e}{2} - Q_0 < 0$.

Therefore,

$$\frac{\frac{e}{2} - Q_0}{C_D} < \frac{\frac{e}{2} + Q_0}{C_S} \tag{3.76}$$

$$\frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} < \frac{C_D}{C_S} \qquad (3.76)(a)$$

$$\therefore \quad \frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} < \frac{C_D}{C_S} < \frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0} \tag{3.79}$$

If the two lower limits are compared as:

$$\frac{-\frac{e}{2} - Q_0}{C_D} < \frac{-\frac{e}{2} + Q_0}{C_S} \tag{3.80}$$

And if the two lower upper limits are compared as:

$$\frac{\frac{e}{2} - Q_0}{C_D} > \frac{\frac{e}{2} + Q_0}{C_S} \tag{3.81}$$

then V_D is limited in the range as

$$\frac{-\frac{e}{2}+Q_0}{C_S} < V_D < \frac{\frac{e}{2}+Q_0}{C_D} \qquad (3.82)$$

Thus the width of the coulomb blockade ΔV_D can be obtained from equation (2.93) as:

$$\Delta V_D = \frac{\frac{e}{2}+Q_0}{C_S} - \frac{-\frac{e}{2}+Q_0}{C_S}$$

$$= \frac{\frac{e}{2}+Q_0+\frac{e}{2}-Q_0}{C_S}$$

$$\therefore \Delta V_D = \frac{e}{C_S} \qquad (3.83)$$

The inequalities (3.80) and (3.81) that we used to set the range of ΔV_D can be written as:

$$\frac{-\frac{e}{2}-Q_0}{C_D} < \frac{-\frac{e}{2}+Q_0}{C_S} \qquad (3.80)$$

$$\frac{-\frac{e}{2}-Q_0}{-\frac{e}{2}+Q_0} > \frac{C_D}{C_S} \qquad (3.80)(a)$$

And

$$\frac{\frac{e}{2}-Q_0}{C_D} > \frac{\frac{e}{2}+Q_0}{C_S} \qquad (3.81)$$

$$\frac{\frac{e}{2}-Q_0}{\frac{e}{2}+Q_0} > \frac{C_D}{C_S} \qquad (3.81)(a)$$

Since $|Q_0| < \frac{1}{2}$, thus $\frac{-e}{2} < Q_0 < 0$ or $0 < Q_0 < \frac{e}{2}$. Compare (3.80)(a) and (3.81)(a), one can obtain

$$\frac{\frac{e}{2}-Q_0}{\frac{e}{2}+Q_0} < \frac{-\frac{e}{2}-Q_0}{-\frac{e}{2}+Q_0} \qquad \text{when } 0 < Q_0 < \frac{e}{2}$$

And

$$\frac{\frac{e}{2}-Q_0}{\frac{e}{2}+Q_0} > \frac{-\frac{e}{2}-Q_0}{-\frac{e}{2}+Q_0} \qquad \text{when } \frac{-e}{2} < Q_0 < 0$$

$$\therefore \frac{C_D}{C_S} < \frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} \qquad when\ 0 < Q_0 < \frac{e}{2} \tag{3.84(a)}$$

$$or\ \frac{C_D}{C_S} < \frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0} \qquad when\ \frac{-e}{2} < Q_0 < 0 \tag{3.84(b)}$$

B. If the two lower limits are compared as:

$$\frac{-\frac{e}{2} + Q_0}{C_S} < \frac{-\frac{e}{2} - Q_0}{C_D} \tag{3.85}$$

And if the two upper limits are compared as:

$$\frac{\frac{e}{2} - Q_0}{C_D} < \frac{\frac{e}{2} + Q_0}{C_S} \tag{3.86}$$

then V_D is limited in the range as

$$\frac{-\frac{e}{2} - Q_0}{C_D} < V_D < \frac{\frac{e}{2} - Q_0}{C_D} \tag{3.87}$$

Thus the width of the coulomb blockade ΔV_D can be obtained from equation (2.98) as:

$$\Delta V_D = \frac{\frac{e}{2} - Q_0}{C_D} - \frac{-\frac{e}{2} - Q_0}{C_D}$$

$$= \frac{\frac{e}{2} - Q_0 + \frac{e}{2} + Q_0}{C_D}$$

$$\therefore \Delta V_D = \frac{e}{C_D} \tag{3.88}$$

The inequalities (2.96) and (2.97) that we used to set the range of ΔV_D can be written as:

$$\frac{-\frac{e}{2} + Q_0}{C_S} < \frac{-\frac{e}{2} - Q_0}{C_D} \tag{3.85}$$

$$\frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0} < \frac{C_D}{C_S} \tag{3.85(a)}$$

And

$$\frac{\frac{e}{2} - Q_0}{C_D} < \frac{\frac{e}{2} + Q_0}{C_S} \tag{3.86}$$

$$\frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} < \frac{C_D}{C_S} \qquad (3.86)(a)$$

Similar to case B, by comparing (3.85)(a) and (3.86)(a), one can obtain

$$\frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} < \frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0} \qquad when\ 0 < Q_0 < \frac{e}{2}$$

And

$$\frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0} < \frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} \qquad when\ \frac{-e}{2} < Q_0 < 0$$

$$\therefore\ \frac{C_D}{C_S} > \frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0} \qquad \text{when } 0 < Q_0 < \frac{e}{2} \qquad (3.89)(a)$$

$$or\ \frac{C_D}{C_S} > \frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} \qquad \text{when } \frac{-e}{2} < Q_0 < 0 \qquad (3.89)(b)$$

C. If the two lower limits are compared as:

$$\frac{-\frac{e}{2} + Q_0}{C_S} < \frac{-\frac{e}{2} - Q_0}{C_D} \qquad (3.90)$$

And if the two upper limits are compared as:

$$\frac{\frac{e}{2} + Q_0}{C_S} < \frac{\frac{e}{2} - Q_0}{C_D} \qquad (3.91)$$

then V_D is limited in the range as

$$\frac{-\frac{e}{2} - Q_0}{C_D} < V_D < \frac{\frac{e}{2} + Q_0}{C_S} \qquad (3.92)$$

Thus the width of the coulomb blockade ΔV_D can be obtained from equation (3.92) as:

$$\Delta V_D = \frac{\frac{e}{2} + Q_0}{C_S} - \frac{-\frac{e}{2} - Q_0}{C_D}$$

$$= \frac{\frac{e}{2} + Q_0}{C_S} + \frac{\frac{e}{2} + Q_0}{C_D}$$

$$= \frac{C_S + C_D}{C_D C_S}\left(\frac{e}{2} + Q_0\right)$$

$$\therefore \Delta V_D = \frac{C_\Sigma}{C_D C_S}\left(\frac{e}{2} + Q_0\right) \qquad (3.93)$$

The inequalities (2.101) and (2.102) that we used to set the range of ΔV_D can be written as:

$$\frac{-\frac{e}{2} + Q_0}{C_S} < \frac{-\frac{e}{2} - Q_0}{C_D} \qquad (3.90)$$

$$\frac{C_D}{C_S} > \frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0} \qquad (3.90)(a)$$

And

$$\frac{\frac{e}{2} + Q_0}{C_S} < \frac{\frac{e}{2} - Q_0}{C_D} \qquad (3.91)$$

$$\frac{C_D}{C_S} < \frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} \qquad (3.91)(a)$$

$$\therefore \quad \frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0} < \frac{C_D}{C_S} < \frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} \qquad (3.94)$$

D. If the two lower limits are compared as:

$$\frac{-\frac{e}{2} + Q_0}{C_S} < \frac{-\frac{e}{2} - Q_0}{C_D} \ldots\ldots\ldots..(3.90)$$

And if the two upper limits are compared as:

$$\frac{\frac{e}{2} + Q_0}{C_S} < \frac{\frac{e}{2} - Q_0}{C_D} \ldots\ldots\ldots(3.91)$$

then V_D is limited in the range as

$$\frac{-\frac{e}{2} - Q_0}{C_D} < V_D < \frac{\frac{e}{2} + Q_0}{C_S} \ldots\ldots\ldots\ldots..(3.92)$$

Thus the width of the coulomb blockade ΔV_D can be obtained from equation (3.92) as:

$$\Delta V_D = \frac{\frac{e}{2} + Q_0}{C_S} - \frac{-\frac{e}{2} - Q_0}{C_D}$$

$$= \frac{\frac{e}{2} + Q_0}{C_S} + \frac{\frac{e}{2} + Q_0}{C_D}$$

$$= \frac{C_S + C_D}{C_D C_S}\left(\frac{e}{2} + Q_0\right)$$

$$\therefore \Delta V_D = \frac{C_\Sigma}{C_D C_S}\left(\frac{e}{2} + Q_0\right) \ldots\ldots\ldots\ldots (3.95)$$

The inequalities (3.90) and (3.91) that we used to set the range of ΔV_D can be written as:

$$\frac{-\frac{e}{2} + Q_0}{C_S} < \frac{-\frac{e}{2} - Q_0}{C_D} \ldots\ldots\ldots.. (3.90)$$

$$\frac{C_D}{C_S} > \frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0} \ldots\ldots\ldots.. (3.90)(a)$$

And

$$\frac{\frac{e}{2} + Q_0}{C_S} < \frac{\frac{e}{2} - Q_0}{C_D} \ldots\ldots\ldots (3.91)$$

$$\frac{C_D}{C_S} < \frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} \ldots\ldots\ldots (3.91)(a)$$

$$\therefore \quad \frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0} < \frac{C_D}{C_S} < \frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} \ldots\ldots\ldots\ldots\ldots. (3.96)$$

The four cases discussed above are summarized In Table 2.1. The width of coulomb blockade ΔV_D and the ratio of capacitance $\frac{C_D}{C_S}$ are listed for etch case.

It can be seen that the width of coulomb blockade is controlled by the background charge and ratio of capacitance $\frac{C_D}{C_S}$. By some given values of these two parameters we can further understand how the width of coulomb blockade can be affected.

Since $|Q_0| < \frac{e}{2}$, we can first consider the case when $Q_0 = 0$. If we have $C_S = C_D = C$, ΔV_D can be obtained from case A and D as

$$\Delta V_D = \frac{C_\Sigma}{C_D C_S}\left(\frac{e}{2} \pm Q_0\right)$$

$$\Delta V_D = \frac{C + C}{C.C}\left(\frac{e}{2} \pm 0\right)$$

$$\Delta V_D = \frac{2C}{C^2}.\frac{e}{2}$$

$$\therefore \Delta V_D = \frac{e}{C} \tag{3.97}$$

Table 3.1 Width of the Coulomb blockade

ΔV_D and the ratio of junction capacitance for case A - D

	ΔV_D	$\frac{C_D}{C_S}$
A	$\frac{C_\Sigma}{C_S C_D}\left(\frac{e}{2} - Q_0\right)$	$\frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} < \frac{C_D}{C_S} < \frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0}$
B	$\frac{e}{C_S}$	$\frac{C_D}{C_S} < \frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} \quad if\ 0 < Q_0 < \frac{e}{2}$ $< \frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0} \quad if\ \frac{-e}{2} < Q_0 < 0$
C	$\frac{e}{C_D}$	$\frac{C_D}{C_S} > \frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0} \quad if\ 0 < Q_0 < \frac{e}{2}$ $> \frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} \quad if\ \frac{-e}{2} < Q_0 < 0$
D	$\frac{C_\Sigma}{C_S C_D}\left(\frac{e}{2} + Q_0\right)$	$\frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0} < \frac{C_D}{C_S} < \frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0}$

In addition, for $Q_0 = 0$, it can also be seen from Table 2.1 that when $C_S \neq C_D$, that ratio $\frac{C_D}{C_S}$ is either smaller than 1 (case B) or larger than1 (case C). From equation (3.83), the width of coulomb blockade ΔV_D in case B is obtained as:

$$\Delta V_D = \frac{e}{C_S} \tag{3.83}$$

Insert $Q_0 = 0$ to inequality (3.84)(a) or (3.84)(b), we have:

$$\frac{C_D}{C_S} < \frac{\frac{e}{2} - 0}{\frac{e}{2} + 0} \qquad (3.84)(a)$$

$$\frac{C_D}{C_S} < 1$$

$$\therefore C_D < C_S$$

or

$$\frac{C_D}{C_S} < \frac{-\frac{e}{2} - 0}{-\frac{e}{2} + 0} \qquad (3.84)(b)$$

$$\frac{C_D}{C_S} < 1$$

$$\therefore C_D < C_S$$

From Equation (3.88), width of coulomb blockade ΔV_D in case C is obtained as:

$$\Delta V_D = \frac{e}{C_D} \tag{3.88}$$

Insert $Q_0 = 0$ to inequality (3.89)(a) or (3.89)(b), we have

$$\frac{C_D}{C_S} > \frac{-\frac{e}{2} - 0}{-\frac{e}{2} + 0} \qquad (3.89)(a)$$

$$\frac{C_D}{C_S} > 1$$

$$\therefore C_D > C_S$$

or

$$\frac{C_D}{C_S} > \frac{\frac{e}{2} - 0}{\frac{e}{2} + 0} \qquad (3.89)(b)$$

$$\frac{C_D}{C_S} > 1$$

$$\therefore C_D > C_S$$

Summarized the conditions above, we can conclude that when $C_S \neq C_D$, the width of the Coulomb blockade is presented as:

$$\Delta V_D = \frac{e}{\max(C_S, C_D)} \quad (3.98)$$

when $Q_0 = +\frac{e}{2}$, from equation (3.78),

$$\Delta V_D = \frac{C_\Sigma}{C_S C_D}\left(\frac{e}{2} - Q_0\right)$$

$$\therefore \Delta V_D = \frac{C_\Sigma}{C_S C_D}\left(\frac{e}{2} - \frac{e}{2}\right)$$

$$= 0$$

Thus there is no coulomb blockade when $Q = +\frac{e}{2}$. Similarly, when $Q_0 = -\frac{e}{2}$, from equation (3.93),

$$\Delta V_D = \frac{C_\Sigma}{C_S C_D}\left(\frac{e}{2} + Q_0\right)$$

$$\Delta V_D = \frac{C_\Sigma}{C_S C_D}\left[\frac{e}{2} + \left(-\frac{e}{2}\right)\right]$$

$$\therefore \Delta V_D = 0$$

Thus there is no coulomb blockade when $Q_0 = -\frac{e}{2}$. Simulated Coulomb blockades with different value of Q_0 are illustrate in Figure 3.14.

3.5.2 Coulomb Staircase

The Coulomb staircase is an I-V phenomenon which has a staircase like structure in single electron device. It occurrs when single electron device have asymmetric tunneling junctions. The appearance of Coulomb staircase is due to the Coulomb blockade taking place periodically with increasing or decreasing source-drain bias.

The mechanism of Coulomb staircase can be qualitatively understood by the free energy diagram as illustrated in Figure 3.15. Staring with an unbiased double junction single electron device which has the Coulomb island with chemical potential $g_{IS}(N)$ as shown in Figure 3.15 (a). N is the number of excess electrons in the Coulomb island.If we

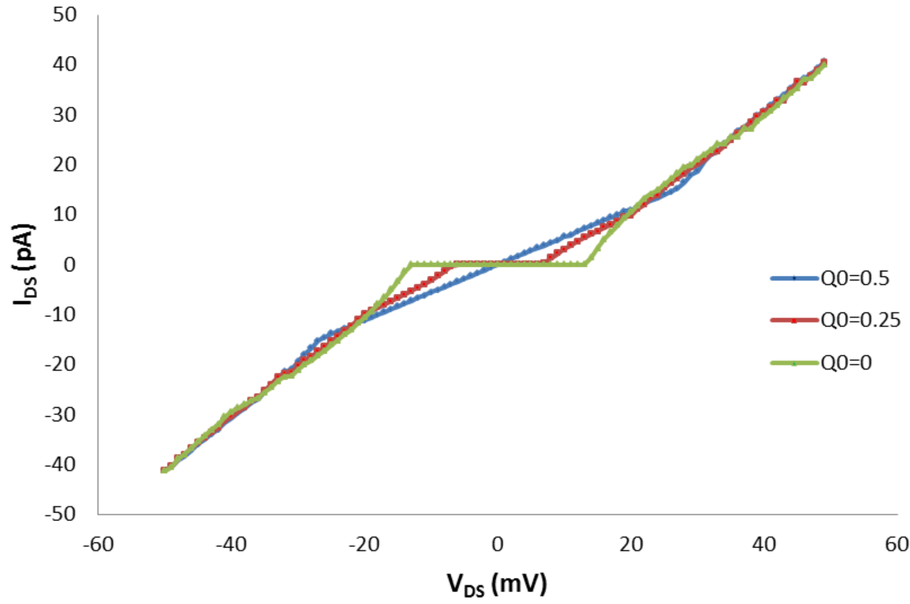

Figure 3.14 Simulated Coulomb blockade for a double junction single electron device with $Q_0 = 0$, $Q_0 = \frac{1}{4}$, and $Q_0 = \frac{1}{2}$. Simulation parameters used for all three case: $C_s = C_D = 0.85aF$, $R_s = R_D = 0.8G\Omega$

applied a negative bias to source electrode V_{DS} and keep the drain electrode grounded, the Fermi level of source will rise up with increased bias and finally aligned with the Fermi level of Coulomb island as showing in Figure 3.15 (b). This is the onset bias of Coulomb blockade since electrons start to be tunneled to the island at this bias. With increasing the bias, the Fermi level is rising up above $g_{IS}(N)$, but is not aligned with $g_{IS}(N+1)$. From Figure 3.15 (c), now it can be seen that the Coulomb island has $N+1$ electron and the electrostatic potential of the coulomb island raised up due to the addition of an electron. Before this electron tunnel out to the drain, the free energy change ΔF for the transition of state $N+1$ to $N+2$ is larger than zero which indicated the second electron cannot be tunneled to the Coulomb island at this applied bias. This is the second Coulomb blockade for the transition of state from N+1 to N+2. When the applied bias raise the Fermi level of source to align with $g_{IS}(N+1)$ as in Figure 3.15 (d), tunneling can

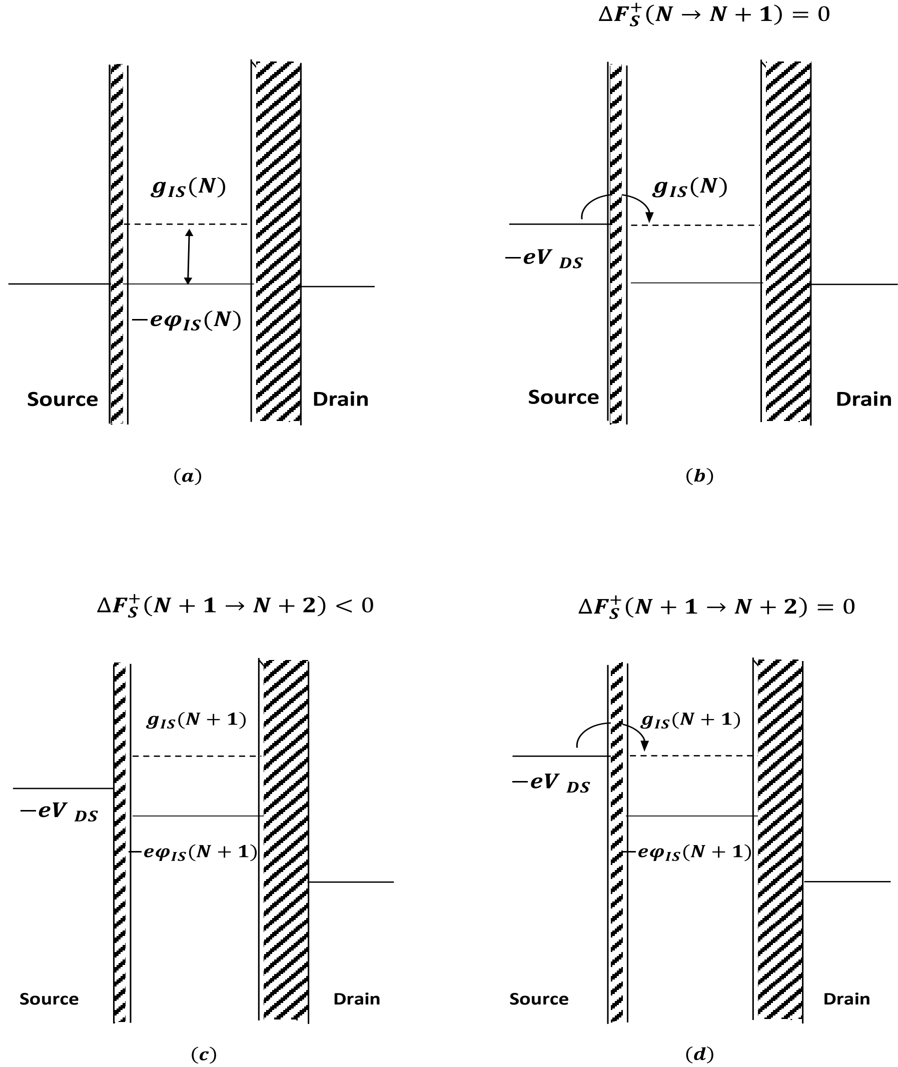

Figure 3.15 Free energy diagram for the mechanism of Coulomb staircase in a double junction single electron device with asymmetric tunneling junctions. (a). No source-drain bias V_{Ds} applied to the device. (b) Increase V_{Ds} until the Fermi level of the source electrode aligned with the chemical potential $g_{IS}(N)$ of Coulomb island. Free energy change $\Delta F_S^+(N \to N+1) = 0$ indicates the tunneling can take place for the transition of state from N to N+1. (c) One electron has been tunneled to Coulomb island, the electrochemical potential of Coulomb island raised. With further increased V_{Ds} from (b), the tunneling cannot take place due to $\Delta F_S^+(N+1 \to N+2) < 0$. (d) Increased V_{Ds} brings the Fermi level for source aligned with $g_{IS}(N+1)$, $\Delta F_S^+(N+1 \to N+2) = 0$, therefore a second electron can be tunneled to the Coulomb island.

be taken place since the free energy change ΔF is zero. That means a second electron can be added in to Coulomb island thus the island is in the state of N+2. From this discussion we know that each stair step (flat region) represents the number of excess electrons reside in Coulomb island. Starting from N=0, with increasing applied bias V_{DS} we can have N+1, then N+2 and N+3 and so on.

The asymmetric tunneling junctions that we mentioned earlier describes tunneling junctions such that have $C_S R_S >> C_D R_D$ or $C_S R_S << C_D R_D$. For a case of $C_S < C_D$ and $R_S \ll R_D$ so that $C_S R_S << C_D R_D$ in a single electron device was shown Figure 3.16. The tunneling rate of electron tunneling from source to the Coulomb island is much faster than from Coulomb island to drain since $R_S \ll R_D$. From Figure 3.16 (c), once an electron was tunneling in to the coulomb island, it takes longer time to tunnel out to the drain as shown in Figure 3.16 (d). As long as the electron tunnels to drain, the Coulomb island is immediately refilled with another electron from source. This is illustrated in Figure 3.16 (c). Therefore the island is always remaining in charged state. The charging energy due to the excess electron in coulomb island blocked the following electron to go into the Coulomb island, thus we have the second Coulomb blockade regime for the transition of N+2.

Similarly, if the tunneling junctions has $C_S > C_D$ and $R_S \gg R_D$ so that $C_S R_S \gg C_D R_D$ as shown in Figure 3.17, the tunneling rate is limited by R_S, which means it takes longer time for the electron to tunnel in to the Coulomb island than it does to tunnel out. As shown in Figure 3.17 (c), Coulomb island is remaining in a charged state of $N-1$ because once the electron goes into the Coulomb island, it will be tunneled out immediately. With further increasing V_{DS} from (b), no tunneling occurs and device was in the Coulomb blockade regime for the state of N-1.

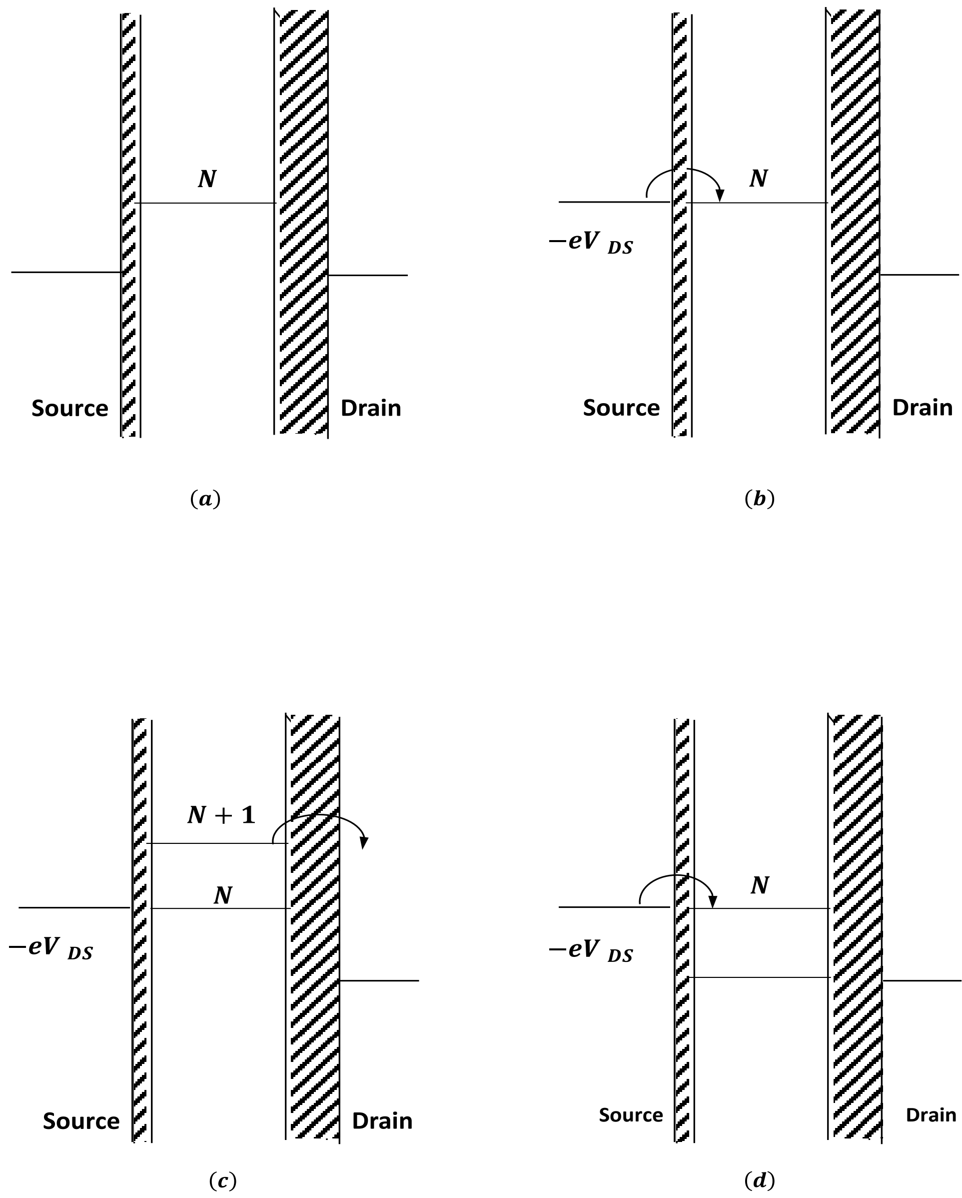

Figure 3.16 Electron tunneling in a asymmetric tunneling junction ($C_S < C_D$ and $R_S \ll R_D$; $C_S R_S << C_D R_D$). (a) Before applied bias V_{DS}. (b) Electron starts to tunnel from source to Coulomb island. (c) One excess electron tunneled to Coulomb island thus it has the state N+1. The Coulomb island remains in this state since the tunneling rate is much slower to tunnel out of the island. (d) Once the electron tunnel out to drain, Coulomb island was refilled by the electron from source immediately and went back to the state in (c).

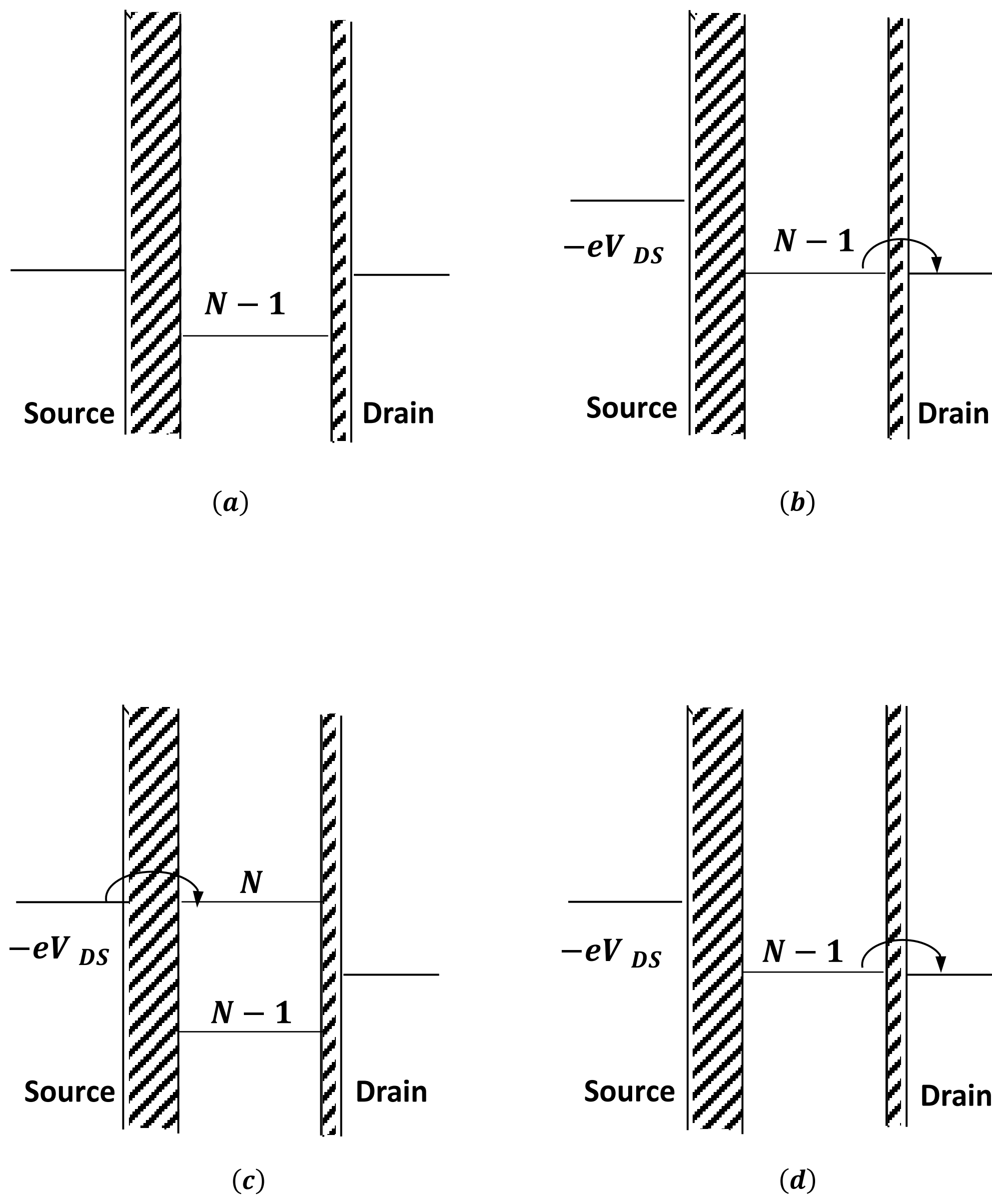

Figure 3.17 Electron tunneling in a asymmetric tunneling junction ($C_S > C_D$ and $R_S \gg R_D$; $C_S R_S \gg C_D R_D$). (a) Before applied bias V_{DS}. (b) Electron tunnels from Coulomb island to drain. (c) One electron tunneled out of Coulomb island thus it has the state N-1. The Coulomb island remains in this state since the tunneling rate is much slower to tunnel in to Coulomb island. (d) Once the electron tunnel in, electron tunneled out of Coulomb island to drain immediately and went back to the state in (c).

A calculated IV characteristic for a double junction single electron device is shown in Figure 3.18 to simulate the Coulomb staircase. The simulation parameter are $C_S = 3aF$, $C_D = 30aF$, $R_S = 80\ M\Omega$, $R_D = 8\ G\Omega$, $Q_0 = 0$ and $T = 0K$.

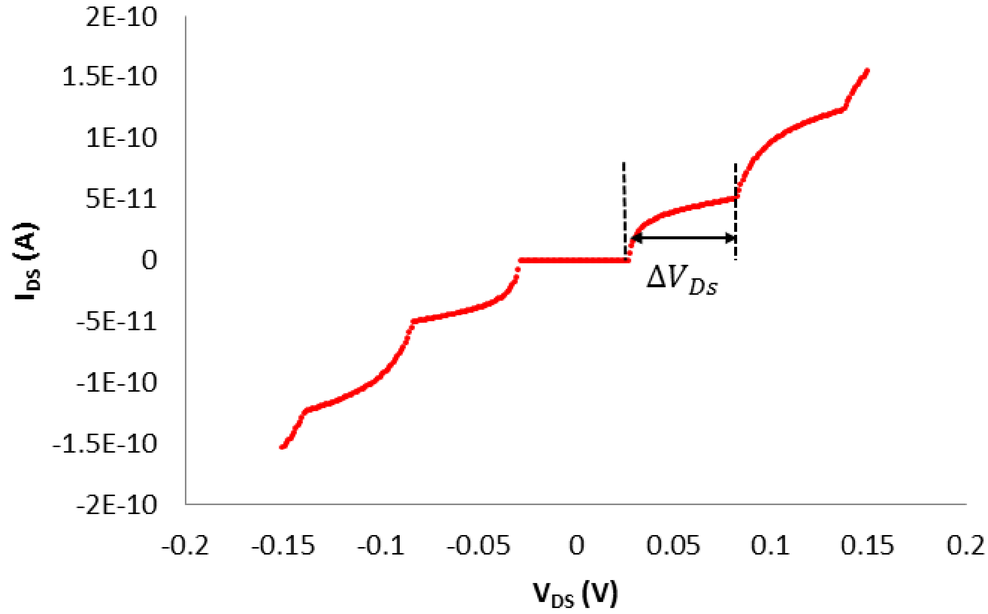

Figure 3.18 Simulated Coulomb Staircase for double junction single electron device with asymmetric tunneling junctions. The width of Coulomb blockade $\Delta V_{DS} = \frac{e}{C_D}$.

The Coulomb Blockade at state N=0 in Figure3.18 is the same as we discussed in the section of Coulomb blockade. The width of the step is obtained from Equation (2.107) for an asymmetric tunneling junction

$$\Delta V_{DS} = \frac{e}{\max(C_S, C_D)}$$

The width of the Coulomb blockade ΔV_{DS} indicates the energy for adding an electron to or removing an electron from Coulomb island therefor it can be considered as a representation of charging energy. Since the charging energy is $E_C = \frac{e^2}{C_\Sigma}$ and is

independent of N, the width of the step for each state such as N+1 or N+2 will be the same as N. The calculation of the width of current step in Coulomb staircase can be obtained by the free energy change. It will be the same as the ΔV_{DS} that we calculated in the section of Coulomb blockade.

We can check the condition for a step in Coulomb staircase presented as N+1. Consider the $Q_0 = 0$ and N=0 in a device with asymmetric junctions such that $C_S R_S <<$ $C_D R_D$. If a source-drain bias $V_{DS}$is applied as illustrated in Figure 3.15 (c), the free energy change $\Delta F_S^+(1 \rightarrow 2)$ is larger than zero for the state of $1 \rightarrow 2$ since the electron can not be tunneled to Coulomb island. This gives the inequality for the V_{DS} from Equation (3.45) as:

$$\frac{e}{C_\Sigma}\left[\frac{e}{2} + (1e - Q_0) - C_D V_{DS}\right] > 0$$

$$\therefore V_{DS} < \frac{3e}{2} \cdot \frac{1}{C_D} \qquad (3.99)(a)$$

The free energy change $\Delta F_S^+(0 \rightarrow 1)$ is smaller than zero for the state of $0 \rightarrow 1$ since the electron can be tunneled to Coulomb island for this condition, then V_{DS} is in the Inequality resulted from Equation (3.45) as:

$$\frac{e}{C_\Sigma}\left[\frac{e}{2} + (0e - Q_0) - C_D V_{DS}\right] < 0$$

$$\therefore V_{DS} > \frac{e}{2} \cdot \frac{1}{C_D} \qquad (3.99)(b)$$

The free energy change $\Delta F_D^-(1 \rightarrow 0)$ is smaller than zero for the state of $1 \rightarrow 0$ since the electron can be tunneled out from Coulomb island. This gives the inequality for the V_{DS} from Equation (3.52) as:

$$\frac{e}{C_\Sigma}\left[\frac{e}{2} - (1e - Q_0) - C_S V_{DS}\right] < 0$$

$$\therefore V_{DS} > \frac{-e}{2} \cdot \frac{1}{C_S} \qquad (3.99)(c)$$

Compare the Inequalities (3.99)(a), (3.99)(b), and (3.99)(c), we obtain the range of V_{DS} as:

$$\frac{e}{2} \cdot \frac{1}{C_D} < V_{DS} < \frac{3e}{2} \cdot \frac{1}{C_D} \tag{3.100}$$

Thus ΔV_{DS} can be obtained as:

$$V_{DS} = \frac{3e}{2} \cdot \frac{1}{C_D} - \frac{e}{2} \cdot \frac{1}{C_D}$$

$$\therefore V_{DS} = \frac{e}{C_D}$$

This is the same as what we obtained from Equation (3.98).

3.5.3 Coulomb Oscillation

When a gate bias V_G is applied to a double junction single electron transistor under a constant source-drain bias V_{DS}, the I-V characteristic which has a structure of periodic peaks of current oscillating with swept gate biasV_G is known a s Coulomb oscillation.

The mechanism of Coulomb oscillation can be qualitatively understood by the free energy diagram of the electron transition in the device with gate bias applied. A schematic free energy diagram is illustrated In Figure 3.19. As a small source-drain bias V_{DS} is applied as shown in Figure 3.19 (b), electron cannot tunneled to the Coulomb island due to insufficient energy to overcome the charging energy and the device is in the Coulomb blockade regime. If now the gate bias V_G is applied to the device as shown in Figure 3.19 (c), it can lower down the chemical potential μ_N of Coulomb island so that chemical potential of source $\mu_S = -eV_{DS}$ is aligned with the μ_N. As long as two chemical potentials of source and Coulomb island are aligned, electron can tunneled to the Coulomb island at the applied V_G. Once the electron tunneling in to the Coulomb island, it can tunnel out to drain since the chemical $\mu_N + 1$ is higher than the chemical potential of drain. This is skown in Figure 3.19 (d). A conductance peak will show up at this V_G in the I_{DS}-V_G of the device. If we keep increasing the V_G from Figure 3.19 (c), it will enter another Coulomb blockade regime with the electron occupancy N+1 since the μ_S is not aligned

with μ_N. Appearance of this Coulomb blockade in the plot of I_{DS}-$V_G$is the bottom flat region separate by the conductance peaks.

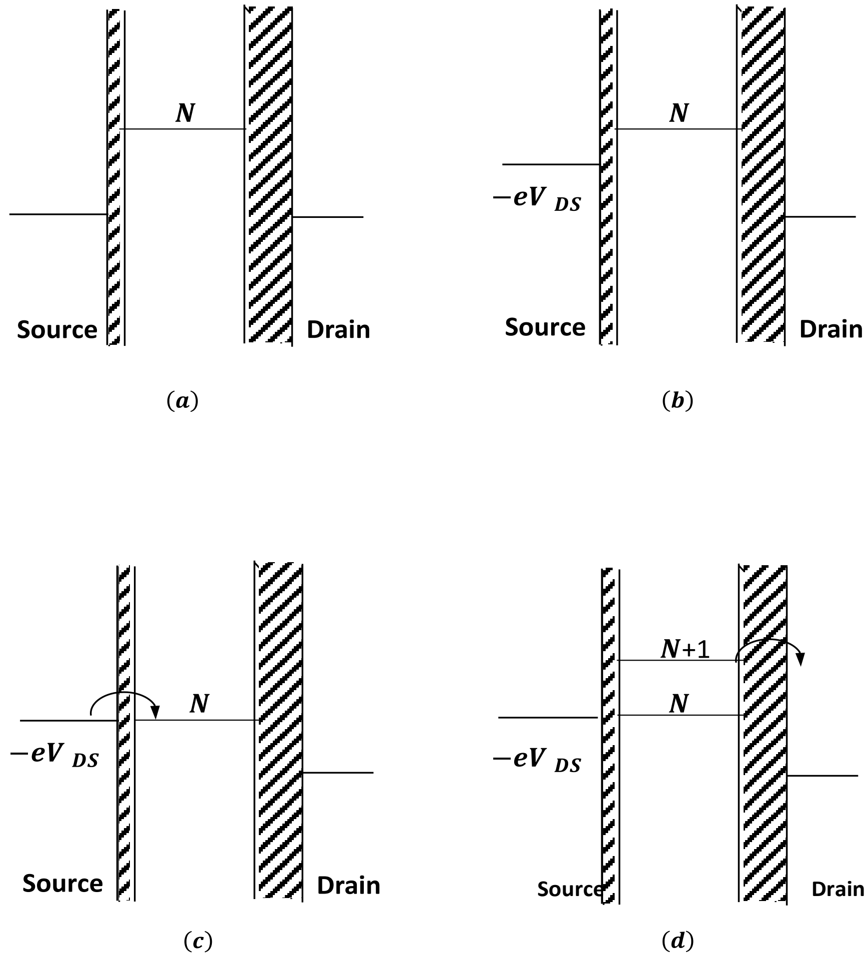

Figure 3.19 Electron tunneling in a asymmetric tunneling junction ($C_S < C_D$ and $R_S \ll R_D$; $C_S R_S \ll C_D R_D$). (a) Before applied Bias V_{DS}. (b) Electron tunnels from source to Coulomb island. (c) One electron tunneled out of Coulomb island thus it has the state N-1. The Coulomb island remains in this state since the tunneling rate is much slower to tunnel in to Coulomb island. (d) Once the electron tunnel in, electron tunneled out of Coulomb island to drain immediately and went back to the state in (c)

A simulated I_{DS}-V_G plot for coulomb Oscillation is demonstrated in Figure 3.20. The bottom flat region next to the peaks is indicated as the Coulomb blockade region for the electron occupancy N, N+1, and N-1. The separation between peaks V_G indicates the energy required to add or remove one electron to or from the Coulomb island.

The addition or subtraction of an electron to or from the Coulomb island requires energy. This energy can be obtained from charging energy of the single electron transistor from Equation 2.81.

$$E_C = \frac{e^2}{C_{TOT}}$$

Since we only swept the gate bias V_G and keep the source-drain bias V_{DS} constant to obtain the Coulomb oscillation, V_G is the source which providing the energy to cause the transition of the electron in Coulomb oscillation. The peaks separation ΔV_G can be obtained from the change of charge $\Delta Q_G^{N\pm1,N}$ and the charging energy E_C. $\Delta Q_G^{N\pm1,N}$ is the charge change induced by the gate and can be obtained from Equation (2.53).

$$\Delta Q_G^{N\pm1,N} = \pm\frac{C_G}{C_{TOT}}e$$

By adding or subtracting an electron through ΔV_G to the coulomb island in singe electron transistor, we have the charge change $\Delta Q_G^{N\pm1,N}$. Thus the energy change of the system $\Delta V_G \Delta Q_G^{N\pm1,N}$ is the charging energy E_C. Then the ΔV_G is obtained from

$$\Delta V_G \Delta Q_G^{N\pm1,N} = E_C$$

$$\Delta V_G \frac{C_G}{C_{TOT}} e = \frac{e^2}{C_{TOT}}$$

$$\therefore \Delta V_G = \frac{e}{C_G} \tag{3.101}$$

The interval ΔV_G between the conduction peaks of the Coulomb oscillation is therefore $\frac{e}{C_G}$.

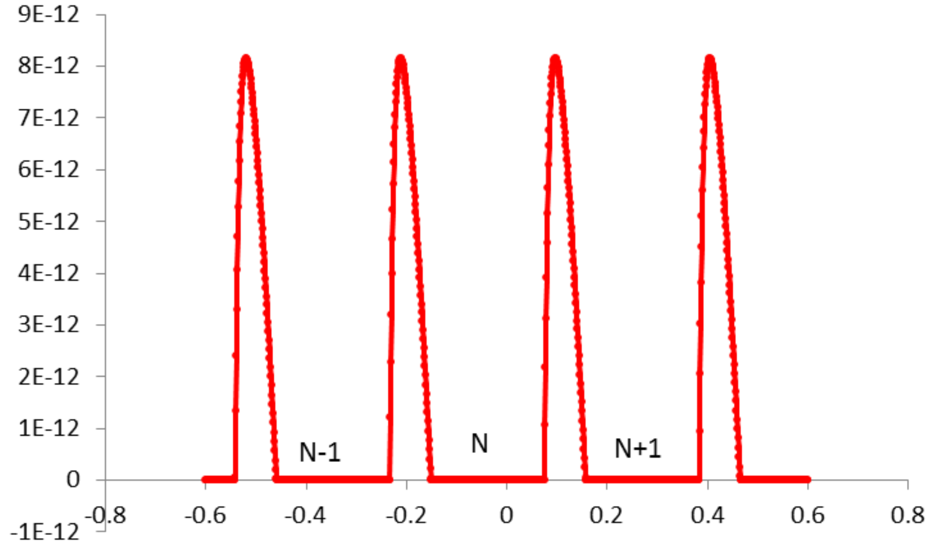

Figure 3.20 Simulated Coulomb oscillation for a double junction single electron device.

3.6 Model for Single Electron Transistor

From previous sections the free change ΔF has been calculated for electron tunneling from all possible configurations. According to the Fermi's golden rule [27], the tunneling rates can be obtained according to the free energy change ΔF and tunneling resistance as following:

$$\Gamma_j^{\pm}(N) = \frac{1}{R_j e^2} \times \frac{-\Delta F_j^{\pm}(N)}{1 - exp\left[\frac{\Delta F_j^{\pm}(N)}{k_B T}\right]} \tag{3.102}$$

Where $\Delta F_j^{\pm}$ is the free energy change in the system when an electron tunnel through the tunnel junction j, R_j is the tunneling resistance of junction j, k_B is the Bolzmann constant (8.617 x 10^{-5} eV/K), e is the electron unite charge (1.602 x 10^{-19} Coulombs), and T is the absolute temperature.

Since the tunneling rates can be all calculated, we can construct a model to describe the electron transitions in a double junction single electron transistor. Based on this model, the tunneling current I as a function of applied source-drain bias V can be calculated.

3.6.1 Components in the Model

Based on the structure of single electron transistor that we fabricated, a model illustrated by the energy diagram is shown in Figure 3.21. This model consists of two tunneling barriers which separate the source(S), Coulomb island (IS) and drain(D).

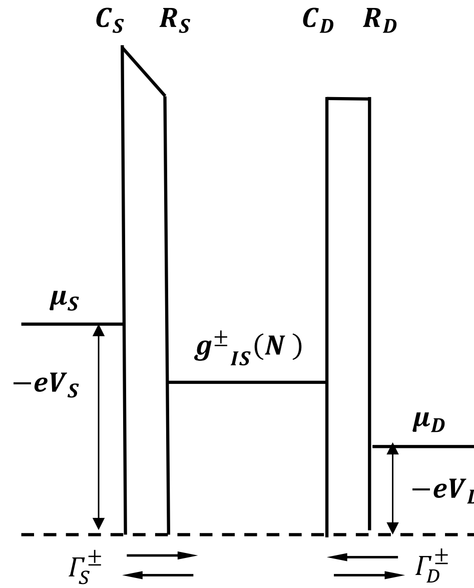

Figure 3.21 Model of a double junction single electron transistor.

Electrons can only be tunneled through the tunneling junctions between each adjacent component, i.e. electron can tunnel from source to Coulomb island, then from Coulomb island to drain. The tunneling rate Γ is calculated through the free energy change ΔF which is function of junction capacitance C and external bias V and electron occupancy in the Coulomb island N. The definition of the tunneling rate and other parameters are described as below:

- $\Gamma_s^{\pm}(N)$: the rate for an electron tunneling from the source electrode (S) to the Coulomb island ("+") or from Coulomb island to source ("–") when the number of electrons in the Coulomb island before tunneling is N

- $\Gamma_D^{\pm}(N)$: the rate for an electron tunneling from drain to Coulomb island ("+") or from Coulomb island to drain ("–") when the number of electrons in the Coulomb island before the tunneling is N.
- $\Delta F_S^{\pm}(N)$: change of free energy for an electron tunneling from source to Coulomb island ("+") or from Coulomb island to source ("–") when the number of electrons in Coulomb island before tunneling is N.
- $\Delta F_D^{\pm}(N)$: change of free energy for an electron tunneling from drain to Coulomb island ("+") or from Coulomb island to drain ("–") when the number of electrons in Coulomb island before tunneling is N.
- $g_S^{\pm}(N)$: chemical potential of Coulomb island when an electron is added to Coulomb island (+) or subtracted from Coulomb island ("–") when the number of electrons in Coulomb island before tunneling is N
- V_S : the bias applied to source
- V_D : the bias applied to drain
- V_D : the bias applied to gate
- μ_S: the chemical potential of source
- μ_D: the chemical potential of drain
- C_S: the capacitance of the tunneling barrier between source and Coulomb island.
- C_D: the capacitance of the tunneling barrier between Coulomb island and drain.
- C_G: the capacitance of gate
- R_S: the tunneling resistance of the tunneling barrier between source and Coulomb island.
- R_D: the tunneling resistance of the tunneling barrier between Coulomb island and drain.

The transportation of electron in a single electron transistor can be described by the terns defined above in the rate equations.

3.6.2 Rate Equations

The tunneling rate is constructed by the free energy change and tunneling resistance of the tunneling junctions as in equation (3.102). Since the free energy changes were calculated in equation (3.48) and (3.53) as:

$$\Delta F_S^{\pm} = \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} \pm (Ne - Q_0)\right] \mp [C_D(V_D - V_S) + C_G(V_G - V_S)]\right\} \qquad (3.48)$$

$$\Delta F_D^{\pm} = \frac{e}{C_{TOT}}\left\{\left[\frac{e}{2} \pm (Ne - Q_0)\right] \mp [C_D(V_S - V_D) + C_G(V_G - V_D)]\right\} \qquad (3.53)$$

Therefore we can obtained the rate of all possible configurations as listed below:

$$\Gamma_S^{+}(N) = \frac{1}{R_S e^2} \times \frac{-\Delta F_S^{+}(N)}{1 - exp\left[\frac{\Delta F_S^{+}(N)}{k_B T}\right]} \qquad (3.103)$$

$$\Gamma_S^{-}(N) = \frac{1}{R_S e^2} \times \frac{-\Delta F_S^{-}(N)}{1 - exp\left[\frac{\Delta F_S^{-}(N)}{k_B T}\right]} \qquad (3.104)$$

$$\Gamma_D^{+}(N) = \frac{1}{R_D e^2} \times \frac{-\Delta F_D^{+}(N)}{1 - exp\left[\frac{\Delta F_D^{+}(N)}{k_B T}\right]} \qquad (3.105)$$

$$\Gamma_D^{-}(N) = \frac{1}{R_D e^2} \times \frac{-\Delta F_D^{-}(N)}{1 - exp\left[\frac{\Delta F_D^{-}(N)}{k_B T}\right]} \qquad (3.106)$$

3.6.3 Master Equations

Now we define $P(N)$ as the probability that the number of excess electrons occupying the Coulomb island is N. At a steady state, the net transition is zero thus the

transition between two adjacent states have the same tunneling rates. Based on this, the master equation is composed as:

$$P(N)[\Gamma_S^+(N) + \Gamma_D^+(N)] = P(N+1)[\Gamma_S^-(N+1) + \Gamma_D^-(N+1)] \tag{3.107}$$

Also, as $P(N)$ is the probability of occupancy of Coulomb island, the summation with N should be equal to the unity 1.

$$\sum_N \mathrm{P}(N) = 1 \tag{3.108}$$

The tunneling current I as a function of V then can be obtained from the drain as:

$$I(V) = e\sum_{-\infty}^{\infty} P(N)[\Gamma_D^-(N) - \Gamma_D^+(N)] \tag{3.109}$$

With the given sets tunneling rate from the specified V_S and V_D and V_G, the unknown $P(N)$ should be obtained by solving the simultaneous equation generated from equation (3.107). Therefore the current $I(V)$ can be obtained as well.

Chapter 4

Fabrication of Single Electron Device

4.1 Introduction

A schematic structure of our proposed single electron device is shown in Figure 4.1. The detailed fabrication process steps for making a single electron device are described in this chapter. Starting with a blank Si substrate, a 4 inch Si wafer as a substrate will go through various fabrication processes including thermal oxidation, optical photolithography, metallization, plasma enhanced vapor deposition (PECVD), reactive plasma etching (RIE), self-assembly monolayer deposition (SAMs), and sputtering deposition. Processing equipment used are described in detail in the UTA NanoFab Facility home pages [28].

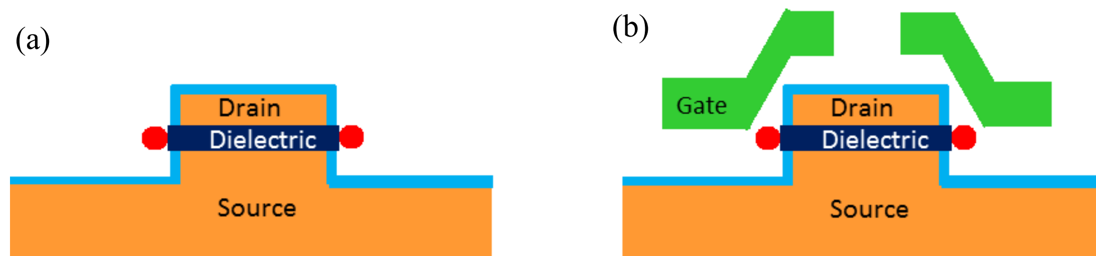

Figure 4.1 Schematic of the structure of proposed single electron device. (a) Single electron device. (b) Single electron transistor.

4.2 Thermal Oxidation

The bare silicon wafer was cleaned with a Piranha solution before going to thermal oxidation furnace. The Piranha solution is prepared with H_2O_2 and H_2SO_4 with a ratio of 1:3. After 30 minutes of immersion in the Piranha solution, the Si wafer was then thoroughly rinsed with water in 2 different water baths in order to get rid of any residuals from the piranha solution. Following the piranha cleaning, the wafer was cleaned with IPA

and methanol to get rid of any other organic impurities and residuals from the piranha cleaning procedures.

1 um SiO_2 was growled on the Si wafer by wet thermal Oxidation process at 1100C at Tystar oxidation furnace. The furnace was preheated to 700C with N_2 ambient before loading the wafer for 30 minutes. When the furnace temperature stabilized at 1100C for 30 minutes, the wafer was slowly loaded into the center of the tube with a rate of 3ins/min to avoid thermal shock. 10 mines after wafer was loaded into the tube and thermally stabilized, water vapor was introduced to the tube with a bubbler system. The bubbler system contains preheated DI water (resistivity > 18.2 MΩ.cm) at 90C and delivers the vapor using N_2 as a carrier gas to the furnace tube. Wet oxidation process was then initiated by flowing O_2 gas at 3liters/minute.

The target thickness of 1um SiO_2 film is reached in 3 hours. After the oxidation process is completed, the O_2 and water flow are cut off and N_2 is will be supplied to the furnace tube while temperature is dropping at a rate of 50c/min to 200C. After the fell temperature is below 200C, the wafer was unloaded from the tube with a rate of 3 in/min.

4.3 Defining the Source Electrode

The source electrode was defined by a 200 nm Cr pattern with a lift-off process on top of the thermal oxide substrate. The substrate was cleaned first with UV-O_3 for 30 minutes. This ensures a removal of any contaminants accumulated during the wafer handling process before the photolithography process.

Photolithography was carried out in order to define the pattern of the source electrode before metal deposition. The substrate was spin coated with a negative photoresist NR9-1000PY (Futurrex Inc.) at spinning speed of 2000rpm/min for 30minutes. This coats the substrate with a 1.3um layer of photoresist. Substrate was then placed on a hot plate at 150C for 2 minutes of prebaking. After the prebake, the substrate was mounted to a sample holder of an aligner. The OAI backside aligner uses a primary wavelength of 365 nm from a mercury short-arc lamp to perform the alignment and

exposure of the coated substrate. The exposure time was 13 seconds. Immediately after the exposure step, a 1 minute post exposure bake at 100 C^0 followed. When post exposure bake was done, further development was carried out by immersing the substrate in the developer RD6 (Futurrex Inc.) for 17 seconds. Then developer was them washed away by rinsing DI water for 30 seconds. After the developer was removed, the substrate was then blown dry N_2. The photoresist pattern was then checked using an optical microscope in order to insure that the photolithography process was well articulated.

Metallization was carried out on the AJA e-beam evaporator. The substrate which now has a patterned photoresist was first clamped on a sample holder and put into a load lock chamber of the evaporator before going into the main chamber. After the load lock vacuum reached a pressure $< 1 \times 10^{-5}$ Torr, the sample holder will was transferred to the main chamber which was always maintained at a pressure below 1×10^{-7} Torr. The metal Cr was chosen to be both the source and drain electrode. 200 nm Cr layer was deposited in the main chamber with the deposition rate around 2 to 3 Å/sec. After unloading from evaporator, the substrate went for a lift-off process. The substrate was immersed in an acetone bath with ultrasonic agitation for 5 minutes then blown dry under a stream of N_2. This removed the photoresist and leaving the desired Cr pattern which serves as the source electrode of the device on the substrate. In order to remove the residual photoresist completely from the lift-off process, we put the substrate through a UV-O_3 cleaner for 30 minutes.

4.4 Isolation between Source and Drain

A thin film of SiO_2 was used as an isolation layer between the source and drain electrode. According to the size of quantum dot (nanoparticle) we used, the thickness of the dielectric layer was carefully chosen. Plasma enhanced vapor deposition (PECVD) technique was used after depositing our dielectric layer because the quality of this thin

layer in such attributes as leakage current, breakdown voltage, and surface roughness is superior to other deposition techniques.

The PECVD chamber was well cleaned with a wet clean procedure and all the parts inside the chamber were wiped with isopropyl alcohol to physically remove any residual particles from the previous runs before deposition. The chamber was then pumped down to 1m Torr for 4 hours. After pumping down, the chamber was heated up to 360 C^0 which was the deposition temperature and plasma clean and preconditioning procedures were followed. Plasma cleaning can further remove organic residuals in the chamber The parameters of the chamber cleaning recipe are described as below:

- Top Electrode Power = 400W
- Bottom Electrode Power = 35W
- Pressure = 600m Torr
- CF_4= 100 SCCM
- N_2O = 10 SCCM
- Temperature = 360C
- Time = 180 sec

After the plasma cleaning, we ran 10 seconds of the chamber precondition recipe before the following deposition process for our samples. Chamber precondition procedure is very important especially for a thin film deposition as we targeted for a thickness less than 10nm. When initiating the plasma for a deposition process, it takes few seconds (around 3 to 5 seconds) to stabilize the plasma while tuning the reflective power to its minimum. We found that the following process after this stabilization step creates a stable plasma with no reflective power. The recipe of chamber preconditioning is same as the final deposition recipe and is described below:

- Pressure = 1 Torr
- SiH4= 21 SCCM
- N2 = 250 SCCM
- N2O = 179 SCCM

- Top Electrode R.F. Power = 1000W
- Bottom Electrode R.F. Power = 30W
- Temperature = 360C

When the chamber cleaning and preconditioning was completed, the samples were loaded into the reaction chamber for 2 minutes in order to reach thermal equilibrium. A film thickness of 85 Å was obtained for a 12 seconds deposition with a deposition rate of 425 Å/minute.

4.5 Defining the Drain Electrode

The drain electrode is defined by a 200 nm Cr pattern on top of the PECVD silicon dioxide. Same as described in the source electrode section, a second photomask was used for photolithography to define the top Cr pattern. We cleaned the sample in the UV-O_3 cleaner for 30 minutes before the lithography process in order to get rid of any contaminants from the sample handling process. Negative photoresist NR9-1000PY was spun coat on samples with a speed of 2000 rpm for 30 seconds. After 120 seconds of soft bake on the hot plate at 150C, the samples were loaded on the sample holder on the OAI back side aligner. The drain pattern was aligned just above the source electrode using the alignment mark on the photomask. Once the alignment was done, the sample was contacted with mask and exposed to 365 nm UV light for 17 seconds. Post exposure bake was carried out on the 100 C^0 hot plate for 60 seconds immediately after exposure. Samples were then developed in RD6 developer for 17 seconds followed by rinsing with copious amounts of DI water and blown dry with N_2.

The samples were again loaded into the e-beam evaporator (AJA Inc.) for 200 nm Cr layer deposition. The deposition and following lift-off processes were the same as described in “definnition of source electrode” section. As shown in Figure 4.2, the drain and the source electrode are now separated by the PECVD SiO_2 layer.

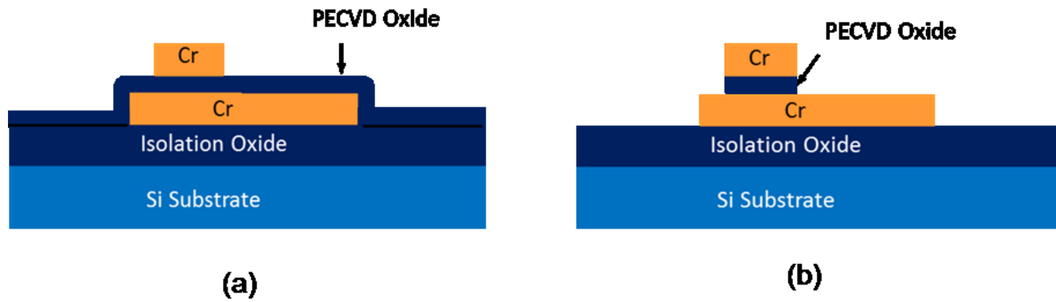

Figure 4.2 PECVD oxide as an isolation layer separates the source and drain electron. (a) The top Cr electrode was deposited on top of the PECVD oxide. (b) RIE etching of the PECVD oxide using Top Cr electrode as mask. The sidewall was created after the RIE etching.

4.6 Sidewall Etching

In order to create a vertical sidewall along the source and drain electrode, samples were dried etched using a reactive ion plasma etcher (Trion Inc.) to vertically etch away the PECVD SiO_2 which is covers the top of the source electrode.

Samples were first cleaned in acetone bath with ultrasonic agitation and then in a UV-O_3 cleaner. 5 minutes of acetone bath with ultrasonic agitation were repeated twice with fresh acetone and beakers used etch time. 30 minutes of UV-O_3 cleaning were then carried out. We usually repeated the Acetone and UV-O_3 cleaning cycles two to three times. This step ensured that the residual photoresist was completely removed from the samples before going to the dry etching chamber.

The etcher reaction chamber was wet cleaned with isopropanol alcohol to physically remove residuals from the previous process. O_2 plasma cleaning process was followed by a wet cleaning process for 5 minutes. Preconditioning of the etcher was carried out for 10 seconds just before the final dry etch process. The same process was used to perform the final etching process and helped to avoid an unstable plasma with high reflective power.

The sample was loaded to reaction chamber and the dry etching process was carried in out in CF_4 which is the reaction gas. The etching recipe is described as below:

- CF_4 flow : 25 sccm
- Process pressure: 20 m Torr
- Top electrode power: 3000 W
- Bottom electrode: 100 W

The drain electrode serves as a hard mask during the process and underneath SiO_2 is etched vertically so that a vertical SiO_2 sidewall along the sidewall of drain electrode is achieved. The source electrode was exposed when the SiO_2 was completely etched away. It served as an etch stop because the Cr is not etched in CF4 (a very slow etch rate compared with the etch rate of SiO_2). We intentionally over etched the SiO_2 so that no residual SiO_2 was left and a 10~20 nm step on source electrode was created. After the dry etching process, the source and drain electrode was separated by a sub-nanometer insulating gap which is controlled by the thickness of SiO_2.

4.7 Attachment of Quantum Dots

Gold nanoparticles with desired size were attached to the sidewall of SiO_2 between the source and drain electrode. In this configuration, the source, nanoparticle and drain are separated by the dielectrics in the scale of sub-nanometer so that the gold nanoparticles serve as a quantum dot in our single electron device.

The attachment of gold particles was achieved by forming a self-assembled monolayer (SAMs) on theSiO_2 surface. A 0.5 mM solution of (3-aminopropyl)triethoxysilane (APTES; $(C_2H_5O)_3$-Si-$(CH_2)_3$-NH_2) was prepared in ethanol alcohol. The sample was then immersed in this solution for 30 minutes in order to form the APTS SAMs on the oxide. An important note is mentioned here ; this wet chemistry process is very sensitive to the surface condition so we always cleaned our samples in UV O3 cleaner for 30 minutes and with Ar plasma sputtering for 5 minutes to get rid of any residuals from previous sidewall etching process. When the APTS SAMs forms, the

oxides surface becomes positively charged in a solution because of the functional groups from APTS SAMs [29, 30]. Samples were rinsed with ethanol and water to get rid of the residual solution after immersion and blown dried by the N_2 stream. Following the APTS SAMs formation, samples were immersed in 10 nm gold colloidal solution for particles attachment. Gold nanoparticles in the colloidal solution are passivated by citrate ions and are negatively charged in the solution. Samples in this solution with oxide surface functionalized by APTS SAMs will attract and attach the nanoparticles due to the opposite charge polarities. The time of the attachment process could vary with the size and concentration of the colloidal solution. For 10 nm the gold particles attachment, the samples were immersed for 8 hours. After removing from the colloidal solution, the samples were rinsed with methanol and water and then blown dried with N_2 stream. We put our samples in the UV-O3 cleaner again to burn off the APTS SAMs after attachment because it might affect the tunneling process since it could create become additional tunnel junctions. Figure 3.1 shows a sidewall attachment of 10 nm gold particles. Note that the attachment could also be randomly on the source/drain electrode but only the particles positioned at the correct distance between two electrodes contributes to the single electron device's operation.

4.8 Passivation

A SiO_2 layer with a thickness of 300~400nm was sputtered on the samples which were attached with particles. This passivation layer was sputtered in a home-build sputtering chamber. Samples were first loaded to the chamber and pumped down to a base pressure less than 1 x 10^{-5} Torr. Ar gas was then released and stabilized at 50 sccm. Plasma was struke at 35 mTorr and stabilized at 10 mT with a RF power at 50 watt. 5 minutes of pre-sputtering with a shutter got rid of the contaminants from the target and stabilized the plasma. After turning the shutter on, the sputtering process ran for 60 minutes and the RF power was turned off for 15 minutes. This prevents over heating of

the samples and sputtering target. For a total sputtering time 7 hours, a 300~400 nm SiO_2 layer was deposited on the samples.

4.9 VIA and Bond Pad Formation

After the passivation SiO_2 was deposited, the source and drain electrodes need to be connected with a bond pad through VIA to perform electrical measurements. Samples were first cleaned in UV-O_3 cleaner 30 minutes to remove any surface contaminants from sample handling. Optical lithography was then applied to the samples to define the VIA. Samples were spun coated with negative photoresist NR9-1000PY at a speed at 2000 rpm. Soft bake at 150 C^0 on a hot plate for 120 seconds was carried out after the resist coating. A third photomask was applied to define and align the VIA structure. Samples were then loaded on the OAI backside aligner and aligned VIA pattern in the position above drain electrode then exposed to UV light for 13 seconds. Post bake at 100 C^0 for 60 seconds was followed immediately after exposure. Samples was finally developed in developer RD6 for 17 seconds followed by a DI water rinse and a blown dry using a N_2 stream. The resist pattern was now opened for VIA and other area was covered and serves as a mask when performing the following dry etch process.

The VIA hole was obtained by dry etching through the passivation SiO_2. DRIE was used for this VIA etching process. Samples were loaded into the reaction chamber with a recipe described as below:

- CF4 flow : 50 sccm
- Process pressure: 25 mTorr
- Top electrode power: 3000 W
- Bottom electrode: 50 W

Samples were dry etched for 300 seconds and 379 nm SiO_2 had been etched away. We stopped the etching because the resist was consumed out at 300 seconds. Samples were cleaned with acetone and repeated with same optical lithography process and the same photomask to put on another fresh resist mask for further dry etch

processing until the source electrode was exposed in VIA. The etching depth of VIA can be measured at the profilometer after removing photoresist. The VIA depth measured on top of the source and drain will be smaller than that on gate when VIA was completely etched through the passivation oxide. This is because the VIA etching stopped on top of source and drain electrode while continuing on gate where the thermal oxide is underneath.

The bond pad was made after the lift-off process for a 200nm Cr layer deposited on top of the passivation oxide. Before the optical lithology defined the bond pad, the samples were cleaned with 2 cycles of combinations of acetone agitation and UV-O_3 exposure in order to get rid of the photoresist residuals from the VIA etching process. In addition, 5 minutes of Ar sputtering was carried out to remove any byproducts formed in the CF_4 chemistry during dry etching which could cause bad contact between the bond pad and source/drain electrode. Optical lithography was applied with the fifth photomask to define the bond pad. Samples were first spin coated with a negative photoresist NR9 1000PY at a speed of 2000 rpm for 30 seconds. A pre-exposure bake was performed at 150 C^0 on a hot plate for 120 seconds. Samples were then aligned and exposed to UV light for 13 seconds on OAI back side aligner using the fifth photomask defining the bond pad. Post bake immediately followed after exposure at 100 C^0 for 60 seconds. Then samples were developed in the developer RD6 for 17 seconds. After developing, the samples were rinsed with water and blown dried by a N_2 stream. Now the bond pad patterns were shown in the samples without photoresist and covered and ready for deposition of Cr.

Cr and Au deposition was carried in AJA e-beam evaporator again with the same process described in “define of source electrode” section. 200 nm Cr and 300 nm Au layers were deposited from this deposition and bond pads were obtained after the lift-off process.

Chapter 5

Electrical Characterization

5.1 Introduction

The electrical characterization of the fabricated single electron device was carried out from a temperature range of 10 K to 295 K. Room temperature measurement was done in the clean room using an Agilent 4155 C semiconductor parameter analyzer. Low temperature measurements were done in the electrical measurement lab using the Agilent 4157 B semiconductor parameter analyzer.

For a detailed scan of a certain voltage range, we used a swept measurement mode in our parameter analyzer. The configuration of this mode is described as follows:

Hole time = 30 seconds

Delay time = 10 seconds

Step delay time = 10 seconds

Integration time = High for Agilent 4155 C; 1000 for Agilent 4157 B.

5.2 Coulomb Staircase Observed from a Double Junction Single Electron Device with 10 nm Au Nanoparticle

A double junction single electron device fabricated with a 10 nm gold nanoparticle as the coulomb island using procedures described in previous chapter was measured for its I-V characteristic using the Agilent 1455 C parameter analyzer. This I-V measurement was carried out at room temperature with swept a source drain bias V_{DS} from -200 mV to 200 mV. Each data point has a step size of 4 mV. The holding time before collecting each data point was 5 seconds to stabilize the measurement. The recorded current-voltage curve was shown in Figure 5.1 [31].

A clear coulomb staircase and coulomb blockade was observed in this device at room temperature. These decisive features prove that our device is working as a single electron device at room temperature.

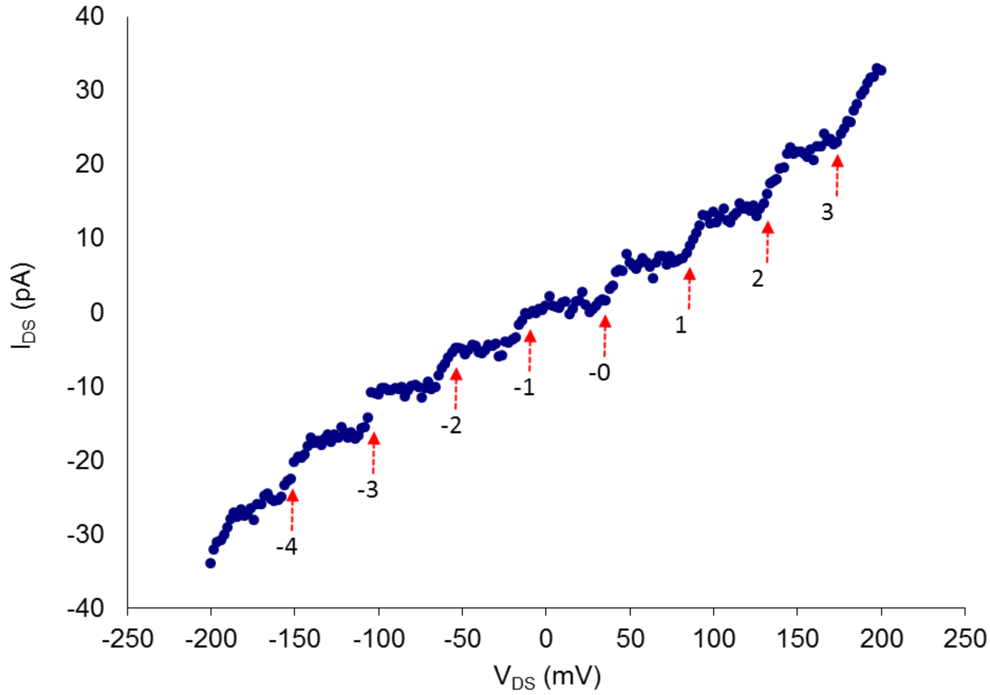

Figure 5.1 [31] I-V Characteristic for double junction single electron device using 10 nm gold as Coulomb island. Coulomb blockade and Coulomb staircase was observed in this device at room temperature. The red arrows indicate the source-drain bias at which there is an abrupt change in current.

Each sharp change of the current was indicated by the red arrow in the IV curve for clarity. The width between the two adjacent arrows was carefully measured and recorded in Table 5.1. One can see that the voltage interval ΔV_{DS} between arrows is highly periodic as shown in Figure 5.2. It indicates that the single electron transport in our device is through a single particle.

The step width of the coulomb blockade represents the energy of adding or removing an electron from or to the Coulomb Island. We calculated the average step width from the voltage intervals ΔV_{DS} between the arrows. The average ΔV_{DS} is 46 ± 3 mV. Compared to this with the thermal energy at room temperature (~25 mV), it is about two times larger. This permits the observation of the Coulomb blockade and Coulomb staircase without smearing out by temperature.

Table 5.1 Voltage interval ΔV_{DS} between the indicated arrows in Figure 5.1

Arrow Index	Marked position (mV)	Voltage Interval (mV)
-4	-150	–
-3	-104	46
-2	-54	50
-1	-12	42
0	36	48
1	82	46
2	130	48
3	174	44

Since the capacitance of the device can be obtained from the step width ΔV_{DS} of the coulomb blockade accoriding to the orthodox theory, one can obtain the C_s and C_D from the following equation:

$$\Delta V_{DS} = {}^{e}/_{\max(C_S, C_D)} \tag{5.1}$$

where C_S and C_D are the capacitance of the source junction and drain junction. This gives the $\max(C_S, C_D)$ as $3.5 \pm 0.2\, aF$. Compared to the self-capacitance for a 10 nm gold particle embedded in silicon oxide with dielectric constant $\varepsilon_r = 4$, it is within a reasonable agreement. The self-capacitance C_{self} considered here is 2.2 aF and is obtained from:

$$C_{self} = 4\pi\varepsilon_0\varepsilon_r r \tag{5.2}$$

where ε_0, ε_r and r are vacuum permittivity, dielectric constant of the souring medium and the particle radius, respectively.

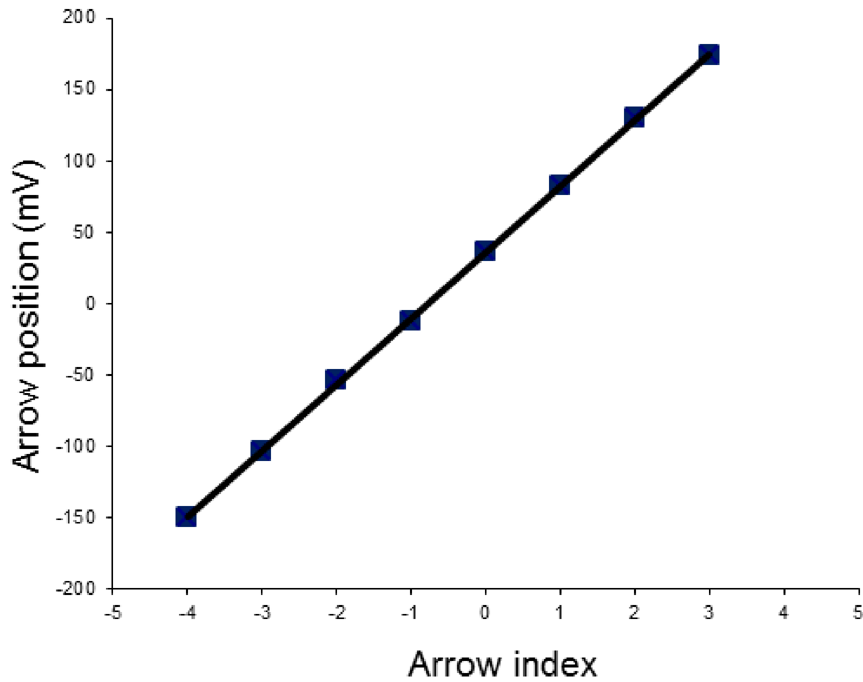

Figure 5.2 Plot of Data points marked by a red arrow in Figure 5.1. Each data point represents a sharp change in current. Data points are separated by an average voltage of 46 mV with a standard deviation of 3 mV. This ΔV_{DS} represents the step size of the coulomb staircase and is found to be highly periodic for the whole range of the voltage scanned in the measurement.

5.3 Coulomb blockade observed from double junction single electron device with 10 nm Au nanoparticle

A clear coulomb blockade without coulomb staircase was observed from the I-V measurement of this device at a temperature of 10K. The coulomb blockade was observed as a flat current area at bias range near zero as shown in Figure 5.3 [31]. The coulomb staircase was not found in this device with increasing or decreasing applied source-drain bias beyond the coulomb blockade indicating that this device has symmetrical tunnel junctions such as $C_S R_S \approx C_D R_D$.

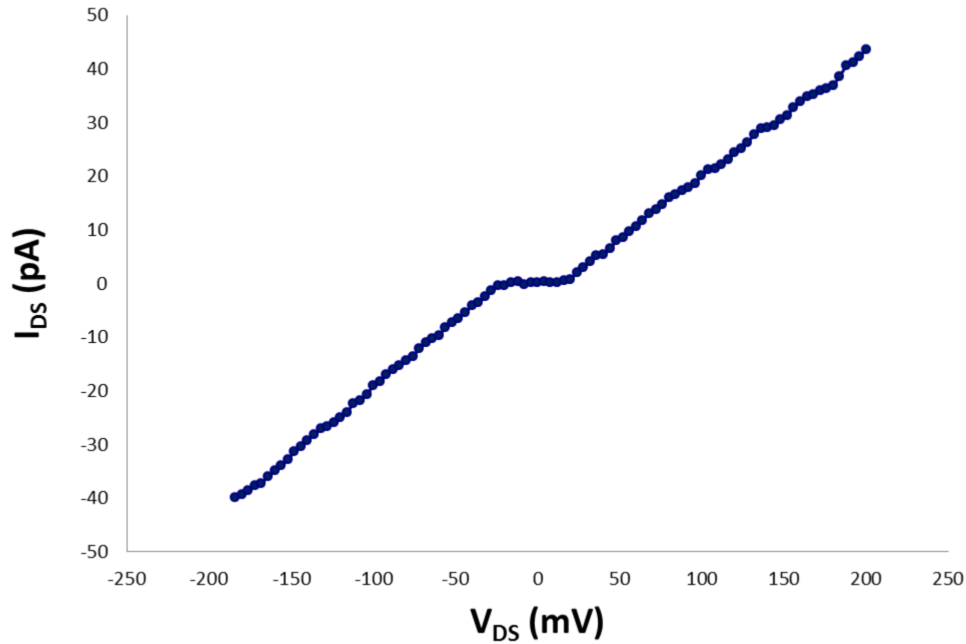

Figure 5.3 [31] I-V Characteristic for double junction single electron device using 10 nm gold as a Coulomb island. The coulomb blockade at a temperature of 10K was observed from this device.

The value of $C_S R_S$ and $C_D R_D$ governs the rate of the electron that tunnels in or out of the coulomb island. The height of the coulomb staircase in the device with asymmetrical tunnel junctions($C_S R_S \gg C_D R_D$ or $C_S R_S \ll C_D R_D$) results form one of the tunnel junctions having a smaller rate which prevents the electron from tunneling out thus the coulomb island remains in a charged state. This charged island blocks the subsequent incoming electron while even increasing the source drain bias. As a result, the step like structure is shown in the bias region beyond the coulomb blockade. In the case of symmetric tunnel junctions, the rate is the same for the electron to tunnel in or out of the Coulomb island. Once the electron tunnesl in, it will immediately tunnel out thus the Coulomb island remains in an uncharged state and no coulomb blockade occurs beyond the zero bias region.

The values of $C_S R_S$ and $C_D R_D$ were determined when the tunnel junctions were formed during fabrication of the single electron device. In this case, the tunnel junctions were formed in between the source or drain electrode and the gold nanoparticle. Depending on the position that the gold nanoparticle attached to the silicon oxide, the two junctions can be either symmetric or asymmetric. Since the attachment of gold is random, there is a higher chance to have device with asymmetric junctions. It is possible however, it is possible to have a device with symmetric tunnel junctions if the nanoparticle is positioned in the middle so that the tunneling distance from the gold nanoparticle to the source electrode is the same as it is to drain electrode.

5.4 Coulomb Oscillation Observed from the Double Junction Single Electron Transistor with 10 nm Au Nanoparticle

A coulomb oscillation was observed from the IV measurement of the single electron transistor at room temperature. This single electron transistor was fabricated by the same fabrication process as the single electron device discussed above. The Coulomb island in this device was made by a 10 nm gold particle. The only difference in the device structure is that a gate was embedded into the device thus a gate operation is available.

Figure 5.4 [31] shows the plot of the source drain current I_{DS} verse gate bias V_G at a constant source drain bias $V_{DS} = 10\ mV$. Gate bias was swept from -350 mV to 350 mV. It is clear that the periodical Coulomb peaks show up with the swept gate bias. The average separation of these peaks is 205 mV. This corresponds to the energy required to add or subtract one electron to or from the coulomb island. The conductance of the device oscillated with the gate bias is another signature of the single electron transport in our fabricated device.

To have a better understanding of this conduction oscillation in our single electron transistor, one can compare this with the IV plot from a single electron device which demonstrates a Coulomb blockade and a Coulomb staircase discussed in the

previous section. For an applied source drain bias at 10 mV, it can be seen that these devices

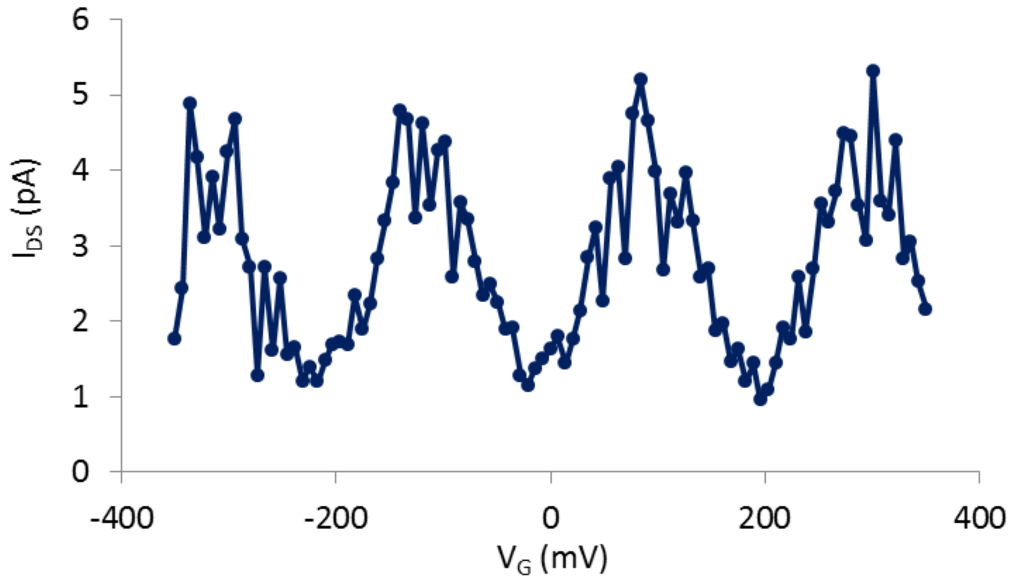

Figure 5.4 [31] I-V Characteristic for double junction single electron device using 10 nm gold as Coulomb island. Coulomb oscillation at room temperature was observed from this device with 10 nm GNP. Source drain bias was kept at 10 mV with sweeping gate bias from -350mV to 350mV.

were under the region of the coulomb blockade since the width of coulomb blockade ΔV_{DS} is ~50 mV. However, with the applied gate bias to the single electron transistor, the chemical potential of the Coulomb island is shifted corresponding to this gate bias. In the case of a positive gate bias application, the chemical potential of the island keeps dropping with an increasing gate bias V_G. Before it aligned with the Fermi level of source or drain electrode, the device was still under the Coulomb blockade regime. Eventually as the two energy levels of electrode and island were aligned, tunneling to Coulomb island was allowed. The conductance of the device is no longer zero at this gate bias and a conductance peak shows up in the IV plot at this gate bias. With further increases of the

gate bias, the device goes into the Coulomb blockade regime again since the chemical potential with the excess electron is not aligned with the source or drain electrode again. This is the bottom region between the two adjacent peaks.

Two Coulomb staircases obtained from a single electron transistor with and without gate bias are shown in Figure 5.5 [31]. The shifting of the coulomb staircase due to the applied gate bias is clearly demonstrated.

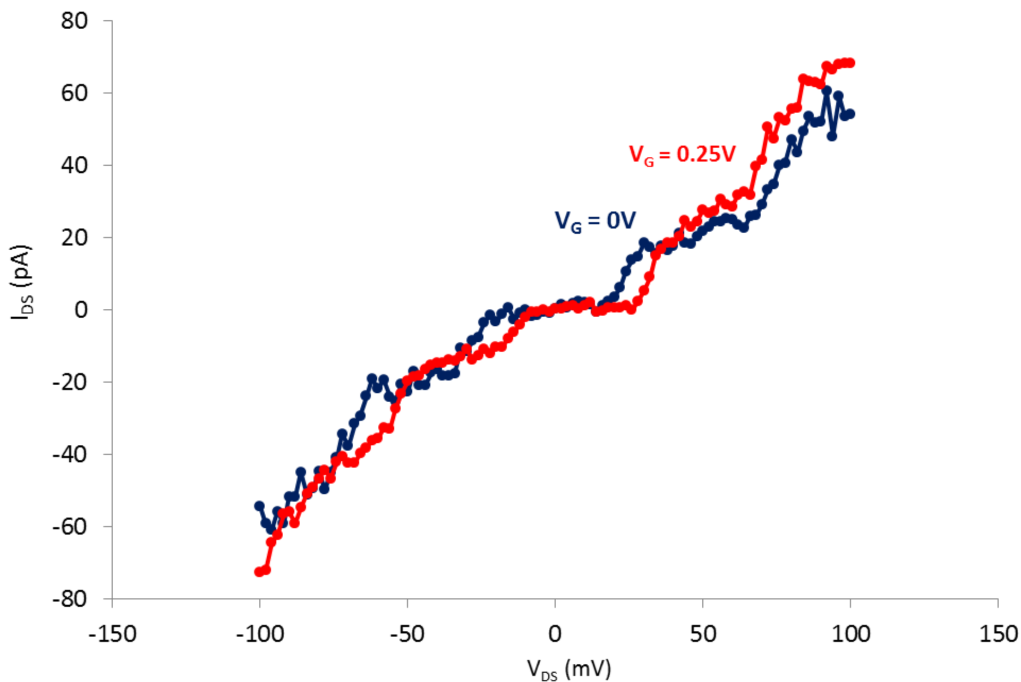

Figure 5.5 [31] Coulomb staircase shifting with gate bias applied. Source drain bias was swept from -100mV to 100mV with gate bias $V_G = 0$ and $V_G = 0.25$, respectively.

The single electron transistor was cooled down to a temperature of 10K then a source-drain bias was swept from -100 mV to 100 mV with an increment of 2 mV. The blue curve represents this device under gate bias $V_G = 0$ and the red curve represents the device under a constant gate bias $V_G = 250\, mV$. When the gate bias is applied, the

whole curve shifts to the right without any other changes. This shifting is a result of the change of chemical potential of the Coulomb island with the applied gate bias. The source and drain chemical potential now need to be aligned with the changed island chemical potential as the requirement for a tunneling to occur, thus the whole regime of coulomb blockade and Coulomb staircase are shifted with this gate bias. This provides the capability for the device operating at either regular conductance or suppressed conductance (Coulomb blockade regime) under a specified gate bias similar the a regular transistor.

5.5 Coulomb Staircase Observed from a Double Junction Single Electron Device with 20 nm Au Nanoparticle

A clear coulomb staircase and coulomb blockade obtained from a single electron device fabricated with 20 nm gold nanoparticle as the coulomb island is shown in Figure 5.6 [31]. This device was fabricated with the same procedure as all other devices with 10 nm gold nanoparticle shown in the previous section. The only differences are the size of the gold nanoparticle and the thickness of the silicon oxide.

The resulting IV characteristic of Coulomb blockade and Coulomb staircase verified the fact that the observed single-electron phenomena in our device originated from the nanoparticles and not from any contamination which can occur from the fabrication process. The width of the coulomb blockade ΔV_{DS} is obtained as $20 \pm 2\ mV$ for this 20 nm gold nanoparticle device. This value is about half of the ΔV_{DS} obtained from 10 nm gold nanoparticle device which has the average width of Coulomb blockade $\Delta V_{DS} = 46 \pm 3\ mV$. From equation (5.1), $\max(C_S, C_D)$ is $8.0 \pm 0.7\ aF$ based on ΔV_{DS} for 20 nm gold device, which is about twice that for the device of 10 nm gold device ($3.5 \pm 0.2\ aF$). This is reasonable if we consider the self-capacitance C_{self} is proportional to the radius r in equation (5.2)

The width of Coulomb blockade ΔV_{DS} is observed to have proportionality with the size (radius) of the nanoparticle. This confirms that the nanoparticles between the source

and drain electrode determined the regime of coulomb blockade and coulomb staircase, not possible contaminants from the fabrication process.

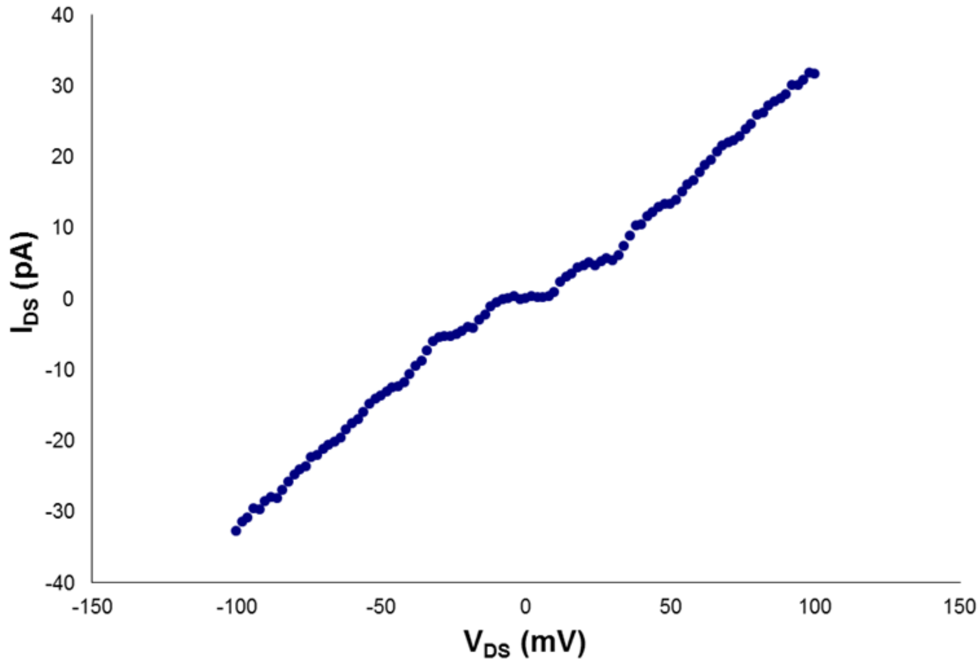

Figure 5.6 [31] I-V Characteristic for the double junction single electron device using 20 nm gold as the Coulomb island. Coulomb blockade and Coulomb staircase was observed a temperature 10K for this device.

5.6 Temperature Effect

When temperature increases, electrons can be thermally excited to a higher energy state. Electron energy therefore has a relationship with temperature described by the Fermi-Dirac distribution. For single electron devices, thermal energy can cause critical problems and prohibit operation in a very low temperature range. In this section, we observe the change of the IV character with varied temperature and compare our experiment data with the calculations based on orthodox theory.

5.6.1 Coulomb Oscillations Observed at a Temperature Variance of 10K to 295K

We fabricated a single electron transistor device with a 10 nm gold nanoparticle and evaluated the IV characteristic at a temperature range from 10 K to 295 K (room temperature). The IV measurements were done at 10 K, 100 K, 200 K, and 295 K in order to compare the effects of temperature on our single electron device. To observe the Coulomb oscillation, a constant 10 mV source drain bias V_{DS} was applied and the gate bias V_G was swept from -450 mV to 450 mV. The measured I-V characteristics were placed in one plot for ease of comparison. Above a temperature of 10 K, each I-V shifted 15 pA for clarity.

The Coulomb oscillation and Coulomb staircase were clearly observed within the entire temperature range. In Figure 5.7 (experimental data from Vishva Ray), clear Coulomb oscillations were observed for the entire temperatures range.

It can be seen that the oscillation peaks broaden with increasing temperatures. This is because with an increase in temperature, more electrons were thermally excited, having sufficient energy to take part in tunneling while. The same cannot be observed at a lower temperature. As a result of the contribution of tunneling from these thermally excited electrons, the Coulomb blockade regime was suppressed. Therefore an earlier onset a and delayed end of the Coulomb oscillation peaks were observed at higher temperatures.

5.6.2 Coulomb Staircases Observed at a Temperature Variance of 10K to 295K

We also measured this single electron transistor device without applying gate bias. Under the source drain bias swept from -150 mV to 150 mV without applying gate bias, clear Coulomb staircases were observed in this device at a temperature range from 10 K to 295K. Four IV characteristics of Coulomb staircase were plotted in the same manner as the Coulomb oscillations discussed above for ease of comparison.

Similar to the observation of coulomb oscillation with varied temperature, we found that the coulomb blockade regime was smeared out with temperature increased.

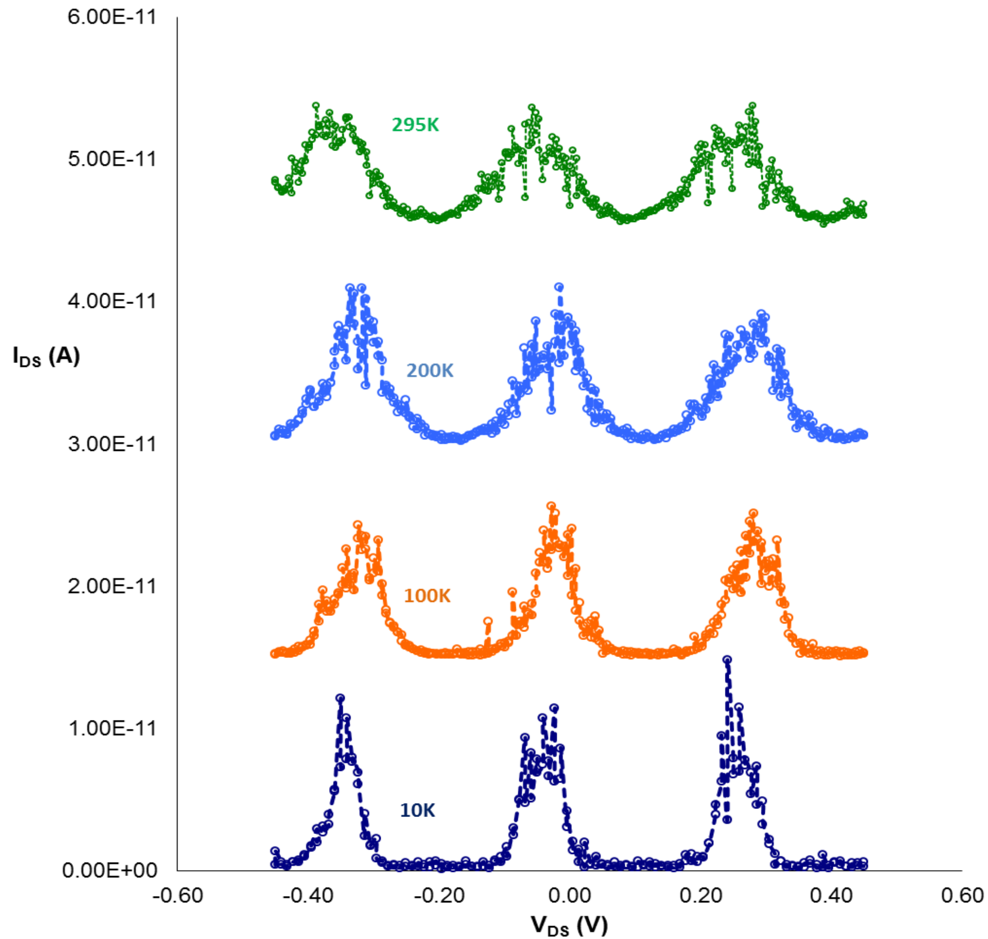

Figure 5.7 IV characteristics for a single electron transistor device using a 10 nm gold nanoparticle as a Coulomb island at various temperatures ranging from 10 K to 295 K (experimental data from Vishva Ray). Gate bias was swept from -450 mV to 450 mV with a constant source-drain bias V_{DS} at 100 mV.

This is also resulted from the thermally excited electrons that have a higher energy and start tunneling before the onset bias been reached.

Comparing the I-V characteristic at 10 K and 259 K in Figure 5.8 (Vishva *et* al), one can see that the abrupt current drop or increase around the onset bias (V_{DS}~-0.5V) has a broadened current step at 295 K compared with that at 10 K. The slope of the current at higher temperature is smaller compared to that at lower temperature. This onset current broadening or current slope decreasing results from a thermal excited

electron tunneling when energy levels between source or drain electrode are not perfectly aligned. For the ideal case when temperature is at 0 K, there is no onset current broadening and the slope of current (dI/dV) is infinite. Therefore this broadening indicates the extent of Fermi Dirac thermal excitation which is directly related to temperature.

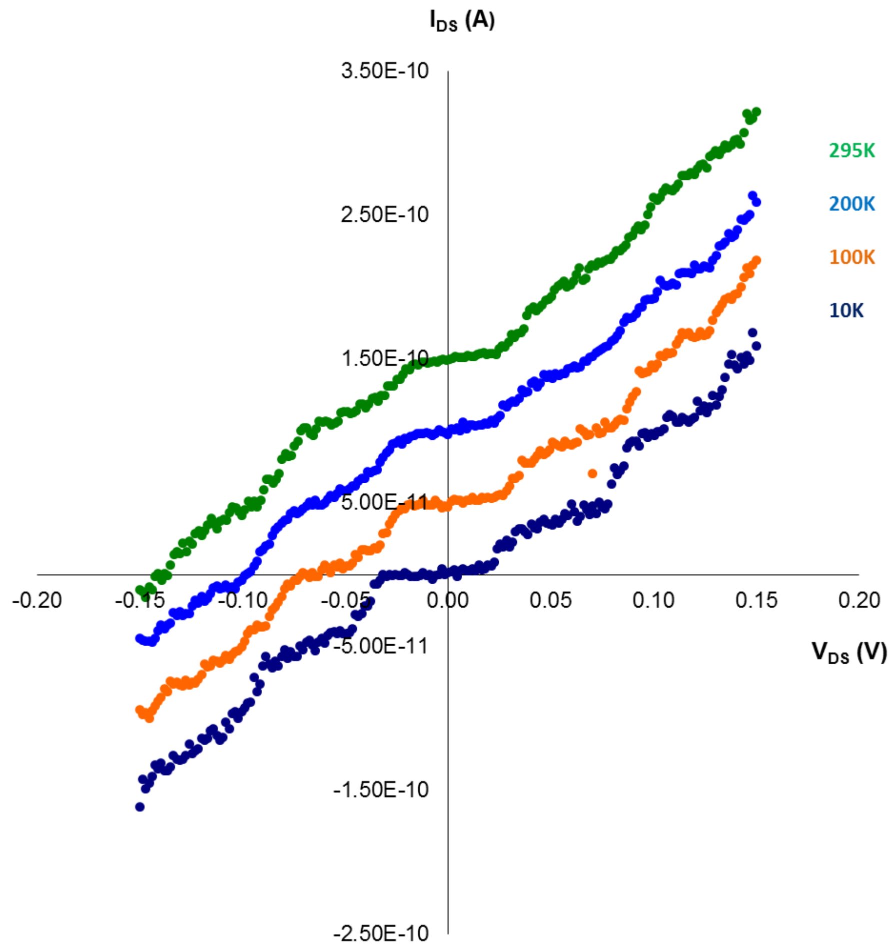

Figure 5.8 IV characteristics for a single electron transistor device using a 10 nm gold nanoparticle as Coulomb island (experimental data from Vishva Ray). The Coulomb staircase at various temperatures was obtained. Above 10K, all plots are shifted up by 75 pA for clarity.

5.6.3 Theoretical Calculations of IV Characteristic at Various Temperatures

In order to evaluate our obtained IV characteristic, a calculation of I-V characteristic is carried out based on orthodox theory with the model of our single electron transistor. The temperature of this calculation is the same as the temperature that we measured in our device. The plot of calculated IV characteristic was generated by the simulator SIMON 2.0

In Figure 5.9 (Pradeep Bhadrachalam *et al.*), four simulated I-V's of our single electron transistor with a gate bias swept at a range the same as in Figure 5.7 are plotted in a range of temperature from 10 K to 295 K. The arrangement of the IV curve is also same as in Figure 5.7.

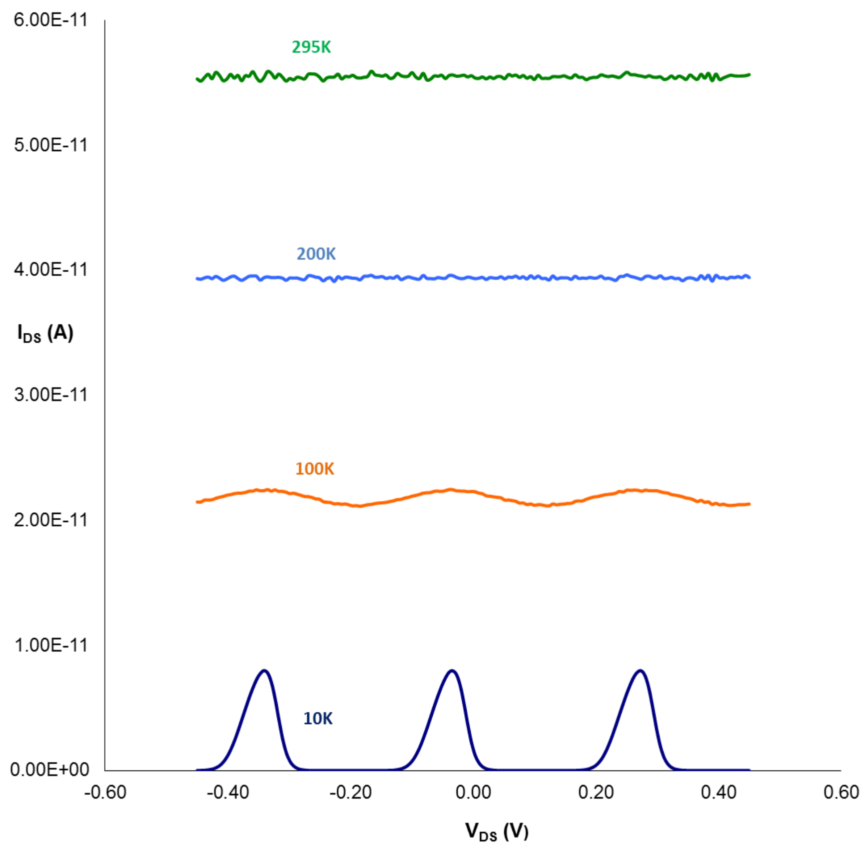

Figure 5.9 Simulated IV characteristics at various temperatures (Pradeep Bhadrachalam *et al.*). Above 10K, all plots are shifted up by 75 pA for clarity.

As the temperature increased, it is clear that the Coulomb oscillation peaks were smeared out by increased temperature. Even at 100 K, we can barely see the oscillation peaks. One can observe that the Fermi Dirac thermal smearing effect is much more pronounced in these calculated IVs. We will compare this with an obtained IV from our device and explain the reasoning in a later section.

In Figure 5.10 (Pradeep Bhadrachalam *et al.*), the calculated IVs for our single electron transistor device were illustrated at a temperature range from 10 K to 295K. The Coulomb staircase can be only obtained at 10K. Similar to the case of Coulomb oscillation, Coulomb staircases were thermally smeared out and the smearing effect is much stronger compared to what we obtained from our device.

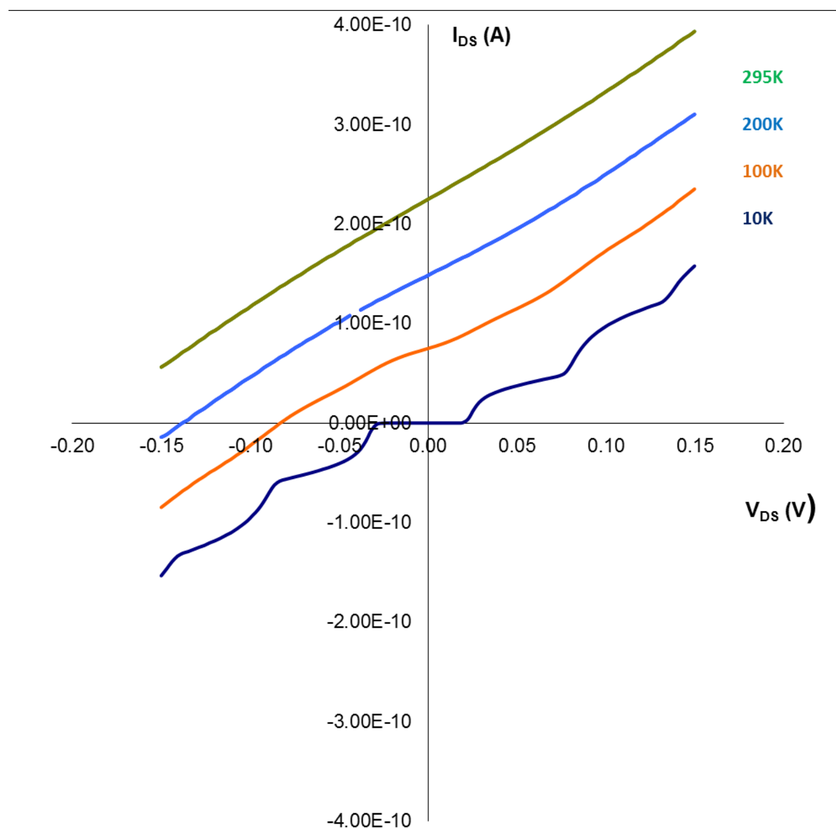

Figure 5.10 IV characteristics at various temperatures for a single electron transistor with a 10 nm gold nanoparticle (Pradeep Bhadrachalam *et al.*). Above 10K, all plots are shifted up by 75 pA for clarity.

When we compared our measured IV with the calculated one, we found that they were matched very well at 10 K. However, they didn't match when the temperature was increased above 10K. The deviation from the mismatch also increased with the change in temperature since the temperature dependency of the IV obtained from our measurement was not as strong as we observed from the calculated IV.

At a temperature of 10 K, we compared the obtained (experimental data from Vishva Ray) and calculated IV characteristic of the Coulomb oscillation in Figure 5.7 and Figure 5.9 and illustrated them in Figure 5.11 It can be seen that two IV characteristics are matched well which indicate that at this temperature, the behavior of the single electron transport in our device is well described by the orthodox theory.

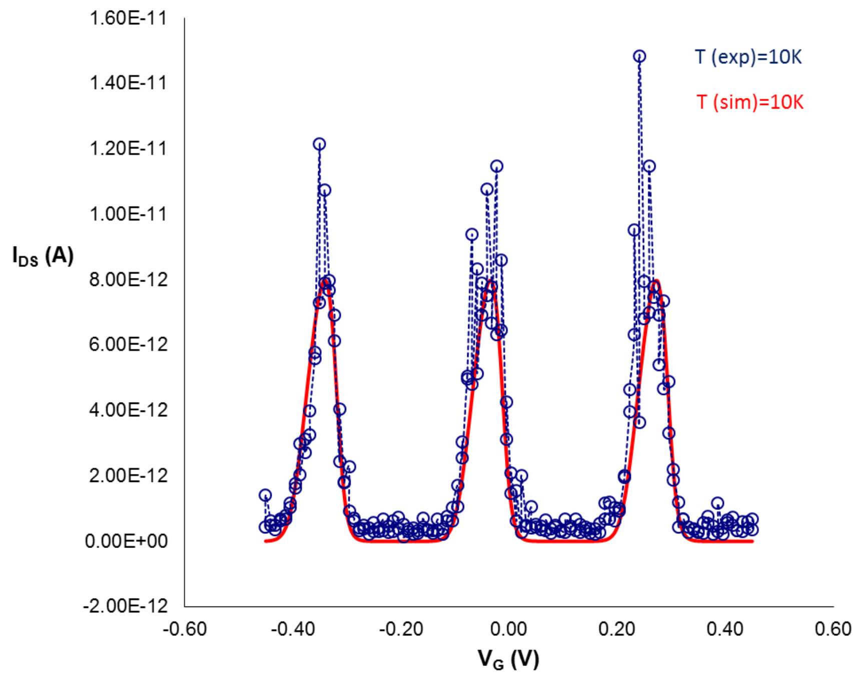

Figure 5.11 IV characteristic of a Coulomb oscillation obtained at 10 K. (experimental data from Vishva Ray). The effective temperature of the cold electron at 10 K was used in orthodox theory calculation

Similarly, we also compared the obtained (experimental data from Vishva Ray) and calculated IV characteristic of Coulomb staircase in Figure 5.7 and Figure 5.9 at 10 K and illustrated them in Figure 5.12. The experimental and theoretical data matched perfectly.

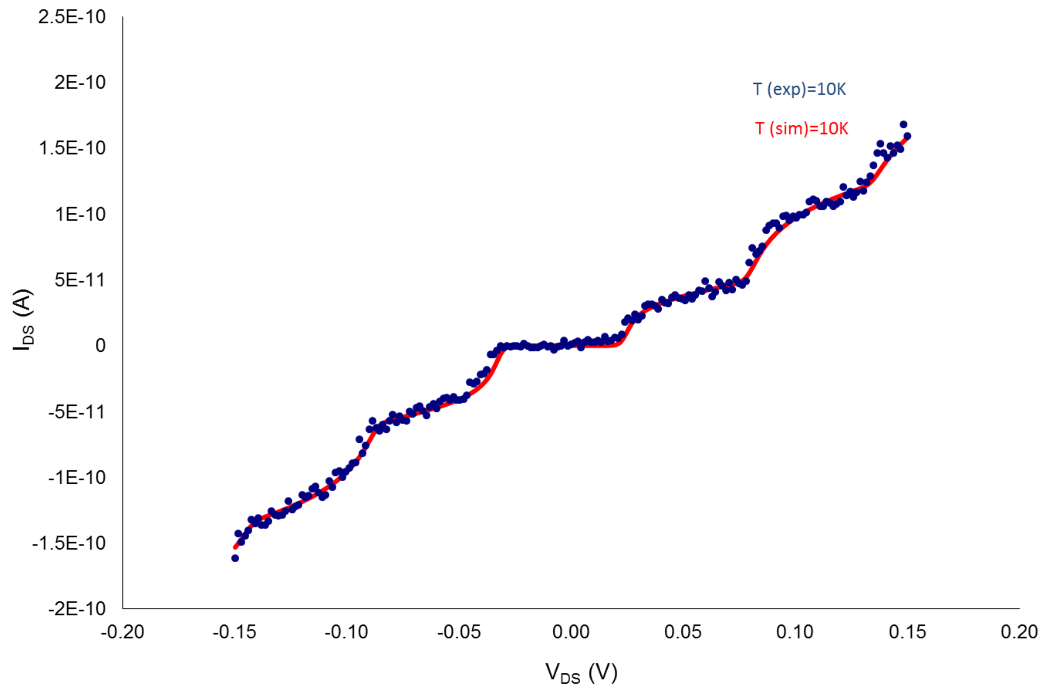

Figure 5.12 IV characteristic of a Coulomb staircase obtained at 10 K (experimental data from Vishva Ray). The effective temperature of the cold electron at 45 K was used in the orthodox theory calculation.

Chapter 6

Energy Filtering

6.1 Energy Filtering Effect in Single Electron Transistor

As the temperature increased above 10 K, the calculated IV is no longer matches the IV obtained from our measurement. The difference came from the fact that Fermi Dirac thermal excitation has a minor effect on the behavior of our fabricated single electron transistor. The main cause of this suppressed Fermi Dirac thermal excitation originated from the formation of the quantum well in the tunnel junctions that serve as an energy filter of electron.

As shown in Figure 6.1(a), when a source-drain bias is applied, the Fermi level μ_L of the source electrode will be raised. As long as it aligned with the energy level ε_D of the quantum dot (QD), electrons can tunnel from the source to the QD, resulting in a current onset in the I-V characteristics. Thermally excited electrons in the source electrode, however, can have higher energy and begin tunneling even if the μ_L of the source electrode is below ε_D.. The resulting current onset is not as shown in the bottom in Figure 6.1 (a).

Now the situation will be totally different when an electron is going to be transferred in the device with an energy filter as shown in Figure 1 (b). A quantum well is inserted between the source and the tunneling barrier as shown in Figure 1 (b). When the electron is tunneled from the quantum well energy level ε_W to the QD energy level ε_D, it can only occur when ε_D is aligned with or below than ε_W. For the case of ε_D is higher than ε_W, electron cannot be tunneled (except for the phonon absorption that can occur when the energy level offset is small, which we will discuss later) since it doesn't have sufficient energy. The resulting current onset therefore has an abrupt change as shown in the bottom of Figure 1 (b). This is the energy filtering effect.

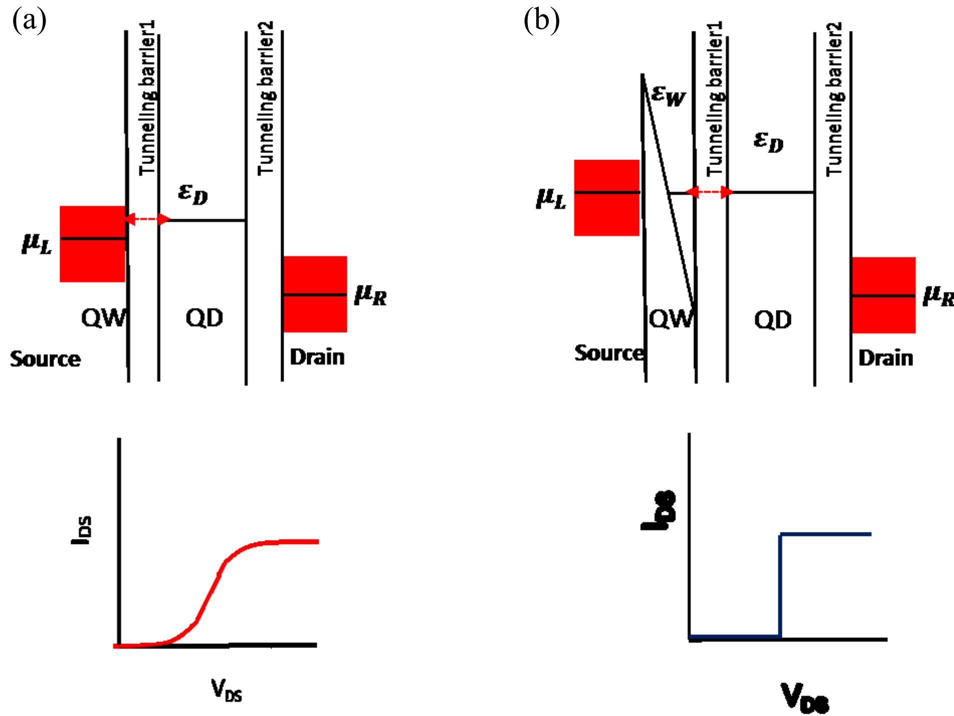

Figure 6.1 Schematic of the electron energy filtering effect in a double junction single electron device. (a) Without energy filtering. (b) With energy filtering.

Thermally excited electrons can be filtered out to obtain only the cool electrons by utilizing discreet energy levels of quantum dots or a quantum well [32-35]. If the electrons are forced to transport through a quantum dot with discreet energy levels, only electrons which are in the energy level aligned with the discreet levels in quantum dot will be transported. Therefore the quantum dot or quantum well serves as the energy filter to allow the transport of electrons which have a specified energy. Such energy filtering behavior has been demonstrated experimentally in a double quantum system [36-38]. Similarly, energy-selective tunneling has also been demonstrated by utilizing the discreet energy level of a quantum dot [32-35]. From previous studies and demonstrations we know that Fermi Dirac thermal excitation can be suppressed through the energy filtering

and we are utilizing this energy filter in our fabricated device to evaluate the effect of cold electron filtering by the measured IV characteristics at a various range of temperatures.

6.1.1 The Structure for Electron Energy Filtering

We created an energy filtering structure in our double-barrier tunneling junction (DBTJ) single electron transistor by forming a quantum well in the tunneling junctions. A layer of native chromium oxide (Cr_2O_3) is formed spontaneously when we fabricated the source and drain electrode using Cr. As shown in Figure 6.2, a quantum well was created because the interface dipoles that formed in the interface of Cr_2O_3/SiO_2 layer [39-42] induce a band bending Cr_2O_3 conduction bend [43-47]. Electrons transport from source to the gold nanoparticle is therefore via tunneling through the tunnel junctions including the quantum well structure. The modeling of electron transport in this single electron transistor device will be discussed in detail in latter section.

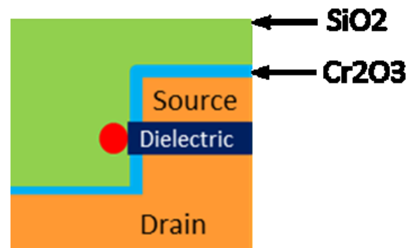

Figure 6.2 Structure of cold electron filtering. A quantum well is formed on the interface of Cr_2O_3/SiO_2.

6.1.2 Effectiveness of Electron Energy Filtering

Calculation of the I-V characteristics based on the model of cold electron filtering was carried out by Pradeep *et al*. at different temperatures. This calculation demonstrated the suppression of Fermi Dirac thermal excitation for a single electron device using semiconducting nanoparticle as the coulomb island. The calculated onset I-Vs and dI/dV are in a very good match with the data from measurement of the device over the temperature range investigated.

The model of cold electron filtering explained that the observed Coulomb oscillation and Coulomb staircase from our single electron transistor at room temperature is due to the transport of cold electrons in our device. The temperature of the energy filtered electron (effective temperature) which takes part of the tunneling is much lower than the operation temperature (reservoir temperature) of the device .We can obtain the effective temperature by comparing the obtained IV from our device with those resulted from Fermi-Dirac smearing.

The IV characteristic obtained at various temperatures from Figure 5.7 and 5.8 were now compared with the simulated IV using the effective temperature. The results were shown in Figure 6.3 to Figure 6.8. For the reservoir temperature at 295 K, 200K, and 100 K, the effective temperature were found to be 45 K, 30 K, 15K, respectively. This result shows that our device can have the cold electron with effective temperature as low as 45 K transporting in our device at room temperature without any physical cooling.

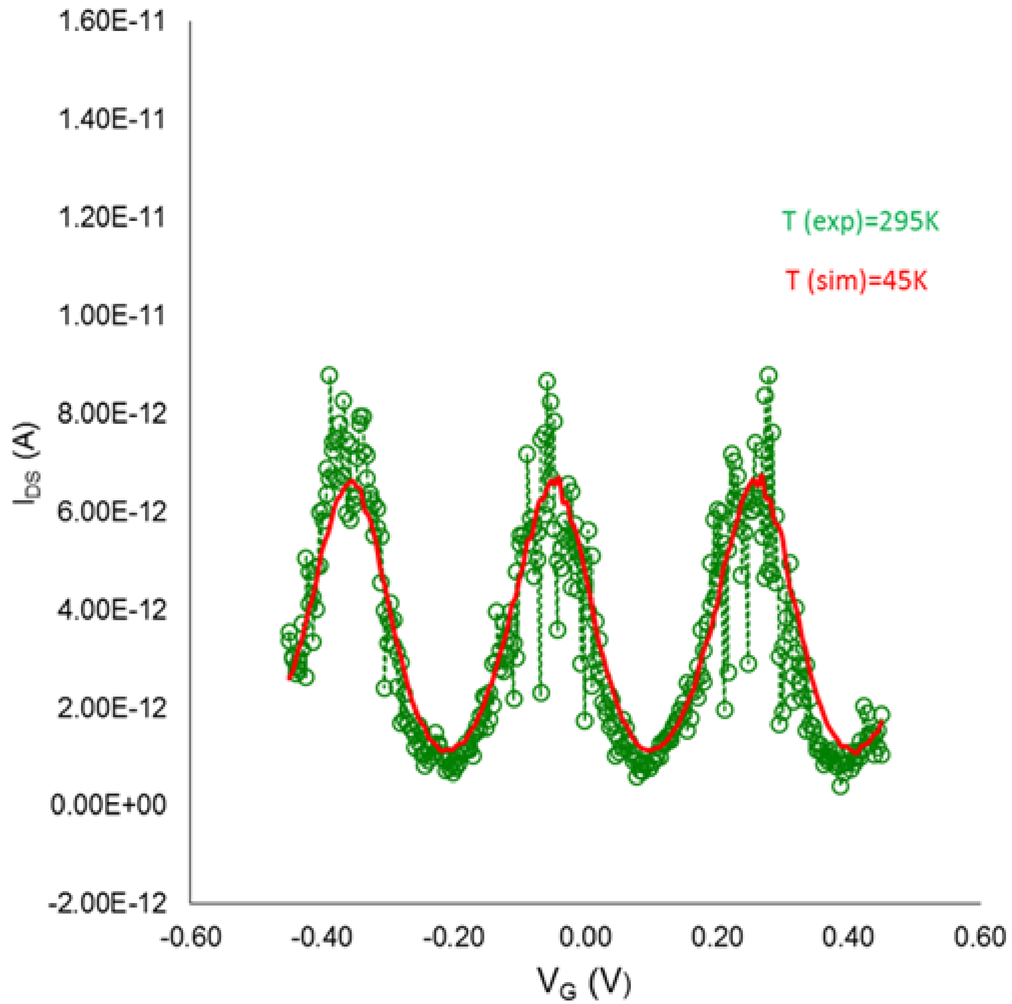

Figure 6.3 IV characteristic of Coulomb oscillation obtained at 295 K (experimental data from Vishva Ray). The effective temperature of the cold electron 45 K were used in orthodox theory calculation.

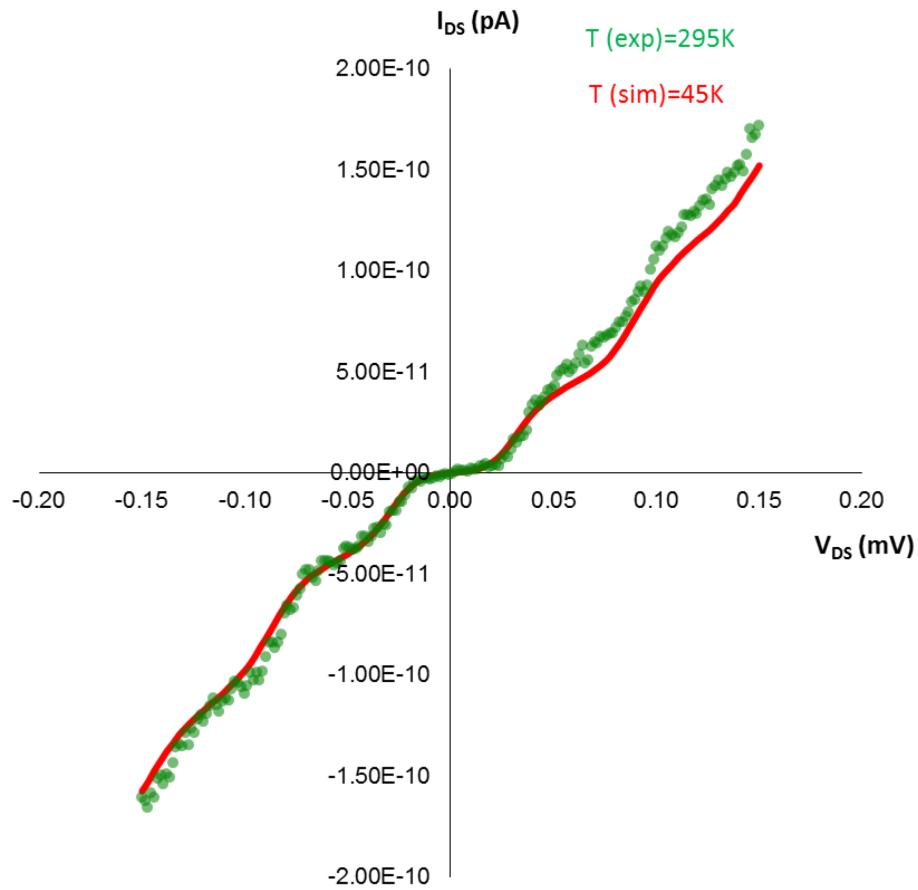

Figure 6.4 IV characteristic of Coulomb staircase obtained at 295 K (experimental data from Vishva Ray). The effective temperature of the cold electron 45 K was used in orthodox theory calculation.

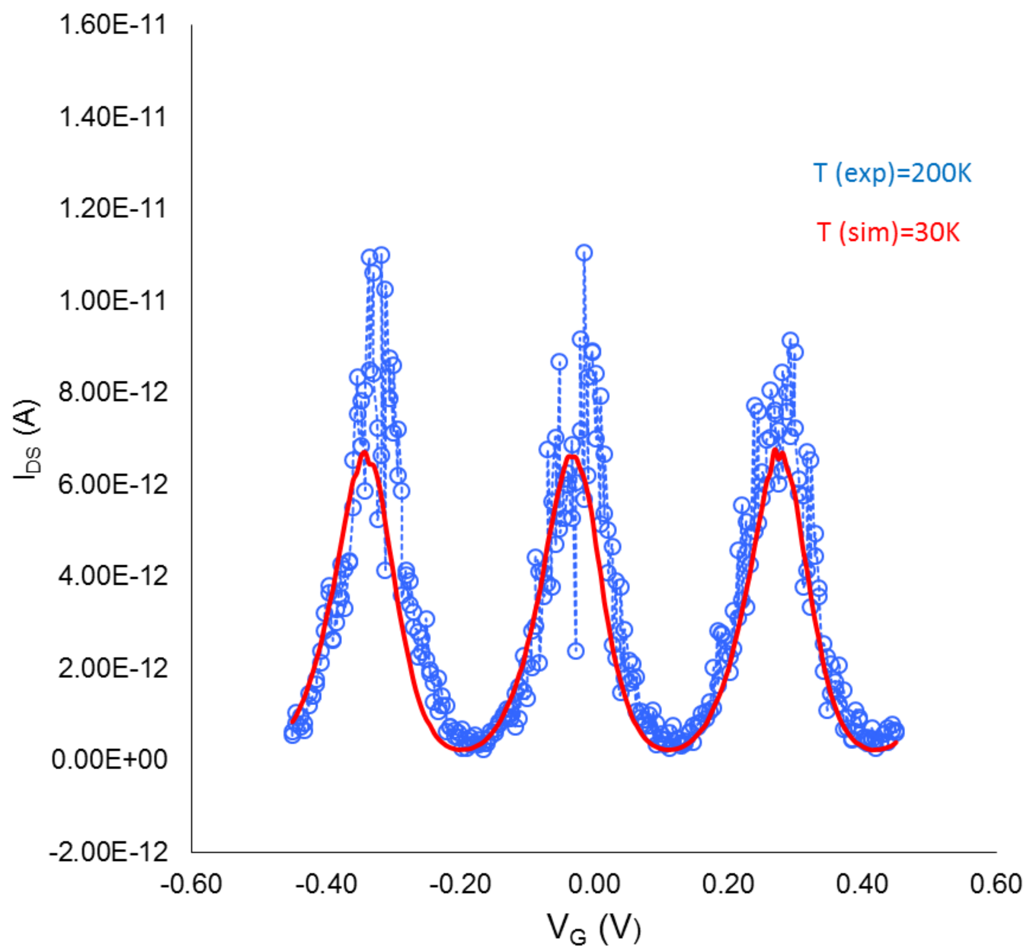

Figure 6.5 IV characteristic of Coulomb oscillation obtained at 200 K (experimental data from Vishva Ray). The effective temperature of the cold electron 30 K were used in orthodox theory calculation

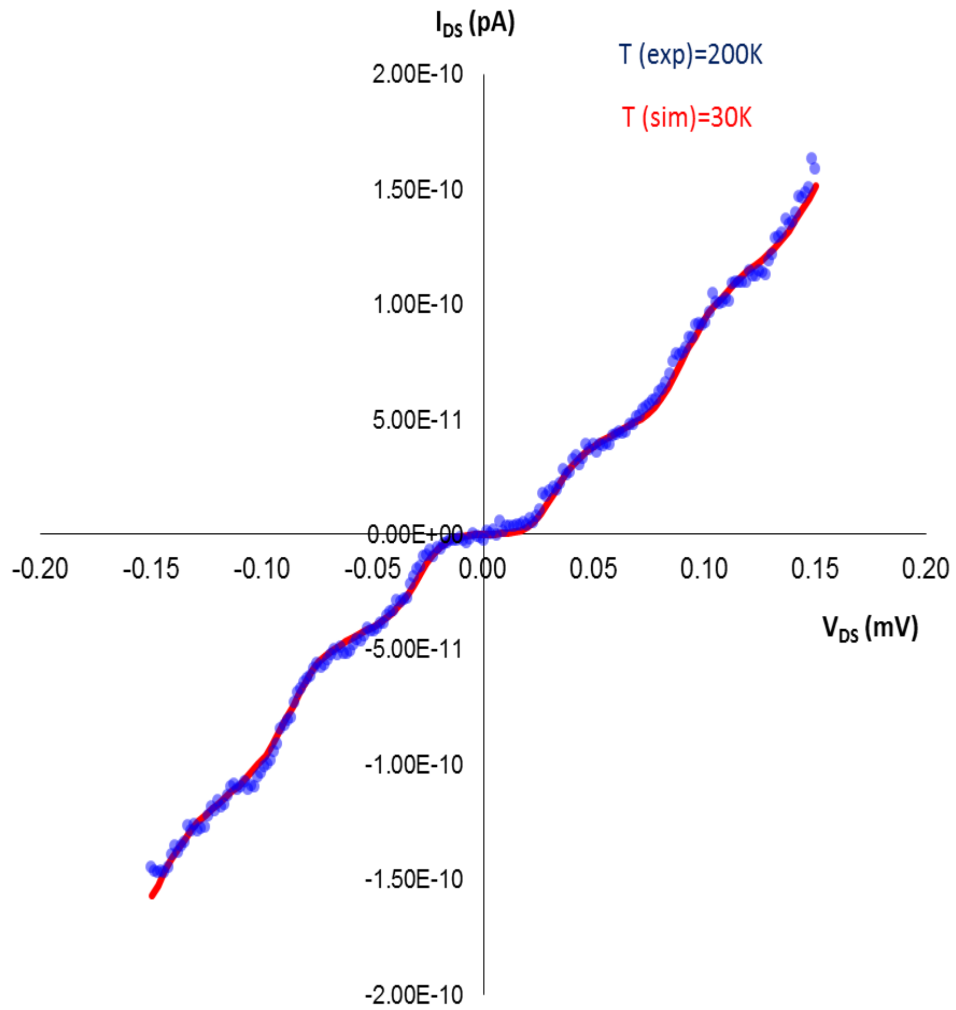

Figure 6.6 IV characteristic of Coulomb staircase obtained at 200 K (experimental data from Vishva Ray). The effective temperature of the cold electron 30 K was used in orthodox theory calculation

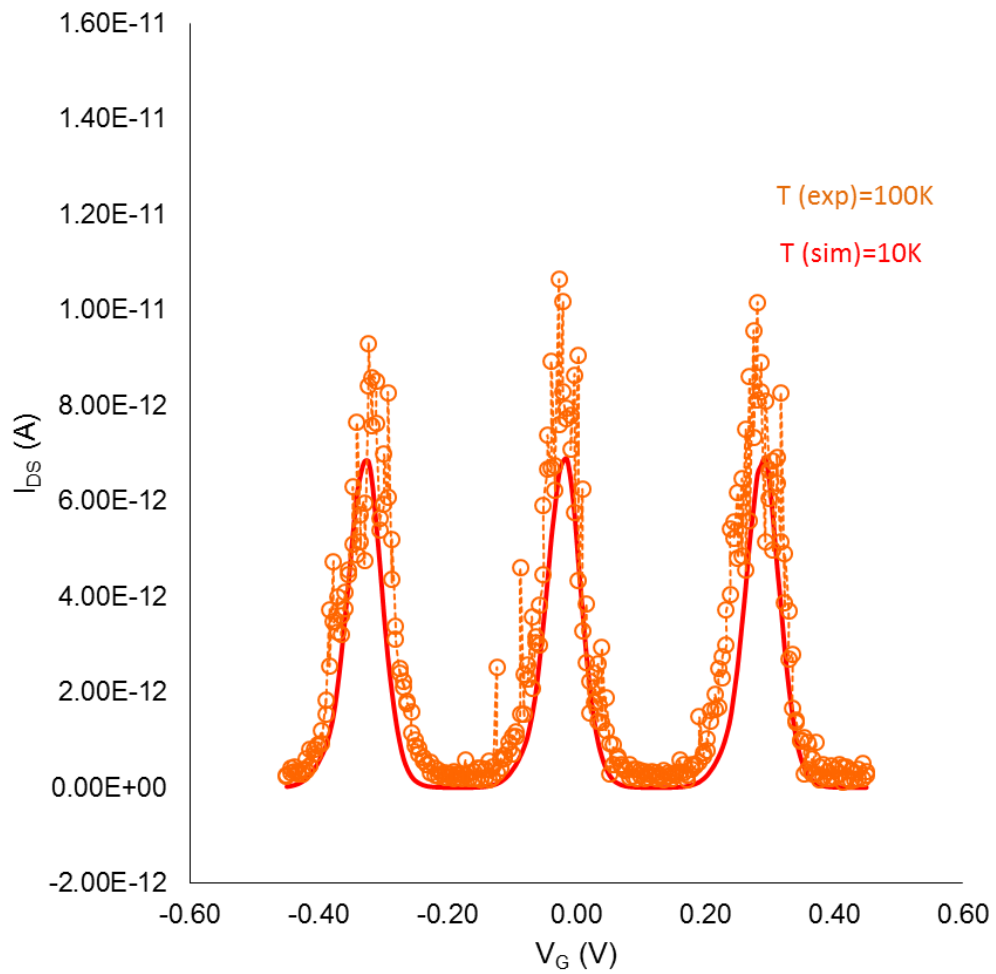

Figure 6.7 IV characteristic of Coulomb oscillation obtained at 100 K (experimental data from Vishva Ray). The effective temperature of the cold electron 10 K was used in orthodox theory calculation

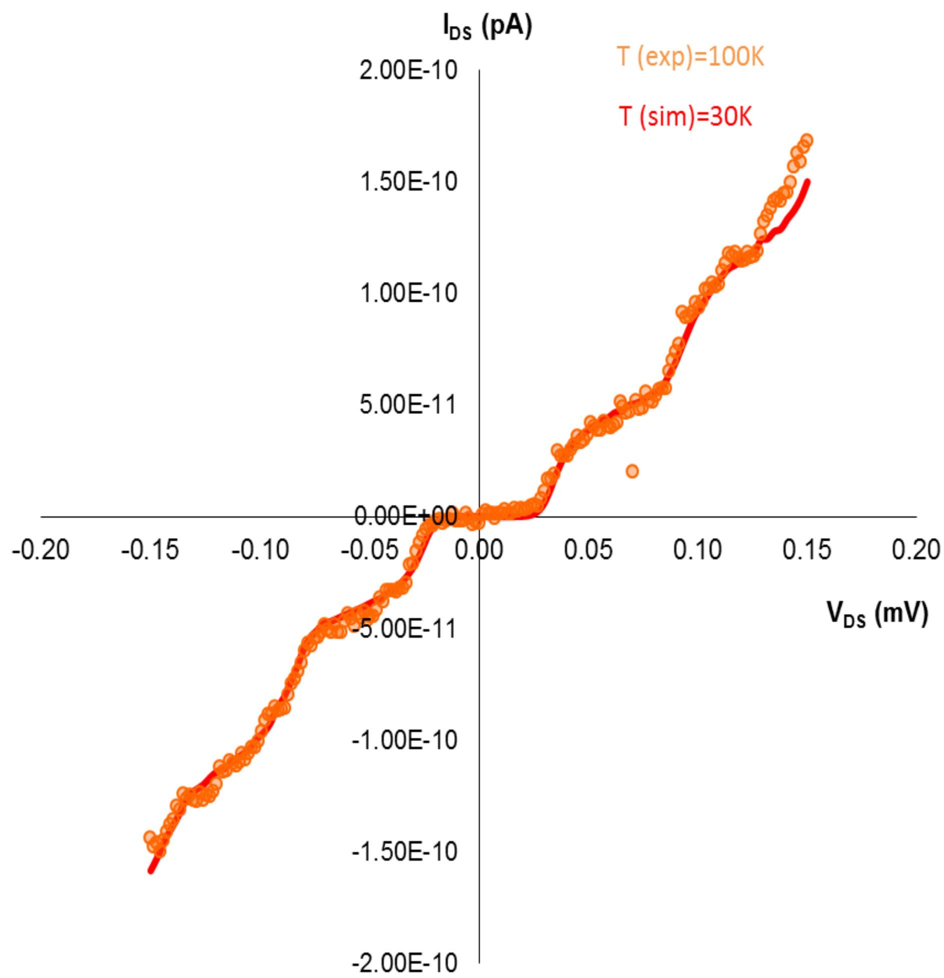

Figure 6.8 IV characteristic of Coulomb staircase obtained at 100 K (experimental data from Vishva Ray). The effective temperature of the cold electron 30 K was used in orthodox theory calculation

6.2 Model for Electron Energy Filtering in Single Electron Transistor

6.2.1 Components in the Model

According to the structure of our single electron device, we construct the model for electron energy filtering as showing in Fig 6.9. The model consist of a source (L), a quantum well (QW), a quantum dot (QD) and a drain (R) and two tunneling barriers separate the source, quantum dot and drain. Tunneling barrier is consisted of Cr2O3 and SiO2 in our device. Quantum well (QW) is formed in the interface of Cr2O3/SiO2 due to a band bending of the Cr_2O_3 conduction band [43-47]. The QW on the drain side is not shown in the model for simplicity because it does not contribute to the energy filtering. Since once the electron tunneling to the quantum well, it has energy higher than the chemical potential of drain. With or without the existence of quantum well in the drain side, it will tunnel to the drain anyway.

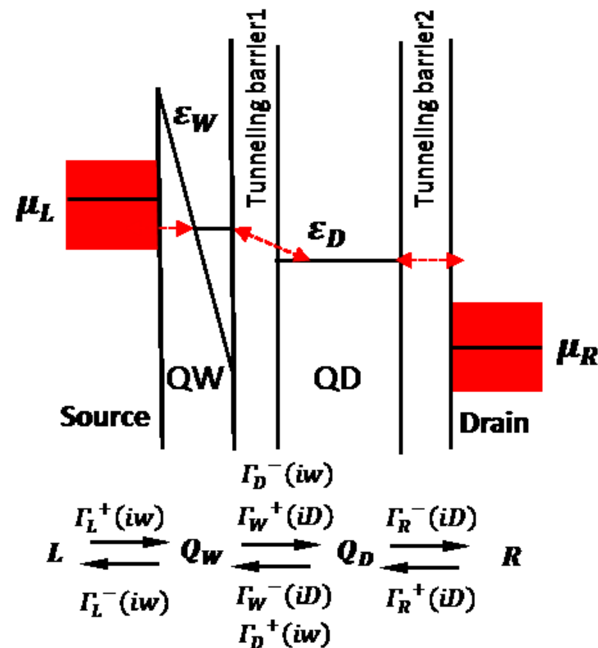

Figure 6.9 Ilustration for model of cold electron filtering

Electrons are sequentially transported through these components by tunneling (i.e. for example, from source tunnel to quantum well, and from quantum well to quantum dot, then from quantum dot to drain). Tunneling rates between etch adjacent component are governed by the positions of chemical potentials/the energy levels μ_L, ε_W, ε_D and μ_R of the source, QW, QD and drain, respectively as shown in Fig. 6.9. The definitions of tunneling rates are described as below:

- $\Gamma_L^{\pm}(i_W)$: the rate for an electron tunneling from the source electrode (L) to the QW ("+") or from QW to L ("–") when the number of electrons in the QW before the tunneling is i_W
- $\Gamma_D^{\pm}(i_W)$: the rate for an electron tunneling from the QD to the QW ("+") or from QW to QD ("–") when the number of electrons in the QW before the tunneling is i_W.
- $\Gamma_W^{\pm}(i_D)$: the rate for an electron tunneling from the QW to the QD ("+") or from QD to QW ("–") when the number of (extra) electrons in the QD before the tunneling is i_D
- $\Gamma_R^{\pm}(i_D)$: the rate for an electron tunneling from the drain electrode (R) to the QD ("+") or from QD to R ("–") when the number of electrons in the QD before the tunneling is i_D

When an electron in the QD, $\varepsilon_D > \mu_R$, with either QW presented or not, it can tunnel out to the drain anyway. So there is no contribution to electron filtering on the drain side and we can ignore it for simplicity in the energy diagram.

For a given set of rates, $\Gamma_L^{\pm}(i_W)$, $\Gamma_D^{\pm}(i_W)$, $\Gamma_W^{\pm}(i_D)$ and $\Gamma_R^{\pm}(i_D)$, we simultaneously solve the rate equations [48], which gives an electrical current *I* at a voltage bias *V.*

Compare the I-V from this model (theoretical) to the I-V from our single electron device (experimental) shows that they are in good agreement. This will be described in detail in the later section.

6.2.2 Elastic Tunneling Probability

For the electron transport between the QW and QD, it can be either elastic tunneling or inelastic tunneling depending on whether the electron energy is conservative or not through tunneling process. Two different conditions are shown in Figure 6.10. Elastic tunneling is that an electron tunnels between two states with same energies. Elactic tunneling probability for which the lifetime broadening with Lorizian distribution [49-51] is defined as $\gamma_{eleastic}(\varepsilon)$.

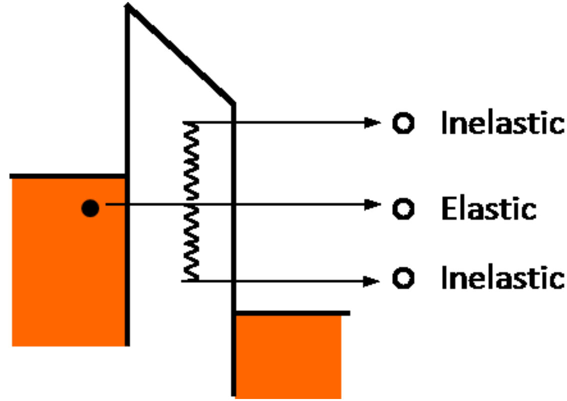

Figure 6.10 Illustration for elastic and inelastic tunneling.

$$\gamma_{elastic}(\varepsilon) = \frac{2}{\hbar}\left(\frac{\hbar T_{elastic}}{2}\right)^2 \frac{\frac{\hbar T_{elastic}}{2}}{\varepsilon^2 + \left(\frac{\hbar T_{elastic}}{2}\right)^2} \tag{6.1}$$

where ħ is the reduced Planck constant and $T_{elastic}$ is the elastic tunneling probability when the QW energy level and QD energy level aligned exactly. ε is the energy difference for the adjacent states (i.e. $\varepsilon = \varepsilon_w - \varepsilon_D$).

6.2.3 Inelastic Tunneling Probability

Inelastic tunneling process involves the electron energy changes when electron tunnels from a lower energy to a higher energy (energy gained) or from a higher energy state to a lower energy (energy lost) as shown in Figure 6.10. Energy gained during

tunneling is possible only when it is coupled with phonon absorption [52, 53]. Energy lost during tunneling can occur through phonon emission [37, 52, 53] and other energy relaxations process [51, 54-57] such as interface-roughness scattering, impurity scattering, and alloy disorder scattering [47, 55-57]. Figure 6.10 (b) and (c) shows the situations for energy gained and energy lost during tunneling process.

Tunneling probability is then discussed in two different situations with either electron gains or loses energy during tunneling process.

When energy gain process occurs, ε<0, tunneling probability through absorption $\gamma absorp(\varepsilon, T)$ is given by [52]:

$$\gamma_{absorp}(\varepsilon, T) = n(|\varepsilon|, T)A(|\varepsilon|) \tag{6.2}$$

where $n(|\varepsilon|, T))$ is the Bose-Einstein distribution function of phonon population [52],

$$n(|\varepsilon|, T) = \frac{1}{e^{\varepsilon/kT} - 1} \tag{6.3}$$

where *T* is the absolute temperature and *k* is the Boltzmann constant. $A(\varepsilon)$ is the Einstein A coefficient for spontaneous emission of phonons [46, 49, 50, 52, 53].

The total tunneling probability $\gamma(\varepsilon < 0, T)$ including with both elastic and inelastic process can be described:

$$\gamma(\varepsilon < 0, T) = \gamma_{absorp}(\varepsilon, T) + \gamma_{elastic}(\varepsilon)$$

$$= n(|\varepsilon|, T)A(|\varepsilon|) + \frac{2}{\hbar}\left(\frac{\hbar T_{elastic}}{2}\right)^2 \frac{\frac{\hbar T_{elastic}}{2}}{\varepsilon^2 + \left(\frac{\hbar T_{elastic}}{2}\right)^2}$$

$$= \frac{1}{e^{\varepsilon/kT} - 1}A(|\varepsilon|) + \frac{2}{\hbar}\left(\frac{\hbar T_{elastic}}{2}\right)^2 \frac{\frac{\hbar T_{elastic}}{2}}{\varepsilon^2 + \left(\frac{\hbar T_{elastic}}{2}\right)^2} \tag{6.4}$$

When energy lost process occurs, ε>0, tunneling probability through phonon emission $\gamma_{emiss}(\varepsilon, T)$ is given by [52, 53]:

$$\gamma_{emiss}(\varepsilon, T) = [n(|\varepsilon|, T) + 1]\, A(|\varepsilon|)$$

$$= \left[1/(e^{\varepsilon/kT} - 1) + 1\right] A(|\varepsilon|) \tag{6.5}$$

In addition to emission process, all other process that results in energy lost during tunneling such as interface-roughness scattering, impurity scattering, and alloy disorder scattering will be included in relaxation process. Tunneling probability through phonon relaxation is $\gamma_{relax}(\varepsilon)$.

The total tunneling probability in which an electron loses the energy in the tunneling process (ε>0) is

$$\gamma(\varepsilon > 0, T) = \gamma_{emiss}(\varepsilon, T) + \gamma_{elastic}(\varepsilon) + \gamma_{relax}(\varepsilon)$$

$$= \left[1/(e^{\varepsilon/kT} - 1) + 1\right] A(|\varepsilon|) + \frac{2}{\hbar}\left(\frac{\hbar T_{elastic}}{2}\right)^2 \frac{\frac{\hbar T_{elastic}}{2}}{\varepsilon^2 + \left(\frac{\hbar T_{elastic}}{2}\right)^2} + \gamma_{relax}(\varepsilon) \quad (6.6)$$

6.2.4 Rate Equations

In order to obtain the tunneling current of this model, we first calculate the free energy change of the system as previous sections. With the same free energy diagram as we constructed before for calculating the charging energy, we now just add a quantum well (QD) energy level to the diagram. Figure 6.11 shows the QD level ε_W in between electrode L and quantum dot (QD). We will calculate the free energy change of the system for each transition between adjacent components in this model. For an electron tunnels from quantum well to the Coulomb Island as showing in Figure 6.11, the free energy change ΔF_W^+ is defined as:

$$\Delta F_W^+ \equiv g_{IS}^+(N) - \varepsilon_W \quad (6.7)$$

where $g_{IS}^+(N)$ is the Fermi energy of the Coulomb Island when an electron is tunneled to Coulomb Island and ε_W is the energy level of QW. Here we make few assumptions for QW as below:

- Voltage drop only occurs at junction T_L and T_R.
- Quantum well acts as electron reservoir that charges the tunnel junction in the same way as we discussed in previous section.

- Quantum well can be occupied by two electrons. Thus it can have two states when it participates in the tunneling with Coulomb Island. The two states are electrons tunnel from the QW with either one or two electrons to Coulomb Island and electrons tunnel from Coulomb Island to QW with residence electrons one or zero.

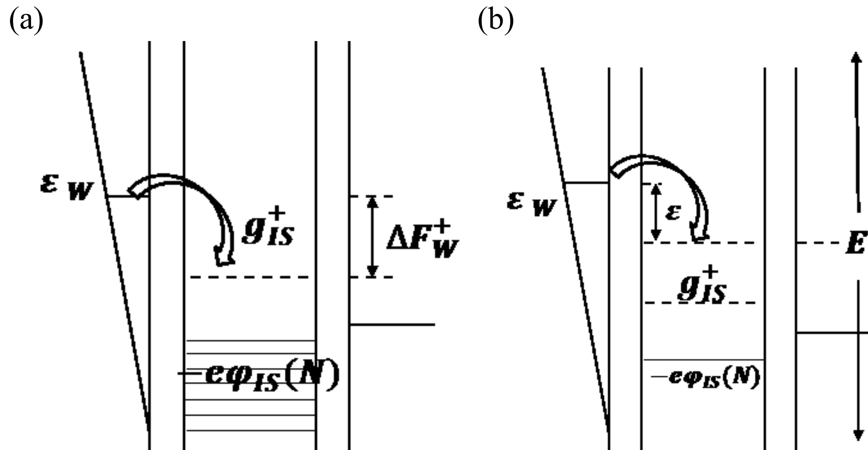

Figure 6.11 Schematic free energy diagram for electron tunneling from Quantum well to Coulomb Island.

The Fermi energy of the Coulomb Island $g_{IS}^+(N)$ can be obtained from Equation (3.65) as:

$$g_{IS} = \frac{e^2}{2C_{TOT}} - e\varphi_{IS}(N) \tag{3.65}$$

And $\varphi_{IS}(N)$ is the electrostatic potential of the Coulomb Island with N electrons, which is obtained from equation (3.67) as:

$$\varphi_{IS}(N) = \frac{C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0)}{C_{TOT}} \tag{3.67}$$

$$= \frac{C_L V_L + C_R V_R + C_G V_G - (Ne - Q_0)}{C_{TOT}}$$

Thus $g_{IS}^+(N)$ is obtained as:

$$g_{IS}^{+}(N) = \frac{e^2}{2C_{TOT}} - e\varphi_{IS}(N)$$

$$= \frac{e^2}{2C_{TOT}} - e\frac{C_L V_L + C_R V_R + C_G V_G - (Ne - Q_0)}{C_{TOT}} \quad (6.8)$$

Consider the case which involves the inelastic tunneling between QW and Coulomb Island, the tunneling can occur even when their energy levels are not aligned. Thus the electron can tunnel to any energy level E in QD rather than the energy level $g_{IS}^{+}(N)$. Figure 6.11 (b) illustrates the inelastic tunneling of the electron from the energy level ε_W in QW to any possible level E in QD. This energy level E is defined by the difference of these two levels ε, as

$$E = \varepsilon_W - \varepsilon$$

The tunneling probability $\hat{\gamma}_W^{+}$ is defined as the probability for an electron tunnel from QW to QD. Since the inelastic tunneling are involved, all energy levels E in QD has contributions to the total tunnel the total tunneling probability $\hat{\gamma}_W^{+}$. The tunneling probability $\hat{\gamma}_W^{+}$ thus should be:

$$\hat{\gamma}_W^{+}(\Delta F_W^{+}) = \int_{-\infty}^{\infty} \gamma(\varepsilon) D_{IS}(E) \left[1 - f_{g_{IS}^{+}(N)}(\varepsilon_W - \varepsilon)\right] d\varepsilon$$

where $f_{g_{IS}^{+}(N)}(\varepsilon_W - \varepsilon)$ is the Fermi-Dirac function of the QD with the Fermi energy $g_{IS}^{+}(N)$ When add one electron to it. $\gamma(\varepsilon)$ is the tunneling probability for tunneling from energy level ε_W to $\varepsilon_W - \varepsilon$. $D_{IS}(\varepsilon - E)$ is the density of state for QD. Since the Fermi energy of the QD is $g_{IS}^{+}(N)$, the tunneling probability $\hat{\gamma}_W^{+}(\Delta F_W^{+})$ becomes:

$$\hat{\gamma}_W^{+}(\Delta F_W^{+}) = \int_{-\infty}^{\infty} \gamma(\varepsilon) D_{IS}(E) \left[1 - \frac{1}{exp\left[\frac{\varepsilon_W - \varepsilon - g_{IS}^{+}(N)}{kT}\right] + 1}\right] d\varepsilon$$

$$\hat{\gamma}_W^{+}(\Delta F_W^{+}) = \int_{-\infty}^{\infty} \gamma(\varepsilon) D_{IS}(E) \left[1 - \frac{1}{exp\left[\frac{-(\varepsilon + \Delta F_W^{+})}{kT}\right] + 1}\right] d\varepsilon \quad (6.9)$$

Since $\varepsilon = \varepsilon_W - E$, the tunneling probability $\hat{\gamma}_W^{+}$ can also be expressed as:

$$\hat{\gamma}_W^+(\varepsilon_W - E) = \int_{-\infty}^{\infty} \gamma(\,\varepsilon_W - E) \times D_{IS}(E) \times \left[1 - f_{g_{IS}^+(N)}(E)\right] dE$$

$$\hat{\gamma}_W^+(\varepsilon_W - E) = \int_{-\infty}^{\infty} \gamma(\,\varepsilon_W - E) \times D_{IS}(E) \times \left[1 - \frac{1}{exp\left[\frac{E - g_{IS}^+(N)}{kT}\right] + 1}\right] dE$$

$$\hat{\gamma}_W^+(\varepsilon_W - E) = \int_{-\infty}^{\infty} \gamma(\,\varepsilon_W - E) \times D_{IS}(E) \times \left[1 - \frac{1}{exp\left[\frac{E - \Delta F_W^+ - \varepsilon_W}{kT}\right] + 1}\right] dE \quad (6.10)$$

Similarly, when the electron tunneling from QD to QW, the free energy change ΔF_W^+ can be defined as:

$$\Delta F_W^- \equiv \varepsilon_W - g_{IS}^-(N) \quad (6.11)$$

Where $g_{IS}^-(N)$ is the Fermi energy of the QD when remove one electron from it. The tunneling probability $\hat{\gamma}_W^-$ is obtained as:

$$\hat{\gamma}_W^-(\Delta F_W^-) = \int_{-\infty}^{\infty} \gamma(\,E - \varepsilon_W) \times D_{IS}(E) \times f_{g_{IS}^-(N)}(E)\, dE$$

$$\hat{\gamma}_W^-(\Delta F_W^-) = \int_{-\infty}^{\infty} \gamma(\,E - \varepsilon_W) \times D_{IS}(E) \times \frac{1}{exp\left[\frac{E - g_{IS}^-(N)}{kT}\right] + 1} dE$$

$$\hat{\gamma}_W^-(\Delta F_W^-) = \int_{-\infty}^{\infty} \gamma(\,E - \varepsilon_W)) \times D_{IS}(E) \times \frac{1}{exp\left[\frac{E + \Delta F_W^- - \varepsilon_W}{kT}\right] + 1} dE \quad (6.12)$$

6.2.5 Master Equations

Now consider the QD as the center where the electron can either tunnel in or out as the QW discussed above. Similarly, when the electron tunneling from QD to QW, the free energy change ΔF_{IS}^+ can be defined as:

$$\Delta F_{IS}^+ \equiv \varepsilon_W - g_{IS}^-(N) \quad (6.13)$$

where $g_{IS}^-(N)$ is the Fermi energy of the QD when remove one electron from it. The tunneling probability $\hat{\gamma}_{IS}^+$ is obtained as:

$$\hat{\gamma}_{IS}^+\,(\Delta F_{IS}^+) = \int_{-\infty}^{\infty} \gamma(\,E - \varepsilon_W) \times D_{IS}(E) \times f_{g_{IS}^-(N)}(E)\, dE$$

$$\hat{\gamma}_{IS}^+\,(\Delta F_{IS}^+) = \int_{-\infty}^{\infty} \gamma(\,E - \varepsilon_W) \times D_{IS}(E) \times \frac{1}{exp\left[\frac{E - g_{IS}^-}{kT}\right] + 1} dE$$

$$\hat{\gamma}_{IS}^{+}\ (\Delta F_{IS}^{+}) = \int_{-\infty}^{\infty} \gamma(\ E - \varepsilon_W)) \times D_{IS}(E) \times \frac{1}{exp\left[\frac{E + \Delta F_{IS}^{+} - \varepsilon_W}{kT}\right] + 1} dE \qquad (6.14)$$

Similarly, $\hat{\gamma}_{IS}^{-}\ (F_{IS}^{-})$ is obtained as

$$\hat{\gamma}_{IS}^{-}\ (\Delta\ F_{IS}^{-}) = \int_{-\infty}^{\infty} \gamma(\ \varepsilon_W - E) \times D_{IS}(E) \times \left[1 - f_{g_{IS}^{+}(N)}(E)\right] dE$$

$$\hat{\gamma}_{IS}^{-}\ (\Delta F_{IS}^{-}) = \int_{-\infty}^{\infty} \gamma(\ \varepsilon_W - E) \times D_{IS}(E) \left[1 - \frac{1}{exp\left[\frac{E - g_{IS}^{+}(N)}{kT}\right] + 1}\right] dE$$

$$\hat{\gamma}_{IS}^{-}\ (\Delta F_{IS}^{-}) = \int_{-\infty}^{\infty} \gamma(\ \varepsilon_W - E) \times D_{IS}(E) \left[1 - \frac{1}{exp\left[\frac{E + \Delta F_{IS}^{-} - \varepsilon_W}{kT}\right] + 1}\right] dE \qquad (6.15)$$

Now we define $P_W(iw)$ as the probability that the number of electrons occupy the QW is iw and $P_{IS}(iIS)$ as the probability that the number of electrons occupy the QD is iIS. iw can be 0, 1 or 2 and iIS can be any integer number N. The tunneling rate Γ for each component and direction can be obtained as below:

$$\Gamma_L^{+}(0) = f_L(\varepsilon_W) \times D_L(\varepsilon_W) \times T_L \qquad (6.16)$$

$$\Gamma_L^{+}(1) = f_L(\varepsilon_W) \times D_L(\varepsilon_W) \times T_L \qquad (6.17)$$

$$\Gamma_L^{-}(1) = [1 - f_L(\varepsilon_W)] \times D_L(\varepsilon_W) \times T_L \qquad (6.18)$$

$$\Gamma_L^{-}(2) = [1 - f_L(\varepsilon_W)] \times D_L(\varepsilon_W) \times T_L \qquad (6.19)$$

$$\Gamma_{IS}^{+}(0) = \sum_N \hat{\gamma}_{IS}^{+}\ (\Delta F_{IS}^{+}) \times P_{IS}(N) \qquad (6.20)$$

$$\Gamma_{IS}^{+}(1) = \sum_N \hat{\gamma}_{IS}^{+}\ (\Delta F_{IS}^{+}) \times P_{IS}(N) \qquad (6.21)$$

$$\Gamma_{IS}^{-}(1) = \sum_N \hat{\gamma}_{IS}^{-}\ (\Delta F_{IS}^{-}) \times P_{IS}(N) \qquad (6.22)$$

$$\Gamma_{IS}^{-}(2) = \sum_N \hat{\gamma}_{IS}^{-}\ (\Delta F_{IS}^{-}) \times P_{IS}(N) \qquad (6.23)$$

$$\Gamma_W^{+}(N) = \hat{\gamma}_W^{+}\ (\Delta F_W^{+}) \times [P_W(1) + P_W(2)] \qquad (6.24)$$

$$\Gamma_W^{-}(N) = \hat{\gamma}_W^{+}\ (\Delta F_W^{-}) \times [P_W(0) + P_W(1)] \qquad (6.25)$$

$$\Gamma_R^{+}(N) = \frac{1}{R_R e^2} \times \frac{-\Delta F_R^{+}(N)}{1 - exp\left[\frac{\Delta F_R^{+}(N)}{kT}\right]} \qquad (6.26)$$

$$\Gamma_R^-(N) = \frac{1}{R_R e^2} \times \frac{-\Delta F_R^-(N)}{1 - exp\left[\frac{\Delta F_R^-(N)}{kT}\right]} \tag{6.27}$$

where $f_L(\varepsilon_W)$ is the Fermi-Dirac function with chemical potential μ_L for source electrode (L) and R_R is the tunneling resistance of the drain electrode (R).

At a steady state, the net transition is zero thus the two adjacent states have the same transition rates. For example, the transition rate for electron to tunnel in to the QW will be the same as the transition rate for electron to tunnel out of it. So we can construct the master equation for the tunneling rate Γ as:

i. for the QW with configuration $iw = 0$ and $iw = 1$

$$P_W(0)[\Gamma_L^+(0) + \Gamma_{IS}^+(0)] = P_W(1)[\Gamma_L^-(1) + \Gamma_{IS}^-(1)] \tag{6.28}$$

ii. for the QW with configuration $iw = 1$ and $iw = 2$

$$P_W(1)[\Gamma_L^+(1) + \Gamma_{IS}^+(1)] = P_W(2)[\Gamma_L^-(2) + \Gamma_{IS}^-(2)] \tag{6.29}$$

iii. for the QD with configuration $iIS = N$ and $iIS = N + 1$

$$P_{IS}(N)[\Gamma_W^+(N) + \Gamma_R^+(N)] = P_{IS}(N+1)[\Gamma_W^-(N+1) + \Gamma_R^-(N+1)] \tag{6.30}$$

iv. the summation of the probability of P_W with all possible configurations must be unity

$$P_W(0) + P_W(1) + P_W(2) = 1 \tag{6.31}$$

v. the summation of the probability of P_{IS} with all possible configurations must be unity

$$\sum_N P_{IS}(N) = 1 \tag{6.32}$$

The probabilities $P_W(iw)$ and $P_{IS}(N)$ are the unknowns for the master equations we constructed above. For a given set of tunneling rates Γ with specified V, the master equations can be solved numerically and the probabilities $P_W(iw)$ and $P_{IS}(N)$ can be obtained.

The tunneling current $I(V)$ can be obtained as:

$$I(V) = e \sum_{-\infty}^{\infty} P_{IS}(N)[\Gamma_R^-(N) - \Gamma_R^+(N)] \tag{6.33}$$

Chapter 7

Silicon Nanopillar Single Electron Device

7.1 Introduction

Our SET architecture has been demonstrated successfully with coulomb blockage/staircase and coulomb oscillations at room temperature in previous chapters. In this SET structure presented, however, the tunneling junction is not controlled because of the random attachment of gold nanoparticles. In order to have a better control of the tunnel junction, we provide the nanopillar SED structure as a solution. All of the device components will be built within a nanopillar by depositions of multiple layers then etched down using nanoparticles as a mask. The source, drain, and most importantly Coulomb Island and tunnel junction can be precisely defined through the deposition technique.

Nanoparticles were utilized as a mask for dry etching process and defined the diameter of the nanopillar. Compared with other fabrication technique of making nano-scale objects, like e-beam lithography, our process is a parallel process and has the advantage of providing the ability of large scale production. Furthermore, the fabricated nanopillar can be addressed in the desired location and interconnected through this process.

A practically feasible fabrication strategy that enables massive manufacturing and integration of nanopillar single electron transistor will be provided with detailed process steps.

7.2 Proposed Structure of Silicon Nanopillar Single Electron Device

The proposed architecture of Si nonopillar single electron device is shown in Figure 7.1. All the components for single electron device were defined within a single nanopillar. Vertical stacked Cr, Cr_2O_3, SiO_2, and Si multilayers were deposited on a silicon dioxide substrate to define the source, drain, coulomb island layers and tunneling junctions. Silicon island layer were separated by two tunneling SiO_2-$Cr2O_3$ layers.

Nanopillar structure was formed by dry etching of this multilayer with silicon oxide and gold nanoparticle as hard masks.

Cr_2O_3 and SiO_2 were chosen to be the tunnel junction in this nanopillar SED. The reason is that a quantum well will be formed in the interface of Cr_2O_3/SiO_2 due to the conduction bend bending of the Cr_2O_3 [43-47]. Through this quantum well, the electron energy filtering can occur so that operation temperature of the SED can be raised up to room temperature.

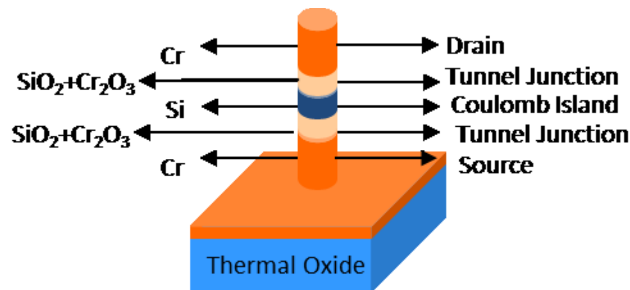

Figure 7.1 Architecture of Si nanopillar single electron device.

The coulomb island is made by a silicon layer with thickness of 5 nm. The size of Coulomb island is determined by the size of the masking nanoparticle for dry etching process.

The components of SED, which include source, tunnel junctions, Coulomb Island, and drain, are vertically aligned in the nanopillar SED. The separation between source and drain, and the width of tunnel junction can be defined by the thickness of the deposited layer. The control of separation can be achieved down to less than 5nm through the deposition technique.

7.3 Fabrication of Nanopillars

The nanopillar structure was formed in 2 step dry etching process. In the first step, a SiO_2 film was dry etched using gold nanoparticle as a hard mask, as shown in Figure 7.2 (a). After SiO_2 nanopillars were formed, gold nanoparticles will be removed, as shown in Figure 7.2 (b) and (c). In second step, we utilized the fabricated SiO_2 nanopillar as the hard mask for dry etching of the multilayers, as shown in Figure 7.2 (d). The reason for using this 2 step dry etching process is because that gold nanoparticle cannot be sustained through the whole dry etching step of multilayer. During the dry etching process, the hard mask will be consumed. The high of SiO_2 nanopillar can be tuned to the desire range so that hard mask will be survived during the whole dry etching process.

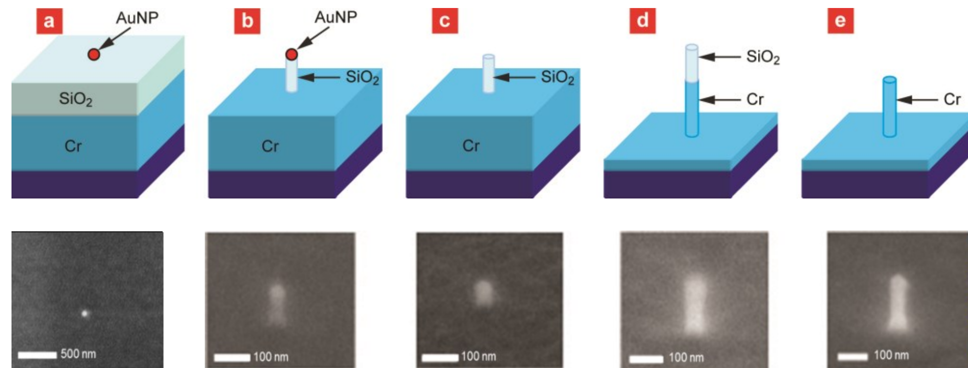

Figure 7.2. Two step dry etching process for fabrication of nanopillars.

In first step, SiO_2 nanopillar will be fabricated by dry etching SiO2 using gold nanoparticle as a hard mask as shown in Figure 7.2 (a). Gold nanoparticles were deposited on the SiO_2 surface by the similar SAMs process mentioned in chapter 4. The SiO_2 substrate was first immersed in APTES solutions for 30 minutes in order to have APTES SAMs formed on the SiO_2 surface. Then the sample was rinsed with ethanol and water to remove the residual solution and blown dried by stream of nitrogen. After SAMs was formed, immersed the sample in the gold colloid solution for gold nanoparticle attachment. Immersion time will depend on the concentration of gold colloid solution and

the desired density of gold attachment. For the 50 nm gold nanoparticle attachment, 1 minute immersion time was used for roughly 1 particale attached at area of 26 um x 26 um.

The dry etching process of SiO_2 nanopillar was carried in the etcher of Technic MicroRIE 800. Sample was first cleaned in the UV-O3 cleaner for 30 minutes. This step is to remove the SAMs of APTES. We found that the residual of APTES will affect the dry etching process, especially for the profile of the nanopillar. It will cause the undercut on the fabricated nanopillar with the APTES presented in the open area during dry etching process.

The dry etching chamber was also cleaned before performing our dry etching process. The dry etching process is strongly affected by the chamber condition which was carried over from previous usage. We use wet chemical cleaning process with the isopropanol alcohol to physically remove residuals from previous process. In addition of wet clean, an oxygen plasma process was performed for 30 minutes to clean the residual from wet chemical clean.

After cleaning of both sample and etcher, we put the sample in the chamber to perform dry etching process with the recipe:

CF4= 25 sccm

O2= 10 sccm

Pressure = 120 mTorr

Power = 150 W

SiO_2 will be dry etched vertically with a etch rate around 50 nm per minute. Almost no undercut in the profile was found under the FE-SEM image for the fabricated SiO_2 nanopillar with a high of 150 nm as shown in Figure 7.3. Usually 1 minute over etch will be carried to ensure that the SiO_2 was fully removed. As the SiO_2 nanopillar was fabricated, the Au nanoparticle was removed by wet etching of gold before going for Cr dry etching as shown in Figure 7.2 (c). This is because that gold will affect the dry etching profile for Cr dry etching. It has nonvolatile product in the Cl_2 chemistry so it will be

sputtered out and be redeposited on the Cr nanopillar and the reaction chamber of the etcher.

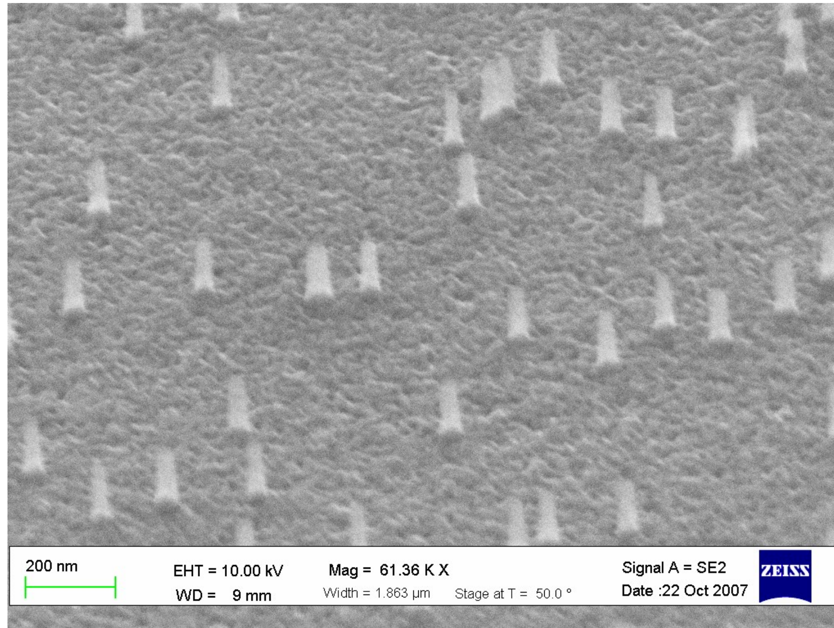

Figure 7.3 FE-SEM image of SiO2 nanopillar on top of Cr.

The second step, Cr nanopillar will be fabricated by dry etching chromium in a RIE etcher with configuration of “inductive coupled plasma” (ICP), using SiO_2 nanopilllar as a hard mask as illustrated in Figure 7.2 (d). Chlorine and oxygen were used as reaction gas in this etching process, with addition of Ar for physical bombardment to improve the profile of the fabricated Cr nanopillar. The chemical etching reaction in this process is

$$Cr + 2O^* + 2Cl \rightarrow CrO_2Cl_2$$

The reaction product is volatile and can be pumped out so that etching can be achieved. It was found that with the pure chemical etching process, the undercut profile will always be obtained on the final Cr nanopillar. Because the requirement for the diameter of the final nanopillar is critical, usually around 50 nm or below, we want to

avoid the undercut to prevent nanopillar "falling down" during the etching process. We found that with the addition of Ar, there will be certain extent of physical etching (bombardment). With the balance between the chemical and physical etching reaction, the optimized etching profile can be obtained. The recipe used for Cr nanopillar dry etching is described

- Pressure = 10 Torr
- Cl_2= 80 SCCM
- O_2 = 20 SCCM
- Ar= 10 SCCM
- Top Electrode ICP Power = 500W
- Bottom Electrode R.F. Power = 50W
- Temperature = 10C

The reaction chamber of the etcher was always performed with oxygen plasma cleaning process to clean the etching residuals from previous usage and precondition the chamber with the same recipe as the real etching to stabilize the initial plasma in the following dry etching of Cr nanopillar.

Our sample with masking SiO_2 nanopillar was first attached on a loading wafer by carbon dot. Then the loading wafer was loaded into the main reaction chamber with a loadlock system. After transferred to the main reaction chamber, sample will stay in the chamber for 5 minutes to thermal equilibrium before starting the dry etching process. 300 nm of Cr layer will be dry etched away in 656 seconds with a rate 0.451 nm per minute in this recipe. Figure 7.4 shows the FE-SEM image of Cr nanopillars with a vertical profile.

Note that in this picture, the oxide mask was remained on top of the Cr nanopillar. It will be stripped off latter by dry etching oxide in the Micro RIE chamber.

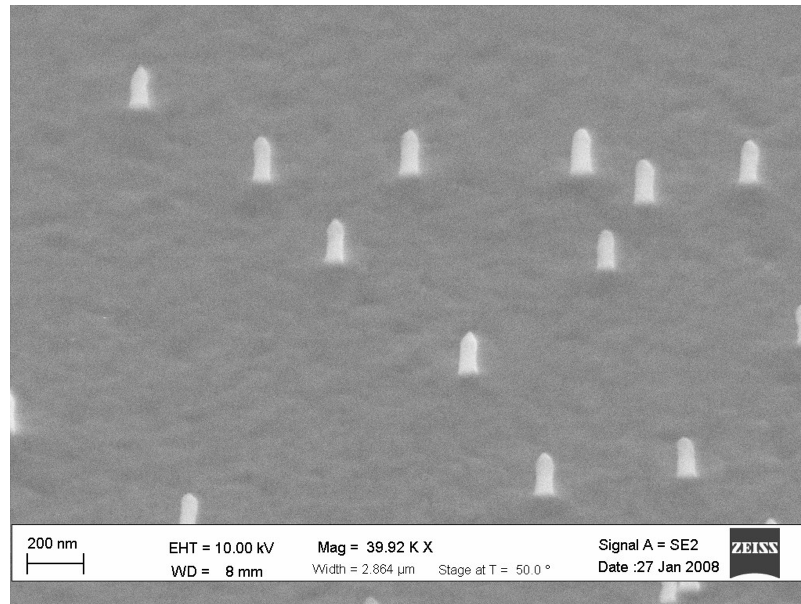

Figure 7.4 Cr nanopillar on top of Cr

7.4 Interconnection of Nanopillars

After the fabrication of nanopillars, they need to be able to interconnect with other devices and outside world. To have connection with the nanopillars, we first planarized the substrate together with nanopillars then partial etch back the planarizer so that only top portion of the nanopillars exposed. A bond pad can be formed in the nanopillar exposed area and a VIA can be created at the area without nanopillars. A simple flow chart to explain the concept is illustrated in Figure 7.5.

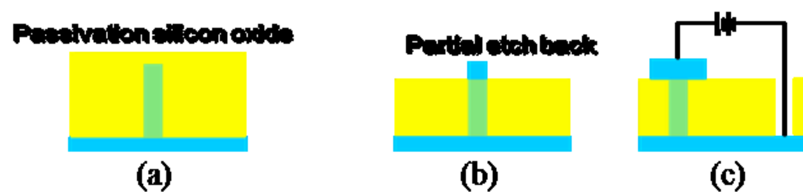

Figure 7.5 Interconnection of the fabricated nanopillar. (a) Planarization (b) Partial etch back (c) VIA etching and bond pad formation.

Spin on glass (SOG) was used as the planarizer to planarize the nanopillars as shown in Figure 6.22 (a). SOG 500F (Filmtronics Inc.) were used with a film thickness around 500~600 nm after post curing. It was first spun coated on the sample with the speed of 3000 RPM for 20 seconds then went to soft baking on a hot plate at 80 C^0 for 1minute and 50 C^0 for 1minute. Following the soft bake, the sample was cured at 425 C^0 for 3 hours in the oven under nitrogen protected atmosphere. A flat SOG surface was obtained where all the nanopillars are underneath.

Partial etch back of SOG was performed to open the contact top contact area on the nanopillar as shown in Figure 7.5 (b). We use the dry etching process to control the removal of SOG in the manner of uniformed and vertical etching. Dry etch process was performed in DRIE chamber with CF_4 as the reaction gas. The etch depth was controlled by the dry etching time calculated from the etch rate of the SOG. Target etch depth was determined by the desired nanopillar high after exposition, SOG film thickness, and original Nanopillar high. For example, if we want to expose 50 nm of the top portion of the nanopillar which has a high of 250 nm, 200 nm SOG film will be remained after etching. For the SOG with thickness of 600 nm, 400 nm SOG will be etched away. SOG dry etch arte is 2.66 nm per minute in DRIE chamber, so we can know the process time for dry etching of SOG. Figure 7.6 and 7.7 showed the FE-SEM images of fabricated nanopillar with SOG film before and after partial etch back process, respectively.

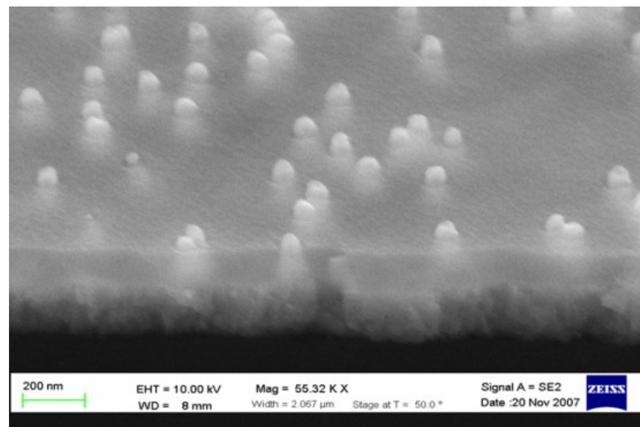

Figure 7.6 Nanopillar under the SOG film before partial etch back process

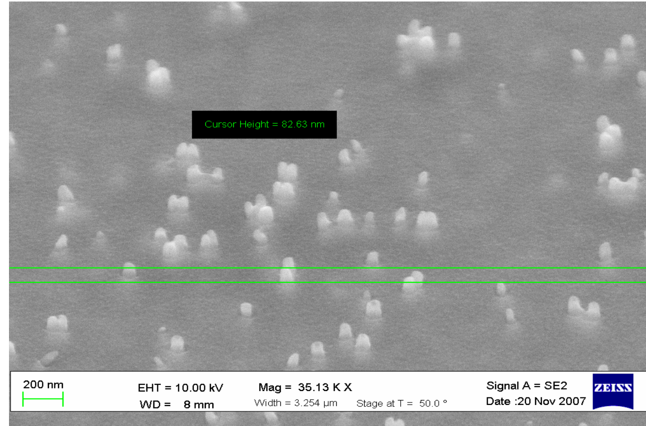

Figure 7.7 Nanopillar under the SOG film after partial etch back process.

Bond pad was made to provide the contact on top of the nanopillar. It was fabricated by photo lithography, metal evaporation, and lift-off process. The resist pattern was defined as an open area on top of the pillar which was partially exposed from SOG, as shown in Figure 7.5 (c). The area where nanopillar was fabricatied was predefined by photo lithography, so it can be aligned with the bond pad pattern on the mask. Negative photoresist, NR 9-1000PY, was used to define the bond pad so bond pad area will be opened after developed for latter lift-off process. Lithography process was carried with same recipe as we describe in the fabrication section. 200 nm Cr layer was deposited on top of the patterned sample in AJA E-beam evaporator. Lift- off process was carried by ultrasonic agitation for a bath of acetone in where sample was immersed. As the photoresist and unwanted Cr removed, bond pad was formed.

VIA was created on the SOG film to open another contact with the bottom of the nanopillar as shown in Figure 6.22 (c). Since the nanopillars were fabricated on the metal substrate, the bottom of the nanopillars were originally connected with the substrate. VIA can be opened in a lateral distance away from the nanopillars so that only metal substrate was exposed. With the bond pad made for the contact on top of the nanopillar and VIA for the bottom, nanopillar can be interconnected with other devices and to outside world.

VIA was created by dry etching of the SOG with photoresist as the mask. Photolithography was applied to define the mask for VIA dry etching process. The fabrication of nanopillars can be confined in the predefined addressable area, so VIA can be defined on the empty area where no nanopillar exists (more detailed process will be described in the coming section). The lithography process is the same as mentioned in the fabrication chapter to define VIA pattern. Negative photoresist NR9-1000 PY was used to define the open area for latter VIA dry etching and other area covered by resist will be protected during the dry etching process.

The dry etching process for VIA formation was carried in the DRIE chamber. SOG will be etched away using CF_4 as the reaction gas. Source electrode will be exposed and serving as the etch stop because metal was not etched in the CF_4 chemistry. Photoresist was removed after dry etching process and VIA formation was completed.

7.5 Integrated Process Flow

In order to describe the all steps in the process for fabrication of nanopillar SED, a complete process flow was illustrated in Figure 7.8.

a. Si nanopillar SED device were fabricated starting on a 4-inch silicon wafer. An isolation silicon oxide layer around 1.5 μm thick is thermally grown on top of the silicon wafer. Source electrode was defined by photolithography, deposition of 200 nm layer of Cr, and lift-off process. The green square indicated the target location where nanopillars were going to be fabricated.

b. Deposition of multilayers for tunneling junctions, Coulomb Island, and drain. Tunneling junctions were composed by sputtering 1 nm of Cr oxide and 1 nm of SiO2 layers in AJA sputter system. Cr oxide was deposited first on top of bottom Cr electrode. Without breaking the vacuum, a 1 nm thick SiO2 layer was deposited by reactive sputtering of silicon. These two thin dielectric layer create an interface where the quantum well can be formed. Following the deposition of tunneling junction, a Coulomb

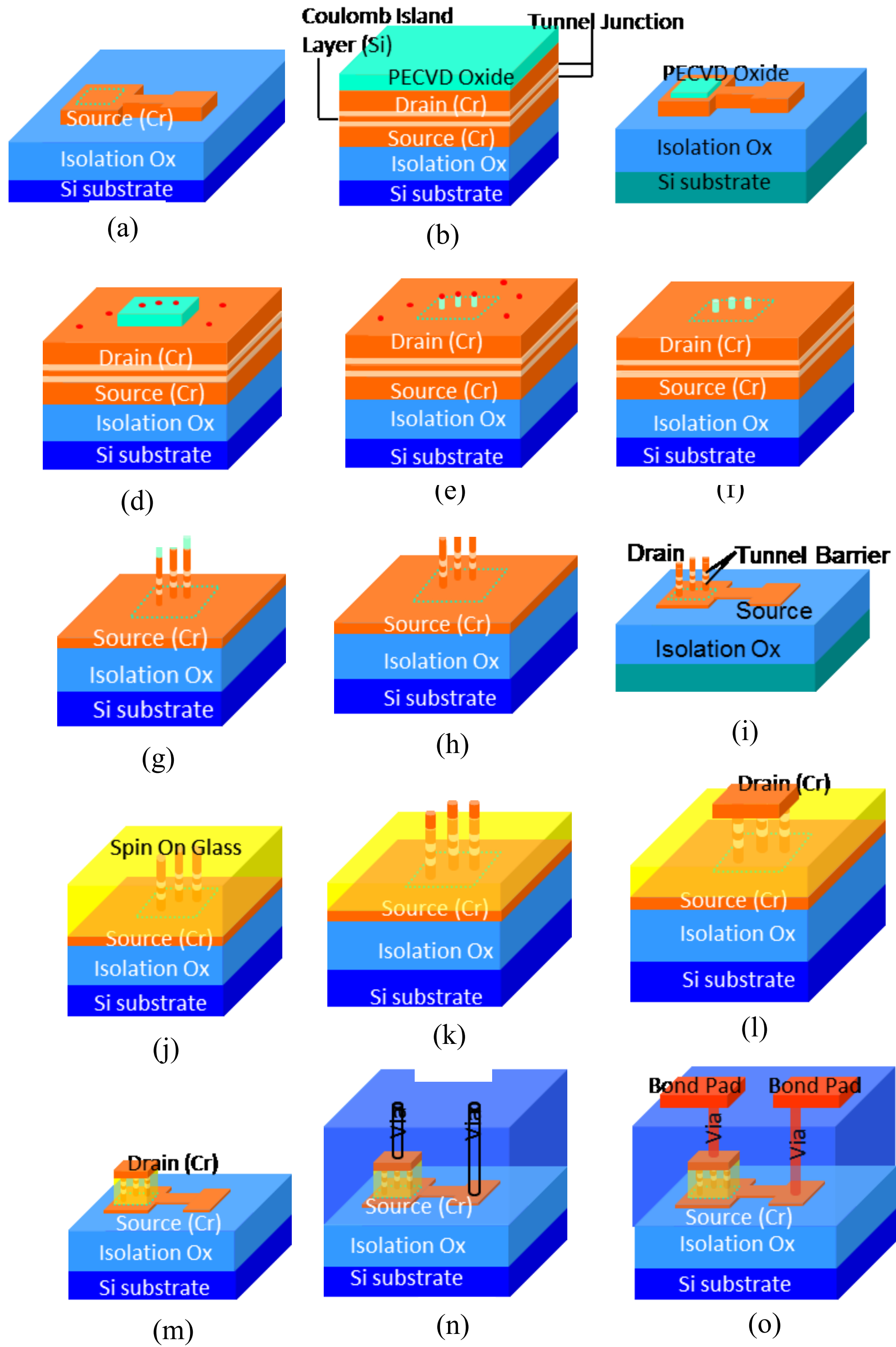

Figure 7.8 Complete process flow for fabrication of silicon nanopillar single electron device.

island layer was deposited by sputtering a 5 nm Si layer in the same chamber. Again, after Si layer, second tunneling junction was sputtered in the same chamber similar to previous one, which was composed with 0.8nm of silicon oxide layer and 1 nm of Cr oxide layer, respectively. Drain electrode was deposited by evaporating a 200 nm Cr layer on the multilayers in AJA e-beam evaporator. Up to here, all the components for Si nanopillar SED were completed. Finally, a PECVD silicon oxide layer was deposited in order to making the silicon nanopillar.

c. PECVD silicon oxide was patterned by dry etching process in DRIE etcher to define the location where Si nanopillars were going to be fabricated. Photoresist were serving as a mask for dry etching process. Only PECVD oxide pattern was showed in this figure in order to show that it is aligned with the source electrode. The multilayers underneath were omitted for clarity.

d. Gold nanoparticles were deposited by forming the SAMs of APTES then immersed the substrate in gold solution for nanoparticle attachment.

e. RIE etching of oxide. Au nanoparticles were serving as hard masks during etching. Silicon oxide nanopillars were fabricated at this step.

f. Removal of Au nanoparticles by wet etching. PECVD oxide nano pillars were located only in the defined drain area.

g. RIE etching of multilayers. PECVE oxide pillars were serving as hard masks during etching. Si nanopillars SED were fabricated in this step. Source, coulomb island and drain were vertically aligned and separated by tunnel junction in all SI nanopillars.

h. Removal of oxide pillars by RIE etching.

i. Si nanopillar SED were fabricated in the pre-defined location (green square) on source electrode.

j. Planarization of the Si nanopillar SED by deposition of spin on glass.

k. RIE etching of spin on glass. Partial etching of spin on glass so that only the drains in the pillars were exposed.

l. Deposition of drain electrode using photolithography, deposition of Cr and lift–off.

m. RIE etching of spin on glass. Drain electrodes were serving as hard masks and source electrode will be exposed after etching.

n. Deposition of passivation layer and formation of VIA. 600 nm SiO_2 was sputtered on the sample in the Home build sputter system. VIA were made by RIE etching of SiO_2 with photoresist as mask.

o. Bond pads were made by evaporation of 100 nm of Cr layer and 300 nm of Au layer in thermal evaporator.

Chapter 8

Electrostatic Funneling for Precise Nanoparticle Placement

8.1 Introduction

Among the challenges of fabrication of single electron device, one difficulty is the manipulation of nano objects like particle or pillars which is usually the core of the device. In our single electron device, the process of quantum dot (gold nanoparticle) placement is not precisely controlled. Quantum dot attachment along the sidewall of source, SiO_2 and drain is random. The distance between source to quantum dot, or quantum dot to drain is varied for each nanoparticle attached on that device. The particle only positioned at a correct tunneling distance between source and drain is participating single electron transport. This leads to a large portion of devices fabricated having open circuit. From our experiments, more than 70% of the devices showing either open circuit or absent of coulomb blockade, staircase, or oscillations. Statistically the yield of working device is around 1% due to the random placement of quantum dot.

Recently, a lot of attention has been given to manipulation of nanoscale objects such as nanoparticles and nanotubes because their unique properties are ultilized in many electronic devices and biological sensors. Many researches have been focused on placing the nanoscale objects on specified substrate locations. Their approaches include the use of microfluids [58, 59], electric fields [60, 61], magnetic field [62], surface functionalization [63-67], capillary forces [68-70], biological templates [71-76], and scanning probe microscopy [77]. Although these methods have had significant success, a method that can provide large-scale placement of nanoscale objects have not yet be demonstrated.

The need for a much higher yield in fabrication of single electron device could be achieved through precise controlling of the nanoparticle placement. We provide a positioning method which can have not only precise placement of nanoparticle but also a parallel process for a large scale fabrication. This method utilizes two different self-

assembled layers (SAMs) selectively formed on the surface of different substrate. Two modified surfaces will then have opposite charges in a solution. While putting the substrates into a colloidal solution of quantum dots (gold for our case) for attachment, the charges from the nanoparticle (negative for gold) provide either the attractive force or repulsive force to the charged surface depending on the polarities of that surface. The nanoparticle can be precisely attached on the desired position through predefined guiding pattern with electrostatic force in the solution. We have named this nanoparticle placement technique by "Electrostatic Funneling". In coming section, more detailed concepts and process will be discussed and the effectiveness of this method will be exhibited.

8.2 Concept

The concept of electrostatic funneling is based on the interaction of attractive and repulsive force between substrate surfaces and nanoparticles. The surface of substrate on where self-assembled monolayer (SMAs) was formed is either positively or negatively charged in an aqueous solution due to the functional group of SAMs dissociated in the solution. When such substrates immerse in a colloidal solution containing negatively charged nanoparticles, attractive and repulsive force between nanoparticles and surface of the substrate will guide the positioning of nanoparticles to a favorite low energy site. Two different SAMs were selectively formed on the surface of two different substrate lines in our predefined guiding structures as illustrated in Figure 8.1 [78]. The surface of alternative lines thus carried opposite charges in aqueous solution determined by the functional group of the SAMs. As a negatively charged nanoparticles approaching to such surfaces, the interaction energy is schematically shown in Figure 8.1 (a). Maximum and minimum interaction energy is located at the center of the line. The nanoparticles were attracting to the positively charged line in Z direction while at the same time were pushed to the center of the line in X direction by the repulsive force from the negatively charged line. The lateral force parallel to the substrate is understood as the gradient of the

interaction energy and its direction is always toward the center of the line where the position of the minimum of the interaction energy is. Once a nanoparticle was placed on the substrate, the other nanoparticles cannot occupy the same site due to the repulsion from the same charges carried on the nanoparticle surface.

The lateral force is a function of the separation between the nanoparticles and the substrates surface. Force is greater when the separation is smaller. Thus when nanoparticles are approaching to the substrate surface, they experience a greater and greater electrostatic force guiding their movement just like a virtual funnel placed on the substrate surface.

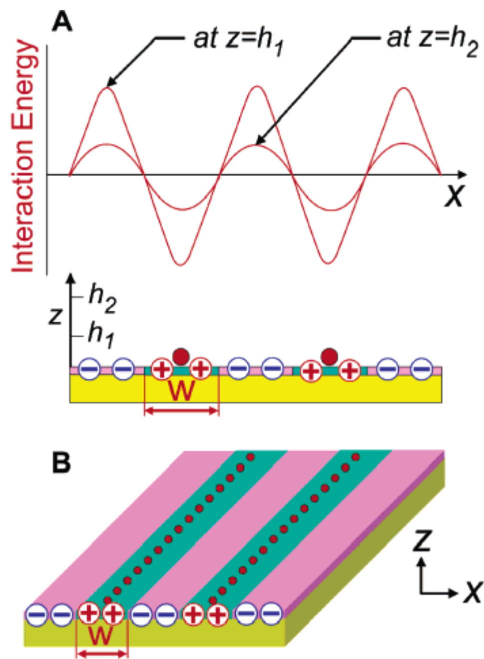

Figure 8.1 [78] Illustration of the concept of electrostatic funneling for presice placement of nanoparticles. (a) Schemic of the interaction energy when a negatively charged nanoparticle approaching to the surface functionalized by possively and negatively charged molecules from SAMs. (b) Placement of nanoparticles at the center of the postively charged line where the interaction energy is minimum.

8.3 Process of electrostatic funneling for precise nanoparticles placement

A guiding structure with alternative lines of copper and silicon oxide was used as a starting substrate as shown in Figure 8.1. A process flow from forming the SAMs to positioning the nanoparticles is illustrated in Figure 8.2.

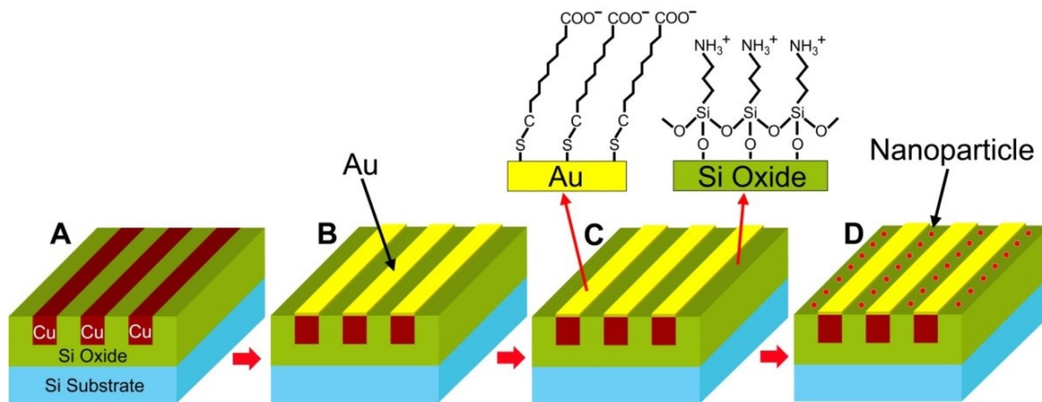

Figure 8.2 [78] Illustration of the process flow of electrostatic funneling. (a) Guiding structure with alternative copper lines (brown) and silicon oxide on a 200 mm Si wafer. (b) Electroless plating of gold on copper lines. (c) Selectively formation of two different SMAs layer on gold and silicon oxide surfaces. SMAs formed on gold and silicon oxide surface are MHA (–COOH; –COO–) and APTES (–NH2; –NH3+), respectively. These SAMs provide the positive charges and negative charges on gold and silicon oxide surfaces, respectively, in an aqueous solution. (d) Immersion of the guiding structure to gold colloidal solution where gold nanoparticles are negatively charged.

The guiding structure was fabricated with damascene technology [79] on a 200 mm silicon wafer. The copper and silicon line width is 120 nm and 80 nm, respectively. Due to the planerization procees by chemical-mechanical polishing (CMP) [79], the guiding structure has a very flate surface with a roughness around 1 to 2 nm scanned by atomic force microsope (AFM). The high difference between copper and silicon lines is 5

nm. For the ease of later process, the wafter was cut into a smaller sample with size of 2 cm x 2 cm. Before carrying any process for the sample, it was carefully cleaned in a aceton sonication bath and put in the UV-O3 cleaner for 30 minutes to remove any organic residual on the sample surface. Immedally after cleaning, sample was immersed in a 1% citric acid solution for 15 minutes to remove the copper oxides and rinse with DI water and dried by blowing with a stream of nitrogen.

Electroless plating of gold on copper line surface was first carried by immersing the sample into a electroless plating solution (Alfa Aesar, composed mainly by $KAu(CN)_2$, NH_4OH and water) at 65 C^0 for 45 seconds. Around 15 nm of gold layer will then selectively coated on copper lines. Samples was rinsed with pure ethanol to remove the plating solution and followed with DI water rinsing and nitogen blown dry. Gold surface is preferable for the formation of MHA and will be disscussed latter.

On the surface of silicon oxide, SAMs of 3-aminopropyltriethoxysilane (APTES, $(C_2H_5O)_3$-Si-$(CH_2)_3$-NH_2; Sigma Aldrich) was selectively formed to provide negative charge [80, 81]. Sample was immersed into a 5 mM of APTES solution in chloroform for 30 minutes at room temperature then followed by isopropanol rinsing to remove the solution and blown dried with nitrogen. After the APTS SAMs formed, the functional group NH_2 can be disassociated to $NH3^+$ in an aqueous solution as shown in Figure 8.2 (c). This provides the positive charge on silicon oxide surface and generates the attraction force for the nanoparticles attachment. Similarly, on gold surface, SAMs of 16-mercaptohexadecanoic acid (MHA, HS-$(CH_2)_{15}$-COOH; Sigma Aldrich) was selectively formed by immersing the sample into a 5 mM MHA solution in ethanol for 3 hours at room temperature, followed by rinsing in a 1% solution of HCl in ethanol for 15 seconds. At last, sample was rinsed with pure ethanol to remove all the solution and dried by blowing nitrogen. The MHA functional group COOH will be disassociated to COO^- in an aqueous solution thus providing the negative charge on gold surface to repel negatively charged nanoparticle.

After SAMs formed, sample was then immersed into a gold colloidal solution containing negatively charged gold nanoparticles with a diameter of ~20 nm (Ted Pella Inc.) for 30 minutes at 4 °C. Then the sample was rinsed with methanol and dried by blowing in a stream of nitrogen. Gold nanoparticles were guided to attache in the center of silicon oxide as shown in Figure 8.2 (d).

8.4 Precise nanoparticles placement in various guiding structures

20 nm gold nanoparticles precisely aligned along the center of the silicon oxide lines in our guiding structure were observed under FE-SEM as shown in Figure 8.3. It can be clear seen that gold nanoparticles were only attached on the silicon oxide but not in the gold lines due to the repulsion charges on the surface of gold lines. It was also found that the separation between nanoparticles is roughly the same. This is due to the same charge from the gold nanoparticle repel with each other.

The degree of the precision for the guided nanoparticles placement has been demonstrated in Figure 8.4 to give a quantitative understanding. The deviation of each nanoparticle from the center of the silicon oxide line was measured for a total of 217 nanoparticles. A standard deviation of 8.2 nm is obtained from the calculation. Compared with the size of nanoparticle which is 20 nm, it is about 3 times smaller.

The evenly dispersed nanoparticles along silicon oxide line were observed so we measured the separation between each nanoparticle. A mean distance from center of the nanoparticle to the adjacent one is around 50 nm. This regular separation raised from the negative charge of etch particle with similar size (< 10% variation) [82] and shape resulting in similar repelling force between etch others.

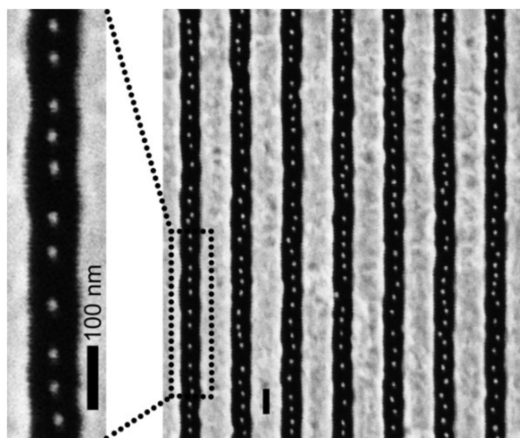

Figure 8.3 [78] FE-SEM images for nanoparticles (bright dots) aligned along the center of silicon oxide lines (dark bands). The bright bands alternating with silicon oxide band are gold lines.

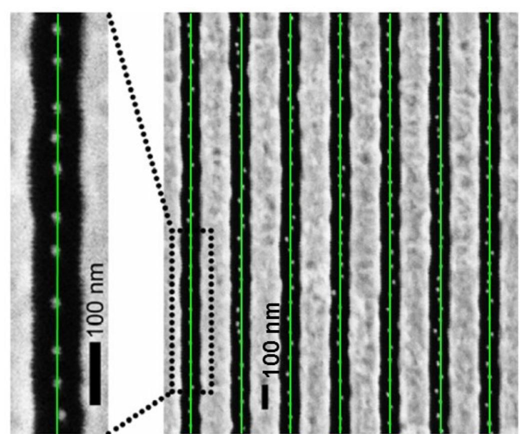

Figure 8.4 [78] Standard deviation of the nanoparticle placement. Green line is drawn arbitrary at the center of silicon oxide.

The method for electrostatically guiding the placement of nanoparticles can be applied to various geometries of the guiding structure. As compared with one dimensional alignment of nanoparticles above, it can also be applied to have other dimensionless placement, which is shown in Figure 6.5. A gold substrate with square pattern arrays on top of silicon oxide was prepared as the 0 dimensional guiding structures. It was prepared by the same procedure as the 1 dimensional guiding structure. Open circular pattern arrays were defined by e-beam lithography with diameter of 130 nm. SAMs of

APTS and MHA were selectively formed on the surface of gold and silicon oxide, respectively, using same process as used for 1 dimensional guiding structure described above. From Figure 6.5, only one 20 nm gold nanoparticle was placed in the center of each silicon oxide pattern. This is because that once the circler pattern is occupied, the repelling force from that nanoparticle repels other nanoparticles to get in. As a result, through the electrostatic funneling, we have the ability to control the placement of single particle on a desired location where is defined by the guiding structure.

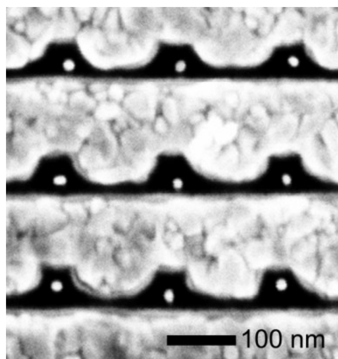

Figure 8.5 [78] FE-SEM images for nanoparticles placed in 0 dimension guiding structure. Bright area is gold and black is oxide pattern. Only individual Au nanoparticle (20nm) was placed inside the oxide pattern.

8.5 Interaction between charged surface and nanoparticles in aqueous solution

The electrostatic funneling effect is a result of the interaction between charged surface of substrate and charged nanoparticles. To get a quantitative understanding of the mechanism, interaction force from different charged surfaces affecting nanoparticles will be interpreted and calculated.

When our sample immersed in the gold colloidal solution, electric double layers [83] formed on all charged surfaces in this aqueous solution. The concept of electric double layer is illustrated in Figure 8.6. When a charged surface immersed in the solution, the final surface charge is balanced by a region of equal counterions with

opposite charges. Within this region, the first layer next to the surface is so called *Stern* or *Helmholtz* layer where some of the ions can bound to the surface. The second layer where counterions from atmosphere get close to the surface by repaid thermal motion is known as *electric diffuse layer*. The double layer is formed in order to neutralize the charged surface and, in turn, causes an electrokinetic potential between the surface and any point in the mass of the suspending liquid because of the rearrangement of the ions in the solution. The voltage difference that is set up is called electrostatic surface potential. With the surface potential obtained, the attractive and repulsive force between charged surface and nanoparticles can be calculated.

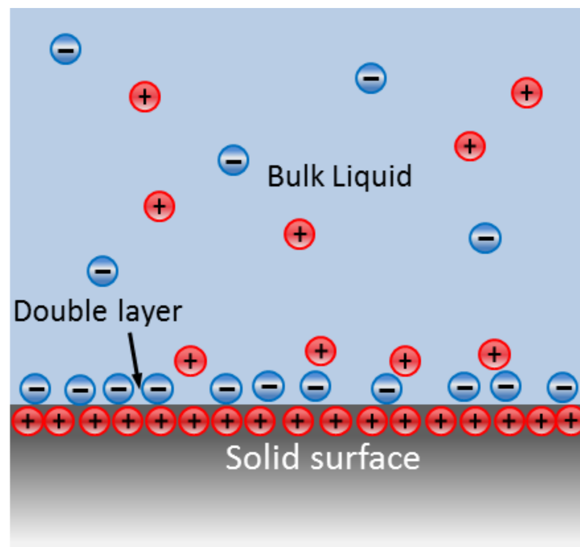

Figure 8.6 Schematic of electrical double layer

The electrostatic surface potential $\psi(\vec{r})$ can be calculated by numerically solving the nonlinear Poisson-Boltzmann equation [83, 84] :

$$\nabla^2\psi(\vec{r}) = -\frac{e}{\varepsilon_r\varepsilon_0}\sum_i Z_r\rho_{0i}exp(-Z_ie\psi(\vec{r})/kT)$$

where e is the unit charge of an electron, ε_r is the dielectric constant of water, ε_0 is the permittivity of free space, z_i is the valency of ion species i, ρ_0 is the concentration of ion species i in the bulk solution, k is the Boltzmann constant, and T is the absolute temperature.

With the obtained surface potential $\psi(\vec{r})$, the force $\vec{F}\ (\vec{R})$ which was exerted on a nanoparticle migrating to the charged surface of the guiding structure can be calculated through [85, 86]:

$$\vec{F}(\vec{R}) = \iint \left\{ \left[kT \sum_i (\rho_i - \rho_{0i}) \right] I.\hat{n} + \left[\frac{\varepsilon_0 \varepsilon_r}{2} \left| \vec{E} \right|^2 I.\hat{n} - \varepsilon_0 \varepsilon_r (\vec{E}.\hat{n}) \vec{E} \right] \right\} dS$$

with $\rho_i = \rho_{0i} exp(-Z_i e \psi(\vec{r})/kT)$ and $\vec{E} = -\vec{\nabla}\psi(\vec{r})$. This force equation is written in a form that gives the physical meaning for first term and second term as the result of osmotic pressure and electrostatic stress (Max well stress), respectively. $\vec{R}$ is the position of the nanoparticle above the charged surface (the vector origin was defined at the center of the oxide pattern).ρ_i is the concentration of ion species i, $\vec{E}$ is the electric field, I is the unite tensor, and $\hat{n}$ is the unite vector pointing normal to the surface S enclosing the nanoparticle at $\vec{R}$.

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Biographical Information

Liang-Chieh Ma was born in Pingjun, Taiwan, on 11th July 1975. He received his Bachelor's degree in Materials Science and Engineering from the Feng Chia University in 1998. He graduated his M.S. in Materials Science and Engineering from the Western Michigan University in 2002.