MEMBRANE TRANSFER OF CRYSTALLINE SILICON THIN FILM SOLAR CELLS

by

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Dedication

To my beloved grandfather

Acknowledgements

"Remember how far you've come, not just how far you have to go.

You are not where you want to be, but neither are you where you used be"

It is humbling to acknowledge those who have helped me through this arduous yet fascinating journey. I am indebted to so many for encouragement and support when it was much needed.

I would like to extend my sincere thanks to my advisor Dr. Weidong Zhou, for his guidance, encouragement and being patient with me all through the years and also for the opportunity to work and perform research in the group. You made me realize that the building blocks are all there, it's just that one has to pick them up and use them to his advantage. I would like to thank Dr. Donald Butler for your helpful insights and Dr. Fuqiang Liu for serving on my committee. I gratefully acknowledge Dr. Zhenqiang Ma at University of Wisconsin – Madison and Jung-Hun Seo for helping with the diffusion.

I am very thankful and would like to extend my sincere thanks to Arvinder Singh Chadha. At a time when I had little encouragement and little knowledge your support, encouragement and questioning has helped me push through. There is a great deal I have learnt from you, from a research perspective and on a personal level. Thank you for having my back at all times. There were times when I was annoyed by the constant questioning, but now I have come to realize their importance. The way you approach any problem is remarkable (that includes you math calculations). It was a pleasure working with you.

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Abstract

MEMBRANE TRANSFER OF THIN FILM CRYSTALLINE SILICON SOLAR CELLS

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Silicon has been dominating the solar industry for many years and has been touted as the gold standard of the photovoltaic world. The factors for its dominance: government subsidies and ease of processing. Silicon holds close to 90% of the market share in the material being used for solar cell production. Of which 14% belongs to single-crystalline Silicon. Although 24% efficient bulk crystalline solar cells have been reported, the industry has been looking for thin film alternatives to reduce the cost of production. Moreover with the new avenues like flexible consumer electronics opening up, there is a need to introduce the flexibility into the solar cells. Thin film films make up for their inefficiency keeping their mechanical properties intact by incorporating Anti-reflective schemes such as surface texturing, textured back reflectors and low reflective surfaces.

This thesis investigates the possibility of using thin film crystalline Silicon for fabricating solar cells and has demonstrated a low cost and energy efficient way for fabricating 2μm thick single crystalline Silicon solar cells with an efficiency of 0.8% and fill factor of 35%.

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Chapter 1

Introduction

1.1 Growing Energy Needs

Growing energy needs and the recent cognizance of eventual fossil fuel shortages along with the evident effects of global warming have created an increasing need for clean and renewable energy sources. Wind, nuclear, hydroelectric, geothermal, biomass and solar are the prominent renewable energy sources. Wind, Hydroelectric and geothermal are geography specific and have been adopted into grid system where ever these sources are available in abundance. Nuclear energy has been developed over a period of time but has not been a major source of power generation due the various reasons such as lack of efficient ways to dispose the radioactive waste, large requirement for security because of growing threat of terrorism. So, if there is one energy source which is not geography specific, abundant and does not amplify the effect of global warming- it is solar energy. Energy generation from sunlight. Figure 1.1 Energy consumption in the United states over the years and a forecast. Data taken from[1]shows the energy consumption in the United States over the years.

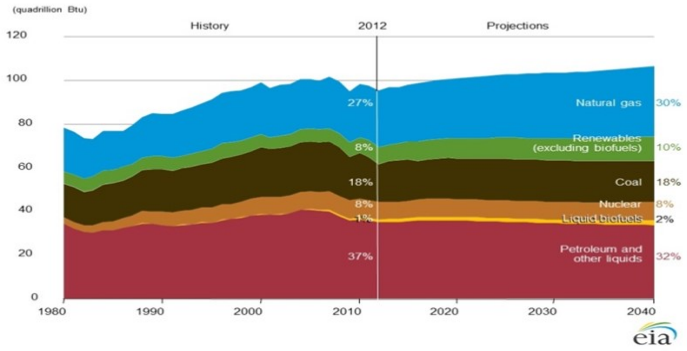

Figure 1.1 Energy consumption in the United states over the years and a forecast. Data taken from[1]

From the above figure it is evident that despite the availability of the renewable sources of energy, in the year of 2013 renewable energy sources amount to only 8% of the net energy consumption[1]. Our power needs have been increasing at a steady rate over the past 33 years, and this trend is not likely to change any time soon. We are converging at a point in time where the use of fossil fuels has to decrease drastically and the contribution of renewable sources of energy must increase rapidly. For this to happen the economics of renewable sources have to be examined closely.

Earth receives around $4x10^{24}$J of energy to the earth's surface per year. The world energy consumption is $7.56x10^{21}$J[2] meaning that solar energy alone can cover the needs the basic energy needs of the world population. Thus solar energy is a good alternative source of energy. But for solar energy to compete economically with other commercially used sources of energy the costs of module production must be reduced to 1USD/Watt with efficiencies above 15% [3].

1.2 State of the Art Bulk Silicon Solar Cell Technologies

Bulk Silicon solar cells have been the workhorse of the solar cell industry for a long time. Most bulk solar cells have high conversion efficiency and the ratio of electrical power output to solar power is about 10-15%. Highest efficiency of 24.4% was demonstrated by [4]. The cell was 250μm thick, with thermally grown oxide on the top for passivation and MgF_2/ZnS was used as an anti-reflective coating. Figure 1.2 is the schematic of the bulk silicon solar cell with 24.4% efficiency

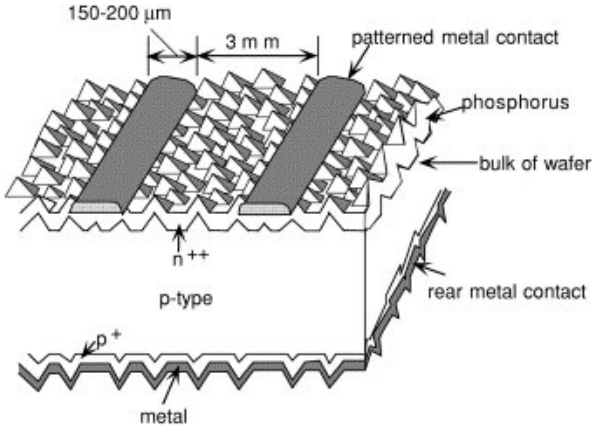

Figure 1.2 is the schematic of the bulk silicon solar cell with 24.4% efficiency

The second most efficient bulk solar cell demonstrated had an efficiency of 22%[5]. The fabricated cell was 330µm with rear oxide passivation, front side texturing and an Alluminum back reflector. The measured fill factor of the cell was 80.9%. Figure 1.3 schematic of 330µm bulk solar cell with 22% efficiency[5]

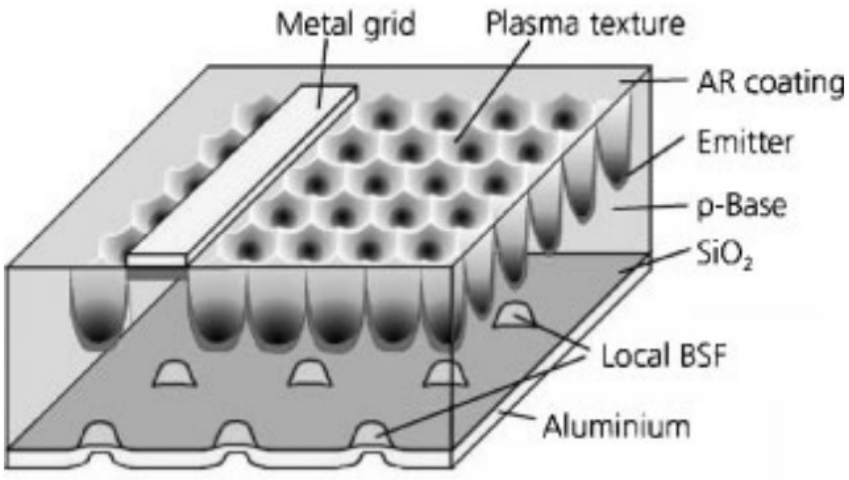

Figure 1.3 schematic of 330µm bulk solar cell with 22% efficiency[5]

Coming in third with an efficiency of 21% [6]. The cell was 43µm thick with low doped front diffusion and random textured pyramids. Figure 1.4 schematic of the 43µm cell with 21% efficiency.

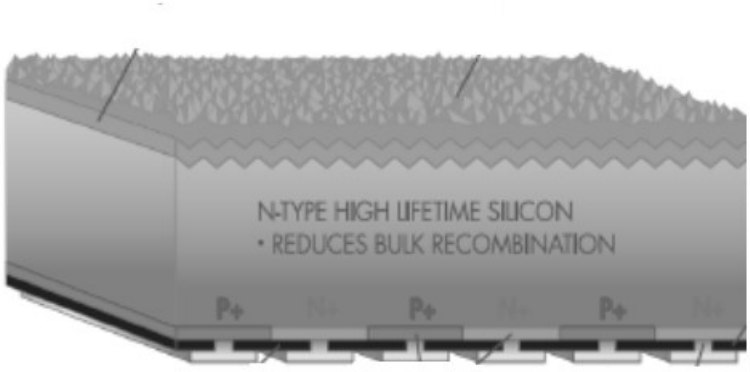

Figure 1.4 schematic of the 43μm cell with 21% efficiency

Although these cells are highly efficient, their cost of manufacturing is high and growing and sawing these wafers leads to a lot of material wastage. These cells are also application limited due to their rugged nature and have very high bulk carrier recombination. The solution: Thin film solar cells. With advantages like low cost/watt ratio, mature fabrication technologies and low manufacturing costs, thin film solar cells are a suitable alternative for Bulk Silicon solar cells.

1.3 State of the Art Technologies for Thin Film Solar Cells

One of the promising ways to achieve commercialization of solar energy is thin-film crystalline Silicon. With advantages of market dominance, non-toxicity, abundance, stability, potential for high efficiency crystalline silicon solar cells have the ability to share the research and infrastructure costs with the integrated circuit industry. Thin film technologies reduce the amount of Silicon used, thus reducing the cost per watt of power output.

In the present situation half of the cost of a finished module is due to the material itself, and around half of the silicon in a Czocharlski process is lost to saw dust. Therefore the potential of using a material which does not require dicing is substantial. There are diverse range of ways to achieve thin-film Silicon cells. However, all the techniques

require deposition or growth on a native or foreign substrate. This step can be avoided by using lift-off techniques before or after cell fabrication.

Silicon can be deposited on to a native substrate from the vapour or liquid phase. The main techniques are chemical vapour deposition (CVD) and liquid phase epitaxy (LPE). CVD process must be optimized for high chemical yields because it can occur on the walls of the reactor. LPE on the other hand only occurs on the exposed surface of the silicon and not on the masked regions. CVD is the most commercially used technique whereas LPE is used for specialized applications III-V deposition. There are other techniques which can be used for deposition such as ion-assisted deposition and sputtering. Open circuit voltage (V_{oc}) is a testament to the quality of the material since it measures recombination rates, including bulk, grain boundary and surface recombinations. Hence, deposition step is mostly followed by recrystallization. There are two types of recrystallization techniques 1) high-temperature recrystallization technique such as zone melting recrystallization and 2) low-temperature recrystallization which includes laser crystallization, solid-phase crystallization (SPC) and rapid thermal processing (RTP). Although an additional step is added to the process recrystallization allows the use low quality, low cost Silicon deposition.

1.2.1 Ribbon Growth

Ribbon growth is a propitious way for thin-film Silicon solar cells. It involves pulling a thin sheet of Silicon from a molten stockpile. Sheet solidification occurs at the meniscus and the geometry of the meniscus and the pull rate determine the rate and direction of cooling. Layers as thin as 5μm have been grown using this technique [7]. A maximum efficiency of 17.8% was demonstrated in Silicon ribbon solar cells[8]

The future of electronics is in the flexibility and the ability to integrate with unusual structures like the human arm, dome of a structure or around a satellite. The

possibilities are numerous. Another problem bulk Silicon poses is the lack of flexibility. In thin form any material is flexible, because the linear strains decrease with temperature [5]. By thinning down Silicon to few microns, while reducing the material cost we are also introducing flexibility, widening the range of applications and areas where solar cells can be used.

1.2.2 Growth on Low-Cost Silicon

Advantages such as thermal stability and thermal c-efficient matching make low-cost Silicon a profitable option. There are two main approaches to growing Silicon on low-cost Silicon. One is to grow an epitaxial layer on ribbon Silicon or a mechanical grade Silicon. Another approach is to use a barrier layer to prevent diffusion of impurities from substrate to an active layer. Moderately doped active layers can be grown on heavily doped substrates. A 20μm cell with efficiency close to 14% was demonstrated using this technique [9].

Multi-crystalline Silicon can also be used for depositing Silicon on Silicon. Cost of multi-crystalline Silicon is too high, so mechanical grade Silicon can be used a substrate. By having a diffusion barrier between the active layer and the substrate can reduce diffusion of impurities from substrate into the active layer. By doping the active layer with Boron the recombination rates can be reduced. Another viable option for a diffusion barrier is the use of Porous Silicon with in a additional advantage of acting like a rear reflector which otherwise is difficult in Silicon substrates.

Thin film Silicon layers can be detached from the substrate, which can be reused later. This process has a high potential due to the fact that the substrate can be recycled and there is no need to compromise on the quality of the Silicon and also inherent material defects and film stresses are absent.

1.2.3 Amorphous Silicon Solar Cells

When Silicon is deposited at low temperature by PECVD using Silane (SiH_4) as the Silicon source, amorphous Silicon is formed. One of the disadvantages of using amorphous Silicon is cell degradation under exposure to sunlight. To overcome the poor material quality and low carrier mobility an intrinsic layer is inserted between p- and n-layer [10]. Low carrier mobility combined with thinner active regions leads to insufficient conductivity to allow flow of carriers. This is overcome by using transparent conducting oxide layer such as SnO_2.

1.2.4 Thin Film Poly Crystalline Silicon on Glass

This 'crystalline silicon on glass' approach combines the well-established strengths of bulk silicon solar cell structure such as stability, durability, abundance and non-toxicity with the advantage of thin-film technology such as reduced material costs and large area monolithic construction. A typical fabrication process flow to construct such a cell would be: Doped Silicon is deposited onto a textured glass using PECVD. Polycrystalline material is formed through a crystallization step. 10.4% efficiency with a fill factor of 72% was developed using the above approach [11]. The structure of the cell is shown in Figure 1.5.

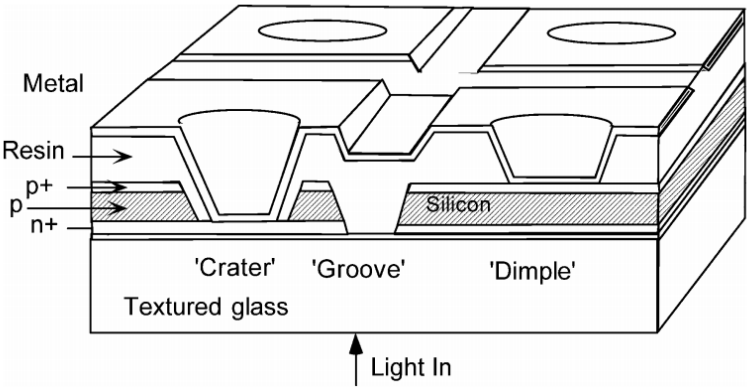

Figure 1.5: Key features of poly crystalline Silicon on glass

Table 1 Non-Silicon Thin Film Technologies with Record Efficiencies

Cell	Area(cm^2)	Fill factor (%)	Efficiency (%)
GaAs [12]	1	82.5	**24.4**
$CuInS_2$ [13]	0.511	76.6	11.4
$CuInSe_2$ [14]	-	72.6	15.4
CdTe[15]	4	75.5	16.5

Non-Silicon technologies have high optical absorption coefficients, tailorable bandgaps and hence high cell efficiencies. However, the devices are unstable, and lack large area scalability.

Table 2 Silicon Thin Film Technologies with Record Efficiencies.

a-Si/CIGS[16]	2.4	-	14.6
a-Si [16]	1	74.1	12.7
c-Si (40 μm)	4.017	78.2	**16**

Table 2 Silicon Thin Film Technologies with Record Efficiencies. Crystalline Silicon thin film solar cells have long lifetime. The large area scalability is simple and their integration with amorphous Silicon and polymer solar cells is easier.

One can clearly conclude that there is a trade-off between cost/watt and performance of the solar cell. Hence, depending on the application a suitable structure can be selected.

Crystalline Silicon solar cells have moderate efficiencies with well established, simple and low-cost fabrication techniques. A practical solar cell has to be low cost, high

efficiency, flexible and must be large area scalable. One of the novel methods designed is transfer printing as demonstrated in [17]

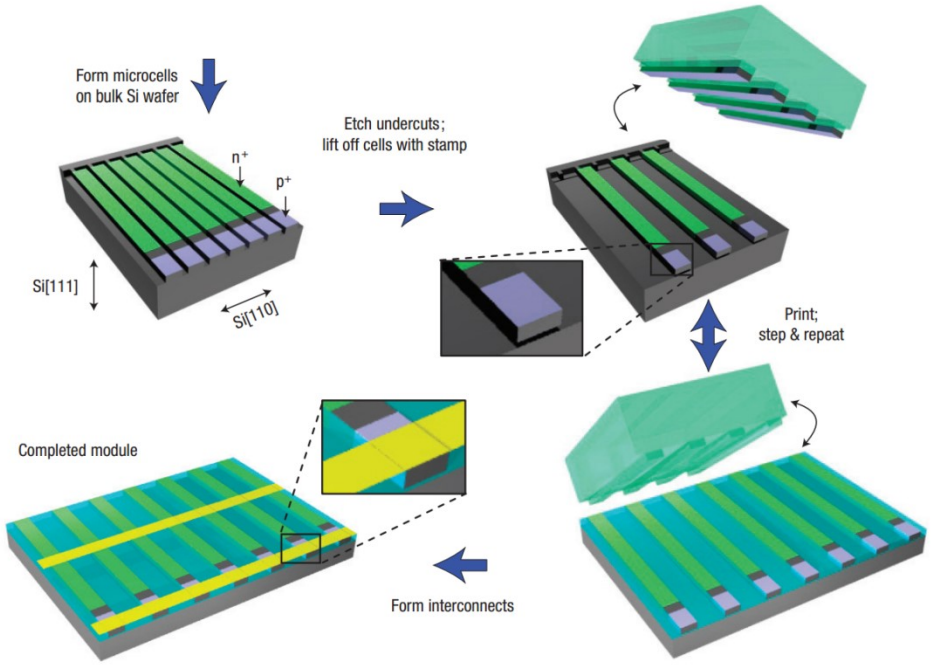

Figure 1.6 fabrication flow for transfer printed crystalline Silicon thin film solar cells.

The above designed process is a low-cost method for crystalline Silicon transfer on to rigid and flexible substrates. With added advantages like reusable materials, room temperature processing. It is easier to incorporate Anti-reflective schemes and back-surface field structures. One of the limitations of the process is that the yield is very low and alignment of structures is very critical.

1.4 Aim of the Thesis

The aim of the thesis is to design, fabricate and characterize thin film crystalline Silicon solar cells

1.5 Overview of the Thesis

Chapter 2 talks about the theory behind Solar cells. The chapter concludes with a discussion about the basic concepts of solar cells like junction design, front and back

contact design, Series resistance and shunt resistance effects and finally schottky and Ohmic contacts.

Chapter 3 summarizes the solar cell structures that were simulated using Medici. This chapter discusses about the simulated results and how diode parameters like emitter doping concentration and junction depth were optimized to achieve maximum efficiency for a given thickness. Simulations were run both for 2μm and 10μm thick solar cells.

Chapter 4 presents the process for the fabrication of the cells. Initially talking about the optimization of photoresist thickness and then moving on to dry etching recipes their etch rates and how problem of sidewall roughness was dealt with. Then the evaporation of finger contacts

Chapter 5 presents the results, and concludes with a discussion on how to improve the efficiency of the solar cell using different enhancement schemes

Chapter 2

Theory of Solar Cells

2.1 Introduction

In this chapter I shall discuss about the physics of solar cells. The chapter starts with introduction to semiconductors and moves on to talk about doping and PN junctions. At a later part of the chapter I shall discuss about solar cells, important parameters and parasitic effects of a solar cell.

2.2 Principles of Semiconductors

2.2.1 Semiconductors

A semiconductor is a material which exhibits the characteristics of a conductor or an insulator depending on chemical alterations or external conditions. They form a special category of materials because of their electrical, optical and material characteristics. Figure 2.1 The band diagram for metals, semiconductors and insulators

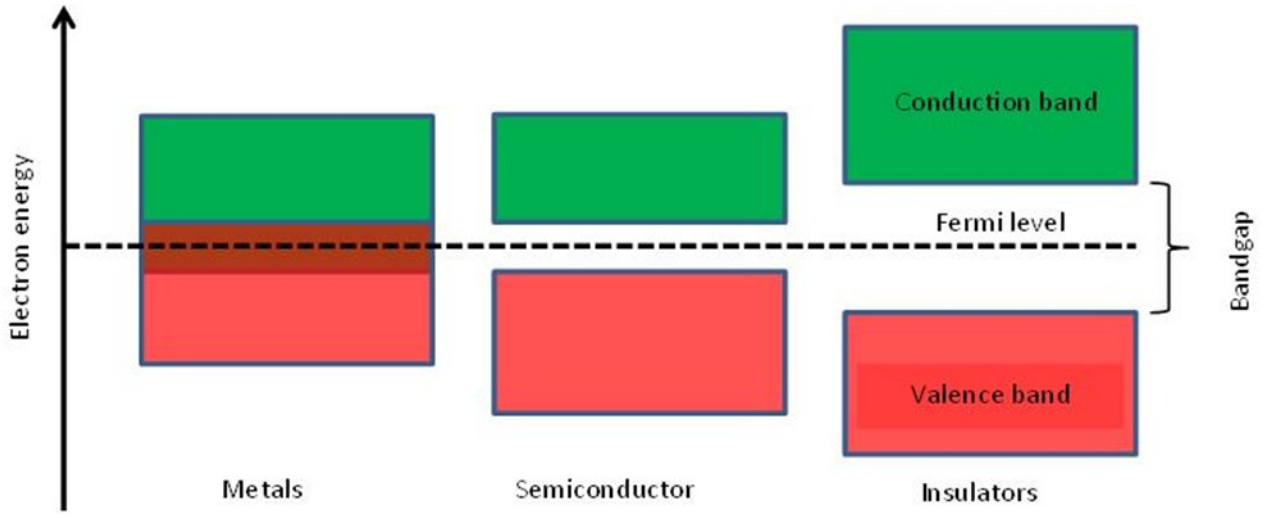

Figure 2.1 The band diagram for metals, semiconductors and insulators

2.2.2 Doping

In its purest form a semiconductor is intrinsic in nature. When certain impurities are incorporated in the semiconductor, its crystal structure is disturbed and starts to exhibit interesting features. This process is called doping. The impurities that are introduced, will have bonds of different strengths compared to that of the perfect crystal and hence will change the local distribution of the electron energy levels. There are two types of impurities: Donor impurity and acceptor impurity. When semiconductor doping leads to increased density of electrons compared to holes, it becomes donor type semiconductor and the process is called n-type doping. In case of Silicon which has four valence electrons, elements from group V such as Phosphorus (P) and Arsenic (As) which are pentavalent are used as donor impurities. When the introduced impurity increases the density of positive charges compared to negative charges, it becomes acceptor type and the process is called p-type doping. Trivalent, group III elements such as Boron (B) and Alluminium (Al) are used as acceptor impurities.

2.3 P-N Junction

On doping a semiconductor with p-type and n-type an interface is formed. The resulting interface is called p-n junction. Fig. 3 shows the schematic of a p-n junction. The junction is depleted of both electrons and holes. There is a tendency of the holes from the p-type to n-type region leaving behind an ionized acceptor. Similarly the electrons drift in the opposite direction leaving behind an ionized donor. The region that is hence formed, which comprises of the ions is known as the space charge region, as shown in the Figure 2.2.The presence of charges on the two extremes gives rise to a built-in potential and the voltage is given by

$$v_{bi} = \frac{KT}{q} * \ln(\frac{N_A N_D}{n_i^2}) \quad (1)$$

Equation 1 Built in potential [18]

The width of the space charge region is given by equation 2[18].

$$W = \frac{\sqrt{2\varepsilon(v_{bi}-v)*(N_A+N_D)}}{q*\sqrt{(N_A N_D)}} \qquad (2)$$

Where,

N_A is the acceptor impurity concentration on the p-side of the junction,

N_D is the donor impurity concentration on the n-side of the junction,

V is the applied voltage

K is the Boltzmann's constant

T is the temperature

n_i is the intrinsic carrier concentration

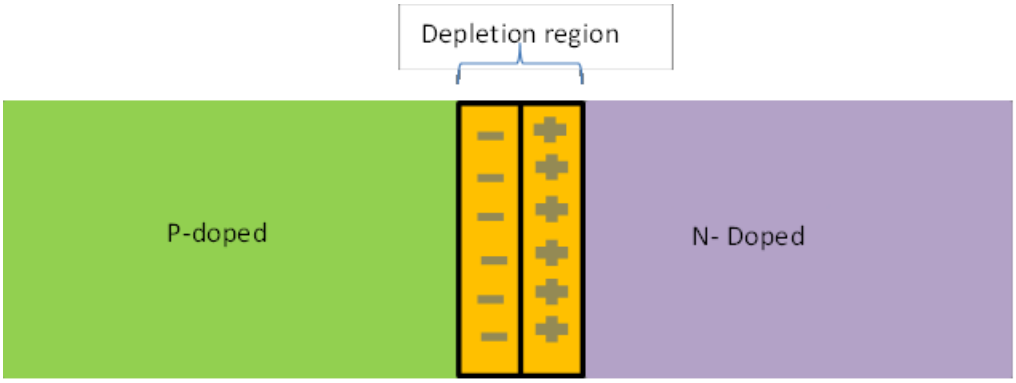

Figure 2.2 Schematic of a p-n junction

2.3.1 Biasing a P-N Junction

The p-n junction is biased by connecting it to the external power supply. It is forward biased when the p-region is connected to positive terminal of the supply and n-region is connected to the negative terminal. Under forward bias the electrons from the n-region and holes from the p-region gain sufficient energy to cross the low potential energy barrier. This results in a current flow across the junction. The current in the

forward bias is due to majority charge carriers and is called diffusion current. The forward bias current-voltage characteristics is as shown in Figure 2.3 The current-voltage characteristics of a p-n junction diode. When p-region is connected to the negative terminal and the n-region is connected to the positive terminal, the junction is said to be reverse biased. Under these conditions the majority carriers are attracted towards the power supply terminals and hence diffusion current becomes negligible. However due to thermal energy there is small presence of electron-hole pairs and hence a small leakage current is present under reverse bias. The current flowing across the junction is given by equation 3.

$$I = I_{sat} \exp\left(\left(\frac{qV}{kT}\right) - 1\right) \qquad (3)$$

Where,

I_{sat} = Saturation current

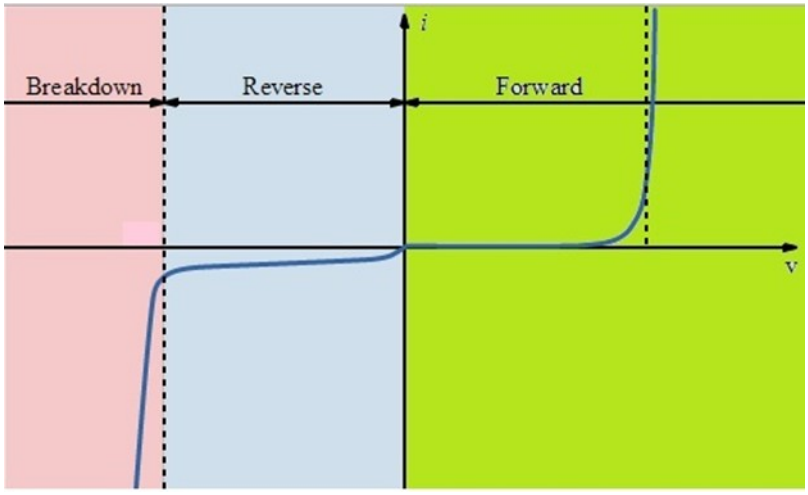

Figure 2.3 The current-voltage characteristics of a p-n junction diode

2.4 Solar Cells

Solar cells are devices made of p-type and n-type semiconductors that convert light energy into electrical energy. Each of the semiconductors has a different band gap which enables them to match different regions on the solar spectrum.

2.4.1 Solar Spectrum

The solar spectrum is well approximated by assuming the sun to be a perfect black body and that it obeys Planck's radiation law. The emitted solar spectrum is similar to the emission spectrum of black body at 6000 K, even though the sun's core reaches temperatures of 20,000,000 K. This is because most of the emitted radiation is absorbed by the Hydrogen ions near the surface of the sun and are the then heated to 6000K. The spectrum of available energy from the sun at the outer edge of the earth's atmosphere is known as air mass zero, AM0 spectrum and has a integrated power density of 1366.1 W/m^2. There are two spectra that are relevant to the earth's surface and are referred to as AM1.5G and AM1.5D. AM1.5G consists of both direct and diffusive radiation from the sun and has an integrated power density of 1000 W/m^2, this spectrum is relevant to for flat panel photovoltaics, while AM1.5D which consists of only direct radiation from the sun. It has a power density of 900 W/m^2 and is applicable to concentrator photovoltaics. Figure 2.4 AM0, AM1.5G, AM1.5D spectra[19, 20].

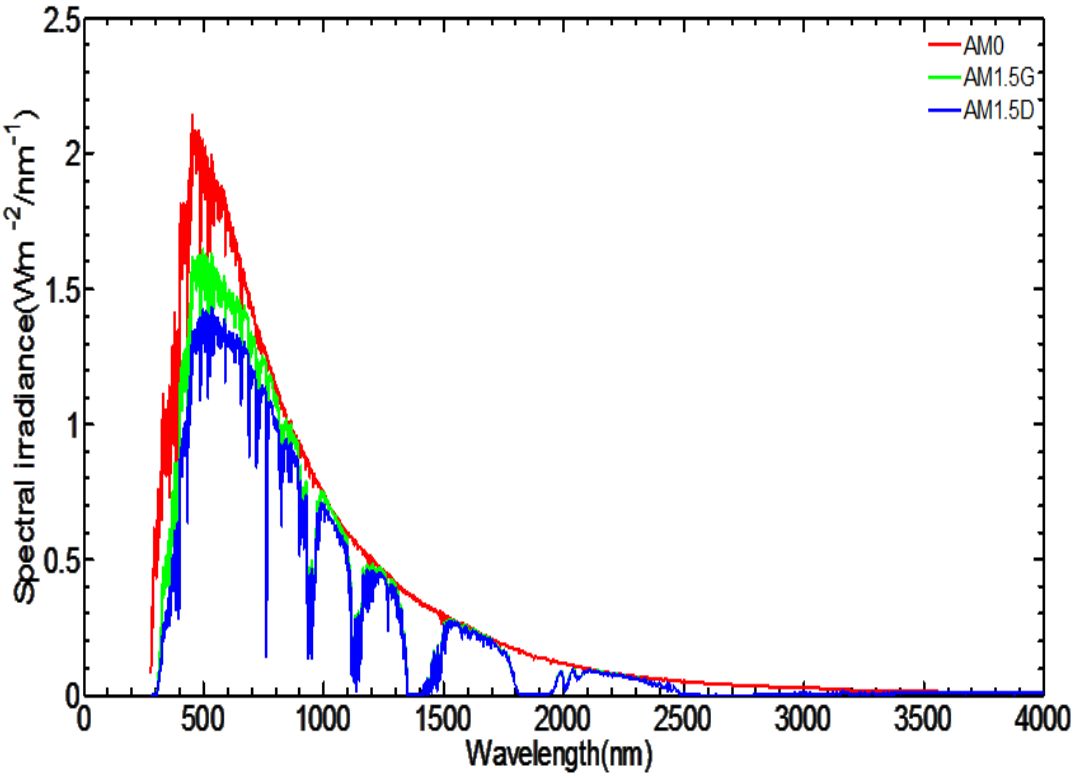

Figure 2.4 AM0, AM1.5G, AM1.5D spectra[19, 20]

The spectral response of the solar cell is similar to the quantum efficiency of the cell. Spectral response of the cell is given by the ratio of the current generated by the solar cell to the power incident on the solar cell, while quantum efficiency on the other hand is the ratio of the number of electrons output by the solar cell to the number of photons incident. Spectral response plays an important role because, it is the parameter measured from the solar cell. Quantum efficiency is determined from the spectral response by replacing the power of the light at a particular wavelength with the photon flux for that wavelength. The relationship between spectral response and quantum efficiency is given by equation 4.

$$Spectral\ response = (\frac{q\lambda}{hc}) * Quantum\ efficiency \qquad (4)$$

Where,

λ is the specific wavelength

h is Planck's constant

C is the speed of light

2.4.2 Working Principle of a Solar cell

When light is incident on the surface of a solar cell, the light of energy less than that of the band gap energy of the semiconductor layer is absorbed. Light consists of packet of photons, when these are absorbed they in turn generate what is known as an electron-hole pair (EHP). In the presence of an external field or when connected to an external circuit, generated carriers can be collected by placing at the extremities of the solar cell metal contact. The current thus generated is known as photocurrent.

2.4.3 Current-voltage Characteristics of a Solar Cell

Excited electrons in the p-n junction need not recombine to the valence and must be collected through an external circuit to obtain a photocurrent. The efficiency of the cell is determined by various limiting factors*.*

2.4.3.1 Photocurrent in Solar Cells.

Under illumination photocurrent is generated in a solar cell which is proportional to the incident spectrum and the cell's external quantum efficiency (EQE). EQE(E) is the probability that a photon with energy E will be absorbed by the solar cell and excite a valence electron into the conduction band that is then collected before recombining. The short circuit current density Jsc is related to the incident spectrum and the EQE by the equation 5. Figure 2.5 the current generation in a solar cell

$$J_{SC} = q \int b_s(E) * EQE(E) * dE \qquad (5)$$

Where,

b_S is the incident spectrum between E and E+dE

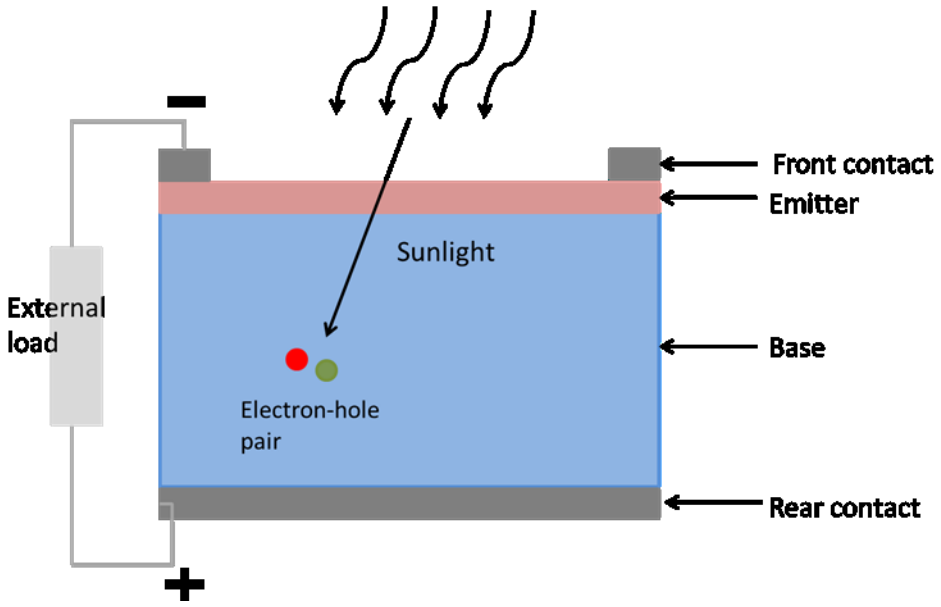

Figure 2.5 the current generation in a solar cell

2.4.3.2 Dark Current in a Solar Cell.

When a solar cell is forward biased, a potential develops between the front and the rear contacts. This potential difference creates a current, and is called the dark current (Jdark), which is the opposite direction of photocurrent. The dark current is given by the equation 6.

$$J_{dark} = J_O(exp^{\frac{qv}{k_b t}} - 1) \qquad (6)$$

Where,

J_o is a constant proportional to the total recombination in the device

The total current can be approximated as the sum of dark current and photocurrent and is given by equation 7.

$$J_{total} = J_{sc} - J_{dark} \quad (7)$$

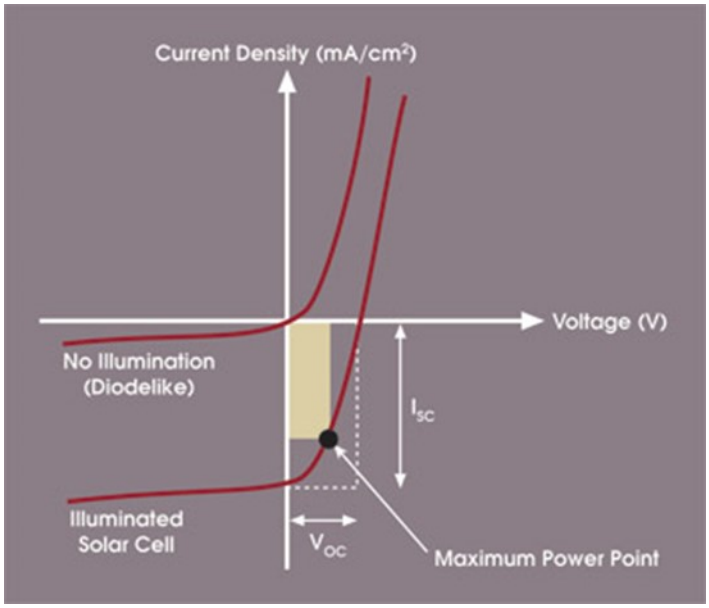

Figure 2.6 The IV characteristics of a solar cell under illumination and in dark [20]

2.4.4 Parameters of a Solar Cell

2.4.4.1 Short Circuit Current.

The current through the solar cell when the voltage across the solar cell is zero is called short-circuit current. Generation and collection of light-generated carriers are the main cause of short-circuit current. Under this condition, charges are free to travel through the circuit and there is no buildup of bias. The photogeneration assumes a maximum due to the absence of opposing diode current. The photocurrent is directly proportional to the intensity of the incident light, because EHPs produce minority carriers. Figure 2.7shows the carrier movement in short circuit mode.

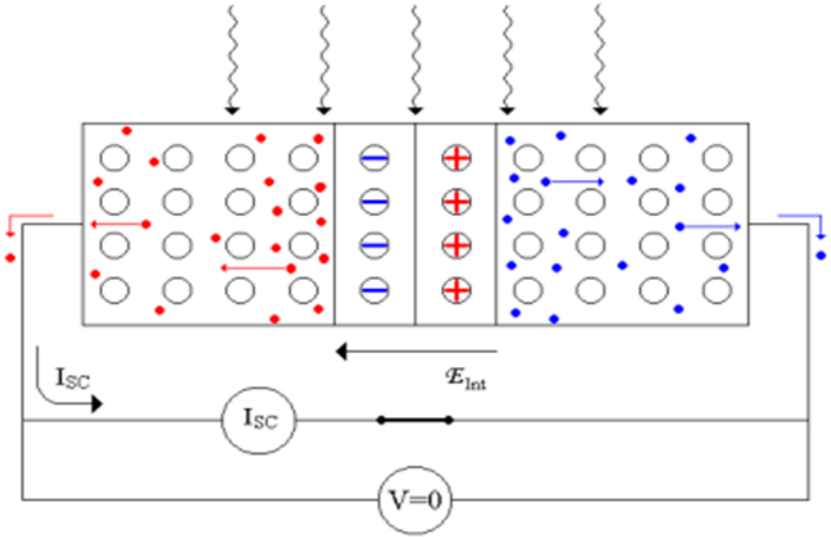

Figure 2.7 The cell under short circuit mode.

The equation for short-circuit can be approximated as:

$$J_{sc} = qG(L_n + L_p) \qquad (6)$$

Where,

G is the generation rate

L_n is the electron diffusion length

L_p is the hole diffusion length

2.4.4.2 Open Circuit Voltage.

The maximum voltage that occurs at the solar cell when there is zero current flowing through the device. Under open circuit conditions there is a charge buildup on each side of the device creating a diode current. Equilibrium is reached in the device when the diode current is equal to the photogeneration current. Figure 2.8 shows the device under open circuit condition.

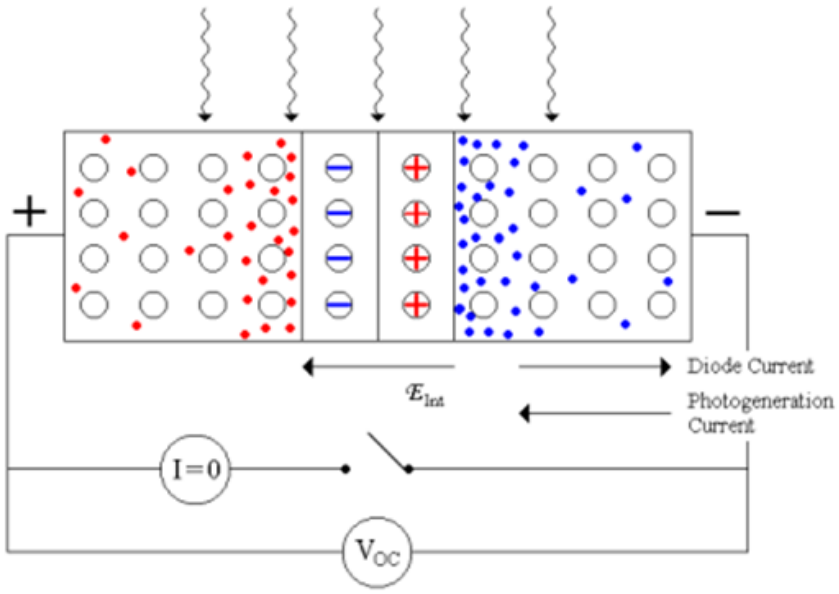

Figure 2.8 Open circuit condition of the device

The open circuit voltage (V_{oc}) can be determined from the carrier concentration of the device as given in equation 7 [10].

$$V_{oc} = \frac{KT}{q} * \ln\left[\frac{(N_A+\Delta n)\Delta n}{n_i^2}\right] \qquad (7)$$

2.4.4.3 Fill Factor.

Power output of the cell is the product of current and voltage. Quality of the cell is given by its fill factor (ff).Fill factor can be defined as the ratio of maximum power to the product of open circuit voltage and short circuit current and is expressed as

$$ff = \frac{I_M * V_M}{I_{SC} * V_{OC}} \qquad (8)$$

By eliminating the dependence on the area of the cell it can be defined as [18]

$$ff = \frac{J_M * V_M}{J_{SC} * V_{oc}} \qquad (9)$$

Where,

J_M and J_{SC} are normalized values of maximum current and I_{sc} with units as mA/cm^2

2.4.4.4 Efficiency.

The efficiency of the solar cell, η is defined as the power density delivered at operating point as a fraction of incident light power density Pin,

$$\eta = \frac{J_M * V_M}{P_{in}} \quad (10)$$

It can also be expressed in terms of Jsc, Voc and *ff* as,

$$\eta = \frac{J_{SC} * V_{oc} * ff}{P_{in}} \quad (11)$$

The standard test condition (STC) as discussed earlier is AM1.5 spectrum with an incident power density of 1000W/m^2.

2.4.5 Parasitic Resistance

In real solar cells there is power dissipation through the resistance of the contacts and through leakage currents around the sides of the device. These effects can be treated electrically equivalent to parasitic resistance in series R_s and in parallel R_{SH}. The equivalent circuit of a solar cell is given in Figure 2.9

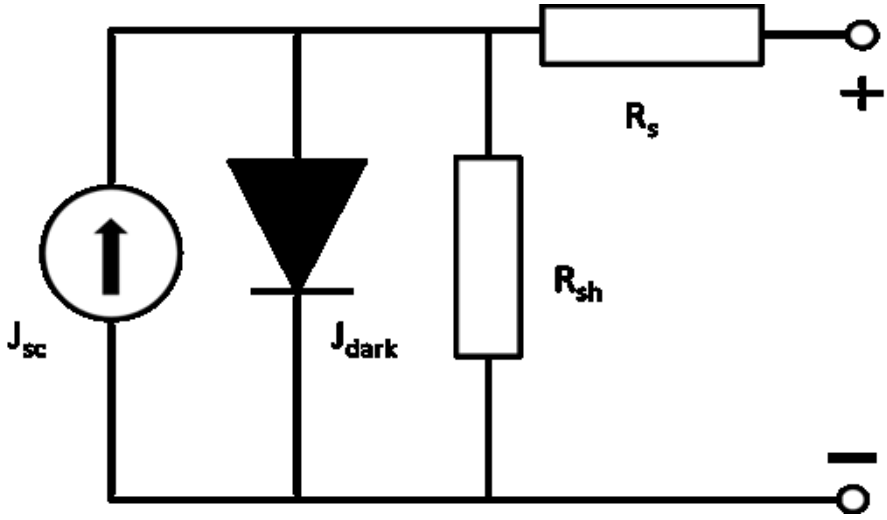

Figure 2.9 Equivalent circuit for a solar cell

Resistance of the cell material to the flow of current is the origin of series resistance, particularly from the top contacts and the device material. The main impact of this resistance is seen on the fill factor of the cell, it reduces with increasing magnitude of resistance, although high values may also reduce the short circuit current.

Figure 2.10 (a) shows the effect of series resistance on the current-voltage characteristics of a solar cell.

The leakage of current through the cell gives rise to parallel or shunt resistance (R_{SH}). Leakage occurs around the edges of the device and in between the contacts of different polarity. It causes major problem in poorly rectifying devices. Low shunt resistance causes power loss in the device, providing alternate paths for light generated current. This reduces the current flowing through the junction of the device and reduces the voltage from the cell.

Figure 2.10(b) shows the effect of shunt resistance on I-V characteristics. For an ideal device the series resistance will be very low and the shunt resistance will be as high as possible.

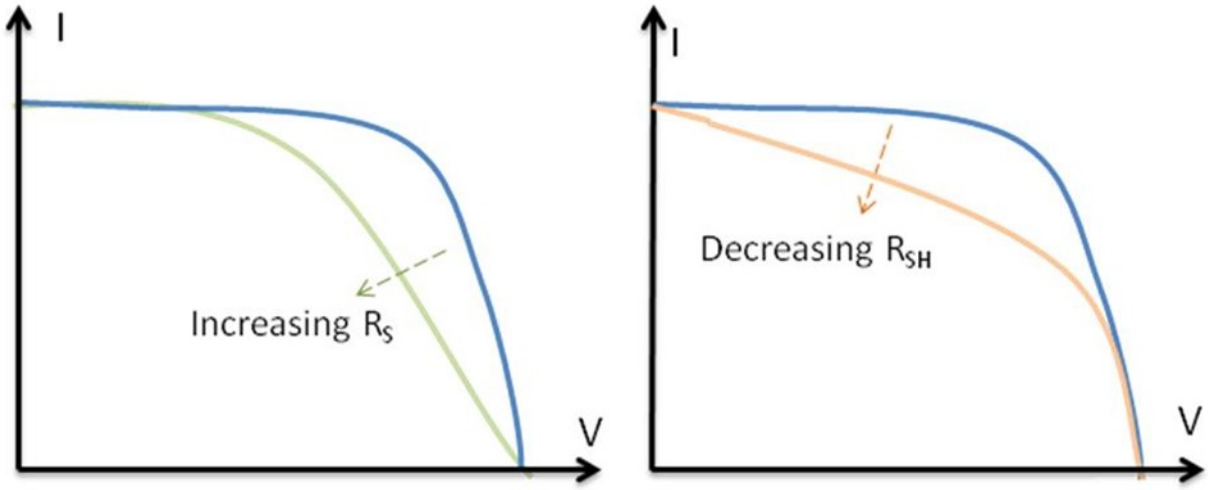

Figure 2.10 (a) effect of series resistance on the I-V characteristics, (b) effect of shunt resistance on the I-V characteristics of the cell [21]

Chapter 3

Simulation

3.1 Introduction

In this chapter I shall discuss about the features and advantages of *Medici,* the tool used for running device simulations. Simulated results for different thickness of the device layer and optimizing the thickness of the emitter region shall be discussed. Finally, finger contact design and optimized device design shall be presented.

3.2 Features of Medici

Medici is an industrial standard simulation tool that can be used to simulate the behavior of MOS, bipolar transistors and other semiconductor devices. It models the two dimensional (2D) distributions of potential and carrier concentrations in a device. It solves Poisson's equation and both the electron and hole current continuity equations to analyze devices such as diodes.

Medici uses a non-uniform triangular simulation grid, and can model arbitrary device geometries with planar and non-planar topographies. The user has the flexibility of adding additional nodes and elements where user specified quantities like potential and impurity concentrations vary by more than specified tolerance. Electrodes can be placed anywhere on the simulating structure. Tool also has the additional feature of automatic I-V curve tracing. The tool also features ray tracing to simulate transmission and reflection and refraction across interfaces. These conditions are solved using syntaxes for each parameter and a general set of program structure. The program starts off with grid generation, the region and profile settings for the devices, specifying contacts, specifying the parameters of the material used in the model, solving for a particular solution and then viewing the output. Medici also has an option of automatically refining the grid and eliminating unnecessary grid points.

After establishing a suitable grid, next necessary step would be to specify the nature, position and the parameters of the materials in the device. This is done using specific statements such as REGION AND PROFILE. In MEDICI the material properties can be automatically invoked by simply specifying the material. It has the added feature where material can be specified by the user. This can be done by mentioning the nature of material (Semiconductor, insulator etc...) under the REGION statement and specifying the corresponding material under the MATERIAL statement.

Medici has various physical models for recombination, photogeneration, absorption and lifetimes for accurate simulations. Boltzmann and Fermi-Dirac statistics are already incorporated in the program.

Medici is a 2D simulation tool that uses both Cartesian and Cylindrical co-ordinate systems. Simulations in the Cartesian system are done in X-Y plane and thus obtained results are assumed to be identical in the Z-plane.

The user specifies the input statements that are needed for the device simulation. Each input statement contains a keyword followed by the parameter list. This includes grid specification which uses the MESH statement. Materials are specified using REGION and PROFILE statements. ELECTRODE statement is used for defining the contacts and its properties are specified using CONTACT statement. Electrical and optical properties of Silicon are specified using the MATERIAL statement. PHOTOGEN specifies the light source. SOLVE is used to solve for a particular solution and the output can be viewed using PLOT statement. The entire program is written in a data file and the program is executed using the command medici <filename.inp>.

3.3 Input Data

In MEDICI simulations the user has to specify the key inputs namely- the structure of the mesh, material properties, type of physical model and a numerical

solution method for iterations. Simulations of the mesh were done in the Cartesian coordinate system. Shockley-Read-Hall(SRH) and Auger physical models were used for recombination statistics and the iterative method used was Newton-Raphsons's method.

Table 3 shows the input parameters for 10μm and 2μm Silicon solar cell simulations

Parameter	Specified value for 10 μm structure	Specified value for 2 μm structure
Thickness of emitter region	0.01-5μm	0.01μm-1 μm
Emitter doping concentration(N_D)	$5x10^{17}cm^{-3}$-$5x10^{19}cm^{-3}$	$5x10^{17}cm^{-3}$-$5x10^{19}cm^{-3}$
Base doping concentration(N_A)	$4.4x10^{16}cm^{-3}$	$4.4x10^{16}cm^{-3}$
Top electrode	ITO	ITO
Bottom electrode	Aluminum	Aluminum
Reflectivity of the back electrode	0.9	0.9
Thickness of the back surface fields	0.5 μm	-
Doping concentration of the back surface fields	$2x10^{19}cm^{-3}$	-

3.4 Simulation Results

3.4.1 External Light Source

The device structures used for simulations are shown in Table 3.1. The light source internally available in MEDICI is AM0 spectrum and is approximated by a blackbody at 5800K.

3.4.2 Simulated Results

Simulations were initially run by varying the junction depth and the doping concentration of the N-layer or the emitter (N_D) while keeping the doping concentration of the P-layer or the base (N_A).Shown in Figure 3.1 Efficiency as a function of junction depth for various values of ND for 2μm and 10μm devices .the variation in efficiency as a function of junction depth for the thin film solar cell without any Lambertian light trapping and back surface fields (BSF).

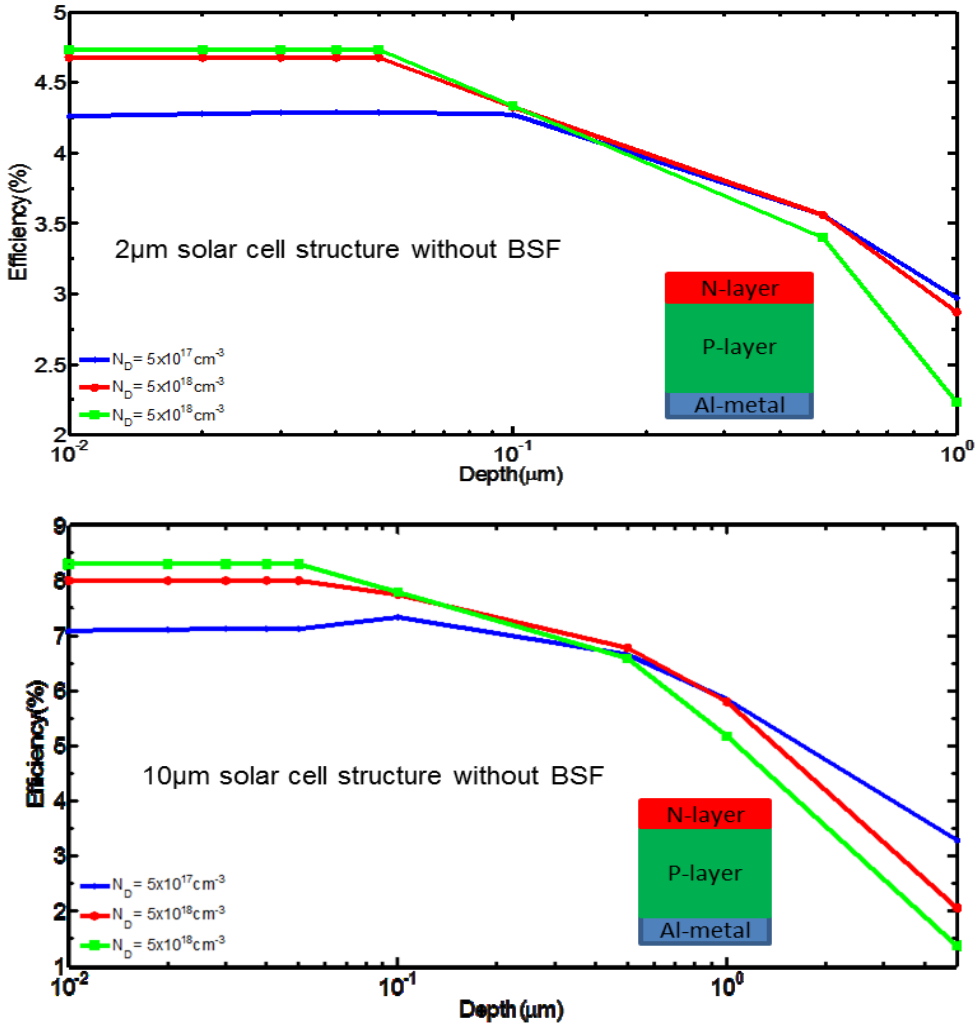

Figure 3.1 Efficiency as a function of junction depth for various values of N_D for 2μm and 10μm devices

Our preliminary simulations show a maximum of 4.7% and 8.4% efficiencies achievable from 2 μm and 10 μm c-Si thin films. Figure 3.2 shows that the efficiency increases to 8% and 10.8% when a 0.1 μm, 0.5 μm thick p+ doped (N_A = 10^{19} cm^{-3}) back surface field is introduced in the 2, 10 μm c-Si thin film cell. For all the cases simulated

the efficiency falls when the junction depth increases beyond 40 nm and is almost independent of the doping concentration.

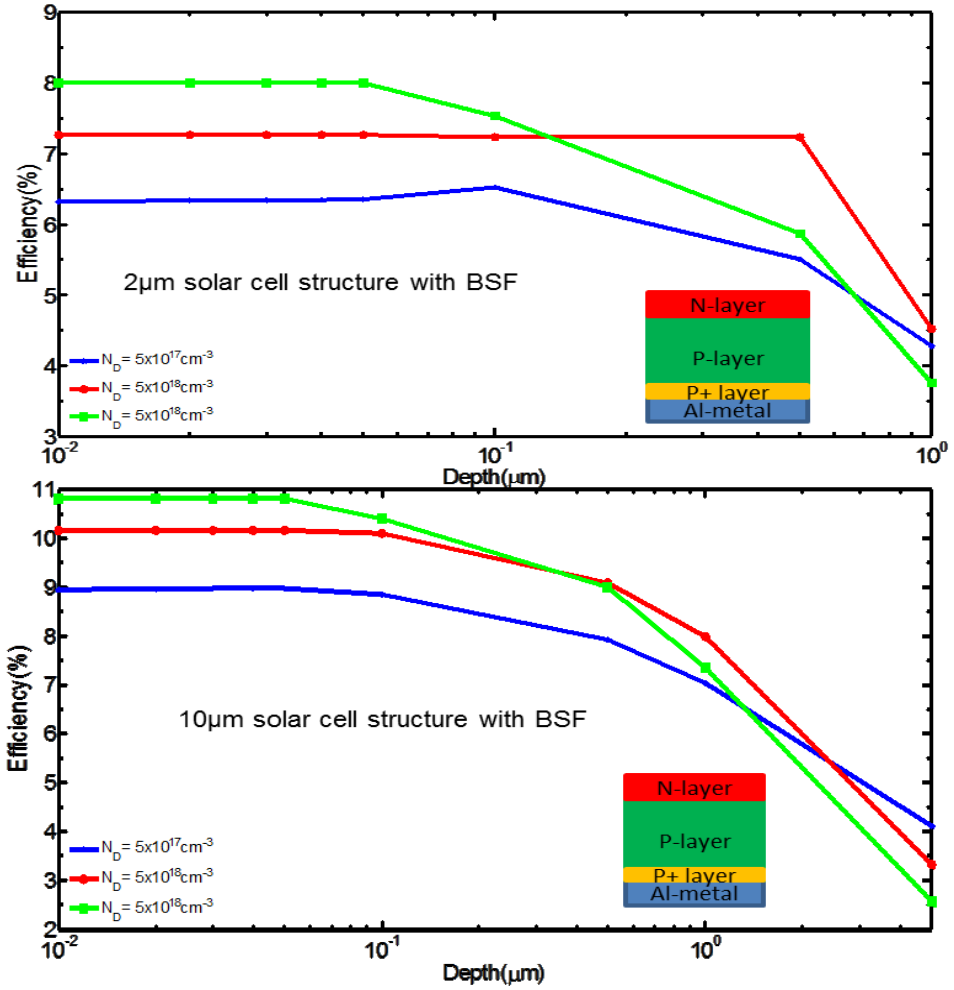

Figure 3.2 The 2, 10 μm crystalline silicon thin film without back surface field. Inset shows the schematic of the simulated structure

3.5 Contact Design

Any semiconductor device has to be connected to external wires to form an electronic circuit. In the case of p-n junction diodes or solar cells, contacts have to be

provided to both p-type and n-type regions of the device in order to connect the diode to an external circuit as shown in Figure 3.3

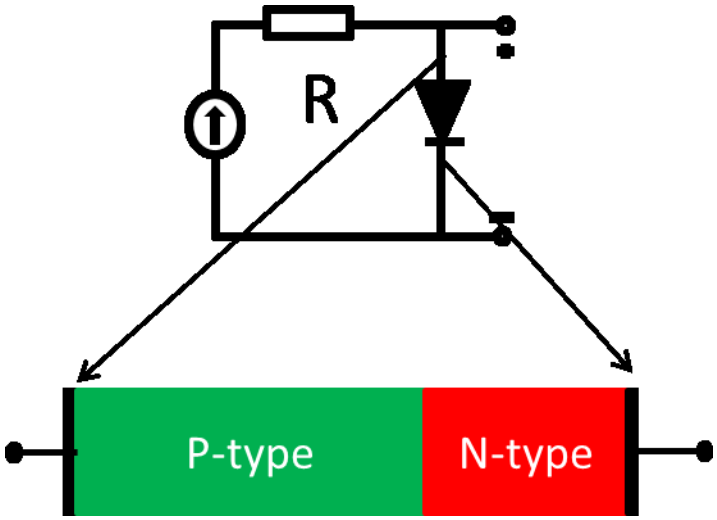

Figure 3.3 The contacts on p and n regions of the diode

When the characteristic of a metal contact formed on a semiconductor is such that the carriers are free to flow in or out of the semiconductor so that there is minimal resistance across the contact, the contact can be termed as an Ohmic contact. For an n type-metal junction the work function of the metal (Φ_m) must be close to or smaller than the electron affinity ($\Phi_{s,n}$) of the semiconductor. However, for a p type-metal junction the work function of the metal must be close to or larger than the sum of the electron affinity and the band gap energy of the semiconductor ($\Phi_{s,p}$) in contact [21].

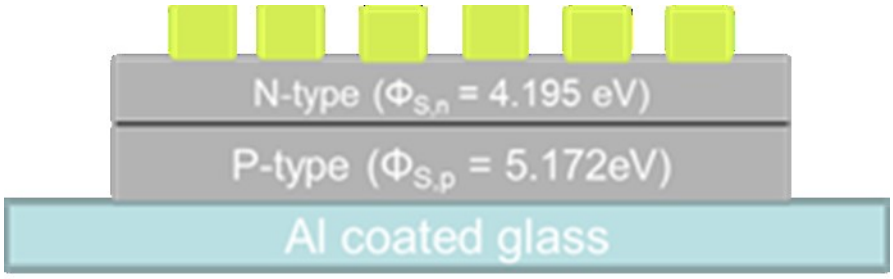

Figure 3.4 Schematic of the cell structure with calculated work functions

Table 4 shows the Proposed Metal for Top and Bottom Contacts for the Device

Contact Location	Metal used	Φ_S (eV)	Φ_m(eV)	$\Phi_m - \Phi_S$	Condition for Ohmic contact	Ohmic Contact
Top	Al	4.084	4.1	-0.09	$\Phi_m < \Phi_{s,n}$	Yes
Top	Ag	4.084	4.26 – 4.74	-0.06	$\Phi_m < \Phi_{s,n}$	Yes
Bottom	Au	5.172	5.1-5.47	0.028	$\Phi_m > \Phi_{s,n}$	Yes

Table 5 Summarizes the Proposed Device Specifications for 2μm and 10μm Thick Solar Cells

Parameter	Proposed specification for 10μm with back surface fields	Proposed specification for 10μm without back surface fields	Proposed specification for 2μm
Emitter concentration(N_D)	$5x10^{19}$ cm^{-3}	$5x10^{19}$ cm^{-3}	$5x10^{19}$ cm^{-3}
Base concentration(N_A)	$4.4x10^{16}cm^{-3}$	$4.4x10^{16}cm^{-3}$	$4.4x10^{16}cm^{-3}$
Emitter thickness	40nm	40nm	30nm
Top metal	Al, Ag	Al, Ag	Al,Ag
Bottom metal	Cr+Au	Cr+Au	Cr+Au
Expected efficiency	16.86%	13.33%	8.16%

Chapter 4

Solar Cell Fabrication

4.1 Introduction

The advantage of having thin film Solar cells (TFSc) is that it can be fabricated on lighter, cheaper and flexible substrates. This ease of fabrication on foreign substrates broadens the scope of applications for TFSC. TFSC can now be used in portable power supplies, wearable electronics and especially in aerospace applications where the mass of the power supply is an essential factor. In this chapter I discuss about the different methodologies incorporated in the fabrication of the 2μm crystalline Silicon solar cell. Ease of fabrication, while keeping the cost low has played an important role in designing the process.

Figure 4.1 shows the schematic of the SOI wafer used in fabrication. A p-type Boron doped (100) Silicon on insulator (SOI) substrate with a device layer thickness of 2μm having a resistivity of 4Ω-cm was used. The thickness of the Silicon oxide layer (Box) was 1 μm and the handle was 300μm.

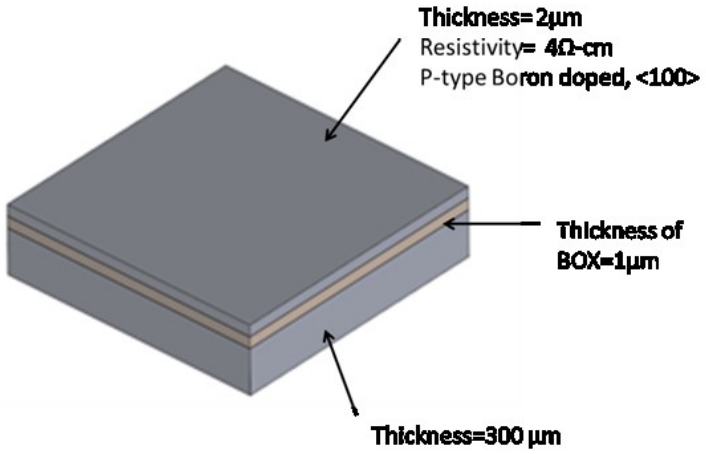

Figure 4.1 The specifications of the SOI wafer used for fabrication

The process flow is as follows- the semiconductor was doped with Phosphorus, release holes were patterned and dry etched, top membrane was released by wet etching and transferred onto a metal coated foreign substrate, finger are patterned on the substrate, the metal is then evaporated and finally metal lift-off is done in Acetone. The fabrication process flow diagram is shown in Figure 4.2

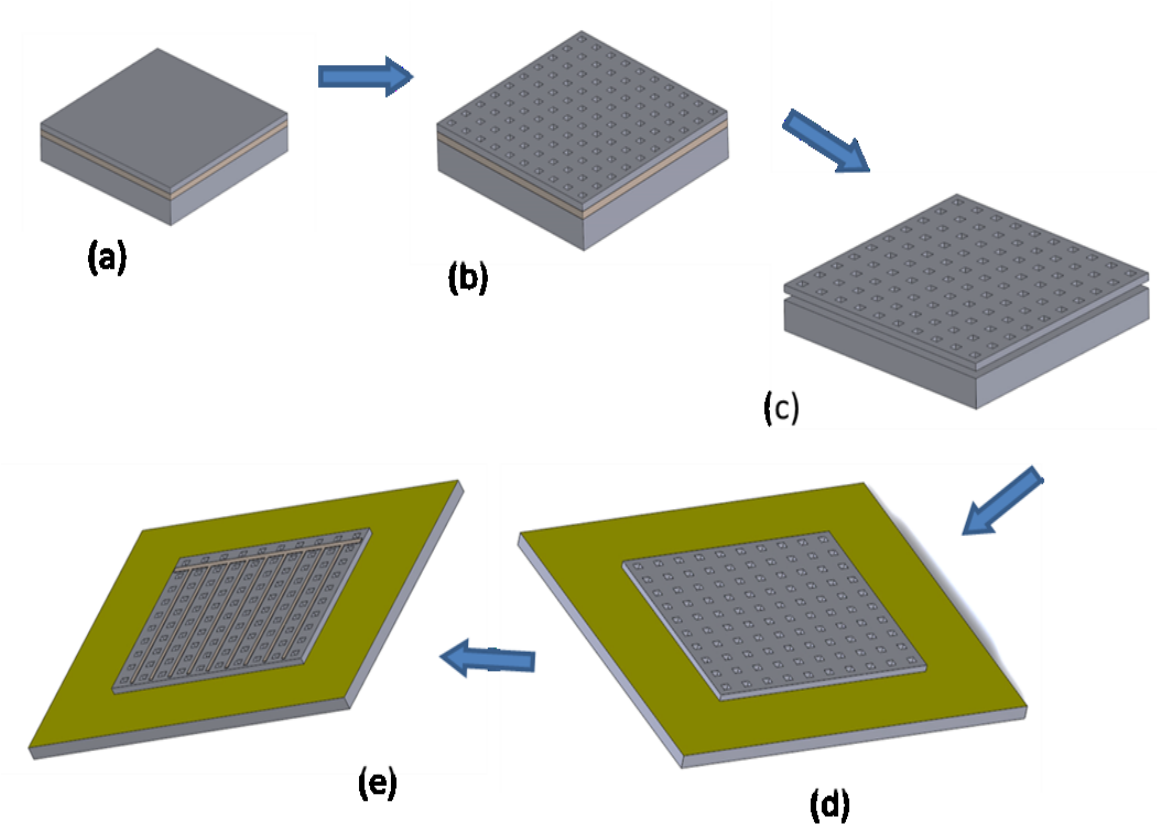

Figure 4.2 The fabrication flow. (a) SOI substrate is cleaned in (2:1) Piranha solution and dipped in aqueous HF solution. (b) Release holes of dimension 25μm x 25μm are patterned on the device layer and etched using DRIE with SF_6 as feed gas. (c) Etched sample is dipped in 40% HF solution to etch the underlying BOX layer. (d) Released membrane is transferred onto a metal coated foreign substrate. (e) Finger contacts are patterned, metal is evaporated and metal lift-off is done using Acetone.

4.2 Diffusion

To construct a solar a p-n junction needs to be formed inside an extrinsic semiconductor material. The intrinsic property of a semiconductor is needed for electron-hole pair generation under illumination. A p-n junction is by diffusing Phosphorus into the above mentioned p-type SOI substrate. Usually, diffusion is accommodated in a conventional quartz furnace at above $900^{O}C$ for prolonged periods ranging from a few minutes to a couple of hours. This results in deep junctions which give rise to cells with very low efficiency as discussed in previous chapters. [22] Discusses diffusion using different scenarios- conventional furnace processing (CFP) and Rapid thermal diffusion (RTD) and concludes that RTD is a better choice for achieving higher dopant concentration with shallow junction depth. Commercially available Phosphorus spin-on dopant (SOD) from Filmtronics was used as a source for diffusion. The peak Phosphorus concentration in the SOD is estimated to be 20×10^{19} cm^{-3}. The SOD is dispensed on to a $1cm^2$ x $1cm^2$ sample using a nozzle after being cleaned in Piranha solution (2:1 H_2SO_4:H_2O_2) to remove organic contaminants and dipped in 50:1 HF solution to strip any native oxide on the surface. An excessive amount of SOD is used to prevent coating discontinuities caused by SOD drying before it reaches the edges of the samples. The samples are then spun at 500 rpm with and acceleration of 150rpm/sec for 5 seconds to make ensure a uniform thickness of SOD over the entire sample. The substrate is then accelerated to 3000rpm and spun for 30 seconds. The samples are then prebaked at $200^{O}C$ for 20minutes. The pre baked samples are then loaded in an RTD furnace. There is ambient Nitrogen flow in the furnace all through the process. The furnace is ramped from base temperature to $800^{O}C$ in 10 seconds. The furnace maintains set temperature for 15minutes before it ramps down to the base temperature in 2minutes. The diffused samples are then dipped in HF solution to strip off the residual SOD and their resistivity is

characterized using a four-point probe. The surface concentration of hence obtained sample was 2 x 10^{18} cm^{-3}. To determine the junction depth a diffused sample of the size 50mm x 50 mm is taken and etched in steps of 10nm until a junction is seen. The junction depth is confirmed by probing the top surface of the sample and the surface etched. At the junction we can see an IV curve similar to that of a Silicon PN junction diode as in Figure 4.3

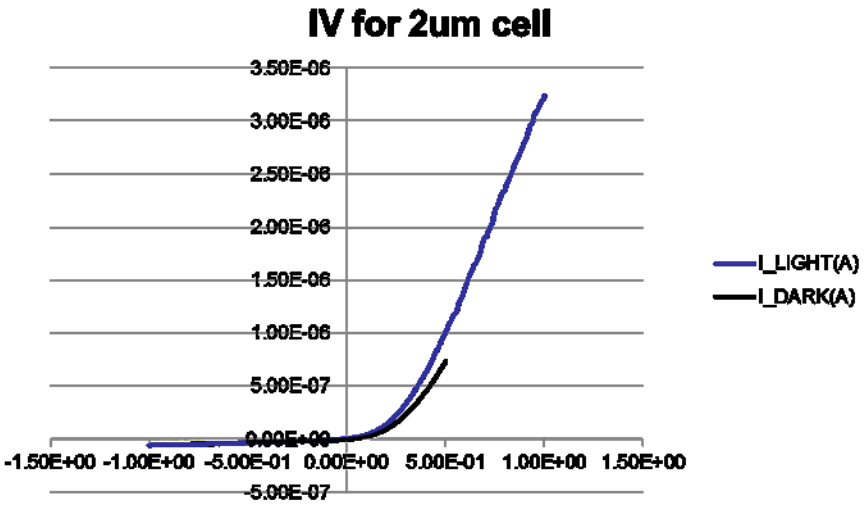

Figure 4.3 IV curve of the etched sample

4.3 Etching

Once a p-n junction has been formed, the next step would be to release the device layer of the SOI so that it can be transferred. This is achieved through two step etching process. First, release holes are patterned and the device Silicon is dry etched to expose the underlying Silicon dioxide (BOX) layer. The BOX is wet etched using a HF solution of suitable concentration. This membrane transfer process discussed in [23] provides an efficient way of transferring thin film Silicon (TFSi) on to foreign substrates.

Photoresist (PR) can be used as an etch stop layer for the dry etching step. Commercially available negative photoresist Futurrex NR9-3000PY was used. Sufficient

photoresist was dispensed using a nozzle on the diffused sample. A cell of 3mm x 3mm containing a 30 x 30 array of 25μm x 25μm release holes is patterned on the sample. Figure 4.4 shows the individual cell and the dimension of the release hole. The thickness of the PR is 4μm.

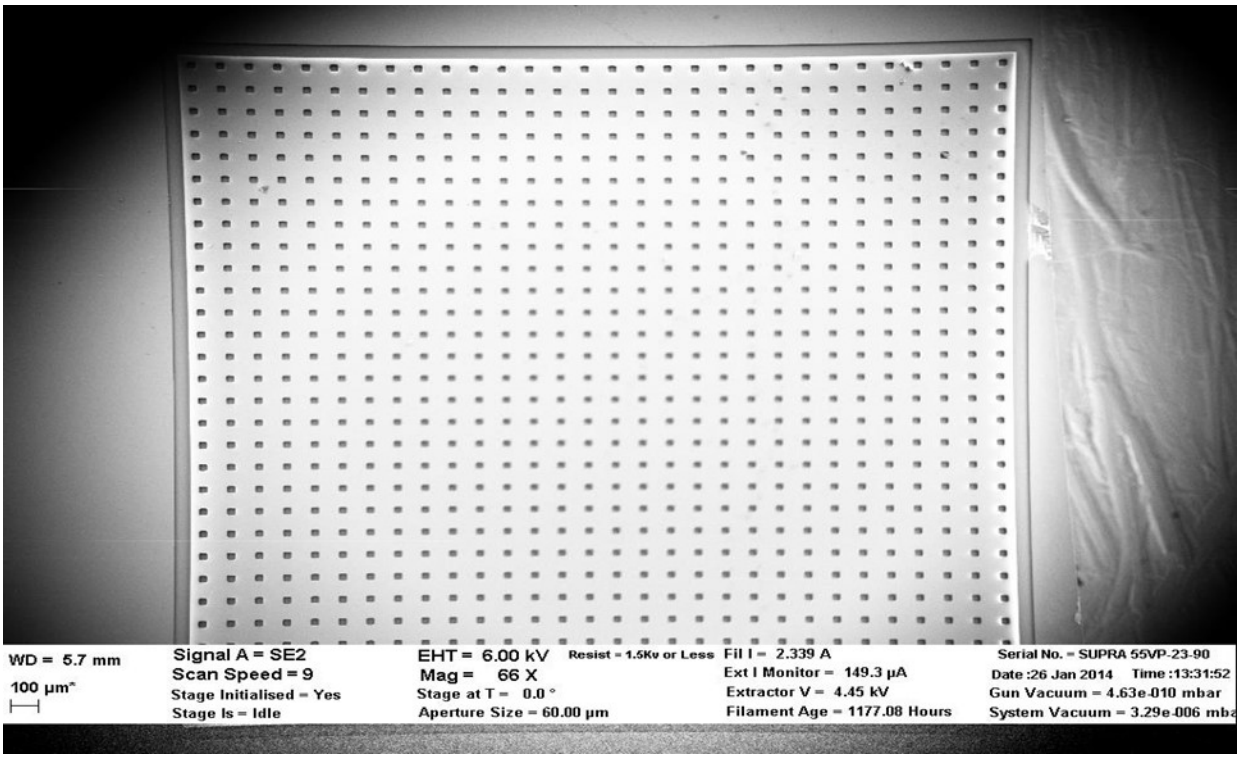

Figure 4.4 SEM image of an individual cell

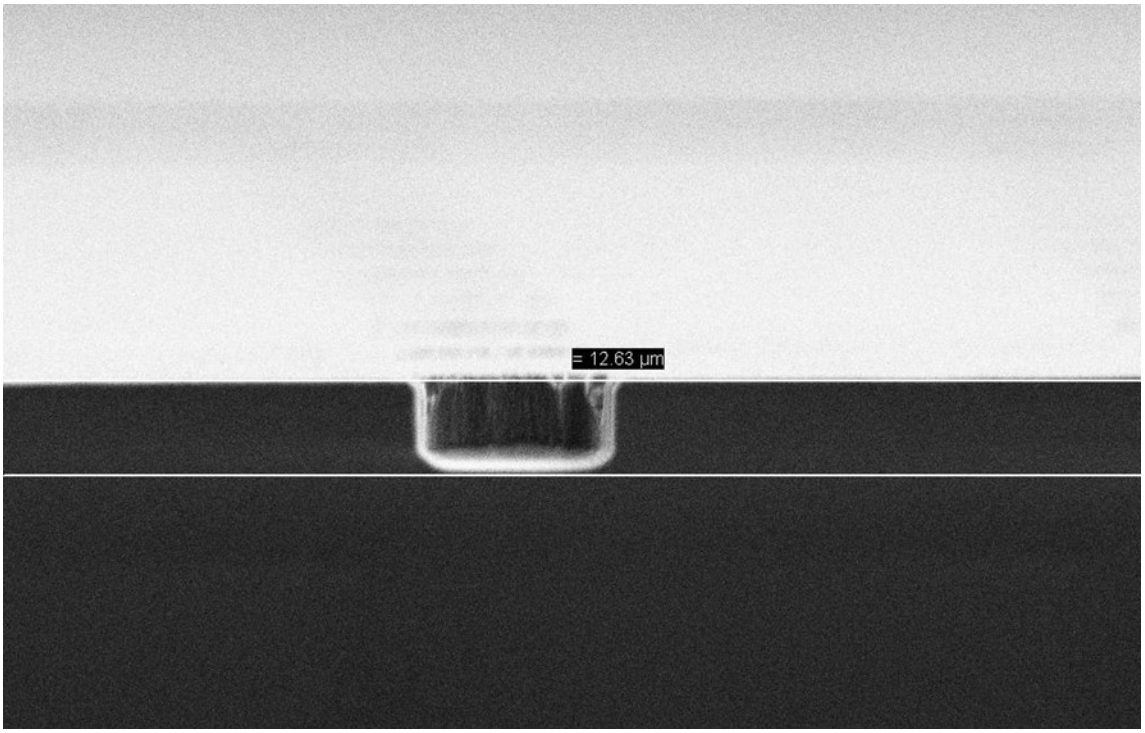

Figure 4.5 image of an individual release hole

4.3.1 Reactive Ion Etching

Reactive Ion etching (RIE) is an anisotropic etching process, which unlike its counterpart is not dependent on the crystalline structure of Silicon. Every dry etch process has four major steps [24]

1. Feed gas is introduced in to the chamber must be broken down into chemically reactive species.
2. These chemically reactive species must diffuse to the surface and be adsorbed.
3. Once on the surface they must react with the exposed film.
4. The reaction products must be desorbed and evacuated off the chamber.

The feed gas used was Silicon hexafluoride (SF6), which forms SF5+, F- ions and F* free radicals. The Oxygen (O2) in the chamber has two main purposes

1. Formation of passivation layer (in this case Silicon oxyflouride (SiOxFy)) which protects the side walls

2. The control of etch rate of Silicon. This is achieved by the rate at which it recombines with SF5+ radicals.

The flow of O2 determines the thickness of the passivation layer. Too low O2 flow results in failing passivation layer which leads to etch isotropic. If the O2 flow is too high, the thickness of the passivation layer increases and thus the etch rate decreases. Hence, maintaining an optimum SF6/O2 is very crucial. The etch rate of Silicon in the process is determined by the flow of the feed gas and formation of free radicals. Pressure of the chamber determines the directionality of the electrons, which in turn determines the anisotropy of etch.

Prior to etching the doped samples, experiment was conducted to determine the thickness of the PR to be spin coated and sidewall profile of the etch. A grating structure was patterned with a PR thickness of 1.3μm. Standard Silicon etch recipe with an etch rate of 1.47nm/sec was run for 30mins. The resulting etch profile is shown in Figure 0.6. There is clear indication of over etch implying insufficient PR and rough sidewalls. As suggested in [25] sidewall roughness can be reduced by shortening the duration of the etch cycle. These issues were addressed using a PR thickness of 4μm and the process cycle was broken down into 12minutes etch run. Figure 0.7shows the etch profile after modifications

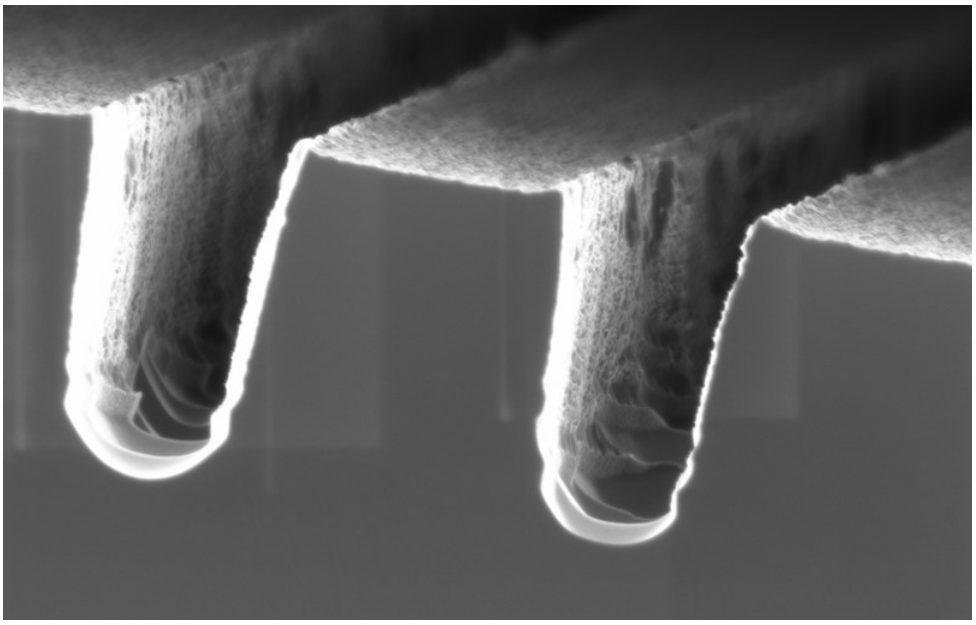

Figure 4.6 Etch profile before process optimization

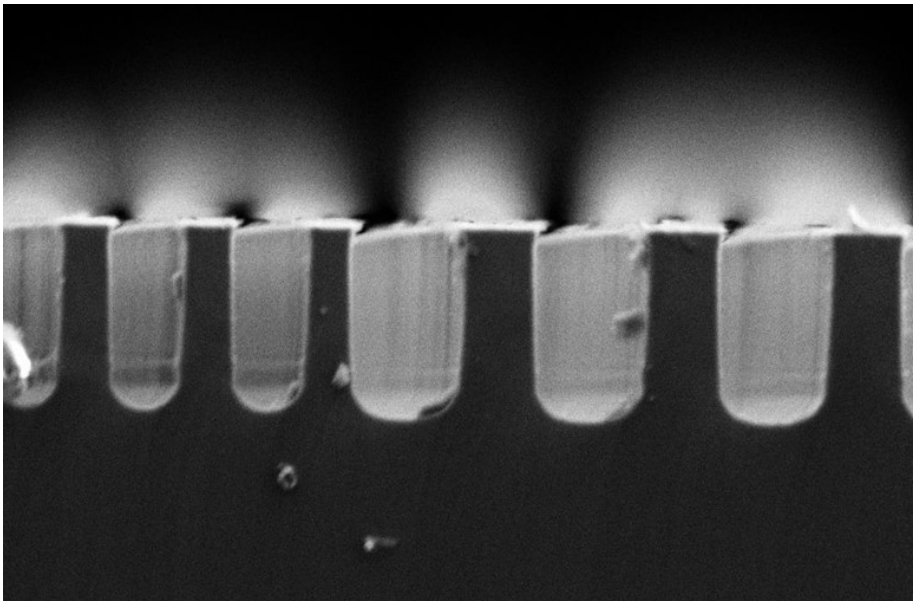

Figure 4.7 Etch profile after process optimization

The real samples were etched using the modified recipe. To completely expose the underlying BOX layer for subsequent processing steps, the samples were etched 5% into the BOX layer. Fig.4 shows the side view of the etched membrane. On observation it can be concluded that Silicon has been completely hed, exposing the BOX.

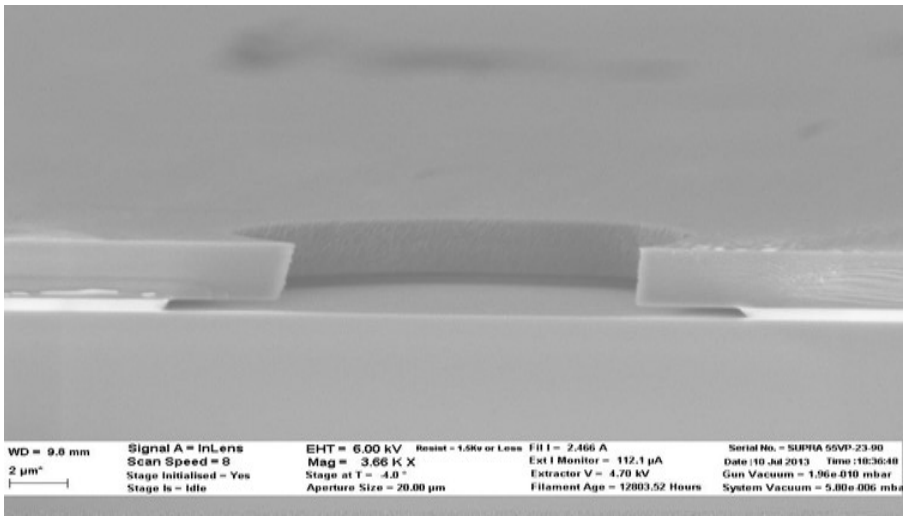

Figure 4.8 cross section of the etched membrane.

4.3.2 Wet Etching

A chemical process wherein a material is removed by a chemical reaction between the etchant and the material to be etched is called wet etching. Wet etching involves three principal steps

- Reactants are transferred to the proximity of the surface to be etched.
- Chemical reaction takes place.
- Reaction products are again transported away from the surface.

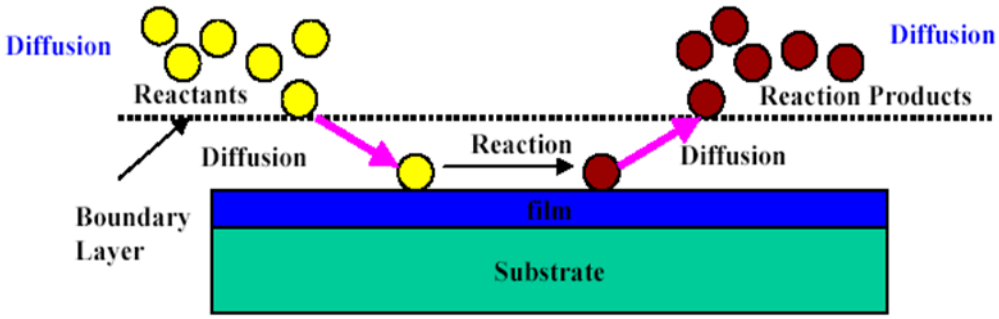

Figure 4.9 Principal steps involved in wet chemical etching

If the etch rate of the material is limited by the rate of chemical reactions at the surface then the process is termed as reaction-rate limited. To etch the BOX layer of the sample we use HF as the etchant. The etch rate of the solution is controlled by diluting the HF in H_2O and the etch selectivity of SiO_2/Si is greater than 100, which implies that the structural integrity of Si is unaffected. The chemical reaction taking place is

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$$

A magnetic stirrer is used to maintain uniformity of the solution, to ensure transfer of reactants to the surface to be etched and the transfer of the reaction products away from the surface. We have used 40% solution of straight HF and water for etching the box layer. Figure 4.10 shows the SEM image of the membrane after BOX layer has been etched.

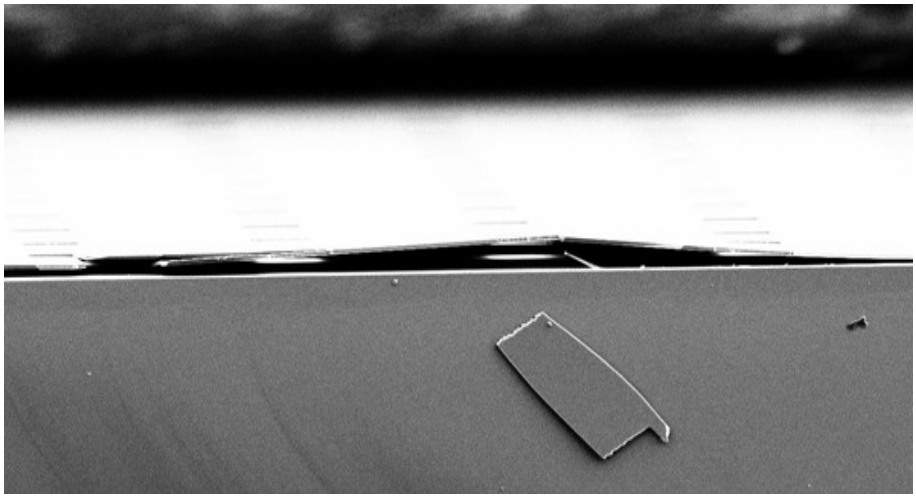

Figure 4.10 Cross-section of the sample after the BOX layer has been etched.

After the BOX layer has been etched away, Si membrane is suspended on the handle of the SOI wafer. The membrane can then be transferred on to any metal coated foreign substrate like glass or Polyethylene terephthalate (PET).

After the membrane has been transferred on to a foreign substrate top contacts after defined by photolithography. Evaporation is used to form coating of a wide variety of metals in which the source heating is done by resistive sources or e-beam sources. Deposition rate is determined by the emitter flux and the geometry of the source. Although the mechanism is more complex, e-beam evaporation is extremely versatile and virtually any material can be evaporated. As compared to thermal evaporation, contamination and wafer heating in an e-beam is minimal.

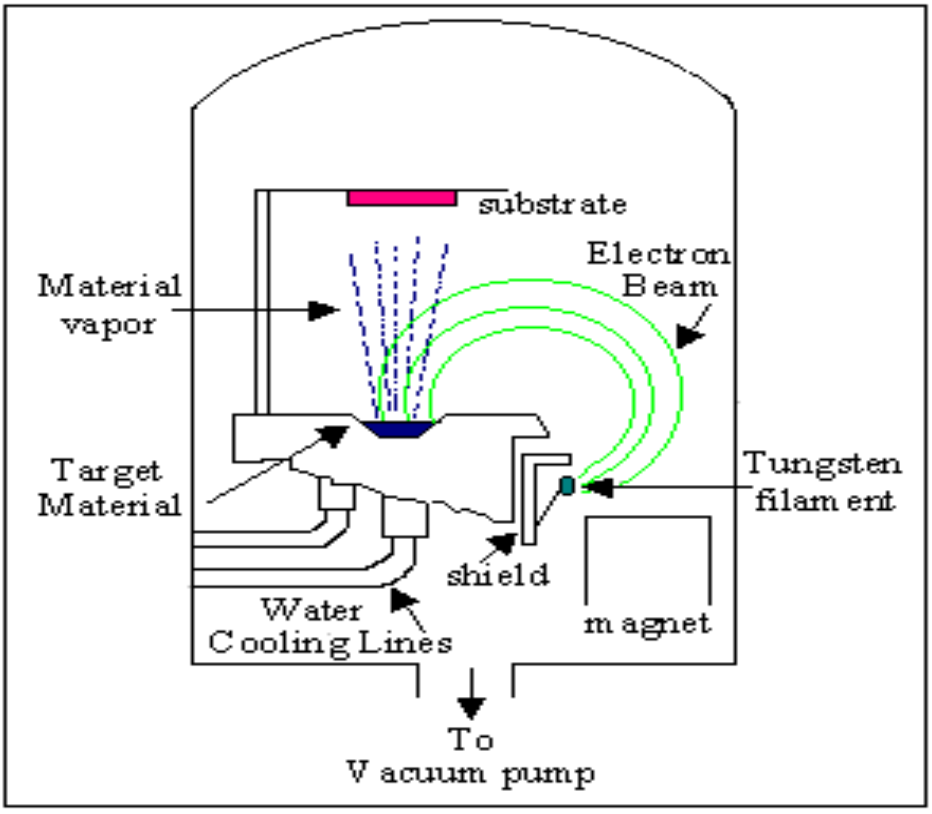

Figure 4.11 Typical e-beam evaporation chamber [26]

Using a focused e-beam the metals are heated and evaporated. The electron temperatures are as high as 10000 K. Electrons are accelerated by a DC 9Kv. Deflection plates are used to raster scan the beam across the charged surface (source).The evaporation occurs at a highly localized point near the beam bombardment spot in the surface of the source, so there is little contamination from the crucible.

Chapter 5

Results and Future Discussion

5.1 Introduction

After transferring the membrane onto a metal coated foreign substrate. The sample was tested under AM1.5 solar radiation. The results of the device shall be discussed in the following sections and finally conclude the chapter with future work and possible improvements to increase the efficiency of the cell.

5.2 Results

Shown in Figure 5.1 is a simple electron micrograph image of the transferred 2μm membrane onto a metal coated glass substrate. High quality 3mm x 3mm Silicon membrane was successfully transferred. The solar cell was tested under standard AM1.5 solar radiation using Newport Solar Simulator

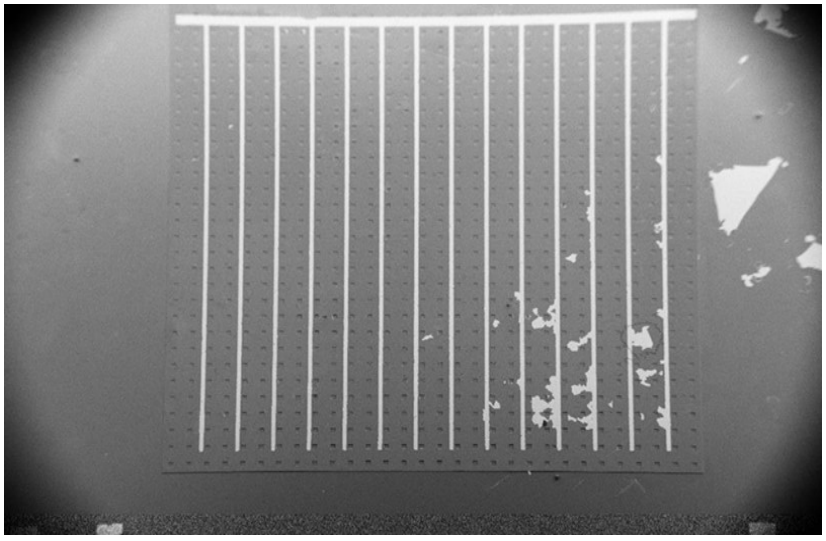

Figure 5.1 SEM image of the 2μm transferred membrane

The beam size of the simulator is 2 x 2 inch, with a collimation angle of less than 6^{o}. Typical power output is 100 mW/cm^2 (1 sun). The system has a Xenon arc lamp with 150W of power.

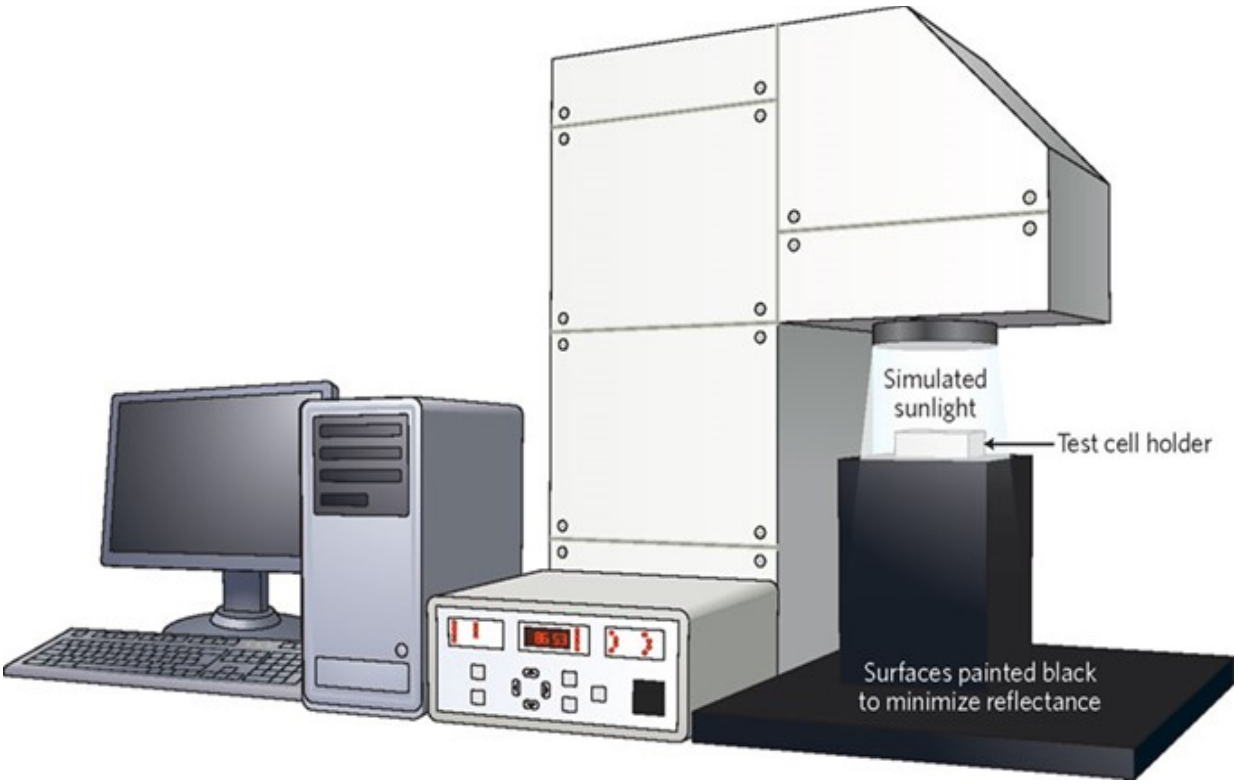

Figure 5.2 Typical solar cell testing setup for Solar cell testing [27]

The device exhibits good I-V characteristics with dark current around 0.1mA with rectifying behavior as shown in Figure 5.3

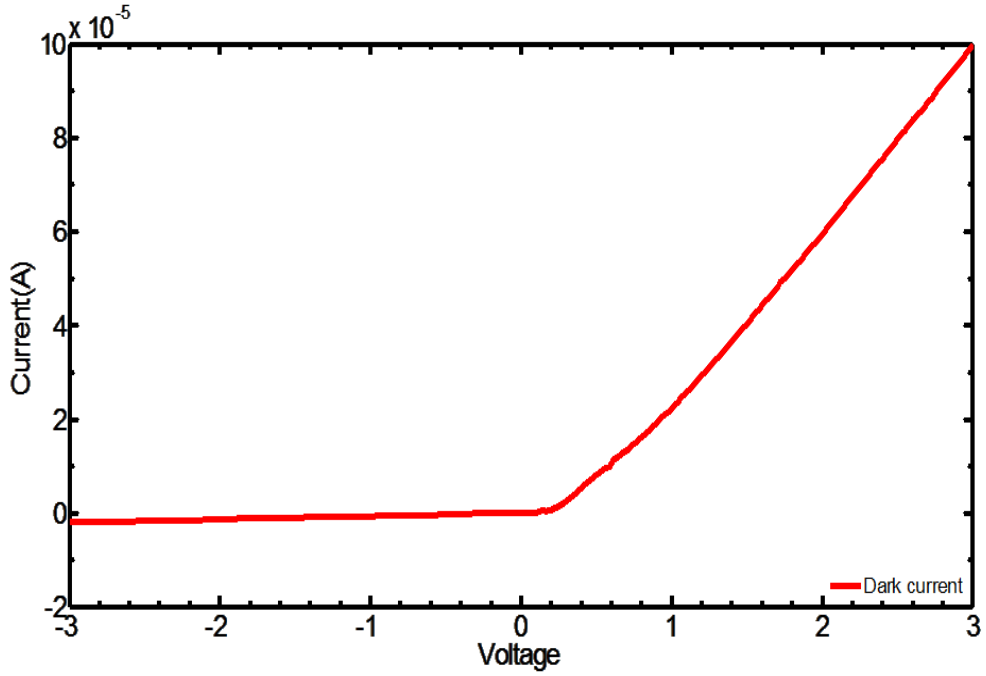

Figure 5.3 I-V curve showing the dark current of the device

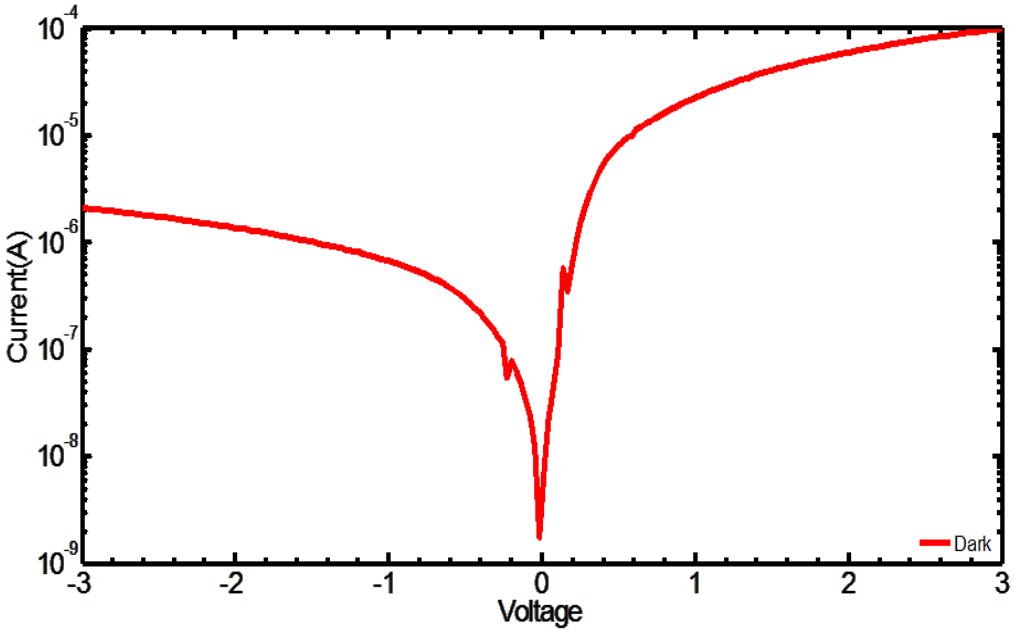

Figure 5.4 Log plot of the dark current

The open circuit voltage of the device is 0.38 V with a power efficiency of 0.8% and the fill factor of the device is 35%. The I-V curve of the device under AM1.5 illuminations is given in Figure 5.5

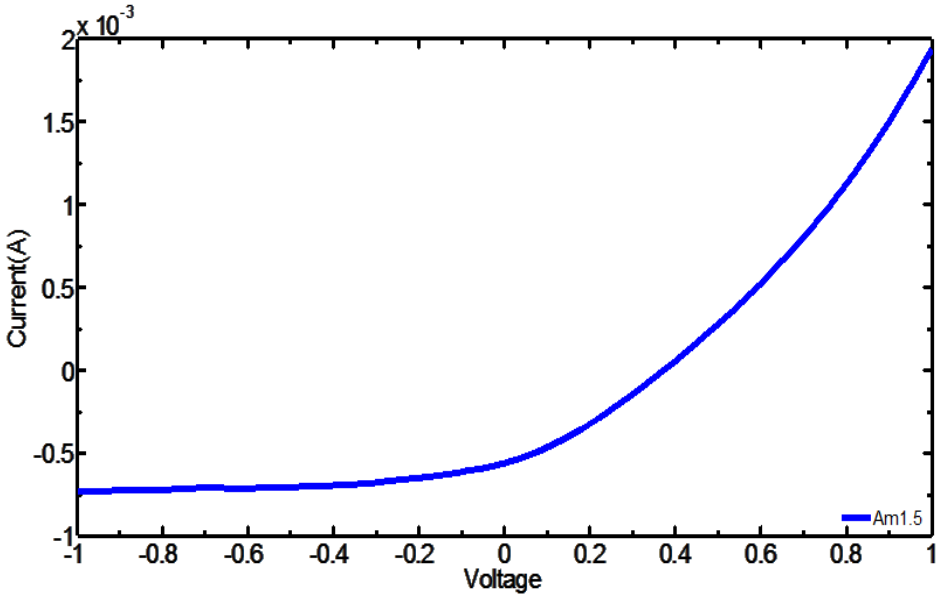

Figure 5.5 I-V curve of the device under AM1.5 illumination.

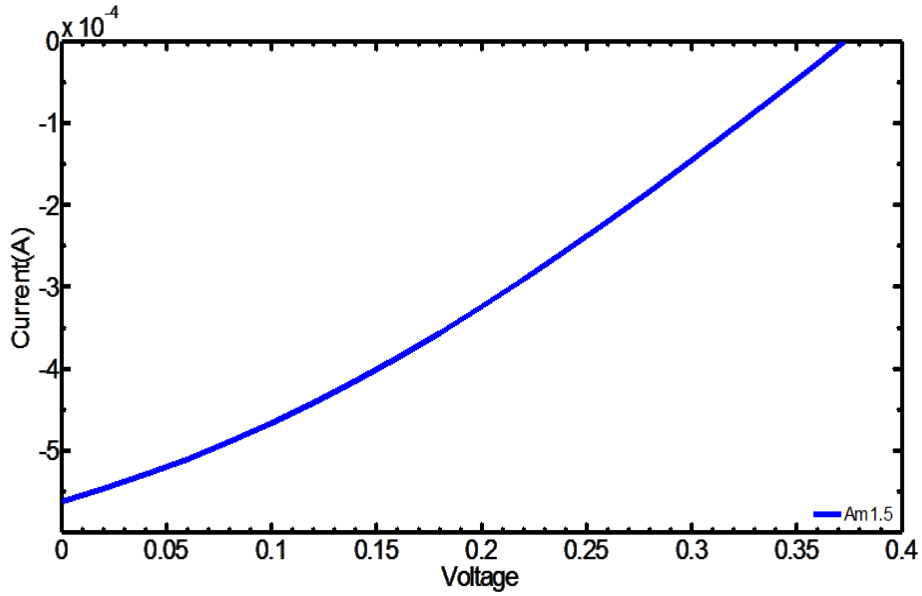

Figure 5.6 IV of the cell in the 4th quadrant

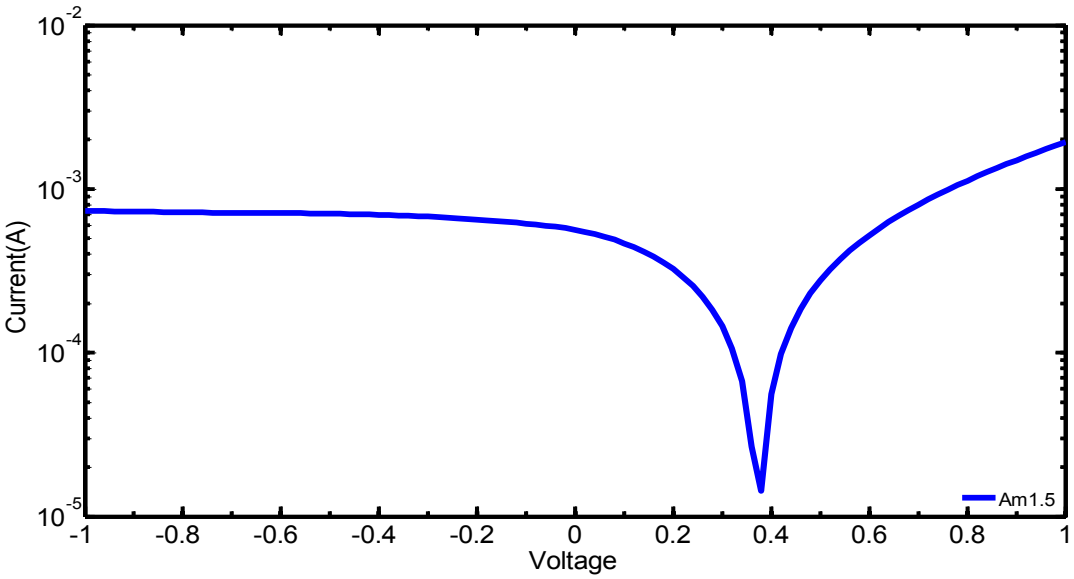

Figure 5.7 Log plot of the IV curve under AM1.5 illumination

The maximum efficiency demonstrated on a single crystalline Silicon solar cell is 21.1% [28] . The cell they talk about is an N-type cell structure with Boron doped emitter. This is contrary to our simulated structure which has a phosphorus emitter. High efficiencies are observed in [28] because of incorporated light trapping mechanism like inverted pyramids on the top surface and rear surface mirror. The rear surface is Phosphorus doped to reduce series resistance. The theoretical efficiency as described in [29] for a 2μm Silicon solar cell is around 17%. This result is obtained by assuming zero surface recombinations. Increasing amounts of surface recombination exacerbate the above trends, which is consistent with the simulated results. Medici takes into consideration Shockley-Read-Hall, Auger, and direct recombination and also recombination component at specific insulator-semiconductor interface.

Figure 5.8 Simulated cell structure

The simulated cell structure as shown in Figure 5.8 consists of a Boron-doped base (P-region), a Phosphorus doped emitter (N-region) and a highly doped P^+ region. The base doping concentration is $4X10^{16}$ cm^{-3}. Three different doping concentrations- $5X10^{17}$, $5X10^{18}$, $5X10^{19}$ cm^{-3} were used with emitter thickness varying from 10nm to 5μm. it has been observed that for a given thickness of the emitter changing the doping concentration does not have a considerable effect on the efficiency. But changing emitter

thickness for a constant emitter concentration has significant effect on the efficiency. Comparatively higher efficiencies are observed at shallower emitters as seen in Figure 3.1. The emitter thickness when measured was close to 1μm, with a doping centration of $3x10^{17}cm^{-3}$.

The efficiency of a solar cell is not only limited by the reflection losses but also by the motion of the sun. The crystalline semiconductor based solar cells suffer from a relatively large reflection losses owing to its high refractive index. Depending on the time of the day, the amount of the solar power received by the cell reduces by a factor of cosine of the angle between the solar cell module surface normal and the sunray. While anti-reflection (AR) coatings are used to reduce the reflection losses, concentrators are used to focus solar radiation from large area onto smaller solar cells area, thereby increasing the cells efficiency. However, this high efficiency is at the expense of a complicated and bulky optics system, tracking system and cooling system

Recently, it was experimentally demonstrated large area solution-processed spherical surface textures and nanoimprinted pyramid surface textures for omnidirectional conformal AR coatings on flexible amorphous silicon solar cells.[30, 31] The incorporation of the surface texturing on crystalline thin film silicon cell, gradually changes its high refractive index to that of the surrounding medium thereby reducing reflection. Both the spherical and the pyramid texture leads to increase in relative cell efficiency from surface normal to oblique incidence as high as 60^{o} demonstrating its omni-directionality. The increased efficiency is a result of reduced reflectivity of the cell over a 400 – 1,200 nm wavelength range. The lower reflection increases the light absorption consequently increasing the short circuit current density in the thin film cell.[32] also, reported Electroless metal-assisted electrochemical etching (MAcEtch) process. A broadband (300 – 1,050 nm) low reflection of 2% resulted from random nano-

scale porous structures embedded in micro-scale pyramid structures. All these surface textures demonstrate the potential of fabrication of large area, high efficiency, and low cost thin film solar cell.

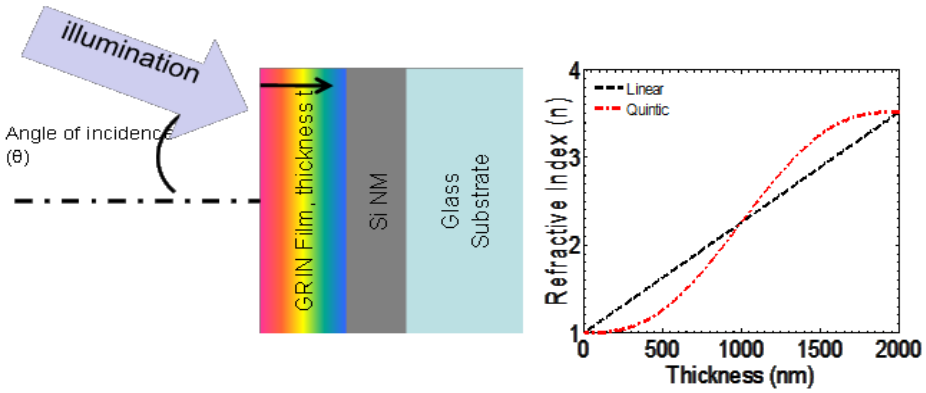

Figure 5.9 (a) Schematic of the GRIN film structure on thin film c-Si; (b) Linear and Quintic GRIN index profiles are considered in this project, for performance comparison and surface texture design.

Shown in Figure 5.10 are the angle dependent simulated absorption, reflection and transmission from untextured, graded index (GRIN) and pyramid textured crystalline thin film silicon. The GRIN simulations involved a t = 2μm thick GRIN Si film on a 2μm silicon thin film with a linear or quintic index. The pyramid texture assumes a two dimensional periodic arrangement of closed packed square lattice with pyramid base of 2.83 μm and height of 2 μm. The simulated results in Figure 5.10 show that the absorption with the graded index and pyramid textured structure is noticeably higher than untextured thin film silicon. The refractive index of the pyramid texture decreases from the refractive index of air at the tip to the index of silicon at the base of the pyramid so that the gradual change in the refractive index reduces the reflection increasing the

absorption in the Si membrane. The oscillations in the reflection and transmission spectrum are due to the thin film interference.

Assuming that there is no damage to the electrical properties to the textured thin c-Si film, the estimated current density from the pyramid texture are 33.85 mA/cm^2 and 35 mA/cm^2 at surface normal incidence and at oblique incidence respectively. These values correspond to 61.25% and 62% current densities increment compared to the current density of a 4 μm untextured thin c-Si film at surface normal and oblique incidence. At higher incidence angles, the second strike in the pyramids enhances the light trapping in the cell resulting in increased absorption. In conclusion, the pyramid texture demonstrates its omni-directionality by maintaining high absorption both at surface normal and oblique incidences.

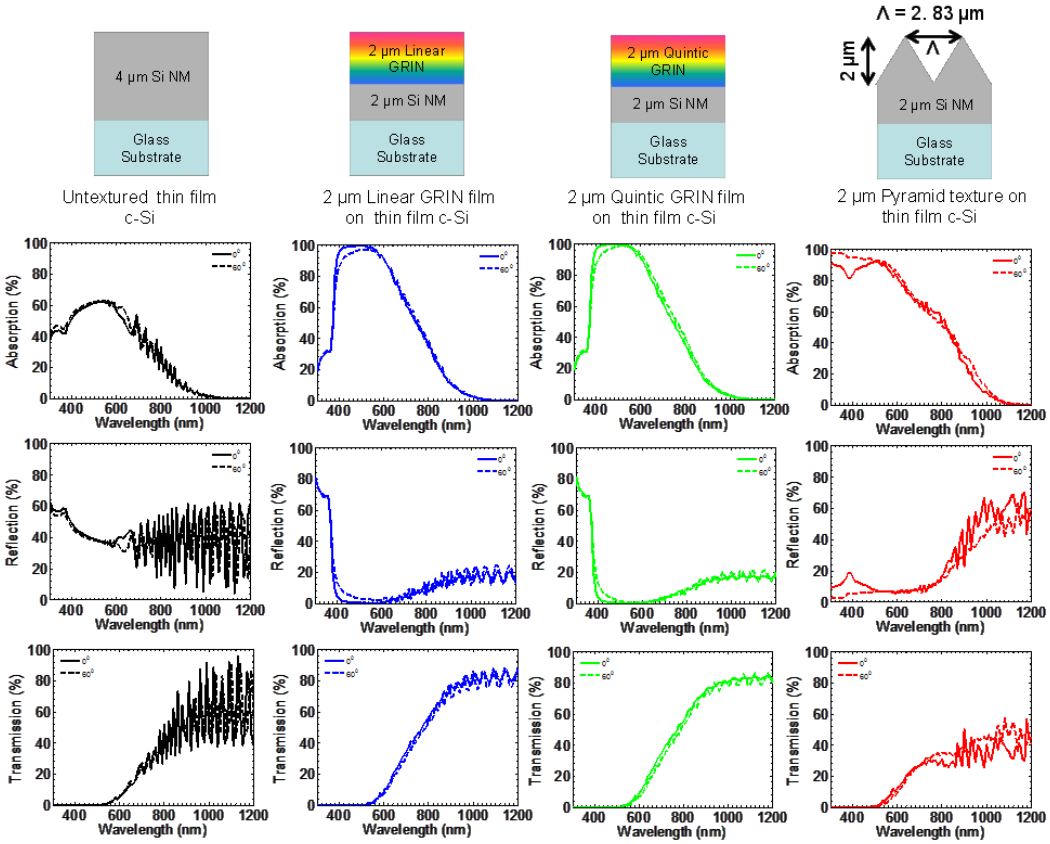

Figure 5.10 Top to bottom rows shows the schematic and simulated absorption, transmission and reflection from untextured, linear and quantic graded (GRIN) films and pyramid texture on thin crystalline silicon film

Appendix A

Synopsys MEDICI PN Diode Transient Simulation

```
ASSIGN NAME=WL N.VALUE=31

COMMENT Create an initial simulation mesh
MESH    ^DIAG.FLI
X.MESH  X.MAX=0.1  H1=0.01 H2=0.02
Y.MESH Y.MIN=0 Y.MAX=25.5 H1=0.1 H2=0.2
Y.MESH Y.MIN=25.5 Y.MAX=25.8 H1=0.01 H2=0.02

COMMENT Region and electrode statement
REGION  NAME=Silicon SILICON Y.MAX=0
REGION  NAME=BACK METAL Y.MIN=0
ELECTR  NAME=Anode Y.MIN=0 Y.MAX=0
ELECTR  NAME=Cathode BOTTOM

COMMENT Specify impurity profiles
PROFILE N-TYPE N.PEAK=4.4e19 Y.MIN=0.0  Y.MAX=0.1 Y.CHAR=0.005
PROFILE P-TYPE N.PEAK=8e16 Y.MIN=0.1 Y.MAX=23.5  Y.CHAR=0.02
PROFILE P-TYPE N.PEAK=2e19 Y.MIN=23.5 Y.MAX=25.5  Y.CHAR=0.005

COMMENT CONTACT CHARAC
CONTACT  NUM=ANODE  TRANSELE
CONTACT  NUM=CATHODE  REFLECTI=0.9

MATERIAL REGION=BACK WAVE.RE=(1.0) INDEX.RE=(1.39)
+FIRST LAST

COMMENT Specify physical models to use
MODELS CONSRH AUGER

COMMENT Symbolic factorization
SYMB    NEWTON CARRIERS=2

COMMENT  Specify light source and photogeneration with raytracing
+       The light spectrum is black body radiation (T = 5800K)
+       which is approximated to the AM0 spectrum.
+       Total incident light power is approximately 100mW/cm^2
+       for [0.2 um, 1.0 um] wavelength band.

PHOTOGEN RAYTRACE BB.RADI BB.TEMP=5800 WAVE.ST=0.2 WAVE.EN=1.0
+       WAVE.NUM=@WL
+       X.ORG=0.05  Y.ORG=-1.5  ANGLE=90  INT.RATIO=1E-2
+       N.INTEG=10  RAY.N=1  RAY.W=0.1

COMMENT Create a log file for the transient I-V data
LOG     OUT.FILE=NC4_01_back.ivl
SOLVE V(CATHODE)=0.0 VSTEP=0.1 NSTEP=7 ELEC=CATHODE
SOLVE V(CATHODE)=0.4 VSTEP=0.01 NSTEP=7 ELEC=CATHODE
SOLVE V(CATHODE)=0.8 VSTEP=0.01 NSTEP=10 ELEC=CATHODE

COMMENT Solving for each wavelength
LOG OUT.FILE="WAVE.SPL"
LOOP STEPS=@WL
```

```
SOLVE WAVE=1:1
L.END

COMMENT plot I-V figure
PLOT.1D IN.FILE="NC4_01_back.ivl" X.AXIS=V(CATHODE) Y.AXIS=I(CATHODE)
+       TITLE="PN - Current vs Voltage" COLOR=3
+       TOP=0 RIGHT=1 LEFT=0 BOTTOM=-2.6E-11
+       DEVICE=POSTSCRIPT     PLOT.OUT=VI_NC4_01_back.eps
    .
```

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Nandan's research interests include thin film photovoltaics and developing novel anti-reflective coating for photovoltaic applications. He plans to pursue a career in process and (or) product development of novel semiconductor based devices.