STUDY AND MANIPULATION OF ELECTRON TUNNELING THROUGH QUANTUM DOTS

by

PRADEEP KRISHNA BHADRACHALAM

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Abstract

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QUANTUM DOTS

Pradeep Krishna Bhadrachalam, PhD

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Supervising Professor: Seong Jin Koh

Fermi-Dirac distribution is the fundamental property which governs the electron energy distribution in solids. At finite temperatures, Fermi-Dirac thermal smearing of electron energies limits the operation of many electronic, opto-electronic and spintronic devices. Examples include single electron transistors, quantum dot resonant tunnel diodes for single photon detection, and single electron turnstile devices. To overcome this intrinsic limitation of Fermi-Dirac thermal smearing, these devices have typically been operated at cryogenic temperatures. Room temperature operation of these devices could be realized, however, if the thermal smearing of electron energies could be suppressed. Until now, studies in the fields of electron-tunneling refrigerators and double quantum dot devices have demonstrated limited manipulation/suppression of electron energy distribution, but those have been carried out at cryogenic temperatures.

Using a double barrier tunneling junction structure as a model system this research has accomplished the following:

- Demonstrated suppression of thermal smearing of electrons at room temperature, without any physical cooling of the system

- Demonstrated that cold electrons whose effective temperature as low as ~45 K can be created at room temperature without any physical cooling
- Systematically investigated the phenomenon responsible for suppression in thermal smearing of electron energies
- Systematically investigated the cold electron transport in the double barrier tunnel junction structure

One of the key achievements of this research was demonstration of effective electron temperature of ~45K at room temperature without any physical cooling of the system. This was realized by filtering out the thermally excited electrons in a double barrier tunneling junction structure. A discrete energy state of a quantum well, created by band bending of Cr_2O_3 conduction band, acted as an electron energy filter, effectively suppressing energy distribution of electrons, thereby creating cold electrons (~45K) at room temperature. This phenomenon of electron energy filtering was observed in double barrier tunnel junction devices fabricated using different quantum dots (~5.5nm, ~6.6nm, ~7nm CdSe and ~7.8nm CdTe). The full width half maximum peak widths of differential conductance measurements of these devices, which is directly related to the Fermi-Dirac distribution of electrons, were found to be much narrower (~15meV at room temperature) than theoretically calculated values (~90meV at room temperature) as a result of suppression of Fermi-Dirac electron energy distribution.

A model which takes electron energy filtering into account was used to numerically calculate the full width half maximum peak widths of differential conductance peaks at different temperatures (77K to 295K) and compared to the experimental results. The theoretical calculations are in very good agreement with the experimental results over the entire temperature range explored.

Precise placement of quantum dots between the electrodes is one of the major challenges which need to be addressed for a large-scale fabrication of the devices investigated in this study. A nanoparticle placement technique, which is capable of precisely placing single nanoparticles onto desired substrate locations over an entire wafer, was demonstrated. Using this nanoparticle placement technique as a base model, a concept for guided placement of quantum dots/nanoparticles onto the double barrier tunneling junction device structure is presented.

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Chapter 1

Introduction

1.1 Overview

Among all the successes of quantum mechanics as it evolved in 1930's, one of the most impressive achievements was to understand tunnel effect - the penetration of matter waves and transmission of particles through a high potential barrier. This has eventually led to two Noble prizes in physics, shared among five researchers, for their research involving tunneling in semiconductors [1.1], superconductors [1.2] and for invention of scanning tunneling microscope [1.3]. Quantum tunneling remains as a hot topic to this day with myriad applications.

Tunneling of electrons through low dimensional objects like metal nanoparticles, quantum dots and individual molecules has great scientific and technological significance. Some examples include single electron transport [1.4-1.6, 1.25-1.26] and quantum dot resonant tunneling spectroscopy [1.7-1.24].

The characteristics of electron tunneling in solids are greatly influenced by the temperature. At finite temperature, electrons in solids are thermally excited to higher energy states following Fermi-Dirac distribution. This thermal excitation of electrons, however, generally imposes significant limitations on proper functioning of various electron systems. For single electron devices, as an example, the electron thermal excitation can wipe out the Coulomb blockade effect. For tunneling spectroscopy of quantum dots, the electron thermal excitation prevents the detection of quantum dot energy levels that are closely spaced. To reduce electron thermal excitation, the electron systems need to be cooled to low temperatures, which limits their practical applications.

This study aims to investigate a novel approach in which the electron thermal excitation is suppressed by filtering out thermally excited electrons using a discrete energy level formed on a quantum well. Using this method, it is demonstrated that the Fermi-Dirac thermal smearing of electrons can be effectively suppressed, which has allowed clear observation of CdSe and CdTe quantum dot energy levels even at room temperature. This energy filtering may potentially be used as an effective strategy to circumvent the intrinsic thermodynamic limitations imposed on solid state electron systems and promises many practical applications.

1.2 Electron Tunneling through Quantum Dots – Electron Energy Filtering

Electron tunneling through quantum dots can yield information about the electronic structure of the discrete energy levels of quantum dot, which is termed as tunneling spectroscopy of quantum dots. At finite temperatures, due to the Fermi-Dirac thermal smearing of electrons, these tunneling spectroscopic studies become impossible when the separation between the adjacent energy levels of quantum dot is comparable to the thermal energy of electrons. Hence, low temperatures are employed to study the electronic structure of such quantum dots using tunneling spectroscopy. However, if the electron energy distribution can be manipulated in such a way that, the Fermi-Dirac thermal smearing of electrons is suppressed, then these spectroscopic studies could be carried out even at room temperature.

Studies in the fields of electron–tunneling refrigerators and double quantum dot devices have shown that a limited manipulation of Fermi-Dirac thermal smearing of electrons is possible at low temperatures, typically below 10 Kelvin [1.27-1.29]. In double quantum dot devices, using a discrete energy state of a quantum dot as energy filter, the thermally excited electrons were filtered out and only the cold electrons were allowed to

participate in tunneling events. These studies were carried out at cryogenic temperatures using two dimensional electron gases to form quantum dots and it was demonstrated that at a reservoir temperature of 0.1K an effective temperature of 0.03K can be achieved [1.29].

In this study, using the double barrier tunneling junction (DBTJ) structure as our model system, we show that an effective electron temperature of ~45K can be achieved at room temperature, without any physical cooling of the system. A discrete energy state of a quantum well formed in the Cr_2O_3 conduction band acts as an energy filter, filtering out thermally excited electrons in our DBTJ devices. To demonstrate this, we fabricated DBTJ devices on a silicon substrate using CMOS-compatible parallel processes. The study was conducted on different quantum dots systems (CdSe and CdTe quantum dots with different sizes) and the same electron energy filtering-cooling effect was consistently observed in all quantum dot systems explored. This phenomenon of electron energy filtering enabled room-temperature tunneling spectroscopy studies of different quantum dots, which would otherwise have not been possible due to the Fermi-Dirac thermal smearing of electrons. The phenomenon of electron energy filtering to create cold electrons may find broad range of applications in many electronic devices, opto-electronic and spintronic devices.

1.3 Organization of Thesis

The main goal of this thesis is to demonstrate suppression of the thermal smearing of electron energies without any physical cooling of the system. The model system chosen for demonstrating this is a DBTJ structure with quantum dots. Electron tunneling through DBTJ devices and the phenomenon of suppression of Fermi-Dirac thermal smearing are explained.

In Chapter 2, the basic understanding of tunnel junction and electron tunneling is provided, followed by introduction to DBTJ device structure. Then a more detailed explanation of different electrical characteristics that can be expected from a DBTJ device with quantum dots is provided. With the aid of energy diagrams different regimes of electron tunneling through quantum dots in a DBTJ are explained.

In Chapter 3, the effect of Fermi-Dirac thermal smearing on the electrical characteristics of DBTJ devices is detailed. A phenomenon for electron energy filtering observed in double quantum dot devices is explained and the research studies in this field of double quantum dot devices are presented.

Chapter 4 describes the fabrication of our DBTJ devices. The fabrication processes used for realizing DBTJ devices are detailed. The processes explained in this chapter include mask designing, thermal oxidation, photo-lithography, evaporation of metal films, deposition of thin dielectric films using plasma enhanced chemical vapor deposition, reactive ion etching, and sputter deposition.

In Chapter 5, the measurement setup used for electrical characterization of the DBTJ devices is presented, as well as the actual electrical data from the DBTJ devices. The electrical characterization data from different DBTJ devices fabricated with different quantum dots is presented.

In Chapter 6, the electrical data presented in previous chapter is analyzed through numerical calculations and compared to Fermi-Dirac calculations. For the purpose of this comparison, the full width half maximum (FWHM) peak widths of experimental differential conductance peaks are measured and compared to the numerically calculated FWHM peak widths. A simulation model which takes into account the electron energy filtering is used to carry out numerical calculations and the results are compared to the experimental data.

In chapter 7, a technique for precise placement of nanoparticles onto desired substrate locations is presented. It is also shown that this technique is capable of selectively placing different sized nanoparticles onto different locations on same substrate. Finally, a concept for placing nanoparticles/quantum dots on the sidewall of the DBTJ devices is proposed. This can considerably increase the yield of the DBTJ devices.

Chapter 2

Theory of Electron Tunneling

2.1 Introduction

In this chapter an introduction to tunnel junctions is given, followed by detailed discussion of double barrier tunneling junction (DBTJ) devices. The outline of this chapter is as follows

a) An introduction to tunnel junctions and electron tunneling through tunnel junctions is given, followed by brief discussion of the DBTJ devices

b) Electron transport through quantum dots in DBTJ devices and different regimes of resonant tunneling in these devices is explained qualitatively with the aid of energy diagrams

c) An introduction to voltage division factor in DBTJ devices, followed by detailed explanation of a method to calculate the voltage division factor of these devices from electrical measurements, nominal size of quantum dots and optical band gap data.

2.2 Tunnel Junctions

A tunnel junction is a barrier, such as a thin insulating layer, between two electrically conducting materials. Electrons pass through the barrier by the process of quantum tunneling. A schematic of tunnel junction is shown in figure 2-1(a). It can be represented by an equivalent circuit diagram consisting of a capacitor of tunnel capacitance C and resistor of tunnel resistance R connected in parallel as shown in figure 2-1(b). The capacitor in a tunnel junction differs from a classical capacitor. In classical capacitor there will be no transfer of charge between the two plates of the capacitor,

where as in tunnel junction the electrons tunnel across the dielectric film when it s energetically favorable. Although represented as a resistor, the tunneling resistance is fundamentally different from an ohmic resistor. In an ordinary resistor the charge transfer or the electron flow is continuous. But for a tunneling resistor, the transfer of electrons through it is discrete. Hence a tunnel junction is often called a leaky capacitor in parallel with a resistor through which the charge transfer is discrete.

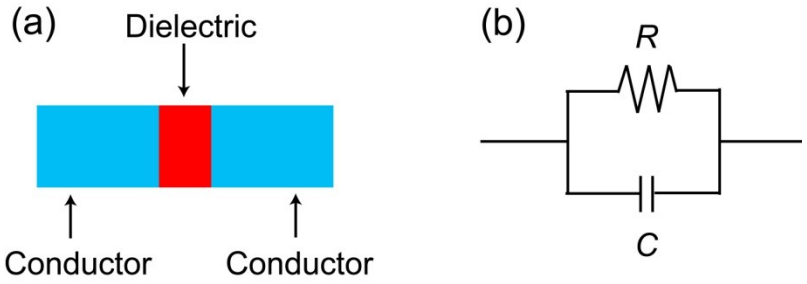


Figure 2-1 Tunnel Junction (a) Schematic of a tunnel junction (b) Equivalent circuit diagram of a tunnel junction

2.3 Double Barrier Tunneling Junction Devices

A double barrier tunneling junction device consists of two conductors in between which a metal nanoparticle or a quantum dot is placed, separated from each of the conducting electrodes by thin tunneling barriers. A schematic of a double barrier tunnel junction is shown in figure 2-2(a) and an equivalent circuit diagram is shown in figure 2-2(b). Typically these double barrier tunneling junctions are formed using scanning tunneling microscope (STM) where the tip of the microscope acts as one metal conductor or source electrode and the substrate on which the nanoparticle sits acts as another metal conductor or drain electrode.

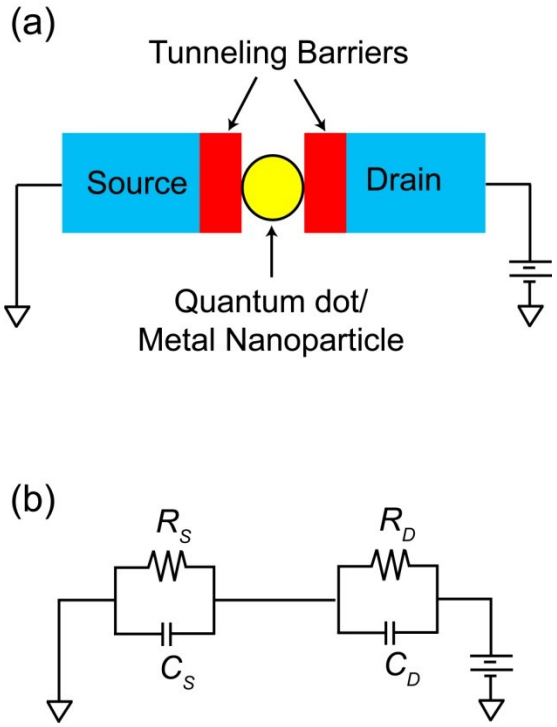


Figure 2-2 Double barrier tunneling junctions (a) Schematic of a double barrier tunneling junction device. (b) Equivalent circuit diagram of a double barrier tunneling junction device

When voltage is applied across the double barrier tunneling junction device the electrons start tunneling from the source electrode to the nanoparticle and from nanoparticle to the drain electrode. Depending on the type of nanoparticle we see different electrical characteristics. In metal nanoparticles we have continuous energy levels and hence when a metal nanoparticle is present in between the electrodes we observe only charging energy in the electrical characteristics. Charging energy is the energy required to transfer or tunnel an extra electron from the source electrode on to the metal nanoparticle. Whereas when we have a quantum dot which has discrete energy levels we can see the energy level structure of the quantum dot and this technique is

called as tunneling spectroscopy. Traditionally STM was used to study the energy levels of quantum dots and it is termed as scanning tunneling spectroscopy (STS) [2.1-2.15]. A more detailed discussion on tunneling spectroscopy of quantum dots will be presented in the following sections of this chapter. This discussion was previously presented in the thesis work of Ramkumar Subramanian [2.16], but an attempt is made to explain it in further detail in order to achieve completeness of this work.

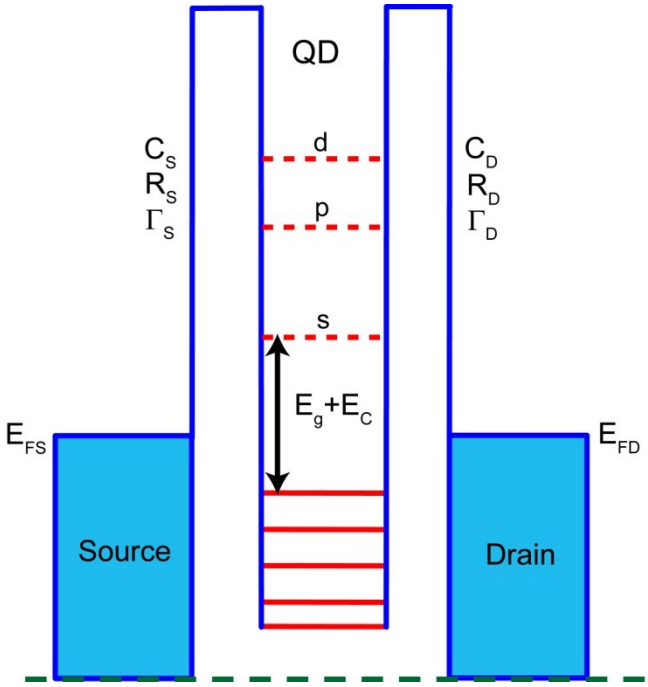


Figure 2-3 Energy diagram of a double barrier tunnel junction with a quantum dot. E_{FS} and E_{FD} are Fermi levels of the source electrode and drain electrode. C_S, R_S, and Γ_S are the capacitance, resistance and tunneling rate of tunnel junction between the source electrode and the quantum dot. C_D, R_D, and Γ_D are the capacitance, resistance and tunneling rate of tunnel junction between the source electrode and the quantum dot. E_g is the band gap of the quantum dot and E_c is the charging energy.

Let us consider a double barrier tunnel junction with a quantum dot in between two metal electrodes separated from each of them by a tunneling barrier. The characteristics of each tunnel junction are defined by the tunneling capacitance (C), tunneling resistance (R) and the tunneling rate (Γ) of the tunnel junction. We can designate the metal electrodes as source and drain electrodes with Fermi levels E_{FS} and E_{FD} respectively and since the quantum dot has discrete energy levels like an artificial atom the we can designate the discrete energy levels as s, p, d and so on. If we look at the energy diagram of the double barrier tunneling junction with quantum dot it will look like the energy diagram shown in figure 2-3.

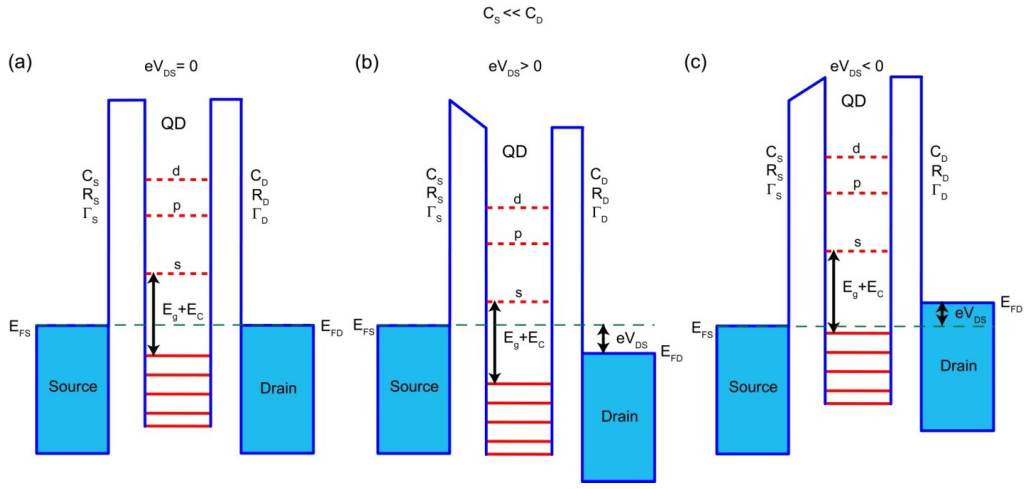


Figure 2-4 Schematics of energy diagrams and their response to voltage bias (a) When no source-drain voltage is applied the Fermi levels of both the source and drain electrodes are aligned to the Fermi level of the quantum dot. (b) When a positive voltage is applied the drain electrode and the quantum dot energy levels start moving down. (c) When a negative voltage is applied the drain electrode and the quantum dot will start moving upward. Note: For simplicity it is assumed that entire the voltage drop is across

the source tunnel junction which has lower capacitance C_S and that the drain and the quantum dot are capacitively coupled whose tunnel junction capacitance C_D is larger.

The electrical measurements done on such DBTJ with quantum dot can yield us information about the band gap and energy level spacing of the quantum dots. This is also termed as electron tunneling spectroscopy or resonant tunneling spectroscopy. Depending on the junction parameters of both the tunnel junctions of DBTJ that is C_S, R_S, Γ_S, C_D, R_D, and Γ_D we can have two different regimes of tunneling spectroscopy. The first scenario is when the incoming electron tunneling rate Γ_S is much slower than the outgoing electron tunneling rate Γ_D, where only the spacing between the energy levels is seen which is also called as shell tunneling regime of tunneling spectroscopy. In the second case when the incoming electron tunneling rate Γ_S is much faster than the outgoing electron tunneling rate Γ_D, where the degeneracy of the energy levels is lifted which is called as shell-filling regime of tunneling spectroscopy. A more detailed explanation with energy diagrams is presented in the later part of this chapter.

In figure 2-4(a) when no voltage is applied to the electrodes the Fermi levels of the both electrodes are aligned to the Fermi level of the quantum dot. When a positive voltage is applied to the drain electrode the chemical potential of the drain electrode decreases and it start to move down as shown in figure 2-4(b). If we apply larger positive bias voltages eventually the empty discrete energy levels in the conduction band of the quantum dot align to the Fermi level of the source electrode and the electrons start tunneling. If we apply a negative voltage to the drain electrode the chemical potential of the drain electrode increases and Fermi level of drain electrode and the quantum dot starts to move up as shown in figure 2-4(c). When enough negative voltage is applied the electrons from the quantum dot valence band will start tunneling to the source electrode.

For simplicity of explanation it is assumed that the entire voltage drop across the device is across the source tunnel junction.

2.3.1 Shell-Tunneling Regime of Tunneling Spectroscopy

In this case the capacitance of source tunnel junction is much smaller than the capacitance of drain tunnel junction $C_S << C_D$ and the resistance of source tunnel junction is much larger than the drain tunnel junction $R_S >> R_D$. Hence the tunneling rate from source to quantum dot Γ_S is much smaller than the tunneling rate from quantum dot to drain Γ_D, and Γ_S becomes the limiting factor for tunneling current. When an electron tunnels from source to the quantum dot under suitable energy conditions, it immediately tunnels out to the drain electrode as the tunneling rate out of the quantum dot Γ_D is significantly larger than the tunneling rate into the quantum dot Γ_S. A schematic representation of this scenario with the aid of energy diagram is presented in figure 2-5 to figure 2-7.

As discussed earlier, when a positive bias is applied to the drain electrode the chemical potential of the drain electrode decreases and the drain electrode along with the quantum dot will move down in the energy diagram. When enough positive voltage is applied the Fermi level of the source electrode aligns with the empty energy level (s-level) in the conduction band of quantum dot. When this happens, a tunneling path opens for an electron to tunnel from the source electrode into the s-level of the quantum dot as shown in figure 2-5(a). This will be seen in the current voltage measurement as a stepwise increase in current with voltage and the particular step in current is denoted as position of s-level of the quantum dot. The s-level of quantum dot consists of two energy states one for positive spin electron and the other for negative spin electron. The electron tunneling to the quantum dot can be of either spin.

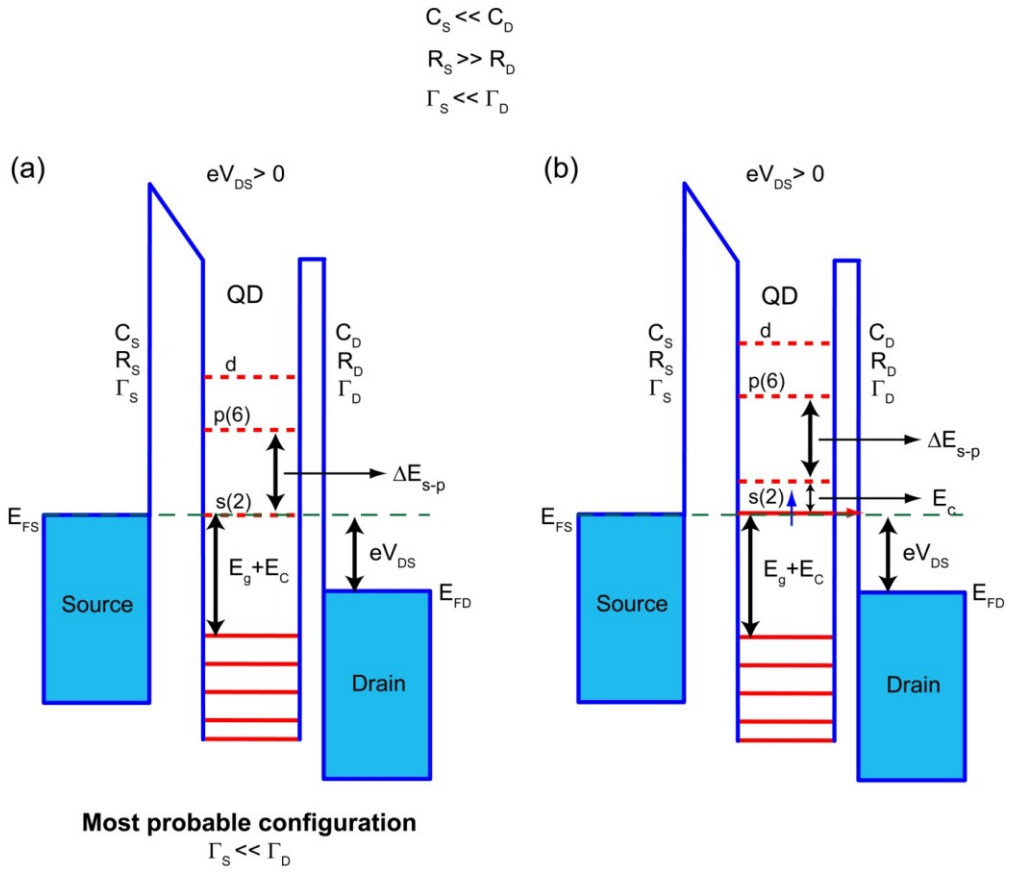


Figure 2-5 Shell tunneling regime of tunneling spectroscopy – electron tunneling through empty s-level of the quantum dot conduction band (a) When enough positive voltage bias is applied to the drain electrode the Fermi level of source electrode aligns with the empty s-energy level of the quantum dot conduction band. This is the most probable configuration as $\Gamma_D >> \Gamma_S$. As soon as electron tunnels to the quantum dot it tunnels out of the quantum dot. (b) An electron tunneling path opens and electrons start tunneling from source electrode through the quantum dot to the drain electrode. Red dotted lines in the quantum dot represent empty energy levels of quantum dot where as solid red lines represent filled energy states.

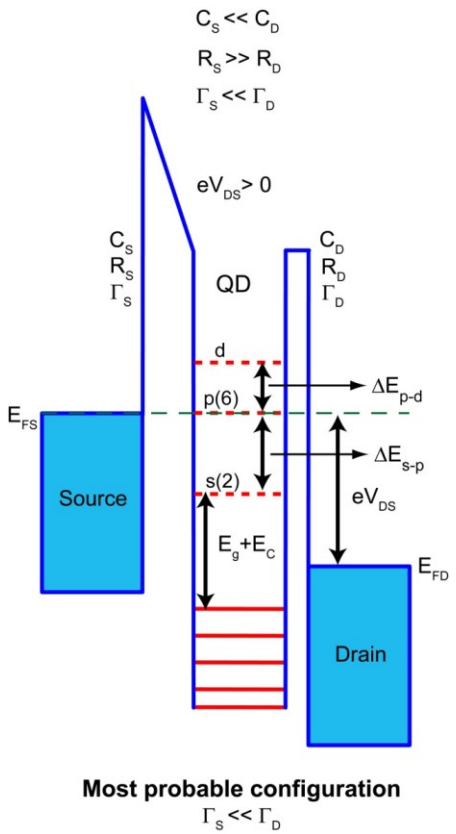


Figure 2-6 Shell tunneling regime of tunneling spectroscopy – electron tunneling through empty s and p-levels of the quantum dot conduction band. When enough positive voltage bias is applied to the drain electrode the Fermi level of source electrode aligns with the empty p-energy level of the quantum dot conduction band. This is the most probable configuration as $\Gamma_D >> \Gamma_S$. As soon as electron tunnels to the quantum dot it tunnels out of the quantum dot. Red dotted lines in the quantum dot represent empty energy levels of quantum dot where as solid red lines represent filled energy states.

As soon as the electron tunnels to the quantum dot the chemical potential of the quantum dot increases and the degeneracy of the s-level of quantum dot is lifted as

shown in figure 2-5(b). But, the tunneling rate out of the quantum dot is much faster than the tunneling rate into the quantum dot so the probability of the quantum dot having an extra electron is zero pertaining to the tunneling rates. Hence, the most probable state of the quantum dot will be with no extra electrons as shown in figure 2-5(a). The electrons tunneling through the quantum dot s-level can be of either spin and in current voltage measurements we will see a single step-wise increase in current due to the alignment of s-energy level to the Fermi level of source. When we consider the differential conductance measurements, a peak in conductance will be observed due to this electron tunneling from source electrode to the quantum dot s-level to the drain electrode.

When the positive voltage bias on the drain electrode is increased further, the chemical potential of the drain electrode decreases further and it moves along with the quantum dot further down in the energy diagram. When enough positive voltage is applied to the drain electrode the Fermi level of the source electrode aligns with the empty state of p-energy level in the quantum dot conduction band as shown in figure 2-6. Until this point the current through the device remains constant and once this alignment happens there is new tunneling paths open for electrons to tunnel from source to drain electrode through the p-level of the quantum dot. So we see another step-wise increase in current in the current voltage measurement due to this alignment of source Fermi level and the p-level of quantum dot. This step in current is attributed to the new tunneling paths that are open due to this alignment and the step is denoted as p which signifies the position of the p-level in the quantum dot. Figure 2-6 represents the most probable configuration, as the rate of electrons tunneling out of the quantum dot is much faster than the rate of electrons tunneling into the quantum dot. The same argument that we made for tunneling of electrons through the s-level holds good for the p-level too. So the degeneracy of the energy levels cannot be broken when the tunneling rate of electron

tunneling out of the quantum dot is faster than the electrons tunneling into the quantum dot. The probability of finding an extra electron on the quantum dot is always zero in this scenario and hence the name shell-tunneling regime of tunneling spectroscopy.

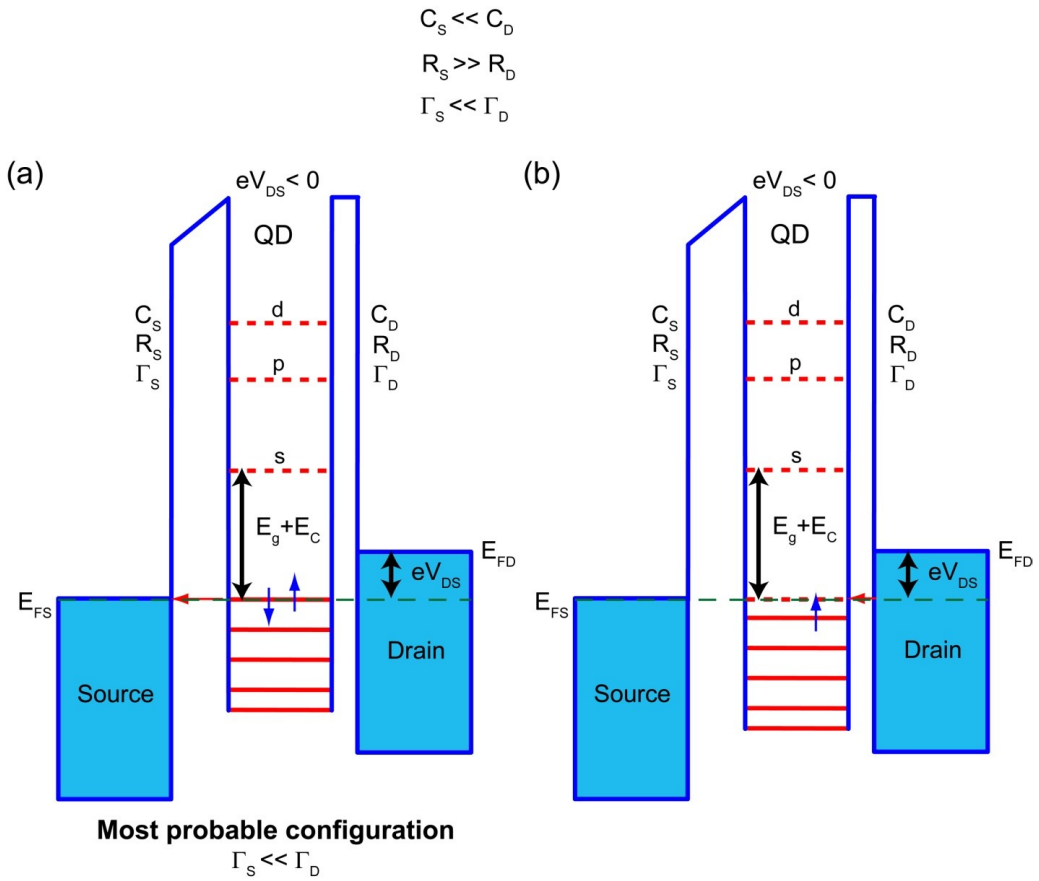


Figure 2-7 Shell tunneling regime of tunneling spectroscopy – electron tunneling through filled states of the quantum dot valence band (a) When enough negative voltage bias is applied to the drain electrode the Fermi level of source electrode aligns with the filled energy levels of quantum dot valence band. This is the most probable configuration as $\Gamma_D >> \Gamma_S$. As soon as electron tunnels out of the quantum dot to the source another tunnels into the quantum dot from the drain electrode. (b) An electron tunneling path opens and electrons start tunneling from quantum dot filled states to the quantum to the

source electrode. The degeneracy of the energy level is lifted and the chemical potential of quantum dot drops by charging energy. Red dotted lines in the quantum dot represent empty energy levels of quantum dot where as solid red lines represent filled energy states.

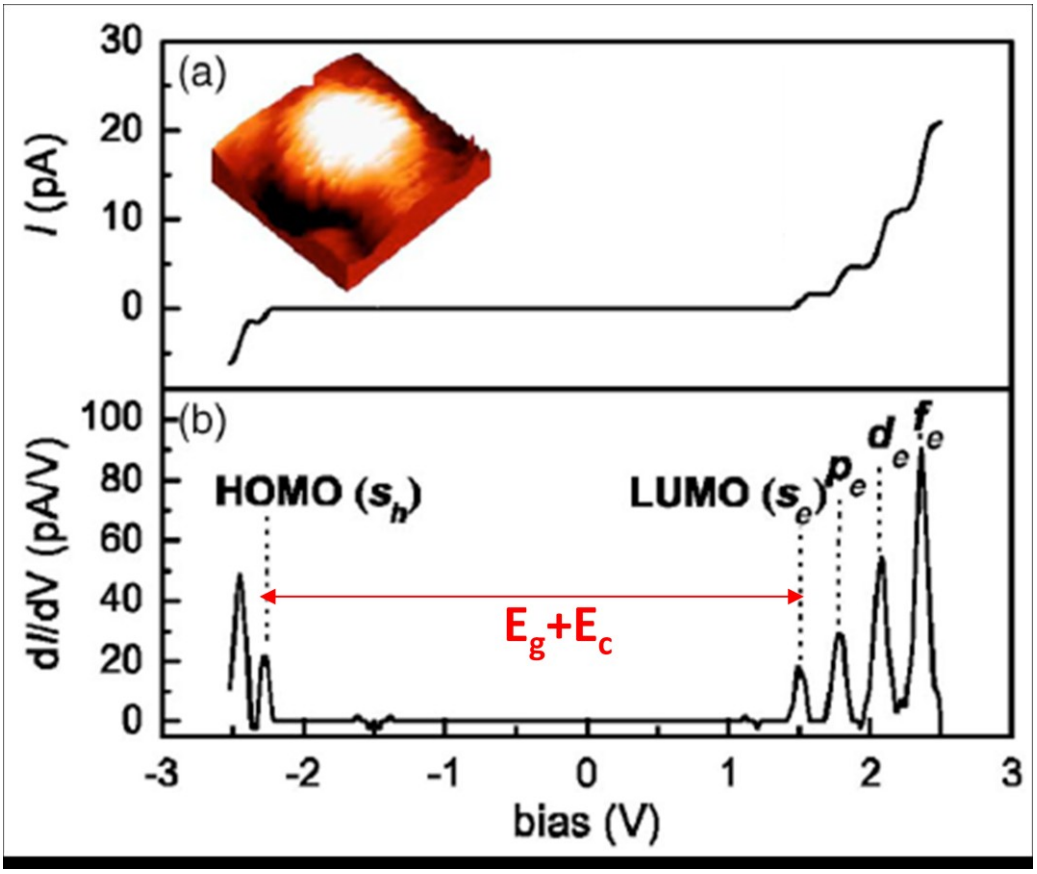


Figure 2-8 Shell tunneling spectroscopy data of ~3.9 nm CdSe quantum dot obtained using STM spectroscopy at cryogenic temperatures (4.5K) [2.14] (a) Current voltage measurements (b) Differential conductance measurements

As discussed earlier in this chapter when we apply negative bias to the drain electrode the chemical potential of the drain electrode increases and the drain electrode along with the quantum dot moves up in the energy diagram with respect to the Fermi level of source electrode. When enough negative voltage is applied to the drain electrode, the filled energy state in the valence band of the quantum dot aligns with the Fermi level of the source as shown in figure 2-7(a). This opens up a tunneling path for the electrons from the quantum dot to the source electrode. This can also be perceived as tunneling of hole from the source electrode to the quantum dot. As the electron tunnels from the highest occupied energy level in quantum dot valence band to the source electrode, the degeneracy of the energy state is lifted, as shown in figure 2-7(b). But, the tunneling rate between the drain and quantum dot is much faster than the tunneling rate between the source and quantum dot, as soon as an electron tunnels out of quantum dot into source electrode, it is filled by another electron tunneling from drain to the quantum dot. Hence the most probable configuration in this scenario is shown in figure 2-7(a).

When we further increase the negative voltage bias on the drain electrode we can open more tunneling paths from even lower filled states of the quantum dot valence band which will appear as a step wise increase in negative current. In the case of shell tunneling regime of the current voltage measurements and the differential conductance measurements yield us the information of the spacing between the energy levels without breaking the degeneracy of the energy levels. Figure 2-8 shows

2.3.2 Shell-Filling Regime of Tunneling Spectroscopy

In this case the capacitance of source tunnel junction is much smaller than the capacitance of drain tunnel junction $C_S << C_D$ and the resistance of source tunnel junction is also much smaller than the drain tunnel junction $R_S << R_D$. Hence the tunneling rate

from source to quantum dot Γ_S is much larger than the tunneling rate from quantum dot to drain Γ_D, and Γ_D becomes the limiting factor for tunneling current.

When an electron tunnels from source to the quantum dot under suitable energy conditions, it stays in the quantum dot – lifts the degeneracy of the quantum dot energy levels as Γ_D is significantly larger than the tunneling rate into the quantum dot Γ_S. A schematic representation of this scenario with the aid of energy diagram is presented in figure 2-9 to figure 2-11. As discussed earlier, when a positive bias is applied to the drain electrode the chemical potential of the drain electrode decreases and the drain electrode along with the quantum dot will move down in the energy diagram. When enough positive voltage is applied the Fermi level of the source electrode aligns with the empty energy level (s-level) in the conduction band of quantum dot. When this happens, a tunneling path opens for an electron to tunnel from the source electrode into the s-level of the quantum dot as shown in figure 2-9(a). As soon as the electron tunnels to the quantum dot the chemical potential of the quantum dot increases and the degeneracy of the s-level of quantum dot is lifted by charging energy of the quantum dot E_c as shown in figure 2-9(b).

Here, the tunneling rate out of the quantum dot is much slower than the tunneling rate into the quantum dot so the probability of the quantum dot having an extra electron is very high pertaining to the tunneling rates. Hence, the most probable state of the quantum dot will be with an extra electron on the quantum dot as shown in figure 2-9(b). When we further increase the positive bias on the drain electrode by E_c, another electron of opposite spin will start tunneling from the source electrode through the quantum dot to drain electrode as shown in figure 2-10.

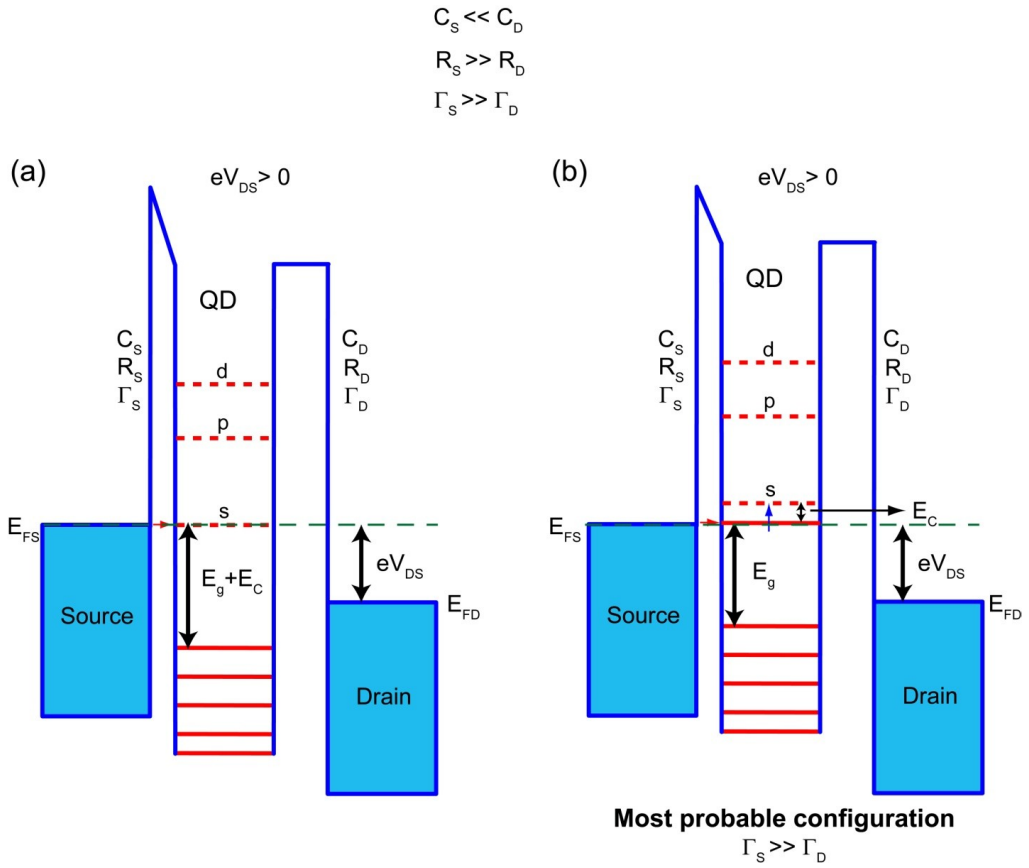


Figure 2-9 Shell filling regime of tunneling spectroscopy – electron tunneling through empty s-level of the quantum dot conduction band (a) When enough positive voltage bias is applied to the drain electrode the Fermi level of source electrode aligns with the empty s-energy level of the quantum dot conduction band. (b) The s-level of quantum dot is occupied by an electron tunneling from the source electrode and then tunnels out of the quantum dot. The degeneracy of the s-level is lifted due to the extra electron in quantum dot. This is the most probable configuration as $\Gamma_S >> \Gamma_D$. Red dotted lines in the quantum dot represent empty energy levels of quantum dot where as solid red lines represent filled energy states

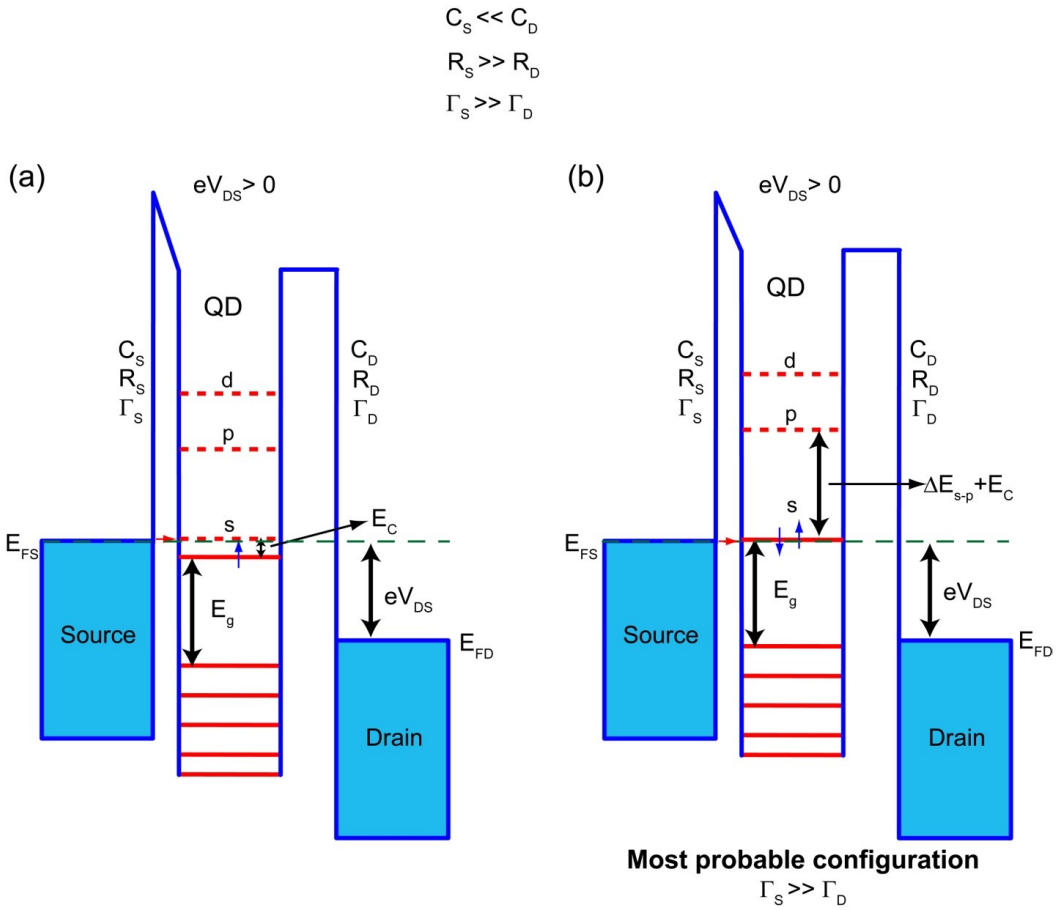


Figure 2-10 Shell filling regime of tunneling spectroscopy – electron tunneling through empty s-level of the quantum dot conduction band (a) When positive voltage bias on drain electrode is further increased by E_c, Fermi level of source electrode aligns with the empty s-energy level of the quantum dot conduction band. (b) An second electron of opposite spin tunnels into the s-level of the quantum dot. This is the most probable configuration as $\Gamma_S >> \Gamma_D$. Red dotted lines in the quantum dot represent empty energy levels of quantum dot where as solid red lines represent filled energy states

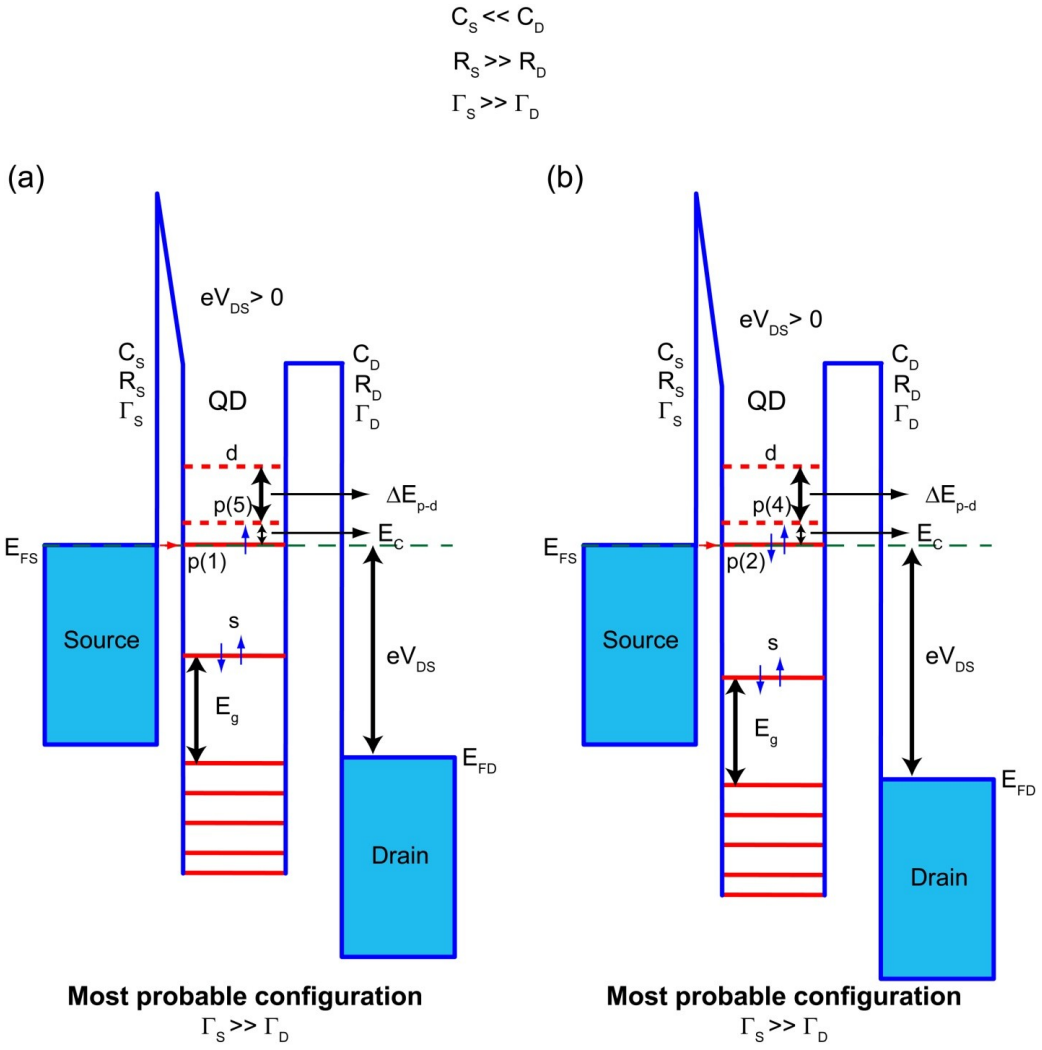


Figure 2-11 Shell filling regime of tunneling spectroscopy – electron tunneling through empty p-level of the quantum dot conduction band (a) When positive voltage bias on drain electrode is further increased by $\Delta E_{s\text{-}p}+E_c$, Fermi level of source electrode aligns with the empty p-energy level of the quantum dot conduction band. an electron starts tunneling through this state lifting the degeneracy of p-level simultaneously. (b) An second electron of opposite spin starts tunneling through the p-level of the quantum dot. These are the most probable configuration as $\Gamma_S >> \Gamma_D$. Red dotted lines in the quantum

dot represent empty energy levels of quantum dot where as solid red lines represent filled energy states

Hence, now the s-level of quantum dot is filled with two electrons and current voltage plot as another step in current, the size of the flat region of this step is equal to E_c, the charging energy of quantum dot. The electrons tunneling through the quantum dot s-level yields two steps in current voltage measurements separated by charging energy E_c. When we consider the differential conductance measurements, a two peak in conductance will be observed due to this electron tunneling from source electrode to the quantum dot s-levels to the drain electrode.

When the positive voltage applied to the drain electrode is further increased the Fermi level of the source electrode aligns with the p-level of the quantum dot conduction band. This is shown schematically using energy diagrams in figure 2-11. As the p-level can accommodate six electrons, we can see six steps in current voltage measurements due to electrons tunneling from the six states in p-level, each step is associated with an extra electron on the quantum dot. The width of these current steps will be equal to the charging energy E_c of the quantum dot. In the differential conductance plot, we can see six conductance peaks separated from each other by a value of E_c. Similarly, the same explanation with the aid of energy diagrams can be conducted for the shell tunneling regime of tunneling spectroscopy in the valence band of the quantum dot when a negative voltage is applied to the drain electrode. We will see the same effect of lifting of degeneracy in the valence band of the quantum dot too. Figure 2-12 shows the current voltage measurements and the differential conductance measurements done on a ~3.5nm InAs quantum dot in the shell filling regime of tunneling spectroscopy.

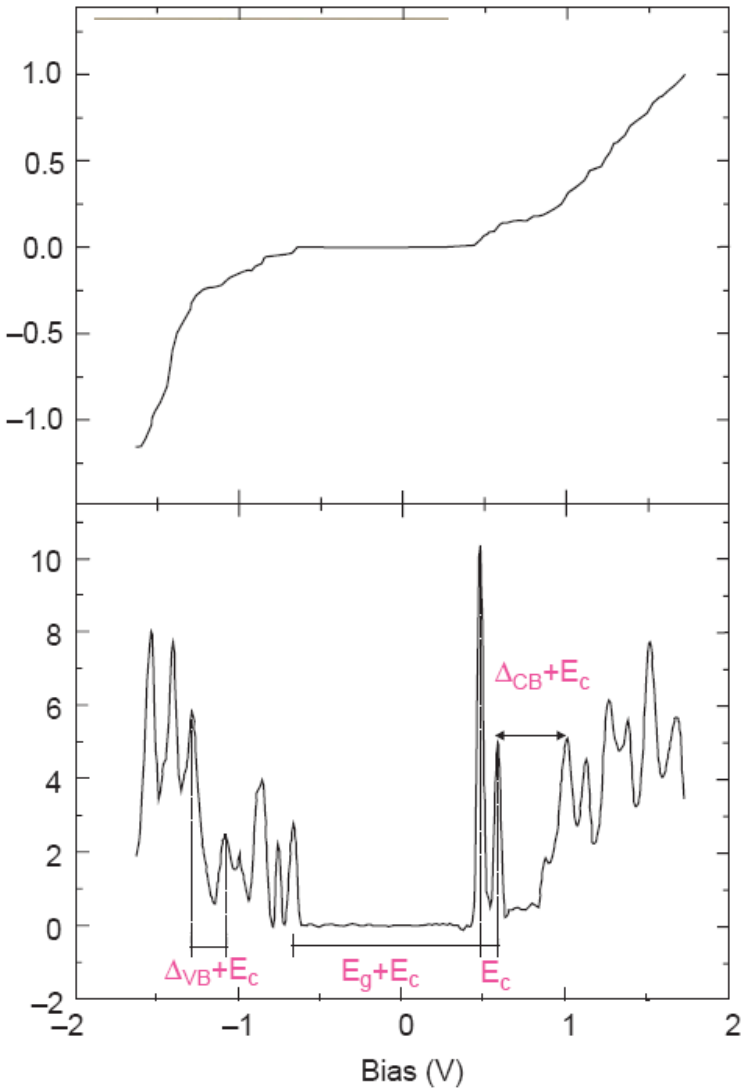


Figure 2-12 Shell filling spectroscopic measurement data of ~3.2 nm InAs quantum dot obtained using STM at 4.2K. Current-voltage measurements and differential conductance measurements show the degeneracy of the energy levels of quantum dot is lifted. Doublet peaks were seen for s-levels and six peaks were seen for the p-level of quantum dot. Peaks to peak separation for the same level conductance peaks is the charging

energy E_c. Peak to peak separation for conductance peaks due to different energy levels is the energy level spacing plus the charging energy [2.17]

In conclusion the electrical characteristics of double barrier tunneling junction devices with quantum dots can vary depending on the junction parameters of the tunnel junctions. The two regime of the tunneling spectroscopy are explained with the aid of energy diagrams. In our DBTJ devices we observe electrical characteristics in shell tunneling regime.

2.3.3 Voltage Division Factor

In the previous section of this chapter when discussing about different regimes of tunneling spectroscopy for the purpose of simplicity it was assumed that the voltage drop across the device is entirely in one of the junctions. But, in reality the voltage drop across the device is the sum of voltage drop across both the tunnel junctions of the device. And the ratio of these voltage drops across the two tunnel junctions is termed as voltage division factor. This ratio of voltage drop is directly related to the capacitance of the tunnel junctions and is given by $\eta = \frac{C_D}{C_S + C_D}$, C_s is the capacitance of source tunnel junction and C_D is capacitance of drain tunnel junction. To obtain the voltage division factor, we can calculate it from the above equation given the capacitances of the tunnel junctions are known.

Depending on the junction capacitances ratio η or the voltage division factor, the differential conductance peaks are offset in actual measurements. Let us consider a quantum dot placed in between two metal electrodes, having a configuration of parallel plate capacitor. In theory the capacitance of parallel plate capacitor is inversely

proportional to the distance between the plates. If the quantum dot is closer to one of the metal electrodes as shown in figure 2-13(a), the capacitance of this junction will be much higher compared to the other junction. In this case, the majority of voltage drop is across the junction with low capacitance and the value of voltage division factor will be close to unity. Let's approximate the voltage division factor η to be 0.98, for the DBTJ shown in figure 2-13(a). Now let us consider another DBTJ of same configuration where the quantum dot is almost at the center of the structure as shown in figure 2-13(b). Here, the capacitances of both the junctions will be almost equal, let's approximate the voltage division factor η to be 0.52, for the DBTJ shown in figure 2-13(a). Assuming that both the quantum dots are of same material and size, and assuming that the DBTJ device is being operated in shell tunneling regime, we expect to see same electrical characteristics from both the devices. But, the tunneling spectra can be completely different. For instance, if we consider differential conductance spectra obtained from the devices, they will look as shown in figure 2-13(c) and 2-13(d). The peak to peak separation will be different and the width of the peak itself will be different. But, we know that both the differential conductance spectra are from essentially same quantum dot and should look the same. The difference seen in the differential conductance spectra is due to the voltage division factor η .

So, after obtaining the electrical data from the DBTJ devices with quantum dots, it is very important to compensate the data with voltage division factor η in order to obtain the real energy level separations and the real peak widths of the differential conductance peaks which give a plethora of information about temperature dependence of measurements.

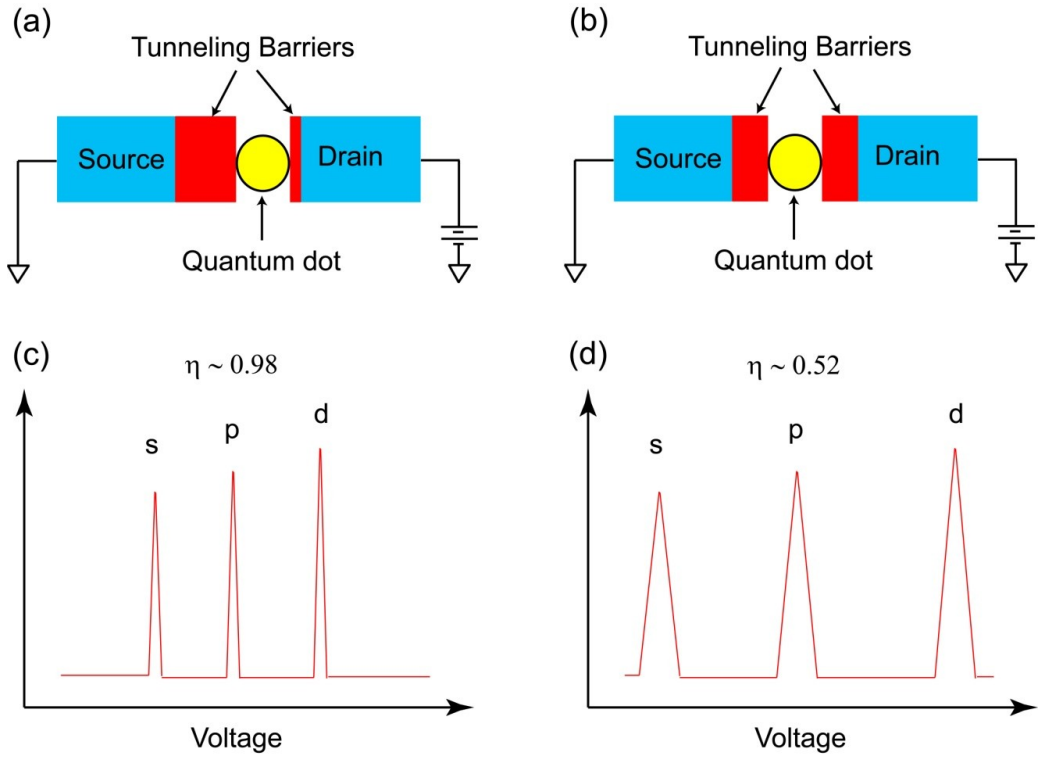


Figure 2-13 Effect of voltage division factor η on the differential conductance measurements [2.16] (a) Schematic of DBTJ device (a) QD is closer to one electrode giving rise η factor close to unity. (b) QD is almost at the center giving rise to η factor close to ~0.5. (c) Differential conductance spectra of DBTJ devices with large η factor (d) Differential conductance spectra of DBTJ devices with small η factor

The following method to obtain voltage division factor is adapted from the paper titled " Energy-filtered cold electron transport at room temperature" (P. Bhadrachalam, R. Subramanian, V. Ray, L.-C. Ma, W. Wang, J. Kim, K. Cho and S.J. Koh). A way to obtain the voltage division factor is to calculate it from the measured band gap or the zero conductance region V_g^{meas} of the current voltage measurement of the DBTJ device and

the optical band gap $E_g^{optical}$ of the quantum dot. The zero conductance region in electrical measurement essentially represents the band gap of the quantum dot in DBTJ device. The optical band gap is related to the measured band gap in the resonant tunneling spectroscopy by the following relation [2.1]

$$\eta e V_g^{meas} = E_g^{optical} + E_{e-h} \tag{2-1}$$

where e is the elementary charge of electron, V_g^{meas} is the measured band gap or the zero conductance region from the electrical measurements and E_{e-h} is the electron-hole coulomb interaction energy,. This interaction energy E_{e-h} can be approximately calculated by the following [2.17-2.21]

$$E_{e-h} = \frac{1.79e^2}{4\pi\varepsilon_0\varepsilon_{in}R} \tag{2-2}$$

where ε_0 is the permittivity of free space, ε_{in} is the dielectric constant of the bulk material of the QD. From the above equations η can be given as

$$\eta = \left[E_g^{optical} + \frac{1.79e^2}{4\pi\varepsilon_0\varepsilon_{in}R} \right] \Big/ eV_g^{meas} \tag{2-3}$$

The η factor can then be determined from above equation by obtaining literature data for the optical band gap for the QD under study, calculating the electron-hole interaction energy, and the measuring zero conductance energy gap V_g^{meas} from the electrical measurement of DBTJ device with QD.

In conclusion for this chapter, the tunnel junctions were introduced and tunneling concepts including tunneling through double barrier tunnel junctions were presented.

Using simple energy diagrams different regimes of tunneling through DBTJ devices and the expected tunneling spectra was explained. The effect of voltage division factor on tunneling spectra was discussed and calculation method for compensating this voltage division factor is presented, which will be used in chapter 6 while interpreting the data from DBTJ devices.

Chapter 3

Electron Cooling Effect – Energy Filtering

3.1 Introduction

In this chapter a brief introduction to electron cooling effect or the energy filtering of thermally excited electrons to create cold electrons is provided. In the previous chapter an introduction to double barrier tunneling junction devices was given and different regimes of resonant tunneling of electrons through quantum dots was discussed. Here, the Fermi-Dirac thermal smearing of electrons and its effect on the electrical characteristics of DBTJ quantum dot devices will be discussed. Then, double quantum dot devices are introduced and energy filtering phenomenon, which suppresses Fermi-Dirac thermal smearing, observed in double quantum dot devices at cryogenic temperatures will be discussed in detail.

3.2 Fermi-Dirac Thermal Smearing

Fermi-Dirac distribution is the fundamental property which governs the distribution of electron energies in solids. At higher temperatures this energy distribution of electrons broadens to such an extent that, it hinders proper functioning of many electronic [3.1-3.3], opto-electronic and spintronic devices [3.4-3.5]. This broadening of electron energy distribution at high temperatures is termed as Fermi-Dirac thermal smearing of electrons. In DBTJ devices also the Fermi-Dirac thermal smearing plays a vital role. At room temperature due to smeared out distribution of electron energies the step-wise increase in current may not be observed depending on the separation between the adjacent energy levels. So, if the separation between the adjacent energy levels is very small the signature of these energy levels is difficult to be seen in the current-voltage

measurements of the DBTJ device with quantum dot. This happens because of the thermal smearing of electron energies.

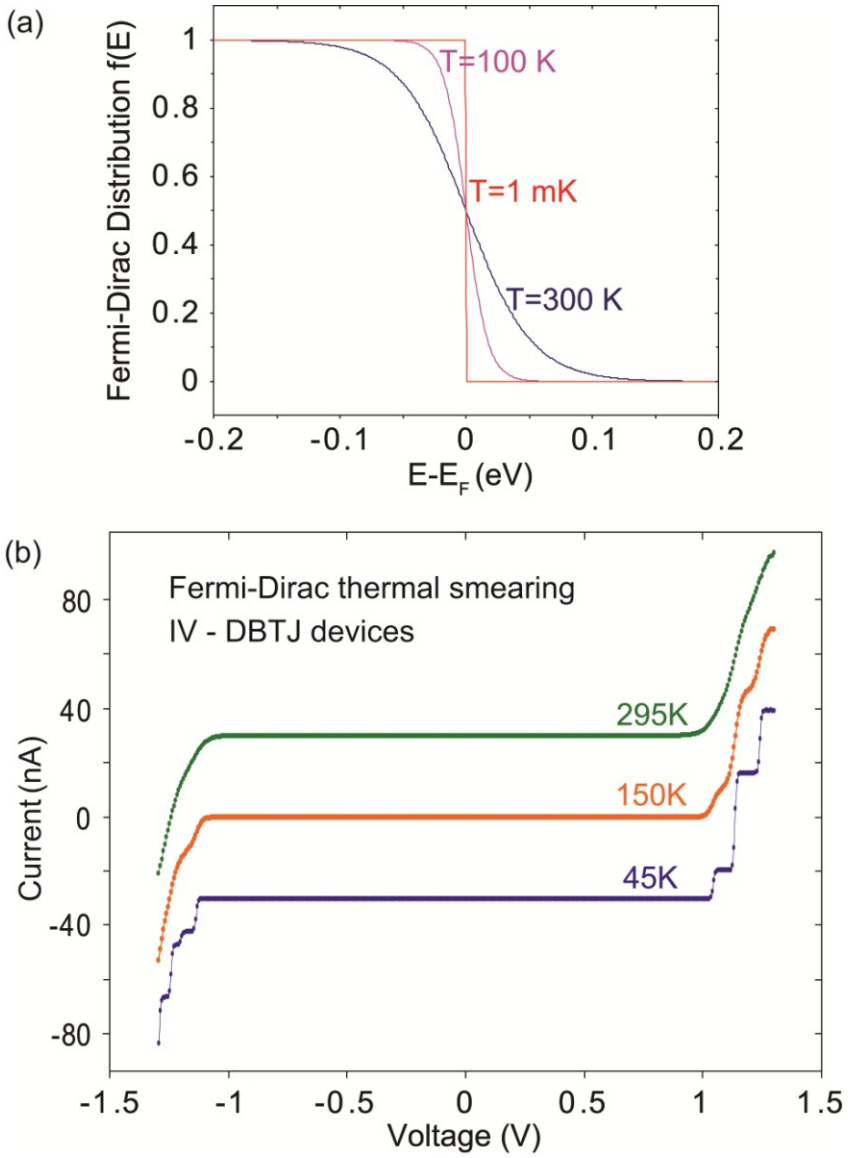


Figure 3-1 Effect of Fermi-Dirac thermal smearing. (a) Fermi-Dirac distribution function at different temperatures (b) Calculated IV characteristics of DBTJ devices at different temperatures

In figure 3-1(a) the Fermi-Dirac distribution or electron energy distribution for different temperatures is shown. As can be seen from figure 3-1(a) the electron energy distribution smears out as the temperature increases. In figure 3-1(b) the simulated current voltage plots of a DBTJ device with quantum dot is shown for different temperatures. As can be seen from figure 3-1(b) at low temperatures the current voltage plots show step-wise increase in current and each jump in current indicates a discrete energy level in the quantum dot aligning to the Fermi level of the source electrode. As the temperature increase these steps smear out due to Fermi-Dirac thermal smearing and at room temperature these steps completely smear out making it impossible to study the energy levels in the quantum dots.

The effect of Fermi-Dirac thermal smearing on the electrical characteristics of is further investigated by theoretically calculating the current through the DBTJ devices with a quantum dot having one single energy level as shown figure 3-2. The following Fermi-Dirac full width half maximum calculations were from the paper titled “Energy-filtered cold electron transport at room temperature” (P. Bhadrachalam, R. Subramanian, V. Ray, L.-C. Ma, W. Wang, J. Kim, K. Cho and S.J. Koh). A quantum dot with one single energy state is considered as shown in figure 3-2 and the current through the quantum dot energy level as voltage is applied is calculated. From the current voltage plots the differential conductance was calculated analytically and the full width half maximum (FWHM) of this differential conductance was obtained. The origin of the width of the differential conductance peak is from the Fermi-Dirac thermal smearing of electrons in the electrodes. For the calculation of FWHM from Fermi-Dirac thermal smearing a DBTJ device in Shell-tunneling regime is considered. Since there is no charge accumulation Γ_S is much smaller than Γ_D (Γ_S and Γ_D: the tunneling rate through tunneling barrier 1 and tunneling barrier 2, respectively); once an electron tunnels from the source to the QD, it

tunnels out to the drain before the other electron from the source tunnels into the QD. Hence the current is determined by Γ_S, the slower rate or the rate determining step. $\Gamma_S(E,V)$, the electron tunneling rate from the source to the QD at electron energy E and voltage bias V, is given by

$$\Gamma_S(E,V) = 2\frac{2\pi}{\hbar}\rho_S(E)\rho_{QD}(E+\eta eV)\left|T(E)\right|^2 f(E) \qquad (3\text{-}1)$$

where $\rho_S(E)$ and $\rho_{QD}(E)$ are the density of states for the source electrode and the QD, respectively, $f(E)$ is the Fermi-Dirac distribution function of the source with Fermi level at μ_S, η is the voltage division factor and $\left|T(E)\right|^2$ is the tunneling transmission probability.

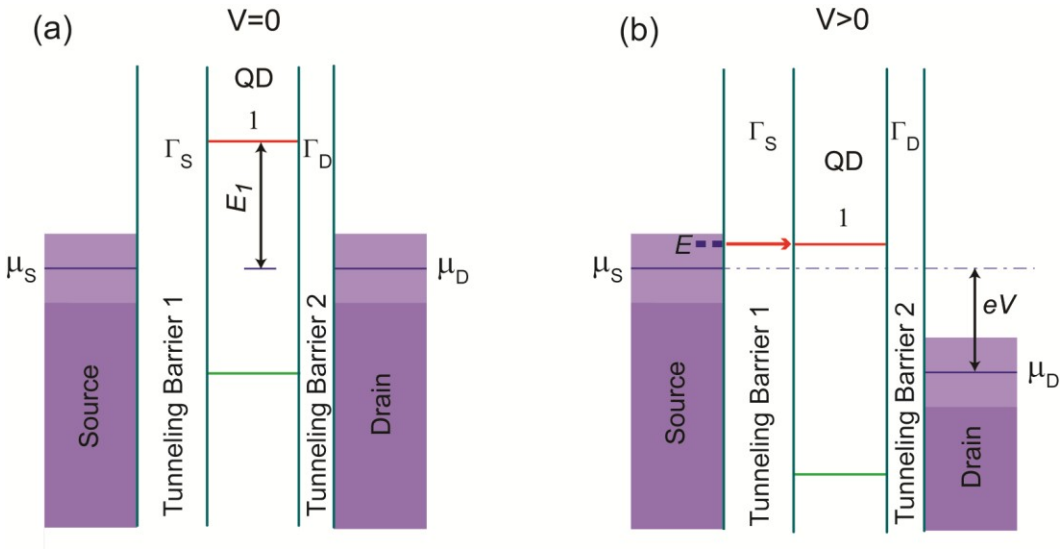


Figure 3-2 The energy diagram for a DBTJ (a) at zero voltage bias (b) positive voltage bias. The lightly shaded region around the Fermi-level of electrodes schematically represent the Fermi-Dirac thermal smearing at non-zero temperatures. When voltage bias is applied as shown in (b) electrons start tunneling even before the quantum dot energy level aligns with the Fermi-level of source electrode.

The current through the device $I(V)$ can then be calculated by integrating $\Gamma_S(E,V)$ with respect to energy E, as $\Gamma_S(E,V)$ is the slower rate or the rate limiting step. So current $I(V)$ is given as

$$I(V) = e\int_0^\infty \Gamma_S(E,V)dE \tag{3-2}$$

where e is the charge of an electron. The above equation (3-2) can be further simplified by approximating $\rho_S(E)$ and $T(E)$ with $\rho_S(E_F)$ and $T(E_F)$, respectively, where E_F ($\approx\mu_S$) is the Fermi energy of the source electrode [3.6], then equation (3-2) transforms as following

$$I(V) = \frac{4\pi e}{\hbar}\int_0^\infty \rho_S(E_F)\rho_{QD}(E+\eta eV)|T(E_F)|^2 f(E)dE$$

$$I(V) \cong \frac{4\pi e}{\hbar}\rho_S(E_F)|T(E_F)|^2\int_0^\infty \rho_{QD}(E+\eta eV)f(E)\,dE$$

$$I(V) \cong \frac{g_0}{e}\int_0^\infty \rho_{QD}(E+\eta eV)f(E)\,dE \tag{3-3}$$

$$\text{where } g_0 = \frac{4\pi e^2}{\hbar}\rho_S(E_F)|T(E_F)|^2$$

Here, $\rho_{QD}(E)$ represents the discrete energy state of the quantum dot which is given by a delta function,

$$\rho_{QD}(E) = \delta(E-(E_1+\mu_S)) \tag{3-4}$$

where E_1 is the energy for the QD level 1, with respect to its reference energy that is the Fermi-level of the source electrode μ_S as show in figure 3-2(a)). From equations (3-4) and (3-3), we get

$$I(V) \cong \frac{g_0}{e} f(E_1 + \mu_S - \eta eV)$$

$$I(V) \cong \frac{g_0}{e} f(\mu_S + (E_1 - \eta eV)) = \frac{g_0}{e} \frac{1}{e^{(E_1 - \eta eV)/kT} + 1} \qquad (3\text{-}5)$$

The above equation (3-5) derived for current through the quantum dot indicates that when there is no charge accumulation on the quantum dot, the current through the device is a function of Fermi-Dirac distribution. Assuming that the quantum dot energy level is a 1eV from the Fermi-level of the source electrode, the current through the device is plotted in figure 3-3.

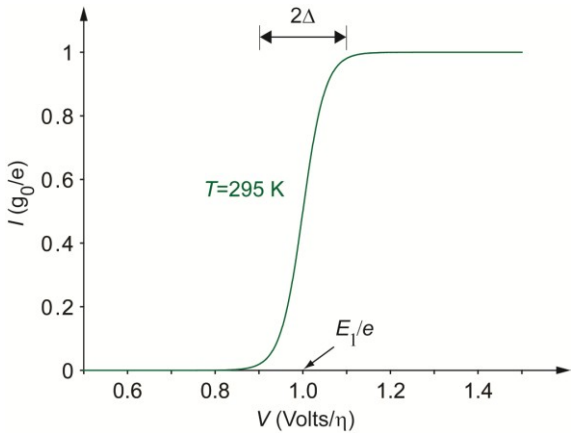


Figure 3-3 I-V characteristics resulting from the Fermi-Dirac thermal smearing. The I-V relationship from equation (3-5) with the QD energy level E_1 at 1.0 eV and T = 295 K. Δ = ~90 mV.

Differentiating equation (3-5) will give us the differential conductance through the device, which is then given by

$$\frac{dI(V)}{dV} = \frac{\eta g_0}{kT} \frac{e^{(E_1-\eta eV)/kT}}{\left[e^{(E_1-\eta eV)/kT}+1\right]^2} \tag{3-6}$$

Figure 3-4 shows the plot of differential conductance as a function of voltage. The maximum *dI/dV* is obtained when $V = E_1/\eta e$, The value of maximum differential conductance is then given by the following

$$\left(\frac{dI}{dV}\right)_{\max} = \left.\frac{dI(V)}{dV}\right|_{V=\frac{E_1}{\eta e}} = \frac{1}{4}\frac{\eta g_0}{kT} \tag{3-7}$$

Let us assume the voltages V_{HM}^{+} and V_{HM}^{-} are voltage values at half of the $(dI/dV)_{max}$ as shown in figure 3-4. These values of V_{HM}^{+} and V_{HM}^{-} can be obtained from the above equations and by solving the following equation,

$$\frac{1}{2}\left(\frac{dI}{dV}\right)_{\max} = \frac{\eta g_0}{kT} \frac{e^{(E_1-\eta eV)/kT}}{\left[e^{(E_1-\eta eV)/kT}+1\right]^2} \tag{3-8}$$

$$\frac{1}{2}\left(\frac{1}{4}\frac{\eta g_0}{kT}\right) = \frac{\eta g_0}{kT} \frac{e^{(E_1-\eta eV)/kT}}{\left[e^{(E_1-\eta eV)/kT}+1\right]^2}$$

$$\left[e^{(E_1-\eta eV)/kT}+1\right]^2 = 8e^{(E_1-\eta eV)/kT}$$

$$\left[e^{(E_1-\eta eV)/kT}\right]^2 - 6e^{(E_1-\eta eV)/kT} + 1 = 0 \tag{3-9}$$

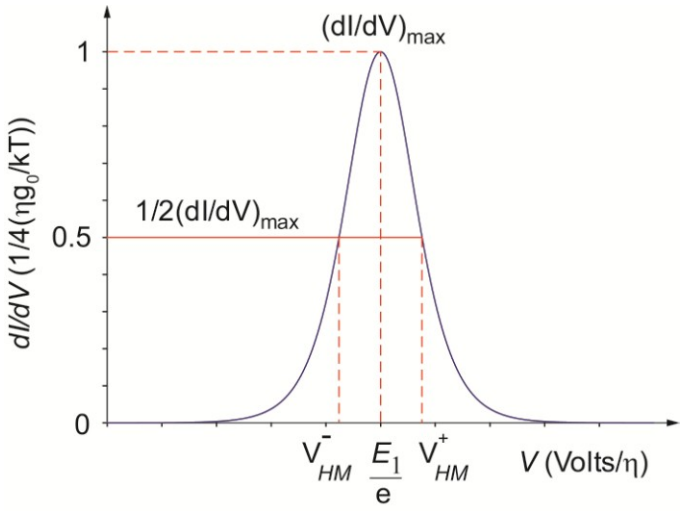


Figure 3-4 The differential conductance, dI(V)/dV, that results from the Fermi-Dirac thermal smearing. V_{HM}^{+} and V_{HM}^{-} are the bias voltages that give the half of the maximum differential conductance value.

By solving above equation (3-9),we obtain two values for voltage V (V_{HM}^{+} and V_{HM}^{-}) which are given by

$$V_{HM}^{+} = \frac{E_1}{\eta e} - \frac{kT}{\eta e}\ln\left(3-2\sqrt{2}\right)$$
$$V_{HM}^{-} = \frac{E_1}{\eta e} - \frac{kT}{\eta e}\ln\left(3+2\sqrt{2}\right) \quad (3\text{-}10)$$

Hence the FWHM of the differential conductance can be obtained (in energy unit) by calculating the difference as shown below

$$FWHM = \eta e\left(V_{HM}^{+} - V_{HM}^{-}\right)$$
$$= kT[\ln(3+2\sqrt{2}) - \ln(3-2\sqrt{2})] = 3.52549\,kT \quad (3\text{-}11)$$

So from the above calculations it can be seen that at a sample temperature T, the minimum FWHM of the conductance peak of differential conductance measurements of a DBTJ device with quantum dot will be at least ~3.5kT where, k is the Boltzmann constant. Depending on the condition, mode and set-up of measurement, the FWHM of conductance peaks can be even larger than this value [3.7]. As discussed earlier, this intrinsic broadening of conductance peaks as a function of temperature becomes a hurdle, when quantum dots with closely-spaced energy levels are being investigated. It means sample must be cooled down to lower temperatures in order to have the measurements on quantum dots with closely spaced energy levels to overcome the intrinsic limitation of conductance peak broadening due to Fermi-Dirac thermal smearing.

3.3 Double Quantum Dot Devices

When two quantum dots are placed in between source and drain electrodes it forms a double quantum dot device. These double quantum dot devices are also called as triple barrier tunneling junction devices as they have three tunneling barriers, two tunneling barriers between the electrodes and each of the quantum dots and another tunneling barrier between the two quantum dots. Typically these double quantum dot devices are fabricated using two-dimensional electron gas (2-DEG) layers [3.8-3.13]. Metal electrodes are placed on the substrate and desired voltages are applied across these electrodes to isolate the electrons in the 2-DEG layer forming quantum dots and electrodes.

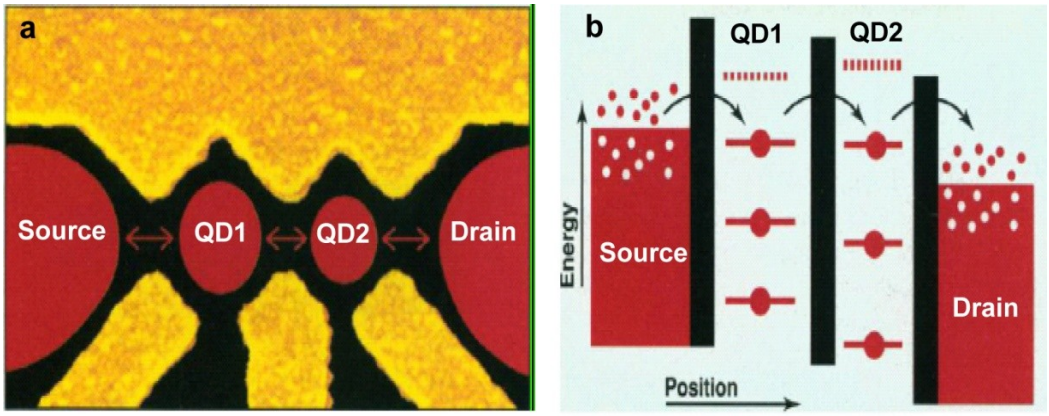


Figure 3-5 Double quantum dot device [3.9] (a) SEM micrograph of a double quantum dot device. The red parts schematically indicate the regions where the electrons are located. Voltages applied to the yellow gates allow tuning of the sizes of the red quantum dot regions, and also the coupling (indicated by arrows) to the leads on the left and right and between the two quantum dots. (b) Double quantum dot energy diagram. Electrons can only occupy discrete energy states in the two quantum dots (the dashed states are unoccupied). Because the energy states are continuous in the two leads, temperature causes a smearing of the occupation probability around the Fermi energy, as indicated by the occupied red dots and unoccupied white dots. Current can only flow when the energy states are aligned, which is indicated by the arrows.

Figure 3-5(a) shows SEM micrograph of double quantum dot device with schematic representation of the source, drain and the quantum dot regions. By varying the voltages applied across the yellow metal electrodes the size and the number of electrons in the quantum dot regions can be manipulated. Figure 3-5(b) shows the energy diagram of the same double quantum dot device. The red and white dots in the source and drain electrodes indicates the thermal smearing of electron energy distribution due to temperature. These devices were fabricated using a hetero-structure

of GaAs/AlGaAs which readily forms 2-DEG at the interface of the two layers. The gate electrodes are then patterned using e-beam lithography and Cr/Au metal deposition on this substrate and voltages are applied on these metal electrodes to isolate the electrons in the 2-DEG at the interface to form quantum dots and the source and drain electrodes. The electrical characteristics of such devices and the suppression in Fermi-Dirac thermal smearing observed in such devices will be discussed in detail in further sections of this chapter.

3.4 Electron Cooling In Double Quantum Dot Devices

In the previous section of this chapter double quantum dot devices were introduced and the typical fabrication procedure of these devices was discussed. In this section the electrical characteristics of such double quantum dot devices and the electron cooling effect observed in the double quantum dot devices will be presented. In double quantum dot device configuration one quantum dot essentially acts as an electron energy filter which filters out the electrons at with high energy and creates cold electrons which tunnel through the second quantum dot. The first quantum dot acts as a low-temperature-pass filter for the other, such that only the cold electrons contribute to the current.

In the source and drain electrodes the electron energy distribution is smeared out due to the thermal energy as indicated by the red dots and white dots in the energy diagram of double quantum dots in figure 3-5(b). However in the quantum dots, because of their discrete energy states there is no thermal smearing of electron energy as there are no empty energy states available, provided the separation between the adjacent energy levels is larger than the thermal energy. In this condition the electrons cannot be excited to higher energy states by the thermal energy which effectively leaves the quantum dot at zero temperature. When enough voltage bias is applied across the

source and drain electrodes the electrons from the source electrode will tunnel into the first quantum dot, but they can only tunnel further to drain electrode through the second quantum dot. This happens when a discrete energy level in the first quantum dot aligns with a discrete energy level in the second quantum dot. When this happens we see a sharp increase in current through the device. Unless the two energy levels are aligned there will be no electrons tunneling from the source to drain electrode and hence no current in the current vs. voltage plot. When the voltage bias across the device is further increased the energy levels misalign and the current drops to zero again. If the voltage across the device is further increased there will be another spike in current whenever the next alignment of energy levels in the two quantum dots happens. Since there are no available empty energy states in the quantum dots there exists no excitation of electrons into higher energy levels and hence the effective temperature of the quantum dot is zero. This means the Fermi-Dirac thermal smearing will be suppressed and it should be depicted in the current-voltage plots.

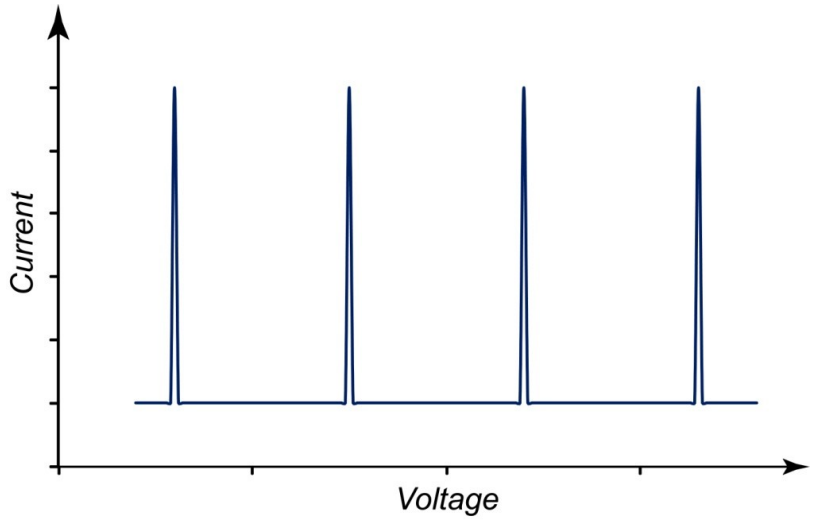


Figure 3-6 Plot showing the expected Current-Voltage characteristic of a double quantum dot device

Figure 3-6 shows a plot of expected current-voltage characteristics of a double quantum dot device. There should be no Fermi-Dirac thermal smearing of electrons in the quantum dots and hence no Fermi-Dirac thermal broadening should be observed in the current-voltage plots. The origin of small peak width of the current peaks in current-voltage plot is the life-time broadening of the elastic tunneling which is given by Lorentzian distribution curve.

In figure 3-7(a) an SEM micrograph of a double quantum dot is shown, which was fabricated by N. C. Van Der Vaart et. al. using 2-DEG formed at the interface in the hetero-structure of GaAs/AlGaAs. Figure 3-7(b) is a energy diagram of the same double quantum dot device. The discrete energy levels in the first quantum dot are denoted as 1, 2, 3, 4 and 5. The discrete energy levels in the second quantum dot are denoted as α and β. When the bias is applied across the source and drain electrodes, the electrons from the source electrode tunnels from source to first quantum dot to the second quantum dot and from there to the drain. This will happen only when the discrete energy levels in both the quantum dots align as discussed above. Figure 3-8 shows the current-voltage measurements done on the double quantum dot. Also in the inset of figure 3-8 the current-voltage measurements done on individual quantum dots is shown. As can be seen from the figure when there is only one quantum dot a step wise increase in current was observed as expected. When the measurements were done on the double quantum dot device spikes in current were observed whenever the energy levels in both quantum dots align. However, it is noticed that the shape of the current peaks is not symmetrical. If the tunneling of electron is purely elastic the shape of the current peaks should be symmetrical and take a Lorentzian distribution form as discussed earlier. This asymmetric shape of the current peaks suggests that there is a part of current which arises from the inelastic tunneling of electrons.

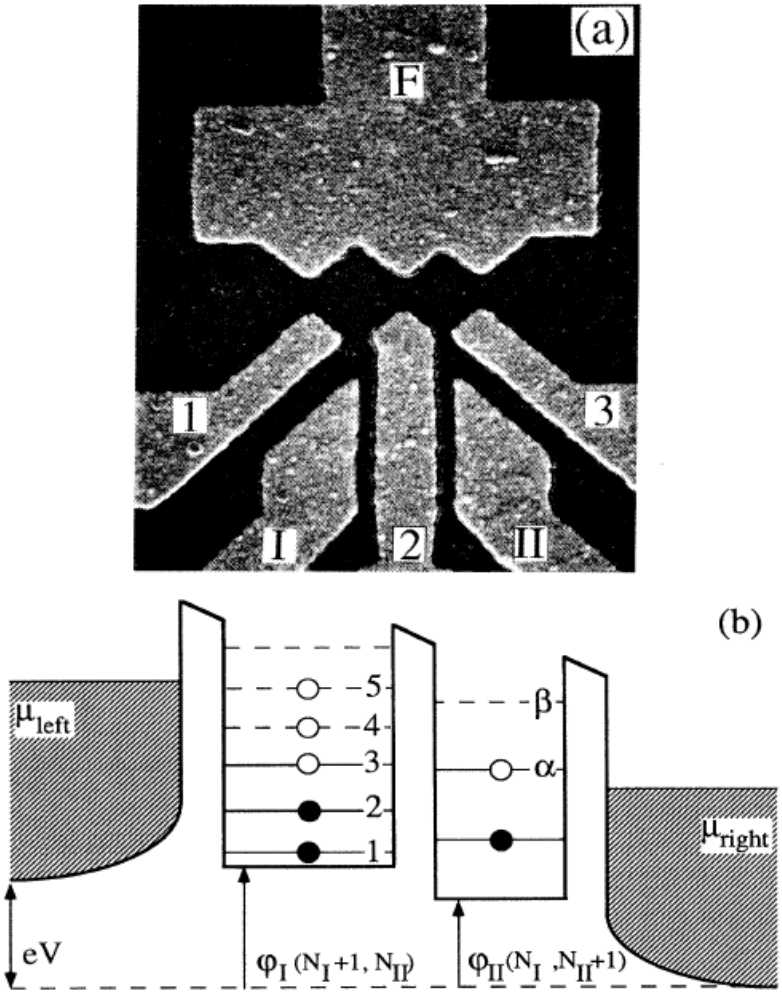


Figure 3-7 [3.10] (a) SEM micrograph of the double quantum dot device fabricated using 2-DEG at the GaAs/AlGaAs interface and the metal gates across which negative voltage was applied to deplete electrons underneath in the 2-DEG forming quantum dots. (b) Energy diagram of the double quantum dot device where the discrete energy levels in the first quantum dot (left) were denoted by 1, 2, 3, 4 and 5, and the discrete energy levels in the second (right) quantum dot were denoted by α and β

A more detailed explanation of the inelastic current or the contribution of inelastic tunneling of electrons to the current through the device can be provided by considering the phonon absorption and phonon emission during the tunneling of electrons through the double quantum dot devices. A detailed study of this was presented by T. Fujisawa et. al. [3.12] in their paper titled, “Spontaneous emission spectrum in double quantum dot devices”. This will be discussed in the later sub-sections of this chapter with the detailed explanation and quantitative analysis presented in their paper.

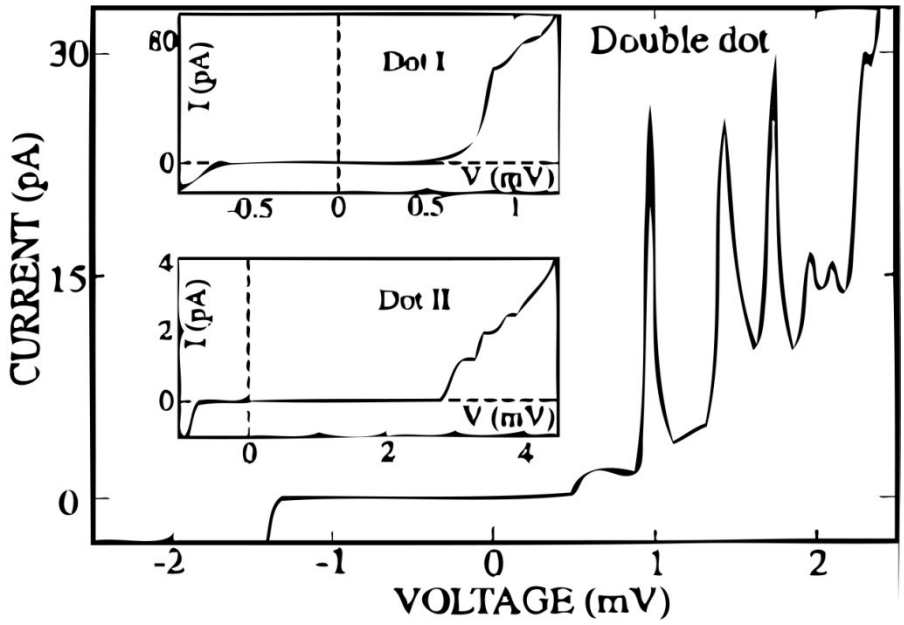


Figure 3-8 [3.10] Current-Voltage measurements done on the double quantum dot device shown in figure 3-7(a). Sharp resonance in current was observed when the discrete energy levels in the two quantum dots align. Inset: Current-Voltage measurements done on individual quantum dots which show step-wise increase in current.

3.4.1 Phonon Absorption and Emission

As discussed in section above the sharp resonances observed in current-voltage measurements of double quantum dot devices must assume Lorentzian distribution shape given the current is due to elastic tunneling of the electron. However, it was observed by N. C. Van Der Vaart et. al. [3.10] that, in their current-voltage measurements done on double quantum dot devices, the tunneling of electrons is not purely elastic but it has contribution from the inelastic tunneling of electrons too. This conclusion was made due to the asymmetrical shape of the resonance peaks in the current-voltage measurements. A more detailed study of this was done by T. Fujisawa et. al. [3.12] They also fabricated their double quantum dot devices using the 2-DEG at the interface of GaAs/AlGaAs hetero-structure, but they used focused ion beam (FIB) patterns in conjunction with three vertical metal gates across which negative voltages are applied to deplete the electron underneath in the 2-DEG to form the double quantum dot devices. Figure 3-9 shows the SEM micrograph of the double quantum dot device fabricated by T. Fujisawa et.al. [3.13]

This structure of double quantum dot device used by T. Fujisawa et. al. [3.13] provides one major advantage over the double quantum dot device structures used in earlier studies by N. C. Van Der Vaart et. al. [3.10] The coupling between the source electrode, quantum dots and the drain electrode can be tuned by changing the voltages applied across the three vertical metal gates. This allowed them to carry on an extensive study of the dependence of current through the double quantum dot device with varying coupling between the components of the device. In figure 3-10(E) the typical current vs energy (ε) plot was shown which was measured at 23mK temperature. The current through the device consists of an elastic part and an inelastic part as shown in the plot.

The origin of inelastic part of current through the device is attributed to the phonon absorption and phonon emission which is schematically represented in figure 3-10 (B) and (D) respectively.

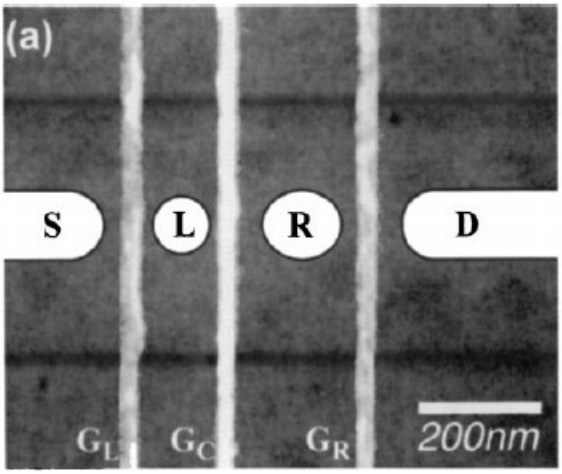


Figure 3-9 SEM micrograph of double quantum dot devices fabricated by T. Fujisawa et. al. [3.13]. Vertical bright line are the metal gates across which negative voltages were applied to deplete the electrons beneath in the 2-DEG forming quantum dots and the electrodes. Horizontal dark lines are the focused ion beam patterns. The white regions denoted by S, L, R and D are schematic representation of source electrode, left quantum dot, right quantum dot and the drain electrodes respectively.

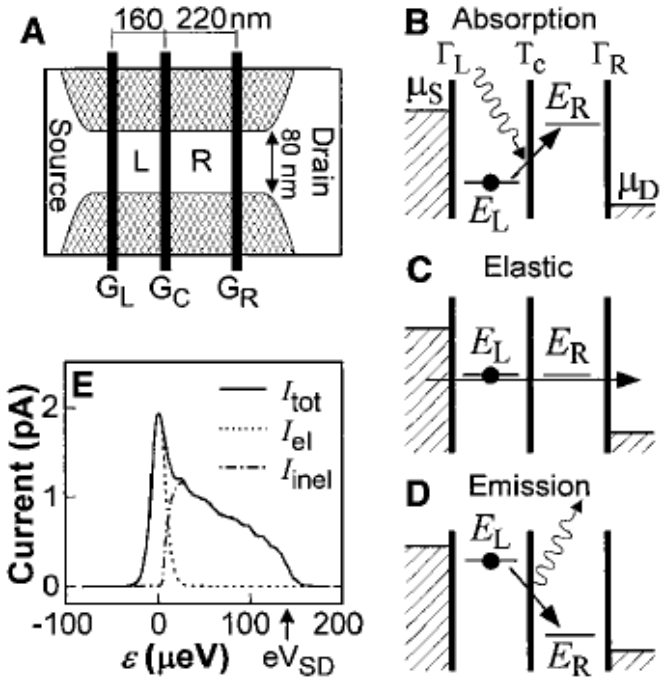


Figure 3-10 [3.12](a) Schematic of double quantum dot device defined in the 2-DEG of GaAs/AlGaAs hetero-structure using focused ion beam pattern (shaded region) and vertical metal gates (black lines) represented by G_L, G_C and G_R. L and R represent the left quantum dot and right quantum dot of double quantum dot device. (b-d) Energy diagrams representing the double quantum dot devices for different electron tunneling situations. (b) phonon absorption, (c) elastic tunneling and (d) phonon emission. μ_S and μ_D are the Fermi energies of the source and the drain electrodes respectively. E_L and E_R are the energy of the discrete energy level in left quantum dot and right quantum dot respectively such that the energy $\varepsilon \equiv E_L - E_R$. An elastic current can flow when ε=0, otherwise a non-zero current requires phonon absorption (ε<0) or phonon emission (ε>0) of energy (e) Measurement of current vs. e at 23mK temperature. The measured current is then split into elastic current (dashed plot) and an inelastic current (dotted-dashed plot).

In figure 3-10(E) a typical measurement of current vs. ε done on the double quantum dot device is shown. The current through the device is decomposed into elastic current $I_{el}(\varepsilon)$ and inelastic current $I_{inel}(\varepsilon)$. The total current $I_{tot}(\varepsilon)$ is then given by the relation

$$I_{tot}(\varepsilon) = I_{el}(\varepsilon) + I_{inel}(\varepsilon) \tag{3-12}$$

where elastic current $I_{el}(\varepsilon)$ dominates when ε =0 and inelastic current $I_{inel}(\varepsilon)$ comes into play when | ε |>0.

The elastic current $I_{el}(\varepsilon)$ is given by the following equation which is Lorentzian line shape

$$I_{el}(\varepsilon) = \frac{eT_c^2\Gamma_R}{\left[T_c^2\left(2 + \Gamma_R/\Gamma_L\right) + \Gamma_R^2/4 + \left(\varepsilon/\hbar\right)^2\right]} \tag{3-13}$$

where e is the elementary charge, T_c is tunnel coupling between the two quantum dots, Γ_L and Γ_R are the tunneling rates for the left and right barrier.

The inelastic tunneling of electrons is a sequential tunneling process of three barriers which yields inelastic current $I_{inel}(\varepsilon)$ as

$$I_{inel}(\varepsilon) = \frac{e}{\left(\Gamma_L^{-1} + \Gamma_{inel}^{-1}(\varepsilon) + \Gamma_R^{-1}\right)} \tag{3-14}$$

when Γ_L and Γ_R are larger than the inelastic tunneling rate Γ_{inel} the current becomes as below

$$I_{inel}(\varepsilon) = e\Gamma_{inel}(\varepsilon) \tag{3-15}$$

In their measurements they observed that the temperature effects the inelastic current through their double quantum dot devices. The temperature dependence of the inelastic current is shown in figure 3-11. A high temperature enhances the current on both the phonon emission side (ε >0) and phonon absorption side (ε <0). To explain this temperature dependence of the current a boson statistics was assumed in the environment. The average occupation number of environmental modes is given by the Bose-Einstein distribution function, $n(\varepsilon > 0, T) = 1 \Big/ \left(e^{\varepsilon / kT} - 1 \right)$. When (ε >0) the inelastic tunneling will be due to phonon absorption and when (ε <0) the source of inelastic tunneling will be emission of phonons. The rates for absorption, Wa and emission, We ,can be expressed very generally by $W_a = B_a \rho$ and $W_e = A + B_e \rho$, where the Einstein coefficients stand for spontaneous emission (A), stimulated emission (Be) and stimulated absorption (Ba) and ρ is the energy density. From the Einstein relations the inelastic tunneling rate was obtained as follows

$$I_{inel}(\varepsilon < 0) = W_a(\varepsilon) = \langle n \rangle A(-\varepsilon) \tag{3-16}$$

$$I_{inel}(\varepsilon > 0) = W_e(\varepsilon) = (\langle n \rangle + 1) A(-\varepsilon) \tag{3-17}$$

Equation (3-16) gives inelastic current due to phonon absorption and equation (3-17) gives inelastic current due to phonon emission. The full width half maximum (FWHM) of the current peaks was measured from the measurement data and they are compared to the FWHM of Fermi-Dirac and also to the thermal energy kT values. A plot showing this is comparison is shown in figure 3-12. As can be seen from the plot the measured FWHM at different temperatures are much narrower than the Fermi-Dirac FWHM and they are even smaller than the thermal energy of corresponding temperature [3.13]. This

indicated that although there is some temperature dependence of measurements, it arises from the phonon absorption and emission.

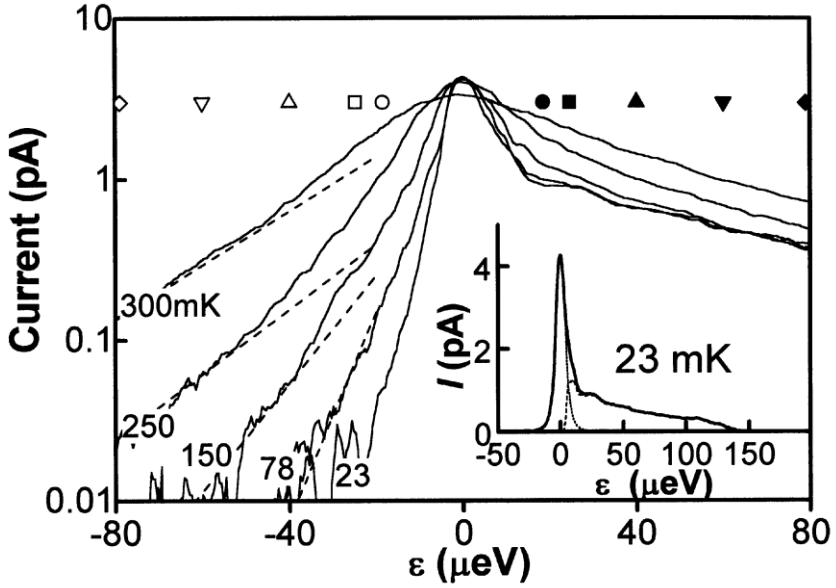


Figure 3-11 [3.13] Temperature dependence of current measurements through the double quantum dot devices.

In summary, previous studies have demonstrated the ability of to suppress the Fermi-Dirac thermal smearing at cryogenic temperatures using double quantum dot devices. This suppression in thermal smearing is due to energy filtering of electron energy distribution through a discrete energy level of a quantum dot. But for practical application this suppression of Fermi-Dirac thermal smearing has to be demonstrated at room temperature. If the same can be demonstrated at room temperature it can make a huge impact on applications of many electronic, opto-electronic and spintronic devices whose operation is limited to cryogenic temperatures at this point. In the following chapters we are going to show that this suppression in Fermi-Dirac thermal smearing by

energy filtering of electron energy distribution can be achieved at room temperature. This was demonstrated using our double barrier tunneling junction devices whose fabrication is detailed in next chapter.

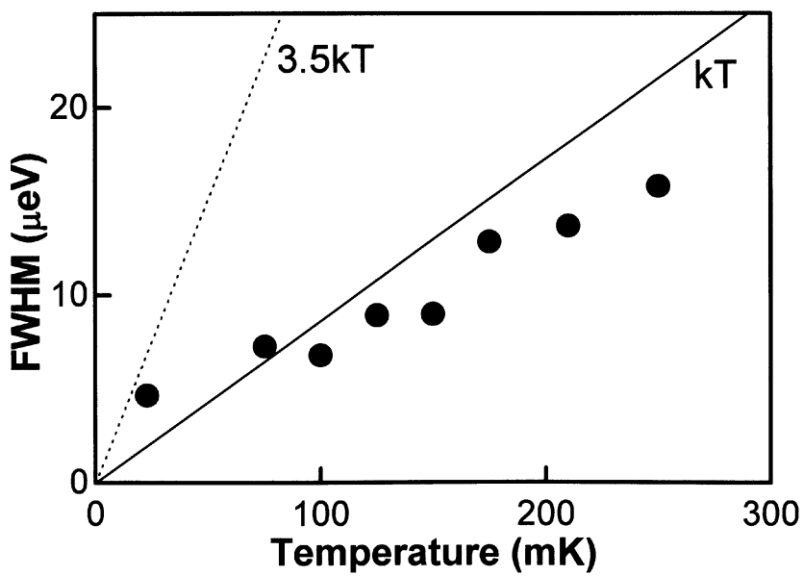


Figure 3-12 [3.13] Comparison of full width half maximum of current peaks at different measurement temperature to the thermal energy (solid Line) and full width half maximum from Fermi-Dirac distribution (dotted line)

Chapter 4

Fabrication of Double-Barrier Tunnel Junction (DBTJ) Devices

4.1 Introduction

The fabrication procedure of the double barrier tunnel junction devices used in this study are provided in this chapter. The challenges faced during the fabrication and the improvements made to the thin film deposition processes and the reactive ion etch processes are also discussed in detail in this chapter. We start with a 4-inch silicon wafer which has to go through several processes like Thermal oxidation, Physical Vapor Deposition (PVD), Chemical Vapor Deposition (CVD), Dry Etching, UV Cleaning, Formation of Self-Assembled Monolayers (SAM's) and Immersion in colloidal particle solutions and so on before our final devices are ready for electrical characterization. All these processes are carried out in a class-1000 cleanroom facility, NanoFab Research Center [4.1], at The University of Texas at Arlington and will be explained in detail in this chapter.

4.2 Design of Photo-Mask for DBTJ Devices

The DBTJ devices under study were fabricated using standard photo lithography technique. For this a photo lithography mask was designed. Each feature in the device like the source electrode, the drain electrode, the via-holes and the bond pads are defined using a separate mask layer. The whole device structure fabrication involves four mask layers. A single mask was designed for all four mask layers such that each mask layer is occupying one quadrant of the mask. The mask design is shown in the figure 4-1 below. In figure 4-1 the top right quadrant contains the first layer of the mask which is the bottom electrode; the top left quadrant has the second layer in the mask lay out which is

the top electrode in the vertical electrode device structure. In the bottom left quadrant of mask lay out the third mask layer which is via-hole layer to make contacts was shown and the final or the fourth layer in the mask is on the bottom right quadrant which is consists of the bond pads to enable electrical characterization of these devices. The zoomed in view of a single die of each of these layers is also shown in the respective corners of figure 4-1.

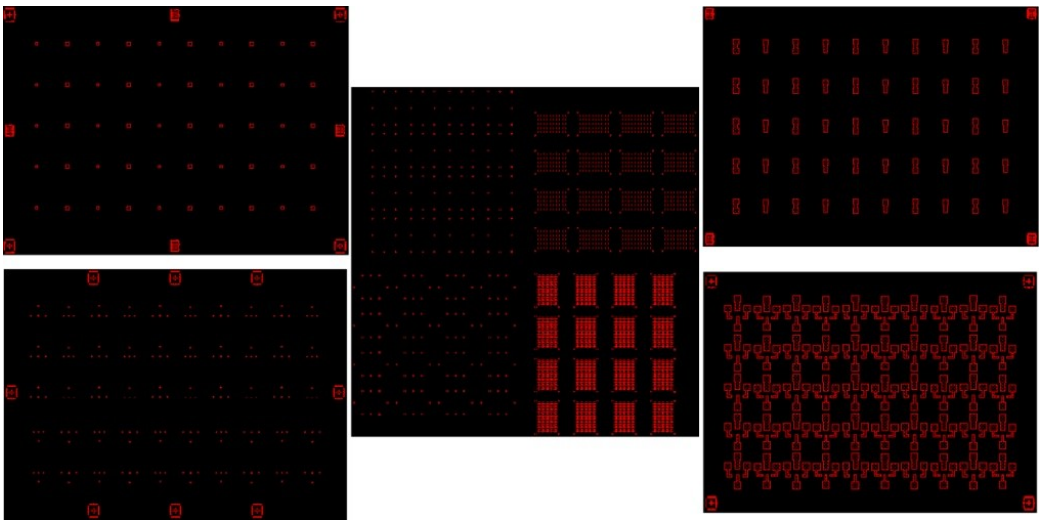


Figure 4-1 Photo mask design layout showing four different mask layers

4.3 Thermal Oxidation - Isolation Oxide Growth

Silicon (100) wafers were used as substrate for fabrication of all the Double-Barrier Tunnel Junction Devices used in current study. Test grade p-type 4" Silicon wafers (Nova wafers) are immersed in acetone and placed in an ultrasonic bath for 5 minutes in order to get rid of any organic impurities on the wafer. The wafers were then rinsed with acetone and isopropanol followed by blow drying with nitrogen. Then the wafers are immersed in a 10:1 Hydrofluoric acid bath for 2 minutes to remove the native

oxide layer on them and then rinsed with copious amounts of DI water and blown dry with nitrogen. This step terminates the surface of silicon wafer with a layer of hydrogen preventing the formation of any native oxide layer. The cleaned wafers were then introduced into the Tystar thermal oxidation furnace for growing the desired thickness of thermal oxide which will serve as an isolation oxide for the device fabrication. The wafers were introduced into the quartz tube held at 750^0C at a slow rate of 1 inch/minute which is preset in the program, to reduce the risk of any thermal shock. During wafer introduction into the furnace, the furnace tube is continually purged with nitrogen gas at 3 liters/minute. Once the quartz tube completely closes the Si wafers will be in the mid zone of the furnace, the temperature of the furnace is slowly ramped up to 1100^0C in order to perform the oxidation. Once the furnace reaches the desired temperature water vapor is flowed into the furnace using a bubbler system with nitrogen being the carrier gas. The bubbler containing ultra pure DI water (18.2MΩ.cm) is maintained at 100^0C. Process time for 1.0 μm thickness silicon-oxide films is calculated [4.2] to be approximately 1 hour and 30 mins. The temperature of the furnace during various steps of oxidation process and process times can be fed in to the tystar oxidation furnace computer while creating the process. The tystar oxidation furnace is totally automated and will take care of the entire process once process parameters are set up. Once the process time is completed, the nitrogen flow through the bubbler is cut-off and pure nitrogen is flowed through the furnace tube. The furnace will be cooled down slowly to 700^0C before opening the furnace to remove the wafers. After removing of the wafers from the furnace they are let to cool down before transferring them into wafer boxes. The thickness of the silicon-oxide film grown is checked with the Gaertner ellipsometer and Ocean optics NC-UV-VIS reflectometer.

4.4 Deposition of Bottom Electrode

The next step in the fabrication process is the defining the bottom source electrode. The silicon wafer with the thermally grown oxide layer was cleaned in 1:3 piranha solution for 5minutes followed by rinsing with copious amount DI water to get rid of any kind of organic impurities adhering to the surface of the oxidized silicon wafers. The cleaning of oxidized silicon wafers in 1:3 piranha solution was important as the wafers which did not go through this step have exhibited problem of metal electrode peel off in some occasions. These wafers were then cleaned in methanol and blown dry with nitrogen and then cleaned in the UV-Ozone cleaner (Novascan Inc.) for 30 min to remove any contaminants from the surface. The negative photoresist NR9-1000PY (Futurrex Inc.) was spin coated on the wafer at 2000rpm for 30 seconds giving a photoresist film thickness of ~1.3-1.4 μm. Pre-exposure bake was done at 150^0C for 60 seconds. The 4" wafer was then cleaved into four equal sized quadrants as our mask was designed to have four different mask layers of our fabrication steps in a single mask - one layer in each quadrant of the mask. The cleaved wafers coated with photoresist were then placed on the sample holder of the OAI-Backside aligner for UV exposure making sure we are using the right quadrant of the mask which will yield the bottom electrode pattern. 365 nm primary wavelength UV light generated by a mercury vapor lamp was used for exposure. The samples were exposed through the photo-mask for 19 seconds. The post exposure bake was done immediately after exposure at 100^0C for 60 seconds. After baking the samples were developed in the resist developer (RD6, Futurrex Inc.) by immersing them in the developer solution for 16 seconds. After development, the samples were rinsed with copious amounts DI water followed by nitrogen blow drying.

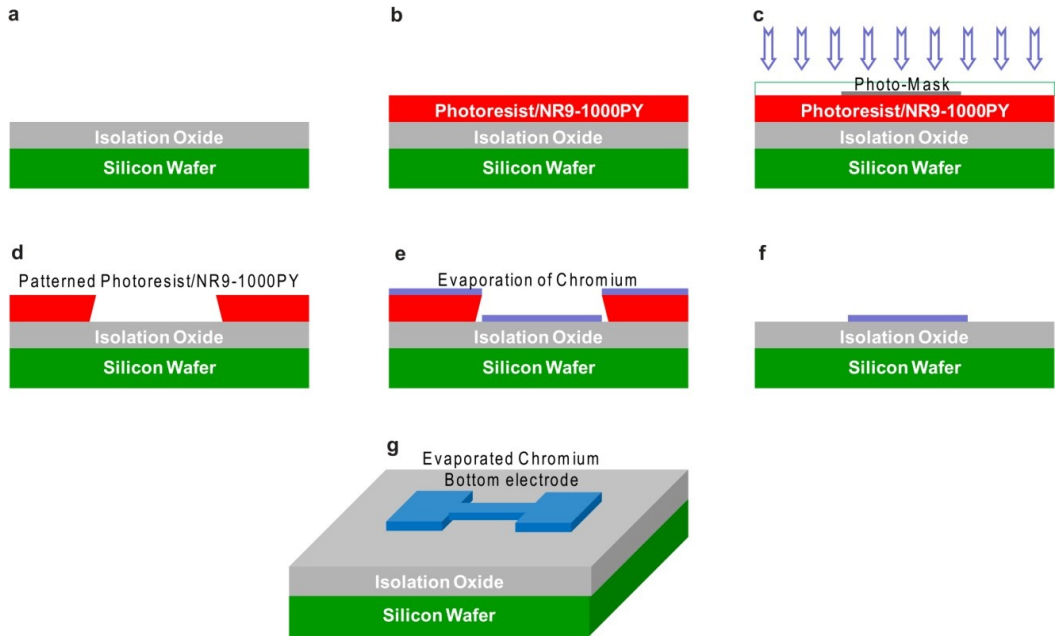


Figure 4-2 Defining the bottom electrode using photolithography, metal evaporation and liftoff (a) Thermal oxide substrate sample (b) Spin Coating of photo-resist on sample (c) Mask Aligner – UV exposure of sample (d) Developing of samples in RD6 (e) e-beam evaporation of chromium (f) Acetone lift-off of sample with metal deposition (g) Sample with patterned bottom electrode

The samples were then placed inside the e-beam evaporator (AJA Inc.) chamber for physical vapor deposition of chromium bottom electrode. After reaching vacuum levels below $5X10^{-7}$ Torr, the chromium metal was evaporated on to the patterned silicon wafer at a rate of 3-4 Å/s for a total thickness of 200 nm. After completion of evaporation to the desired thickness, the samples were unloaded from the chamber and immersed into an acetone bath in the ultrasonic agitator to facilitate the lift-off process. After 10 minutes, the acetone was replaced with fresh acetone and ultrasonic agitation of the samples was continued for an additional 10 minutes to get rid of most of the photoresist residues. Once

completed with the lift-off process, the samples were again rinsed with acetone and blown dry with nitrogen. To remove any remnants of the photoresist, the samples were then cleaned inside the UV-Ozone cleaner for 30 minutes. Two more cycles of acetone sonication and UV-ozone cleaning are repeated before proceeding to the next step of fabrication. Figure 4-2 shows the schematic representation of photolithography process, metal deposition and liftoff processes involving the definition of bottom electrode

4.5 Deposition of Plasma Enhanced Chemical Vapor Deposition (PECVD)/ Atomic Layer Deposition (ALD) Dielectric Film

After defining the bottom electrode the next step in the fabrication process is deposition of thin dielectric layer which acts as an insulating layer between the top and the bottom electrodes. This insulating dielectric layer should be of very high quality in order for the electrical leakage current to be low. For this thin insulating layer either plasma enhanced chemical vapor deposition (PECVD) of silicon oxide / atomic layer deposition (ALD) of aluminum oxide was employed. The PECVD silicon oxide deposition process is done using the TRION-ORION PECVD chamber. Process development and optimization was carried out in order to achieve very high quality oxide films [4.3-4.4] which are few nanometers thick (~5nm -7nm).

A typical chemical vapor deposition process consists of chemical dissociation of gas precursors which are adsorbed on to the surface of the substrate and react chemically to form a thin film. Typically the decomposition of these process gases occurs at high temperatures (~1000^0C) in the process chamber. In PECVD this decomposition of gases is achieved even at low temperature due to the presence of plasma which enhances the decomposition of precursor gases. The precursor gases used in PECVD growth silicon oxide are Silane (SiH_4) and nitrous-oxide (N_2O). The chemical reactions

taking place during the film growth are shown below. Chemical decomposition of the precursor gases that is decomposition of silane into silicon and hydrogen, decomposition of nitrous oxide into nitrogen and oxygen and then reaction between the reactive species that is silicon and oxygen to form silicon oxide film.

$$SiH_4 \rightarrow Si + 2H_2$$
$$2N_2O \rightarrow 2N_2 + O_2$$
$$Si + O_2 \rightarrow SiO_2$$

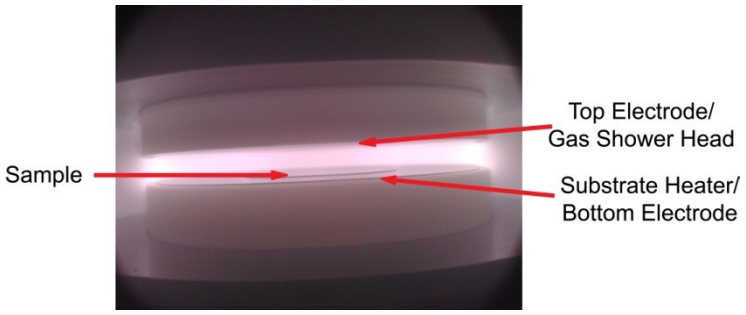


Figure 4-3 Photograph depicting the plasma inside TRION orion PECVD chamber [4.5]

The various factors affecting the quality of PECVD silicon dioxide film are listed below:

a) Dilution of Silane precursor gas

b) Pressure

c) Substrate temperature

d) Radio frequency power

In PECVD plasma is generated using radio frequency (RF) power which helps to decompose the process. The reactive ion species generated thus react at the hot substrate surface and form the film. RF power gives sufficient energy for decomposition of the gases as well as prevents any gas phase reactions. Figure 4-3 shows the actual

photographic image of the plasma in TRION orion PECVD chamber while depositing silicon oxide film.

Table 4-1 Effect of silane dilution and pressure on PECVD silicon oxide film quality

Sample #	Silane Flow (sccm)	Pressure (mTorr)	Dep. Rate (A/sec)	Etch Rate (A/min)	Topography/AFM Images
1	21	1000	3.63	160	Little grainy
2	10	500	2.98	168	Smooth
3	10	2000	0.88	104	Rough
4	16	1250	2.29	164	Little grainy
5	22	500	6.23	172	Smooth
6	22	2000	1.87	132	Rough

For the PECVD film to be of good quality the general trend of parameters should be high dilution of silane, moderate to high pressures in the chamber, high RF power which helps in complete decomposition of precursor gases, high temperature [4.3] of the substrate which increases the chances of reaction of species on the substrate. In the previous studies with carefully designed set of experiments the effect of all these parameters was studied, in order to get a very high quality film [4.5]. From these studies it is known that high RF power (~500W) and high substrate temperature (360^0C) helps in obtaining good quality films. To further improve the quality of the deposited silicon oxide films a small set of experiments were carried out as shown in Table 4-1 below. The films deposited using these parameters are then characterized using microscope (AFM) scanning for roughness measurements, wet etch rates compared with dry thermal oxide

etch rate etched with 50:1 HF solution, breakdown voltage measurement and scanning electron micrographs to check for presence of pin holes.

For above set of experiments we have the RF Power (500Watt), substrate temperature (360^0C) and deposition time (180seconds) as constant. We also have N2O flow 179sccm and N2 flow 250sccm as our constants. We conducted these set of experiments to study the effect of silane dilution and pressure in same set of experiments. Sample 1 is the initial parameters of our PECVD silicon oxide film deposition and we designed experiments around these parameters to further improve the quality of the film. From the above experiments we concluded that when we go to very high pressures beyond 1500mT we see localized deposition spots on the substrate. And we observed that with more dilution of precursor gases we have better quality film. The AFM images showing the topography of these films are shown in figure 4-4.

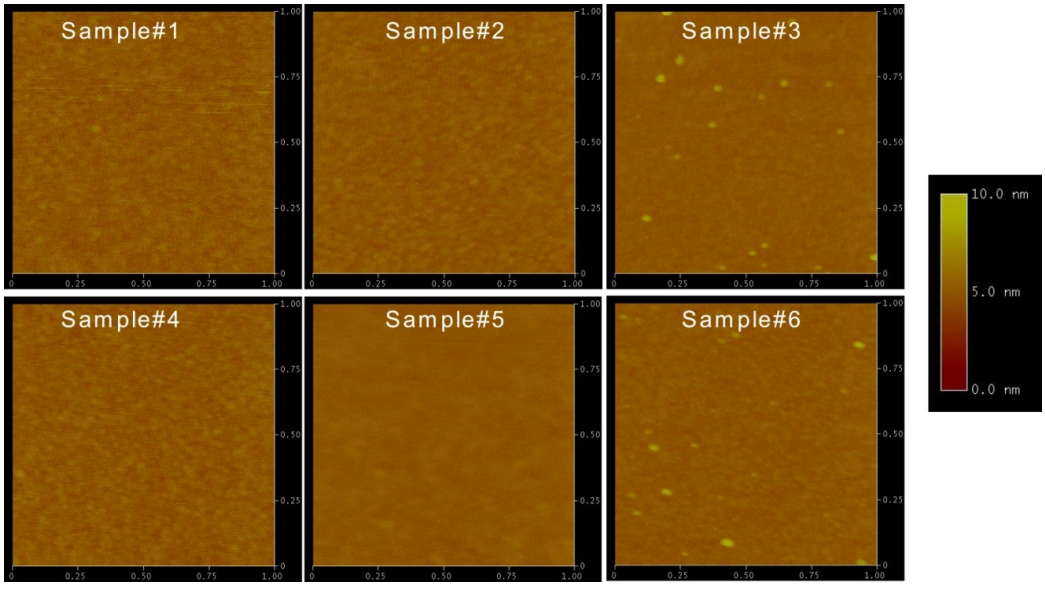


Figure 4-4 AFM/Topography images of PECVD silicon oxide films I

Based on the conclusions from above experiments to further improve the quality of deposited PECVD films we considered studying further dilution of silane [4.6]. We carried out another set of experiments; where we increased the dilution of silane gas further to see the effect. The experimental parameters and results are shown in the Table 4-2. In these experiments we have all the other parameters similar except for the silane flow. The parameters used are RF Power (500Watt), substrate temperature (360^0C), deposition time (180seconds), N2O flow 179sccm and N2 flow 250sccm as constant.

Table 4-2 Effect of further silane dilution on PECVD silicon oxide film quality

Sample #	Silane Flow (sccm)	Dep. Rate (A/sec)	Etch Rate (A/min)	Topography/AFM Images
7	5	1.75	124	Smooth
8	10	3.125	110	Smooth

Figure 4-5 shows the AFM images depicting the topography of sample 7 and sample 8. The films are found to be very smooth from the AFM images. The etch rate of these films in 50:1 HF was found to be roughly twice the etch rate of thermal oxide (50 A/min), which indicates that the quality of these films is very good. To further investigate the electrical properties of the films we deposited ~10nm thin films on chromium substrate. Another layer of top chromium was deposited and the PECVD silicon oxide was etched to measure the break down voltage of these films. We found the break down voltage to be close to the break down voltage of thermal oxide in both the samples ~5MV/cm.

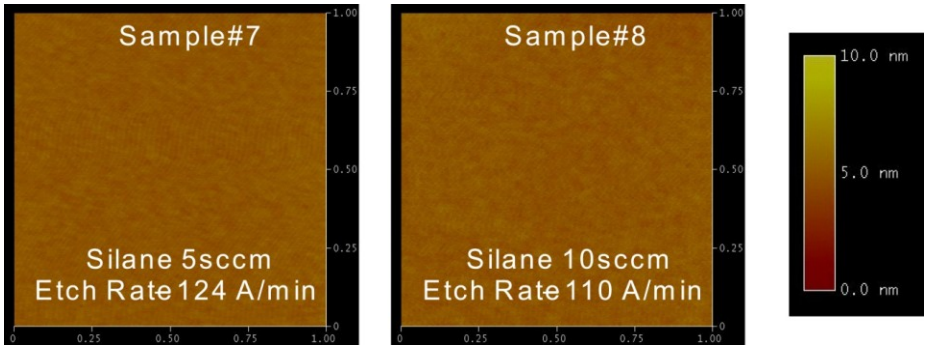


Figure 4-5 AFM/Topography images of PECVD silicon oxide films II

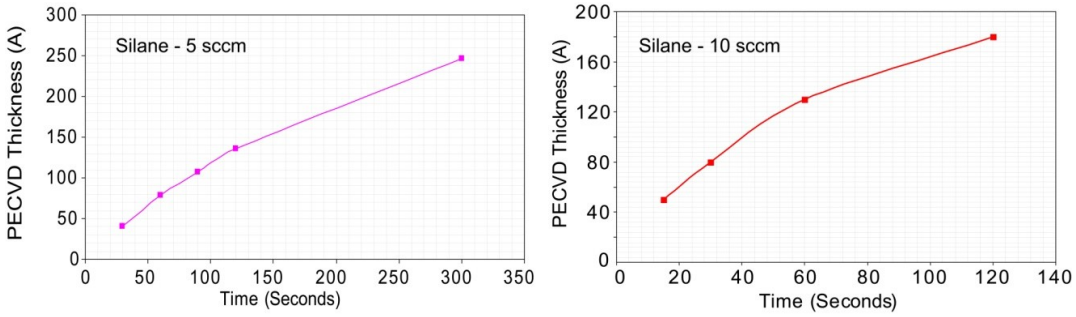


Figure 4-6 PECVD silicon oxide reference deposition charts

We further investigated the repeatability of the process and carried out as series of deposition experiments to obtain the deposition charts we can refer to for obtaining different films thicknesses using deposition recipe 7 and deposition recipe 8. The deposition charts for these recipes are shown in Figure 4-6

After further investigating the leakage current behavior of these two recipes we determined that the following recipe gives the best quality film suitable for our device fabrication.

SiH_4 Flow : 10 sccm

N_2O Flow: 179 sccm

N_2 Flow : 250 sccm

Pressure: 1000 mTorr

Substrate Temperature: 360^0C

R.F Power: 500 W

4.6 Deposition of Top Electrode

We use photolithography, metal evaporation and lift-off to define the top electrode, similar to the way we defined the bottom electrode as shown schematically in figure 4.2 before. After the deposition of the PECVD silicon dioxide film/ALD Aluminum oxide film, the samples were cleaned in the UV-Ozone cleaner for 30 minutes. The samples were then coated with NR9-100PY photoresist using spin coating followed by pre-exposure baking 150^0C for 90 seconds and the samples subsequently exposed with UV-light in OAI Backside Aligner. This being the second layer in our device fabrication, taking aid of the alignment marks we have to align this layer to the bottom electrode layer. Once aligned the samples are shined with 365nm UV-Light for 19seconds. Post exposure bake was done at 100^OC for 60 seconds followed by developing the the samples in RD6 developer solution for 16 seconds. The samples were then rinsed with copious amounts of DI water and blown dry with nitrogen.

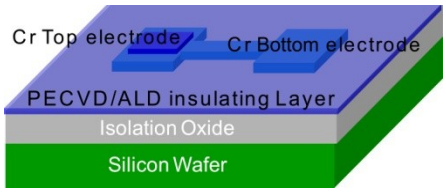


Figure 4-7 DBTJ device structure after PECVD/ALD and top electrode deposition

These samples with patterned photoresist were then loaded into the AJA e-beam evaporator and chromium metal of 200 nm thickness was evaporated on the sample. After metal evaporation lift-off was done by sonicating the samples in ultrasonicator in an acetone bath for 15 minutes. These samples were then transferred to UV-ozone cleaner for 30 minutes to burnout any residual photoresist. Two more cycles of acetone sonication and UV-ozone cleaning were done to completely get rid of any residual resist. The bottom and top electrode are now separated by the thickness of the deposited PECVD oxide/ ALD Aluminum oxide layer. With the samples thoroughly cleaned we can proceed to the most critical step in our fabrication process which is the removal of the PECVD/ALD dielectric film using dry etching.

4.7 Reactive Ion Etching of the Dielectric Film

In this step of device fabrication using top electrode as the hard mask and the PECVD silicon oxide/ALD aluminum oxide dielectric insulating layer was etched to form a side wall on which the quantum dots will be attached to fabricate DBTJ devices. The etching of the samples is either done in TRION Deep Reactive Ion Etch (DRIE) or Plasmatherm Reactive Ion Etcher to form a smooth sidewall. Extra care must be taken to make sure there is no polymer formation during the etching of the dielectric film as the polymer formation can become a impede electron tunneling.

4.7.1 TRION Deep Reactive Ion Etcher

Several sets of experiments were carried out to determine the right etching conditions which yields no polymer formation while etching the dielectric film with smooth sidewall. Table 4-3 shows the parameters used to run the experiments to find the right etch conditions.

Table 4-3 Effect of RIE Power, CF_4 flow and O_2 flow on polymer formation and conductivity of the Top and Bottom Cr electrodes

Sample #	RIE Power (Watt)	CF_4 Flow (sccm)	O_2 Flow (sccm)	Top Cr Conductivity	Bottom Cr Conductivity
1	100	105	20	6-8mA	5-7mA
2	100	105	0	6-8mA	5-7mA
3	100	25	20	1-2mA	50-100μA
4	100	25	0	1-2mA	50-100μA
5	50	25	0	0.1-0.5mA	~ 20μA
6	50	25	20	0.1-0.5mA	~ 20μA
7	50	105	0	5-7mA	3-5mA
8	50	105	20	5-7mA	3-5mA
9	75	65	10	1-2mA	50-100μA

For the above set of experiments the pressure was set constant at 20 mTorr, the ICP power was set constant at 3000 Watt and the over etch time was 180 seconds. Over etching of the PECVD oxide layer is done to ensure complete etch of the dielectric layer and a formation of step on the bottom chrome electrode as depicted in figure 4.8. In these set of experiments we also employed a photolithography step to cover the isolation oxide as shown in figure 4.8, to minimize the global loading effect in the DRIE chamber [4.7]. The pressure was set to minimum to have more anisotropic etch as well as low residence time [4.8] of etch gases in the chamber which will be helpful in minimizing the polymer formation [4.9] during the etch process.

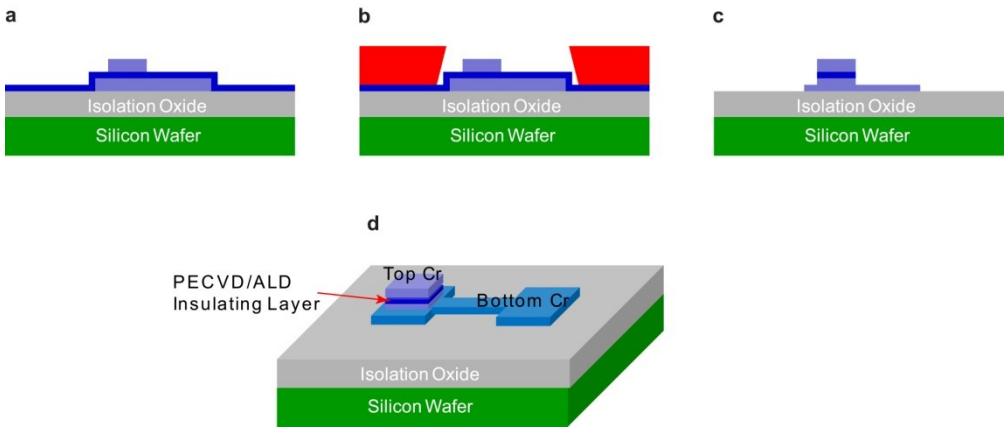


Figure 4-8 DRIE etching of the PECVD/ALD dielectric film (a) Sample after top electrode deposition (b) Mask-Alignment step to cover the thermal oxide area (c) Sample after RIE etching of thin dielectric film layer and removal of resist (d) 3-D schematic of the same sample in (c)

All these experiments were carried out in a clean chamber environment. The chamber was wet cleaned and then conditioned with photoresist for 30 minutes followed by O_2 plasma cleaning for 30minutes. After conditioning the chamber we etched the

samples and measured the conductivity of samples to determine the right etching condition with minimum polymer formation. Higher conductivity of both top and bottom electrodes implies no polymer formation indicating the etch conditions to be ideal for our sample etching. From the above experiments it is determined that high CF_4 flow and high power with or without the addition of 20% O_2 flow are the ideal etch conditions for etching the dielectric films. However, due to inconsistency of the tool conditions the sample surface was sometimes contaminated in TRION chamber.

4.7.2 PLASMATHERM Reactive Ion Etcher

To overcome the inconsistent results from the TRION DRIE etching of samples we started using Plasmatherm RIE for sidewall etch of the samples. This tool gave us very consistent results in terms of etch rate and conductivity of electrodes after the etching. This tool was a PECVD deposition tool which was modified to use as an etcher. We have RF power connected to the top electrode and the chamber and the bottom chuck are grounded. In order to have good etch rate we have to place the samples on the electrode connected to the RF power, which drives the ions onto the sample. This will have two advantages, the etch rate will be faster and also the formation of polymer will be checked due to the ion bombardment of the sample.

We used the same lithography steps to cover the oxide area on the sample as shown in Figure 4-8 to minimize the loading effect. The samples were then loaded on to a 4” silicon loding wafer using kapton tape. The loading wafer is then attached to the top electrode of the chamber and held in place with the aid of kapton tape. The recipe used for etching consists of only CF_4 chemistry with a flow of 200 sccm. The power used was maximum which is 200 Watt. The pressure is adjusted to have stable plasma. We want low pressures to have anisotropic etch but the tradeoff is when we go to low pressures

the plasma was not stable. So the minimum pressure used was 80mTorr. With this recipe we have very consistent oxide etch rate of 25nm/min. Also there is negligible conductivity drop of both the top electrode and the bottom electrode.

4.8 Attachment of Quantum Dots

We mainly used two different types of quantum dots (CdSe and CdTe) for our DBTJ device fabrication. We purchase ~7 nm and ~5.5 nm CdSe quantum dots suspended in toluene from NN-Labs. We purchased ~7.8 nm CdTe nanoparticles from American Elements Inc initially. We then switched to Sigma-Aldrich from December 2013 for purchasing ~7.8 nm CdTe quantum dot powder which are negatively charged when suspended in DI water.

The samples once removed from the etching chamber were sonicated in acetone bath for 10minutes followed by acetone rinsing. These samples were then blown dry with nitrogen and subsequently cleaned in the UV-Ozone chamber for 30 minutes. Three cycles of acetone sonication and UV-Ozone cleaning is done to get rid of any residual resist from the samples.

The SAMs of 3-AminopropylTriethoxysilane (APTES – Sigma Aldrich) was formed on the chromium and silicon dioxide surfaces of the sample by immersing the substrate in a 1mM solution of the APTES in chloroform for 30 minutes. This was followed by rinsing in chloroform (Sigma Aldrich) and 2-Propanol solutions and blown dry with nitrogen. The samples were immediately immersed in the CdSe QD/toluene or the CdTe QD/DI water solution containing the quantum dots.

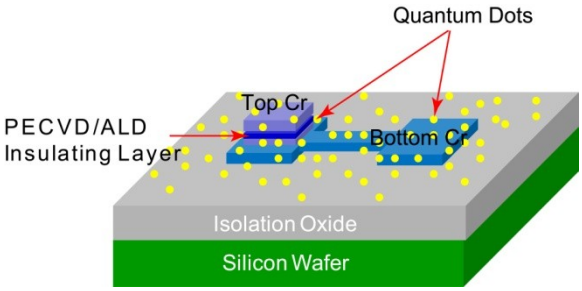


Figure 4-9 Schematic of DBTJ device after attachment of quantum dots

For CdSe QD's a diluted quantum dot solution was prepared by taking 1ml of the concentrated quantum dot solution (as is from manufacturer) and dissolving it in 25 ml of pure toluene (Sigma Aldrich). The APTES functionalized substrates were immersed in this diluted colloidal quantum dot solution for 12-16 hours. Once the immersion was completed, the samples were rinsed with pure toluene and methanol (J T Baker Inc) and blown dry with nitrogen. During this quantum dot attachment process, the quantum dots are randomly attached all over the substrate surface including the exposed sidewall of the electrodes and dielectric. A schematic after the quantum dot attachment is shown in figure 4.9. After the attachment of quantum dots the APTES SAM's layers on the substrate and the organic surface ligands on the quantum dots are removed by UV-Ozone treatment of samples for 30 minutes.

4.9 Passivation of DBTJ Devices

After the attachment of quantum dots to the sidewall of our devices we form a double barrier tunnel junction i.e source-quantum dot tunnel junction barrier and quantum dot-drain tunnel junction barrier. The next step in our device fabrication is passivation of the devices using sputtered silicondioxide. For this purpose we use the home-built sputtering machine with a three in silicondioxide target. The samples after UV-Ozone

cleaning were carefully clamped on to the sample holder and the distance between the sample holder and the silicondioxide target is adjusted to 3.5 inches. The following deposition recipe was used for depositing the silicondioxide passivation layer.

RF Power: 90 W

Pressure: 10 mTorr

Argon flow rate: 37.5 sccm

Deposition rate: 30 A/minute

A silicondioxide film thickness of ~270-300 nm was obtained after sputtering for 90 minutes. The sputtering was carried out in two steps of 45 minutes each instead of a continuous 90 minute deposition. In between the two deposition steps we give a break of atleast 30 minutes to make sure the samples are not over heated during the deposition process. Once the deposition of sputtered SiO_2 was completed, the samples were loaded into the e-beam evaporator (CHA or AJA Inc.) to further deposit 600nm of e-beam evaporated silicondioxide to finish the passivation.

4.10 Deposition of Bond Pads for DBTJ Devices

For electrical characterization of the fabricated devices we have to make contacts with the source and drain electrodes. This involves two steps, first we have to etch via-holes through the passivation oxide and the we have to do photolithography and metal deposition to define the bond pads.

4.10.1 Etching of Via-Holes

Via-holes are etched through the passivation oxide to make electrical contact with the electrodes. For making the via-holes we use photolithography to define the areas to be etched using the third mask layer shown in figure 4.1. After defining the via-hole

areas to be etched using the photoresist as mask to protect the passivation oxide, we etch the passivation oxide in the via-hole areas using DRIE once again. This has to be done atleast four times, each time for 300 seconds, in order etch ~1000 nm thick passivation oxide. The resist acting as mask during the DRIE etching will only last for 300 seconds and after each cycle of etching we have to remove the residual resist using acetone sonication and form a new photoresist masking layer. Care must be taken while doing the later cycles of photolithography to minimize any misalignment of via-hole patterns. For the photolithography we use the same NR9-1000PY resist that we used in previous steps.

The etch recipe used for etching of via-holes in DRIE is slightly different than the recipe we use for sidewall etching. In order to prevent the complete consumption of resist we use lower RIE power. The recipe for via-hole etching is listed below

CF4 flow rate – 25 sccm

He flow rate – 25 sccm

Process pressure – 25 mTorr

Top ICP power – 3000 Watt

Bottom RIE power – 50 Watt

Process time – 300 seconds

4.10.2 Deposition of Bond Pads

After etching through the via-holes, the metal contact was confirmed by checking the etch depths with profilometer and and by checking the conductivity of metal surface, before proceeding to the next step of deposition of bond pads. Once the via-hole etching is confirmed the samples are sonicated in acetone bath for 10 minutes followed by UV-Ozone cleaning for 60 minutes.

The final and fourth layer in the photomask was used to define the final bond pads/contacts with the underlying source and drain electrodes. A layer of NR9-1000PY negative photoresist is again spun coated on the substrates at 2000 rpm for 30 seconds. Pre-exposure bake is done at 150^0C for 60 seconds. With the aid of the alignment marks on the photomask and the substrate, the substrate was aligned to the corresponding feature on the photomask using the OAI mask aligner. Once aligned, the substrate is brought into contact with the photomask and exposed to the UV light for 19 seconds. Post exposure bake is done at 100^0C for 60 seconds followed by developing the exposed photoresist in the resist developer RD6 for 16 seconds. The samples were then rinsed with copious DI water and then blown dry with nitrogen. The wafers are then loaded in the e-beam evaporator (AJA Inc.) and the chamber is evacuated till the pressure reaches 5×10^{-7} Torr. 3000 Å of titanium and 250 Å of gold are evaporated at the rate of 3-4 Å/sec. Lift-off of is done by first immersing the wafers in an acetone bath for 1 hour followed by ultrasonic agitation in an clean acetone bath for 15 minutes. The samples are then rinsed with acetone, blown dry with nitrogen and subsequently cleaned in the UV-Ozone cleaner for 30 minutes. The final sample structure is shown schematically in figure 4.10.

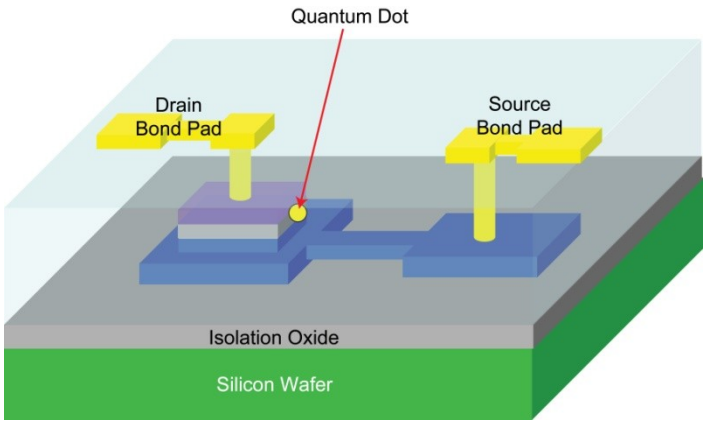


Figure 4-10 Final sample device structure after bond pad deposition

4.11 Wafer Dicing and Mounting of Individual Dies on a Chip Carrier

For electrical characterization in the ST-500 (Janis) low temperature probe station, individual dies had to be diced and mounted onto a chip carrier for the ease of handling the samples without dropping them while mounting/dismounting of samples from the chamber. After the final bond pad deposition step, individual dies of about ~2 cm x 1.5 cm in size were diced using a diamond tip scriber pen. Extra care was taken to, not dice the wafer too close to the working devices. A small scratch was made with diamond scriber per, far away from the working device location and using the teflon tweezers the wafer was carefully broken into ~2cm x 1.5cm piece along the scratch made using diamond tip scriber pen.

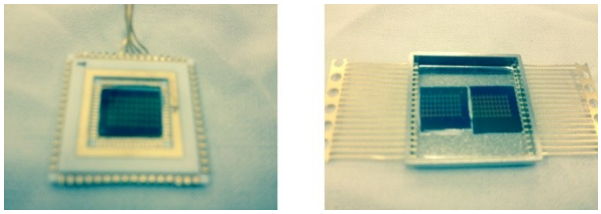


Figure 4-11 Chip carriers used for mounting the samples in ST-500 probe station chamber

Once diced, these dies were thoroughly rinsed with acetone and dried with a stream of nitrogen. The diced pieces were cleaned once again in the UV-ozone chamber for 30 minutes to ensure clean surfaces. Ceramic chip carriers (CCF06404; Kyocera) which can accommodate one single die or metal chip carrier slightly larger in size which can accommodate two dies were used for mounting the dies containing DBTJ devices. Figure 4.11 shows the two different types of chip carriers used for mounting the DBTJ devices. A drop of conducting silver paint (SPI supplies) was placed on the chip carrier,

which acts as an adhesive and the diced die were placed on top of it. The diced samples were secured in position on the chip carrier by gently pressing on the top of the diced piece of sample using teflon tweezers taking care not to press close to the working devices. The chip carriers were let to dry for at least 2 hours before being loaded to the ST-500 chamber for electrical characterization.

Chapter 5

Electrical Characterization of DBTJ Devices

5.1 Introduction

In this chapter the electrical characteristics of the fabricated DBTJ devices are presented. For electrical characterization of these devices three different set ups were used. The Agilent-4155C parameter analyzer was used for current-voltage measurements at room temperature inside the NanoFab Research Center cleanroom. For current-voltage characteristic measurements in 105-BA electrical characterization lab, Agilent-4157B parameter analyzer was used. This parameter analyzer was connected to a low temperature probe station ST-500 (Janis Inc.) for electrical characterization at low temperatures. The direct differential conductance of DBTJ devices was done using SR-830 dual phase lock-in amplifier (Stanford Research), SR-570 current preamplifier (Stanford Research), SIM-980 Summing amplifier (Stanford Research), SIM-983 Scaling amplifier (Stanford Research) along with Agilent-4157B. All the electrical characterization setups were explained in detail with schematics in this chapter. Although the setups for electrical measurements were explained previously by Vishva Ray [5.1] and Ramkumar Subramanian [5.2], an attempt was made to explain the measurement setups again with any modifications made since.

5.2 Current-Voltage Measurements Set-up

The current voltage measurements on DBTJ devices were done either using Agilent-4155C parameter analyzer in NanoFab Research Center clean room (or) Agilent-4157B parameter analyzer in 105-BA electrical characterization lab. The Agilent-4155C parameter analyzer is connected to a probe station which is only capable of doing room

temperature measurements. All the low temperature measurements were done using Agilent-4157B parameter analyzer which is connected to ST-500 low temperature probe station (Janis Inc.). In this section all the intricate details pertaining to the current voltage measurements of DBTJ devices will be discussed.

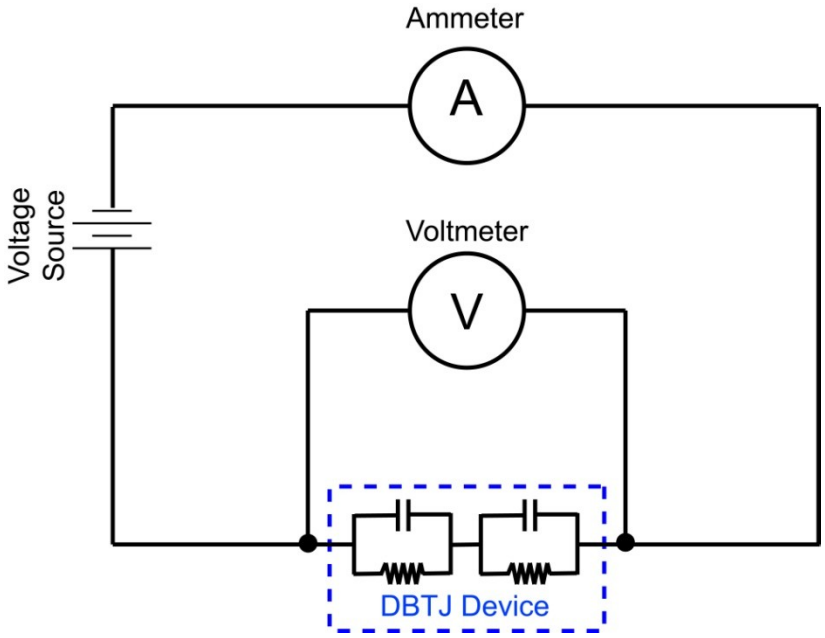


Figure 5-1 Schematic of Kelvin (4-wire) resistance measurement used for current-voltage measurements of DBTJ devices

For measuring the current-voltage characteristics of our DBTJ devices, Kelvin (4-wire) connections [5.3] were used to eliminate the residual resistance effects of the test leads and contacts. Figure 5.1 shows the schematic of the Kelvin connection used for current-voltage measurements on the DBTJ devices. In this configuration, the current is forced through the DBTJ device through the Force leads while the voltage across the DBTJ device is measured through a second set of leads known as the Sense leads. Although some small current may flow through the sense leads, it is usually negligible

and can be ignored for all practical purposes. To cancel the effects of the residual resistance, the test leads are connected as close to the device as possible.

5.2.1 Current-Voltage Measurements with Agilent-4155C

After fabrication of DBTJ devices the initial measurements were done using Agilent-4155C. The aim of these initial measurements was to find devices showing good current-voltage characteristics at room temperature. After identifying good devices which are showing sharp increase in current with increasing voltage (after the band gap voltage of quantum dots), slow measurements were also done on these devices. Care must be taken while doing these measurements. All these DBTJ devices are very sensitive to static charge. A static discharge wrist strap must be worn while doing any electrical measurements on these devices. After initial fast measurements on the devices, good devices were identified and slow measurements were run on these devices. Table 5-1 provides the details of all the parameters used for fast and slow measurements done on the DBTJ devices using Agilent-4155C parameter analyzer.

Table 5-1 Parameters for current-voltage measurements using Agilent-4155C parameter analyzer

	Fast Measurements	Slow Measurements
Point to Point spacing(mV)	20-25 mV	4 mV
Initial Hold time	0 seconds	30 seconds
Delay time	0 seconds	10 seconds
Wait time	1 seconds	5 seconds
Integration time	Medium	Long

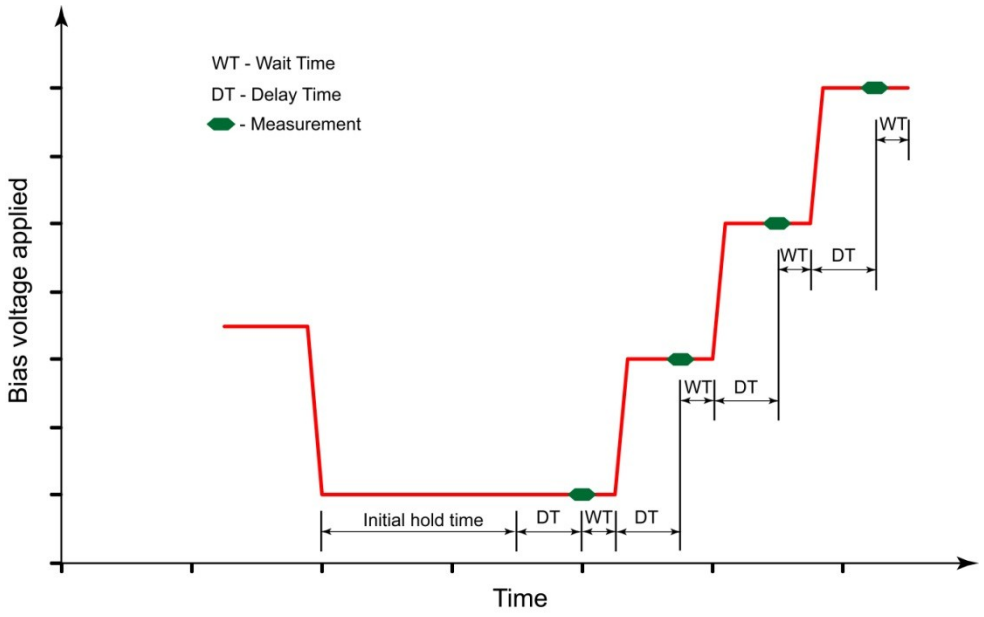


Figure 5-2 Sweep measurement parameters used for Agilent-4155C parameter analyzer

All the room temperature current-voltage data from DBTJ devices, using Agilent-4155C parameter analyzer were obtained using the parameters listed in Table 5-1 and to minimize the noise tri-axial cables were used during all the current-voltage measurements. The current-voltage measurements were done in voltage sweep mode, where the voltage bias across the DBTJ device is increased in a stepwise manner and the current across the device is measured. The physical meaning of Initial hold time, delay time and wait time can be understood by looking at figure 5.2. The initial hold time is the time for the parameter analyzer would wait before starting the measurement sweep mode. This is a one-time hold time applied only for the first point. The delay time is the time for which the system will wait, after applying the bias voltage at that particular step, before taking the current measurements. The wait time is the time for which the system will wait after completion of measurements and before applying the bias voltage for next step. So each measurement step consists of a delay time, actual measurement and wait

time. Only the initial point will have hold time in addition to the delay time, actual measurement and wait time.

5.2.2 Current-Voltage Measurements with Agilent-4157B in ST-500 Low Temperature Probe Station

All the low temperature measurements and some of the room temperature current-voltage measurements were done using Agilent-4157B parameter analyzer. This parameter analyzer is connected to the ST-500 low temperature probe station (Janis Inc.) in electrical characterization lab (105-BA). For loading samples into this probe station, the samples were diced and mounted onto the chip carriers as described in section 4.12 of chapter 4 of this thesis. Figure 5.3 shows the photographic images of the sample loading procedure.

For loading the samples to ST-500 low temperature probe station, first the chamber was vented with ultra dry nitrogen. During sample loading or unloading the user always wore a hair net and a face mask so as not to contaminate the interior chamber of the probe station. First, the optical microscope arm was rotated to the side, by loosening the screw which secures the microscope position, such that the top of the probe station was easily accessible. The top lid of the chamber was opened by unscrewing the four restraining screws. Care was taken release the screws slowly to let any built up pressure to vent slowly. Removing the lid gives access to top cover of the radiation shield. The top cover of the radiation shield was removed by unscrewing the four restraining screws. Extreme care was taken so as not to drop the screws inside the chamber. It would be impossible to recover any screws dropped into the chamber. Removing the top cover of radiation shield gives access to the sample stage. There are two screws with alumina washers and clamps which are used to secure the chip carrier with sample onto the

sample stage. After loosening up the screws for the sample mount, the chip carrier was placed at the center of the sample stage of the probe station. The chip carrier was then clamped in place by tightening the screws. Care must be taken to not over tighten these screws as this might result in cracking of the alumina washers. The radiation cover was then positioned on top and the screws tightened. The radiation cover was greased with thermally conducting apiezon grease to allow good thermal contact. Finally, after re-inspecting the o-ring around the top cover of the probe station, it was secured onto place by tightening the four screws.

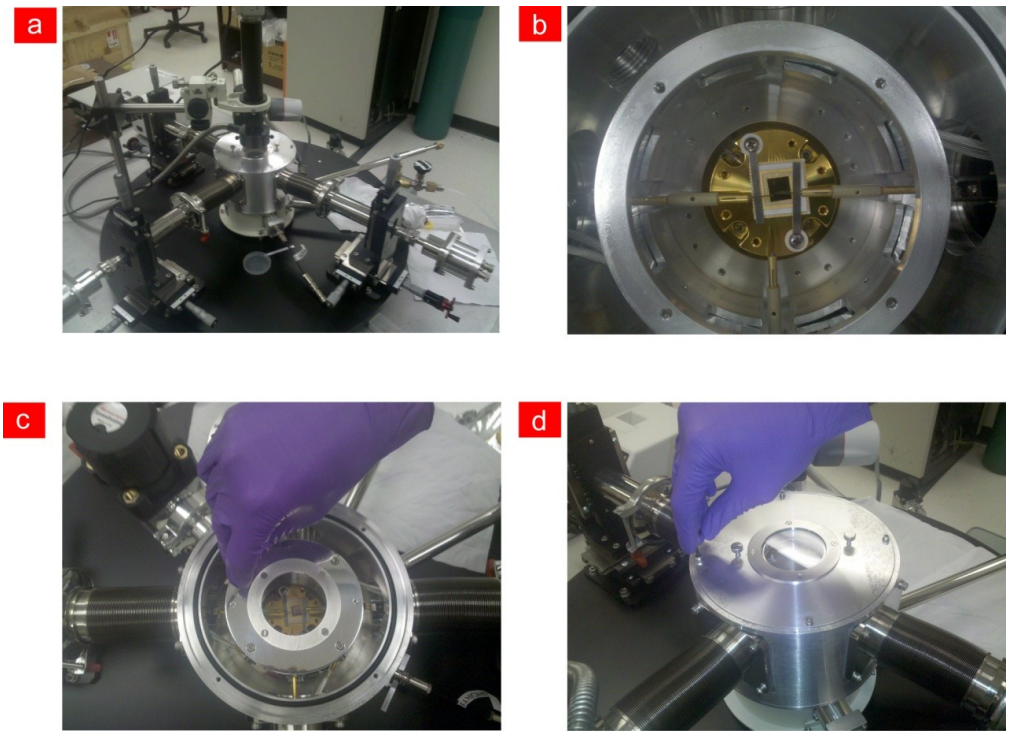


Figure 5-3 (a) Photograph of Janis ST-500 low temperature probe station showing the micromanipulators and optical microscope with boom. (b) The chip carrier mounted on the chuck held in place by clips (c) Radiation shield of the ST-500 and, (d) Top/vacuum cover of the ST-500 probe station [5.2]

Once the sample loading is completed, the chamber is purged with ultra dry nitrogen for a minimum of 15 minutes, while the dry mechanical pump (BOC Edwards, XD-5 dry scroll pump) is on. This helps in purging out any moisture that might have adsorbed on to the inner wall of probe station chamber while the chamber was open. After 15 minutes, the nitrogen flow is turned off and the chamber is pumped down to ~$5x10^{-3}$ Torr. It takes about 5 hours to reach this vacuum level. While doing low temperature measurements the chamber is further pumped down to even low pressures using a turbo pump (BOC Edwards). Before cooling down the sample stage for low temperature measurements the chamber vacuum must reach to at least $5x10^{-6}$ Torr. To reach this vacuum level the chamber has to be pumped down with turbo on for 12-15 hours. Only after reaching this vacuum level liquid nitrogen was flown through the sample stage to cool down the chamber. The liquid nitrogen was flow through the sample stage from a transfer line attached to the ST-500 low temperature probe station.

The liquid nitrogen dewar was refilled before every attempt to cool down the chamber to make sure there is enough liquid nitrogen to hold the sample stage at low temperature for at least one week. The liquid nitrogen dewar was refilled from the big liquid nitrogen tank using a transfer line. Protective eye wear and low temperature gloves are must while handling liquid nitrogen. After refilling the liquid nitrogen dewar, it is gently transferred to its previous position which was marked with a circle on the floor. Any change in the dewar position will affect the alignment of the transfer line going to the probe station.

Once the chamber is under high vacuum (<$5x10^{-6}$ Torr), the liquid nitrogen can be flow through the sample stage in order to cool down the sample. Before doing this, the sample stage temperature controller (Lake Shore 331) must be turned on and the stage temperature must be set to 300 K and heater mode must be set to high. The reason for

doing this is to hold the sample stage at room temperature while the surroundings of the chamber are cooled down, so that any condensation, happening during the initial stages of cooling down, will happen on the chamber walls instead of the sample itself. This is very important step, failing to follow this step will result in condensation on sample surface, which forms a thin layer of ice obstructing the electrical measurement of devices. The Lake Shore 331 temperature controller reads the temperature of the stage through a silicon diode located beneath the sample stage close to the top surface of the stage. The heater that is controlled by the temperature controller is also located under the sample stage.

With the heater controlled by Lake Shore 331 temperature controller on the liquid nitrogen transfer line is dropped into the liquid nitrogen dewar through the top orifice. This should be done slowly and once the lower end of transfer line touches the liquid nitrogen the valve on the transfer line must be opened slowly by rotating it in clock-wise direction. By the time the transfer line reached the bottom of dewar the valve was opened 2 turns. Once the transfer line reached the bottom of the dewar it was lifted up about 1 inch and the screw holding the transfer line was tightened. This is done to make sure that any accidental ice formation at the bottom of dewar won't impede the flow of liquid nitrogen through the transfer line. This part of cooling down the chamber using liquid nitrogen is explained in more detail in the ST-500 low temperature probe station manual. Once the transfer line is in place on the dewar end, the other end of the transfer line is gently slid into the liquid nitrogen entrance port on ST-500 low temperature probe station. This requires at least two individuals, one to hold the liquid nitrogen entrance port arm on ST-500 while the other person can gently slide the transfer line through it. Once it is all the way in the screw which holds the transfer line in place is tightened. At this point the liquid nitrogen will start to flow through the stage of ST-500 probe station, while the heater on

the sample stage is set to 300 K. The liquid nitrogen is left to flow for at least two hours before the temperature of the stage is cooled down. The cooling down can be done with the aid of automatic ramp control option of the Lake Shore 331 temperature controller. After the initial temperature holding time of 2 hours, the stage temperature is cooled down at a rate of 1 K/minute. This was done by setting the temperature of the stage to 77 K, and turning on the ramp option of the temperature controller with a ramp down rate of 1 K/minute. The cooling down of stage takes about 3 hours at this rate. Once the temperature reached 100 K the liquid nitrogen flow valve on the transfer line is completely closed and reopened to about 1-1½ turns which is just enough to cool down the temperature of stage to 77 K. This was done to prevent excessive flow of liquid nitrogen and accumulation of liquid nitrogen in the stage of ST-500 probe station. Failing to do this will cause multitude of problems like excessive ice formation on the liquid nitrogen vent port of ST-500 probe station, water condensation on the top view port of the ST probe station, condensation of ice on the sample and stage of the probe station and difficulty in raising the temperature of stage after the end of measurements.

For measurements done at temperature other than liquid nitrogen temperatures (150 K and 225 K) the stage heater was used to raise the temperature of stage to desired temperature while the liquid nitrogen is still kept flowing. This was done using the ramp option of Lake Shore 331 temperature controller. Once the desired temperature is reached the flow of liquid nitrogen was adjusted so there is no excessive ice formation on the liquid nitrogen vent port of ST-500.

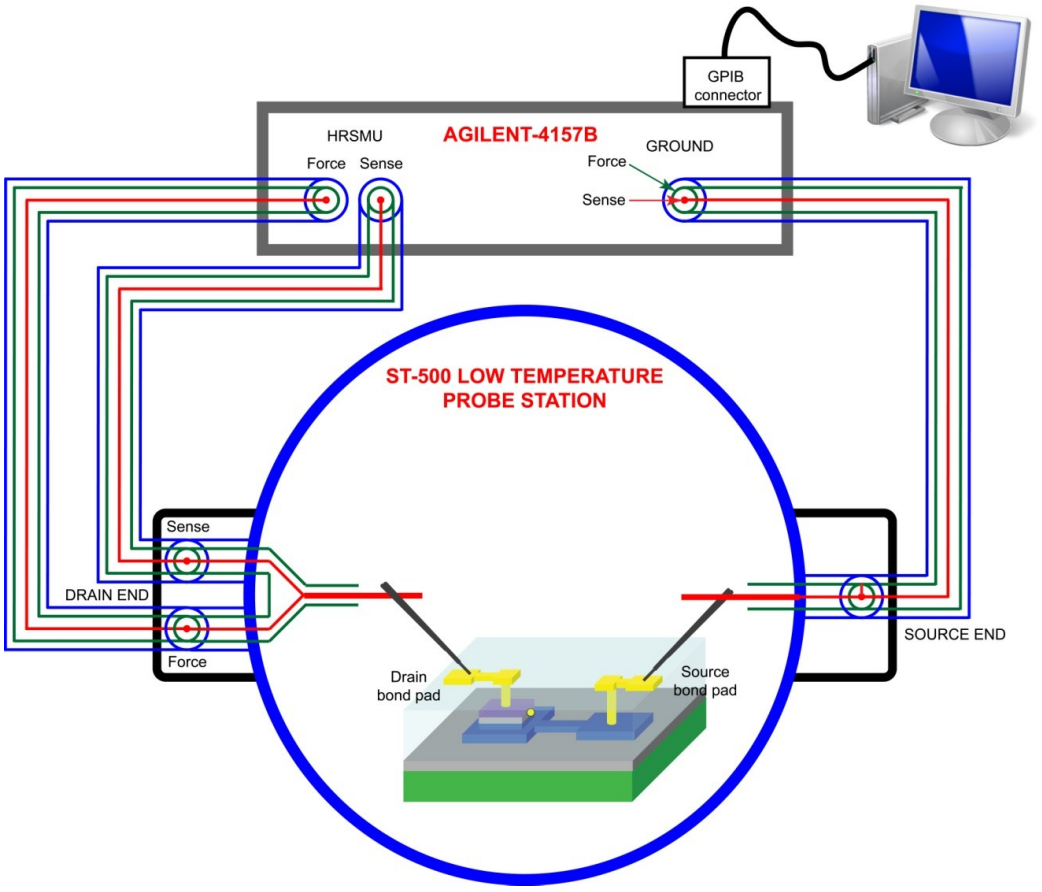


Figure 5-4 Schematics showing measurement setup and electrical connections for current-voltage measurements with Agilent-4157B parameter analyzer

Before starting any electrical measurements the Agilent-4157B was turned on and left to warm up for at least 30 minutes. The measurement setup and the electrical connections were shown schematically in figure 5.4. Low-noise triaxial cables SC-22 (Keithley Instruments Inc.) were used for these current-voltage measurements. The tri-axial cables have a center core conductor which carries the actual signal, the inner conductor is called the guard which is held at same potential as the center core

conductor, and the outer conductor is called shield which isolates the signal from any electromagnetic radiations which can cause noise.

Auto calibration settings on Agilent-4157B parameter analyzer must be turned off during the measurements. If this setting is not turned off the parameter analyzer automatically tries to calibrate itself once every 30 minutes, which will stop any running measurements and can potentially, ruin the device. Once the auto calibration is turned off, the wires were connected one by one starting from HRSMU force port of Agilent-4157B to force port on drain side of probe station, then HRSMU sense port of Agilent-4157B is connected to sense port on drain side of probe station. Then a specially made tri-axial cable was used to connect the ground port on Agilent-4157B to the sense port on source side of probe station. This tri-axial wire made in-house, using low-noise tri-axial cable SC-22 (Keithley Instruments Inc.) has tri-axial male connectors CS-631 (Keithley Instruments Inc.) on both ends. On the probe station end of the wire the center conductor i.e the force and the inner conductor i.e the sense in this case are shorted inside the tri-axial male connector as shown in figure 5.4. While connecting all these wires an anti-static wrist strap which is connected to safe ground terminal was worn.

After connecting all the wires, before we go on and touch a good device there are certain procedures to follow in order to minimize the chances of shorting the device due to electrostatic charge. Any metal surface can become charged due to accumulation of electrons, so does the probe tips inside the probe station. Any charge accumulated on the probes must be discharged and the both the probes must be brought to same potential before touching any good DBTJ device. This is done by touching both the probes on a dummy bond pad like a gate bond pad in this case. When the probes are brought in contact with bond pad, it skid gently on the surface leaving a scratch on the surface indicating the probe is in good contact with the bond pad. It is important to ensure

that the probes are in good contact with the bond pads to have good low-noise measurements. Once any charge accumulated on the probes is discharged, now the charge accumulated on the source and drain bond pads must be discharged. For doing this, first the probe on the source end of probe station is brought in contact to the source bond pad, then the probe on the drain end of probe station is touched to the same bond pad. This discharges any charge built up on the source bond pad. After this the probe on source side of probe station is gently lifted followed by lifting of drain side probe. The same process is repeated for the drain bond pad to remove any charge built up on the drain bond pad of DBTJ device. After this the probe on source end of probe station is lifted and moved to source pad of the device.

To minimize any external noise arising from ground loops, which is very source of noise in any measurement set-up, the outer shield of the tri-axial cables is isolated from the ground of the mechanical pump and other ground connections. After all the connections were made and the probes touched on the source and drain bond pads, 0V bias was manually applied through the Agilent-4157B and the microscope, light source for the microscope and the LCD monitor cables were unplugged from these devices and their power adapters removed from the power strip. This was done to ensure no ground loops existed. Only the Agilent 4157B should act as the ground. After the power cords of microscope, light source and the LCD monitor cable, the 0V bias was turned off. Now the device is ready for measurements.

Table 5-2 Parameters for current-voltage measurements using Agilent-4157B

Initial Hold time	600 seconds
Delay time	30 seconds
Step Delay Time	1 second
AV Number (High Speed Measurements)	1023
AIT Number (High Resolution Measurements)	100

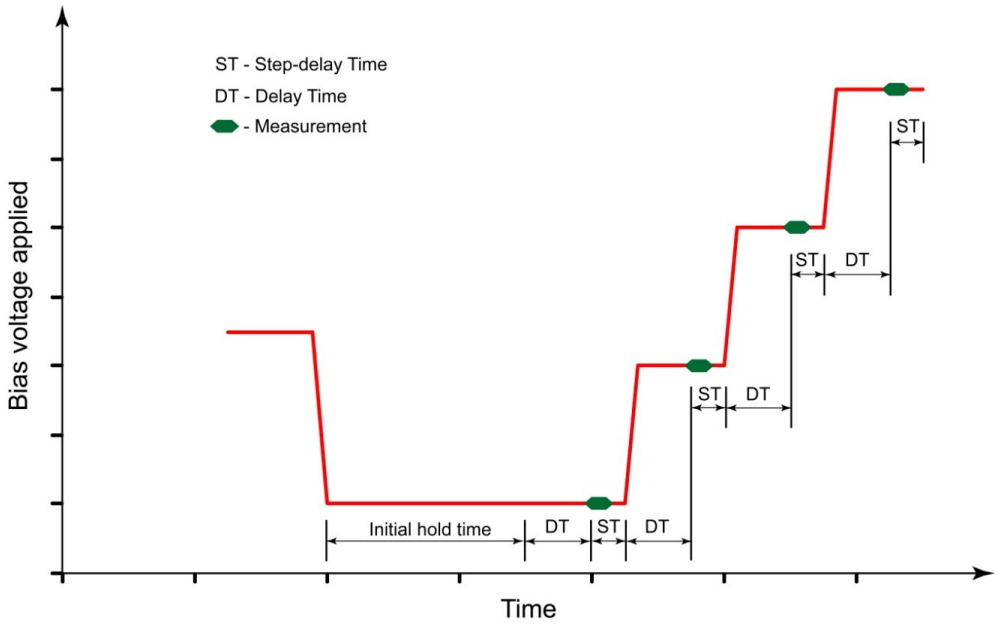


Figure 5-5 Sweep measurement parameters used for Agilent-4157B parameter analyzer

All the measurements were done in remote mode using a Lab view program as interface for communication between the Agilent-4157B and the computer. This program is developed in house. The Agilent-4157B is connected to the computer using as GPIB connector-IEEE 488.1 (National Instruments). All the parameters for current-voltage

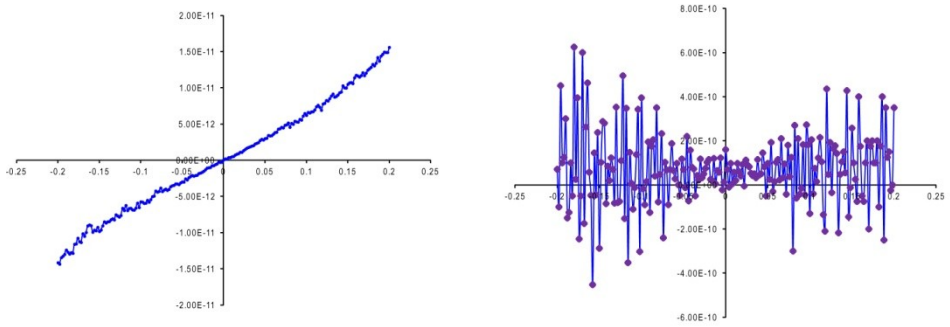
measurements are setup in the Lab view program used to control the Agilent-4157B parameter analyzer. The details of the parameters used are listed in Table 5-2.

5.3 Differential Conductance Measurements

Differential conductance measurements performed on quantum dot DBTJ devices provide information about the electron energy structure within the quantum dots. The differential conductance data was obtained either by numerically differentiating the current-voltage plots using Keithley Differentiation Method [5.4] or by direct differential conductance measurements using lock-in amplifier.

5.3.1 Numerical Differentiation – Keithley Method

The normal numerical differentiation of the current-voltage curves gives the differential conductance curves or the dI/dV curves. But the differential conductance curves might have very high noise depending on the quality and noise level of current-voltage measurements. Figure 5.6 shows current-voltage measurement plots and differential conductance plot obtained from normal numerical differentiation.



Current-voltage measurement

Numerically differentiated current-voltage plot to obtain dI/dV plot

Figure 5-6 Plots showing the noise in differential conductance obtained by numerically differentiated current-voltage measurements

To circumvent this problem of noise-level, a different approach was adopted for doing numerical differential conductance calculations. This method of numerical differentiation, known as keithley method, was originally developed for differential conductance measurements using Keithley 6221/2182A measurement setup. In the Keithley method, an alternating current is added to a linear staircase sweep. The amplitude of alternating portion of the current is differential current *(dI)*. The differential current is constant throughout the test. The current source is synchronized with the nanovoltmeter. The voltage is measured at each step and the difference in voltage or delta voltage is calculated between consecutive steps. Each delta voltage is then averaged with the previous delta voltage to calculate the differential voltage *(dV)*. A step-wise current impulse is sourced as shown in figure 5.7 and the resultant voltage measured at each increment of current. The keithley delta mode measurement method is shown in figure 5.7.

If the voltages measured at points A, B, C …H in figure 5.5 are V1, V2, V3 …. V8 respectively. The calculations for differential voltage *(dV)* from the measured values of *V* are detailed below:

$$dV1 = \frac{\left[(V1 - V2)/2 + (V3 - V2)/2\right]}{2} \cdot (-1)^0 \qquad (5\text{-}1)$$

$$dV2 = \frac{\left[(V2 - V3)/2 + (V4 - V3)/2\right]}{2} \cdot (-1)^1 \qquad (5\text{-}2)$$

$$dV3 = \frac{\left[(V3 - V4)/2 + (V5 - V4)/2\right]}{2} \cdot (-1)^2 \qquad (5\text{-}3)$$

$$dV4 = \frac{\left[(V4 - V5)/2 + (V6 - V5)/2\right]}{2} \cdot (-1)^3 \qquad (5\text{-}4)$$

$$dV5 = \frac{\left[(V5 - V6)/2 + (V7 - V6)/2\right]}{2} \cdot (-1)^4 \tag{5-5}$$

$$dV6 = \frac{\left[(V6 - V7)/2 + (V8 - V7)/2\right]}{2} \cdot (-1)^5 \tag{5-6}$$

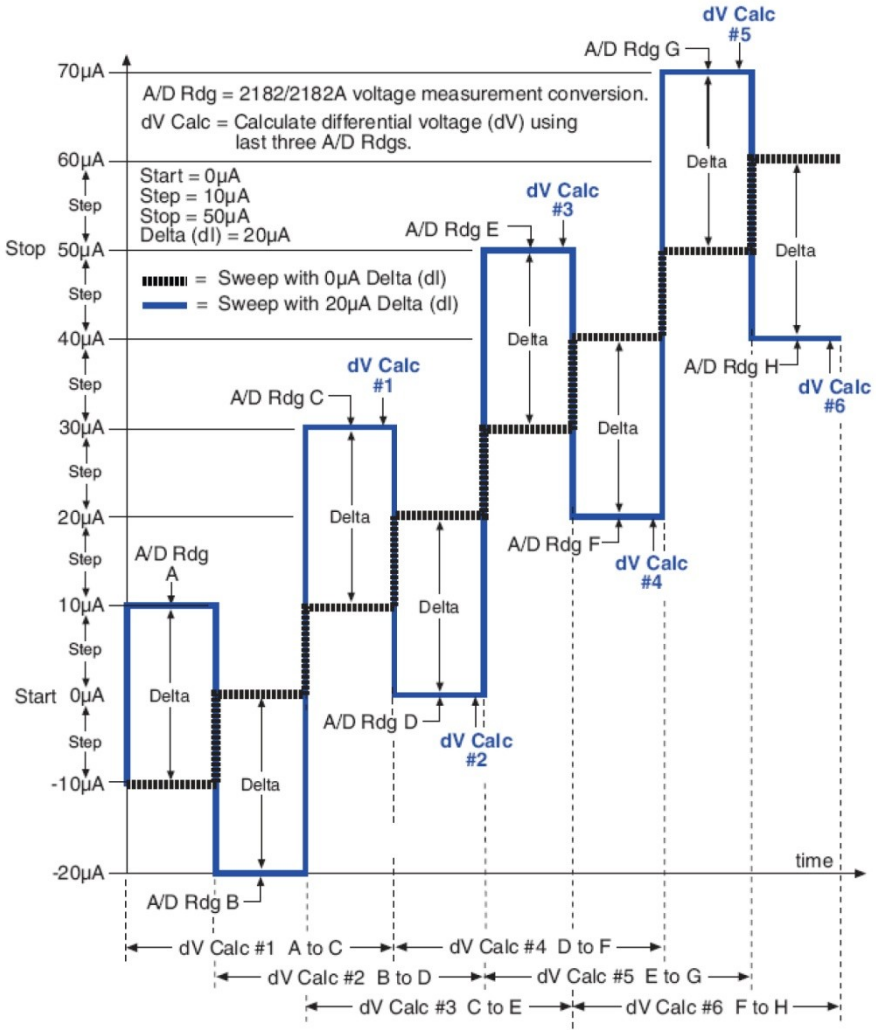


Figure 5-7 Keithley delta mode method of differential conductance measurement [5.4]

The differential current *(dI)* value is known and constant throughout the test and the differential voltage *(dV)* values are calculated from the measured voltages as shown above. The differential conductance *(dI/dV)* can be calculated easily. In the current study, instead of sourcing current, voltage was sourced and the resultant current through the DBTJ devices was measured using either Agilent-4155C or Agilent-4157B parameter analyzer. A simple staircase sweep of voltage was performed and the resultant current was measured. The current-voltage data was re-arranged to appear like the pulse input in figure 5.7. Using the above mentioned equations the averaged differential voltage *(dV)* and differential current *(dI)* values are calculated. Thus the differential conductance *(dI/dV)* was numerically calculated. The keithley method of numerically calculating the differential conductance proved to produce less noise than the conventional numerical differentiation method.

5.3.2 Direct Differential Conductance Measurements Using Lock-In Amplifier

In this section the measurement setup of direct measurement of differential conductance *(dI/dV)* using lock-in amplifier will be discussed. Lock-in amplifiers are used to detect and measure very small AC signals, all the way down to a few nanovolts. Accurate measurements may be made even when the small signal is obscured by noise sources many thousands of times larger. Lock-in amplifier uses a technique known as phase-sensitive detection to single out the component of the signal at a specific reference frequency and phase. Noise signals, at frequencies other than the reference frequency, are rejected and do not affect the measurement.

The measurement setup for direct differential conductance measurements is shown in figure 5.8. As can be seen from the above figure 5.8 the lock-in amplifier is used in conjunction with several other instruments to obtain the direct differential conductance

measurements. The basic idea of this setup is to mix a small reference AC signal (whose frequency is know) with the DC bias and the output signal at this particular frequency will be measured. The output signal gives us the direct differential conductance.

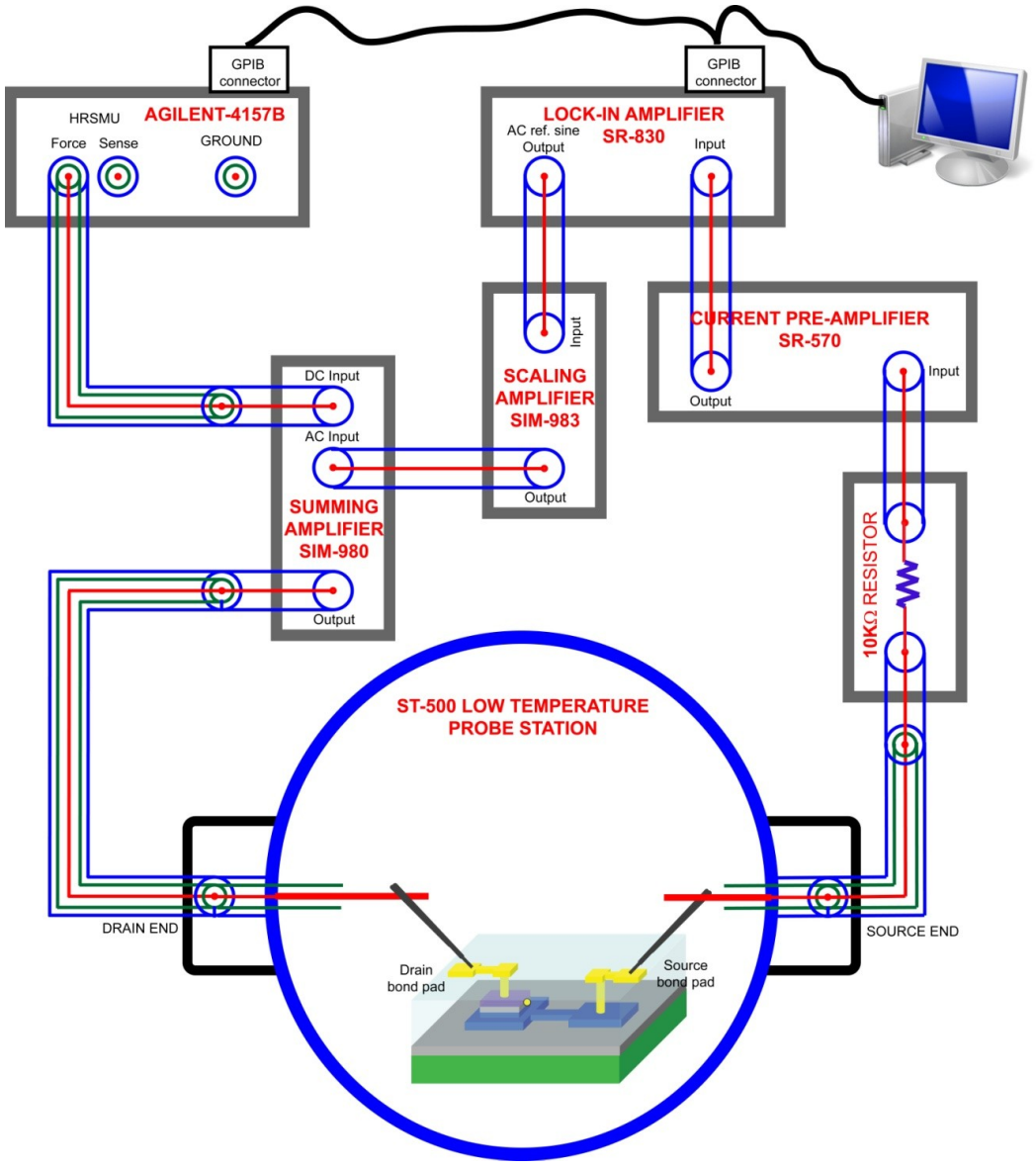


Figure 5-8 Measurements setup for direct differential conductance measurements using Lock-in amplifier

The DC signal from Agilent-4157B is mixed with AC reference sine signal from the Lock-in amplifier. The AC reference sine signal is first scaled down to 1 mV from the 4 mV output coming from SR-830 lock-in amplifier using the scaling amplifier SIM-983. The scaled down AC reference sine signal is then mixed with the DC signal from Agilent-4157B using the summing amplifier SIM-980. This signal is passed through the DBTJ device and the output signal from the device is passed through current pre-amplifier SR-570 to attenuate the signal, before sending it back to the Lock-in amplifier. The lock-in amplifier then multiplies this input signal with the reference sine-wave signal. Mathematically speaking, sine waves of differing frequencies are orthogonal, i.e. the average of the product of two sine waves is zero unless the frequencies are exactly the same. The product of this multiplication yields a DC output signal proportional to the component of the signal whose frequency is exactly locked to the reference frequency. The low pass filter (which follows the multiplier) provides the averaging which removes the products of the reference with components at all other frequencies. A detailed mathematical derivation of how the differential conductance measurement was obtained from the DC output signal of lock-in amplifier is discussed earlier in the thesis of Ramkumar Subramanian [5.2]. However, this mathematical derivation is revisited in this chapter in order to have a comprehensive understanding of differential conductance *(dI/dV)* measurements using SR-830 lock-in amplifier.

Let us consider a current-voltage plot where current *I* varies as a function of the applied bias voltage *V*. We can denote it with the following relation

$$I = I(V) \tag{5-7}$$

If we add an infinitesimally small voltage of ΔV, then the current I at the voltage $V_0 + \Delta V$ is given by,

$$I(V_0 + \Delta V) = I(V_0) + \left(\frac{dI}{dV}\right)_{V_0} .\Delta V \tag{5-8}$$

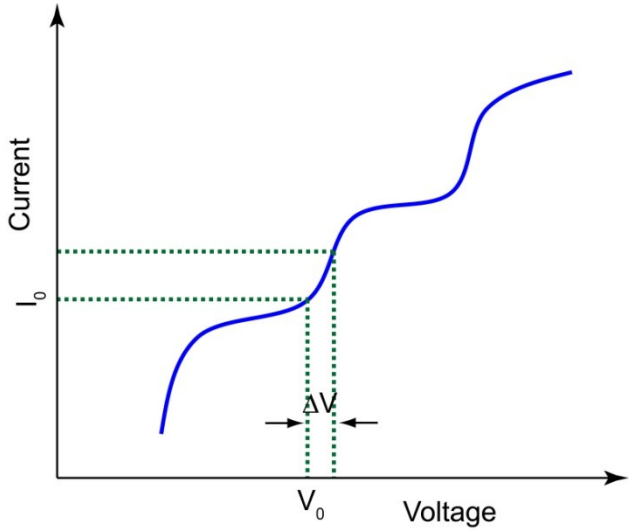


Figure 5-9 Current-Voltage plot where at voltage V_0, current is I_0 and with increase of voltage by ΔV the current increases

The infinitesimally small voltage ΔV can be written as a sine function as shown below

$$\Delta V = V_{input} \sin \omega_{ref} t \tag{5-9}$$

From the above two equation (5-8) and (5-9), assuming that there is no phase difference, the equation for current I as a function of time t can be written as follows

$$\Rightarrow I(t) = I(V_0) + \left(\frac{dI}{dV}\right)_{V_0} .V_{input} \sin \omega_{ref} t \tag{5-10}$$

If there is a phase difference, then the above equation (5-10) transforms as follows

$$I(t) = I(V_0) + \left(\frac{dI}{dV}\right)_{V_0} .V_{input} \sin\left(\omega_{ref} t + \theta_{sig}\right) \tag{5-11}$$

where, θ_{sig} , is the phase difference. This is the equation for current output from the DBTJ device. This signal is fed back to SR-830 lock-in amplifier, which multiplies it with a reference signal (in this case it is from internal sine-wave generator) using a phase sensitive detector or multiplier. The phase sensitive detector (PSD1) output is the product of two sine waves

$$V_{PSD1} \propto I(t) \cdot V_{ref} \sin\left(\omega_{ref} t + \theta_{ref}\right) \tag{5-12}$$

where, $V_{ref} \sin\left(\omega_{ref} t + \theta_{ref}\right)$, is the reference signal from the internal oscillator of the lock-in amplifier SR-830.

$$V_{PSD1} \propto I(t) \cdot V_{ref} \sin\left(\omega_{ref} t + \theta_{ref}\right) \tag{5-13}$$

$$V_{PSD1} \propto \left[I(V_0) + \left(\frac{dI}{dV}\right)_{V_0} .V_{input} \sin\left(\omega_{ref} t + \theta_{sig}\right) \right] \cdot V_{ref} \sin\left(\omega_{ref} t + \theta_{ref}\right) \tag{5-14}$$

$$\begin{aligned} V_{PSD1} \propto & \left\{ I(V_0) \cdot V_{ref} \sin\left(\omega_{ref} t + \vartheta_{ref}\right) \right\} \\ & + \left\{ \left[\left(\frac{dI}{dV}\right)_{V_0} .V_{input} \sin\left(\omega_{ref} t + \theta_{sig}\right) \right] \cdot V_{ref} \sin\left(\omega_{ref} t + \theta_{ref}\right) \right\} \end{aligned} \tag{5-15}$$

$$V_{PSD1} \propto \left\{ I(V_0) \cdot V_{ref} \sin\left(\omega_{ref} t + \vartheta_{ref}\right) \right\} + \frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_{ref} \begin{Bmatrix} \cos\left[(\omega_{ref} - \omega_{ref})t + \theta_{sig} - \theta_{ref}\right] \\ -\cos\left[(\omega_{ref} + \omega_{ref})t + \theta_{sig} + \theta_{ref}\right] \end{Bmatrix} \quad (5\text{-}16)$$

$$V_{PSD1} \propto \left\{ I(V_0) \cdot V_{ref} \sin\left(\omega_{ref} t + \vartheta_{ref}\right) \right\} + \frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_{ref} \begin{Bmatrix} \cos\left[\theta_{sig} - \theta_{ref}\right] \\ -\cos\left[2\omega_{ref} t + \theta_{sig} + \theta_{ref}\right] \end{Bmatrix} \quad (5\text{-}17)$$

When the phase sensitive detector (PSD1) output is passed through a low pass filter, all ac components are filtered/removed including the *2ωt* terms, leaving the following pure DC component of signal

$$V_{PSD1} \propto \frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_{ref} \left\{\cos\left(\theta_{sig} - \theta_{ref}\right)\right\} \quad (5\text{-}18)$$

When the signal is passed through phase sensitive detector and the low pass filter, only the signal close to the reference frequency is detected and retained. So the noise close to reference frequency is the only noises present in the signal, noises at all other frequencies are removed by the low pass filter. Noise at frequencies very close to the reference frequency will result in very low frequency ac output along with the phase sensitive detector output. Their attenuation depends upon the low pass filter bandwidth and rolloff. A narrower bandwidth will allow only the signal at the reference frequency which will result in a true DC output and be unaffected by the low pass filter.

In general, SR-830 lock-in amplifier uses a phase-locked loop (PLL) to generate the reference signal. However in this case, since the internal oscillator was used to generate the reference signal, it is automatically phase locked. When the θ_{sig} is the same

as θ_{ref} then, cos (θ_{sig} - θ_{ref}) = cos (0) = 1, otherwise the output of the single phase sensitive detector (PSD1) contains the cosine term. So the output signal is dependent on the phase difference. This phase dependency of the PSD output signal was taken care of by adding another PSD and the signal is multiplied with a reference whose phase is shifted by 90^0. The PSD2 uses the reference signal which is 90^0 phase shifted, so the output from PSD2 can be written as follows

$$V_{PSD2} \propto I(t) \cdot V_{ref} \sin\left(\omega_{ref} t + \theta_{ref} + 90^0\right) \tag{5-19}$$

$$V_{PSD2} \propto \frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_{ref} \left\{\cos\left(\theta_{sig} - \theta_{ref} - 90^0\right)\right\} \tag{5-20}$$

$$V_{PSD2} \propto \frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_{ref} \left\{\sin\left(\theta_{sig} - \theta_{ref}\right)\right\} \tag{5-21}$$

The above proportionality equations (5-18) and (5-21) showing output of the two phase sensitive detectors PSD1 and PSD2 can be rewritten as shown below, by adding a gain term *G*. This gain value is a combination of gain from both the lock-in amplifier SR-830 (if operating in current input mode) and the current pre-amplifier (SR-570) gain values.

$$X = V_{PSD1} = G \cdot \frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_{ref} \left\{\cos\left(\theta_{sig} - \theta_{ref}\right)\right\} \tag{5-22}$$

$$Y = V_{PSD2} = G \cdot \frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_{ref} \left\{\sin\left(\theta_{sig} - \theta_{ref}\right)\right\} \tag{5-23}$$

The *X* and *Y* represent the signal as a vector, relative to the lock-in reference oscillator signal, where *X* is called the 'in-phase' component and *Y* is called the 'quadrature' component. This is because, when phase difference (θ_{sig} - θ_{ref}) = 0, the PSD

measures only *X* or the signal and *Y* is equal to zero. The phase dependency of the output signal can be removed by computing the magnitude of the vector signal. If *R* is the magnitude of the vector signal, then

$$R = \sqrt{X^2 + Y^2} \tag{5-24}$$

$$R = \sqrt{\begin{aligned}&\left[G \cdot \frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_{ref} \left\{\cos\left(\theta_{sig} - \theta_{ref}\right)\right\}\right]^2 \\ &+\left[G \cdot \frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_{ref} \left\{\sin\left(\theta_{sig} - \theta_{ref}\right)\right\}\right]^2\end{aligned}} \tag{5-25}$$

$$R = \frac{1}{2} G \cdot \left(\frac{dI}{dV}\right)_{V_0} \cdot \left(\sqrt{2} \cdot V_{input,RMS}\right) \cdot \left(\sqrt{2} \cdot V_{ref,RMS}\right) \tag{5-26}$$

$$R = G \cdot \left(\frac{dI}{dV}\right)_{V_0} \cdot \left(V_{input,RMS}\right) \cdot \left(V_{ref,RMS}\right) \tag{5-27}$$

R measures the signal amplitude and does not depend upon the phase between the signal and lock-in reference. In SR-830 which is a dual-phase lock-in amplifiers, two PSDs with reference oscillators 90° apart are present, and it is capable of measuring X, Y and R directly. The output of the lock-in amplifier *R* thus obtained is an amplified signal containing gain from the current preamplifier and lock-in amplifier. It can be converted to real differential conductance term as follows

$$\left(\frac{dI}{dV}\right)_{V_0} = \left(\frac{R}{G}\right) \frac{1}{\left(V_{input,RMS}\right) \cdot \left(V_{ref,RMS}\right)} \tag{5-28}$$

So by adding a small AC component to the DC bias voltage, the differential conductance of DBTJ devices can be measured directly. This is accomplished by using SR-830 lock-in amplifier with the measurement setup shown in figure 5.8. After loading the DBTJ devices mounted on chip carrier into to ST-500 low temperature probe station as discussed in earlier sections, the electrical wires were connected to get the measurement setup ready. Figure 5-10 shows the measurement setup with all the wires connected

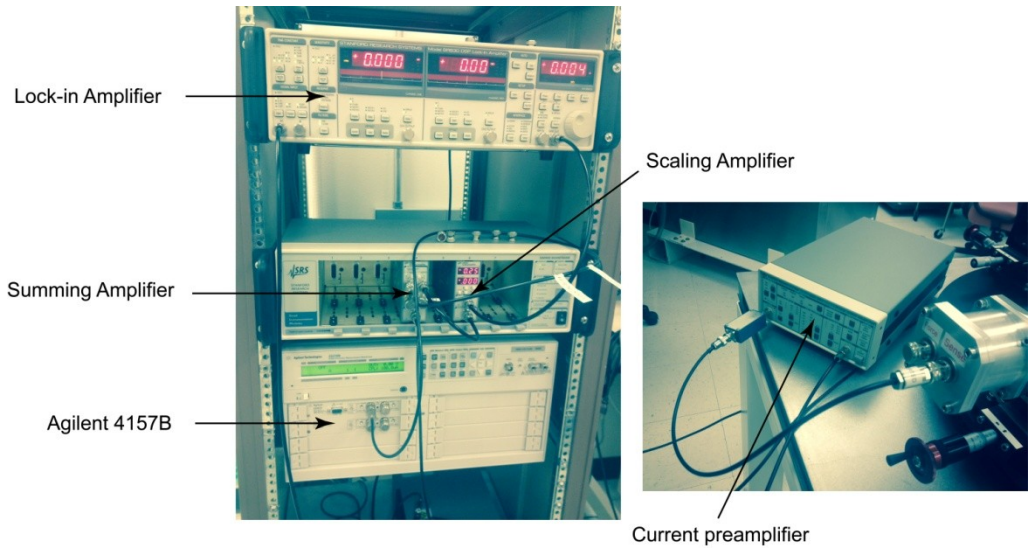


Figure 5-10 Actual measurement setup for direct differential conductance measurements using lock-in amplifier

All the wires used for making the electrical connections were custom made in house using low-noise cable. All the equipment were turned on for at least 30 minutes to warm up before connecting the wires. Anti-static wrist strap was worn, to minimize the risk of shorting the device from static charge, before making any electrical connection of the wires. First the HRSMU force on Agilent-4157B is connected to the input1 on summing amplifier SR-980. A special tri-axial to BNC adapter was used for making this

connection, to ensure the guard is isolated. The sine-out on SR-830 is connected to the input port on scaling amplifier SR-983 and the output of SR-983 is connected to input 2 on summing amplifier SR-980. The scaling amplifier is set to 0.25 times, which means amplitude of the input of scaling amplifier is scaled down by a factor of four. The setting on summing amplifier is selected to '+' which means the two inputs will be added. The output from the summing amplifier is connected to the drain side of the ST-500 probe station. Then the source side of probe station is connected to the 10KΩ resistor box (low noise metal-film resistor, 0.5W, Allied Electronics Inc.) and the other end of resistor box is connected to the SR-570 current pre-amplifier. The purpose of the resistor is to protect the equipment from high currents in the event of shorting of the device under test. The output of the SR-570 current preamplifier is the connected to the Input A on SR-830 lock-in amplifier. The only ground connected in this setup is the ground of the Agilent-4157B, all other equipment were left floating without any ground. This was done to avoid any ground loop formation that can be source of noise.

After lowering the probe tips, and manually forcing 0V bias voltage through HRSMU force of Agilent-4157B. The digital microscope, light source and LCD monitor were all unplugged and the power chords removed from the power strip. All this was done while holding the HRSMU force at 0 V. After all these steps were completed, the output of the HRSMU was turned off and the system was ready for measurement.

The measurements were done and data was collected by remotely controlling the SR-830 lock-in amplifier and Agilent-4157B using a Labview program developed in house. There are several settings available for the SR-830 lock-in amplifier and the current pre-amplifier SR-570. Selecting wrong settings can result in no signal from the DBTJ device under test. First the settings used for SR-830 lock-in amplifier will be discussed.

5.3.2.1 Lock-In Amplifier SR-830 Settings

The list of parameters that have to be carefully selected for SR-830 lock-in amplifiers [5.5], in order to get a good signal from the DBTJ device under test are

- Amplitude of the sine out
- Frequency of the sine out
- Input type
- Notch filters
- Time constant (cut-off frequency and slope), and,
- Sensitivity

1. Amplitude of the sine out: The amplitude of the sine out has to be a small as possible in order to obtain the smallest changes in differential conductance of the devices under test. The minimum amplitude that can be generated in SR-830 is 4mV. A scaling amplifier SR-983 was employed to further decrease the amplitude of the sine out wave to 1mV, before mixing it with the DC voltage bias.
2. Frequency of sine out: Selection of frequency varies from device to device, depending on the current range of the device. To determine the right frequency the current-voltage measurements were performed on the device and depending on the current range of device the frequency to be used is determined. Depending on the current range of the device, the resistance of the device is estimated. Then using the capacitance of the cables ($5x10^{-12}$ Farad) [5.6] the RC delay time of the circuit was calculated. From these estimated RC delay times, the range of frequency around which the measurements have to be carried out was determined.

3. Input type: There are three different options for input type i.e. A (single input), B (differential input) or current (I). In this particular case of measurement setup input A is the appropriate selection, since the input we are providing to SR-830 lock-in amplifier is the attenuated voltage signal from the current pre-amplifier SR-570, which convert the current signal into voltage signal.

4. Notch filters: The line notch filters are pre-tuned to the line frequency (50 or 60 Hz) and twice the line frequency (100 or 120Hz). Both the notch filters with an attenuation depth of 30 dB are used to reduce any line noise.

5. Time constant: The time constant is a low pass filter with tunable cutoff frequency. Depending on the time constant selected the cutoff frequency changes. Smaller time constant implies larger cutoff frequency which in turn implies more noise. Larger time constants mean lower cutoff frequency which means lower noise. But the trade off comes in the form of settling time, a settling time of at least 5x of the time constant is necessary for accurate measurements. This means longer measurements times are imminent when using time constants of beyond 10 seconds. The maximum filter slope of 24 dB/oct was chosen to reduce any ac noise in the output.

6. Sensitivity: The sensitivity is the scale of the measured output and can be varied from 2nV to 1V scale in the voltage scale and from 2fA to 1μA (RMS) in the current scale. The auto gain mode automatically adjusts the sensitivity to the required scale.

5.3.2.2 Current Pre-Amplifier SR-570 Settings

The parameters for SR-570 [5.7] which have to chosen carefully to get good signal from the DBTJ device under test are listed below.

- Bias voltage
- Input offset
- Invert
- Filter type and cut-off frequencies
- Gain mode
- Sensitivity

1. Bias voltage: This option was disabled as there was no need to apply any additional bias in this particular measurement setup.
2. Input offset: This option was also disabled as there was no need to offset the signal.
3. Invert: The invert option can invert the output of SR-570 with respect to input signal. This option was disabled as well.
4. Filter type and cut-off frequencies: There are three different options for filter type i.e. high pass filter, low pass filter and band pass filter. The filter type and the cut-off frequencies are selected depending on the operating frequency of the measurements. Since the range of frequencies we are operating, depending on device current, are between 7 Hz – 15 Hz, a band pass filter of 3 Hz – 30 Hz with 6 dB/oct roll off was chosen.
5. Gain mode: There are three options for gain mode i.e. low noise mode, high bandwidth mode and low drift mode. An wrong gain setting can potentially chop-off all the signal coming from the device. Figure 5-11 shows plots of amplifier gain and current noise in different modes (low noise and high bandwidth) for several different sensitivity ranges. As our measurement units have very low currents (1 nA-10 nA) and the operational frequency setting of 7-15 Hz, only high

bandwidth mode can be used. As shown in figure 5-11, the plots for amplifying bandwidth for several different sensitivity setting, if we operate at 10 Hz frequency and use low noise mode about ~50% of actual signal is cutoff for 1 nA/V sensitivity. Where as in high bandwidth mode the actual signal is not cut-off. So high bandwidth was chosen. Again these setting are dependent on the current range of the device and the frequencies we are operating at. For a high current device it will be better to run the measurement in low noise mode rather than high bandwidth mode.

Table 5-3 Operational bandwidth and current noise for various gain modes and sensitivity settings [5.7]

Sensitivity (A/V)	Bandwidth (3dB)		Noise/$\sqrt{Hz}^2$		DC Input Impedance
	High BW	Low noise	High BW	Low noise	
1 mA/V	1 MHz	1 MHz	150 pA	150 pA	1 Ω
100 μA/V	1 MHz	500 kHz	100 pA	60 pA	1 Ω
10 μA/V	800 kHz	200 kHz	60 pA	2 pA	100 Ω
1 μA/V	200 kHz	20 kHz	2 pA	600 fA	100 Ω
100 nA/V	20 kHz	2 kHz	600 fA	100 fA	10 kΩ
10 nA/V	2 kHz	200 Hz	100 fA	60 fA	10 kΩ
1n A/V	200 Hz	15 Hz	60 fA	10 fA	1 MΩ
100 pA/V	100 Hz	10 Hz	10 fA	5 fA	1 MΩ
10 pA/V	20 Hz	10 Hz	10 fA	5 fA	1 MΩ
1 pA/V	10 Hz	10 Hz	5 fA	5 fA	1 MΩ

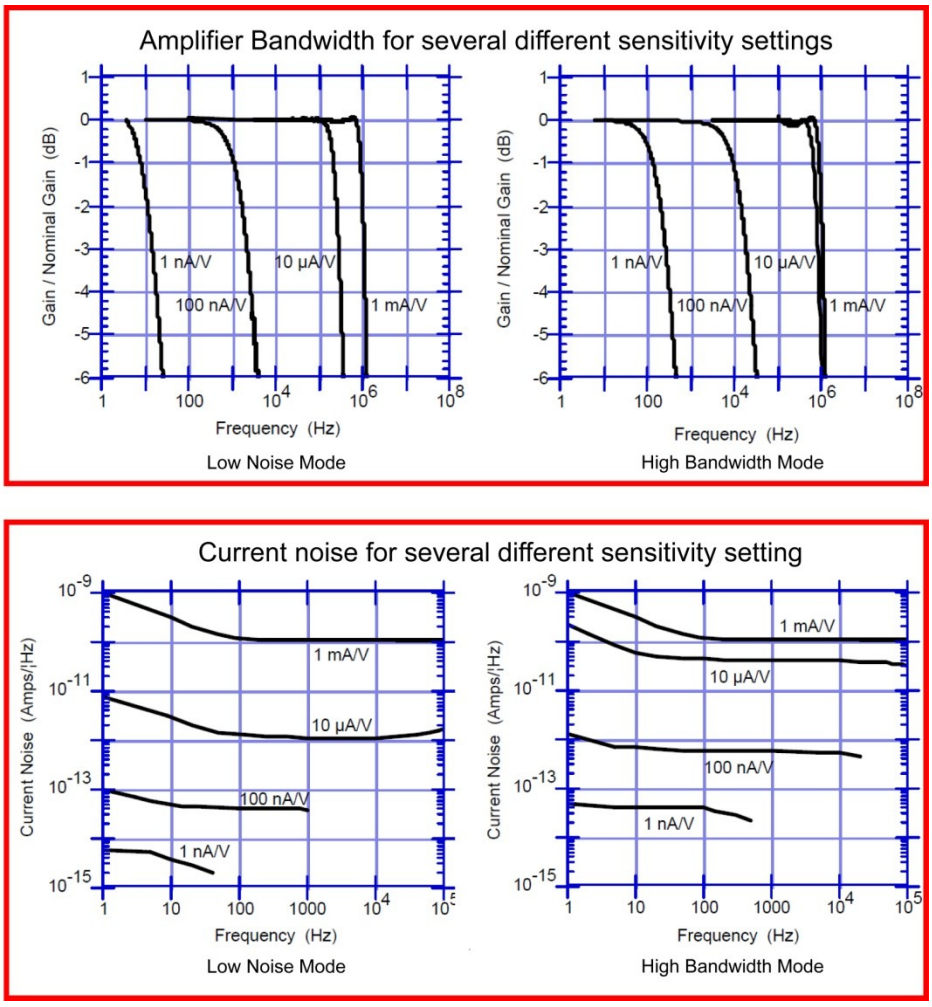


Figure 5-11 Plots showing amplifier bandwidth and current noise as function of frequency for several different sensitivity settings on the current pre-amplifier SR-570. [5.7]

6. Sensitivity: This determines the amount of gain in the signal output from SR-570. Depending on the current range of the specific DBTJ device unit, the sensitivity was chosen. For example, for a measurement on device with current range of 1 nA at +1V, the sensitivity was chosen as 5n A/V. Wrong sensitivity settings can give output overload error.

5.4 Electrical Measurements of CdTe And CdSe DBTJ Devices

In this section the electrical measurements done on the CdTe DBTJ devices and the CdSe DBTJ devices are presented. All the current-voltage measurements are done by either using Agilent-4155C or Agilent-4157B parameter analyzer. The differential conductance data is obtained by using keithley method of numerical differentiation that was discussed in the earlier sections of this chapter or by measuring direct differential conductance using lock-in amplifier.

5.4.1 DBTJ Devices with ~7.8nm CdTe Quantum Dots

In figure 5-12 current-voltage (IV) measurements done on ~7.8nm CdTe DBTJ device is shown. The band gap of bulk CdTe is ~1.44eV. For the ~7.8nm CdTe the theoretical band gap should be ~1.65eV [5.22]. In the IV measurement this band gap is clearly seen. The zero conduction region of the IV curve represents the band gap of the quantum dot. Depending on the voltage division factor across both the tunnel junctions of the DBTJ devices, the zero conduction region of the IV measurements can be larger than the theoretical band gap of the quantum dot. As the conduction band energy levels align with the source an increase in current is observed with increasing voltage bias. The DBTJ devices were probed in such a way that the conduction band is always on the positive bias side of the IV measurement. This measurement was done at room temperature. The current onset is observed around 0.715 Volts as indicated by the first red arrow in figure 5-12.

The step-wise increase of current with voltage bias was observed only on the positive bias side i.e. the conduction band side, no signature of step-wise increase of current was observed on the negative bias side of the IV measurement. Further investigation of the IV data was required to determine the reason for this absence of any

signature of step-wise increase in current on the negative bias side of the measurement. In order to do this the IV data obtained was digitally filtered by using the Keithley method to obtain the differential conductance data and a noise free IV data. This data is presented in figure 5-13.

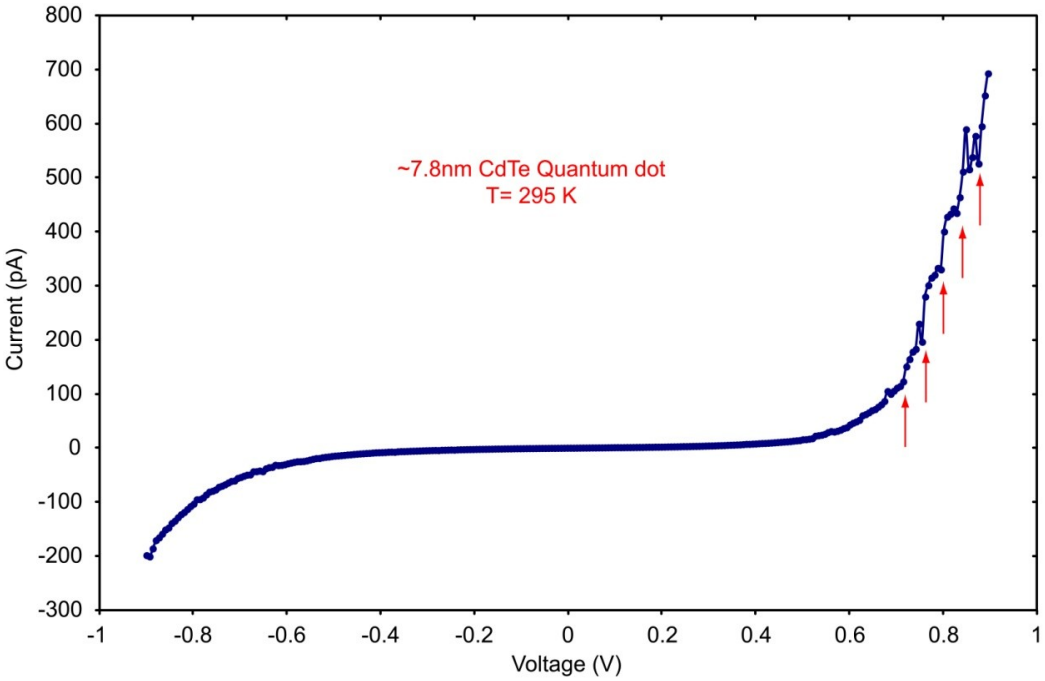


Figure 5-12 Current-Voltage measurement of ~7.8nm CdTe DBTJ device- Device#1

The IV plot shown in figure 5.13(a) is the digitally filtered data obtained by using Keithley method discussed in earlier section 5.1.2.1 of this chapter. A zoomed in view of this data is shown in figure 5.13(b). The noise in this IV plot has reduced compared to the original IV plot measured, at the same time the step-wise increase in current is still clearly seen. Each point where an increase in current was observed is denoted by a red arrow in figure 5.13(b). The spacing between each current jump was measured. The size of all the steps was found to be equal and around ~40mV. Since all the steps were equal in size,

the steps that are seen in the IV plot can be understood as charging energy of the ~7.8nm CdTe quantum dot.

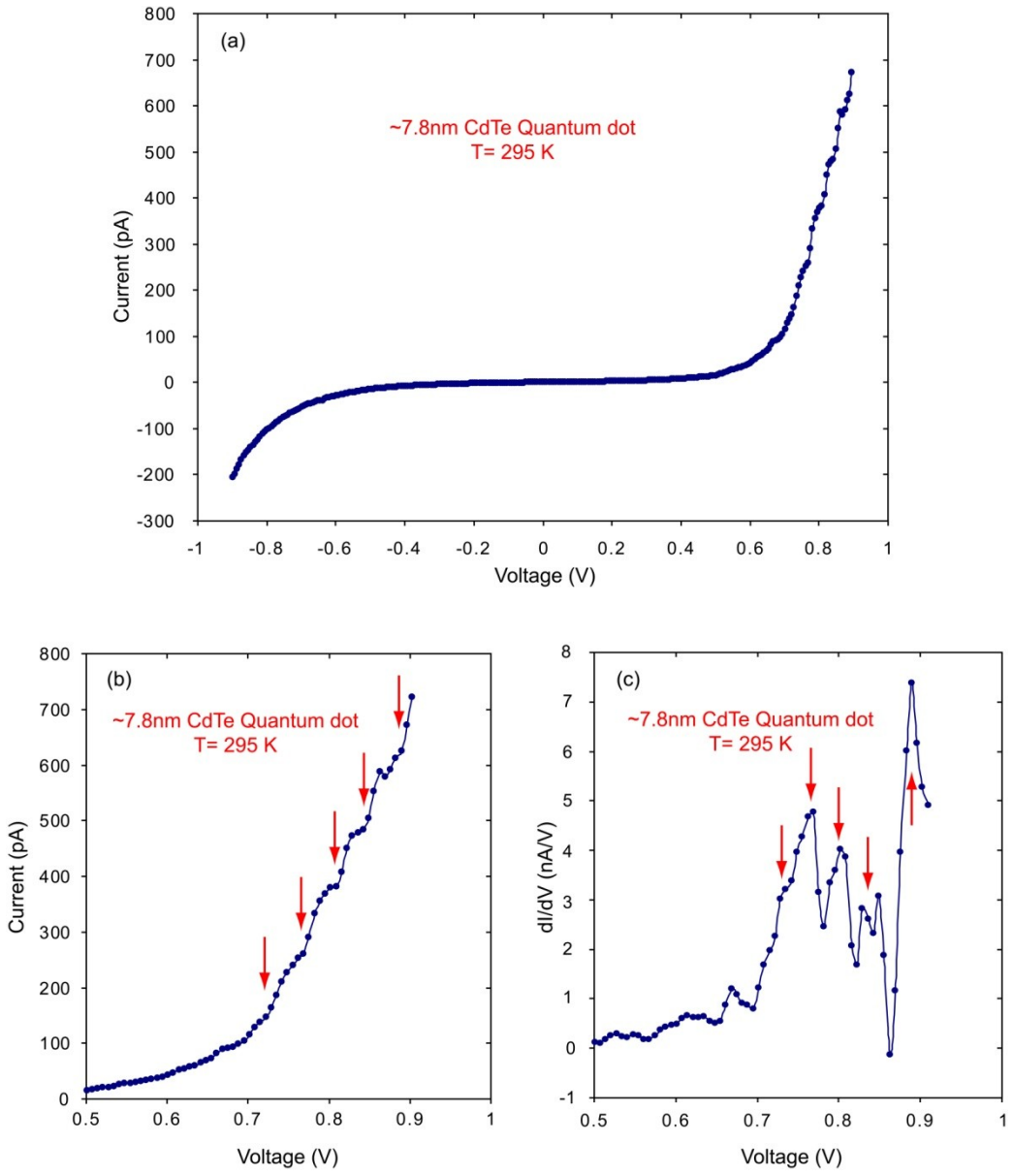


Figure 5-13 Current-Voltage plots and differential conductance plot of ~7.8nm CdTe quantum dot device, obtained using keithley numerical differentiation method- Device#1

The size of the CdTe quantum dot might be too large to see any separation between the energy levels in the conduction band. In most of the DBTJ devices the step wise increase in current was not seen in the negative bias region or the valence band region. Only a handful of DBTJ devices showed clear steps in the negative bias region or the valence band region. The absence of steps on the negative bias region can be because of the position of the particle and the tunnel junction characteristics. In our device fabrication as already discussed, the position of quantum dots is random and so controlling the characteristics of the tunnel junctions is highly impossible. It depends on the several different factors like the thickness of dielectric layer, the dry etching condition, the position of the quantum dot with respect to the electrodes and the material of the tunnel junction region.

Figure 5.13(c) shows zoomed in view of the differential conductance plot of ~7.8nm CdTe quantum dot device, which was obtained by numerically differentiating the IV data using keithley method of numerical differentiation. Clear conduction peaks were seen in this plot, which were indicated by red arrows.

Figure 5.14 shows IV and dI/dV characteristics of another ~7.8nm CdTe quantum dot device. Even though the background current is very high, the band gap of the quantum dot can still be seen. The onset of sharp jump in current can be considered as the end of band gap and onset of conduction band. A similar trend of step-wise increase in current with bias voltage was observed in the IV measurements done at room temperature. The size of these steps was also equal as observed in previous device. The measured width of the steps is found to be ~42mV, which is around the same value as observed in the previous device. Figure 5-14(b) shows the zoomed in view of the IV measurement in which the step-wise increase in current more visible. In this device, there was some sharp increase in current even in the negative bias region as indicated by the

arrows in figure 5.14(a). In figure 5.14(c) the numerical differential conductance calculated using keithley method was presented and the zoomed in view of the positive bias region is shown in figure 5.14(d). The band gap of the ~7.8nm CdTe is not clearly visible in the IV plot in figure 5.14(a) due to the background current. This background current can be due to leakage from a poor quality dielectric layer or leakage from some defect states in passivation layer on the periphery of the DBTJ device. In the differential conductance plot shown in figure 5.14(c) the band gap of the device can be clearly seen. The measured band gap or the zero conduction region from the differential conductance plot was ~1.596eV. This value is in good agreement with the theoretically predicted band gap for ~7.8nm CdTe quantum dots.

The most interesting phenomenon was the occurrence of such sharp features in the IV characteristics of DBTJ devices at room temperature for ~7.8nm CdTe quantum dot device. Similar IV- characteristics and differential conductance peaks were observed for ~7nm CdSe quantum dot devices at room temperature in previous studies done by RamKumar Subramanian [5.2]. This phenomenon will be investigated in more detail in the following chapter, where simulations were done to fit the experimental data and a new model was proposed for explaining the underlying cause.

As already stated these IV characteristics at room temperature were not limited to one kind of quantum dots this was observed in DBTJ quantum dot devices fabricated using ~7nm CdSe, ~6.6nm CdSe and ~5.5nm CdSe, in addition to the ~8nm CdTe quantum dot devices for which the data was already presented.

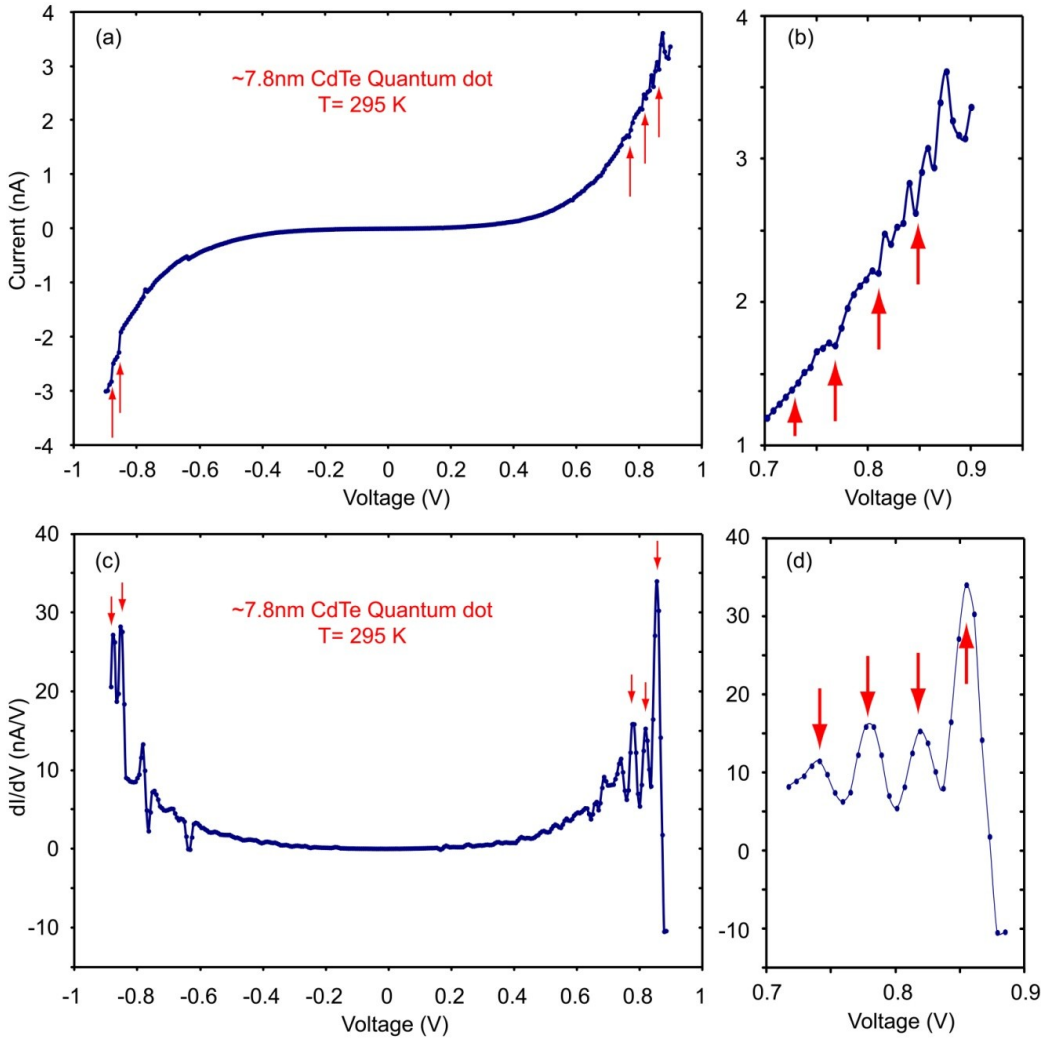


Figure 5-14 Current-Voltage plots and differential conductance plot of ~7.8nm CdTe quantum dot device, obtained using keithley numerical differentiation method- Device#2

5.4.2 DBTJ Devices with ~7nm CdSe Quantum Dots

The DBTJ devices when fabricated with a different quantum dots, the IV characteristics changed according to the band gap and energy level spacing of the quantum dots. When ~7nm CdSe quantum dots were used in fabrication of DBTJ devices, an increase in zero conduction region compared to CdTe quantum dot devices

was observed and the energy levels in the conduction band can be seen as the step-wise increase in current or the width of steps in the positive bias side of IV measurement. The band gap of bulk CdSe is 1.77eV as compared to the band gap of 1.44eV of CdTe, hence a larger zero conduction region is expected. Also, the size of the particle is smaller and hence the energy level spacing is wide enough to be resolved.

In figure 5-15(a), IV measurement done on a DBTJ device fabricated with ~7nm CdSe quantum dot at room temperature is presented. The keithley numerical differentiation method was used to obtain the dI/dV plot shown in figure 5-15(b). The current onset or the sharp increase in current starts at ~0.960eV, which was expected. For ~7nm CdSe devices since the band gap of CdSe is larger the zero conduction region is expected to be larger than the ~8nm CdTe devices. As expected, the zero conduction region in this measurement is larger and is measured to be ~2.08eV. The theoretical band gap of ~7nm CdSe quantum dots is ~1.937eV. Taking into account the voltage division factor 'η', the measured band gap of ~7nm CdSe quantum dot is within the range of expected value.

The most interesting feature of these measurements is the capability to see the sharp increase in current (~30-40meV) even at room temperature. When the differential conductance plots are observed closely, the conduction peaks are very narrow. Previous studies done on CdSe quantum dots using Scanning tunneling microscope [5.8-5.21] mostly at cryogenic temperatures, reported by other authors, shows that the peak width is much broader compared to our conductance peak width.

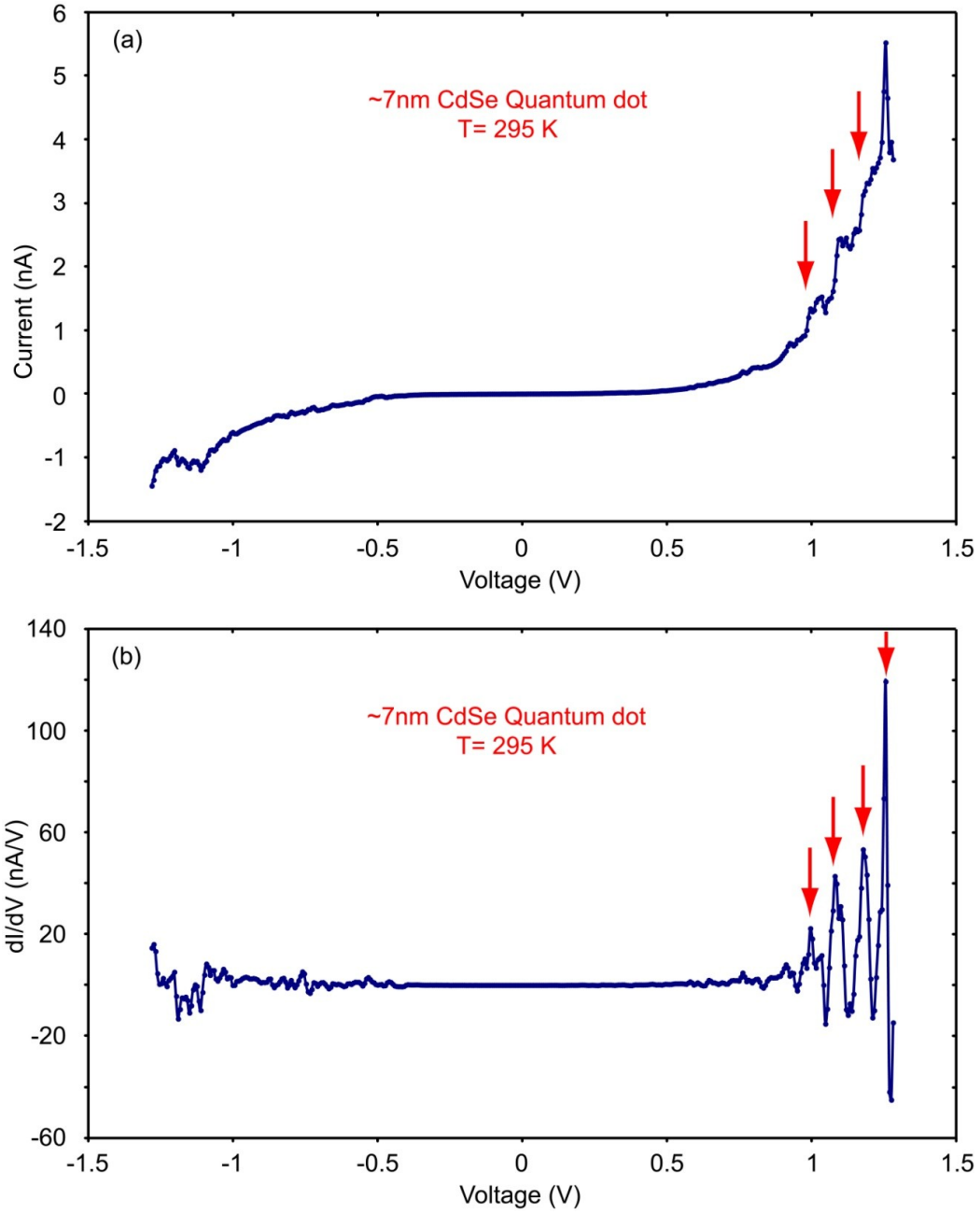


Figure 5-15 IV and dI/dV plots of ~7nm CdSe quantum dot device- Device#3

However, the same phenomenon of very sharp step wise increase of current in IV measurements at room temperature and very narrow peak widths in differential conductance measurements at different temperatures was reported by Ramkumar Subramanian [5.2] of our group. Figure 5-16 shows the IV measurement done at room temperature on ~7nm CdSe quantum dot device. The width zero conduction region in this IV measurement was found to be ~2.12eV, which is very close to the zero conduction region reported in the present study ~2.08eV. The sharp step-wise increase was seen in both the negative-bias region and the positive-bias region. On the negative bias region each jump in current represents a hole energy level in the valence band and in the positive-bias region each jump in current is represented by a electron energy level in the conduction band of quantum dot.

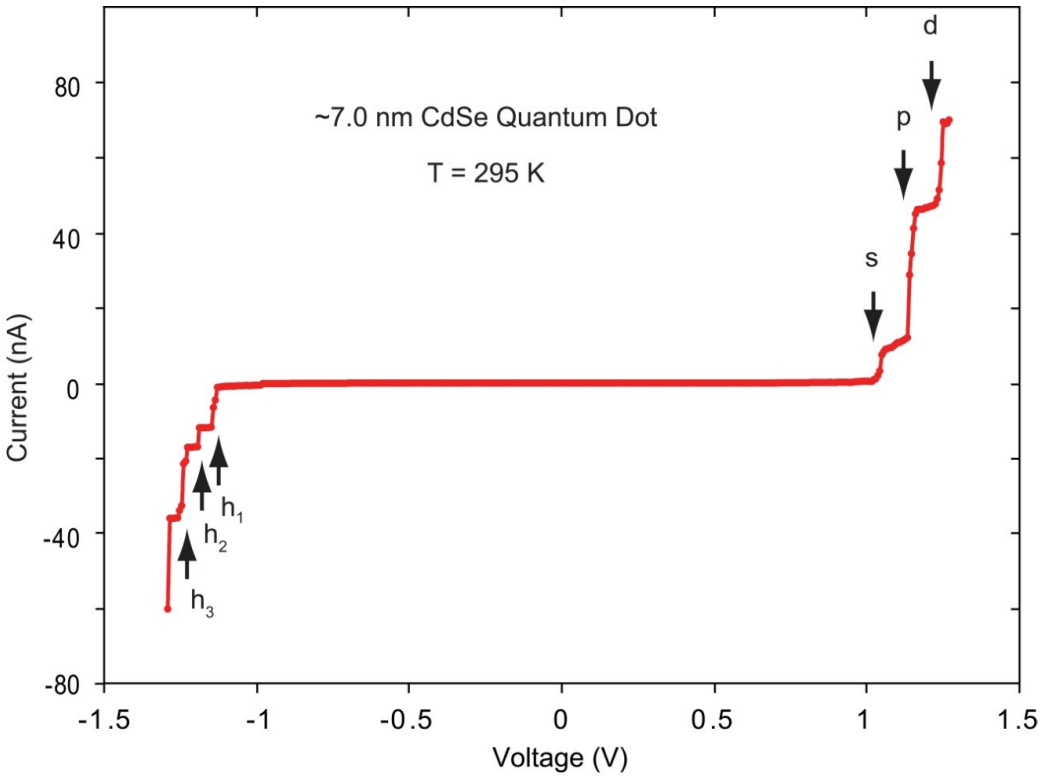


Figure 5-16 Current-Voltage measurement done on DBTJ device with ~7nm CdSe quantum dot- Device#4 [5.2]

Several devices showing similar IV characteristics at room temperature were seen and in order to further investigate the underlying phenomenon behind this observation, direct differential conductance was measured at different temperatures.

The direct differential conductance measurements were done on ~7nm CdSe quantum dot devices at ~77K, 150K, 225K and 295K. Figure 5-17 shows the direct differential conductance measurements of a DBTJ device with ~7nm CdSe quantum dot at different temperatures. As can be seen from the plot, the differential conductance peaks are very narrow and the width of the peaks changes as a function of temperature as expected. A more detailed analysis of the peak widths, their comparison with the work done by other authors and simulations to match this experimental data is presented in the following chapter. For now, this differential conductance data shows that the peak widths are temperature dependent. Also, the distance between the peaks remains the same with a small shift in the position of the peaks, which is due to the background charge fluctuations. In figure 5-17, the position of the peaks at different temperatures was readjusted to make them all aligned to the 77K data. The peak to peak separation remains the same at all the temperatures.

The differential data presented here will be used in later chapters, to match to the simulated differential conductance plots at different temperatures. A model was proposed and the current through the device was calculated using the proposed model. Then the differential conductance is obtained by numerically differentiating the current through the device. The s-peak or the first conductance peak from the above direct differential measurements was matched with the numerically calculated conductance peak using the proposed model at different temperatures. And the full width half maximums (FWHM) from the experimental data are compared with the FWHM of the numerically calculated values using the proposed model. In this chapter we are going to show some more

electrical measurement data for different sized quantum dots i.e. ~6.6nm CdSe and ~5.5nm CdSe.

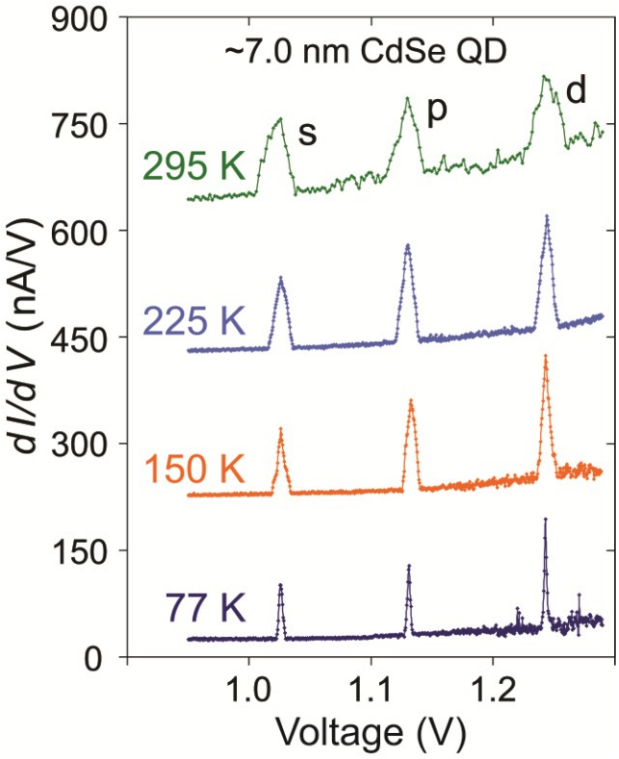


Figure 5-17 Differential conductance measurements of DBTJ device with ~7nm CdSe quantum dot at different temperatures- Device#5 [5.2]. These experiments were conducted along with Dr. Ramkumar Subramanian

5.4.3 DBTJ Devices with ~6.6nm CdSe Quantum Dots

In figure 5-18(a) the IV plot for a DBTJ device with ~6.6nm CdSe quantum dot was shown. Figure 5-18(b) shows the differential conductance plot for the same deice obtained by using keithley numerical differentiation method.

The zero conduction region DBTJ device with ~6.6nm CdSe in the above IV data is measured to be ~2.408eV, which is larger compared to the ~2.08eV and ~2.12eV

measured for the ~7nm CdSe devices. This is expected as the band gap for ~6.6nm CdSe is larger than the ~7nm CdSe. Also, clear steps in IV measurements were observed, with sharp increase in current even at room temperature. This indicates that the same phenomenon of suppression in Fermi-Dirac thermal smearing is occurring in DBTJ devices fabricated with different quantum dots.

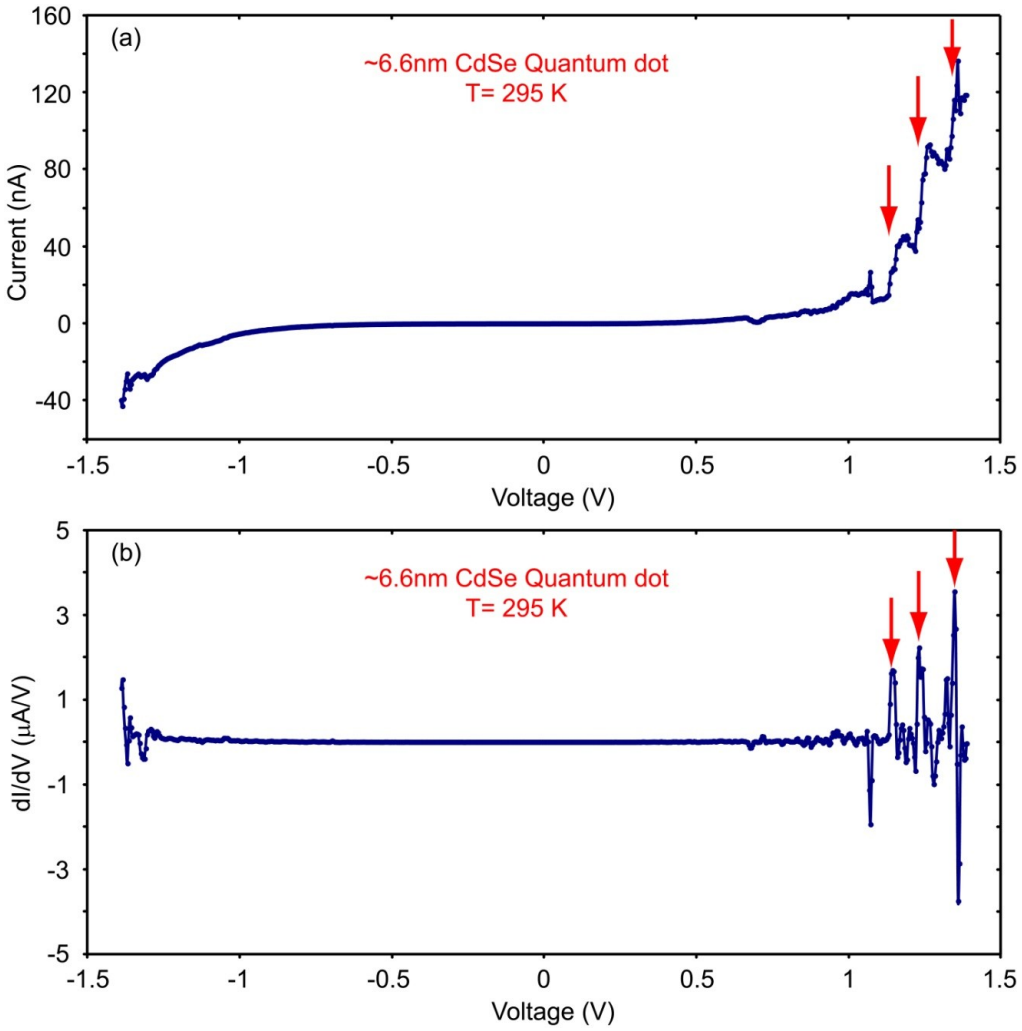


Figure 5-18 IV and differential conductance plots of DBTJ device with ~6.6nm CdSe quantum dot- Device#6

5.4.4 DBTJ Devices with ~5.5nm CdSe Quantum Dots

The same DBTJ devices were fabricated with ~5.5nm CdSe quantum dots, IV measurements and direct differential measurements were performed on these devices. These devices were fabricated along with Ramkumar Subramanian [5.2]. The data being presented here will be further used for during the numerical calculations using a new model which will be proposed in the following chapter, which explains the underlying cause for observing the sharp increase in currents at room temperature.

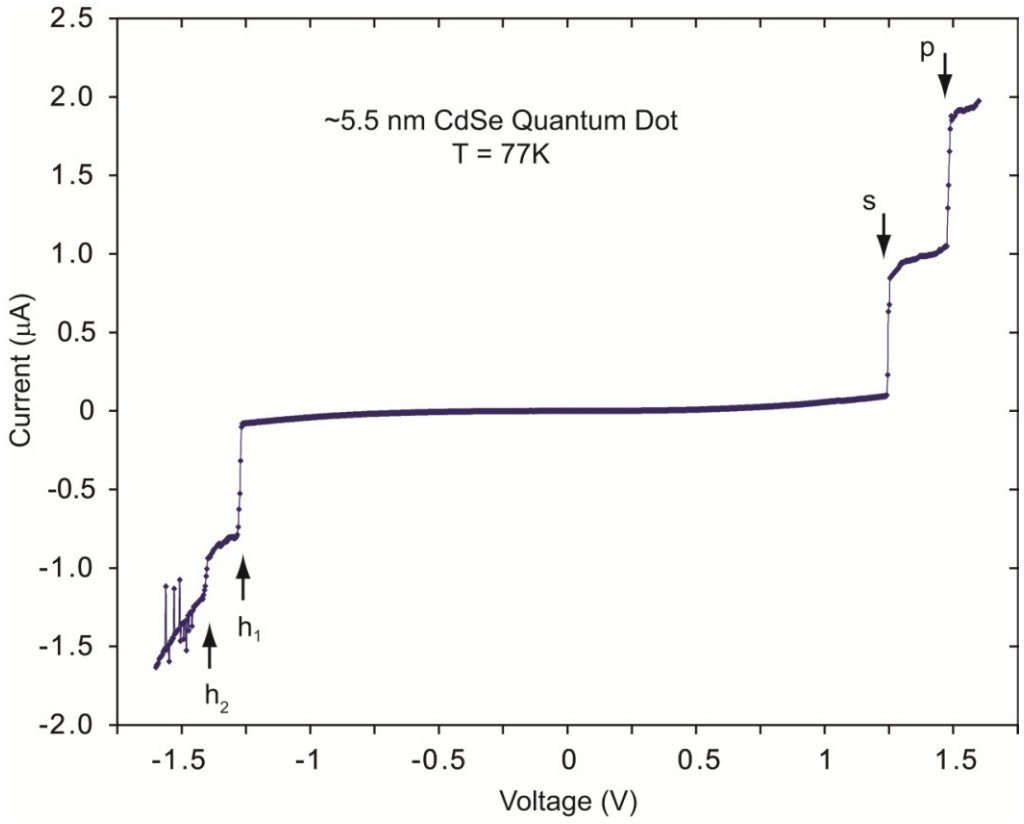


Figure 5-19 IV plot obtained from DBTJ device with ~5.5nm CdSe quantum dot at 77K-Device#7 [5.2]. These experiments were conducted along with Dr. Ramkumar Subramanian

Figure 5-19 shows the IV plot obtained from DBTJ device with ~5.5nm CdSe quantum dot at 77K. At low temperature much sharper step-wise increase in current was observed.

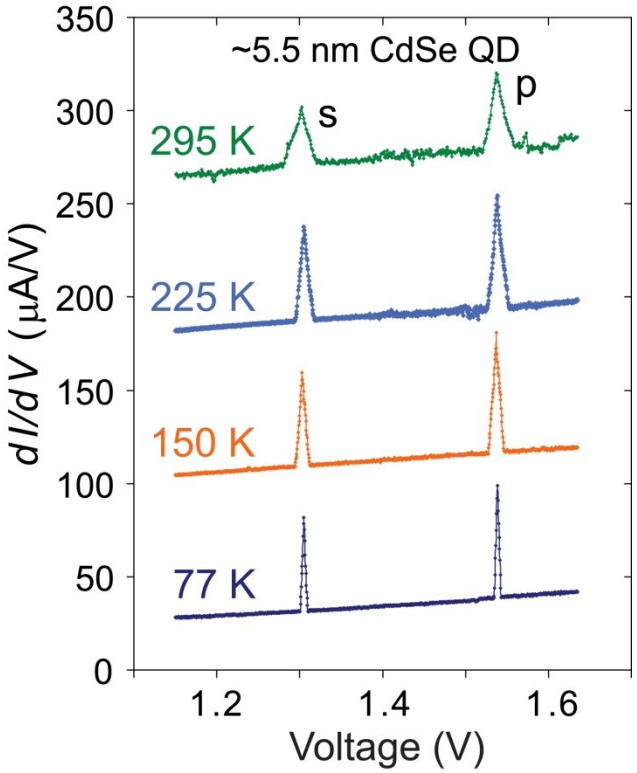


Figure 5-20 Direct differential conductance plots of DBTJ device with ~5.5nm CdSe quantum dots measured at 77K, 150K, 225K and 295K- Device#7 [5.2]. These experiments were conducted along with Dr. Ramkumar Subramanian

The zero conduction region for the ~5.5nm CdSe device is even larger compared to the ~6.6nm CdSe and ~7nm CdSe devices. This was expected as the smaller the quantum dot size, larger will be its band gap. The measured band gap of ~5.5nm CdSe device from the IV plot is ~2.548eV. Also, differential conductance measurements were

done on the same device at different temperatures. The data of direct differential conductance measurements obtained from this device using lock-in amplifier was shown in figure 5-20. As can be seen from figure 5-20 the conductance peak widths decrease with decreasing temperatures.

In the above differential conductance plot, the measurements were shifted vertically to have a comparison of peak to peak separation. Also, the measurements done at different temperatures will have a small shift in voltage (~15meV) at which the peaks appear, this is due to the background charge. This was taken care of by aligning all the data to the 77K data for clarity and easy comparison. The peak to peak separation remains the same for all the measurements done at different temperatures. This data was also used in theoretical calculations done in the following chapter to validate the proposed model which explains the sharp step wise increase in current and narrow conductance peaks seen in the DBTJ devices.

5.4.5 Comparison of Zero-Conductance Gap of CdSe DBTJ Devices

Table 5-4 Comparison of zero-conductance region of DBTJ devices

Device #	Type of Quantum dot	Optical band gap of quantum dot [5.22]	Zero-conductance gap from IV data
3	~7nm CdSe	~1.94 eV	~2.08 eV
5	~7nm CdSe	~1.94 eV	~2.16 eV
6	~6.6nm CdSe	~1.95 eV	~2.408 eV
7	~5.5nm CdSe	~2.00eV	~2.548 eV

In this section the zero-conductance gap in the electrical measurements of DBTJ devices with different sized CdSe quantum dots presented so far are compared.

With the increasing optical band gap of the quantum dots used, an increase in zero-conductance region was observed. The width of this zero-conductance region is dependent on the optical band gap of the quantum dots, electron-hole coulomb interactions and voltage division factor 'η' of the particular DBTJ device. A more detailed calculation of these terms is presented in the following chapter, where the voltage division factors of device#5 and device#7 are calculated to aid in the theoretical simulations.

Chapter 6

Simulation of Electrical Characteristics of DBTJ Devices

6.1 Introduction

In the previous chapter the electrical characterization data obtained from the DBTJ devices fabricated with different quantum dots was presented. The IV data showed very sharp step wise increase in current in the DBTJ devices even at room temperature, which is rather unusual characteristic of these devices at room temperature. Also, the differential conductance data from these devices showed very narrow conductance peaks at all the measured temperatures. In this chapter the experimental data will be compared to the experimental data from other authors for similar quantum dots using scanning tunneling microscope (STM) [6.1]. Also, a comparison of experimental data to the simulated data using existing mathematical simulator for DBTJ devices i.e. SIMON will be shown. Then a new model will be proposed and this model will be used to do the theoretical calculations of current through the DBTJ devices. Finally, the theoretical calculations will be compared with the experimental data to validate the proposed model.

6.2 Comparison of Experimental Results to SIMON Simulation and Scanning Tunneling Spectroscopy (STS) Data

The experimental results for ~7nm CdSe devices and the ~5.5nm CdSe devices were used here for comparison with numerical simulation and experimental results from other authors. Most commonly used multi-purpose single electron device simulation software SIMON (Simulation of Nano-structures) was used for carrying out these simulations at different temperatures.

6.2.1 SIMON Simulation of ~7nm CdSe Quantum Dot Device

In the previous chapter the electrical data for ~7nm CdSe quantum dot devices was shown. The data presented for device #5 will be used here, and simulation were done to check if the existing models and simulators for these devices can be explain the electrical data obtained from our devices at room.

The SIMON simulator for single electron devices was used for carrying out the simulations. Figure 6-1(a) shows the experimental data obtained at room temperature from the DBTJ device with ~7nm CdSe quantum dot. In figure 6-1(b) the simulated data for the ~7nm CdSe quantum dot device was presented. The simulations were done at three different temperatures 295K, 150K and 45K. As can be seen from the simulations, the DBTJ device does not show any sharp step-wise increase in current at 295K or the room temperature. Only when the device temperature was lowered to 45K in the simuation, the sharp step-wise increase in current was observed. However, for the fabricated DBTJ devices these features were seen in experimental IV data even at room temperature. This unusual behavior of the DBTJ devices fabricated is taken up for discussion in this chapter and a very detailed explanation of the reasons behind this will be presented in the further sections of this chapter.

From the simulations shown in figure 6-1(b), it can be seen that as the temperature increases the steps in the current-voltage plots smear out. This smearing out of steps in the current-voltage plots is due to the Fermi-Dirac thermal smearing of electrons. As the temperature increases the electron energy distribution widens and this smears out the step like features in the IV plots. From the comparison of the experimental data to the simulation using SIMON it was deduced that the fabricated DBTJ devices, when measured at room temperature are yielding us IV data which is equivalent to IV

measurement done at ~45K. Therefore, at this point it can be safely assumed that there is suppression in the Fermi-Dirac thermal smearing of electrons.

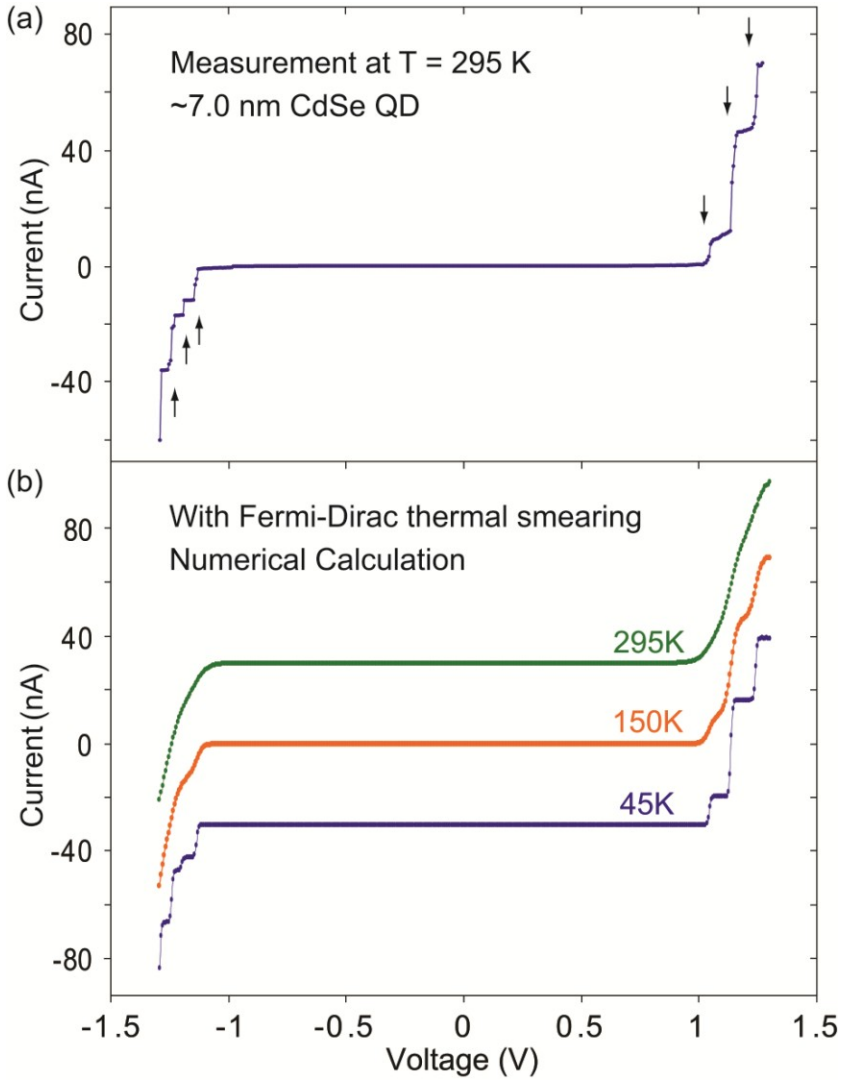


Figure 6-1 Comparison of experimental IV-data at room temperature and numerically calculated data using SIMON for DBTJ device with ~7nm CdSe quantum dot (a) Experimental data at room temperature [6.2] (b) SIMON simulations at different temperatures

6.2.2 Comparison of Differential Conductance with STS Data and Fermi-Dirac Calculations

In this section the comparison of differential conductance data at room temperature to low temperature data from other authors is done. For this purpose the differential conductance data at different temperatures for DBTJ devices with ~7nm CdSe and ~5.5nm CdSe quantum dots was used. In figure 6-2(a) and figure 6-2(b) the direct differential conductance measurements done at different temperatures for ~7nm CdSe and ~5.5nm CdSe devices was shown respectively. In figure 6-2(c) comparison of differential conductance peaks widths was shown. The plot in green is the experimental data of first differential conductance peak (s-peak) in the current study from ~5.5nm CdSe device at room temperature and the plot in red shows first differential conductance peak (s-peak) of ~5nm CdSe measured at 4.9K using scanning tunneling spectroscopy (STS). A more appropriate comparison can be made, when the full width half maximum (FWHM) peak widths of the differential conductance peaks from the current study were compared to FWHM peak widths from STS differential conductance [6.1] data at different temperatures.

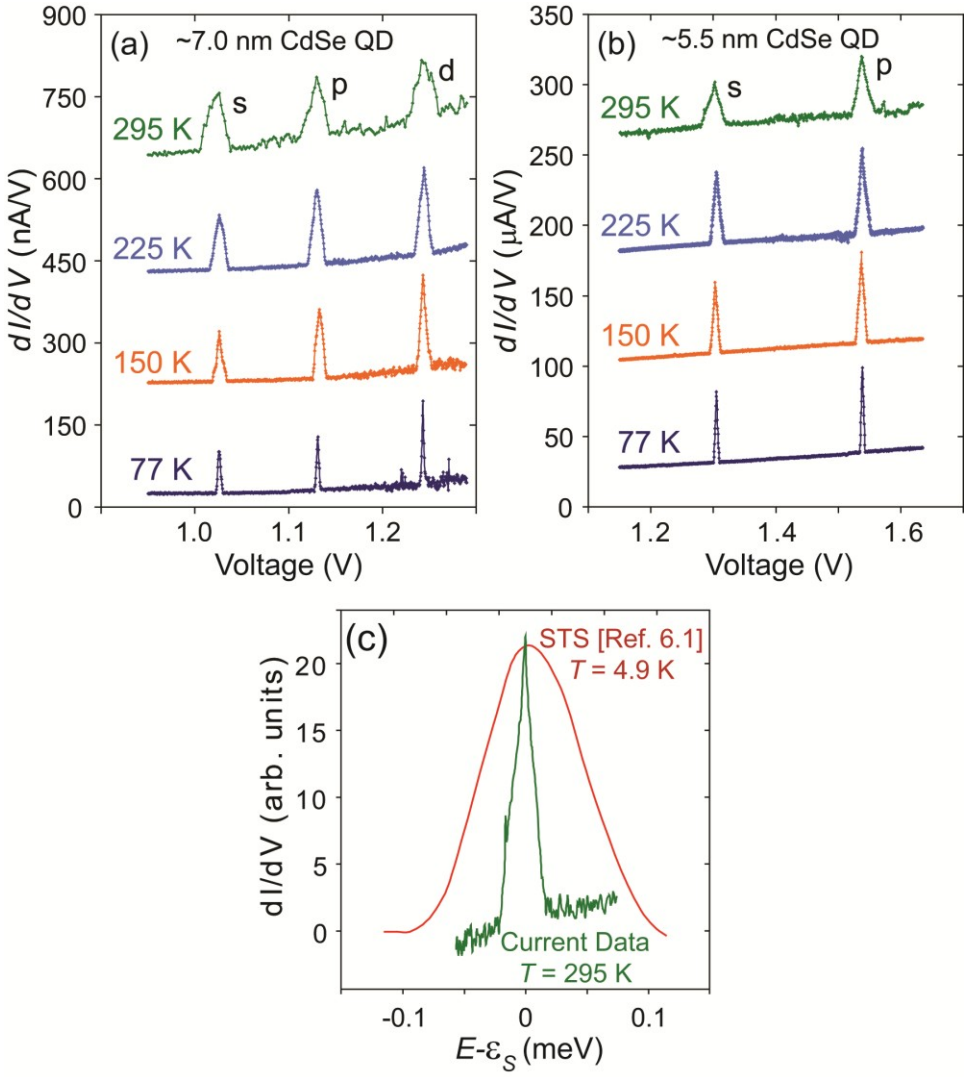


Figure 6-2 Experimental dI/dV data for ~7nm and ~5.5nm CdSe devices and comparison to STS data ~5nm CdSe [6.1] (a) dI/dV measurements done on ~7nm CdSe devices at 77K, 150K, 225K and 295K. [6.2] (b) dI/dV measurements done on ~5.5nm CdSe devices at 77K, 150K, 225K and 295K. [6.2] (c) Comparison of room temperature ~5.5nm CdSe experimental data (s-peak) to ~5nm CdSe STS data (s-peak) at 4.9K. The experiments were performed in collaboration with Dr. Ramkumar Subramanian.

6.2.2.1 Calculation of Full Width Half Maximum (FWHM) of Differential Conductance Peaks

For obtaining the FWHM peak widths of differential conductance peaks, the voltage division factor must be taken into account and the measured FWHM peak widths from the differential conductance plots must be compensated of the voltage division factor η. In a DBTJ device, the voltage bias 'V' applied across the source and drain electrodes is divided between the two tunneling junctions. The voltage division factor η is the ratio of voltage bias drop across the junction between the source electrode and the quantum dot. The calculation of voltage division factor was discussed in detail in chapter 2 of this thesis. The relationship between voltage division factor η, the zero-conductance region 'V_g^{meas}' in the from the differential conductance measurement and the optical band gap of quantum dot is given by following equation

$$\eta e V_g^{meas} = E_g^{optical} + E_{e-h} \tag{6-1}$$

where e is the elementary charge of electron, V_g^{meas} is the measured band gap or the zero conductance region from the electrical measurements and E_{e-h} is the electron-hole coulomb interaction energy,. This interaction energy E_{e-h} [6.4-6.8] can be approximately calculated by the following

$$E_{e-h} = \frac{1.79e^2}{4\pi\varepsilon_0\varepsilon_{in}R} \tag{6-2}$$

where ε_0 is the permittivity of free space, ε_{in} is the dielectric constant of the bulk material of the QD. From the above equations (6-1) and (6-2) η can be given as

$$\eta = \left[E_g^{optical} + \frac{1.79e^2}{4\pi\varepsilon_0\varepsilon_{in}R} \right] \Big/ eV_g^{meas} \qquad (6\text{-}3)$$

Using the above equation (6-3) and the optical band gap data, voltage division factor η is calculated for the DBTJ devices shown in figure 6-2(a) and figure 6-2(b). The main assumption in the calculation of voltage division factor η is that the size of the quantum dot whose energy levels are being studied is same as the nominal size of the quantum dots. The optical bandgap $E_g^{optical}$ was obtained using nominal CdSe QD sizes [6.9]. The FWHM calculations for ~7nm and ~5.5nm CdSe DBTJ devices are summarized in Table 6-1 below

Table 6-1 Voltage division factor η for the DBTJ devices in Figure 6-2(a) and 6-2(b)

DBTJ device #	CdSe QD Dia. (nm)	$E_g^{optical}$ (eV) [6.9]	E_{e-h} (eV)	V_g^{meas} (V)	η
#5 Fig. 6-2(a)	~7.0	1.937	0.092	2.169	0.94
#7 Fig. 6-2(b)	~5.5	2.000	0.117	2.548	0.83

Table 6-2 and Table 6-3 summarize the FWHMs of the measured differential conductance peaks in Figure 6-2(a) and 6-2(b), respectively. FWHMs at different temperatures for differential conductance peaks were measured in (mV). The 'η' values obtained from Table 6-1 were used to obtain the FWHMs in energy scale (meV) after voltage division factor compensation.

Table 6-2 FWHMs of the differential conductance peaks for the DBTJ device with ~7nm CdSe quantum dot in figure 6-2(a)

	s-peak		p-peak		d-peak	
Temperature	FWHM (mV)	FWHM (meV)	FWHM (mV)	FWHM (meV)	FWHM (mV)	FWHM (meV)
77 K	3.8	3.6	3.5	3.3	2.4	2.3
150 K	6.9	6.5	7.6	7.1	7.0	6.6
225 K	10.4	9.7	9.3	8.7	9.7	9.1
295 K	16.1	15.1	15.6	14.7	17.7	16.6

Table 6-3 FWHMs of the differential conductance peaks for the DBTJ device with ~5.5nm CdSe quantum dot in figure 6-2(b)

	s-peak		p-peak	
Temperature	FWHM (mV)	FWHM (meV)	FWHM (mV)	FWHM (meV)
77 K	4.3	3.6	4.3	3.6
150 K	8.4	7.0	9.4	7.8
225 K	10.7	8.9	12.2	10.2
295 K	18.9	15.7	16.9	14.0

Figure 6-3 shows the FWHMs (in energy unit) as a function of temperature. The FWHMs at each temperature have very small deviations at a given temperature. The FWHM values at the same temperature are very close to each other without regard to quantum dot levels (s, p or d) or the samples measured (DBTJ device with 7.0 nm CdSe quantum dot or with 5.5 nm CdSe quantum dot).

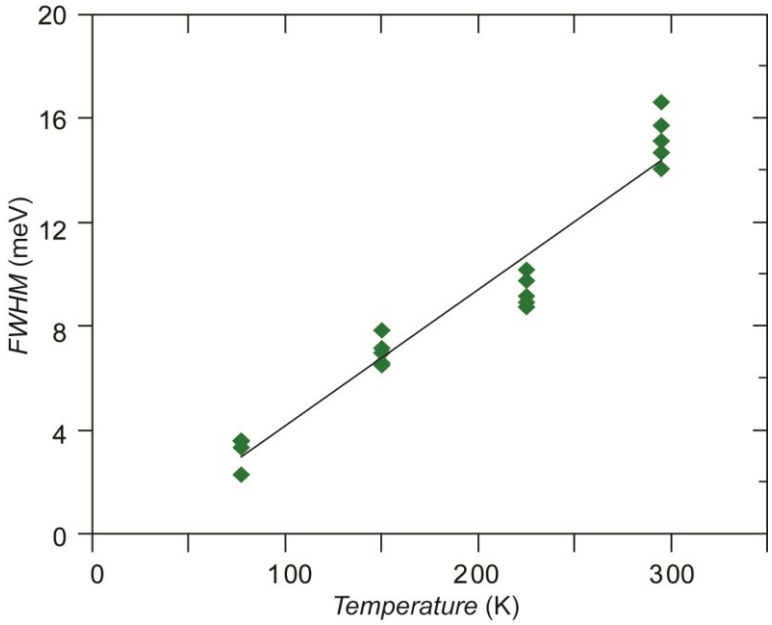


Figure 6-3 Linear relationship between temperature and the FWHMs of the differential conductance peaks

6.2.2.2 Comparison of Experimental Differential Conductance FWHM Peak Widths with STS and Fermi-Dirac FWHM Peak Widths

These FWHM peak widths obtained from the experimental data are compared to the Fermi-Dirac thermal smearing FWHM peak widths and STS data [6.1] at different temperatures. This gives an idea of the extent of suppression in Fermi-Dirac thermal smearing in the DBTJ devices under study.

In figure 6-4 a comparison of peak widths as a function of temperature was shown. The plot in green represents the conductance FWHM peak widths at different temperatures from the current study, the plot in blue represents the numerically calculated FWHM peak widths using Fermi-Dirac distribution and the plot in red is FWHM peak widths obtained from the STS measurements of ~5nm CdSe quantum dots [6.1]. From this plot it can be observed that the slope of STS data and the slope of numerically

calculated FWHM using Fermi-Dirac distribution are same, where the slope of the FWHM peak widths plot from current study is different. This is another strong indication that there is suppression in Fermi-Dirac thermal smearing in the DBTJ devices fabricated for this study and they don't follow the Fermi-Dirac thermal distribution of electron. The unusual slope of this plot arises from the phonon-emission, phonon-absorption and relaxation, as will be discussed in detail, in further sections of this chapter.

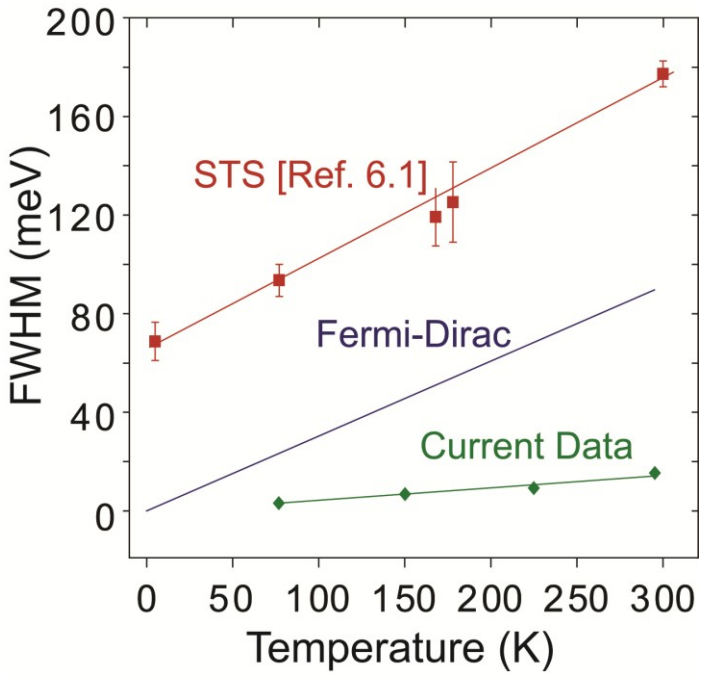


Figure 6-4 Comparison of FWHM peak widths of differential conductance peaks of current study (green), Fermi-Dirac distribution (blue) and STS [6.1] (red)

6.3 Electron Energy Filtering - Simulation Model

The existing model for simulating the current through the DBTJ devices does not explain the experimental data of DBTJ devices. A simulation model proposed in the

paper titled “Energy-Filtered Cold Electron Transport at Room Temperature” (P. Bhadrachalam, R. Subramanian, V. Ray, L.-C. Ma, W. Wang, J. Kim, K. Cho and S.J. Koh) was used for completing the numerical calculations. The following sections, from section 6.3.1 to section 6.3.4 consists of the work presented in the above mentioned paper.

6.3.1 Theory of Electron Energy Filtering

In figure 6-5 a comparison the existing model of tunnel junctions and the idea of new model is shown. In figure 6-5(a), shows the energy diagram, when there a quantum dot with one single energy level in between two metal electrodes. When a voltage bias is swept across the two electrodes, the current-voltage plot will look like the plot shown at the bottom of figure 6-5(a). When the bias is applied the Fermi level of the drain electrode starts moving down with increasing voltage bias and the quantum dot energy level also moves down with the drain electrode assuming that the drain electrode and quantum dot are capacitively coupled to each other. Once the quantum dot energy level comes to the proximity of the Fermi level of source electrode, the electrons start tunneling from the source electrode to the quantum dot. At room temperature this electron tunneling starts even before the quantum dot energy level aligns with the source Fermi energy level; this happens because of the thermally excited electrons which can occupy higher energy states due the Fermi-Dirac distribution of electron which can tunnel to the quantum dot. The Fermi-Dirac thermal smearing is schematically represented by lightly shaded region near the electrode Fermi level in figure 6-2.

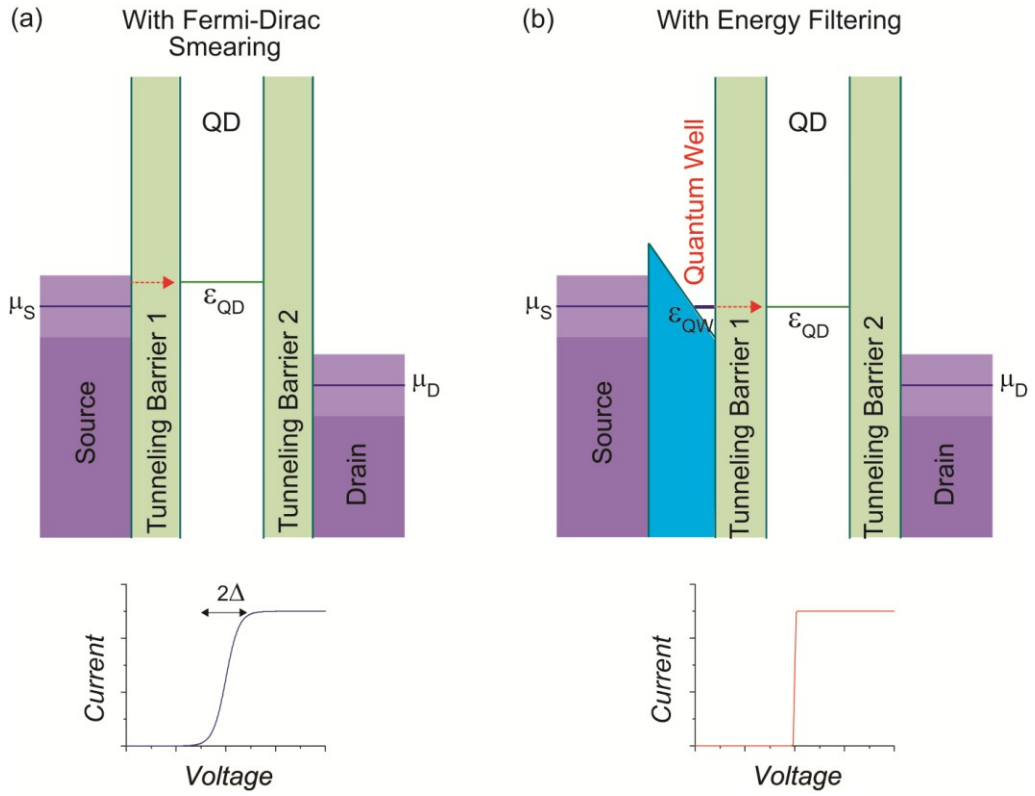


Figure 6-5 Energy diagrams showing two different scenarios and two different IV characteristics (a) with Fermi-Dirac thermal smearing and (b) with energy filtering

In the same structure, if a quantum well is introduced in between the source and the quantum dot, there will be an electron cooling effect or energy filtering effect. When voltage bias is swept across the electrodes, the drain electrode Fermi energy level will move down in the similar fashion as above. But the electrons from the source electrode tunnel into the quantum well before they tunnel into the quantum dot, and when the quantum dot energy level aligns with the quantum well energy level, then electrons tunnel into quantum dot. Since the quantum well has discrete energy states, there will not be any thermal smearing of electrons in the quantum well. The presence of quantum well causes an energy filtering effect; in this case the current increase will be very sharp and

abrupt. So even at room temperature there should be very sharp increase in current as the electron in the quantum well cannot gain any thermal energy and move to higher energy states, since there are no available energy states. The expected IV plot for the device structure with the quantum well in between source and quantum dot is shown in figure 6-5(b) below. This explains the origin of very abrupt current jumps in the IV data shown in chapter 5 for DBTJ devices at room temperature. However, the differential conductance measurements done at different temperatures have shown dependence on the measurement temperature, which can be explained using phonon absorption, phonon emission and relaxation. This explanation was provided in detail in further sections of this chapter.

6.3.2 Quantum Well Formation in DBTJ Devices

A closer look at our DBTJ device structure reveals that the choice of materials used for fabrication of the device inherently favors the formation of quantum well. Chromium is the metal used for electrodes; it is well known that chromium forms a native oxide. The dielectric material forming the tunneling junctions is silicon dioxide. In figure 6-6 the details of the materials used for fabrication of DBTJ devices is shown and the energy diagram of the tunnel junction is also shown.

The chromium metal used for electrodes forms a native oxide the chrome-oxide conduction band edge is ~0.1eV higher than the Fermi-level of chromium metal. Silicon-dioxide is also present in the tunnel junction region, this is the passivation layer used for covering the devices after the attachment of quantum dots, a zoomed in view of schematic was shown in figure 6-6 (a). Figure 6-6(b) shows the energy landscape of chromium, chrome-oxide and silicon-dioxide, where E_F is the Fermi level of chromium, E_C and E_V represent conduction band and valence bands of respective materials. When

these materials are put together, there will be band-bending in the conduction band edge of chrome-oxide. This band-bending originates from the surface charges trapped at the interface of chrome-oxide and silicon-dioxide layers or from the difference in oxygen areal density in the two materials in contact [6.9]. This band-bending in the conduction band edge of chrome-oxide leads to the formation of a quantum well as shown in figure 6-3(c). The Fermi-Dirac thermal smearing is schematically shown by the lightly shaded region near the electrode Fermi level. These thermal excited electrons are filtered by the discrete energy levels in the quantum well indicated by dotted circle in figure 6-3(c). This explains the sharp step-wise increase in current in the fabricated DBTJ devices even at room temperature. With this energy-filtering as main concept, a model is constructed to facilitate numerical calculation of current through the DBTJ devices.

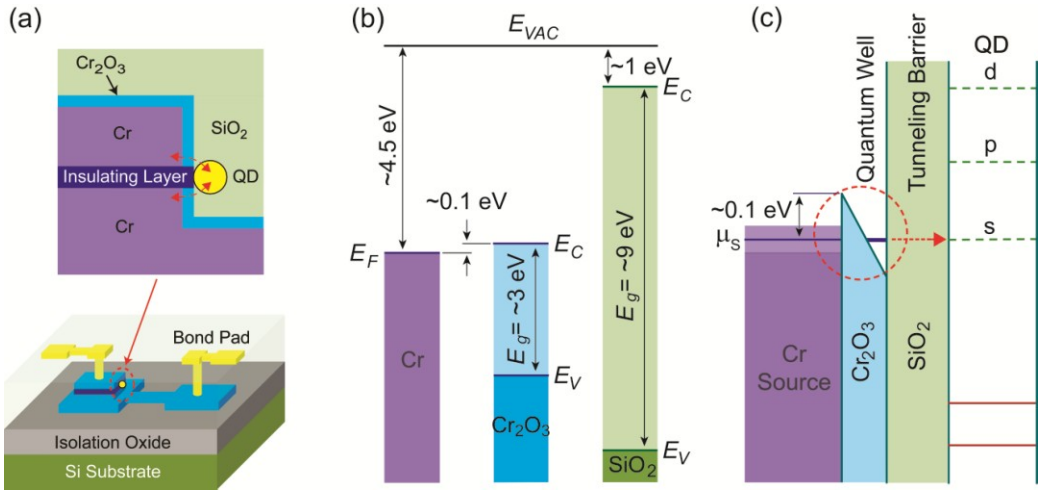


Figure 6-6 Formation of quantum well (a) Schematics showing zoomed in view of tunneling junction region (b) Energy landscape of different materials in tunnel junction region and (c) Energy diagram showing the formation of quantum well in chrome-oxide

6.3.3 Simulation Model for Electron energy Filtering

Figure 6-7 shows the model system constructed for carrying out the numerical calculation of current through the DBTJ devices in current study. The system is made of the following components, a source (S), a quantum well (QW), a quantum dot (QD) and a drain (D), with tunneling barriers separating them. For simplicity only one energy level is considered in the quantum dot. The chemical potential of the source, quantum well, quantum dot and the drain electrodes are represented by μ_S, ε_{QW}, ε_{QD} and μ_D respectively.

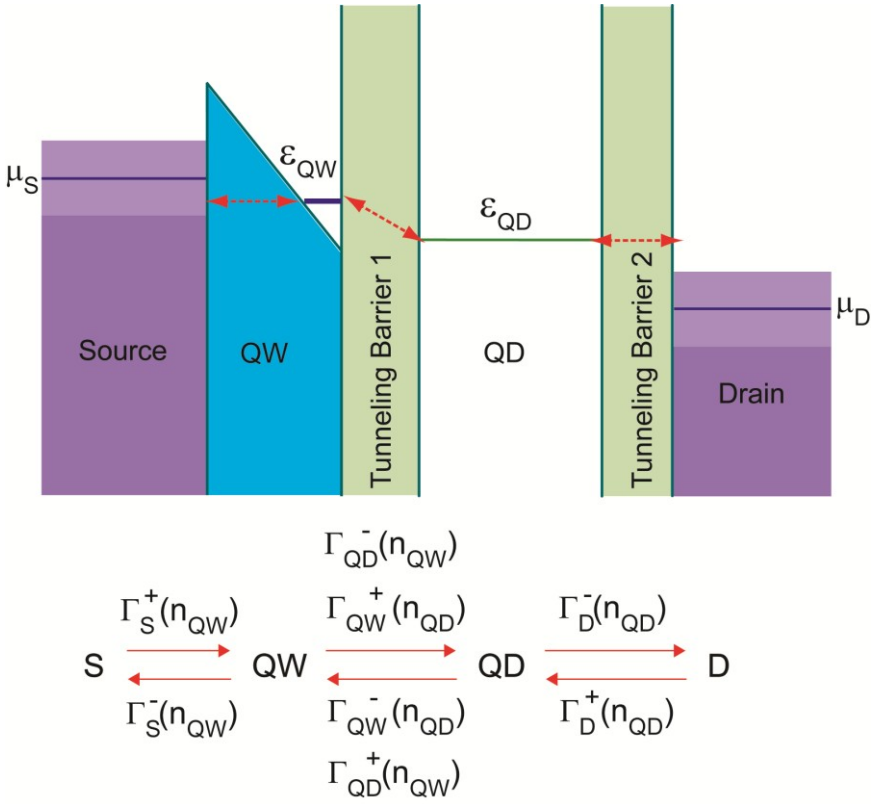


Figure 6-7 Model system used for numerical calculations

When positive voltage bias is applied the electrons start tunneling from the source to the quantum well to the quantum dot and finally to the drain. To calculate the current through the device first we have to calculate the tunneling rates between the adjacent components of the system. The tunneling rates between the adjacent components of the model are represented as follows

- Tunneling rates between source and quantum well: $\Gamma_S^{\pm}\left(n_{QW}\right)$ is the tunneling rate between the source (S) and the quantum well (QW). 'n_{QW}' represents the number of electron in quantum QW before tunneling and the superscript '+' and '-' represents the addition of electron to the QW and removal of electron from the QW respectively.
- Tunneling rates between quantum well and quantum dot: $\Gamma_{QW}^{\pm}\left(n_{QD}\right)$and $\Gamma_{QD}^{\pm}\left(n_{QW}\right)$ are the tunneling rates between the QW and the QD. $\Gamma_{QW}^{\pm}\left(n_{QD}\right)$ represent rate of electrons tunneling between QW and QD. n_{QD}, represents the number of electron in quantum QD before tunneling and the superscript '+' and '-' represent the addition of electron to the QD and removal of electron from the QD respectively. Similarly, $\Gamma_{QD}^{\pm}\left(n_{QW}\right)$ represents rate of electrons tunneling between QD and QW. n_{QW}, represents the number of electron in quantum QW before tunneling and the superscript '+' and '-' represent the addition of electron to the QW and removal of electron from the QW respectively.
- Tunneling rates between the quantum dot and drain: $\Gamma_D^{\pm}\left(n_{QD}\right)$ represents rate of electrons tunneling from QW to QD. n_{QD}, represents the number of

electron in quantum QD before tunneling and the superscript '+' and '-' represent the addition of electron to the QD and removal of electron from the QD respectively.

The tunneling events between the source (S) and quantum well (QW) and between the quantum dot (QD) and drain (D) are considered to be purely elastic. The electron tunneling between the QW and the QD comprises of elastic tunneling component and inelastic tunneling component. During inelastic tunneling process the electron gains or losses energy while tunneling as shown in Figure 6-8(a) and 6-8(b). This gain or loss of energy of electron is compensated by phonon absorption, phonon emission and relaxation processes. In order to get these tunneling rates we have to calculate the tunneling probabilities which in turn are dependent on the probability of phonon absorption, emission and relaxation. So, we have to calculate these probabilities of phonon absorption, emission and relaxation rates in order to get the final tunneling rates between the adjacent components of the model. These tunneling probabilities are a function of energy ε. In the following sections the elastic tunneling probability and inelastic tunneling probabilities are defined and the functional forms that can be used for calculating the tunneling probabilities are shown.

6.3.3.1 Elastic Tunneling Probability

The elastic tunneling probability $\gamma_{elastic}(\varepsilon)$, is assumed to take the form of Lorentzian distribution and is given by

$$\gamma_{elastic}(\varepsilon)=\frac{2}{\hbar}\left(\frac{\hbar T_{elastic}}{2}\right)^{2}\frac{\frac{\hbar T_{elastic}}{2}}{\varepsilon^{2}+\left(\frac{\hbar T_{elastic}}{2}\right)^{2}} \tag{6-4}$$

where ħ is the reduced Planck constant and $T_{elastic}$ is the elastic tunneling probability when the QW energy level and QD energy level align exactly

6.3.3.3 Inelastic Tunneling Probability - Electron Gains Energy

The gain of the energy of electron during tunneling shown in figure 6-8(a), happens through phonon absorption process. The tunneling probability of the inelastic tunneling through phonon absorption represented by $\gamma_{absorption}(\varepsilon,T)$ is given by

$$\gamma_{absorption}(\varepsilon,T)=n(|\varepsilon|,T)A(\varepsilon) \tag{6-5}$$

where ε <0 (for the energy gain), $n(|\varepsilon|,T)$ is the Bose-Einstein distribution function of phonon population, $n(\varepsilon>0,T)=1\Big/\left(e^{\varepsilon/kT}-1\right)$, where T is the absolute temperature and k is the Boltzmann constant and $A(\varepsilon)$is the Einstein A coefficient for spontaneous emission of phonons [6.10-6.11].

Since the total tunneling probability in this case consists of both inelastic and elastic tunneling of electrons, the elastic part of electron tunneling has also to be considered. The total tunneling probability $\gamma(\varepsilon<0,T)$ is then given by

$$\gamma(\varepsilon<0,T)=\gamma_{absorption}(\varepsilon,T)+\gamma_{elastic}(\varepsilon) \tag{6-6}$$

$$\gamma(\varepsilon<0,T)=n(|\varepsilon|,T)A(|\varepsilon|)+\frac{2}{\hbar}\left(\frac{\hbar T_{elastic}}{2}\right)^2\frac{\frac{\hbar T_{elastic}}{2}}{\varepsilon^2+\left(\frac{\hbar T_{elastic}}{2}\right)^2} \quad (6\text{-}7)$$

$$\gamma(\varepsilon<0,T)=1\Big/\left(e^{|\varepsilon|/kT}-1\right)A(|\varepsilon|)+\frac{2}{\hbar}\left(\frac{\hbar T_{elastic}}{2}\right)^2\frac{\frac{\hbar T_{elastic}}{2}}{\varepsilon^2+\left(\frac{\hbar T_{elastic}}{2}\right)^2} \quad (6\text{-}8)$$

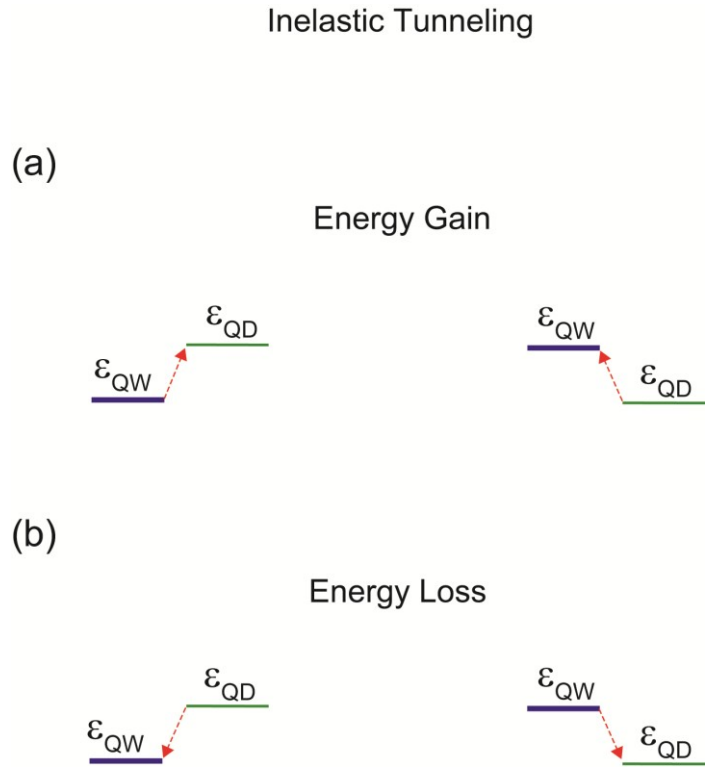


Figure 6-8 Schematically representing Inelastic electron tunneling (a) Electron gains energy (b) electron losses energy.

6.3.3.3 Inelastic Tunneling Probability - Electron Loses Energy

Inelastic electron transport in which electron loses the energy as shown in figure 6-8(b) can occur through a phonon emission and other energy relaxation processes (e.g., interface-roughness scattering, impurity scattering, etc.), which are represented by $\gamma_{emission}(\varepsilon,T)$ and $\gamma_{relaxation}(\varepsilon,T)$, respectively. The tunneling probability through phonon emission $\gamma_{emission}(\varepsilon,T)$ is given by [6.10-6.11]

$$\gamma_{emission}(\varepsilon,T)=\left[n(\varepsilon,T)+1\right]A(\varepsilon) \tag{6-9}$$

$$\gamma_{emission}(\varepsilon,T)=\left[1\Big/\left(e^{\varepsilon/kT}-1\right)+1\right]A(\varepsilon) \tag{6-10}$$

The total tunneling probability with which an electron loses the energy in the tunneling $\gamma(\varepsilon>0,T)$ is then given by

$$\gamma(\varepsilon>0,T)=\gamma_{emission}(\varepsilon,T)+\gamma_{relaxation}(\varepsilon)+\gamma_{elastic}(\varepsilon) \tag{6-11}$$

$$\gamma(\varepsilon>0,T)=\left[1\Big/\left(e^{\varepsilon/kT}-1\right)+1\right]A(\varepsilon)+\gamma_{relaxation}(\varepsilon)+\frac{2}{\hbar}\left(\frac{\hbar T_{elastic}}{2}\right)^2\frac{\frac{\hbar T_{elastic}}{2}}{\varepsilon^2+\left(\frac{\hbar T_{elastic}}{2}\right)^2} \tag{6-12}$$

6.3.3.4 Functional Forms Used for Spontaneous Emission of Phonons, Relaxation Rate and Elastic Tunneling

In order to calculate the tunneling probabilities from above equations functional forms were assumed for $A(\varepsilon)$, $\gamma_{relaxation}(\varepsilon)$ and $\gamma_{elastic}(\varepsilon)$. $A(\varepsilon)$ which represents the Einstein A coefficient of spontaneous emission of phonons and the functional form of $A(\varepsilon)$ shown in figure 6-9(a), will be zero at zero energy it will reach a maximum and then decreases to zero after certain energy value which is the cut-off energy [6.10-6.12]. The cut-off energy or the effective debye cutoff energy is assumed to be 20meV. The tunneling probability through relaxation $\gamma_{relaxation}(\varepsilon)$ assumes a functional form as shown in figure 6-8(b) with relaxations rate of the order of ~10^{12} [1/sec]. This relaxation rate constitutes of all the relaxation paths which comprises of interface roughness scattering, impurity scattering and defect-assisted relaxation [6.13-6.14]. The value of relaxation rate is assumed based on the theoretical and experimental studies which claim that it can be of the order of ~10^{12} [1/sec] or greater [6.13-6.15]. For elastic tunneling probability $\gamma_{elastic}(\varepsilon)$ the functional form assumed is Lorentzian distribution [6.12, 6.16] as shown in figure 6-9(c).

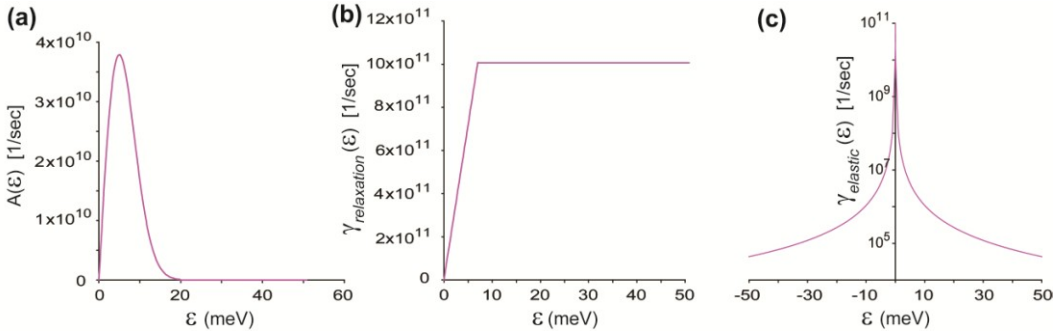


Figure 6-9 The functional forms assumed for carrying out the tunneling probability calculations (a) $A(\varepsilon)$ (b) $\gamma_{relaxation}(\varepsilon)$ (c) $\gamma_{elastic}(\varepsilon)$

6.3.3.5 Tunneling Rate Equations

Since we have the tunneling probability equations we can deduce tunneling rate equations between adjacent components of the model. For doing this we need to consider the probabilities of occupancy of the QW and QD. Let probability that the QW is occupied by n_{QW} number of electrons is represented by $P_{QW}\left(n_{QW}\right)$. It is assumed that n_{QW} can be either 0, 1 or 2 that is the QW can either have one electron or two electrons or no electrons in it. Likewise, $P_{QD}\left(n_{QD}\right)$ is the probability that n_{QD} number of electrons that occupy the QD level. It is assumed that n_{QD} can be either 0 or 1 that is the QD can either have one extra electron on it or no extra electrons. The tunneling rates $\Gamma_S^{\pm}\left(n_{QW}\right)$, $\Gamma_D^{\pm}\left(n_{QD}\right)$, $\Gamma_{QW}^{\pm}\left(n_{QD}\right)$ and $\Gamma_{QD}^{\pm}\left(n_{QW}\right)$ can now be given by the product of the tunneling probabilities and the occupation probabilities. Hence we can write the following relations

- The tunneling rate equations between the source (S) and quantum well (QW)

$$\Gamma_S^{+}(0) = f_S\left(\varepsilon_{QW}\right) \times D_S\left(\varepsilon_{QW}\right) \times T_S \tag{6-13}$$

$$\Gamma_S^{+}(1) = f_S\left(\varepsilon_{QW}\right) \times D_S\left(\varepsilon_{QW}\right) \times T_S \tag{6-14}$$

$$\Gamma_S^{-}(1) = \left[1 - f_S\left(\varepsilon_{QW}\right)\right] \times D_S\left(\varepsilon_{QW}\right) \times T_S \tag{6-15}$$

$$\Gamma_S^{-}(2) = \left[1 - f_S\left(\varepsilon_{QW}\right)\right] \times D_S\left(\varepsilon_{QW}\right) \times T_S \tag{6-16}$$

where $f_S(E)$ is the Fermi-Dirac distribution function of the source (S) electrode with chemical potential μ_S, ε_{QW} is the energy of the quantum well energy state, T_S is the tunneling probability of electrons tunneling from source (S) to quantum

well (QW) and $D_S(E)$ represents the density of states for the source (S) electrode.

- The tunneling rate equations between the quantum well (QW) and quantum dot (QD). These tunneling rate equations will constitute of both elastic and inelastic tunneling.

$$\Gamma_{QD}^{+}(0) = \gamma(\varepsilon_{QD} - \varepsilon_{QW}, T) \times P_{QD}(1) \tag{6-17}$$

$$\Gamma_{QD}^{+}(1) = \gamma(\varepsilon_{QD} - \varepsilon_{QW}, T) \times P_{QD}(1) \tag{6-18}$$

$$\Gamma_{QD}^{-}(1) = \gamma(\varepsilon_{QW} - \varepsilon_{QD}, T) \times P_{QD}(0) \tag{6-19}$$

$$\Gamma_{QD}^{-}(2) = \gamma(\varepsilon_{QW} - \varepsilon_{QD}, T) \times P_{QD}(0) \tag{6-20}$$

$$\Gamma_{QW}^{+}(0) = \gamma(\varepsilon_{QW} - \varepsilon_{QD}, T) \times [P_{QW}(1) + P_{QW}(2)] \tag{6-21}$$

$$\Gamma_{QW}^{-}(1) = \gamma(\varepsilon_{QD} - \varepsilon_{QW}, T) \times [P_{QW}(0) + P_{QW}(1)] \tag{6-22}$$

where $\gamma(\varepsilon, T)$ is the tunneling probability between the quantum well (QW) and quantum dot (QD) which is determined by ε_{QW} and ε_{QD}, the energies of the QW and QD energy states respectively.

- The tunneling rate equations between the drain (D) and quantum dot (QD)

$$\Gamma_{D}^{+}(0) = f_D(\varepsilon_{QD}) \times D_D(\varepsilon_{QD}) \times T_D \tag{6-23}$$

$$\Gamma_{D}^{-}(1) = [1 - f_D(\varepsilon_{QD})] \times D_D(\varepsilon_{QD}) \times T_D \tag{6-24}$$

where $f_D(E)$ is the Fermi-Dirac distribution function of the drain (D) electrode with chemical potential μ_D, ε_{QD} is the energy of the quantum well energy state,

T_D is the tunneling probability of electrons tunneling from quantum well (QW) to the drain (D) electrode and $D_D(E)$ represents the density of states for the drain (D) electrode.

From the above sets of equations (6-13) to (6-24) the tunneling rates $\Gamma_S^{\pm}(n_{QW})$, $\Gamma_D^{\pm}(n_{QD})$, $\Gamma_{QW}^{\pm}(n_{QD})$ and $\Gamma_{QD}^{\pm}(n_{QW})$ can be determined by knowing the position of μ_S, ε_{QW}, ε_{QD} and μ_D which are determined by the voltage bias V applied between the source and the drain electrodes. If η is the voltage division factor of the device, then the relationship between the values of μ_S, ε_{QW}, ε_{QD}, μ_D and V are as follows

$$\begin{aligned} \mu_S - \mu_D &= eV \\ \Delta(\varepsilon_{QW} - \varepsilon_{QD}) &= \eta eV \\ \Delta(\varepsilon_{QD} - \mu_D) &= (1-\eta)eV \end{aligned} \tag{6-25}$$

6.3.3.6 Master Equations and Numerical Current-Voltage Calculations

Now the steady state transitions rates between adjacent configurations are considered. At steady state, the transition rates between two adjacent configurations are the same. When the quantum well (QW) has zero electrons the transition rate of electrons tunneling into the QW is same as the transition rate of electrons tunneling out of the QW when it has one electron in it. This can be written in equation form as below

$$P_{QW}(0)\times\left[\Gamma_S^{+}(0)+\Gamma_{QD}^{+}(0)\right] = P_{QW}(1)\times\left[\Gamma_S^{-}(1)+\Gamma_{QD}^{-}(1)\right] \tag{6-26}$$

Similarly, when the quantum well (QW) has one electron the transition rate of electrons tunneling into the QW is same as the transition rate of electrons tunneling out of the QW when it has two electrons in it. This can be written in equation form as below

$$P_{QW}(1)\times\left[\Gamma_S^+(1)+\Gamma_{QD}^+(1)\right]=P_{QW}(2)\times\left[\Gamma_S^-(2)+\Gamma_{QD}^-(2)\right] \tag{6-27}$$

If we consider transition rates for two QD configurations, when the quantum dot (QD) has zero electrons the transition rate of electrons tunneling into the QD is same as the transition rate of electrons tunneling out of the QD when it has one electron in it. This can be written in equation form as below

$$P_{QD}(0)\times\left[\Gamma_{QW}^+(0)+\Gamma_D^+(0)\right]=P_{QD}(1)\times\left[\Gamma_{QW}^-(1)+\Gamma_D^-(1)\right] \tag{6-28}$$

The sum of occupation probabilities of the QW and QD must be unity. This can be written as below

$$P_{QW}(0)+P_{QW}(1)+P_{QW}(2)=1 \tag{6-29}$$

$$P_{QD}(0)+P_{QD}(1)+=1 \tag{6-30}$$

By solving above five equations for given set of tunneling rates $\Gamma_S^{\pm}(n_{QW})$, $\Gamma_D^{\pm}(n_{QD})$, $\Gamma_{QW}^{\pm}(n_{QD})$and $\Gamma_{QD}^{\pm}(n_{QW})$ for a specific voltage V, the probabilities of occupation of the QW and QD can be obtained. After obtaining the values of $P_{QW}(0)$, $P_{QW}(1)$, $P_{QW}(2)$, $P_{QD}(0)$ and $P_{QD}(1)$ by solving the above five equations simultaneously, the current through the device can be calculated by using the following equation

$$I(V)=e\left[P_{QD}(1)\times\Gamma_D^-(1)-P_{QD}(0)\times\Gamma_D^+(0)\right] \tag{6-31}$$

where e is the charge of an electron. From the I(V) data, the differential conductance(dI/dV) data is obtained by numerical differentiation. The FWHM of the calculated differential conductance peaks are then measured at different temperatures and compared to the experimental results in the following sections.

6.3.4 *Comparison of Differential Conductance FWHM Peak Widths of Experimental Data and Numerical Calculations*

In figure 6-10 the calculated I-V results were presented along with the differential conductance data obtained using numerical differentiation. The numerical calculations were performed using the simulation model explained earlier in this chapter, assuming a single energy level in the quantum dot. These numerical calculations were done at four different temperatures, 77K, 150K, 225K and 295K. From the numerical differential conductance calculations the FWHM of conductance peaks were measured and compared to the FWHM data from the experimental results calculated in section 6.2.2 of this chapter. The FWHM peak widths of the differential conductance peaks from the numerical calculations from the model are found to be a very good match to the experimental FWHM peak widths over the temperature range 77K-295K. Hence, our new simulation model fully explains the observed experimental results and the underlying phenomenon of electron energy filtering. This theoretical understanding gives us capability of creating similar energy filtering structures in other electronic devices whose room temperature operation faces the same Fermi-Dirac thermal smearing problem.

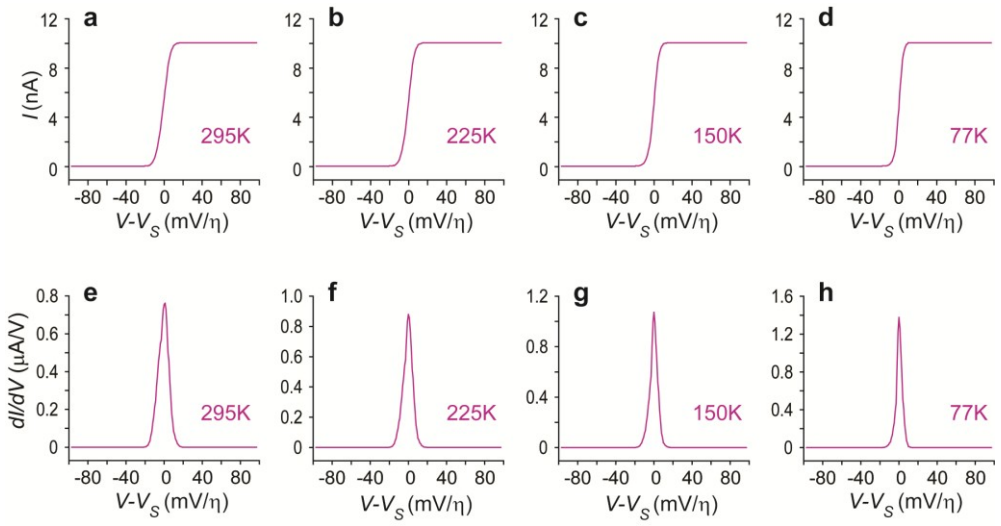


Figure 6-10 Numerically calculated I-V's and dI/dV's obtained from the simulation model (a)-(d) I-V's calculated at different temperatures 295K-77K. (e)-(h) Numerical dI/dV's obtained from I-V's at different temperatures 295K- 77K

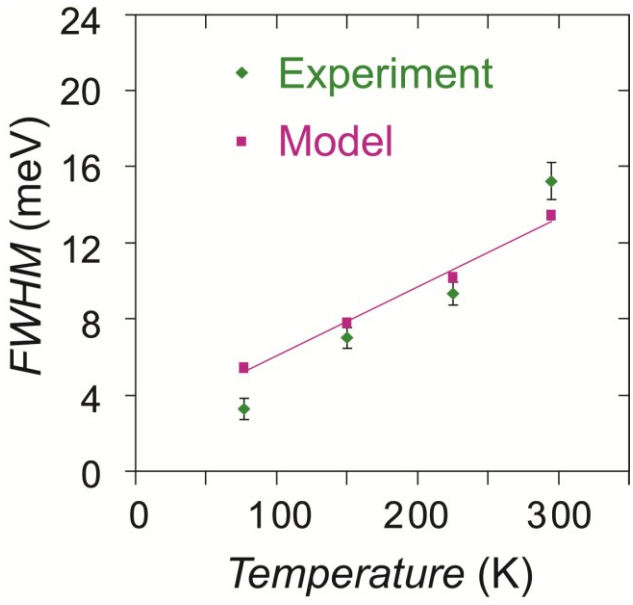


Figure 6-11 Comparison of dI/dV FWHM peak width from experimental data and simulation model at different temperature

In the earlier sections of this chapter we showed that suppression in Fermi-Dirac thermal smearing was observed in our DBTJ devices. This was confirmed by comparing our experimental results to the numerical calculations done taking Fermi-Dirac thermal smearing into account. A new phenomenon of electron energy filtering is responsible for the suppressed Fermi-Dirac thermal smearing and this claim is validated by construction new simulation model taking energy filtering into account. Numerical calculations were carried out using this simulation model and the results were compared to the experimental results. The numerical calculations from simulation model are found to be in very good agreement with the experimental results which validated our simulation model.

Chapter 7

Precise Placement of Single Nanoparticles: A Route to Improve the Yield of DBTJ Devices

7.1 Introduction

In previous chapters (chapter 4) functionalization of substrate surface with Self-Assembled Monolayers (SAM's) was introduced in the context of attachment of CdSe and CdTe nanoparticles. In this chapter we will see a novel technique for precise placement of individual nanoparticles onto desired locations on a substrate surface and the possible use of this approach of nanoparticle placement for fabricating the DBTJ devices will be presented. This concept of precise positioning of nanoparticles when employed for fabrication of DBTJ devices can significantly increase the yield of our devices.

7.2 Concept of Electrostatic Gating

If we have a substrate consisting of positively and negatively charged surfaces and if we immerse such substrate into a colloid containing negatively charged nanoparticles [7.1-7.3]. Then the negatively charged nanoparticles are attracted towards the positively charged surface of the substrate due to electrostatic attraction. Using this simple concept of electrostatic attraction and by engineering the substrate surfaces we can achieve precise placement of individual nanoparticles.

For attaining the attachment of single nanoparticles onto desired substrate locations we engineer the substrate surface in such a way that we can form positively charged circular surfaces surrounded by negatively charged regions. When we immerse such surfaces into a colloid solution containing negatively charged nanoparticles, then

the negatively charged nanoparticles are attracted towards the positively charged circular pattern area as shown in figure 7-1(a). Once a nanoparticle attaches onto the circular pattern area the surface potential mapping of the surface changes in such a way that the second nanoparticle to approaching the surface will be prohibited due to the change in surface potential as shown in figure 7-1(b).

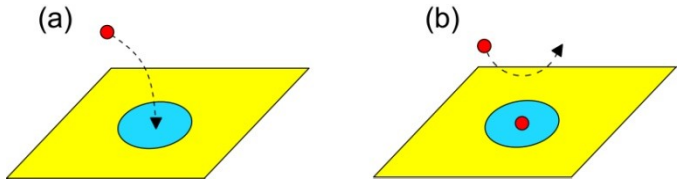


Figure 7-1 Concept of electrostatic gating for single particle placement (a) No nanoparticle is attached onto the substrate location. (b) A nanoparticle is attached onto the substrate location and another nanoparticle is trying to approach the substrate

If we have an array of such circular patterns on our substrate, we can place individual nanoparticles onto desired substrate locations on a large scale over the entire area of the wafer. This approach of placing individual nanoparticles onto desired locations is not limited to planar structures. We can use this concept of electrostatic guiding of nanoparticles to precisely place nanoparticles on even 3-dimensional structures as long as we can fabricate the necessary guiding structures. This concept of electrostatic guiding of nanoparticles can be employed to increase the yield of our DBTJ devices. In later parts of this chapter we will propose a concept for this and we will also propose the fabrication procedures involved to achieve this.

The key factors which have to be controlled for precise placement of individual nanoparticles are the definition of guiding structure itself i.e the size and shape of the structure, the charge density on the nanoparticles and the ion concentration of the colloid.

7.3 Effect of Ion Concentration Vs. Debye Length / Dilution Vs. Inter-Particle Distance

In this section the effect of ion concentration of the colloid solution on the debye length will be investigated. By changing the concentration of ion we can effectively change the interactions in between the nanoparticles in the colloid. When we have more ions in the colloid we the debye length of the nanoparticles will be less and as we decrease the concentration of ions in colloid the debye length increases. The concentration of ions can be altered by addition of DI-water to the colloid and the change in debye length of nanoparticles will have direct effect on the inter-particle distance.

A series of experiments were conducted to investigate this effect using ~20nm Au nanoparticles as our colloid system. For these experiments a 2 cm x 2 cm piece of silicon wafer was chosen as substrate material. The Si wafers are sonicated in acetone followed by acetone rinsing, Isopropanol rinsing and blow drying with nitrogen. These wafers are then treated with UV-Ozone for 30 minutes. The wafers thus prepared will have a thin layer of native Si oxide. These samples are immersed in 1mM APTES solution in chloroform for 30 minutes. This form a SAM's layer of APTES on the Si oxide surface and the surface becomes positively charged when immersed in colloid due to the amine termination of APTES. After 30 minutes the samples are removed from APTES and rinsed with chloroform followed by isopropanol rinsing and blow drying with nitrogen. Now the samples are ready for immersion in ~20nm Au colloid.

The experimental conditions of these samples are shown in Table 7-1. As seen from the data increasing the dilution of colloid increases inter-particle distance. So by

diluting the colloid the ion concentration of colloid can be tailored and this can be utilized in engineering the electrostatic potential mapping during the placement of nanoparticles.

Table 7-1 Effect of dilution of colloid on inter-particle distance

Sample #	Experimental conditions	Average number of particles /500nm^2	Average Inter-particle distance(nm)
1	1:1 Dilution of gold colloid	77	55.61
2	1:3 Dilution of gold colloid	55	65.80
3	1:5 Dilution of gold colloid	49.5	69.36
4	1:1 Dilution of centrifuged gold colloid	53.5	66.72
5	1:3 Dilution of centrifuged gold colloid	43.5	73.99
6	1:5 Dilution of centrifuged gold colloid	37.5	79.69

In figure 7.2 an SEM image of sample #1 that is 1:1 dilution of commercial gold colloid is seen. This gives an idea of how the inter-particle distance was obtained. A square of 500nm x 500nm was drawn in the SEM image and, the number of nanoparticles inside the square area were counted. By counting the number of particles in three different locations on each sample the average number of particles is obtained. This value divided by area of the square gives the average inter-particle distance.

As seen from Table 7-1 the centrifuged and diluted samples have increased in inter-particle distance as of most of the ions in the colloid are gotten rid of during the centrifuge process. Low ion concentration implies increase in debye length hence increase in inter-particle distance.

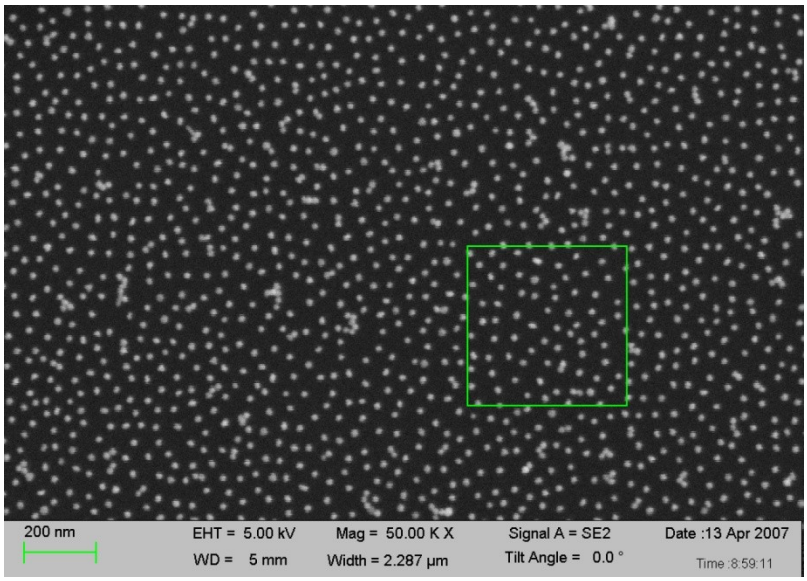


Figure 7-2 SEM Image of ~20nm Au nanoparticles on Si wafer surface

The above set of experiments proves that in addition to the electrostatic guiding structure, the concentration of ions in the colloid can also be modified to engineer the electrostatic forces during the placement of nanoparticles. In the later sections of this chapter the importance of dilution/ion concentration of colloid will be demonstrated in context to limiting placement of one single nanoparticle placement onto each location on the substrate.

7.4 Sample Preparation and Experimental Procedure - Single Particle Placement (SPP)

In this section the sample preparation of precise placement of single nanoparticles onto pre-defined substrate locations will be presented. This involves defining the structures for guiding the nanoparticles and modifying the sample surface with self assembled monolayers (SAM's) to form negatively and positively charged surfaces on the sample.

7.4.1 Defining the Structures for Nanoparticle Placement

In this section the procedure for preparation of samples for single particle placement (SPP) is presented. For defining the electrostatic guiding structure, e-beam writing is employed. The substrate used for preparing these samples is 100 silicon wafers. First the silicon wafer is sonicated in acetone for 10 minutes followed by rinsing in acetone, rinsing in isopropanol and blow drying with nitrogen. The Si wafer is then transferred to UV-Ozone cleaner for 30minutes. The cleaned Si wafer is then diced into 2cm x 2cm pieces for easy handling during e-beam writing.

The e-beam resist used for this purpose is positive PMMA resist. The wafer pieces are spin coated with PMMA resist at 3000 rpm for 60 seconds. The samples are then pre-baked for 120 seconds at 180^0C. The samples are then transfer to ZEISS LEO e-beam writer for e-beam lithography. After writing the desired patterns on the sample, they are developed in 1:3 Methly Iso-Butyl Ketone/Isopropanol solution for 60 seconds. This is followed by isopropanol and DI-water treatment of samples. Extra care must be taken while developing the the samples and during the subsequent steps of isopropanol treatment, DI-water treatment and blow drying of samples with nitrogen. If the samples are not treated gently the patterns on the sample can be destroyed.

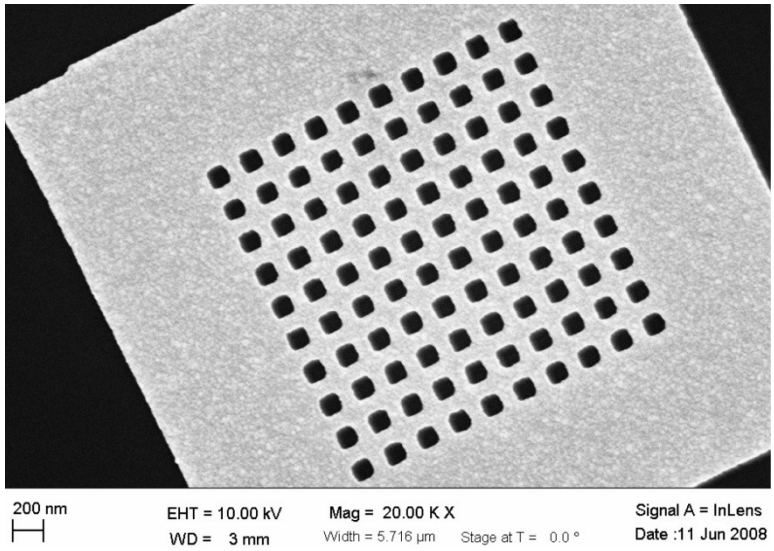


Figure 7-3 SEM Image of a sample e-beam pattern with ~130 nm Si squares

After nitrogen blow drying, the samples are transferred to AJA e-beam evaporator for deposition of chromium and gold layers. Approximately ~5nm of Cr metal is deposited which acts as adhesion layer in between the Si substrate and the gold film, The thickness of gold film deposited on these samples is ~15nm. After the metal deposition the samples go through lift-off and cleaning process, which involves at least 6 cycles of acetone sonication for 10 minutes and UV-Ozone treatments for 30 minutes. The cleaned samples are then immersed in ethanol overnight to remove any gold oxide formed during the UV-Ozone treatment.

7.4.2Self-Assembled Monlayers (SAM's) Formation

The samples removed from ethanol after overnight immersion will be free from gold oxide which can be a hindrance in the formation of 16-Mercaptohexadecanoic acid (MHA) SAM's on gold surface. The samples are rinsed with ethanol and blown dry with nitrogen. Now the samles are ready for surface modification with SAM's layers.

Two different SAM's layers are employed in these experiments. 3-Aminotriethoxysilane (APTES) SAM's which forms a positively charged surface due to their Amine termination are immobilized onto Si oxide surface and 16-Mercaptohexadecanoic acid (MHA) SAM's which forms negatively charged surface due to their –COOH termination are immobilized onto gold surface.

First APTES SAM's were formed on the Si oxide surface by immersing the samples in 1mM APTES solution in chloroform for 30 minutes. The samples are subsequently rinsed with chloroform, isopropanol and blown dry with nitrogen. Then the samples are immediately immersed in 1mM MHA solution in ethanol for 3 hours, after which they are thoroughly rinsed with ethanol and blown dry with nitrogen. Now the samples are ready for immersion in the colloid solution. On these samples treated with APTES and MHA SAM's solutions, the Si oxide surface will be positively charged due to the APTES SAM's layer formation and the gold surface will be negatively charged due to MHA SAM's formation.

7.5 SPP of ~20nm Au Nanoparticles

The experimental results showing precise placement of ~20nm Au nanoparticles onto predefined substrate locations is presented in this section. Also, the precision of nanoparticle placement and the yield of nanoparticle placement is presented along with theoretical simulations explaining the phenomenon responsible for single particle placements. The theoretical calculations are in very good agreement with the experimental results and fully explain the single particle placement technique.

7.5.1 Placement of Single ~20nm Au Nanoparticles

In this section placement of single ~20nm Au nanoparticles onto desired substrate locations will be demonstrated using the electrostatic guiding technique discussed in earlier sections of this chapter. The samples are prepared using the e-beam writing and the sample surface is modified by SAM's layers. These samples are then immersed in ~20nm Au colloid for attachment of nanoparticles onto the sample surface.

After lot of optimization of the size of guiding structures and concentration of ions in the colloid the right condition for placement of one single nanoparticle onto each substrate location is determined. The size of the guiding structure with facilitates placement of one single nanoparticle is found to be ~130nm in diameter and the appropriate gold colloid ion concentration is determined to be 1 :2 diluted ~20nm Au nanoparticle solution. In figure 7-4(a) the SEM image sample processed with these conditions is shown. As seen from the SEM image, in this particular pattern 97/100 Si oxide circles are occupied by one single nanoparticle. The pattern locations where more than one naoparticle are attached or no nanoparticles are attached are indicated by red arrows. Figure 7-4(b) is a substrate location outside of the patterned area where the Si oxide surface is saturated with nanoparticles.

This sample has several such patterns and for statistical purposes four such patterns containing 10x10 array of Si oxide circles were considered and the yeild was found to be 91%. This technique of single particle placement can be employed on wafer scale as long as the whole wafer surface can be patterned with guiding structures.

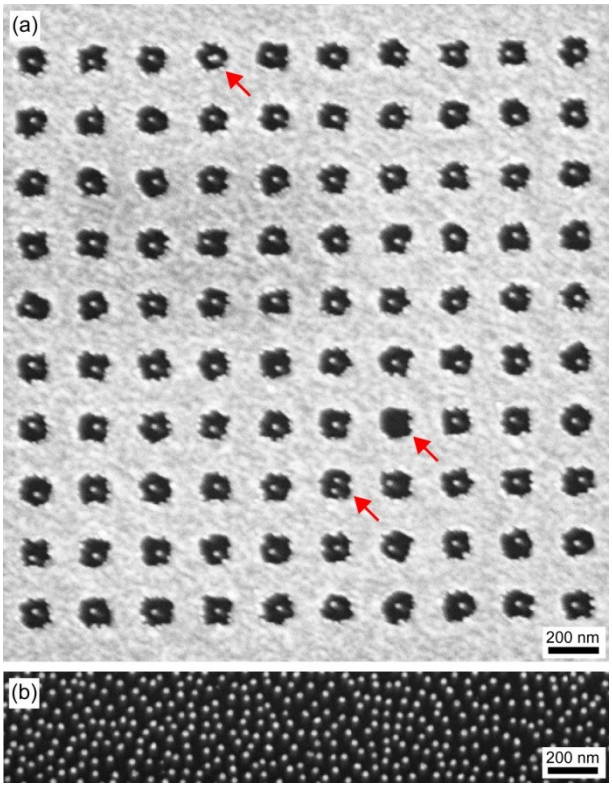


Figure 7-4 SEM image single ~20nm Au nanoparticles placed onto substrate locations (a) Inside the pattern area showing single particle placement (b) Outside the pattern area where the substrate is saturated with Au nanoparticle

7.5.2 Precision of SPP

The precision of placement of each of these single nanoparticles onto the substrate locations is measured. The precision is obtained by measuring the deviation of the nanoparticles from the centre of the Si oxide circle. For obtaining this data, the deviation of nanoparticles from the centre of Si oxide circle is measured for four arrays of 10x10. In total measurements were done on 364 individual nanoparticles. These measurements were taken from the same patterns that are considered for obtaining the yield data. Figure 7-5(a) depicts a histogram graph showing the number of nanoparticles

attached on each Si oxide circle area. Figure 7-5(b) is plot showing the precision of placement of nanoparticles, each dot indicated superimposed positions of each of 364 individual nanoparticles on Si oxide circle area. The measured precision of the single particle placement is ~12.1nm.

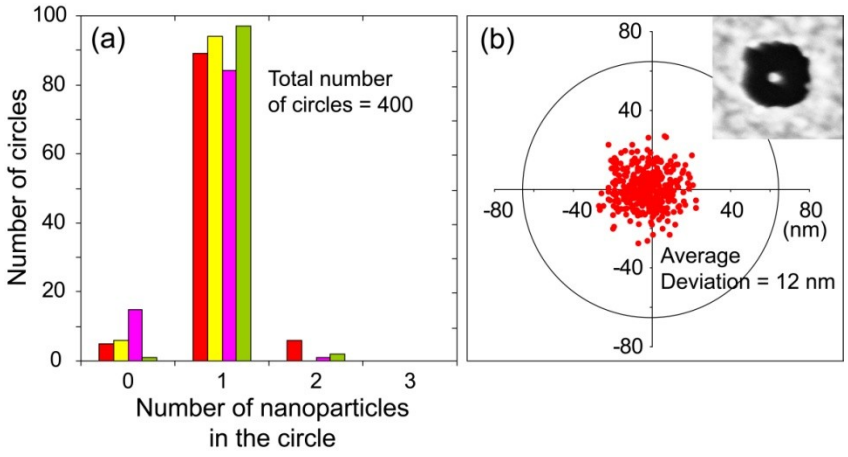


Figure 7-5 Statistics of single particle placement (SPP) (a) Yield of SPP and (b) Precision of SPP

7.5.3 Calculation of Electrostatic Potential and Force Plots Using COMSOL

The single-particle placement demonstrated above can be quantitatively explained by calculating the forces exerted on a nanoparticle as it is approaching the surface of the sample [7.4-7.6]. For calculating these forces the electrostatic potential has to be calculated first and using these electrostatic potential values we can calculate the forces acting on the nanoparticles as they approach the surface of sample. For obtaining these electrostatic potential values non-linear poisson boltzman equation has to be solved. All these calculations were done using COMSOL a commercially available

simulation software capable of solving non-linear differential equations in 3-dimensional space.

First the guiding structure used for single particle placement was constructed in COMSOL software [7.7]. Then the electrostatic potential can be obtained by solving nonlinear Poisson-Boltzmann equation given below

$$\nabla^2\psi(\vec{r}) = -\frac{e}{\varepsilon_r\varepsilon_0}\sum_i z_i\rho_{0i}\exp(-z_i e\psi(\vec{r})/kT) \tag{7-1}$$

where *e* is the unit charge of an electron, ε_r is the dielectric constant of water, ε_0 is the permittivity of free space, z_i is the valency of ion species *i*, ρ_{0i} is the ion concentration of ion species *i* in the bulk (unit: m^{-3}), *k* is the Boltzmann constant, and *T* is the absolute temperature. Figure 7.6 shows the electrostatic potential plots for two conditions. In first situation the Si oxide area is empty and a ~20nm AuNP is 80nm away from the surface of sample in z-direction as shown in inset of figure 7-6(a). In the second situation the Si oxide area is already occupied by a ~20nm AuNP and the second ~20nm AuNP is 80nm away from sample surface in z-direction as shown in inset of figure 7-6(b).

With electrostatic potentials ψ ($\vec{r}$) obtained, Force $\vec{F}$ ($\vec{R}$) [7.8-7.11] acting on the nanoparticles is calculated using the equation given below

$$\nabla^2\psi(\vec{r}) = -\frac{e}{\varepsilon_r\varepsilon_0}\sum_i z_i\rho_{0i}\exp(-z_i e\psi(\vec{r})/kT) \tag{7-2}$$

$$\vec{F}\left(\vec{R}\right) = \iint_S \left[\left(kT\sum_i(\rho_i-\rho_{0i})\right)\mathrm{I}\cdot\hat{n} + \left(\frac{\varepsilon_0\varepsilon_r}{2}\left|\vec{E}\right|^2\mathrm{I}\cdot\hat{n} - \varepsilon_0\varepsilon_r(\vec{E}\cdot\hat{n})\vec{E}\right)\right]dS \tag{7-3}$$

where $\rho_i = \rho_{0i}\exp(-z_i e\psi(\vec{r})/kT)$ and $\vec{E} = -\vec{\nabla}\psi(\vec{r})$,

where, ρ_i is the ion concentration of ion species *i*, $\vec{E}$ is the electric field, I is the unit tensor, and $\hat{n}$ is the unit vector pointing normal to the surface *S* enclosing the nanoparticle at distance $\vec{R}$. The origin of the first term of Eq. (7-3) is from the osmotic pressure and the second term originates from electrostatic stress. The plots showing the calculated forces acting on the ~20nm AuNP are shown in figure 7-7. The force calculations were done for two conditions. In first situation the Si oxide area is empty and a ~20nm AuNP is 80nm away from the surface of sample in z-direction as shown in inset of figure 7-7(a). In the second situation the Si oxide area is already occupied by a ~20nm AuNP and the second ~20nm AuNP is 80nm away from sample surface in z-direction as shown in inset of figure 7-7(b).

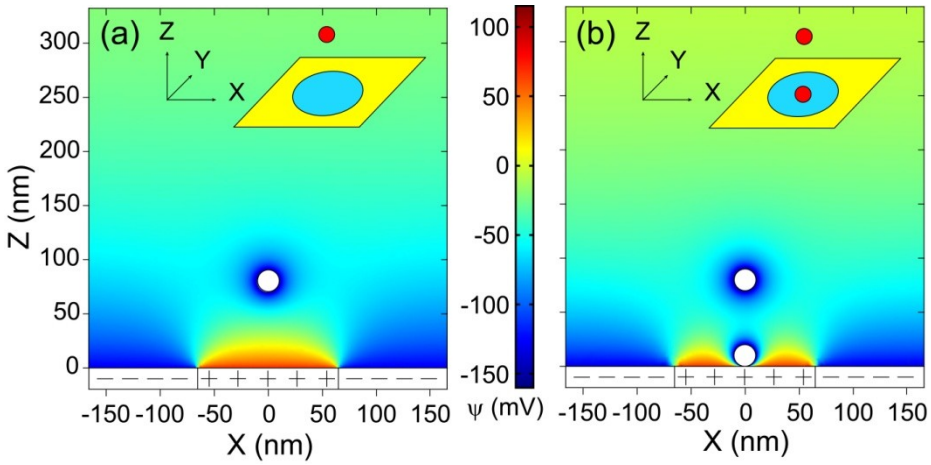


Figure 7-6 Plots showing electrostatic potential mappings obtained by solving nonlinear Poisson-Boltzmann equation. (a) Empty substrate location with a nanoparticle approaching the surface. (b) Substrate location occupied by one nanoparticle and another approaching the substrate.

As seen from the force plots in figure 7-7(a) when there is no ~20nm AuNP occupying the Si oxide surface the repulsive force due to the negatively charged Au surface of sample is very low as indicated by the dotted circle in figure 7-7(a). Once the nanoparticle overcomes this repulsion force it will be attracted towards the center of the positively charged Si oxide area. Where as in the second situation when the Si oxide area is already occupied by one ~20nm AuNP, the surface potential changes in such a way that a second nanoparticle will cannot overcome the free energy barrier.

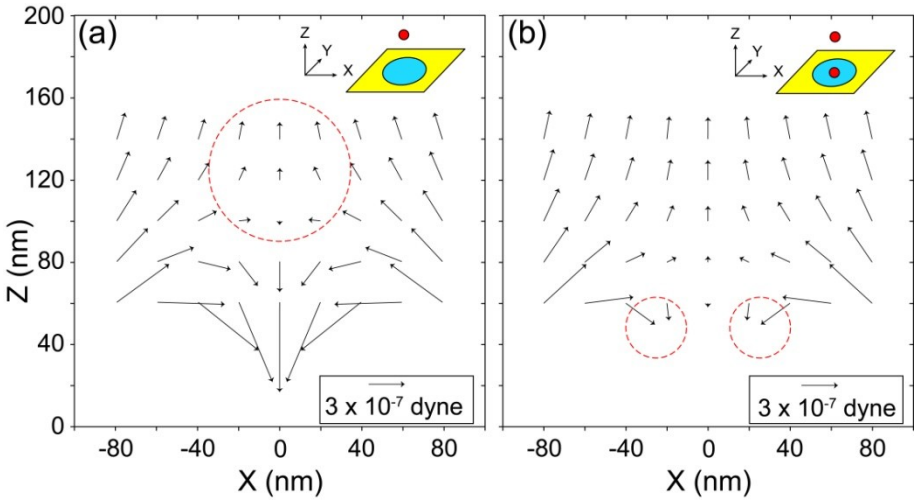


Figure 7-7 Plots showing the forces acting on the ~20nm AuNP (a) Empty substrate location with a nanoparticle approaching the surface. (b) Substrate location occupied by one nanoparticle and another approaching the substrate.

7.6 Size-Selective Placement of Single Nanoparticles

The single particle placement technique introduced in earlier sections enables even placement of different sized nanoparticles on to different predefined locations on the

sample substrate. This capability of single particle placement technique will be explored in this section and the initial results obtained are presented here.

7.6.1 Concept of Size-Selective Placement

If a sample consisting of two different sized guiding structure is fabricated in a similar fashion as discussed in section 7.4. This technique of particle placement can essentially be used for placement of two different sized particles onto different locations on the same substrate. A schematic depicting this idea is shown in figure 7-8.

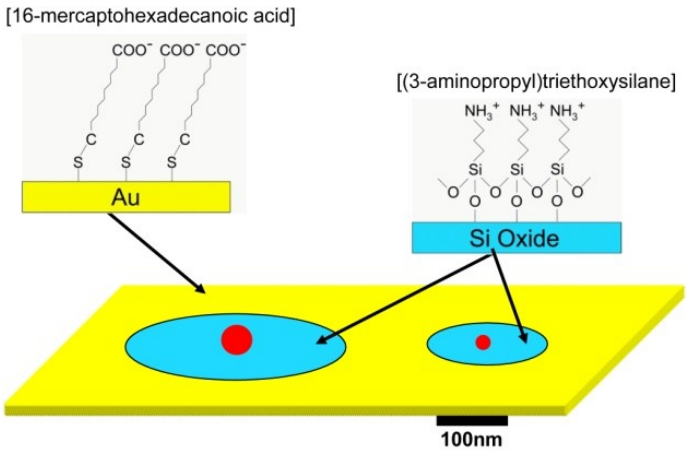


Figure 7-8 Concept of Size-selective placement of nanoparticles

For demonstrating size-selective single particle placement, ~20nm AuNP's and ~50nm AuNP's were chosen. Single particle placement for ~20nm AuNP's was already shown in previous section. The size of the guiding structures has to ~130nm for 1:2 diluted ~20nm AuNP's placement. The right size of guiding structure for ~50nm AuNP's placement has to be determined before attempting the size selective placement of nanoparticles.

7.6.2 SPP of ~50nm Au Nanoparticles

The technique of single particle placement is not limited to placement of ~20nm AuNP's, this technique can be used for placement of different shaped, sized and different species of nanoparticles onto different locations on the same substrate. These capabilities of single particle placement technique are put to test by attempting to place two different sized nanoparticles onto different locations on the same substrate. For demonstrating this ~50nm and ~20nm AuNP's were chosen. The size of guiding structure to be used for ~20nm AuNP placement is already known. To determine the right size of guiding structure for ~50nm AuNP, different sized square guiding structure with sizes ranging from ~150nm to 250nm were tried. The right size for placement of ~50nm AuNP's was determined to be ~200nm square pattern. Figure 7-9 shows an SEM image of single particle placement demonstrated using ~50nm AuNP on 5x5 array of ~200nm square guiding structures. As can be seen from the figure 7-9 the yield of placement is about 92%, but the precision is not that great.

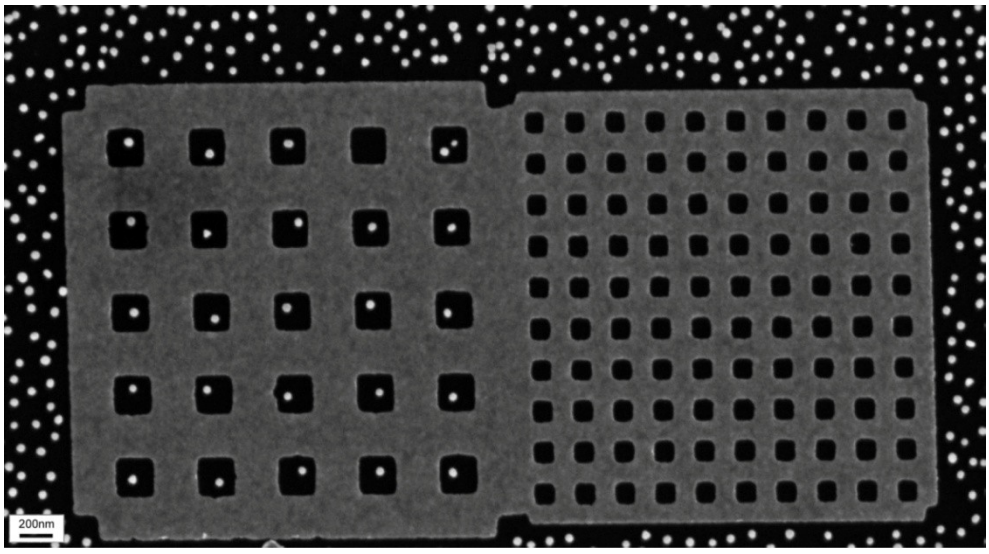


Figure 7-9 Single particle placement of ~50nm AuNP's

The above experimental results proved that the concept of selective placement of nanoparticles of different sizes is possible. As can be seen from figure 7.9, the ~50nm Au nanoparticles occupy only the ~200nm Si oxide squares and all of the ~130nm squares intended for placement of ~20nm Au nanoparticles are empty. But before attempting to place ~20nm Au nanoparticles, the precision of placement of ~50nm Au nanoparticles must be addressed.

7.6.3 Change in Pattern Shape Towards Increasing the Precision of SPP

Although the yield of placement of ~50nm AuNP's is good the precision of placement has taken toll. This is due to the square guiding structures being used for placement of nanoparticles. In order to improve the precision of placement, the ideal shape of the guiding structure is circular areas of Si oxide. With the PMMA positive resist it is very difficult to write circular patterns.

This challenge was overcome by modifying the patterns to write hexagons instead of squares and then over develop the samples so that the pattern with rounded edges looks like more of a circle than a hexagon. Figure 7-10 shows SEM image of one such pattern written using PMMA resist. As can be seen from image the patterns appear to be more circular than like hexagons although the actual pattern we attempted to write were hexagons.

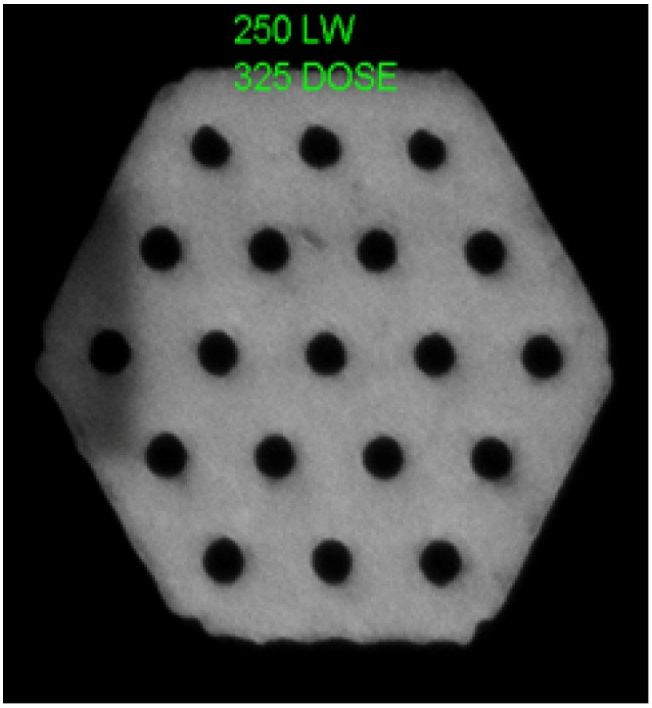


Figure 7-10 SEM image of ~180nm hexagonal patterns which are over developed to look like circular patterns

7.6.4 Size-Selective Placement of ~50nm and ~20nm Au Nanoparticles

For selective placement of ~50nm and ~20nm Au nanoparticles onto different locations on same substrate, first the required guiding structures must be fabricated on the same sample. The substrate used for these experiments is Si wafer which has a thin layer of native oxide. The guiding structures were defined using e-beam lithography, metal evaporation, metal lift-off and SAM's layer formation as defined in section 7.4.

During the size selective placement of nanoparticles, the placement of ~50nm AuNP's will be carried out first and then the samples were cleaned with UV-ozone to get rid of all the SAM's layers. A fresh SAM's layer was formed by immersing sample in APTES for 30 minutes and MHA for 3 hours following the procedures explained in section

7.4.2. After forming fresh SAM's layers the samples are immersed in ~20nm AuNP's colloid. Figure 7.11 shows SEM images of samples which has gone through ~50nm and ~20nm AuNP colloids. In the SEM images the ~50nm AuNP are attached only outside of the patterned area. Although the circular patterns are ~130nm in size the ~50nm AuNP's cannot attach in these circular patterns because of the repulsion force from the negatively charged Au surface being dominant as discussed in earlier sections. But when the samples are placed in ~20nm AuNP colloid the repulsive force can be overcome by the ~20nm AuNP's and they attach on to the ~130nm circular patterns.

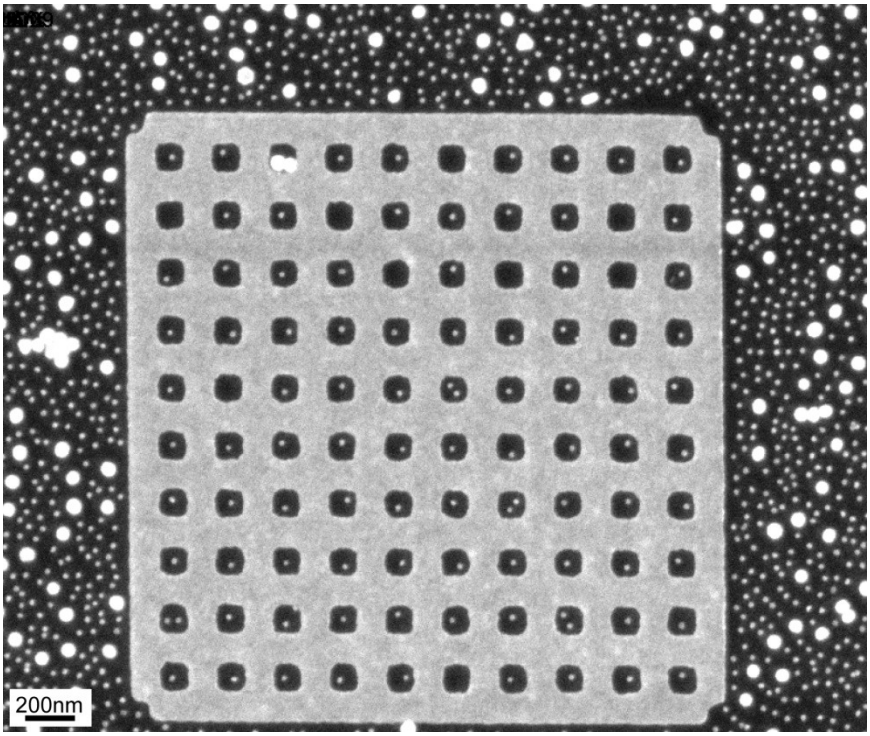


Figure 7-11 SEM image depicting size selective placement of ~50nm and ~20nm AuNP's

The same size selective placement of ~50nm and ~20nm AuNP experiment was carried out with different variations of the size of guiding structures and concentration of

gold colloid. The right condition for attachment of ~50nm and ~20nm AuNP's is ~160nm guiding structures for ~50nm AuNP's and ~100nm guiding structures for ~20nm AuNP's. The SEM image shown in figure 7.12 shows that when the ~50nm AuNP's are attached at the center of ~160nm guiding structures, no other nanoparticles can approach these circular Si oxide patterns. Also, as can be seen from the image the ~50nm AuNP's cannot attach in the ~100nm Si oxide pattern area. And the ~20nm AuNP's attachment in 6x6 array of ~100nm Si oxide circles is almost perfect. Out 36 patterned Si oxide circles 35 of them are single ~20nm AuNP's. By further tuning the ion concentration in ~50nm colloid, the yield of ~50nm AuNP placement can be improved.

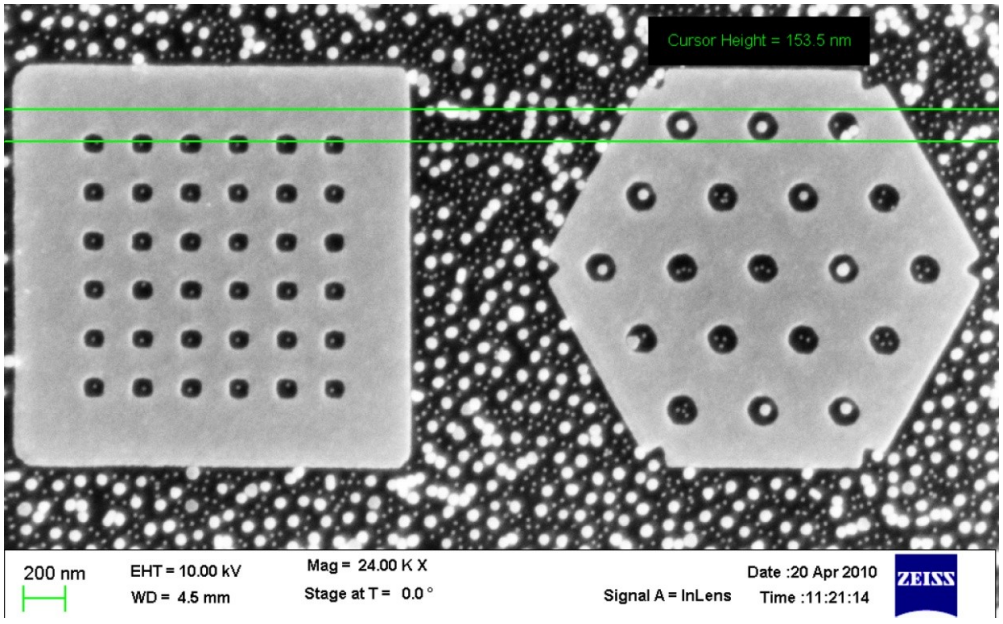


Figure 7-12 SEM image of size selective placement of ~50nm and ~20nm AuNP's

7.7 Concept for Precisely Guiding Quantum Dots onto Sidewall of DBTJ Devices

The nanoparticle placement technique introduced in earlier section of this chapter is not limited to planar structures. This technique can also be used on vertical structures as long as we can modify the surface of these vertical structures to form positive and negatively charged surfaces to form the guiding structures.

In this section some modifications to the existing DBTJ device was proposed so that, the nanoparticle placement technique can be used for placement of quantum dots onto the dielectric layer of the sidewall structure in our DBTJ devices. For realizing this, the key will be formation of guiding structure.

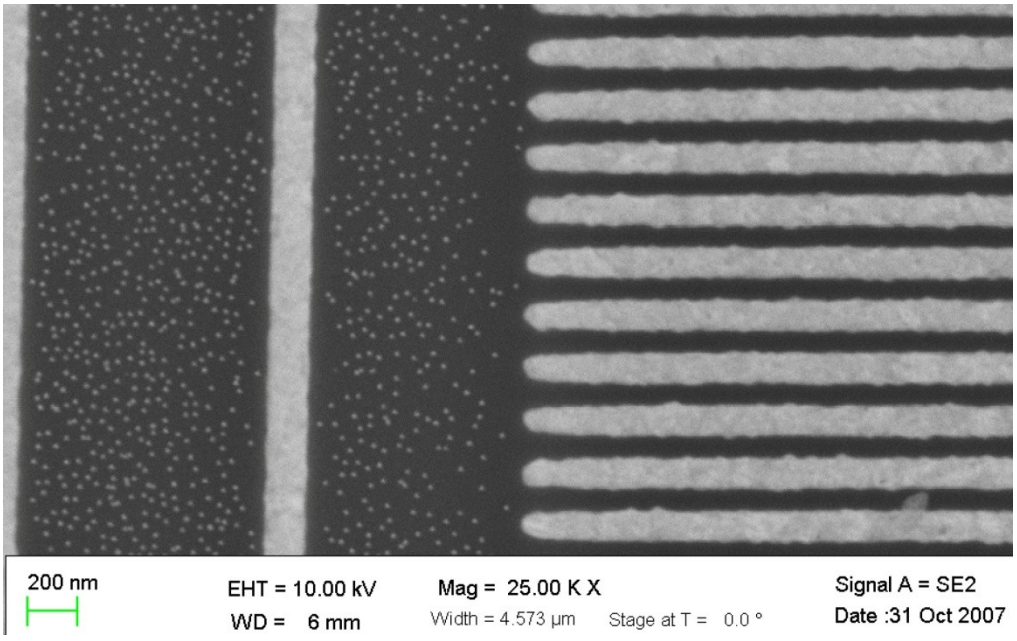


Figure 7-13 SEM image showing no attachment of ~20nm AuNP's in Si oxide trench area, when the trenches are narrow, due to high repulsive forces from the gold surface

The present structure being used for DBTJ devices consists of chromium bottom and top electrodes which must be replaced with gold to form the guiding structure for precise placement of quantum dot on the dielectric layer of the sdewall. Before realizing the precise placement of quantum dots on the vertical electrode structure, initial studies were done to check the attachment on a K-wafer (Texas Instruments) which has trench structures. When the Si oxide trenches are narrow the ~20nm AuNP's did not attach inside the Si oxide trench area, however outside the trench area they are saturated. The SEM image of K-wafer with ~20nm AuNP's was shown in figure 7-13. From this experiment it is realized that if we replace our electrodes with gold instead of chromium to form guiding structures for quantum dot placement it is not enough. There won't be any attachment of quantum dots on the sidewall of dielectric layer due to high repulsive forces from negatively charged gold surface.

Another set of experiments were conducted to check if APTES can form on the chromium surface. In figure 7-14 an SEM image showing the results of this experiment was shown. The ~20nm AuNP's are attached on the chromium surface and there is no AuNP attachment on the gold surface. So a chromium intermediate layer can be used to reduce the repulsive forces from the gold surface of the electrodes.

Figure 7-15 depicts the idea of proposed structure of electrodes for DBTJ devices. If the chromium electrodes are replaced by gold metal, MHA can be formed on the electrodes and the negatively charged quantum dots can be guided onto the dielectric insulating layer so the quantum dots are attached only on the dielectric layer of the sidewall instead of random attachment of quantum dots.

In the structure shown in figure 7-15, a thin chromium layer was seen between the gold and the PECVD/ALD oxide layer. This chromium layer serves two purposes, firstly it acts as adhesion layer between the PECVD/ALD oxide and gold layers and

secondly APTES can be readily formed on chromium which can facilitate attachment of negatively charged quantum dots. This was checked by having chromium and gold layers side by side on a Si wafer, then process the sample through APTES and MHA solution to form SAM's layers and then immerse the samples in ~20nm AuNP colloid. The SEM image of this experiment was shown in figure 7-14

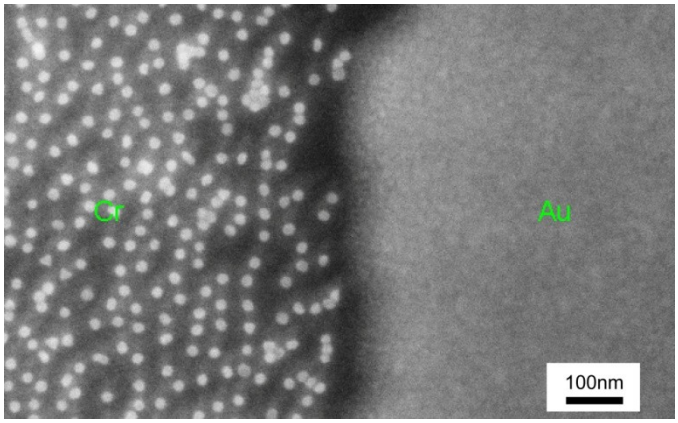


Figure 7-14 Selectivity of ~20nm AuNP attachment on Cr and Au surfaces.

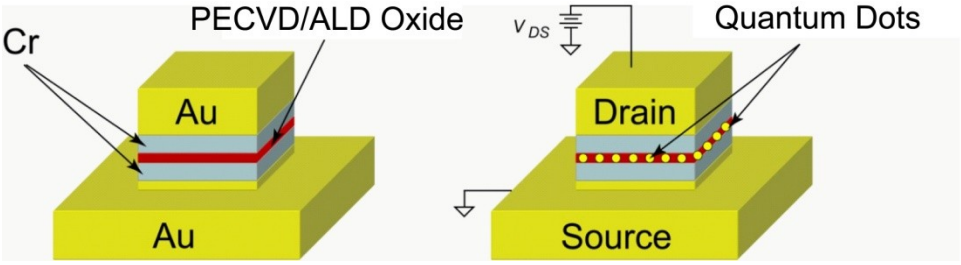


Figure 7-15 Proposed structure of DBTJ devices for precise placement of quantum dots

The structure proposed in figure 7-15 will enable the precise placement of quantum dots onto the dielectric layer on the sidewall. This in turn will increase the chances of finding the quantum dots in the right distance range from electrodes for

tunneling of electrons to take place. The yield of DBTJ device is expected to increase by many folds with the use of the precise nanoparticle placement technique.

This technique of precise placement of nanoparticles/quantum dots onto the sidewall of the DBTJ device sidewall can increase the yield of these devices considerably. Compared to the current procedure of random placement of nanoparticles/quantum dots, this technique of precise placement can place the nanoparticles/quantum dots onto a position on sidewall where the chances of tunneling will be very high through them. Thus, this technique will increase the yield of the devices.

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Biographical Information

Mr. Pradeep Krishna Bhadrachalam was born in Guntur, India on 5th of july 1984. He completed his bachelor's degree in Metallurgical Engineering from Jawaharlal Nehru Technological University College of Engineering at Hyderabad, India in May 2005. After graduating with his bachelor's degree he worked as an Engineering trainee at Bharat Heavy Electricals Limited at Hyderabad from July 2005 to June 2006. He started pursuing his Master's Degree in Materials Science and Engineering department of The University of Texas Arlington in August of 2006. He joined Dr. Koh's research group in January 2007 and switched to Doctorate program in May 2008. During his course of study he received Best Graduate Student Researcher Award from The Minerals, Metals, and Materials Society (TMS) annual conference held at San Diego, CA, in March 2011. He received NanoFab Award for Best Citizen from the NanoFab Research Center in February 2012 at The University of Texas at Arlington. He was also awarded Best Student Paper Award from Materials Science and Engineering Department twice in February 2012 and March 2013 at The University of Texas at Arlington. He received first prize at the inter-university research presentation competition, the 5th North Texas Inter-University Materials Science and Engineering Symposium sponsored by North Texas Chapter of ASM International in April 2014.