ANALYTICAL AND EXPERIMENTAL INVESTIGATION OF THERMAL TRANSPORT IN THREE-DIMENSIONAL INTEGRATED CIRCUITS (3D ICs)

by

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July 15, 2014

Abstract

ANALYTICAL AND EXPERIMENTAL INVESTIGATION OF THERMAL TRANSPORT IN THREE-DIMENSIONAL INTEGRATED CIRCUITS (3D ICs)

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The University of Texas at Arlington, 2014

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Thermal management of three-dimensional integrated circuits (3D ICs) is recognized to be one of the foremost technological and research challenges currently blocking the widespread adoption of this promising technology. The computation of steady-state temperature fields in a 3D IC is critical for determining the thermal characteristics of a 3D IC and for evaluating any candidate thermal management technology. An analytical solution for the three-dimensional temperature field in a 3D IC based on solution of the governing energy equations using Fourier series expansion for steady-state temperature fields is studied. Comparison of the predicted temperature fields with finite-element simulation shows excellent agreement. The model is used to compute the temperature field in a 3D IC, and it is shown that by utilizing a thermal-friendly floorplanning approach, the maximum temperature of the 3D IC is reduced significantly.

Several 3D IC manufacturing and packaging approaches require adjacent die sizes to be different from one another since this enables differentiated manufacturing and design. However, it is expected that unequally-sized die may cause deteriorated thermal performance due to heat spreading and constriction. Heat transfer model for predicting the three-dimensional temperature field in a multi-die 3D IC with unequally-sized die is

studied. The model is used to compare the thermal performance of unequally-sized die stacks with a uniformly-sized die stack. Results indicate that the greater the degree of non-uniformity in the die stack, the greater in the peak temperature rise.

An analytical modeling of heat transfer in interposer-based microelectronic systems is described. The analytical model is developed to study the effect of various parameters on the temperature field in an interposer system.

A non-iterative, analytical heat transfer model for computing three-dimensional temperature fields in a 3D IC has been proposed. The governing energy equations with appropriate boundary conditions for N-die stack with different values of N are solved by first writing the solution in terms of infinite series, followed by deriving and solving ordinary differential equations for the coefficients in the series. Steady-state temperature fields predicted by the model compare well with FEM-based simulation results and previously developed iterative models. In addition, temperature computation based on the proposed models is much faster than numerical simulations or iterative approach. Expressions for the temperature field are derived for perfect contact between layers as well as for non-zero thermal resistance between layers. Several applications of the model are also discussed. These include temperature computation for a 3D IC with a large number of strata, as well as the effect of inter-die thermal contact resistance. The Results may find applications in development of tools for rapid thermal computation for 3D ICs. Experimental measurements help validate thermal models for predicting the temperature field in a 3D IC. Experimental results on thermal performance of a two-die 3D IC are presented. Heaters and temperature sensor circuits embedded in each layer are utilized to generate heat and measure temperature rise in each layer respectively. Both steady-state and transient data are reported. The experimental setup and theoretical model for measuring thermal contact resistance between two adjacent die introduced and the

experimental value of thermal contact resistance compere well with theoretical model result. The experimental setup and procedure are described and the results used to determine inter-die thermal resistance of two-die stack.

Table of Contents

Acknowledgements ... iii

Abstract ... v

List of Illustrations ... xi

Chapter 1 Introduction ... 1

1.1 Fabrication Methods of 3D ICs ... 1

1.2 Advantages of 3-D Packaging Technology ... 2

1.2.1 Size and Weight ... 3

1.2.2 Silicon Efficiency ... 3

1.2.3 Delay ... 3

1.2.4 Power Consumption ... 4

1.2.5 Speed ... 5

1.2.6 Interconnect Usability and Accessibility ... 5

1.2.7 Bandwidth ... 6

1.3 3D IC Design Methods ... 6

1.3.1 Bottom-Up Wafer-Scale Fabrication ... 8

1.3.2 Top-Down Wafer-Scale Fabrication ... 8

1.3.3 3D IC Stacking ... 8

1.4 Cooling Systems ... 9

1.5 Thermal Management of 3D ICs ... 16

1.6 Thesis Organization ... 18

Chapter 2 Analytical Solution for Steady-State and Transient Temperature

Field in Vertically Integrated Three-Dimensional Integrated Circuits (3D ICS) ... 20

2.1 Introduction ... 20

2.2 Steady-State Heat Conduction Model for a 3D IC ... 24

2.3 Application of Analytical Model to Understand Thermal-Friendly Floorplanning 38
2.4 Transient Heat Conduction Model for a 3D IC 41
2.5 Conclusions 47
Chapter 3 Determination of Temperature Distribution in Three-Dimensional Integrated Circuits(3D ICS) with Unequally-Sized Die 48
3.1 Introduction 48
3.2 Steady-State Heat Conduction Model for Non-Uniformly Sized 3D IC 51
3.2.1 Solution to Three Relevant Heat Transfer Problems 52
3.2.2 Solution to the N-Die Heat Transfer Problem 58
3.3 Model Results 61
3.4 Application of Model for Comparison of Non-Uniformly Sized Die Stack with Uniform Die 68
3.5 Conclusions 69
Chapter 4 Analytical Modeling of Temperature Distribution in Interposer-Based Microelectronic Systems 70
4.1 Introduction 70
4.2 Steady-State Heat Conduction Model 72
4.3 Model Results 77
4.4 Conclusions 83
Chapter 5 An Explicit Analytical Model for Rapid Computation of Temperature Field in a Three-Dimensional Integrated Circuit (3D IC) 84
5.1 Introduction 84
5.2 Steady-State Thermal Conduction in a Multi-Die 3D IC 87
5.2.1 Perfect Thermal Contact 88

5.2.2 Non-Zero Thermal Contact Resistance Between Interfaces 93

5.3 Results and Discussion 95

5.4 Conclusions 110

Chapter 6 Experimental Measurement of the Thermal Performance and

Thermal Contact Resistance of an Un-Equally Sized Two Die Stack 111

6.1 Introduction 111

6.2 Experimental Setup 113

6.3 Results and Discussion 118

6.4 Determination of Thermal Contact Resistance Between Two Die 124

6.5 Conclusions 133

Chapter 7 Conclusions and Future Study 134

7.1 Summary of Main Conclusions 134

7.2 Future Research in Analytical Model 135

7.3 Future Research in Experiment 136

Appendix A LAB View Program 138

References 139

Biographical Information 156

List of Illustrations

Figure 1-1 Stacked Die and Wafer Level Integration [Lu et al.,2009;Tummala et al., 2009; Fukushima et al., 2009; Choudhury, 2010]:(a) Die-on-Die, (b) Die-on-Wafer, (c) Self-Assembly of Die-on-Wafer, (d) Wafer-on-Wafer,(e) Die, Stacked-Die, 3D-WLP on System Wafer.. 2

Figure 1-2 A Graphical Illustration of Silicon Efficiency between 2-D and 3-D Technology [Said et al., 1998] 4

Figure 1-3 A Comparison between the Wiring Lengths in 2-D and 3-D Structure [Lakhani et al., 1996] 4

Figure 1-4 Accessibility and Usability of Interconnection in 2-D and 3-D Packaging [Said et al., 1998] 5

Figure 1-5 Possible Numbers of Interconnections in 3-D and 2-D Structure [Said et al., 1998] 6

Figure 1-6 Schematic Diagrams of Assembled 3D IC Structures; Dashed Line Indicates Bonded Interface: (a) SOI-Based Face-to-Back Process with Closely Coupled Layers; (b) Face-to-Face Bonding (c) Face-to-Back Process [Topol et al., 2004] 7

Figure 1-7 Conventional Air Cooling.[King et al., 2010].. 10

Figure 1-8 High-Power Liquid Cooled 3D-PCB-Packages (28 x 28 x 20 mm^3) [Schindler-Saefkow et al., 2006] 11

Figure 1-9 Multidimensional Heat Transfer System (MHTS) [Phan et al.,2010]............... 13

Figure 1-10 Schematic of a 3D Package with an Efficient Pyramid Lid…………………...14

Figure 1-11 (a) Cross Section through a Chip Stack with TSVs Embedded in a Fluid Containment with Electrical Feed-Through. (b) Detailed View of TSV, Fluid Channels, and Solder Concept [Brunschwiler et al., 2009] 14

Figure 1-12 Schematic Representations of the Three Cooling Configurations for the DRAM on Logic Stack Used for the Thermal Analysis [Oprins et al., 2012]........ 15

Figure 2-1 Schematic of the N-Die 3D IC 24

Figure 2-2 Plot Showing the Accuracy of the Hotspot Temperature Computation as a Function of the Number of Terms Considered in Equations (10), (13) and (16) . 33

Figure 2-3 Plot Showing the Temperature Profile Across the Hotspot on Die1 as a Function of the Number of Iterations Carried Out …..……………………………..34

Figure 2-4 (a) Computed Temperature Field for the Two-Die 3D IC, (b) Cross-Section Temperature Curve Comparing the Model with Finite-Element Simulations…....35

Figure 2-5 (a) Computed Temperature Field for the Three-Die Case, (b) Cross-Section Temperature Profiles Compared with Finite-Element Simulations 37

Figure 2-6 (a) Schematic Showing the Two Floorplans Considered, (b) Temperature Plots on the Device Planes of the Three Die for the Two Floorplans 40

Figure 2-7 Schematic of the Two-Die Stack for Transient Temperature Field Computation. 42

Figure 2-8 Comparison of Transient Temperature Profile at the Hotspot in a Two-Die 3D IC Predicted by the Analytical Model and Finite-Element Simulations 46

Figure 3-1 Schematic of the Cross-Section View of the N-die Stack Comprising Unequally Sized Die 52

Figure 3-2 Schematics of Three Single-Die Heat Transfer Problems Solved in Section 2.1. In Each Case, the Four Side Walls Are Adiabatic 53

Figure 3-3 Effect of the Number of Terms Considered in the Double Summation on Accuracy of Temperature Computation 62

Figure 3-4 Effect of the Number of Iterations on Temperature Computation Accuracy ... 63

Figure 3-5 Plot Showing the Accuracy of the Hotspot Temperature Computation as a Function of the Number of Terms Considered in Equations (10), (13) and (16) . 64

Figure 3-6 Plot Showing the Temperature Profile Across the Hotspot on Die1 as a Function of the Number of Iterations Carried Out. 64

Figure 3-7 Computed Temperature Field in a Three-Die, Unequally-Sized Stack with Non-Uniform Heating (a) Power Map,(b) Temperature Field 66

Figure 3-8 Computed Temperature Field in a Three-Die, Unequally-Sized Stack with Non-Uniform Heating (a) Thermal Friendly Power Map,(b) Temperature Field .. 67

Figure 3-9 Comparison of Temperature along the Centerline of Die2 for Three Cases of Three-Die Stacks with Different Amounts of Die Size Non-Uniformity 69

Figure 4-1 Schematics of the Top and Side Views of Interposer-Based 2.5D System 73

Figure 4-2 Schematics of Substrate and Single Chip Heat Transfer Problems Solved in Section 4.2. In Each Case, the Four Side Walls Are Adiabatic 75

Figure 4-3 Effect of the Number of Terms Considered in the Double Summation on Accuracy of Temperature Computation 78

Figure 4-4 Effect of the Number of Iterations on Temperature Computation Accuracy ... 79

Figure 4-5 Temperature Field on the Top Surface of Substrate with a Hotspot on Each Chip 80

Figure 4-6 Comparison of Temperature at Top Surface of Substrate, Determined from the Analytical Model with Finite-Element Simulation Results Along the Cross-Section Line Shown in Figure 4.5 80

Figure 4-7 Computed Temperature Field at the Top Surface of Substrate in Different Locations of Chips. Power Map Is Shown Using Hatched Lines 81

Figure 4-8 Computed Temperature Field at the Top Surface of Substrate in Different Locations of Substrate Heat Spots. Power Map Is Showing Using Hatched Lines82

Figure 4-9 Computed Temperature Field at Top Surface of Substrate for (a) Active Interposer, (b) Passive Interposer 83

Figure 5-1 Schematic of the N-Die Stack, and a Cross-Section View of the ith Die Showing the Heat Generation Distribution 87

Figure 5-2 A Model for Thermal Contact Resistance Between Two Adjacent Die 94

Figure 5-3 Temperature at Top Surface of Fifth Die in a Ten-Die Case for Different Number of Terms Included in the Double Summations 96

Figure 5-4 Maximum Temperature Rise in N-die Stack as a Function of Number of Die for Two Different Cases 97

Figure 5-5 Temperature Rise at Top Surface of Die 5 for a Ten-Die Stack Case with Different Values of Thermal Contact Resistance 98

Figure 5-6 Maximum Temperature Rise at Top Surface of Die 5 in a Ten-Die Stack Case with Different Values of Convective Heat Transfer Coefficient 99

Figure 5-7 (a) Thermally Unfavorable Power Map of a 5-die Stack, (b) Computed Temperature Field for the Power Map. 100

Figure 5-8 (a) Thermally Favorable Power Map of a 5 - Die Stack, (b) Computed Temperature Field for the Power Map 101

Figure 5-9 (a) Powermap of a 15-Die Stack Representative of an APU-GPU Microprocessor Unit, (b) Computed Temperature Field for the Power Map 102

Figure 5-10 (a) Powermap of an Alternative, Thermally-Friendly Floorplan for the 15-Die Stack, (b) Computed Temperature Field for the Power Map 104

Figure 5-11 Temperature Map in Different Height for Three Die Case (a) Power Map, (b) z=0.5 mm,(c) z=0.25 mm,(d) z=0 mm 106

Figure 5-12 Temperature Map in Different Height for Three Die Case (a) Powermap for Three Die Case for Every Die, (b) Temperature Distribution at z=0.5 mm for Every Die, (c) Temperature Distribution at z=0.25mm for Every Die,(d) Temperature Distribution at z=0mm for Every Die... 108

Figure 5-13 Temperature Rise at the Center of Each Die in z Direction (a) Die 1, (b) Die 2, (c) Die 3... 109

Figure 6-1 Schematic of the Two Die in the 3D IC. Blue Lines Show the Heater, and Red Lines Show the Top Die Sensor and Green Lines Show the Bottom Die Sensor114

Figure 6-2 (a) An Image of the Two-Die 3D IC on a LCC Substrate,(b) the Image of Gold Wire Bonding Under a Microscope 115

Figure 6-3 (a) Top and Side View of the Socket, (b) An Image of the Soldered Socket Used for Accessing Thermal Features on the 3D IC 116

Figure 6-4 Substrate Mounted in the Socket and Soldered Wires 117

Figure 6-5 Image of the Experimental Setup for Thermal Calibration of Temperature Sensors on Each Die 118

Figure 6-6 Thermal Calibration Curve for Top and Bottom Die Sensor......................... 119

Figure 6-7 Experiment Setup for Studying Heater Effects on Sensors 120

Figure 6-8 (a) Plot Showing Temperature Rise in Each Sensor Due to Heating in Bottom Die, (b) Top Die.. 121

Figure 6-9 Plot Showing Temperature Rise in Top and Bottom Die Sensors as a Function of Heating in the Same Die 122

Figure 6-10 Plot Showing Transient Characteristics of the Top and Bottom Die. Red and Green Curves Show Temperature Rise in Top and Bottom Die Sensor After Starting a 0.6W Power at t=0 in (a) Top Die, (b) Bottom Die............................ 123

Figure 6-11 Temperature Rise in Bottom Die Sensor vs. Time by Heating the Top Die for Different Values of Coefficient of Convective Heat Transfer,(a) Finite Element Simulation,(b) Experiment... 125

Figure 6-12 Experimental Setup for Measuring Thermal Contact Resistance between Two Die 127

Figure 6-13 Temperature Distributions at Top Surface, Finite Element Simulation (a) Top Die Heater Generating 1.18 W Power, (b) Bottom Die Heater Generating 0.6 W Power 129

Figure 6-14 (a) Measured Temperature Rise in Top Die Sensor Due to 0.38 W Power in Top Die (b) Measured Temperature Rise in Bottom Die Sensor Due to 0.6 W Power in Top Die 130

Figure 6-15 Geometry and Dimension of Copper Pillars Used to Make Attachment Between Two Die 132

Chapter 1

Introduction

Three-dimensional integrated circuits (3D IC) technology refers to the vertical integration of circuits on multiple semiconductor substrates [Banerjee et al., 2001; Patti et al., 2006]. By using 3D-integration, the system size reduced in comparison to traditional assembly based on 2D planar architecture [Beyne, 2006].

1.1 Fabrication Methods of 3D ICs

3D architectures created by vertical stacking can be developed by using different techniques which are die-on-die stacking, die-on-wafer stacking, wafer-on-wafer stacking, package-on-package and combination of multiple stacking techniques.

As illustrated in Figure 1.1(a), in die-on-die stacking technique vertical connection of die is made by using inter-die metal connections such as wire bonding, through silicon vias (TSV). Therefore this technique provides significant reduction in size and weight of the package [Lu 2009; Patti 2006].

Die-on-wafer stacking which is shown in Figure 1.1(b) ,attaches dissimilar die to wafer by using metal, oxide or adhesive bonding between die and host wafer which contain other circuits and components . Self –assembly techniques are also used for stacking wafer to wafer or chips to wafer by utilizing liquid surface tension. As illustrated in Figure 1.1(c), 5-10 μm silicon micro bumps are directly self-assembled on wafer and chip with similar pattern .Chips are located on wafer with 200nm accuracy and then attached to wafer by increasing temperature without applying any mechanical pressure [Fukushima et al., 2009].

As shown in Figure 1.1(d) wafer on wafer stacking is done by aligning, bonding and thinning the wafers. In this method metal to metal bonding and through-substrate vias (TSVs) are used for interconnects, inter-wafer routing and heat removal [Lu, 2009].

Because all the process is done at the wafer level before die separation, the interconnect density is better than other techniques [Patti, 2006].

Stacked system on wafer as illustrated in Figure 1.1(e) extend the wafer level packaging to the next level and integrate die, packages and stacked-dies on the system wafer [Tummala et al., 2009].

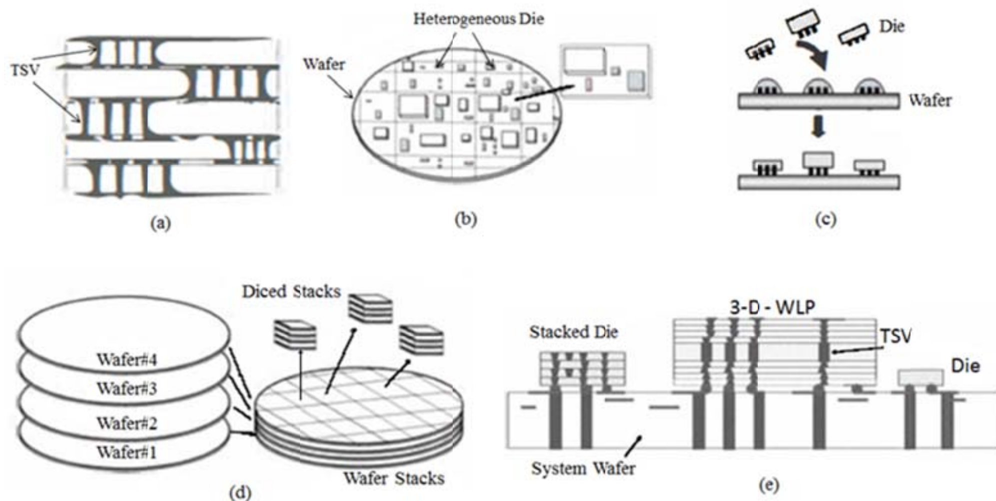


Figure 1.1 stacked die and wafer level integration [Lu *et al*.,2009;Tummala *et al*., 2009;Fukushima *et al*., 2009; Choudhury, 2010]: (a) Die-on-die, (b) Die-on-Wafer, (c) Self-assembly of die-on-wafer,(d) wafer-on-wafer,(e) Die,Stacked-die,3D-WLP on system wafer.

Package on package stacking technology is also used to integrate more IC functionalities in a cellular device printed circuit board (PCB) [Carson *et al*., 2009; Black, 2006].

1.2 Advantages of 3-D Packaging Technology

The following subsections discuss briefly the rule of 3-D packaging technology in enhancing system performance which cannot be achieved by using conventional packaging technologies [Said *et al*., 1998].

1.2.1 Size and Weight

By using 3-D packaging technology the system performance increases in comparison to conventional packaging technologies. By replacing 2D IC with 3D IC, size and weight reduce significantly. It has been reported that 40 to 50 times reduction in size and weight is achievable by using 3-D technology compared to two dimensional (2-D) packaging [Said *et al*., 1998].

1.2.2 Silicon Efficiency

The printed circuit board area occupied by the chip in packaging technology is defined as chip footprint [Ladd *et al*., 1993] which is very important in packaging technology (Shown in Figure 1.2).

Silicon efficiency is defined as the ratio of footprint area to the total substrate area .3-D technology results in more efficient use of silicon substrate area and enhances the silicon efficiency to 100% in comparison to 2-D packaging technology [Said *et al*., 1998].

1.2.3 Delay

Delay refers to the time a signal spends to travel between the functional circuit blocks in a system. In high speed systems, the time of travel of a signal along interconnect is called the time of flight and it is a key factor in delay time [Franzon *et al*., 1993]. The time of flight is dependent on interconnect length. As shown in Figure 1.3, by using 3-D packaging the interconnect length decrease therefore the delay also reduces.

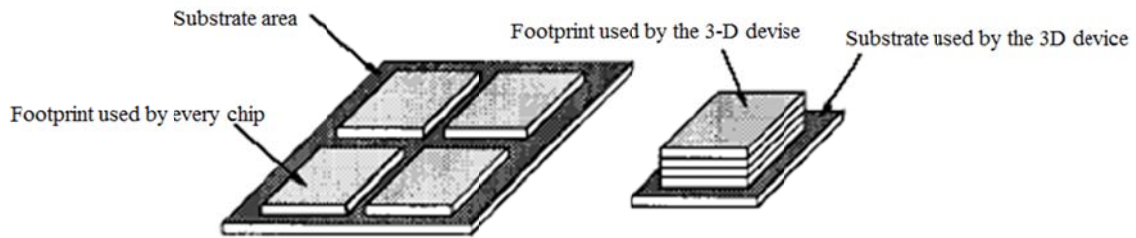


Figure 1.2 A graphical illustration of silicon efficiency between 2-D and 3-D technology [Said *et al*., 1998].

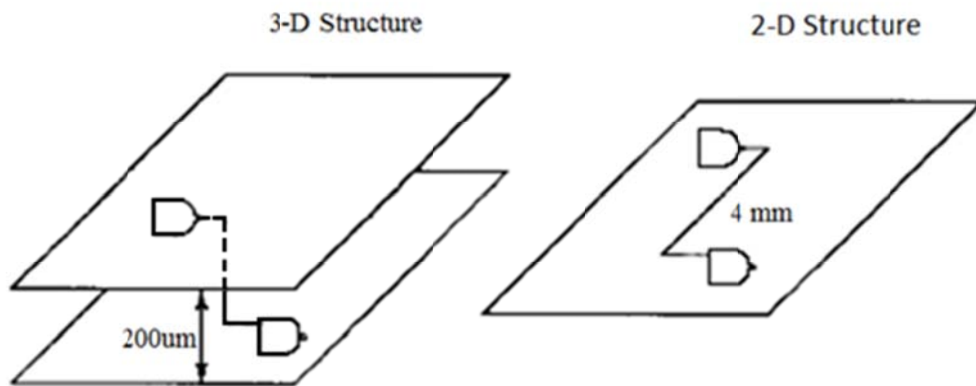


Figure 1.3 A comparison between the wiring lengths in 2-D and 3-D structure [Said *et al*., 1998].

1.2.4 Power Consumption

In an electronic system the energy dissipated, E, due to the interconnect parasitic capacitance, C, is given by, $E = CV^2$, and therefore the power consumption is $P = fCV^2$, where V is the voltage moving across the C and f is the number of transitions per second (frequency).The parasitic capacitance (*C)* is proportional to the interconnect length and it is decreased in 3-D packaging due to reduction in interconnect length that is why the power consumption is also decreased [Said *et al*., 1998].

1.2.5 Speed

Utilization of 3-D technology may allow the 3-D device to run at a faster rate of transitions per second (frequency) without any increase in power consumption. Furthermore, because of the reduction in parasitic, size and noise of a 3-D device the transition per second increase which enhance the overall system performance [Said *et al*., 1998].

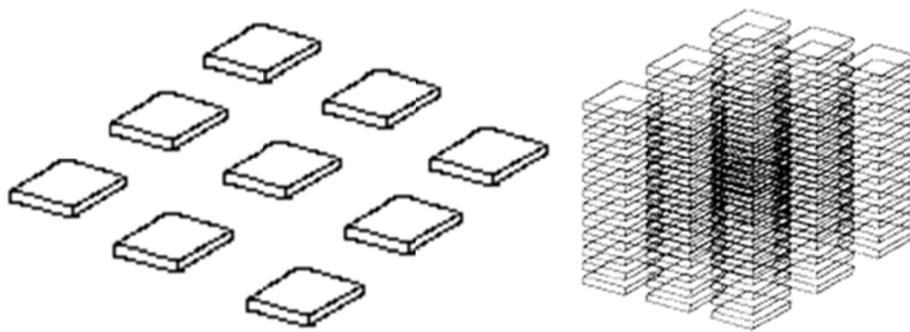


Figure 1.4 Accessibility and usability of interconnection in 2-D and 3-D packaging [Said *et al*., 1998].

1.2.6 Interconnect Usability and Accessibility

By using the same interconnect length the center element has access to eight neighbors in 2-D packaging technology while the 3-D packaging configuration provides access to 116 neighbors by assuming a typical thickness of 0.6 mm for every die [Sienski *et al*.,1996; Ackerman *et al*., 1996] as shown in Figure 1.4. Hence, 3-D packaging results in reduction in interconnect length which results in reduction of transmission delay between chips.

As illustrated in Figure 1.5 using vertical interconnection allows using maximum portion of the available interconnects in comparison to traditional packaging technologies. In 3-D packaging technology the accessibility depends on the type of vertical interconnection used and the density of available vertical interconnection [Turlik *et al*.,

1994; Doane *et al*., 1993]. In conventional 2-D packaging peripheral interconnections are used which the accessibility is limited to periphery length of the stack element while in 3-D packaging area interconnection provides the most usability and accessibility.

1.2.7 Bandwidth

In computing and communication systems, the interconnect bandwidth is a main performance limiting factor. The 3-D technology can be used to integrate a CPU and memory chips and decrease interconnect bandwidth [Said *et al*., 1998].

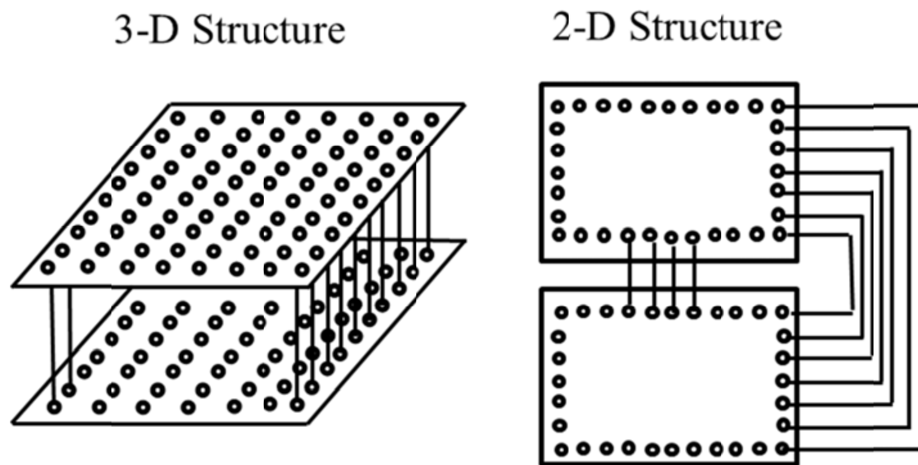


Figure 1.5 Possible numbers of interconnections in 3-D and 2-D structure [Said *et al*., 1998].

1.3 3D IC Design Methods

3D IC fabrication can be done by using different processing sequences. The simplest way to differentiate between different methods is by distinguishing between chip-level and wafer-level processing during the layering of key circuit components [Topol *et al*., 2006].

The process can be more specified by determining whether the face to face or face to back approach is used for layer stacking as shown in Figure 1.6. The details of

some common 3D assembling methods are presented in the next subsection [Topol *et al.*, 2006].

Higher density and smaller interlayer connection dimension are key process technology elements for optimizing 3D ICs. Chip to chip and chip to wafer methods have been used to achieve this goal. A wafer level stacking of 3D ICs is more cost-effective than the chip-stacking techniques and it increased design flexibility because key processing steps have not been developed at the die level [Topol *et al.*, 2006].

There are two principal design methods of 3D circuits: bottom up and top-down fabrication which are explained in the next subsection.

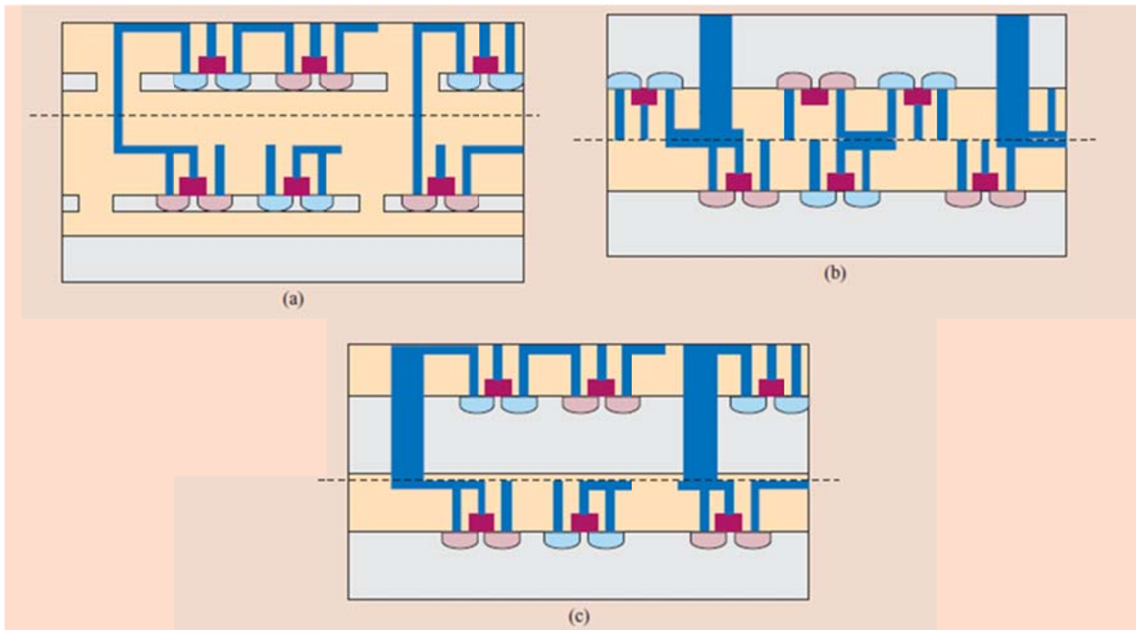


Figure 1.6 Schematic diagrams of assembled 3D IC structures; dashed line indicates bonded interface: (a) SOI-based face-to-back process with closely coupled layers, (b) face-to-face bonding, (c) face-to-back process [Topol *et al.*, 2004].

1.3.1 Bottom-Up Wafer-Scale Fabrication

In the bottom-up approach, the layering process is in a sequence and doesn't need wafer stacking. At first the bottom-most layer is created by using standard CMOS technology, then the second Si layer is formed and devices are fabricated on the second layer and additional layers are added on the top layer in a similar method.

The sequential layers are fabricated by using solid-phase crystallization and without additional wafer stacking. This method provides single-crystal silicon and improves device quality in comparison to other methods [Chan *et al*., 2001]. Thermal budget limitation and the performances in the underlying layers are some concerns of this method.

1.3.2 Top-Down Wafer-Scale Fabrication

In top-down method multiple 2D IC circuits are fabricated and then put together to make 3D IC [Guarini *et al*., 2009]. In this approach the performance of every layer is optimized and is verified functionally before stacking together. This method results in acceptable yield and lower manufacturing expenses. This is attractive when layers of dissimilar technologies are stacked. High quality, tight alignment tolerances, high process reliability and integrity of contacts between layers are challenges of this method [Guarini *et al*., 2009].

1.3.3 3D IC Stacking

As illustrated in Figure 1.6, 3D IC structures have been characterized according to the parts of the circuit design that are layered and depending on the 3D application a specific input/output (I/O) or interlayer via density is achievable.

The position of the top of the second layer after stacking with respect to the top of first layer defines the process as face-to face when two tops are facing each other and face-to-back if they are not. The face to face approach is using more for creating 3D ICs.

Generally these options are used to make chip to chip, wafer to wafer and chip to wafer 3D ICs.

By removing the Si substrate between layers, as depicted in Figure 1.6(a), the distance between device layers is minimized and bonding between layers is achievable by using an adhesive interlayer, and then interlayer electrical connections formed [Topol *et al*., 2004].

Face to face bonding option is shown in Figure 1.6(b) which is using for creating high density Cu-Cu bonded links between layers, however this method needs deep vias to bring signals out of the package.

The structure shown in Figure 1.6(c) has the lowest via density and the largest interlayer via dimensions [Cahill *et al*., 1995]. The choice of structure and fabrication method depends on the application of the 3-D IC technology.

1.4 Cooling Systems

Recently cooling of high heat flux systems such as computer microprocessors and memories have become very important because multitasking and faster computation increased by decreasing the package size. The heat flux is increasing to Kilowatt per centimeter-square in the new design of these systems, and this phenomenon has become the present trend in fabrication of 3D ICs [Phan *et al*., 2010].

Even though 3D ICs technology have major potential in reducing interconnect lengths and improving system performance, it has many thermal management challenges and removing heat from such architectures has been proven to be difficult. In order to keep the system temperature and also junction temperatures below the maximum temperature limit, several cooling systems have been developed. The designed cooling systems should be able to reduce the hotspot and junction temperatures.

Conventional cooling methods such as natural and forced convection have been studied which can reduce the junction temperature to around room temperature and has limitation in reducing temperature.

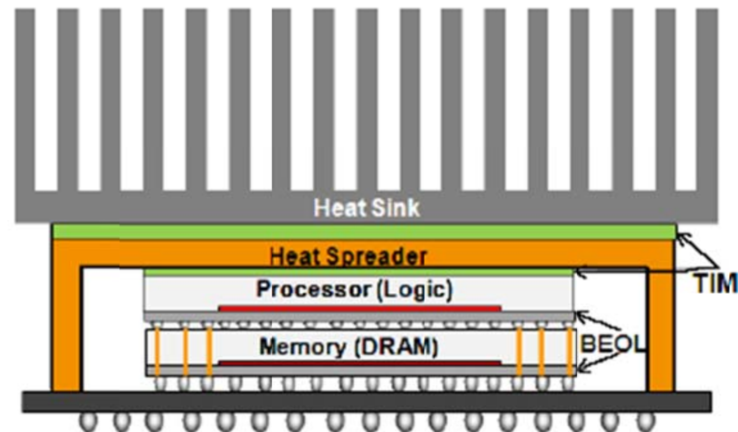


Figure 1.7 Conventional air cooling [King *et al*., 2010].

In the package shown in Figure 1.7 the processor chip which dissipates more power attaching at top of the memory and under the heat sink to be thermally more effective. Delivering the power to the processor is more challenging in this design because processor chip needs more I/O connections than memory chip and needs more TSVs through the memory chip to achieve the processor. This makes memory design and layout more difficult and consumes valuable memory chip area. By moving the memory chip to the top, fewer TSVs are needed in the processor chip because of the lower number of I/Os in memory chip. However, putting the processor on the bottom is not thermally efficient since the processor dissipates much more power than memory chips. In case of adding more memory chips the thermal resistance is increased between the bottom most layer and heat sink. It is limiting the number of chips are used to be

thermally advantageous. Another limitation of convection cooling is the limitation in decreasing the junction temperature which can be around room temperature [King *et al*., 2010].

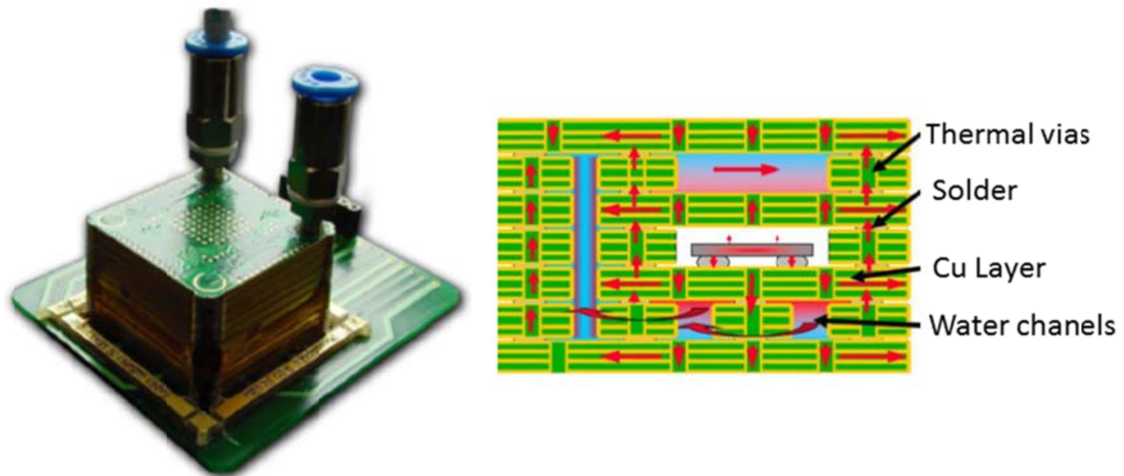


Figure 1.8 High-power liquid cooled 3D-PCB-packages (28 x 28 x 20 mm^3) [Schindler-Saefkow *et al*., 2006].

One of the biggest challenges in 3D ICs is dissipating heat from the center of the package to the environment [Schindler-Saefkow et al., 2006]. The fluid cooling has been used to optimally transfer generated heat inside the package through the thermal paths to the water channels or the environment. The design which is used in the study is shown in Figure 1.8. In the package the thermal vias are used for vertical heat dissipation and the metal layers are used for the horizontal heat dissipation. By having more heat exchanges with water, the package can be optimized more. By using water circulation in a high power 3D package to dissipate heat, having more layers of power components is possible. The utilized package and cooling system would however become complicated and expensive, and water leakage can be a big problem in electrical environment. In addition, these works are based on chip level thermal management and the sub-ambient

cooling of 3-D ICs by using solid-state cooling technologies have not been studied in these works [Schindler-Seafkow *et al*., 2006].

Solid state cooling such as thermoelectric or thermal diodes are also used in microelectronic thermal managements and it gives the possibility to achieve sub ambient temperature with precise control ability. Multidimensional Heat Transfer Systems (MHTS) have been studied to cool a 0.4W/mm^2 stack die to 7°C below ambient temperature by using four or more TEMs (Thermoelectric Module). When the die power and dimension grow vertically the MHTS is a workable solution. However, it is difficult to keep the system, structural stability and integrity for high vibration applications [Phan *et al*., 2010]**.**

In another study, an efficient lid has been designed for cooling stacked flip-chip 3D packages. In the assembly process TEM is placed between the top chip and the lid and also between the exposed area of the bottom chip and the lid. A Schematic of the pyramid lid which has been used for the experiment is shown in Figure 1.9.

By using TIM between the pyramid lid and bottom chip and making contact between them the thermal resistance decreases significantly in comparison to the standard lid 3D package. The thermal resistance at edge location decreases more in comparison to chip center and mid chip locations which decreases the temperature more. In the center and mid-chip locations the generated heat goes through the top chip and the lid and then to the environment while at the edge locations the heat directly goes to the lid through the TIM. By using this efficient lid design for 3D package the temperature reduces more in comparison to using standard lids. However designing a specific lid for different package architecture is difficult and expensive [Sikka *et al*., 2012].

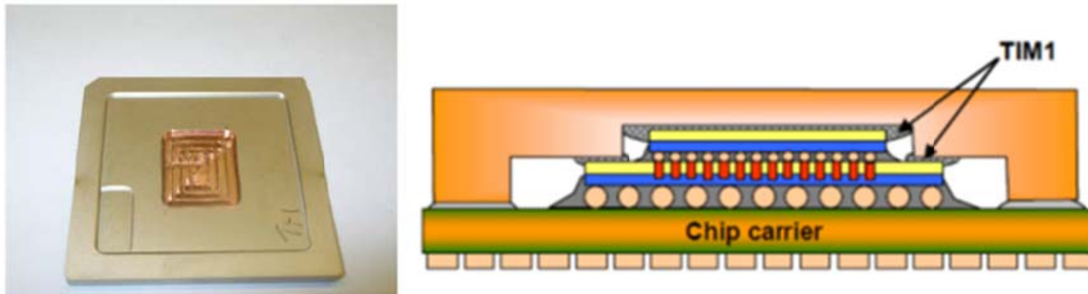


Figure 1.9 Schematic of a 3D package with an efficient pyramid lid [Sikka *at al.,* 2012].

Interlayer cooling in vertically integrated packages has been investigated experimentally. The chip stack with TSVs is embedded in a coolant with electrical feed-troughs and solder balls are attached to the chip. The coolant is pumped in between the individual dies. Water is used for cooling because of its superior thermo-physical properties and an isolated sealing of the electrical TSVs is needed to be done. Thin layer of solder rings used as both seal and low resistance electrical connection. The power generated on each die is transferred by conduction to the wiring layers and then to the coolant. Double side heater has been used for experiment and the most efficient structure for the top and bottom areas has been defined, and the results for best performing devices have also been discussed. At the end, the pressure gradient change and local heat transfer have been investigated for different designs of interconnects [Brunschwiler *et al*., 2009].

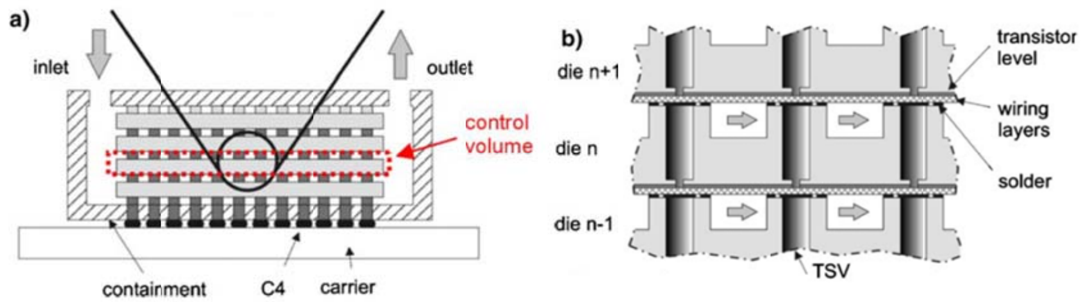


Figure 1.10 (a) Cross section through a chip stack with TSVs embedded in a fluid containment with electrical feed-through, (b) Detailed view of TSV, fluid channels, and solder connect [Brunschwiler *et al*., 2009].

Thermal analysis of a packaged DRAM on logic which is presented in Figure 1-11 has been considered and the effect of power generation in logic die on the temperature distribution of DRAM has been studied as well. The fabricated stack consists of a logic die and a DRAM die which is used for experiment and the simulation is done by using thermal Finite Element.

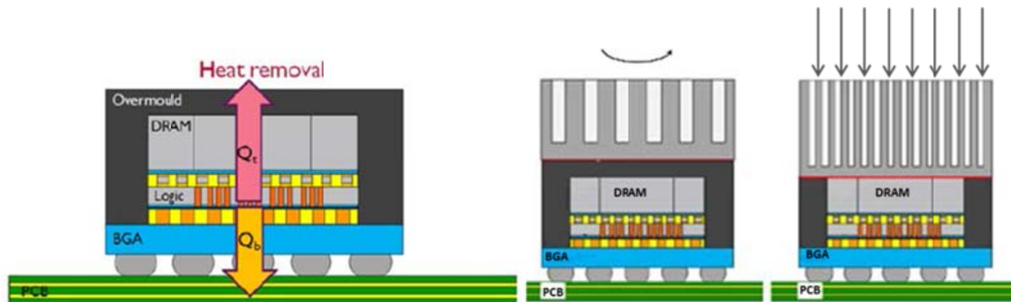


Figure 1.11 Schematic representations of three cooling configurations for DRAM on logic stack used for thermal analysis [Oprins *et al*., 2012].

At first, the effect of cooling from the top side of the package is investigated. The effect of generating heat in logic integrated hot spot heaters on the DRAM temperature rise is evaluated. The results show that temperatures rise in logic die is up to 7x higher than temperature rise in DRAM die. It is also observed that higher bump density reduces

logic temperature and increases DRAM temperature. In addition, a thermal finite element model is used to assess the thermal behavior of the package. In the case of medium and high power package configuration, most of the heat is removed through the heat sink on top of the package and this heat passes through the logic-DRAM interface. In the case of low power package applications, cooling through the PCB is sufficient and lower thermal resistance between the logic and DRAM improves spreading of heat from the logic die. In this case, DRAM is acting as an effective heat remover for logic die and prevents increasing temperature in both the logic and DRAM die. Furthermore, the simulation results for different die thickness conclude that the minimum die thickness of 50μm is required to deal with hot spots on the logic die [Oprins *et al*., 2012].

Copper multi-microchannel vapor venting heat exchanger has been designed and attached to a silicon thermal test chip. The hydraulic, thermal and venting performance improved in comparison to non-venting heat exchanger flow. The porous hydrophobic membrane is used to separate and transfer the vapor phase from two phase flow; as a result the pressure drop improves and the pumping power reduces [David *et al*., 2011].

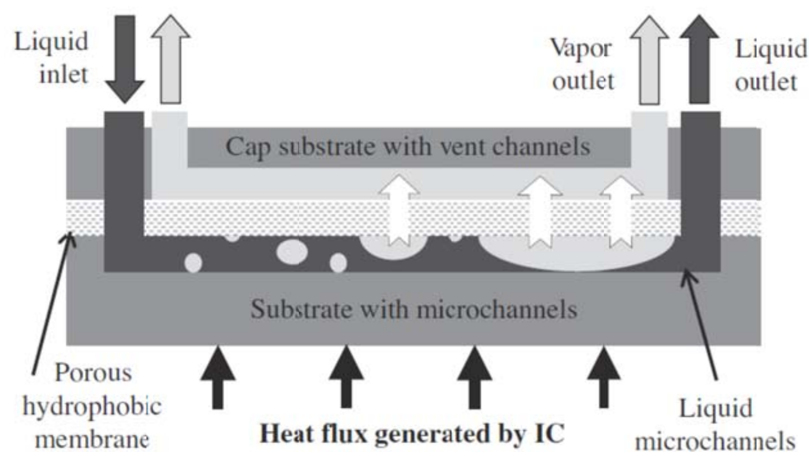


Figure 1.12 Schematic of a vapor venting heat exchanger [David *et al*., 2011].

1.5 Thermal Management of 3D ICs

According to Moor's law, the number of IC elements doubles every 18 mounts on a unit silicon area [Schaller. 1997]. While 3D ICs result in similar performance benefits as dimensional scaling without the associated cost, one of the main technological challenges in 3D IC technology is thermal management of a multi-die stack, particularly providing cooling for various substrates in the stack. In order to minimize the space, the thickness of chips decreases to some tens of microns and then they are attached to each other and to the substrate [Pinel *et al*., 2002]. While one side of a traditional 2D IC on a single substrate is typically available for heat removal; there is an inherent lack of direct contact with a heat sink for device layers in the middle of the stack. The utilization of through-substrate vias (TSVs) for cooling has been investigated widely [Sapatnekar *et al*., 2003; Cong *et al*., 2007].

Because of stacking several active devices vertically, the power density increase while the footprint area which is available for heat removal doesn't change in comparison to 2D architecture especially for the top most die which is located further from the heat sink and heat dissipation path is longer. Thus thermal management of 3D technology is recognized as an important issue [Das *et al*., 2004].

Some resent works on thermal analysis of 3D IC have been done [Skadron *et al*., 2004; Chiang *et al*., 2001; Im *et al*., 2000; Puttaswamy *et al*., 2006]. Numerical simulation has been studied to predict the temperature distribution in stacked die package by modeling each die for a given power distribution and then the superposition is done by using the introduced process in the paper [Joiner *et al*., 2009].

The steady state heat conduction model for a two-layer body based on solving the diffusion equations for every layer and corresponding boundary conditions is

proposed and the effect of first, second and third kind of boundary condition at one side of the body on temperature distribution is studied. In this work, the power distribution in every layer has not been considered and it only considered all the heat generation only at the end of the body and it is not an accurate assumption for 3-D ICs modeling because every active device and layer generate power [Haji-Sheikh *et al*., 2003].

In another study, the two-die layer model has been developed and the number of layers has been increased. The nonhomogeneous boundary conditions have been applied to the bottom and top most die and the compatibility boundary condition applied to interlayers. A recursive relation to find eigen coefficients and temperature distribution is derived and the results for three layer case is presented. In multilayer model the heat generation in every layer has not been considered, it is also time consuming to use the recursive equations for finding the coefficients of temperature distribution for higher number of layers [Rodrigo, 2008].

A thermal aware placement algorithm for 3D IC has been proposed [Yan *et al*., 2009]. An analytical model for temperature field distribution of a first level package with a nonuniform power map has been developed and compared with numerical simulation [Kaisare et al., 2009]. Thermal analysis has been done for a typical 3-D stack with hotspots and the effect of hot spot location and dimension on temperature distribution has been analyzed [Torregiani *et al*., 2009].

The design and placement of through silicon vias for thermal dissipation in 3D chips has been investigated in some studies [Cong et al., 2007; Goplen et al., 2006; Savidis et al., 2010]. A model for thermal analysis of complex 3D multi-processor system has been proposed and validated against experimental data of a silicon chip. The model has been utilized to evaluate the effect of TSVs in improving the thermal performance of the 3D system [Ayala *et al*., 2010].

In another research, thermal performance of 3D SiP with copper filled TSV has been performed numerically and the effect of chip thickness with different non-uniform heat source has been investigated. The results showed by increasing the number of stacked layers the maximum junction temperatures increased and as a result the allowable temperature limited the number of chips. In addition, the importance of chip thickness examined which showed by thinning the chip, the maximum junction temperature and thermal resistance increased [Lau *et al*., 2009].

An analytical solution for a 3D stacked system with volumetric heat generation has been proposed. The method is very general and applicable for different number of layers with different thermal properties, different internal heat generation rate and different boundary conditions. While the model is comprehensive, it is not applicable to real 3D stacked problems because in real problems the heat generation is happening at surface and it is not volumetric [Geer *et al*., 2009].

Because of the importance of having accurate and realistic analytical model, this dissertation emphasizes the analytical and experimental investigation of thermal management of 3D ICs.

1.6 Dissertation Organization

This dissertation discusses research developed for thermal management of 3D ICs. Analytical model to predict temperature distribution in vertically integrated three-dimensional integrated circuits with equally sized die, and unequally sized die and interposer based microelectronic systems have been studied. The model utilized to do thermal friendly predesign of 3D ICs. Experimental work toward investigating thermal behavior of a two die stack by applying different current to one die and studying the effect on the other die has been done. Steady state and transient measurement have been

done and a method is presented to measure thermal contact resistance between two die experimentally and calculate theoretically.

In chapter 2, an analytical solution for the three-dimensional temperature field in a 3D IC based on solution of the governing energy equations using Fourier series expansion for steady-state temperature fields is studied and compared well with finite-element simulation results [Choobineh *et al*., 2012]. Chapter 3 presents a heat transfer model for predicting the three-dimensional temperature field in a multi-die 3D IC with unequally-sized die and the model is used to compare the thermal performance of unequally-sized die stacks with a uniformly-sized die stack [Choobineh *et al*., 2013]. Chapter 4 describes an analytical model of heat transfer in interposer-based microelectronic systems and it is utilized to study the effect of various parameters on the temperature field in an interposer system. Chapter 5 outlines an explicit analytical model for rapid computation of temperature field in a three dimensional integrated circuit (3D IC).

Chapter 6 explained experimental measurement of the thermal performance of a two-die 3D integrated circuit and introduces a method to measure thermal contact resistance between two die.

Chapter 7 summarizes the thesis, the important contributions of this work explain and the future research based on the achievements of this work proposes.

Chapter 2

Analytical Solution for Steady-State and Transient Temperature Field in Vertically Integrated Three-Dimensional Integrated Circuits (3D ICS)

2.1 Introduction

Three-dimensional integrated circuits (3D IC) technology is a promising approach for next-generation semiconductor microelectronics [Banerjee et al., 2001; Patti, 2006; Loh et al., 2007]. By stacking multiple Silicon stratum and interconnecting circuits on different stratum using through-Silicon vias (TSVs) and metal micropads, it is possible to attain significant electrical performance benefits without resorting to the excessively expensive alternative of dimensional scaling [Patti, 2006]. For example, significant reduction in signal transmission delay and interconnection power in 3D ICs has been demonstrated compared to traditional SOCs [Alam et al., 2010; Savidis et al., 2010]. In addition, 3D IC technology enables compact integration of heterogeneous technologies and offers the exciting possibility of cost-effective manufacturing strategies such as differentiated technologies in various strata, reciprocal design symmetry, etc. [Alam et al., 2010]. 3D IC technology may also enable modular design and manufacturing of system components such as memory. Due to the promising benefits of the 3D IC technology, it is now an important component of ITRS projections.

Much of the research focus in this field in the past decade has been on development of manufacturing technologies underlying 3D ICs, such as etching and filling of deep vias, wafer thinning and thin wafer handling, etc. [Pozder at al., 2007; Morrow et al., 2006]. As these manufacturing technologies have become more and more mature, novel design methodologies are being investigated to take advantage of the unique features of 3D IC technology [Loh et al., 2007; Alam et al., 2010]. Thermal-electrical co-design is particularly important in 3D ICs due to the closely coupled nature of thermal and

electrical performance. A number of papers have proposed design methodologies to recognize thermal constraints during the electrical design process of 3D ICs [Jain et al., 2011; Goplen et al., 2003; Cong et al., 2004]. Reconciliation of thermal and electrical design objectives during block-level floorplanning has been shown to significantly improve both thermal and electrical performance [Jain et al., 2011]. It has been shown that meeting a mixed electrical-thermal objective during floorplanning results in a configuration that does not expend significant thermal or electrical penalties [Jain et al., 2011]. On the other hand, a purely electrical optimization approach leads to a design for which thermal management is extremely challenging. Methodologies for exploiting reciprocal design symmetry (RDS) for reducing peak temperature rise have also been proposed [Alam et al., 2010].

It is widely recognized that thermal management of 3D ICs is a major technological barrier in widespread implementation of this technology [Jain et al., 2010; Venkatari et al., 2011]. Stacking multiple silicon strata increases the power density without any enhancement in the footprint area available for heat removal. This problem is particularly exacerbated in the case of ultra-thin wafers where the heat sources in adjacent die may be within 50 μm of each other. The importance of thermal conduction through the micro pad bonding layer between adjacent die has been characterized [Jain et al., 2010]. The role of through-silicon vias (TSVs) for heat conduction away from local regions of high power density – often referred to as hotspots – has been analyzed [Cong et al., 2007; Goplen et al., 2006]. While TSVs present several technological challenges in terms of mechanical stress development around the TSV, reliability, etc. [Lu et al., 2009], it has also been recognized that optimal placement of TSVs may aid in thermal management of a 3D IC.

A number of recent papers have investigated a variety of thermal management approaches for 3D ICs. Liquid cooling of 3D ICs has been evaluated [King et al., 2010; Kim et al., 2010; Brunschwiler et al., 2009]. Unfilled TSVs have been proposed to be used as conduits for supplying a cooling fluid to the inter-die layers of 3D ICs. Thermoelectric cooling of 3D ICs has also been proposed [Phan et al., 2010]. While these novel approaches are quite promising, it is likely that they will be reserved only for very advanced applications such as high-performance computing. Thermal management of mainstream 3D ICs will need to be done through smart electrical-thermal co-design that minimizes the thermal dissipation problem at its root and does not require expensive system-level thermal management.

The problem of increased power density in 3D ICs was recognized quite early [Kleiner et al., 1995; Chiang et al., 2001], and a number of papers have investigated thermal management of 3D ICs in the recent past [Venkatari et al., 2011]. Analytical, one-dimensional heat flow models have been developed [Jain et al., 2010]. While these models are a good first step towards understanding the thermal performance of 3D ICs, they do not account for non-uniform heat generation, which is critical for accurate prediction of temperature fields in 3D ICs. Some analytical models for heat conduction in multilayer structures have also been developed [Geer et al., 2007; Haji-Sheikh et al., 2003]. An analytical model for temperature field distribution of a first level package with a nonuniform power map has been developed and compared with numerical simulation [Kaisare et al., 2009].These models do not fully capture the heat generation physics in 3D ICs. For example, in the work by Geer, et al. [Geer et al., 2007], power dissipation in a multilayer structure is modeled as volumetric heat generation which may not be an accurate model for 3D ICs. Models based on non-volumetric heat dissipation have also been proposed [Haji-Sheikh et al., 2003]. While these models are more comprehensive,

heat generation only at one end of the multi-die stack is accounted for, while inter-layer heat generation is not considered. Numerical simulations have been conducted for predicting the temperature field in 3D ICs [Puttaswamy et al., 2006]. While numerical simulations provide good results, they also suffer from several disadvantages. In the case of FEM-based numerical models, computational speed and interfacing with the electrical design flows are major concerns. Numerical models that are typically computed in stand-alone software are difficult to interface with traditional electrical design and analysis codes. Such interfacing is more easily achieved with analytical models that can be built into electrical design codes. Numerical models for 3D ICs also need to be validated against either experimental data or accurate analytical models. Development of analytical heat transfer models is thus highly desirable not only for reasons outlined above, but also for developing a good, basic understanding of the thermal management problem in 3D ICs.

This chapter develops analytical three-dimensional heat transfer models for 3D ICs. Both steady-state and transient models are presented. These models are based on Fourier series expansion and Laplace transforms respectively, and account for non-uniform heat generation at the device plane on each stratum in a multi-die 3D IC. Steady-state and transient temperature fields predicted by these models compare well with FEM-based simulation results. The analytical models presented here compute the temperature field faster than FEM-based methods. These models present the temperature field in closed-form equations with minimal iteration requirements. Thus, these models are easier to integrate with other electrical design simulations as compared to finite-element analysis, which are typically carried out in a separate software package. In addition, analytical models enable parametric analysis of the heat transport problem and aid in novel thermal design of 3D ICs. The next section outlines the analytical model for

determining the three-dimensional steady-state temperature field in a 3D IC with non-uniform heat generation in each die. The model is used to solve for the die temperatures in two-die and three-die 3D ICs for two different floorplans to illustrate the application of the model to a realistic problem. The subsequent section describes the transient model and discusses the results.

2.2 Steady-State Heat Conduction Model for a 3D IC

The geometry under consideration is shown in Figure 2.1. The die stack consists of N die, each of size a by b. Thickness of the ith die is ci. The orientation of the x and y axes are common to each die. A heat sink is attached to the bottom-most die. Heat transfer from the bottom-most die to the air, which typically occurs through a thermal interface material, heat spreader, heat sink and forced air cooling, is lumped together and modeled using a combined convective boundary condition, represented as h. For low-power applications where no heat sink is provided, the convective boundary condition models the heat dissipation through the electrical package. It is assumed that no heat loss occurs from the top-most die. All side surfaces are assumed to be adiabatic.

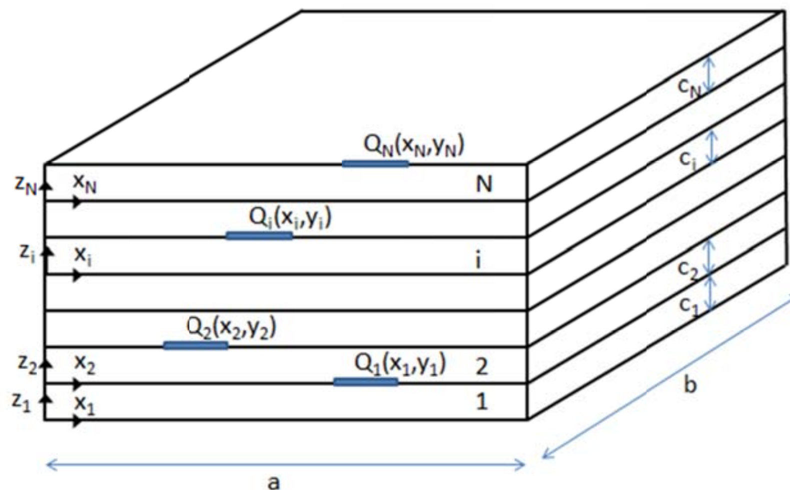


Figure 2.1 Schematic of the N-die 3D IC.

Let $Q_i(x,y)$ be the heat generation in the device plane at the top of the ith die. The primary interest is in determining the temperature fields $T_i(x,y,z_i)$. This analysis is greatly simplified by deriving the temperature field assuming that instead of all N heat sources, only the i^{*th} heat source $Q_{i^*}(x,y)$ is active. Since the governing energy equations are linear, the temperature field due to each active heat layer may be computed separately and then added linearly to provide the temperature field due to all N heat sources.

Let $T_{i,i^*}(x,y,z_i)$ be the steady-state temperature rise in the ith die due to heat generation $Q_{i^*}(x,y)$ in the i^{*th} die. For brevity of nomenclature, the subscript i^* is omitted henceforth, and the temperature field in this case is represented as $T_i(x,y,z_i)$. Each die is treated as a separate domain. Governing energy equations and boundary conditions are written and solved separately for each die. Some boundary conditions are based on requiring the temperature of adjacent die in the plane of intersection to be equal to each other. Let $q_i(x,y)$ be the heat flux entering the ith die at $z_i=c_i$. Let k_i be the thermal conductivity of the ith die. Let $T_{0i}(x,y)$ be the temperature profile at the intersecting plane between die i and $i-1$. Assuming constant thermal conductivity, each $T_i(x,y,z_i)$ satisfies the following governing steady state energy equation and adiabatic boundary conditions:

$$\frac{\partial^2 T_i}{\partial x^2} + \frac{\partial^2 T_i}{\partial y^2} + \frac{\partial^2 T_i}{\partial z_i^2} = 0 \qquad (1)$$

$$\frac{\partial T_i}{\partial x} = 0 \qquad \text{at } x=0,a \qquad (2)$$

$$\frac{\partial T_i}{\partial y} = 0 \qquad \text{at } y=0,b \qquad (3)$$

The z-direction boundary conditions for $T_i(x,y,z_i)$ are given as follows:

For $i=1$,

$$\frac{\partial T_1}{\partial z_1} = \frac{h}{k_1} T_1 \qquad \text{at} \quad z_1=0 \tag{4}$$

$$\frac{\partial T_1}{\partial z_1} = \frac{1}{k_1} q_1(x, y) \qquad \text{at} \quad z_1=c_1 \tag{5}$$

For $i=N$,

$$T_N = T_{0N}(x, y) \qquad \text{at} \quad z_N=0 \tag{6}$$

$$\frac{\partial T_N}{\partial z_N} = 0 \qquad \text{at} \quad z_N=c_N \tag{7}$$

For all other die,

$$T_i = T_{0i}(x, y) \qquad \text{at} \quad z_i=0 \tag{8}$$

$$\frac{\partial T_i}{\partial z_i} = u_i \cdot \frac{1}{k_i} q_i(x, y) \qquad \text{at} \quad z_i=c_i \tag{9}$$

where $u_i = \begin{vmatrix} 1 & i \le i^* \\ -1 & i > i^* \end{vmatrix}$

The term u_i accounts for the correct direction of heat flow below and above the heat source at the i^{*th} die.

The governing energy equations are solved by utilizing Fourier cosine series expansion [Carslaw *et al.*, 1986]. Briefly, the temperature field is written as a two-variable infinite series comprising of products of the eigenfunctions in the *x* and *y* directions. An extra term is added in order to account for the zeroth term of the Fourier cosine expansion. This zeroth-order term is selected in such a way that it satisfies the respective *z* boundary condition. Finally, the coefficients of the infinite series are determined by

using the non-homogeneous boundary condition and comparing the coefficients with corresponding coefficients in the two-variable Fourier cosine series expansion of the non-homogeneous term. When two non-homogeneous boundary conditions are encountered, the temperature field is split into two parts, each containing only one non-homogeneous boundary condition. The two problems are then solved separately and solutions combined linearly to obtain the solution for the original problem. The temperature fields are determined to be as follows:

For $i=1$,

$$T_1(x,y,z_1) = c_{1,0}\left(z_1 + \frac{k_1}{h}\right) + \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} c_{1,nm}\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)\left[\cosh(\gamma_{nm}z) + \frac{h}{k_1\gamma_{nm}}\sinh(\gamma_{nm}z)\right] \quad (10)$$

where $\gamma_{nm} = \sqrt{\left(\frac{n\pi}{a}\right)^2 + \left(\frac{m\pi}{b}\right)^2}$

To do so, the Fourier cosine series expansions of heat flux $q_1(x,y)$ is first written as follows

$$q_1(x,y) = b_{1,0} + \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} b_{1,nm}\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right) \quad (11)$$

where the coefficients $b_{1,0}$ and $b_{1,nm}$ may be determined as

$$b_{1,0} = \frac{1}{ab}\int_0^b\int_0^a q_1(x,y)\,dx\,dy \quad (12)$$

where

$$b_{1,nm} = \begin{cases} \dfrac{2}{ab} \displaystyle\int_{y=0}^{b} \int_{x=0}^{a} q_1(x,y) \cos\left(\frac{n\pi x}{a}\right) dxdy & n \neq 0; m = 0 \\ \dfrac{2}{ab} \displaystyle\int_{y=0}^{b} \int_{x=0}^{a} q_1(x,y) \cos\left(\frac{m\pi y}{b}\right) dxdy & n = 0; m \neq 0 \\ \dfrac{4}{ab} \displaystyle\int_{y=0}^{b} \int_{x=0}^{a} q_1(x,y) \cos\left(\frac{n\pi x}{a}\right) \cos\left(\frac{m\pi y}{b}\right) dxdy & n \neq 0; m \neq 0 \end{cases} \tag{13}$$

By applying the non-homogeneous z-direction boundary condition of die1, equation (5), the coefficients $c_{1,0}$ and $c_{1,nm}$ in equation (10) are given by

$$c_{1,0} = \frac{1}{abk_1} \int_{y=0}^{b} \int_{x=0}^{a} q_1(x,y) dxdy \tag{14}$$

$$c_{1,nm} = \begin{cases} \dfrac{2}{abk_1 P_{nm}} \displaystyle\int_{y=0}^{b} \int_{x=0}^{a} q_1(x,y) \cos\left(\frac{n\pi x}{a}\right) dxdy & n \neq 0; m = 0 \\ \dfrac{2}{abk_1 P_{nm}} \displaystyle\int_{y=0}^{b} \int_{x=0}^{a} q_1(x,y) \cos\left(\frac{m\pi y}{b}\right) dxdy & n = 0; m \neq 0 \\ \dfrac{4}{abk_1 P_{nm}} \displaystyle\int_{y=0}^{b} \int_{x=0}^{a} q_1(x,y) \cos\left(\frac{n\pi x}{a}\right) \cos\left(\frac{m\pi y}{b}\right) dxdy & n \neq 0; m \neq 0 \end{cases} \tag{15}$$

where $P_{nm} = \gamma_{nm} \sinh(\gamma_{nm} c_1) + \dfrac{h}{k_1} \cosh(\gamma_{nm} c_1)$

For $i=N$,

$$T_N(x,y,z_N) = c_{Nb,0} + \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} c_{Nb,nm} \cos\left(\frac{n\pi x}{a}\right) \cos\left(\frac{m\pi y}{b}\right) \cosh\left(\gamma_{nm}(c_N - z_N)\right) \tag{16}$$

In order to find coefficients in equation (16), the Fourier cosine series expansions of temperature distribution $T_{0N}(x,y)$ are first written as follows

$$T_{0N}(x,y) = b_{N,0} + \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} b_{N,nm}\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right) \tag{17}$$

where the coefficients $b_{N,0}$ and $b_{N,nm}$ may be determined as

$$b_{N,0} = \frac{1}{ab}\int_0^b\int_0^a T_{0N}(x,y)dxdy \tag{18}$$

where

$$b_{N,nm} = \begin{cases} \dfrac{2}{ab}\displaystyle\int_{y=0}^{b}\int_{x=0}^{a} T_{0N}(x,y)\cos\left(\frac{n\pi x}{a}\right)dxdy & n \neq 0; m = 0 \\ \dfrac{2}{ab}\displaystyle\int_{y=0}^{b}\int_{x=0}^{a} T_{0N}(x,y)\cos\left(\frac{m\pi y}{b}\right)dxdy & n = 0; m \neq 0 \\ \dfrac{4}{ab}\displaystyle\int_{y=0}^{b}\int_{x=0}^{a} T_{0N}(x,y)\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)dxdy & n \neq 0; m \neq 0 \end{cases} \tag{19}$$

By applying the non-homogeneous z-direction boundary condition of the Nth die, equation (6), the expressions for coefficients $c_{Nb,0}$ and $c_{Nb,nm}$ are given by

$$c_{Nb,0} = \frac{1}{ab}\int_{y=0}^{b}\int_{x=0}^{a} T_{0N}(x,y)dxdy \tag{20}$$

$$c_{Nbnm} = \begin{cases} \dfrac{2}{ab\cosh(\gamma_{nm}c_N)}\displaystyle\int_{y_N=0}^{b}\int_{x_N=0}^{a} T_{0N}(x,y)\cos\left(\frac{n\pi x}{a}\right)dxdy & n \neq 0; m = 0 \\ \dfrac{2}{ab\cosh(\gamma_{nm}c_N)}\displaystyle\int_{y_N=0}^{b}\int_{x_N=0}^{a} T_{0N}(x,y)\cos\left(\frac{m\pi y}{b}\right)dxdy & n = 0; m \neq 0 \\ \dfrac{4}{ab\cosh(\gamma_{nm}c_N)}\displaystyle\int_{y_N=0}^{b}\int_{x_N=0}^{a} T_{0N}(x,y)\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)dxdy & n \neq 0; m \neq 0 \end{cases} \tag{21}$$

For $i \neq 1$ and $i \neq N$,

$$T_i(x,y,z_i) = \begin{array}{c} c_{iA,0} z_i + \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} c_{iA,nm} \cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)\sinh(\gamma_{nm} z_i) + \\ c_{iB,0} + \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} c_{iB,nm} \cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)\cosh(\gamma_{nm}(c_i - z_i)) \end{array} \tag{22}$$

The coefficients $c_{iA,0}$ and $c_{iA,nm}$ for equation (16) are given by

$$c_{iA,0} = \frac{1}{abk_i}\int_{y=0}^{b}\int_{x=0}^{a} u_i \cdot q_i(x,y)\,dxdy \tag{23}$$

$$c_{iA,nm} = \left| \begin{array}{ll} \frac{2u_i}{abk_i\gamma_{nm}\cosh(\gamma_{nm}c_i)}\int_{y=0}^{b}\int_{x=0}^{a} q_i(x,y)\cos\left(\frac{n\pi x_i}{a}\right)dxdy & n \neq 0; m = 0 \\ \frac{2u_i}{abk_i\gamma_{nm}\cosh(\gamma_{nm}c_i)}\int_{y=0}^{b}\int_{x=0}^{a} q_i(x,y)\cos\left(\frac{m\pi y}{b}\right)dxdy & n = 0; m \neq 0 \\ \frac{4u_i}{abk_i\gamma_{nm}\cosh(\gamma_{nm}c_i)}\int_{y=0}^{b}\int_{x=0}^{a} q_i(x,y)\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)dxdy & n \neq 0; m \neq 0 \end{array} \right. \tag{24}$$

The coefficients $c_{iB,0}$ and $c_{iB,nm}$ for equation (16) are given by

$$c_{iB,0} = \frac{1}{ab}\int_{y=0}^{b}\int_{x=0}^{a} T_{0i}(x,y)\,dxdy \tag{25}$$

$$c_{iB,nm} = \left| \begin{array}{ll} \frac{2}{ab\cosh(\gamma_{nm}c_i)}\int_{y_1=0}^{b}\int_{x_1=0}^{a} T_{0i}(x,y)\cos\left(\frac{n\pi x}{a}\right)dxdy & n \neq 0; m = 0 \\ \frac{2}{ab\cosh(\gamma_{nm}c_i)}\int_{y=0}^{b}\int_{x=0}^{a} T_{0i}(x,y)\cos\left(\frac{m\pi y}{b}\right)dxdy & n = 0; m \neq 0 \\ \frac{4}{ab\cosh(\gamma_{nm}c_i)}\int_{y=0}^{b}\int_{x=0}^{a} T_{0i}(x,y)\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)dxdy & n \neq 0; m \neq 0 \end{array} \right. \tag{26}$$

Note that the heat fluxes q_i and intersecting temperatures T_{0i} are unknown, but may be determined once temperature fields have been computed, using heat flux conservation and temperature matching at the interface between adjacent die. It is thus possible to employ an iterative approach to solve for the temperature fields by initially guessing the heat fluxes q_i. The procedure is as follows:

1. Assume only one of the $Qi(x,y)$, $i=1,2,\ldots,N$ is active.
2. Assume a value for the heat fluxes $q_i(x,y)$ for each die $i=1,2..,N-1$.
3. Solve for $T_1(x,y,z_1)$ from equation (10). Determine the interface temperature field between die 1 and die 2, $T_{02}(x,y)=T_1(x,y,z_1=c_1)$.
4. Using T_{02} and the assumed value of q_2, Solve for $T_2(x,y,z_2)$ from equation (22). Determine $T_{03}=T_2(x,y,z_2=c_2)$.
5. Repeat step 3 for each die from $i=2$ to $i=N-1$, until $T_{N-1}(x,y,z_{N-1})$ is determined and is used to determine the interface temperature field $T_{0N}(x,y,z_N)$.
6. Determine $T_N(x,y,z_N)$ from equation (16).
7. Once all temperature fields have been computed, calculate the heat fluxes q_i:

$$q_{i,new}(x,y) = \begin{vmatrix} u_i k_i \dfrac{\partial T_{i+1}}{\partial z_{i+1}} & i \neq i^* \\ Q_i^* - k_i \dfrac{\partial T_{i+1}}{\partial z_{i+1}} & i = i^* \end{vmatrix} \tag{27}$$

8. Update the heat fluxes and repeat steps 2 through 6 until the change in the temperature fields between successive iterations is sufficiently small.

$$q_i(x,y) = wq_i(x,y) + (1-w)q_{i,new}(x,y) \tag{28}$$

9. Repeat steps 2 to 8 for next *Qi(x,y).* Once the temperature fields resulting from all *Qi(x,y)* determined, add them linearly to achieve the final temperature distribution for every die.

The analytical model is implemented by considering up to N_t terms in each double integral. Double integrals are evaluated using a two-dimensional Gauss quadrature [Hamming *et al*., 1986]. Using this approach, the temperature field for a two-die stack and a three-die stack are computed and compared with finite-element based simulations. For these simulations, each die is assumed to be 10mm by 10mm with 0.5mm Silicon thickness. For the two-die case, each die is assumed to have a hotspot dissipating 10W over a 1mm by 1mm area centered at (2.5mm, 2.5mm) for die1 and (7.5mm, 7.5mm) for die2. The three-die case considers 10W hotspots at (2.5mm, 2.5mm), (5.0mm, 5.0mm) and (7.5mm, 7.5mm) for die1, die2 and die3 respectively. A convective heat transfer coefficient value representative of typical forced air cooling based thermal management is assumed for each case.

Figure 2-2 shows a plot of N_t versus the temperature solution obtained at the center of the hotspot in die1 in the three-die case. The resulting temperature is plotted as a fraction of the temperature if 1000 terms are used in the double summations in equations (10), (13), and (16). Figure 2.2 shows that around 25 terms are sufficient to reach within 1% of the temperature predicted by 1000 terms. This results in significant savings in computation time without sacrificing the quality of the computed result.

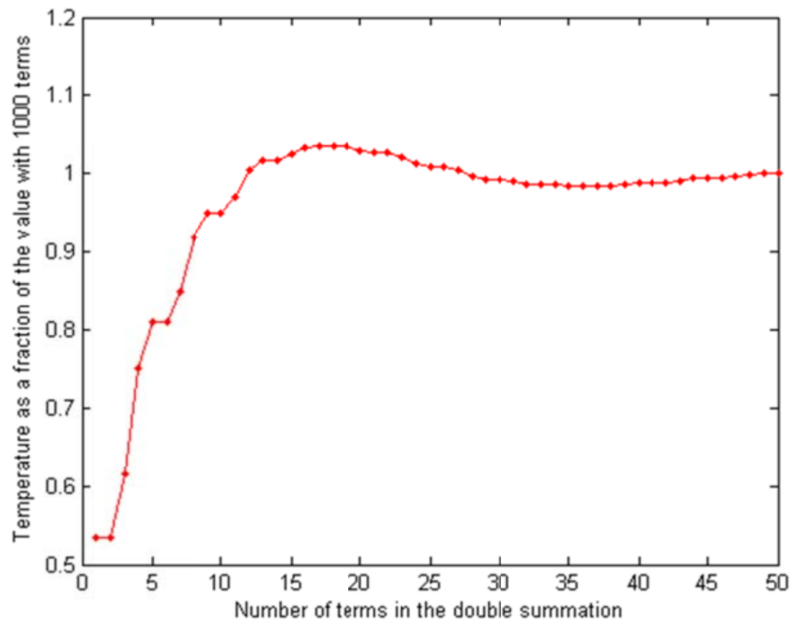


Figure 2.2 Plot showing the accuracy of the hotspot temperature computation as a function of the number of terms considered in equations (10), (16) and (22).

Figure 2.3 shows a plot of the temperature curve along the x-direction at y=2.5mm for the device plane in die1 for the three-die case at successive iterations. This plot shows that the temperature solution stabilizes within ±0.5 °C within around 7 iterations. Thus, a relatively small number of iterations are found to be sufficient for engineering accuracy.

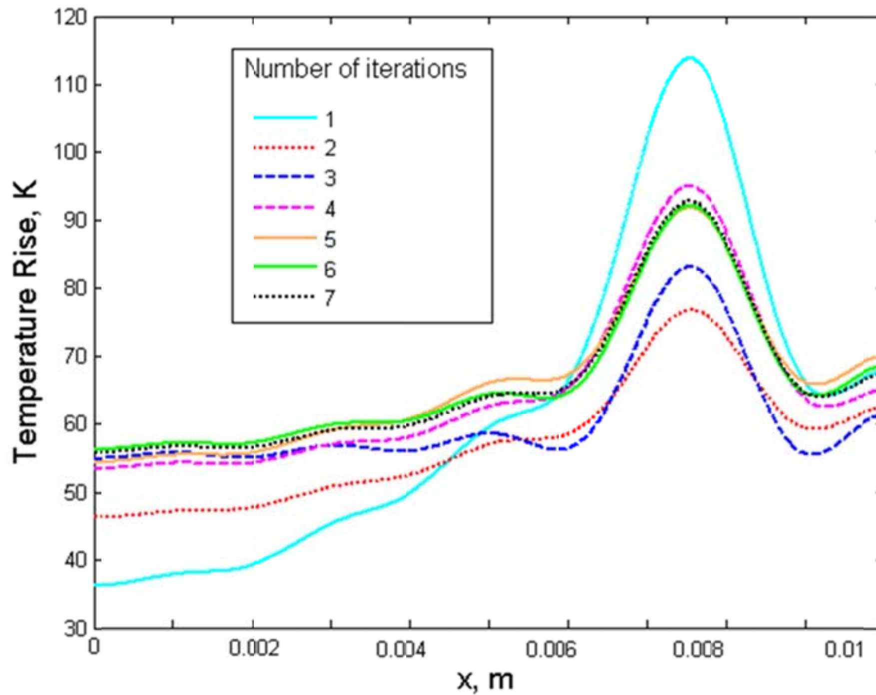
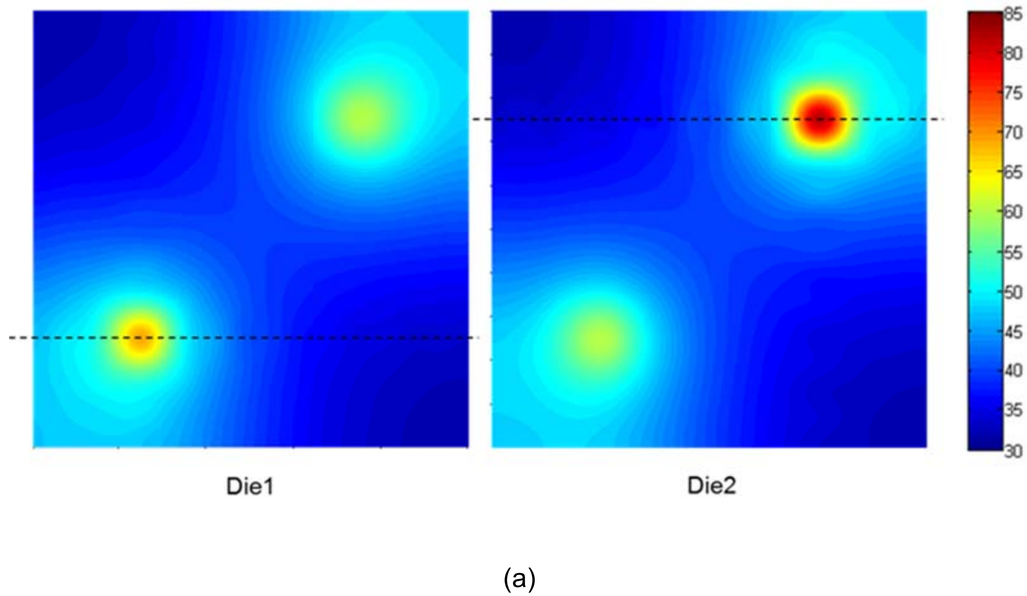


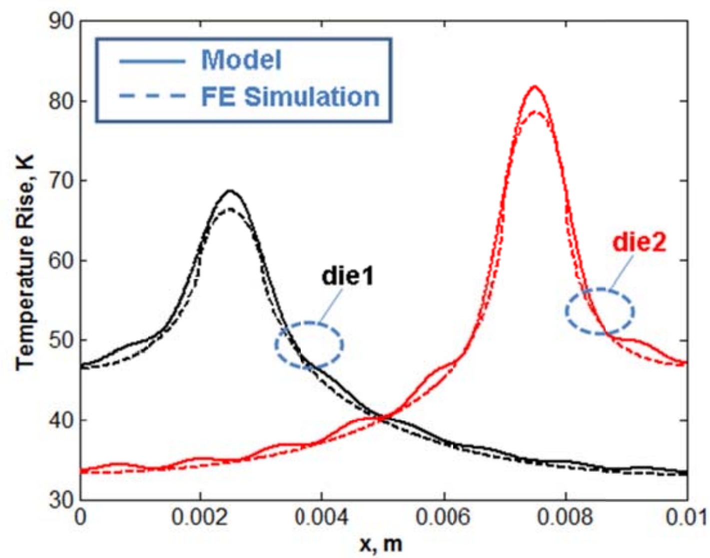
Figure 2.3 Plot showing the temperature profile across the hotspot on die1 as a function of the number of iterations carried out.

Figure 2.4(a) shows the temperature fields on die1 and die2 for the two-die case computed using the analytical model. Figure 2.4(b) shows a temperature curve along the x-direction at y=2.5mm and y=7.5mm for die1 and die2 respectively. Results are compared with finite-element simulation results, also shown in Figure 2.4(b). These simulations are carried out in a finite-element software package. Mesh refinement is carried out to rule out mesh dependency of the results. Temperature profiles from the analytical model and finite-element simulation results have similar shapes. Good agreement between the analytical model and Finite Element simulation results is observed, with the maximum deviation between the two being around 4%. There is some waviness in the analytical solution as a result of representing the solution as a sum of

cosine terms. This is observed to be reduced as the number of terms in the solutions is increased.



(a)

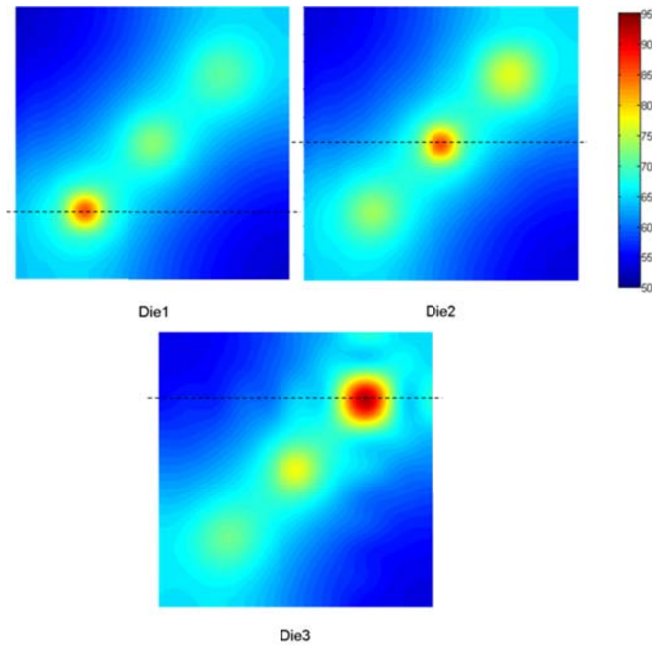


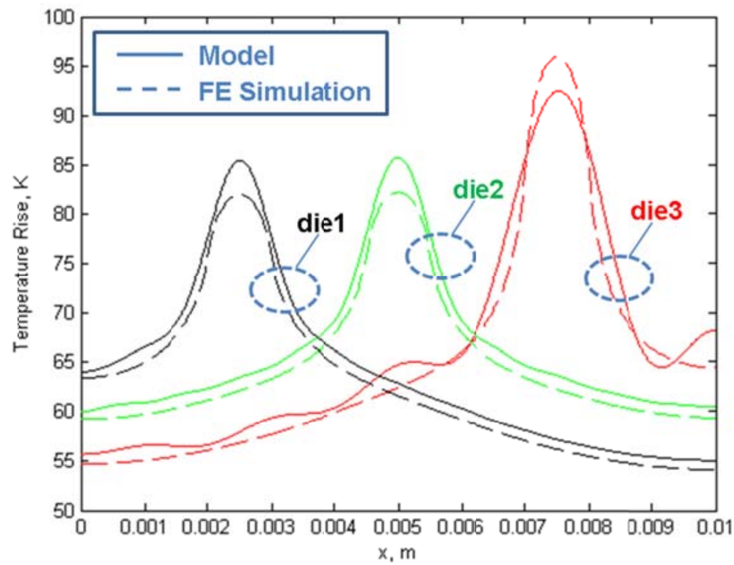
(b)

Figure 2.4 (a) Computed temperature field for the two-die 3D IC, (b) Cross-section temperature curve comparing the model with finite-element simulations.

Figure 2.5(a) shows the temperature fields on die1, die2 and die3 for the three-die case computed using the analytical model. Figure 2.5(b) plots the temperature curves along the x-direction at y=2.5mm, y=5.0mm and y=7.5mm for die1, die2 and die3 respectively.

Similar to the two-die case, comparison with finite-element simulation results show excellent agreement, within 4% of each other. The deviation between the two is found to be further reduced by increasing the number of elements in the finite-element simulation or by employing finer domain discretization for calculating the double integrals for the analytical models. This shows the capability of the analytical model to compute temperature fields for 3D ICs comprising of more than two die. While the current research attention is mostly focused on two-die stacks, it is expected that this will lead to 3D ICs with vertical integration of more than two die.





(b)

Figure 2.5 (a) Computed temperature field for the three-die case, (b) Cross-section temperature profiles compared with finite-element simulations.

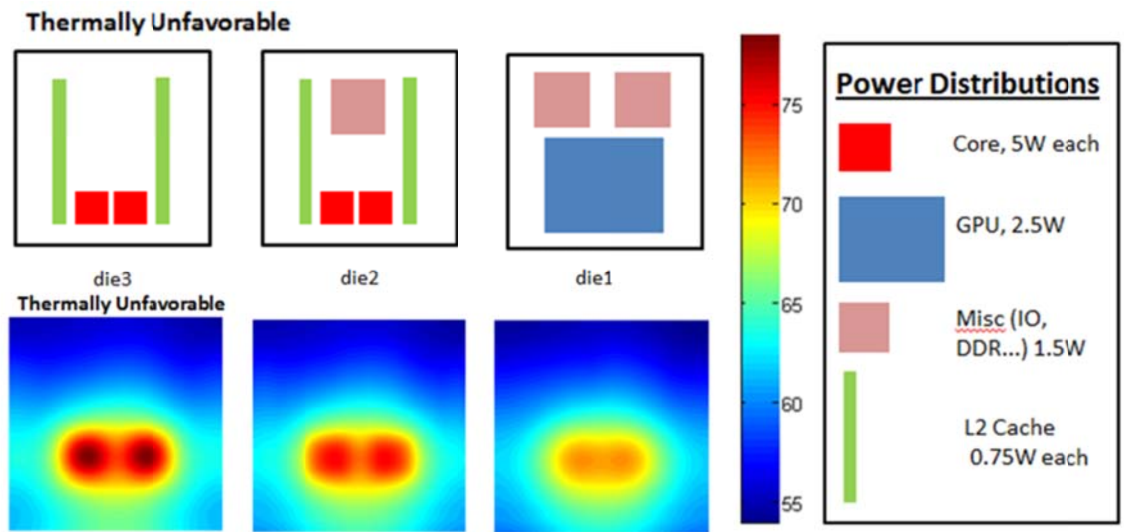
The next section illustrates the use of the steady-state analytical model to understand thermal optimization of the block-level floorplanning process [Sarrafzadeh *et al*., 1996]. It is shown that the analytical model may be used for temperature computation for block-level floorplans during the electrical design process of 3D ICs. Significant reduction in steady-state temperature may be obtained by thermal-friendly placement of heat dissipating blocks in a multi-die stack.

2.3 Application of Analytical Model to Understand Thermal-Friendly Floorplanning

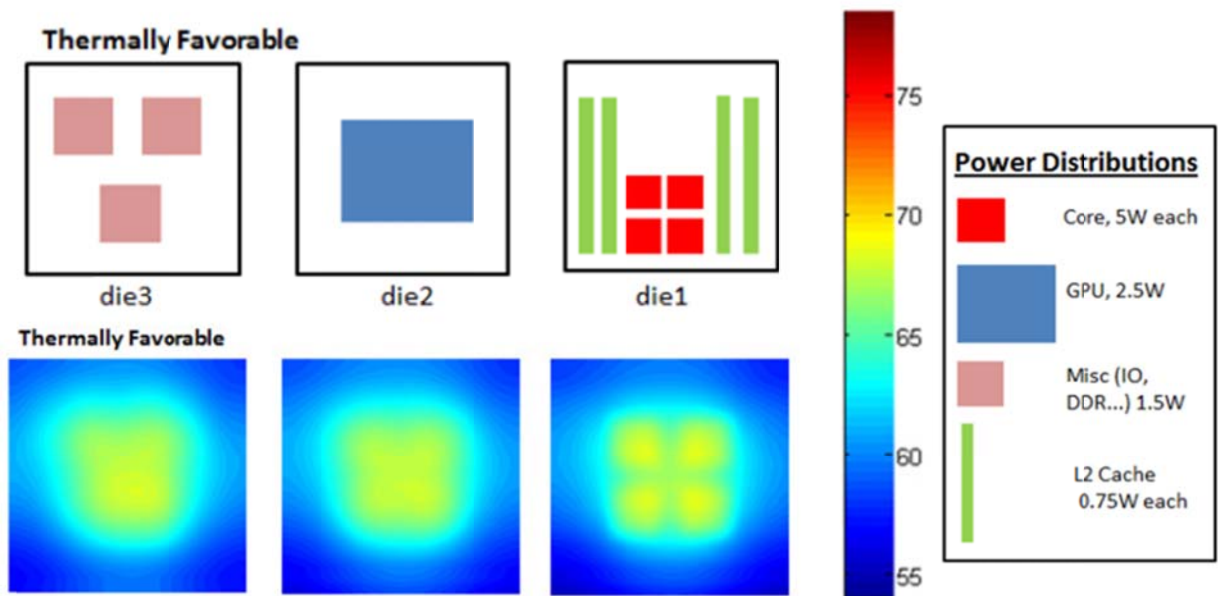
A primary advantage of analytically derived expressions for the temperature distribution in a 3D IC over finite-element simulations is the capability of being incorporated in the chip design flow with other electrical design considerations. Finite-element simulations are usually executed in separate software which makes it difficult to interface with an independent electrical design flow. On the other hand, the analytical models in section 2.2 can easily be made a part of the principal electrical design process of the 3D IC. This could be done, for example, by coding and compiling the temperature field equations derived in section 2.2 in a higher-level language such as C++. The resulting executable can be integrated much more easily with electronic design tools such as Verilog, SPICE, etc. Exchange of input and output parameters between the two could be utilized to make temperature computation an inherent part of each design iteration.

In this section, block-level floorplanning and 3D IC temperature computation using the models presented in section 2.2 is considered. The models presented in this work are used for rapid temperature field computation to aid thermal-friendly re-arrangement of the floorplan which results in significant reduction in peak temperature. This section considers a three-die stack for a four-core APU that integrates core compute

and graphics processing capabilities. The various blocks and their assumed power distributions are shown in Figure 2.6(a). Blocks placed in the remaining space are assumed to dissipate small enough power density to be considered thermally insignificant. Two possible floorplans are considered. The first floorplan places cores in die2 and die3, and the GPU unit in die1. The computed temperature field is shown in Figure 2.6(b). It is clear that in this case, the close proximity of cores on die2 and die3 leads to a large local power density, and thus a large temperature rise. When the floorplan is redesigned to be more thermal-friendly by moving the cores to die1 – the die closest to the heat sink – and by avoiding spatial overlap between the cores, around 13% reduction in peak temperature is observed. While case (2) is not necessarily thermally optimal, it illustrates the process in which the models presented in this work could be used for thermal design optimization of a 3D IC. A general design optimization needs to consider not only thermal effects but also a variety of other factors, including electrical performance, manufacturability, etc. By providing an analytical method for temperature computation, the current work contributes towards effective and optimal design of 3D ICs.



(a)



(b)

Figure 2.6 (a) Schematic showing the floorplan and temperature plot for thermally unfavorable case, (b) floorplan and temperature plot for thermally favorable case.

2.4 Transient Heat Conduction Model for a 3D IC

The transient governing energy equations for temperature fields in each die contains an extra transient term in the governing partial differential equation (PDE).

$$\frac{\partial^2 T_i}{\partial x_i^2} + \frac{\partial^2 T_i}{\partial y_i^2} + \frac{\partial^2 T_i}{\partial z_i^2} = \frac{1}{\alpha_i} \frac{\partial T_i}{\partial t} \tag{29}$$

where α_i is the thermal diffusivity of the material of the ith stratum.

Spatial boundary conditions remain the same as in equations (2) through (9), except that the heat generation terms Q_i are now time-dependent in general. It is assumed that the temperature field is zero at $t=0$.

This transient heat conduction problem may be solved by combining the approach in section 2.2 with Laplace transforms. Briefly, the Laplace transform is utilized to convert time-dependent PDE and boundary conditions for each $T_i(x,y,z_i,t)$ into time-independent PDE and boundary conditions in corresponding Laplacian fields $\overline{T_i}(x, y, z_i)$. The resulting PDEs and boundary conditions are similar in nature to ones presented in section 2.2 and are solved iteratively to determine $\overline{T_i}(x, y, z_i)$. Inverse Laplace transforms are computed numerically to determine the time-dependent temperature fields $T_i(x,y,z_i,t)$ from the computed Laplacian fields $\overline{T_i}(x, y, z_i)$. The de Hoog's quotient difference method algorithm [deHoog *et al*., 1982] as implemented by Hollenbeck [Hollenbeck *et al*., 2012] is utilized for the numerical inversion. This procedure is illustrated using a two-die stack as follows:

Assume a two-die stack with nomenclature similar to section 2.2. The two-die stack is shown in Figure 2.7. Note the orientation of the z_2 axis is taken to be downward since this choice enables a more compact form of the solution. The heat sources $Q_1(x,y,t)$

and $Q_2(x,y,t)$ are assumed on the two die. Similar to the treatment in section 2.2, the temperature distributions $T_1(x,y,z_1,t)$ and $T_2(x,y,z_2,t)$ are split into contributions from $Q_1(x,y,t)$ alone and $Q_2(x,y,t)$ alone, and superimposed for obtaining the final solution.

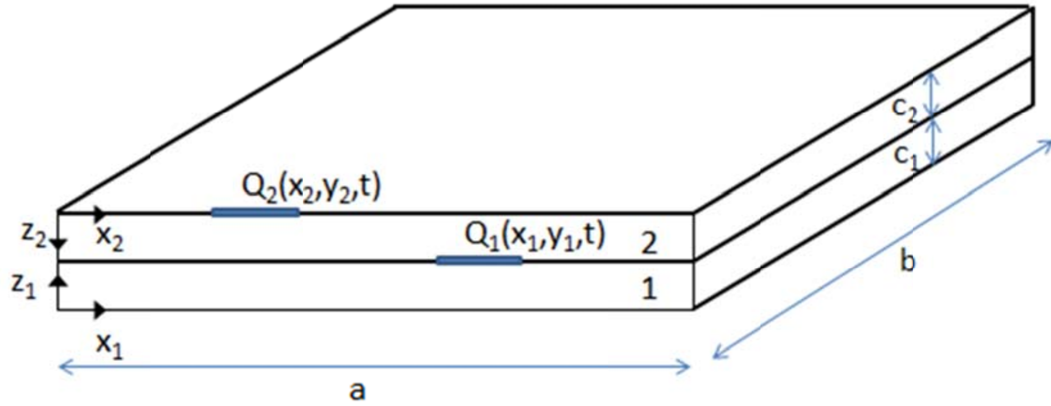


Figure 2.7 Schematic of the two-die stack for transient temperature field computation.

For the contributions from $Q_1(x,y,t)$ alone, the governing energy equations after applying Laplace transform for $i=1, 2$ are

$$\frac{\partial^2 \overline{T}_i}{\partial x^2}+\frac{\partial^2 \overline{T}_i}{\partial y^2}+\frac{\partial^2 \overline{T}_i}{\partial z_i^2}=\frac{p}{\alpha_i}\overline{T}_i \tag{30}$$

$$\frac{\partial \overline{T}_i}{\partial x}=0 \qquad \text{at } x=0,\ a \tag{31}$$

$$\frac{\partial \overline{T}_i}{\partial y}=0 \qquad \text{at } y=0,\ b \tag{32}$$

$$\left.\frac{\partial \overline{T}_1}{\partial z_1}\right|_{z_1=0}=\frac{h}{k_1}\overline{T}_1\Big|_{z_1=0};\quad \left.\frac{\partial \overline{T}_2}{\partial z_2}\right|_{z_2=0}=0 \tag{33}$$

$$k_1 \frac{\partial \overline{T}_1}{\partial z_1}\bigg|_{z_1=c_1} = \overline{q}_1(x_1, y_1); \quad \overline{T}_2\big|_{z_2=c_2} = \overline{T}_0(x_1, y_1) \tag{34}$$

where all variables with an overbar are Laplace transforms of corresponding variables, and p is the Laplace parameter.

The solutions for the Laplacian temperature fields are given by:

$$\overline{T}_i(x,y,z_i) = c_{i0}\left(e^{\beta_i z_i} + A_i e^{-\beta_i z_i}\right) + \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} c_{i,nm}\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)\left[\cosh\left(\gamma_{i,nm} z_i\right) + \frac{h_i}{k_1 \gamma_{i,nm}}\sinh\left(\gamma_{i,nm} z_i\right)\right] \tag{35}$$

where $\beta_i = \sqrt{\frac{p}{\alpha_i}}$, $\gamma_{i,nm} = \sqrt{\left(\frac{n\pi}{a}\right)^2 + \left(\frac{m\pi}{b}\right)^2 + \beta_i^2}$ and $A_i = \frac{\beta_i - \frac{h_i}{k_i}}{\beta_i + \frac{h_i}{k_i}}$ for $i=1,2$.

Expressions for $c_{i,0}$ and $c_{i,nm}$ for $i=1,2$ are given by

$$c_{2,0} = \frac{1}{ab\left(e^{\beta_2 c_2} + A_2 e^{-\beta_2 c_2}\right)} \int_{y=0}^{b}\int_{x=0}^{a} \overline{T}_0(x,y)\,dx\,dy \tag{36}$$

$$c_{2,nm} = \begin{cases} \dfrac{2}{abP_{2,nm}} \displaystyle\int_{y=0}^{b}\int_{x=0}^{a} \overline{T}_0(x,y)\cos\left(\frac{n\pi x}{a}\right)dx\,dy & n \neq 0; m = 0 \\ \dfrac{2}{abP_{2,nm}} \displaystyle\int_{y=0}^{b}\int_{x=0}^{a} \overline{T}_0(x,y)\cos\left(\frac{m\pi y}{b}\right)dx\,dy & n = 0; m \neq 0 \\ \dfrac{4}{abP_{2,nm}} \displaystyle\int_{y=0}^{b}\int_{x=0}^{a} \overline{T}_0(x,y)\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)dx\,dy & n \neq 0; m \neq 0 \end{cases} \tag{37}$$

where $P_{2,nm} = \cosh\left(\gamma_{2,nm} c_2\right) + \frac{h}{k_2 \gamma_{2,nm}}\sinh\left(\gamma_{2,nm} c_2\right)$

Respective boundary conditions at the heat sink and package ends, $h_1=h$ and $h_2=0$ in the above equation. Note that the intermediate temperature $T_0(x,y)$ and heat flux

$q_1(x,y)$ are not known in advance. However, the solution may be determined iteratively by guessing $q_1(x,y)$, solving for $T_1(x,y)$ and $T_2(x,y)$, determining $q_2(x,y)$ from the derivative of $T_2(x,y)$, updating $q_1(x,y)=Q_1(x,y)-q_2(x,y)$, and repeating the process until reasonable accuracy is obtained. This procedure is similar to the one outlined in section 2.2.

For the contributions from $Q_2(x,y,z_2,t)$ alone, the governing energy equations after applying the Laplace transform for $i=1,2$ are

$$\frac{\partial^2 \overline{T}_i}{\partial x^2}+\frac{\partial^2 \overline{T}_i}{\partial y^2}+\frac{\partial^2 \overline{T}_i}{\partial z_i^2}=\frac{p}{\alpha_i}\overline{T}_i \tag{38}$$

$$\frac{\partial \overline{T}_i}{\partial x}=0 \qquad \text{at } x=0,a \tag{39}$$

$$\frac{\partial \overline{T}_i}{\partial y}=0 \qquad \text{at } y=0,b \tag{40}$$

$$\left.\frac{\partial \overline{T}_1}{\partial z_1}\right|_{z_1=0}=\frac{h}{k_1}\overline{T}_1\Big|_{z_1=0};\quad \left.\frac{\partial \overline{T}_2}{\partial z_2}\right|_{z_2=0}=\overline{Q}_2(x,y) \tag{41}$$

$$k_1\left.\frac{\partial \overline{T}_1}{\partial z_1}\right|_{z_1=c_1}=\overline{q}_1(x,y);\quad \overline{T}_2\Big|_{z_2=c_2}=\overline{T}_0(x,y) \tag{42}$$

The solution for $\overline{T}_1(x,y,z_1)$ is the same as given in equation 35. The solution for $\overline{T}_2(x,y,z_2)$ is given by

$$\overline{T}_2(x,y,z_2)=\begin{matrix} c_{2A,0}\left(e^{\beta_2(z_2-c_2)}-e^{-\beta_2(z_2-c_2)}\right)+\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}c_{2A,nm}\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)\sinh\left(\gamma_{nm}(z_i-c_i)\right)+ \\ c_{2B,0}\left(e^{\beta_2 z_2}+e^{-\beta_2 z_2}\right)+\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}c_{2B,nm}\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)\cosh\left(\gamma_{nm}z_i\right)\end{matrix} \tag{43}$$

Expressions for $c_{2A,0}$, $c_{2B,0}$, $c_{2A,nm}$ and $c_{2B,nm}$ are given by

$$c_{2A,0} = \frac{1}{abk_2\beta_2\left(e^{\beta_2 c_2} + e^{-\beta_2 c_2}\right)} \int_{y=0}^{b}\int_{x=0}^{a} -\overline{Q}_2(x,y)\,dxdy \tag{44}$$

$$c_{2B,0} = \frac{1}{ab\left(e^{\beta_2 c_2} + e^{-\beta_2 c_2}\right)} \int_{y=0}^{b}\int_{x=0}^{a} \overline{T}_0(x,y)\,dxdy \tag{45}$$

$$c_{2A,nm} = \begin{cases} \dfrac{2}{abk_2\gamma_{2,nm}\cosh\left(\gamma_{2,nm}c_2\right)} \displaystyle\int_{y=0}^{b}\int_{x=0}^{a} -\overline{Q}_2(x,y)\cos\left(\frac{n\pi x}{a}\right)dxdy & n \neq 0; m = 0 \\ \dfrac{2}{abk_2\gamma_{2,nm}\cosh\left(\gamma_{2,nm}c_2\right)} \displaystyle\int_{y=0}^{b}\int_{x=0}^{a} -\overline{Q}_2(x,y)\cos\left(\frac{m\pi y}{b}\right)dxdy & n = 0; m \neq 0 \\ \dfrac{4}{abk_2\gamma_{2,nm}\cosh\left(\gamma_{2,nm}c_2\right)} \displaystyle\int_{y=0}^{b}\int_{x=0}^{a} -\overline{Q}_2(x,y)\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)dxdy & n \neq 0; m \neq 0 \end{cases} \tag{46}$$

$$c_{2B,nm} = \begin{cases} \dfrac{2}{ab\cosh\left(\gamma_{2,nm}c_2\right)} \displaystyle\int_{y=0}^{b}\int_{x=0}^{a} \overline{T}_0(x,y)\cos\left(\frac{n\pi x}{a}\right)dxdy & n \neq 0; m = 0 \\ \dfrac{2}{ab\cosh\left(\gamma_{2,nm}c_2\right)} \displaystyle\int_{y=0}^{b}\int_{x=0}^{a} \overline{T}_0(x,y)\cos\left(\frac{m\pi y}{b}\right)dxdy & n = 0; m \neq 0 \\ \dfrac{4}{ab\cosh\left(\gamma_{2,nm}c_2\right)} \displaystyle\int_{y=0}^{b}\int_{x=0}^{a} \overline{T}_0(x,y)\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)dxdy & n \neq 0; m \neq 0 \end{cases} \tag{47}$$

$$c_{2nm} = \begin{cases} \dfrac{2}{abP_{2,nm}} \displaystyle\int_{y=0}^{b}\int_{x=0}^{a} \overline{T}_0(x,y)\cos\left(\frac{n\pi x}{a}\right)dxdy & n \neq 0; m = 0 \\ \dfrac{2}{abP_{2,nm}} \displaystyle\int_{y=0}^{b}\int_{x=0}^{a} \overline{T}_0(x,y)\cos\left(\frac{m\pi y}{b}\right)dxdy & n = 0; m \neq 0 \\ \dfrac{4}{abP_{2,nm}} \displaystyle\int_{y=0}^{b}\int_{x=0}^{a} \overline{T}_0(x,y)\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)dxdy & n \neq 0; m \neq 0 \end{cases} \tag{48}$$

where $P_{2,nm} = \cosh\left(\gamma_{2,nm}c_2\right) + \dfrac{h}{k_2\gamma_{2,nm}}\sinh\left(\gamma_{2,nm}c_2\right)$

The iterative procedure for obtaining the solution for $\overline{T}_1(x,y,z_1)$ and $\overline{T}_2(x,y,z_2)$ is similar to the one outlined in section 2.2.

Once the solutions for the Laplace transforms of the temperature fields for heat generation on each die have been determined, the actual temperature field is determined by numerically evaluating the inverse Laplace transform.

Figure 2.8 shows the temperature as a function of time at the hotspot on die1 for the two-die case described above. Results from both the analytical model and finite-element simulations are presented, and excellent agreement within 2.6% is observed. The model presented in this section may be helpful in characterizing the transient thermal behavior of 3D ICs during events of core startup or shutdown, core switching, etc. where there is significant transient behavior of power sources.

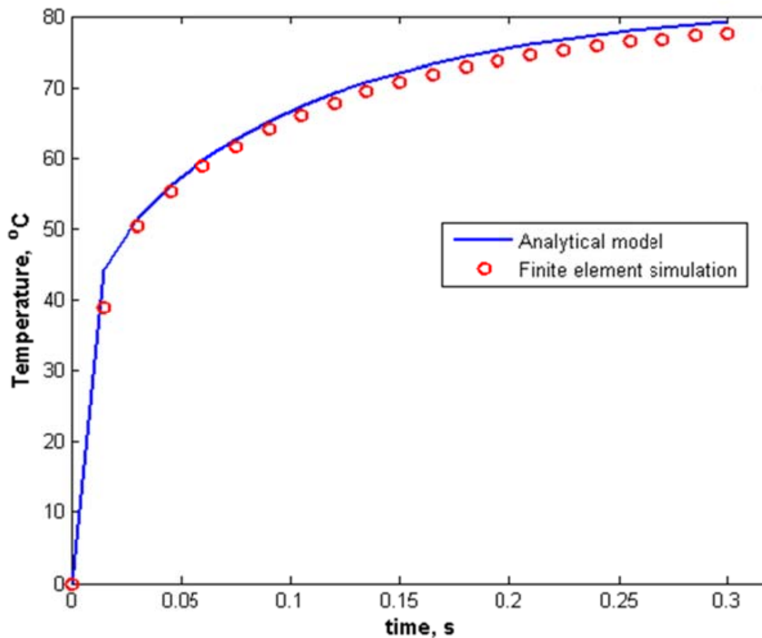


Figure 2.8 Comparison of transient temperature profile at the hotspot in a two-die 3D IC predicted by the analytical model and finite-element simulations.

2.5 Conclusions

This chapter presents an analytical model to determine three-dimensional, steady-state and transient temperature fields in a 3D IC based on solutions of the governing energy equations. An iterative approach that takes advantage of temperature and heat flux matching at interfaces is proposed. The temperature solution based on this approach converges within around 7 iterations, and is in good agreement with finite-element simulation results. The analytical approach provides good physical insight into the problem of determining temperature fields in 3D ICs. In addition, it is expected to more easily interface with mainstream electrical design tools as compared to finite-element based methods. The work presented here also underscores the need for thermal-friendly pre-Silicon design, which helps minimize the system-level thermal dissipation challenge and leads to higher reliability without compromising electrical performance. This work is expected to aid in developing temperature characterization and prediction tools for 3D ICs. In addition, this work may also help in characterization of various thermal management strategies being proposed for 3D ICs.

Chapter 3

Determination of Temperature Distribution in Three-Dimensional Integrated Circuits(3D ICS) with Unequally-Sized Die

3.1 Introduction

Three-dimensional integrated circuits (3D IC) technology refers to the vertical integration of circuits on multiple semiconductor substrates [Banerjee *et al*., 2001; Patti *et al*., 2006]. 3D ICs offer several advantages over traditional microelectronic designs, including heterogeneous design integration, reduced interconnect delay, etc. [Pozder *et al*., 2007; Alam *et al*., 2010]. It has been estimated that 3D integration provides roughly the same performance benefits as dimensional scaling by one technology node without the prohibitive associated costs [Jones-Savidis *et al*., 2010]. Vertical integration is usually implemented by bonding of metal pads on frontside or backside of adjacent die, which in addition to mechanical adhesion also provide a pathway for electrical communication between the die [Pozder *et al*., 2007]. 3D IC technology also often necessitates signal transmission from one face of a die to the other. This is usually implemented using through-silicon vias (TSVs), which are metal-filled vias etched all the way through the substrate [Savidis *et al*., 2010].

Thermal management of 3D ICs has widely been recognized as a significant technology challenge for widespread implementation of this technology [Jones, 2007; Venkatadri *et al*., 2011]. While the back face of the die was traditionally available for heat removal, for example by attachment to a heat sink using a thermal interface material, in 3D ICs, both faces of the die are utilized for electrical interconnection with adjacent die. The heat removal challenge is particularly exacerbated for die in the middle of the vertical stack. Early work in this field focused on investigation of thermal management challenges in 3D ICs [Kleiner *et al*., 1995; Chiang *et al*., 2001] and the thermal implications of various

electrical design models being considered for 3D IC technology [Goplen *et al*., 2006; Cong *et al*., 2007].

Thermal envelope available for 3D IC design has been estimated by modeling changes in block-level power consumption due to three-dimensional design and its impact on thermal management [Black *et al*., 2006]. A number of thermal management approaches have been investigated for meeting the heat dissipation challenge in 3D ICs. [Brunschwiler *et al*., 2009; Kim *et al*., 2010; Kota *et al*., 2009; Phan *et al*., 2010]. These approaches include liquid cooling [Brunschwiler-Kim-Kota13-15], thermoelectric-based cooling [Phan *et al*., 2010], etc. A limited amount of experimental work on measurement of thermal characteristics of 3D ICs has also been reported in the past few years [Oprins *et al*., 2011; Oprins *et al*., 2012; Matsumoto *et al*., 2011].

While most of the thermal modeling work for 3D ICs has assumed identically sized die [Venkatadri *et al*., 2011; Jain *et al*., 2010; Rahman *et al*., 2001; Ayala *et al*., 2010; Jain *et al*., 2011], manufacturing and packaging considerations often require that the die size not be the same [Jones, 2007]. For example, making the bottom die larger than the top die allows wire bond connections to be made to the exposed area of the bottom die. Further, by employing die-on-wafer bonding, significant yield improvement can be obtained without requiring the die to be the same size [Jones, 2007]. Finally, having unequally sized die is also necessitated for implementation of heterogeneous design. For example, the same memory die designed using a pre-specified bond pad layout could be implemented on multiple logic die designs for different applications, none of which need to necessarily be the same size [Alam *et al*., 2010]. The memory die does not need to be designed for each application separately, resulting in significant reduction in cost and design time.

The nature of heat transfer in unequally-sized die is inherently different from a stack of identical die due to heat spreading and constriction. A variety of thermal simulation approaches including finite-difference and finite-element modeling have been employed for determining the temperature field in a 3D IC [Rahman *et al*., 2001; Ayala *et al*., 2010; Jain *et al*., 2011]. Analytical heat transfer models developed for uniformly-sized die [Geer *et al*., 2007; Haji-Sheikh *et al*., 2003; Choobineh *et al*., 2012] are not applicable if the die sizes are not uniform. Edge effects, which are usually neglected in the analysis of identical die may be important for unequally-sized die. Past work on heat spreading and constriction in electronic packages has only considered two layers of unequally-sized substrates [Lee *et al*., 1995]. Another paper reported finite-difference modeling of heat conduction in unequally-sized 3D IC stacks [Jain, 2010]. While such approaches help determine the temperature profile in a 3D IC, a more fundamental approach involving analytical solutions of the governing energy equations would help develop a basic understanding of thermal management of unequally-sized 3D IC stacks, and how such stacks differ from uniformly-sized stacks. Recent work has reported the use of a novel thermal lid for thermal management of unequally-sized die stack [Sikka *et al*., 2012]. Given the growing interest in thermal management of 3D ICs in general, and unequally-sized die stacks in particular, it is essential to develop a fundamental understanding of this problem and derive analytical expressions for the temperature field based on solutions of the governing energy equations. Such approach is likely to help improve thermal design of 3D ICs.

This chapter presents an analytical model for understanding heat transfer characteristics of a stack of unequally sized die with non-uniform heating on each die. Governing energy conservation equations with appropriate boundary conditions are solved, resulting in three-dimensional temperature fields for each die. The non-uniform

die size presents interesting modeling challenges, necessitating an iterative approach for determining the temperature field. Results are in excellent agreement with finite-element simulations. The model is used for comparing the thermal performance of non-uniform 3D ICs with a uniformly-sized 3D IC. It is found that the larger the degree of non-uniformity in a die sizes, the higher is the temperature, due to additional thermal spreading/constriction resistance. This work provides a useful tool for understanding the fundamentals of heat transfer in 3D ICs and evaluating the realistic thermal impact of 3D integration.

3.2 Steady-State Heat Conduction Model for Non-Uniformly Sized 3D IC

The die stack consists of N dies, each of which is a cuboid of size a_i by b_i by c_i. Figure 3.1 shows the *x-z* cross-section of the geometry under consideration. All dies in the stack are assumed to center around a common axis. The model presented in this manuscript can also be used for non-concentric die stacks with appropriate transformations in the *x* and *y* axes. A heat sink is attached to the bottom-most die, which is modeled using a convective boundary condition. It is assumed that the top-most die is connected to the electrical package, through which no heat loss occurs. All side surfaces are assumed to be adiabatic. $Q_i(x,y)$ is the known heat generation that occurs in the device plane at the top of the ith die. The primary interest is in determining the temperature fields $T_i(x,y,z)$.

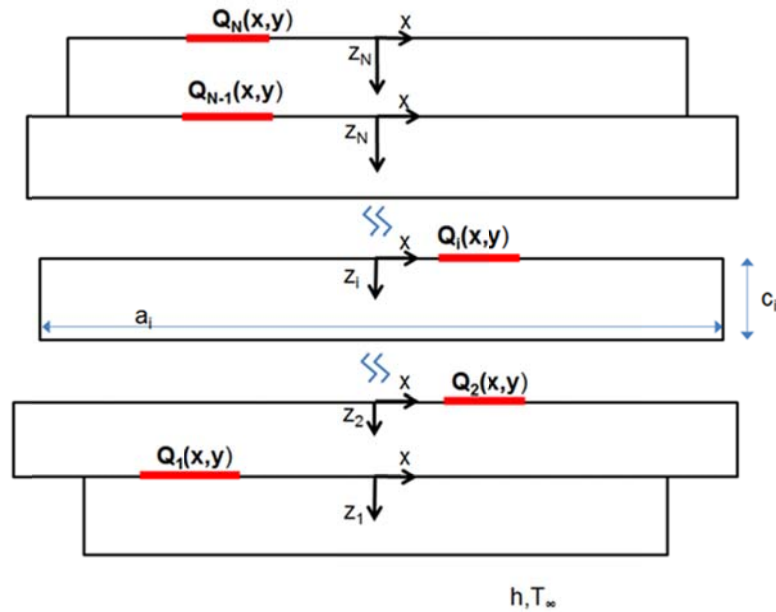


Figure 3.1 Schematic of the cross-section view of the N-die stack comprising unequally sized die. The size of the ith die in the direction perpendicular to the paper is bi. All die are assumed to be concentric, and the origin of coordinates for each die is assumed to be located at the center of the top x-y plane of the die.

The model for determining temperature in the N-die stack requires solutions for three heat transfer problems pertaining to single die. These problems and their solutions are presented in section 3.2.1. Section 3.2.2 combines these solutions to provide a model for the N-die temperature field.

3.2.1 Solution to Three Relevant Heat Transfer Problems

Figure 3.2 schematically shows three relevant heat transfer problems in a single die that will be used to derive the multi-die temperature field. Each problem comprises a single die of size *a* by *b* by *c*, with a temperature-independent thermal conductivity k_i.

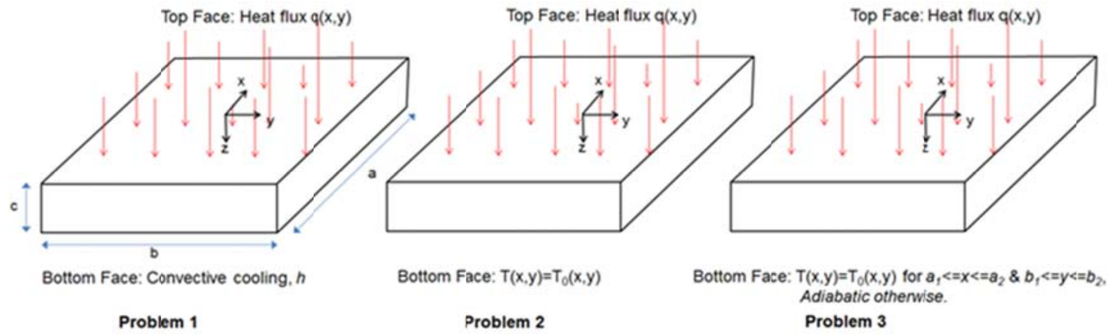


Figure 3.2 Schematics of three single-die heat transfer problems solved in section 3.2.1. In each case, the four side walls are adiabatic.

In problem 1, a heat flux *q(x,y)* is incident on the top surface of the die. Heat loss occurs through the bottom, which is modeled using a convective heat transfer coefficient *h*. In this case, the governing energy equation is

$$\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}=0 \qquad (1)$$

Boundary conditions in *x* and *y* directions are

$$\frac{\partial T}{\partial x}=0 \quad \text{at } x=\pm\frac{a}{2} \qquad (2)$$

$$\frac{\partial T}{\partial y}=0 \quad \text{at } y=\pm\frac{b}{2} \qquad (3)$$

Boundary conditions in *z* direction are

$$\frac{\partial T}{\partial z}=-\frac{1}{k}q(x,y) \quad \text{at z=0} \qquad (4)$$

$$\frac{\partial T}{\partial z}=-\frac{h}{k}T \quad \text{at } z=c \qquad (5)$$

Problem 1 is solved by utilizing Fourier cosine series expansion [Ozisik, 1898]. Briefly, the temperature field is written as a two-variable infinite series comprising products of the eigenfunctions in *x* and *y* directions. The coefficients of the infinite series are determined by using the non-homogeneous boundary condition and comparing the coefficients with corresponding coefficients in the two-variable Fourier cosine series expansion of the non-homogeneous term. The solution for the temperature field *T(x,y,z)* is as follows:

$$T(x,y,z) = d_0\left(\left(c-z\right)+\frac{k}{h}\right)+ \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} d_{nm}\cos\left(\frac{n\pi\left(x-0.5a\right)}{a}\right)\cos\left(\frac{m\pi\left(y-0.5b\right)}{b}\right)\left[\cosh\left(\gamma_{nm}\left(c-z\right)\right)+\frac{h}{k\gamma_{nm}}\sinh\left(\gamma_{nm}\left(c-z\right)\right)\right] \tag{6}$$

where $\gamma_{nm} = \sqrt{\left(\frac{n\pi}{a}\right)^2+\left(\frac{m\pi}{b}\right)^2}$

To do so, the Fourier cosine series expansions of heat flux *q(x,y)* are first written as follows

$$q\ (x,y) = b_{1,0} + \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} b_{1,nm}\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right) \tag{7}$$

where the coefficients $b_{1,0}$ and $b_{1,nm}$ may be determined as

$$b_{1,0} = \frac{1}{ab}\int_{-b/2}^{b/2}\int_{-a/2}^{a/2} q(x,y)dxdy \tag{8}$$

where

$$b_{1,nm} = \begin{cases} \dfrac{2}{ab}\displaystyle\int_{-b/2}^{b/2}\int_{-a/2}^{a/2} q(x,y)\cos\left(\frac{n\pi x}{a}\right)dxdy & n \neq 0; m = 0 \\ \dfrac{2}{ab}\displaystyle\int_{-b/2}^{b/2}\int_{-a/2}^{a/2} q(x,y)\cos\left(\frac{m\pi y}{b}\right)dxdy & n = 0; m \neq 0 \\ \dfrac{4}{ab}\displaystyle\int_{-b/2}^{b/2}\int_{-a/2}^{a/2} q(x,y)\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)dxdy & n \neq 0; m \neq 0 \end{cases} \tag{9}$$

By applying the non-homogeneous z-direction boundary condition, equation (4), the coefficients d_0 and d_{nm} are given by

$$d_0 = \frac{1}{abk}\int_{-b/2}^{b/2}\int_{-a/2}^{a/2} q(x,y)dxdy \tag{10}$$

$$d_{nm} = \begin{cases} 0 \quad if \quad n = 0; m = 0 \\ \dfrac{2}{abkP_{nm}}\displaystyle\int_{-b/2}^{b/2}\int_{-a/2}^{a/2} q(x,y)\cos\left(\frac{n\pi(x-0.5a)}{a}\right)dxdy \quad if \quad n \neq 0; m = 0 \\ \dfrac{2}{abkP_{nm}}\displaystyle\int_{-b/2}^{b/2}\int_{-a/2}^{a/2} q(x,y)\cos\left(\frac{m\pi(y-0.5b)}{b}\right)dxdy \quad if \quad n = 0; m \neq 0 \\ \dfrac{4}{abkP_{nm}}\displaystyle\int_{-b/2}^{b/2}\int_{-a/2}^{a/2} q(x,y)\cos\left(\frac{n\pi(x-0.5a)}{a}\right)\cos\left(\frac{m\pi(y-0.5b)}{b}\right)dxdy \quad if \quad n \neq 0; m \neq 0 \end{cases} \tag{11}$$

where $p_{nm} = \gamma_{nm}\sinh(\gamma_{nm}c) + \frac{h}{k}\cosh(\gamma_{nm}c)$

Problem 2, shown schematically in Figure 3.2(b) comprises a known heat flux *q(x,y)* at the top of a die. The temperature distribution on the bottom face is given as $T_0(x,y)$. Similar to problem 1, in this case, the governing energy equation, and *x* and *y* boundary conditions are given by equations (1) and (2)-(3) respectively. The *z*-boundary conditions are given by

$$T(x,y) = T_0(x,y) \qquad \text{at } z=c \tag{12}$$

$$\frac{\partial T}{\partial z} = \frac{1}{k} q(x, y) \qquad \text{at } z=0 \tag{13}$$

The solution for Problem 2 is

$$T(x,y,z) = \begin{matrix} d_{A0} + \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} d_{A,nm} \cos\left(\frac{n\pi(x-0.5a)}{a}\right)\cos\left(\frac{m\pi(y-0.5b)}{b}\right)\cosh(\gamma_{nm} z) + \\ d_{B0}(z-c) + \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} d_{B,nm} \cos\left(\frac{n\pi(x-0.5a)}{a}\right)\cos\left(\frac{m\pi(y-0.5b)}{b}\right)\sinh(\gamma_{nm}(z-c)) \end{matrix} \tag{14}$$

where $\gamma_{nm} = \sqrt{\left(\frac{n\pi}{a}\right)^2 + \left(\frac{m\pi}{b}\right)^2}$

The coefficients $d_{A,0}$ and $d_{A,nm}$ are found by applying the boundary condition equation (12).

The Fourier cosine series expansions of temperature distribution $T_0(x,y)$ are first written as follows

$$T_0(x, y) = b_0 + \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} b_{nm} \cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right) \tag{15}$$

where the coefficients b_0 and b_{nm} may be determined as

$$b_0 = \frac{1}{ab} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} T_0(x, y) dxdy \tag{16}$$

where

$$b_{nm} = \begin{cases} \frac{2}{ab} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} T_0(x, y) \cos\left(\frac{n\pi x}{a}\right) dxdy & n \neq 0; m = 0 \\ \frac{2}{ab} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} T_0(x, y) \cos\left(\frac{m\pi y}{b}\right) dxdy & n = 0; m \neq 0 \\ \frac{4}{ab} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} T_0(x, y) \cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right) dxdy & n \neq 0; m \neq 0 \end{cases} \tag{17}$$

Then

$$d_{A,0} = \frac{1}{ab} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} T_0(x,y)\,dxdy \tag{18}$$

$$d_{A,nm} = \begin{cases} 0 \quad if \quad n=0; m=0 \\ \dfrac{2}{ab\cosh(\gamma_{nm} c)} \displaystyle\int_{-b/2}^{b/2} \int_{-a/2}^{a/2} T_0(x,y) \cos\left(\frac{n\pi(x-0.5a)}{a}\right) dxdy \quad if \quad n \neq 0; m=0 \\ \dfrac{2}{ab\cosh(\gamma_{nm} c)} \displaystyle\int_{-b/2}^{b/2} \int_{-a/2}^{a/2} T_0(x,y) \cos\left(\frac{m\pi(y-0.5b)}{b}\right) dxdy \quad if \quad n=0; m \neq 0 \\ \dfrac{2}{ab\cosh(\gamma_{nm} c)} \displaystyle\int_{-b/2}^{b/2} \int_{-a/2}^{a/2} T_0(x,y) \cos\left(\frac{n\pi(x-0.5a)}{a}\right) \cos\left(\frac{m\pi(y-0.5b)}{b}\right) dxdy \quad if \quad n \neq 0; m \neq 0 \end{cases} \tag{19}$$

Similar to problem 1, the coefficients $d_{B,0}$ and $d_{B,nm}$ are found by applying the boundary condition equation (13)

$$d_{B,0} = \frac{1}{abk} \int_{-b/2}^{b/2} \int_{-a/2}^{a/2} q(x,y)\,dxdy \tag{20}$$

$$d_{B,nm} = \begin{cases} 0 \quad if \quad n=0; m=0 \\ \dfrac{2}{abkp_{nm}} \displaystyle\int_{-b/2}^{b/2} \int_{-a/2}^{a/2} q(x,y) \cos\left(\frac{n\pi(x-0.5a)}{a}\right) dxdy \quad if \quad n \neq 0; m=0 \\ \dfrac{2}{abkp_{nm}} \displaystyle\int_{-b/2}^{b/2} \int_{-a/2}^{a/2} q(x,y) \cos\left(\frac{m\pi(y-0.5b)}{b}\right) dxdy \quad if \quad n=0; m \neq 0 \\ \dfrac{4}{abkp_{nm}} \displaystyle\int_{-b/2}^{b/2} \int_{-a/2}^{a/2} q(x,y) \cos\left(\frac{n\pi(x-0.5a)}{a}\right) \cos\left(\frac{m\pi(y-0.5b)}{b}\right) dxdy \quad if \quad n \neq 0; m \neq 0 \end{cases} \tag{21}$$

where $p_{nm} = \gamma_{nm} \cosh(\gamma_{nm} c)$

Problem 3, shown schematically in Figure 3.2(c) has a known heat flux *q(x,y)* at the top of the die. On the bottom face, the temperature is known to be $T_0(x,y)$ in a region

bound by $a_1 <= x <= a_2$ and $b_1 <= y <= b_2$, whereas the remainder of the bottom face is adiabatic. Problem 3 is solved by guessing a temperature profile for the adiabatic region on the bottom face, $T_m(x,y)$, so that the temperature profile on the entire bottom face is $T_g(x,y)$ which combines the known field $T_0(x,y)$ with the guessed field in the adiabatic region $T_m(x,y)$. By doing so, problem 3 reduces to problem 2 and the solution is given by equations (12) through (21). Once the temperature field is determined, the outgoing heat flux in the adiabatic region of the bottom face may be computed by the following equation:

$$Q_{bottom}(x,y) = k\left(\frac{dT}{dz}\right)_{(z=c)} = \begin{array}{l} k\sum_{m=0}^{\infty}\sum_{n=0}^{\infty} d_{A,nm}\cos\left(\frac{n\pi(x-0.5a)}{a}\right)\cos\left(\frac{m\pi(y-0.5b)}{b}\right)\gamma_{nm}\sinh(\gamma_{nm}c) + \\ kd_{B,0} + k\sum_{m=0}^{\infty}\sum_{n=0}^{\infty} d_{B,nm}\cos\left(\frac{n\pi(x-0.5a)}{a}\right)\cos\left(\frac{m\pi(y-0.5b)}{b}\right)\gamma_{nm} \end{array} \quad (22)$$

The guessed temperature profile in the adiabatic region on the bottom face is updated as follows:

$$T_{m,new}(x,y) = (1-w)\cdot T_m(x,y) + w\cdot\left(\frac{Q_{bottom}(x,y)\cdot c}{k} + T(x,y,z=0)\right) \quad (23)$$

where w is a weighing function between 0 and 1.

The problem is solved again, and the procedure is repeated until $Q_{bottom}(x,y)$ is reasonably close to zero in the adiabatic region of the bottom face. This provides the solution to problem 3.

The next sub-section discusses the determination of the temperature field in the N-die stack of unequally sized die using the solutions of the three problems discussed above.

3.2.2 Solution to the N-Die Heat Transfer Problem

The N-die stack comprising of non-uniformly sized die, with heat generation $Q_i(x,y)$ occurring on the device plane of each die is now considered. In order to determine

the temperature field for each die, $T_i(x,y,z)$ for $-\frac{a_i}{2} \le x \le \frac{a_i}{2}$ and $-\frac{b_i}{2} \le y \le \frac{b_i}{2}$, each die is considered as a separate domain, and the governing energy conservation equation with appropriate boundary conditions is solved for each die. Continuity of the temperature field and conservation of heat flux at the interface is utilized to derive boundary conditions at the interface between adjacent die. The heat flux entering each die from the top is initially guessed and the guess is iteratively improved until sufficient accuracy is obtained. The procedure is as follows:

1- Because of linearity of governing energy equation, assume only one of the heat sources Qi(x,y) at top surface is active , $i=1,2,\ldots,N-1$.

2- Assume a value for heat fluxes $q_i(x, y)$ entering each die at the top face, $i=1, 2,\ldots, N-1$.

3- The heat transfer problem for die1 is identical to problem 1 discussed in section 3.2.1. $T_1(x, y, z_1)$ is thus determined from equations (6) through (11). As a result, $T_{02}(x,y)$, the interface temperature field between die1 and die2 is computed, since $T_{02}(x,y)=T_1(x,y,z=c_1)$.

4- Temperature fields for die 2 through $N-1$ are computed sequentially. For solving the temperature profile in the ith die, the interface temperature between die i and die $i-1$, $T_{0i}(x,y)$ is already known from the previously determined temperature field of the $(i-1)^{th}$ die since $T_{0i}(x,y)=T_{i-1}(x,y,z=c_{i-1})$. As a result, depending on whether the $(i-1)^{th}$ die is larger or smaller than the ith die, the problem of the ith die is identical to problem 2 or problem 3 respectively, solutions for which are presented in section 3.2.1. Based on the computed temperature profile $T_i(x,y,z_i)$, the interface temperature between die i and i+1, $T_{0,i+1}(x,y)$ is computed and used

to compute the temperature profile in the next die. This procedure is repeated until the *(N-1)*th die.

5- For the Nth die, the heat flux entering the top face is known to be $Q_N(x, y)$ and the temperature at the bottom is given by the interface temperature between the Nth and $N\text{-}1^{th}$ die, $T_{0N}(x,y)$. In this case, the problem is identical to problem 2 or problem 3 depending on whether the Nth die is smaller or larger than the $(N\text{-}1)^{th}$ die.

6- Once all temperature fields have been computed, the heat fluxes $q_i(x_i,y_i)$ for die $i=1,2,3,..(N\text{-}1)$ are computed using energy conservation at the interface between the ith and $(i+1)^{th}$ die as follows:

$$q_i(x,y) = Q_i(x,y) - \delta(x,y)k_{i+1}\left(\frac{\partial T}{\partial z_{i+1}}\right)_{z=c_{i+1}} \tag{24}$$

Where $\delta(x,y)$ captures the effect of whether (x,y), the point on die i under consideration lies within or outside the projection of the $(i+1)^{th}$ die.

$$\delta(x,y) = \begin{vmatrix} 1 & if \\ 0 & otherwise \end{vmatrix}\left(-\frac{a_{i+1}}{2} \le x \le \frac{a_{i+1}}{2}\right) and \left(-\frac{b_{i+1}}{2} \le y \le \frac{b_{i+1}}{2}\right) \tag{25}$$

7- The heat flux fields $q_i(x,y)$ are updated based on a weighted average of the current and new values.

8- Steps 3 through 7 are repeated until the change in the temperature field between successive iterations is sufficiently small and the results are temperature field due to applying only $Q_i(x,y)$.

9- Once the temperature fields due to all $Q_i(x,y)$, $i=1, 2,\ldots,N\text{-}1$, calculated from step 1 to 8, they are added linearly together to have the final temperature fields.

3.3 Model Results

The analytical model outlined in section 3.2.2 is used to solve the temperature profile in a multi-die stack with N=3. The three die are assumed to be 8mm by 8mm, 10mm by 10mm and 4mm by 4mm respectively. A single hotspot of size 1mm by 1mm and total power of 2.5W is assumed on each die. The location of the hotspots with respect to the center point of the die is (-1.5mm, 2.5mm), (0mm, 0mm) and (-1.5mm, 1.5mm) respectively. The 8mm by 8mm die is assumed to be stacked next to the heat sink, which is modeled with a convective heat transfer coefficient of $5000W/m^2K$. Each die was assumed to be 0.5mm thick, with a thermal conductivity of 150W/mK which is representative of Silicon.

Double integrals in equations (8)-(9) and (10)-(11) are evaluated using a two-dimensional Gauss quadrature [Hamming *et al.*, 1986]. Figure 3.3 shows the predicted temperature rise at the center of a hotspot as a function of the number of terms included in the double summations in equations (6) and (14). The temperature rise is reported as a fraction of the temperature rise with 1000 terms, which is assumed to be the accurate value. It is seen that the predicted temperature value reaches within around 2% of the eventual value with only around 20 terms. Thus, limiting the double summations to only the first 20 terms significantly reduces computation time without affecting accuracy.

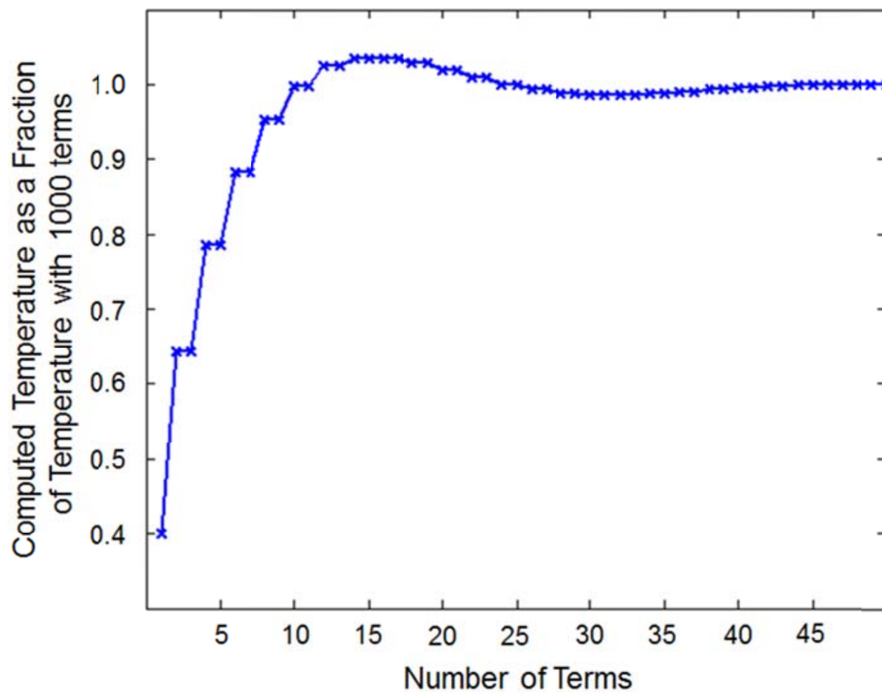


Figure 3.3 Effect of the number of terms considered in the double summation on accuracy of temperature computation.

Figure 3.4 plots the computed temperature along a line passing through the center of the hotspot on the second die as a function of the number of iterations employed, following the procedure described in section 3.2.2. The solution becomes stable within 5-6 iterations, the solution stabilizes. Beyond the sixth iteration, the difference in the temperature field between successive iterations is less than 0.1%. As a result, the solutions described in this paper were computed using only 7 iterations. This contributes to reduction of computation time without sacrificing quality of results.

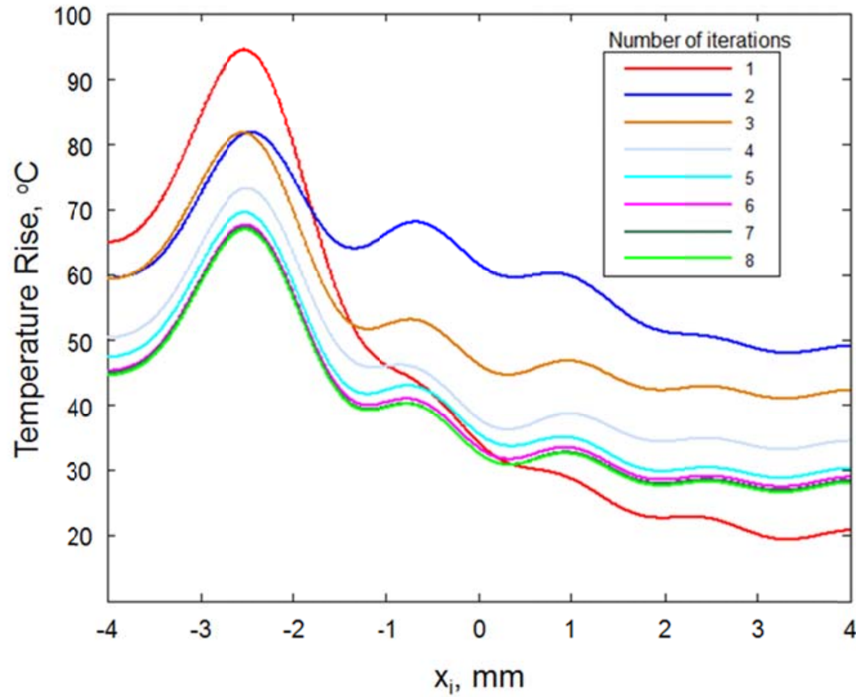


Figure 3.4 Effect of the number of iterations on temperature computation accuracy.

Based on the computational simplifications discussed above, the temperature field on a three-die stack described above is computed and compared with finite-element simulation results. Figure 3.5 shows the temperature field on the three dies predicted by the model. A plot of temperature along lines shown in Figure 3.5 is presented in Figure 3.6. There is excellent agreement of the computed temperature fields with finite-element simulations carried out in commercial software. The temperature rise predicted by the model is within ±4% of finite-element simulation results. Figures 3.5 and 3.6 validate the model presented in sections 3.2.1 and 3.2.2.

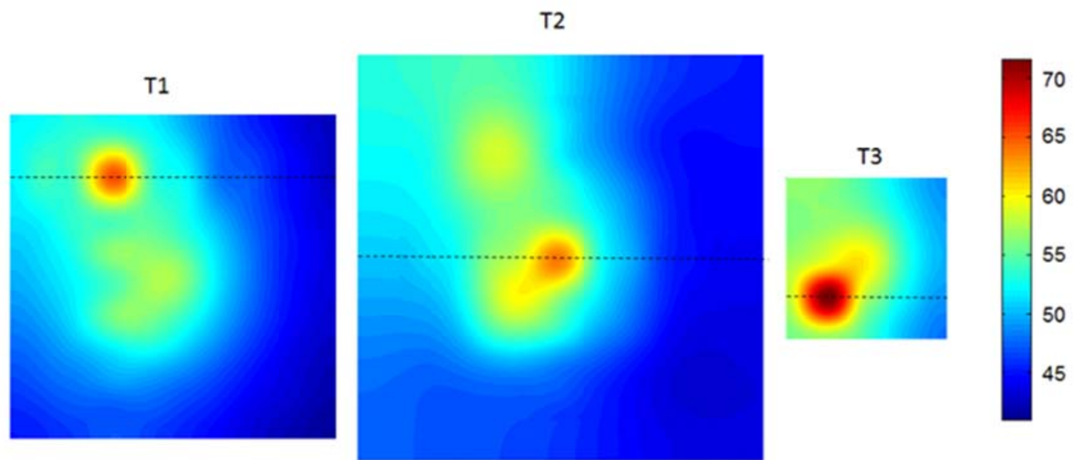


Figure 3.5 Temperature field on the device plane of each die in a three-die stack with a hotspot on each die

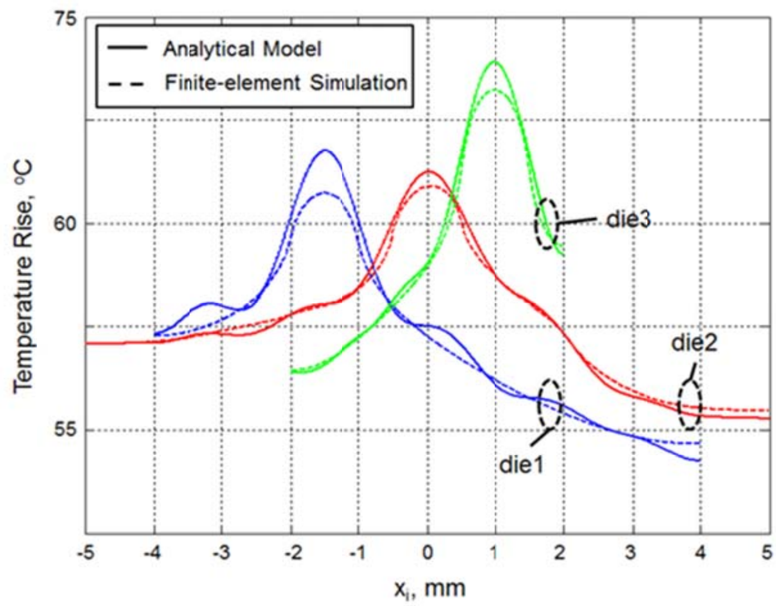
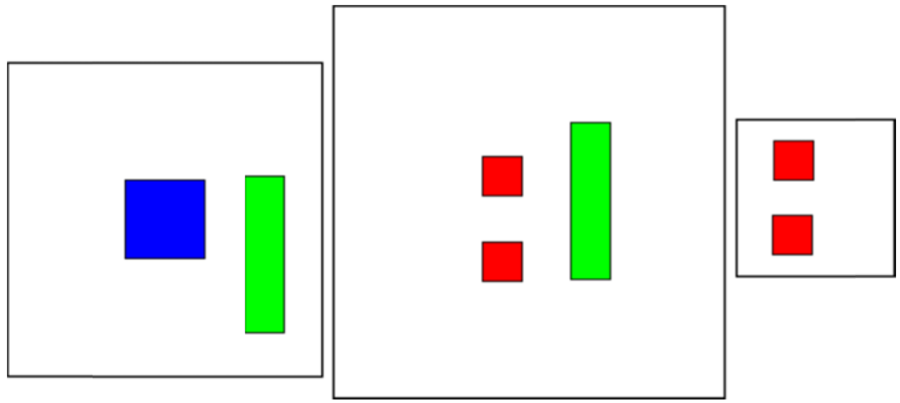
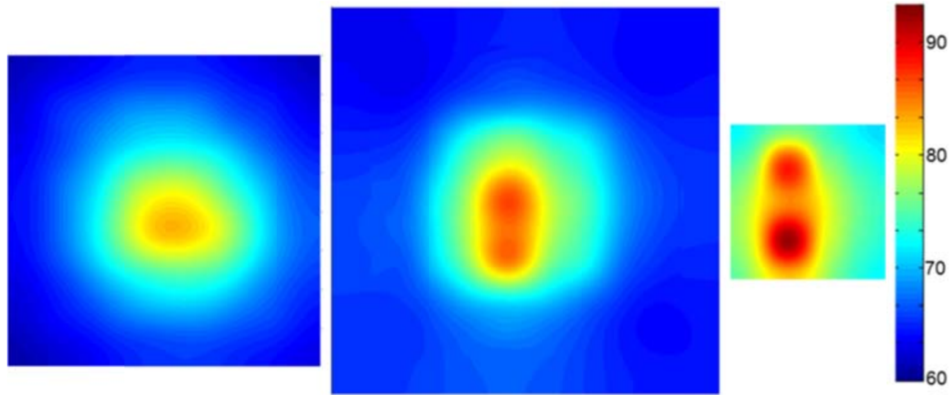


Figure 3.6 Comparison of temperature determined from the analytical model with finite-element simulation results along the cross-section lines shown in Figure 3.5.

As further illustration of the model presented above, the temperature field in an unequally-sized three-die stack with a more complicated power map was computed. The power map, shown in Figure 3.7 is representative of a typical multi-core microprocessor that combines computing capability with graphics. In this case, the four cores were assumed to be distributed in die 2 and 3, whereas the graphics processing unit (GPU) was located in die 1. The temperature map for this floorplan was computed using the model presented in this section, and is shown in Figure 3.7. The temperature map clearly shows the influence of the cores that have the highest power density among all heat-generating blocks. In addition, the close proximity of cores with each other, particularly inter-die proximity is also seen to cause an increase in temperature. For minimizing temperature rise, not only do the cores have to be physically separated within each die, but also in adjacent die. By moving two cores to die 1 which is closer to heat sink and avoiding the overlap of hot spots in two adjacent die as shown in Figure 3.8 the maximum temperature and also overall temperature decrease significantly. This underlines the application of the model presented above to computation of temperature fields in unequally-sized die stacks.

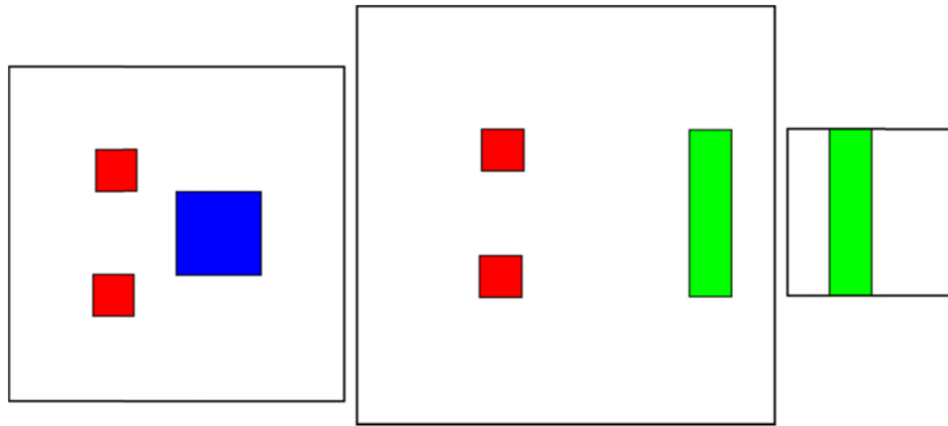


(a)

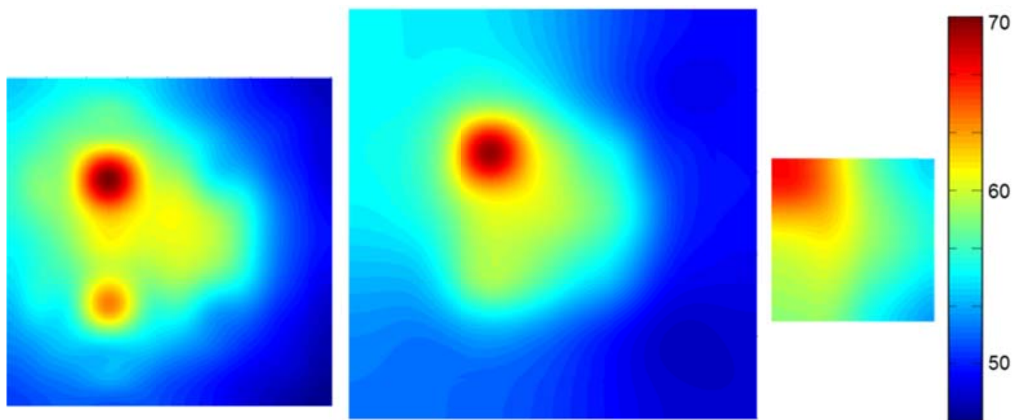


(b)

Figure 3.7 Computed temperature field in a three-die, unequally-sized stack with non-uniform heating (a) Thermal unfriendly power map,(b) temperature field



(a)



(b)

Figure 3.8 Computed temperature field in a three-die, unequally-sized stack with non-uniform heating,(a) Thermal friendly power map,(b) temperature field.

3.4. Application of Model for Comparison of Non-Uniformly Sized Die Stack with Uniform Die Stack

Unequally-sized die stacks are motivated primarily by the inherent manufacturing and electrical design benefits. However, it is important to compare the thermal performance of an unequally-sized die stack with an equivalent die stack with uniformly-sized die. In general, changes in the die footprint between adjacent die is likely to cause increased thermal resistance due to heat constriction and spreading [Lee *et al*., 1995]. Thus, the larger the degree of non-uniformity, the larger is the expected peak temperature. This is examined quantitatively using the model presented in section 3.2. Two unequally-sized three-die stacks with varying degree of non-uniformity are compared with an equivalent three-die stack with equally sized die. The equally-sized die is assumed to have die of size 10mm by 10mm. The first unequally-sized die stack is assumed to comprise of die of size 11mm by 11mm, 10mm by 10mm and 9mm by 9mm. The second unequally-sized die stack is assumed to comprise of die of size 13mm by 13mm, 10mm by 10mm and 6mm by 6mm. The total silicon area is roughly the same in each case. One hotspot of the power 3.3W and size 1mm by 1mm is assumed on each die for the three cases considered here. Figure 3.9 shows the temperature along a line passing through the hotspot on die2 in each of the three cases. Both cases of non-uniform die stacks exhibit higher temperature than the uniform die stack. In addition, the peak temperature is higher for the die stack with the greater degree of non-uniformity in die size. This shows the effect of changes in die size among adjacent die on peak temperature in a die stack. This effect primarily occurs due to additional thermal resistance due to heat spreading and constriction as heat flows from one die to another.

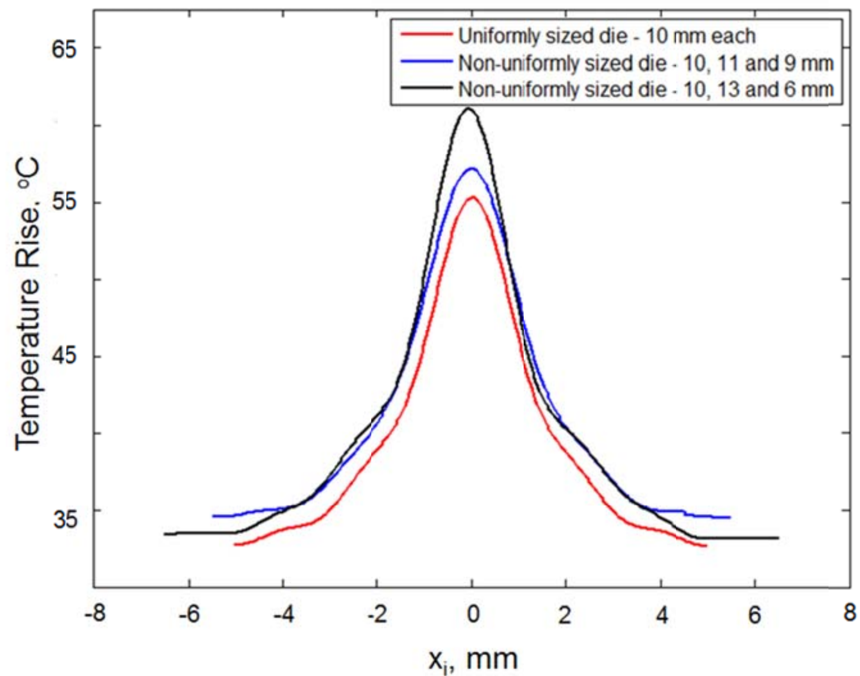


Figure 3.9 Comparison of temperature along the centerline of die2 for three cases of three-die stacks with different amounts of die size non-uniformity.

3.5 Conclusions

While stacking die with different size in a vertically-integrated 3D IC is attractive from design and manufacturing considerations, doing so introduces additional thermal spreading and constriction resistance in the multi-die stack. The model presented in this work provides an analytical tool for predicting the three-dimensional temperature field in a multi-die stack with an arbitrary number of unequally-sized die. The model shows that the larger the degree of non-uniformity in the die size, the larger is the temperature rise. Tools based on the model presented in this manuscript may be useful in rapid design iterations and in thermal-electrical optimization of unequally-sized 3D ICs.

Chapter 4

Analytical Modeling of Temperature Distribution in Interposer-Based Microelectronic Systems

4.1 Introduction

Three-dimensional integrated circuits (3D IC) technology refers to the vertical integration of multiple transistor planes using through-silicon vias (TSVs) and inter-substrate bonding [Pozder *et al*., 2007; Banerjee *et al*., 2001]. Such integration offers several electrical benefits including reduced interconnect length, increased design flexibility, etc. [Savidis *et al*., 2010]. While there is much research currently under way for the design and development of a multi-die 3D IC stack, the semiconductor industry is also investigating technologically much less aggressive products that do not involve complete 3D integration. An interposer-based system is one such example, and is often referred to as 2.5D integration [Knickerbocker *et al*., 2012 ; Rau *et al*., 2011; Lau *et al*., 2011]. An interposer is essentially a large substrate capable of carrying several die on it. These dies are bonded on the interposer substrate which facilitates inter-die electrical communication through interconnects embedded in the interposer and through bond pads in the bond layer between the interposer and each die. As a packaging technology, interposers are an alternative to System-on-Chip (SoC) [Wolf *et al*., 2002] and System-in-Package (SiP) [Tummala *et al*., 2001] technologies, and offer several advantages over these traditional technologies. For example, interposers lead to much greater design flexibility. A functional module may need to be designed and manufactured only once and may then be dropped on a variety of interposer products for different applications. Compared to wire bonds, the interconnect delay is also expected to be significantly reduced.

One of the foremost technological challenges in interposer technology is the development of a fundamental understanding of thermal transport in the interposer. Due to the presence of heterogeneous materials and multiple heat sources – some of which may overlap with each other – it is important to develop analytical methods to predict the temperature field in interposer systems. Analytical methods offer a much better fundamental understanding of heat transfer compared to finite-element based simulations. Analytical methods lend themselves better to parametric design analysis. Moreover, analytical methods for predicting the temperature field are easier to interface with electrical design tools. Such integration may significantly improve thermal performance of interposer systems by facilitating thermal-friendly pre-silicon design.

Thermal management of 3D ICs has been recognized as a significant challenge of this technology [Jones, 2007]. A number of papers have investigated thermal management of 3D ICs during the recent past years [Jain *et al*., 2010; Jain *et al*., 2011; Choobineh *et al*., 2012; Venkatadri *et al*., 2011] Analytical heat transfer models for multi-die 3D IC stacks have been proposed [Venkatadri *et al*., 2011]. Experimental measurements of thermal performance of 3D IC systems have also been reported [Colgan *et al*., 2012; Oprins *et al*., 2012].

This chapter considers thermal conduction in a general interposer system and outlines an analytical method to predict the three-dimensional temperature distribution in the interposer as a function of heat generation in the interposer and overlying dies. Results are found to be in excellent agreement with finite-element simulations. The analytical model is used to illustrate several design scenarios expected to arise in interposer technology. The next section describes the analytical model. Section 4.3 discusses an implementation of the model and presents thermal profiles of several design cases using the analytical model.

4.2 Steady-State Heat Conduction Model

The interposer based system consists of *N* heterogeneous chips on a substrate. The substrate dimension is a by b by c and every chip is a cuboid of size a_i by b_i by *ci* for each *i=1, 2.., N*. Figure 4.1 shows the x-z and x-y cross-sections of the geometry under consideration. A heat sink is assumed to be attached to the bottom of the substrate, which is modeled using a convective boundary condition. While there are other all side surfaces are assumed to be adiabatic. $Q_i(x,y)$ is the known heat generation that occurs at the top of the ith chip and $Q_{int}(x,y)$ is the known heat generation at the top surface of the interposer. Note that $Q_i(x,y)$ and $Q_{int}(x,y)$ utilize different frames of reference as shown in Figure 4.1. The primary interest is in determining the temperature fields $T_{int}(x,y,z)$ in substrate and Ti*(x,y,z)* for i=1, 2,…, N in every chip.

This problem is solved in an iterative fashion. Schematics of substrate and single chip heat transfer problems is shown in Figure 4.2.The total heat flux entering the substrate is the sum of $Q_{int}(x,y)$ and heat flux entering from each of the N die. This heat flux field is first guessed, and the guessed field is iteratively improved until reasonable accuracy is reached. Assuming that the guessed value of the heat flux field entering the interposer is $q_{g,int}(x,y)$, and the governing energy equation for the interposer is

$$\frac{\partial^2 T_{\text{int}}}{\partial x^2} + \frac{\partial^2 T_{\text{int}}}{\partial y^2} + \frac{\partial^2 T_{\text{int}}}{\partial z^2} = 0 \qquad (1)$$

Boundary conditions in x and y directions are

$$\frac{\partial T_{\text{int}}}{\partial x} = 0 \text{ at } x = 0, a \qquad (2)$$

$$\frac{\partial T_{\text{int}}}{\partial y} = 0 \text{ at } y = 0, b \qquad (3)$$

Boundary conditions in z direction are

$$\frac{\partial T_{\text{int}}}{\partial z} = -\frac{1}{k_{\text{int}}} q_{g,\text{int}}(x, y) \quad \text{at} \quad z = c \tag{4}$$

$$\frac{\partial T_{\text{int}}}{\partial z} = -\frac{h}{k_{\text{int}}} T_{\text{int}} \quad \text{at} \quad z = 0 \tag{5}$$

This problem is solved by utilizing Fourier cosine series expansion [Ozisik, 1989]. Briefly, the temperature field is written as a two-variable infinite series comprising products of the eigenfunctions in x and y directions. The coefficients of the infinite series are determined by using the non-homogeneous boundary condition in z direction and comparing the coefficients with corresponding coefficients in the two-variable Fourier cosine series expansion of the non-homogeneous term. The solution for the temperature field $T_{int}(x,y,z)$ is as follows:

$$T_{\text{int}}(x,y,z) = d_0\left(z + \frac{k}{h}\right) + \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} d_{nm} \cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)\left[\cosh(\gamma_{nm} z) + \frac{h}{k\gamma_{nm}}\sinh(\gamma_{nm} z)\right] \tag{6}$$

where

$$\gamma_{nm} = \sqrt{\left(\frac{n\pi}{a}\right)^2 + \left(\frac{m\pi}{b}\right)^2} \tag{7}$$

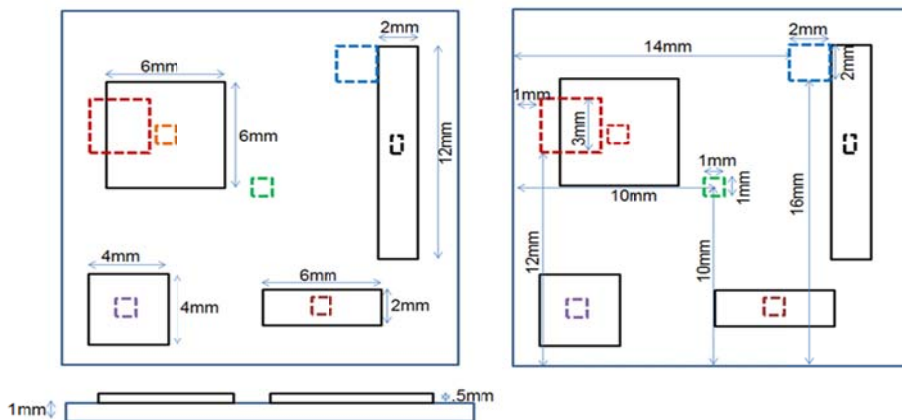


Figure 4.1 Schematics of the top and side views of interposer-based 2.5D system.

The coefficients d_0 and d_{nm} are given by

$$d_0 = \frac{1}{abk_{\text{int}}} \int_0^b \int_0^a q_{g,\text{int}}(x, y) dxdy \tag{8}$$

$$d_{nm} = \frac{\delta_{nm}}{abk_{\text{int}} P_{nm}} \int_0^b \int_0^a q_{g,\text{int}}(x, y) \cos\left(\frac{n\pi x}{a}\right) \cos\left(\frac{m\pi y}{b}\right) dxdy \tag{9}$$

where

$$p_{nm} = \gamma_{nm} \sinh(\gamma_{nm} c) + \frac{h}{k_{\text{int}}} \cosh(\gamma_{nm} c) \tag{10}$$

δ_{nm} is 0 when both n and m is equal to *0*, when only one of them is equal to *0* it is *2* and otherwise it is *4*. The interposer temperature field is obtained and then utilized to determine the temperature field at the bottom of each die. In case of perfect thermal contact between the interposer and die, the temperature at bottom of each die is the same as the temperature at the top of the interposer at the same location. In reality, there is likely to be a thermal contact resistance $R_i(x,y)$ due to the presence of a bonding layer between the ith die and interposer. In such a general case, the temperature at the bottom of each die, represented as $T_{0i}(x, y)$ is given by

$$T_{0,i}(x, y) = T_{\text{int}}(x, y, z = c) + q_{g,\text{int}}(x, y) \cdot R_i(x, y) \tag{11}$$

The thermal conduction problem for each of the die thus reduces to one in which the bottom temperature is specified, while the top face experiences a known heat flux. The side walls are adiabatic, as commonly used assumption.

Mathematically, the problem may be written as

$$\frac{\partial^2 T_i}{\partial x^2} + \frac{\partial^2 T_i}{\partial y^2} + \frac{\partial^2 T_i}{\partial z^2} = 0 \tag{12}$$

Subject to the boundary conditions

$$\frac{\partial T_i}{\partial x} = 0 \quad \text{at } x = 0, a_i \tag{13}$$

$$\frac{\partial T_i}{\partial y} = 0 \quad \text{at} \quad y = 0, b_i \tag{14}$$

$$T_i(x, y) = T_{0,i}(x, y) \quad \text{at} \quad z{=}c \tag{15}$$

and

$$\frac{\partial T}{\partial z} = \frac{1}{k} q_i(x, y) \quad \text{at} \quad z{=}0 \tag{16}$$

The solution is given by

$$T_i(x, y, z) = \begin{array}{c} d_{A0} + d_{B0}(z - c_i) + \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} d_{A,nm} \cos(\frac{n\pi x}{a_i}) \cos\left(\frac{m\pi y}{b_i}\right) \cosh(\gamma_{nm} z) + \\ \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} d_{B,nm} \cos\left(\frac{n\pi x}{a_i}\right) \cos\left(\frac{m\pi y}{b_i}\right) \sinh(\gamma_{nm}(z - c_i)) \end{array} \tag{17}$$

where $\gamma_{nm} = \sqrt{\left(\frac{n\pi}{a_i}\right)^2 + \left(\frac{m\pi}{b_i}\right)^2}$

(18)

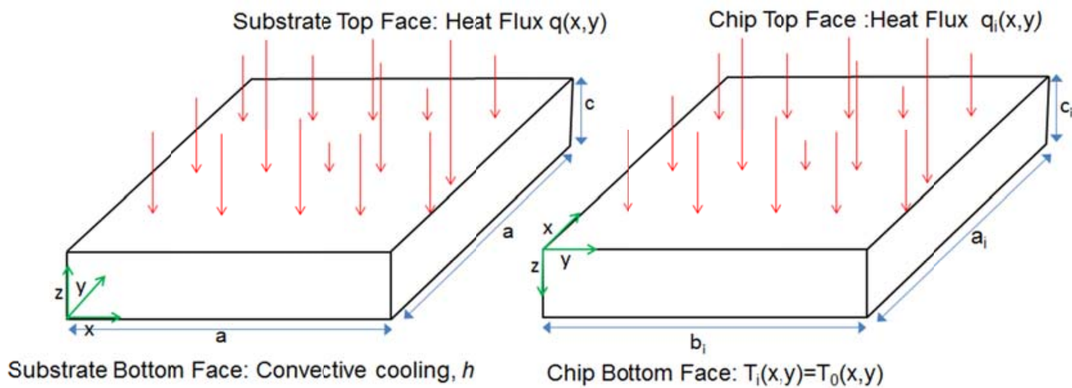


Figure 4.2 Schematics of substrate and single chip heat transfer problems solved in section 4.2. In each case, the four side walls are adiabatic.

The coefficients $d_{A,0}$, $d_{B,0}$, $d_{A,nm}$ and $d_{B,nm}$ are given by

$$d_{A,0} = \frac{1}{a_i b_i} \int_0^{b_i} \int_0^{a_i} T_{0,i}(x,y) dxdy \tag{19}$$

$$d_{B,0} = \frac{1}{a_i b_i k} \int_0^{b_i} \int_0^{a_i} q_i(x,y) dxdy \tag{20}$$

$$d_{A,nm} = \frac{\delta_{nm}}{a_i b_i \cosh(\gamma_{nm} c_i)} \int_0^{b_i} \int_0^{a_i} T_{0,i}(x,y) \cos\left(\frac{n\pi x}{a_i}\right) \cos\left(\frac{m\pi y}{b_i}\right) dxdy \tag{21}$$

$$d_{B,nm} = \frac{\delta_{nm}}{a_i b_i k p_{nm}} \int_0^{b_i} \int_0^{a_i} q_i(x,y) \cos\left(\frac{n\pi x}{a_i}\right) \cos\left(\frac{m\pi y}{b_i}\right) dxdy \tag{22}$$

where

$$p_{nm} = \gamma_{nm} \cosh(\gamma_{nm} c_i) \tag{23}$$

Once the temperature fields in the substrate and each die are computed, an iterative scheme is used to update the guessed heat flux fields $q_{g,int}(x,y)$ and repeat the process until reasonable convergence and accuracy are obtained. $q_{g,int}(x,y)$ is updated as follows:

$$q_{g\,\text{int},\,new}(x,y) = (-1)k \left(\frac{\partial T_i}{\partial z_i}\right)_{z=c_i} \tag{24}$$

$$q_{g,\text{int}}(x,y) = w q_{g,\text{int}}(x,y) + (1-w) q_{g\,\text{int},new}(x,y) \tag{25}$$

In practice, a weighted average of the newly updated value $q_{gint,new}(x,y)$ and the older value $q_{g,int}(x,y)$ is computed and used for the next iteration. This approach ensures numerical stability of the iterative procedure. A weighing function of $w=0.5$ is found to

provide sufficient stability in all simulations presented in this chapter. The iterative computations are carried out until the difference in the computed temperature fields between two successive iterations is reasonably small.

4.3 Model Results

The analytical model outlined in section 4.2 is used to solve the temperature profile in an interposer based integration with N=4. The top view of the geometry is shown in Figure 4.1. The substrate is assumed to be 20mm by 20mm by 1mm and four chips are assumed to be 4 mm by 4mm by 0.5mm, 6mm by 6mm by 0.5mm, 2mm by 12mm by 0.5mm and 6mm by 2mm by 0.5mm respectively. Three hotspots are assumed at top face of substrate and a single hotspot is assumed at top face of every chip. The heat sink at the bottom of substrate is modeled with a convective heat transfer coefficient of 5000W/m2K. The substrate thickness is 1mm and each chip is assumed to be 0.5mm thick. The thermal conductivity of silicon is 150W/mK, which is independent of space and temperature.

Double integrals in equations (8)-(9) and (19)-(22) are evaluated using a two-dimensional Gauss quadrature [Hamming *et al.*, 1986]. Figure 4.3 shows the predicted temperature rise at the center of top surface of substrate as a function of the number of terms included in the double summations in equations (6) and (17). It is seen that with only around 25 terms, the predicted temperature value reaches close to the eventual value with an error of less than 2%. Thus, limiting the double summations to only the first 25 terms significantly reduces computation time without affecting accuracy.

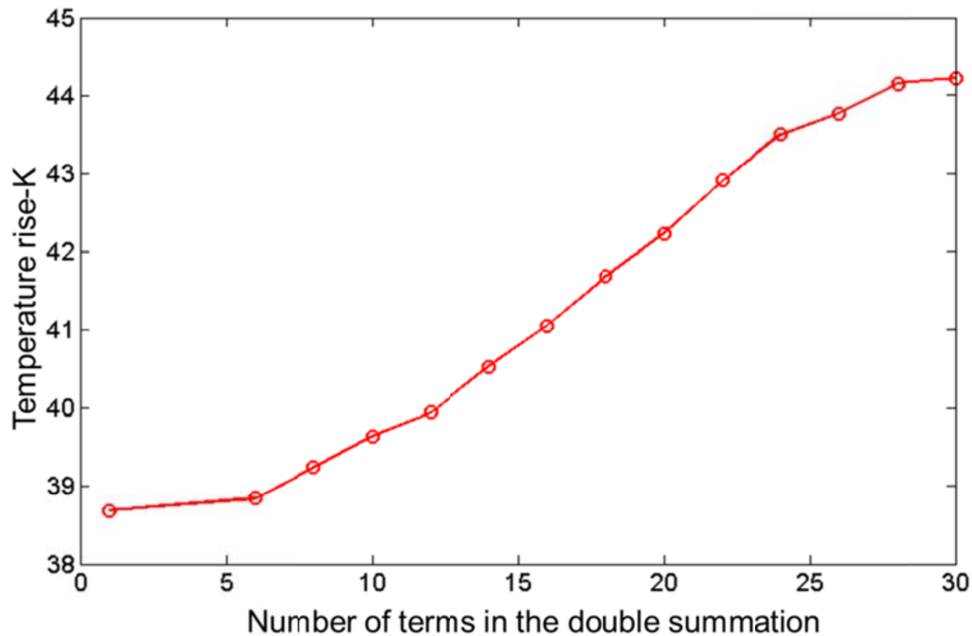


Figure 4.3 Effect of the number of terms considered in the double summation on accuracy of temperature computation.

Figure 4.4 plots the computed temperature along a line passing through the center of chip 1 at top surface of substrate as a function of the number of iterations employed, following the procedure described in section 4.2. The solution becomes stable within 7-8 iterations. Beyond the seventh iteration, the difference in the temperature field between successive iterations is less than 0.1%. As a result, the solutions described in this paper were computed using only 8 iterations. This contributes to reduction of computation time without sacrificing quality of results.

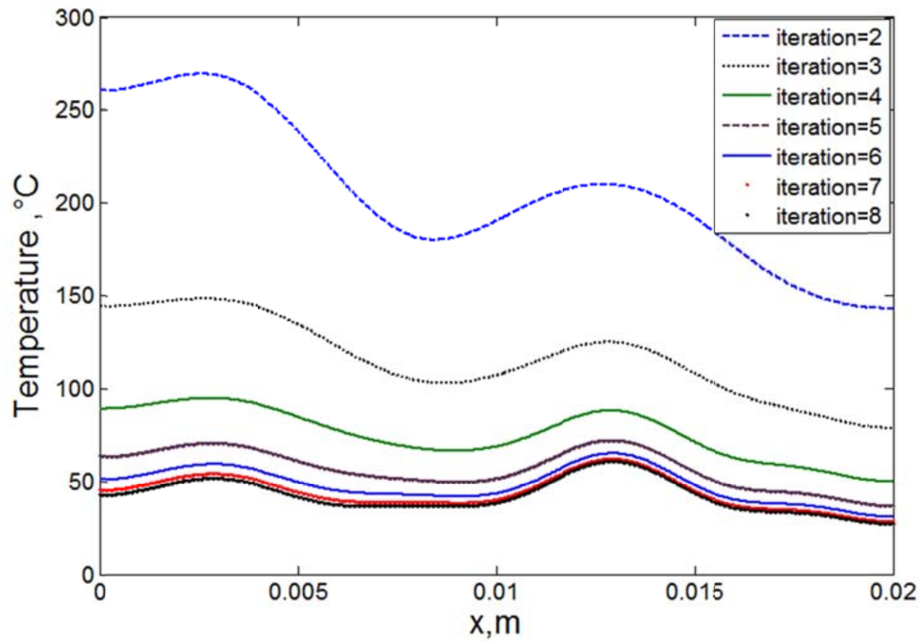


Figure 4.4 Effect of the number of iterations on temperature computation accuracy.

Based on the computational simplifications discussed above, the temperature field on an interposer base integration described above is computed and compared with finite-element simulation results. Figure 4.5 shows the temperature field on the top surface of substrate predicted by the model. A plot of temperature along the line shown in Figure 4.5 is presented in Figure 4.6. There is good agreement of the computed temperature fields with finite-element simulations carried out in commercial software. Figures 4.5 and 4.6 validate the model presented in sections 4.2.

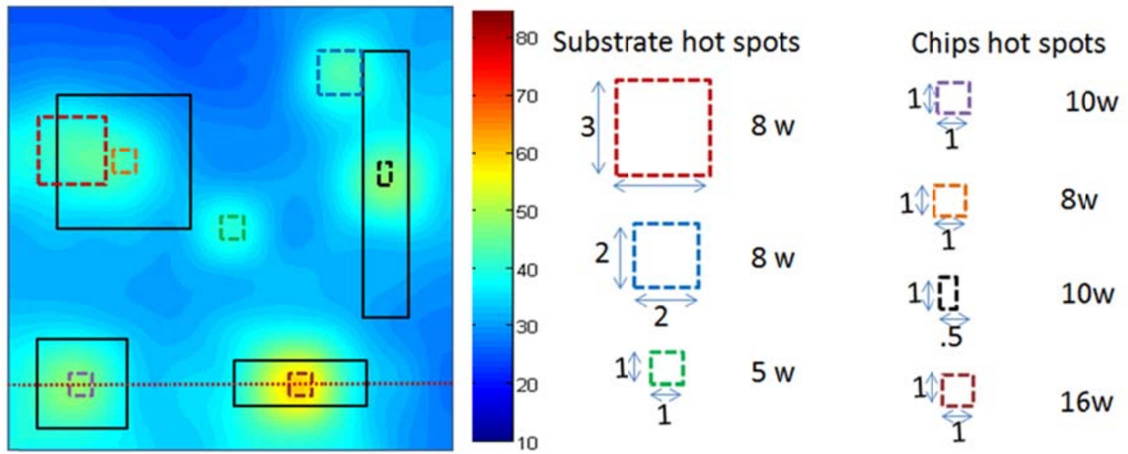


Figure 4.5 Temperature field on the top surface of substrate with a hotspot on each chip.

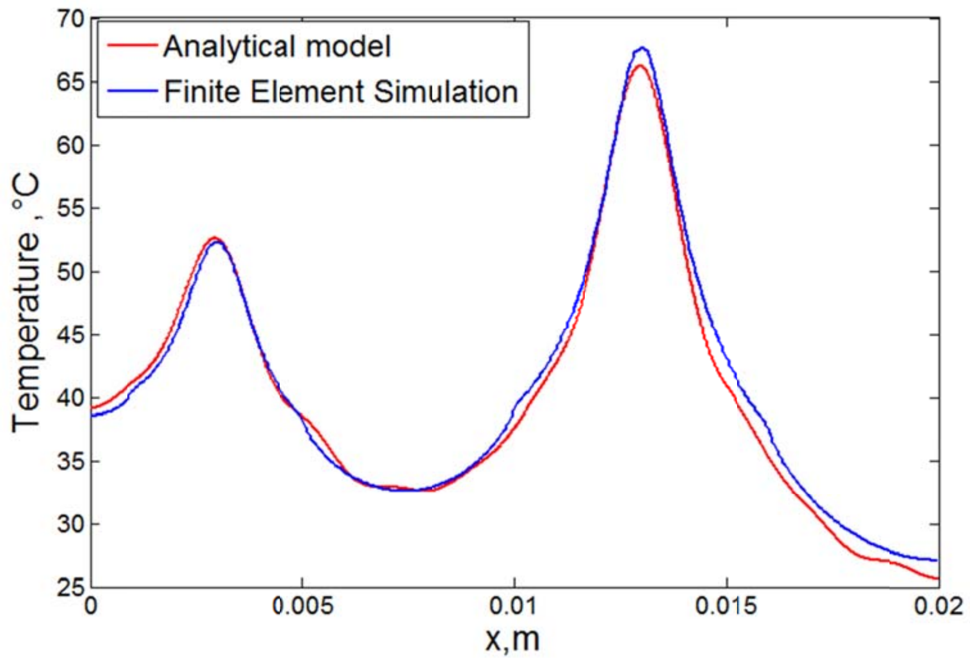


Figure 4.6 Comparison of temperature at top surface of substrate, determined from the analytical model with finite-element simulation results along the cross-section line shown in Figure 4.5.

In Figure 4.7, the effect of the location of chips on the temperature profile of substrate is studied and as shown in the Figure 4.7, when the chips are very close to each other, case(c), the average temperature at the top surface of substrate is the highest in comparison to other cases. In the case (a), the distance between chips is highest and they are located at the corners, the maximum temperature is more than other cases and the temperature field is less uniform. In order to decrease the maximum temperature and also have more uniform temperature field, it is better to have a configuration similar to case (b).

In Figure 4.8, the effect of the location of interposer hot spots on temperature field of substrate is studied. The results show that in order to decrease the maximum temperature and have more uniform temperature field, the location of substrate hot spots and chip hot spots should be different and not having overlap with each other. T in every figure indicates the temperature rise in comparison to the ambient.

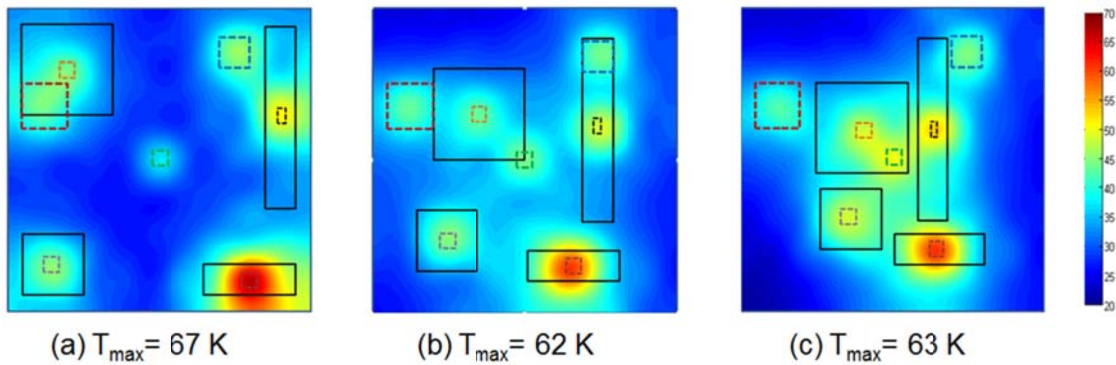


Figure 4.7 Computed temperature field at the top surface of substrate in different locations of chips. Power map is shown using hatched lines.

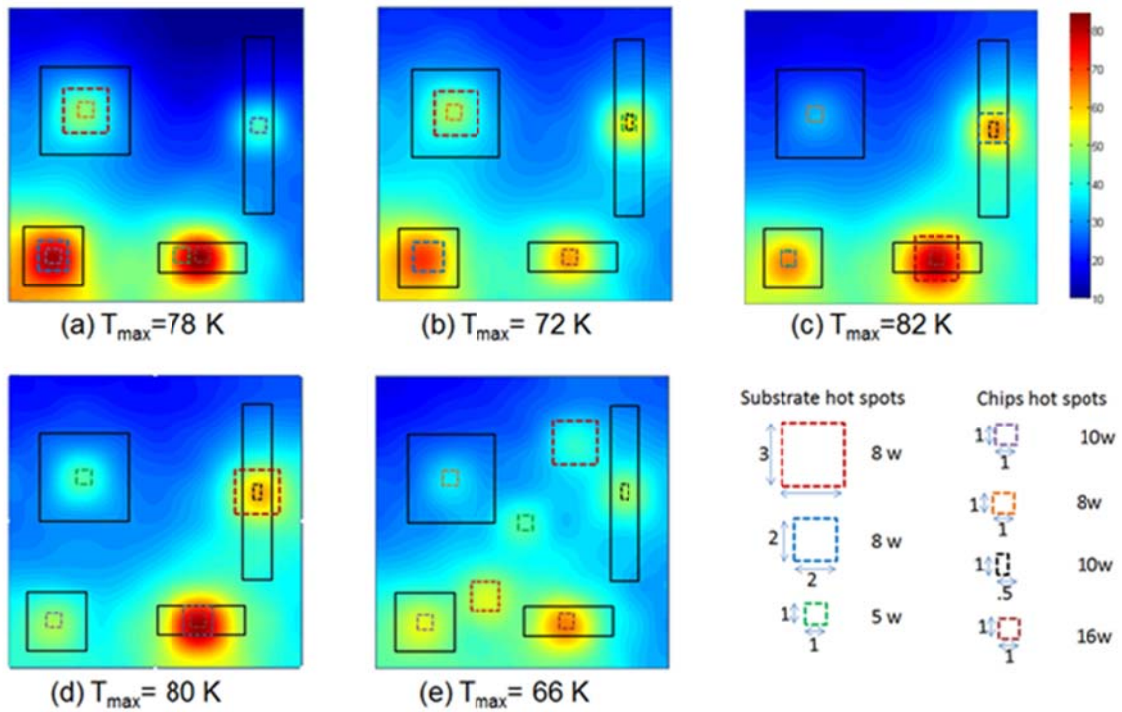


Figure 4.8 Computed temperature field at the top surface of substrate in different locations of substrate heat spots. Power map is showing using hatched lines.

In interposer based system, when the substrate heat fluxes are active it is called active interposer and when they are not active it is called passive interposer. In Figure 4.9, the effect of interposer hotspots on the temperature field at top surface of substrate has been studied. As it is shown in Figure 4.9, when the hotspots are active (case a) the maximum temperature and the overall temperature is more than the passive interposer (case b).

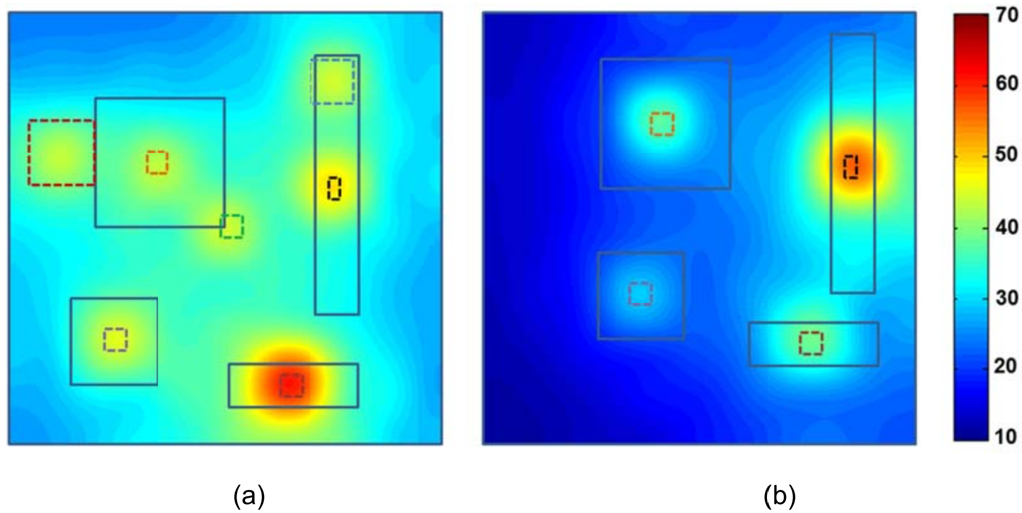


Figure 4.9 Computed temperature field at the top surface of substrate for (a) active interposer, (b) passive interposer.

4.4 Conclusions

In this chapter a general interposer system is introduced which consists of a substrate and N chips bonded on the top surface of the substrate. An analytical model is established to predict the temperature distribution in the substrate and chips as a function of heat generation in the substrate and chips. Results from the analytical model agree well with finite-element simulation. Several design cases for the location of chips and interposer hotspots are studied and the results illustrated that the best way to reduce the maximum and average temperatures, and to have more uniform temperature field in the substrate is by locating the chips not only far from each other but also far from the corners. The results from the case study of substrate hot spot locations shows that the best thermal design is by avoiding overlap with chips hotspot and keeping the hotspots as far away from each other as possible.

The analytical model presented in this work is expected to lead to a better fundamental understanding of the thermal performance of interposer-based 3D IC systems, and lead to helpful thermal design rules.

Chapter 5

An Explicit Analytical Model for Rapid Computation of Temperature Field in a Three-Dimensional Integrated Circuit (3D IC)

5.1 Introduction

3D integrated circuits (3-D ICs) technology is a promising approach for next-generation semiconductor microelectronics [Banerjee *et al*., 2001; Patti *et al*., 2006; Loh *et al*., 2007]. A 3D IC is formed by vertical interconnection of multiple substrates containing active devices [Topol *et al*., 2006]. 3D ICs offer reduced die footprint and interconnect length without requiring dimensional scaling of transistors [Li *et al*., 2010]. As a result, 3D ICs may result in similar performance benefits as dimensional scaling without the associated cost. One of the main technological challenges in 3D IC technology is in thermal management of a multi-die stack, and particularly in providing cooling to various substrates in the stack [Li *et al*., 2010]. While one side of a traditional 2D IC on a single substrate is typically available for heat removal, there is an inherent lack of direct contact with a heat sink for device layers in the middle of the stack. Utilization of through-substrate vias (TSVs) for cooling has been investigated widely [Goplen *et al*., 2006; Cong *et al*., 2007]. A number of microfluidics based approaches have been suggested for addressing this challenge [King *et al*., 2010; Kim *et al*., 2010; Brunschwiler *et al*., 2009; Wei *et al*., 2004; Khan *et al*., 2012; Brunschwiler *et al*., 2008 ; Tan *et al*., 2011].

An associated challenge in understanding and addressing thermal management in 3D ICs is to accurately and rapidly compute temperature fields in a 3D IC. This capability is important not only for cooling the 3D IC, but also to ensure optimal electrical performance. For example, the capability to predict peak temperature on each die in a 3D IC may be utilize to make smart decisions about load balancing and reallocation and

maximize electrical performance of the stack [Coplen *et al*., 2003]. Towards this, a 1D resistance network based thermal model has been proposed [Jain *et al*., 2010]. While this model highlighted important thermal phenomena that occur in 3D IC, its one-dimensional nature does not account for non-uniform heat generation on each die. Thermal network analysis for thermal design of the chip has been proposed and the effect of the area ratio of the interconnection in the interconnection layer on the maximum temperature is investigated. It also has been shown that in thermal network method the computational time is shorter than CFD method and it is very useful in parametric studies [Hatakeyama *et al*., 2010]. Thermal analysis of a typical 3D stack has been carried out using Finite Element simulations [Torregiani *et al*., 2009]. While numerical computations provide reasonable results, they have several disadvantages. Finite-element simulations are typically difficult to interface with traditional electrical design and analysis codes.

Heat transfer in a multi-layer structure with heating on top has been analyzed [Haji-Sheikh *et al*., 2003]. A thermal model for a 3D IC has been proposed by assuming heat generation to be volumetric in nature [Geer *et al*., 2007]. Iterative three-dimensional heat transfer models with non-uniform heat generation in each die for 3D ICs have been developed for uniformly-size die [Choobineh *et al*., 2012] as well as for unequally-sized die [Choobineh *et al*., 2013]. These models solve the underlying energy conservation equations in each die in an iterative fashion by guessing the heat transfer $Q_i(x,y)$ from one die to the adjacent die, and then using energy conservation equations to improve upon the guess until convergence. The analytical nature of these models contributes towards a fundamental understanding of the heat transfer problem. However, the iterative nature of these models increases computation speed. It is desirable to develop a non-iterative analytical model for computing the temperature field in a 3D IC.

An iterative three-dimensional heat transfer models with non-uniform heat generation in each die for 3D ICs was developed [Choobineh *et al*., 2012] and also temperature distribution in three-dimensional integrated circuits (3D ICs) with unequally-sized die was determined. [Choobineh *et al*., 2013]. Steady-state and transient temperature fields based on Fourier series expansion and Laplace transforms were studied respectively. The introduced models are faster than FEM-based models and more suitable to integrate with other electrical design simulations. While iterative models have been provided more accurate results in comparison to Finite Element simulation, it has also been recognized that a non-iterative analytical model would be faster and more accurate [Choobineh *et al*., 2012].

This chapter presents a non-iterative, analytical heat transfer model for computing three-dimensional temperature fields in a 3D IC. The governing energy equations with appropriate boundary conditions for N-die stack with different values of N are solved by first writing the solution in terms of infinite series, followed by deriving and solving ordinary differential equations for the coefficients in the series. Steady-state temperature fields predicted by this model compare well with FEM-based simulation results and previously developed iterative models. In addition, temperature computation based on the proposed models is much faster than numerical simulations or iterative approach. Section 5.2 describes the basic problem being addressed here, and outlines the solution methodology. Expressions for the temperature field are derived for perfect contact between layers (section 5.2.1) as well as for non-zero thermal resistance between layers (section 5.2.2). Accounting for non-zero thermal contact resistance is important, since such contact resistance is expected to exist between adjacent die in a 3D IC, and has been experimentally measured [Oprins *et al*., 2012; Matsumoto *et al*., 2011; Colgan *et al*., 2012]. Results from this model are compared with previous papers

for both accuracy and computation time. Several applications of the model are discussed in section 5.3. These include temperature computation for a 3D IC with a large number of strata, as well as the effect of inter-die thermal contact resistance. Results discussed in this chapter may find applications in development of tools for rapid thermal computation for 3D ICs.

5.2 Steady-State Thermal Conduction in a Multi-Die 3D IC

Figure 5.1 shows the front view of the N-die stack under consideration, and top view of one of the die. The die stack consists of *N* die, each die is a cuboid of size *a* by *b* by c_i. Thermal conductivity k_i of each die is assumed to be isotropic and temperature-independent. Heat removal from bottom-most die is modeled using a convective heat transfer coefficient *h*. All side surfaces and the top surface are assumed to be adiabatic. This is justified since the side surface area is small, and since typically, heat transfer from the top die, which is connected to the electronic package is insignificant. Spatially-varying heat generation $Q_i(x,y)$ is assumed to occur on the top surface of each die. The primary interest is in developing a model for rapidly computing the temperature fields $T_i(x,y,z)$.

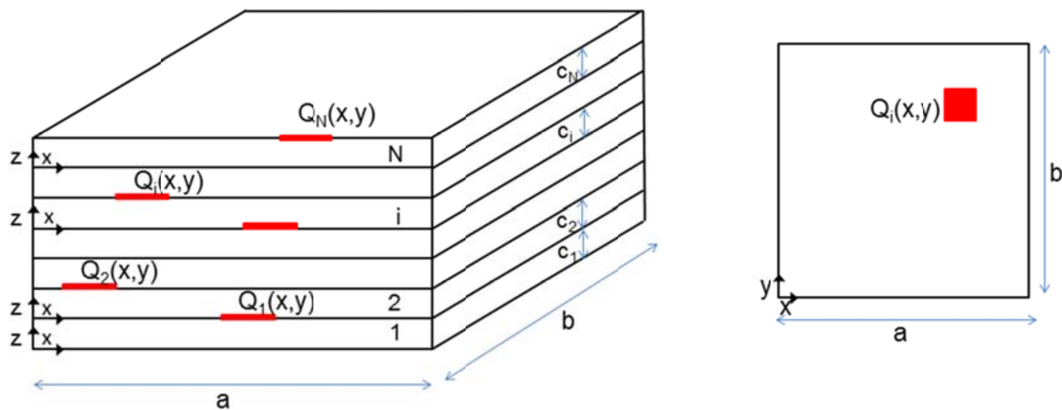


Figure 5.1 Schematic of the N-die stack, and a cross-section view of the ith die showing the heat generation distribution.

In this case, the governing energy conservation equation is

$$\frac{\partial^2 T_i}{\partial x^2}+\frac{\partial^2 T_i}{\partial y^2}+\frac{\partial^2 T_i}{\partial z^2}=0 \qquad (1)$$

Subject to boundary conditions

$$\frac{\partial T_i}{\partial x}=0 \quad \text{at} \quad x=0,a \qquad (2)$$

$$\frac{\partial T_i}{\partial y}=0 \quad \text{at} \quad y=0,b \qquad (3)$$

Boundary conditions in the z direction include heat flux condition at the top of the Nth die, and convective boundary condition at the bottom of the first die.

$$\frac{\partial T_1}{\partial z}=\frac{h}{k_1}T_1 \quad \text{at} \quad z=0 \qquad (4)$$

$$\frac{\partial T_N}{\partial z}=\frac{1}{k_N}Q_N(x,y) \quad \text{at} \quad z=c \qquad (5)$$

In addition, continuity of temperature and conservation of heat flux at the interfaces between adjacent die provide additional boundary conditions. Two specific cases are considered in the following sub-sections, one with perfect thermal contact between adjacent die, and one with a given thermal contact resistance between adjacent die.

5.2.1 Perfect Thermal Contact

In case of perfect thermal contact between adjacent die, the temperature of the two die at the interface must be equal.

$$T_{i+1}\big|_{z=0} = T_i\big|_{z=c_i} \qquad i=1,\ldots, N-1 \tag{6}$$

Further, energy conservation at the interface yields

$$k_i \frac{\partial T_i}{\partial z}\bigg|_{z=c_i} = Q_i(x,y) + k_{i+1}\frac{\partial T_{i+1}}{\partial z}\bigg|_{z=0} \qquad i=1,\ldots, N-1 \tag{7}$$

The governing equation represented by equations (1)-(7) is solved using Fourier cosine series expansion in the homogeneous x and y directions [Ozisik, 1989]. Similar to the approach outlined in a previous chapter the solution for the temperature field $T_i(x,y,z)$ is written as:

$$T_i(x,y,z) = a_{i,0}(z) + \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} a_{i,nm}(z)\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right) \tag{8}$$

This section presents an analytical approach to derive explicit expressions for the z-dependent coefficients $a_{i,0}(z)$ and $a_{i,nm}(z)$ that eliminates the need for iterative determination of the temperature fields using temperature and heat flux matching at the interfaces, as discussed in the previous chapter. To do so, the Fourier cosine series expansions of heat generation rates $Q_i(x,y)$ are first written as follows

$$Q_i(x,y) = b_{i,0} + \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} b_{i,nm}\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right) \tag{9}$$

where the coefficients $b_{i,0}$ and $b_{i,nm}$ may be determined as

$$b_{i,0} = \frac{1}{ab}\int_0^b\int_0^a Q_i(x,y)\,dxdy \tag{10}$$

$$b_{i,nm} = \frac{\delta_{nm}}{ab}\int_0^b\int_0^a Q_i(x,y)\cos(\frac{n\pi x}{a})\cos(\frac{m\pi y}{b})\,dxdy \tag{11}$$

where $\delta_{nm} = \begin{vmatrix} 0 & n=0; m=0 \\ 2 & n \neq 0; m=0 \\ 2 & n=0; m \neq 0 \\ 4 & n \neq 0; m \neq 0 \end{vmatrix}$

and $\gamma_{nm} = \sqrt{\left(\frac{n\pi}{a}\right)^2 + \left(\frac{m\pi}{b}\right)^2}$

To determine *$a_{i,0}(z)$* and *$a_{i,nm}(z)$*, the temperature field given in equation (8) is first substituted in the governing energy equation (1), which results in ordinary differential equations for *$a_{i,0}(z)$* and *$a_{i,nm}(z)$* and the solusion is given in equations (13) and (15)

$$a''_{i,0}(z) = 0 \tag{12}$$

$$a_{i,0}(z) = A_{i,0} + B_{i,0} z \tag{13}$$

$$a''_{i,nm}(z) = \gamma_{nm}^2 \tag{14}$$

$$a_{i,nm}(z) = A_{i,nm} \exp(\gamma_{nm} z) + B_{i,nm} \exp(-\gamma_{nm} z) \tag{15}$$

By substituting $a_{i,0}(z)$ and $a_{i,nm}(z)$ expressions, equations (13) and (15), in the temperature distribution equation (8) and applying boundary conditions in z direction, equation (6) and (7), the ordinary differential equations for finding coefficients *$A_{i,0}$* , *$B_{i,0}$* , *$A_{i,nm}$* and *$B_{i,nm}$*, would be provided and then by solving these equation the coefficients have been found .

$$a'_{1,0}(0) = \frac{h}{k_1} a_{1,0}(0) \tag{16}$$

$$k_N a'_{N,0}(c_N) = b_{0,N} \tag{17}$$

$$a_{i+1,0}(0) = a_{i,0}(c_i) \tag{18}$$

$$k_i a'_{i,0}(c_N) = b_{0,i} + k_{i+1} a'_{i+1,0}(0) \quad (19)$$

$$a'_{1,nm}(0) = \frac{h}{k_1} a_{1,nm}(0) \quad (20)$$

$$k_N a'_{N,nm}(c_N) = b_{N,nm} \quad (21)$$

$$a_{i+1,nm}(0) = a_{i,nm}(c_i) \quad (22)$$

$$k_i a'_{i,nm}(c_i) = b_{i,nm} + k_{i+1} a'_{i+1,nm}(0) \quad (23)$$

After solving the ordinary differential problems from equation (16) to (19) for $A_{0,i}$ and $B_{0,i}$, these coefficients would be

$$B_{0,N} = \frac{b_{0,N}}{k_N} \quad (24)$$

$$A_{0,i+1} = A_{0,i} + B_{0,i} c_i \qquad i=1,\ldots,N-1 \quad (25)$$

$$k_i B_{0,i} = b_{0,i} + k_{i+1} B_{0,i+1} \qquad i=1,\ldots,N-1 \quad (26)$$

$$B_{0,i} = \frac{1}{k_i} \sum_{i^*=i}^{N} b_{0,i^*} \qquad i=2,\ldots,N \quad (27)$$

$$A_{0,i} = \frac{1}{h} \sum_{i^*=1}^{N} b_{0,i^*} + \sum_{i^*=1}^{i} B_{0,i^*} c_{i^*} \qquad i=1,\ldots,N \quad (28)$$

Because of the complexity of equations (20) to (23) finding an explicit solution for $A_{i,nm}$ and $B_{i,nm}$ is not possible and a set of *2N* by *2N* equations should be solved implicitly by using matrix inversion method in order to find the coefficients and finally having the temperature distribution.

$$\gamma_{nm}(A_{1,nm} - B_{1,nm}) = (\frac{h}{k_1})(A_{1,nm} + B_{1,nm}) \tag{29}$$

$$k_N \gamma_{nm}(A_{N,nm}\exp(\gamma_{nm}c_N) - B_{N,nm}\exp(-\gamma_{nm}c_N)) = b_{N,nm} \tag{30}$$

$$A_{i+1,nm} + B_{i+1,nm} = A_{i,nm}\exp(\gamma_{nm}c_i) + B_{i,nm}\exp(-\gamma_{nm}c_i) \qquad \text{i=1,…,N-1} \tag{31}$$

$$k_{i+1}\gamma_{nm}(A_{i+1,nm} - B_{i+1,nm}) = k_i\gamma_{nm}[A_{i,nm}\exp(\gamma_{nm}c_i) - B_{i,nm}\exp(-\gamma_{nm}c_i)] - b_{i,nm} \quad \text{i=1,…,N-1} \tag{32}$$

When all the layers are the same material and thermal conductivity of all layers considered to be equivalent and equal to k, then the solution is simpler and it is as describe in the following part.

The coefficients in equations (13) and (15) are determined by applying the boundary conditions in z direction, equations (4) to (7), resulting in a set of *2N* equations in *2N* variables, i.e. $A_{i,0}$ and $B_{i,0}$, where *i=1,2,..,N*. By careful rearrangement of terms, the explicit analytical solution is derived to be

$$B_{i,0} = \sum_{i^*=i}^{N} \frac{b_{0,i^*}}{k} \qquad \text{i=1,…, N} \tag{33}$$

$$A_{i,0} = \frac{k}{h}\sum_{i^*=1}^{N} \frac{b_{0,i^*}}{k} + \sum_{i^*=1}^{i-1} c_{i^*}\left[\sum_{j=i^*}^{N} \frac{b_{j,0}}{k}\right] \qquad i=1,\dots, N \tag{34}$$

Similarly, an analytical solution for $A_{i,nm}$ and $B_{i,nm}$ is found by inserting the expression for $a_{i,nm}$ in equation (15) into the *z* boundary conditions. This result in

$$A_{i,nm}=\frac{\left[\left(\frac{b_N}{k\lambda_{nm}}\right)+\sum_{i^*=1}^{N-1} r_{i^*,nm}\exp(\gamma_{nm}\sum_{j=i^*+1}^{N} c_j)+\sum_{i^*=1}^{N-1} r_{i^*,nm}\exp(-\gamma_{nm}\sum_{j=i^*+1}^{N} c_j)\right]}{\left[\exp(\gamma_{nm}\sum_{i^*=1}^{N} c_{i^*})-P_{nm}\exp(-\gamma_{nm}\sum_{i^*=1}^{N} c_{i^*})\right]}\exp(\gamma_{nm}\sum_{i^*=1}^{i-1} c_{i^*})$$
$$-\sum_{i^*=1}^{i-1} r_{i^*,nm}\exp\left[\gamma_{nm}\sum_{j=i^*+1}^{i-1} c_j\right]$$

i=1,…,N (35)

$$B_{i,nm}=\frac{\left[\left(\frac{b_N}{k\lambda_{nm}}\right)+\sum_{i^*=1}^{N-1} r_{i^*,nm}\exp(\gamma_{nm}\sum_{j=i^*+1}^{N} c_j)+\sum_{i^*=1}^{N-1} r_{i^*,nm}\exp(-\gamma_{nm}\sum_{j=i^*+1}^{N} c_j)\right]}{\left[\exp(\gamma_{nm}\sum_{i^*=1}^{N} c_{i^*})-P_{nm}\exp(-\gamma_{nm}\sum_{i^*=1}^{N} c_{i^*})\right]}P_{nm}\exp(-\gamma_{nm}\sum_{i^*=1}^{i-1} c_{i^*})$$
$$+\sum_{i^*=1}^{i-1} r_{i^*,nm}\exp\left[-\gamma_{nm}\sum_{j=i^*+1}^{i-1} c_j\right]$$

i=1,…,N (36)

where

$$r_{i-1,nm}=\frac{b_{i-1}}{2k\gamma_{nm}} \quad (37)$$

$$P_{nm}=\frac{\gamma_{nm}k-h}{\gamma_{nm}k+h} \quad (38)$$

5.2.2 Non-Zero Thermal Contact Resistance between Interfaces

This sub-section considers the case where a non-zero thermal contact resistance R_i exists between the ith and $(i+1)^{th}$ die. In such a case, continuity at interfaces, described previously by equation (6) is modified to the following:

Figure 5.2 A model for thermal contact resistance between two adjacent die

$$T_{i+1}\big|_{z=0} = T_i\big|_{z=c_i} + q_{flow} R_i \qquad \text{for} \quad i=1,\ldots, N-1 \tag{39}$$

$$q_{flow} = kR_i \frac{\partial T_{i+1}}{\partial z}(z=0) \tag{40}$$

$$T_{i+1}\big|_{z=0} = T_i\big|_{z=c_i} + kR_i \frac{\partial T_{i+1}}{\partial z}(z=0) \qquad \text{for} \quad i=1,\ldots, N-1 \tag{41}$$

Similar to the perfect thermal contact presented in section 5.2.1, the temperature solution for this case is still governed by equation (8), with expressions for coefficients given by equations (13) and (15). An explicit expression for coefficients $A_{i,0}$, $B_{i,0}$ is given by

$$B_{i,0} = \sum_{i^*=i}^{N} \frac{b_{i^*,0}}{k} \qquad i=1,\ldots, N \tag{42}$$

$$A_{1,0} = \frac{1}{h} \sum_{i^*=1}^{N} b_{0,i^*} \tag{43}$$

$$A_{i+1,0} = \frac{1}{h} \sum_{i^*=1}^{N} b_{0,i^*} + \sum_{i^*=1}^{i} c_{i^*} \sum_{j=i^*}^{N} \frac{b_{j,0}}{k} + \sum_{i^*=1}^{i} kR_{i^*} \sum_{j=i^*+1}^{N} \frac{b_{j,0}}{k} \qquad i=1,\ldots, N-1 \tag{44}$$

Due to the added complexity in boundary condition equation (41), the coefficients $A_{i,nm}$ and $B_{i,nm}$ in equation (15) cannot be described explicitly. Instead, a set of 2N equations in unknowns $A_{i,nm}$ and $B_{i,nm}$ are derived using the z boundary conditions. The equations are

$$\gamma_{nm}(A_{1,nm} - B_{1,nm}) = (\frac{h}{k})(A_{1,nm} + B_{1,nm}) \tag{45}$$

$$k\gamma_{nm}(A_{N,nm}\exp(\gamma_{nm}c_N) - B_{N,nm}\exp(-\gamma_{nm}c_N)) = b_{N,nm} \tag{46}$$

$$A_{i+1,nm}(1-kR_i\gamma_{nm}) + B_{i+1,nm}(1+kR_i\gamma_{nm}) = A_{i,nm}\exp(\gamma_{nm}c_i) + B_{i,nm}\exp(-\gamma_{nm}c_i) \quad \text{i=1,…, N-1} \tag{47}$$

$$(A_{i+1,nm} - B_{i+1,nm}) = A_{i,nm}\exp(\gamma_{nm}c_i) - B_{i,nm}\exp(-\gamma_{nm}c_i) - \frac{b_{i,nm}}{k\gamma_{nm}} \quad \text{i=1,…, N-1} \tag{48}$$

A solution of equations (45)-(48) by using commonly available techniques such as matrix inversion results in solutions for the coefficients $A_{i,nm}$ and $B_{i,nm}$ and finally having the temperature distribution.

5.3 Results and Discussion

Based on the analytical method described in the previous section, the temperature field on a two-die stack is computed and compared with finite-element simulation results, and a previously reported iterative method [Choobineh *et al.*, 2012].

Each die of size 10mm by 10mm is assumed to have a 2.0W hotspot of size 1 mm by 1 mm, centered at (2.5mm, 2.5mm) for die1 and (7.5mm, 7.5mm) for die2 respectively. Heat dissipation is assumed to occur through a heat sink attached to die1. The heat sink is modeled using a convective heat transfer coefficient of 5000W/m^{2}K. A plot of temperature rise along a horizontal line passing through the hot spot centers is shown in Figure 5.3. The temperature field computed using the model presented in

Section 5.2.1 is in excellent agreement with finite-element simulations carried out in commercial software. The non-iterative model presented in this paper is found to be more accurate than the previously reported iterative model [Choobineh *et al*., 2012]. More importantly, the computation time for the non-iterative model is much lower than both finite-element simulations and the iterative model. This improvement is particularly significant when the number of die in the stack is larger than 10, making this model appropriate for rapid temperature computation for large, multi-die systems.

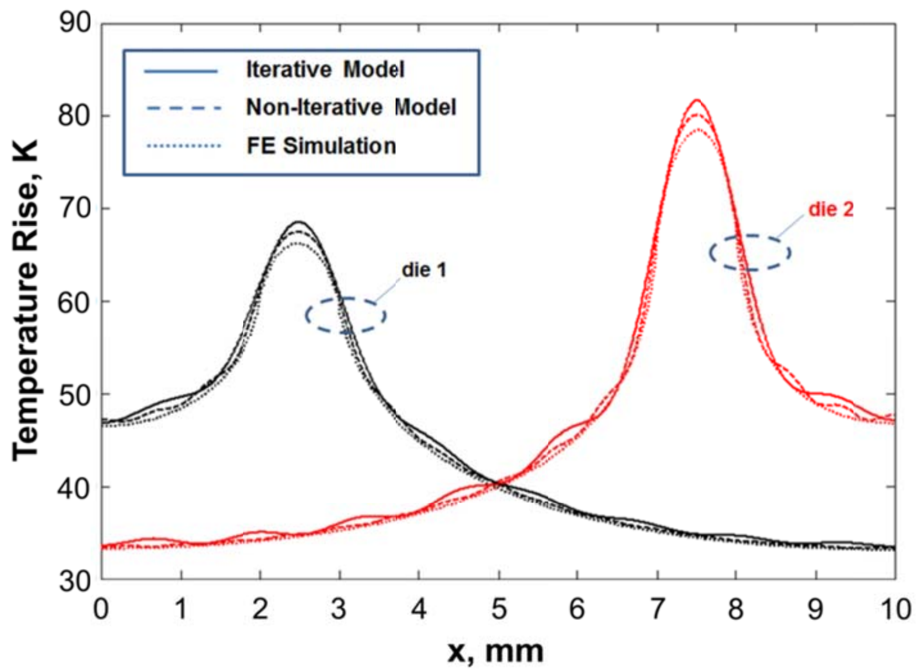


Figure 5.3 Comparison of temperature rise determined from the non-iterative model with iterative model [Choobineh *et al*., 2012] and finite-element simulation results along the cross-section lines in the middle of every hot spot.

Temperature plot in the center of hot spot of 2.0W power at top surface of fifth die for a ten die stack by using different values of number of terms included in the double summations in equations (8), is shown in Figure 5.4. It is found that using about 20

eigenvalues provides sufficient accuracy, and that further eigenvalues do not contribute significantly to the computed temperature value.

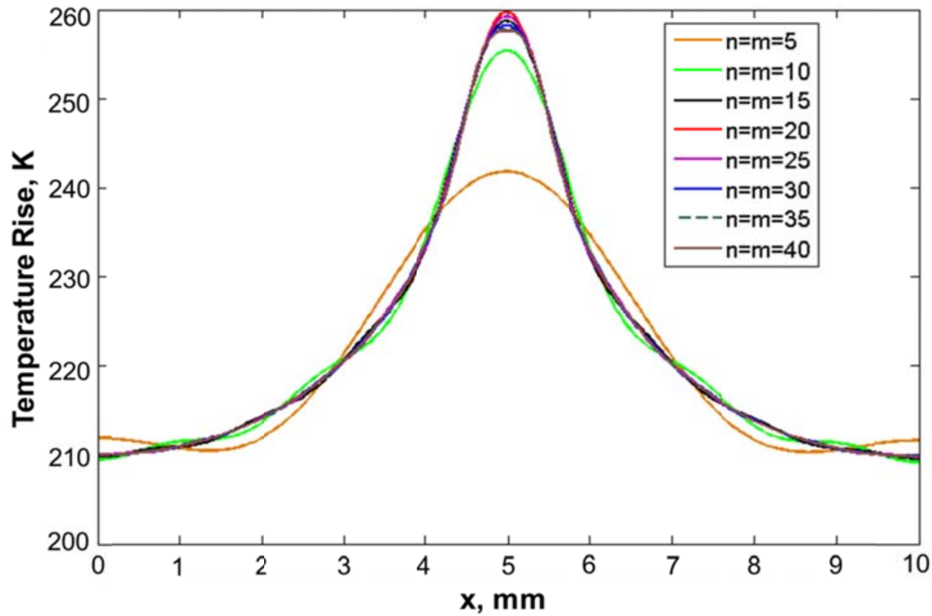


Figure 5.4 Temperature at top surface of fifth die in a ten-die case for different number of terms included in the double summations.

Figure 5.5 plots the maximum temperature rise in the 3D IC as a function of number of die in the stack. While the model is capable of accounting for any general heat generation distribution, in this case, a single hotspot of size 1mm by 1mm and power 2.0W is assumed to be present on each die. Two specific cases are considered – one in which the hotspots are vertically aligned with each other, and a second case in which the hotspots are alternatively staggered, as shown in Figure 5.5. As expected, the temperature increases rapidly as the number of die in the stack increases. Further, the temperature rise in the first case, where the hotspots are aligned, is greater than the

second case. This happens because of increased power density due to overlap of hotspots in the first case.

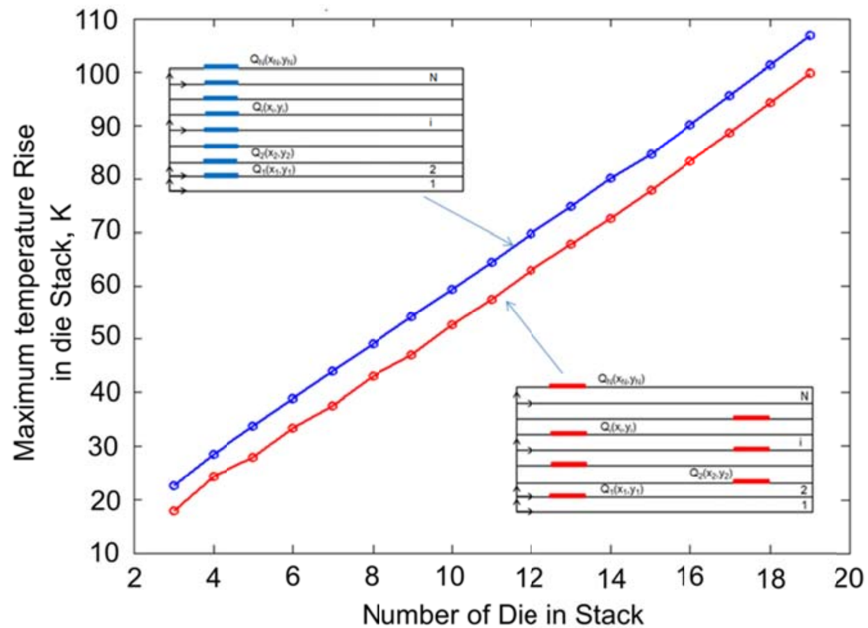


Figure 5.5 Maximum temperature rise in N-die stack as a function of number of die for two different cases.

Depending on the nature of integration, some thermal contact resistance may exist between adjacent die in a 3D IC stack [Oprins *et al*., 2012; Matsumoto *et al*., 2011; Colgan *et al*., 2012]. This thermal contact resistance may occur due to the presence of an underfill material around metal pillars that bond adjacent die together. In addition, a non-zero thermal contact resistance may also occur due to imperfect bonding between metal pads on adjacent die. Since thermal contact resistances are known to impact thermal characteristics of microsystems [Bozorg-Grayeli *et al*., 2013], it is important to carry out an evaluation of the effect of thermal contact resistance on the temperature field in a 3D IC stack. Figure 5.5 shows the temperature curve along a line passing through the

hotspot on die5 in a 10 die stack, where each die has an aligned, 2.0W hotspot of size 1mm by 1mm. This curve is plotted for a number of thermal contact resistance values, computed using the model presented in section 5.2.2. For comparison, the perfect thermal contact resistance model, presented in section 5.2.1 is also plotted. Figure 5.6 shows that, as expected, temperature rise increases as thermal contact resistance increases. This plot shows the importance of engineering the inter-die interface in order to reduce thermal contact resistance and hence reduce temperature rise

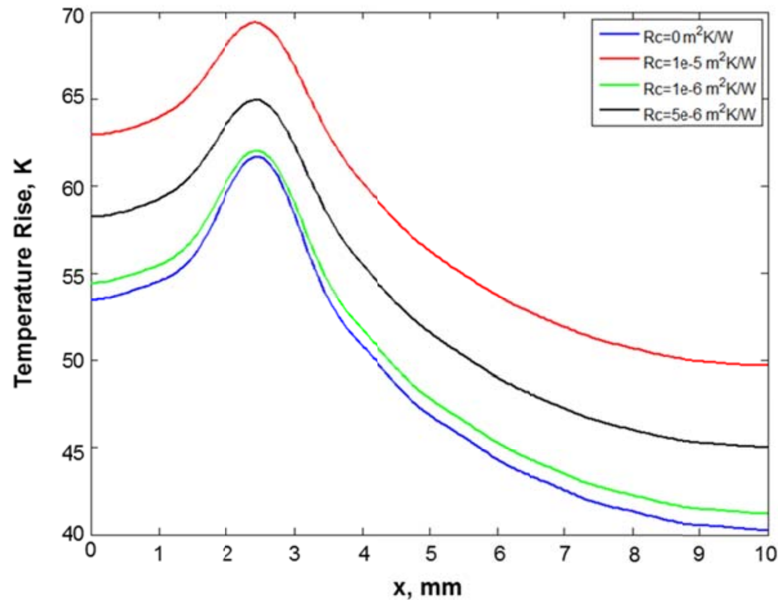


Figure 5.6 Temperature rise at top surface of die 5 for a ten-die stack case with different values of thermal contact resistance.

Further, the effect of the convective boundary condition at the bottom-most die is investigated. Figure 5.7 plots the peak temperature in a ten-die stack similar to the one considered in Figure 5.5 as a function of convective heat transfer coefficient. It is found that the maximum temperature in the ten-die stack decreases rapidly when convective heat transfer coefficient increases. The temperature reduction is significant at low values

of the convective heat transfer, but this effect diminishes somewhat as the heat transfer coefficient increases.

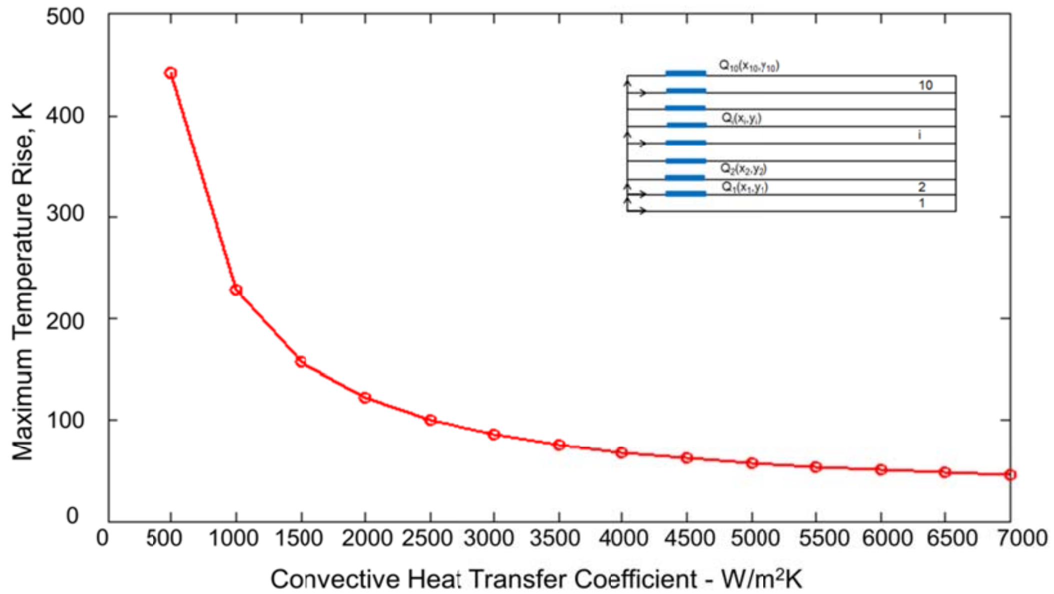
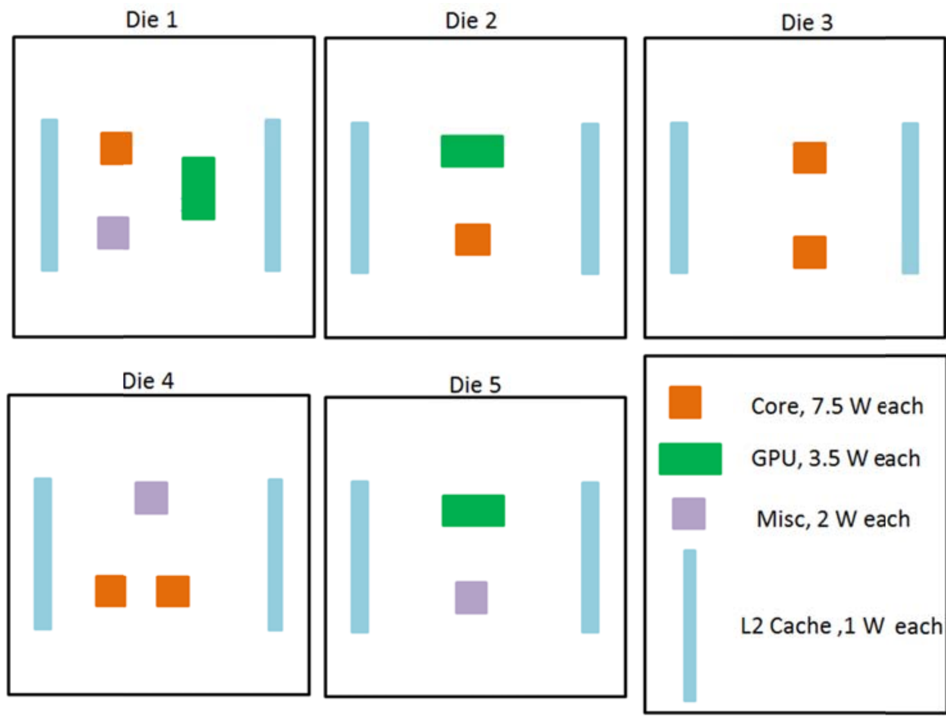
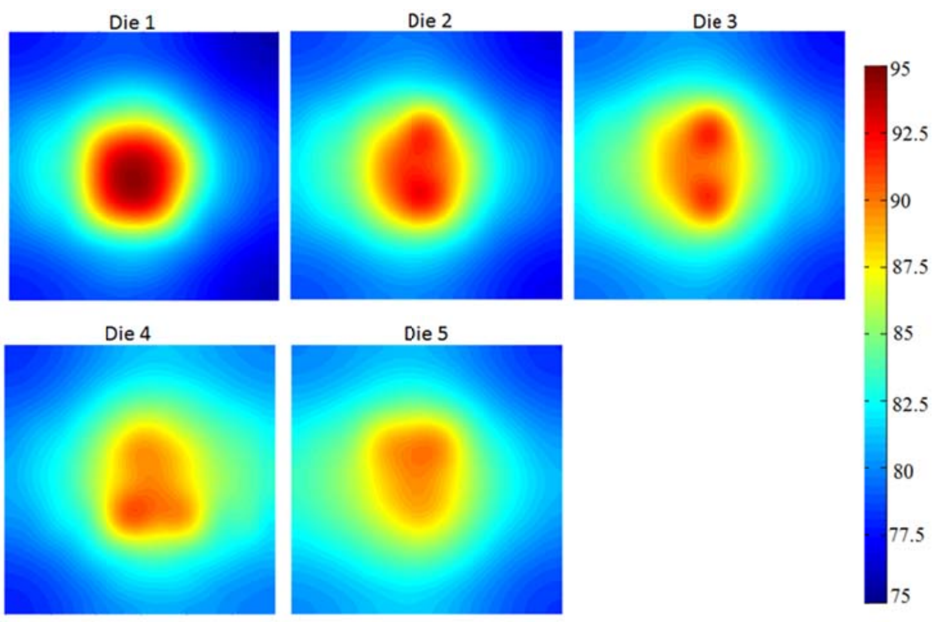


Figure 5.7 Maximum temperature rise at top surface of die 5 in a ten-die stack case with different values of convective heat transfer coefficient.

Finally, in order to demonstrate the capability of the analytical model, the temperature field for a 5-die case with non-uniform heat generation shown in Figure 5.8(b) and the related power map showed in Figure 5.8(a).

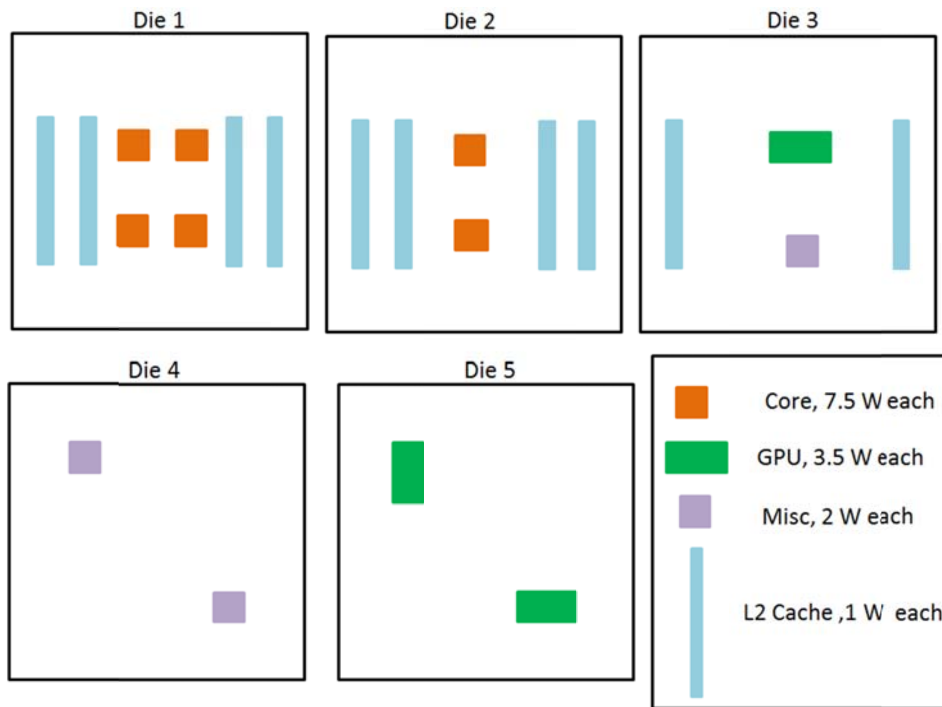


(a)

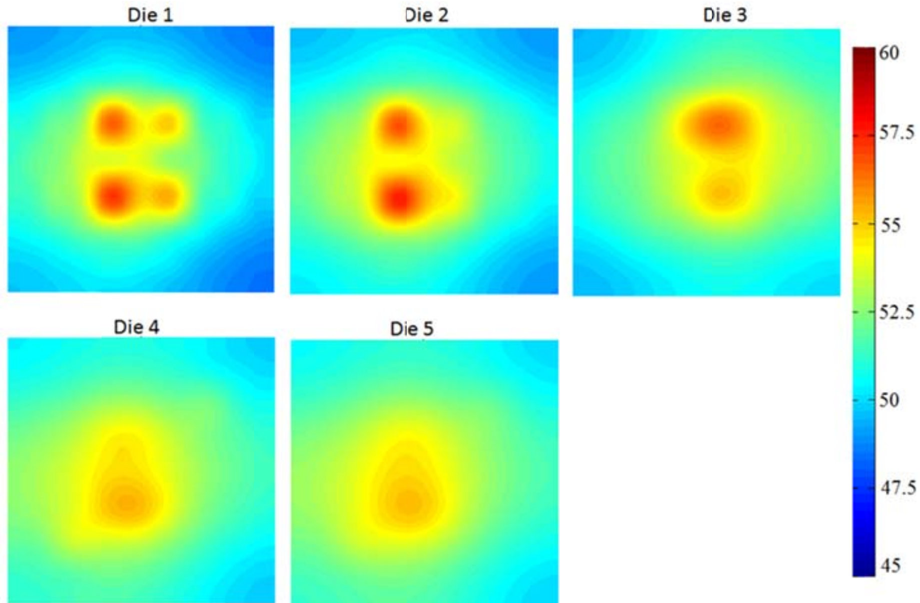


(b)

Figure 5.8 (a) thermally unfavorable Power map of a 5-die stack, (b) Computed temperature field for the power map.



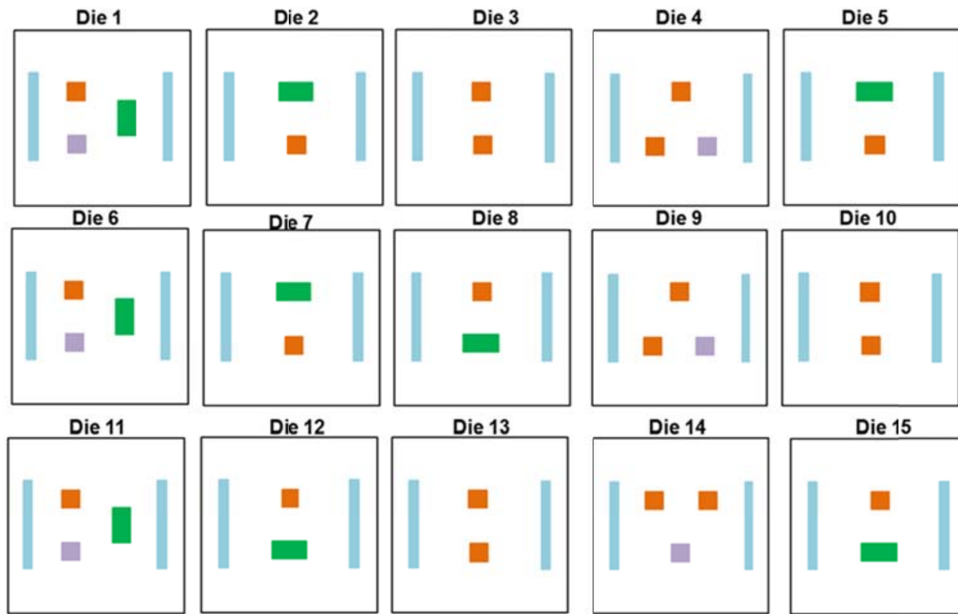
(a)



(b)

Figure 5.9 (a)Thermally favorable power map of a 5 - die stack, (b) Computed temperature field for the power map.

The temperature profile for a 15-die case with non-uniform heat generation on each die is computed. The heat generation profile for each die is shown in Figure 5.10(a). Each of the orange, blue, green and gray blocks corresponds to a heat generation rate of 75.0, 20.0, 17.5 and 4.0W/cm^2 respectively. The temperature field on each die is computed using the model presented in section 5.2.1. The computed temperature fields are shown in Figure 5.10(b) for each die. The temperature fields shown in Figure 5.10(b) take into account non-uniform heat generation rates in different blocks as well as their in-plane and out-of-plane proximity. The computation time for the model for a 15 die stack is about 170 seconds, which is much faster than both finite-element simulations as well as iterative models for temperature computation [Choobineh *et al.*, 2012].



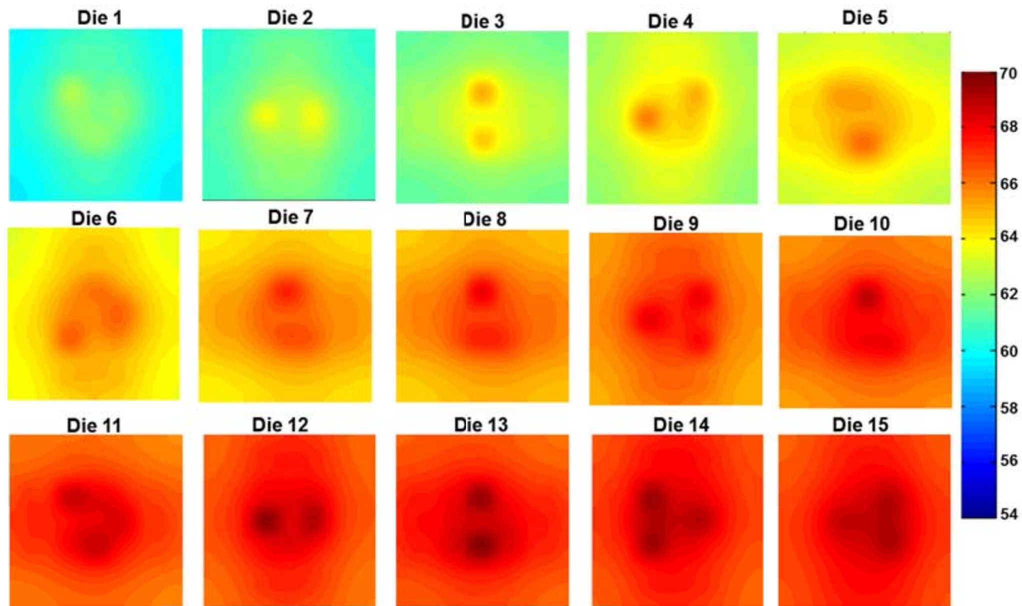
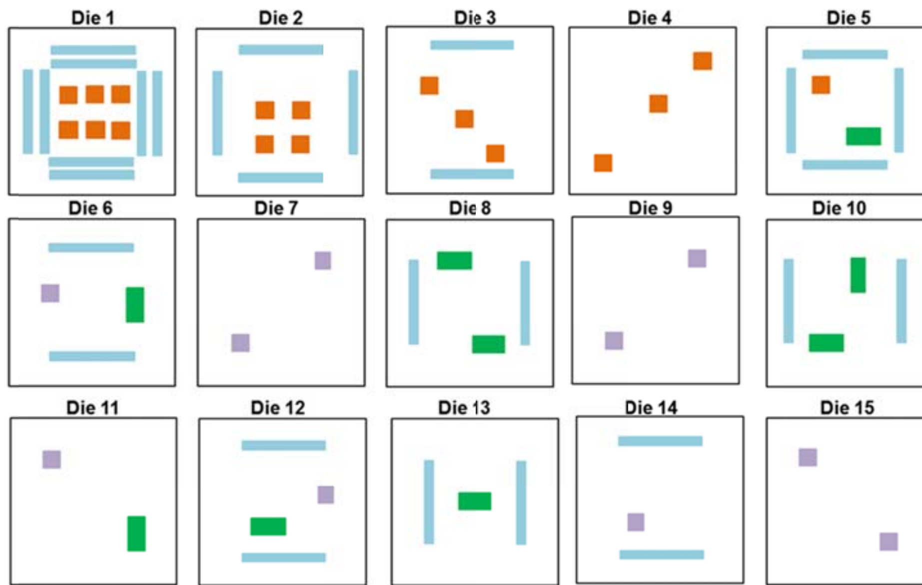


Figure 5.10 (a) Powermap of a 15-die stack representative of an APU-GPU microprocessor unit, (b) Computed temperature field for the power map.

The floorplan for the 15-die case considered in Figure 5.10 is redistributed in order to obtain a more thermal friendly floorplan. It is expected that distributing the orange blocks – that generate the highest power density – more uniformly amongst all dies may result in a more uniform and lower temperature distribution. The resulting heat generation profile and computed temperature distribution on each die are shown in Figures 5.11(a) and 5.11(b) respectively. Note that temperature distributions in Figures 5.10(b) and 11(b) are both plotted in the same color range, for ease of comparison. As expected, the thermal friendly redistribution of heat generating blocks results in considerably reduced temperature and greater thermal uniformity. The redistribution of the floorplan carried out here is based on reducing power density by distributing the high power density blocks uniformly; the power map in Figure 5.11(a) is not necessarily thermally optimal. Determination of a thermally optimal power map may require iterative redistribution with several steps. Further, floorplanning optimization is a multi-disciplinary process [Jain *et al*., 2011] that requires the optimization of several objectives related to thermal and electrical performance. It is expected that the analytical model presented in this work may aid such a multidisciplinary floorplanning optimization process by computing the temperature distribution at each step.



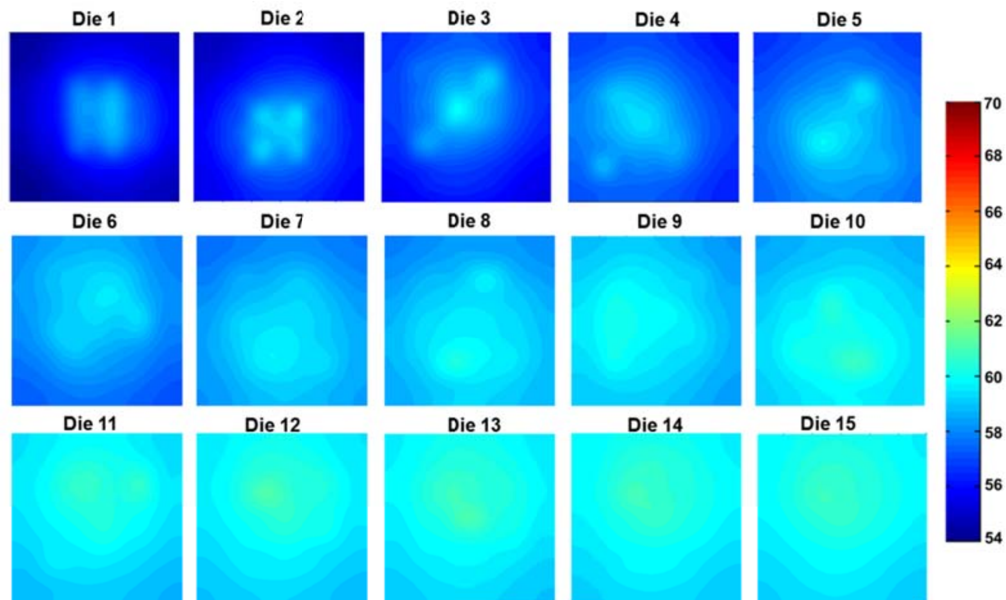


Figure 5.11 (a) Powermap of an alternative, thermally-friendly floorplan for the 15-die stack, (b) Computed temperature field for the power map.

In a 3-die case, the temperature distribution of every die in three different heights regarding to the coordinate shows in Figure 5.1, are illustrated in Figure 5.12(b), (c) and (d) and the power map of every die is shown in Figure 5.12(a). z=0.5 mm which indicates top surface of every die is shown in Figure 5.12(b). The maximum temperature of die 1 occurs at top surface because the heat sink is located at the bottom of die1 and heat moves easily from the top to the bottom surface. The maximum temperature of die2 which is located in the middle happens at the bottom surface because of the effect of die2 and die1 hot spots together. The maximum temperature of die3 happens at top surface.

Figure 5.13 shows the temperature change at the center of every die in z direction for the powermap presented in Figure 5.12(a). As it is illustrated by increasing the height the temperature rise increased for all the three cases.

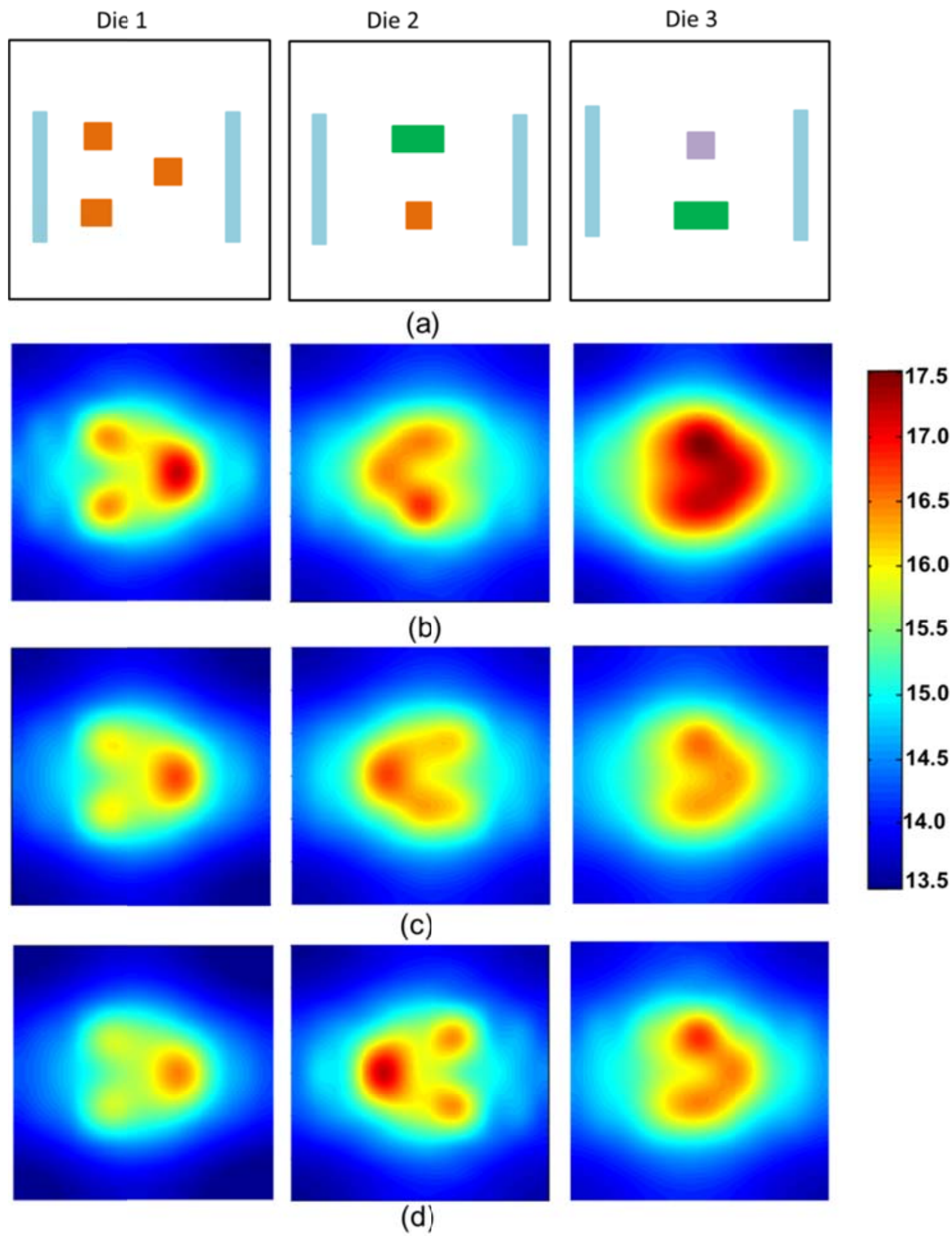
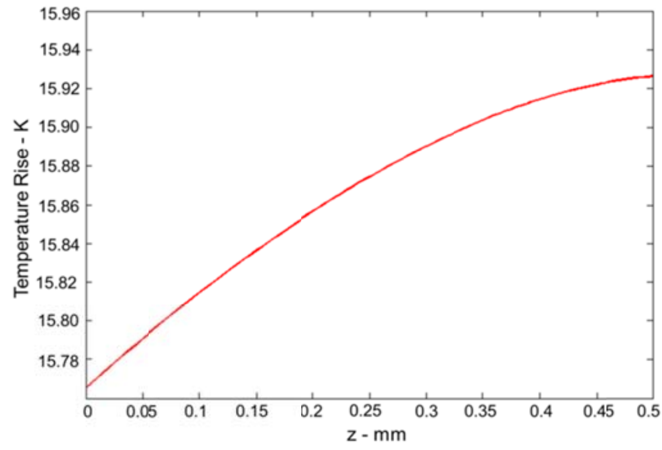
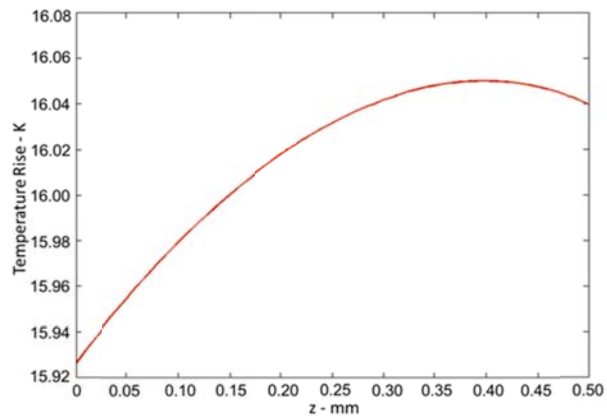


Figure 5.12 Temperature map in different height for three die case (a) power map for three die case for every die, (b) Temperature distribution at z=0.5mm for every die, (c) Temperature distribution at z=0.25mm for every die,(d) Temperature distribution at z=0.0mm for every die.



(a)



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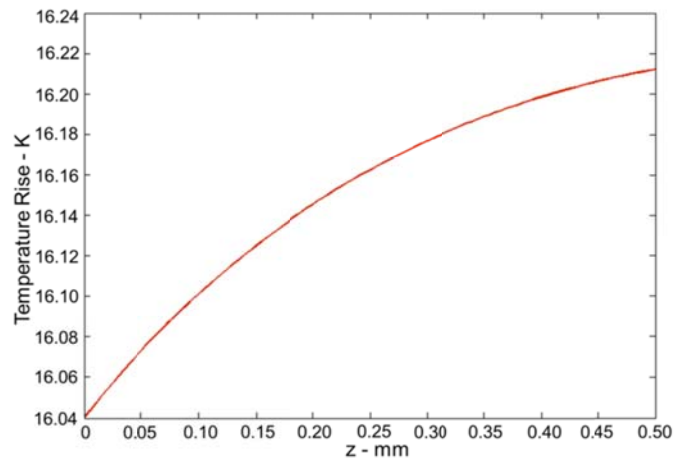


(c)

Figure 5.13 Temperature rise at the center of each die in z direction, (a) die 1, (b) die 2, (c) die 3.

5.4 Conclusions

In this chapter a non-iterative analytical approach for computing three-dimensional temperature field in a 3D IC has been investigated. For different values of number of stacks in 3D IC, the governing energy equations with appropriate boundary conditions have been solved. The steady state temperature field predicted by the model compared well with Finite Element simulation and the iterative model which presented in the past. Furthermore the model is much faster than numerical model and iterative model. The temperature distribution for large number of die has been presented and the effect of inter-die thermal contact resistance investigated. Also several application of the work discussed and the results may be useful in design and fast thermal computation of 3D IC.

Chapter 6

Experimental Measurement of the Thermal Performance and Thermal Contact Resistance of an Un-Equally Sized Two Die Stack

6.1 Introduction

Thermal management of three-dimensional integrated circuits (3D ICs) has attracted significant research interest in the recent past [Venkatadri *et al*., 2011; Jain *et al*., 2010; Jain *et al*., 2011; Choobineh *et al*., 2012; Oprins *et al*., 2011; Colgan *et al*., 2012] due to the promising electrical performance of stacked microelectronic systems [Black *et al*., 2006; Alam *et al*., 2010], and the accompanying challenge of thermal management of multiple, parallel heat generating planes [Jones, 2007; Jain *et al*., 2010]. In order to fully utilize the electrical benefits for vertical integration, it is essential that any thermal penalty associated with 3D ICs be kept to a minimum, and novel means of cooling of multi-stack systems be investigated.

The application of TSVs for heat removal from multiple die stacks has been investigated [Lau et al., 2011; Oprins et al., 2012; Kleiner et al., 1995].Liquid cooling of 3-D ICs has also been studied [King et al., 2010; Kim et al., 2010; Brunschwiler et al., 2009; Jiang et al., 2002].

Several applications of thermal modeling of 3D ICs to improve their electrical design have also been reported [Alam *et al*., 2009]. Each of these applications relies on an accurate method for temperature estimation in a 3D IC. While the temperature field in a 3D IC can be determined from a finite-element simulation, an analytical-based temperature computation approach is desirable since it provides a better physical understanding of the thermal problem, and is also easier to integrate with electrical design tools. Several recent papers have discussed the thermal modeling and analysis of

3D ICs. A thermal resistance model of a general, N-layer 3D IC has been proposed [Jain *et al*., 2010]. Analytical models for predicting the temperature profile on a 3D IC have been developed [Choobineh *et al*., 2012; Choobineh *et al*., 2013; Haji-Sheikh *et al*., 2003; Geer *et al*., 2007]. Compact-modeling based tools have also been extended to account for vertically-stacked die [Skadron *et al*., 2004]. Regardless of the approach used for temperature computation, the accuracy of the predicted temperature field depends on accurately knowing the values of several physical parameters.

Some thermal contact resistance exist between two adjacent die in a 3D stack depending to the nature of the integration[Oprins *et al*., 2011; Matsumoto *et al*., 2011; Colgan *et al*., 2012]. The thermal contact resistance occurs because of the underfill materials around the metal pillars which bond two adjacent die together. This thermal contact resistance would affect the thermal characteristic of the package [Bozorg-Grayeli *et al*., 2013; Yovanovich *et al*., 2005]. The inter-die thermal contact resistance is one of the least well-known among these parameters, primarily because of difficulties in either determining it analytically or measuring it experimentally. Some works on analytical estimation based on a simple thermal resistance combination has been reported [Jain *et al*., 2010], but this does not account for thermal contact resistance. The temperature distribution of a fabricated three layer 3D stacked with equally sized die obtained experimentally and a simulation model has been developed. Based on the experiment and simulation the equivalent thermal conductivity of the interconnects is determined and the value used to estimate the total thermal resistance of 3D chip stack [Matsumoto *et al*., 2011]. However the thermal measurement in a 3D IC with unequally sized die is required and also determination of thermal contact resistance is important to develop an appropriate cooling system. A few numerical and experimental works have been done to measure the thermal resistance of the package [Oprinse *et al*., 2011; Colgan *et al*.,

2012]. In general, there is a lack of experimental data on thermal management and determination of thermal contact resistance of a 3D IC, which inhibits the accuracy of computational models since experimental data often used to validate computational models and determine key fitting parameters.

This chapter presents experimental results on thermal performance of a two-die 3D IC. Heaters and temperature sensor circuits embedded in each layer are utilized to generate heat and measure temperature rise in each layer respectively. Both steady-state and transient data are reported. The experimental setup and theoretical model for measuring thermal contact resistance between two adjacent die introduced and the experimental value of thermal contact resistance compered well with theoretical model result. Results indicate a unique asymmetry in the thermal performance of the unequally sized two-die stack and may be useful in future design and thermal management of 3D ICs.

Section 6.2 describes the experimental procedure including the setup for performing the thermal calibration and measurements. Section 6.3 presents and discusses results, and Section 6.4 provides the experimental method to measure inter die thermal resistance.

6.2 Experimental Setup

The 3D IC used in this work is a two-die stack comprising a large die and a smaller die. The smaller die is bonded to the large die in an asymmetric position. Each die contains an embedded heater and a resistance thermometry based temperature sensor. Each heater and sensor is accessible by I/O pads located on the periphery of the bottom die. Sensors are located at approximate center of each die, and heaters are serpentine structures that cover the entire die in a nearly uniform fashion. Figure 6.1 shows a schematic of the two-die stack, heater and sensor of every die.

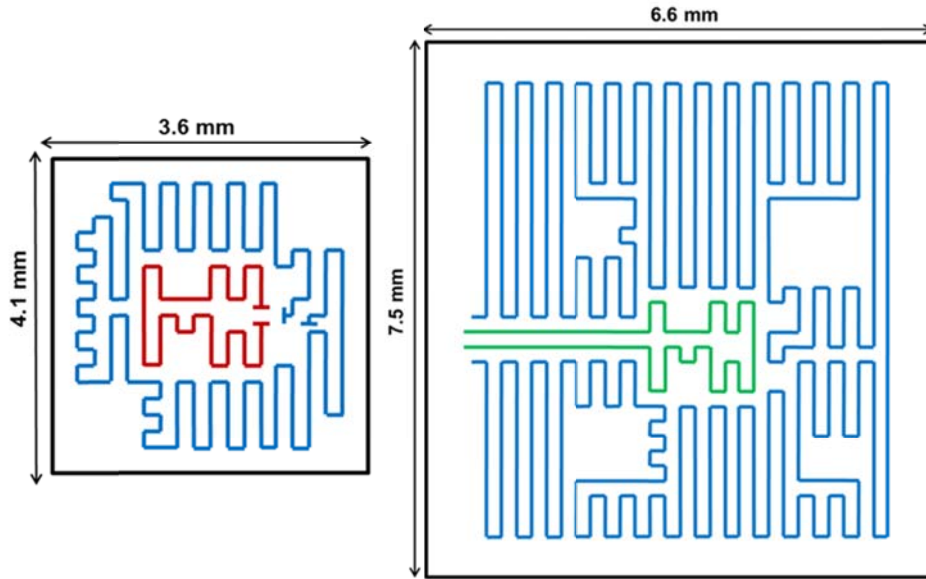
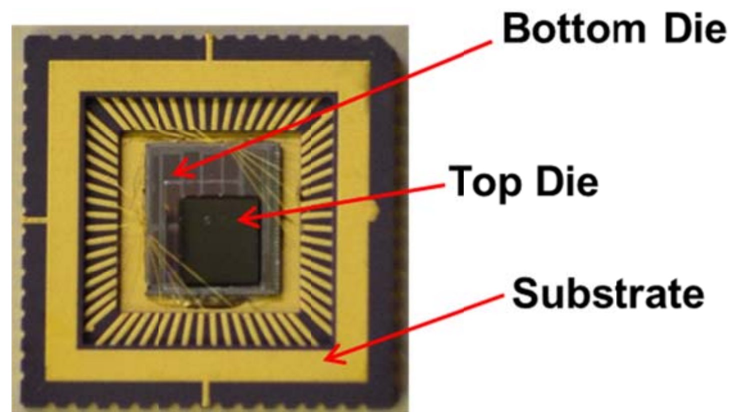
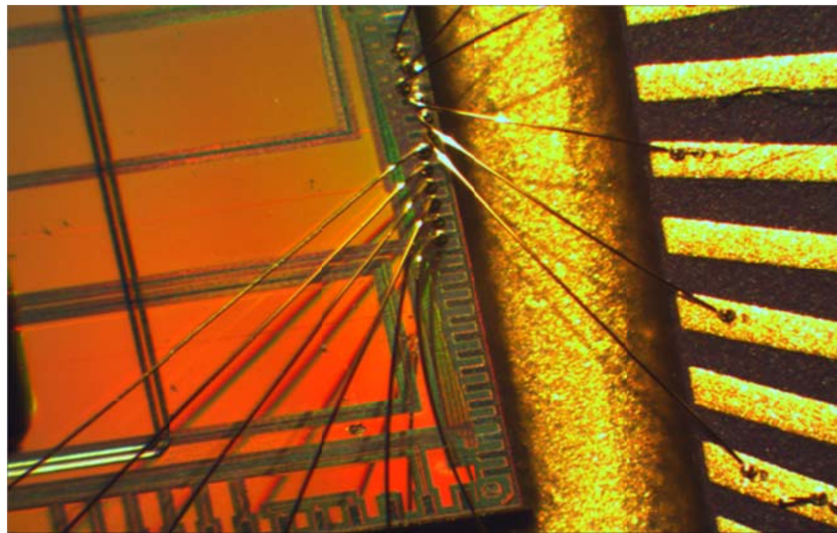


Figure 6.1 Schematic of the two die in the 3D IC. Blue lines show the heater, Red lines show the top die sensor and green lines show the bottom die sensor.

The 3D IC is first glued on a leadless chip carrier (LCC) substrate. In order to access the I/O pads located on the periphery of bottom die, gold wire bonding connections are made between the die I/O pads and LCC contact pads as shown in Figure 6.2. Wire bond integrity is verified by visual inspection under a microscope. After wire bonding, because the size of LCC pads are small and it is impossible to access them by regular solder wiring, the LCC substrate is mounted on a compatible pin socket .The top and side view of socket are shown in Figure 6.3(a). Finally, fine electrical wires are soldered on the socket leads as shown in Figure 6.3(b). In this manner, heater and sensor elements on each die are accessed through I/O pads on bottom die, wire bonds, LCC contact pads, socket pins and finally soldered wires. The image of the entire package is shown in Figure 6.3(c).

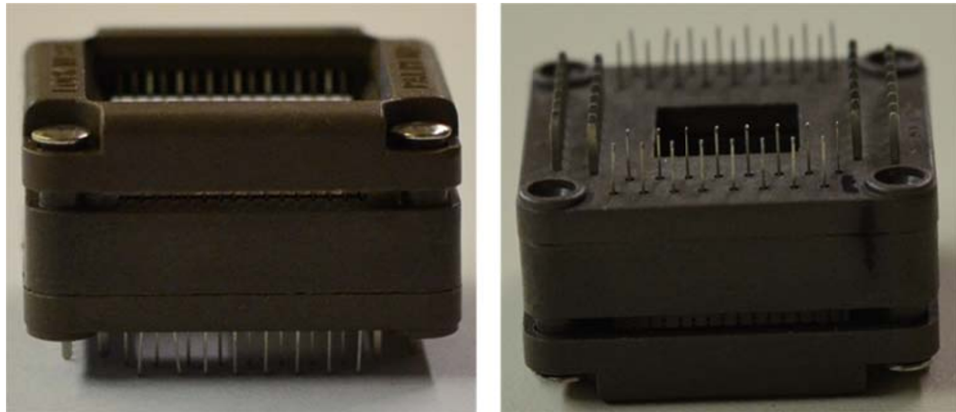


(a)

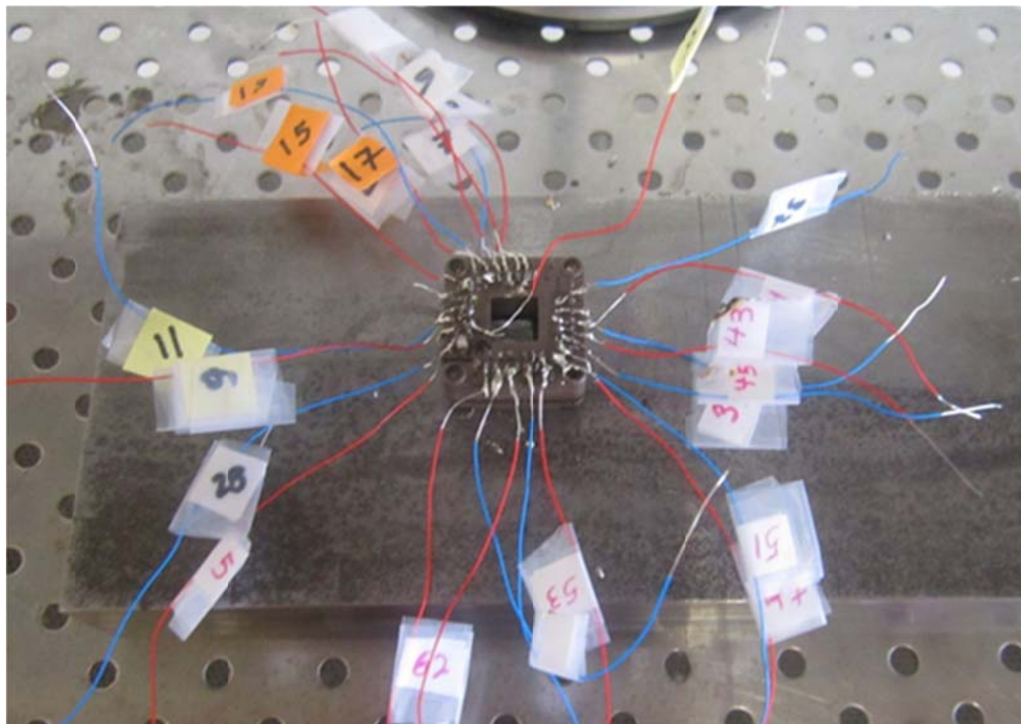


(b)

Figure 6.2 (a) An image of the two-die 3D IC on a LCC substrate, (b) the image of gold wire bonding under a microscope.



(a)



(b)

Figure 6.3 (a) Top and side view of the socket, (b) An image of the soldered socket used for accessing thermal features on the 3D IC

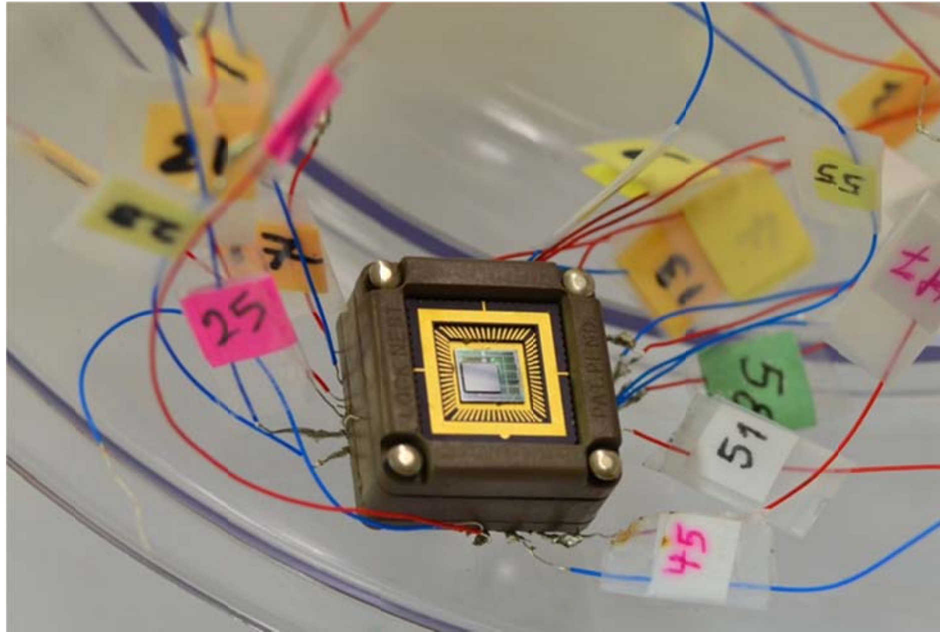


Figure 6.4 Substrate mounted in the socket and soldered wires.

Calibration is carried out by measuring the resistance of each sensor and heater at several temperatures between 20 °C to 90 °C. A Boeckel Scientific CCC 0.5d incubator is used for changing the temperature and Keithley 2401 and Keithley 2612 instruments are used for supplying a test current and measuring voltage respectively. A waiting period of 30 minutes is implemented at each temperature to eliminate thermal transient effect. A test current of only 10 μA is used to minimize self-heating effects. The experimental setup for thermal calibration is shown in Figure 6.5.

Figure 6.5 Image of the experimental setup for thermal calibration of temperature sensors on each die.

After doing the calibration the effect of generating power in every heater by increasing current on every sensor has been studied.

6.3 Results and Discussion

The electrical resistance of top and bottom die sensors which measured in the calibration test as a function of temperature is shown in Figure 6.6.

The experimental data shown in circles and the linear fit was done and shows accurate fitness. This is reasonable because the electrical resistance of metals increases linearly with temperature around room temperature.

The slope of the curve show the temperature coefficient of resistivity which is 0.00374°C^{-1} and 0.00369°C^{-1} for the top and bottom sensors respectively. The temperature coefficient of resistivity for the top and bottom heaters is also measured in the same way and they are in the same range, within experimental error bounds. This is in good agreement with the standard value of thermal coefficient of resistivity of

Aluminum which is 0.004°C^{-1}. Note that some deviation is to be expected since thermophysical properties of materials are known to deviate from standard bulk values.

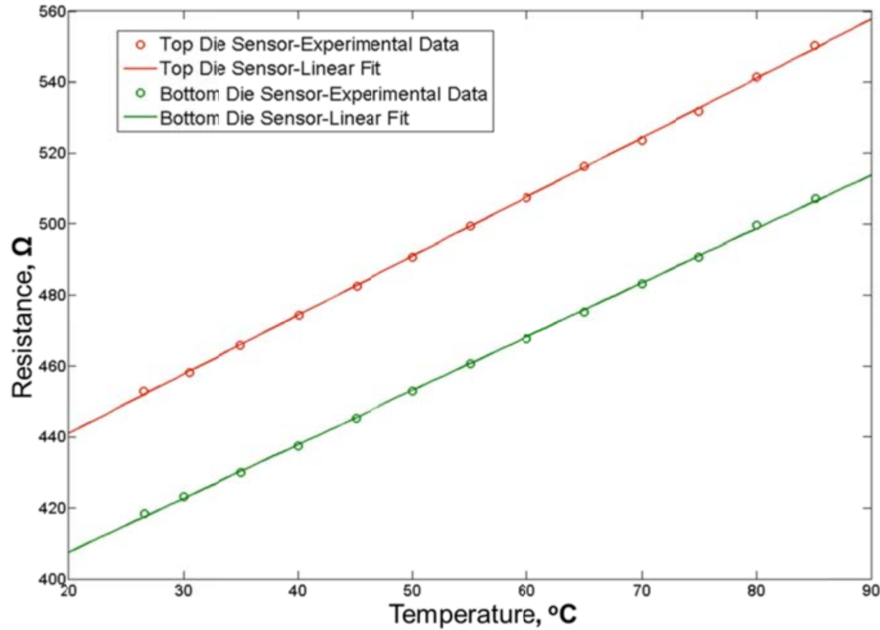


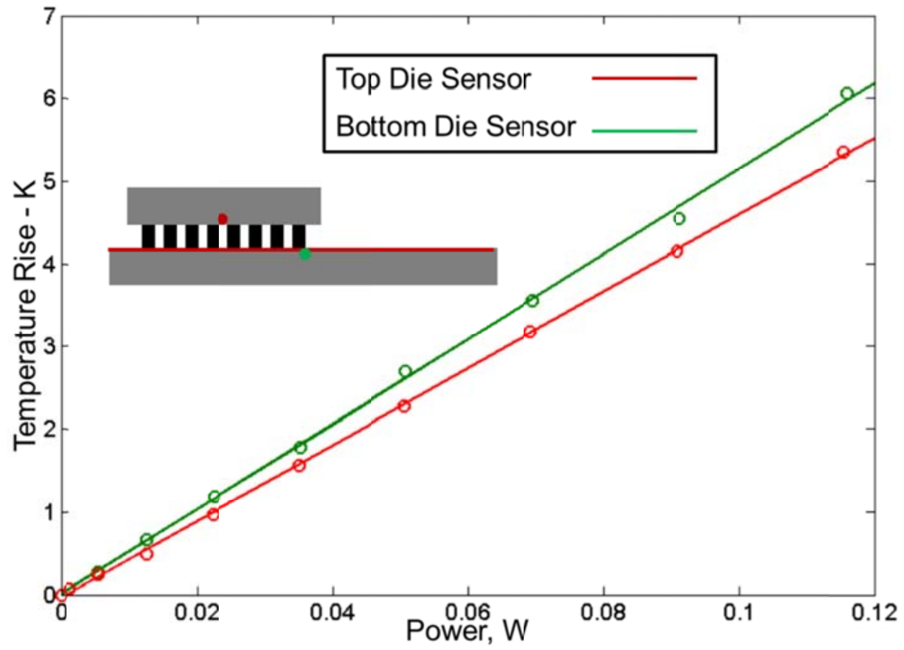
Figure 6.6 Thermal calibration curve for top and bottom die sensor.

Once the devices are calibrated, the measured electrical resistance of each sensor is utilized to determine its temperature rise, based on calibration curves similar to ones shown in Figure 6.8(a) and (b).

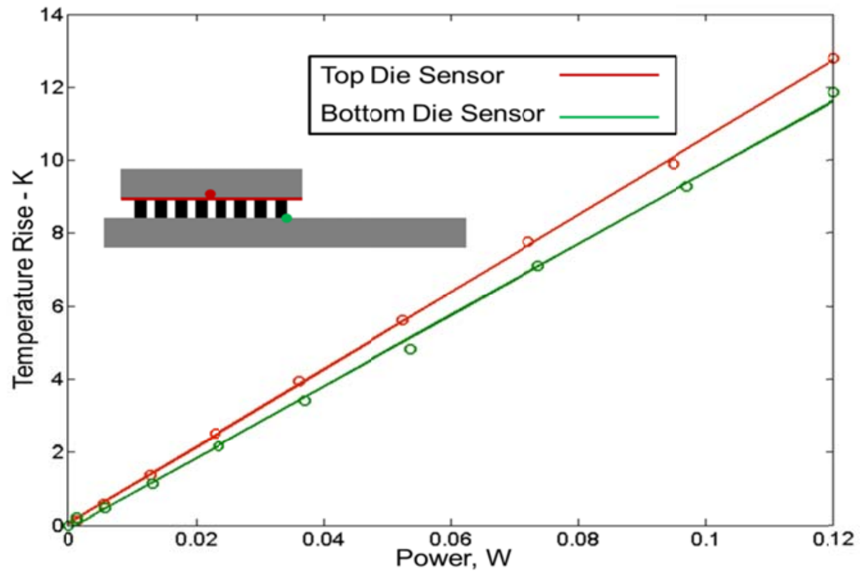
The heating current in either the top or bottom heater is increased and then the electrical resistance of every sensor measured and temperature rise has been calculated. The experiment setup is shown in Figure 6.7. For measuring the electrical resistance of sensors, a small current 10μA is used to avoid the self-heating effect. The effect of bottom die heating is shown in Figure 6.8(a). The experimental data is modeled with a linear fit because of the linearity of the fundamental governing energy equations. The

effect of heating the top die on both sensors has been shown in Figure 6.8(b). In both the cases, heating top die and bottom die, the temperature sensor in the layer which is heating showed more temperature rise. This happened because of the closer distance of the top and bottom die sensor to the respective heaters.

Figure 6.7 Experiment setup for studying heater effects on sensors.



(a)



(b)

Figure 6.8 (a) Plot showing temperature rise in each sensor due to heating in bottom die, (b) top die.

The temperature rise in the top and bottom die sensor as a result of heating up the respective heater is shown in Figure 6.9. As shown in this figure, for a given value of heating power, the temperature rise in the top die is significantly more than the temperature rise in the bottom die. The reason is that the generated heat in the top die should conduct through the bottom die and then to the substrate and surroundings while the generated heat in the bottom die only needs to pass through the substrate and then goes to the ambient.

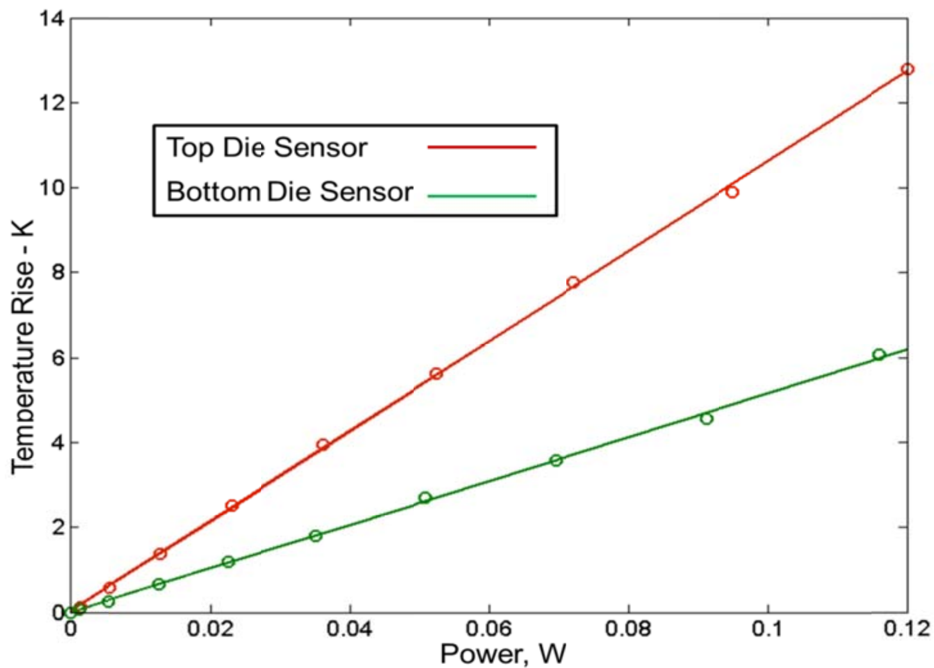
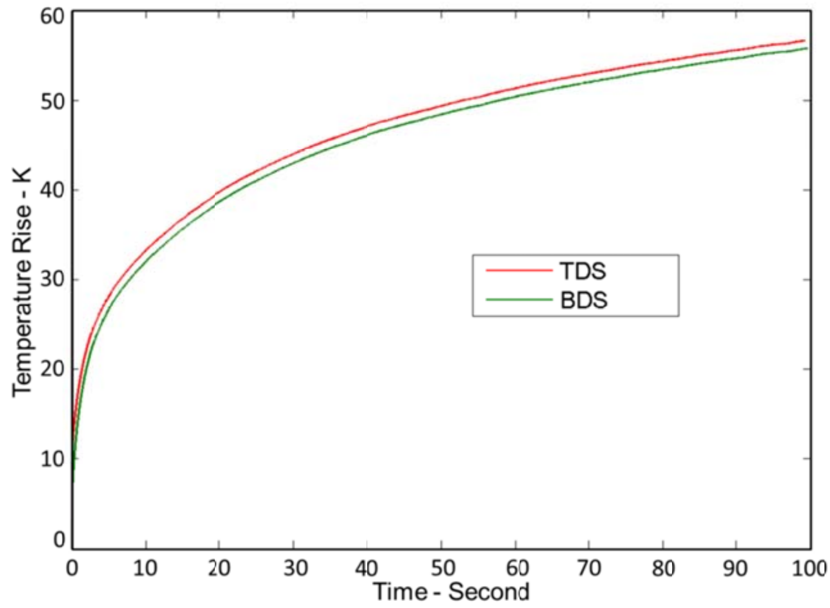
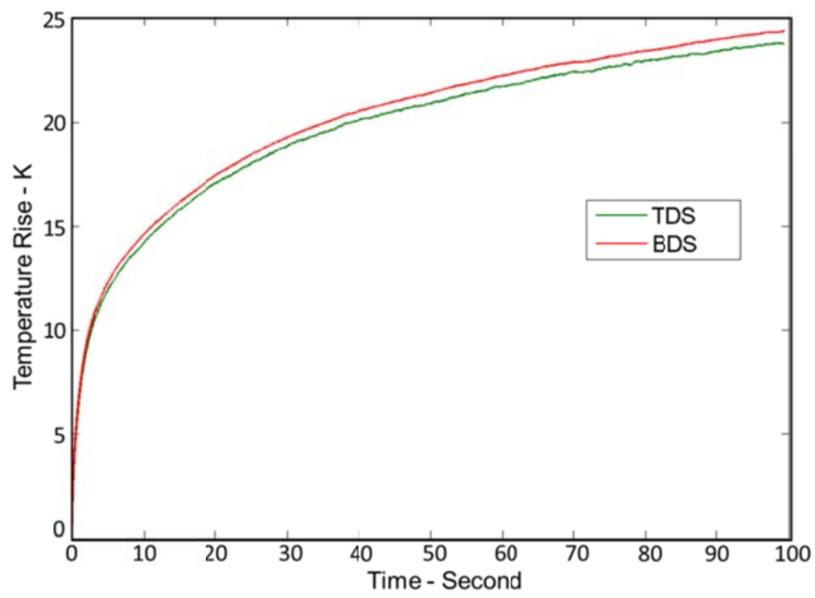


Figure 6.9 Plot showing temperature rise in top and bottom die sensors as a function of heating in the same die.

Transient measurements are also taken to characterize the transient response of the two die stack. Figure 6.10 shows a plot of the temperature rise in the top and bottom die sensors as a function of time after starting a 0.6W power at t=0 in either top or bottom die. The top die has shown higher temperature rise and also it heats up faster than the bottom die.



(a)



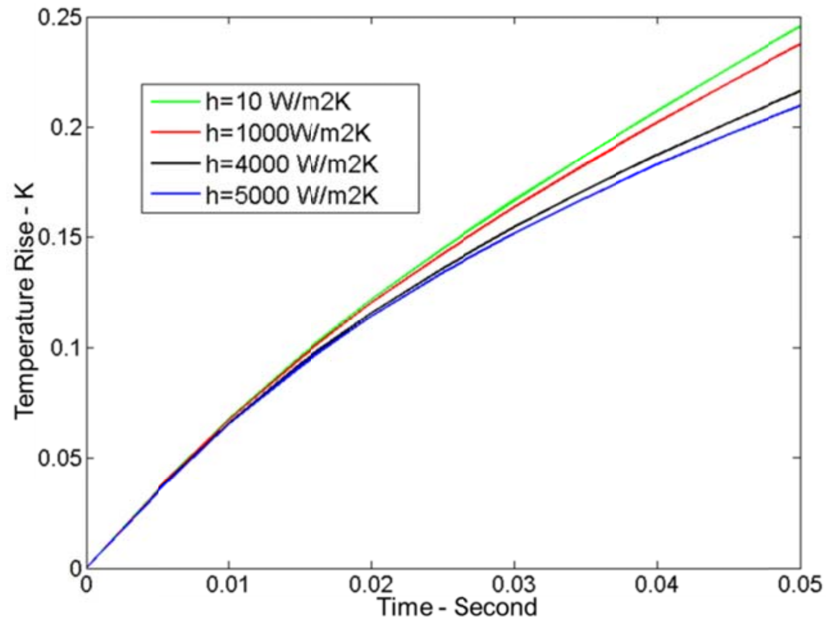
(b)

Figure 6.10 Plot showing transient characteristics of the top and bottom die. Red and Green curves show temperature rise in top and bottom die sensor after starting a 0.6W power at t=0 in (a) Top Die, (b) Bottom Die.

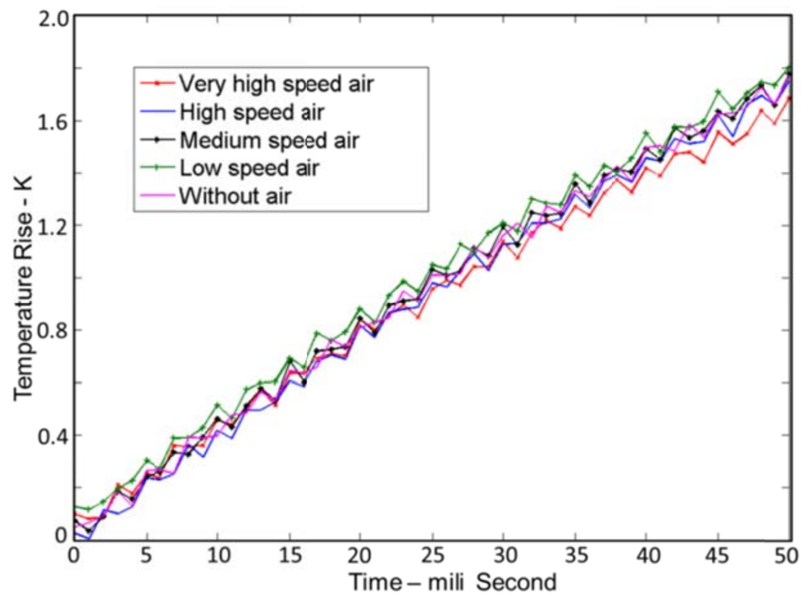
6.4 Determination of Thermal Contact Resistance between Two Die

Some thermal contact resistance exists between two adjacent die in a 3D stack depending on the nature of the integration [Oprins *et al*., 2011; Matsumoto *et al*., 2011; Colgan *et al*., 2012]. The thermal contact resistance occurs because of the underfill materials around the metal pillars which bond two adjacent die together. This thermal contact resistance would affect the thermal characteristic of the package [Bozorg-Grayeli *et al*., 2013; Yovanovich *et al*., 2005] and it is important to do the experiment in order to determine thermal contact resistance between two die.

A simulation based model has proposed in order to investigate thermal contact resistance between adjacent die. Finite Element simulation has been done by considering different values of the convective heat transfer coefficient and results presented in Figure 6.11(a). They illustrated that for the first 25ms, the temperature rise in the two die stack doesn't depend on the convective heat transfer coefficient and in this time period it can be considered that the thermal waves are in the domain and the boundaries don't affect the temperature plot. The experimental measurements data which is shown in Figure 6.11(b) also approve the simulation results. This performance can be used to determine the inter-die thermal resistance in a two die stack.



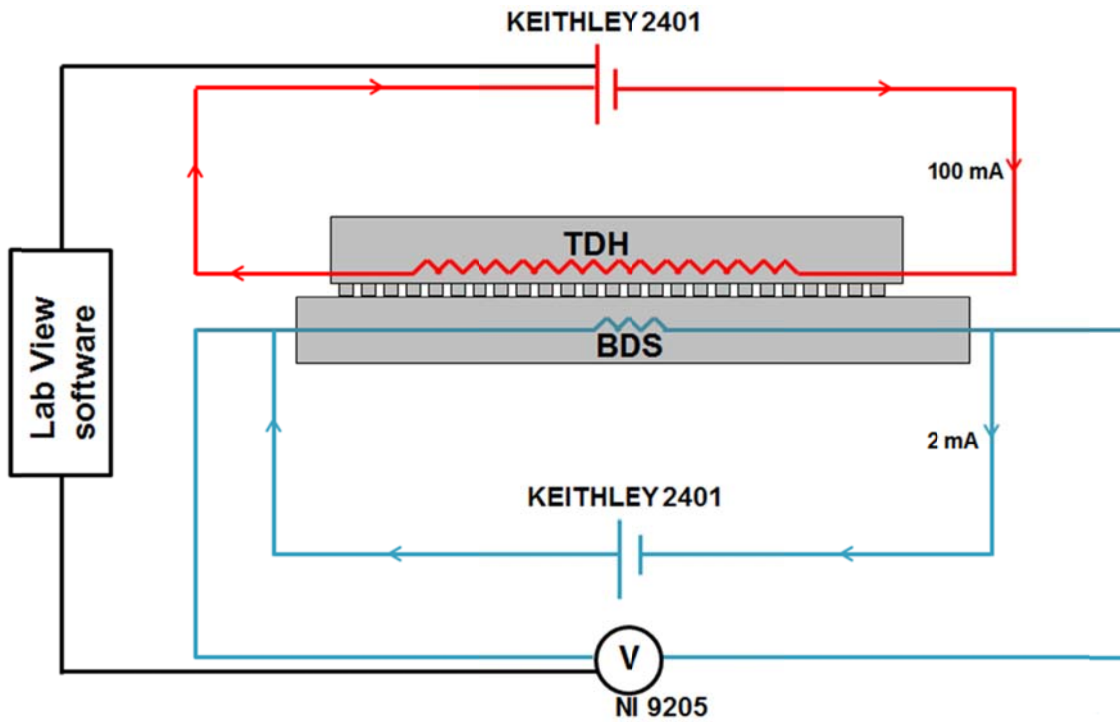
(a)



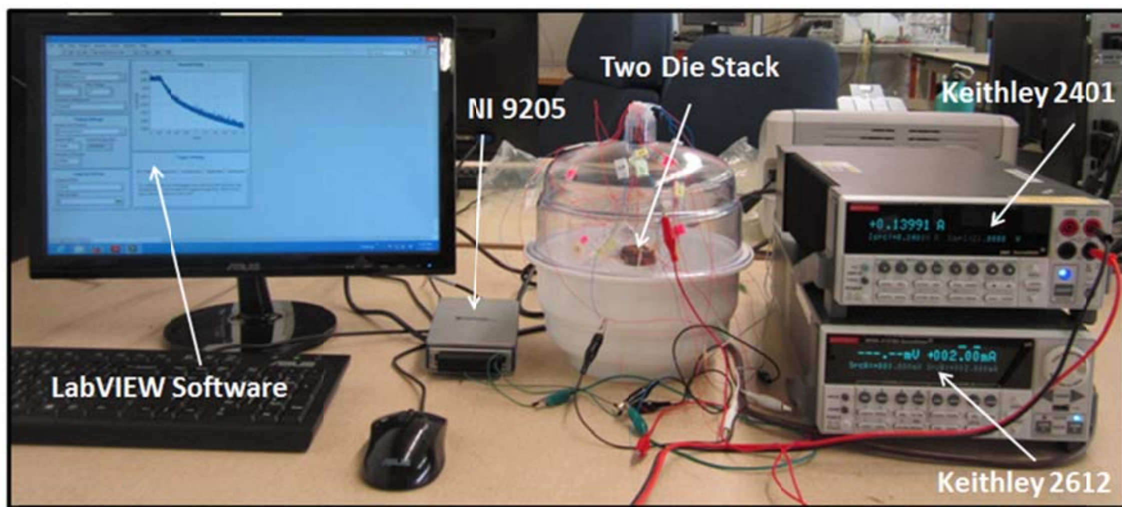
(b)

Figure 6.11 Temperature rise in bottom die sensor vs. time by heating the top die for different values of coefficient of convective heat transfer, (a) Finite Element simulation, (b) Experiment.

For doing the experimental measurement because the time steps are very small the data acquisition should be done very fast. In order to do very fast and accurate measurement, the LabVIEW was programmed (As shown in Appendix A). The measurement has been done every micro second according to the suggested experiment setup displays in Figure 6.12(a) and (b) and the temperature rise has been calculated to determine the inter-die thermal resistance.



(a)



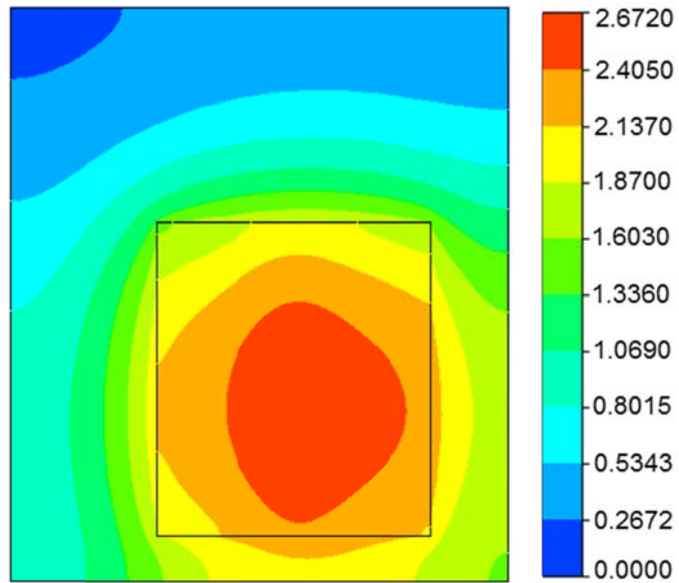
(b)

Figure 6.12 Experimental setup for measuring thermal contact resistance between two die

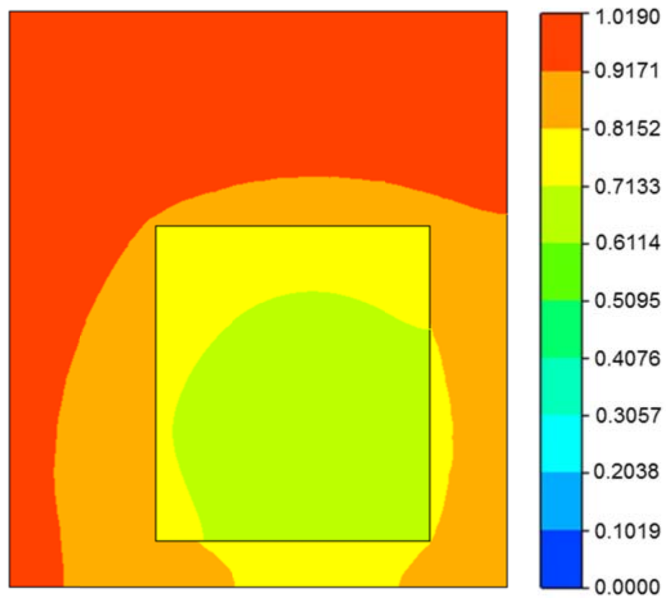
At first, for a given value of power in one die, the transient Finite Element simulation was carrying on by using commercial software ANSYS. Different values of thermal contact resistance have been applied between two die. The Finite Element temperature distributions at top surfaces for two different cases at time equal to 25ms are illustrated in Figure 6.13(a) and (b).

In order to determine thermal contact resistance, temperature rise in one sensor for the first 25ms was plotted and compared with the equivalent experimental temperature rise plot .The value of thermal contact resistance that the Finite Element plot matches with the experimental curve is the value of thermal contact resistance.

The comparison of Finite Element simulation and experiment for different cases as shown in Figure 6.14(a) and (b) indicates that the experimental value of thermal contact resistance is 1e-5 Km^2/W.

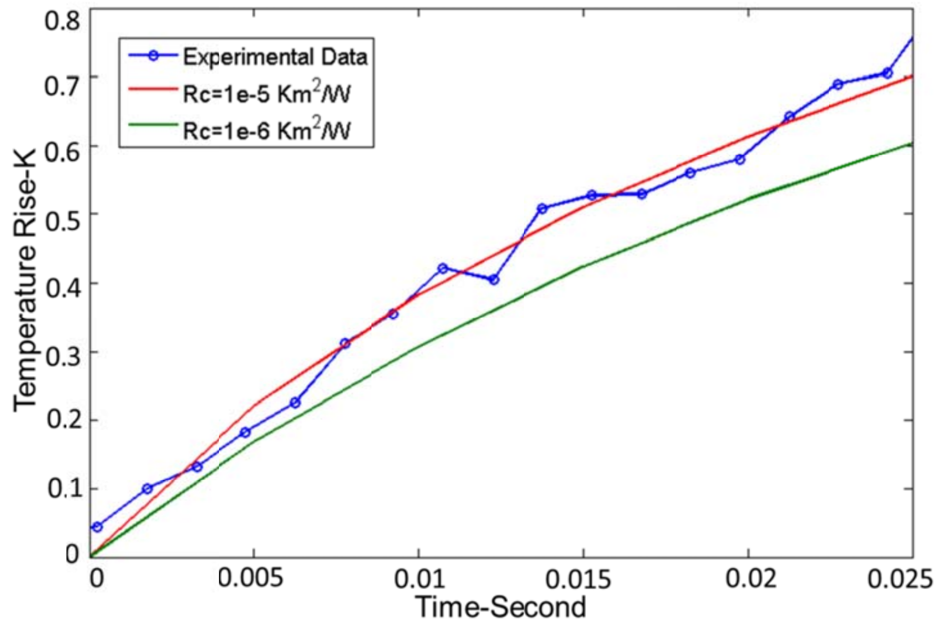


(a)

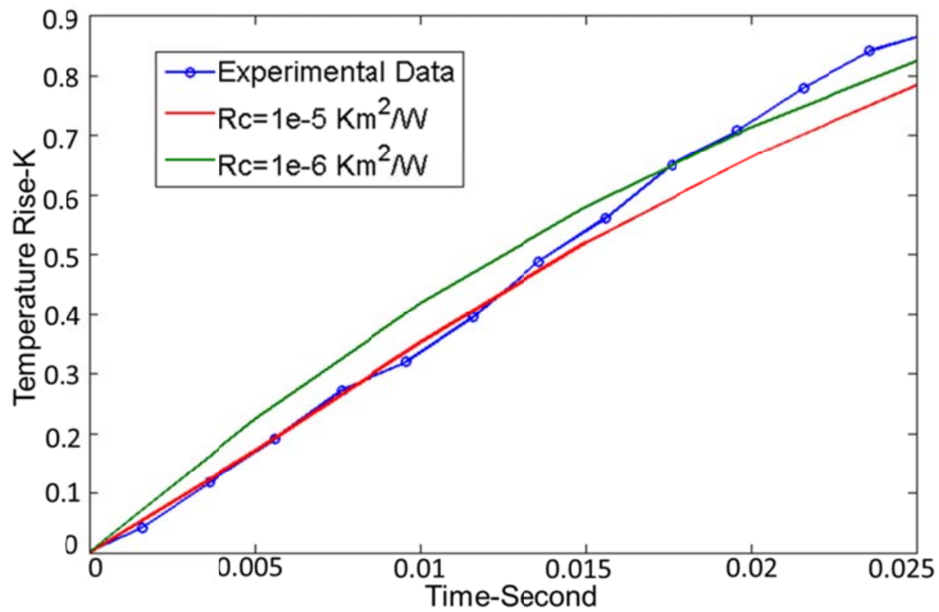


(b)

Figure 6.13 Finite Element temperature distributions at top surfaces (a) Top die heater generating 1.18W power, (b) Bottom die heater generating 0.6W power.



(a)



(b)

Figure6.14 (a) measured temperature rise in Top Die Sensor due to 0.38W power in Top Die, (b) Measured temperature rise in Bottom Die Sensor due to 0.6W power in Top Die.

A theoretical model has been expanded to validate the experimental results. The Copper pillars are utilized between two die for attachment and the under filled material which is considered to be air. The geometry and dimensions of Copper pillar arrays between two die has been shown in Figure 6.15. Thermal conductivities are set as the bulk thermal conductivities which are 401W/mK and 0.0257W/mK respectively for Copper and air.

Because of the symmetry of the geometry only one copper-air cell has been used for calculations. The thickness of every die is provided, however the cupper pillars height is unknown. The distance between the top surface of top die and the top surface of bottom die is measured and then by subtracting the top die thickness from the measured value, the cupper pillars height is achieved and used to calculate the thermal contact resistance between two die.

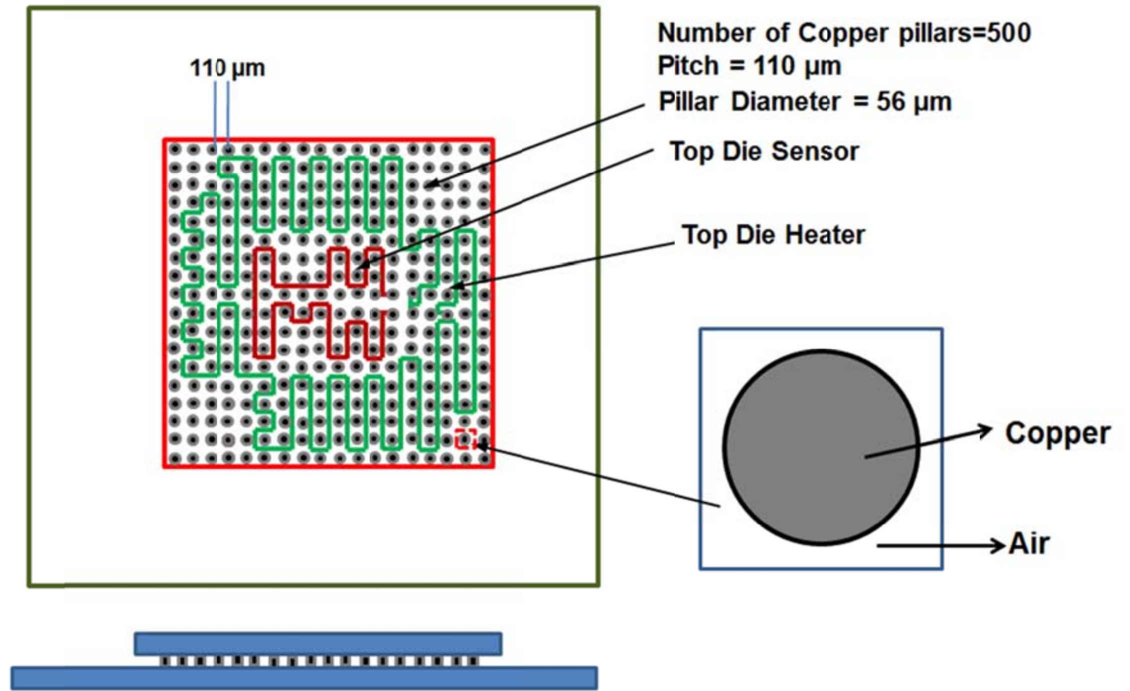


Figure 6.15 Geometry and dimension of Copper pillars used to make attachment between two die.

The theoretical value of thermal contact resistance is calculated from equation (3) and (4) which is 0.735e-6 Km^2/W and has a very good agreement with the experimental result.

$$f_{Copper} = \frac{\pi R^2}{L^2} \tag{1}$$

$$f_{Air} = 1 - f_{Copper} \tag{2}$$

$$\frac{1}{R_{total}} = \frac{1}{R_{Copper}} + \frac{1}{R_{Air}} \tag{3}$$

$$\frac{1}{R_{total}} = \frac{k_{Copper} f_{Copper} A_{total}}{height} + \frac{k_{Air} f_{Air} A_{total}}{height} \tag{4}$$

$$R_{total} A_{total} = \frac{height}{k_{Copper} f_{Copper} + k_{Air} f_{Air}} = 0.735 \times 10^{-6} Km^2 / W \tag{5}$$

6.5 Conclusion

This chapter discusses experimental thermal characterization of a two-die 3D IC using heater and temperature sensor circuits embedded in each die. The effect of heating one die on itself and on the other die has been examined. Measurements indicate that the top die heats up more and faster than the bottom die. This is expected to be related to the packaging of the die.

A method to measure thermal contact resistance between two die has been proposed and the experimental value has been compared well with theoretical results. Measurements presented in this work are expected to enhance the understanding of heat transport in 3D ICs.

Chapter 7

Conclusions and Future Study

7.1Summary of Main Conclusions

An analytical model to determine three-dimensional, steady-state and transient temperature fields in a 3D IC based on solutions of the governing energy equations has been done. An iterative approach that takes advantage of temperature and heat flux matching at interfaces is proposed. The analytical approach provides good physical insight into the problem of determining temperature fields in 3D ICs. In addition, it is expected to more easily interface with mainstream electrical design tools as compared to finite-element based methods. The work presented here also underscores the need for thermal-friendly pre-Silicon design, which helps minimize the system-level thermal dissipation challenge and leads to higher reliability without compromising electrical performance. This work is expected to aid in developing temperature characterization and prediction tools for 3D ICs. In addition, this work may also help in characterization of various thermal management strategies being proposed for 3D ICs.

While stacking die with different size in a vertically-integrated 3D IC is attractive from design and manufacturing considerations, doing so introduces additional thermal spreading and constriction resistance in the multi-die stack. An analytical tool for predicting the three-dimensional temperature field in a multi-die stack with an arbitrary number of unequally-sized die has been presented. The model shows that the larger the degree of non-uniformity in the die size, the larger is the temperature rise. Tools based on the presented model may be useful in rapid design iterations and in thermal-electrical optimization of unequally-sized 3D ICs.

A general interposer system is introduced which consists of a substrate and N chips bonded on the top surface of the substrate. An analytical model is established to

predict the temperature distribution in the substrate and chips as a function of heat generation in the substrate and chips. Results from the analytical model agree well with finite-element simulation. Several design cases for the location of chips and interposer hotspots are studied and the results illustrated that the best way to reduce the maximum and average temperatures, and to have more uniform temperature field in the substrate is by locating the chips not only far from each other but also far from the corners and the best thermal design of substrate hot spot locations is by avoiding overlap with chips hotspot and keeping them as far away from each other as possible.

A non-iterative analytical approach for computing three-dimensional temperature field in a 3D IC has been investigated. For different values of number of stacks in 3D IC, the governing energy equations with appropriate boundary conditions have been solved. The steady state temperature field predicted by the model compared well with Finite Element simulation and the iterative model which presented in the past. Furthermore the model is much faster than numerical model and iterative model. The temperature distribution for large number of die has been presented and the effect of inter-die thermal contact resistance has also been investigated.

The experimental thermal characterization of a two-die 3D IC using heater and temperature sensor circuits embedded in each die has been done and the effect of heating one die on itself and on the other die has been explored. Experimental data is expected to help validate analytical and simulation models that have been proposed for 3D ICs. A method to measure thermal contact resistance between two die has been proposed and the experimental value has been compared well with theoretical results. This will facilitate the development and implementation of robust, thermal-aware design and optimization tools for 3D ICs.

7.2 Future Research in Analytical Model

For the determination of temperature distribution in three dimensional integrated circuits with unequally sized die only one case has been studied; it is important to investigate the effect of die size on temperature field and finding the best design in order to decrease the temperature rise in N-die stack.

In the interposer based problem which is explained in chapter 4,only silicon substrate is propose and it is necessary to examine different substrate materials (for example glass), and the effect of substrate material on temperature distribution should be studied.

In chapter 5, a non-iterative analytical heat transfer model for computing three-dimensional temperature fields in a 3D IC is proposed. While the model is very accurate and useful, it can be more effective by expanding the model to N-die stack with un-equally sized die.

7.3 Future Research in Experiment

The experimental work is limited to a two-die stack; similar measurements in the future may help characterize heat transfer in a multi-die stack with greater than two die. Devices with more than two die may be design and the thermal management be studied. The effect of different underfill materials also needs to be investigated.

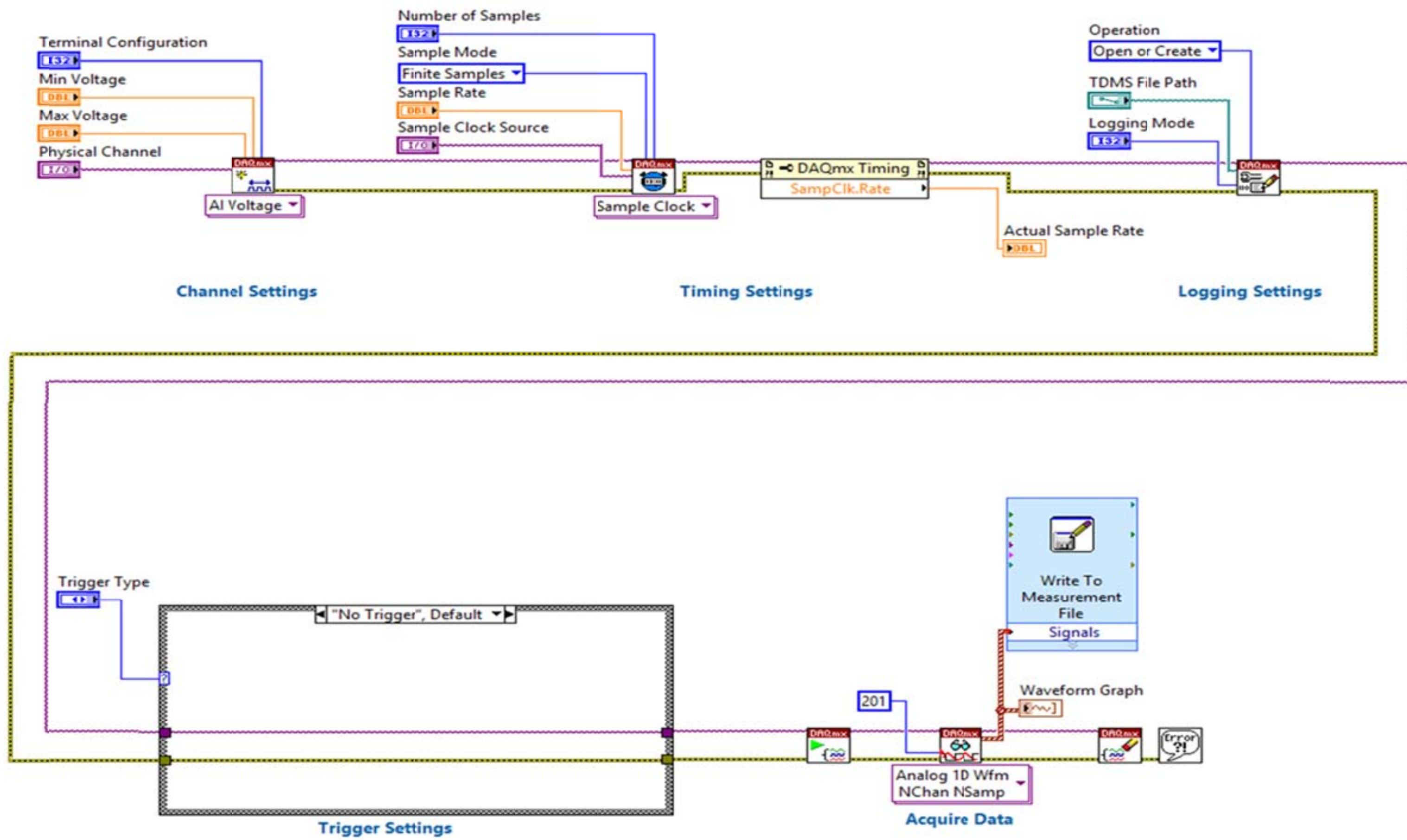
Packaging is an important factor in thermal management of 3D ICs. It is significant to design different packaging methods, the effect of different packaging styles on temperature profile be studied and the best packaging method determined experimentally.

Cooling of 3D ICs is very important and it is necessary to do the analytical modeling and experimental investigation of 3D ICs while considering microfluidic cooling.

Appendix A

LabVIEW Program

Lab VIEW program used for doing high speed measurement.



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