STRUCTURAL INTEGRITY OF TSVs IN 3D PACKAGE UNDER THERMAL LOADING

by

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Abstract

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In this advanced technological era, all electronic equipments tend to be light in weight, and have high performance with low power consumption and low prices. Gain in both performance and cost via Moore's law is starting becoming difficult post 28nm technology node. Three dimensional chips staking with TSV technology has gained momentum to meet such requirements of significant miniaturization and power reduction which result in increased performance. Vertically interconnected TSVs provide the shorter effective electrical interconnect path, resulting in reduced signal latency between strata and greater signal bandwidth. Moreover, TSVs offer high density integration, increased number of input/output terminals and reduction in power consumption by cutting out the power losses which enables the elimination of heating. However, the unique issues related to yield and reliability of critical areas in TSV based 3D ICs need to be evaluated. In this research 3D chip is subjected to thermal loading, heating thermal cycling. Under the loading, the critical area of concern is Si & Cu interface. This research involves the investigation of the interfacial cracking of Si & Cu, elastic strain energy developed at the interface under thermal cycling. The high coefficient of thermal expansion mismatch between Si & Cu causes the pressing issues related to interfacial de-lamination. When the 3D IC is thermal cycled the different materials in the contact tend to expand/contract according to their CTE's. The contact material (at the interface) is (usually) the weakest point in the model so it is expected to absorb the stresses of thermal mismatch by yielding in creep. The amount of creep an interface can endure is limited, and then it will begin to crack.

Structural integrity of Si & Cu was developed by stress intensity factor, and this developed stress intensity factor was compared with the fracture toughness of Si. FEA was used to

examine the mechanical effects by doing a series of stress analysis under low/high thermal cycling, which take into account the magnitude of thermal load, TSV geometry, etc. Large stresses were developed at the interfaces result in interface failures. Interfacial de-lamination of TSVs was encountered mainly driven by a shear stress concentration for the heating conditions and mixed mode fracture was occurred under cooling conditions at the interface. The parameters affecting the crack growth at the interface have been investigated.

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Chapter 1

Introduction

1.1 Evolution: PTH to TSV semiconductor packaging

In the past 30 years, the microelectronics industry has experienced rapid technological change which has largely been driven by Moore's law to constantly increase circuit speed and device density. Semiconductor packages for electronic equipments have grown with the development of packaging technologies required for higher density (with more pins), smaller and thinner chips [2]. Nowadays, Miniaturization in semiconductor packages is strongly required with increasing demand for tablet computers and Smartphone, further high-volume, high speed, low power consumption. Figure 1 shows the trends of semiconductor packages.

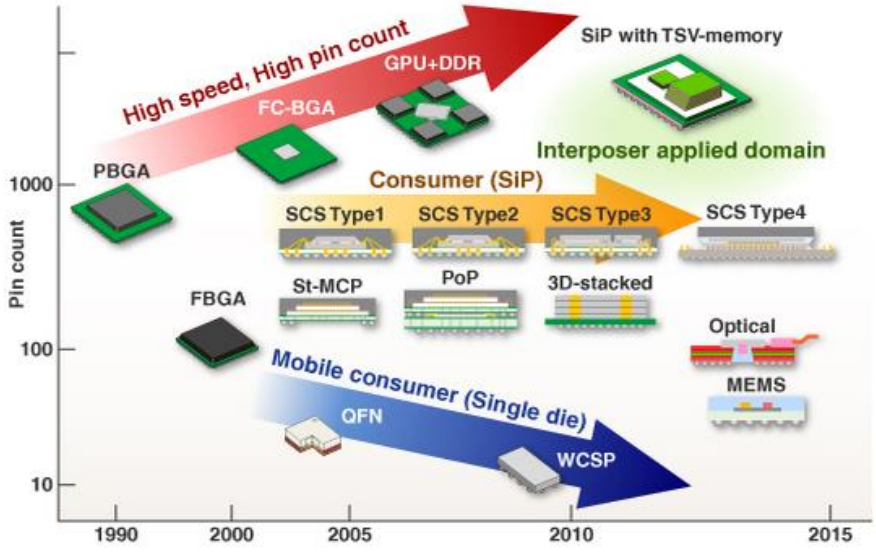


Figure 1.1: Trend of Semiconductor Packages [18]

At the time of 2nd generation computers from 1950s every components on a typical PCB was a through hole component which was become known as plated though hole (PTH) and was used to connect the components to make the contact with the required conductive layer [3]. The first breakthrough in technology took place in the '80s, with the introduction of Surface Mount Technology (SMT) as alternative to Through Hole Technology for the assembly of components

on PCB. Comparing the device pitch of PTH and SMT, the pitch for PHT is large 1.8-2.54mm whereas for SMT it is reduced down to 0.3-0.4mm [4]. Further development of Quad Flat Pack offered further I/O count capabilities up to 200-300. Ball Grid Array was designed in early '90s capable to interconnect several components in the same package, considered as a 2D phase of BGA. In early 2000, the requirements for further miniaturization in industry pushed the existing limits, in order to use the 3rd dimension of package. This was achieved by stacking two or more chips in the same BGAs, or two BGAs one on top of each other. Meanwhile the System in Package (SiP) was widely used for 3D BGA.

The recent rapid dissemination of smart phones and other mobile electronic terminals reflect the demand for faster, thinner and smaller products which are more compact and power efficient. The SiP technique is proposed to meet these requirements which integrate several semiconductor devices into a single package. Stacked dies with wire bonds in BGA are an example of 3D packages. Other 3D packaging configurations are called package-on-package (PoP) or package-in-package (PiP) in nomad devices. The idea behind all these new 3D packages is to enable better integration with a smaller footprint, smaller BGA ball pitches and at the lowest cost. Among the various 3-D packaging technologies, 3D ICs with TSV technology is the most promising one. Through-Silicon Vias (TSVs) are being used to fabricate three dimensional vertically stacked devices, where specific components such as logic, memory, sensors, and actuators are fabricated on separate wafers and then interconnected by either wafer-to-wafer or chip-to-wafer methods.

1.2 3D Packaging

The semiconductor industry has been trying to maintain Moore's law by showcasing the development and progress towards 3D ICs. Each 3D technology like 3D system-in-packages, 3D wafer-level-packaging, and 3D integrated circuits attributes to the advancement of the industry.

Talking about the 3D System-In-Packages, the design is composed of several devices stacked in one packages. Stacking of SiP could be vertical or horizontal which uses silicon interposer for the multiple chips connection. Wirebonds are usually preferred for these connections. Due to their length and the amount of space incorporated make them a limiting factor in SiPs. In comparison with systems-on-chips (SoC), these systems are having large increase in density. However, it is considered that this technology is well developed amongst 3D stacked chips.

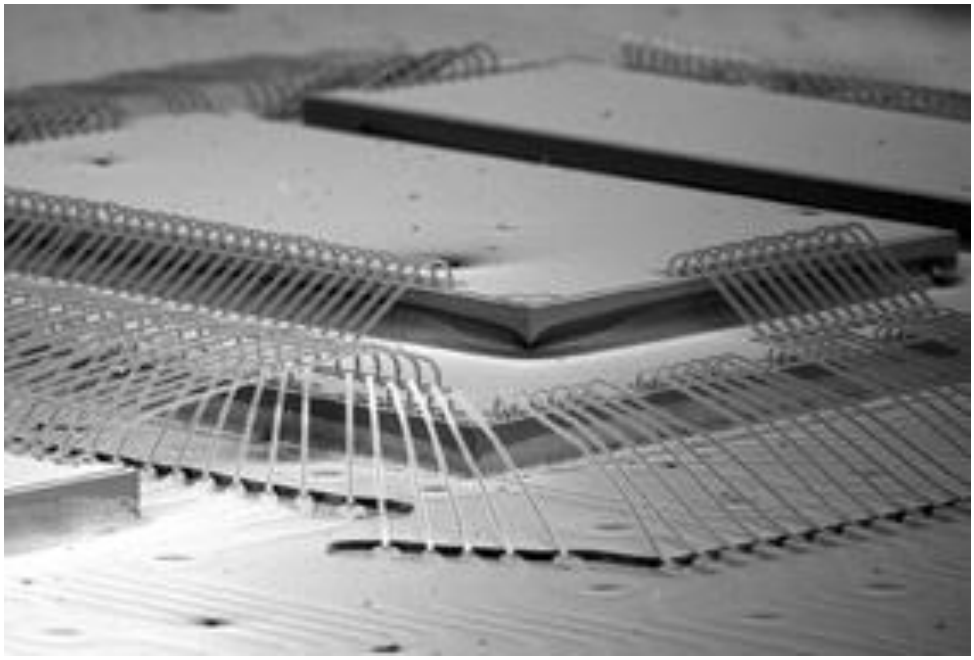


Figure 1.2: A SiP which uses wire bonding [20]

Secondly, 3D Wafer-Level-Packaging (WLP) is closely compacted package than the SiP since the interconnecting methods are different for both. Through-silicon Vias (TSV) are used in some of the WLPs, providing the vertical interconnects perpendicular to the chip surfaces. As it requires less space to operate and shorter pathway for current TSVs enhances the performance of the chips. It could also be functioned as a flip chip bumping, an application of solder bumps on the bottom of a chip to allow them to communicate when stacked [22]. Bumps and microbumps, like TSVS, make the WLP more densely packed then SiPs [21].

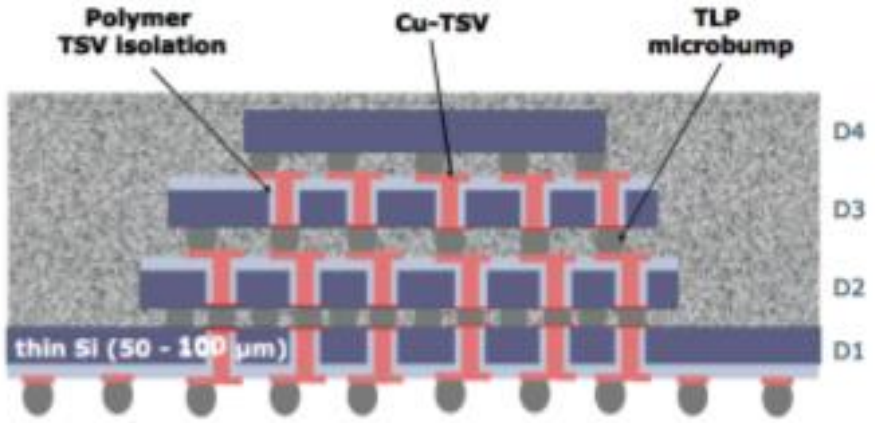


Figure 1.3: WLP which uses microbumps [22]

3D integrated circuits have emerged as a superior to SiP and WLP stacked technologies by offering highly dense package to achieve higher bandwidth and power efficiency. The wirebonding technology is replaced by through-silicon vias in these systems. TSVs connect die to die, bring them closer and present the highly integrated stacked chips. However the integration makes the design of ICs very crucial. In 3D Ics, shorter interconnect path length minimizes the power losses via joule heating and allow one chip to be a multifunctional, all the while reducing the form for the system [22]. 3D ICs allow miniaturization, saving space on the board and in the end product. They're ideal for extremely compact mobile devices. A 3D ICs example is given in figure 4.

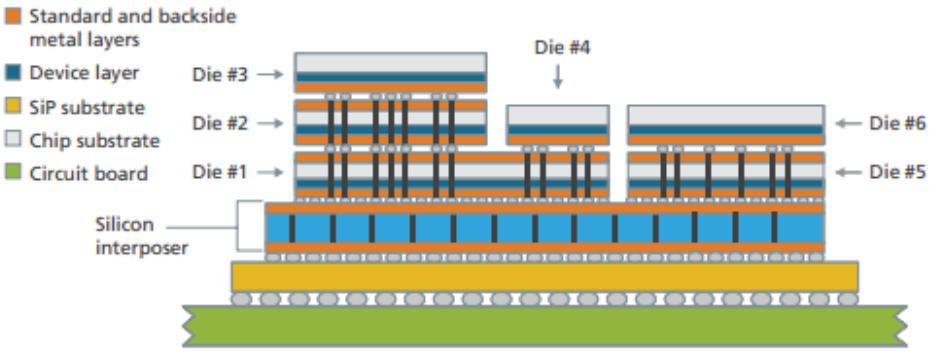


Figure 1.4: 3D IC using TSVs and 6 die [23]

1.3 3D ICs – advantages & challenges

In this advanced technological era, all electronic equipments tend to be light in weight, and have high performance with low power consumption and low prices. These equipments require miniaturization with respect to their packaging technology in order to satiate this tendency. Three-dimensional (3-D) ICs has become popular to meet such miniaturization needs. As 3D ICs offers dense systems which gives a smaller form factor. Such designs take full advantage of silicon wafer, having silicon efficiency, defined as the ratio of the available area on the silicon over the total area of the substrate, of over 100% compared to 2D systems [24]. 3-D integration provides enhanced inter-connectivity, high device integration density, a reduction in the number and length of the long global wires, and the potential to combine disparate heterogeneous technologies [15–17]. Wafer thinning of these system further accomplish a greater density. This feature allows these compact chips to be easily fit into cell phones or any mobile devices without decreasing the components on the chip.

In comparison with 2D there is a significant performance increase in 3D ICs due to reduced length of interconnects, which could make the other devices to be added to the chips because of the less surface area is occupied. In addition to that the signal must have to travel longer to reach to the destination where interconnects are only constrained to two dimensions, whereas for 3D ICs case shorter vertical interconnect reduce the time of signal transmission. David et.al have suggested that about a 65% delay drop could be seen in 3D ICs over their 2D equivalencies [25], while Al-Sarawi et.al suggests a 30% decrease in delay due to lower parasitic capacitance [24]. This also leads to a decrease in signal scattering, which in turn means up to 30% less power is required to drive the system [24]. The ability of 3D ICs to integrate disparate technologies is one of the most critical attributes of 3D ICs. This feature offers distinctive openings for highly heterogeneous and multi-functional systems. Giving of an example of such system, one example is a real-time image processing system where the image sensors capture the light on the top most plane, analog circuits on the plane below convert the

signal to digital data, and the remaining two planes of digital logic process the information from the upper planes [27, 28].

Power consumption is the most important design criterion. 3D IC power consumption has become more critical since on-chip temperature pose a risk to circuit integrity. Thermal management has been done by installation of cooling fans to avoid failure on die due to greater power consumption. 3D IC minimizes the circuit level power consumption by reducing the number and the length of interconnect. Another benefit of 3D Integration is to provide a potential solution to the greater expense in systems integration and reductions in yield. With 3D ICs, the die size does not have to be increased to provide greater functionality, but rather can be reduced into smaller dies which are vertically stacked [29]. The number of die defects can be reduced per die by the reduction of the size of a 2-D die. 3-D integration also supports the use of multiple technologies, allowing circuits to incorporate older and cheaper technologies for the non-critical components within a system [29]. Even the most advanced devices and chips can all be packed into one seamless system, using the 3D technology [26].

Challenges of 3D ICs are the major issues for chip designers and architects [21]. For an optimal performance, professional needs to take another look into the vertical interconnected chips layout designs. The increase in integration adds more chances of flaws in the design and structures. Moreover, failure of one component could lead to drop in overall performance or entire chip breakdown. It is restrained to rehabilitation as everything is integrated closely. Heat dissipation is a major concern because of the increased density of these chips. The system can easily get affected by the temperature increase and could cause the change in many material properties due to thermal expansion mismatch. The stresses in the system could result into discrete type of failures, from via cracking to the delamination of the substrate. There are still many unknowns to be tested for 3D ICs. The manufacturing and optimization of the design and materials of the 3D structures are in uncertainty. It will take more years to perfecting the structure, reliability, and manufacturability of these circuits.

Chapter 2

Characterization of Through Silicon Via

2.1 TSVs from Electrical standpoint

TSV technology, one of the advanced 3D packaging technologies, is expected to improve packaging density compared with that using wire bonding (Figure 2) [5]. The TSV joins two separately processed wafers or dies to form a 3-D IC. Each additional device plane that is stacked requires another set of TSVs to connect signals, different power domains, and various clock signals to properly operate the newly connected device plane [7].

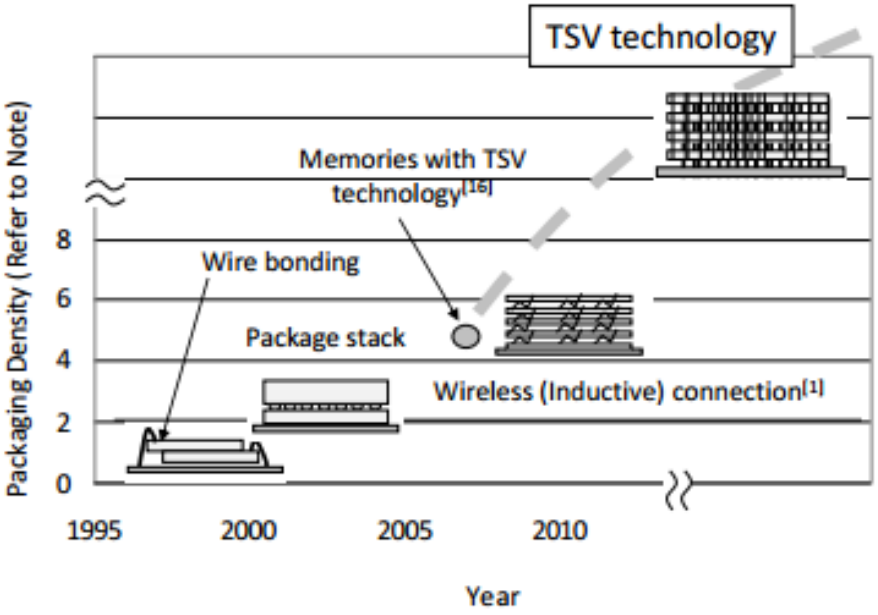


Figure 2.1 Transition of 3D Packaging [6]

TSV provides short electrical connections between the top and bottom surface of a silicon substrate. In silicon stacking TSVs provide short connections between transistors that are vertically separated from each other. In the area of packing, TSVs used in silicon interposers also provide short electrical path to the printed circuit board. The material properties of the medium surrounding the vertical connections in TSV modeling are making the TSV design challenging. As a semiconductor the silicon medium; losses, capacitance efforts

and coupling behavior of TSVs are unique and are quite different for similar structures in a perfectly insulating medium. Hence, the electrical modeling of TSVs becomes important.

2.2 Benefits of TSVs

3D ICs with TSVs are expected to have a broad impact in areas such as networking, graphics, mobile communications, and computing, especially for applications that require ultra-light, small, low-power devices. Specific application areas include multi-core CPUs, GPUs, packet buffers/routers, smart phones, tablets, cameras, DVD players, and set-top boxes [25]. Compared with other interconnection technologies, such as wire bonding, the advantages of TSV include: 1) Better electrical performance 2) Lower power consumption 3) Wider data width and thus bandwidth 4) Higher density. TSV technology is expected to contribute to obtaining high-performance that would be difficult using conventional technologies. For stacking of ICs TSVs provide short interconnection lengths as compared to wirebond technology. TSV addresses the data exchange issues of wire bonding and offers several other attractive advantages including shorter interconnects between the die, reducing power consumption caused by long horizontal wiring, and eliminating the space and power wasted by buffers (repeaters that propel a signal through a lengthy circuit). TSV also reduces electrical parasitic in the circuit (i.e., unintended electrical effects), increasing device switching speeds. In addition, TSV accommodates much higher input/output density than wire bonding, which consumes much more space [8].

(1) TSV technology can reduce the total wiring length, compared with 2D implementation. Shorter wiring lengths will lead to higher speeds in signal propagation and a reduction of mutual coupling which causes signal delays, and will finally result in high-speed data transmission. In addition, by using TSV technology, it is possible to increase the design flexibility, to reduce the wiring length and, finally, to increase the processing speed, by stacking and interconnecting chips which transmit and receive data frequently [6]. Due to shorter delay of TSVs, due to the smaller interconnection length (1mm long wirebond as compared to 60μm

long TSV), the speed of the processor-memory interface has increased from 3.2Gbps to 12.8Gbps [5]. Thus the use of TSVs enhances the electrical performance.

(2) Heating issues arise by electrical resistance. Further, increasing current due to parasitic capacitance increases due to the length and the number of wires also causes heating. TSV technology can reduce the wiring length which enables the elimination of such heating. As a result, reduces power consumption by cutting out power losses due to wiring resistance or parasitic capacitance. Furthermore, the shorter circuit length results in reducing the number of repeaters (signal reshaping components) while at the same time reducing the power required by such repeaters needed for compensating the decay and delay of signals [6]. Recent studies have shown that 3D DDR3 DRAM [Kang et al,2010] can be enabled by using TSVs whereby 50% reduction in standby power and 25% reduction in active power is possible as compared to quad-die package with an increase in I/O speed from 1066Mbps to 1600Mbps [5].

(3) Wide I/O memory is used in mobile applications where TSV technology is used to stacked logic and memory on top of each other. It uses a very large numbers of slow, lower pins for high bandwidth. By increasing the IO bus data between the two circuits, wide I/O increases the bandwidth. Wide I/O 2 provides up to 68GBps bandwidth, at lower power consumption (better bandwidth/Watt) with 1.1V supply voltage. From a packaging standpoint, the Wide I/O 2 is optimized to stack on top of a system on chip (SOC) to minimize power consumption and footprint [10]. The 3D TSV could be as small as 2 μm [11], which indicates the potential of wider data links composed of huge number of TSVs. The benefit of wider data bus stems from the characteristics of DMA memory access, which usually deliver large data chunk within continuous addressing spaces. Wider bus provides more data in a fixed-length memory burst and thus reduces the number of memory commands to be scheduled [11].

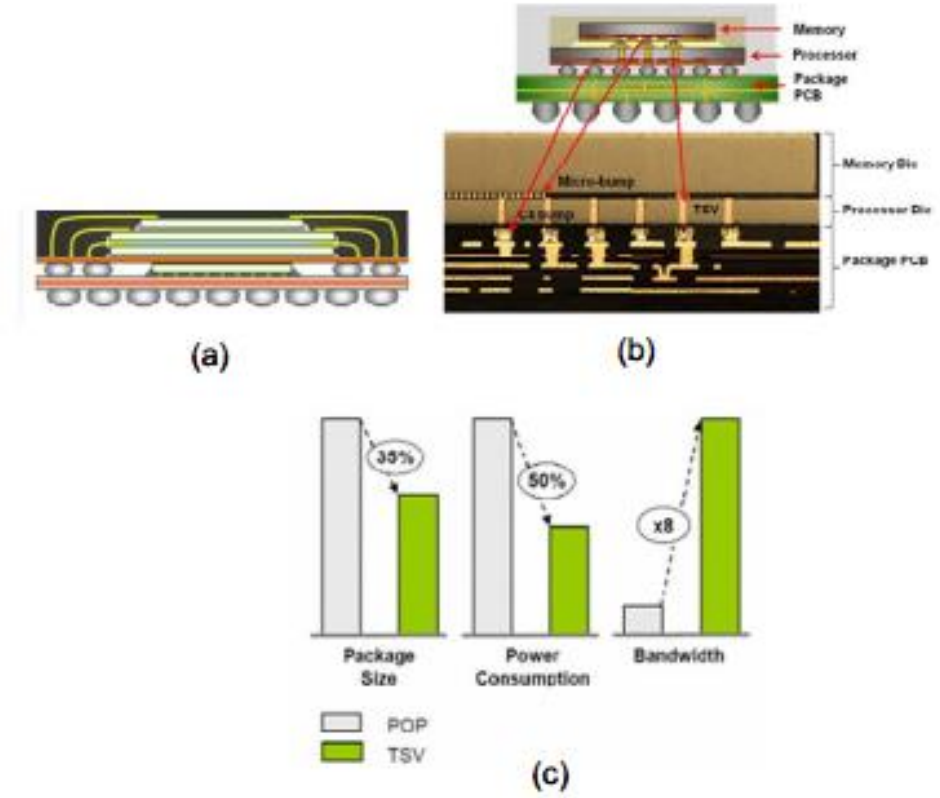


Figure 2.2: (a) FC-POP, (b) TSV-SiP with wide I/O DRAM and (d) Performance Benefits [5]

(4) As shown in the figure 3 the wirebonds on the top tier in the memory stack is around 1mm long which requires large amount of package area whereas TSV allows stacking dies onto one another and increases the density of any given package [5]. By stacking the dies, the interconnection length reduces and therefore the package area can be reduced. For high density integration, it has been reported that TSV technology can potentially be used effectively for stacking processor cores in a CPU composed of multi cores to realize a highly parallel processor.

2.3 Structural Issues of TSVs

Through-silicon-vias (TSV) has gained tremendous momentum recently in semiconductor industry. However, TSV involves disruptive manufacturing technologies. In particular, TSVs may cause significant thermal mechanical stress, which not only results in systematic mobility/performance variations, but also leads to mechanical reliability concerns such as interfacial cracking. The main structural issues with TSVs are due to high CTE difference between TSV and filling material, internal heat generation (joule heating), keep out zone and the interfacial cracking due to thermal mechanical stresses.

As different materials have different coefficient of thermal expansion, in response to a change in temperature they expand and contract differently to their CTEs which cause stresses referred as thermal mismatch stresses. In the TSV technology tungsten (W), poly-silicon, and copper(Cu) have all been considered as fill materials of TSVs. Since copper has low resistivity, it is widely used material for TSV fill. However, there is large coefficient of thermal expansion (CTE) differences between silicon substrate, dielectric material, and filled metal as the CTE of copper is six times larger than the CTE of silicon dioxide.

Table 2.1: Material Properties of Si and Cu [18]

Material	Young's Modulus [Gpa]	Poisson Ratio	Coefficient of Thermal Expansion (CTE) [ppm/^{o}C]
Silicon	169	0.26	2.3
SiO2	75	0.17	0.5
Copper	117	0.3	16.7

Due to the significant coefficients of thermal expansion (CTE) mismatch between TSV fill material such as copper and silicon substrate, thermo-mechanical stress builds up during 3D IC fabrication process and thermal cycling of TSV structures [13].

Higher CTE mismatch will generate higher thermal stress at the interface of different materials and result in materials failure or de-lamination and reduce the life of the electronic device. The tensile stress on silicon can create reliability problem such as cracking. In addition that it can change mobility of carriers. Therefore, TSV stress induced by CTE mismatch may cause timing violation if cells on a critical path are placed near TSVs [17]. This tensile stress leads to enhancement of electron mobility. Nonetheless, the mobility of hole is either intensified or degraded depending on TSV and transistor channel direction. Longitudinal tensile stress reduces the mobility of hole while transverse tensile stress increases the mobility [17].

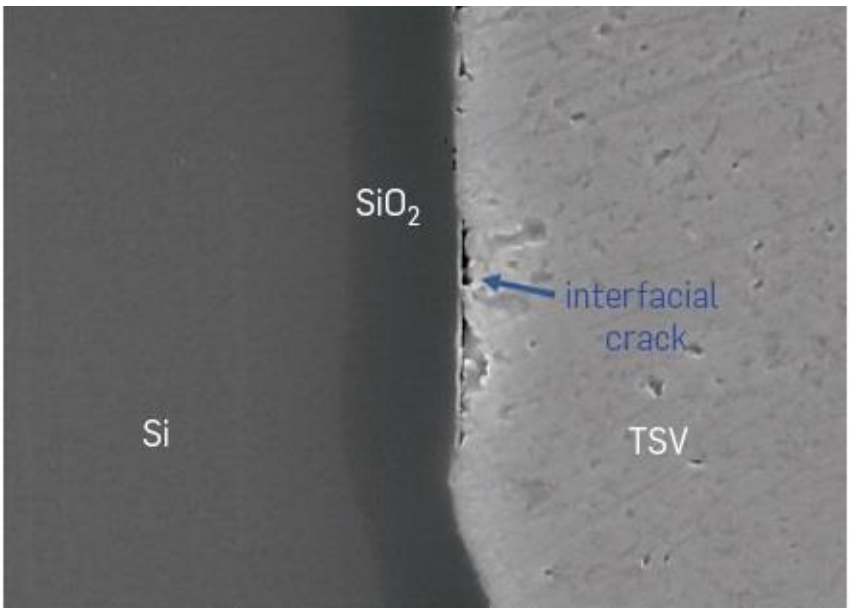


Figure 2.3: Crack growth due to thermo-mechanical stress - Interfacial crack between dielectric liner and silicon substrate [13]

These thermo-mechanical stresses not only exist in silicon active regions to the TSVs, but also in surrounding interconnect and insulation regions. De-lamination and interface de-bonding can occur in response to stress and deformation in materials around the TSVs [14]. If there is a small defect such as a void around a TSV, TSV-induced stress can drive the interfacial cracking between dielectric liner and silicon substrate or the cohesive cracking in dielectric liner and silicon substrate as shown in figure 4. These cracks may damage transistors

nearby, create conducing paths between TSVs (= short circuit), and cause the entire chip operation failure in the worst case [13]. Moreover, Through-silicon via (TSV) causes tensile stress which results in device electrical performance in their neighborhood. Keep-out zone (KOZ) is a conservative way to avoid this effect on devices by spacing away from TSV at the damage of increased overall area and cost. KOZ is the area surrounding each TSV from which all logic cells must “keep out” so that they are not influenced by the TSV-induced stress [15].

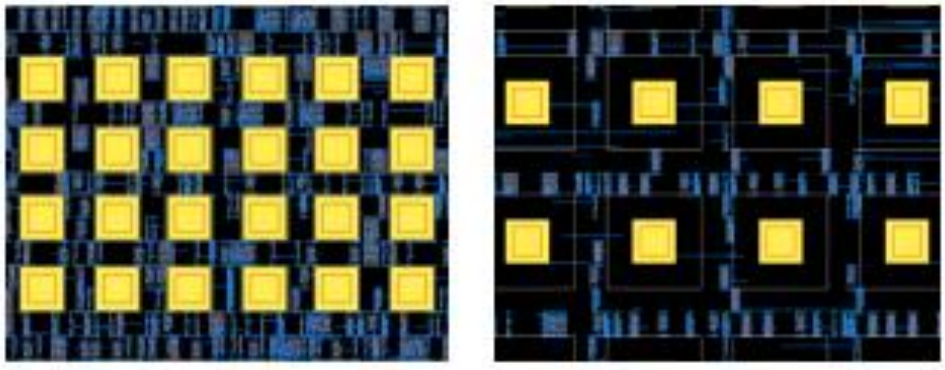


Figure 2.4: Layouts with small versus large KOZ around TSVs. TSV landing pads are large yellow squares. [15]

However, owing to already large TSV size, large KOZ can significantly reduce the placement area available for cells, thus requiring larger dies which negate improvement in wire-length. KOZ is usually large because it is defined such that stress outside it is under preset tolerance [15]. Large KOZ only worsens the situation as illustrated in Fig. 1 as it reduces the TSV stress-induced carrier mobility variation in surrounding logic cells at the cost of increasing die size [15].

The current passing through the TSVs results in localized heat generation (joule heating), which could be detrimental to the device performance [1]. It can cause a substantial change in the junction temperature which could be quite detrimental to the over-all performance of 3D IC. During high current stressing in the solder joints, the effect of current crowding and Joule heating is responsible for the failure in the chip/anode side of the solder joints [16]. The

primary contributor for Joule heating in the solder joints is to be the extremely thin and small dimension of Cu or Al traces on the Si chip [16]. Further investigation in this area will be carried out in this work.

Chapter 3

Fracture of TSV structures

Due to CTE mismatch thermo-mechanical stresses originating from within the IC which could causes TSV fracture. FEA technology offers variety of Fracture Mechanics models such as J integral approach, Stress Intensity Factor approach, etc.

3.1 J- integral based fracture Criteria

The J-integral parameter is used in assessing fracture integrity of cracked engineering structures, which undergo large plastic deformation at the crack tip. The J-integral is valid for nonlinear elasticity or deformation theory of plasticity where no or little unloading occurs. It is frequently used to characterize initiation of crack growth and a small amount of crack propagation. The J integral approach is a general energy release rate approach applicable to non-linear materials [20]. In this study, the elastic-plastic analyses of cracks will focus only on the J-integral fracture parameter. For a cracked body with the crack tip, a definition of J under mode-I condition is

Equation 1

$$J = \int_{\Gamma} \left(w dy - T_i \frac{\partial u_i}{\partial x} ds \right)$$ [19]

Where, w is the strain energy density with components of stress and strain tensors and Ti = σij*ni are the ith component of displacement and traction vectors, nj is the jth component of unit outward normal to integration path, dS is the differential length along contour C, and ui,1 = $\left(\frac{\partial u}{\partial x}\right)$ is the differentiation of displacement with respect to x1 [19]. In Finite Element Analysis, the energy domain integral methodology is used for numerical calculation of J. The initiation of

crack growth in a structure containing flaws can be characterized when the crack driving force exceeds the material fracture roughness.

Equation 2

$$\text{Crack initiation} \quad J = J_{Ic}$$

$$\text{Crack instability} \quad \begin{cases} J = J_R \\ \frac{\partial J}{\partial a} = \frac{dJ_R}{da} \end{cases}$$

[19]

Equation (2) represents this failure criterion. This is a good definition of failure when the uncracked ligament is small (e.g., part-through surface cracks in pipes or through-wall cracks in small-diameter pipes) or the amount of subsequent stable crack growth is limited (e.g., cracks in brittle materials) [19].

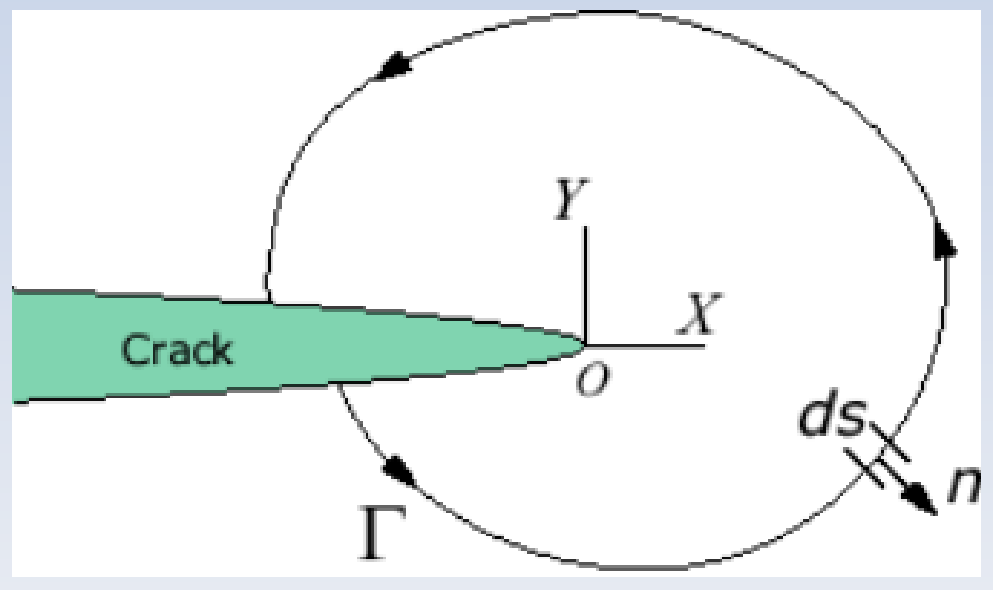


Figure 3.1: J integral as a fracture parameter – arbitrary contour around a crack tip [20]

The stable crack growth, if occurs in a structure, can also be characterized by the J integral parameter with some limitations. In this regard, the J-tearing theory is a very prominent

concept to quantify the stable crack growth. It is based on the fact that fracture instability can occur after some amount of stable crack growth in tough and ductile materials with an attendant higher applied load level at fracture. The onset of fracture instability is defined when J and $\partial J/\partial a$ exceed JR and $dJ_R=da$ simultaneously, as also expressed by Eq. (3). The corresponding crack-instability load is either equal to or higher than the crack-initiation load. The difference between these two failure loads can be significant, if the structural geometry and material permit appreciable amount of stable crack growth. Otherwise, the fracture criterion based on the initiation of crack growth provides a conservative estimate of structural integrity [19].

3.2 Stress Intensity Factor Approach

The stress intensity factor approach is applicable to provide a failure criterion for a homogeneous, linear elastic material, and brittle materials. The stress state near the tip of a crack due to residual loads is determined by the stress intensity factor. When this stress state becomes critical a small crack grows ("extends") and the material fails. The load at which this failure occurs is referred to as the fracture strength. The experimental fracture strength of solid materials is 10 to 1000 times below the theoretical strength values, where tiny internal and external surface cracks create higher stresses near these cracks, hence lowering the theoretical value of strength [21]. Stress Intensity, K, as the name implies, is a parameter that amplifies the magnitude of the applied stress that includes the geometrical parameter Y (load type). These load types are categorized as Mode-I, -II, or -III. The Mode-I stress intensity factor, K_{Ic} is the most often used engineering design parameter in fracture mechanics and hence must be understood if we are to design fracture tolerant materials used in bridges, buildings, aircraft, or even bells. Typically for most materials if a crack can be seen it is very close to the critical stress state predicted by the "Stress Intensity Factor" [21]. The magnitude of *K* depends on sample geometry, the size and location of crack, and the magnitude and the model distribution of loads on the material. Crack tips produce a $1/\sqrt{r}$ singularity. The stress fields near a crack

tip of an isotropic linear elastic material can be expressed as a product of $1/\sqrt{r}$ and a function of θ with a scaling factor *K* [31].

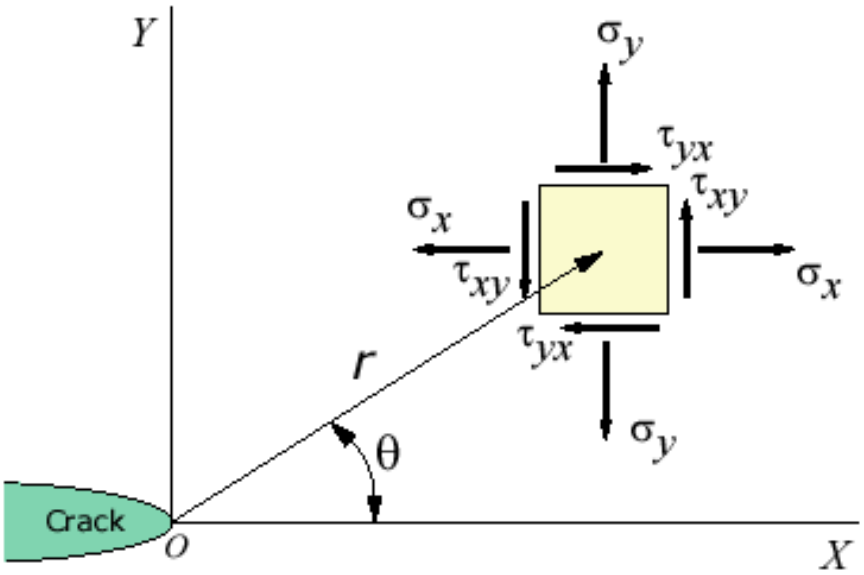


Figure 3.2 : Distribution of stresses in vicinity of crack tip [30]

Equation 3

$$\lim_{r \to 0} \sigma_{ij}^{(I)} = \frac{K_I}{\sqrt{2\pi r}} f_{ij}^{(I)}(\theta)$$

$$\lim_{r \to 0} \sigma_{ij}^{(II)} = \frac{K_{II}}{\sqrt{2\pi r}} f_{ij}^{(II)}(\theta)$$

$$\lim_{r \to 0} \sigma_{ij}^{(III)} = \frac{K_{III}}{\sqrt{2\pi r}} f_{ij}^{(III)}(\theta)$$

[30]

Where the superscripts and subscripts *I*, *II*, and *III* denote the three different modes that different loadings may be applied to a crack. The factor *K* is called the **Stress Intensity Factor [**30**]**.

3.3 Stress Intensity Factor and Fracture Toughness

Based on the linear theory the stresses at the crack tip are infinity but in reality there is always a plastic zone at the crack tip that limits the stresses to finite values. It is very difficult to model and calculate the actual stresses in the plastic zone and compare them to the maximum allowable stresses of the material to determine whether a crack is going to grow or not. An engineering approach is to perform a series of experiments and reach at a critical stress intensity factor K_c for each material, called the **fracture toughness** of the material. One can then determine the crack stability by comparing *K* and K_c directly [31].

Equation 4

$$K_{Ic} = Y \sigma \sqrt{\pi a} \quad [21]$$

Where Y is a dimensionless parameter that depends on both the specimen and crack geometry, and the Greek symbol "Sigma" is an applied stress and "a" is crack length [21]. Fracture toughness is a quantitative way of expressing a material's resistance to brittle fracture when a crack is present. If a material has much fracture toughness it will probably undergo ductile fracture. Brittle fracture is very characteristic of materials with less fracture toughness [31].

3.4 Fracture modes

There are three different kinds of fracture modes of crack tip deformation, the opening (Mode I), the in-plane shear (Mode II), and the out-of-plane shear (Mode III). Mode I is tensile mode crack whereas Mode II and III are shear mode cracks. Mode I is the most common load type encountered in engineering design. In Mode I, the crack surfaces move directly apart under tensile stress as shown in figure 3.3. The deformations in mode I are symmetric with respect to the planes perpendicular to the y axis and the z axis.

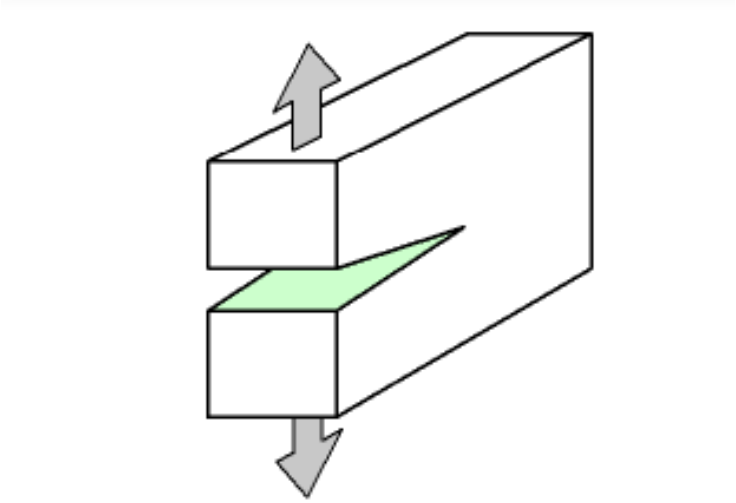


Figure 3.3: Mode I fracture [30]

Furthermore the tensile mode has two types of crack, R-crack, C-crack. Interfacial crack is the shear mode as well as tensile mode type crack. R -crack may grow in Si during heating ($\Delta T > 0$) when the circumferential stress is tensile ($\sigma\theta > 0$). C -crack may grows in Si during cooling ($\Delta T < 0$) when the radial stress is tensile ($\sigma r > 0$). Interfacial crack can grow during both heating and cooling, leading to pop -up of TSV [32].

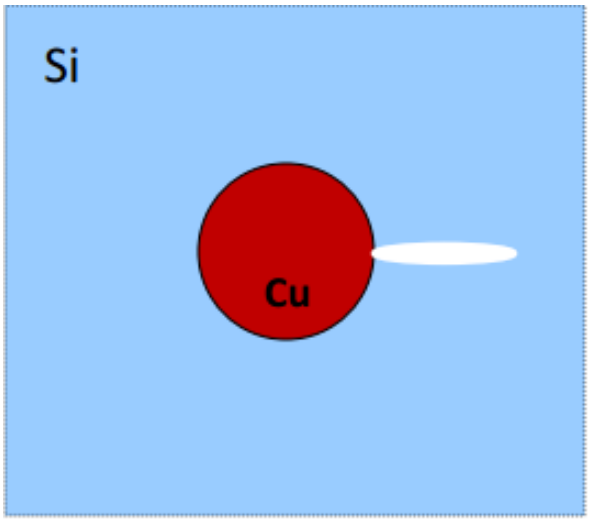
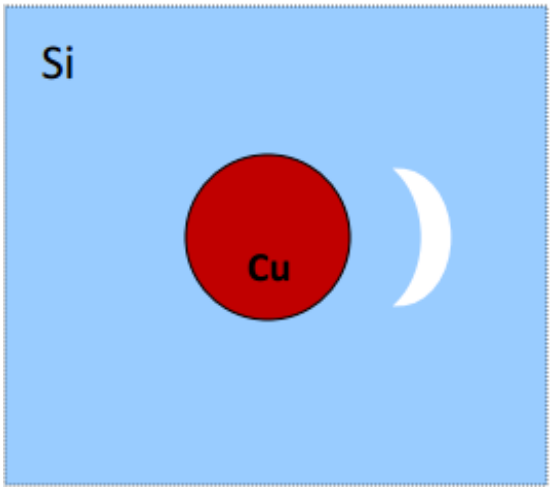


Figure 3.4 : R-crack due to tensile mode [32]



Figue 3.5: C-crack due to tensile mode [32]

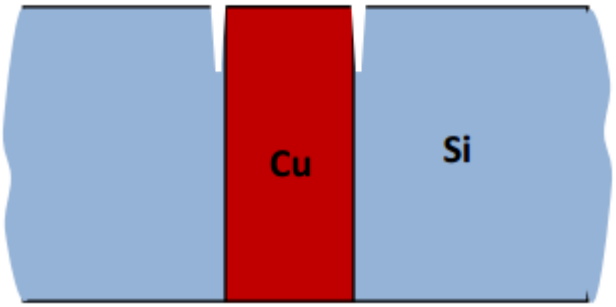


Figure 3.6: Interfacial crack due to shear mode & tensile mode [32]

The tensile stress in X and Y directions, and the shear stress in the X-Y plane can calculated in terms of K and position can be written as [31]:

Equation 5

$$\sigma_y = \frac{K}{\sqrt{2\pi r}} \cos\frac{\theta}{2}\left(1 + \sin\frac{\theta}{2}\sin\frac{3\theta}{2}\right)$$

$$\sigma_x = \frac{K}{\sqrt{2\pi r}} \cos\frac{\theta}{2}\left(1 - \sin\frac{\theta}{2}\sin\frac{3\theta}{2}\right)$$

$$\tau_{xy} = \frac{K}{\sqrt{2\pi r}}\left(\sin\frac{\theta}{2}\cos\frac{\theta}{2}\cos\frac{3\theta}{2}\right)$$

(6)

Crack initiation and propagation accompany fracture. The manner through which the crack propagates through the material gives great insight into the mode of fracture. In ductile materials (ductile fracture), the crack moves slowly and is accompanied by a large amount of plastic deformation. The crack will usually not extend unless an increased stress is applied. On the other hand, in dealing with brittle fracture, cracks spread very rapidly with little or no plastic deformation. The cracks that propagate in a brittle material will continue to grow and increase in magnitude once they are initiated [32].

Mode II is sliding or in-plane shear mode where the crack surfaces slide over one another in a direction perpendicular to the leading edge of the crack [21].

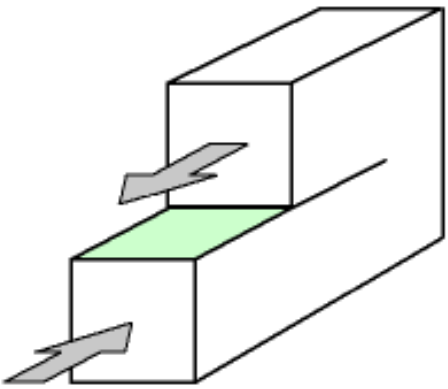


Figure 3.7: Mode II fracture [30]

Mode III is tearing and anti-plane shear mode where the crack surfaces move relative to one another and parallel to the leading edge of the crack [21].

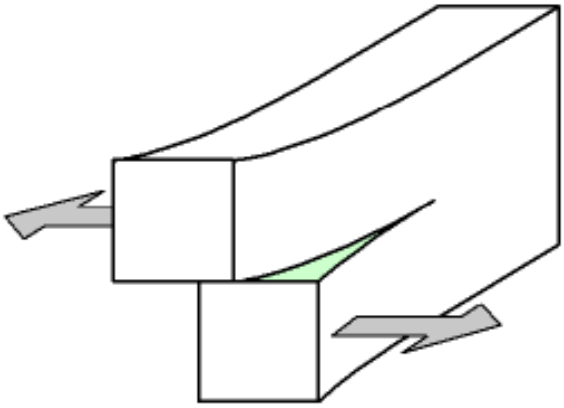


Figure 3.8: Mode III Fracture [30]

Another important mannerism of crack propagation is the way in which the advancing crack travels through the material. A crack that passes through the grains within the material is undergoing transgranular fracture. However, a crack that propagates along the grain boundaries is termed an intergranular fracture [31].

Chapter 4

Finite Element Modeling and Analysis

4.1 Model Description

ANSYS Mechanical 15 was used to implement Finite Element Method. This research presents two kinds of cases, the first study has been carried out on the compact model from [1] work for interfacial de-lamination under two kinds of thermal cycling and the second study was the fracture mechanics analysis involves Cu/SiO2 interfacial cracks and Si cracking. The former presents the reliability issue in 3-D TSV structures subjected to continuous thermal cycling and reports the interfacial de-lamination in copper-filled TSVs which built up by interfacial shear stresses. The latter demonstrates the thermo-mechanical reliability issues induced by Cu filled TSV stress, this work is addressing TSV cracking by locating a crack in the middle at the interface of Cu TSV and SiO2, and Si cohesive cracking where the crack is set to be of the same length.

In the first study, a 3D TSV package is modeled to demonstrate the technique for structural integrity of TSV/SiO2 interface region under thermal cycling. The package footprint is based on a HDI mobile application package (memory-on-logic) footprint (see Figure) [1-57]. The Quarter symmetric model from [1] work has been considered to determine the possible interfacial de-lamination caused by the high thermal expansion difference between Cu & Si.

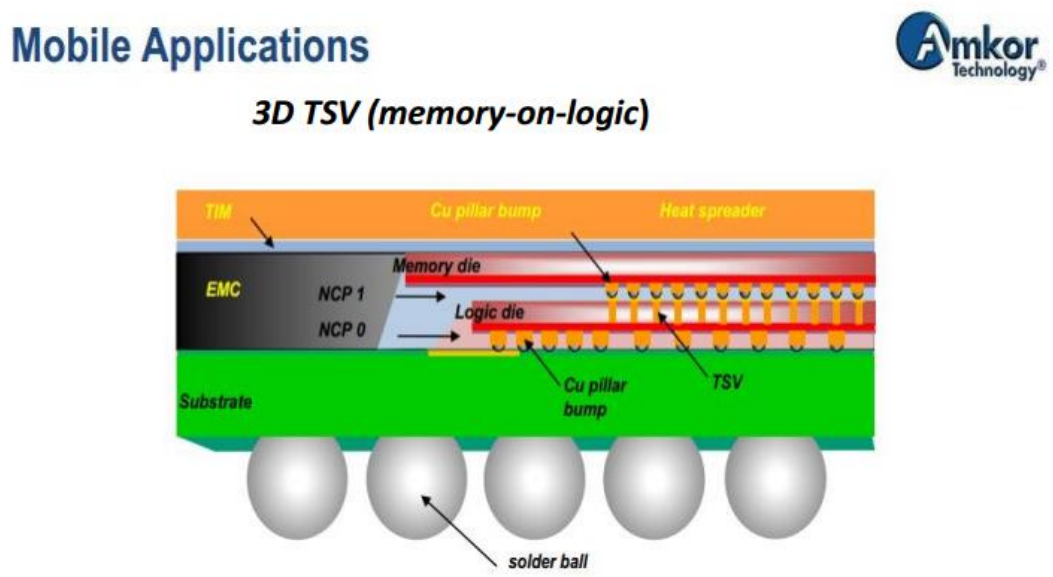


Figure 4.1: Package footprint [1]

Further to simplify the analysis, sub-modeling has been leveraged to focus particularly the interface region. In the sub-model, SiO2 liner (1 µm thick) is considered to capture the interfacial interaction of Cu/SiO2 region. In this compact model the TSV diameter is taken as 9 µm. The following figures [ ] and [ ] shows the global quarter symmetric model and the compact model.

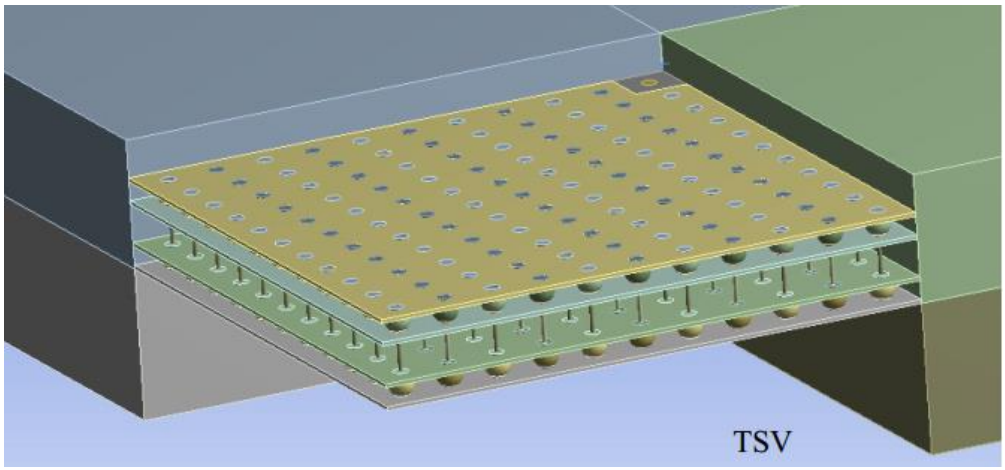


Figure 4.2: Quarter symmetry model – internal view [1]

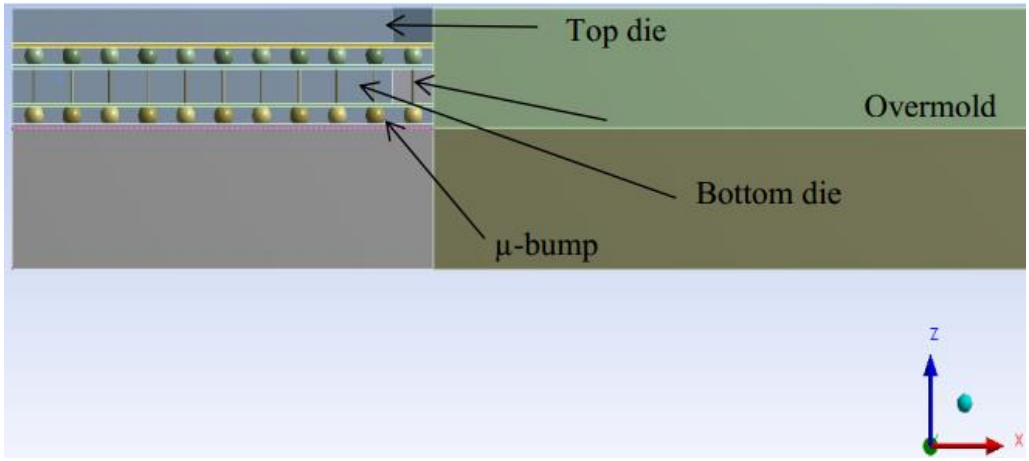


Figure 4.3: Package Cross-section [1]

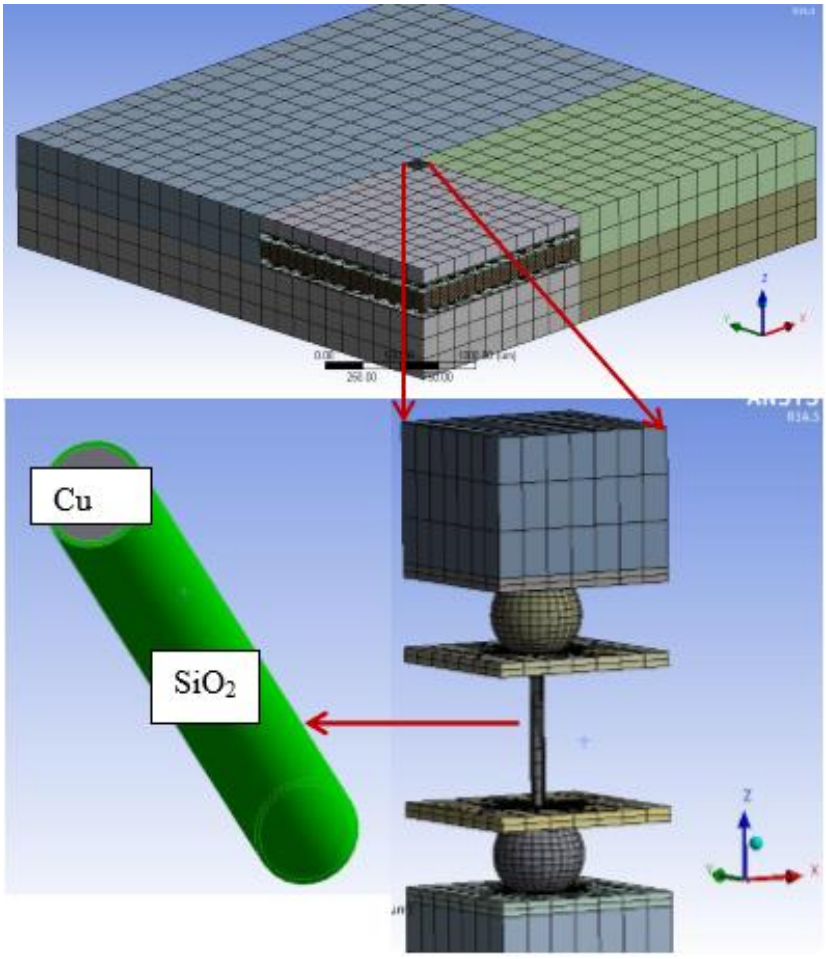


Figure 4.4: Corner region (detailed view) [1]

Figure shows the ANSYS models for a smaller array footprint which is feasible for practical computational times. In this sub-model only Si die with Cu TSV and SiO2 Liner is thermal cycled. The model is simulated under two kinds of thermal loading of -25˚C to 135˚C and 25˚C to 425˚C for linear & non-linear case. Thermal cycling profile is shown in figure :

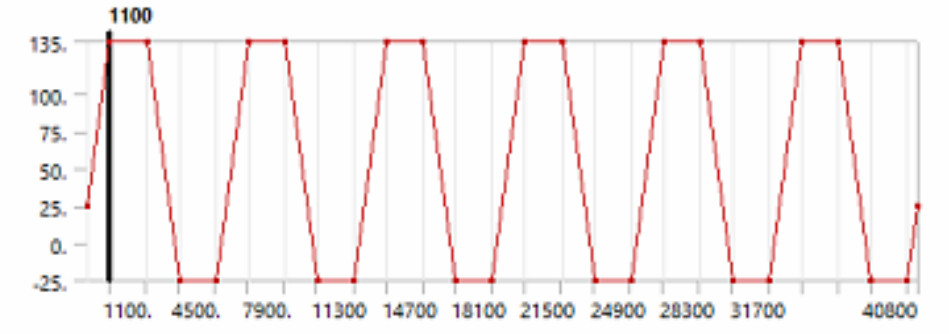


Figure 4.5: Thermal cycling profile (-25˚C to 135˚C)

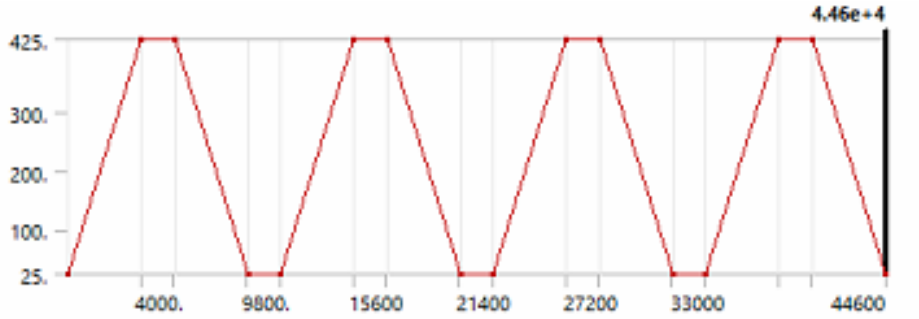


Figure 4.6: Thermal cycling Profile (25˚C to 425˚C)

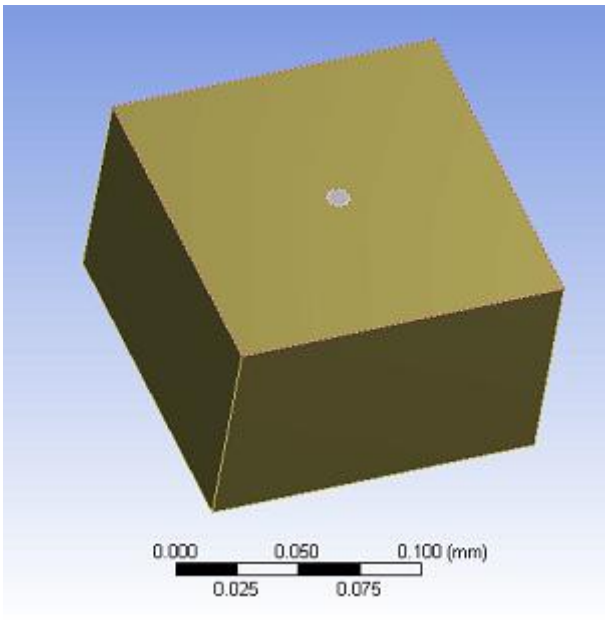


Figure 4.7: Si Die with Cu TSV & SiO2 Liner

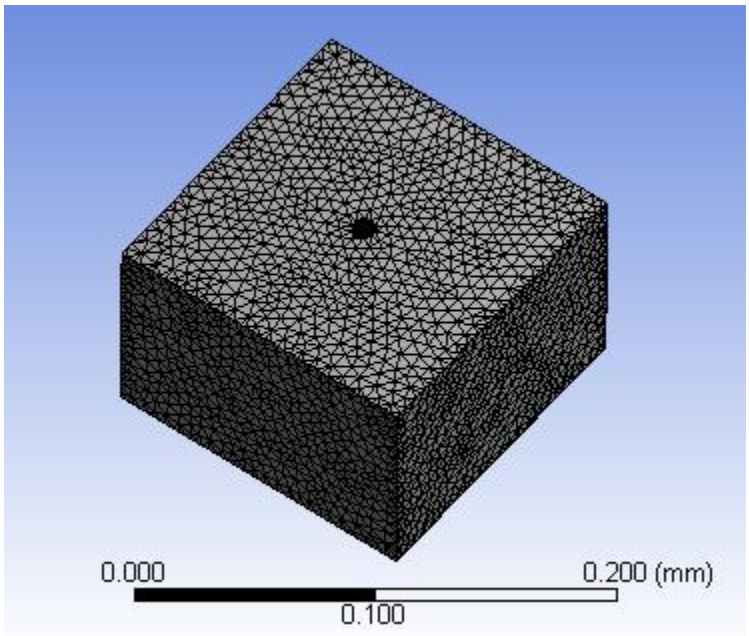


Figure 4.8: Meshed Sub Model

For the non-linear modeling the Elastic-Plastic copper is used. Multi linear isotropic Hardening was used for the elastic-plastic simulation. Figure shows the plastic strain-stress diagram.

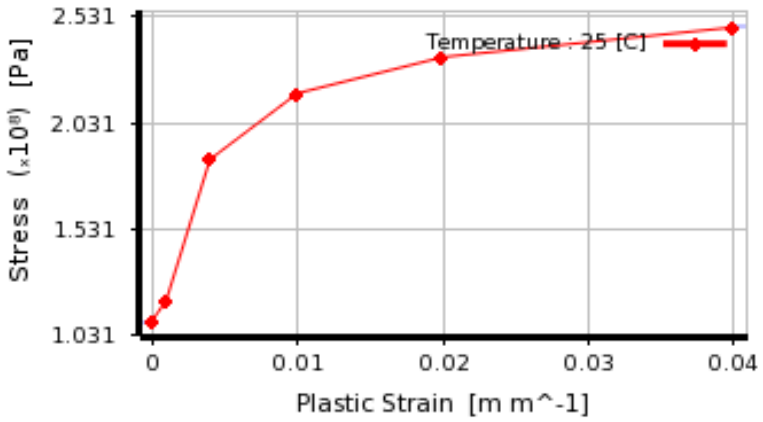


Figure 4.9: Plastic Strain – Stress Diagram

When the stresses on a ductile material become higher than the elastic limit, material will yield, developing large permanent deformation. The material response beyond yield referred as Plasticity. Plasticity is a property of materials to undergo irreversible deformation without any increase in stresses or loads [35]. The yield criterion of Cu is compared with that of the equivalent stresses (Von-Mises stresses). The transition from elastic to plastic behavior is called yield [35].

4.2 Cracked Simple Model

A simplified approach has been taken to model the crack. The model is similar to the sub model as it considers a Cu TSV with SiO2 dielectric embedded in Si wafer. An assumption has been made for the cracking here as because of a SiO2 liner the possibility of having Si crack is less but the layer of SiO2 is considerably thin. So this research considers Si cracking as well as interfacial cracking. Higher mismatch of thermal expansion leads to yielding in creep. The amount of creep endurance is limited and then it will begin to crack. Thermal cycling can potentially drive Si cracking and Interfacial crack growth. The interfacial failure of the TSV/SiO2 by the presence of shear stress under both heating and cooling conditions has been focused.

The comparison among the different aspect ratio models have been made to find the crack driving force. Relatively higher aspect ratios are considered by keeping the diameter

constant and varying the height of the model. Further the effects of increased diameter of TSV was evaluated by keeping the liner diameter same. The modeling of crack depends on the critical stressed locations as well as at the center of the interface. Based on J-integral method critical energy release rate was derived for both linear Cu and elastic-plastic copper. As there are three basic modes of fracture, the critical energy release rate corresponding to these three modes were determined. The following figure shows the crack on TSV/SiO2 liner. This is the first case to be considered.

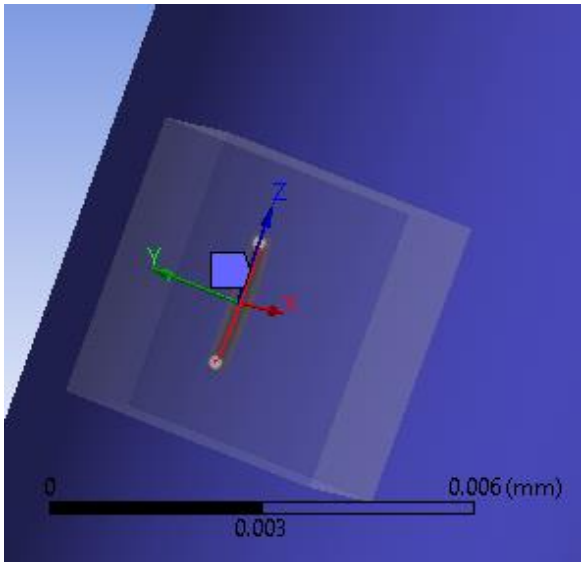


Figure 4.10: Crack at the center of Cu TSV

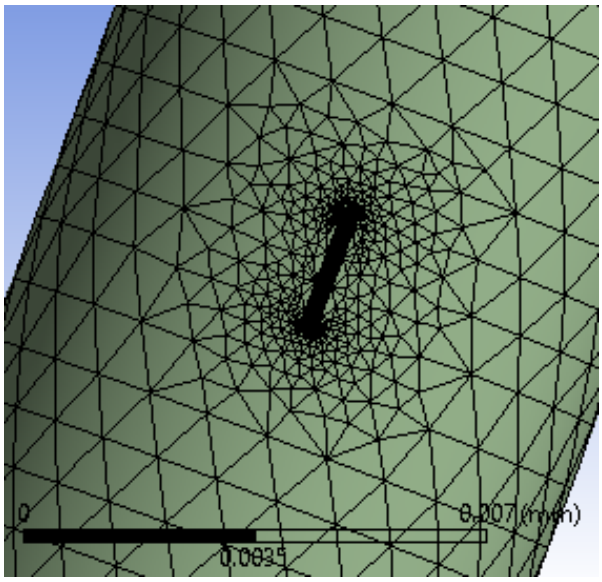


Figure 4.11: Crack Mesh on Cu TSV

Similarly the following figure shows the crack in Si at an assumed location.

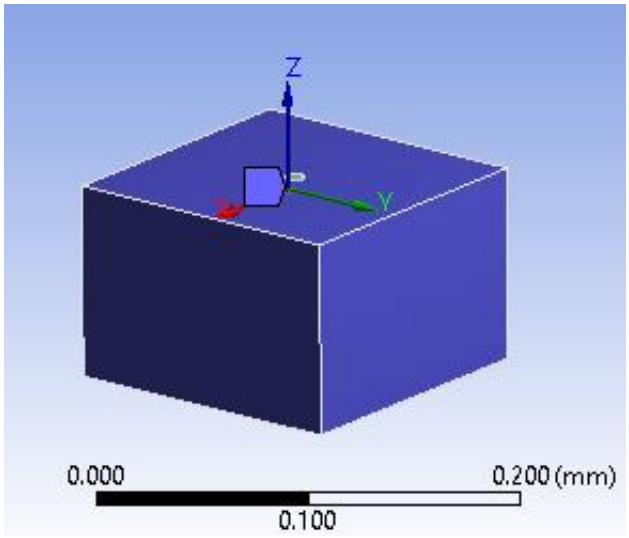


Figure 4.12: Si Cracking

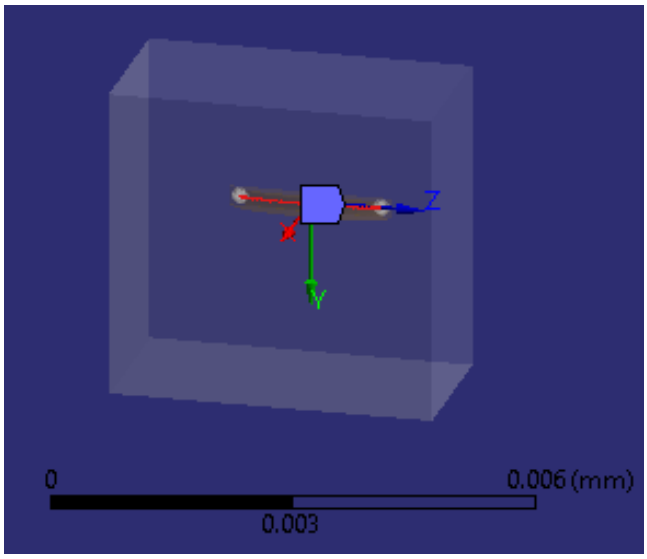


Figure 4.13 : Crack on Si Surface

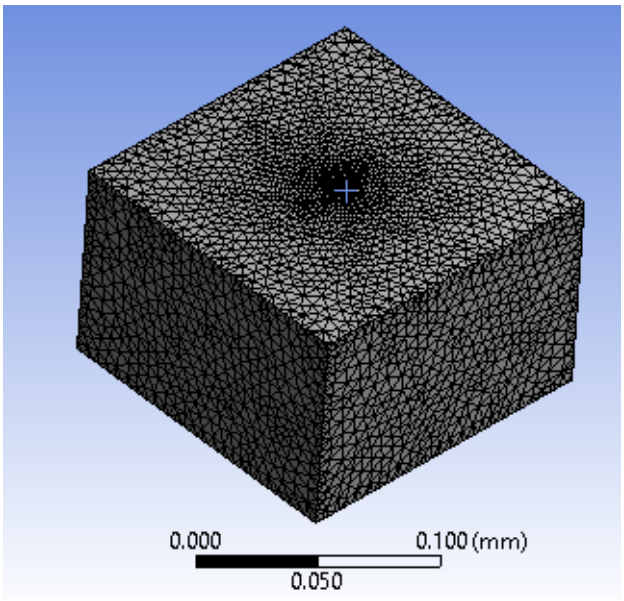


Figure 4.14: Crack Mesh in Si

The model was meshed with the fine meshing option. To ensure the optimum number of elements for the model, mesh sensitivity analysis was carried out. The simplified model has reduced mesh count which add into speeding up the solution process. It is necessary to perform mesh sensitivity analysis so that the quality of results is not compromised with the short computational time. In the model each layer is assumed to be perfectly bonded to each other.

4.3 Material Properties and Dimensions

All the material properties used in the analysis of global/compact model of first study are derived from [1] and as shown in Table.

Table 4.1: Material properties for first study

Material	E – GPa	v	CTE – ppm/^{o}C	Plastic curve for Cu	
Die	131	0.28	3		
Die Attach	10	0.3	33		
Solder Mask	4	0.4	52		
Over Mold	5, 25, 40	0.3	8,32 (post Tg)		
Cu Pad	110	0.34	17		
Cu TSV	121	0.3	17.3	Strain	Stress
				.001	121
				.004	186
				.01	217
				.02	234
				.04	248
SiO2	71.4	.16	.5		
Linear Cu	121	0.3	17.3		
Polyimide	1.2	.34	52		

Table 4.2: Package Dimensions

Component	Thickness (µm)	Length (mm)	Width (mm)	Diameter (µm)	Height (µm)
Silicon Die	100	3	3		
TSV	10	-	-	9	100
SiO2	0.5			10	
Substrate	400	5	5	-	-
Solder Bumps	-	-	-	80	90

The material properties and the model dimensions of the simple model of second study is as shown in the below table.

Table 4.3: Model Dimensions of second study

Component	Thickness (µm)	Length (mm)	Width (mm)	Diameter (µm)	Height (µm)
Silicon Die	95	0.143	0.143	-	
SiO2	10				
TSV	9	-	-	9	95

Table 4.4: Material Properties for second study

Material	E – GPa	v	CTE – ppm/^{o}C	Plastic curve for Cu	
				Stress (MPa)	Strain
Cu TSV	70	0.34	18	110 120 186 217 234 248	0 0.001 0.004 0.01 0.02 0.04
SiO2	70	0.16	0.6		
Silicon Die	130	0.28	2.6		

Chapter 5

Results and Discussion

5.1 Case -1: Compact model Study

Talking about the first study, [1] work involves feasibility of compact modeling technique where the compact model was validated against its full array counterpart for different output parameters including stress-strain distribution in the Cu/TSV region. The Von-Mises stress in TSV (Cu region) was 156 MPa Max and 115 MPa Min as shown in the figure , which was above the yield strength of Cu (70 MPa) for this case. So there is a possibility of potential interfacial crack in Cu TSVs and Si cracking due to high thermal mismatch. The compact model of [1] work has been thermal cycled under two kinds of thermal loading of -25˚C to 135˚C and 25˚C to 425˚C for linear & non-linear case.

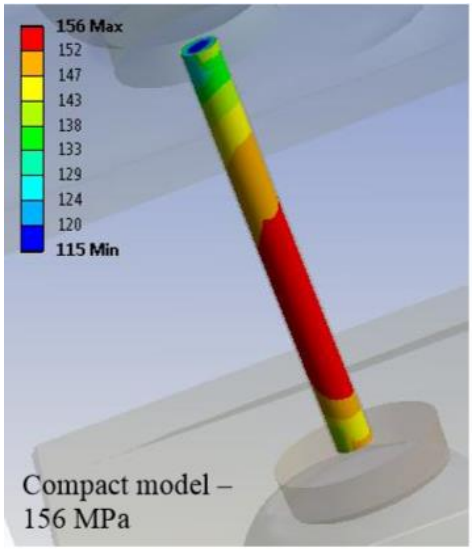


Figure 5.1: Von-mises stress in TSV (Cu region- sub model)

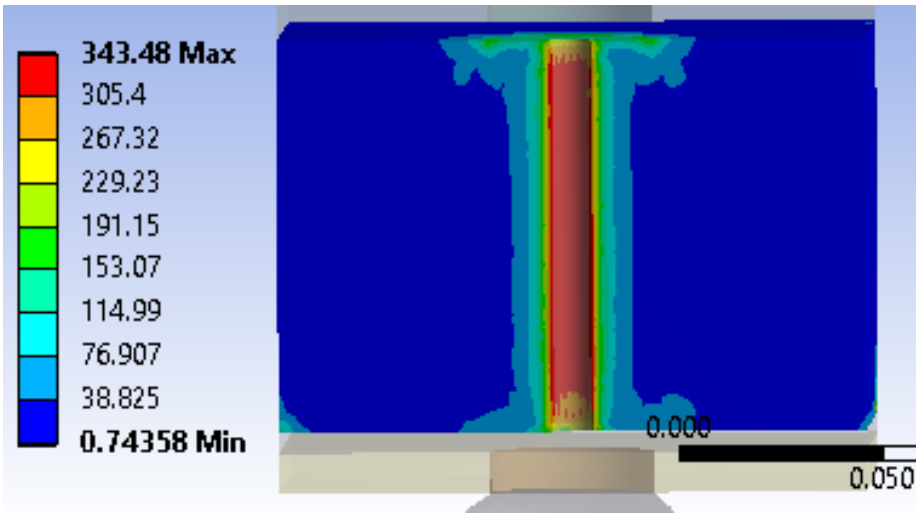


Figure 5.2: Von-Mises stress in Si (sub-model)

Table shows the comparison of linear and non-linear analysis for linear copper & elastic-plastic copper.

Table 5.1: Stress and strain distribution in Cu TSV for linear/ nonlinear case

	Equivalent Von-Mises stress (MPa) for -25˚C to 135˚C	Equivalent Von-Mises stress (MPa) for 25˚C to 425˚C
Linear Cu TSV	573.43	403.95
Elastic-plastic Cu TSV	110.68	247.7

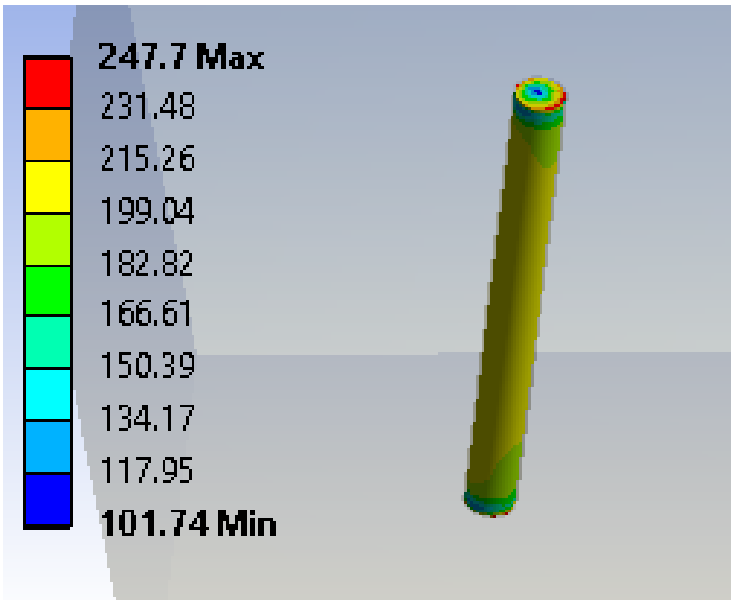


Figure 5.3: Equivalent stress in Elasto-plastic Cu TSV under 25˚C to 425˚C

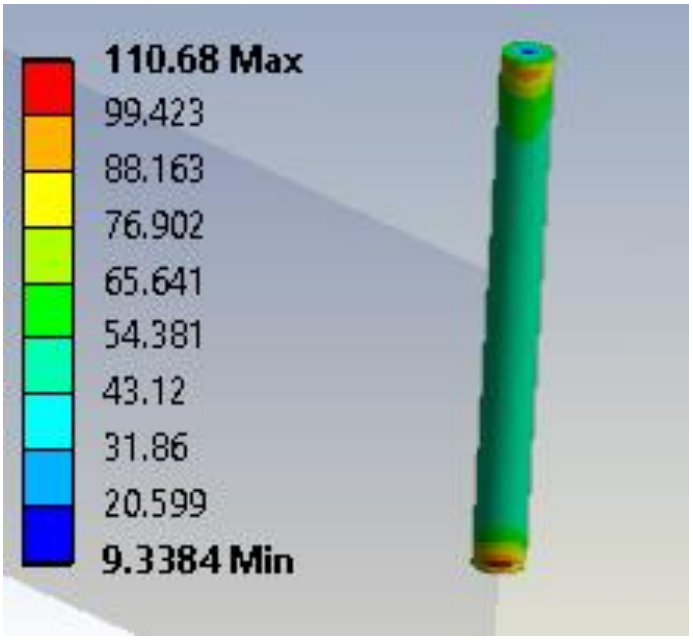


Figure 5.4: Equivalent stress in elasto-plastic Cu TSV under -25˚C to 135˚C

A linear FEA analysis has been undertaken to observe the Cu TSV behavior. It can be inferred from the table that the Cu TSV experiences higher Von-Mises stress which is much

higher than the yield strength for Cu and it is necessary now to perform he non-linear analysis. So the non-linear analysis is performed in order to determine the plastic behavior of Cu TSV.

The non-linear analysis results for two different cycling suggest that in comparison to the small thermal cycling at low temperatures at the large thermal cycling at high temperatures, plasticity and/or creep is activated, result in significant stresses in Cu which ultimately causes interfacial sliding. Interfacial shear stresses are higher due to maximum CTE mismatch under large thermal cycles which is responsible for the interfacial de-lamination.

5.2 Case-2: Simple Model Fracture Analysis

The methodology used in this simple model of the second study can be implemented to the compact model of first study. Again the linear and nonlinear thermal stress analyses for TSVs have been performed. The model has been heated up to 425˚C and stress analysis has been performed to get the idea of possible critical locations. This analysis shows the high stress concentration near the interface between Cu TSV and SiO2 liner results into top-up TSV. In this case ($\Delta T>0$), the interfacial crack develops with a pure shearing mode and causes mode II fracture. J-integral approach is used for the linear elastic and elastic-plastic analyses of crack to characterize the growth rate using Paris law. Critical strain energy release rate has been calculated for three modes of fracture toughness.

The model has an aspect ratio of 10 which has been varied to find the crack driving force. It is evident that as the aspect ratio increases Von-Mises stresses on Cu TSV increases and the energy release rate increases. The following figures showcase the Equivalent stresses in TSV for the model of aspect ratio 10 under heating and cooling conditions.

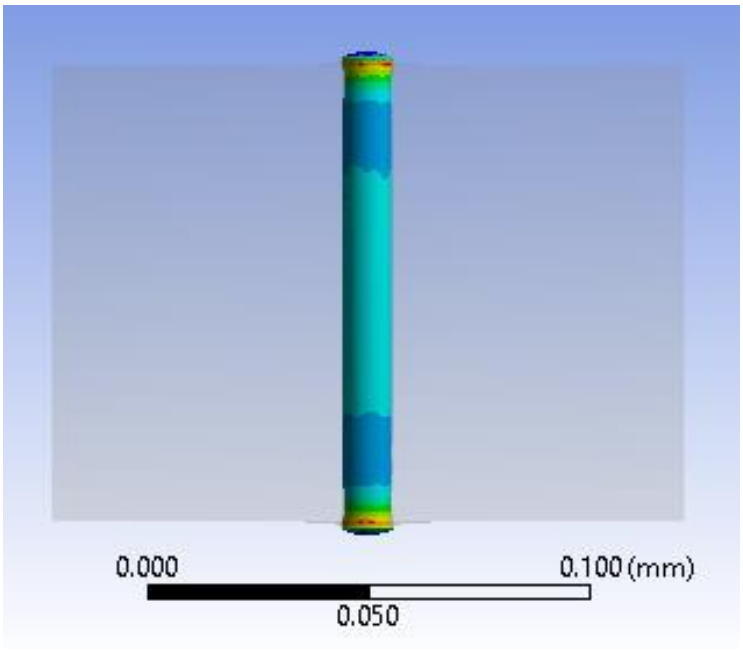


Figure 5.5: TSV pop-up under heating conditions

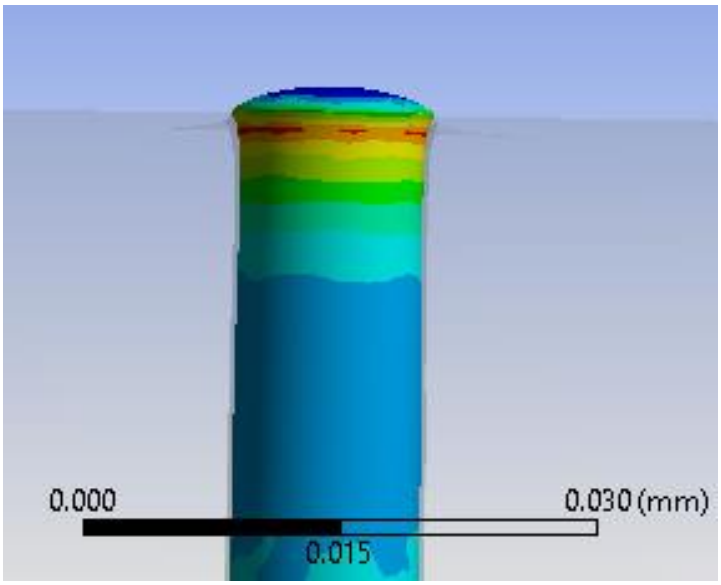


Figure 5.6: Enlarged view of TSV pop-up

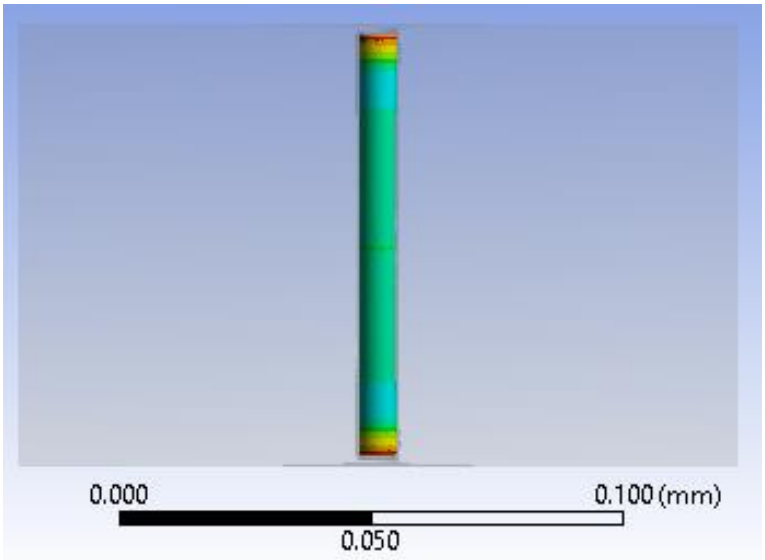


Figure 5.7: Contraction of TSV under cooling conditions

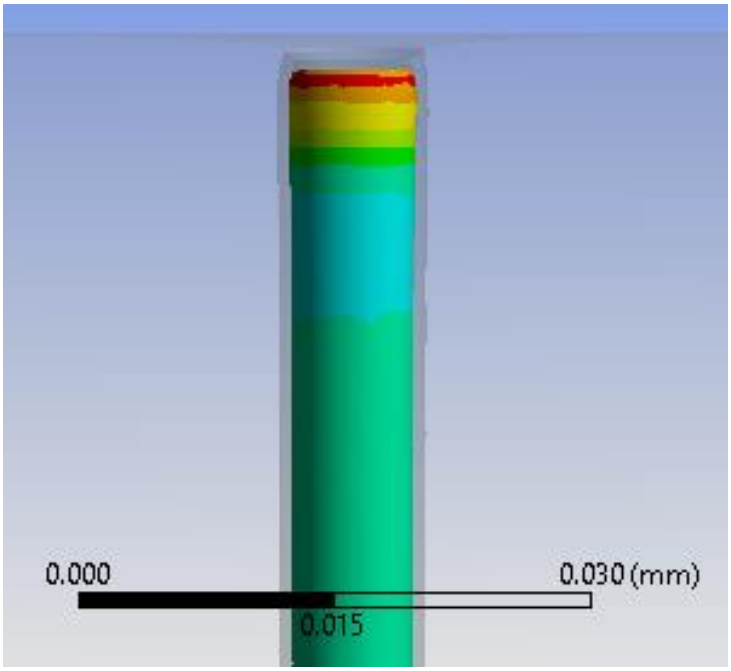


Figure 5.8: Enlarged view of TSV contraction

The above figures suggest that for the model with relatively high aspect ratio of 10, interfacial delamination drives due to both the shear stress and the tensile stress in case of

cooling conditions and leads to mixed mode fracture. Apparently under heating conditions the interfacial crack is propelled only by shear stress.

In this research only cracking is considered only under the heating conditions. Following figure shows the changes in strain energy release rate by increasing the thickness of Si for Cu cracking in the linear elastic & elastic-plastic model under heating conditions.

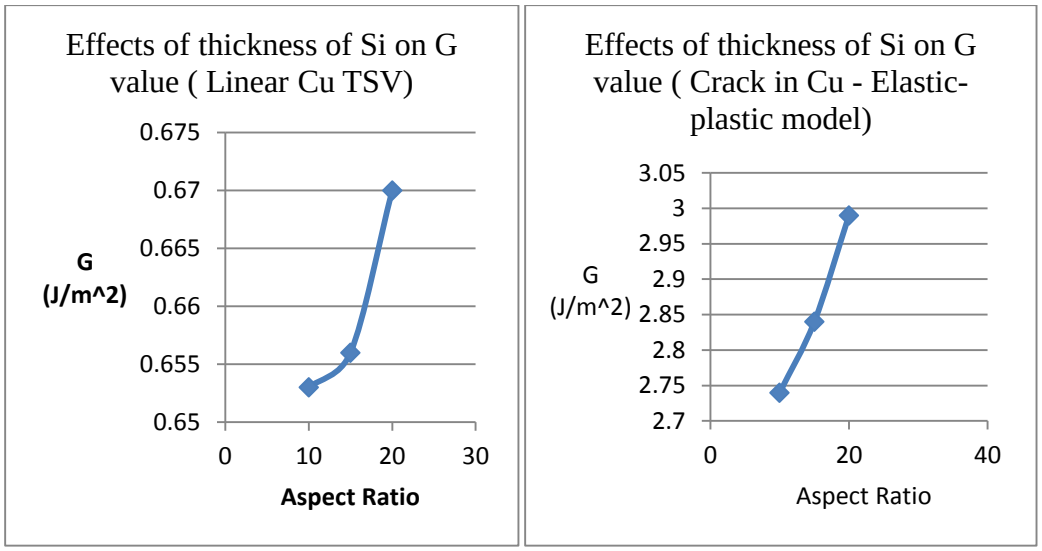


Figure 5.9: Effects of thickness of Si on G value (Linear & Elastic-plastic Cu TSV)

It can be inferred from the above figures that strain energy release rate increases by increasing the thickness of the Si die in both the linear elastic & elastic-plastic model under heating conditions. The debonding energy of Cu/SiO2 interface is 0.7 to 10 J/m^2. The values of strain energy release rate are less than of their critical value so crack would not be growing in linear elastic model. In case of elastic-plastic model interfacial delamination was occurred.

When the elastic-plastic model is considered, structural integrity of Si & Cu has been calculated by comparing the stress intensity factor with fracture toughness of Si. The calculated stress intensity factor (KI, KII & KIII) for three different aspect ratios was then compared with the fracture toughness of the silicon in case of Si cracking as shown in figure.

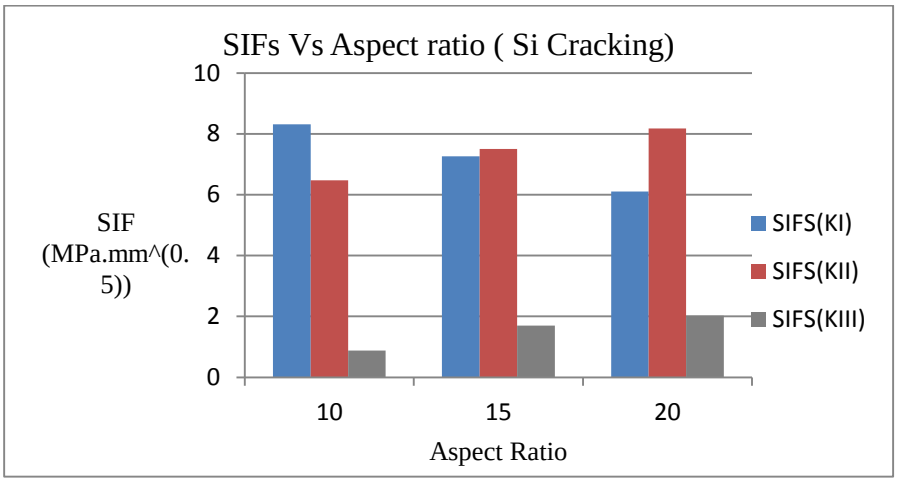


Figure 5.10: SIFs Vs Aspect Ratio (Si Cracking)

This comparison of stress intensity factors of three modes for three different aspect ratios indicates that KI decreases with the increase in thickness of Si whereas KII & KIII increases with the increases in the thickness of Si. For a brittle material like Silicon the fracture toughness is given according to the crystal directions and mainly failure occurs along 111 plane and its value for K_{1c} is given as 0.83 to 0.95 MPa.m^(0.5) [34]. So the values obtained were less than of this critical value which implies that Si wouldn't break under these conditions.

Chapter 6

Conclusion

6.1 Conclusion

Finite element model of 3D TSV package was developed. Finite element analysis was carried out on the compact model from [1] work to find the potential interfacial de-lamination under two kinds of thermal cycling and the fracture mechanics analysis was established to find the structural integrity of Si & Cu for Cu/SiO2 interfacial cracks and Si cohesive cracks. As expected the equivalent stresses in linear elastic compact model were higher than that of the nonlinear compact model. The non-linear analysis results for two different cycling suggest that in comparison to the small thermal cycling at low temperatures at the large thermal cycling at high temperatures, plasticity and/or creep is activated, result in significant stresses in Cu which ultimately causes interfacial sliding. Interfacial shear stresses are responsible for the interfacial delamination.

The simplified model was developed to perform fracture analysis. When the model has been heated up to 425˚C the high stress concentration found near the interface between Cu TSV and SiO2 liner, resulted into top-up TSV. In this case ($\Delta T>0$), the interfacial crack developed with a pure shearing mode and mode II fracture was occurred. J-integral approach was used for the linear elastic and elastic-plastic analyses of crack to characterize the growth rate using Paris law. Strain energy release rate was increased by increasing the thickness of the Si die in both the linear elastic & elastic-plastic model for Cu TSV cracking under heating conditions. In case of elastic-plastic model interfacial delamination was occurred. Structural integrity of Si & Cu has been calculated by comparing the stress intensity factor with fracture toughness of Si. This comparison of stress intensity factors of three modes for three different aspect ratios indicates that KI decreases with the increase in thickness of Si whereas KII & KIII increases with the increases in the thickness of Si. The SIFs values obtained were less than the fracture toughness of Si hence it did not fail under the given conditions.

6.2 Future Work

A lot of things could be possible to study in the future. The crack driving forces under reflow process will be investigated. By varying the diameter of Cu TSV and keeping the same aspect ratio, strain energy release rate will be calculated. It would be interesting to see the changes in fracture modes by changing the material properties. The methodology used in simple model would be applied to the global model to understand the effects of fracture to the complete model.

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