Experimental and Simulation Board Level Reliability Assessment of Wafer Level Chip Scale Packages (WCSPs) Under Thermal Cycling

by

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Abstract

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Various studies have been conducted to study the effect of varying board thickness on thermo-mechanical reliability of BGA packages. Wafer level chip scale packages (WLCSP) have also been studied in this regard to determine the effect of PCB build-up thickness on the solder joint reliability. The studies clearly demonstrate that the thinner Printed Circuit Boards (PCBs) result in longer thermo-mechanical fatigue life of solder joints. Due to an extensive research, literature and past trends to support the theory that thinner PCBs perform better than thicker ones, Texas Instruments (TI) opted to move forward by decreasing the thickness of their PCBs by 30% to improve the reliability of their packages. The thickness was reduced by decreasing the thicknesses of individual layers and keeping the total number of layers constant. When subjected to thermal cycling, it was observed that the thinner board was failing earlier than the thicker board. Since this behavior of a WCSP is in contrast to the past trends, it required extensive study to determine and understand the pre-mature physics of failure/causality of failure in the thinner board.

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Chapter 1

Introduction and Motivation

1.1 Role of Packaging in Microelectronics

Microelectronic packaging has evolved by leaps and bounds in the past few decades. As predicted by Moore's Law "The number of transistors will double every 18 months" [1]. As shown in the figure below, the number of transistors per square inch on a chip has increased from 2300 to 2,600M from 1975 to 2011.

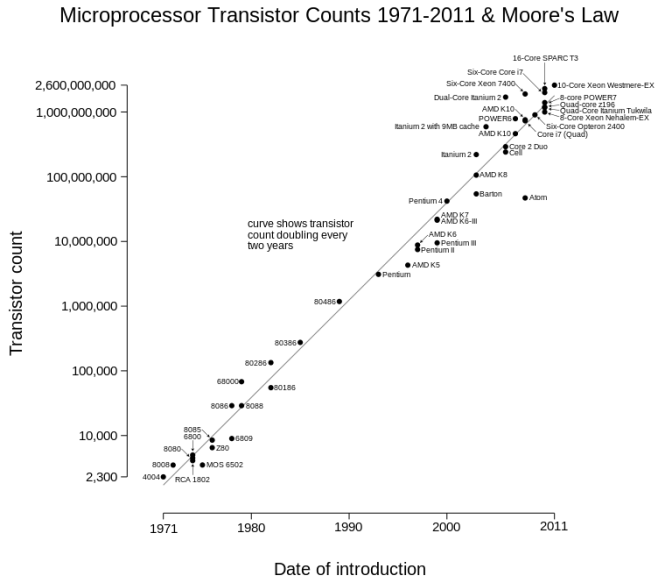

Figure 1-1 Moore's Law

As of 2015, the highest transistor count in a commercially available CPU (in one chip) is over 5.5 billion transistors, in Intel's 18-core Xeon Haswell-EP. This enormous growth in the number of transistors and reduction in package size to meet requirements

of hand held devices signifies the importance of packaging in microelectronics – more than ever before.

Further, packaging plays a vital role in any electronic device from the performance and cost standpoint. It is the whole package and not just the chip that is shipped; packaging significantly contributes to the total cost - equal to or greater than that of the silicon [2].

- Interconnect scaling – nm (chip) to cm (PCB)
- Heat dissipation from the device
- High speed signaling
- Mechanically housing the device – protection from environment

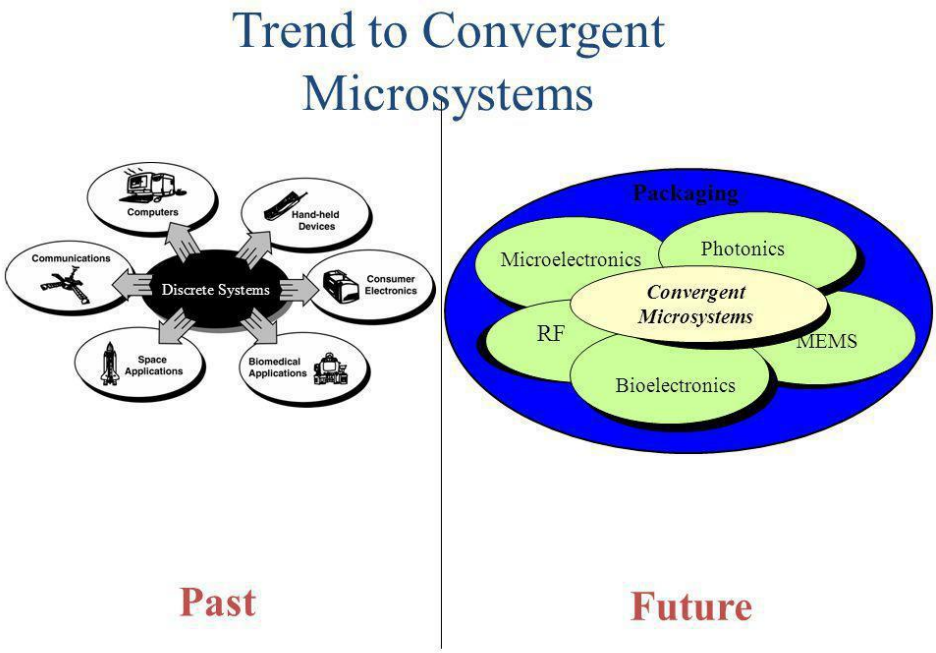

Figure 1-2 Convergent Microsystems

1.2 Wafer Level Chip Scale Package (WLCSP)

Wafer Level Chip Scale Package (WLCSP) refers to the packaging technology of an integrated circuit at the wafer level, instead of the traditional process of assembling individual units in packages after dicing them from a wafer [3]. This process is an extension of the wafer Fab processes, where the device interconnects and protection is accomplished using the traditional fab processes and tools. In the final form, the device is a die with an array pattern of bumps or solders balls attached at an I/O pitch that is compatible with traditional circuit board assembly processes.

1.2.1 Package Description

WLCSP is essentially a true chip-scale packaging (CSP) technology, since the resulting package is of the same size of the die [4](Figure 1-3). WLCSP technology differs from other ball-grid array (BGA) and laminate-based CSPs in that no bond wires or interposer connections are required. The key advantages of the WLCSP is the die to PCB inductance is minimized, reduced package size, and enhanced thermal conduction characteristics [5].

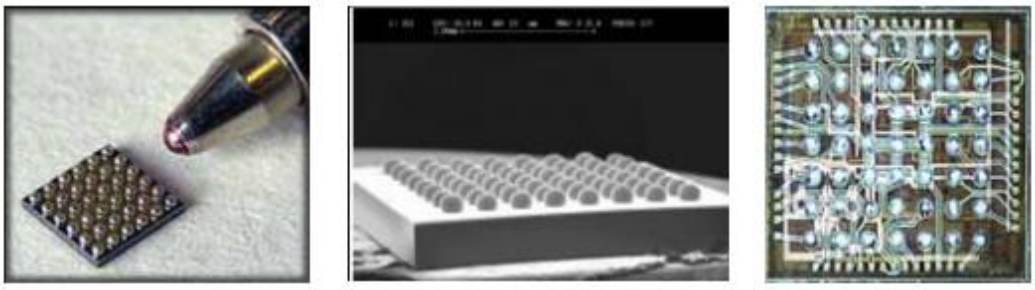

Figure 1-3 Freescale WLCSP

1.2.2 Package Construction

In Wafer Level Chip Scale Packaging, the bare die is processed to have solder balls attached directly to the device, removing the need for external casing and wiring. (Figure 1-4). The silicon die is covered with a nitride passivation layer, except for pad openings. A polymer dielectric is then added, followed by a metallic compound re-distribution trace layer. Another polymer dielectric layer is added, followed by the Under Bump Metallization (UBM) deposition. A solder ball is attached onto each UBM stud. After processing, the device is essentially a die with an array pattern of solder balls, attached at a pitch compatible with traditional circuit board assembly processes. There is no need for external packaging material to protect the chip [6].

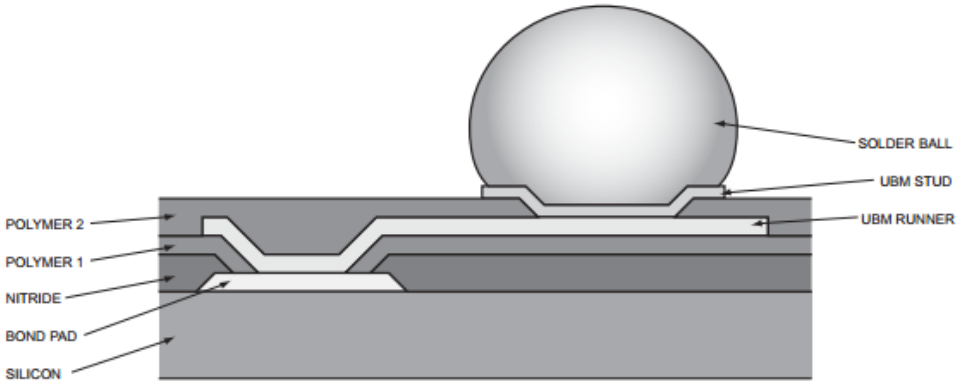

Figure 1-4 - Typical WLCSP Cross-section

1.3 Design for Reliability

1.3.1 Design for Reliability

When a product performs the functions for which it is designed, then that product is said to be reliable. When it does not, it is said to be unreliable. To ensure that the electronic product performs its function effectively for the claimed period of time, two approaches are commonly practiced

- Design the systems packaging up-front for reliability

- Conduct accelerated test on the systems packaging for reliability after the system is designed, fabricated and assembled

Traditional industrial practice involves testing for reliability after the IC after the packages are fabricated and assembled. If problems are found during these tests, packages are redesigned, rebuild and retested for reliability. Since this practice requires huge amount of time and resources, it can be avoided by using the first approach i.e testing the system and fixing its issues upfront in the design process, even before the IC and the system-level packages are fabricated [7]

1.3.2 Board Level Reliability (BLR)

Board level reliability is a very important aspect to ensure the reliability of the package. As the package should withstand the effect of temperature, shock and vibration while performing its due function effectively, it is very important to ensure its reliability by following certain standard protocols. As we are primarily concerned about the behavior of the WCSP package under thermal cycling in this work, we will be looking at the board level reliability of the package under thermal cycling.

There are many indicators used to describe reliability and one of the most widely used is the failure rate. If a plot of failure rate versus time is depicted, a curve in the shape of a bathtub cross-section is obtained as shown in Figure 1-5 . Hence it's widely referred to as a bathtub curve

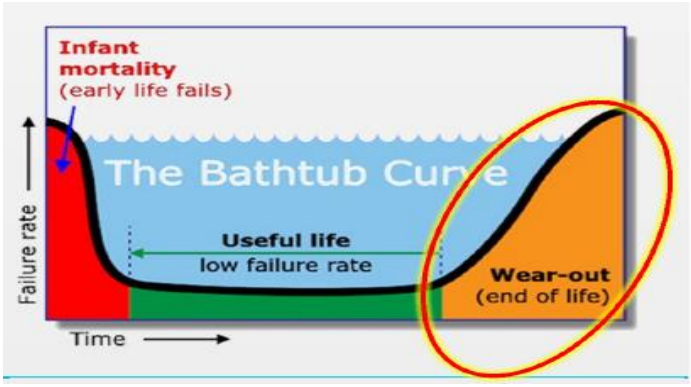

Figure 1-5 Bathtub Curve

Three different phases of failure are seen from the bathtub curve; infant mortality, useful life and failures due to wear-out. The failures during the early life are primarily due to fabrication, process and assembly defects. The failure rate useful life region is almost constant as failed and poorly manufactured parts have already been screened out and removed from the system. The remaining majority of the parts have negligible or no defects at all and therefore reach their warranted life in most of the cases with some random failures in between. Eventually, as the product has performed its function for a designated period of time, mechanical, electrical and environmental effects start causing failures in at a higher rate. This is called the wear-out region where thermal & mechanical stresses cause permanent failure in the product.

To estimate the reliability of the package, environmental stress test are used to simulate the end use environment conditions and to uncover specific materials and process related marginalities that may be experienced during operational life. Few consortiums such as Joint Electronic Device Engineering Council (JEDEC) and Institute for Printed Circuits (IPC) have adapted, documented and standardized many of the reliability tests. Since the scope of this work is only during thermal cycling, we'll briefly discuss about it.

1.3.3 Thermal Cycling (TC) Test

Thermal cycling induces thermo-mechanical stresses caused by difference of thermal expansion between the printed circuit board (PCB) and the device package interconnects. The embrittlement effect of solder joints – comprised of compounding dislocation that leads to crack initiation and growth [8] . Due to difference in coefficient of thermal expansion between various package components, they warp and expand unevenly resulting in generation of internal thermal stresses which results in crack propagation in dielectric, fatigue and adhesion problems. These thermo-mechanical

behaviors can be detected during thermal cycling tests. For reliability assessment, Weibull distribution is most commonly used to accurately reflect the behavior of the product in terms of failure rate [9].

1.4 Motivation & Objective

The wafer-level package (WLP) is a type of chip-scale package (CSP), which enables the IC to be attached face down to the printed circuit board (PCB) using conventional SMT assembly methods. The chip's pads connect directly to the PCB pads through individual solder balls (Figure 1-6). WLP technology differs from other ball grid array, leaded, and laminate-based CSPs because no bond wires or interposer connections are required. In general, underfill material is not required for WLP. However, in certain applications such as mobile devices, underfill can enhance WLP mechanical robustness. The main advantages of the WLP are a small package size, a minimized IC-to-PCB inductance, and a shortened manufacturing cycle time [10]

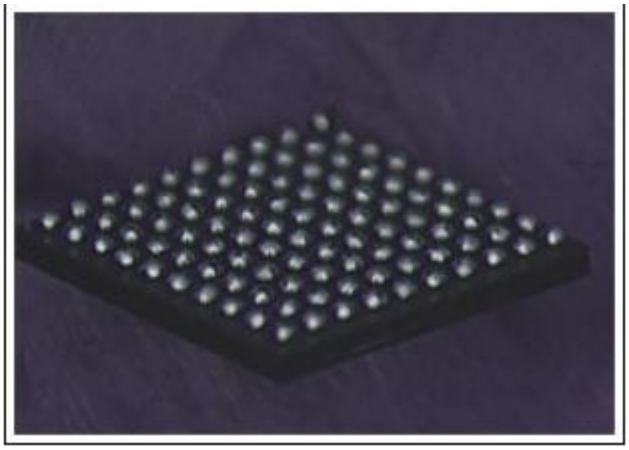

Figure 1-6 10 x 10 WLP with circuit side view

1.4.1 Motivation

As we know from literature as the thickness of Printed Circuit Board (PCB) increases it becomes more stiff and as a result it transfers more stresses to the solder balls. This results in crack generation and propagation which eventually causes a failure in the solder joint (Figure 1-7).

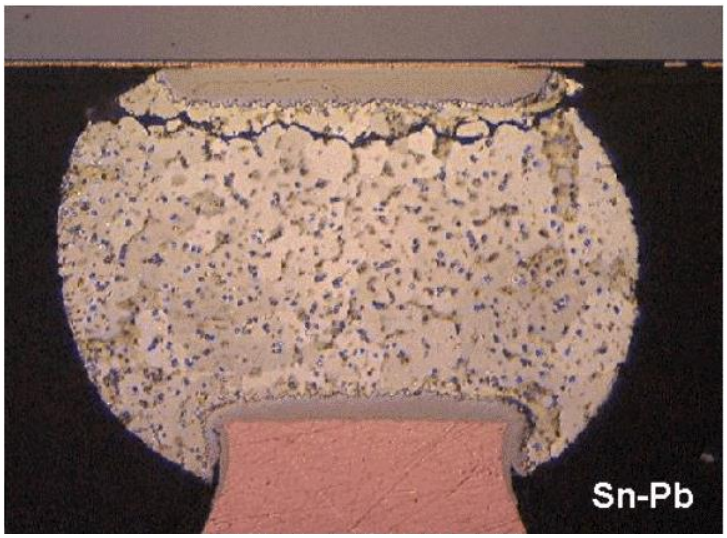

Figure 1-7 Solder Joint Crack

Texas Instruments reduced the thickness of their boards from 1mm to 0.7mm based on available literature and past trends, and expected that the reliability of the boards will increase as the boards will become more compliant after reducing their thickness. Surprisingly, the results showed a contrast to the previous trends and available literature. Upon subjecting the boards to thermal cycling, the 0.7mm boards failed much earlier as compared to the 1mm board. Since this behavior was not in line with the past trends, there was a scope to look deeper into the problem and come up with a reasonable justification for this behavior.

1.4.2 Objective

The primary objective of this work is to find the root cause of the failure and come up with best practices about how Texas Instruments can improve the reliability of their boards under thermal cycling based on Finite Element Analysis (FEA) prediction. Samples of PCBs were provided by TI for experimental and FEA purposes. In this work, FEA models were developed based on the dimensions provided by TI using commercially available ANSYS 15.0. The samples of PCBS were tested for different material properties such as Young's Modulus using Instron Micro tester, In-plane & out of plane coefficient of thermal expansion (CTE) using Thermo Mechanical Analysis (TMA), PCB cross sectioning and layer by layer analysis, storage modulus using Dynamic Mechanical Analysis (DMA), using Optical Microscope & board warpage using Digital Image Correlation (DIC) technique with oven. These material properties were incorporated in the FEA models to examine the FEA behavior of the boards.

FEA models are used to determine the fatigue correlation parameters such as strain energy density and plastic strain range. These parameters are a measure of the energy dissipated through plastic and creep deformation which is related to the damage done to the solder joint. Using these parameters, different life prediction models were used to calculate life cycles to failure. Further, reasons for low board reliability in a 0.7mm board as compared to its 1mm counterpart have been discussed in detail and design improvements have been suggested to improve the reliability of the thinner board.

Chapter 2

Literature Review

A lot of work has been done on the reliability of Wafer Level Chip Scale Packages. Fatigue and damage of solder joints that are caused due to thermal cycling and power cycling have been a subject of interest for the researchers. Albrecht *et. al* [11] studied the effect of applied interposer, the influence of package level interfaces, geometry, package constitution, ball array on the board level reliability of Chip Scale Packages.

Lau *et. al* [12] studied the thermal-fatigue life of the corner solder joint of the WLCSP assembly by a time-temperature dependent creep analysis and the empirical equation given by Darveaux. A non-linear time-temperature dependent finite element analyses were performed to determine the shear stress, shear creep strain, shear stress and shear creep strain hysteresis loops, and creep strain energy density of the corner solder joint. It was found that the thermal-fatigue life of the corner solder joint of the WLCSP is more than 2000 cycles (60 minutes cycle between -20°C and 110°C with 15 minutes ramp, 20 minutes hold at hot, and 10 minutes hold at cold)

Lau *et. al* [13] performed creep analysis of a Wafer Level Chip Scale Package (WLCSP) on Printed Circuit Board (PCB) build-up under thermal cycling. The studied the effect of PCB build-up layer on the solder join t reliability of a WLCSP. The compared the effect of deformation of the PCB with and without a build-up layer. It was found that the PCB without build-up layers deforms 65% more than the board with buildup layers. This is due to the following reasons

- The global mismatch of thermal expansion between the silicon chip and the build-up PCB which forces the whole assembly to deform into a concave shape

- the local mismatch of thermal expansion between the build- up resin and the FR-4 PCB which forces the build-up PCB to deform into a convex shape (just opposite to the global deformation)

Due to this reason the board with build-up layers was bending 65% less as the other one because its bending due to local mismatch was neutralized by the bending due to global mismatch in the opposite direction.

Further, three different thicknesses of PCBs were tested for their deformations under thermal cycling. The thicknesses used were 0.5mm, 1mm and 1.5mm. The conclusions drawn from the results of the tests are given below

- The thinner the PCB, the smaller the creep shear strain range
- The creep shear strain range at the center of the corner solder joint is the smallest and at the upper-right corner of the corner solder joint is the largest due to strain concentration
- The strain energy density range at the center of the corner solder joint is the smallest and at the upper-right corner of the corner solder joint is the largest due to stress and strain concentrations

In order to conclude the study of Lau *et. al* we can safely say that with the presence of microvia build-up layer, the thinner PCB results in smaller shear stress range, creep shear strain range, and creep strain energy density range in the solder joints under the thermal loading. Hence, the thinner build-up board should lead to longer thermal fatigue life of solder joints.

Although there are a number of factors that affect CSP assembly yield and solder joint reliability, Primavera *et. al* [14] studied a few of them that standout as being the most critical; board thickness, component device construction and attachment pad size. From his study, Primavera *et. al* concluded that as the board thickness and overall stiffness

decreases, the resulting stress the solder joint experiences decreases. It was predicted that 2X increase in fatigue life can be realized by assembling a CSP on a thin board.

Since the main cause of board warpage is Coefficient of Thermal Expansion (CTE) mismatch between the chip and the board, Fan *et. al* [15] studied the effect of CTE mismatch between chip and board and how it effects the fatigue life of solder joints. It was concluded that lowering the CTE of PCB can also reduce the stresses in solder joints. Three different CTEs were assigned to the PCB and Inelastic Strain Energy Density was calculated. It was found that as the CTE decreased the strain energy also decreased which means that higher CTE accounts for lower fatigue life of solder joints.

From the above literature it can be concluded that solder joint fatigue life is highly affected by the thickness of the PCB and its material properties. As the thickness of PCB decreases, it consequently decreases its stiffness and becomes more compliant. Due to this compliance, it undergoes large deformation when subjected to thermal cycling but the stresses generated at the far corner region of the solder joint are less as compared to the case where a stiffer board is subjected to thermal cycle and generates more stresses at the solder joint. These high stresses eventually result in the reduction of solder joint fatigue life. In this work, the behavior of WCSP is studied in detail and the reason for premature failure in the thinner board is presented.

Chapter 3

Material Characterization

Since it is necessary to have all the required material properties to accurately model a package in ANSYS workbench and predict board level reliability of that package based on FEA results, it was imperative to have all the required material properties of the WCSP provided by Texas Instruments. The material properties required to model a package in ANSYS workbench are given below

- Coefficient of Thermal Expansion (CTE)
- Young's Modulus (E)
- Shear Modulus (G)
- Poisson Ratio (υ)

To determine these properties the equipment and techniques used are given below

- Sun Microsystems Oven with DIC
- Instron Microtester with 2kN Load Cell
- Thermo-mechancial Analysis
- Dynamic Mechanical Analysis

Sample preparation and test procedures for all the tests conducted for material characterization will be explained in this section. .

3.1 Coefficient of Thermal Expansion (CTE)

Coefficient of Thermal Expansion (CTE) is defined as the tendency of a material which defines the amount by which it expands or contracts when heated or cooled

$$\alpha = \frac{\epsilon}{\Delta T}$$

Where,

α – Coefficient of Thermal Expansion (CTE) ppm/°C

ϵ - Strain (mm/mm)

ΔT – Difference in Temperature (°C)

Since we will be thermal cycling the package from -40°C to 125°C in the oven, it was necessary to know the CTE of the package so the FEA model of the package would complement the actual condition as closely as possible.

3.1.1 Heating/Cooling Oven

The oven used for heating the package was a Sun Microsystems Oven with a door for easy access to place and remove packages in the oven. The oven has a 12”x4” borosilicate glass at the top wall for the cameras to view the package clearly. The purpose of using a borosilicate glass is to avoid any reflection caused due to illumination from glass surface into the camera eye. There are two openings on each side wall of the oven which are covered by rubber corks. Thermocouple wires are connected to the sample through these openings which are closed with the rubber corks after the wires have been carefully passed through them.

Figure 3-1 Heating Oven

3.1.2 Digital Image Correlation Technique – CTE Measurement

Digital Image Correlation (DIC) is a non-contact technique to measure in-plane and out of plane deformations and strains. A pair of 5MP cameras was used to capture the images. The cameras were positioned at an angle of 15~20deg from the vertical to have a view of package's in-plane as well as out of plane deformations. The cameras were connected to a software VICSnap to view the image clearly on the screen and select area to be analyzed.

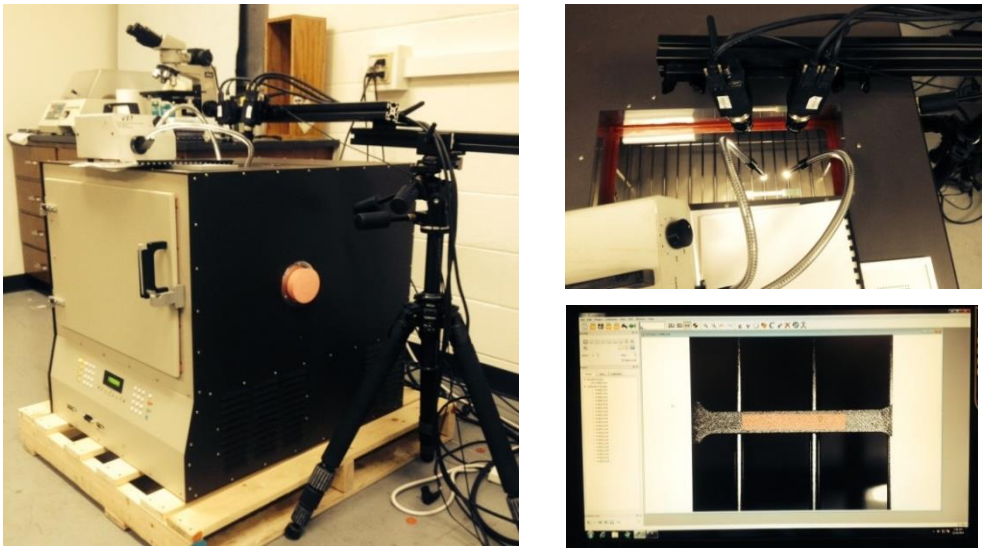

Figure 3-2 DIC Setup

3.1.2.1 *DIC Calibration*

It is of utmost importance that before using DIC, the cameras have been calibrated properly so they can measure the smallest deformation correctly. To calibrate the DIC, a calibrating panel with white base and black dots was used. The pitch between the dots was 4mm and the total number of dots was 108. First the sample is focused so that the image on the software is clearly visible and sharp, then the calibrating panel is kept at the same height as of the sample and images are taken by the software at different angles of the calibrating panel. The panel is tilted in all directions to get a good

focus of the DIC cameras from all directions and angles. The software is then used to analyze the images of the panel and once the software is able to view the dots on calibrating panel clearly, the DIC is ready for testing.

3.1.2.2 Sample Preparation

Since the DIC works on the principal of tracing movements of small dots during heating or cooling, it is very important to prepare the testing sample in such a way that it has clearly visible dots on its surface. To achieve this, samples of 15mmx51mm were cut out from PCB and painted using matt enamel paint. First, a layer of white paint is applied on the sample and left to dry. Once it has dried, black paint is sprinkled on the white layer carefully in such a way that the surface neither gets very large blots nor very few dots. There should be enough dots on the surface for the DIC to trace their movement during expansion. This sample is then kept inside the oven and thermocouples are then connected to it at 3 different locations to measure temperature during the test and avoid any temperature difference within the sample due to thermal mass.

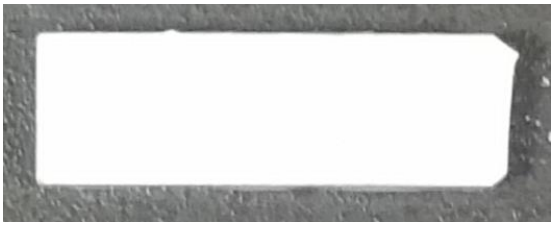

Figure 3-3 White Base

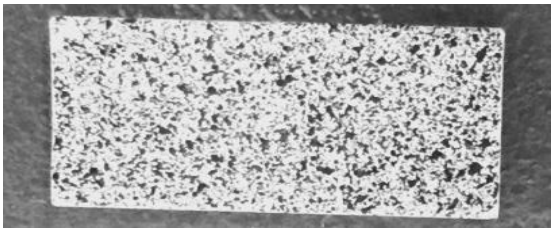

Figure 3-4 Black Speckles

3.1.2.3 CTE Results

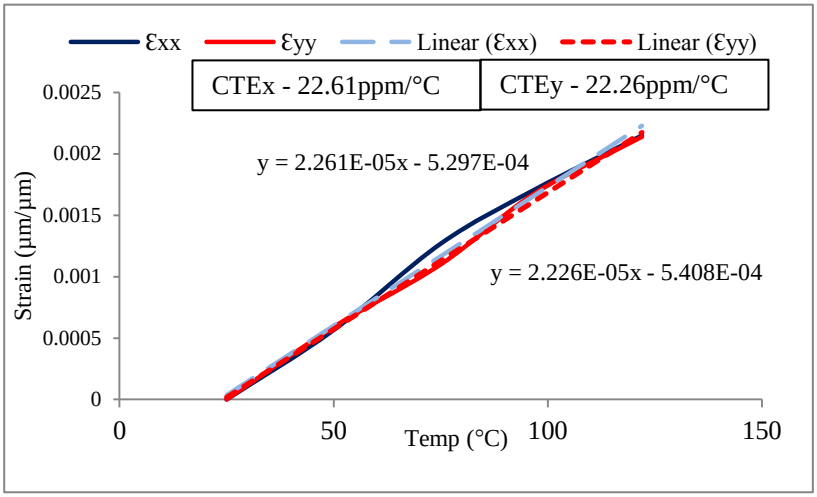

Figure 3-5 Thin Board CTE

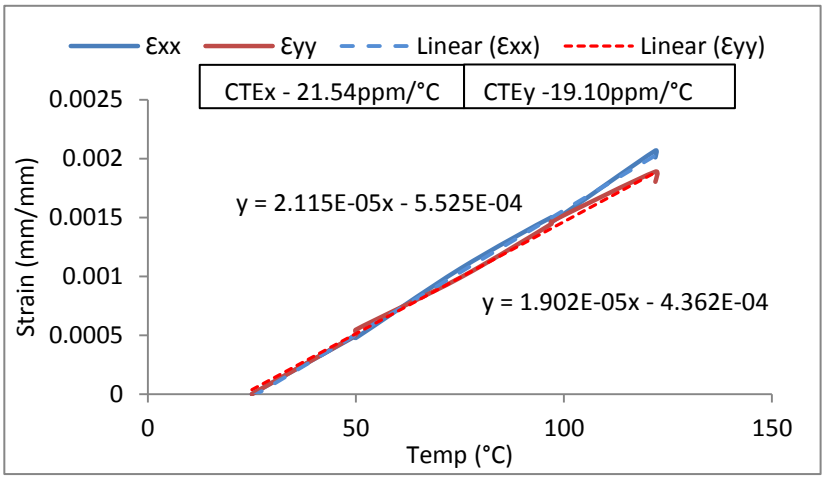

Figure 3-6 Thick Board CTE

3.2 Young's Modulus Measurement

Young's Modulus or Elastic Modulus defines the stiffness of compliance of a material when subjected to tensile or compressive loading. Materials that deform by a small amount when tensile load is applied to them are said to be stiffer as compared to the materials that deform by a considerable amount when tensile or compressive loading is applied to them. Mathematically, Young's Modulus is defined by the stress produced in a material when some strain is applied to it.

$$E = \frac{\sigma}{\epsilon}$$

Where,

E – Young's Modulus (MPa)

σ – Stress (MPa)

ϵ - Strain (mm/mm)

3.2.1 Instron Microtester – Young's Modulus Testing

To conduct Young's Modulus tests, an Instron Microtester of 2kN load cell was used to apply tensile loading to the samples. An extensometer is placed on the sample to measure strain during sample extension. The extensometer is connected to a software to while the instron is also connected and it gives in-situ force-displacement graph during the test. Stress is calculated by dividing the stress from the cross-sectional area of the sample and strain is measured using the extensometer. From the stress and strain, Young's Modulus is calculated for a sample.

3.2.1.1 Sample Preparation

ASTM standard was followed to prepare dog bone samples for Instron test. The reason for preparing dog bone samples is to make sure there is enough grip section available for the instron grips to hold the sample tightly during the test. The final shape of the sample is shown in the fig below

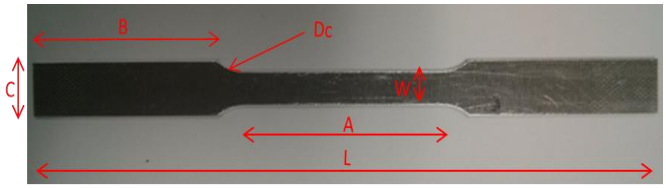

Figure 3-7 Dogbone Sample

The dimensions of the sample as referred from the ASTM standards is given below

Table 3-1 Dogbone Sample Dimensions

Dimensions	Value (mm)
L - Overall Length	100
C – Width of grip section	10
W – Width	6
A – Length of Reduced Section	32
B – Length of Grip Section	30
Dc – Curvature Distance	4
R – Radius of Curvature	6

3.2.1.2 Experimental Setup

To measure the Young's modulus of PCB samples, Instron MicroTester 5848 with a max. load cell of 2kN was used to apply force. The grip section of dog bone sample is clamped vertically between the two jaw faces of the instron tester and an extensometer is placed on the samples with its pins gripping the sample tightly. The extensometer pins have an initial gap of 12mm between them. When tensile force is applied on the specimen, the extensometer pins which are tightly gripping the specimen

open accordingly and the change in length is measured from where strain is calculated using Instron software.

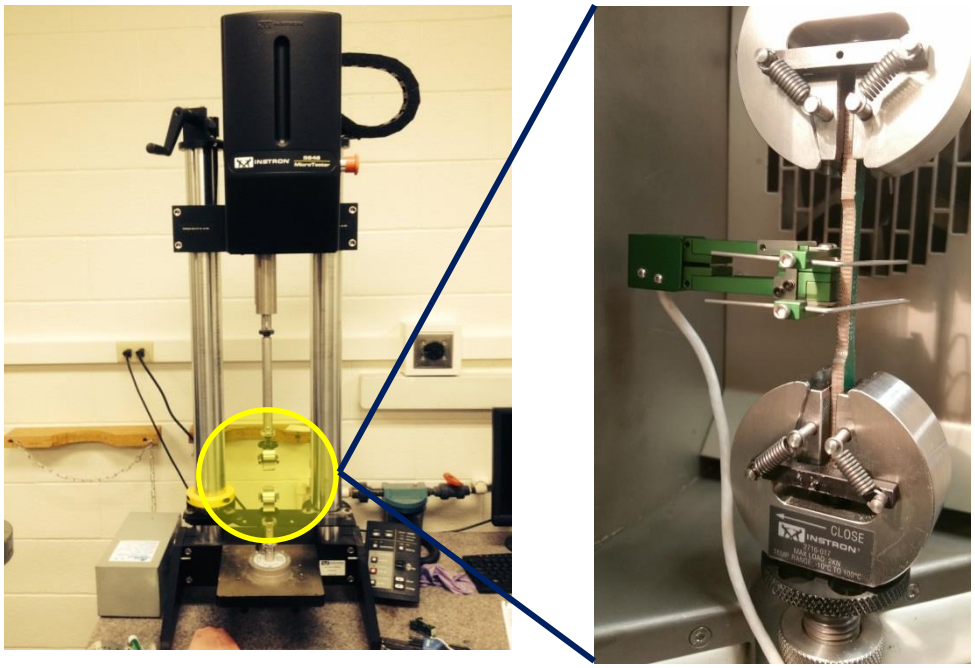

Figure 3-8 Instron Setup

The test setup and procedure as shown in fig 4 was benchmarked by testing an aluminum sample and calculating the Young's Modulus. The experimental result was compared with the theoretical result and was found to be in complete agreement with the theoretical value.

3.2.1.3 Instron Results

The Young's modulus values as measured by the Instron tester for 0.7 and 1mm boards are shown in the fig below

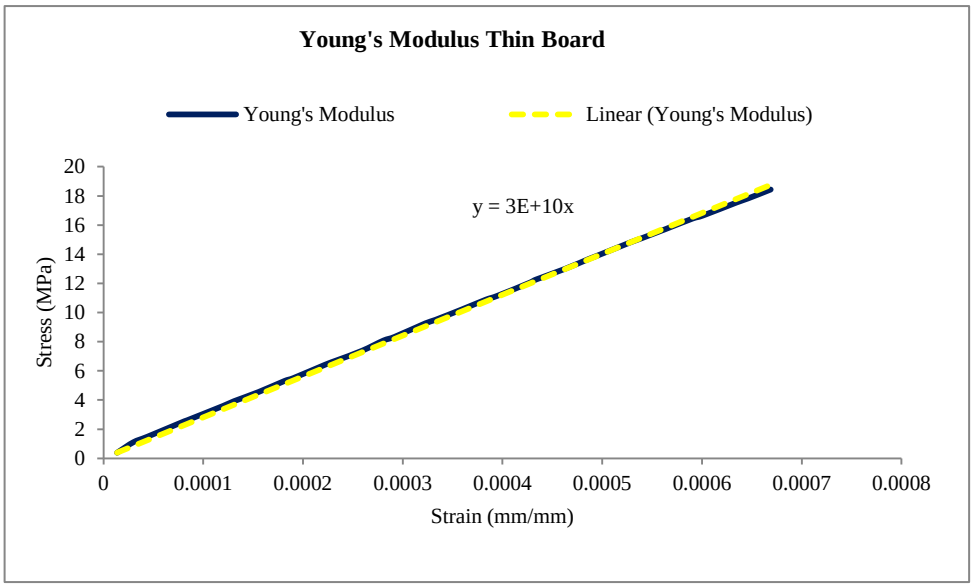

Figure 3-9 Thin Board Young's Modulus

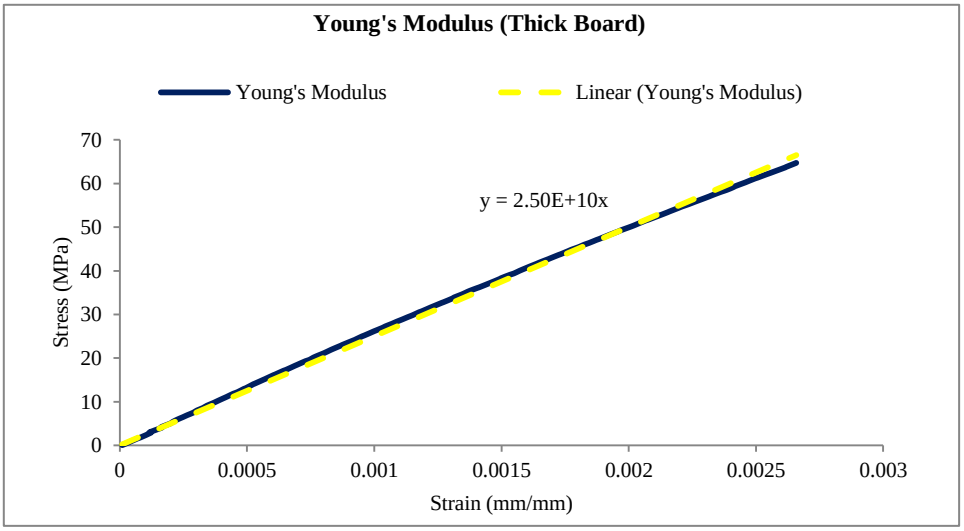

Figure 3-10 Thick Board Young's Modulus

3.3 Storage and Loss Moduli Measurement

The storage and loss modulus in viscoelastic materials measure the stored energy, representing the elastic portion, and the energy dissipated as heat, representing the viscous portion [16]. The tensile storage and loss moduli are defined as follows

$$\text{Storage: } E' = \frac{\sigma}{\epsilon} cos\delta$$

$$\text{Loss: } E'' = \frac{\sigma}{\epsilon} sin\delta$$

3.3.1 Sample Preparation and Fixture

Rectangular samples of 40mm x 3mm were used for the test. Samples were mounted in a dual cantilever beam fixture as shown below

Figure 3-11 Bending Fixture for DMA

3.3.1.1 DMA Results

The results of both the thin and thick boards for storage and loss moduli are given below

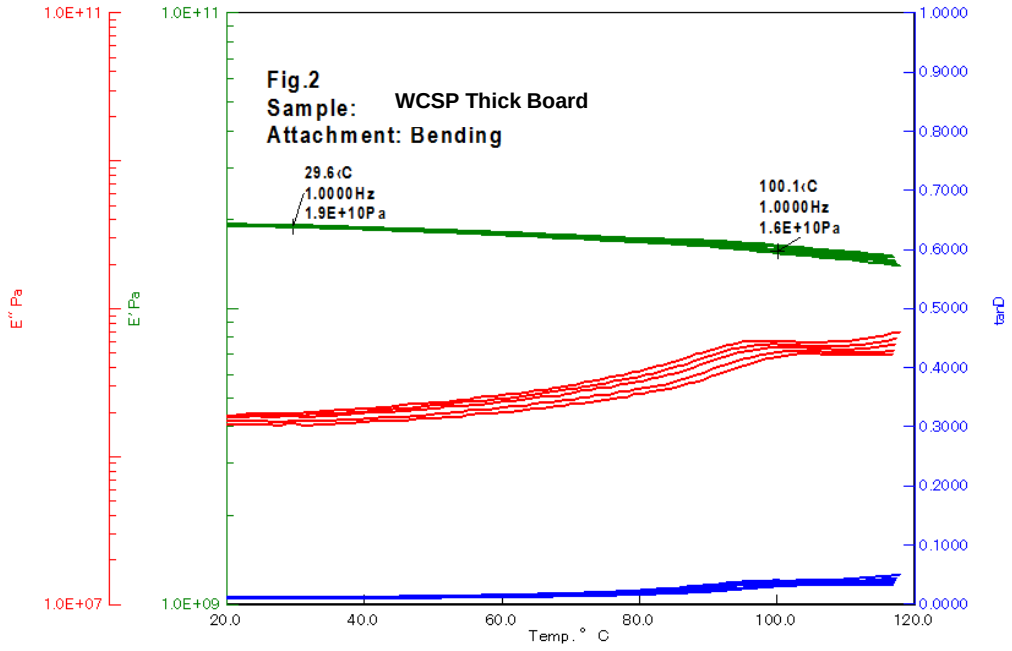

Figure 3-12 Thick Board Storage & Loss Moduli

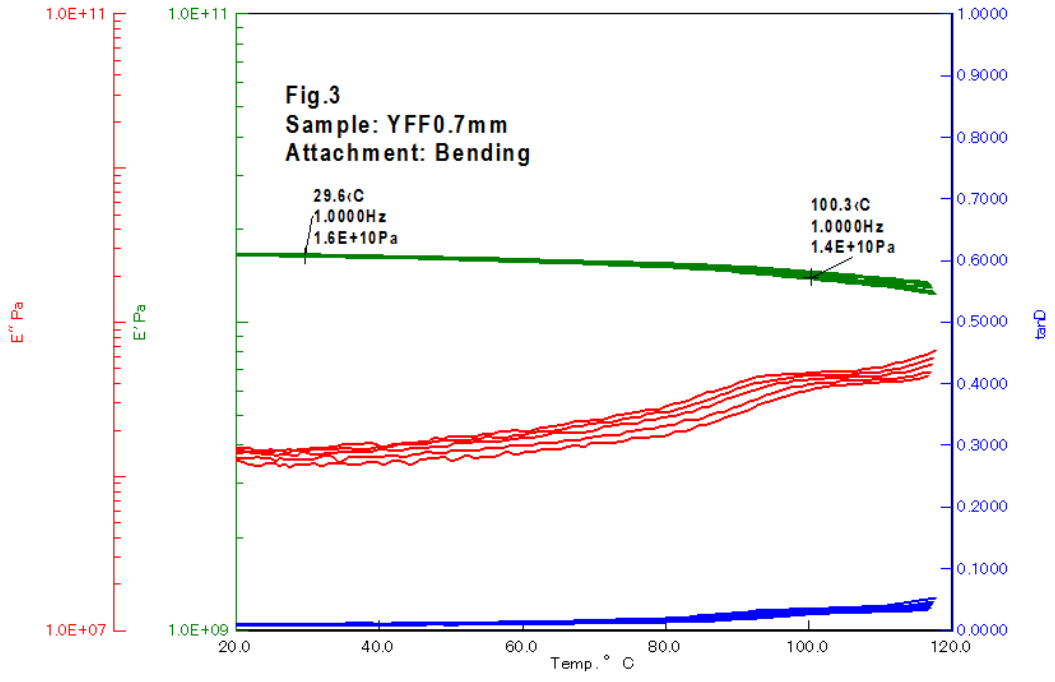

Figure 3-13 Thin Board Storage & Loss Moduli

Chapter 4

Modeling & Simulation

In order to be able to predict board level reliability of the package, an FEA model was developed using commercially available ANSYS workbench 15.0. The dimensions of the package were provided by Texas Instruments and the model was developed based on those dimensions. Since the WCSPs is known to be of a small size, the largest dimension of the package was smaller than 4mm with an array of 7x7 solder balls. The schematic of the package cross-section is shown below

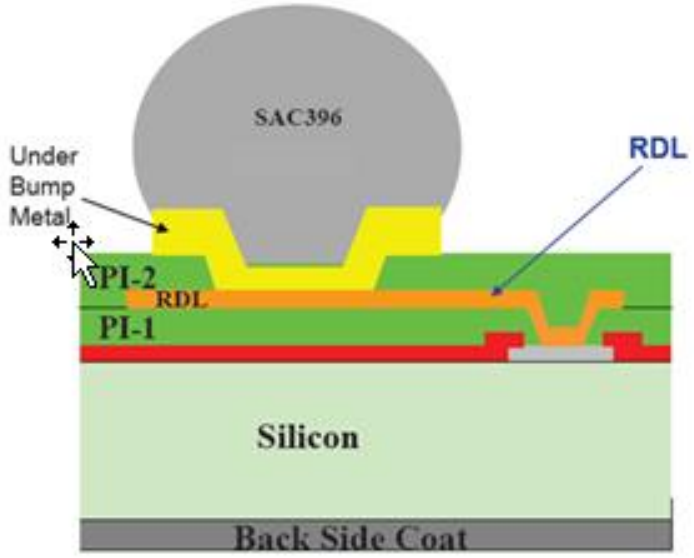

Figure 4-1 WCSP Board Layup

As shown above, the solder used in this package is a lead free solder SAC396. The Under Bump Metal (UBM), Polyamide (PI) 1 & 2 and Copper Redistribution Layer (RDL) were modeled individually to capture their effect on board's warpage. The material properties for these layers were extracted from available literature [17, 18, 19]. These

properties combined with the material properties collected by material characterization have been summarized in the table below

Table 4-1 Model Material Properties

Material	Property				
	E (GPa)	CTE (ppm/°C)	ν		
			xy	yz	xz
PCB (Thin Board)	30	23	0.11	0.39	0.39
PCB (Thick Board)	25	20	0.11	0.39	0.39
Die	131	3	0.28		
RDL	130	16.8	0.34		
Polyamide	1.2	52	0.25		
Mold	24	20	0.3		
Cu	110	17	0.34		
Solder Mask	4	30	0.4		

4.1 FEA Model

Commercially available ANSYS workbench 15.0 was used to model both the packages. Package dimensions, solder ball size and array were provided by Texas Instruments. Both the boards were cross-sectioned and viewed in a digital microscope using a 20X lens to get the detailed layup of the board and the package.

Although the cross-section revealed details of every layer in the PCB as well as 1st level, the PCB was modeled as a block to reduce computational time and use bulk material properties as determined by experiments.

However, the RDL and Polyamide layers were modeled individually and the material properties were assigned from the literature. Quarter symmetry of the full model was used for faster computation. The dimensions used for this model are given below

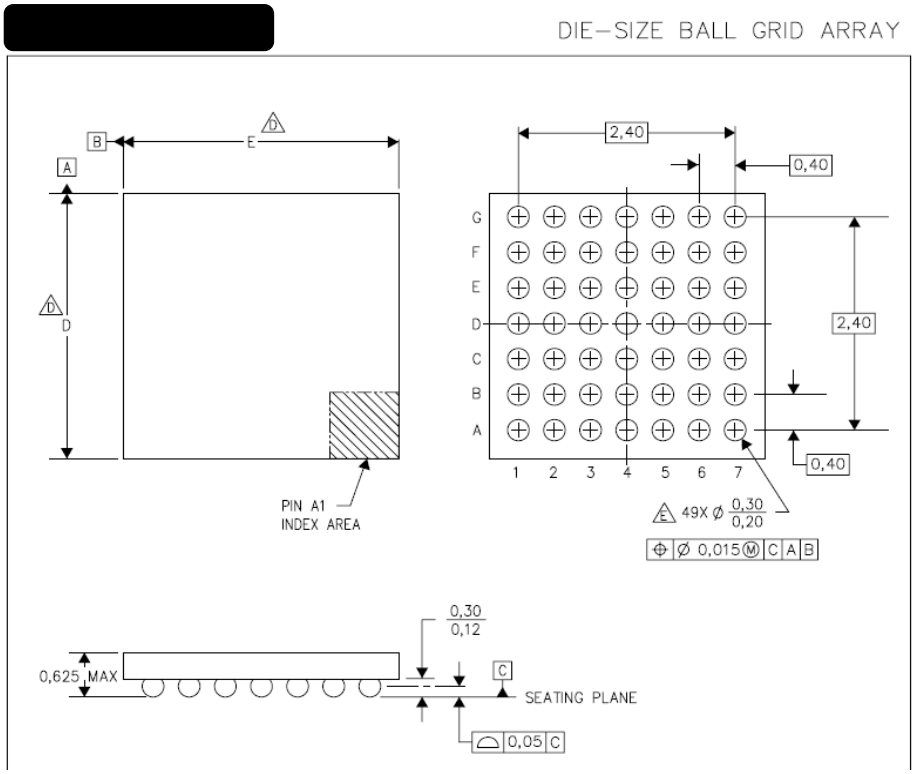

Figure 4-2 Model Dimensions

4.2 Material Properties

All materials except SAC396 and PCB were modeled linear elastic. PCB was modeled linear orthotropic and SAC alloy was modeled viscoplastic using Anand's viscoplastic model for SAC396 [20]. The elastic part of the constitutive law of lead-free solder 396 can be described by a temperature-dependent Young's modulus and Poisson's ratio (v=0.40). The temperature-dependent Young's modulus is

E=100501−194*T*(MPa) in which the absolute temperature *T* is in Kelvin. The coefficient of thermal expansion of the solder is taken to be 23.5 ppm/K

4.2.1 Anand's Viscoplastic Model

Solder is modeled as rate-dependent viscoplastic material using Anand's viscoplastic model, which takes into consideration both creep and plastic deformations to represent the secondary creep of solder. Anand's viscoplastic constitutive law has been used to describe inelastic behavior of lead-free solder. Anand's law accounts for solder's strain-rate and temperature sensitivity through its nine material constants A, Q, ξ, m, n, h_0, a, s_0, ŝ

Anand's viscoplasticity for solder can be described as follows

$$\frac{d\varepsilon_p}{dt} = A \sinh\left(\xi \frac{\sigma}{s}\right)^{\frac{1}{m}} \exp\left(-\frac{Q}{kT}\right)$$

With the rate of deformation resistance equation

$$\dot{s} = \left[h_0(|B|)^{\alpha} \frac{B}{|B|}\right] \frac{d\varepsilon_p}{dt}$$

where,

$$B = 1 - \frac{s}{s^*}$$

and

$$s^* = \hat{s}\left[\frac{1}{A}\frac{d\varepsilon_p}{dt} exp\left(-\frac{Q}{kT}\right)\right]^n$$

There are nine material constants in Anand's viscoplasticity law which are given in table below for SAC396

Table 4-2 Anand's Constants for SAC396

S. No	Constant	Unit	Value
1	s_0	MPa	3.3
2	Q/R	1/K	9883
3	A	sec^{-1}	15.7E+06
4	ξ	Dimensionless	1.06
5	m	Dimensionless	0.3686
6	h_0	MPa	1077
7	$\hat{s}$	MPa	3.15
8	n	Dimensionless	0.0352
9	a	Dimensionless	1.6832

4.2.2 Loading & Boundary Conditions

Since the boards were originally tested by TI when subjected to thermal cycling, therefore to replicate the original loading conditions thermal cycling loading was applied from -40°C to 125°C. All bodies were considered to be stress free at 125°C. Symmetric boundary conditions were applied to two symmetric faces with the center node fixed (all DOF zero) to avoid rigid body motion. A total of three cycles with a complete cycle of 60min with 15min ramp and 15mil dwell were applied as shown in fig below

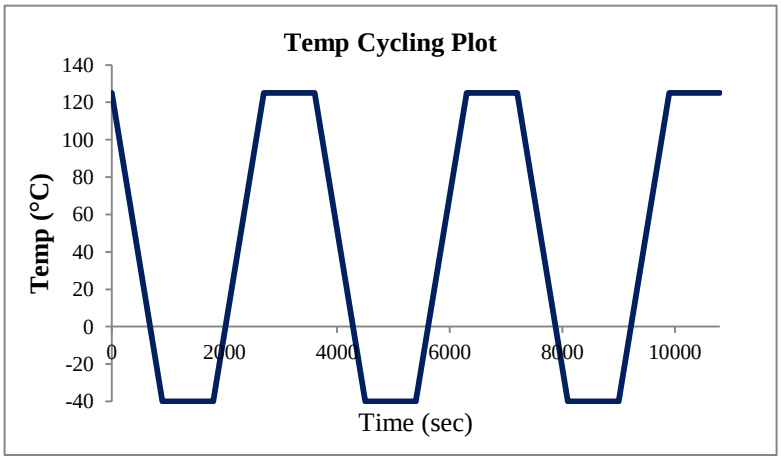

Figure 4-3 Temp Cycling Plot

4.2.3 Meshing and Simulation

The model was meshed using hex dominant method (All Quad) for the solder balls of while the far corner solder was giving body sizing of 20µm in addition to the hex dominant method. The rest of the layers were divided in at least three number of divisions for better results. The fully meshed quarter model is shown in the fig below

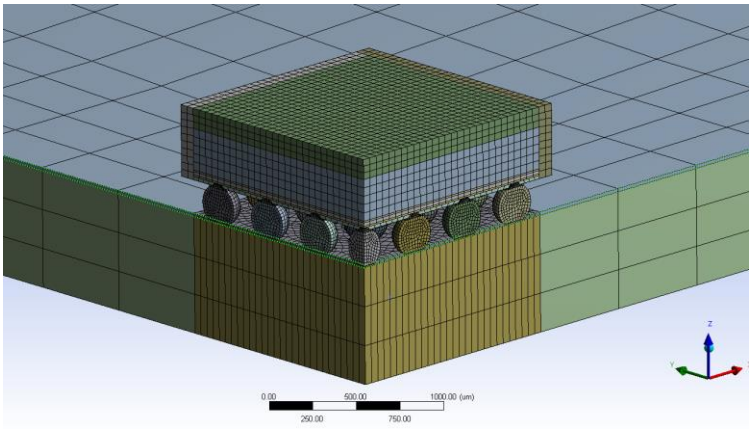

Figure 4-4 Fully Meshed Quarter Model

Since the full model is a 7x7 array, a quarter symmetry has three full and one half ball visible as shown below

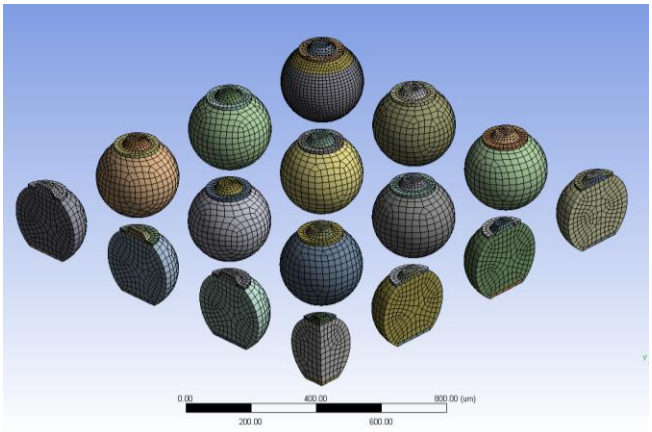

Figure 4-5 Meshed Solder Balls

Since the critical solder ball is the far corner ball, it not only has a refined mesh, a 25μm layer is also modeled in that solder to calculate the volume averaged plastic work in that ball to eventually calculate the life cycles to failure.

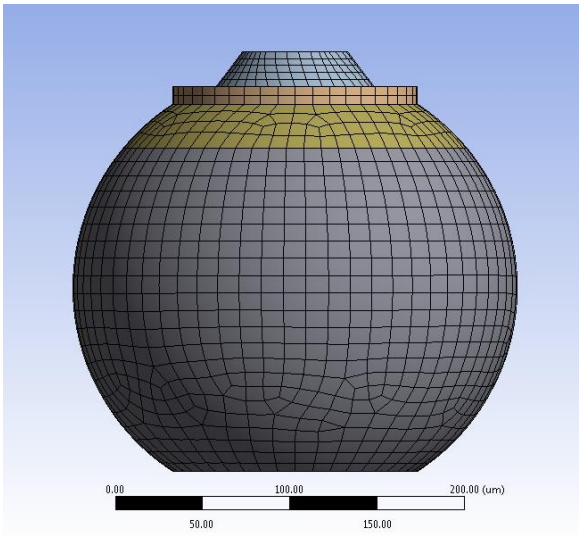

Figure 4-6 Far Corner Solder with 1mil layer

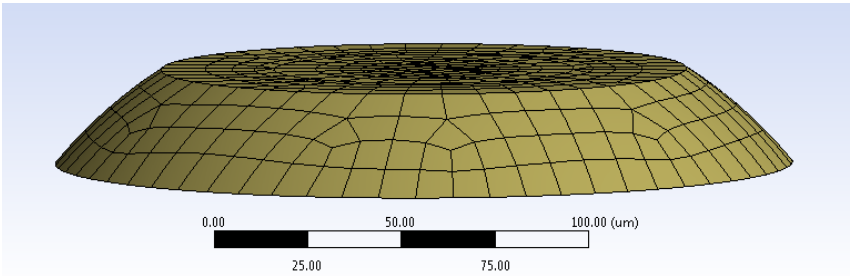

Figure 4-7 1mil layer in corner solder

Volume averaging technique for the 25 micron layer is used to avoid stress singularity at the solder and under metal bump interconnect. By volume averaging, the average viscoplastic strain energy density (SED) accumulated per thermal cycle is

calculated by normalizing the viscoplastic strain energy density per thermal cycle of each element by the total volume of all the elements. To get stabilized results, the average viscoplastic SED calculated in second cycle is subtracted from the third cycle.

$$\Delta Wave = \frac{\Sigma \Delta W.V}{\Sigma V}$$

$$\Delta W = (\Delta Wave)3rd - (\Delta Wave)2nd$$

Chapter 5

Results

Since the far corner solder joint is the most critical solder, the results reported here are for that solder ball. The correlation parameters used to determine the maximum Plastic Work are Total Equivalent Strain and Maximum Von Mises Stress.

5.1 Thin Board Results

5.1.1 Total Equivalent Strain

Since solder demonstrates viscoplastic behavior, it was imperative to report the total equivalent strain in the corner solder to capture the effect of both elastic and plastic deformations. The total equivalent strain in the thin board was found to be 20% micro strain in the far corner solder ball as shown in the figures below

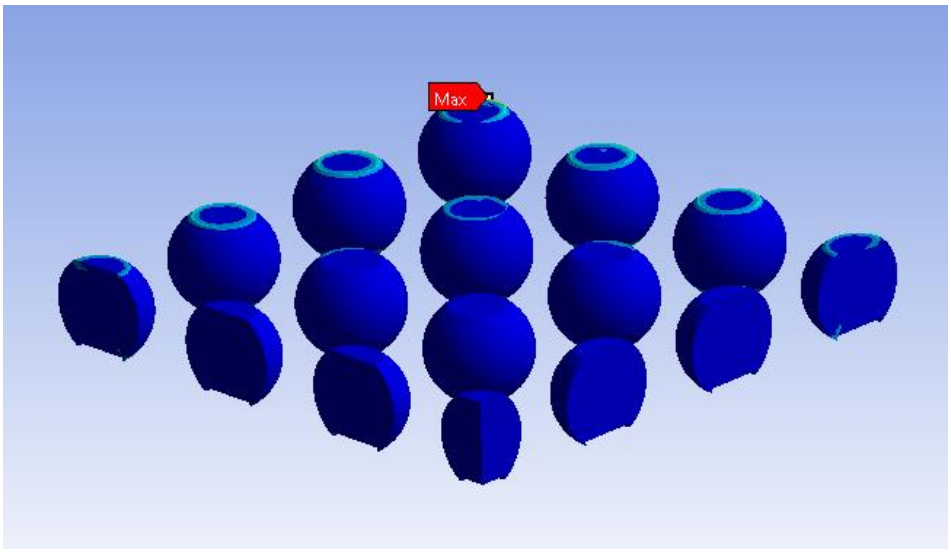

Figure 5-1 Solder Balls Strain Plot

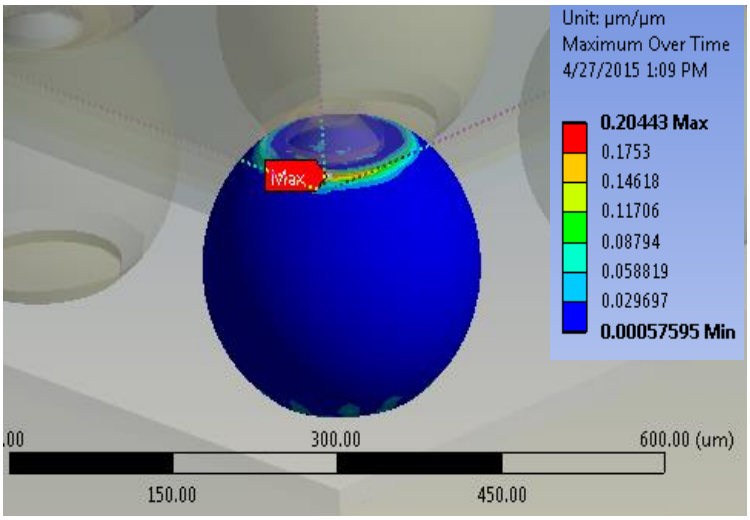

Figure 5-2 Equivalent Strain in Thin Board's Solder

5.1.2 Maximum Von Mises Stress

The maximum Von Mises Stress of 31MPa was also found at the similar location as maximum strain as shown below

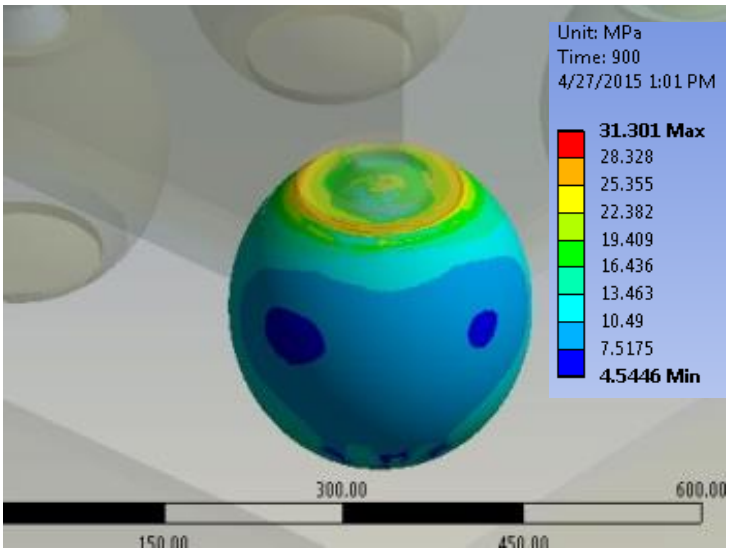

Figure 5-3 Max Stress in Thin Board's Solder

The FEA results were compared from available experimental results from Texas Instruments. There was a perfect qualitative match between the two results. The experimental result for the thinner board is shown below

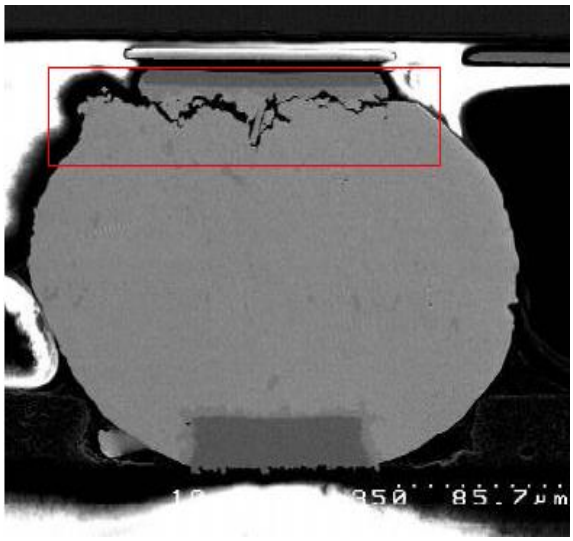

Figure 5-4 Experimentally Cracked Solder Joint

5.2 Thick Board Results

5.2.1 Total Equivalent Strain

The total equivalent strain in the thick board was found to be 14% micro strain. The reason for higher strain in the thicker board is due to the fact that although it's thicker but is less stiffer than the thinner board and consequently results in higher strain as shown in the figure below

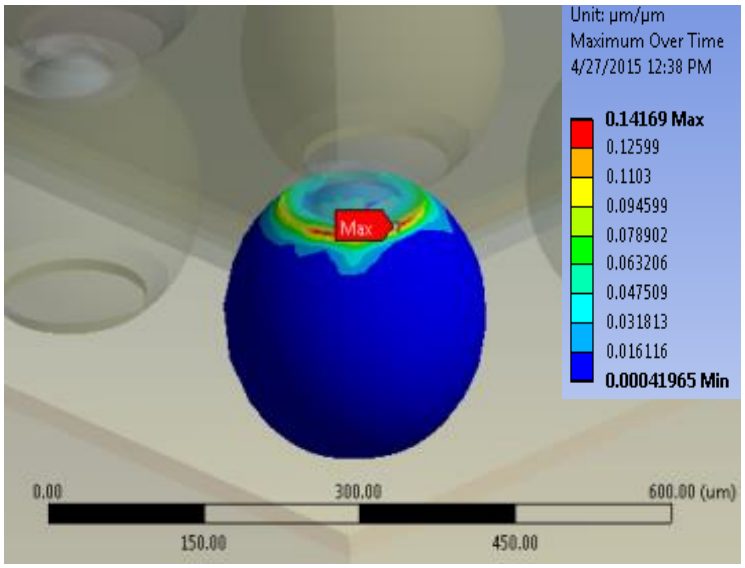

Figure 5-5 Max Strain in Thick Board's Solder

5.2.2 Maximum Von Mises Stress

The maximum von mises stress in the thicker board was found to be 29MPa

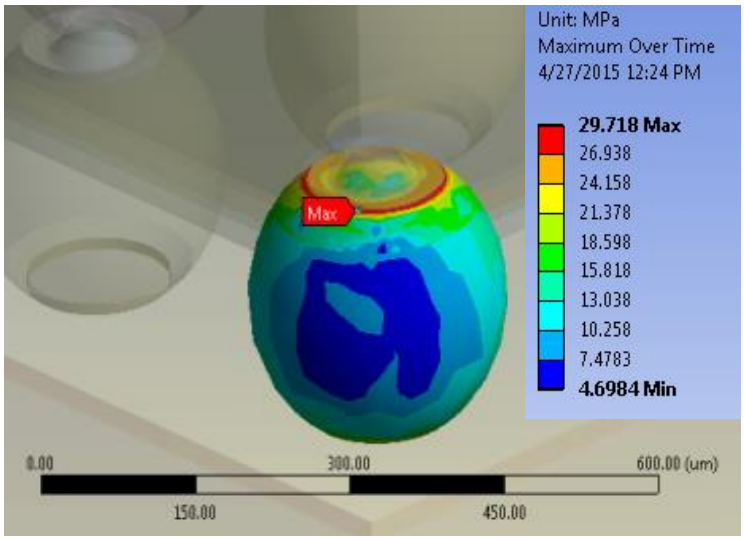

Figure 5-6 Max Stress in Thick Board's Solder

5.3 Results' Analysis

As seen from the results above, the thinner board has less strain but more von mises stress as compared to the thicker board which has a higher strain and less von mises stress. This result is initially in agreement with the experimental results from Texas Instruments as the thinner board was failing earlier than the thicker one.

Life cycles to failure were calculated for both the boards using the volume average plastic work obtained from ANSYS. The fatigue indicator ΔW calculated by the FEM is used to calculate the life cycles to failure using Schubert *et. al* [21] & Che and Pang [22] correlation given below

$$N_f = \left(\frac{A}{\Delta W}\right)^k$$

Where,

N_f = Predicted life cycles to failure

A = 1.256×10^8 MPa

k = 0.4021

The correlation parameters used in this work have been leveraged from Zhao *et. al* [20] work where these correlations were calculated experimentally for Wafer Level Chip Scale Packages (WCSPs). The reason for not using the correlation parameters from Schubert *et. al* work itself is that it provides a very pessimistic number for cycles to failure and the relative error is more than 50% off. The life cycles to failure calculated for both the boards have been plotted below

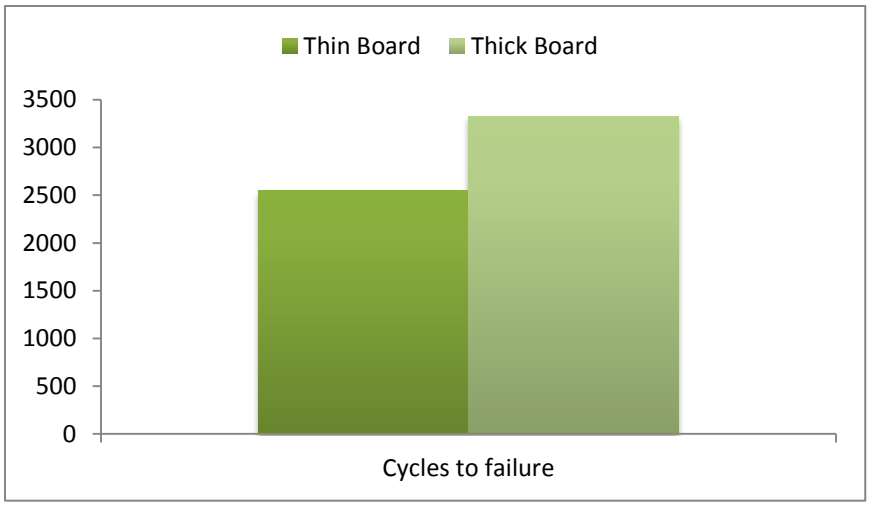

Figure 5-7 Life Cycles to Failure Comparison

5.3.1 Cycles to failure

Since the thicker boards is predicted to have more cycles to failure than the thinner boards, the prediction is in agreement with the experimental results, therefore it was necessary to determine the reason causing the thinner board to fail earlier as compared to the thicker board.

5.3.2 Board's Cross-Section Study

To have a detailed study of the boards, the boards were cross-sectioned using a mechanical cutter and placed in an epoxy which was left to solidify for a few hours. The board inside the solidified epoxy was polished using a 600 and then 1200 sand paper to make the cross-section clearly visible. The cleaned and polished sample is then kept under a 10X magnification lens to study the individual layer of both the boards. The sample once ready for observation with a lens is shown below

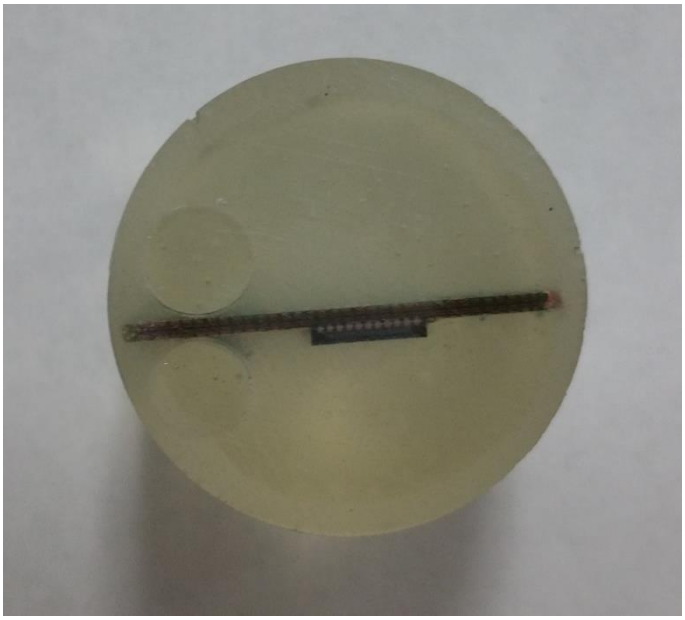

Figure 5-8 Cross-Sectioned Sample in an Epoxy

The experimental setup of the cross-section imaging is shown in the figure below

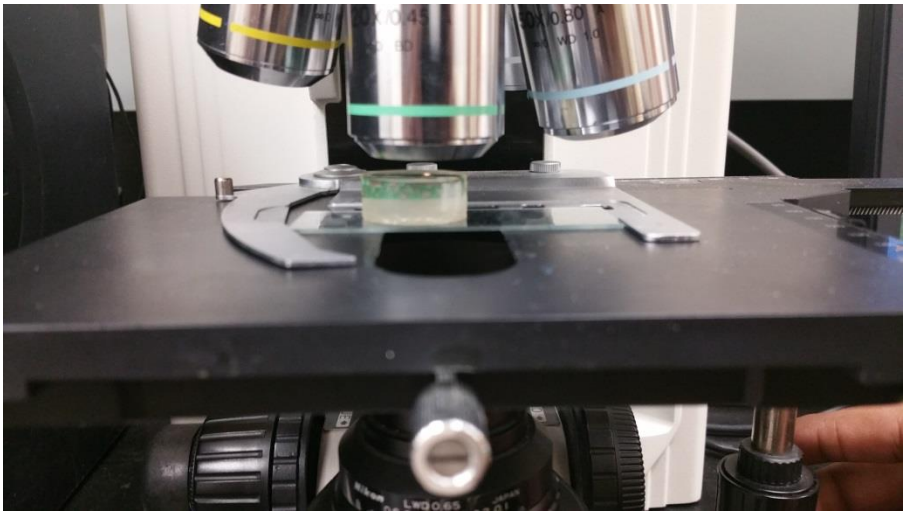

Figure 5-9 Cross-sectioned Sample Under a 10X Lens

5.3.2.1 Cross-Section Results

The detailed cross-section with the thickness of individual layers is shown in the figures below

Thick Board Cross-Section

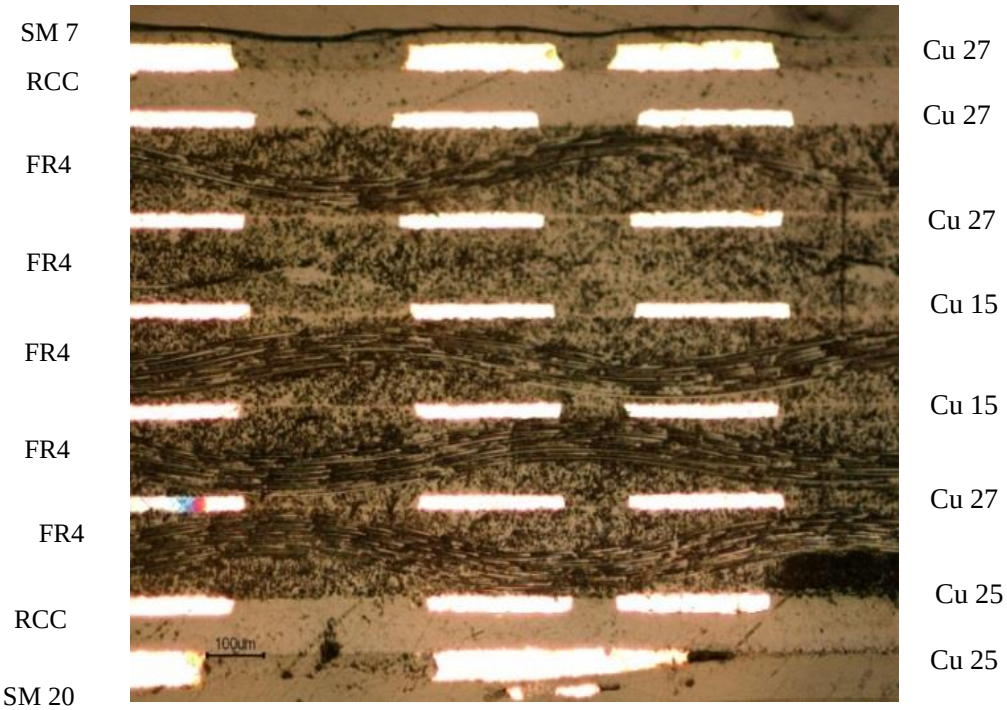

Figure 5-10 Thick Board Cross-Section

Total Cu thickness – 162mm

Vol. of board (mm^3) – 576

Cu/Vol. of board ($\mu m/mm^3$) – 0.2815

Thin Board Cross-Section

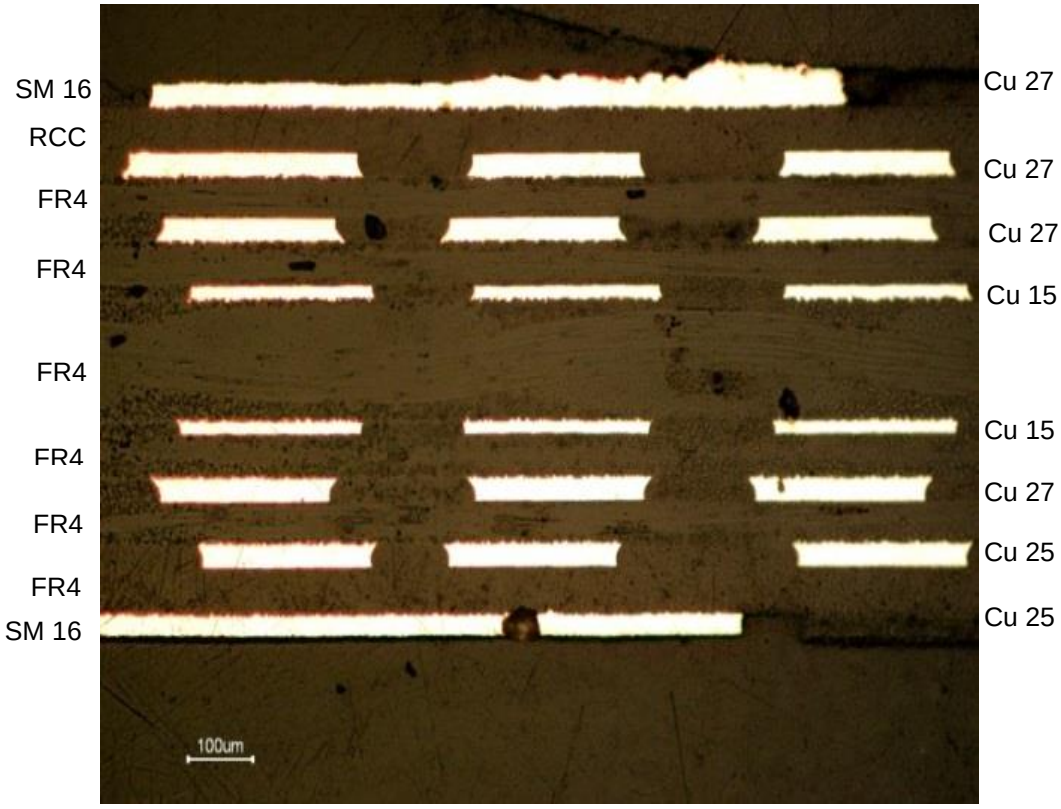

Figure 5-11 Thin Board Cross-Section

Total Cu thickness – 184mm

Vol. of board (mm^3) – 403

Cu/Vol. of board ($\mu m/mm^3$) – 0.456

5.3.3 Boards' Layers Stack Comparison

As seen from the cross-section, the two boards in discussion have a completely different layup as far as the thicknesses of individual layers are concerned. The plot below describes how both the boards are different in their layup

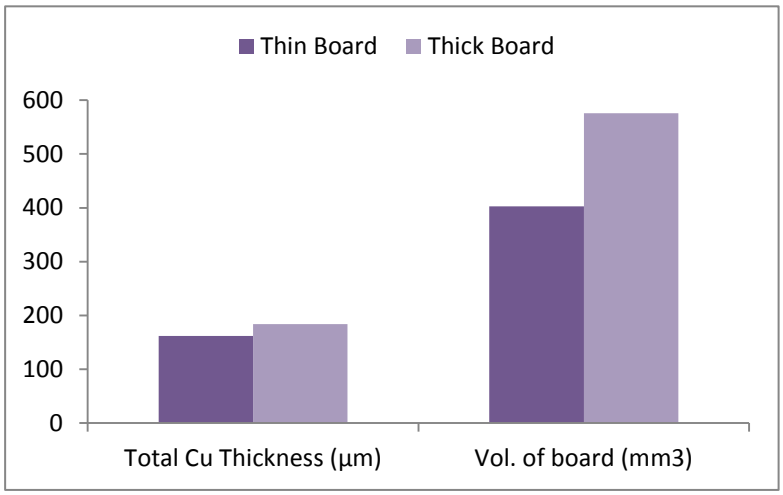

Figure 5-12 Cu Content Comparison in both the Boards

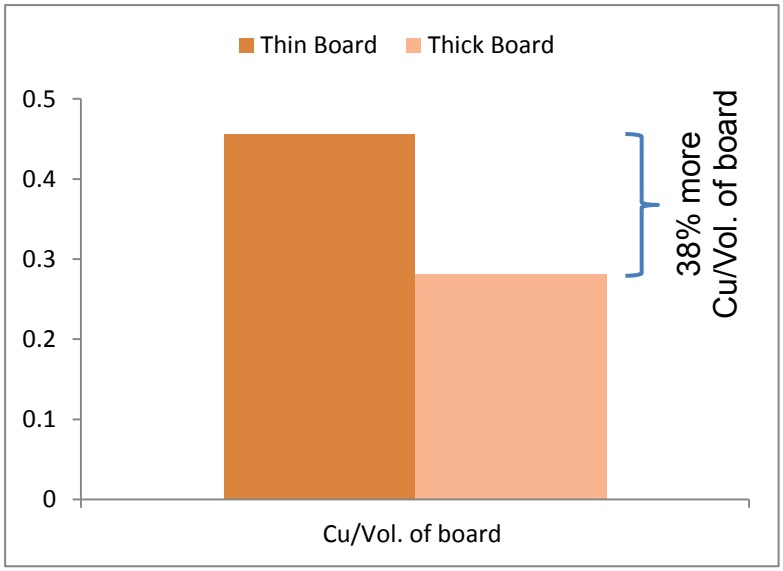

Figure 5-13 Cu/Vol of Board Plot

Chapter 6

Conclusion

As seen from the results above, the thinner board has 38% more Cu/Vol. of board and the thicker board has 38% more FR4/Vol. of board. Since Cu is much more stiff than FR4, the thinner board becomes more rigid than the thicker board. Due to this rigidity it transfers more stresses to the solder balls during thermal cycling. In contrast to the thin board, the thicker one has more FR4 due to which it is more compliant as shown by the strain produced in it during thermal cycling. Due to higher stresses in the thinner board, it has lower life cycles to failure as compared to the thicker board. From this study it could be concluded that the it's not just the thickness of the board that affects its life cycles to failure but its rigidity. The rigid the board, the higher stresses it will put on the solder ball and eventually the solder will fail much earlier and have lower number of cycles to failure.

6.1 Future Work

The following interesting studies could be conducted to take this work forward

- To analytically determine the relation of board's stiffness with the amount of Cu present in its stack
- Find a relation that predicts life cycles to failure based on board's stiffness
- Perform a similar stud on a different set of boards (different thicknesses form this study) to further validate the results

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Biographical Information

Hassaan Ahmad Khan earned his Bachelor's degree from NED University of Engineering & Technology (Pakistan) in 2011. He joined Toyota Pakistan as a Trainee Engineer in 2012 and was promoted to Quality Engineer a year later. He worked there from Jan 2012 to Aug 2013. To pursue an advanced degree in Mechanical Engineering, he enrolled in the University of Texas at Arlington for Fall 2013. He joined the Electronic Mems & Nano Electronic Systems Packaging Center (EMNSPC) headed by Prof. Dereje Agonafer and started working as a Research Assistant. Due to his keen interest in research activities he was awarded EMNSPC Scholarship in the second semester that continued until his graduation. He was extensively involved in a Texas Instruments project funded by the Semi-Conductor Research Corporation (SRC) for more than 3 semesters. His research interests include Board Level Reliability (BLR) under different loading conditions, thermo-mechanical simulation, fracture analysis and material characterization. He authored and co-authored 4 papers in conferences of international repute including ITherm 2014 (Orlando, FL) and InterPACK 2015 (SF, CA). He was offered a position at GlobalFoundries as Equipment Engineer in Malta NY before graduation.