A HIGH FREQUENCY MEMRISTOR EMULATOR CIRCUIT

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Abstract

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In this thesis, a low power, high frequency memristor emulator has been designed. The purpose of emulator circuit is to mimic the behavior of a memristor. The circuit consists of a summing amplifier, an integrator and a multiplier. The circuit has been implemented using commercial off the shelf (COTS) components in Keysight ADS simulation tool.

For CMOS implementation, the emulator circuit has been designed using IBM 0.18um technology. The design of each circuit has been explained in this work. The Opamp designed achieves a gain of 89 dB, output swing of 1.584V and a bandwidth of 3.67 MHz. The circuit designed using Cadence Spectre provides results consistent with the block level simulation. From the simulations, it is observed that the circuit exhibits memristive behavior up to 16 kHz, after which the circuit behaves as a simple resistor. This circuit can be used to compensate process variations in amplifiers, can be programmed to required resistance values by applying a train of pulses with proper count, amplitude and duration.

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Chapter 1

Introduction

Memristor was first devised by Leon. O Chua in 1971. The purpose was to find a missing link between flux and charge. Passive elements such as R, L and C provide relation between Voltage – Current, Flux – Current and Voltage – Charge respectively. There was a link missing to relate Flux and Charge. Hence, a mathematical model of element which exhibits this relation was devised.

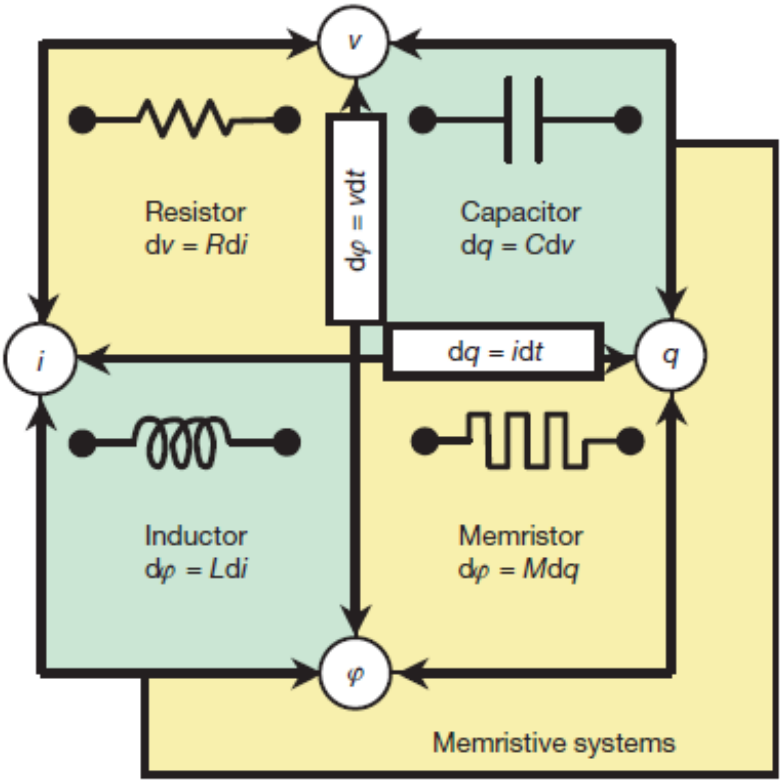

Figure 1-1 Four passive elements [1]

The term “memristance” was coined because this element can remember all the inputs applied. The resistance of the device according to the input applied.

When the input signal is removed, the resistance of the device freezes. Hence, by measuring the resistance at different intervals, one can determine which input signal has been applied and amplitude of the signal applied.

Even though the first mathematical model of memristor was devised in 1971, the equivalent model on semiconductor was developed by R.S. Williams of HP labs in 2008. This memristor model exhibits the pinched hysteresis loop and satisfies the requirements of, memristor and memristive devices, in general. Figure 2 shows the characteristic pinched hysteresis loop of a memristor.

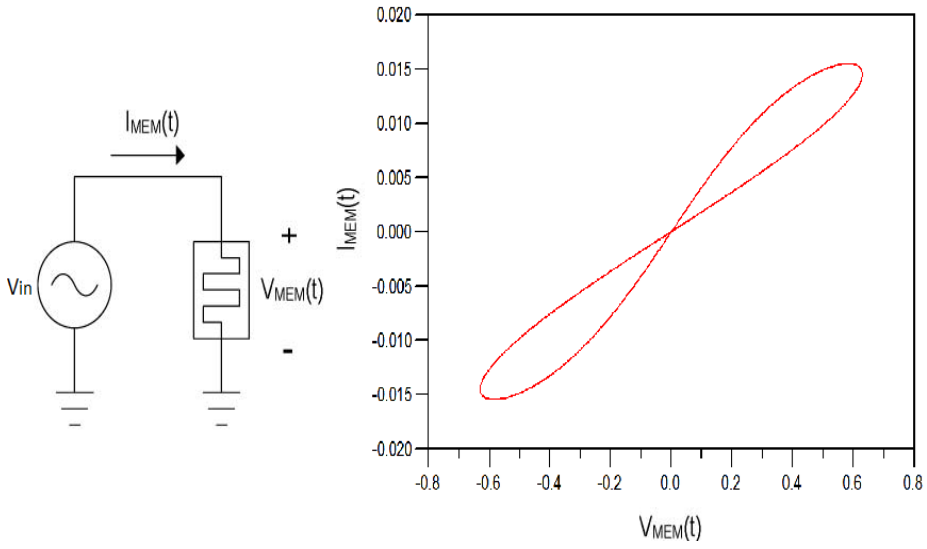

Figure 1-2 Memristor "Pinched Hysteresis" Loop [33]

Some of the important properties of memristor are i) non-volatility, ii) dynamic response, iii) low energy consumption and iv) high density [25]. Because of these properties, memristor finds a wide range of applications such as "Fine Programmable Resistors", amplitude modulators, non-volatile memories, memory threshold logics and it can mimic the function of synapse to emulate brain cells in neuromorphic circuits.

However, only HP labs have developed memristor model. Due to very small device dimensions [23], it is not available as a commercial component in the electronics market. Hence, efforts have been put to design circuits which can mimic the behavior of a memristor. Since memristor's purpose is to remember the previously applied signals, integrator forms the core of the emulator circuit. Multiplier circuit is commonly used to generate quadratic relation between current and voltage or vice versa.

Over the past few years, memristor emulator circuits have been designed using commercial components and implemented on PCB or breadboards. [30] implement memristor emulator based on LED/LDR optocoupler. The optocoupler is chosen because LED's brightness controls the conductance of LDR. When output of LED is low, the resistance of LDR is high and when output of LED is high, resistance of LDR is low. Since the photocell has a non-linear response, a 1KΩ resistor is used to operate the optocoupler in linear region. The change in the intensity of light results in change in the slope of conductance, leading to change in the resistance. The signal is offset to operate LDR in linear region. The highest frequency up to which memristive behavior can be seen is 280 Hz.

In another type of emulator circuit [31], a voltage controlled conductance G_M has been used. A JFET transistor has been used to realize the variable conductance by operating the device at very small V_{DS}. The gate voltage V_{GS} causes change in the slope of conductance characteristics. Hence, as the input signal changes, the conductance of the JFET changes. The highest frequency of operation achieved is 2Hz. The resistor R and condenser C in the integrator determine the frequency of operation.

Kim [29] employs a dual current mirror circuit to copy the current flowing through input resistor R_S. The current mirror formed by PMOS copies the negative part of current, whereas, NMOS current mirror copies positive part of current to R and C. A buffer has been added to prevent discharge of capacitor. A multiplier is used to multiply voltage across R and C to generate quadratic relation, generating the pinched hysteresis loop. The frequency up to which memristive behavior can be seen is 800Hz.

Some of the limitations of these circuits are the use of potentiometer [30, 31], which is used to vary the conductance of the devices. This causes a hindrance when designing circuit at transistor level. Also, due to a large number of blocks, the delay is very high and hence higher frequency of operation cannot be achieved. In addition, the circuits occupy large areas.

The objective of this work is to develop a compact, low power and high frequency memristor emulator circuit. The purpose is to design a circuit which can mimic the behavior of a memristor, so that it can be used for compensating process variations or to be used as a memory element in non-volatile memories.

This thesis is divided into 4 sections:

Chapter 1 gives a brief introduction to memristor and the need for emulator circuits. The research objectives of this thesis are also described.

Chapter 2 provides a background study on memristors, their properties and some applications.

Chapter 3 provides design of proposed emulator circuit. It first shows block level simulation of circuit with commercial off the shelf (COTS) components. Then

CMOS implementation of the circuit in IBM 0.18 um technology is described with emphasis on each block.

Chapter 4 concludes this thesis with contribution of this work and set of objectives for further research.

Chapter 2

Background

2.1 Introduction to Memristors

Till 1971, there existed three passive elements i.e. resistor, capacitor and inductor. They relate the variables as voltage – current, charge – voltage and flux – current. However, there was a missing link between flux and charge. Hence, Leon Chua proposed a mathematical model which can give the relation between the two variables, called the memristor [2]. Since flux is the integral of voltage and charge is the integral of current, the quantity memristance is given by

$$M(q) = \frac{d\phi(q)}{dq} \tag{1}$$

Where M indicates memristance of the circuit. Since integration refers to addition of all the inputs till current time instant *t*, this passive element adds up all the signals up to the current instant. Hence, the circuit "remembers" all the signals that have been applied to it. Hence, it is also called the memory resistor.

However, there was no semiconductor device which can generate memristive behavior. In May 2008, Stanley Williams and his group at HP developed the first semiconductor model of memristor as shown in Figure 2-1.

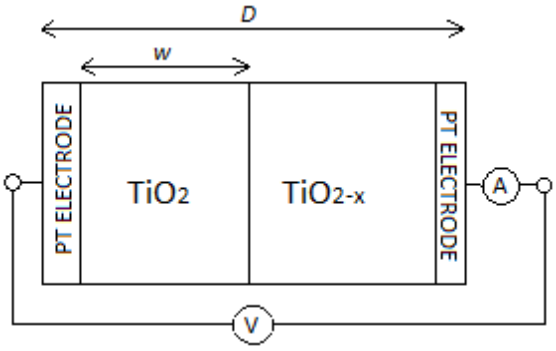

Figure 2-1 Memristor semiconductor model [33]

The device consists of two platinum electrodes, a layer of platinum dioxide and a layer of titanium. However, when potential is applied, the titanium sucked out [3] oxygen molecules out of platinum. What they found was a layer of platinum, layer of TiO_2 and a conductive layer of TiO_{2-X} with oxygen vacancies as shown in Figure 2-2.

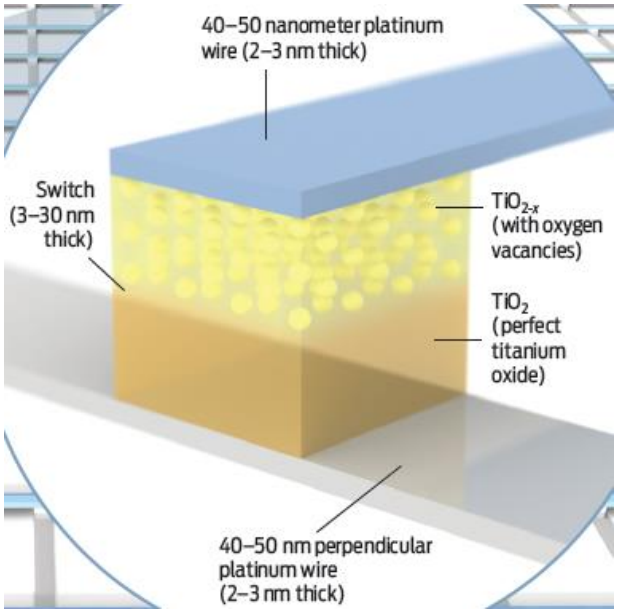

Figure 2-2 Device after applying an external voltage [3]

To verify the properties of the device, positive and negative voltages were applied. When a positive voltage is applied, the oxygen vacancies, which are donors of

electrons, move away from the positive terminal. Hence, the effective area of TiO_{2-X} increases and the conductance of the device increases as shown in Figure 2-3.

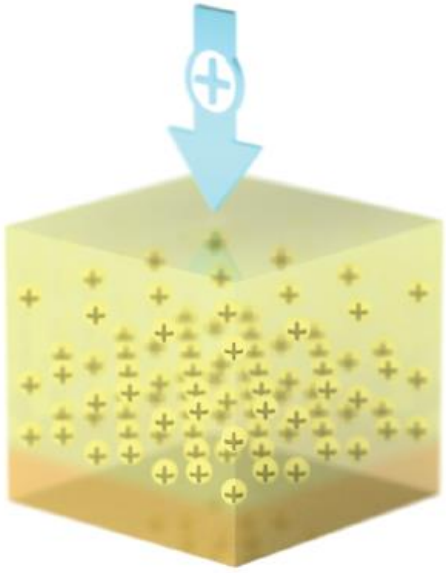

Figure 2-3 Positive voltage effect [3]

When a negative potential is applied, the oxygen vacancies move towards the negative electrode and the conductance of the device decreases, as shown in Figure 2-4.

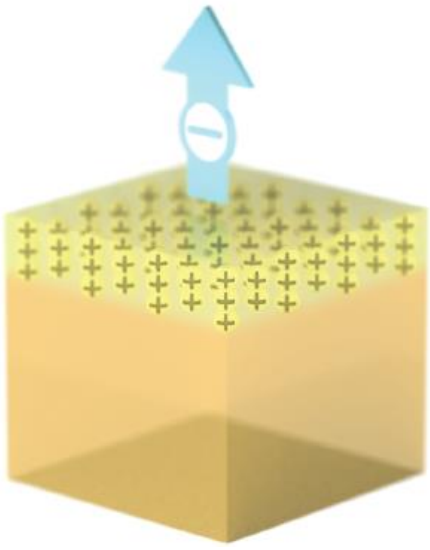

Figure 2-4 Negative voltage effect [3]

The most important characteristic of the device is when the voltage applied is removed, the oxygen vacancies do not move back to their original position. Once the applied signal is cutoff, the position of the oxygen vacancies is fixed and the resistance of the device remains constant. The resistive equivalent of the circuit is similar to two resistances connected in series. R_{ON} indicates the on-state resistance of the device (usually in hundreds of ohms) and R_{OFF} is the off-state resistance of the device (in hundreds of kilo ohms). As boundary between doped (TiO_{2-X}) and undoped (TiO_2) changes, based on the voltage applied, the resistance of the device changes accordingly as seen in Figure 2-5.

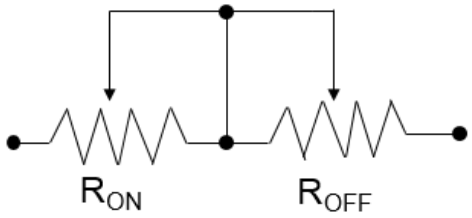

Figure 2-5 Resistor equivalent of memristor [1]

Integrating equation (1), general expression for memristance or memductance is given by

$$I(V) = m.V^2 + A.V \tag{2}$$

Where m indicates the memductance and A is a constant. When we plot I vs V for memristor, a pinched hysteresis loop is observed as seen in Figure 2-6.

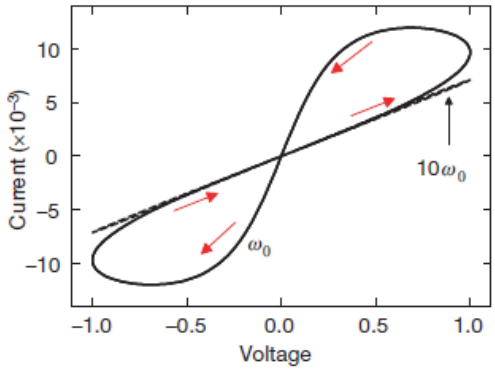

Figure 2-6 Memristor Pinched Hysteresis Loop [1]

For a sinusoidal input signal, the resultant flux over a cycle is zero. As the frequency increases, oxygen vacancies are not mobile enough to move as the input changes. Hence, due to lower mobility, the oxygen vacancies are immobile and hence the resistance of the device remains constant. Hence, at higher frequencies, the device behaves as a resistor as seen in Figure 2-6.

If a train of positive or negative pulses is applied, the memristance of the device decreases or increases respectively [4]. For a positive pulse train, the oxygen vacancies move away from the positive electrode and hence the conductance of device increases. After the resistance is programed to a specific value, the pulse train can be removed as seen in Figure 2-7.

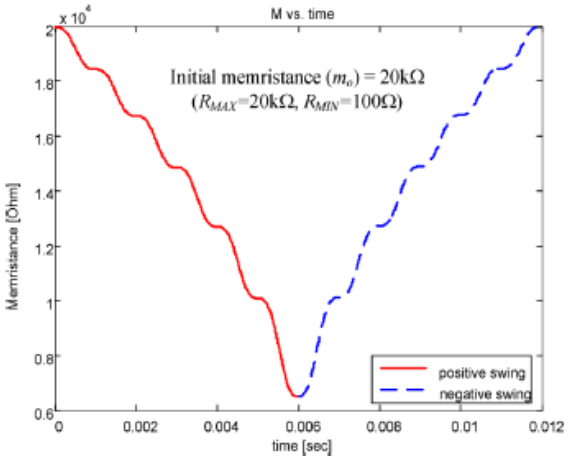

Figure 2-7 Memristance for pulse train [4]

Memristance of a device depends on the following parameters, 1) Amplitude of the input signal applied, 2) Duration of the applied signal, 3) Frequency of the applied signal, and 4) Duty cycle of the input signal. As input amplitude changes, the oxygen vacancies move and the resistance of the device changes accordingly. As the duty cycle increases, duration for which input is high increases, leading to lower resistance of memristor. For an unbalanced input, the flux accumulates over time and the device conductance [4] changes as seen in Figure 2-8.

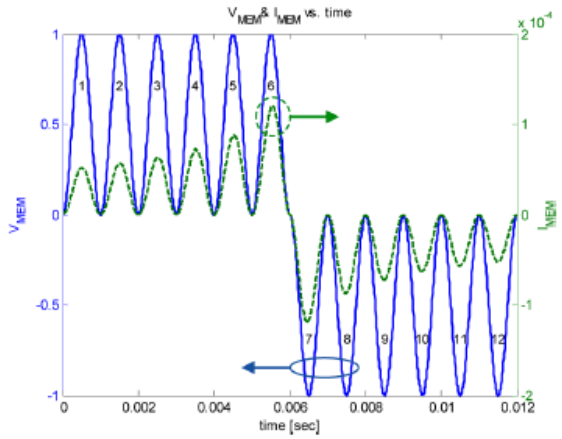

Figure 2-8 Unbalanced Input (blue) vs device current (green dotted) [4]

2.2 Properties of a Memristor

Some of the important properties of a memristor are:

1) Non volatility

Memristor remembers the signals that have been applied from $-\infty$ to current time instant *t*. If the input signal is removed, the resistance of device freezes and does not change until the input signal is applied again.

2) Dynamic Response

The boundary between TiO_2 and TiO_{2-X} changes as the input amplitude changes. When the signal amplitude reaches the peak, the boundary reaches either end of the device and the device switches from on state to off state or vice versa. The non-linearity of the device and boundary conditions on state variable [25] generate hysteretic behavior.

3) High Density

The first memristor fabricated by HP had device dimensions of 30nm X 30nm. Due to very small size of the device, memristor can be used in high density memory application, especially high speed non-volatile memories.

4) Fast switching

Memristor switches from on state to off state and vice versa in pico seconds range. When the polarity of the signal applied reverses, the boundary switches to either extremes of the device and the device conductance changes. Also, due to high ion mobility u_v and small dimension D, the rate of switching is very fast as seen from equation 3 [3].

$$t_s \sim (D^2 . R_{OFF}) / [(2 . u_V . v) + R_{ON}] \quad (3)$$

Where, t_s is switching time for device, u_v is ion mobility, D is device dimension and v is external bias voltage.

5) Small parasitics and CMOS compatible

Memristor exhibits very small parasitics. They exist at the interface of thin platinum layer and titanium dioxide layer. Also, this device can be combined with MOSFETS to form hybrid cmos-memristor crossbar array for low power medical applications [20].

6) Low energy consumption

When memristor switches from low resistance to high resistance or vice versa, amount of energy consumed is in femto-Joules [24].

2.3 Applications of Memristor

Due to small dimension, non-volatility and low power dissipation, a wide range of analog, digital and neuromorphic circuits can be designed which incorporate memristor, some of which are listed below.

A.1) Fine Programmable Resistors

In amplifier and filter circuits, resistors need to be programmed for specific application or for compensating the PVT (Process, Voltage and Temperature) variations. The programmable resistors are made of MOS based switch control circuits. But due to large capacitance offered by mos devices, an alternate compensation circuit is needed. Floating gate devices were exploited where the resistance of device is programmed by charging the floating gate through Fowler-Nordheim and avalanche

injection. However, the problem with this approach is the damage to gate oxide, which could lead to faulty device functioning. The use of memristor in this case was proposed. By applying a train of pulses, the resistance can be programmed to the required value for PVT compensation.

A.2) Programmable Gain Amplifier

A simple programmable gain amplifier is shown in Figure 2-9. By applying a train of pulses to the memristor, resistance of the device can be programmed to specific value and the gain of the amplifier, which is dependent on memristor based load resistance, can be programmed to the required value. In [13], memristor is programmed with a pulse voltage of 0.5V and frequency is ten times the input signal frequency.

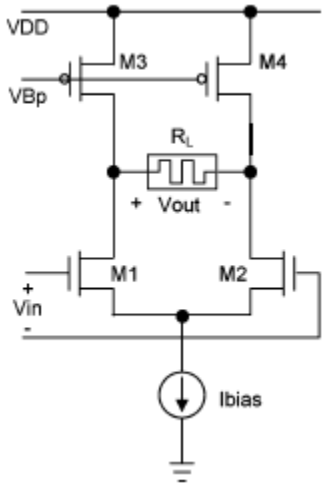

Figure 2-9 Memristor based programmable gain amplifier [13]

In addition, by changing the pulses train duty cycle and the number of pulses applied, the small signal voltage gain of the amplifier can be programmed as shown in figure 2-10.

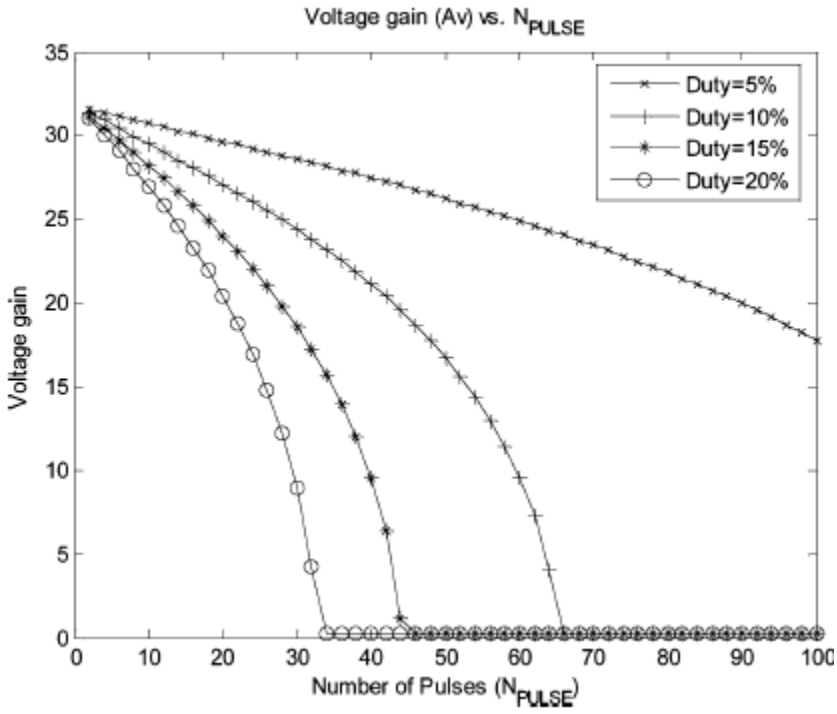

Figure 2-10 gain variation with pulse count [13]

A.3) CMOS-Memristor hybrid circuit for emulating function of Synapse

Synapse is a link which connects two neurons. The exchange of information between neurons occur due to flow of ions through the membrane. When there is an influx of ions, it is called potentiation and the conductance of the synapse increases. When the flux of ions drop, it is called depression and the conductance of the synapse decreases. In [19, 20], hybrid memristor-cmos logic has been used to mimic the neuron synapse link as seen in Figure 2-11.

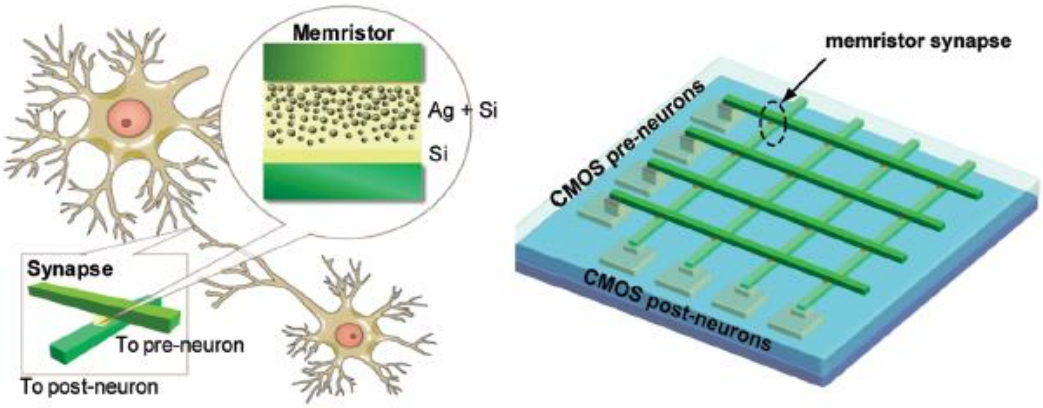

Figure 2-11 a) Memristor as a synapse [19]

The memristance is programmed by applying a train of positive pulse of amplitude 3.2V and then a train of negative pulses of amplitude -2.8V. As a result, the conductance of memristor changes according to the input amplitude, frequency and duration as seen in Figure 2-11.

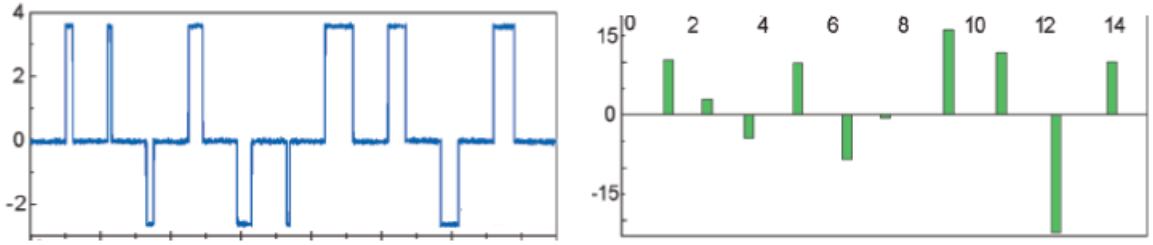

Figure 2-11 b) Input pulses (blue) and conductance of synapse (green) [19]

A.4) Memristor based threshold logic (MTL) gates

Memristor is used at inputs of a gate as a resistors to weigh the current flowing from the inputs to the gates as shown in Figure 2-12. A current mirror is used to isolate current flowing through different inputs and a current comparator is used to compare the sum of total current with reference current I_{ref}. If the summed current is greater than

I_{ref}, the output of MTL gate is logic 1, else the output is logic 0. A positive voltage of 1V denotes logic 1 and 0V denotes logic 0.

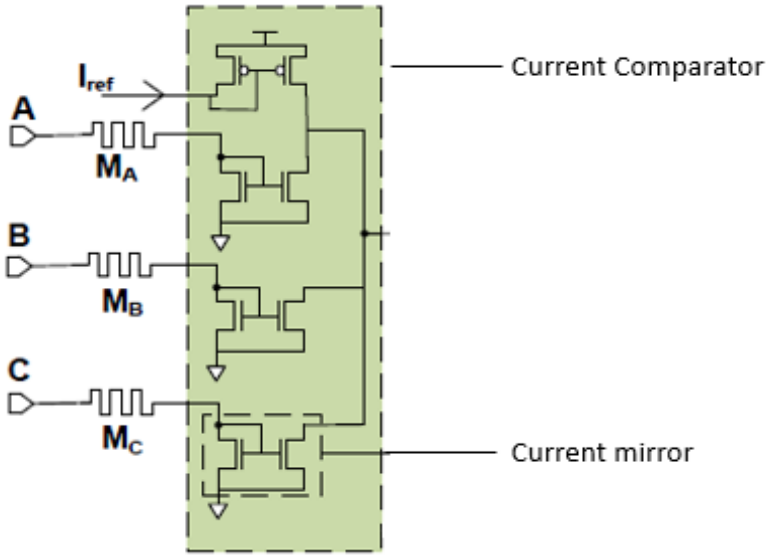

Figure 2-12 Memristor-based Threshold Logic gate [25, 26]

A.5) Memristor based memory

Memories based on memristor have been implemented on crossbar array by growing memristor at each junction of row and column lines. Logic 0 and is represented by memristance values M0 and M1 respectively with value of M0 at least twice that of M1. Figure 2-13 shows the memristor based memory array. To write a value into memristor, there are two approaches. First is to reset the memristance to M0 and then apply voltage pulse of proper duration to program memristor to required resistance value. In second approach, iterative read and write pulses are applied to monitor the resistance value of memristor. To read the memristance programmed value, the transistor along the corresponding row is turned on by applying read voltage V_{read}. The voltage drop across the resistor is compared to reference voltage V_{ref} using a sense

amplifier and the output of sense amplifier is logic 0 or logic 1 based on the programming of the memristor.

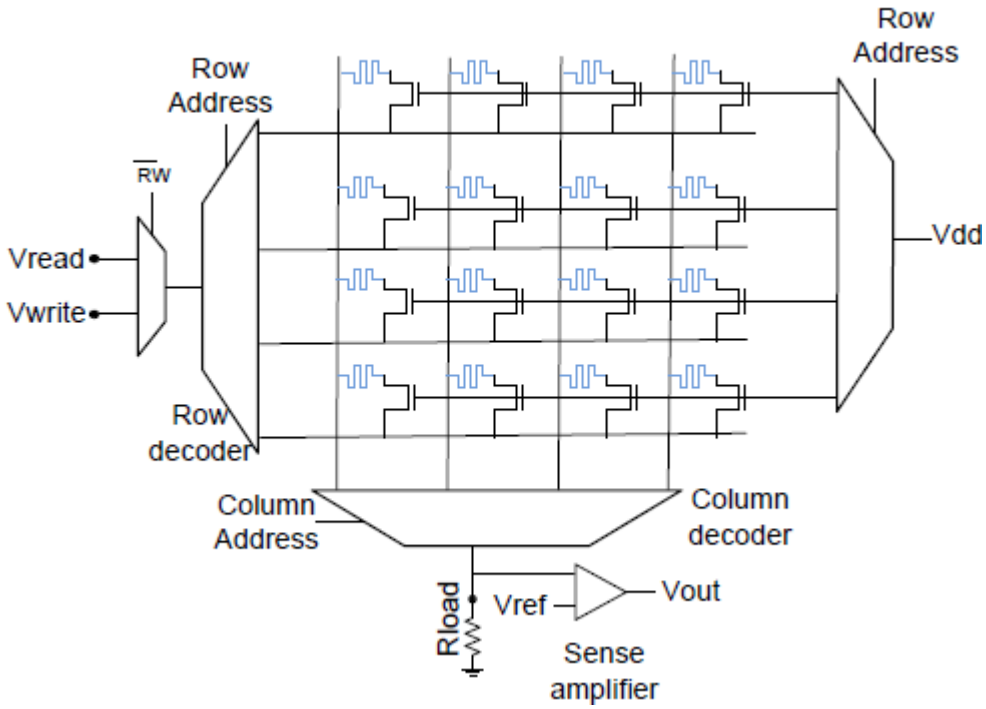

Figure 2-13 Memristor based memory array [25]

2.4 Memristor Emulator

However, due to small device dimensions, memristor is not available as a commercial component in the electronics market. Hence, efforts are being put to design circuits which can mimic memristive behavior. In [30], an emulator circuit based on Light Dependent Resistor is designed as shown in Figure 2-12.

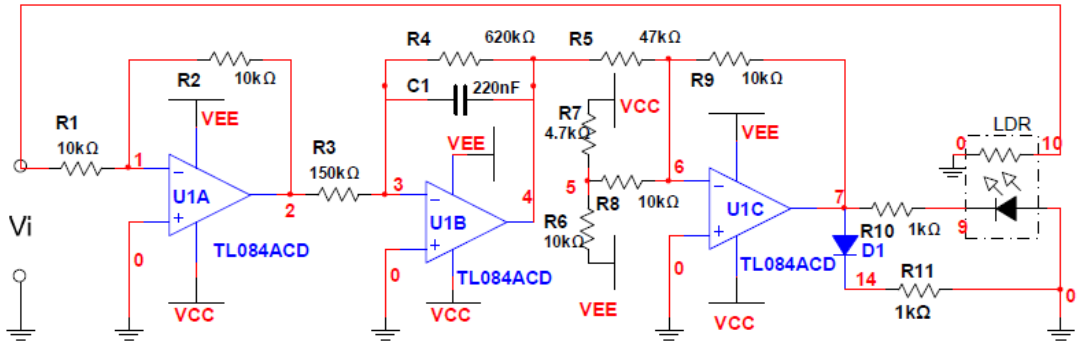

Figure 2-14 Memristor based on LED/LDR optocoupler [30]

In this circuit, an optocoupler is used to generate variable resistance based on the input signal. Based on input voltage the brightness of LED changes. The change in intensity causes the current through photocell to change. A potentiometer is used to bias the LDR in linear region. Based on the intensity of light, the slope of conductance changes, implying change in resistance.

A series resistance of 1KΩ and diode D1 is used with LED to prevent reverse breakdown of the device. Opamp U1A forms a buffer to minimize current drawn from the input. Opamp U1B makes the integrator along with resistors R3, R4 and capacitor C1. R6 and R7 form the trimpot to adjust the linear range for conductance of LDR. Input dependent resistance is modelled by LED and LDR, realized by using Silonex NSL-32, an analog optocoupler.

This circuit exhibits memristive behavior up to 280Hz, and the frequency range is determined by R3, R4 and C1. The Opamp operate at ±15V and an input of 0.4V and 0.8V is used. The circuit is implemented on breadboard using COTS (Commercial Off-

The-Shelf) components. In another type of emulator circuit [31], an enhancement type JFET is used to generate variable conductance as shown in Figure 2-13.

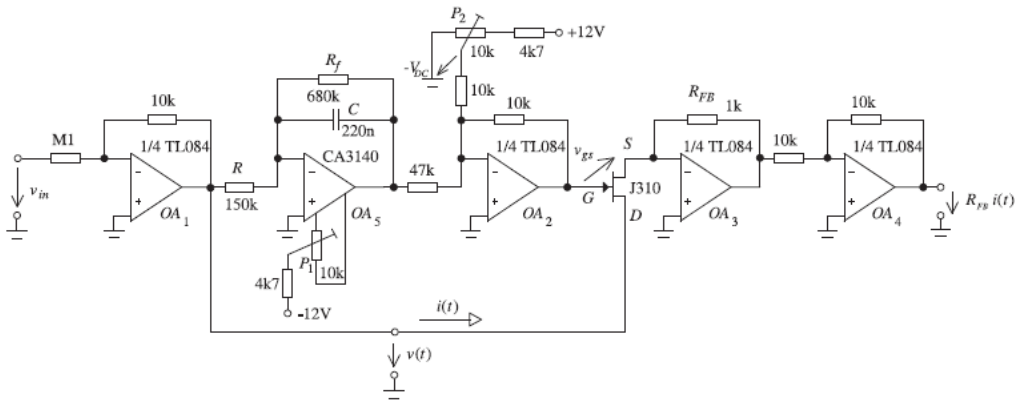

Figure 2-15 Analogue model of memristor [31]

The most important part is realizing the voltage controlled conductance G_M. It is realized using the D-S (Drain to Source) channel of JFET. Based on the applied Vds (Drain-source voltage), the channel current changes. Here, the Vds applied to JFET is very small, to operate the device in linear region. By changing the Vgs (gate-source voltage), the slope of current characteristics change, which results in change in resistance. Higher the slope, lower is the resistance and vice versa.

In this circuit, Opamp OA_1 forms a buffer, to lower the current drawn from the input and provide impedance matching between the input source and memristor model. Opamp OA_2 forms an integrator, along with resistors R, R_f and C. The chosen values of these components determine the frequency band of operation. Opamp OA_2 acts as a summing amplifier and potentiometer P2 determines the conductance region of the JFET device. The current through the device, I_{DS}, causes a voltage drop across the

feedback resistor R_{FB} and OA_4 is used to provide correct sign of output voltage, proportional to the memristor current.

For an input voltage of 0.4V, the I_{DS} vs v(t) graph is plotted using DSO. The circuit exhibits memristive pinched hysteresis loop and the frequency at which the memristive behavior falls to a straight line is 2Hz. At higher frequencies, the circuit behaves as a linear resistor. Instead of analog type memristor emulator model, a digital memristor emulator was developed [28], as seen in Figure 2-15.

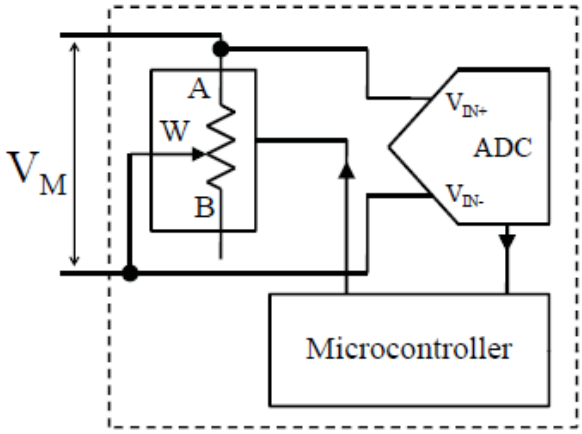

Figure 2-16 Digital memristor emulator circuit [28]

Programmable memristor acts as a digital potentiometer. When memristor is programmed, amplitude of programming pulses is crucial. For voltages below a threshold level, the resistance change in memristor is small and for larger voltages, the accuracy of programming the resistance to required value is affected. Hence, a train of pulses with small width and small amplitude (below a threshold level) is preferred in programming the memristor.

This circuit consists of a digital potentiometer, an ADC and a microcontroller. The, A and B terminals of potentiometer, serve as external connections. The voltage

across these terminals is given to the ADC. The ADC provide the value of voltage at memristor's terminals to the microcontroller. The microcontroller is programmed to calculate the value of resistance, based on the code, and update the value of the resistance by changing the wiper terminal of the digital potentiometer. Hence, as the input changes, the input to microcontroller changes, the resistance value is updated by microcontroller and wiper terminal of the digital potentiometer changes accordingly. As the input increases, the resistance decreases and vice versa.

The digital potentiometer used for simulation is AD5206, a 10KΩ, 256 positions digital potentiometer and microcontroller used is dsPIC30F2011, which has a 12-bit internal ADC. The circuit operates at ±2.5V and the memristance can be observed up to 50Hz. A memristor emulator employing current mirror is described in [29]. The purpose is to mirror the input current into the capacitor and resistor. The voltages across them is multiplied and fed back to the non-inverting terminal of the input amplifier as shown in Figure 2-15.

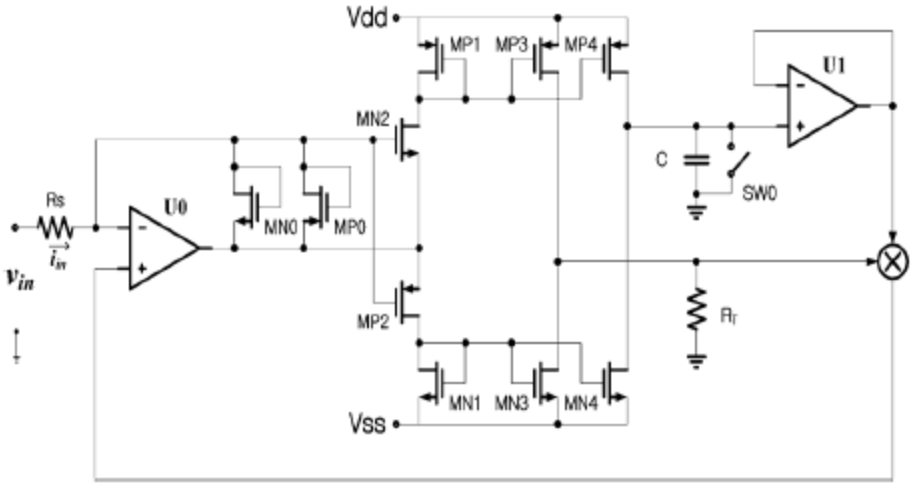

Figure 2-17 Current mirror based memristor emulator [29]

The input voltage is translated to current by passing it through resistance Rs. The purpose of using complementary current mirrors is to copy positive and negative current signal into resistor R_T and capacitor C. When positive voltage is applied, the positive part of current is duplicated by current mirror MP1 and MP4 to capacitor and MP1 and MP3 to resistor. The voltage drop across them is multiplied by an analog multiplier and the output is fed back to the non-inverting terminal of Opamp U0. For negative part of current, current mirrors MN1 and MN3 copy current to resistor and MN1 and MN4 copy to capacitor. Opamp U1 is used to prevent the discharge of capacitor during programming phase. A switch SW0 is added to reset the circuit by shorting the capacitor to ground. The above circuit is an incremental type memristor emulator and by adding an inverter in the feedback path, decremental memristance can be achieved.

The circuit was developed using commercial components and the hysteresis was observed on oscilloscope. The highest frequency up to which the memristive behavior can be observed is 800Hz. At higher frequencies, the pinched hysteresis falls to a straight line. The circuit operates at $\pm$15V and supply used for current mirror is $\pm$5V.

Table 1 shows comparison of different architectures.

Table 2-1. Comparison of existing architectures

Sr. No.	Supply voltages	Hysteresis Frequency
[30]	±15V	280Hz
[31]	±15V	2Hz
[28]	±2.5V	50Hz
[29]	±15V and ±5V	800Hz

Chapter 3

Low Power, High Frequency memristor emulator circuit

In this chapter, design and analysis of the proposed circuit is explained. In section 1, the block level design will be explained along with the simulation results. Then, in section 2, cmos implementation of the circuit will be explained with description of each block. In section 3, the results of ADS block simulation and cmos implementation results will be discussed and comparison with other architectures will be shown.

3.1 ADS Block Simulation

A simple and compact memristor emulator circuit is designed. It consists of a summing amplifier, an integrator and a multiplier circuit. The circuit is implemented in Keysight ADS and commercial components have been used for the simulation as shown in figure 3-1.

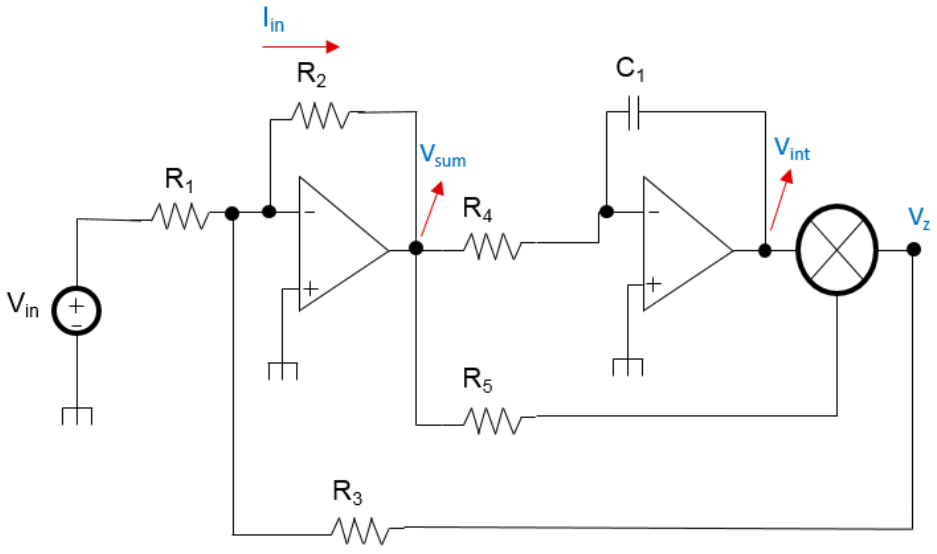

Figure 3-1 Proposed Memristor emulator circuit [33]

The first Opamp acts as a summing amplifier, which adds the input voltage and the output of the multiplier circuit. The second stage is integrator, which is formed by Opamp, R4 and C1. The frequency band of operation is determined R4 and C1. The output of integrator and summing amplifier are fed to the multiplier.

The multiplier generates second order signals which establishes a quadratic relation between current I_{in} and output voltage V_z. By applying KCL at different nodes we find the following relations.

Voltage at the output node of summing amplifier is given as:

$$V_{sum} = \left(-\frac{R2}{R1}\right) \cdot V_{in} + \left(-\frac{R2}{R3}\right) V_z \tag{4}$$

Integrator output is given by:

$$V_{int} = \left(\frac{-1}{R4 \times C1}\right) \int V_{sum}\, dt \tag{5}$$

Output from summing amplifier and integrator is fed to the multiplier:

$$V_z = V_{sum}\, V_{int} = \left(\frac{-1}{R4.C1}\right) \int V_{sum}^2\, dt \tag{6}$$

Relation between I_{in} and V_z is given as:

$$I_{in} = \left(\frac{Vin}{R1}\right) + (m).V_z^2 + (A.V_{in}^2) + (B.V_{in}.V_z) \tag{7}$$

Where, *m* is the memductance of the circuit and *A, B* are constants consisting of Rs and Cs.

The circuit has been designed using the specifications from the commercial components. The Opamp used is TL082CP, which is a high gain and high slew rate Opamp. The analog multiplier used is AD633ANZ, which is the only four quadrant

analog multiplier IC. Table 2 shows the list of commercial components used for simulation.

Table 3-1. List of commercial components used

Sr. No.	Component	Commercial part used for simulation	Qty.
1	Opamp	TL082CP	1
2	Multiplier	AD633ANZ	1
3	Capacitor	0.5uF	1
4	Resistors	1KΩ	2
		2KΩ	1
		5KΩ	2

The circuit operates at a supply voltage of ±15V and an input of 0.6V is applied. The circuit exhibits memristive behavior up to 16 KHz and at higher frequencies the pinched hysteresis falls to a straight line. Figure 3-2 shows the memristive hysteresis curve.

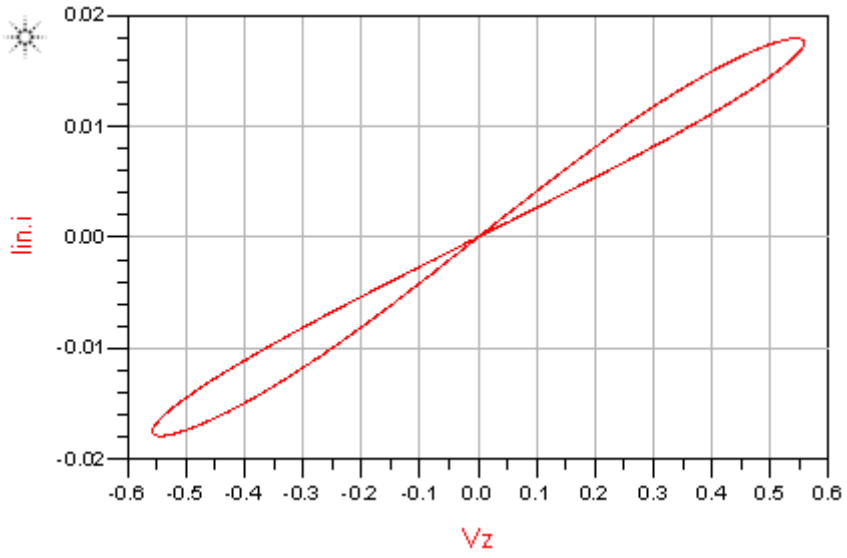

Figure 3-2 Memristor pinched hysteresis loop

It is imperative to understand how the circuit generates the hysteresis loop. Initially, as the input signal increases, the output of the summing amplifier increases with opposite sign. The integrator accumulates the signals by charging the capacitor. The output of both integrator and summing amplifier are negative. Hence, the output of multiplier is positive and hence the current starts increasing, following a parabolic curve as shown in figure 3-3 and region 1 in Figure 3-4.

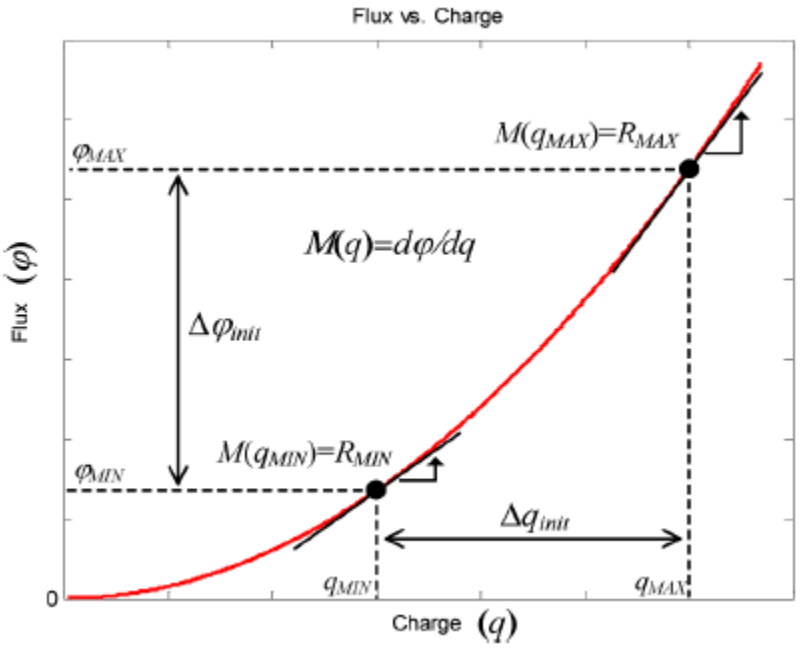

Figure 3-3 Quadratic behavior of memristor [4]

But as the input signal changes sign, the output of summing amplifier is decreasing. But the output of integrator still has the same sign. Hence, due to opposite sign of signals at multiplier's input, the output is negative and the current falls, following a quadratic path again, as seen in region 2 of Figure 3-4. Due to large R and C for integrator, the time taken for signal to change its sign is longer than the summing amplifier. Similarly, when the output of integrator is negative and output of summing amplifier is negative, the current increases in reverse manner (Region 3 of Figure 3-4). When the output of integrator and summing amplifier are of opposite sign, the current falls again (Region 4 of Figure 3-4).

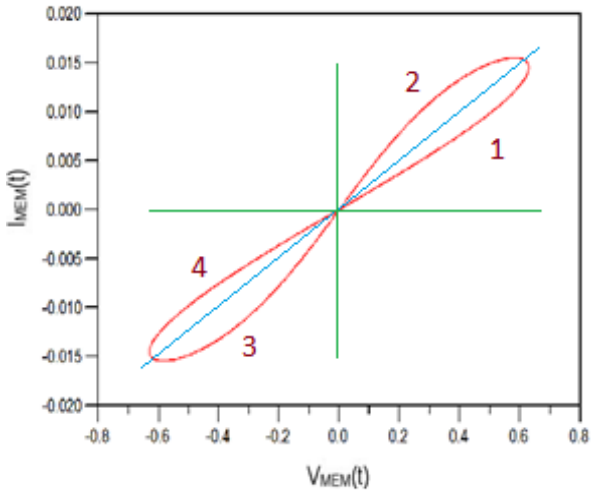

Figure 3-4 Behavior from circuit's point of view

As can be seen from the above figures, for a sinusoidal input signal, the resistance of the device remains same. As the frequency increases, the capacitor cannot charge and discharge quickly. Hence, the integrator output remains nearly constant. Hence, a higher frequencies, the circuit behaves as a resistor as shown in Figure 3-5.

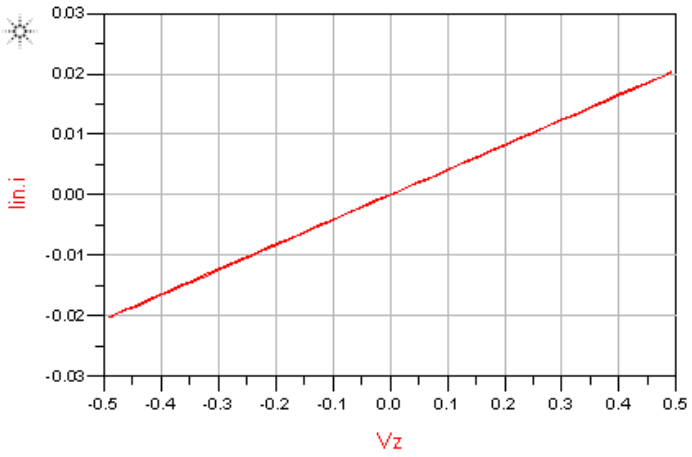

Figure 3-5 Circuit behavior at high frequencies at 16 KHz

An offset compensation circuit has been added to the Opamps for block simulation. The transistors in the circuit mismatch in parameters with each other during

fabrication. Hence, there exists a certain degree of mismatch in every circuit. This is one of the causes for offset voltage to exist in circuits. For an Opamp, it is expected that when both the inputs are equal, the output should be zero. However, due to non-idealities, the output of Opamp is not zero but another value. This is called DC offset [36], as shown in Figure 3-6.

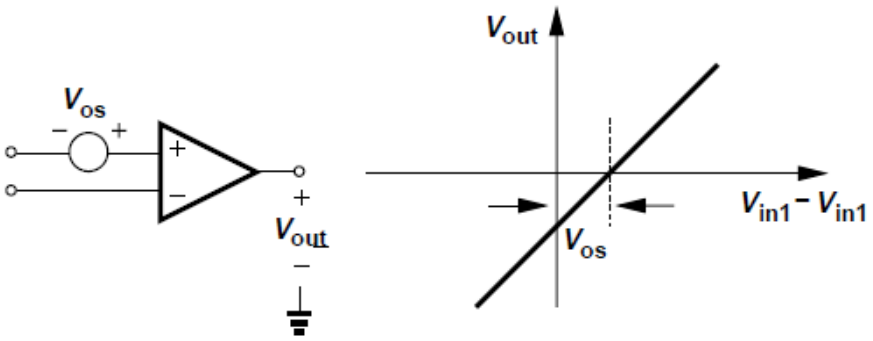

Figure 3-6 Offset in Opamp [36]

For a non-inverting amplifier, the close loop gain is given by

$$V_{out} = [1 + \left(\frac{R_2}{R_1}\right)].V_{in} \tag{8}$$

However, when offset voltage exists, the gain of amplifier is given by

$$V_{out} = \left[1 + \left(\frac{R_2}{R_1}\right)\right].(V_{in} + V_{os}) \tag{9}$$

Because of the change in DC level, the operation of input transistor of next stage will be affected. For an integrator the output voltage, when input is zero and offset voltage appears at non-inverting terminal, is given by

$$V_{out} = V_{os} + \int V_{os} . \left(\frac{1}{R.C}\right) dt \tag{10}$$

The offset voltages keeps on building up and eventually drives the Opamp into saturation. Hence, a simple offset compensation circuit is made using a potential divider network as shown in Figure 3-7.

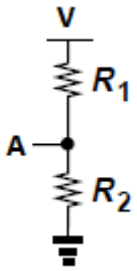

Figure 3-7 potential divider network

The offset voltage for the commercial component is 5mV. Hence, the resistor values are chosen such that 5mV voltage occurs at node A. This will prevent saturation of the amplifier and the circuit can exhibit memristive behavior. A train of pulses is applied to the input and it is expected that the conductance of device increases. The capacitor stores charge across it and as the number of pulses increase, the charge increases and hence voltage at the output of integrator increases as seen in Figure 3-8.

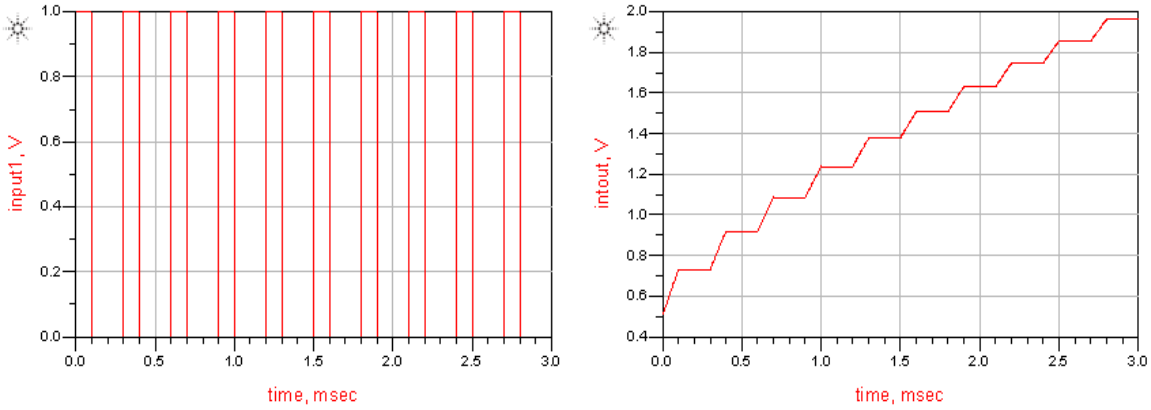

Figure 3-8 Pulse train test

3.2 CMOS IC Implementation

The proposed memristor emulator circuit is designed and implemented in 0.18um CMOS process. This section includes design and analysis of Opamp and multiplier circuit. Simulation results are compared with block level simulation and with existing memristor emulator circuits.

3.2.1 Opamp

Two stage Opamp topology has been used for design of the Opamp. For the design, high gain and output swing are critical for memristor emulator circuit. Because of high gain, the gain error due to feedback reduces. The telescopic cascode Opamp provides a high gain due to cascade of transistors. However, the output swing is very poor due to stacking of transistors, causing the overdrive voltage to limit the voltage swing. Folded-cascode amplifiers provide high gain and equally large output swing. The main disadvantage of it is higher power consumption, due to additional bias current of the folded structure [36].

The two stage Opamp provides high gain and sufficient bandwidth for the current application. The amplifier can be used as a buffer, by shorting the output and the inverting terminal, an advantage over telescopic cascode. The amplifier generates large voltage swings and utilizes entire voltage headroom. Though this topology provides low speed, it has moderate power dissipation. Specifications for the Opamp are as shown in table 3.

Table 3-2. Opamp specifications

Gain	=>90 dB
Bandwidth	>3MHz
Output swing	±0.7V
Slew rate	13V/us

Figure 3-9 shows the Opamp schematic. It consists of a differential amplifier with current mirror and a common source amplifier as the output stage. The differential amplifier provides high gain and the CS amplifier provides high output swing.

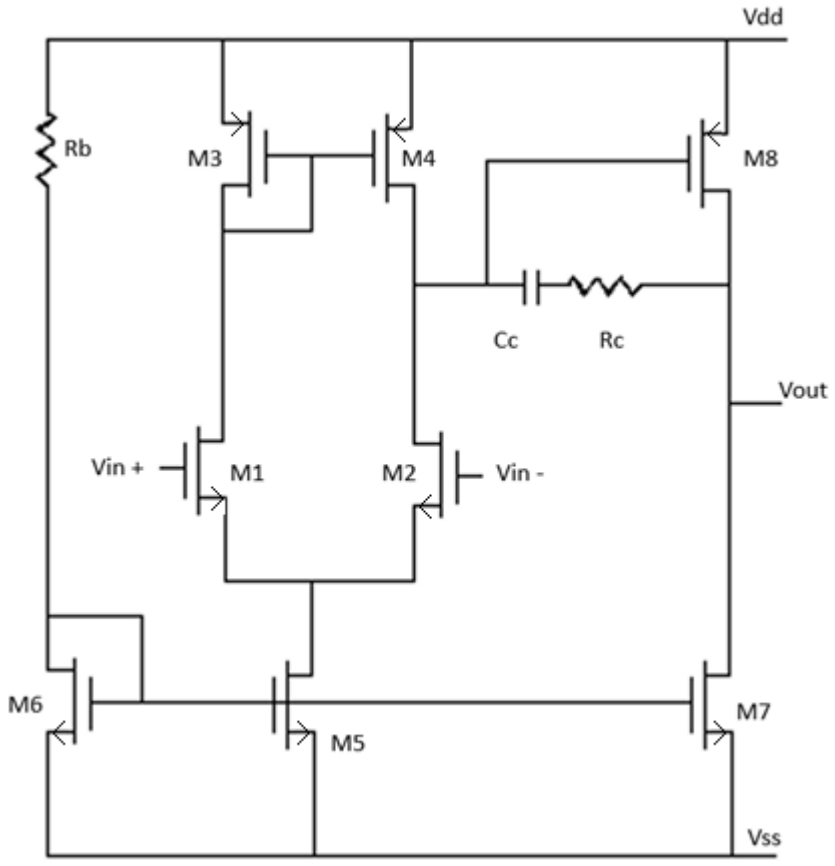

Figure 3-9 Two stage Opamp schematic

For the differential stage, NMOS devices are used as input pairs. Due to higher mobility, NMOS input pair provide higher gain and lower noise compared to PMOS input pairs. The open loop gain of the Opamp is the multiplication of gain of differential stage and gain of common source amplifier, which is given by

$$A_{total} = A_1 . A_2 \tag{11}$$

$$A_V = ((2. g_{m1} . (r_{o1} || r_{o3})) . (g_{m8} . (r_{o7} || r_{o8})) \tag{12}$$

For a circuit to work as an amplifier, the transistors must operate in saturation region. Hence, the biasing of transistors is important to achieve high gain and voltage swing. The Resistor Rb and transistor M6 form the biasing circuit for the amplifier. The channel length is larger than the width of the device to reduce the bias current consumed and to increase gain, CMRR (common mode rejection ratio) and PSRR (power supply rejection ration).

Transistor M5 acts as a tail current source for the differential pair. The channel length of M5 is comparable to the width because the transistor has to provide larger current to the differential pair. Also, the amount current flowing through the differential pair determines the transconductance of the device g_m, which is given by

$$g_m = \sqrt{2. k' . \left(\frac{W}{L}\right) . I_D} \tag{13}$$

Higher the value of g_m, higher is the gain of the amplifier. Also, increasing the channel length of M5 leads to higher CMRR of the amplifier and reduce effects due to process variations. The minimum output voltage is given by the overdrive voltage of transistor M7, which is given by

$$V_{out\,min} = V_{ov} = \sqrt{\frac{2.I_{D7}}{u_n.C_{ox}.(\frac{W_7}{L_7})}} \quad (14)$$

When designing the amplifier, the output swing is assumed such that the overdrive voltage of transistors is small. Operating at smaller overdrive voltage, higher gain and CMRR can be achieved. The device dimensions of MOS transistors are chosen to maximize the gain and reduce errors due to mismatches. Transistors M1 and M2 form the input differential pair. The transistor's width is chosen to be high to increase the gain of the amplifier. Transistors M3 and M4 are active load devices which offer higher resistance due to being operated in saturation region.

Rc and Cc are compensation elements which determine the location of the dominant pole. Cc is the miller capacitance, which exists in parallel with the signal flow path, and by applying miller's theorem, the capacitance is split and a part of it, which is multiplied by the gain of differential, appears at the input of the second stage circuit. Hence, the resistance at the input of second stage is given by Rc and input impedance of second stage, and the capacitance at the input of second stage is given by Cc ($1+A_V$) and the gate-drain capacitance of transistor M7, C_{gd7}. These two elements, Rc and total capacitance at input of second stage, determine the dominant pole of the amplifier. Smaller the value of Cc and the dimension of transistor M7, lower is the total capacitance and hence the dominant pole frequency is higher. Hence, a larger bandwidth can be achieved. Transistor M8 is the input transistor for the CS stage. The width of it is chosen high for providing higher gain. Transistor M7 is chosen to have higher width compared to M5 for higher current through the transistors and to achieve

higher output swing. An inverter stage, made of nmos and pmos, can be added at the output stage to provide rail to rail swing. But it provides higher capacitance and the bandwidth is affected due to large transistor sizes.

The output impedance and gain of second stage is given by

$$r_{out} = g_{m8}.r_{o8}.r_{o7} + r_{08} + r_{07} \tag{15}$$

$$A_2 = \frac{g_{m8}}{g_{ds8}+g_{ds7}} \tag{16}$$

The designed Opamp achieves a gain of 89.3dB and a bandwidth of 3.67MHz. Minimum input voltage should be higher than the threshold voltage of transistor M1/M2 and the overdrive voltage of transistor M5. The frequency response of the circuit is shown in Figure 3-10.

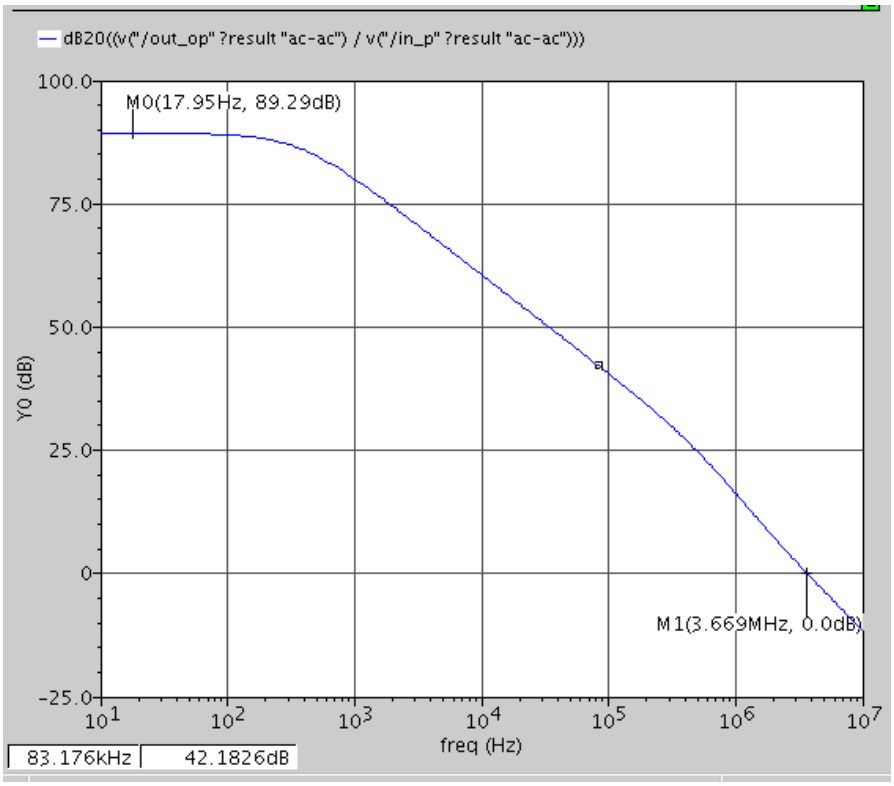

Figure 3-10 Frequency response of Opamp

To check the output swing of the circuit, a buffer amplifier is made by shorting the output and the inverting terminal. The input voltage applied to non-inverting terminal and it is swept from -2V to 2V. The output varies from -744mV to 840mV and the total swing is 1.584V.For the supply voltage of 1.6V, the Opamp achieves very high output swing. The output swing of Opamp is shown in Figure 3-11 below.

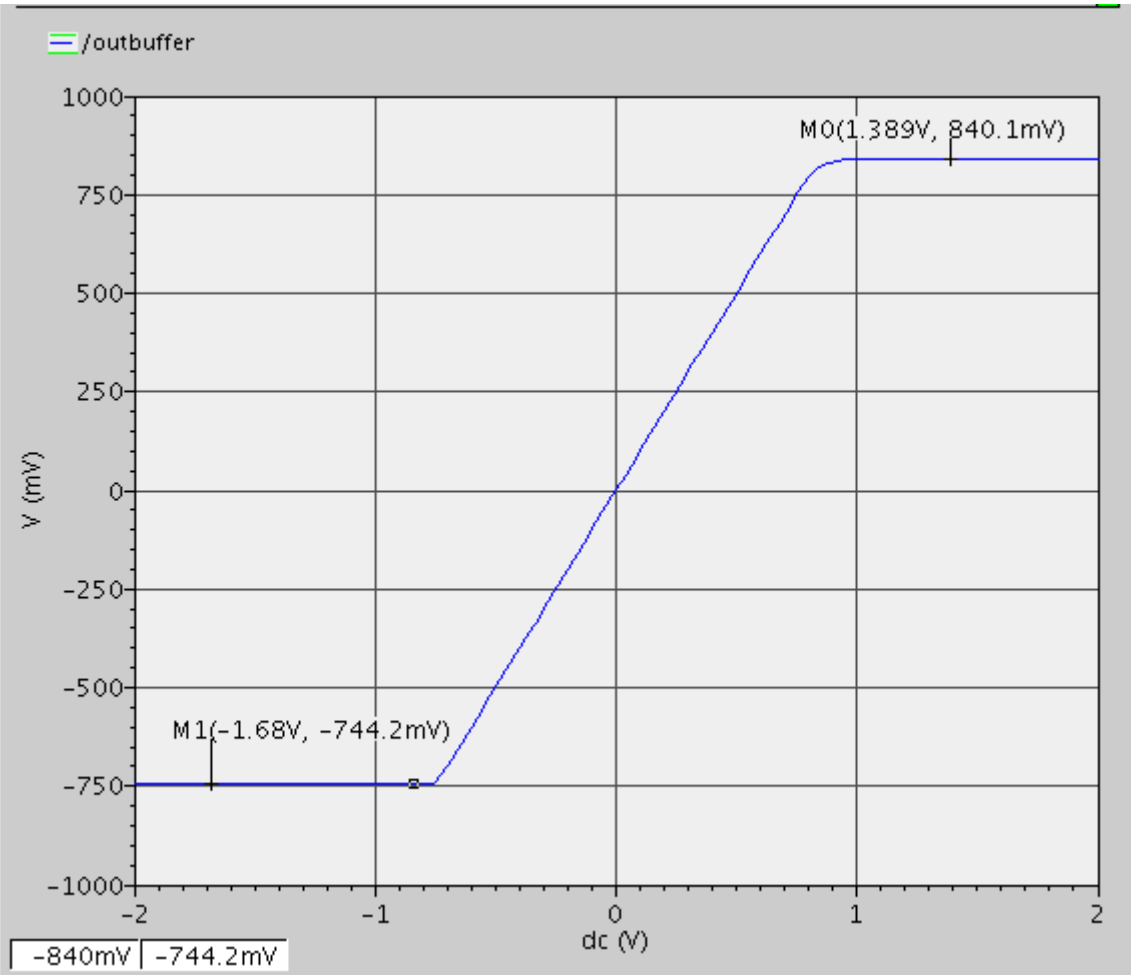

Figure 3-11 output swing of Opamp

The Opamp performance parameters from schematic simulation are summarized in table 4 as shown below.

Table 3-3. Summary of Opamp performance parameters

Parameter	Value
Power supply	±0.9V
Gain	89.3dB
3dB bandwidth	394Hz
Unity gain bandwidth	3.67MHz
Output swing	1.584V

3.2.2 Multiplier

The analog multiplier for emulator circuit is realized using Gilbert cell architecture. It consists of three NMOS differential pairs and a pair of NMOS active load devices. For the upper input pairs, the output of integrator is applied and to the bottom pair, the output of summing amplifier is given. The tail current source is realized by using a current mirror, realized by transistors M9 and M10. The circuit has been designed for maximum output swing. The purpose of using nmos differential pairs for inputs is because of higher mobility of nmos and better noise performance. The schematic of the circuit is shown in Figure 3-12.

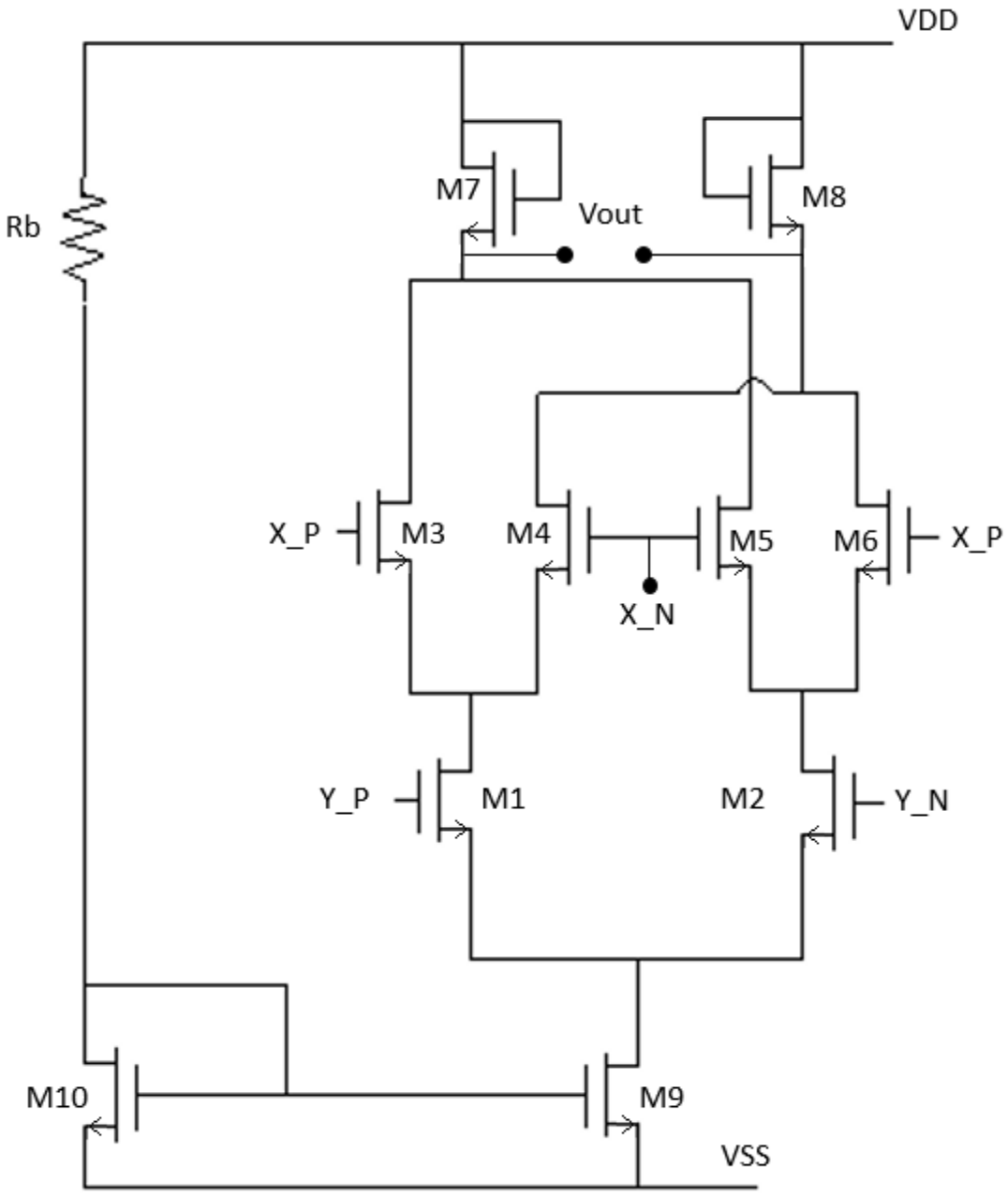

Figure 3-12 Gilbert cell multiplier schematic

Transistors M9, M10 and resistor Rb form the biasing circuit for the multiplier. The transistor size of M9 is chosen larger, in order to maximize the current flowing through the differential pairs. Transistors M1-M9 have same transistor sizes, with M7

and M8 acting as active load devices. All the devices follow the square law and the working principle is explained as follows.

By applying KCL, the output current is given by

$$I_{out} = (I_3 + I_5) - (I_4 + I_6) \quad (17)$$

$$I_{out} = (I_3 - I_4) - (I_6 - I_5) \quad (18)$$

On substituting square law current equations for pairs M3-M4 and M5-M6 with I_{y1} and I_{y2} respectively, we get

$$I_{out} = kV_x\sqrt{\frac{2I_{y1}}{k} - V_x^2} - kV_x\sqrt{\frac{2I_{y2}}{k} - V_x^2} \quad (19)$$

Assuming V_x is small and on further calculations, the final relation between I_{out}, V_x and V_y is given by

$$I_{out} = \sqrt{2}kV_xV_y \quad (20)$$

Figure 3-13 a) shows the response of the multiplier circuit. The output is plotted with respect to inputs V_x and V_y. First V_x is assumed to be 0.8V and V_y is swept from -0.6V to 0.6V. Then, V_x is swept for a range of voltages along with dc sweep of V_y, which is shown in Figure 3-13 b). From the results, it can be seen that multiplier circuit works well for voltages below he supply rail. When voltages above the supply are applied, the multiplier response saturates and shows rail voltage as output voltage.

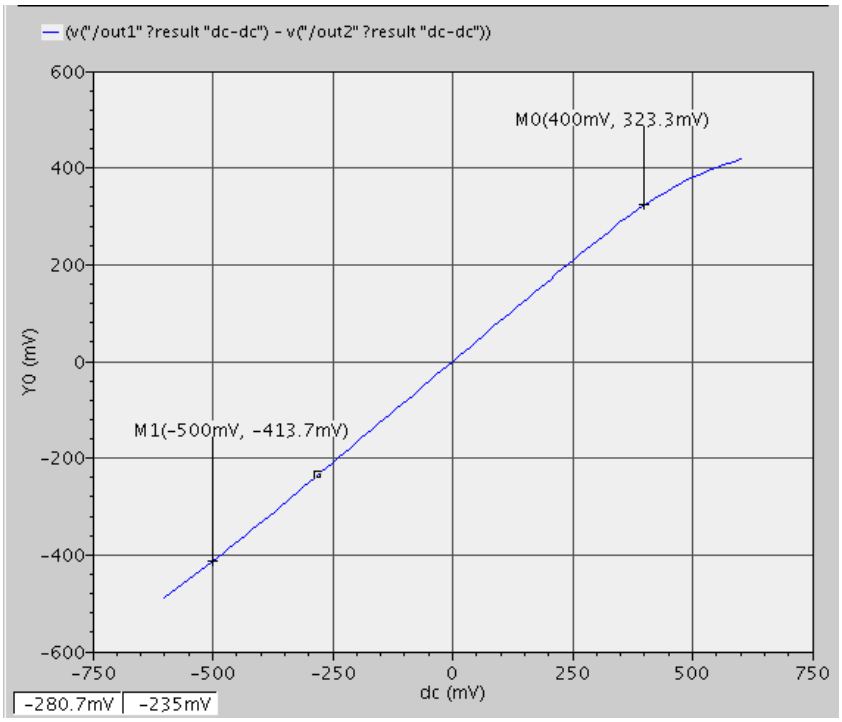

Figure 3-13 a) dc sweep of V_y

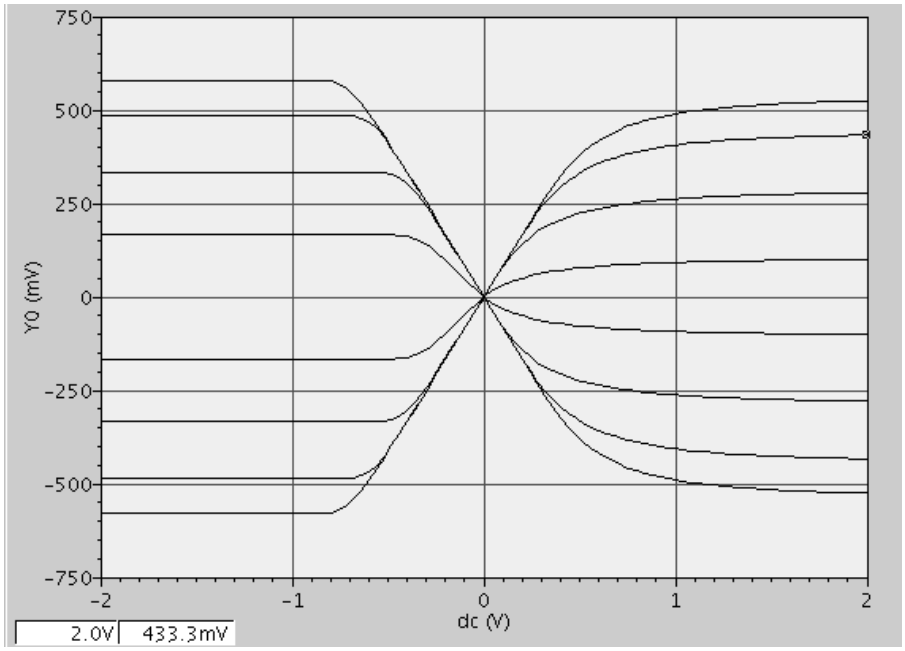

Figure 3-13 b) sweeping both the inputs V_x and V_y

Since the multiplier inputs are differential, inverters have been added at the inverting inputs. Hence, four quadrant operation of the circuit is achieved. The multiplier output is taken from two different nodes. Hence, a simple double to single amplifier is used to generate the single ended output signal for the feedback to summing amplifier inverting input. Since no amplification of the signal is required, transistors of minimum sizes are used to this circuit. In addition, the parasitic capacitance is lower because of small dimensions of the transistors. The circuit is shown in Figure 3-14.

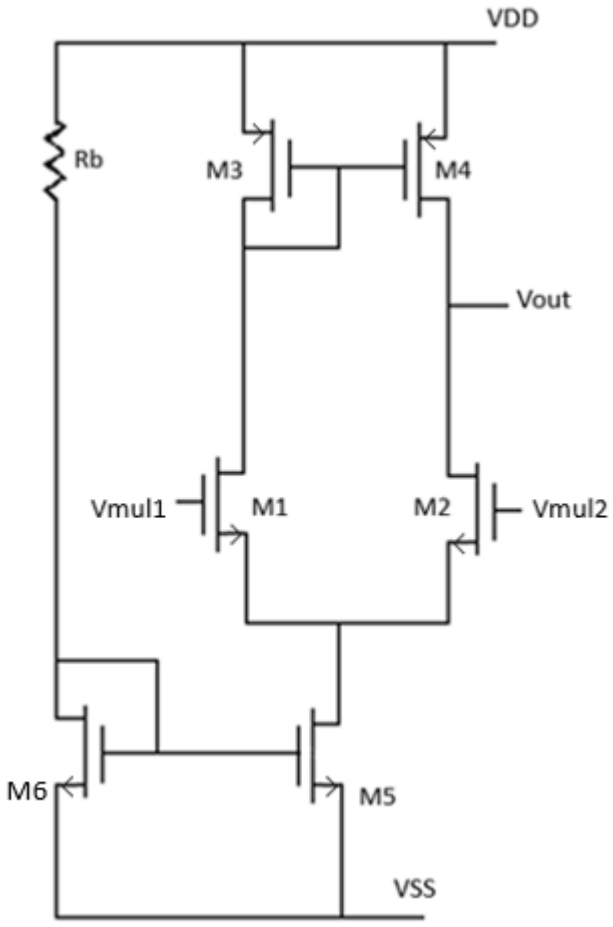

Figure 3-14 Double to single ended circuit

The complete schematic of emulator circuit, implemented using CMOS process is shown in Figure 3-15. All the designed components in the circuit operate at ±0.9V and a sinusoidal signal of amplitude 0.6V is applied to the input of emulator circuit.

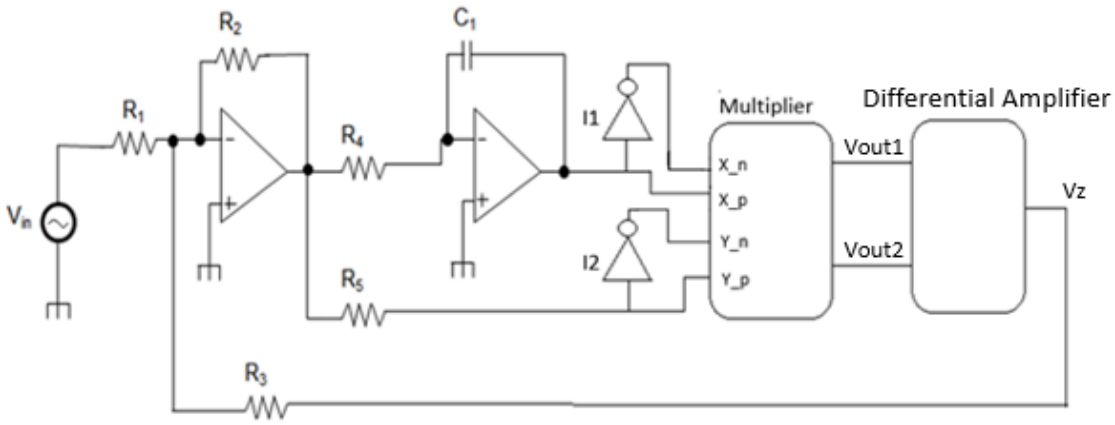

Figure 3-15 complete cmos circuit schematic

As expected the circuit exhibits memristive behavior and as the frequency increases, the pinched hysteresis falls to a straight line as seen in Figure 3-15 a) and 3-15 b) respectively.

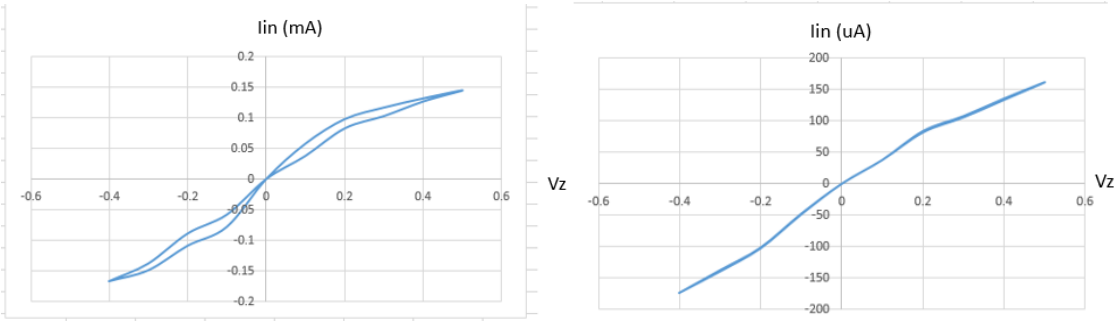

Figure 3-16 a) circuit behavior at low frequencies and b) higher frequencies

Following set of figures show the comparison of results between ADS block simulation and circuit, implemented in 0.18um CMOS process, for different frequencies.

1) Vin = 0.6V and frequency = 1KHz

ADS Block implementation:

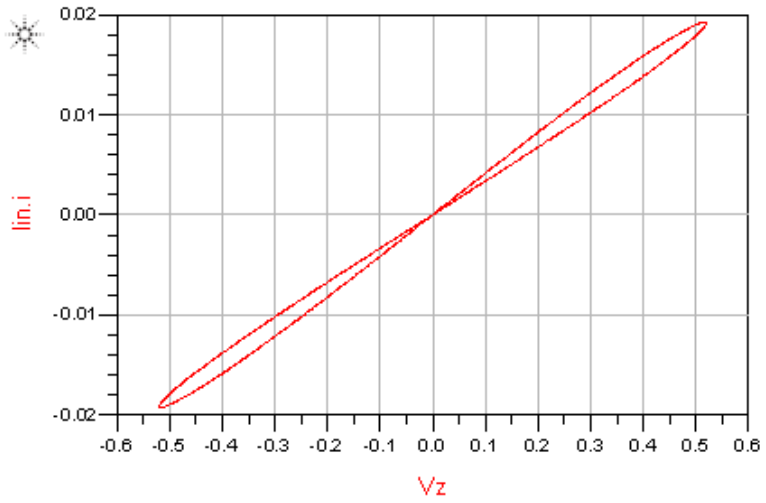

Figure 3-17 pinched hysteresis at 1KHz

CMOS Implementation:

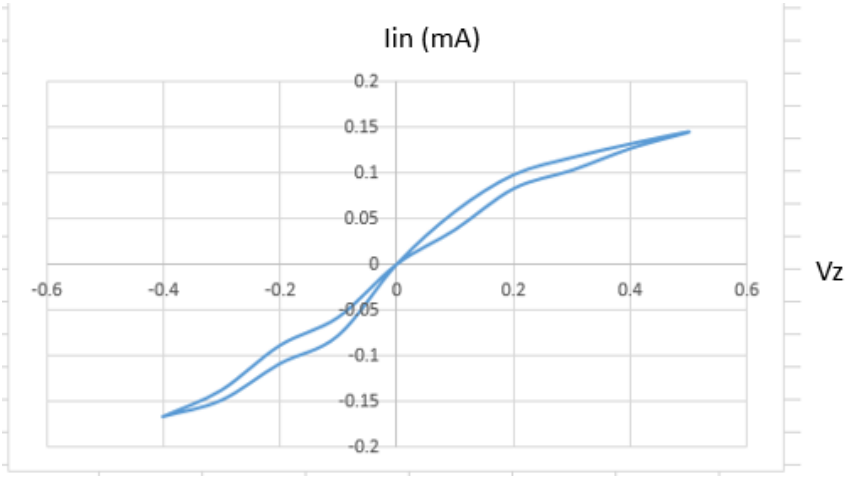

Figure 3-18 pinched hysteresis at 1KHz

2) Vin =0.6V and frequency = 2KHz

ADS Block implementation:

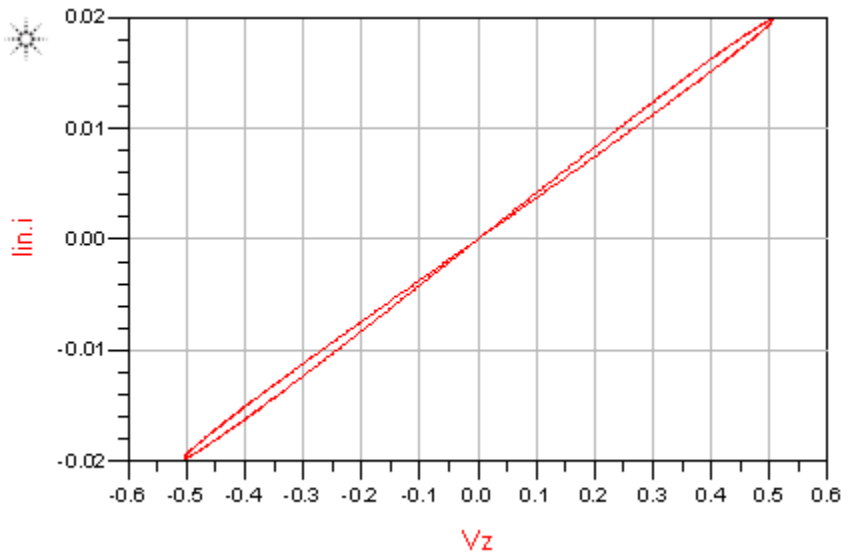

Figure 3-19 pinched hysteresis at 2KHz

CMOS Implementation:

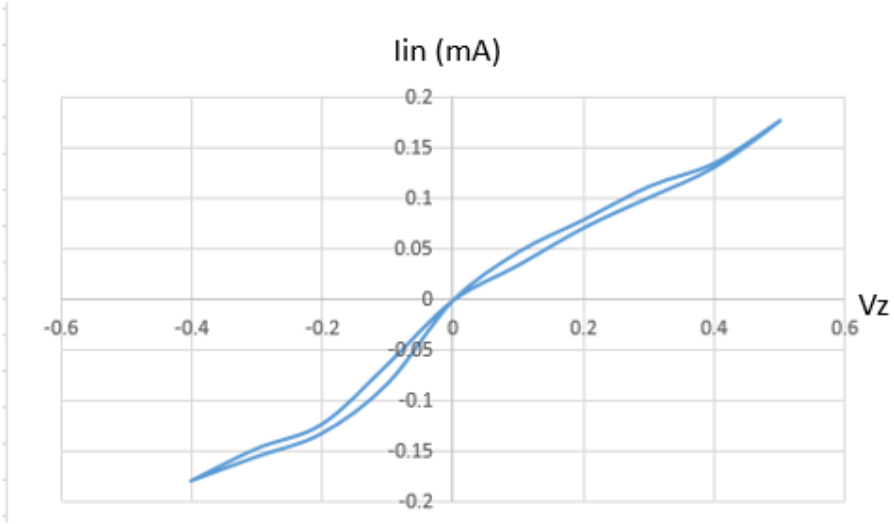

Figure 3-20 pinched hysteresis at 2KHz

3) Vin =0.6V and frequency = 4KHz

ADS Block implementation:

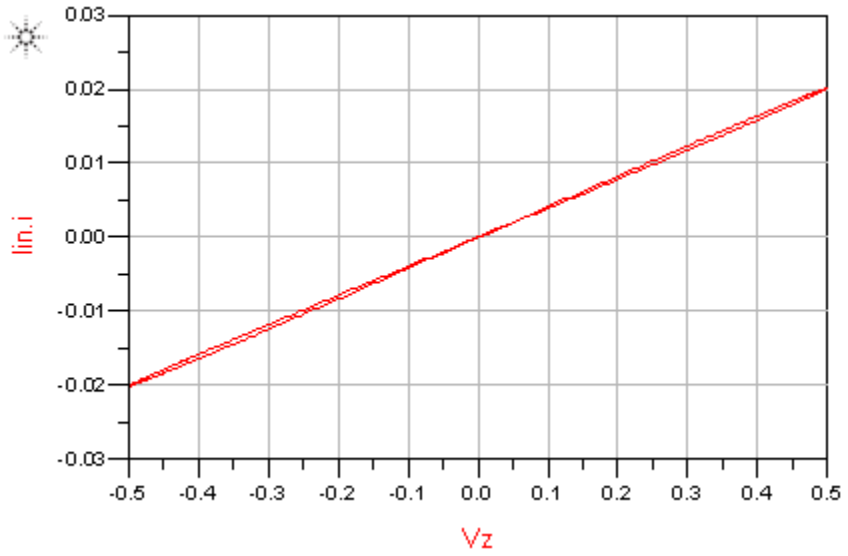

Figure 3-21 pinched hysteresis at 4KHz

CMOS Implementation:

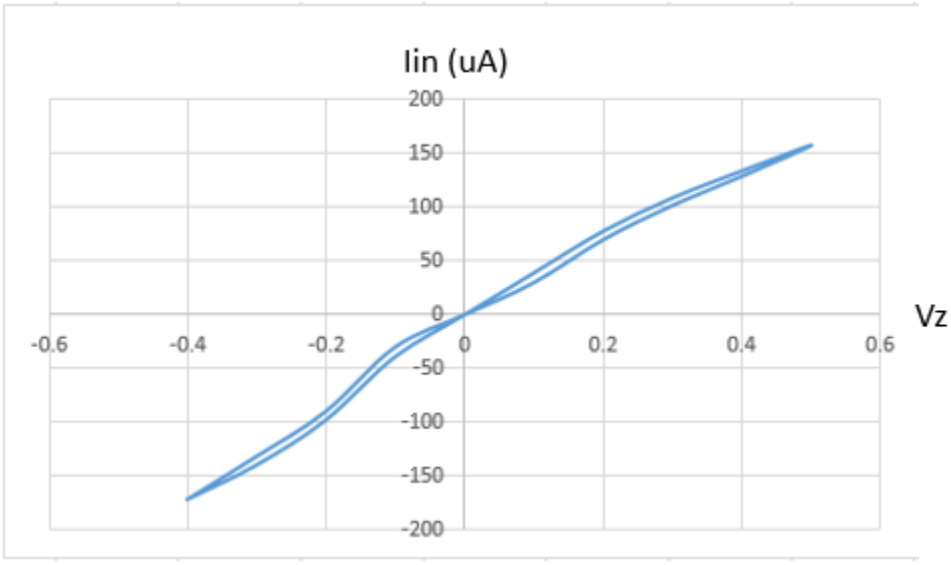

Figure 3-22 pinched hysteresis at 4KHz

4) Vin =0.6V and frequency = 8KHz

ADS Block implementation:

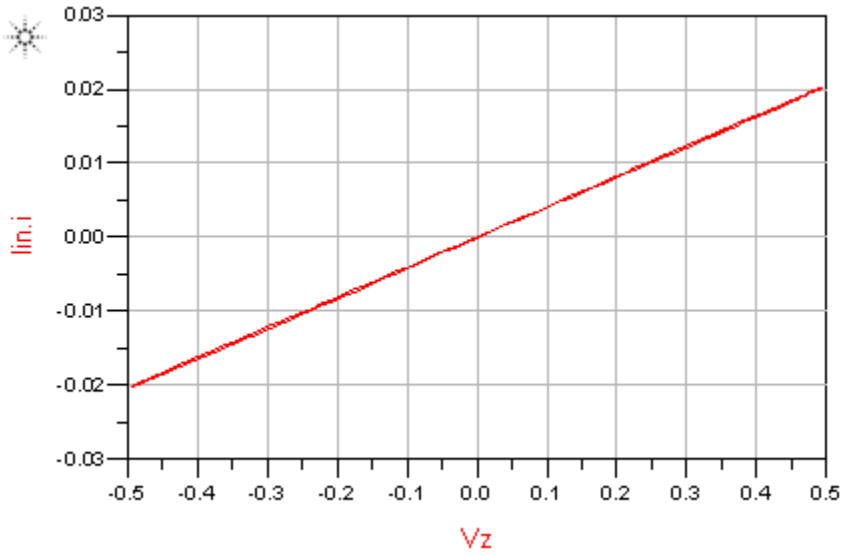

Figure 3-23 pinched hysteresis at 8KHz

CMOS Implementation:

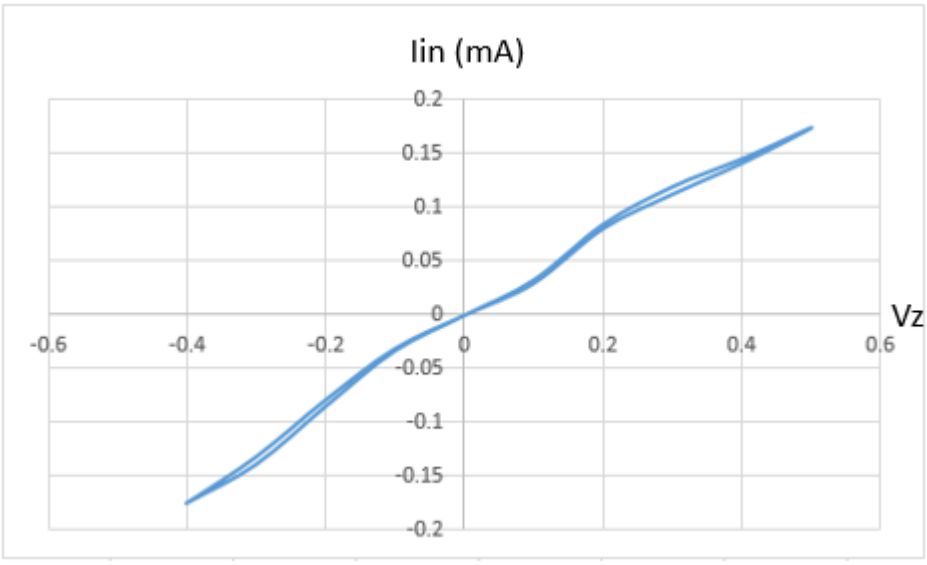

Figure 3-24 pinched hysteresis at 8KHz

5) Vin =0.6V and frequency = 16KHz

ADS Block implementation:

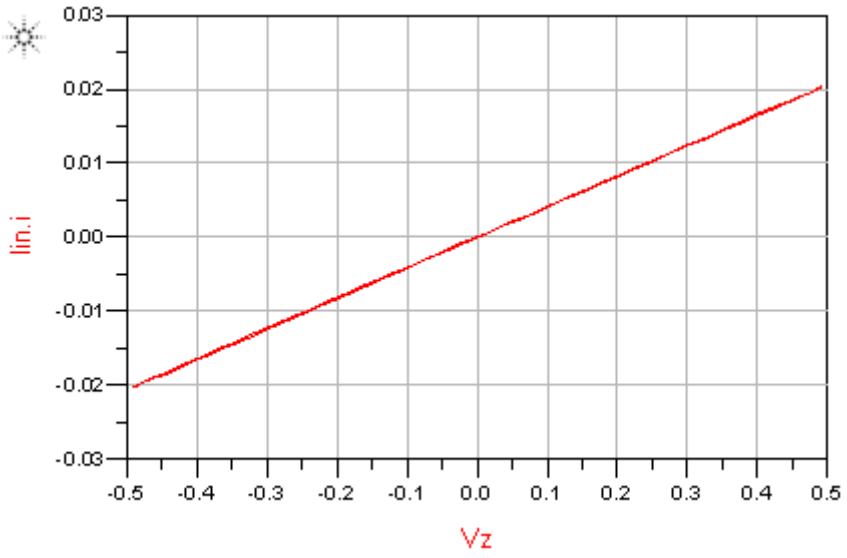

Figure 3-25 pinched hysteresis at 16KHz

CMOS Implementation:

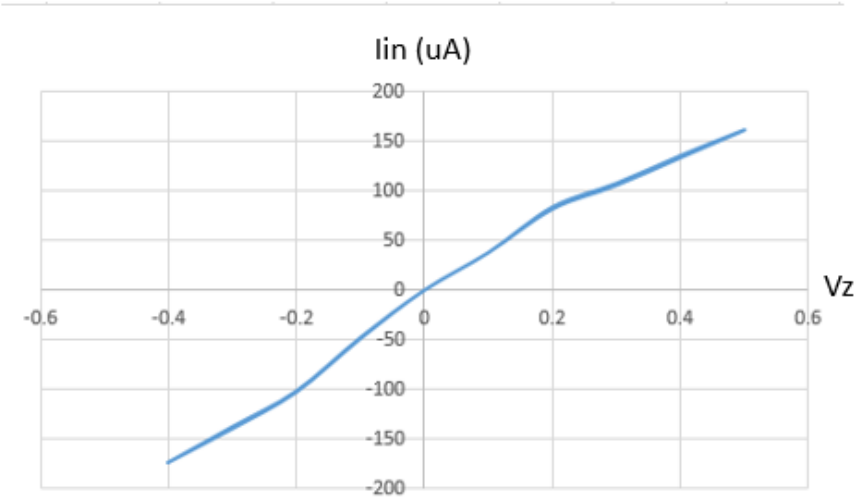

Figure 3-26 pinched hysteresis at 16KHz

Hence, the cmos circuit behaves similar to the circuit implemented using commercial components. At 16KHz and higher frequencies, the circuit behaves as a resistor. Table 5 shows the comparison of above designed circuit with the existing emulator circuits.

Table 3-4. Comparison with existing architectures*

Sr. No.	Supply	Hysteresis Frequency
[30]	±15V	280Hz
[31]	±15V	2Hz
[28]	±2.5V	50Hz
[29]	±15V and ±5V	800Hz
This work (ADS simulation)	±15V	16KHz
This work (CMOS implementation)	±0.9V	16KHz

* - All the circuits implemented are based on TiO_2 based memristor. Memristors based on silver chalcogenide [7] and solution processed memristors [12] have been fabricated but they do not have fast switching characteristics compared to original semiconductor model.

Chapter 4

Conclusion

In this thesis, simple, low power, high frequency memristor emulator circuit has been proposed. The purpose is to mimic the behavior of memristor, the fourth passive element. The circuit consists of summing amplifier, integrator and a multiplier. The integrator forms the core of emulator circuit by adding up the signals that have been applied to its input. The multiplier's purpose is to multiply the outputs of summing amplifier and integrator, resulting in quadratic relation between current I_N and voltage V_Z.

For ADS block level simulation, commercial off the shelf (COTS) components have been used. The frequency at which the memristor emulator behaves as a resistor is 16 kHz. The Opamp (TL082CP) and multiplier (AD633ANZ) require a dual supply of $\pm$15V. Resistor R_4 and capacitor C_1 determine the frequency band of operation.

For CMOS implementation, the circuit has been designed using IBM 0.18um technology. Two stage Opamp topology has been chosen for design of Opamp due to low speed, high output swing and high gain requirement. The multiplier has been implemented using a four quadrant Gilbert Multiplier cell. The circuit operates at a VDD of $\pm$0.9V and the highest frequency up to which memristive behavior is observed is 16 kHz. The results are consistent with the block level simulation. The simulation has been performed in Cadence Spectre environment.

For future work, it is intended that a chip for memristor emulator is made. The purpose is to use it for compensation of process variations in amplifiers [27].The chip can be used in fine programmable resistors and variable gain amplifiers [13], whose gain can be programmed to a specific value by applying a train of pulses.

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