A SWITCHED CAPACITOR BASED TRANSIMPEDANCE AMPLIFIER FOR DETECTION OF HAB THROUGH OPTICAL SENSING

by

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April 21, 2016

Abstract

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In the recent years, there has been a substantial increase in the manifestation of harmful algal blooms. A certain species called cyanobacteria that is commonly present in freshwater bodies are found to release a class of deadly toxins known as microcystin. This toxin poses a threat to humans and wildlife since they can cause severe illness or even death on consumption of contaminated water.

Traditional sampling methods are essentially lab based detection methods that are inconvenient and demands extensive manual effort. Hence, large-scale occurrence of harmful blooms in water resources demands the development of efficient and reliable methods for monitoring and detection of harmful algal blooms through remote sensing.

In this thesis work, an optical sensing readout circuit has been discussed for a lab-on-chip system that can remotely detect and report the presence of a deadly toxin known as microcystin-LR released by a species of harmful algal bloom. Since a transimpedance amplifier is an integral block of the optical sensing readout circuit, a low power, low noise switched capacitor based transimpedance amplifier design has been proposed for the optical sensing readout circuit. It has been designed in cadence using an operational amplifier and a logic control circuit in 0.18um CMOS technology.

The simulated results of the proposed design show a low power consumption of 7.2uW with a high transimpedance gain of 121.3 dB ohm. A low input referred noise of 65.59fA/$\sqrt{Hz}$ could also be achieved through correlated double sampling. This design is more compact, less noisy and less power consuming as compared to existing architectures and thus is best suited for the portable optical sensing system for detection of harmful algal blooms.

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Chapter 1

Introduction

1.1 Motivation

One of the most important environmental crises that humanity faces today is the constant increase in contamination of water bodies by industrial waste and other natural toxic phenomenon prevalent on a world-wide scale. Statistics show that close to 3 billion people do not have clean and safe drinking water. Also, about 35% of deaths in developing countries are attributed to this [5]. Approximately 1.8 million deaths occur due to illness arising from use of unclean water of which the majority is children in developing countries [5].

Though it has been predicted that consumption of water around the world would double in the next 20 years, ensuring the quality of water is still undervalued. This poses an important threat to global health [5]. There is a necessity to study and understand the behavior of cyanobacterial blooms since it plays a major role in public health [3]. It has become a major concern since water bodies face continuous eutrophication.

The water distribution system is defenseless against deliberate as well as unintended contamination of water bodies. Though there have been many technological advances; extensive work remains to be undertaken for the decontamination of water.

Although some issues have been prevalent for a long time they have recently become critical while few other issues have newly evolved. Irrespective of the cause, there is a need for the water industry to intensify its control. Moreover there is also need for a better understanding of the problems faced by water resources in a real-time scenario. This aids in gaining quintessential information that will help authorities to categorize and recognize changes in water qualities over time and also identify new threats to water quality.

Traditional sampling methods at discrete locations are a tedious procedure thus an effective way of monitoring is through remote sensing. Remote sensing through satellite monitoring is inefficient since there is no adequate spatial resolution. Other similar techniques to remotely monitor include use of air-borne devices which face the same limitations. Thus, there is a need for a less expensive, reliable and high-precision method to detect the presence of these harmful toxins.

Due to inconsistencies and variations pertaining to the optical properties of waterbodies, it is unfeasible to develop a single, all-inclusive algorithm for detecting and mapping algal bloom. It would be quite a complex process hence we narrow the detection to one kind of toxin which is the microcystin leucine-arginine (MC-LR) [4].

This work focusses on detection of a specific toxin called the microcystin leucine-arginine (MC-LR). This toxin comes under the classification of hepatotoxins. The detection of the microcystin leucine-arginine (MC-LR) toxin is done using an optical

sensor. A few desired features in the optical sensor include capability of functioning autonomously, real-time in situ monitoring and integrable on lab-on-chip system. The presence of MC-LR antigens can be detected by means of an optical sensor. The optical sensor comprises of a periodic nano-hole array structure which exhibits the phenomenon of enhance optical transmission. The surface of the nanostructure behaves as a bio-transducer layer containing immobilized antibodies [2].

The principle behind this is that a specific protein structure called antibodies tends to bind with a specific target molecule called the antigen. A label is produced when an antibody binds with an antigen. The sensor developed for the detection of MC-LR comprises of immobile antibodies and binds with the antigen which is MC-LR in this case [2].

The idea is to design a lab-on-chip system that is capable of detecting a specific toxin known as the microcystin leucine-arginine (MC-LR) produced by a specific species of algal blooms. The lab-on-chip system includes an optical sensor capable of detecting MC-LR and an optical sensing readout circuit. Since the sensor is designed to detect a single form of toxin, a thorough analysis of the contamination of a water source can be performed. By employing this lab-on-chip system a waterbody could be actively scanned for toxins in situ and it is possible to receive information of any immediate threat.

1.2 Readout circuit

Figure 1.1 shows the readout circuit for the optical sensing circuit. The readout circuit system takes in the light from the optical sensor and processes it to give an equivalent readable voltage value that could be utilized for further processing.

The photodetector takes in light from the optical sensor and converts optical power to photocurrent. The transimpedance amplifier block converts the photocurrent signal to an equivalent voltage signal based on the transimpedance gain. It is followed by a post amplifier block that further amplifies the voltage signal to bring it to the input voltage range of the ADC block. The ADC block produces the digital equivalent to the analog voltage signal so that it is suitable for further processing.

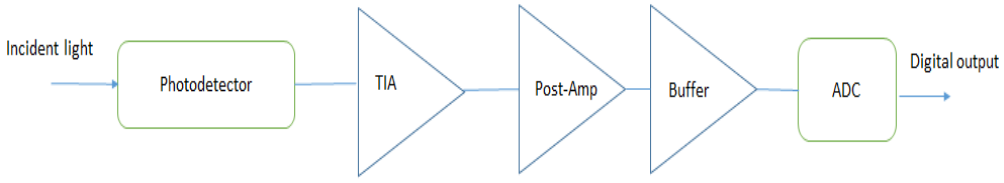


Figure 1-1 Block diagram of readout circuit

One of the integral blocks is the transimpedance amplifier block. This work proposed a better performing transimpedance amplifier design for the optical sensing readout system. The most commonly used architecture is the resistive feedback transimpedance amplifier. Though this architecture is simple and widely used in discrete circuits it is unsuitable for integrated circuit design due to drawbacks such as large area,

large power consumption and considerable thermal noise added by the feedback gain resistor.

The proposed switched capacitor based transimpedance amplifier design has compatibility with CMOS technology, high accuracy and good linearity. It has other desirable features such as low noise and low power that makes it a more superior choice in the current era of digital systems where there is need for minimal power consumption. The switched capacitor based transimpedance amplifier is capable of discretizing the measurement making it easier for signal processing and moreover power can be conserved since it is based on a switching system. In this work, the proposed design is compared with a conventional transimpedance amplifier which is the common gate amplifier to compare and contrast the performance parameters, namely, power, noise, gain etc.,

The proposed switched capacitor based transimpedance amplifier is best suited for the readout circuit of the optical sensing circuit since it provides a low power, low noise feature that enables realizing a lab-on-chip platform for detection of harmful algal blooms.

1.3 Outline

The thesis work is structured into the following sections-

Chapter 1 discusses the inspiration behind this thesis work, the devastating effects of eutrophication of water sources and the imperative need for an efficient

detection system. It briefly describes the readout circuit for optical current sensing and the benefits of the proposed work as compared to the existing work.

Chapter 2 explains in detail about the toxin Microcystin-LR (MC-LR), different MC-LR Detection Methods and concept behind the surface plasmon sensor. It focusses on the transimpedance amplifier block in particular and the principle behind it. It also briefly reviews some of the existing transimpedance amplifier designs.

Chapter 3 explains the block level design of the optical sensing readout circuit and the working of the commercial blocks simulated in ADS. It also discusses the design of the proposed switched capacitor based transimpedance amplifier. It justifies the performance of the proposed design through simulation and post extraction results. Also, compares and contrasts the performance of the proposed design with a conventional transimpedance amplifier design which is the common gate amplifier.

Finally, chapter 4 summarizes the overall design, analysis and the results of the proposed design. It concludes the thesis work with the contribution of the proposed design to improve the overall performance of the system and the future research work that could be performed to accomplish the idea of a complete lab-on-chip system for detection of harmful algal blooms.

Chapter 2

Background

Clean water suitable for human and wildlife consumption is an indispensable resource which is quintessential for continued sustainable development. However it is becoming increasing difficult to meet the growing needs to provide for the increasing population. Industrial development, agricultural run-off, natural phenomenon such as climate change and other such natural disasters are a significant threat to clean water supply [5]. The presence of harmful algal blooms has become a common occurrence worldwide due to increased eutrophication of surface water resources. A certain species of harmful cyanobacterial blooms are known to release poisonous toxins.

Among all of the cyanotoxins, microcystins are found to be the most toxic. Microcystins are cyclic heptapeptide hepatotoxins and in specific Microcystin-LR (MC-LR), where L and R stand for the amino acids leucine and arginine respectively, is found to be the most toxic and common [6]-[8] especially because these are highly soluble and chemical stable . Continued ingestion of microcystins can cause liver cancer and in larger quantities could be fatal [8]. The microcystin-LR is highly detrimental to public health and the World Health Organization (WHO) has established a limitation of 1 μg/L of MC-LR in drinking water [8]. Public as well as private sectors water distributers are required to follow this guideline. The quality evaluation methods of water parameters currently used are mainly laboratory based, require fresh supplies of chemicals, trained

personnel and are time consuming [5]. There is a rising demand for simple, real-time and reliable methods for the detection of pollutants and contaminants in water. A more beneficial technique would be to employ remote detection and monitoring systems which includes, application specific sensors, instrumentation and signal processing [5].

The methods employed to detect water contaminants can be broadly classified into two categories, which are, traditional laboratory based methods and modern real time monitoring methods. Some of the commonly employed lab based methods include standard mass spectrometry, ion sensitive electrodes, UV-Vis measurement methods and amperometric sensors [5]. Modern real-time monitoring approaches include fiber optic sensors, electromagnetic wave sensors such as microwave sensors, lab-on-chip sensors, biosensors etc., [5].

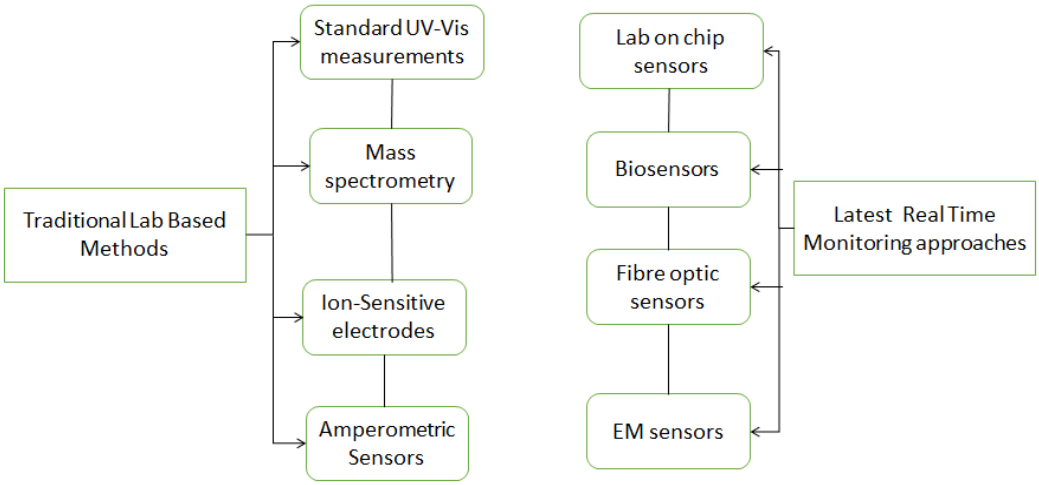


Figure 2-1 Different methods of detection

It is currently not possible for simultaneous detection of various water parameters by employing only one type of sensor. Both traditional as well as latest water monitoring methods do not have sufficient means for this. Novel application specific sensors need to be developed that are more robust, more sensitive and more accurate that allow acute detection of specific water pollutants with high reliability and minimum manual effort [5].

Another possibility would be to merge various technologies into a single system, an approach known as sensor fusion. This approach is the integration of the best available methods for the detection of different water pollutants that provide high sensitivity, long-term stability and at the same time enable real-time in-situ data collection [5].

The feasible monitoring system could consist of a system of sensors positioned at significant water bodies that are capable of autonomous operation [21] [5]. Such a system should meet a broad range of requirements such as portability, robustness, cost-effectiveness, long battery life, depending on the type of the sensors and the time period for monitoring [21] [5].

2.1 Existing MC-LR Detection Methods

The most accurate and commonly employed method for detection of Microcystin-LR is liquid chromatography paired with mass spectrometry. But the drawback of this method is that the sample preparation and the lab processing process is time consuming and tedious. This method also requires considerable equipment along with excessive operational cost [8]. Some of the biochemical detection methods include enzyme-linked immunosorbent assays, competitive enzyme immunoassays [12], [13], and protein phosphate inhibition assays [12], [13], [2].

Another method of detection that has been implemented is the optical fiber-based detection using fluorophore labelled biomolecules [2]. An example of commercially available assays would be the dipstick assays that are based on colloidal gold particles and lateral flow mechanisms [2]. The methods mentioned above have a low sensitivity since they are not quantifiable methods. One of the recent methods of detection of MC-LR is through optical detection, by utilizing surface plasmon sensor.

In the optical detection method employing surface plasmon sensor, the interaction between antigen and antibodies is detected through excitation of surface plasmon waves on the sensor surface. The setup comprises of a prism-based free-space [2]. But the drawback of this sensor is that it demands for precision control of the incident beam used for excitation of surface plasmon (SP) waves making the system larger in size and prone to mechanical noises [2].

2.2 Principle of surface plasmon sensor

The phenomenon occurs when a polarized light is incident on a conducting layer of gold present between a buffer and a sensing surface with a high refractive index under the condition of total internal reflection. When the light is incident on the glass an evanescent wave is produced. This wave interacts with free electrons in the gold layer and electron charge density waves are generated. These waves are called plasmons.

This phenomenon tends to reduce the power of the reflected light. The refractive index of the solution adjacent to the gold layer can be determined by finding the resonance angle at which the power of the reflected light falls to a minimum. The drawbacks of this process are the high operation cost and bulkiness. This phenomenon is generally employed to detect bio-molecular interactions that modify the resonance angle at the gold interface.

2.3 Periodic nanostructure based sensor for MC-LR detection

The optical sensor developed for the detection of MC-LR is an experimental setup for developing a lab-on-chip (LOC) sensing system used for real-time monitoring of MC-LR intensity in water resources on a large scale. This sensor is a label-free MC-LR detection in water at low part-per-trillion levels [2]. It comprises of a two-dimensional subwavelength nanohole array structure that exhibits extraordinary optical transmission. This phenomenon is sensitive to changes in refractive index of the medium surrounding the sensor [31].

The surface of the sensor comprises of immobile antibodies which behaves as a bio-transducer layer. When light is incident on the nanohole structure, the incoming photons are converted to excited surface plasmon waves. The excited waves are re-radiated into forward propagating waves. This excitation and re-radiation process is sensitive to surface condition. In an experimental setup, to test the working of the sensor, a known concentration of MC-LR is added to DI water. Since the bulk refractive index of DI water is 1.33 and the bulk refractive index of MC-LR is 1.42, when there is an interaction between the antibody and the antigen, the effective refractive index of the medium increases which shifts the transmission signal and is sensed by the biosensor.

A series of experiments were performed with varying concentrations of MC-LR in DI water to determine the limits of detection of this sensor. The intensity of the transmission signal was detected for different concentrations of MC-LR in DI water. It was found that greater the concentration of MC-LR, higher the effective refractive index of the medium and thus a larger shift in transmission intensity. As a result of this experiment, the detection limit of this sensor was found to be 10 ng /L [2].

2.4 Principle of Transimpedance amplifier

A transimpedance amplifier is used to convert an input current to an output voltage. This block is essential since the subsequent blocks in signal processing function with voltage and not current. Hence the current from the sensor needs to be converted

to equivalent voltage. A simple resistor can perform this operation with a transimpedance gain equal to its resistance value.

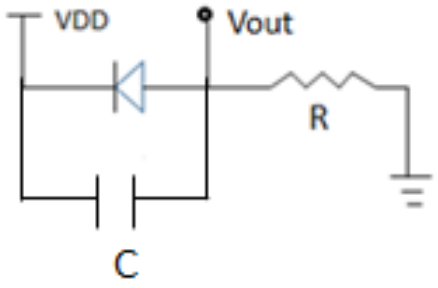


Figure 2-2 Basic transimpedance circuit

The drawback of this simple design is that the RC component introduces a trade-off between gain, noise and bandwidth. The transimpedance amplifier gain is directly proportional to the resistance R while noise and bandwidth are inversely proportional to R. There is a direct trade-off between noise - speed and gain - speed. Thus there is a need for a better design that ameliorates the trade-off.

2.5 Existing transimpedance amplifier design for optical sensing

1) Resistive feedback transimpedance amplifier - A basic design of a transimpedance amplifier is an operational amplifier with resistor and capacitor in the feedback loop. The transimpedance gain is dependent on the value of the feedback resistance. Figure 2.3 shows the resistive feedback architecture.

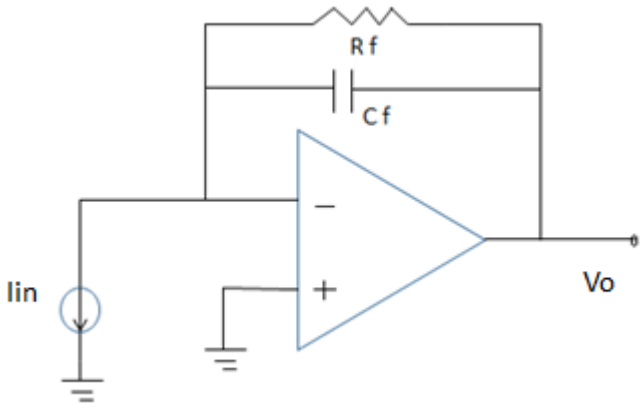


Figure 2-3 Resistive feedback TIA

For higher gain, there is need for a large resistance and at some point it may reach the limitations of component fabrication. To cancel out the effect of the zero introduced by the feedback resistance and input capacitance, a feedback capacitance is necessary to ensure stability. Few drawbacks are the error induced due to lack of accuracy in the fabrication of the resistor, large area and thermal noise.

2) TIA with active feedback - A transimpedance amplifier design is discussed in [24]. The design provides high sensitivity sensing of current from nano-device and other molecular systems. Figure 2-4 shows the transimpedance amplifier design with active feedback.

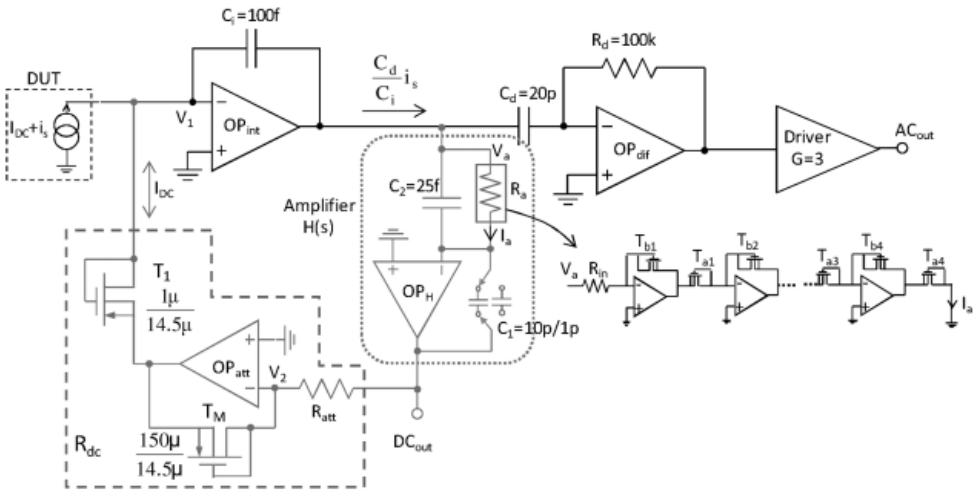


Figure 2-4 TIA with active feedback [24].

This design is based on integrator-differentiator arrangement with a feedback topology to reduce standing current. This design can be made use of to emulate very high resistances in the order of giga-ohms and still achieve high linearity and low noise performance. The design faces a drawback which is increased power consumption. This makes it unsuitable for temperature - sensitive applications.

3) DCF-TIA - A low noise and a high speed transimpedance amplifier design is discussed in [25]. This design is used for detection of reflected light from laser for the application of unmanned vehicles. Figure 2-5 shows the design of dual mode CMOS feed-forward TIA design.

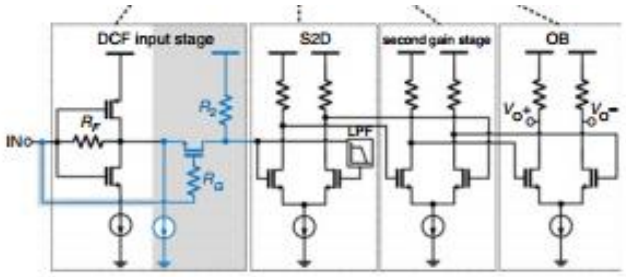


Figure 2-5 DCF-TIA [25]

It comprises of an inverter transimpedance stage with resistive feedback and a common gate amplifier with feed-forward input [25]. The gain of this modified inverter based transimpedance amplifier is double that of the conventional inverter based transimpedance amplifier. But this modified design maintains the input impedance and bandwidth as the conventional INV TIA design. This design manages to reduce noise as well.

The design achieves a transimpedance gain of 76dBohm. An average noise current spectral density of 6.4pA/$\sqrt{Hz}$ has been achieved for this design.

4) RCG-TIA with noise cancellation - A transimpedance amplifier design is discussed in [26] for detecting infra-red light for a medical application. It is used for monitoring the light transmitted from a patient's finger. The light from the monitoring sensor is converted to a range of voltage and further processed by an ADC. The design is a two-stage transimpedance amplifier with the first stage being a regulated common gate and the second stage being a parametric amplifier [26]. Figure 2-6 shows the transimpedance amplifier design.

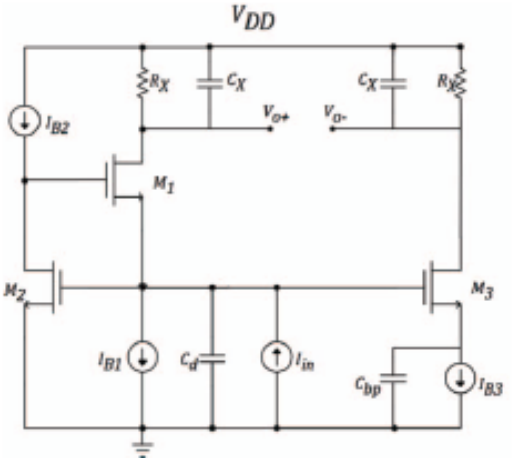


Figure 2-6 RCG TIA with noise cancellation [26]

The regulated common gate enhances the gain and the balun operation facilitates noise cancelling. This design was able to achieve power consumption lower than 250uW and a low input referred noise. Since the output is differential, the gain is doubled while the outputs are anti-phase so this enables effective noise cancelling.

Since the issue with the resistive feedback based transimpedance amplifier is the need for large resistors which lead to a large area and are prone to fabrication limitations, the “switched capacitor” concept is used for imitating these large resistance values using smaller capacitances. This concept is very useful in realizing transimpedance amplifiers. The switching mechanism provides a way to reduce power consumption in the circuit and also cancel offset in amplifier or unwanted low frequency noise components by making use of correlated double sampling.

Chapter 3

Switched Capacitor based Transimpedance Amplifier

The need for low power, low noise circuits has become crucial due to high device density, high operating frequency, need for portability and concerns regarding environment & power conservation. The preceding chapters discuss the prominent features of the switched capacitor based transimpedance amplifier. The switched capacitor based transimpedance amplifier has high precision, high linearity, CMOS integratable and is highly suitable for Lab-on-chip type of systems. They also offer desirable features such as low power and low noise. Thus the design of a switched capacitor based transimpedance amplifier has been proposed for the readout circuit of the optical sensing system.

3.1 Board Level Design

A readout circuit was designed using the EDA tool, advanced design systems to model the PCB. The purpose was to model the behavior of the optical sensing readout circuit which is to convert the optical sensing current to equivalent voltage for further processing. Figure 1.1 shows the block diagram of the readout circuit.

3.1.1 PIN Photodetector

The photodetector is expected to receive a minimum 1.74uW of optical power and produce 1μA of current. The component FDS1010 by Thorlabs is chosen for this since it is best suited for measuring pulsed light sources, to convert optical power to an equivalent electrical current. Following table enumerates the electrical characteristics of the photodiode.

Table 3-1 Electrical characteristics of FDS1010 [27]

Spectral Response	400-1100 nm
Bandwidth	8 MHz
NEP @ 900nm	5.5 x 10-14 W/$\sqrt{Hz}$
Dark current	600nA max (5V)
Junction capacitance	375pf @ 5V
Package	0.45 " X 0.52"

The anode of the photodiode generates a current that is a function of power and wavelength of the incident light. Figure 3-1 shows the responsivity of FDS1010 to estimate the photocurrent. The bandwidth and the rise time response can be found from the diode capacitance and the load resistance. The following equation shows how to find the bandwidth and rise time.

$$F_{BW} = \frac{1}{2\pi * R_L * C_J} \quad (3.1)$$

$$t_r = \frac{0.18}{F_{BW}} \quad (3.2)$$

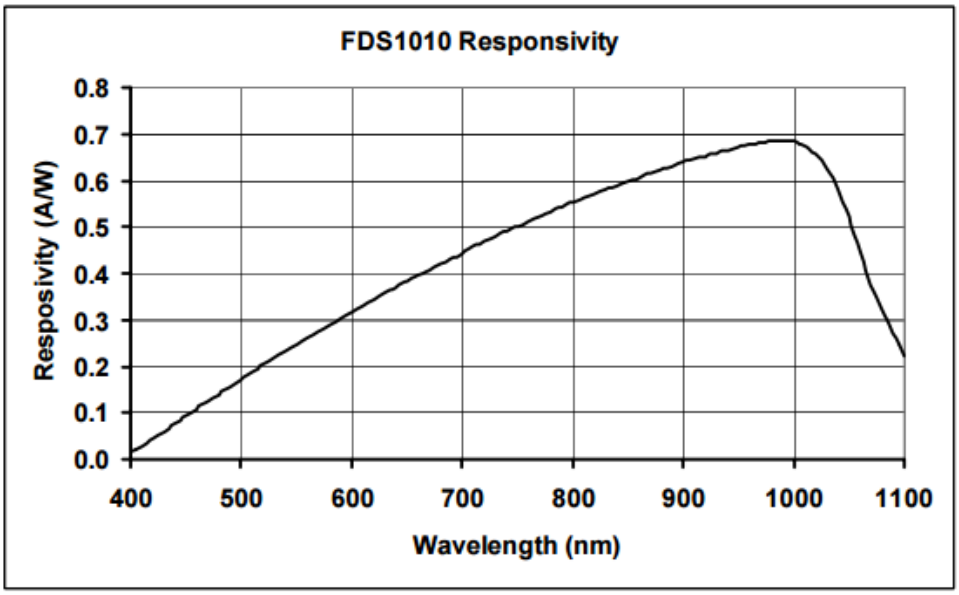


Figure 3-1 Responsivity vs Wavelength [27]

3.1.2 Transimpedance amplifier

The TIA is designed to give a transimpedance gain of 89.54dB to produce 30m V for every microampere of current. An extra post amplifier is used to provide additional gain of 30.46dB so that output voltage is in the order of volts. OPA380 is chosen as the TIA of this readout circuit. Figure 3-2 shows the transimpedance amplifier configuration designed and simulated in ADS.

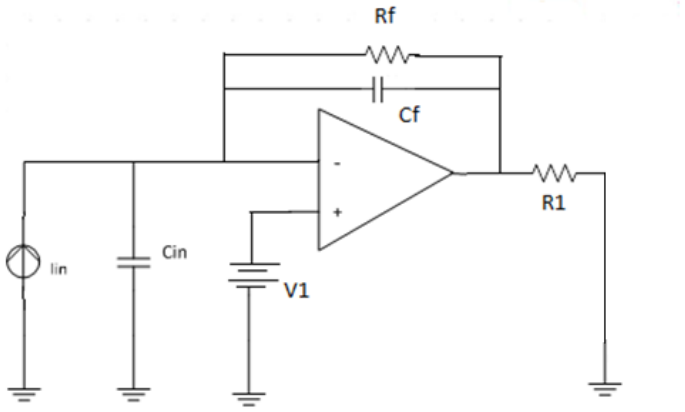


Figure 3-2 OPA 380 – TIA configuration

The junction capacitance of the photodetector (FDS1010) is 375pF. The output of the photodetector is connected directly to the inverting input of the transimpedance amplifier. The bandwidth and the rise time are given by equations 3.1 and 3.2 respectively. Here, the load resistance is given by the following equation.

$$R_L = \frac{R_f}{(1+A)} \tag{3.3}$$

Where, R_f is the feedback resistor of the transimpedance amplifier and A is the open loop gain of the transimpedance amplifier. The bandwidth of the photodetector is given by the following equation with load resistance replaced by that of the transimpedance amplifier.

$$\mathrm{f_{BW}} = \frac{1}{0.18\,(2\pi)\mathrm{C_{PD}}\frac{\mathrm{R_f}}{1+\frac{\mathrm{GBW}}{\mathrm{f_{3dB}}}}} \approx \frac{\mathrm{GBW}}{0.18\,(2\pi)\mathrm{C_{PD}}\,\mathrm{R_f f_{3dB}}} \tag{3.4}$$

Assuming, the speed of the photodetector to be equal to the f_{3dB} of the transimpedance amplifier,

$$f_{BW}^2 = \frac{GBW}{0.18\,(2\pi)C_{PD}\,R_f} \tag{3.5}$$

From the datasheet of OPA380, GBW is 90MHz. The R_f was set to 30kohm to get a 89.54dB gain. C_{TOT} is the total capacitance given by the following equation.

$$C_{TOT} = C_{PD} + C_{DIFF} + C_{COM} \tag{3.6}$$

Where, C_{DIFF} and C_{COM} are parasitic differential-mode and common-mode input capacitances given by the datasheet of OPA 380. The values are 3pF and 1.1pF respectively. Hence, C_{TOT} is 379.1pF. The value of feedback capacitance is given by solving the following equation for C_f.

$$\frac{1}{2\pi R_f\left(C_{f+}C_{stray}\right)} = \sqrt{\frac{GBW}{4\pi R_f C_{TOT}}} \tag{3.7}$$

A value of 2.4pF was obtained for the feedback capacitance. The stray capacitance value is 0.2pF from the datasheet of OPA 380. Figure 3-3 shows the ouput of the transimpedance amplifier simulated in ADS. The input current provided has a magnitude of 1uA with a pulse width of 1us. The output voltage obtained was 30mV as expected for the desired gain of 89.54dB.

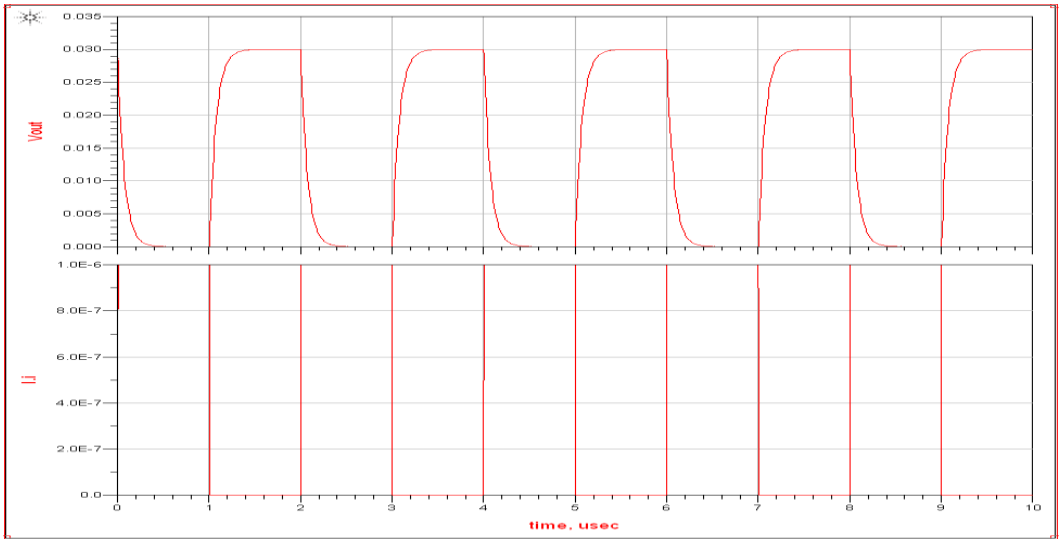


Figure 3-3 Input current (bottom) and TIA output (top)

3.1.3 Post-Amplifier

Since the gain of the transimpedance amplifier is 89.54dB, a post amplifier is required that could provide the additional gain of 30.46dB to make the magnitude of output of overall amplifier in the order of volts. OPA 846 is chosen for the post amplifier and designed to obtain 30.46dB.

3.1.4 Buffer

The OPA 380 was used in the buffer configuration with unity gain to serve the output load. Figure 3-4 shows the overall readout circuit for the optical sensing circuit simulated in ADS and Figure 3-5 (a)-(d) shows the input as well as the output at each node of the overall system.

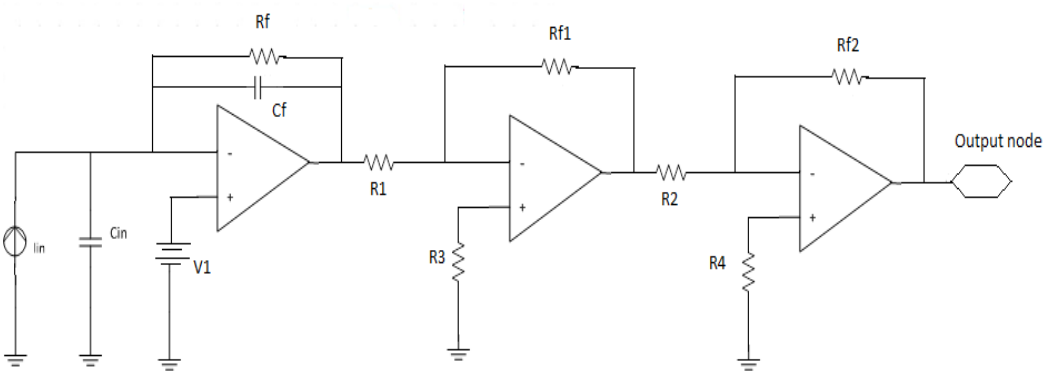
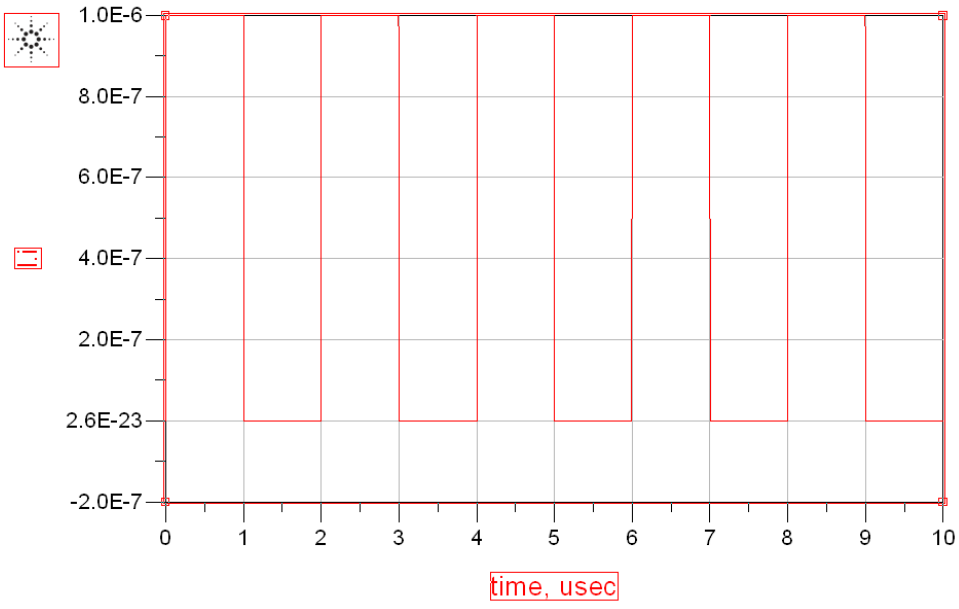
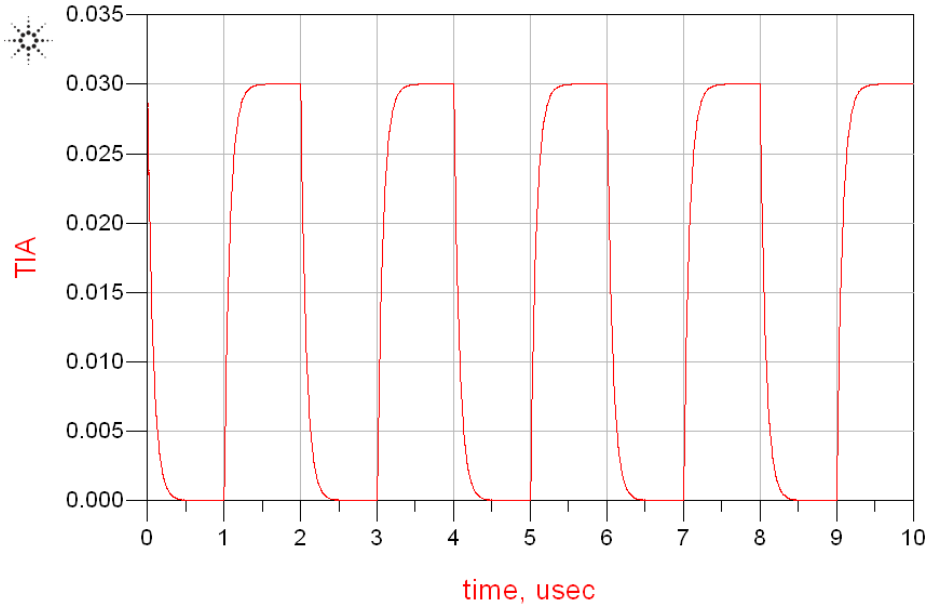


Figure 3-4 Overall readout circuit



(a)


0.035
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0.025
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0.000
TIA
0
1
2
3
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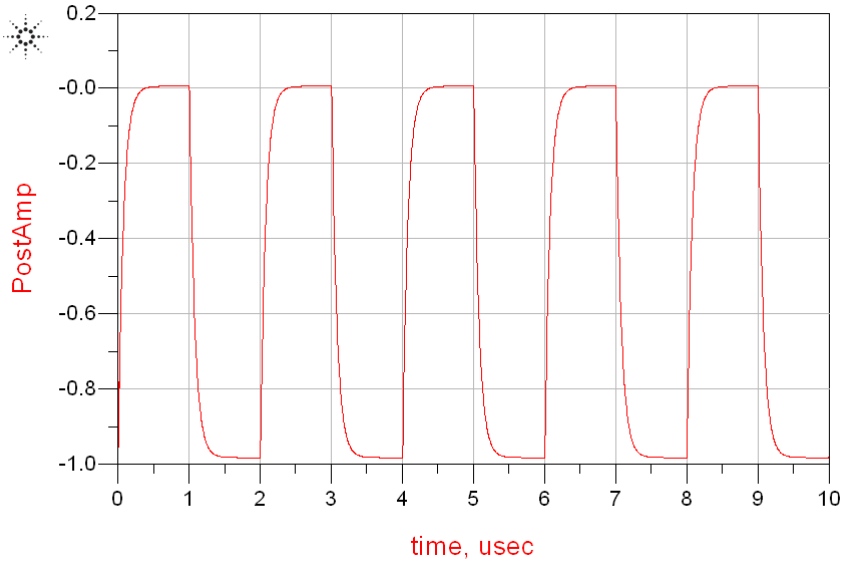
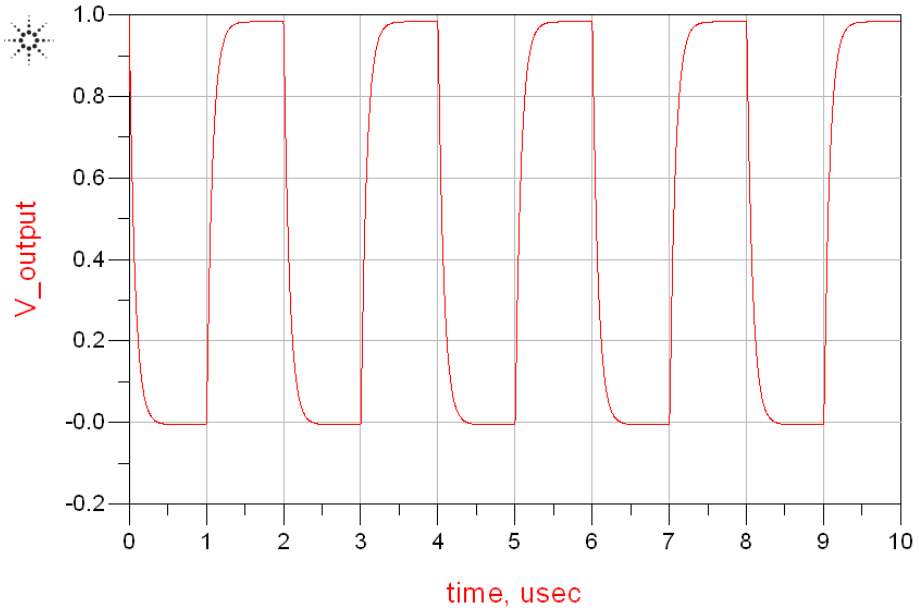
7
8
9
10
time, usec

(b)


0.2
-0.0
-0.2
-0.4
-0.6
-0.8
-1.0
PostAmp
0
1
2
3
4
5
6
7
8
9
10
time, usec

(c)



(d)

Figure 3-5 (a) Input current (b) TIA output (c) Post-Amp output (d) Final output

Figure 3-5 (a) shows the input current with magnitude of 1uA with a pulse width of 1us. Figure 3-5 (b) depicts the output voltage at the output node of the transimpedance amplifier. 30mV was obtained as expected for a gain of 89.54dB and the output is inverted since the design is in an inverting configuration.

Figure 3-5 (c) portrays the output voltage at the output node of the post amplifier. 1V was obtained in an inverted manner and output was as expected for a gain of 30.46dB. Finally, Figure 3-5 (d) illustrates the output of the buffer 1V was obtained as expected for a unity gain and the output is inverted since the design is in an inverting configuration.

3.2 Conventional TIA - Common gate Amplifier

The basic implementation of a transimpedance amplifier is the common gate configuration. Following Figure 3.1 shows the basic common gate amplifier configuration.

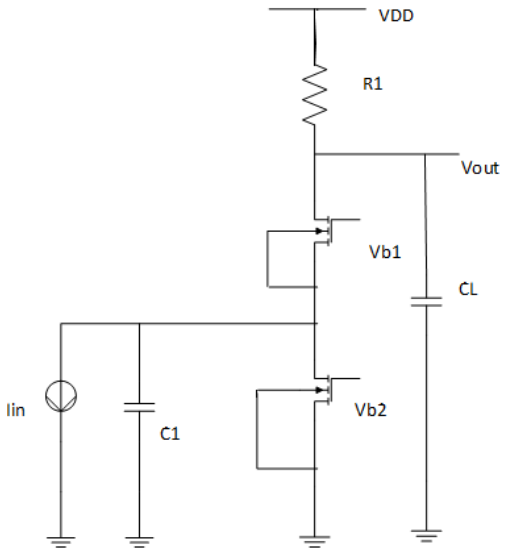


Figure 3-6 Common gate amplifier

The input impedance of the common gate amplifier is $1/g_m$ where g_m refers to the transconductance value of the transistor. The transimpedance gain is given by the following equation.

$$\frac{Vo}{Iin} = \frac{R_1}{(1+s\frac{C_1}{(gm+g_{mb})})(1+sR_1\,C_L)} \tag{3.8}$$

$$R_{in} \approx \frac{1}{g_m} \tag{3.9}$$

The advantage of this configuration is the simplicity of its design and its high stability. However, the drawback of the common gate configuration is that it is difficult to achieve a large bandwidth in combination with a moderate transimpedance gain for a low noise application. A feedback topology is required to improve the trade-off.

3.2.1 Noise Analysis

The major factors contributing to the input noise current are the bias current and the resistor R_1. The noise could be reduced by increasing the resistance value of the resistor R_1 but the limitation of voltage headroom restricts increasing of the resistance value. Hence the common gate amplifier configuration is not suitable for low noise applications. Figure 3-7 gives the noise model for the common gate configuration.

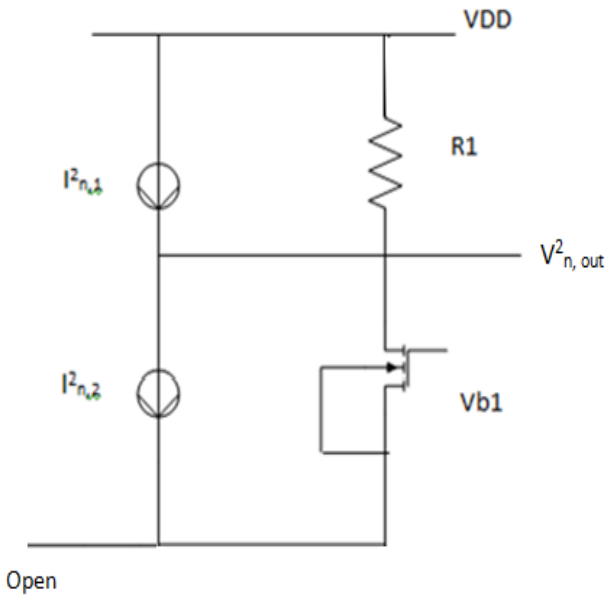


Figure 3-7 Noise model – common gate amplifier

The following equations give the overall output noise voltage and the input referred noise current for the common gate amplifier respectively.

$$V_{n,out}^2 = \left(I_{n,1}^2 + I_{n,2}^2\right)R_1^2 = 4kT\left(\frac{2}{3}g_m + \frac{1}{R_1}\right)R_1^2 \quad \left(\frac{V^2}{Hz}\right) \qquad (3.10)$$

$$I_{n,in}^2 = 4kT\left(\frac{2}{3}g_m + \frac{1}{R_1}\right) \quad \left(\frac{A^2}{Hz}\right) \qquad (3.11)$$

3.2.2 Simulation of Common gate configuration

Figure 3-8 shows the common gate configuration designed in cadence. The design has been implemented in 0.18um CMOS technology. The circuit was simulated using Cadence Spectre simulator. The power supply used for designing in this technology is Vdd=1.8V. Since the sensor current is modeled as a pulse current with magnitude of 1uA and with pulse duration of 1us, the same was provided to the common gate amplifier configuration. Figure 3-8 shows the input current signal given to the common gate amplifier.

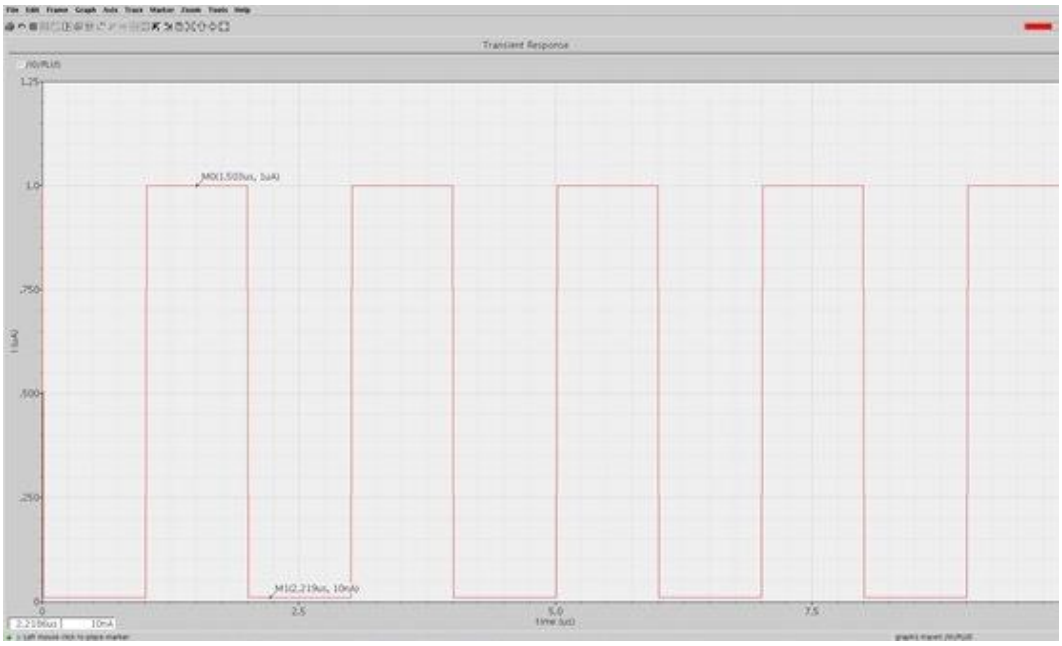


Figure 3-8 Input current signal - common gate amplifier

The common gate was designed for a transimpedance gain of 80.08dBohm. This was the gain that could be achieved with maintaining the operation region of amplifier in saturation. Hence for an input current of 1uA, an output voltage of 10mV was observed. Following Figure 3-9 shows the output voltage of the common gate amplifier.

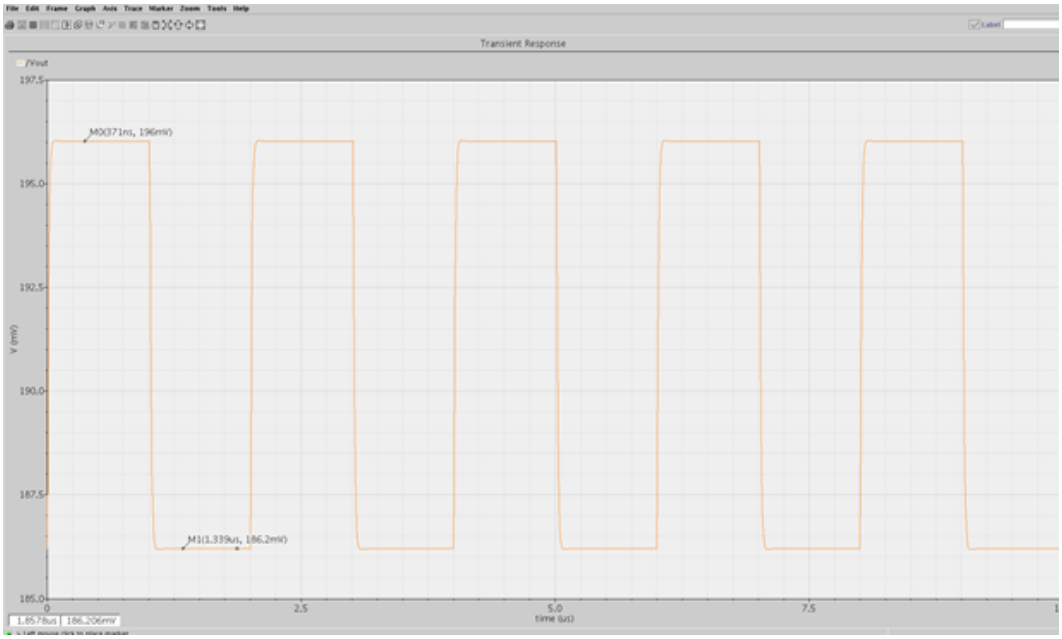


Figure 3-9 Output voltage- common gate amplifier

Figure 3-10 shows the power consumption plotted through simulation using cadence spectre. The average power is 17.28uW and the peak power is 17.33uW.

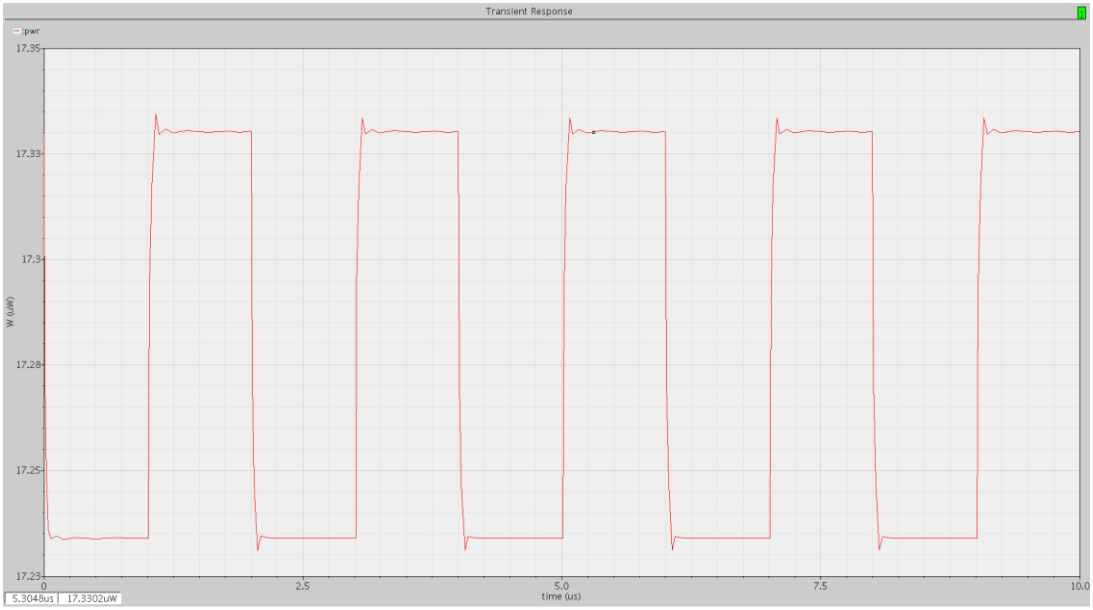


Figure 3-10 Power consumption- common gate amplifier

Figure 3-11 shows the output noise plotted through simulation using cadence spectre.

The output noise at 500 kHz is found to be 623.5nV/$\sqrt{Hz}$.

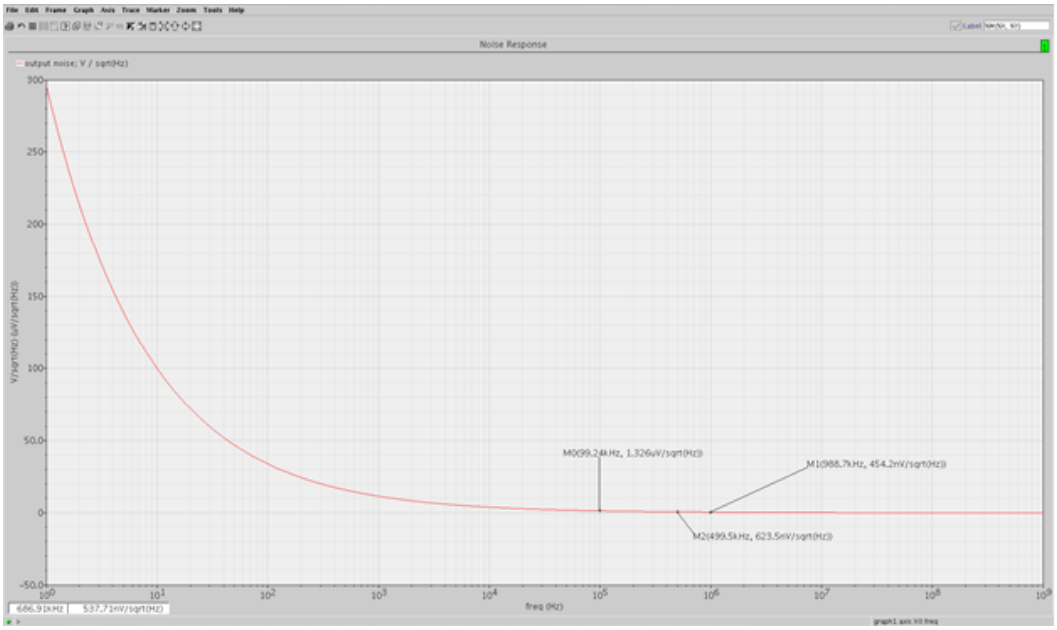


Figure 3-11 Output noise- common gate amplifier

3.3 Proposed design

The switched capacitor based transimpedance amplifier has been designed using an operational amplifier and a logic control block that controls the switching system in the circuit to achieve low power consumption and low noise, which is critical for the toxin detection system. The proposed design has been implemented in 0.18um CMOS technology. The circuit was simulated using Cadence Spectre simulator. The power supply used for designing in this technology is Vdd=3.3V. The following sections discuss the design of the Operational Amplifier, the logic control circuit and finally the switched capacitor design.

3.3.1 Operational Amplifier

The operational Amplifier is comprised of two stages. The first stage is a folded cascode structure and the second stage is a common source amplifier. Figure 3-12 shows the design of the two-stage operational amplifier.

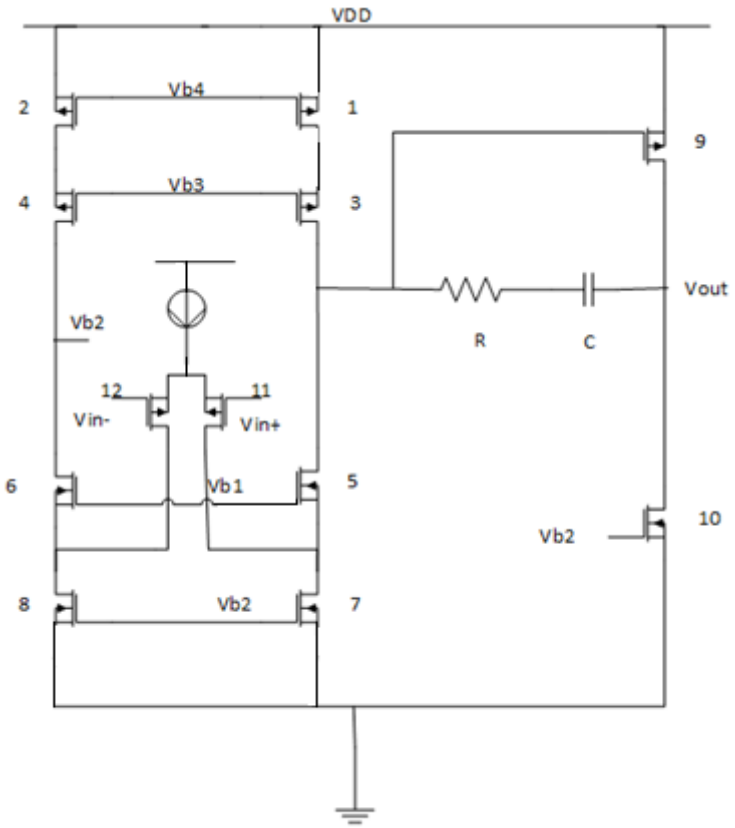


Figure 3-12 Operational Amplifier design

The operational amplifier needs to have a large gain to reduce the effect of feedback gain error. Also a high output swing is necessary for measuring the output range from the sensor. Thus the folded cascode structure is used since it offers a relatively high output swing as well as provides a high gain as compared to a telescopic structure.

The folded cascode structure has a differential PMOS input with active current mirror load. Transistors 1-2 are the input differential pair. The folded cascade structure is used for higher gain and majorly contributes to overall gain of the operational amplifier while the common source amplifier is used to drive the load at the output. The resistor between the first and second stage is the RHP zero compensating resistor and the capacitor between the two stages is the miller capacitance. The resistor and capacitor is used for pole splitting in the operation amplifier. They are used to improve the phase margin.

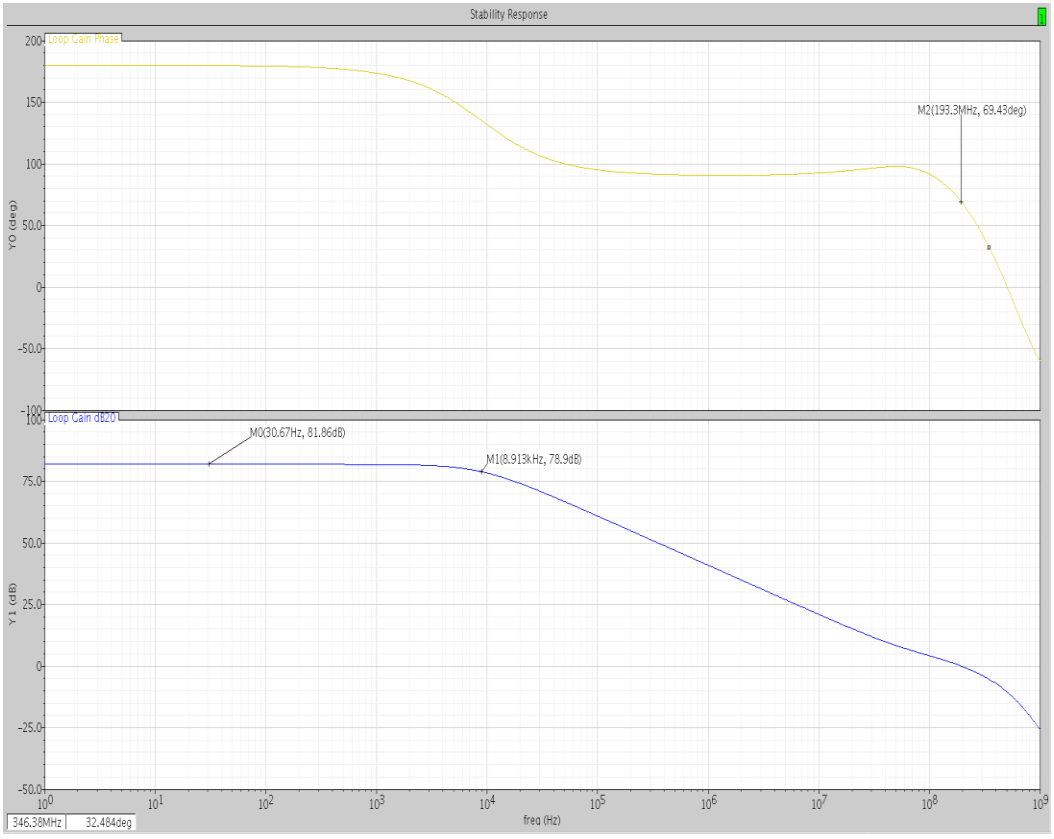


Figure 3-13 Plots of opamp gain and phase

The operational amplifier in Figure 3-13 has a DC gain of 81.86 dB with a phase margin of about 69 deg. The unity gain frequency is at 193.3 MHz. The output swing of the operational amplifier is measured by connecting it in a unity-gain buffer configuration. The output is connected to the inverting terminal. The non-inverting terminal is ranged from VDD to VSS. The DC transfer curve shows an output swing from 0V to around 2.7V giving a total of 2.7V swing of a 3.3V Vdd-Vss. Figure 3-14 shows the DC transfer curve of the operational amplifier.

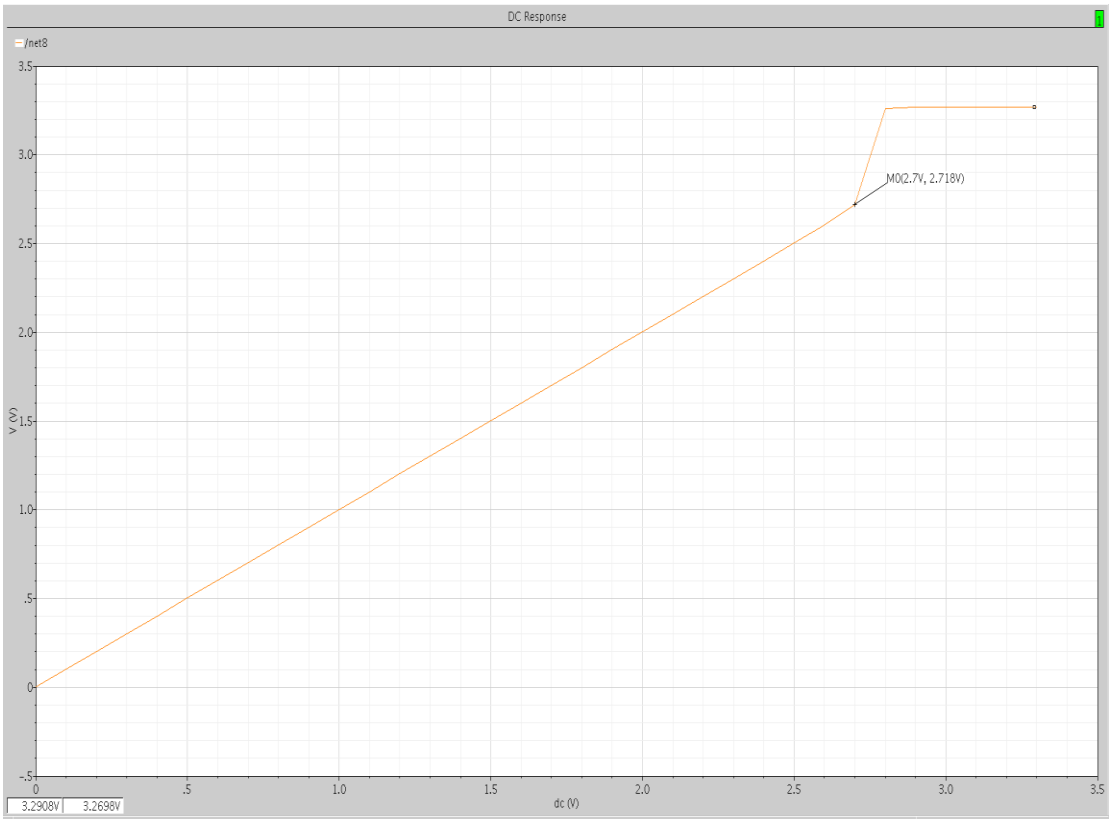


Figure 3-14 DC Transfer curve

The op-amp performance parameters from schematic simulation are summarized in the table below.

Table 3-2 Performance parameters of operational amplifier

Parameters	**Value**
Gain	81.86 dB
3dB Bandwidth	8.9 KHz
Unity Gain Bandwidth	193.3MHz
Phase Margin	69.43 degree
Output Swing	2.7V

3.3.2 Logic control circuit

The switched capacitor based transimpedance amplifier design in Figure 3-18 has three switches. The logic control circuit is designed to obtain the three phases of clock signal as shown in Figure 3-17. A single clock signal of 4MHz frequency is provided to the logic block to generate three different phase control signals. The digital circuit

block includes a series of inverters, Nand gates, or gates and TSPC D flip-flops. The inverters are used to create delaying in the 4MHz input clock signal, the NAND and OR gates are used to perform logic operation on the delayed signals, and the TSPC D flip-flops are used as a frequency divider. Figure 3-15 shows the overall block of the logic control circuit. Figure 3-16 (a)-(d) shows the circuit design of the individual blocks.

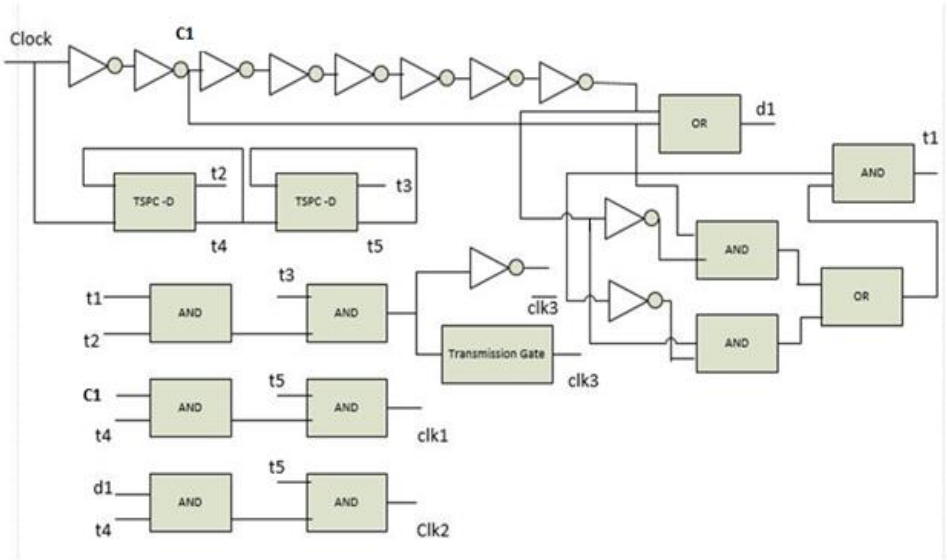
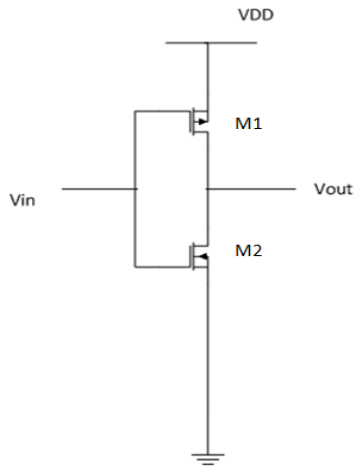
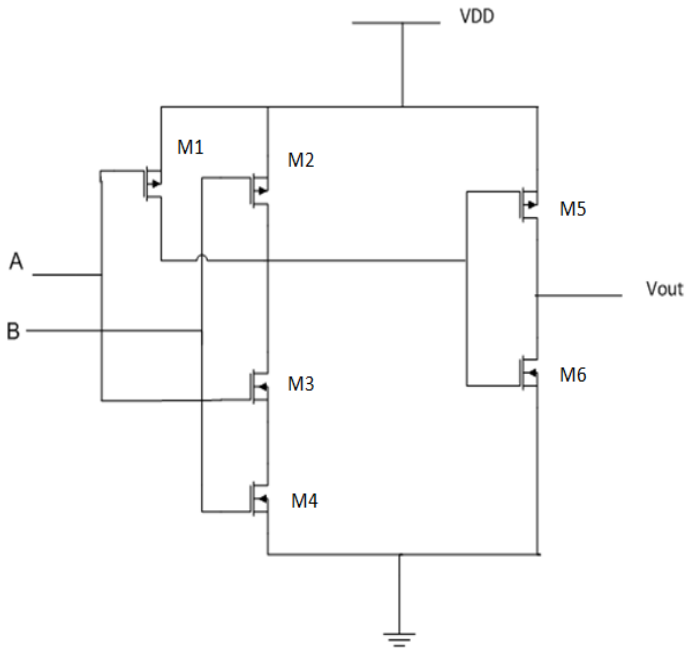


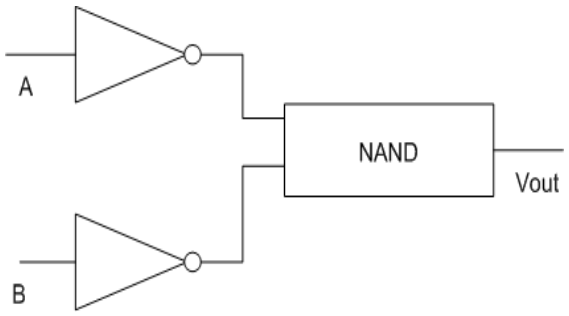
Figure 3-15 Logic control block



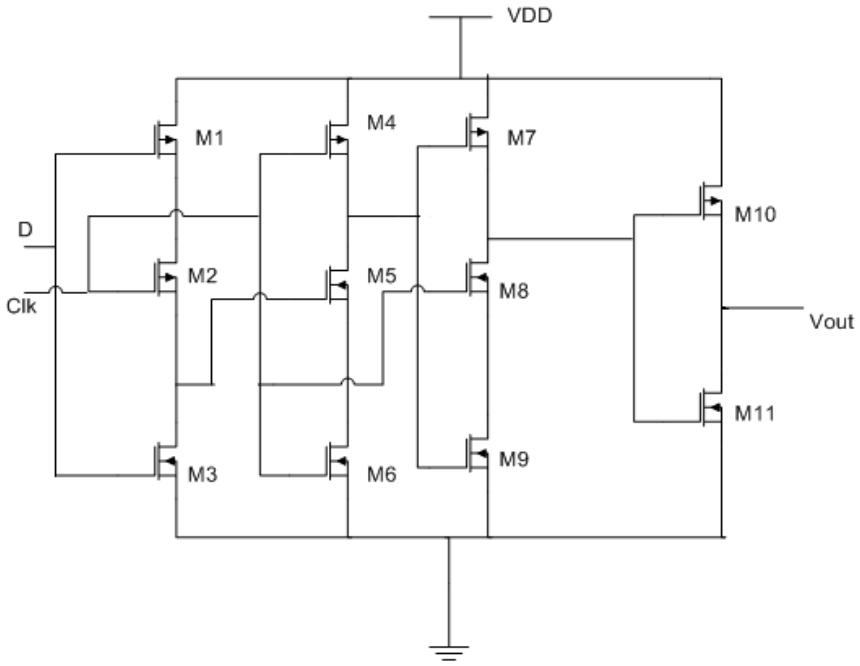
(a)



(b)



(c)



(d)

Figure 3-16 (a) Inverter (b) NAND gate (c) OR gate (d) TSCP D flip-flop

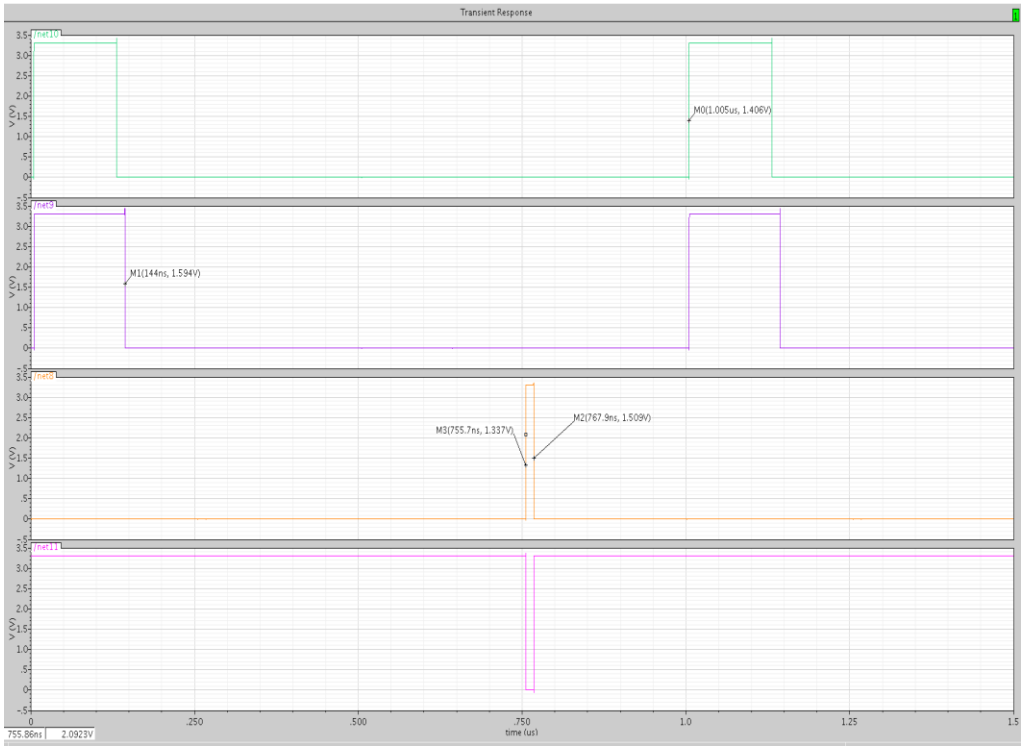


Figure 3-17 Three clock phases

Figure 3-17 shows the three clock phases used to control the switched capacitor based transimpedance amplifier.

3.3.3 Switched capacitor circuit

The switched capacitor based transimpedance amplifier design is shown in Figure 3-18. The circuit resembles a charge integrator. The amplifier produces an output voltage inversely proportional to the value of the feedback capacitor and proportional to the total input charge that flows through during the specified time period. The design

also has a sample and hold circuit to hold the output voltage until the subsequent sampling period.

The circuit has three switches controlled by three phases of clock signal Φ1, Φ2 and Φ3. The switches are NMOS transistors. The capacitors C_f, C_{out} and the charging time T are chosen based on the required gain.

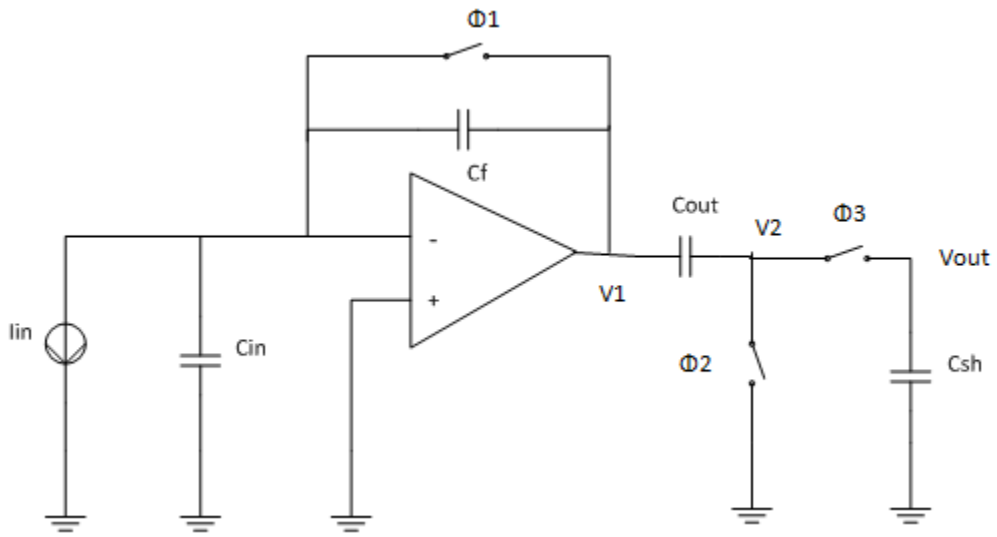


Figure 3-18 Switched capacitor circuit

Figure 3-19 shows the three phases of clock signal to control the three switches respectively in the circuit.

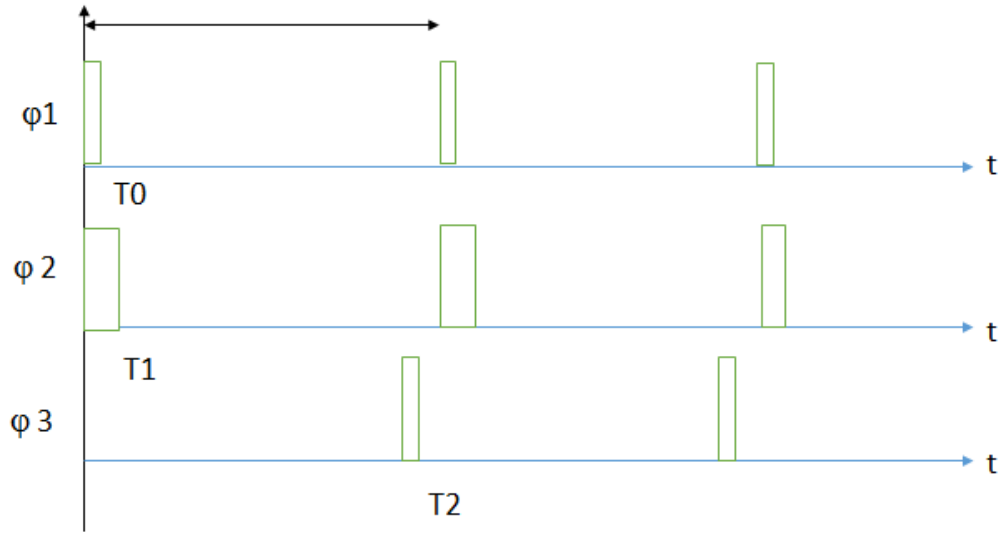


Figure 3-19 Timing diagram of three phases

An input clock signal of 4MHz frequency is provided to the logic control circuit as explained in the above section. The logic control circuit provides the three phases of clock signal. The pulse duration of the three phases of clock signal is much lesser than the clock period T.

The circuit is clocked at 1MHz with three different phases. Figure 3-20 and Figure 3-21 below shows voltage response at nodes V1, V2 and V_{out} respectively, within the circuit to a sample input current Iin. Charges on capacitors C_f and C_{out} are reset to 0 during Φ1. After Φ1 goes low at T0, the input current begins to charge C_f and V1 begins to rise with a slope proportional to the magnitude of Iin. After Φ2 goes low at T1, V2 follows the change of V1. The sample and Hold (S&H) circuit, consisting of a NMOS

switch Φ3 and a capacitor Csh, samples V2 at the end of Φ 3 and hold the value till next time Φ 3 is on [1].

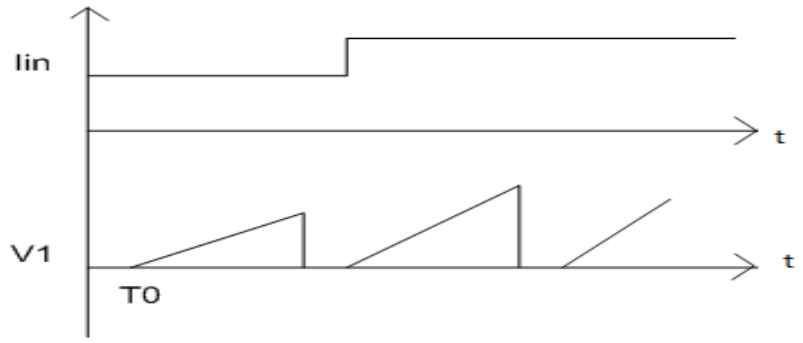


Figure 3-20 Input current (top) and Voltage at node V1 (bottom)

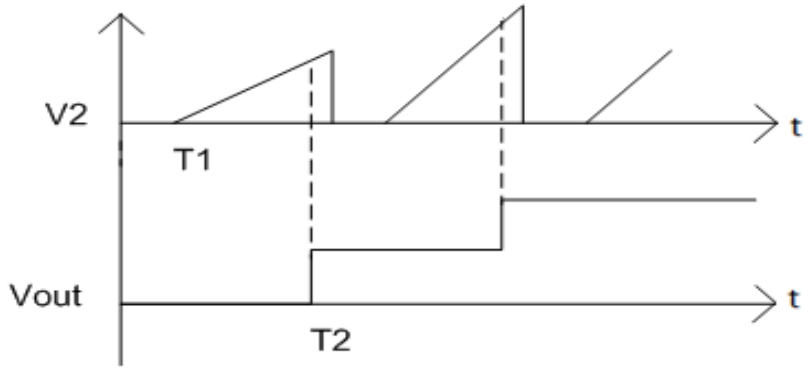


Figure 3-21 Voltage at node V2 and Voltage at node V_{out} (bottom)

3.3.4 Analysis of proposed design

The following sections discuss analysis done on the transimpedance amplifier, NMOS switches and the buffer.

3.3.4.1 Switched capacitor design

The basic switched capacitor topology has two phases (i) reset phase and (ii) Amplification phase. The behavior of the circuit in each of the phases is discussed below.

(i)Reset phase

In this phase both switches across capacitors C_f and C_{out} are on. Figure 3-22 shows the configuration of the switched capacitor circuit in the reset phase. The V1 is at the same potential as the virtual ground and the potential V2 is at 0 since it is connected to actual ground. Hence, the voltage across C_f and C_{out} is reset.

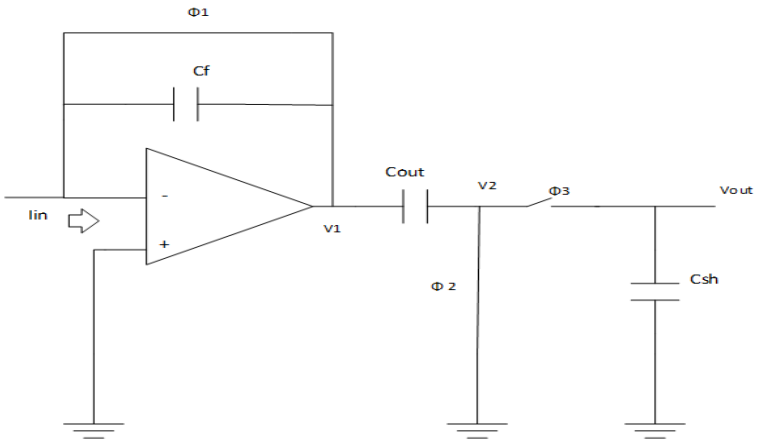


Figure 3-22 Reset Phase

(ii)Amplification phase

There are three phases of switching in this amplification phase. The behavior of the switched capacitor circuit during the three phases is discussed below:

(a) Φ1 is open and Φ2 is closed: In this phase, the operational amplifier behaves as a charge integrator. Figure 3-23 shows the configuration of the switched capacitor circuit in this phase. Thus, the voltage V1 (T0) at time instant T0, where, T0 is the time at which Φ1 opens, is a result of integration of optical sensing current. Voltage V2 (T0) is still at 0 since it is connected to ground.

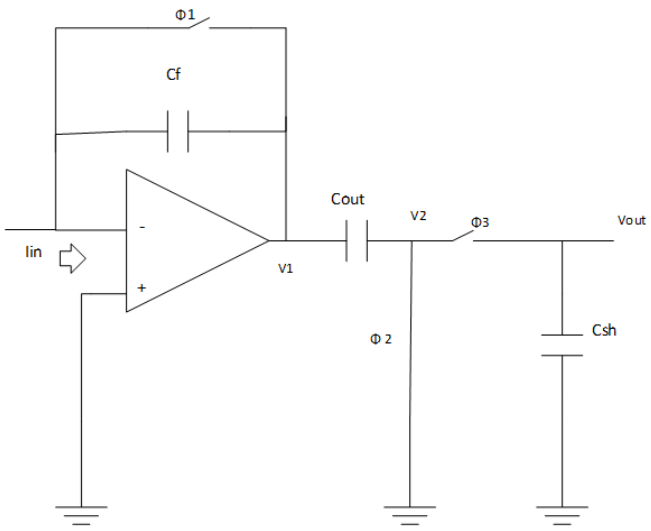


Figure 3-23 Φ1 low and Φ2 high

(b) Φ1 is open and Φ2 is open: In this phase, the voltage V2 (t) is no longer connected to ground. It follows the change in voltage V1 (t). This phase employs correlated double sampling phenomenon to cancel flicker noise and circuit offset.

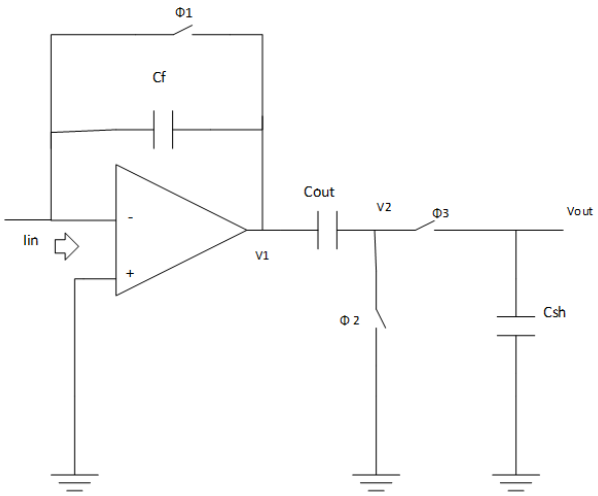


Figure 3-24 Φ1 low and Φ2 low

(c) Φ3 is closed: In this phase, the sample and hold circuit samples V2 when Φ3 goes high at time instant T2 and the switch is closed. V_{out} (T2) is the sampled output which is held until the next time Φ3 goes high.

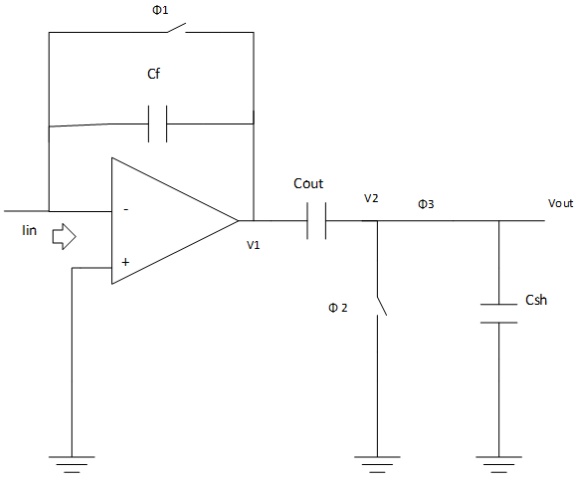


Figure 3-25 Φ3 is high

The switched capacitor based transimpedance amplifier output voltage at the end of each clock period is given by the following expression:

$$Vout(nT) = \frac{1}{Cf}\int_{T1+(n-1)T}^{T2+(n-1)T} Iin(t)dt \qquad (3.12)$$

Where n=1, 2, 3…

The assumption here is that the optical current frequency is far less than the clock frequency. It is considered as a pseudo dc signal when seen within the clock period. The TIA output is given by the following equation [1]:

$$Vout(nT) \approx \frac{1}{Cf}.Iin(nT)(T2 - T1) \approx \frac{T}{Cf}.Iin(nT) \quad (3.13)$$

The low frequency gain of the switched capacitor based transimpedance amplifier is proportional to the time period and inversely proportional to the capacitance C_f. In this case the time period T is chosen as 603ns and C_f is chosen as 525.8fF. Since the optical sensing current Iin is 1uA, the calculated gain is around 121dB. Thus the transimpedance could be in the range of few Mohm.

3.3.4.2 NMOS Switch

The switches used in the design of switched capacitor based transimpedance amplifier are NMOS switches. For this application since the optical sensing current is between the range 0-1uA there is need for transfer of a strong logic 0 and no lesser need for transfer of a strong logic 1, hence an NMOS switch is chosen. The equivalent resistance is given by the following expression:

$$R_{on} = [\mu_n C_{ox} (W/L) (V_{DD}-V_{TH})]^{-1} \quad (3.14)$$

Where, μ_n is the mobility of charge carriers in NMOS device, C_{ox} is oxide capacitance of NMOS device, W and L are device dimensions of NMOS device, V_{TH} is threshold voltage of NMOS device. Unfortunately the NMOS switches used in the design have non-idealities such as charge injection and clock feed through.

Dummy Switch

The charge injected by the NMOS switches is removed by using an additional NMOS switch. This dummy switch is controlled by a clock signal complementary to the clock signal of the switch whose non-idealities need to be removed. Hence when the actual switch turns off the dummy switch turns on and the charge injected by the actual switch is absorbed by the dummy switch.

Assuming equal splitting of the charge between drain and source, the transistor size for the dummy switch is found. The following expression is used to choose the size of dummy switch:

$$\Delta q_1 = W_1 L_1 C_{ox}/2\ (V_{CK}-V_{in}-V_{TH1}) \quad (3.15)$$

$$\Delta q_2 = W_2 L_2 C_{ox}\ (V_{CK}-V_{in}-V_{TH2}) \quad (3.16)$$

$$\Delta q_1 = \Delta q_2 \quad (3.17)$$

$$W_2 = 0.5\ W_1 \text{ and } L_2 = L_1 \quad (3.18)$$

3.3.4.3 Buffer

The operational amplifier used for buffer is the same as the two stage operational amplifier used for switched capacitor design with the non-inverting input connected to the output node in the buffer configuration. The circuit behaves as an inverting voltage follower.

3.3.5 Noise sources and Correlated Double Sampling

Thermal and flicker are the two most significant types of noise. Following section describes the two types of noises in details.

(i)Thermal noise is due to random fluctuations that are caused in the drain current due to random motion of charge carriers in the channel. Since the transistor operates in the triode region, the thermal noise is given by the following equation [33]:

$$S_I = \frac{4kT}{R_{on}} [A^2/Hz] \quad (3.19)$$

Where, k is the Boltzmann constant, k=1.38$*$10^{-23} J/K, T is absolute temperature of the device in degrees Kelvin, and R_{on} is the on-resistance in ohms for the transistor [33].

(ii)Flicker noise or 1/f noise is due to the phenomenon of trapping and releasing of charge carriers when they move through the channel of the transistor. The power spectral destiny is given by the following equation.

$$S_{Id}(f) = \frac{I_d^2 \alpha_H}{fWLN} [A^2/Hz] \quad (3.20)$$

The above equations is obtained from "*Hooge's bulk mobility fluctuation model*" [34] where, α_H is Hooge's empirical factor and N is the total number of free carriers.

3.3.5.1 Correlated Double Sampling

As discussed above two major noise contributions possible noise sources of the SCTIA are thermal noise and flicker noise. The shot noise contributions due to leakage current are negligible. Apart from these noise contributions from the clock phases

controlled by switched functioning in deep triode region are highly weakened when input referred to the transimpedance amplifier.

Correlated double sampling is employed to cancel offset in operational amplifier and the low frequency noise. At the end of first phase the overall noise voltage is amplified by the charge integrator part of the circuit and stored as a voltage across the capacitance C_{out}. Figure 3-26 and Figure 3-27 depicts the working phases.

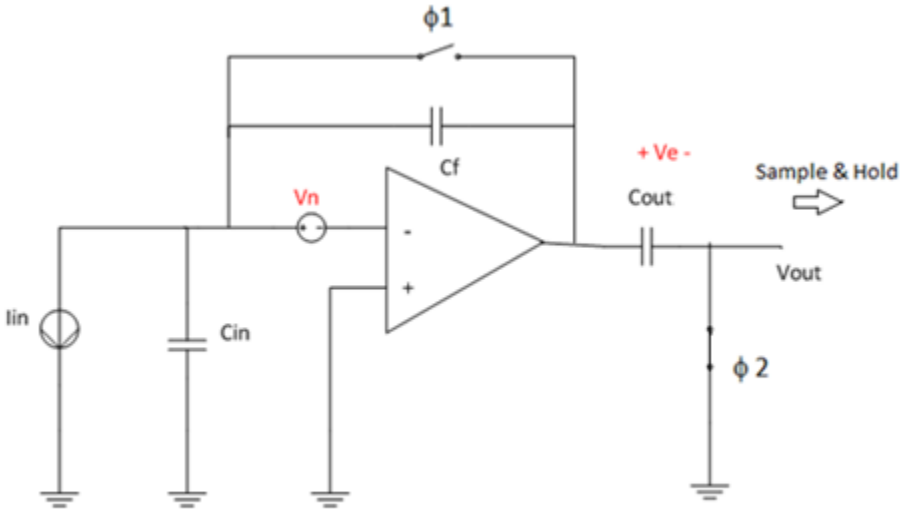


Figure 3-26 Correlated Double sampling – Phase1

In the phase Φ2, the offset, the low frequency noise along with the signal is amplified by charge integrator part of the switched capacitor circuit. The amplification is equal to the ratio of the capacitance value C_{in} and C_f respectively. The resultant voltage produced by the charge integrator is stored across C_{out}. At the end of Φ2, the output

which is the amplification of both signal and error is subtracted from previously stored output across C_{out} [1].

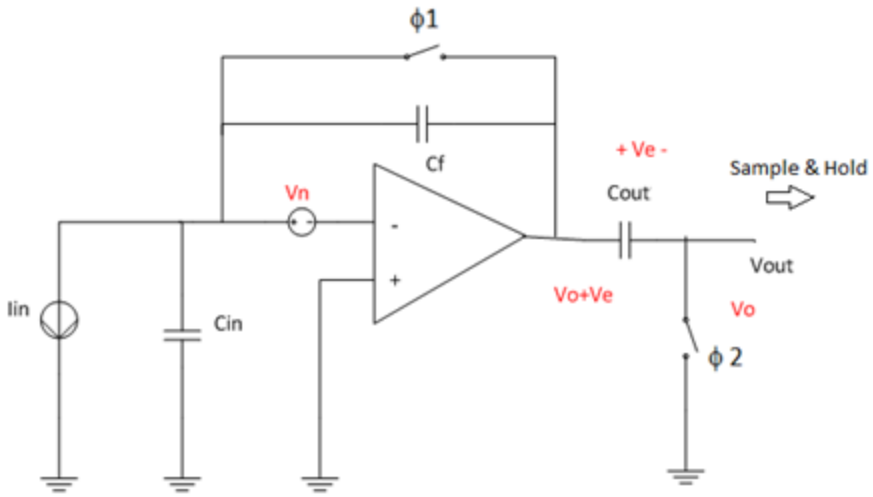


Figure 3-27 Correlated Double sampling – Phase2

3.3.6 Simulation Results

Since the sensor current is a pulse current. A similar current input was provided to the switched capacitor based transimpedance amplifier circuit with two different magnitudes, namely, upper value of 1uA and lower value of 500nA with pulse duration of 1us. Figure 3-28 shows the input current of the above specifications.

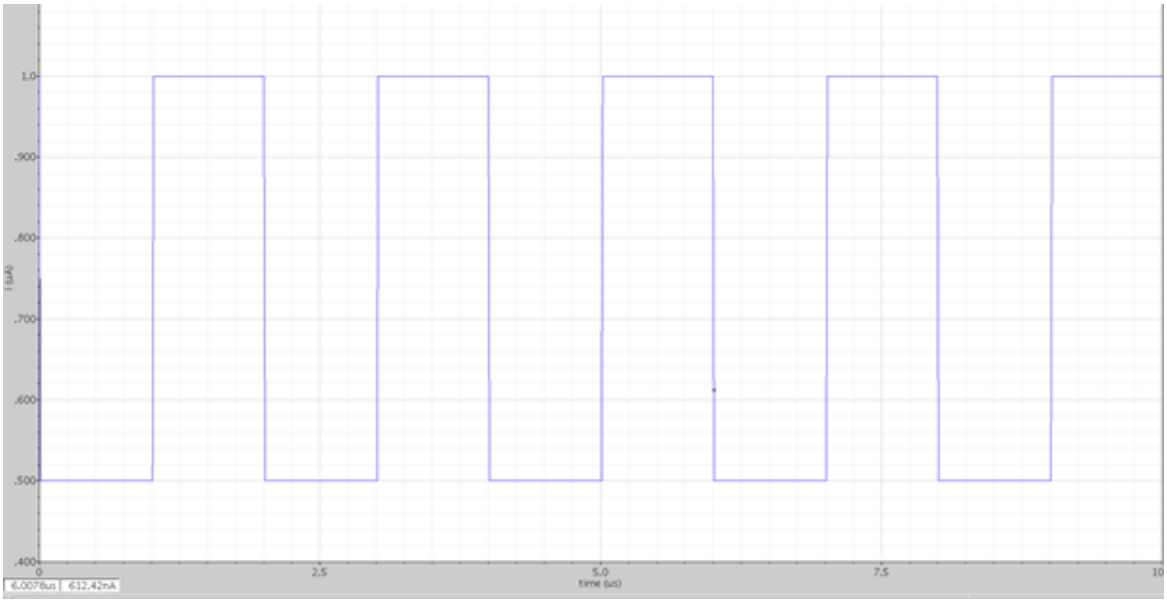


Figure 3-28 input current - SCTIA

Figure 3-29 shows the output voltage of 1.16V and 0.592 V from the switched capacitor circuit for current magnitude 1uA and 500nA respectively. The initial variations in voltage value is due to contribution of stored channel charge. The transimpedance gain achieved is 121.2dB

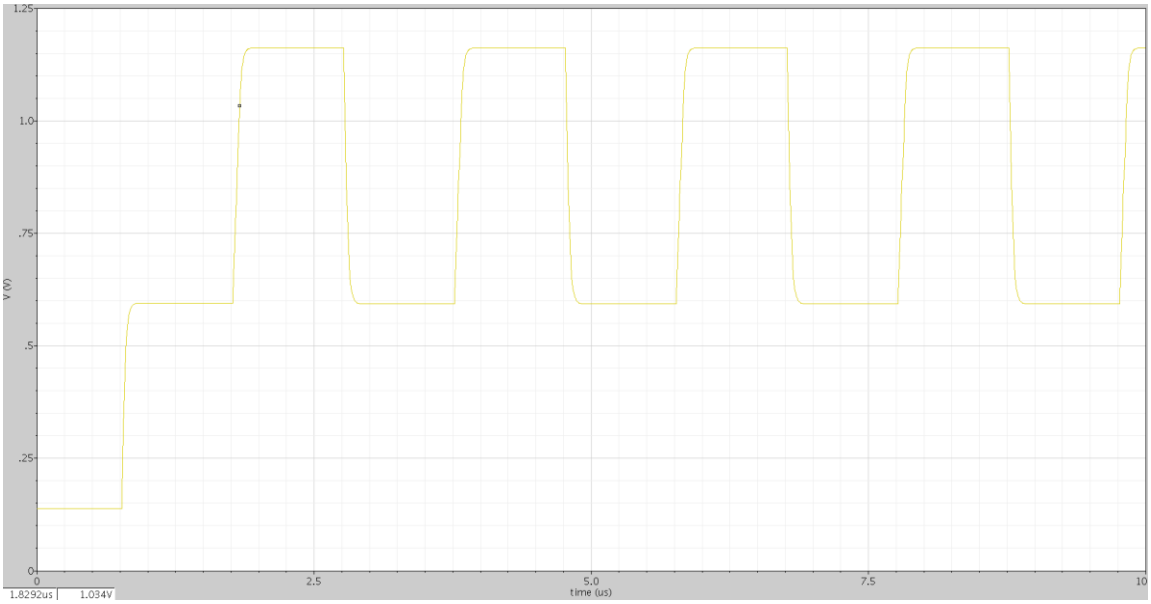


Figure 3-29 Output voltage - SCTIA

Figure 3-30 shows the output noise simulated and swept over frequency range. The noise at 500kHz is 76.22nV/$\sqrt{Hz}$ which is quite low compared to a conventional transimpedance amplifier or other existing architectures.

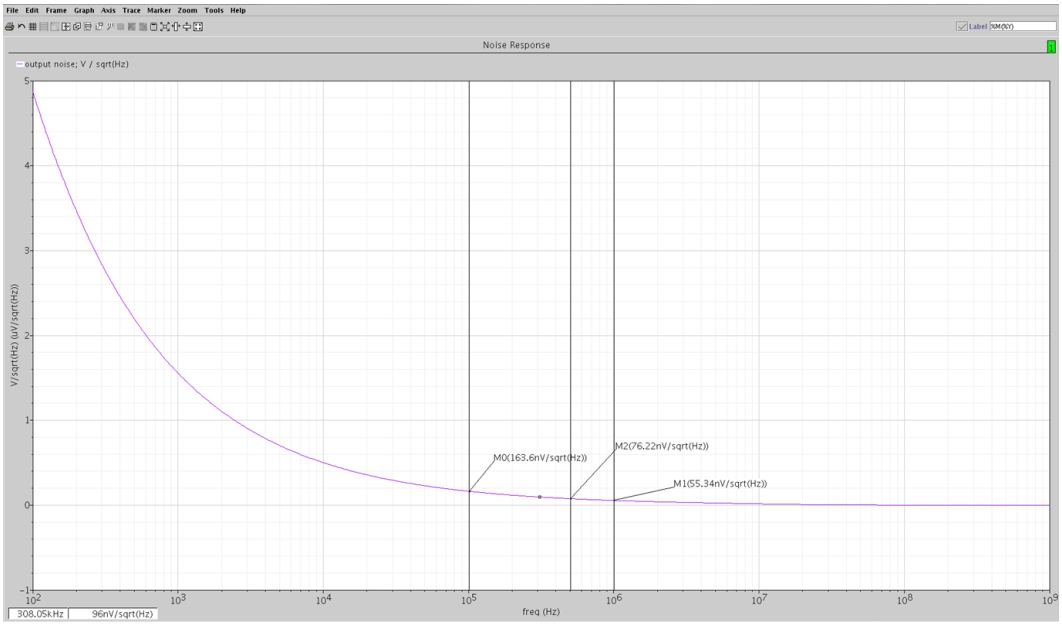


Figure 3-30 Noise-SCTIA

Figure 3-31 shows the power consumption of the switched based transimpedance amplifier. The peak power reached is 7.2uW. The power consumption is very low compared to a conventional transimpedance amplifier or other existing architectures.

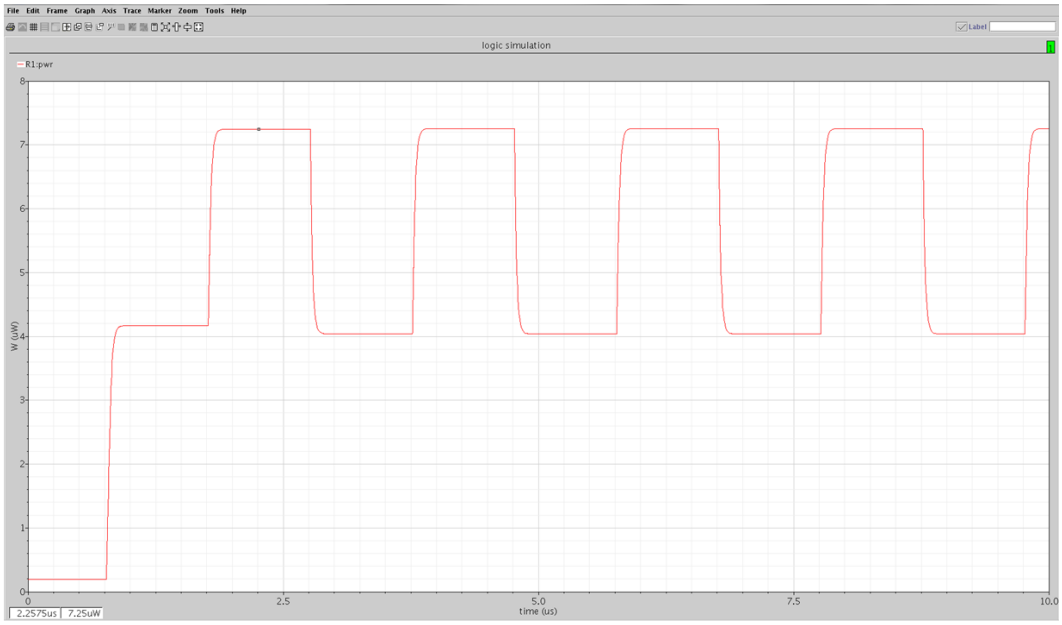


Figure 3-31 Power- SCTIA

3.3.7 Layout and Post-Layout simulation

3.3.7.1 Operational amplifier layout

Figure 3-32 shows the post extraction simulations results for the operational amplifier.

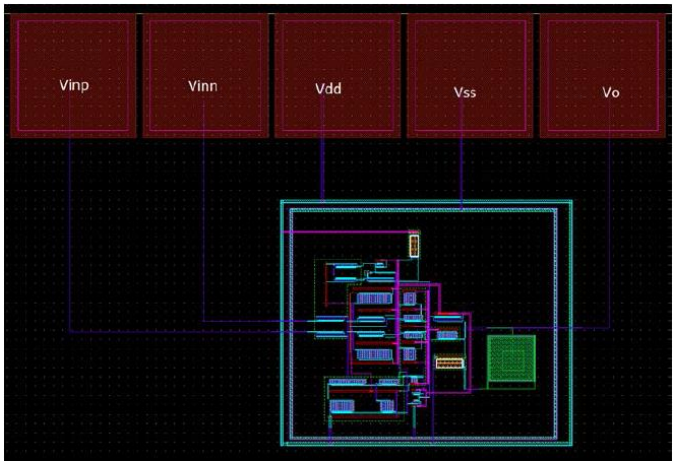


Figure 3-32 Operational amplifier layout

The layout has a total of 5 pads. The gain obtained is 78dB which is less than the expected 81.86dB and the phase margin is 58 degree.

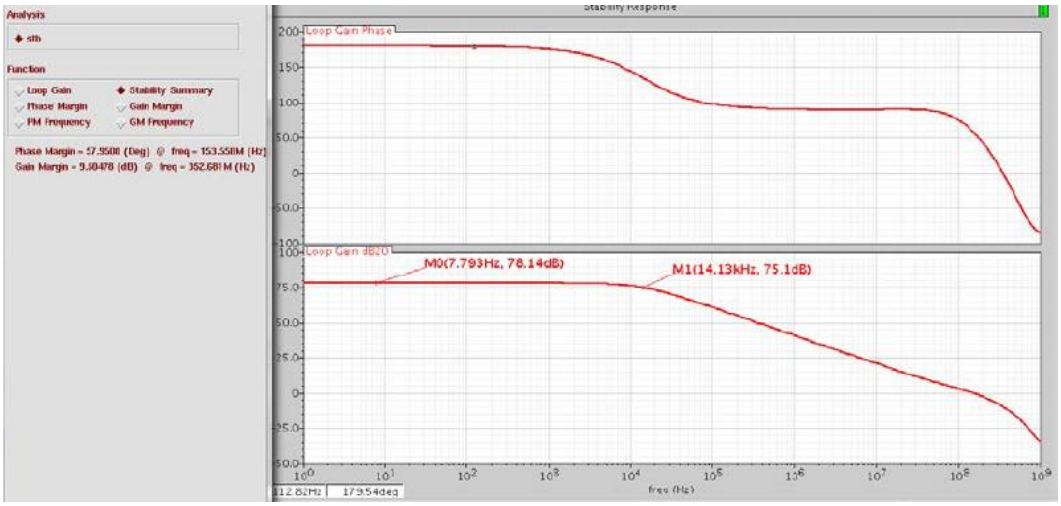


Figure 3-33 stability curve of operational amplifier - post layout

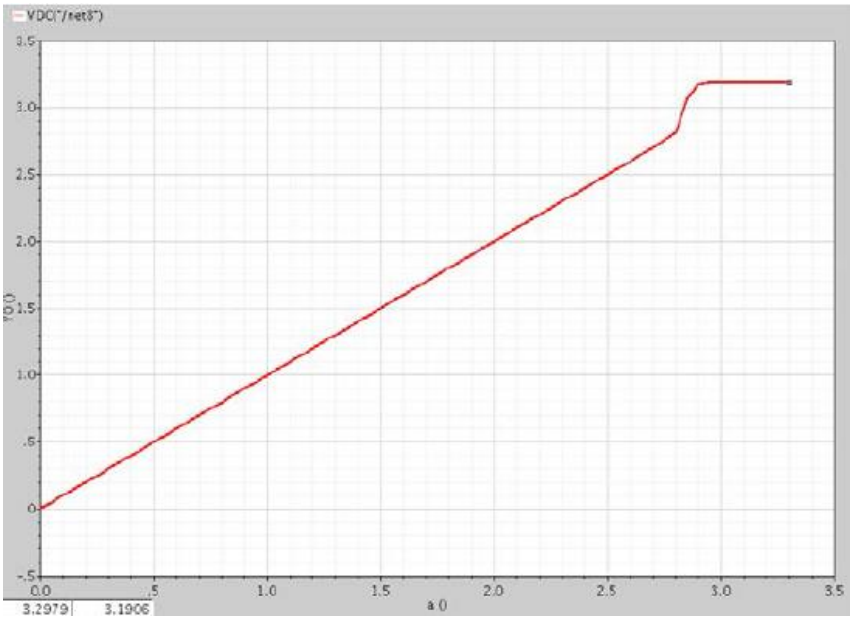


Figure 3-34 DC transfer curve - post layout

Figure 3-34 shows the DC transfer curve for the operational amplifier post layout. The output swing is 2.7V which is similar to the simulated output.

3.3.7.2 Logic control layout

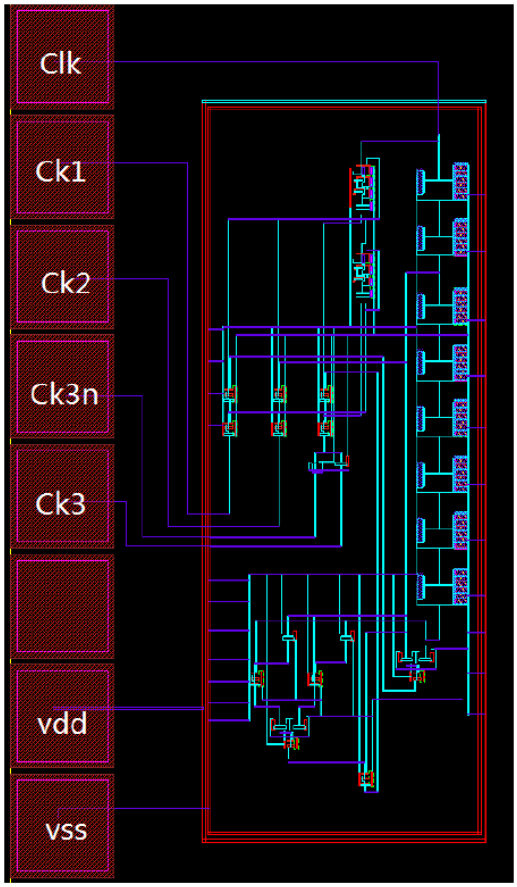


Figure 3-35 Logic control circuit layout

Figure 3-33 shows the post extraction simulations results for the operational amplifier. The layout has 7 pads.

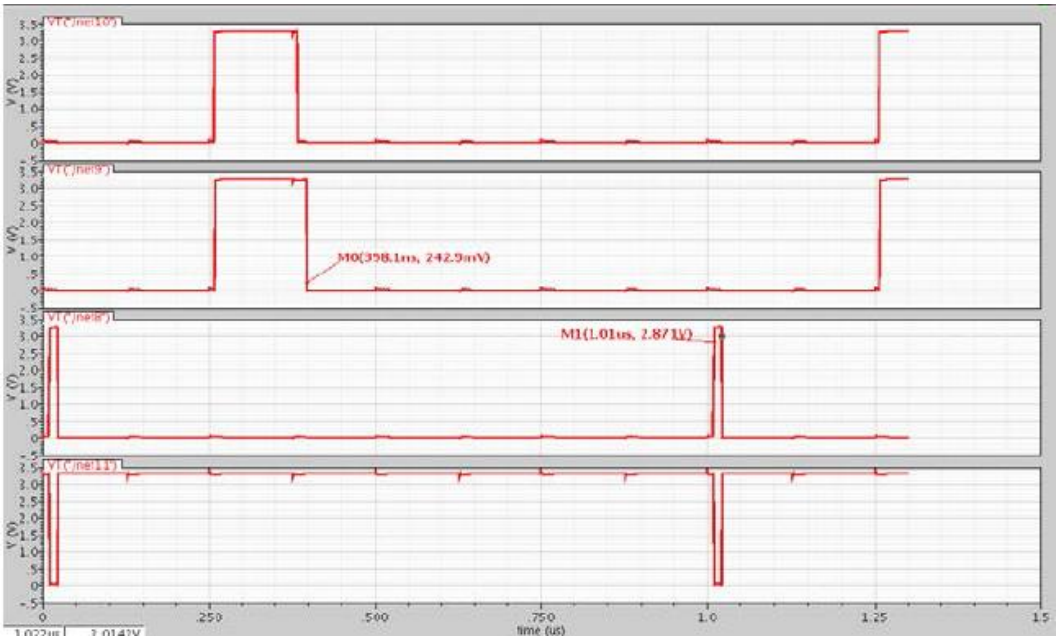


Figure 3-36 Phases of clock signal - post layout

Figure 3-36 shows the three phases of clock signal generated to control the switches in the switched capacitor based transimpedance amplifier. The charging time is 603ns which is less than the expected 612ns.

3.3.7.3 Switched capacitor circuit layout

Figure 3-37 shows layout for the switched capacitor circuit made up of the operational amplifier circuit, logic control circuit and the buffer blocks.

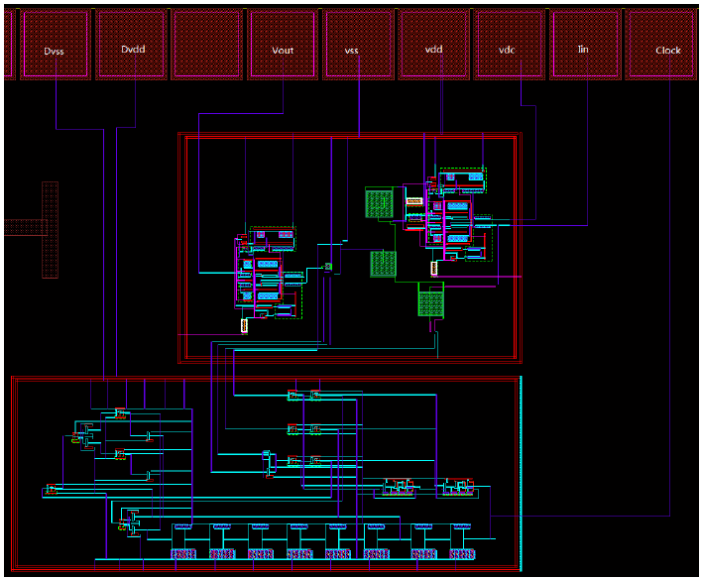


Figure 3-37 switched capacitor layout

Figure 3-38 shows post layout simulation of the switched capacitor circuit. The Gain is 120.69 which is less than the expected 121.2 dB. The simulation was performed for input currents of 1uA and 500nA respectively with pulse width of 1us. The output voltages obtained were 1.083V and 542.4V respectively.

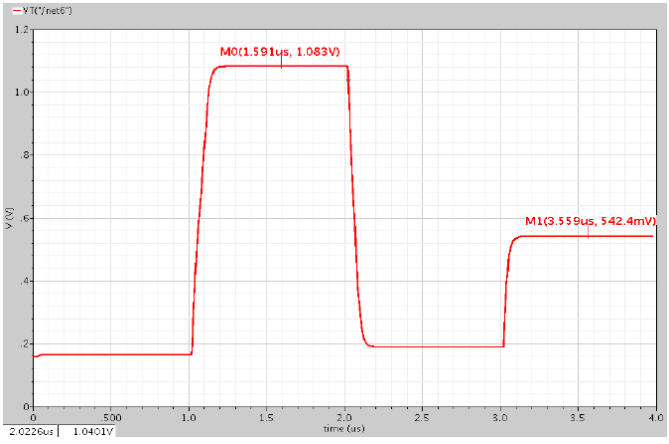


Figure 3-38 output voltage of SC-TIA – post layout

3.3.8 Comparison of simulated and extracted results

Due to the effect of parasitics, the gain of the operational amplifier has reduced while there is an increase in the 3dB bandwidth during post-extracted simulation. The voltage swing result taken during post extraction simulation is well matched with the circuit schematic simulation results. Also, parasitics contribute to decreased unity gain bandwidth and phase margin in the post extraction simulation as compared to the schematic simulations

Similarly, the charging time has decreased due to drifting of charging time because of parasitic capacitances during the post extraction simulation. Since the transimpedance gain of the switched capacitor circuit is proportional to the charging time. The transimpedance gain has decreased in the post extraction simulation as compared to the circuit schematic simulation. The following table illustrates the comparison results.

Table 3-3 Comparison of simulation and post extraction results

	Simulated results	Extracted results
Operational Amplifier		
Gain	81.86dB	78.14dB
3dB bandwidth	8.9kHz	14.13KHz
Unity gain bandwidth	193.3MHz	153.56MHz
Phase margin	69.43 degree	57.95 degree
Output swing	2.7V	2.7V
Logic control circuit		
Charging time	612ns	603ns
Switched capacitor circuit		
Transimpedance Gain	121.2dB	120.69dB

Chapter 4

Conclusion and future work

A switched capacitor based trans-impedance amplifier is proposed for an optical sensing readout circuit. This switched capacitor based trans-impedance amplifier design has a large gain to accommodate current in the microampere range, low power consumption and low input referred noise. Correlated double sampling was employed to achieve very low input referred noise.

The switched capacitor based trans-impedance amplifier is designed using 0.18µm CMOS process technology. The switched capacitor based trans-impedance amplifier is realized using an operational amplifier and a logic control circuit to control the switches in the design. The chosen operational amplifier has a differential-to-single ended folded cascode structure with active current mirror load as the first stage to support high gain and the common source amplifier as second stage with a compensation resistor, capacitor pair to ensure stability.

The switched capacitor trans-impedance amplifier design was simulated using Cadence spectre. The circuit provides a trans-impedance gain of 121dB and a low power consumption of 7.2uW. A low input referred noise of 65.59fA/$\sqrt{Hz}$ could be achieved. A conventional transimpedance amplifier, namely, common gate amplifier was also designed and simulated using cadence spectre. The performance of the proposed

switched capacitor based transimpedance amplifier was compared with the conventional transimpedance amplifier.

The following table shows the superior performance of the switched capacitor based amplifier as compared to the conventional transimpedance amplifier.

Table 4-1 Comparison of conventional TIA and SC-TIA

	Common gate Amplifier -TIA	Switched capacitor -TIA
Gain	80.08dB ohm	121.3dB ohm
Input referred Noise	61.72pA/$\sqrt{Hz}$	65.59fA$\sqrt{Hz}$
Power	17.33uW	7.2uW
Technology	0.18um CMOS	0.18um CMOS

The low power consumption of the proposed circuit makes it suitable to incorporate to a lab-on-chip system where conserving battery life is essential. Moreover since the sensor current is quite small in the range of micro-ampere it tends to easily suffer from noise. Since the switched capacitor circuit has a low input referred noise, it is superior to other transimpedance amplifier designs. Also, since the sensor current is a pulse signal, the switched capacitor is ideal to handle pulsed signal .Thus the switched capacitor based transimpedance amplifier is best suited for this application.

The circuits have been fabricated in Magnachip CMOS process. The DRC, LVS and extraction of the layouts have been performed using cadence assura. The chip has 184 pads. The dimensions of the chip are 3.8mm X 3.8mm. The future work is to perform chip testing with a probe-station and test equipment to validate the performance of the switched capacitor based transimpedance amplifier. Our future goal would be to build a complete lab on chip system, where the switched capacitor based transimpedance amplifier could be integrated with optical sensor and supporting analog blocks such as post amplifier and buffer to test in real time a complete optical sensing readout circuit.

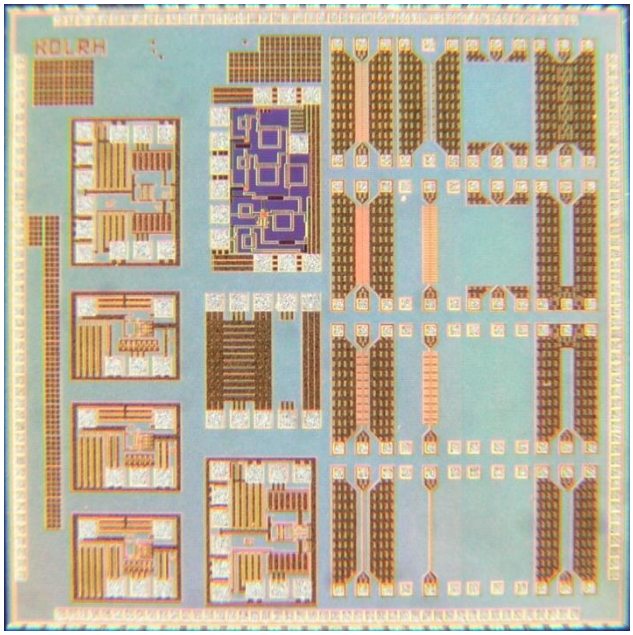


Figure 4-1 Chip

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