EXPERIMENTAL AND COMPUTATIONAL BOARD LEVEL RELIABILITY ASSESSMENT OF THICK BOARD QFN ASSEMBLIES UNDER POWER CYCLING

By

SUMANTH KRISHNAMURTHY

Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE IN MECHANICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

May 2016

Copyright © by Sumanth Krishnamurthy 2016

All Rights Reserved

Acknowledgements

I would like to begin by thanking Lord Almighty for giving me this wonderful opportunity and my family for being my source of strength and supporting me always.

I would like to my advisor and mentor, Dr. Dereje Agonafer for giving me a great opportunity to join his team. His guidance helped me tread this path and I have learnt so much from him. It was an honor to have worked with him.

I am grateful to Dr. A. Haji-Sheikh and Dr. Kent Lawrence for being my committee members and evaluating my thesis work.I would also like to thank Mr. Alok Lohia for his expert guidance during my work on Texas Instruments- SRC funded project.

I would like to extend my thanks to Ms. Sally Thompson and Ms. Debi Barton helped me greatly throughout my degree. A special thanks to all the members of EMNSPC team. It was great working with all of you.

April 8, 2016

Abstract

EXPERIMENTAL AND COMPUTATIONAL BOARD LEVEL RELIABILITY ASSESSMENT OF THICK BOARD QFN ASSEMBLIES UNDER POWER CYCLING

Sumanth Krishnamurthy, M.S.

The University of Texas at Arlington, 2016

Supervising Professor: Dereje Agonafer

Quad Flat No-Lead Package (QFN) is one of the latest cutting edge technologies that took the industry by storm due to its excellent electrical and thermal performance, compact size and low cost. Due to its compact size, QFN package is an ideal choice for handheld portable applications and where package performance is required. In QFN packages, the electrical contact to the Printed Circuit Board (PCB) is made through soldering of the lands underneath the package body rather than the traditional leads formed along the perimeter. However, using thick PCBs can be detrimental to the reliability of the package. The motivation of this work is to understand the reliability of such packages under power cycling and mitigate failures.

Fatigue failure of solder interconnects is a major reliability concern in electronic packaging. Traditionally, accelerated thermal cycling (ATC) have long been performed to assess reliability of solder interconnects. In real life applications, the actual package (or assembly) is experiencing Power Cycling (PC) apart from environmental temperature fluctuations, which exhibits non-uniform temperature distribution throughout the assembly having chip as the only heat source. In this study, the plastic work induced in the solder

joints is assessed by subjecting the package through power cycling. Plastic work can be used to estimate the number of cycles it requires to initiate and propagate the crack inside the solder joint. ANSYS workbench is used for Finite Element (FE) modelling of the package under study. The orthotropic material properties of the PCB for the ANSYS model are determined experimentally using Thermomechanical Analysis (TMA), Dynamic Mechanical Analysis (DMA) and Instron MicroTester. The analysis includes solving a model with the quarter symmetry QFN model under PC. The effect of Coefficient of Thermal Expansion (CTE) of the PCB is studied to assess the reliability of the package.

Table of Contents

Acknowledgements iii

Abstract iv

Table of Contents vi

List of Illustrations viii

List of Tables ix

Chapter 1 INTRODUCTION 1

1.1 Types of Packages 1

1.2 Quad Flat No-Lead (QFN) Packages 2

1.3 Board Level Reliability (BLR) Industry Standards 4

1.4 Power Cycling 6

1.5 Motivation and Objective 7

1.5.1 Motivation 7

1.5.2 Objective 9

Chapter 2 LITERATURE REVIEW 10

Chapter 3 MATERIAL CHARACTERIZATION 12

3.2 Thermo Mechanical Analyzer 14

3.3 Dynamic Mechanical Analyzer 16

3.4 Instron MicroTester 19

Chapter 4 MODELING AND SIMULATIONS 23

4.1 Introduction to Finite Element Modeling 23

4.2 Package Geometry 25

4.3 Modelling Methodology 33

Chapter 5 RESULTS 37

5.1 Temperature Distribution 37

5.2 Stress Distribution 39

5.3 Plastic work 40

5.4 Variation of PCB CTE 43

Chapter 6 CONCLUSION 45

6.1 Summary and Conclusion 45

6.2 Future Work 45

REFERENCES 47

BIOGRAPHICAL STATEMENT 50

List of Illustrations

Figure 1-1 Broad classification of different types of packages 1

Figure 1-2 Cross Section of a Generic QFN Package 2

Figure 1-3 Section View of a QFN Package 3

Figure 1-4 Cross-section of 16 Layered Board 8

Figure 3-1 TMA/SS6000 14

Figure 3-2 DMA7100 16

Figure 3-3 Young's Modulus Measurement (z-direction) 18

Figure 3-4 Instron MicroTester 19

Figure 3-5 Extensometer Mounted on the Sample 19

Figure 3-6 Dog Bone Sample [18] 20

Figure 3-7 Stress vs Strain Graph 22

Figure 4-1 QFN package configuration (mm) 25

Figure 4-2 Exposed thermal pad dimensions 26

Figure 4-3 Quarter Model of QFN on Thick Board 28

Figure 4-4 Symmetry Conditions 28

Figure 4-5 Modeling Methodology 33

Figure 4-6 Meshed Quarter Symmetry Model of QFN 34

Figure 4-7 Convective Boundary Condition 35

Figure 4-8 Power Cycling Plot 36

Figure 5-1 Temperature Distribution Top View 37

Figure 5-2 Temperature Distribution Isometric View 38

Figure 5-3 Stress Distribution in the Solder Joints 39

Figure 5-4 Plastic Work in the Solder Joints 40

Figure 5-5 Effect of Variation of PCB CTE on Plastic Work 44

List of Tables

Table 1-1 Thermal environments for electronic products 5

Table 3-1 TMA 6000 Test Results 15

Table 3-2 ASTM Standards for Dog Bone Sample Preparation 21

Table 3-3 Young's Modulus Measurement Test Results 22

Table 4-1 Package Dimensions 27

Table 4-2 Structural Properties of Package Components 29

Table 4-3 Anand's constant for SAC305 solder 30

Table 4-4 Thermal Properties of Package Components 31

Table 5-1 Energy Based Models 42

Table 5-2 CTE of the PCB 43

Chapter 1

INTRODUCTION

1.1 Types of Packages

The semiconductor industry is under increasing pressure to reduce power, down-size devices, leverage advanced technology and create multi-function devices. Semiconductor packaging must keep pace.

A few improvements which have already been noticed on this front are: increasing the number of pins, decreasing package size, and increasing circuit density so that more and more devices can be accommodated in a smaller area. Going forward, the demand for new packages with even greater sophistication will drive package innovation (Figure 1-1 below). [1]

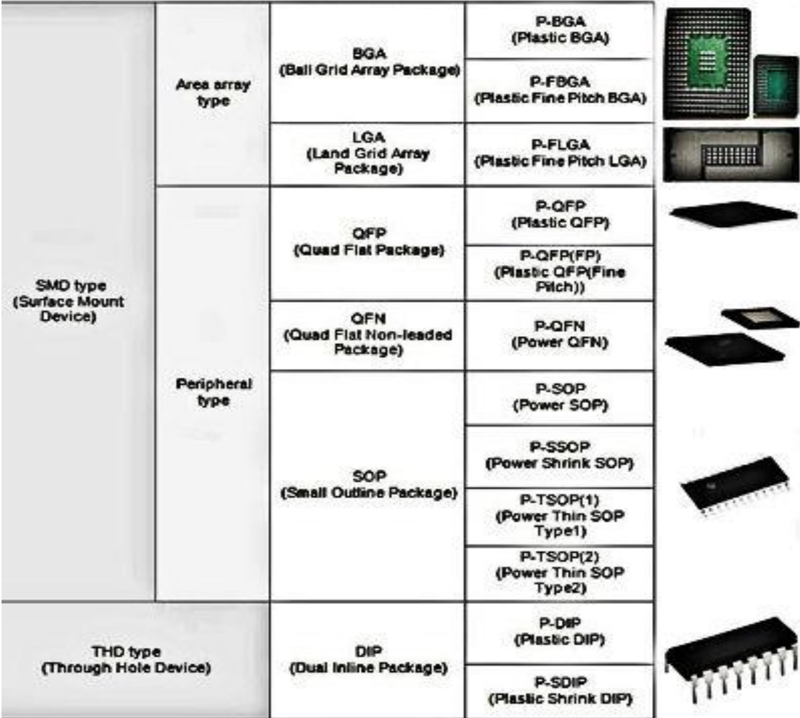


Figure 1-1 Broad classification of different types of packages

There is one more type of package (other than SMD and THD) called Contactless Package. PLLMC (plastic leadless module carrier package) is an example of contactless package.

1.2 Quad Flat No-Lead (QFN) Packages

As worldwide mobility increases, consumers wanting to "stay connected" in the digital world have demanded smaller and lighter products. Consumer-electronics manufacturers are striving to reduce product size to meet this demand. Smaller, thinner, and thermally enhanced packages help achieve product miniaturization. A performance analysis has shown that quad flatpack no-lead (QFN) packages have better thermal performance than dual in-line surface mount technology (SMT) packages. Other benefits of the QFN packages are low inductance and capacitance, small package volume, smaller board routing area, and no external leads, compared to conventional leaded packages. Figure 1-2 shows the cross section of a generic QFN package. [2]

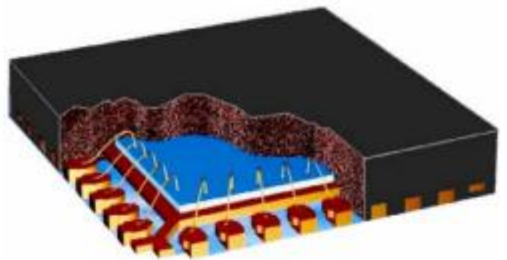


Figure 1-2 Cross Section of a Generic QFN Package

The QFN package is a thermally enhanced standard size IC package designed to eliminate the use of bulky heat sinks and slugs. This package can be easily mounted using standard PCB assembly techniques and can be removed and replaced using standard repair procedures.

The QFN package is designed so that the lead frame die pad (or thermal pad) is exposed on the bottom of the IC. This provides an extremely low thermal resistance (θ_{JC}) path between the die and the exterior of the package. Figure 1-3 shows the section view of a QFN package. [3]

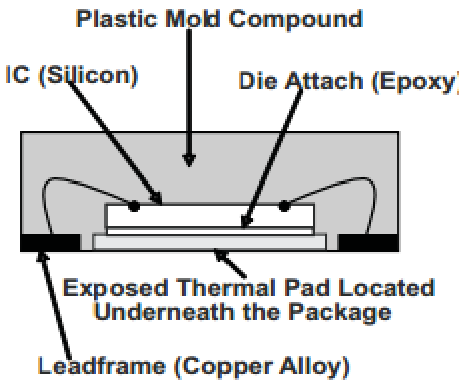


Figure 1-3 Section View of a QFN Package

This device package has gained popularity in the industry because of its superior thermal and electrical characteristics. The compact size of QFN package makes it an ideal choice for handheld portable applications and where package performance is required.

This work requires the use of QFN packages that were obtained from Texas Instruments (TI) for analysis. The properties of these packages are discussed in the later chapters.

1.3 Board Level Reliability (BLR) Industry Standards

Reliability can be defined as the ability of a system or component to perform its required functions under stated conditions for a specified period of time. To quantify reliability, “ability” should be interpreted as a “probability”. From this definition it is clear that all products always fail eventually. Indeed, a probability of zero failure during a certain amount of time is physically impossible, even for integrated circuit (IC) [4].

To estimate the reliability of the package, environmental stress test are used to simulate the end use environment conditions and to uncover specific materials and process related marginalities that may be experienced during operational life. Few consortiums such as Joint Electronic Device Engineering Council (JEDEC) and Institute for Printed Circuits (IPC) have adapted, documented and standardized many of the reliability tests [5].

These reliability tests are either focused on package level or board level. Package level or 1st level reliability tests are dedicated to the robustness of the package component materials and design to withstand extreme environmental conditions and does not consider the interconnects when it is mounted on board. Whereas for the board level or 2nd level reliability tests, stresses are examined on the solder joint of the surface mount package when mounted on board [6].

Table 1-1 shows different temperature ranges for various service environments for electronic products [5].

Table 1-1 Thermal environments for electronic products

Use condition	Thermal excursion (°C)
Consumer electronics	0 to 60
Telecommunications	-40 to 85
Commercial aircraft	-55 to 95
Military aircraft	-55 to 125
Space	-40 to 85
Automotive-passenger	-55 to 65
Automotive-under the hood	-55 to 160

1.4 Power Cycling

Power Cycling refers to the act of turning an electronic equipment or a device off and then turning it back on again multiple times.

A more realistic and accurate prediction of fatigue life in the second level solder interconnect can be conducted through power cycling. Fatigue is the dominating failure mechanism of solder interconnects and enhancement of its life is one of the major concerns for package designers and users. Conventionally, fatigue life is obtained empirically through accelerated thermal cycling (ATC) with hundreds of parts. To reduce development time and cost, virtual qualification attempts are made using numerical simulation tools, such as finite element analysis.

Modeling of life prediction is usually conducted for ATC condition, which assumes uniform temperature throughout the assembly. In reality, an assembly is subjected to Power Cycling i.e. non-uniform temperature with chip as the only source of heat generation. This non-uniform temperature and different coefficient of thermal expansion (CTE) of each component makes the package deform differently than the case of uniform temperature [7].

1.5 Motivation and Objective

1.5.1 Motivation

Modeling of life prediction is usually conducted for Accelerated Thermal Cycling (ATC) condition, which assumes uniform temperature throughout the assembly. In reality, an assembly is subjected to Power Cycling (PC) i.e. non-uniform temperature with chip as the only source of heat generation. This non-uniform temperature and different coefficient of thermal expansion (CTE) of each component makes the package deform differently than the case of uniform temperature [7].

Also, ATC is generally considered to be a conservative test method. This is generally true in the case of ceramic packages. However, it may not be true in the case of organic packages. Hence, the effect of power cycling on board level reliability is studied in this work.

Compact size, cost effectiveness, excellent thermal and electrical characteristics makes QFN package a popular choice in the industry. Although QFN package is widely used in handheld devices, some customers like defense and automotive require it for heavy industry application demanding thicker Printed Circuit Boards. A thick PCB consists of large number of Copper layers (>8) and large board thickness (>3 mm).

However, from the available literature we know that, as the thickness of PCB increases, there is a decrease in the reliability and fatigue life of the package. This is because the stiffness of the board increases and flexibility decreases resulting in more

transfer of stresses on the solder joint. Cross-section of a typical thick PCB with 16 copper layers, is shown in Figure 1-4.

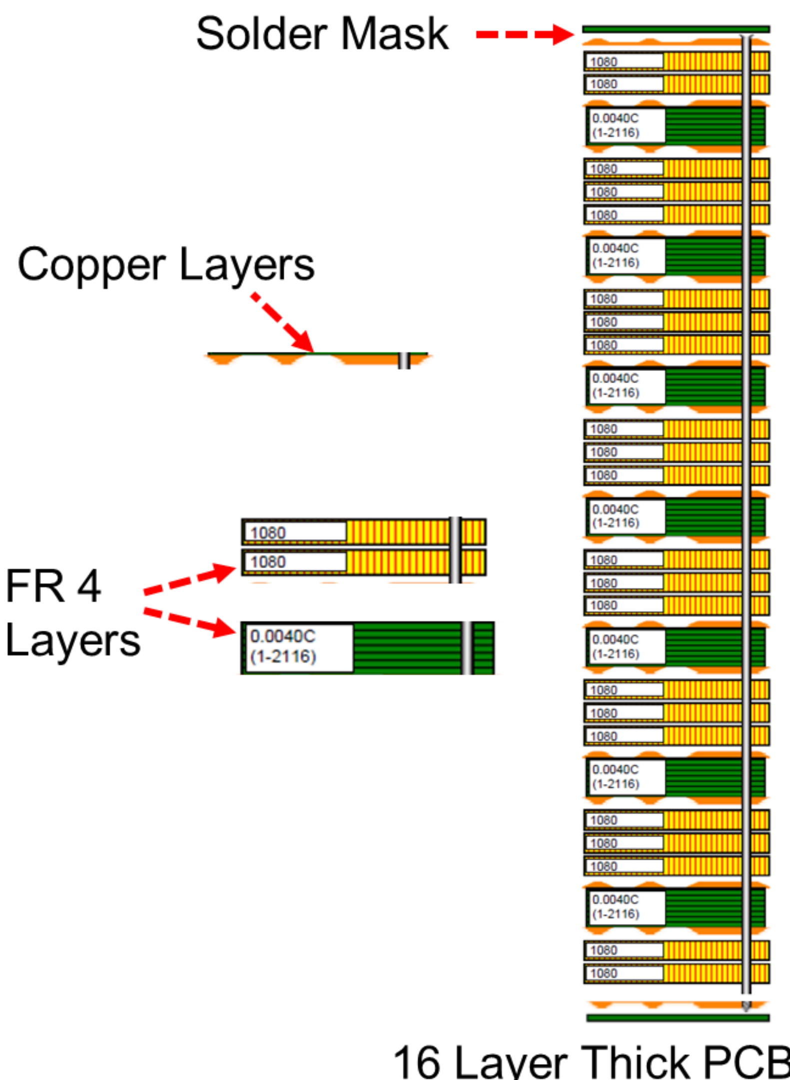


Figure 1-4 Cross-section of 16 Layered Board

1.5.2 Objective

The primary objective of this work is to analyze the failures observed in the QFN package with thick FR4 board under PC condition. Understand the root cause of the solder joint failures and methods to improve the mechanical reliability of the package thus making it to qualify the BLR industry standard for customers use.

Finite Element Analysis (FEA) is used to determine the fatigue correlation parameters such as plastic work and plastic strain. These parameters are a measure of the energy dissipated through plastic and creep deformation which is related to the damage done to the solder joint. Using these parameters, various energy based life prediction models can be examined.

The board level reliability of QFN packages on thick PCBs under Power Cycling is studied. Also, the CTE of the PCB is varied and the resulting plastic work in the critical solder joint is analyzed.

Chapter 2

LITERATURE REVIEW

Development of new electronic packages has focused on low cost, small size and high performance and high reliability. A lot of effort has been made for high reliability Power cycling is one of reliability requirements requested in package development. Compared to thermal cycling modeling, the work done on PC is very limited.

Typical work can be summarized as follows: Darveaux [8] (1995) published thermal and power cycling limits for plastic BGA. Ham et al [9] (2000) compared power cycling simulation to Moire interferometry measurements results, the deformation agreed well with finite element predictions. Syed [10] (2001) gave the predicting methodology within 25% accuracy for solder joint reliability in thermal, power and bend cycles. Myllykoski [11] (2002) studied and compared the thermal cycling and power cycling for BGA assemblies. Most of the above work considers the power cycling as a pure thermal-mechanical failure problem [12].

Yong Liu and Scott Irving [12] worked on power cycling with consideration for both electromigration and thermal mechanical failure. Two major investigations were made by them for the simulation: One is the classical solder joint fatigue (SJF) failure during the power cycling. This part consists of a non-linear thermal mechanical stress simulation for the fatigue life analysis. Another is the solder joint life with consideration of both migration and thermal fatigue life analysis. The criterion of migration was studied and was applied to the power cycling. The effects of current migration to the power cycling was discussed.

Birzer et al. [13] performed board level stress tests of QFN packages under temperature cycling, drop, bend and power cycling tests. They observed that the QFNs on thick boards with many metal layers are critical as compared to thin boards regarding temperature cycling reliability. Also, apart from the board thickness; board design, materials and surface mount technology (SMT) process has significant influence on the board level reliability of QFN packages [5].

This work deals with power cycling only as a pure thermal-mechanical failure problem.

Chapter 3

MATERIAL CHARACTERIZATION

In order to accurately determine the fatigue correlation parameters from finite element analysis, it is necessary to input actual material properties for each material. The thick PCBs were characterized for finding following material properties-

- Coefficient of Thermal Expansion (CTE)
- Young's Modulus.

To characterize the PCB, we use

- Thermo Mechanical Analyzer (TMA)
- Instron MicroTester
- Dynamic Mechanical Analyzer (DMA).

The TMA is used to obtain the Coefficient of Thermal Expansion (CTE) in all the 3 directions. Instron MicroTester is used to obtain the in-plane Young's Modulus (E_{xy}) and DMA is used to obtain the out-of-plane Young's Modulus (E_z).

Now, let us define Coefficient of Thermal Expansion (CTE) and Young's Modulus.

Coefficient of Thermal Expansion (CTE):

The change in length or volume of a material for a unit change in temperature is defined as The Coefficient of Thermal Expansion (CTE). The overall coefficient is the linear thermal expansion per degree Fahrenheit or Celsius. It is calculated by the change in length divided

by the quantity of the length at room temperature, multiplied by the change in temperature [14].

Generally it is given by-

$$\alpha = \frac{\epsilon}{\Delta T}$$

Where,

α - Coefficient of Thermal Expansion (ppm/°C)

ϵ - Strain (mm/mm)

ΔT - Temperature Difference (°C)

Young's Modulus (E):

Young's Modulus is an elastic property of a material which can be defined as the ratio of stress to strain.

$$E = \frac{\sigma}{\varepsilon}$$

ϵ - Strain (mm/mm)

E - Young's Modulus (N/mm^2)

σ - Stress (N/mm^2)

3.2 Thermo Mechanical Analyzer

Figure 3-1 TMA/SS6000

TMA measurements record changes caused by changes in the free volume of a polymer [15]. Experimentally, a TMA consists of an analytical train that allows precise measurements of position and can be calibrated against known standards. The sample is coupled to a temperature system with a furnace, heat sink and a temperature measuring device (Thermocouple). Fixtures to hold the sample during the test are commonly made of quartz due to its low CTE. The fixtures can be of expansion, three-point bending, parallel rate and penetration tests. TMA data determines the Coefficient of Thermal Expansion (CTE) and from the same set of data, Glass Transition Temperature (Tg) can be calculated. For an anisotropic material, the CTE will be different depending on which direction it has

been measured. For example, a composite of an epoxy will show distinct CTEs corresponding to the x, y, and z directions [16].

To obtain the CTE, TMA 6600 is used as a tool. 134mil PCB is placed in the holder with a Tension probe (made of quartz) with the test settings being as follows

- Start and end limit temperatures - ~+25°C to ~+125°C
- PCB specimen size - 4 x 4 x 3.45 mm
- Ramp Input - 5°C/min
- Start and End load - 100mN

An Aluminum sample is benchmarked to gain confidence in the test before measuring the CTE of the 134 mil PCB. The CTE is measured in all the 3 directions by changing the orientation of the sample.

Test Results:

Table 3-1 TMA 6000 Test Results

Direction	Coefficient of Thermal Expansion (ppm/°C)
x	16
y	16
z	84

3.3 Dynamic Mechanical Analyzer

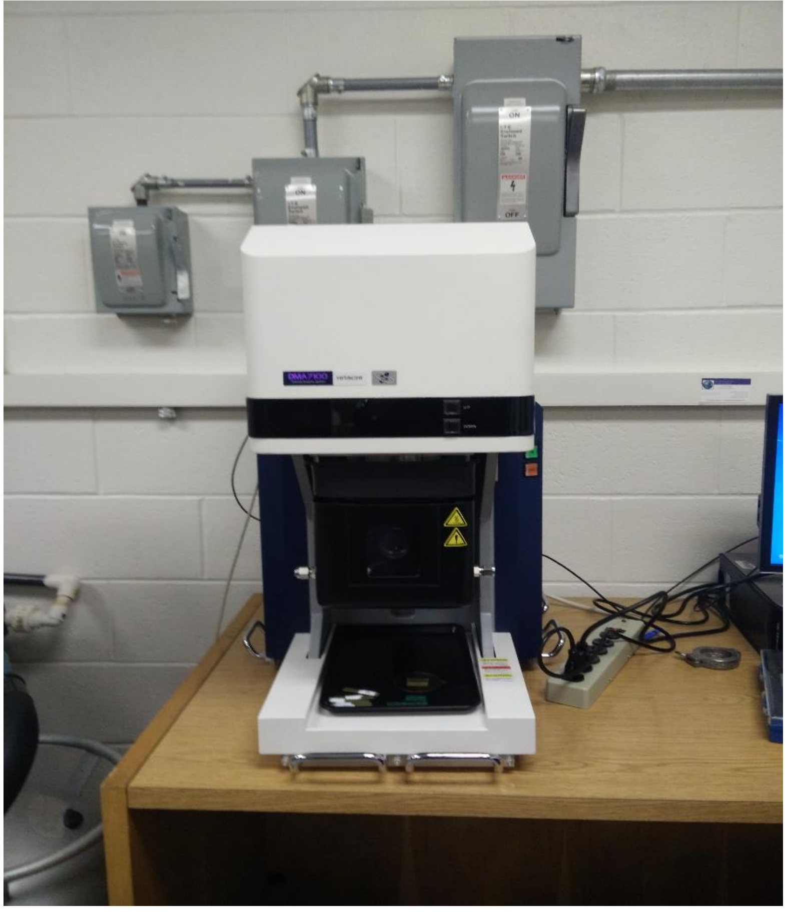


Figure 3-2 DMA7100

Dynamic Mechanical Analysis, otherwise known as DMA, is a technique where a small deformation is applied to a sample in a cyclic manner. This allows the materials response to stress, temperature, frequency and other values to be studied. The term is also used to refer to the analyzer that performs the test. DMA is also called DMTA for Dynamic Mechanical Thermal Analysis.

DMA works by applying a sinusoidal deformation to a sample of known geometry. The sample can be subjected by a controlled stress or a controlled strain. For a known stress, the sample will then deform a certain amount. In DMA this is done sinusoidally. How much it deforms is related to its stiffness. A force motor is used to generate the sinusoidal wave and this is transmitted to the sample via a drive shaft. One concern has always been the compliance of this drive shaft and the affect of any stabilizing bearing to hold it in position. [17]

To obtain the out-of-plane Young's Modulus, DMA 7100 is used as a tool.

- Temperature - ~+25°C
- Frequency - 0.01 Hz (~0 Hz)

Although DMA is generally used to measure the loss and storage modulus, at room temperature and at 0 Hz, the Young's Modulus will be equal to storage modulus as the storage modulus is the elastic response of the sample and the loss modulus is the viscous response of the sample. Since the temperature applied is not beyond the room temperature, the viscous response can be neglected. Viscous response will be prominent after the Glass Transition Temperature (T_g).

Test Results:

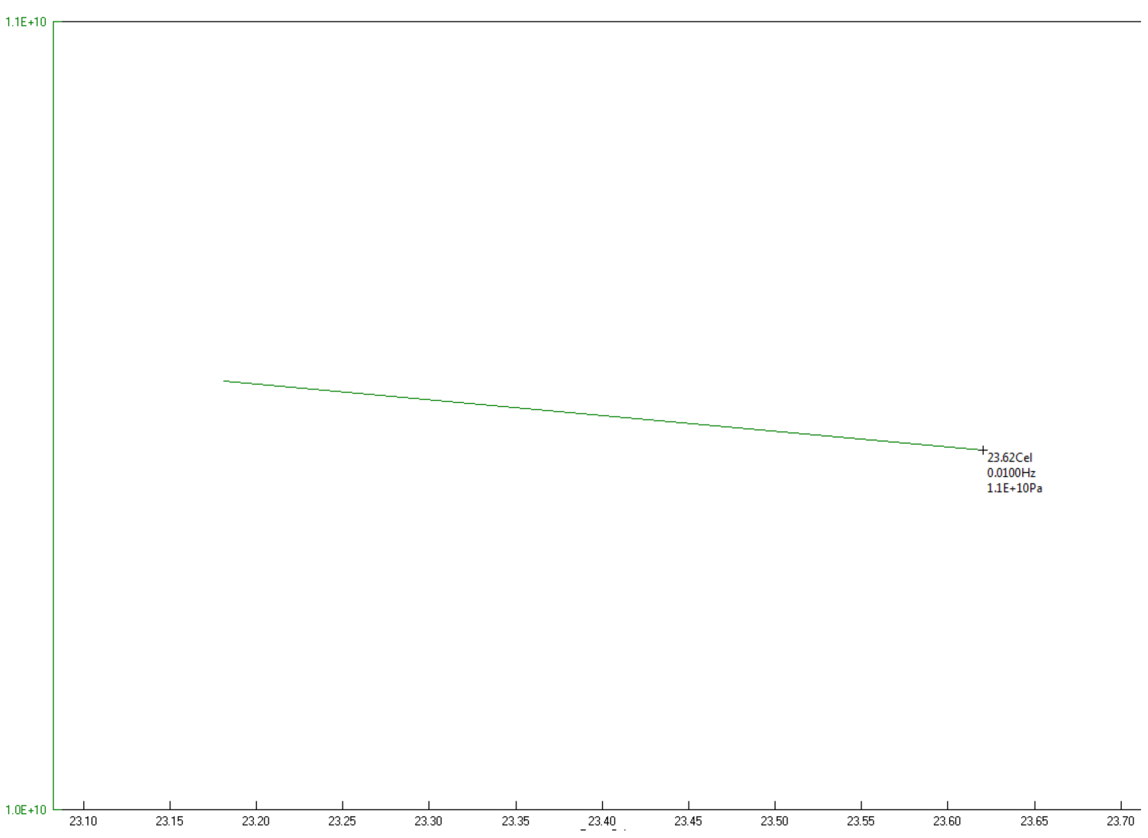


Figure 3-3 Young's Modulus Measurement (z-direction)

The value obtained for Young's Modulus Measurement (z-direction) from the DMA is 11 GPa.

3.4 Instron MicroTester

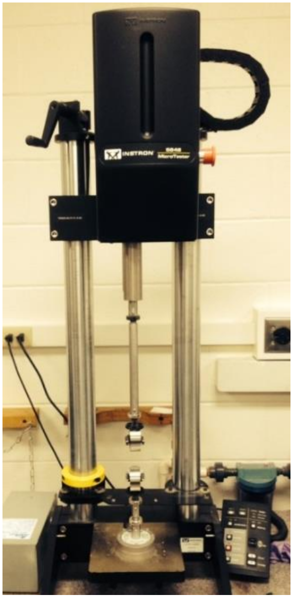


Figure 3-4 Instron MicroTester

Figure 3-5 Extensometer Mounted on the Sample

A tensile test is performed to determine the in-plane Young's Modulus for which an Instron MicroTester of 2kN load cell is used. To measure strain during sample extension, an extensometer is placed on the sample.

The extensometer along with Instron is connected to a computer which has a software that gives the force-displacement graph during the test. Stress is calculated by dividing the force from the cross-sectional area of the sample and strain is measured using the extensometer. The ratio of stress to strain gives the Young's Modulus of the sample.

ASTM standard is followed to prepare dog bone samples for Instron test.

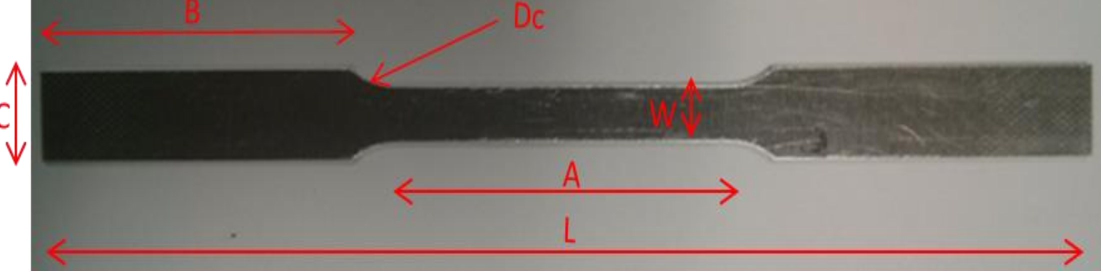


Figure 3-6 Dog Bone Sample [18]

The dimensions of the sample as referred from the ASTM standards are as follows:

Table 3-2 ASTM Standards for Dog Bone Sample Preparation

Dimensions	Value (mm)
L - Overall Length	100
C – Width of grip section	10
W – Width	6
A – Length of Reduced Section	32
B – Length of Grip Section	30
Dc – Curvature Distance	4
R – Radius of Curvature	6

Test Results:

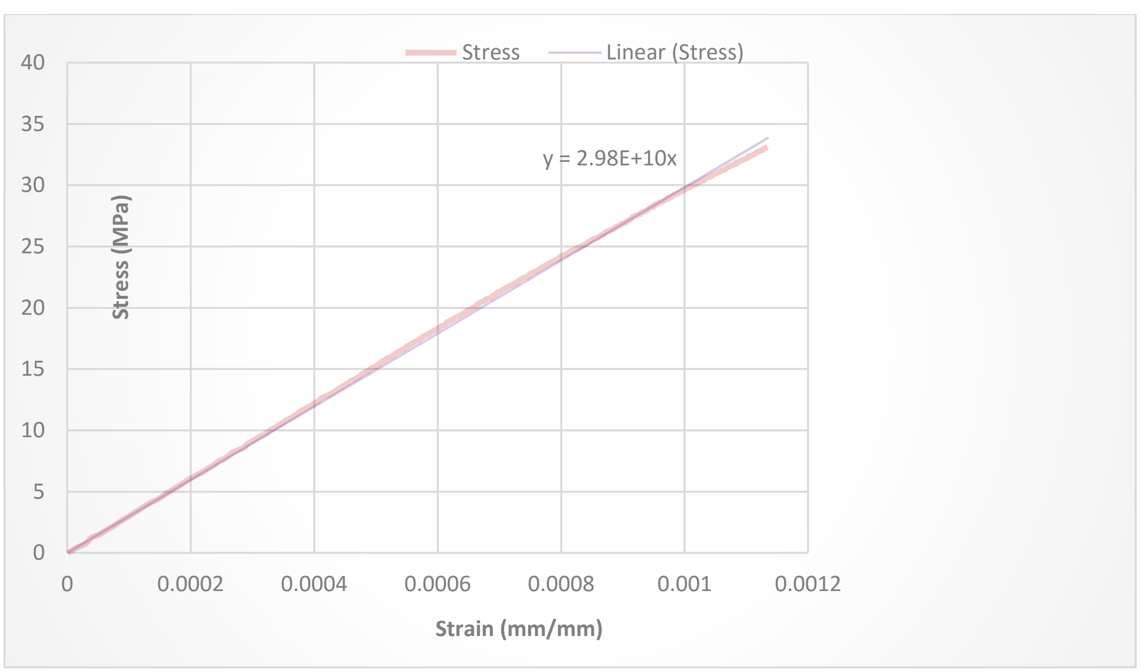


Figure 3-7 Stress vs Strain Graph

The value obtained for Young's Modulus from the Instron MicroTester is 29.8 GPa.

Table 3-3 Young's Modulus Measurement Test Results

Direction	Young's Modulus (GPa)
x	29.8
y	29.8
z	11

Chapter 4

MODELING AND SIMULATIONS

4.1 Introduction to Finite Element Modeling

The finite element method is a numerical method for solving problems of engineering and mathematical physics. Typical problem areas of interest in engineering and mathematical physics that are solvable by use of the finite element method include structural analysis, heat transfer, fluid flow, mass transport, and electromagnetic potential. This process of modeling a body by dividing it into an equivalent system of smaller bodies or units (finite elements) interconnected at points common to two or more elements (nodal points or nodes) and/or boundary lines and/or surfaces is called discretization. In the finite element method, instead of solving the problem for the entire body in one operation, we formulate the equations for each finite element and combine them to obtain the solution of the whole body.

Briefly, the solution for structural problems typically refers to determining the displacements at each node and the stresses within each element making up the structure that is subjected to applied loads. In nonstructural problems, the nodal unknowns may, for instance, be temperatures or fluid pressures due to thermal or fluid fluxes [19].

FEA consists of three steps:

1. Preprocessing:
    - A geometric model is created.
    - Elements and mesh are generated.
    - Material properties are input.

2. Solution:

    - Loads and boundary conditions are applied.
    - Output control and load step control are selected.
    - Solver is selected.
    - The solution is obtained.

3. Post processing:

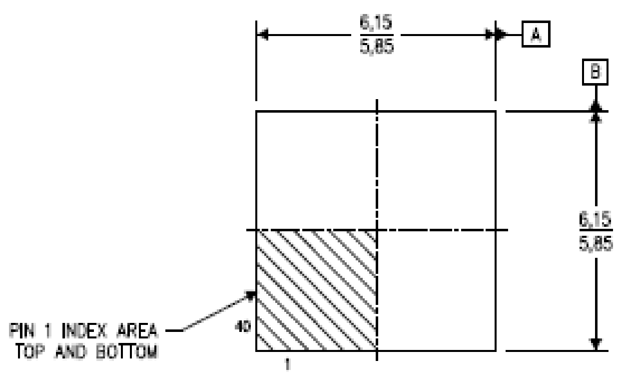
- Results are reviewed and listed as needed.

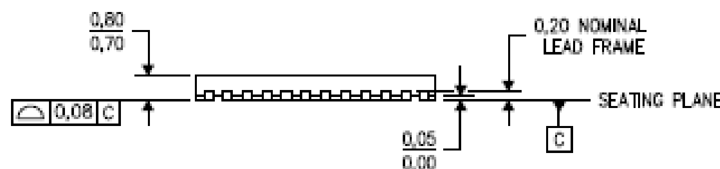
Assumptions:

- All materials considered linear elastic except solder.
- PCB is considered orthotropic.
- Solder is modeled as rate-dependent viscoplastic material using Anand's viscoplastic model.

4.2 Package Geometry

A 3D 6 x 6mm QFN package is modeled in ANSYS v16.1 using the package drawings. The package drawings are shown in Figure 4-1.





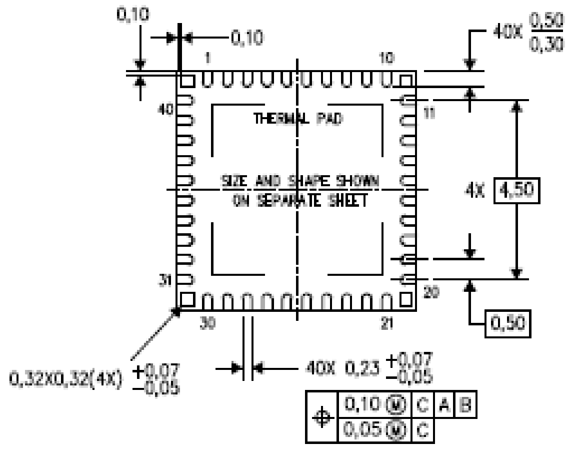


Figure 4-1 QFN package configuration (mm)

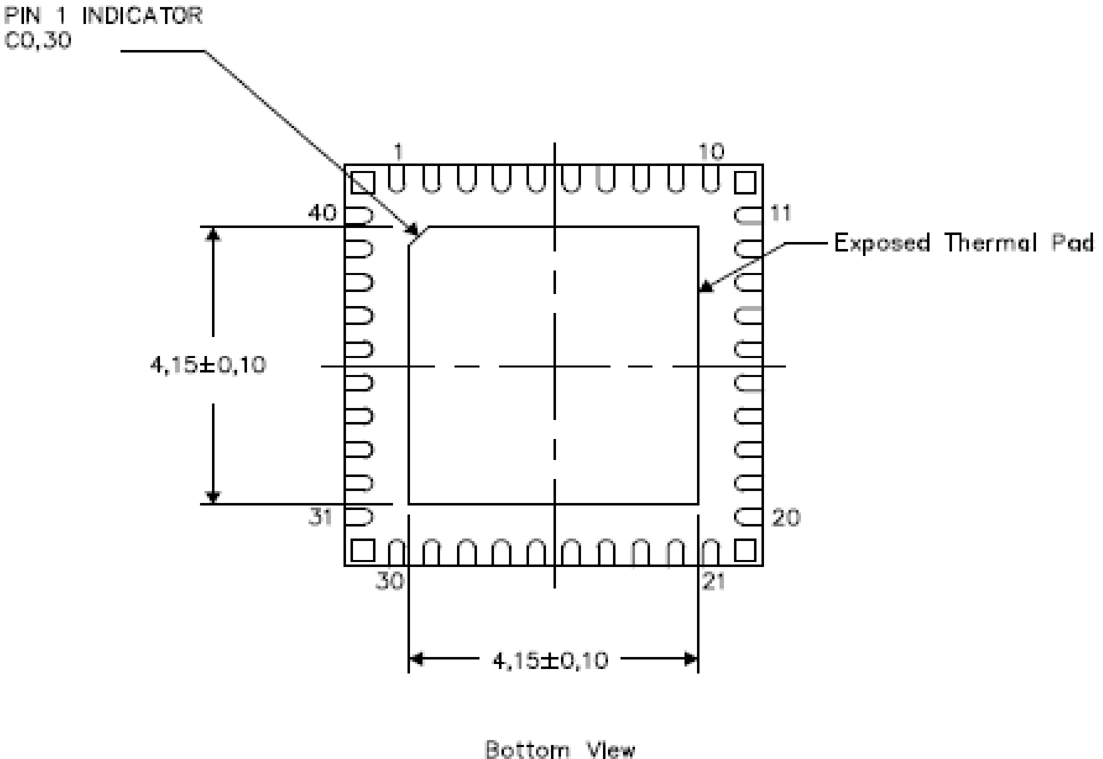


Figure 4-2 Exposed thermal pad dimensions

Figure 4-2 shows the exposed pad dimensions. This exposed thermal pad is designed to be attached directly to the PCB so that there is a low resistance to the heat path between the die and the PCB. The thermal pad is soldered directly to the PCB.

Table 4-1 shows all the package dimensions that were used for the ANSYS model.

Table 4-1 Package Dimensions

Component	Dimensions (mm)
Package	6 x 6 x 0.75
Die	4.315 x 3.245 x 0.19
Die Pad	4.8 x 4.8 x 0.1
Exposed Thermal Pad	4.15 x 4.15 x 0.1
Solder Thickness	0.3
Anchor Pin	0.32 x 0.32 x 0.2
Pitch	0.5
PCB	15 x 15 x 3.45

Figure 4-3 shows a 3D quarter geometry of 6 x 6mm QFN package. To save computational time, a quarter model is considered. This does not affect the accuracy of the results. Symmetric conditions are applied on the two faces as shown in the diagram figure 4-4.

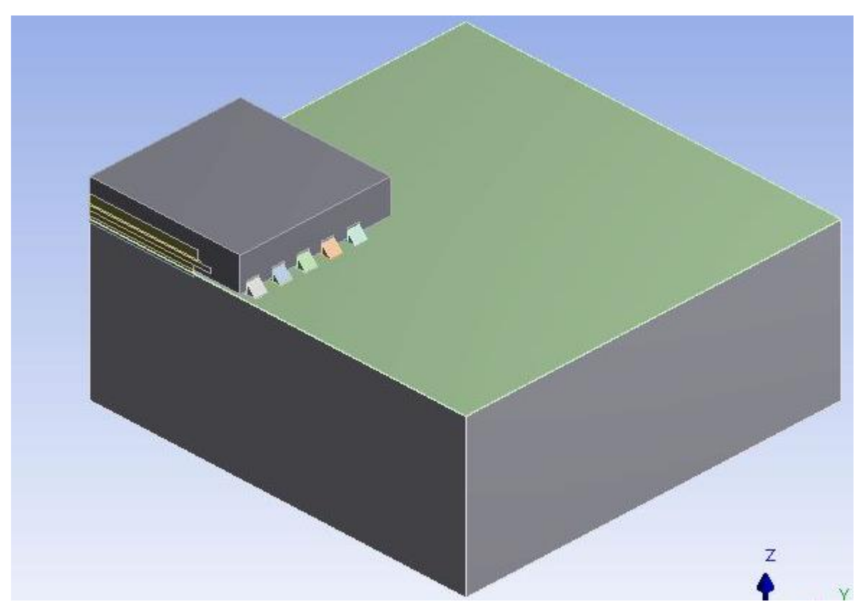


Figure 4-3 Quarter Model of QFN on Thick Board

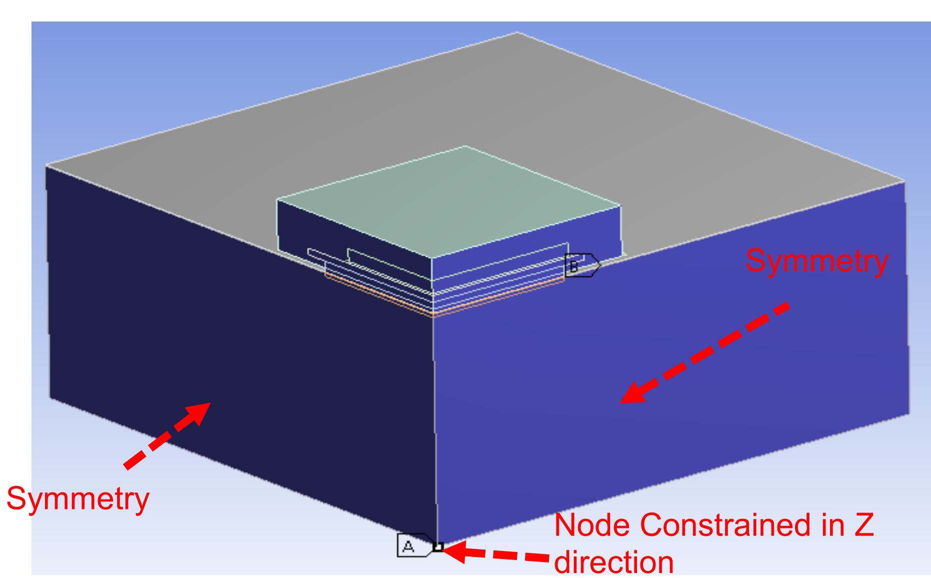


Figure 4-4 Symmetry Conditions

Table 4-2 shows the structural properties of all package components considered for this simulation.

Table 4-2 Structural Properties of Package Components

Material	Young's Modulus (GPa)	Poisson's Ratio	Coefficient of Thermal Expansion (ppm/°C)
Die	131	0.278	2.61
Die Attach	11.8	0.3	64
Lead frame	129	0.34	17
Epoxy Mold Compound	3	0.3	10.3
Exposed Die Pad	129	0.34	17

SAC305 is an alloy made of 96.5% tin, 3% silver and 0.5% copper. It is used as the material for solder. Anand's viscoplastic constitutive law is used to describe the inelastic part of the lead-free solder. This constitutive law follows the materials perspective that dislocation motion is the cause of both creep and plastic deformation, and combined them into inelastic strain [20]

The total strain is expressed as,

$$\varepsilon_{ij} = \varepsilon_{ij}^{e} + \varepsilon_{ij}^{in}$$

where ε_{ij}^{in} is the inelastic strain tensor.

The Anand's model consists of two coupled differential equations that relate the inelastic strain rate to the rate of deformation resistance.

The strain rate equation is represented by,

$$\frac{d\varepsilon_{in}}{dt} = A\left[\sin h\left(\xi\ \frac{\sigma}{s}\right)\right]^{\frac{1}{m}} \exp\left(-\frac{Q}{RT}\right)$$

The rate of deformation resistance is given by,

$$\dot{s} = \left\{ h_0 (|B|)^{\alpha} \frac{B}{|B|} \right\} \frac{d\varepsilon_p}{dt}$$

$$B = 1 - \frac{s}{s^*}$$

$$s^* = \hat{s} \left[\frac{1}{A} \frac{d\varepsilon_p}{dt} \exp\left(-\frac{Q}{RT} \right) \right]$$

where $\frac{d\varepsilon_{in}}{dt}$ is the effective inelastic strain rate, σ is the effective true stress, s is the deformation resistance, T is the absolute temperature, A is pre-exponential factor, ξ is stress multiplier, m is strain rate sensitivity of stress, Q is activation energy, R is universal gas constant, h_0 is hardening/ softening constant, $\hat{s}$ is coefficient for deformation resistance saturation value, n is strain-rate sensitivity of saturation value, and a is strain-rate sensitivity of hardening or softening. Anand's viscoplasticity law consists of nine material constants and is listed in Table 4-3 [5].

Table 4-3 Anand's constant for SAC305 solder

Anand's constants	SAC305
s_0 (MPa)	2.15
Q/k (K)	9970
A(1/sec)	17.994
ξ	0.35
m	0.153
h_0 (MPa)	1525.98
$\hat{s}$ (MPa)	2.536
n	0.028
a	1.69

Apart from the structural properties, we also need thermal properties of the package for the transient thermal analysis. Since these properties were not readily available, a reasonable assumption is made as most of these are standard materials (E.g.: Copper, FR-4, Silicon etc.).

Table 4-4 Thermal Properties of Package Components

Material	Thermal Conductivity (W/m/˚C)	Density (Kg/m^3)	Specific Heat (J/Kg/˚C)
Copper Lead Frame	390	8900	390
Die attach/ fillet	2	1910	920.9
Copper exposed pad	390	8900	390
PCB	173.77 (x) 173.77 (y) 0.64 (z)	1666	1369
Epoxy Mold Compound	0.8	1910	920.9
Die	140	2330	703
Solder Mask	0.25	1910	920.9
Solder SAC305	57	9630	167

As the PCB is a layered composite consisting of Copper and FR-4, it has orthotropic properties. The following equations were used to calculate the thermal conductivity of the PCB. [21]

$$\kappa_{In-plane} = \frac{\sum_{i=1}^{N} \kappa_i t_i}{\sum_{i=1}^{N} t_i} \qquad \kappa_{Through} = \frac{\sum_{i=1}^{N} t_i}{\sum_{i=1}^{N} t_i / \kappa_i}$$

where t is thickness of given layer

and κ is thermal conductivity of that layer

4.3 Modelling Methodology

- A model is created according to the package dimensions and material properties are assigned.
- A transient thermal analysis is performed with the die as the only source of heat generation i.e., a power cycle is applied to the die.
- The resulting temperature distribution of the body is then transferred to static structural.
- The thermal load is imported from transient thermal in static structural and plastic work is calculated and the critical solder joint is identified.

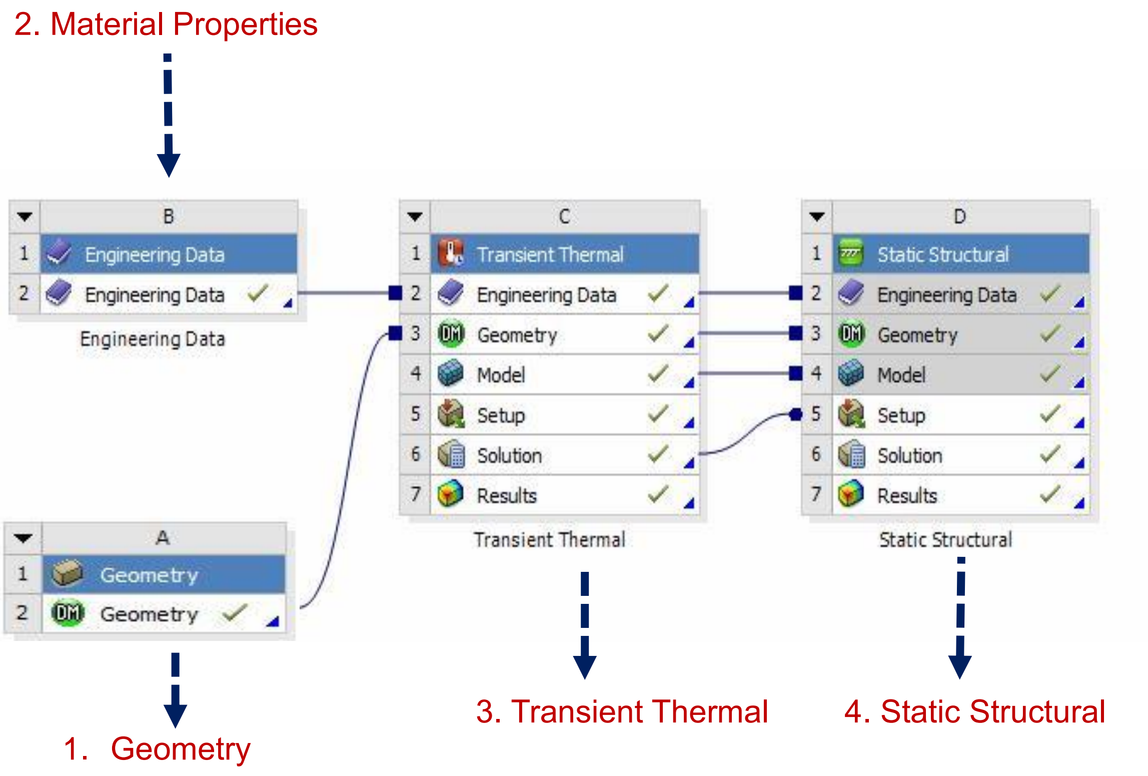


Figure 4-5 Modeling Methodology

Meshing:

The 6x6 40 pin QFN model is meshed with ~83k elements. Mesh refinement and mesh sensitivity analysis is performed to reach maximum accuracy. Since sub modeling technique is not employed, the model is meshed finely.

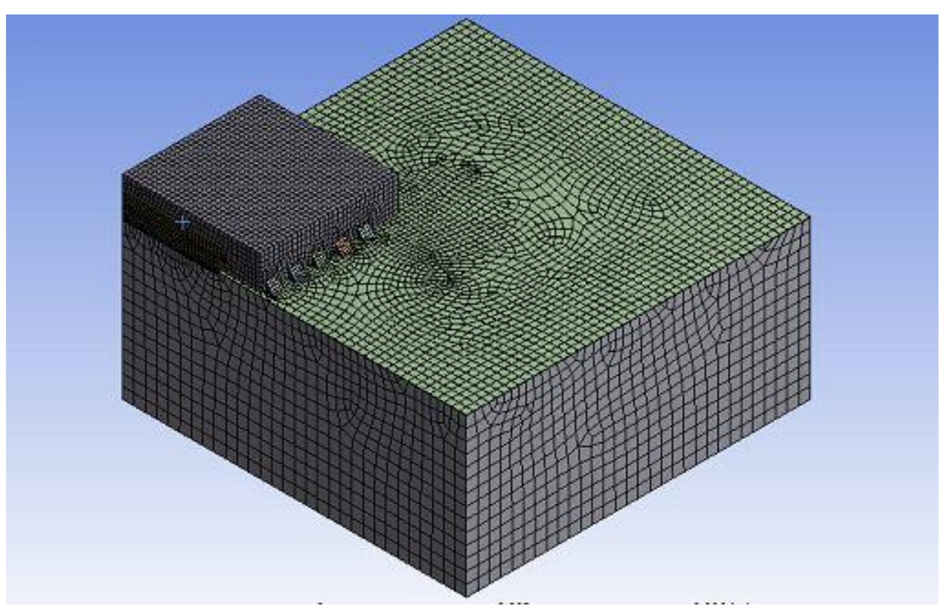


Figure 4-6 Meshed Quarter Symmetry Model of QFN

Boundary Conditions:

- Symmetry boundary conditions at quarter symmetry cut faces.
- Convective boundary condition on all the surfaces exposed to the environment.
- One center node constrained in z - direction.

The convective heat transfer co-efficient is chosen such that the maximum temperature in the package does not exceed 125˚C. The convective heat transfer co-efficient considered for this analysis is 23 W/(m² ˚C).

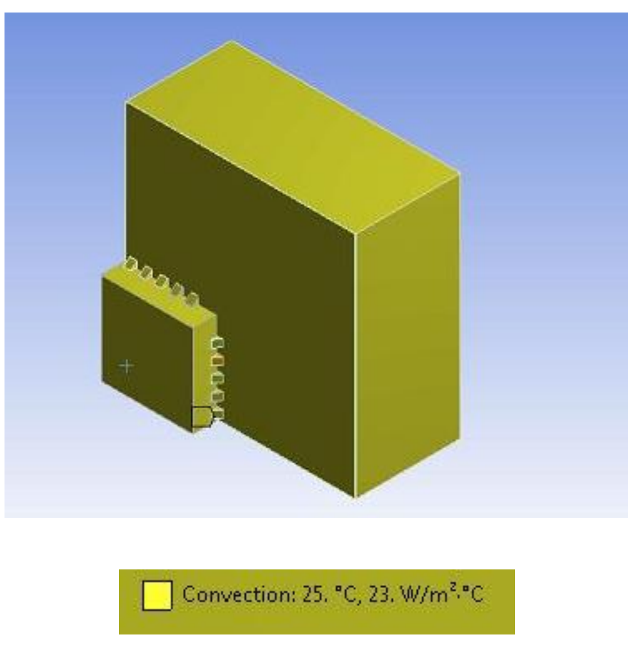


Figure 4-7 Convective Boundary Condition

Loading:

- 3 cycles of a very low power of 0.5 W is applied to the die with 800 seconds ON and 800 seconds OFF.

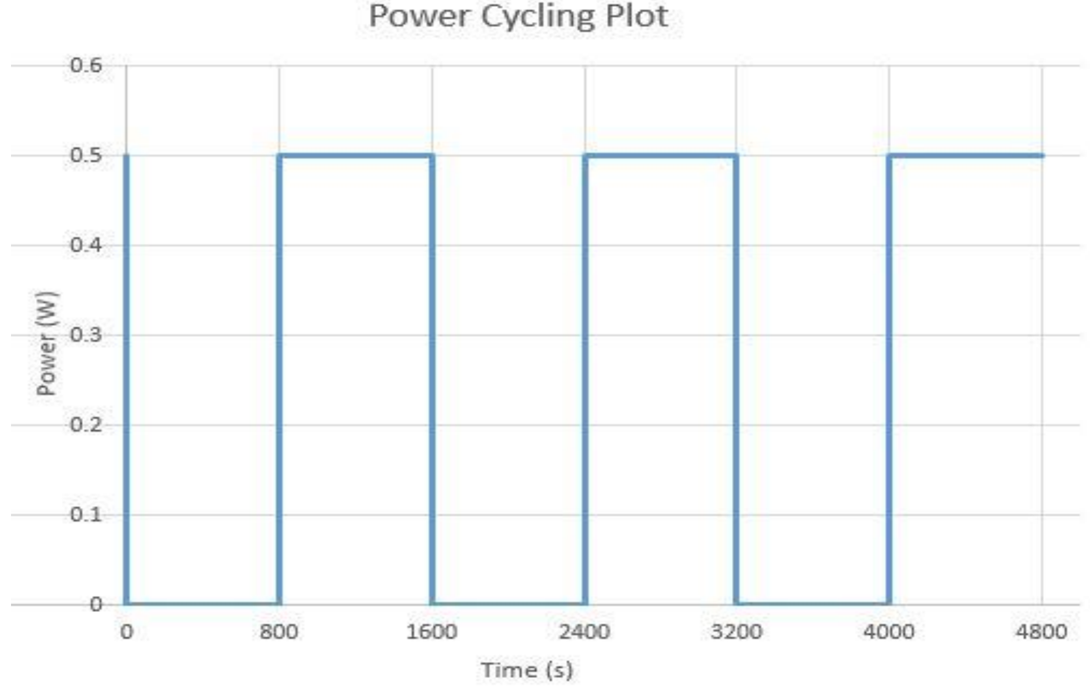


Figure 4-8 Power Cycling Plot

Chapter 5

RESULTS

5.1 Temperature Distribution

When 3 power cycles of 0.5W is applied to the die, there is a non-uniform heat distribution within the package. Figure 5-1 and Figure 5-2 show the temperature distribution in the package after 4800 seconds.

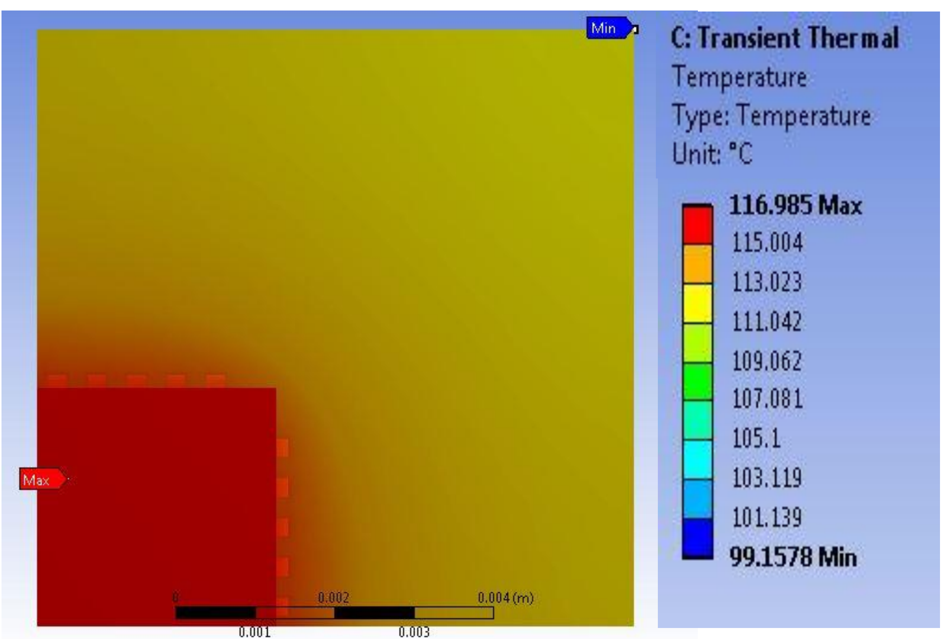


Figure 5-1 Temperature Distribution Top View

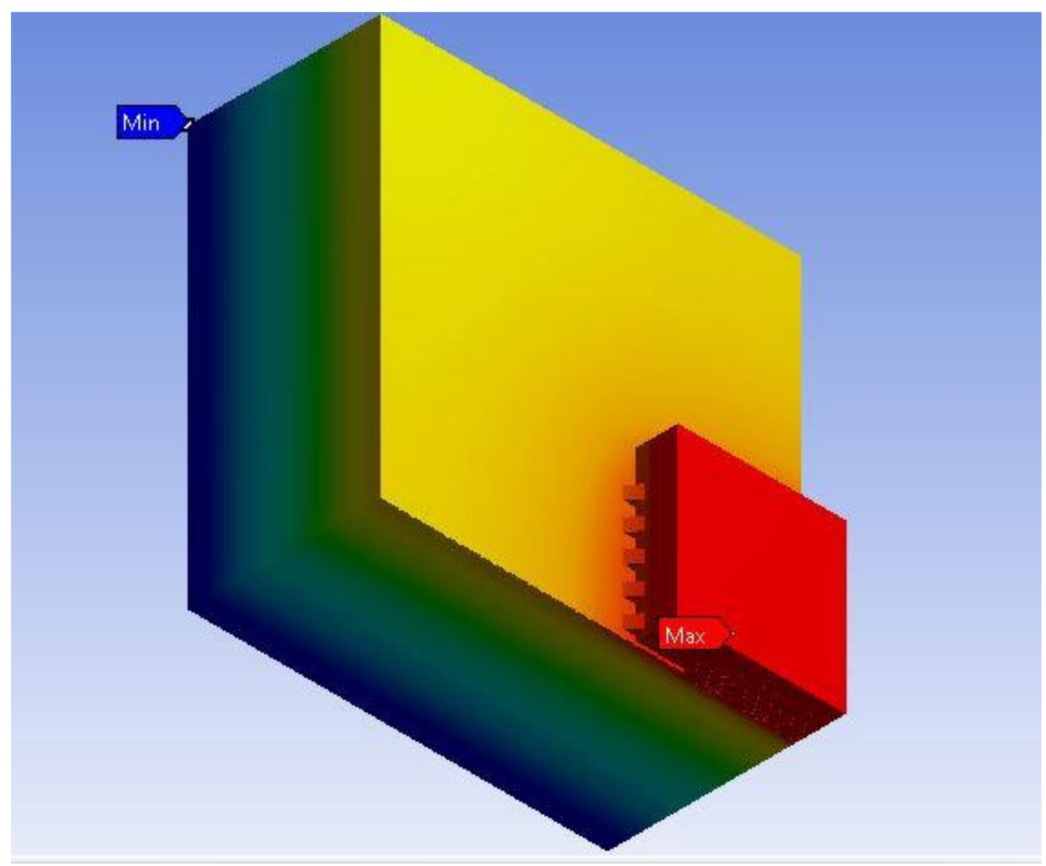


Figure 5-2 Temperature Distribution Isometric View

The maximum temperature in the package is 116.98˚C and the minimum is 99.15 ˚C. This non uniform temperature distribution is transferred to static structural module where the stresses induced because of the temperature distribution are analyzed.

5.2 Stress Distribution

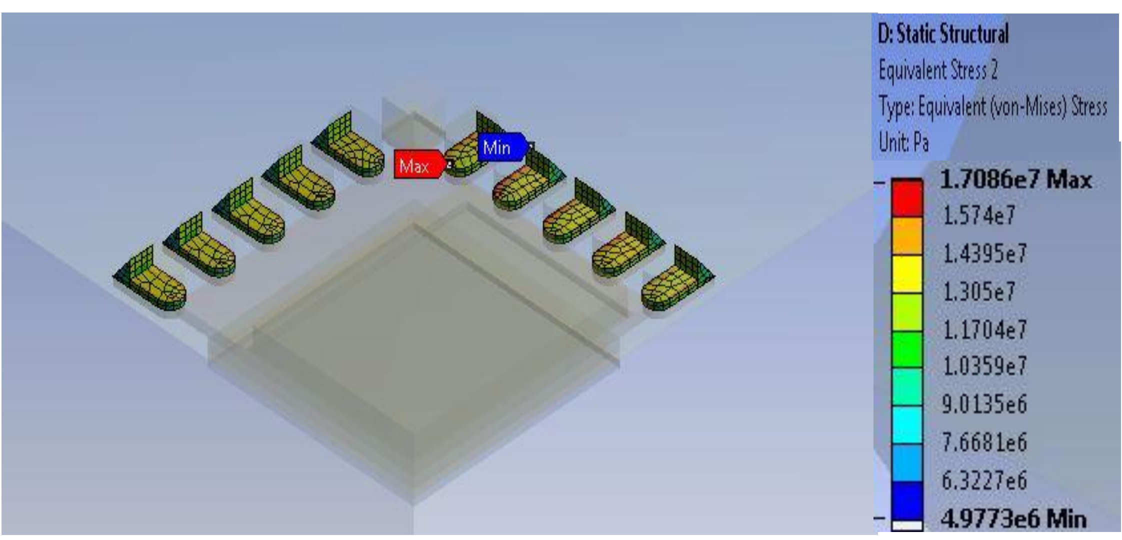


Figure 5-3 Stress Distribution in the Solder Joints

The maximum stress in the solder is 17.08 MPa and the minimum stress is 4.9 MPa.

5.3 Plastic work

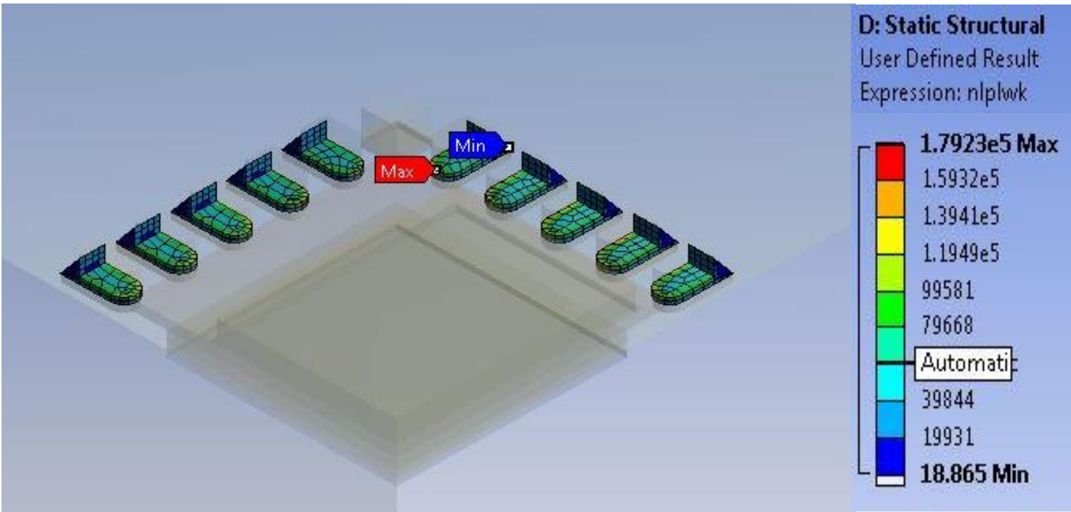


Figure 5-4 Plastic Work in the Solder Joints

The maximum volume averaged plastic work in the solder is 0.17 MPa. This is calculated by using a user defined results. The expression used to calculate plastic work is ‘nlplwk’. The maximum plastic work is seen in the corner solder joint and hence it can be considered as the critical solder joint.

Using this data, different energy based life prediction models are used to calculate the number of cycles to failure. This is used to correlate with the number of cycles to failure obtained from the experimentation using the same loading conditions which is beyond the scope of this work. The best life prediction model can be selected once the experimentation is done.

Energy Based Models:

Darveaux [22] and a lot other groups have shown that the increment of inelastic strain energy density per cycle can be used as a fatigue indicator. The inelastic strain energy density (inelastic strain energy per unit volume) is defined by

$$W^{in} = \int \sigma_{ij} \, d\varepsilon_{ij}^{in}$$

where σ_{ij} is the stress tensor and ε_{ij}^{in} in is the inelastic strain tensor. Since we are using Anand's constitutive law for the solder, the inelastic strain in this case is the viscoplastic strain.

Wei Sun et. al. [23] derived a new curve fitted fatigue correlation model for QFN packages based on simulated accumulated creep strain energy density and corresponding experimental results.

$$N_{cha} = 741.37 \, W_{acc}^{(-0.3902)}$$

where N_{cha} is the characteristic life (cycles to 63.2% failure) and W_{acc} (unit in megapascal) is the accumulated creep strain energy density per cycle.

Note the inelastic strain in this case is the creep strain because Schubert's hyperbolic sine constitutive law was used to describe the solder material behavior.

Schubert [24] proposed a fatigue model based on dissipated energy density during one thermal cycle and characteristic life. In this work we will examine the model for SAC solder. The equation for the model is given by

$$N_f = 345 \, W_{cr}^{(-1.02)}$$

where N_f is the characteristic life (cycles to 63.2% failure) and W_{cr} (unit in megapascal) is the strain energy density per cycle.

Morrow's [25] energy based model is used predict the low cycle fatigue life N_f in terms of inelastic strain energy density W_p (MPa) as shown below

$$N_f^n W_p = A$$

where n is the fatigue exponent and A is material ductility coefficient. These constants were determined by Pang [24] for SnAgCu solder alloys which will be used in the Morrow's model in this study. For temperature 125°C and frequency 0.001Hz, the constants n and A were taken as 0.897 and 311.7 respectively.

Syed [26] determined a life prediction model using strain energy density (or plastic work). The equation for the model is written below.

$$N_f = 674.08 \Delta W^{(-0.9229)}$$

The unit for plastic work (ΔW) is MPa or its equivalent MJ/m^3.

The number of cycles to failure can be calculated using different energy based life prediction models and the best model can be selected after correlating with the experimental results.

Table 5-1 Energy Based Models

Energy Based Model	Equation
Wei Sun's Model	$N_{cha} = 741.37\ W_{acc}^{(-0.3902)}$
Schubert's Model	$N_f = 345\ W_{cr}^{(-1.02)}$
Morrow's Model	$N_f^{0.897} W_p = 311.7$
Syed's Model	$N_f = 674.08 \Delta W^{(-0.9229)}$

It will be possible to select the best energy based model once the experimental data is obtained.

5.4 Variation of PCB CTE

The CTE of the PCB is varied to analyze its impact during Power Cycling. This CTE is obtained by removing the layers of the PCB and measuring it using the TMA. Since we are concerned purely about the effect of CTE on plastic work due to power cycling, we do not change any other property such as Young's Modulus when we run the simulations.

Trial #1: No Layers Removed.

Trial #2:1 Solder Mask and 1 Copper Layer removed on one side.

Trial #3: 1 Solder Mask and 1 Copper Layer on both sides.

Table 5-2 CTE of the PCB

Trial #	In-plane CTE	Out-of-plane CTE
1	16	84
2	11.87	64.15
3	10.3	48.48

Figure 5-5 shows the effect of variation of PCB CTE on the plastic work.

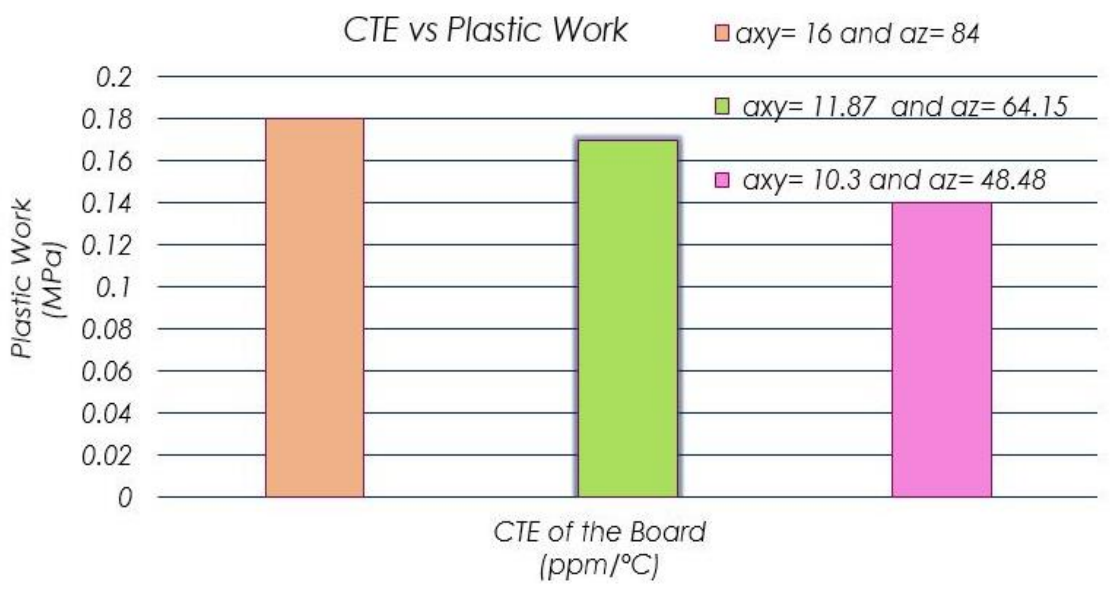


Figure 5-5 Effect of Variation of PCB CTE on Plastic Work

We can observe that as the CTE of the PCB decreases, the plastic work in the critical solder joint decreases. This is because the CTE mismatch between the mold compound and the PCB decreases which in turn decreases the stresses developed in the solder joint.

Chapter 6

CONCLUSION

6.1 Summary and Conclusion

In this study, a 3D Finite Element model of QFN package is analyzed to assess the board level reliability under power cycling. ANSYS Workbench 16.1 is used for Finite Element (FE) modelling of the package under study. The orthotropic material properties of the PCB for the ANSYS model are determined experimentally using Thermomechanical Analysis (TMA), Dynamic Mechanical Analysis (DMA) and Instron MicroTester. The plastic work induced in the solder joints is assessed by subjecting the package through power cycling. Plastic work can be used to estimate the number of cycles it requires to initiate and propagate the crack inside the solder joint. The analysis includes solving a model with the quarter symmetry QFN model under PC.

Power Cycling is performed, critical solder joint is identified and plastic work is obtained. CTE of the thick PCB is varied and its effect on the plastic work is determined. It is observed that plastic work decreases with decrease in the PCB CTE. This is because the difference in the CTE between mold compound and PCB decreases.

6.2 Future Work

The number cycles to failure under power cycling can be determined experimentally and the best fatigue model can be chosen. Also, PC can be coupled with ATC to predict the life cycle of the packages.

This work considers only the change in CTE after layer removal. The change in other properties such as Young's modulus are not considered. Therefore, impact of layer

removal of PCB on the reliability of the package under Power Cycling can be studied (i.e., considering the variation of all the properties). A Multi Variable Design Optimization can be performed for optimum material and geometrical properties.

REFERENCES

[1] Deepak Behera, Sumit Varshney, Sunaina Srivastava, and Swapnil Tiwari, "*A brief primer on embedded SoC packaging options*", Freescale Semiconductor, 2011

[2] Frank Mortan and Lance Wright, "*Quad Flat No-Lead Logic Packages*", Texas Instruments, 2004.

[3] Y. B. Quek, "*QFN Layout Guidelines*", Texas Instruments, 2006.

[4] G. Q. Zhang, *Mechanics of Microelectronics*, XIV ed. Springer, 2006.

[5] Tejas Shetty, "*Board Level Reliability Assessment of Thick FR-4 QFN Assemblies under Thermal Cycling*", The University of Texas at Arlington, 2014

[6]R. Rodgers, "*Cypress Board Level Reliability Test for Surface Mount Packages*", Cypress Seminconductor White paper, 2012.

[7] Izhar Z. Ahmed and S.B. Park, "*An Accurate Assessment of Interconnect Fatigue Life through Power Cycling*", Inter Society Conference on Thermal Phenomena, 2004

[8] Darveaux, R., Mawer, A., "*Thermal and Power Cycling Limits of Plastic Ball Grid Array (PBGA) Assemblies*", Proc. Surface Mount International, 1995, pp.3 15-326.

[9] Ham, S., Cho, M., Lee, S., "*Thermal Deformation of CSP Assembly During Temperature Cycling and Power Cycling*", 2000 International Symposium on Electronic Materials and Packaging. IEEE,2000.

[10] Syed, A., "*Predicting Solder Joint Reliability for Thermal, Power & Bend Cycle within 25% Accuracy*", Proceedings of the Electronic Components and Technology Conference, Orlando, Florida, May 2001.

[11] Myllykoski, P., Reinikainen, T. and Rodgers, B., "*Power Cycling Simulation of BGA Assemblies*", vo1.5, 2002, pp.95-130.

[12] Yong Liu and Scott Irving, "*Power Cycling Simulation of an IC Package: Considering Electromigration and Thermal-Mechanical Failure*", Fairchild Semiconductor Corp, Electronic Components and Technology Conference, 2003

[13] C. Birzer and S. Stoeckl, "*Reliability investigations of leadless QFN packages until end-of-life with application-specific board-level stress tests*," in ECTC, San Diego, 2006.

[14] *Coefficient of Thermal Expansion for Various Materials At Different Temperatures*, BAL Seal Engineering.

[15] R.Bird, C. Curtis, R.Amstrong, O. Hassenger, *Dynamics of Polymer Fluids*, 2nd ed., Wiley, New York, 1987.

[16] *Basics of Thermomechanical Analysis with TMA 4000*, Kevin Menard, Bruce Casel, PerkinElmer, Inc., Shelton, CT USA.

[17] *Dynamic Mechanical Analysis (DMA), A Beginner's Guide*, PerkinElmer.

[18] Abhishek Deshpande, "*Comprehensive Design Analysis of Thick FR-4 QFN Assemblies for Enhanced Board Level Reliability*", The University of Texas at Arlington, 2015

[19] Daryl L. Logan, "*A First Course in Finite Element Method*", Fifth Edition

[20] J. Pang, *Lead Free Solder: Mechanics and Reliability*, X ed. Springer, 2012.

[21] Electronics Cooling, "*Conduction heat transfer in a Printer Circuit Board*", May 1st, 1998.

[22] R. Darveaux, "*Effect of simulation methodology on solder joint crack growth correlation*", in ECTC, Las Vegas, 2000.

[23] W. Sun, W. H. Zhu, and R. Danny, "*Study on the Board-level SMT Assembly and Solder Joint Reliability of Different QFN Packages*", in EuroSimE IEEE, London, 2007, pp. 1-6.

[24] Schubert, R. Dudek, and E. Auerswald, "*Fatigue life models for SnAgCu and SnPb solder joints evaluated by experiments and simulation*," in ECTC, New Orleans, 2003, pp. 603-610

[25] J. D. Morrow, "*Cyclic plastic strain energy and fatigue of metals*," American Society for Testing and Materials Testing Standard ASTM STP 378, 1964.

[26] A. Syed, "*Accumulated creep strain and energy density based thermal fatigue life prediction models for SnAgCu solder joints*", in ECTC, 2004, pp. 737-746 Vol1.

BIOGRAPHICAL STATEMENT

Sumanth Krishnamurthy received his Bachelor's degree in Mechanical Engineering from Visvesvaraya Technological University, India, in the year 2013. He pursued his Master's in Mechanical Engineering in University of Texas at Arlington from Fall 2014. He joined the Electronics MEMS & Nanoelectronics Systems Packaging Center (EMNSPC) under Dr. Dereje Agonafer and developed a keen interest in reliability and failure analysis of electronic packages. His research interest includes reliability, fracture mechanics, thermo-mechanical simulation and material characterization. During his graduate studies, he was an integral part of the SRC funded project where he worked closely with the industry liaisons. Upon graduation, Sumanth plans to pursue his career in the field of electronic packaging.