Computational Analysis of Impact Loading on Wafer Level Chip Scale Packages Mounted on Printed Circuit Boards of Varying Thickness

by

Anik Mahmood

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DEDICATION

This thesis is dedicated to my family and friends who made everything possible. I would also like to thank all of them who inspired and motivated me to get going and finishing my degree.

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ABSTRACT

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Anik Mahmood, M.S.

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Supervising Professor: Dereje Agonafer

In the electronic industry one of the popular package is Chip Scale Package (CSP) due to its small form factor and low cost. To meet the need of new functionality and portability of the recent devices, CSPs' have been most favorable choice for a long time. On the other hand, with the miniaturization process of these portable devices there is a growing risk of drop impact failure in day to day use. It's not only the mechanical loading that is affecting the reliability of these devices but also thermal and thermo-mechanical loads are acting simultaneously. To analyze and ensure the reliability one should look through all the dimensions that can cause failure. The smaller the devices are getting they are becoming more prone to accidental drop and experience impact load, causing board interconnect failure by the repeatability of the drop occurrences. Therefore, the reliability of these products due to various loadings are being researched by taking multi-dimensional approach.

To ensure product quality and to integrate more complicated functionality in these devices reliability test is very important. To meet the robust and quick production demand, one of the popular choices for manufacturers is to complement drop/shock testing with the aid of computational simulation using Finite Element Analysis (FEA). In this work, a

comprehensive study has been carried out to investigate the effect of impact loading on the solder joints of Wafer Level Chip Scale Packages (WLCSP) component boards in environmental condition and also in elevated temperatures. In the environmental temperature the analysis approach was chosen as to observe the behavior of the solder joints failure during drop loading due to thickness and layer stack-ups difference in the Printed Circuit Boards (PCB). As drop test is dependent on modulus of elasticity and density of the materials they were experimentally determined for each board configuration. To understand the solder joint behavior under both thermal and mechanical load, drop test with respect to elevated temperature and using PCBs of varying thickness and layer stack-ups were simulated using Finite Element Method. The same WLCSP is used for different boards and subjected to drop test according to the JEDEC specifications [1]. To simulate the actual drop test modified Input G method, that is Direct Acceleration Input (DAI) method, was followed. The purpose of this study is to give an insight of how the impact loading is affected by the change of layer stack-ups and thicknesses of PCB mounted with small Wafer Level Chip Scale Packages (WCSPs) in the environmental and also in elevated temperatures. The comparison of the boards has been made to understand the effect of PCB layer stack-ups, thickness, and also temperature effect on the reliability of solder interconnects by considering the stress-strain generation that is induced in the PCBs during the drop test.

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INTRODUCTION

1.1 Wafer Level Chip Scale Package (WLCSP)

1.1.1 What is Wafer Level Chip Scale Package (WLCSP)

"The recent trends to portable and wireless on one hand, and commodity prices for all phones and PCs on the other hand, has brought on the need for much smaller Integrated Circuit (IC) and system-level packages that are also low in cost" (Tummala 2001) [2]. This vision gave a mission statement that is to develop cheap smaller sized packages which ultimately results in low cost chip scale packages such as Thin-profile Fine-pitch Ball Grid Array (TFBGA), Quad-Flat No-Lead (QFN) and Wafer Level Chip Scale Package (WLCSP).

Chip Scale Packages (CSP's) are defined as packages that are less than 1.2 times the size of the chip. This definition of CSP has been redefined as chip size package inferring a 1:1 relationship between chip and package size. (Philip Garrou) [3].

In another word, a chip scale package (CSP) is defined as any IC package which occupies a footprint area of no more than 50% greater than that of the chip it packages and which has a perimeter no more than 20% greater than that of chip it packages (Tummala 2001 [2]. In Figure 1.1 the size comparison is shown below.

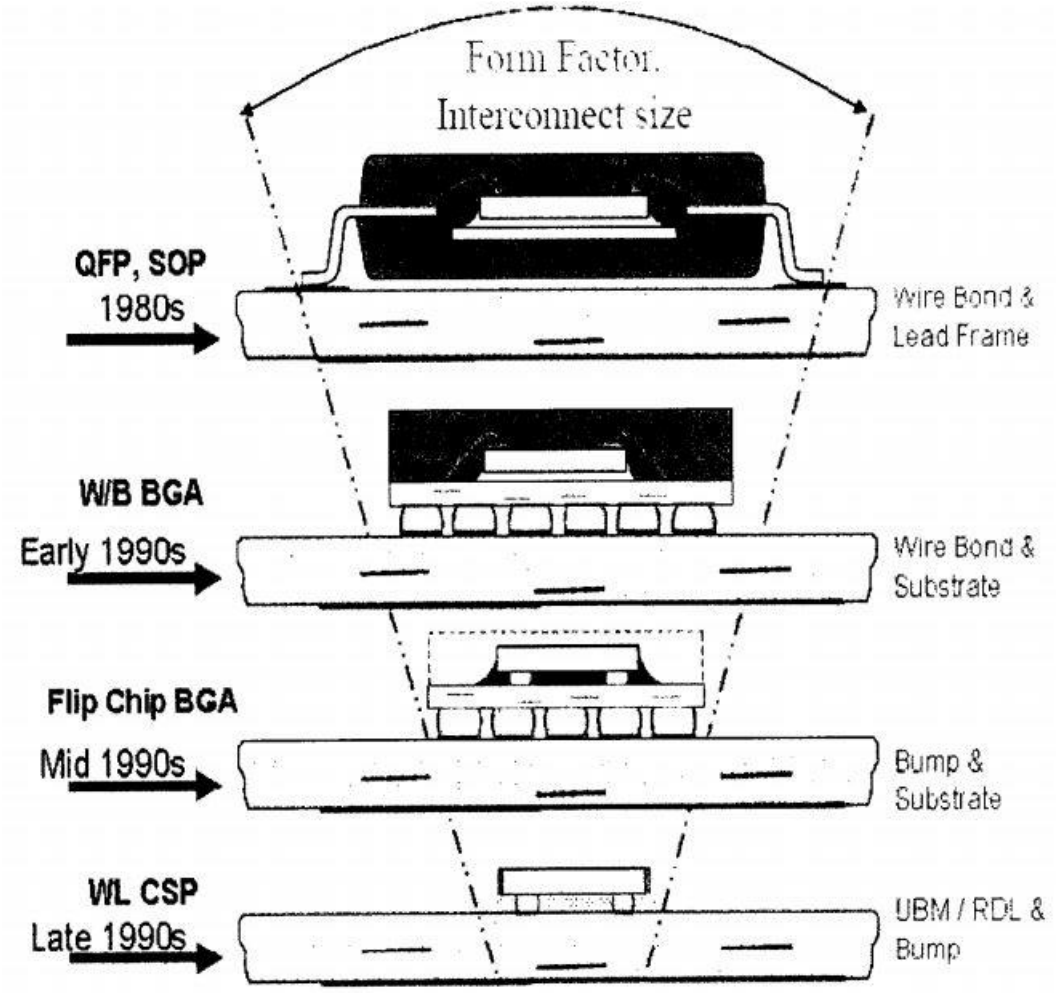

Figure 1.1: Size Comparison of Different Electronic Packages [4]

Wafer Level Chip Scale Package (WLCSP) denotes to the technology of packaging an integrated circuit at the wafer level. The traditional process of assembling individual units in packages is to integrate them after dicing from a wafer. This process is an extension of the wafer Fab processes. Here, the device interconnects and protection are accomplished using the traditional fab processes and tools. Finally, the device shapes as a die with an array pattern of bumps or solder balls attached at an I/O pitch that is compatible with traditional circuit board assembly processes (Freescale Semiconductor AN3846) [5]

WLCSP is one of the fastest growing segments in semiconductor packaging industry due to its advances in integrated circuit (IC) fabrication and the demands of a growing market for faster, better, smaller, yet less expensive electronic products with high performance and low-cost packaging (Xuejun Fan 2008) [6].

The main advantage of WLCSP is the small form factor because it is fundamentally a chip size package. Another advantage is its low packaging cost. The packaging cost per wafer in WLCSP remains a relatively constant percentage of the total IC cost, which means it becomes more cost-effective with decreasing die size or increasing wafer size (Xuejun Fan 2008). Figure 1.2 shows the cost comparison of different packages.

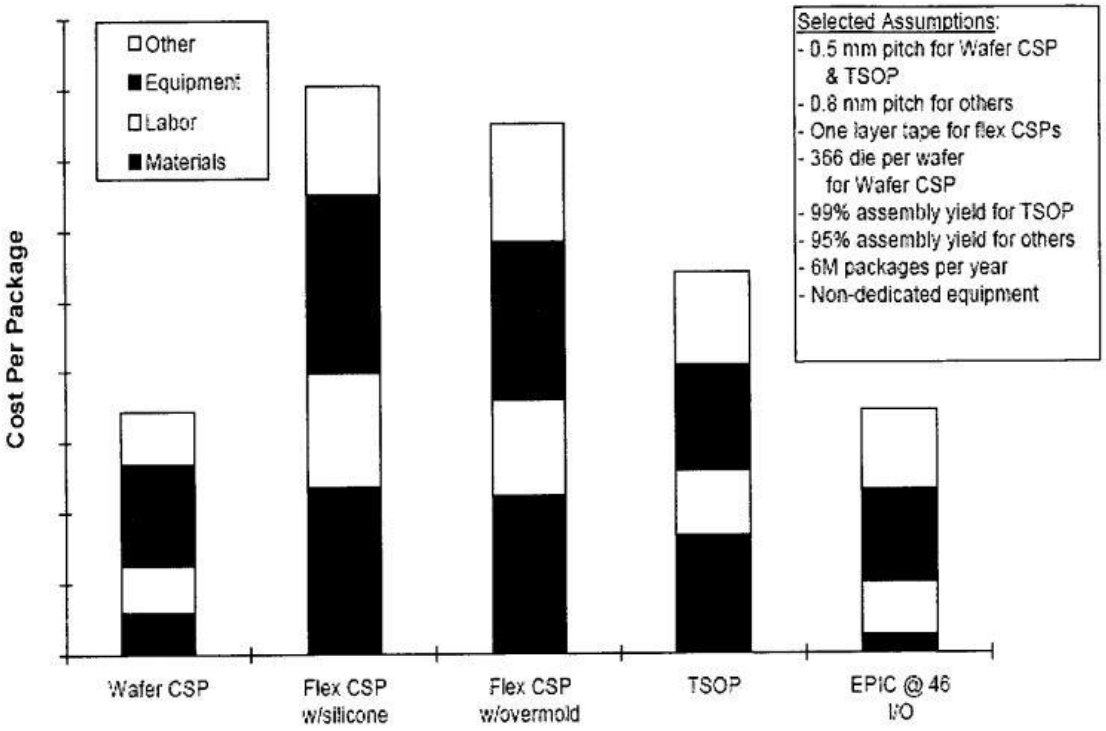

Figure 1.2: Cost Comparison of Different Packages [7]

1.1.2 Package Construction & Description

Wafer Level Chip Scale Packaging uses the processed bare die to have solder balls attached directly to the device, removing the need for external casing and wiring like Figure 1 3. The first layer of a WLCSP is of dielectric, followed by a Copper metal redistribution layer (RDL). This RDL works to re-route the signal path from the die peripheral to a solder ball pad. Then again, a second dielectric layer is deposited to cover the RDL metal, which makes the pattern for the solder ball array. The silicon die is buried with a nitride passivation layer, except for pad openings. The second layer of dielectric is covered by the Under Bump Metallization (UBM) deposition. Solder balls are attached onto each UBM stud. When finished, the device shapes as a die with an array pattern of solder balls, attached at a pitch compatible with traditional circuit board assembly processes. For the protection of the chip no external packaging material is required.

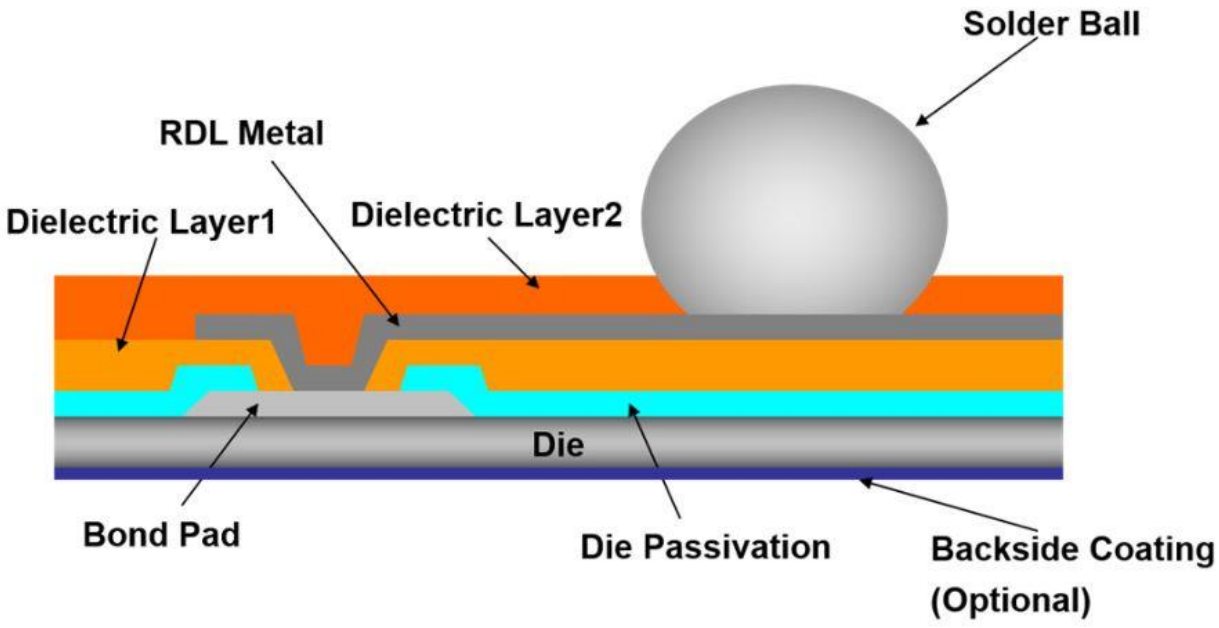

Figure 1.3: Typical WLCSP Construction

For this particular study, the WLCSP was chosen is Texas instruments (TI) YFF (S-XBGA-N49) as shown in Figure 1.4 [8]. There are total 49 solder balls/interconnects in a single WLCSP as a pattern of 7X7 array. The chip size is 2.8X2.8 mm and pitch is 0.40 mm. The top view of the 3D model for only the solder interconnects are shown in Figure 1.5. In this particular package no underfill was used by TI as they mentioned the board level reliability is good without underfill.

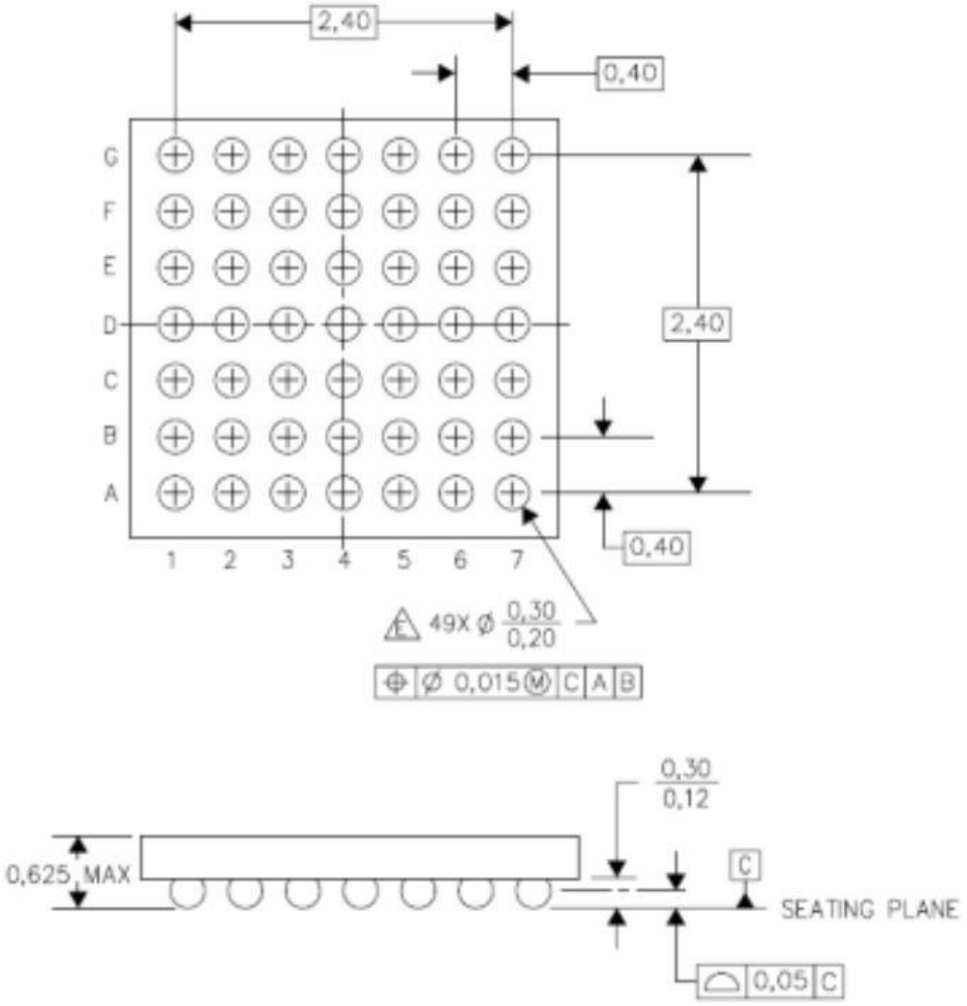

Figure 1.4: TI 49YFF Solder Ball Pattern [8]

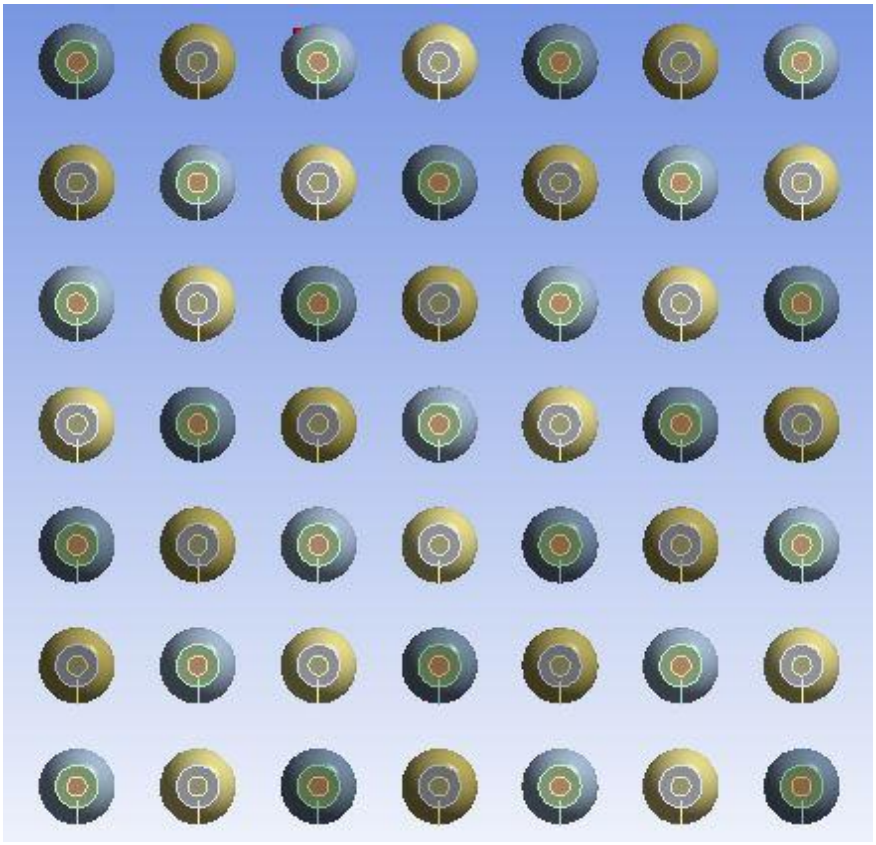

Figure 1.5: Solder Interconnect 3D Pattern

1.2 Motivation & Objective

1.2.1 Board Level Reliability (BLR)

In these days Board Level Reliability or BLR is a very common term used in the Electronic Industry which actually encompasses detailed methodologies for various mechanical and thermal test for the surface mounted Integrated Circuit (IC) components on PCBs guided by standardization community. BLR is a board based topic that determines the degradation behavior of the IC assembly on the PCBs. This BLR mostly targets the reliability issues of

the BGA, CSP, and QFN packages and try to characterize the life of these packages while in use in the customer's end. For BLR the distinctive requirement is that the components should be surface mounted to the test board. This ensures that, the emulation is identical to the thermos-mechanical stresses that the component would experience in the real time application. That is why the test board design, construction, material properties, test setup, and to monitor and list any slight variations/changes to the test methodology is very important to take care of.

BLR thermos-mechanical characterization includes the test of temperature cycling, thermal shock, mechanical shock, drop/impact test, vibration and mechanical bending test [9]. There are many ways to quantify the reliability and one of the most common way to describe it as the failure rate. The failure rate of the products vs time is shown in Figure 1.6 which is called the 'Bathtub Curve'.

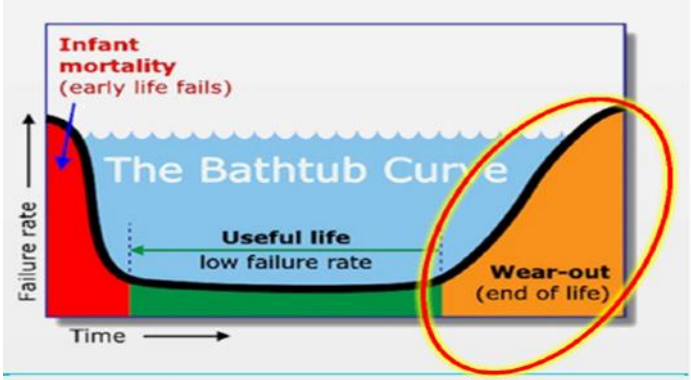

Figure 1.6: Reliability vs Time (Bathtub Curve)

The Infant mortality as seen from the curve is the region where the failures are counted in the early life during the fabrication, production, process and assembly defects. The Useful life region is counted for the actual life cycle of the products and is almost constant as the failed and poorly manufactured parts have been already screened out. The next part Wear-out refers to that time line where the products are started to permanently

fail because of the thermal and mechanical stresses. To ensure the reliability of the final products there are few associations such as Joint Electronic Device Engineering Council (JEDEC) and Institute for Printed Circuits (IPC) have been standardized and documented the procedures to perform many reliability tests. This study is scoped only to the JEDEC standard Drop Test.

1.2.2 Scope of The Study: Drop Reliability

Drop Test is a popular board level reliability test for the electronic industry and becomes an integral part of the reliability testing and is used to simulate the impact load conditions that may arise in the day-to-day use. Drop test is categorized under the mechanical reliability testing and according to Xin Qu et-al [10] reliability under thermal stress is not as critical as under mechanical stress like drop-impact. Therefore, product manufacturers especially the portable electronics industry are increasingly tending to perform drop reliability test which will accurately capture the end users' load conditions and the products can be designed to withstand the loadings. This is also bolstered by Wu et al, as the failure to drop impact is one of the most prevalent failure modes of portable electronics [11].

There are different methods to determine whether an IC assembly can withstand the drop impact requirement for the final product. This drop tests can be done in either Product level or Board Level. The product level test is done after the finalization of the IC assembly design and is the best method to measure the final device performance during drop impact. But to withstand this drop impact there is a need for study of design reliability and therefore board level test is performed and become very popular. The product level tests are usually done at the stage where there is less possibility to modify or change the preliminary stage design of the IC package assembly and for further optimization. Also the issues such as difference in board design, component locations, board support types and locations can be

avoided by conducting the board level drop test. A board level drop test only considers the input forces acting on the board and the package itself and do not consider the housing or any other parts of the final product assembly. In this way it becomes easier to generalize the test method for any kind of package-board assembly and to generate and compare results for any further modification. It is also very helpful to compare package performance if same inputs are using for the same boards or vice versa.

Board level drop shock reliability heavily depends on the experimental methods which is influenced by so many factors such the drop height, drop table, drop ground material, orientation of drop, and variations in product design etc. [12] [13]. The complex architecture of IC package makes it expensive, time consuming and difficult to test solder joint reliability and to find dominant failure criterion and location for different drop shock orientation. Also the smaller size of the solder balls makes it difficult to figure out the location of the failure, to measure the strain and displacement by mounting the strain gages on the location of the board and package interface.

Due to demand for short time to market, efficient reliability testing within little possible time has becoming very important for semiconductor and electronics industry. That's why there comes a faster and cheaper solution Finite Element Modeling (FEM) of the drop impact test which is validated by numerous researchers around the globe and is accurate reliable and that truly imitate the physics behind the actual drop test. Computer Aided Engineering (CAE) becomes highly demanding in this modern era for the reliability analysis of the IC packages. Thermal Cycling, Thermal Shock, Drop Testing, and other Thermo-mechanical reliability tests can be performed accurately with the aid of finite element modeling and can predict the failure mechanism, life cycle and other important parameters as close as the

real-time reliability tests. CAE is widely used because of its convenience for virtual prototyping and design for reliability. Before performing any real time test or build any prototype CAE helps to understand how the end product will behave in the real world situation. And as always the industry needs Faster, Better, and Cheaper solution there is no other alternative rather than CAE to beat the market need. Validated FEM models can be beneficial for the Design of Experiment studies like package geometry, material, board geometry, package board interconnection means and other parameters which facilitates the research and development sector to envision new design and solutions. According to Tee et al, FEM is useful to evaluate the feasibility of new package concept without any investment in prototyping and testing [14].

1.2.3 Objective of The Study

This work focuses on the parametric study of the various customer Boards used with the same WCSP described above. The main objectives are as followings:

1. Investigate the effect of board geometry (thickness) for the same WCSP package in drop test reliability.
2. Study the temperature effect during the drop test for variation in the board thickness.
3. Understand the deformation, strain and stress generation on the solder interconnect due to the changes in board thickness.
4. Identify the material properties of the different customer boards with Thermo-Mechanical Analyzer (TMA) and Universal Testing Machine (UTM).
5. Remove layers from the top of the board, experimentally figuring out the material properties and run simulation with these virtual/imaginary boards and investigate

changes in stress generation in the solder interconnect and to predict the overall assembly behavior due to drop occurrence.

6. Study the dynamic behaviors of the board by performing Modal analysis. Full transient dynamic analysis has been carried out to inspect the board strain histories at different locations.
7. Inspect the local stress generation at the solder interconnect by performing local model analysis.

To perform drop simulation JEDEC standard JESD22-B111 [1] has been followed throughout the entire work and ANSYS 16.01 was used as finite element modeling software.

Chapter 2

LITERATURE REVIEW

There has been a significant amount of research done on the drop impact reliability in the last decades. The JEDEC has published a step by step guide JESD22-B111 [1] to perform drop impact test and how to list all the failures and any other important observations obtained from the board level drop reliability test for the handheld electronics. Both experimentally and analytically researchers have been explored the dynamic behavior/response of the system subject to drop impact. A comprehensive study of the literature published related to the drop test is necessary to understand the various methodologies and findings that have been addressed to comprehend the drop reliability issues. Liam and Low offered a method to examine the drop impact response at product level at different impact orientations, drop height [13]. The drop impact behavior has been studied at the product level [12]. Tee, et al. [15] developed a life prediction model for the BGA assembly by performing comprehensive drop tests and failure analysis. They also employed the simulation methodology to correlate the drop failure and both analytically and experimentally and thus offered the life prediction model.

Previously, drop test computational method was reported by Wu [16] [17] who used explicit solver to simulate drop test at both component and product level. Zhu et al. [18] showed sub-modeling technique to perform BGA drop simulation. To date, various shock/impact modeling techniques have been developed to predict board dynamic strains and transient solder joint stresses. Earlier. explicit dynamics was the most widely used method to perform drop simulation [19]. There has been much effort employed to explore new ideas to perform drop simulation following new methodologies with the advancement of the CAE

software system and to reduce the modeling and computational time and expense. Equivalent layer models for solder interconnects has been employed by Lall, et al. to reduce the computational time [20]. Shell element modeling in global model was shown by Syed, et al. [21] and solid to solid sub-modeling technique for the half model was adopted by Dhiman, et al. [22]. Further, to reduce the computational time and modeling complicacy shell to solid sub-modeling technique using beam shell based quarter symmetry models was explained [23]. Though there are different methodologies to perform the simulation, Tee et al. [24] have shown an approach by using implicit solver to simulate drop test in Input G method which is less time consuming and does not require to model full experimental setup for the FEM simulation.

The effect of solder alloy compositions on drop reliability showed by Syed, et al. [25]. After the awareness of the Lead (Pb) free solder alloy industries shifted from SnPb to mostly SnAgCu (SAC) alloy and thus needed much more detailed analysis for the Board Level Drop Reliability (BLDR). And it has been found that SAC alloy performs poorer compare to the SnPb alloy solder interconnections. Since then several studies have been performed to improve the performance of the SAC alloy by adding micro-alloying additions [26] [27] or lowering the Ag content [28]. To improve the solder joint reliability during thermal cycling of the BGA and flip chip packages underfill material was developed and used. Later it has been found that it also improves the BLDR if correct underfill can be employed in the assembly [29] [30].

2.1 JEDEC Drop Test Method

A board level drop test method has been standardized by the Joint Electronic Device Engineering Council (JEDEC) in the report JESD22-B111 [1], to perform the BLDR on IC packages and evaluate the mechanical behavior. According to JEDEC standard test board consists of 15 components mounted on the top of the board in 3 rows and 5 columns array.

The JEDEC specified board is shown in the Figure 2.1 with all the dimensions. The main objective to introduce the general board design is to minimize the variation in terms of geometrical dimensions, parameters while performing the BLDR test.

The failure of the components according to this board setup has been studied by many researchers till now. Wong, et al. [31] identified principal reasons that lead to the failure of the interconnections due to this board setup as follows:

1. Due to the differential flexing of PCB and the Package the interconnections are elongated and bent
2. IC packages produce large inertia
3. The impact force generates stress waves on the whole PCB-Package assembly

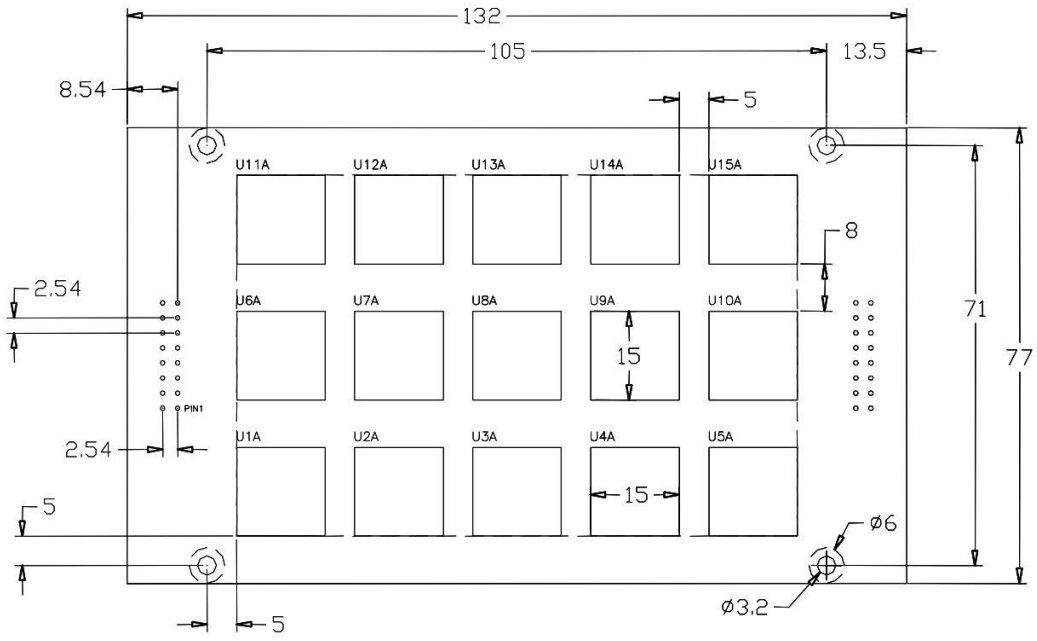

Figure 2.1: JEDEC Drop Board Construction

The excessive flexing of the board due to the drop impact creates differential bending on the package and acts as the main driver to fail the interconnects. The point to identify here

about the flexing is the board does not flex uniformly in each location and thus the more flexing part of the board fails the interconnect faster than the other regions. Therefore, the failure of the interconnects is not intrinsic to the components but they are location dependent. This JEDEC standard is thus helpful to understand the location dependent failure criterion of the solder balls.

The schematic for the JEDEC drop test equipment setup is shown in Figure 2.2. The board is mounted on the drop table by four screws around the four corners and the drop table goes down and strikes the rigid base. This screws act as standoff between the base plate and the board which allow the board to bend up and down upon the drop impact. This base should be of felt material according to JEDEC to produce the desired load conditions. The drop height is adjusted to produce certain G levels. The preferred G level is 1500 Gs and the input should be of half-sine wave impulse of 0.5ms as per JEDEC shown in Figure 2.3. According to JEDEC the board should be mounted on the base plate facing downwards (see Figure 2.2) and there shouldn't be any relative movement between the drop table and the board or the base plate.

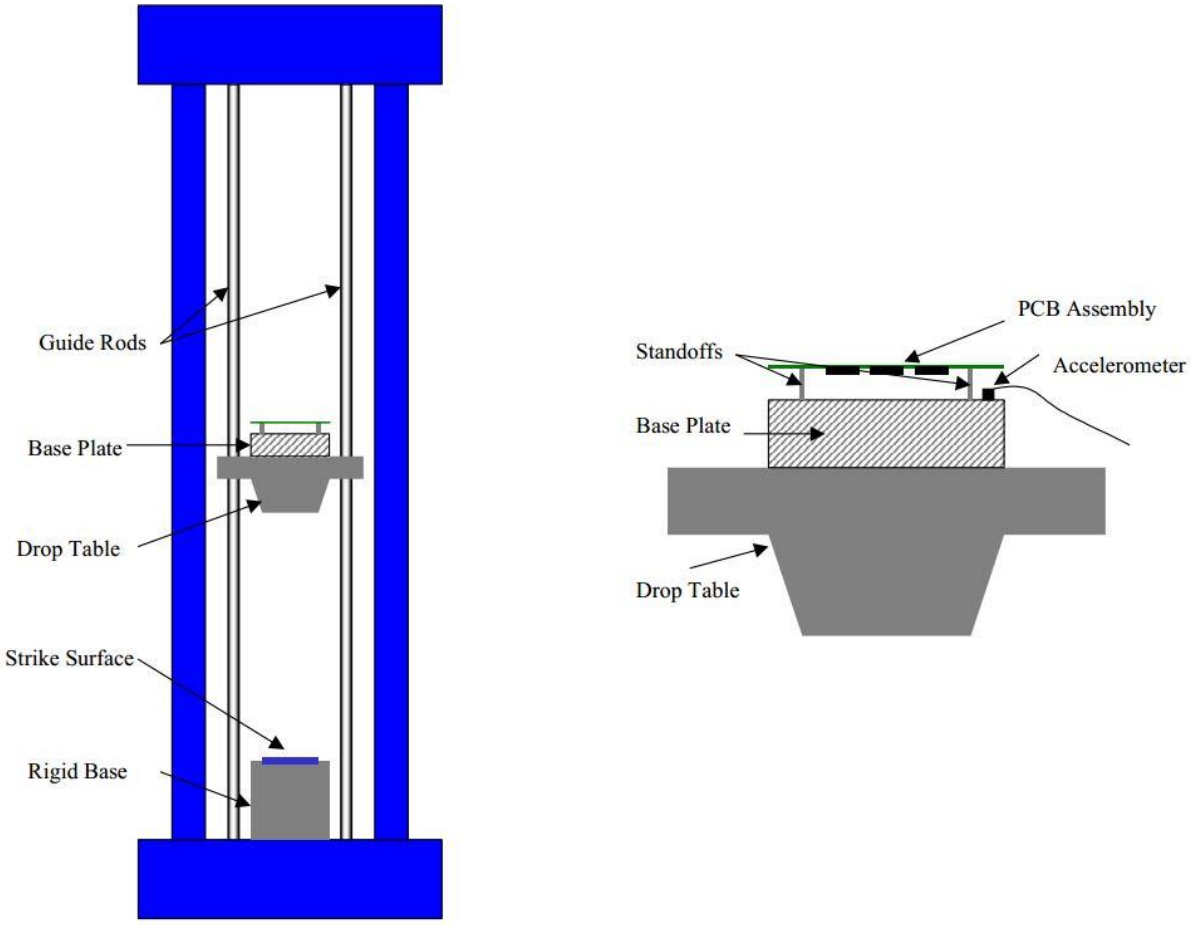

Figure 2.2: Schematic of JEDEC Drop Experimental Setup

$$A(t) = A_o \sin\left(\frac{\pi t}{t_w}\right)$$

$$\sqrt{2gH} = \frac{2A_o}{C}\frac{t_w}{\pi}$$

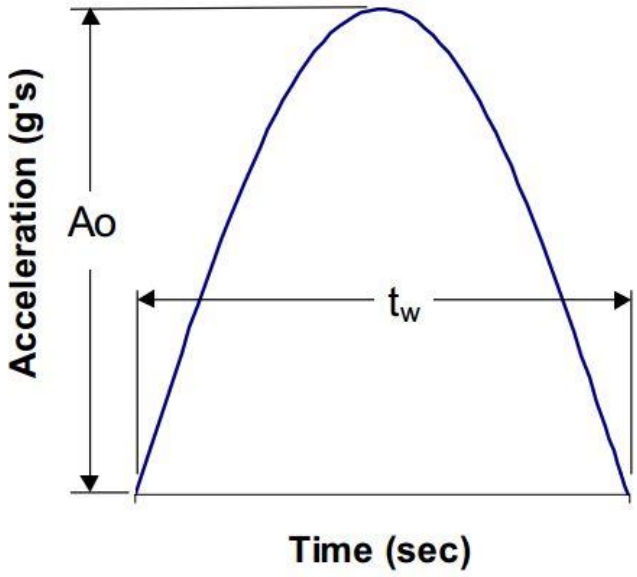

Figure 2.3: Drop Acceleration Input

Researches have been reported from the experimental conclusions that there are mainly three modes of failure of interconnections. These failures occur due to the crack propagation at different locations upon certain level of drop impact force [32] are shown in Figure 2.4.

1. Package-solder interconnect interface failure
2. Board-solder interconnect failure
3. Board via crack

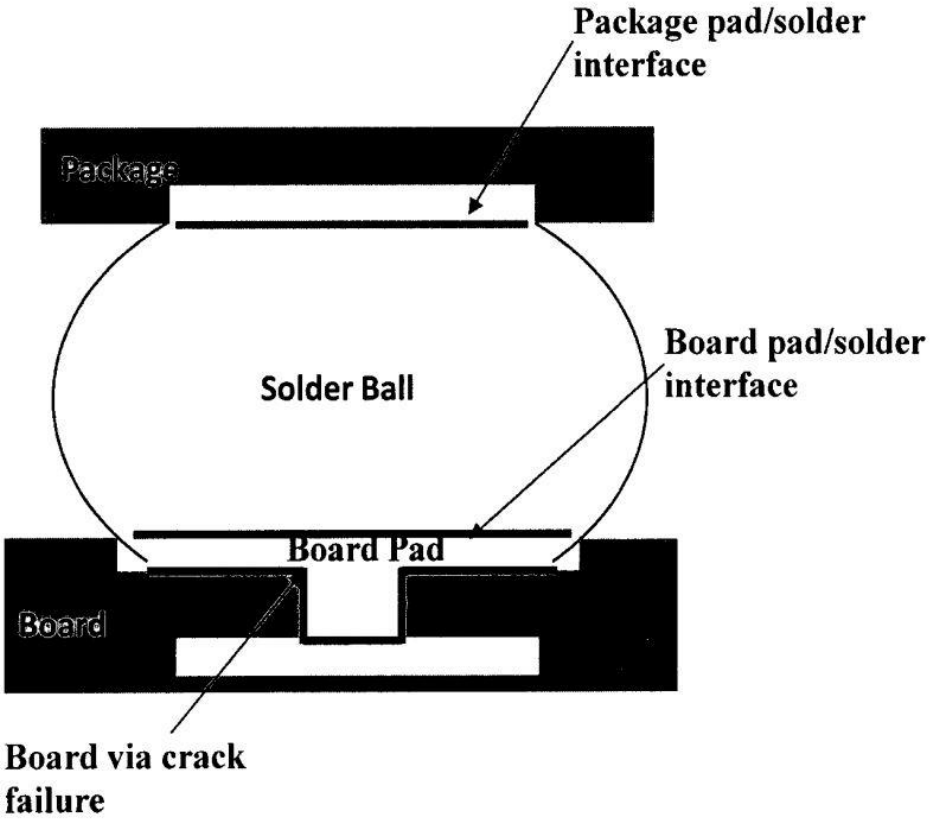

Figure 2.4: Failure Modes of Package

2.2 Finite Element Modeling

Till date, numerous researches have been published addressing the methodologies to determine the dynamic response of drop impact test. The dynamic analysis can be done using various methods and they are shown in the Figure 2.5.

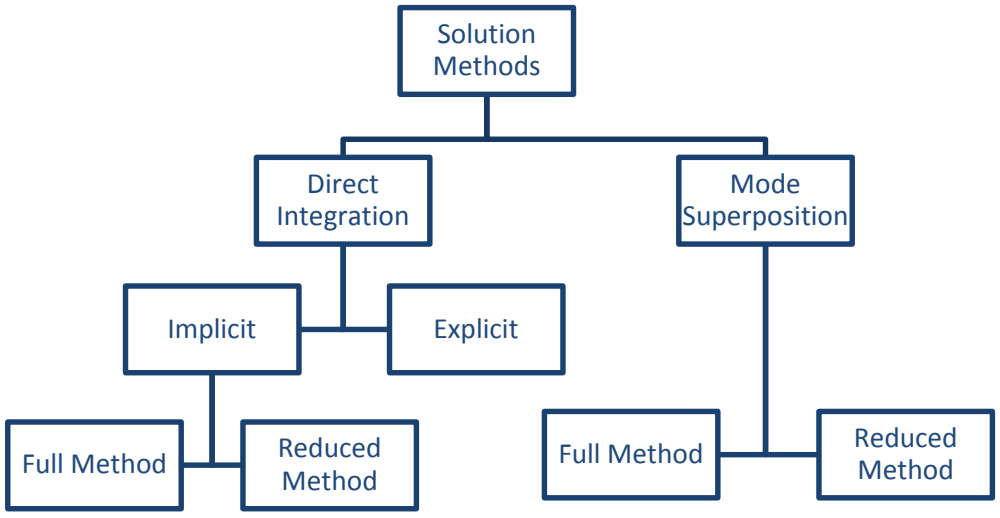

Figure 2.5: Finite Element Modeling Techniques for Dynamic Response of the System

As seen from the above picture the most popular method is known as Direct Integration Method. Another method is mode superposition method. In this work focus has been made on the Direct Integration Method. For Direct Integration Method there are two techniques to solve the problem and they are Implicit and Explicit algorithm for iterations. The implicit technique can be implemented using full system matrices to calculate the transient response or reduced matrices.

Explicit and Implicit methods use time integration to solve for unknown quantitates like displacement solution given the correct force and boundary conditions. In this case the force comes from the acceleration input. Implicit integration assumes a constant average acceleration for each time step between t_n and t_{n+1}. Here, $t_n$is the time at the beginning of each time step and $t_{n+1}$is the time at the end of each time step. After evaluating the governing equation (2.1) resulting acceleration and velocities are calculated at the end of

each time step t_{n+1}which is basically leads to determine the unknown displacement. The governing equation for a dynamic system is as follows:

$$[M]\{a\} + [C]\{v\} + [K]\{x\} = \{F\} \quad (2.1)$$

Where, [M] is mass of the system, {a} is the acceleration, [C] is the damping coefficient, {v} is the velocity, [K] is the stiffness matrix, {x} is displacement, and {F} is force acting upon the system.

Implicit integration method solves for {x} but to do that need to invert the stiffness matrix [K], and thus this method gets more computationally expensive. But as this method directly solves for unknown displacement {x} this is called Implicit Integration method. On the other hand, explicit time integration method solves for {a} first and to do that [M] needs to inverted which is trivial compared to inverting [K] matrix. After figuring out the {a} this method solves for the unknown displacement {x} and that is why it's called explicit method. But to solve this method accurately there is a need for very minuscule time steps otherwise the solver can't solve the problem because of stability issues. Therefore, in this method each iteration is quick but need a large number of iterations to reach the convergence.

Overall, the implicit method is unconditionally stable in solving linear elastic problems but not suitable for the wave propagation problems or highly nonlinear problems [7]. On the other hand, explicit method is conditionally stable but very much suitable for highly nonlinear problems and wave propagation problems but is conditionally stable with the very small increment in time step size.

2.3 Mathematical Model

The above equation 2.1 can be rewritten as following

$$[M]\{\ddot{D}_n\} + [C]\{\dot{D}_n\} + [K]\{D_n\} = \{R_n\} \qquad (2.2)$$

Now the explicit integration uses the following expression of the general form and is combined with the equation of motion at time step n:

$$\{D_{n+1}\} = f(\{D_n\}, \{\dot{D}_n\}, \{\ddot{D}_n\}, \{D_{n-1}\}, \dots) \quad (2.3)$$

And the implicit algorithm uses the following general form and is combined with the equation of motion at time step n+1:

$$\{D_{n+1}\} = f(\{\dot{D}_{n+1}\}, \{\ddot{D}_{n+1}\}, \{D_n\}, \{\dot{D}_n\}, \{\ddot{D}_n\}, \dots) \quad (2.4)$$

Explicit Model:

For the explicit model $\{D_{n+1}\}$ and $\{D_{n-1}\}$ can be expanded by using the Taylor series:

$$\{D_{n+1}\} = \{D_n\} + \Delta t\{\dot{D}_n\} + \frac{\Delta t^2}{2}\{\ddot{D}_n\} + \frac{\Delta t^3}{6}\{\dddot{D}_n\} + \cdots \quad (2.5)$$

$$\{D_{n-1}\} = \{D_n\} - \Delta t\{\dot{D}_n\} + \frac{\Delta t^2}{2}\{\ddot{D}_n\} - \frac{\Delta t^3}{6}\{\dddot{D}_n\} + \cdots \quad (2.6)$$

Subtracting equation 2.5 from 2.4 and neglecting the higher order terms the velocity and acceleration at time step n can be approximated by the central difference method as following:

$$\{\dot{D}_n\} = \frac{1}{2\Delta t}(\{D_{n+1}\} - \{D_{n-1}\}) \quad (2.7)$$

$$\{\ddot{D}_{n-1}\} = \frac{1}{\Delta t^2}(\{D_{n+1}\} - 2\{D_n\} + \{D_{n-1}\}) \quad (2.8)$$

Substituting equations 2.7 and 2.8 into equation 2.2 at time step n and solving for $\{D_{n+1}\}$:

$$\left[\frac{1}{\Delta t^2}M + \frac{1}{2\Delta t}C\right]\{D_{n+1}\} = \{R_n\} - [K]\{D_n\} + \frac{2}{\Delta t^2}[M]\{D_n\} - \left[\frac{1}{\Delta t^2}M - \frac{1}{2\Delta t}C\right]\{D_{n-1}\} \quad (2.9)$$

Implicit Formulation

Using the Newmark relations, the equations for displacement and velocity at time step n+1 can be expressed as:

$$\{\dot{D}_{n+1}\} = \{\dot{D}_n\} + \Delta t[\gamma\{\ddot{D}_{n+1}\} + (1-\gamma)\{\ddot{D}_n\}] \quad (2.10)$$

$$\{D_{n+1}\} = \{D_n\} + \Delta t\{\dot{D}_n\} + \frac{1}{2}\Delta t^2[2\beta\{\ddot{D}_{n+1}\} + (1-2\beta)\{\ddot{D}_n\}] \quad (2.11)$$

Where γ and β are numerical constants that control the characteristics of the algorithm. Solving for 2.11 and substituting it into 2.9 we obtain the following:

$$\{\ddot{D}_{n+1}\} = \frac{1}{\beta\Delta t^2}\left(\{D_{n+1}\} - \{D_n\} - \Delta t\{\dot{D}_n\}\right) - \left(\frac{1}{2\beta} - 1\right)\{\ddot{D}_n\} \quad (2.12)$$

$$\{\dot{D}_{n+1}\} = \frac{\gamma}{\beta\Delta t}\left(\{D_{n+1}\} - \{D_n\}\right) - \left(\frac{\gamma}{\beta} - 1\right)\{\dot{D}_n\} - \Delta t\left(\frac{\gamma}{2\beta} - 1\right)\{\ddot{D}_n\} \quad (2.13)$$

Substituting the 2.12 and 2.13 into 2.2 at time step n+1 and solving for displacement we obtain:

$$[K^{eff}]\{D_{n+1}\} = \{K_{n+1}\} + [M]\{\frac{1}{\beta\Delta t^2}\{D_n\} + \frac{1}{\beta\Delta t}\{\dot{D}_n\} + \left(\frac{1}{2\beta} - 1\right)\{\ddot{D}_n\} + [C]\{\frac{\gamma}{\beta\Delta t}\{D_n\} + \left(\frac{\gamma}{\beta} - 1\right)\{\dot{D}_n\} + \Delta t\left(\frac{\gamma}{2\beta} - 1\right)\{\ddot{D}_n\} \quad (2.14)$$

Where, $[K^{eff}] = \frac{1}{\beta\Delta t^2}[M]\frac{\gamma}{\beta\Delta t}[C] + [K]$

2.4 Board Level Drop Simulation in ANSYS

Due to the short time to market the BLDR has been analyzed with the help of computer simulation for a long period of time. There has been numerous researches done on the numerical modeling studies. And there are several techniques to perform the drop test numerically based on the method adopted by the user such as dynamic vs static (loading type), free-fall vs Input-G (loading method) and implicit vs explicit (solver algorithm). Each combination of the modeling technique has its own advantages and disadvantages. The solver algorithm basically depends on the user time, experience, loading method and ease of use of the software. Previously difference between the solver algorithm has discussed. Following is the discussion about the loading methods.

2.4.1 Free Fall Method

The free fall method actually simulates the whole drop test process that took place in real. In this method the user has to model the drop block, board and other particulates like the

guiding rod etc. But one can skip most of the complicated parts involved in the real drop test process as the model will generate complicacy and take a long time to solve. That is why most of the cases the best approach is to design the board-package assembly with the drop board, standoffs and drop table avoiding the guiding rods and felt material (if the material properties are unknown). The whole modeling details is shown in the Figure 2.6. It is clear that the packages are mounted on the board that is connected to the drop block with standoffs. This setup is dropped from a certain height on the contact surface to produce the certain level of G's. This G is highly dependent on the contact surface condition and material properties used for the contact surface, drop height, and the felt material properties of felt [24]. There are certain drawbacks of this technique. First gathering all the material properties that can represent exact experimental setup is quite challenging, Secondly, the size of the finite element model becomes very large for the problem comparing the size of the package used in board-package assembly. Primarily our main interest is to analyze the dynamic response of the solder interconnections and the ratio of the size of the interconnections compared to the size of the drop block is too small which becomes very expensive to mesh the model and thus result in very long period of time to solve. This free fall method uses the explicit time integration to solve the problem and the explicit algorithm works accurately if the time step is chosen not bigger than the smallest element dimension in the model following the equation 2.15:

$$\Delta t = l\sqrt{\frac{\rho}{E}} \qquad (2.15)$$

Where, l is the characteristic length of the element, ρ is the density of the material used for that particular element and E is young's modulus of the material.

As a result, a very finely meshed model will take a very long time to solve the free fall method problem.

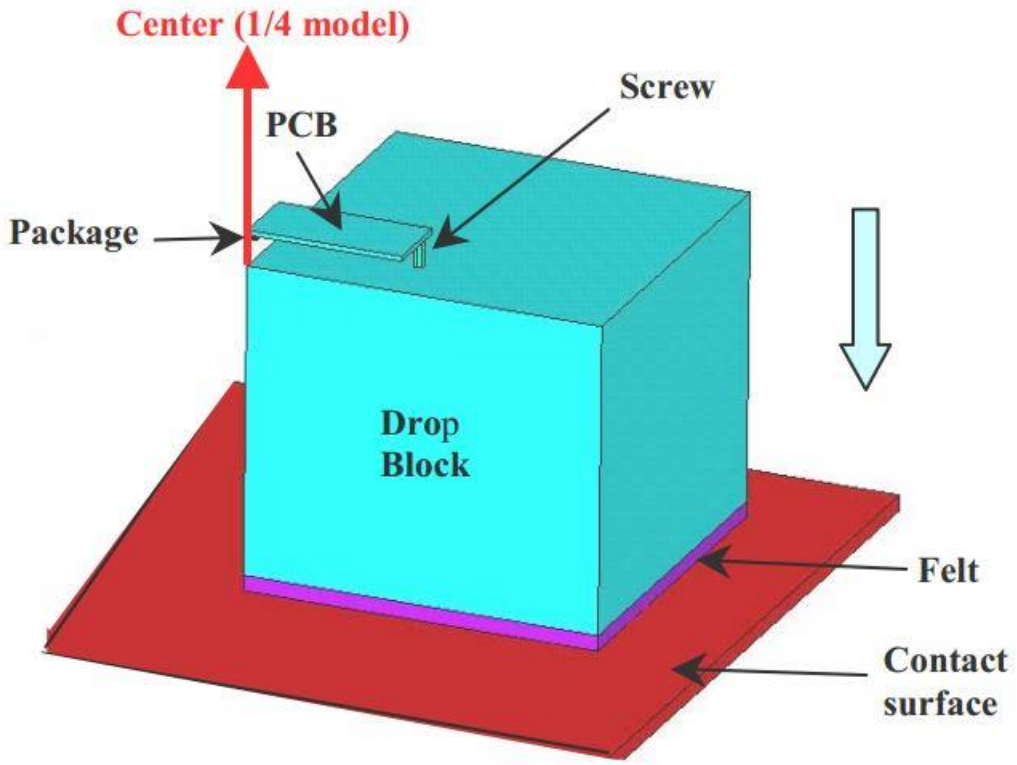

Figure 2.6: Schematic of Free Fall Method [33]

2.4.2 Input G Method

This approach was first introduced by Tee, et al. [24] and is most widely used for its convenience to solve the drop reliability problem. This method bypasses the geometrical detail of the drop table, fixture, contact surface, and friction of guiding rods, felt material etc. But their complex effects on the real experiment is taken care of in the simulation by using the same impact pulse as input. The JEDEC drop test defines to create 1500 G as input impact pulse on the board-package assembly after the drop block hits the strike surface. Thus this 1500 G impact pulse actually acts as the damaging force to the solder interconnections. So in the Input G method this impact of 1500 G is used as input to the

board-package assembly. Figure 2.7 illustrates the Input G method for a PCB assembly with 4 screw hole configuration. This method reduces the model size since no other particulates are not needed to model except the board and package itself. That is why Input G method is much faster than Free Fall method and bypasses many technical difficulties in the finite element model. For this Input G method any technique like Implicit integration, Explicit Integration or Mode Superposition Method can be used [21].

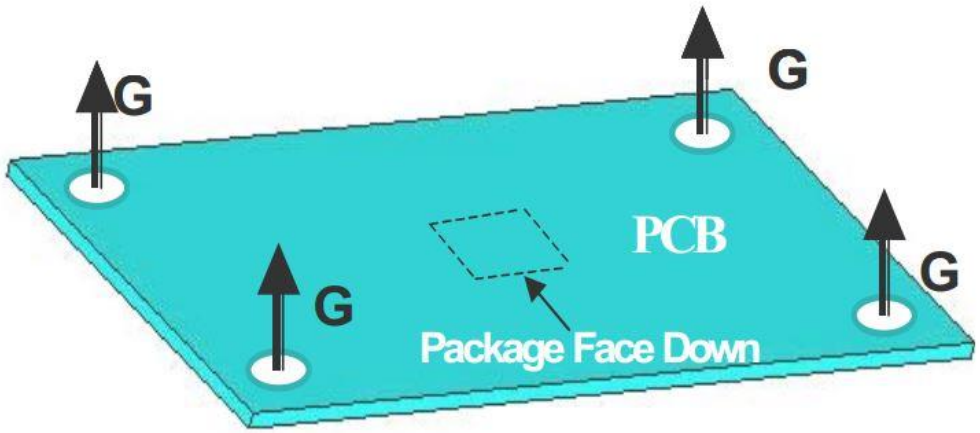

Figure 2.7: Schematic of Input G Method [33]

2.5 Modeling Methods: Global and Local modeling

To capture the accurate dynamic results in the solder interconnects submodeling is very important technique to adopt. Submodeling technique let the user to simply to build the model and gives much accurate results in the particular region of interest. Submodeling method utilizes two separate models: Global and Local model. A global model represents the whole structure that is the full geometry of the exact object. And the local model represents any particular region of interest in the global model in detail with very fine mesh. The procedure to solve the local model is as follows:

1. Create the local model of the specific region of interest from the global model with appropriate mesh details
2. Solve the global model first for the specific problem definition
3. After solving the global model submodeling algorithm interpolates the deformation from the global model to the submodel cut boundaries and solves for the local stress

Submodeling technique is used in the industry level for any kind of complex problem and for electronic industry it is widely popular [21]. For the board level test simulation, the problem arises with the dimension ration between the very small solder ball and the board dimension itself. Even though for the Input G technique it poses challenges when the package and the solder ball size is too small compared to the board dimension. Mainly for the geometrical size mismatch meshing becomes very challenging to be evenly distributed in the overall geometry. The ratio between the solder ball and the board length is about 10^6 [7]. This means that with hundreds of solder interconnections in the board modeling and meshing the whole geometry is difficult and to obtain very accurate results for the solder interconnects is quite challenging. Therefore, submodeling technique is adopted to boost the efficiency of the numerical solution. Following are the steps that Syed, et al. adopted to investigate the dynamic behavior of different components on a JEDEC board:

1. Calculating the stiffening effect of a component
2. Global board level model which includes the component stiffness effect
3. Submodeling approach to transfer boundary conditions to local/submodel
4. Detailed solder interconnections model including calculations of intermetallic layer response

Component Stiffening Effect: Syed has used beam elements to model the solder interconnections and shell element for the component body to simplify the overall model. But this method requires to calculate effective component stiffness of the objects like substrate, die, die attach, mold etc. which are used to build the package and then this one single effective stiffness is used in the shell element. Similarly, the component and the interconnection effective stiffness is calculated. The solid element model is shown in Figure 2.8.

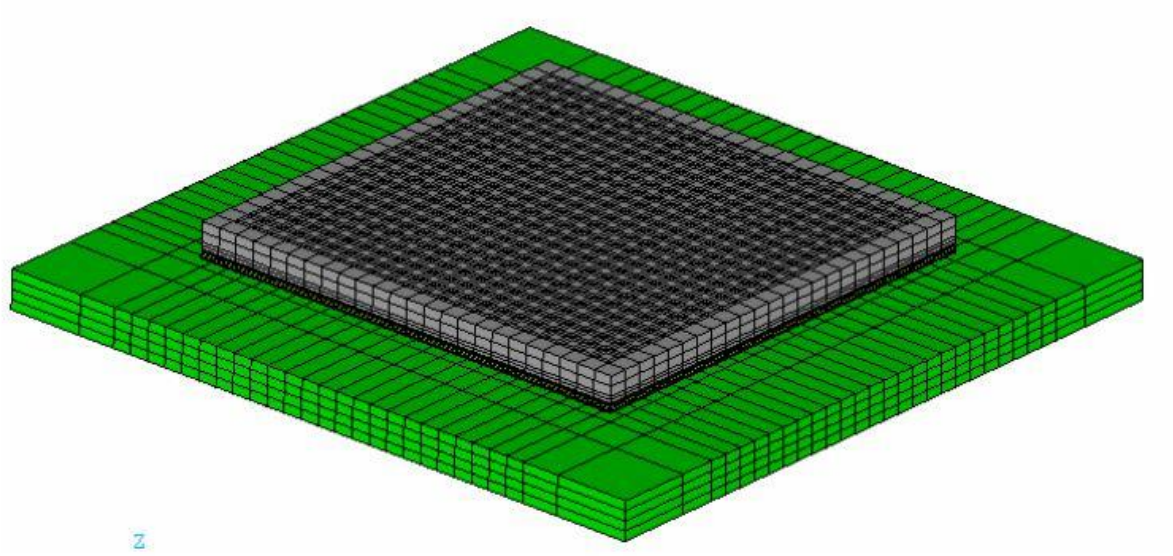

Figure 2.8: Component level model for effective stiffness Full model [20]

2.5.1 Global Model

Board level modeling consists of shell element. The board level modeling is shown in Figure 2.9. in the board level modeling there are two sets of material properties one for the component region and other for the non-component region. The component region has the effective modulus, density based on the components.

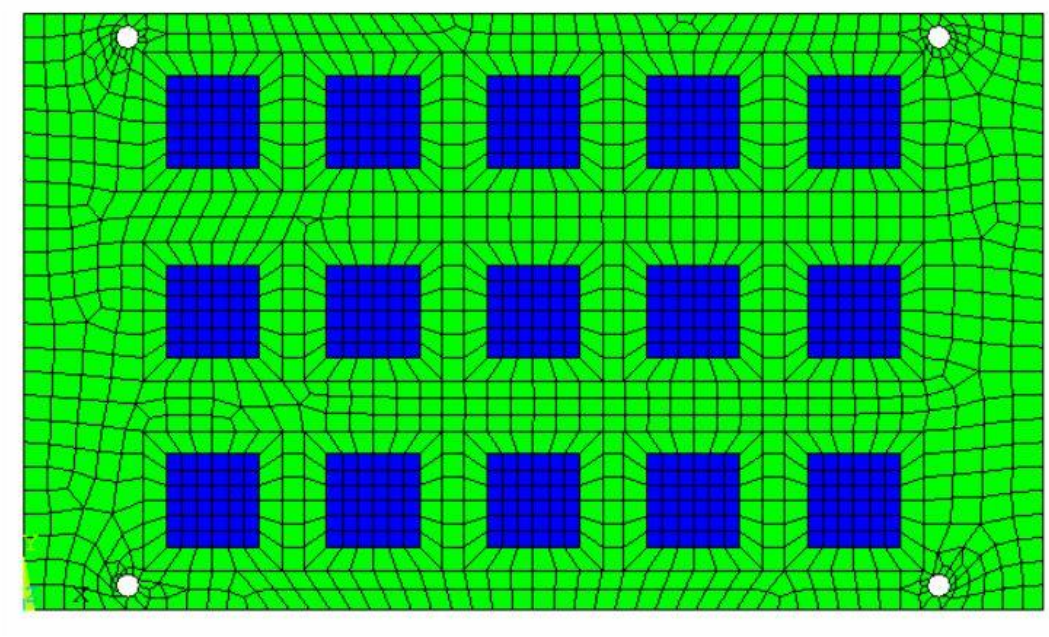

Figure 2.9: Global level modeling [20]

2.5.2 Local Model

After analyzing the global model these results are used apply on the local component level model to calculate interconnections stress accurately. The local model and the solder joint level model is shown in the Figure 2.10. Since the solder joints are modeled as rectangular blocks in the local model the stress calculated from this step is not accurate enough. Therefore, one more step was added to create another local model of the solder joint itself (Figure 2.11) and using the same principal of submodeling detailed calculation was achieved.

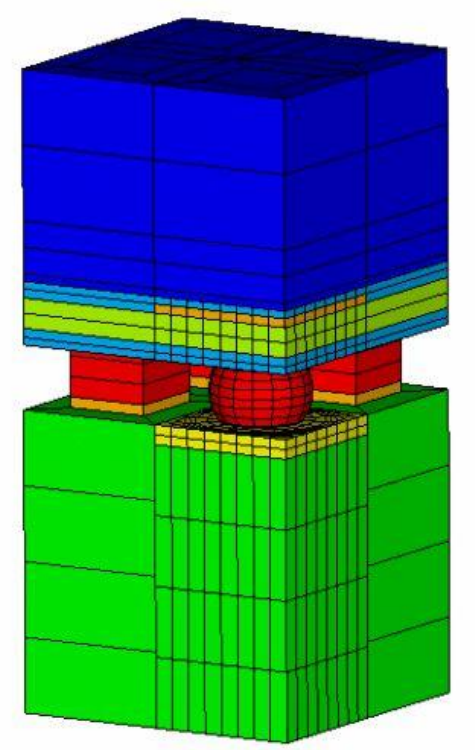

Figure 2.10: Local Model [21]

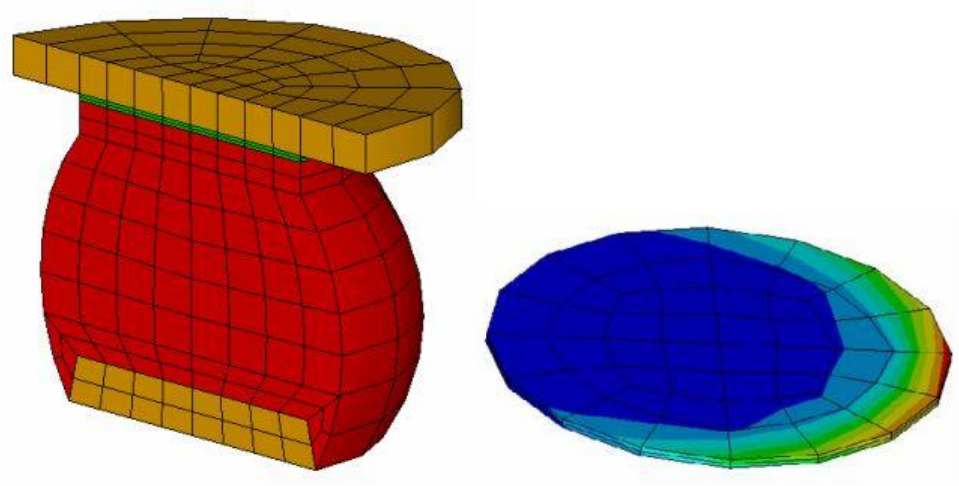

Figure 2.11: Detailed Solder Joint [21]

Chapter 3

FINITE ELEMENT MODELING

In this thesis comprehensive studies are being carried out using finite element analysis to investigate the board layer properties effect on the drop reliability in both environmental and elevated temperatures. It has been observed that changing any material properties related to the elastic modulus and the density changes the overall drop reliability. Global and local models are developed to analyze the dynamic behavior of the board assembly upon drop shock input. Finite element models i.e. both global and local models used in the simulation described in details with the loading conditions, boundary conditions and submodeling technique adopted to link the global and local FE models.

3.1 Global Model

A Finite Element model of JEDEC test board using ANSYS 16 is shown in Figure 3.1. As for the symmetry the model is cut into quarter of the full model and the dimension is 66 mm X 38.5 mm of the board. Only the lower left quarter model is designed. The package size remains the same as 2.8 mm X 2.8 mm for all the different board thickness. The quarter symmetry model is shown in the Figure 3.2. This global model does not include all the minute details in the solder interconnections which is included in the local model.

3.1.1 Solder Bump Model

In this technique the global model is designed as a simplified version of the whole board-package assembly. The solder joints are modeled as rectangular blocks and the dimension of the solder joints are 0.14 mmX0.14 mm and the thickness is taken as 0.24 mm. Though the original thickness of the solder interconnections is 0.22 mm and there is copper pad beneath it on 0.01 mm thickness and on the top there is under bump material which thickness is 0.01 mm. But to avoid complicacy of this very tiny dimension of the under

bump material and the copper pad the overall thickness is taken for the interconnections as 0.24 mm.

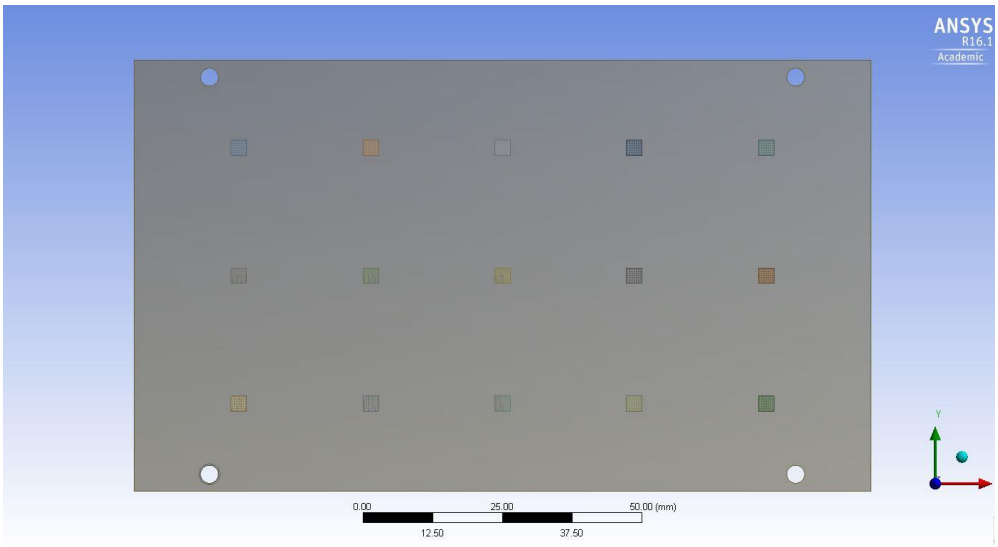

Figure 3.1: Global Model Full

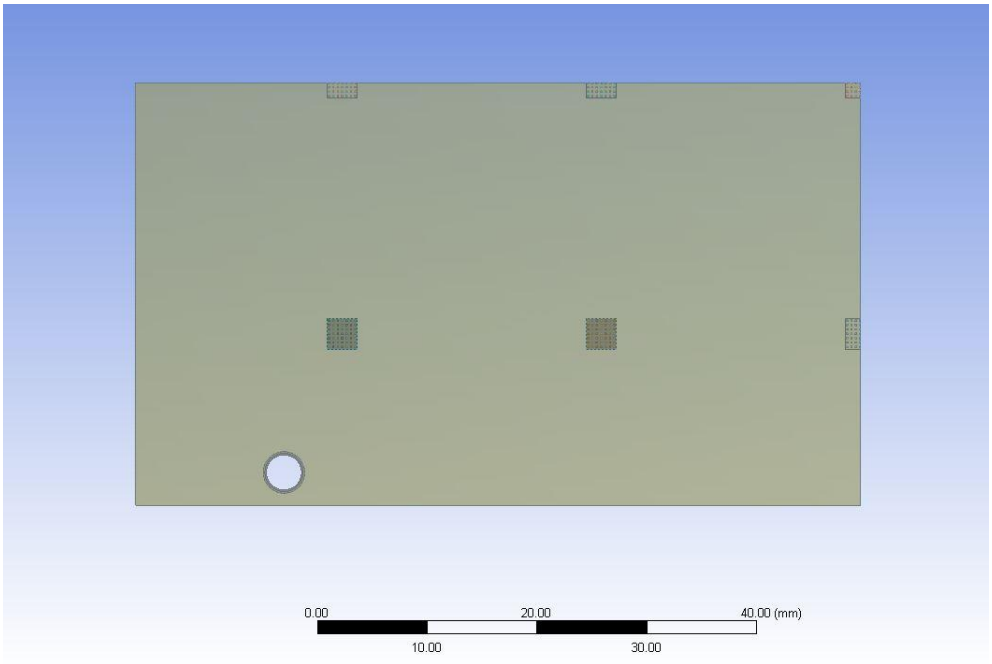

Figure 3.2: Quarter Symmetry Global Model

3.1.2 Equivalent Material Properties Model

The equivalent material properties along the thickness are often used to increase the computational efficiency and to portray the model accurately in the software. Though it can't describe the interlayer stress caused by the mismatch of the young's modulus but still it is effective to run the simulation perfectly and to achieve results as accurate as possible. In the software it is very difficult to run the simulation if the dimension ratio is too big e.g. the board dimension is 66mmX38.5mm and let the thickness as 1mm but the package has layers of die, mold, RDL etc. those have dimensions of 2.8mmX2.8mm and the thickness vary from 0.01mm to 0.25mm. So it is very difficult to handle this kind of details in simulation and might end up with error. For this reason, the package top side is modeled with effective young's modulus which helps to create only one layer with the same dimension/volume as it would be with all those different layers. This technique helps to minimize the computational time and also better than comparing only taking the die and mold layers on the package top and discounting the other layers such as the copper layer, die attach layer etc. This method has the effective material properties for all the layers that consists the package top and represent them by only one single block as shown in Figure 3.3.

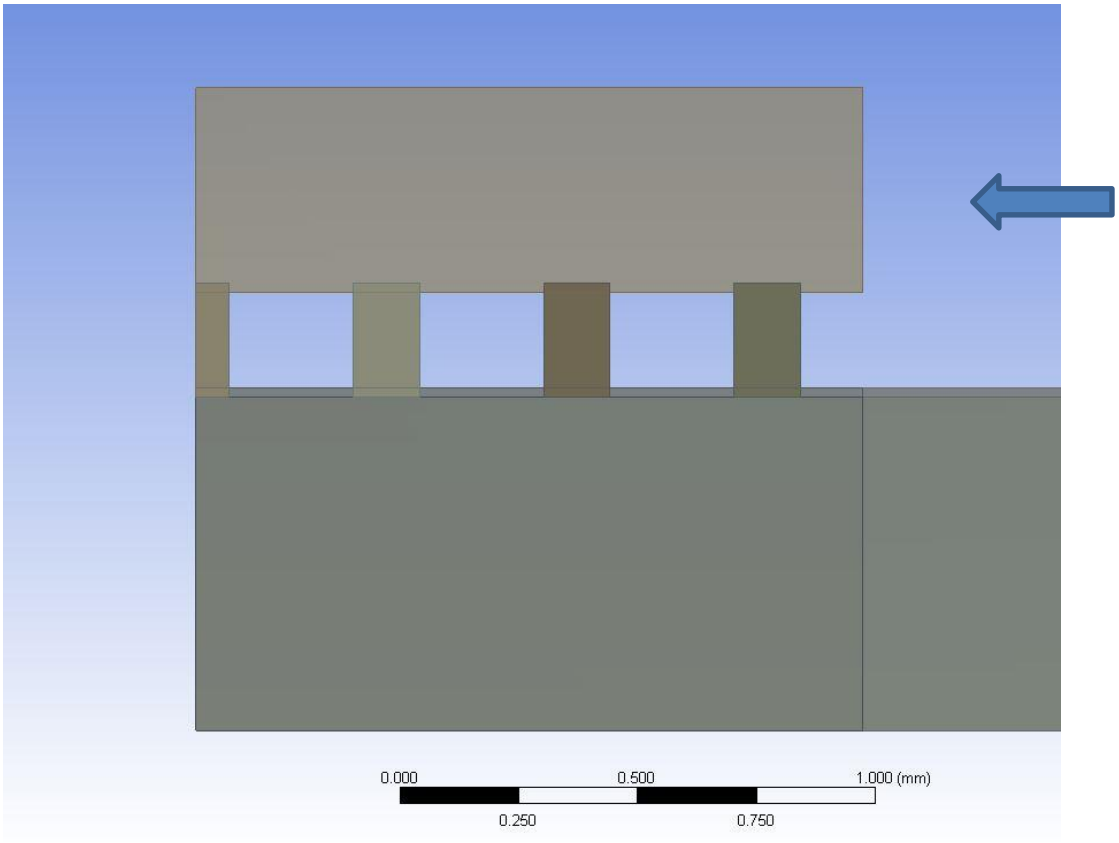

Figure 3.3: Equivalent Material Properties Package Global Model

To get the equivalent young's modulus the formula was used from the theory of the composite beams with isotropic materials with narrow width. The equivalent young's modulus is derived from the following equation:

$$E = \frac{(AD - B^2)}{\bar{A}D} \qquad (3.1)$$

Where, E is young's modulus,

$$A = \sum_{i=1}^{n} E_i b(y_i - y_{i-1}) \quad (3.2)$$

$$B = \frac{b}{2}\sum_{i=1}^{n} E_i(y_i^2 - y_{i-1}^2) \quad (3.3)$$

$$D = \frac{b}{3}\sum_{i=1}^{n} E_i(y_i^3 - y_{i-1}^3) \quad (3.4)$$

Where, b is the breadth and y is the distance from the mid-plane of the composite structures shown in the Figure 3.4.

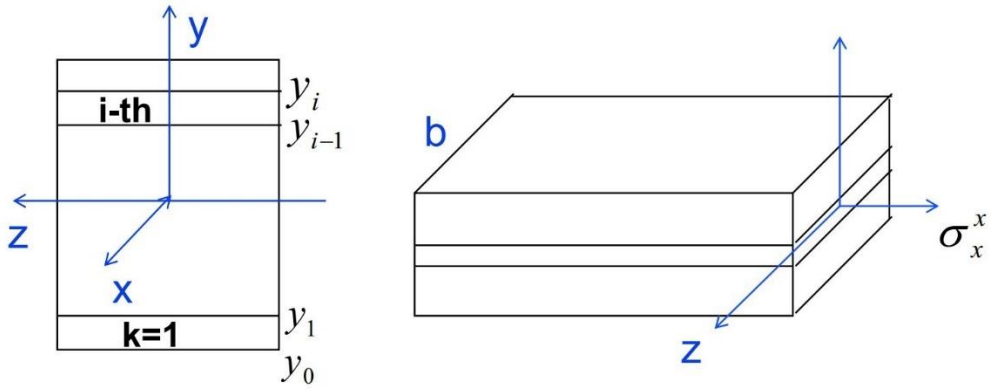

Figure 3.4: Composite Beam with isotropic Materials []

The final meshed model of the global model is shown in figure 3.5. and 3.6.

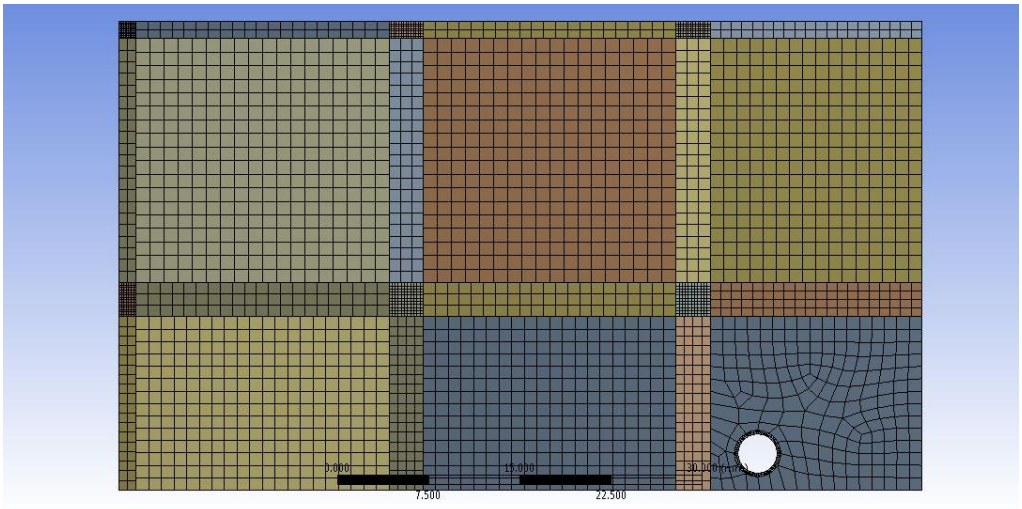

Figure 3.5: Quarter Symmetry Global Model (Meshed)

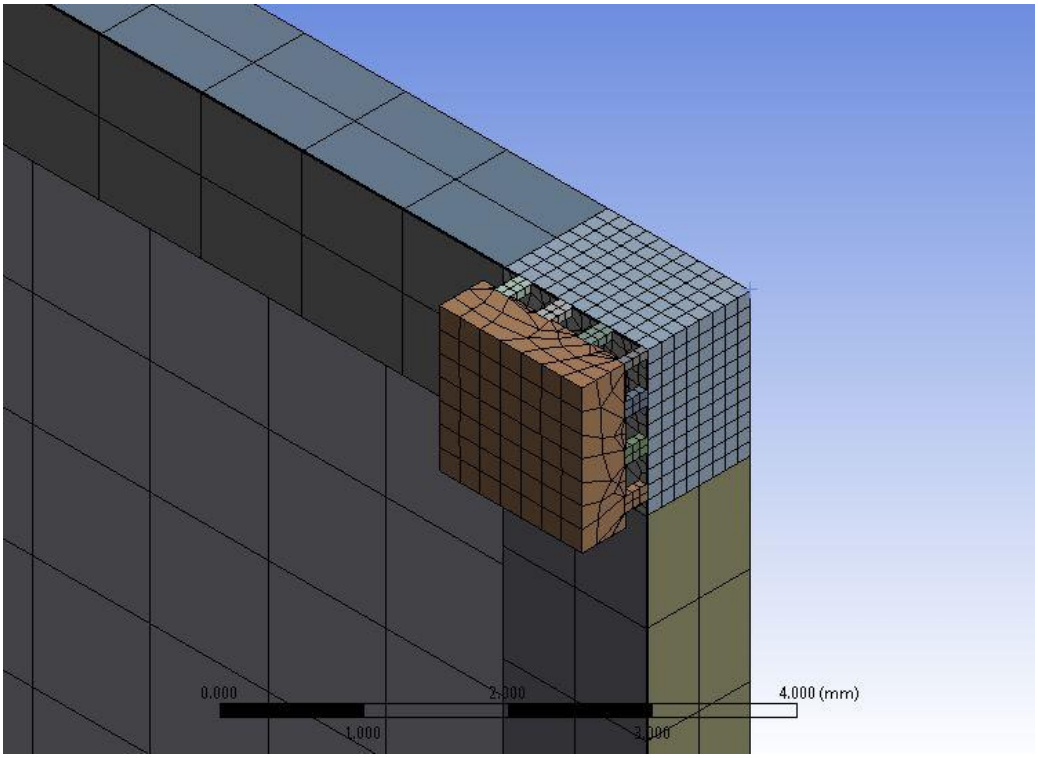

Figure 3.6: Global Model Meshing Detail

3.2 Local Model

The local model created in ANSYS is with all the details as shown in Figure 3.7. In the local model the minute detail like solder interconnections and the package layers are taken into consideration. Solder interconnects are modeled as spherical solder balls instead of the square block for the results accuracy. As the chip size is 2.8 mm X 2.8 mm the cut boundary was taken with this dimension. The refined mesh model is shown in the Figure 3.8 & Figure 3.9.

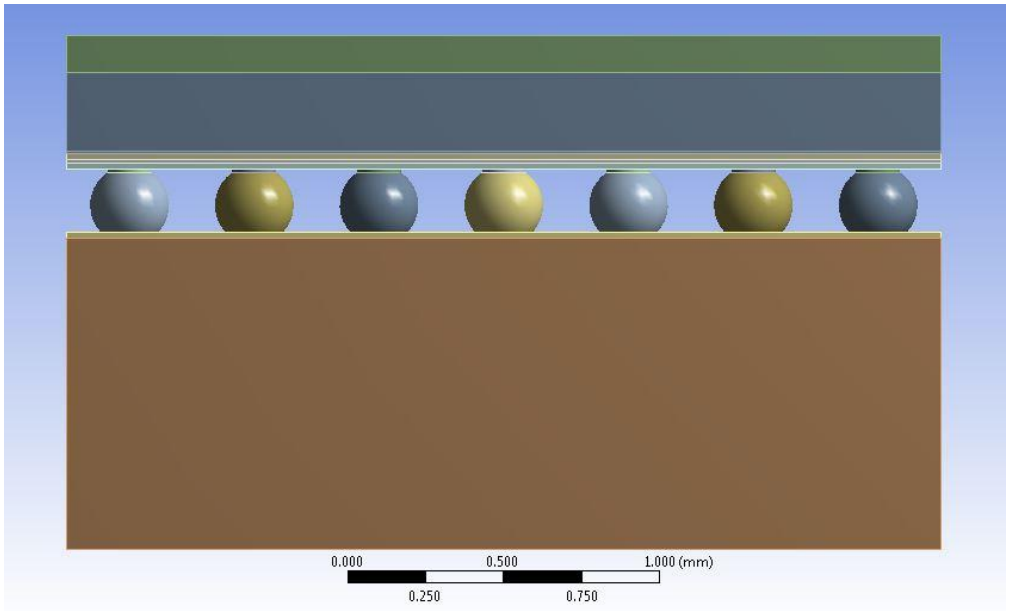

Figure 3.7: Local FE Model with Detailed Layers

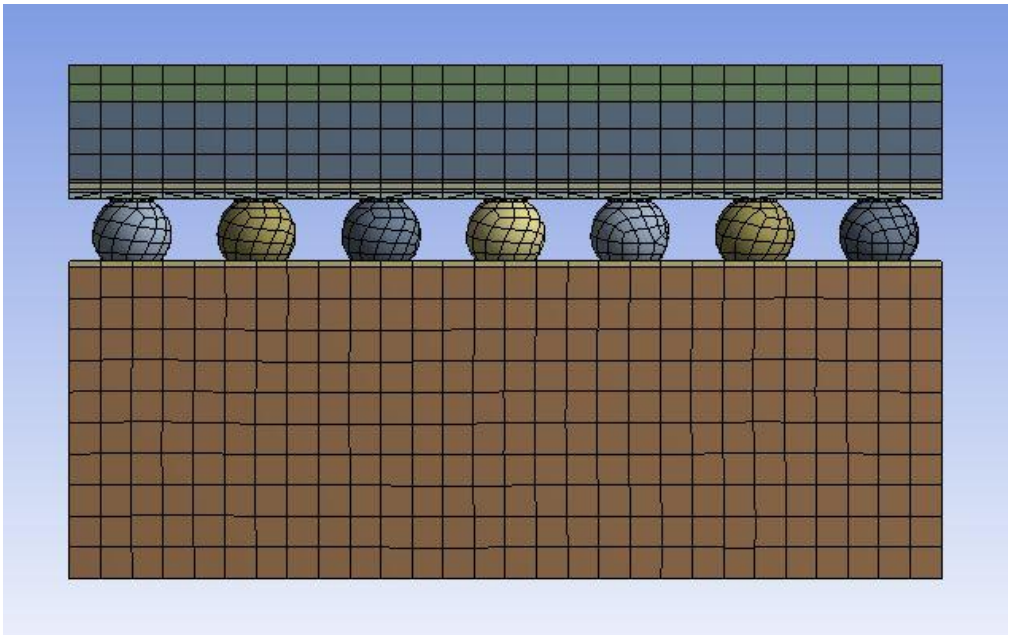

Figure 3.8: Local FE Model (Meshed)

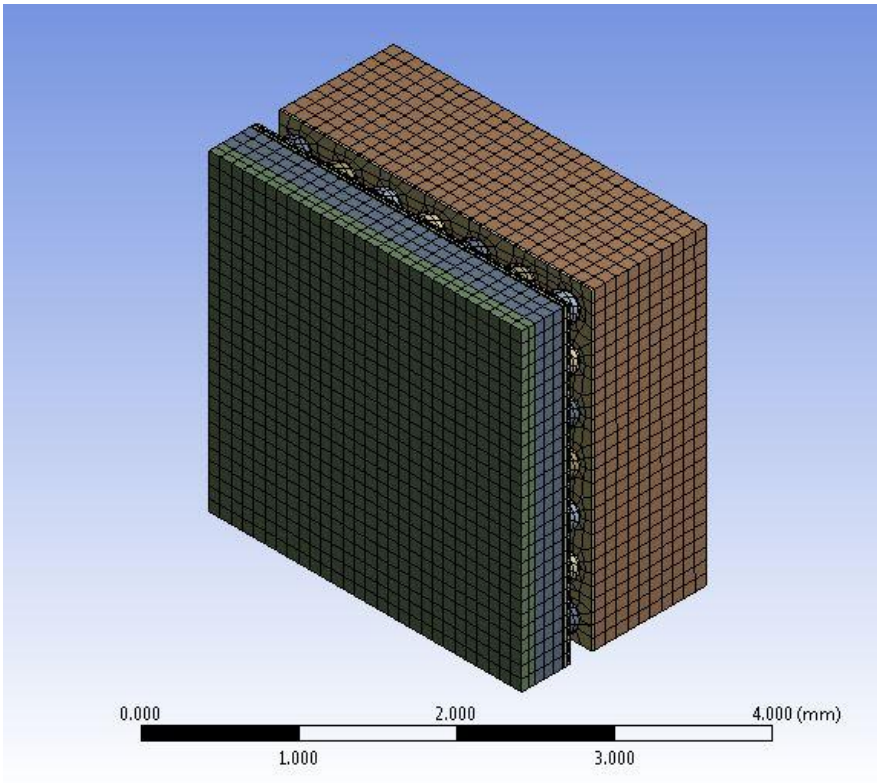

Figure 3.9: Local FE model (Meshed)

3.3 Problem Definition and Loading Conditions

3.3.1 Board Selection

According to JEDEC specification 15 WLCSP packages are mounted on the boards with a dimension of 132mmX66mm. The thickness of the was chosen from 0.7mm, 0.89mm, 0.94mm, and 1mm. Here, 0.89mm and 0.94mm boards are not actual boards but they are customized using in house milling operation on the 1.00mm board.

3.3.2 Loading Condition

According to JEDEC the input acceleration should be 1500 G which is used in the FE simulation that is adopted form the Input G technique described by Tee et, al. [24]. Typically, the acceleration impulse measured by the accelerometer attached to the board is described by the following equation:

$$a = \begin{cases} 1500g\ sin\frac{\pi t}{t_w},\ t \le t_w,\ t_w = 0.5 \\ 0,\ t > t_w \end{cases} \qquad (3.5)$$

Where, a is acceleration (m/s^2), g is acceleration due to gravity (m/s^2) and t is time in milliseconds (ms). Here, the peak value of the acceleration is 1500g and the impulse duration is only 0.5 ms and there is no rebound. It is assumed in the simulation to apply this impulse directly to the board as the whole drop setup of the drop table and the board act as a rigid body. This is the assumption of the Input G method.

3.3.3 Direct Acceleration Input (DAI)

This Input G method is used with modification to apply the loads which is called Direct Acceleration Input (DAI) method [7]. In this method the acceleration input is directly applied to the body as body force. The problem formulation is shown below.

$$[M]\{\ddot{u}\} + [C]\{\dot{u}\} + [K]\{u\} = \begin{cases} -[M]1500g\ sin\frac{\pi t}{t_w},\ t \le t_w,\ t_w = 0.5 \\ 0,\ t > t_w \end{cases} \qquad (3.6)$$

$$\{u\}|_{t=0} = 0$$

$$\{u\}|_{t=at\ hole} = 0$$

These equations formulate the problem definition as the original definition except that the difference in the rigid body movement. In this method the surfaces of the screw holes are fixed at all time. The accelerations used in the simulation with this method are shown in the table below with the illustration in a graph too.

Time	Acceleration
0	0
0.00005	4.54E+09
0.0001	8.64E+09
0.00015	1.19E+10
0.0002	1.4E+10
0.00025	1.47E+10
0.0003	1.4E+10
0.00035	1.19E+10
0.0004	8.64E+09
0.00045	4.54E+09
0.0005	-4.7E-06

Table 3.1: Acceleration Input

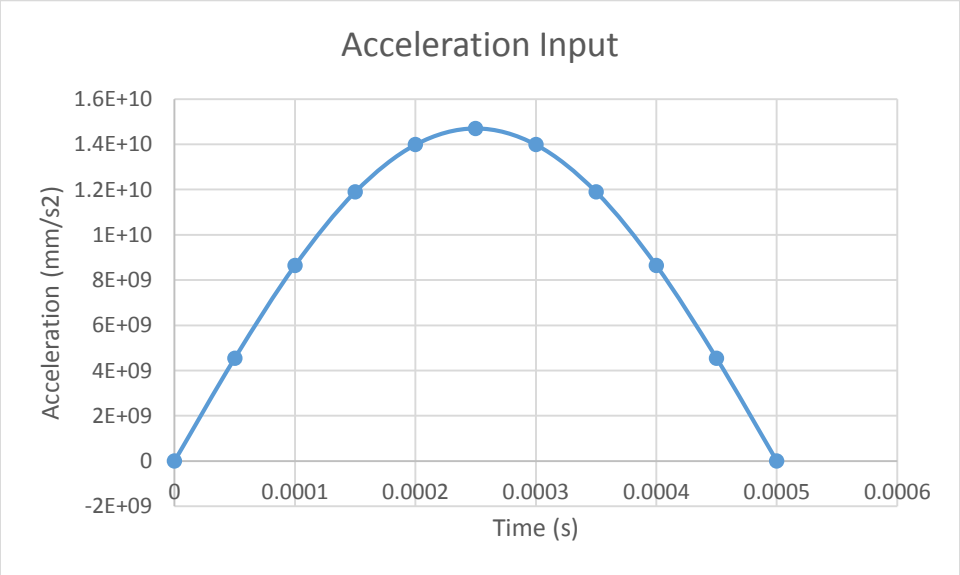

Figure 3.10: Acceleration Input Graph

3.3.4 Transient Dynamic Analysis

To perform the simulation in ANSYS 16 and to use the DAI method the module chosen was Transient Dynamic module in the ANSYS Workbench. In the ANSYS 16 it is easier to simulate dynamic load than the earlier releases as in the previous versions the user has to depend on the ANSYS APDL. But this new release makes it easier to perform the dynamic loading problems within the Workbench without the use of the APDL. This transient module uses the Newmark Time Integration method which is explained earlier in the chapter 2. The transient full method was used to solve the dynamic problem. The full method does not reduce the dimension of the problem as the original matrices are used to compute the solution [34]. In this full method all kinds of nonlinearities are specified and automatic time stepping is used and the major advantage is all kinds of loads can be applied to the problem definition. The main disadvantage is it requires a large amount of solution time with the increased complexity of the model.

3.3.5 Modal Analysis

Modal analysis is the study of the dynamic properties of a structure under vibration [7]. Modal analysis is performed on the global model to find the natural frequencies of the system during the impact. It is also very helpful to find out the initial time step for the transient dynamic analysis module [35]. A general recommendation for selection of the initial time step is to use the following equation:

$$\Delta t_{initial} = 1/20 f_{response} \qquad (3.7)$$

Where $f_{response}$ is the frequency of the highest mode of interest. In order to determine the mode of interest a preliminary modal analysis is required to perform prior to the transient structural analysis. It is also helpful to examine the various mode shapes to determine which frequency may be the highest mode of interest that captures the full response of the

structure. As for the different board has different highest mode of interest is obtained in the preliminary modal analysis which is shown in the table below. But to compare all of the results the highest mode shape is taken among all the boards for all the transient analysis initial time step. For all the boards table 3.2 shows the natural frequencies for the first 5 modes. Figure 3.11 shows the comparison of the natural frequencies against the board thickness.

	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5
1mm	225.14	587	848.84	1255.9	2055.5
0.94mm	209.79	547.16	790.83	1170.1	1915.3
0.89mm	206.75	539.4	779.19	1152.9	1887.2
0.86mm	206.96	540.06	779.94	1154	1889.1
0.7 mm	137.14	358.03	516.68	764.27	1251.8

Table 3.2: Natural Frequencies of the JEDEC Boards

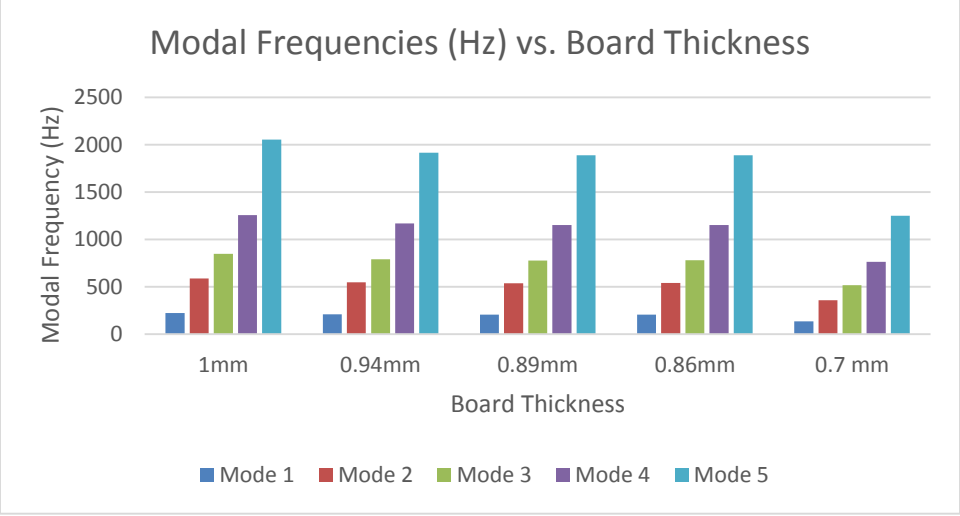

Figure 3.11: Modal Frequencies Vs Board thickness

3.4 Submodel Technique

Submodeling is also known as the cut boundary displacement method. This is based on the Saint-Venant principle. In this principle a set of boundary conditions is substituted by another statically equivalent set and define that the stress distribution in a region distant from the applied boundary conditions remain the same in two configurations. The principle of submodeling in ANSYS is as follows:

- First, the full model is analyzed to determine the global displacements of the structure under the appropriate loading conditions.
- Then the global model displacement field is transferred to define the boundary conditions for the refined meshed local model. The detailed stress for the interested regions of the original model can hence be obtained.

The submodeling technique is shown in the Figure 3.12. Submodeling technique is used for all the simulation performed in this study.

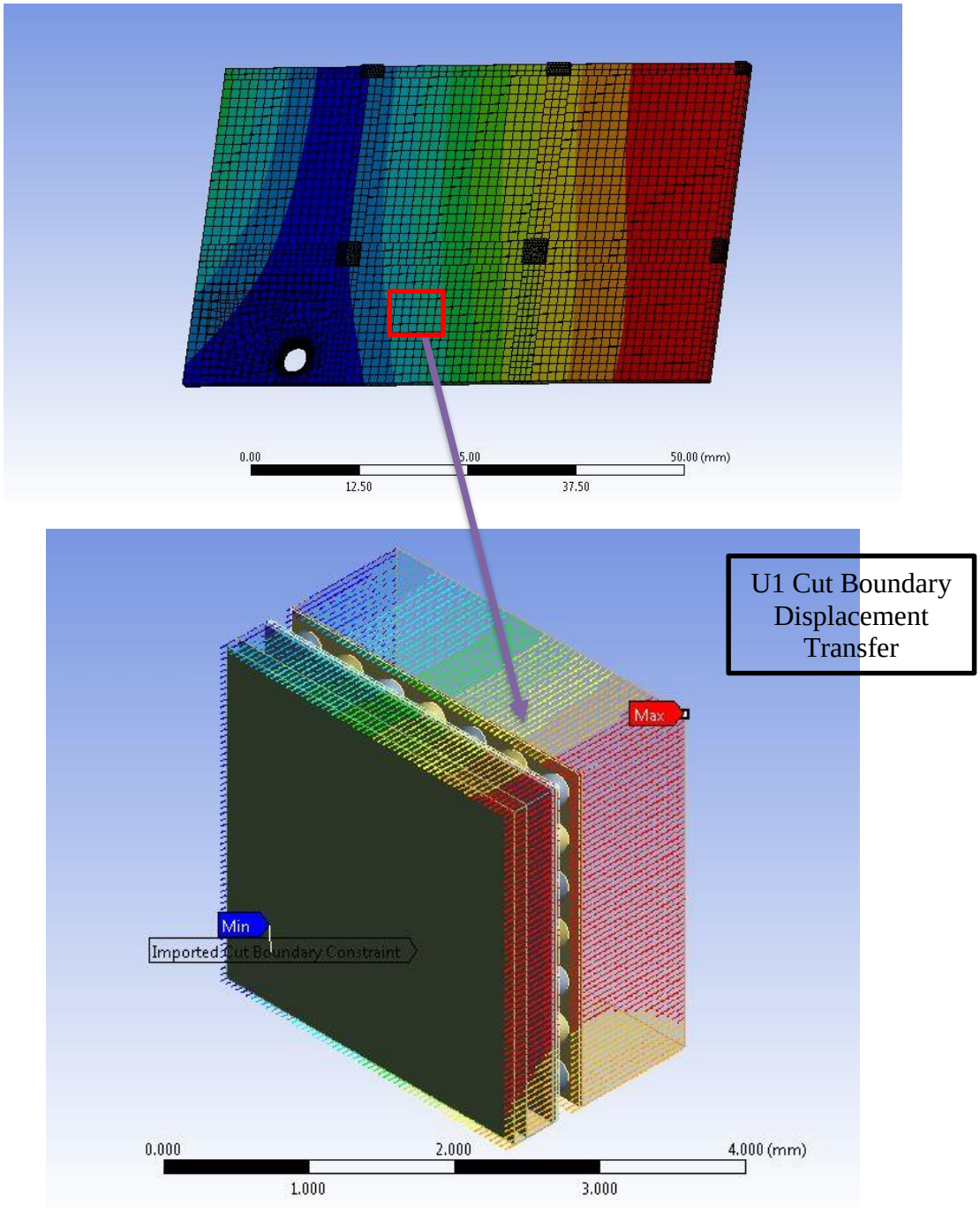

Figure 3.12: Cut Boundary Displacement Transfer from Global to Local Model

Chapter 4

EXPERIMENTAL MATERIAL PROPERTIES

4.1 PCB Layer Details

The layout of the PCB was determined after taking cross-sections from the boards. To make the cross-section visible, the boards were polished using sand paper of grade 600 and 1200 after cutting them. Then the boards were placed under an optical microscope with 10x the magnification to get the microscopic level images of the inner layers of the boards. Then, with Analyzing Digital Images (ADI) software, the dimensions of the layers of the both 1 mm and 0.7 mm boards were determined. The number of the copper layers and the prepreg layers were observed and noted down. This step was helpful for doing layer removal operations on the 1.00 mm board as the milling dimensions needed to be known. The PCB configuration is 1+6+1 of copper layers. There are two copper layers on either side of the core layers of 6 coppers. The cross-section of the 1.00 mm board is shown in the Figure 4.1.

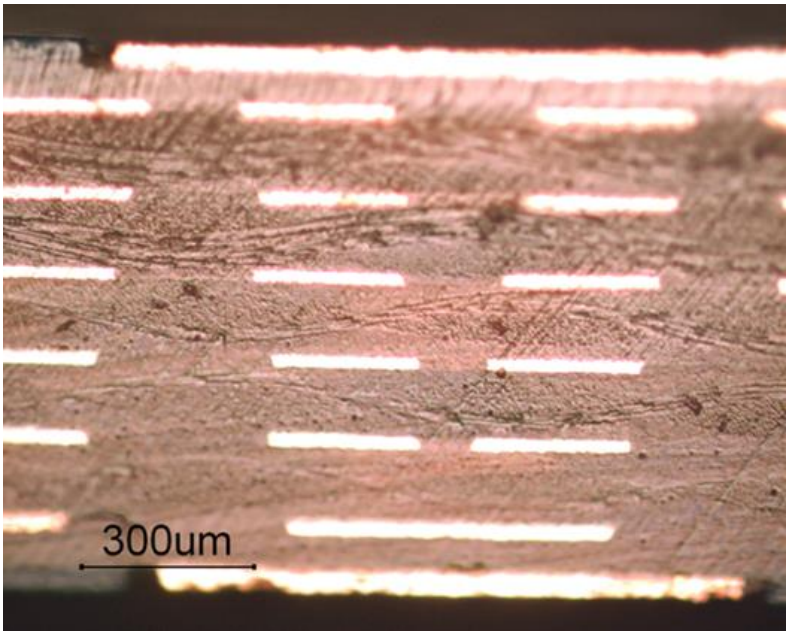

Figure 4.1: Cross-section of 1.00 mm Board

Copper Layer L1 - 60 µm
FR4 Dielectric Layer - 50 µm
Copper Layer L2 - 30 µm
FR4 Dielectric Layer – 120 µm
Copper Layer L3 – 30 µm
FR4 Dielectric Layer – 120 µm
Copper Layer L4 – 30 µm
FR4 Dielectric Layer – 120 µm
Copper Layer L5 – 30 µm
FR4 Dielectric Layer – 120 µm
Copper Layer L6 – 30 µm
FR4 Dielectric Layer – 120 µm
Copper Layer L7 – 30 µm
FR4 Dielectric Layer – 50 µm
Copper Layer L8 – 60 µm

Figure 4.2: Schematic Diagram of the 1.00 mm Board

The total thickness of the copper of 1 mm PCB is 300 µm and thickness of FR4 layer is 700 µm. The percentage of copper is around 30%. To observe the effect of individual layers on the behavior of the whole board, prepreg layers were removed from one side of the 1 mm board. The prepreg layers consist of one copper layer and one FR-4 layer. The layers were removed by using milling machine with a carbide cutter. Layers were removed from only one side as the board was very thin and was difficult to remove from both sides. After removal of the first copper layer, the overall thickness of the board became 0.94 mm. After removing the second layer from the top, that is FR4 layer, the thickness of the board became 0.89 mm. The copper percentage of 0.94 mm board became 25.5% and for the 0.89 mm board it became 27%. This 0.89 mm board has more copper than the 0.94 mm board as the FR4 layer has been removed from the top but not the copper under that layer. That is why the volume of copper increases in this board than to the FR4 volume comparing to the 0.94 mm board. The copper percentage of 0.7 mm board, on the other hand, is 25.7%. The total thickness of the copper layers is 180 µm and thickness of FR4 is 520 µm. The percentage of copper in each board is shown in the table below:

Board Thickness	Copper Percentage
1.00 mm	30
0.94 mm	25.5
0.89 mm	27
0.7 mm	25.7

Table 4.1: Percentage of Copper in the Boards

The cross section and the diagram of the 0.7 mm board is shown in the Figure 4.3 & 4.4 respectively.

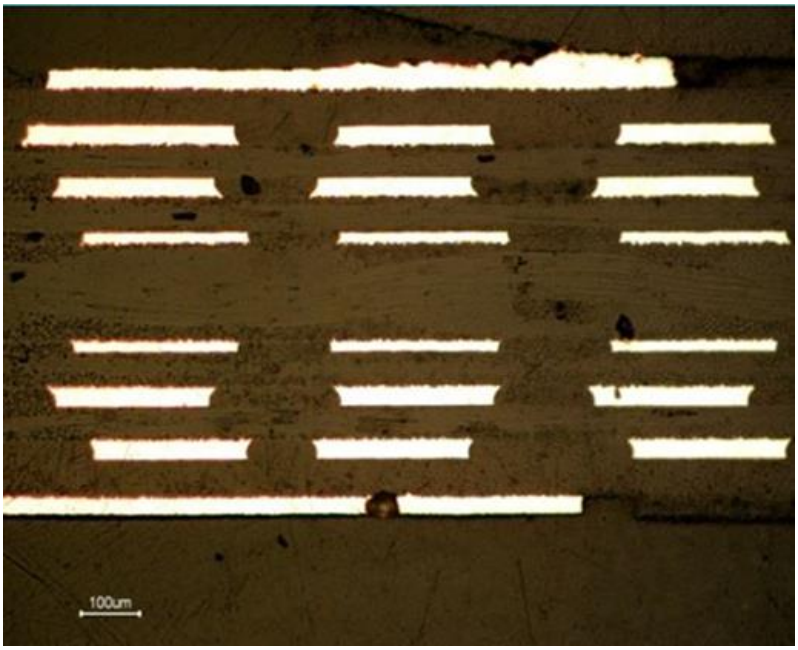

Figure 4.3: Cross-section of the 0.7 mm Board

Copper Layer L1 - 25 µm
FR4 Dielectric Layer - 60 µm
Copper Layer L2 - 25 µm
FR4 Dielectric Layer – 60 µm
Copper Layer L3 – 25 µm
FR4 Dielectric Layer – 60 µm
Copper Layer L4 – 15 µm
FR4 Dielectric Layer – 160 µm
Copper Layer L5 – 15 µm
FR4 Dielectric Layer – 60 µm
Copper Layer L6 – 25 µm
FR4 Dielectric Layer – 60 µm
Copper Layer L7 – 25 µm
FR4 Dielectric Layer – 60 µm
Copper Layer L8 – 25 µm

Figure 4.4: Schematic of the 0.7 mm Board

As it can be seen from the above figures, the copper in the prepreg layers are evenly distributed compared to the copper layers in the core. The coppers in the core layers are distributed in woven pattern making it difficult to actually pinpoint the actual volume of copper. So the copper percentage anticipated is a rough percentage.

4.2 Material Characterization

The main purpose of the study was to investigate the material properties of the 0.7 mm and 1.00 mm boards and how they perform during the BLDR test. Later, it was observed that as the isotropic material properties are affecting the board level reliability it is possible to study of the Design of Reliability by removing layers form the thick board and creating two new boards. Material properties like Elastic Modulus (E) and Density (ρ) and Coefficient of Thermal Expansion (CTE) play important role in the BLR. As the thermal expansion of the board rely heavily on the CTE and the young's modulus of each layer of the Package and the board and also the solder interconnects. Because all the materials in the whole board-package assembly is different and behave differently under thermal loading condition. Similarly, for the mechanical shock input the resulting behavior of the materials differ from each other and thus create mismatch in the bending deformation. Thus generating excessive curvature in the board, solder interconnects experiences high stresses and fail consequently.

To perform simulation and to evaluate the desired results, it was absolutely necessary to determine all the material properties of the PCBs that were required. This was done to accurately model the WCSP assembly with the board and to perform FEA simulations. The material properties required for complete assessment of the results are given below:

- Young's Modulus, E (GPa)
- Coefficient of Thermal Expansion, CTE (1/^{o}C)
- Shear Modulus, G (GPa)

- Poisson's Ratio, v

A brief description of the material properties and their method of determination is given in this chapter.

4.2.1 Elastic Modulus (E)

When an object is stretched or compressed, young's modulus shows the elastic properties under this condition. It measures the stiffness of the material. It can be defined as the ratio of stress vs strain or it is the slope of the stress-strain curve before the yield point of the curve and its unit is Pascal. The young's modulus shows how much the material resists deformation under load. Higher young's modulus means that the material is stiffer and less flexible. The following equation defines the young's modulus.

$$E = \frac{\sigma}{\varepsilon} \qquad (4.1)$$

Where,

E = Young's Modulus

σ = Stress

ε = Strain

Sample Preparation

The samples for measuring the young's modulus is in the shape of dog-bone. The reason for that is to create necking in the reduced section and there is a curvature between the two sections to avoid stress concentration. The grip section was wide enough for grip and had a dimension of 10 mm whereas the dimension of the reduced section was 6 mm. The reduced section ensures greater force density and ensured rupture in the right place. CNC machine was used to create the dog-bone samples. The samples were taken from the long bare section of the board. The dimensions of the sample are given below in Figure 4.5.

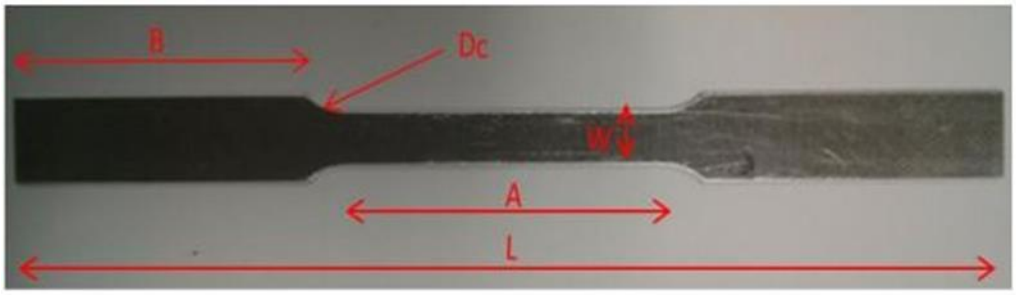

Figure 4.5: Dimension of the Dog Bone Sample

The dimensions are listed below in the table 4.2.

Dimensions	Length (mm)
Length – L	100
Width of Grip – C	10
Width – W	6
Length of Reduced Part – A	32
Length of Grip Section – B	30
Curvature – D_c	4
Radius of Curvature – R	6

Table 4.2: Dimensions of the Dog Bone Sample

The dimensions of the samples were made following the ASTM standards. The ASTM standard E8 was followed for the tensile test [36]. During the testing, precaution was taken so that there was no slippage while the test was running. There was also limit set on the

jaws so that too much pressure was not applied while the jaws were being tightened. The samples were properly aligned; as improper alignment would have caused erroneous results.

The Young's Modulus, E was measured using two instruments. One is Instron Microtester and the other one is Shimadzu Universal Testing Machine.

4.2.1.1 Instron Microtester

The software used for Instron Microtester 5848 is Bluehill. The sample is placed in the jaws by moving the jog in position. The lower jaw was fixed first following the directions. The upper jaw was fixed after that. The extensometer was mounted on the sample after the sample was placed. The distance between the two clips should be 12 mm. A rate of 2 mm/min was applied to the sample with a load cell of 2 kN. The strain was measured from the extension of the clips of the extensometer. Both the load cell and the extensometer were calibrated before the test.

4.2.1.2 Shimadzu Universal Tensile Testing Machine

For Shimadzu Universal Testing Machine (Figure 4.6), Trapezium software was used to measure the young's modulus of the samples. The samples were placed inside the jaws following the direction of placement (Figure 4.7).

Figure 4.6: Shimadzu Universal Testing Machines

Figure 4.7: Samples inside the Jaws of Shimadzu

4.2.2 Coefficient of Thermal Expansion (CTE)

It is the measurement of change of length, shape or volume per unit temperature. That is the material expands or contracts due to its CTE when it is heated or cooled. It causes a lot of stress if there is a hindrance to free expansion or contraction of the bodies.

$$\alpha = \Delta l/(l.\Delta T) \qquad (4.1)$$

Where,

α = Coefficient of Thermal Expansion

l = Original length

∆l = Change of length

∆T = Change of Temperature

The importance of CTE will be more evident while performing the temperature dependent drop test simulation as during the elevated temperature the expansion of the materials dependent on the CTE. As CTE plays a significant role and so determining this property for the board was essential for this study.

4.2.2.1 Thermo-Mechanical Analyzer (TMA)

The instrument used for measuring CTE was Thermo Mechanical Analyzer or TMA SS 6000 from Hitachi as shown in Figure 4.8. This series offers a broad load range of 0.01mN to 5.8 N and has measurement capability from single fiber to stiff bulk compositions. The range of displacement is from negative to positive 500µm. This makes way for higher number of materials to be tested and measured. It has high resolution and accuracy, which makes it possible to measure samples with low expansion as well.

Figure 4.8: Hitachi TMA SS 6000

4.2.2.2 Theory of Operation

The TMA consists of many parts but mainly consists of a probe to measure the displacement, a motor that controls the probe, an LVDT, and a sample cylinder made of quartz. The motor generates force and it is given on the sample via the probe. The probe moves due to the expansion of the sample and the displacement is measured by the LVDT placed vertically on top.

4.2.2.3 Sample Preparation

There is no specific standard for the sample preparation but for the given TMA there are some dimensional criteria. The samples for TMA are very small compared to other techniques like Digital Image Correlation (DIC) technique. No special treatments are needed to make samples for TMA, except not to use high speed cutter as it would leave residual heat in the samples. That heat will interfere with the CTE measurement and will give erroneous results. The maximum permissible length of the sample can be 20 mm and the diameter of the sample can be 8 mm. To avoid buckling as the thickness of the board is very small, the sample lengths were taken as 10-12 mm. The samples we taken in rectangular shape as that was easy to make. The width of the samples was taken as 6 mm.

4.2.2.4 CTE Measurement

The samples were placed in the stage inside the quartz cylinder. To measure the z-directional CTE, the samples were placed on the stage on its thickness. A square sample of 6x6 mm^2 was taken to measure the z-directional CTE. To measure the xy-directional CTE, the samples were placed on its length. A rectangular sample of 12x6 mm^2 was taken to measure the X & Y directional CTE. A constant load of -100 mN was given to the sample through the probe. After the temperature difference was set from room temperature to 250ºC, a ramp of 5ºC/min was set. After the test is done, the CTE is corrected by removing the quartz coefficient from the probe.

4.2.2.5 Results

The values of CTE and young's modulus of all the boards are given in the Table 4.3 below.

Boards	CTE (ppm/°C) Directional			Young's Modulus (GPa)
	X	Y	Z	
1mm	20	20	60	22
0.94mm	14.5	14.5	79	21
0.89mm	15	15	63	22.4
0.7mm	13.2	13.2	50.5	18

Table 4.3: CTE and Young's Modulus of all the Boards

Chapter 5

DYNAMIC ANALYSIS OF PCB PACKAGE ASSEMBLY

The theory behind the solder joint failure has been established numerically and experimentally and it states that due to impact loading PCB experiences multiple bending deformation which ultimately leads to interconnections failure. Differential flexing between the PCB and the IC package causes stress generation on the interconnects and ultimately leads to failure, Wong et, al. [37]. During the Impact, PCB experiences sinusoidal loading. This sinusoidal loading causes the PCB to bend up and down. This bending results in cyclic change among the dynamic resistance of the interconnects and strains of PCB. Cyclic changing in the solder interconnects causes closing and opening at critical crack locations and growing the cracks big enough fails the interconnect [19]. Figure 5.1 shows the bending of PCB and IC Package during the drop impact loading.

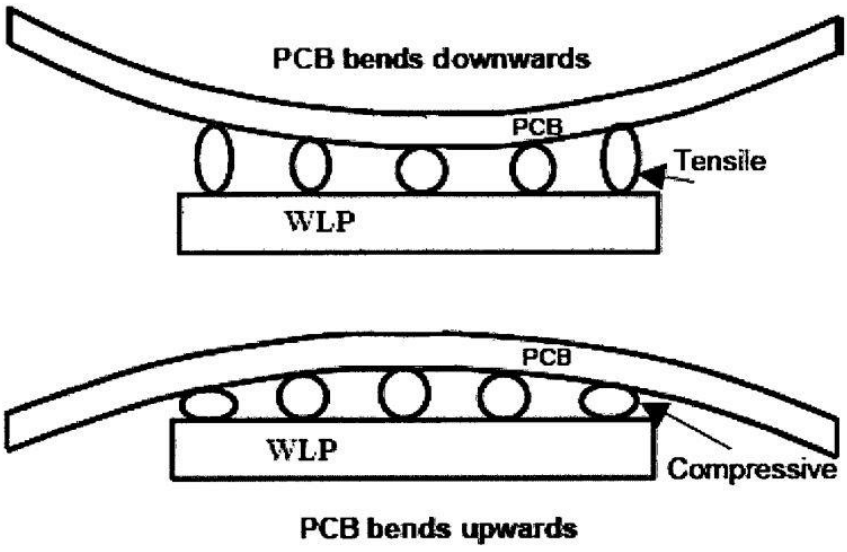

Figure 5.1: PCB Bending during Impact Loading

When the PCB moves downwards it generates tensile stresses and during the upward movement it causes compressive stresses in the interconnections. For both the cases the corner solder joints experience the maximum stress. This happens due to the difference in stiffness of the PCB and the Package. That is why the material characteristics of the PCB and Package is very important to consider as those properties actually decides the failure life of the interconnects. This cyclic bending causes strains in PCB and stresses on to the interconnections. The amount of strain formed in the PCB depends upon the location of the and degree of PCB bending relative to the screw hole fixed boundary conditions.

In this chapter, the dynamic response of the board is discussed, PCB deformation is calculated at different locations, strains are shown in the different locations and stresses of the interconnects are calculated.

5.1 Dynamic Response

Due to the input shock loading, the PCB vibration goes on even after the input shock pulse duration of 0.5 ms. This output vibration is generated because of the output acceleration and this reaches a higher value than the input acceleration of 1500 G. In Fig. 5.2 the time history comparison of the net output acceleration of the PCB-Package assembly are shown along with the input shock pulse. It is noted that the peak value for the 0.89 mm board is highest and reaches 3924.923 G at 0.875 ms and 0.94 mm and 1.00 mm boards follow the same trend too. It is also visible that the output acceleration curve for 0.89 and 0.94 mm boards follow the exactly same trend until 0.3 ms and after that they get separated. These three boards reach their top acceleration value at around the same time while the 0.7 mm board reaches its top output acceleration of 3893.878 G in the positive bending direction at 0.975 ms and towards the negative bending direction at 4.975 ms which is 7374.08 G. Thus dynamic response of the 0.7 mm board is completely different from the other boards

which is understandable because modal analysis reveals that the 1st natural frequency is only 137.14 Hz (7.29 ms) which is 69.61 Hz lower than the value of the next thick board 0.89 mm.

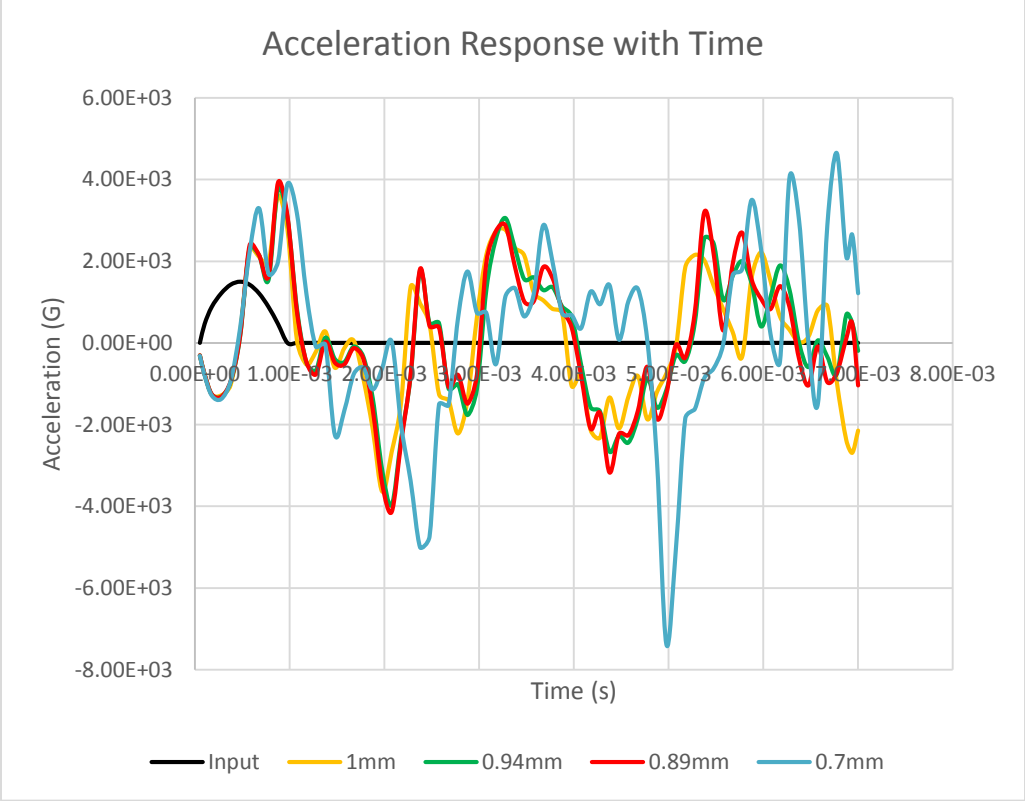

Figure 5.2: Acceleration vs Time

5.2 Deformation Analysis

Since the bending mode has the direct influence on the stress generation it is important to analyze the deformation of the PCB bending. Also deformation is not uniquely related to forces or stresses which ultimately points to consider the material properties differences in the boards drop analysis. Time history of the out of plane displacement is considered in this case. The deformation refers to the warpage of the PCB bending mode and is

calculated for the full PCB and also at the center of the PCB. The deformation that actually considers the full PCB is referred as warpage of the board. The board deformation also helps us to validate the method of the simulation of DAI which shows that the PCB bending occurred in sinusoidal manner which is expected as from the cyclic bending due to the impact load. Figure 5.3 shows the board deformation of the full PCB.

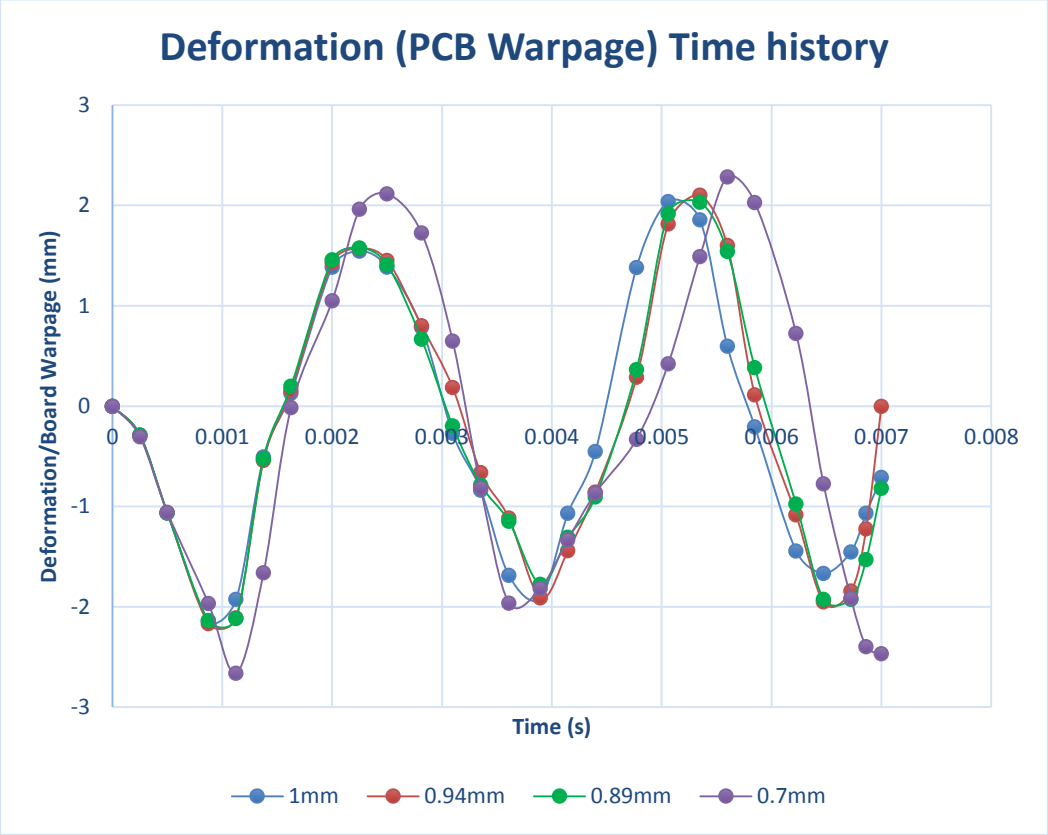

Figure 5.3: Board deformation of full PCB

The deformation of the full PCB accounted for all the boards. Here, deformation followed the sinusoidal bending mode for all the boards and closely related to each other but the maximum bending is occurred in the 0.7 mm board as seen from the above figure. This is due to the difference in the density and the elastic modulus of the 0.7 mm board. 0.7 mm

board has a higher density than all other boards but the modulus is the minimum. On the other hand, all other boards have closely related density and the elastic modulus. The maximum deformation for the boards are listed as follows.

Board Thickness (mm)	Max Deformation (mm)
0.7	2.286
0.89	2.031
0.94	2.101
1.00	2.040

Table 5.1: Maximum Board Deformation

It is evident from the data is that the 0.89 mm board has the lowest maximum deformation and the 0.7 mm has the highest. The 0.89 mm board has the lowest density among all the boards but the elastic modulus is the highest.

The deformation at the PCB center is also calculated. This only accounts the PCB center point deformation along the time. The warpage is the total deformation of the PCB but this deformation at the center is only considering the changes in length in out of plane direction (z direction) with time. Figure 5.4 shows the center deformation. This deformation helps us to understand the effect of material properties difference that is how changing a property can change the deformation behavior of the boards. It is imperative that the tone of the deformation is same meaning this deformation also followed the same sinusoidal path but generated different set of data and different maximum values at the center of each PCB because all the deformation is the result of same bending mode and shape. Generating different set of data depends on the location from where the results are collected as deformation is a function of geometry.

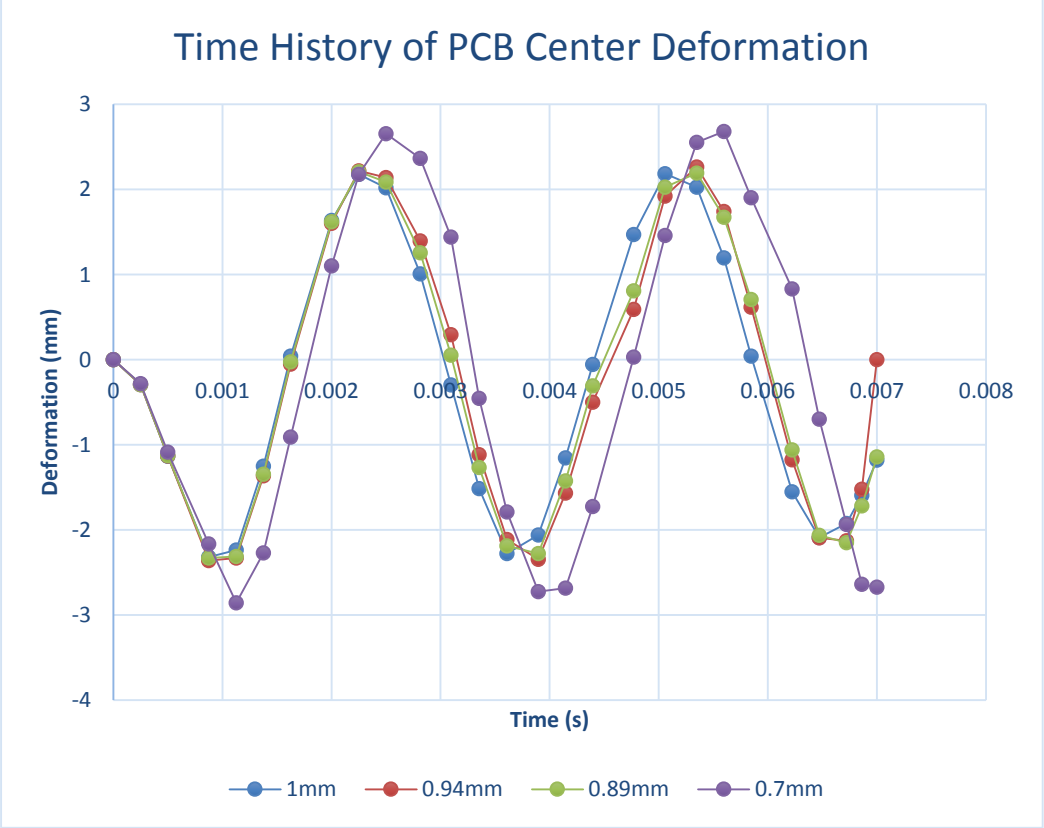

Figure 5.4: Deformation Time History at PCB Center

Following table shows the maximum values of the deformation at the center of the PCB.

Board Thickness (mm)	Max Deformation (mm)	Time of Max Deformation Occurred (ms)
0.7	2.680	5.60E-03
0.89	2.207	2.25E-03
0.94	2.264	5.35E-03
1.00	2.186	5.06E-03

Table 5.2: Maximum Board Deformation at the Center of PCB

As expected from the full PCB board deformation this center deformation is also followed the same trend but the maximum values are different and more than the previous ones. But as the. 0.7 mm board deform more than any other board so the maximum value is still the highest for center deformation than any other boards. Since the 0.7 mm board has the higher density and lower elastic modulus that is why this phenomenon is observed.

5.3 Board Strain Analysis

The local bending mode of the PCB effects the stress generation on the solder interconnections. Thus it is necessary to study the board strain as this strain is causing the stress generation on the interconnects. The strains are measured at different locations. All the strain calculated here is in x direction. First the strains are measured at the PCB center location which is shown in the Figure 5.5. This strain is measured at the bottom of the PCB at the center location.

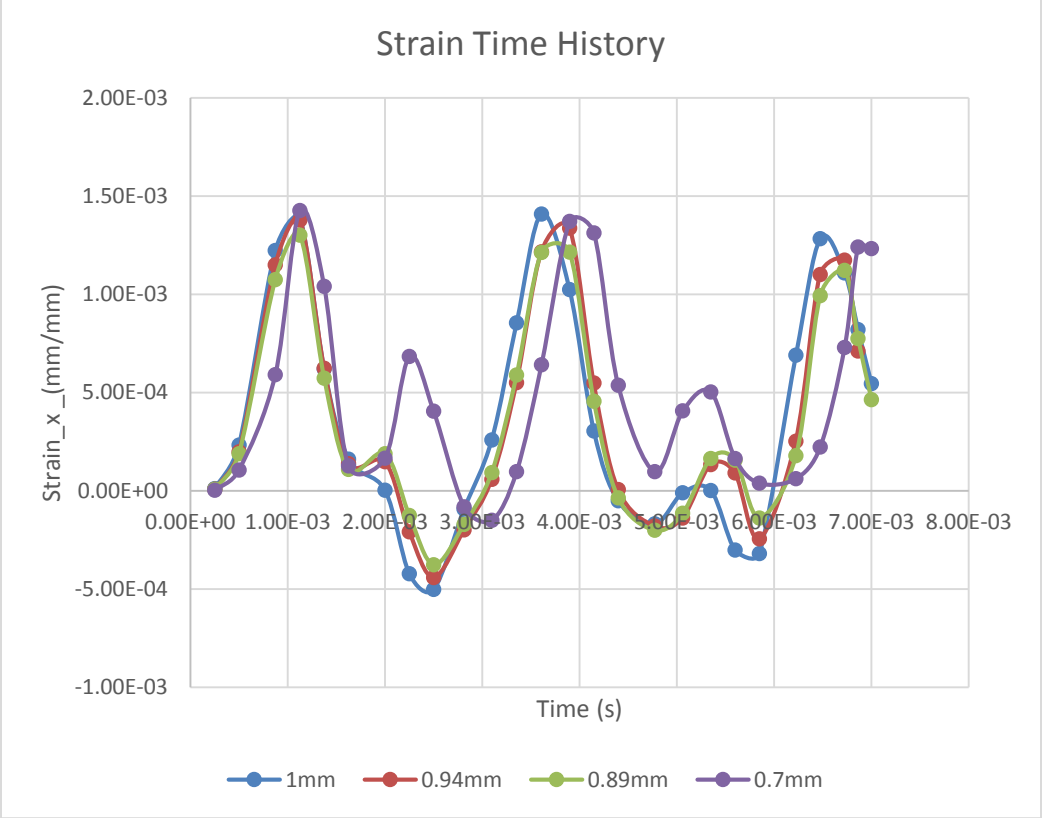

Figure 5.5: Strain at PCB Center Location

It is evident from the graph that 0.7 mm board has the highest strain 0.00143 (mm/mm). The second highest stress is generated on the 1.00 mm board which is 0.00141 (mm/mm). The lowest strain is generated on the 0.89 mm board and that is 0.00130 (mm/mm). The highest strain generated for all the boards are at very similar time 1.13 ms except for the 1.00 mm board which occurred at 3.61 ms.

The strain at the bottom left corner of the U1 package is also calculated. The strain is measured at the bottom of the PCB. Figure 5.6 shows the time history graph of the strain at U1 Package corner.

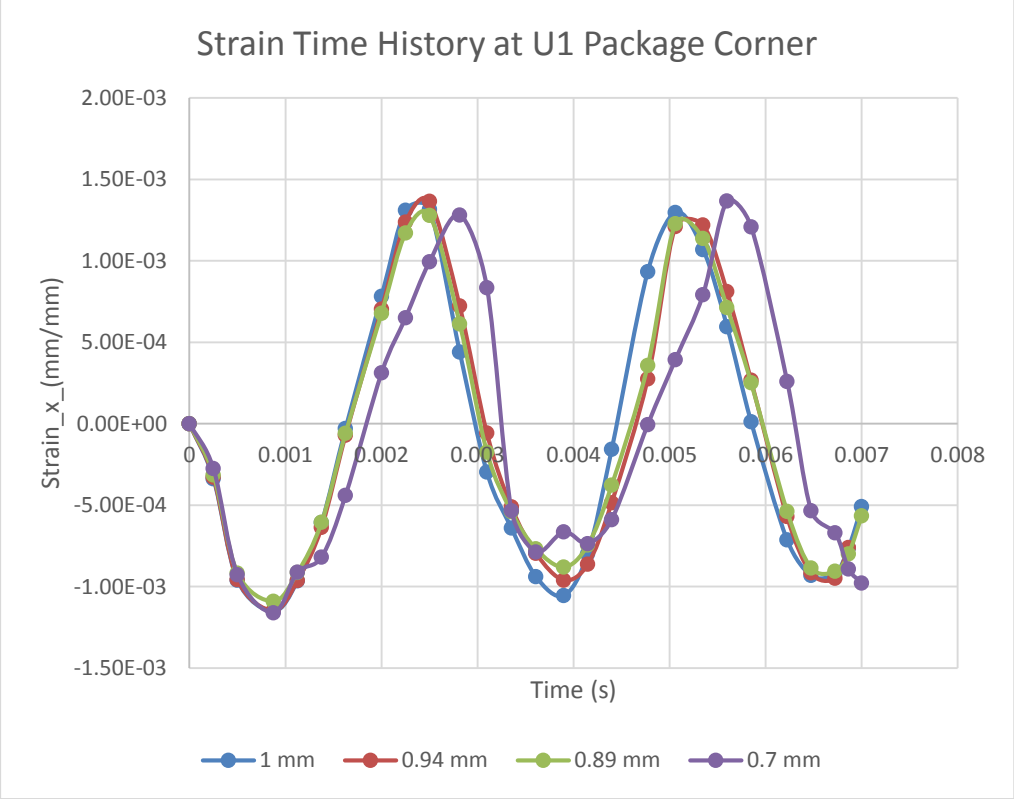

Figure 5.6: Strain Time History at the U1 Package Corner Location

From the above figure it can be seen that the 0.7 mm has the highest strain generation at this location too which is 0.00137 (mm/mm). And the lowest strain is generated for the 0.89 mm board which is 0.00128 (mm/mm). But this time 0.94 mm board has more strain than the 1.00 mm board and the value is 0.00136 (mm/mm). Except the 0.7 mm board all the highest strain has generated at a similar time around 2.5 ms but for the 0.7 mm board it took longer time and occurred at 5.6 ms (approx.).

Next, the strain at U2 package location has also considered. The strains are calculated as previously from bottom left corner location of the U2 package at the bottom of the PCB. Figure 5.7 shows the strain time history of the U2 package.

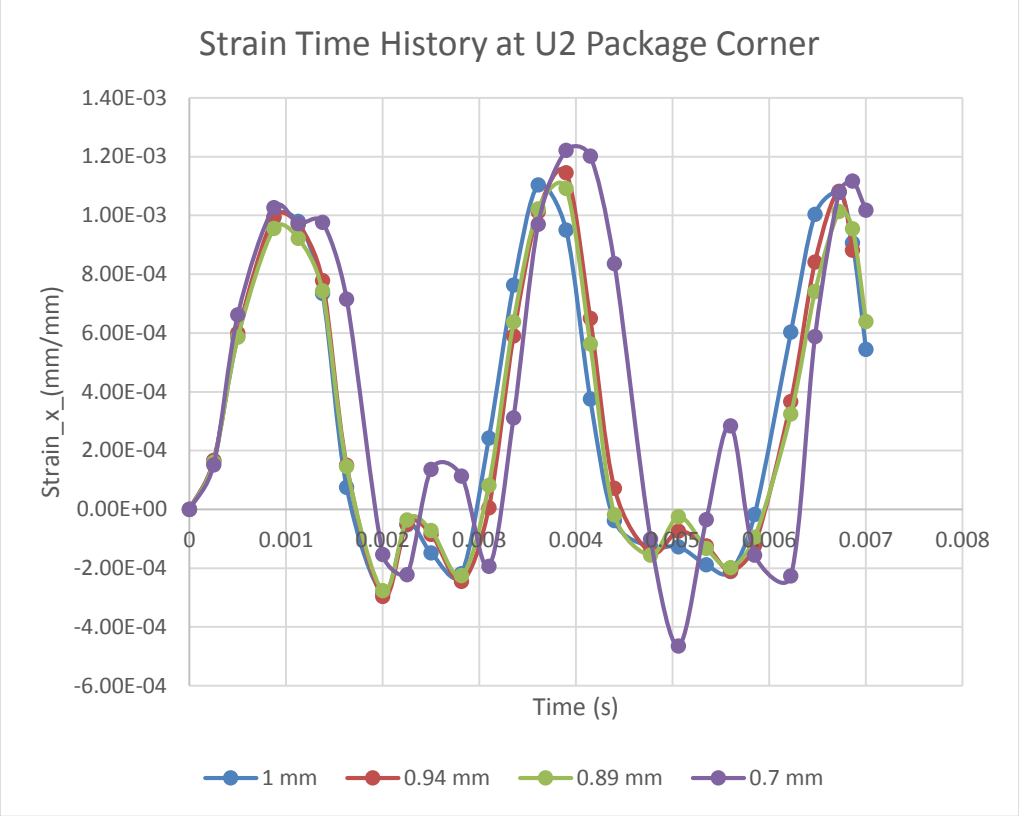

Figure 5.7: Strain Time History at the U2 Package Location

The overall strain at this location is less for all the boards than the U1 package location. From the above figure, at this location the highest strain is generated for the 0.7 mm board which is 0.00122 (mm/mm) and the lowest strain is generated for the 0.89 mm board which is 0.00109 (mm/mm) which is consistent with the previous results. For this location also the 0.94 mm board results in higher strain than the 1.00 mm board. The time require to produce this highest strain for all the boards do not follow the same pattern as before U1 package location. The peak strain is occurred for all the boards are at closely spaced time difference. Figure 5.8 shows the overall time history of the strain for all the boards at U1 and U2 package location.

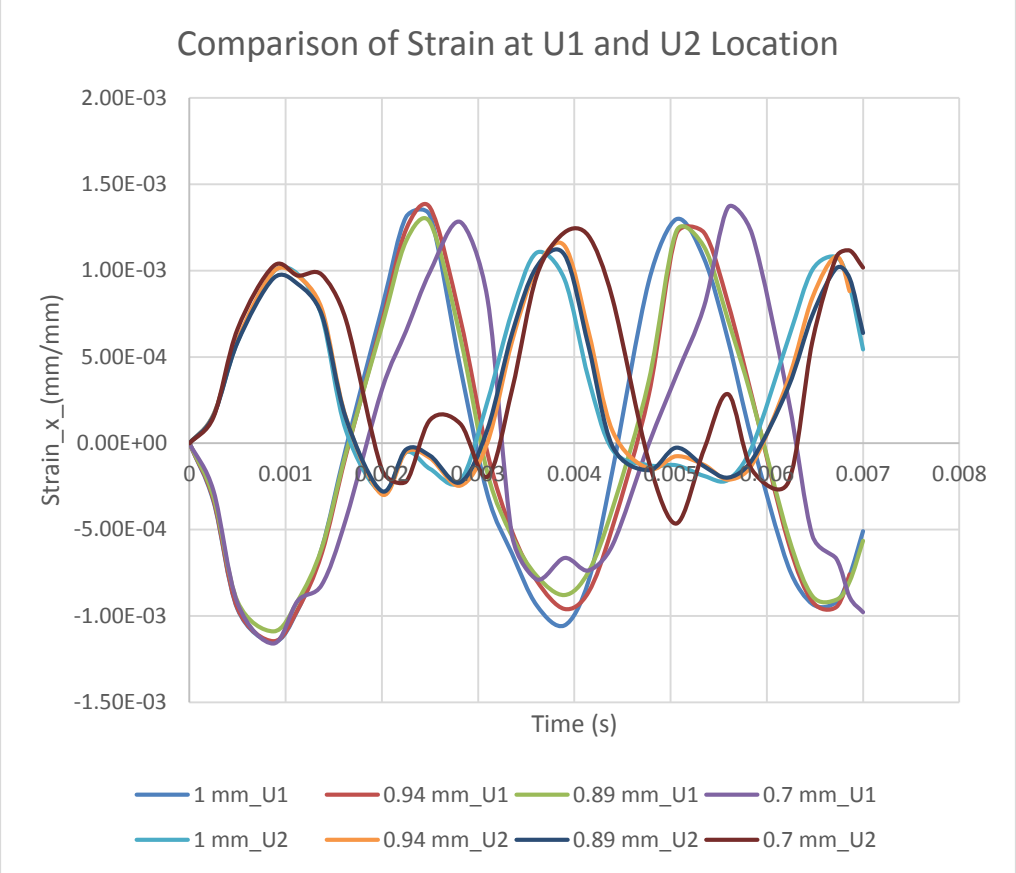

Figure 5.8: Comparison of Strain at U1 and U2 Location

This is evident from the above figure that at U1 location all the boards result in higher strain than the U2 location.

From the above observations it can be discussed that- the 0.7 mm board generated more strain rather than any other boards at any location and the 0.89 mm board results in lowest strain generation. For the 1.00 mm board and 0.94 mm board the results vary at the Package corner and PCB center location. And among all the strains the strain at U8 location or PCB center is highest for all the boards.

5.4 Board Strain Analysis

In this section stress distribution in the solder joints are calculated for different boards. The reliability of the interconnections is the main concern during the drop impact as this affect the functionality of the system. Researchers have been established that the dominant stress that causes the solder joints to fail is peeling stress. It has been researched that the first maximum principal stress follows the same pattern as the peeling stress and also the Von Mises stress reflects the same pattern of the peeling stress or stress at z direction (S_z) [18].

Figure 5.9-5.12 shows the maximum stress location at U1 package on the solder interconnections for 0.7 mm, 0.89 mm, 0.94 mm and 1.00 mm board respectively.

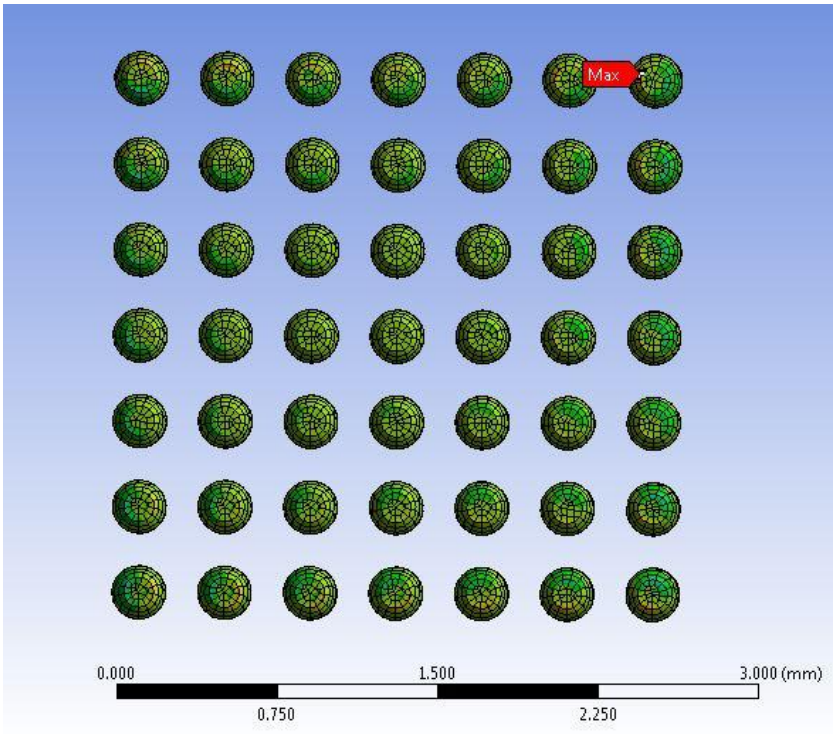

Figure 5.9: 0.7 mm maximum Stress at Corner Solder Joint

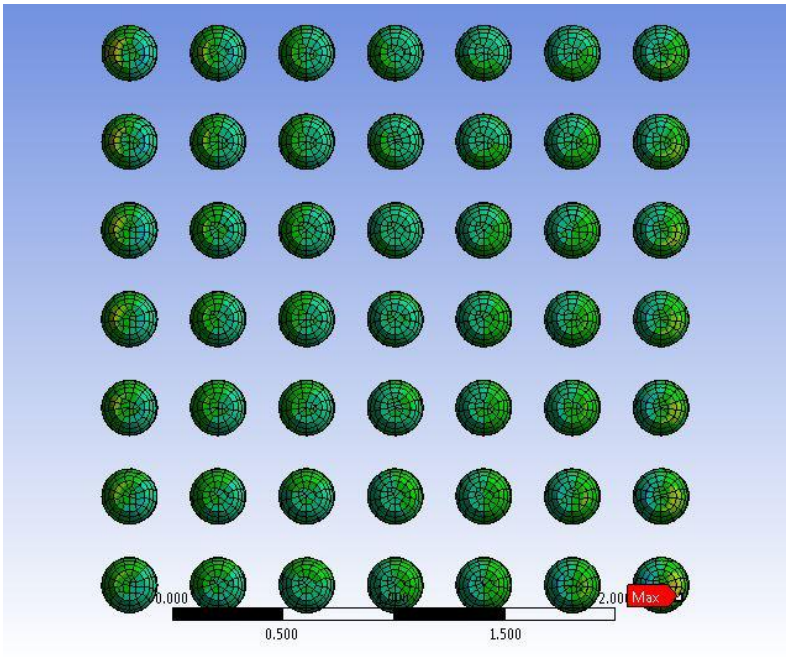

Figure 5.10: 0.89 mm Maximum Stress at Corner Solder Joint

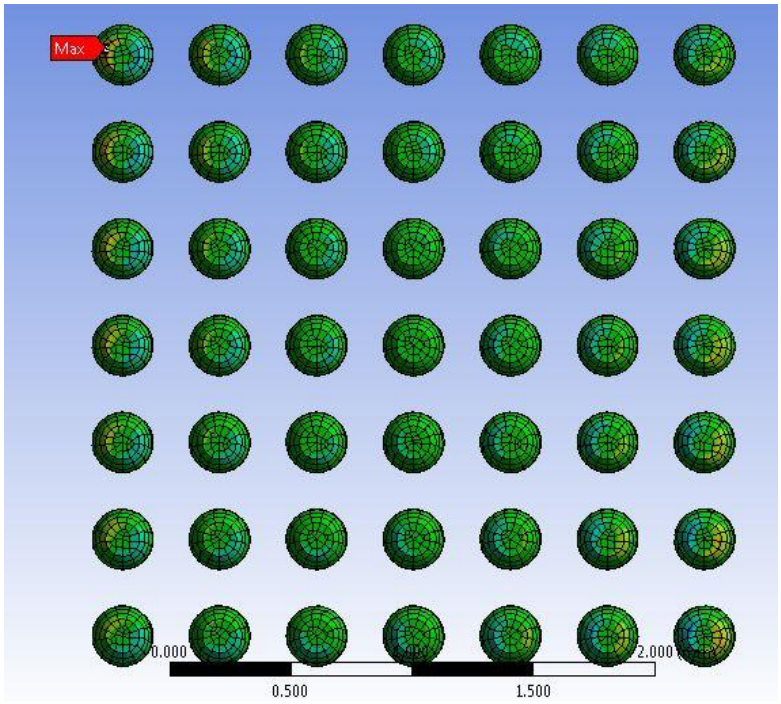

Figure 5.11: 0.94 mm Board Maximum Stress at Corner Solder Joint

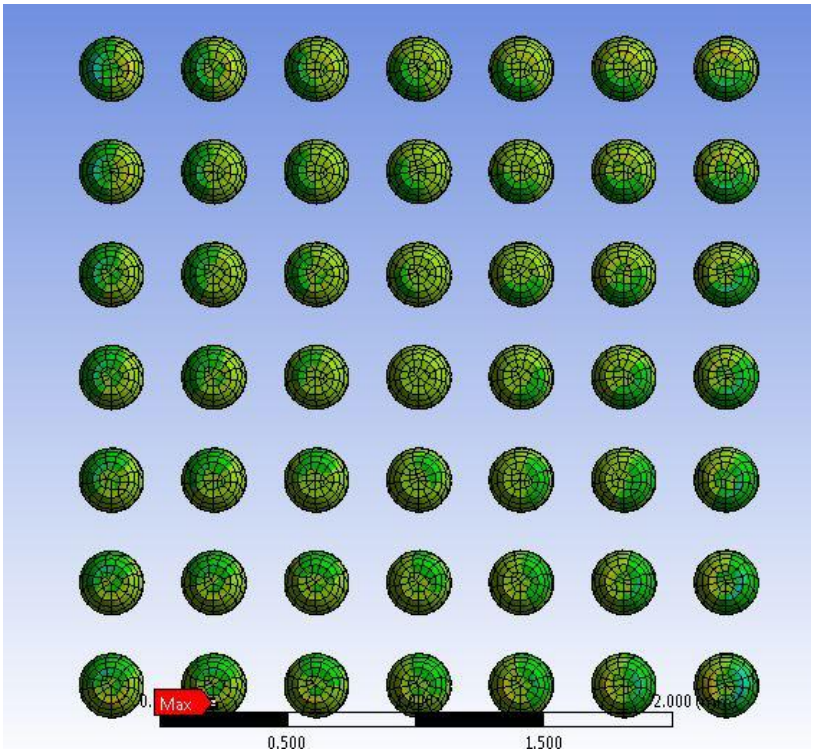

Figure 5.12: 1.00 mm Board Maximum Stress Location

From the above figures it can be seen that for the thin boards all the maximum stress is generating at the corner solder joints though it varies the position of the joint. For the 0.7 mm board it is on the top left corner, for the 0.89 mm board the location is bottom left corner, for 0.94 mm board it is at top right corner. Only for the 1.00 mm board the location differs slightly from the corner solder joint to the next right solder interconnection. This changing of location is due to the difference of the bending mode of the boards. This is clear that this location of the critical joint depends on the bending mode of the board and for different material properties the first mode varies significantly for each boards. This region of maximum stress for the 1.00 mm board is still considered as the corner position as shown by Chong et, al. [38].

Figure 5.13 shows the comparison of the maximum peeling stresses generated on the solder joints for different boards.

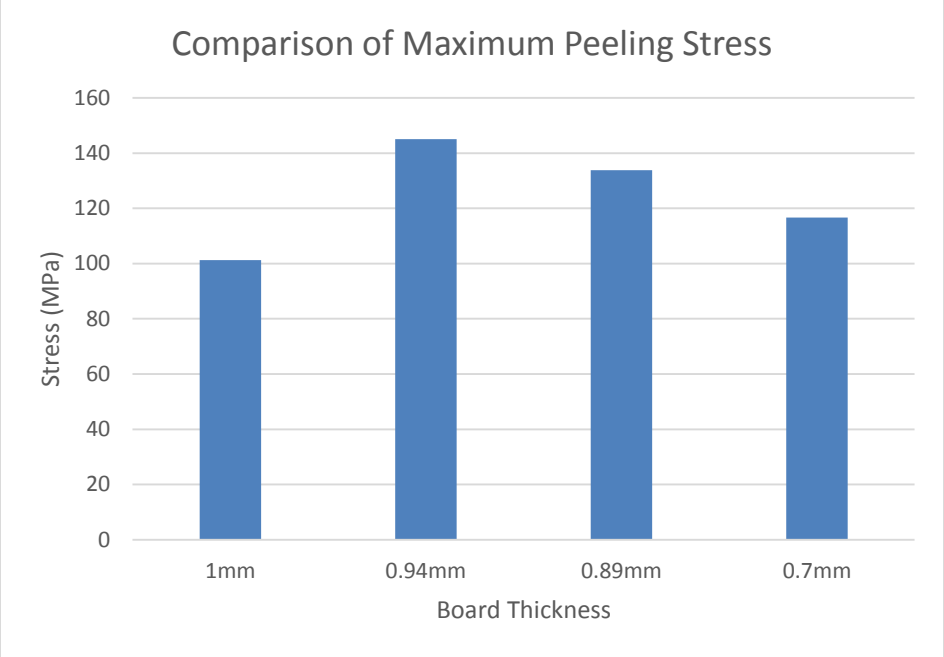

Figure 5.13: Maximum Peeling Stress Comparison

The above chart shows that, 0.94 mm board experiences the maximum stress and the 1.00 mm board experiences minimum stress at the solder interconnections. This happens due to the material properties difference. 1.00 mm board has the highest density and the highest copper percentage but not the highest elastic modulus compared to other boards and thus results in the lowest stress. But this is not definitive as this model only takes care of the isotropic material properties of the structures but not the orthotropic material properties or the nonlinearities present in materials.

Chapter 6

DYNAMIC ANALYSIS DUE TO ELEVATED TEMPERATURES

The temperature effect was considered for the 0.7 mm and 1.00 mm boards only. The temperatures were considered are as follows.

0.7 mm board	25°C	35°C	45°C	65°C	75°C
1.0 mm board	25°C	50°C	75°C	100°C	

Table 6.1: Elevated Temperatures for 0.7 mm and 1.0 mm Boards

Effect of temperature is studied similarly by calculating the deformation, strain and the solder joint stress of the local model.

6.1 Deformation of the Boards Due to Elevated Temperature

Figure 6.1 shows the deformation of the 0.7 mm board due to temperature effect. This deformation was calculated taking the full PCB as warpage.

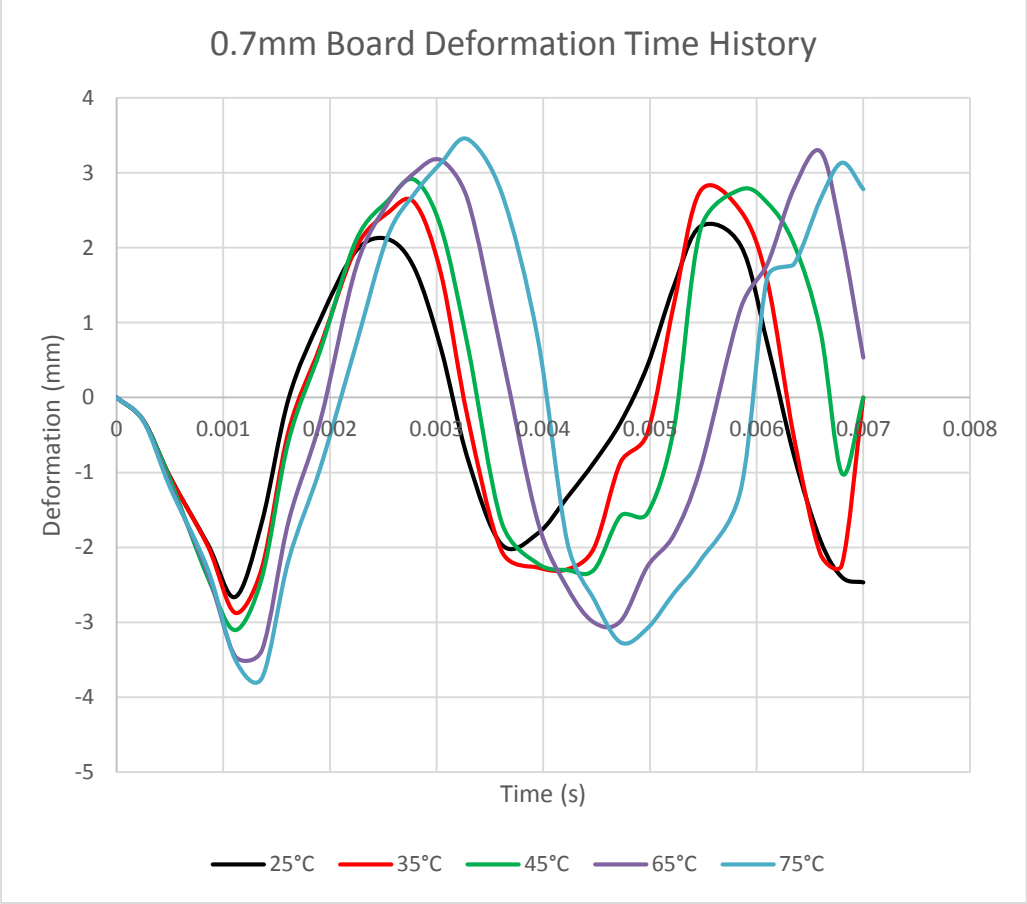

Figure 6.1: 0.7 mm Board Deformation at Different Temperature

The board deformation changes with the change of temperature and it follows a linear relationship with temperature change. The 1st positive and negative peak for all the temperature follows a simple linear relation with increasing time as shown in the above figure. Though the 2nd peak deviates from this trend. Furthermore, the maximum deformation at the 65°C and 75°C is much higher, more than 4 mm. This is because, when the temperature is increased than a certain range the board experienced distinct thermal loads and the drop load together. The explanation for this behavior lies in the low elastic

modulus at high temperatures and the joint loads together created high bending consequence on this thin board.

Figure 6.2 shows the deformation for the full PCB of the 1.00 mm board.

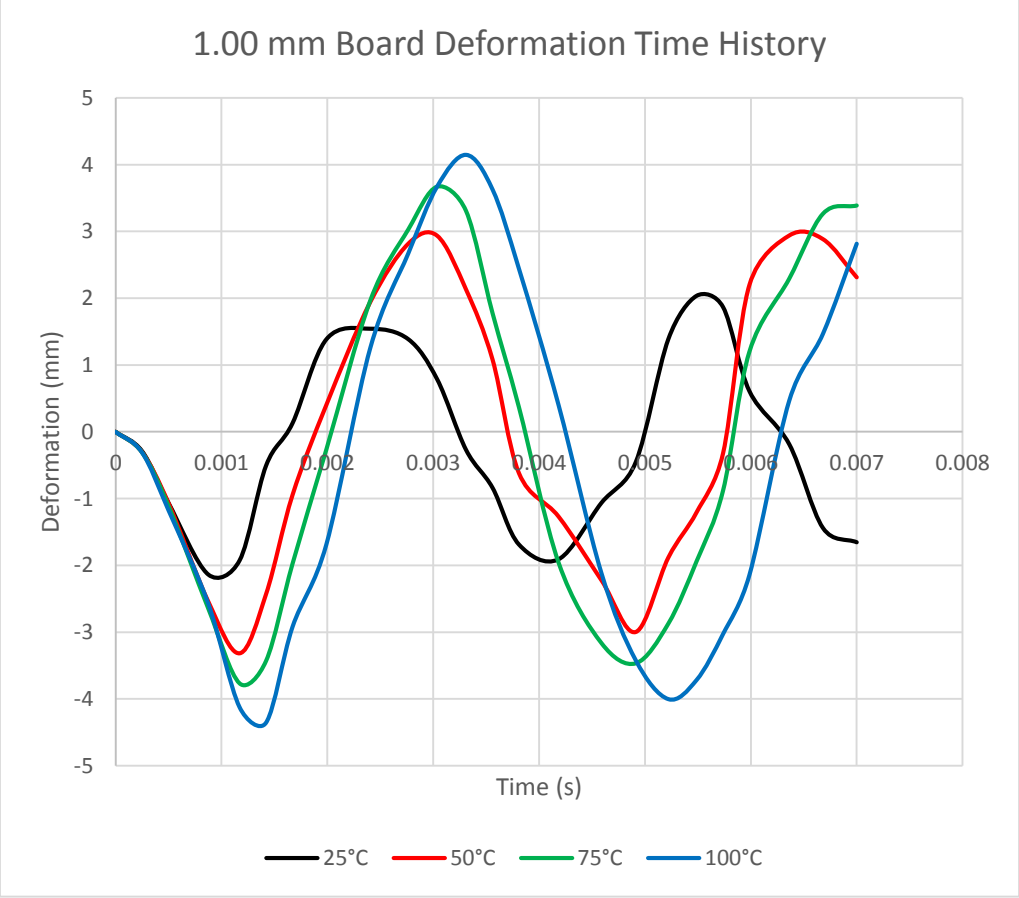

Figure 6.2: 1.00 mm Board Deformation at Different Temperatures

For the 1.00 mm board the deformation follows the sinusoidal wave for the elevated temperatures. From the above figure at 100°C, the first peak of deformation took place at 1.42 ms. The first peak at 100°C, took longer time to generate than the peaks at other temperatures. This maximum time is also greater than the time 0.7 mm board took to reach maximum. At 100°C the maximum deformation is 4.91 mm which is almost doubled the

value at room temperature which is 2.54 mm. The reasoning behind this behavior is 1.00 mm board has higher CTE than the 0.7 mm board and low elastic modulus at high temperatures. Thus, 1.00 mm board resulted in higher deformation. So increasing the temperature for both the boards caused in relaxing of the PCB material and resulted into increased deflection. Table 6.2 shows the percentage change in the deformation due to elevated temperatures.

Temperature	0.7 mm	1.00 mm
35°C	8.984381	
45°C	17.44158	
50°C		48.36134
65°C	33.16515	
75°C	36.60708	70.50692
100°C		93.05326

Table 6.2: Percentage Change in Deformation at Elevated Temperatures

It is obvious that the percentage change shows the difference of deformation between the two boards. It is mainly due to the smaller size of the package and the rapid change in the modulus also.

6.2 Temperature Effect on Strain

Like previous analysis the strain is calculated again for the change of temperature. This time the strain is calculated at a different location. Following Dhiman et, al. [22], the strain

measurement was taken along the path (1-2) on the top of the PCB. The (1-2) path was created by taking three points from the left bottom corner of the U1, U2 and U3 packages at a distance of 1 mm X 1 mm in x and y direction accordingly as shown in the Figure 6.3 below.

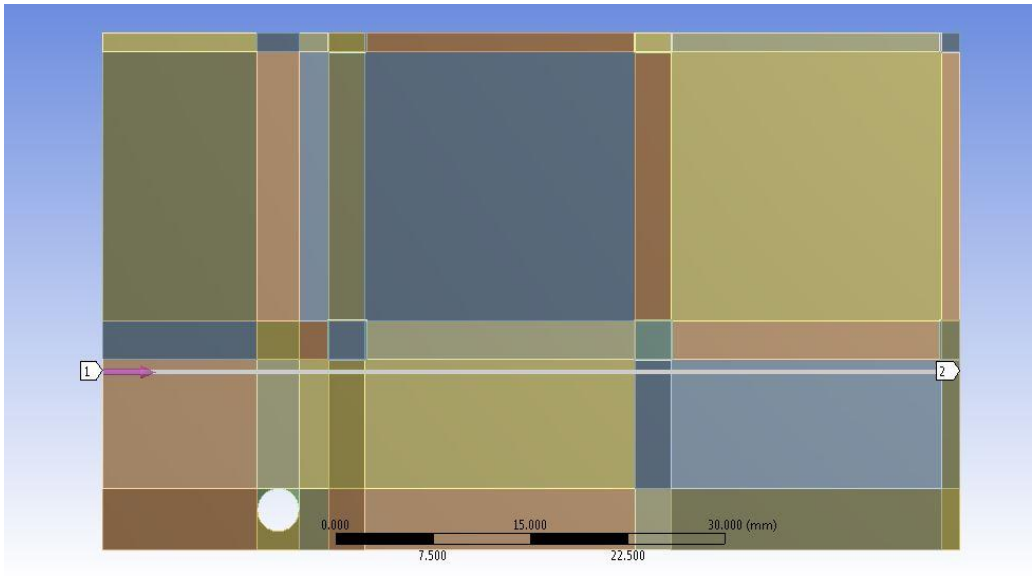

Figure 6.3: 1-2 Path along the PCB

The strain along the path 1-2 is shown in Figure 6.4 for the 0.7 mm board. The strain is measured along the x axis at all the elevated temperatures. In the Figure 6.5 the strain along the x axis for the 1.00 mm board is shown at the increased temperatures.

It is noticeable from the Figure 6.4 that after crossing the 45°C temperature the strain along the axis changes the direction and creates positive peak. For the 1.00 mm board all the temperatures was considered is equal or higher than 50°C. That is why all the strain curves created positive peaks at those temperatures. At 75°C for the 1.00 mm board the peak strain was 0.00248 (mm/mm) and for the 0.7 mm board the peak strain was 0.00188

(mm/mm). This is consistent with the deformation results. Because increasing the temperatures, resulted in increased deformation in the thicker board which ultimately leads to high strain values.

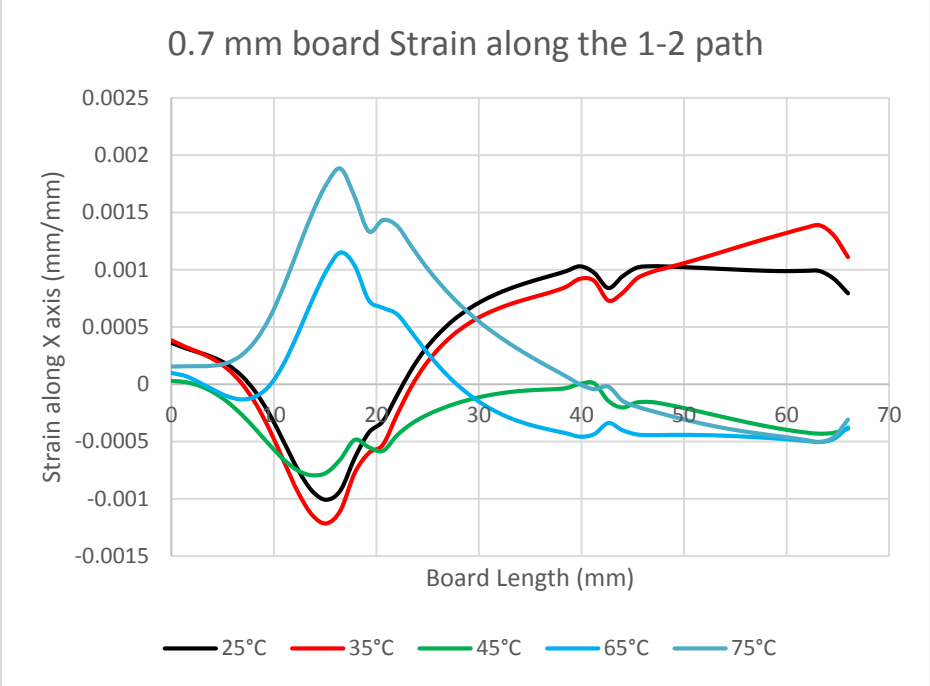

Figure 6.4: Strain at Elevated Temperature for 0.7 mm Board

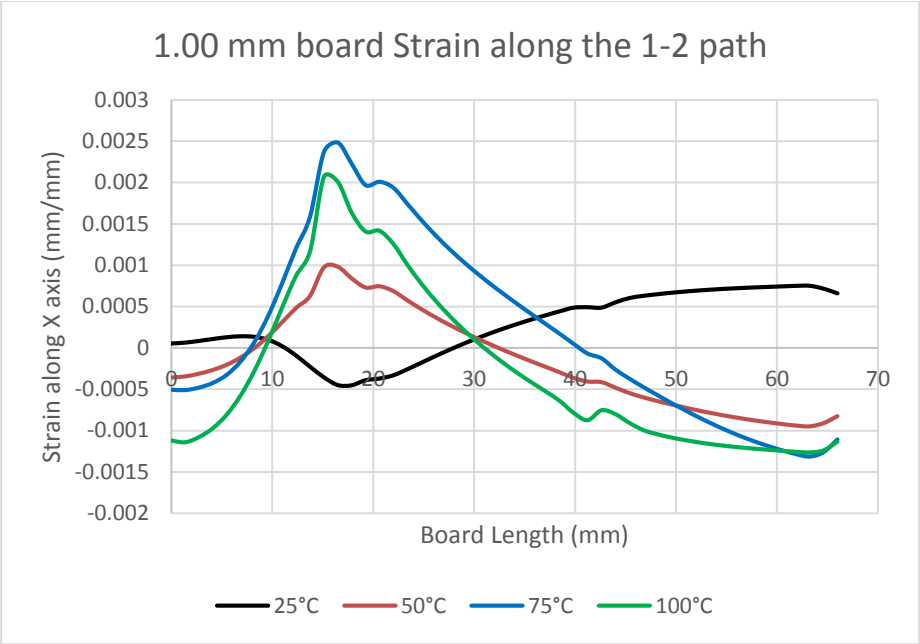

Figure 6.5: Strain at Elevated Temperature for 1.00 mm Board

The strain time history at the center of the PCB for the 0.7 mm board is shown in Figure 6.6 and for the 1.00 mm board is shown in the Figure 6.7 respectively.

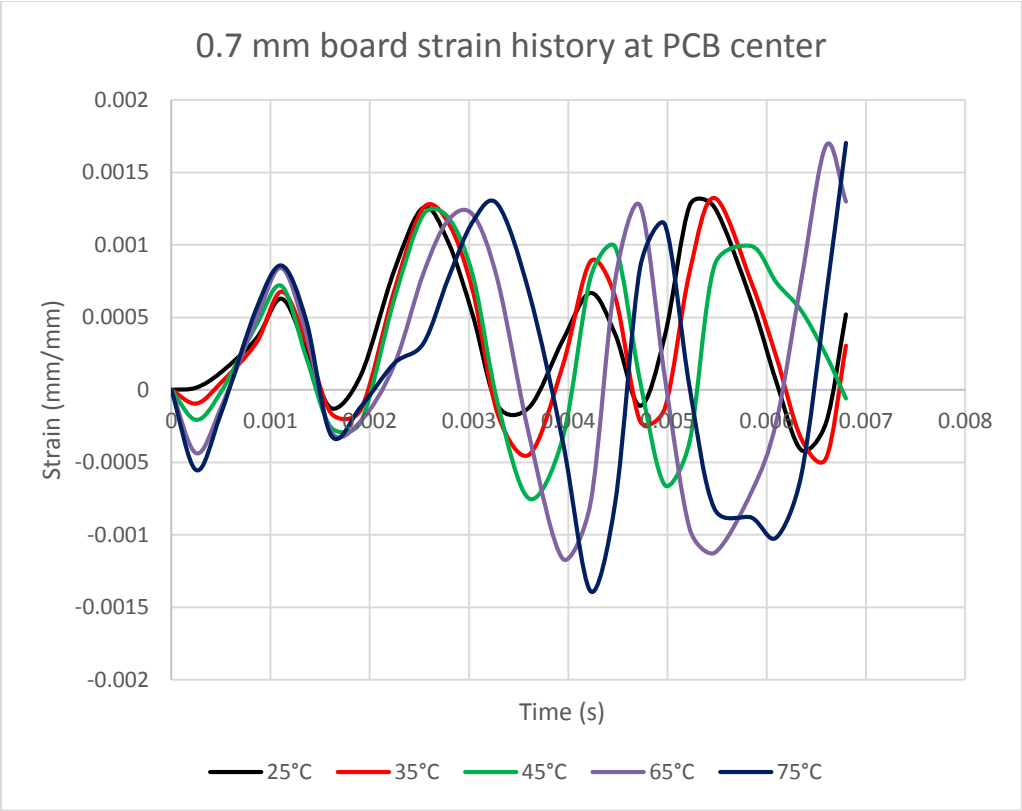

Figure 6.6: Strain Time History at the Center of The 0.7 mm PCB

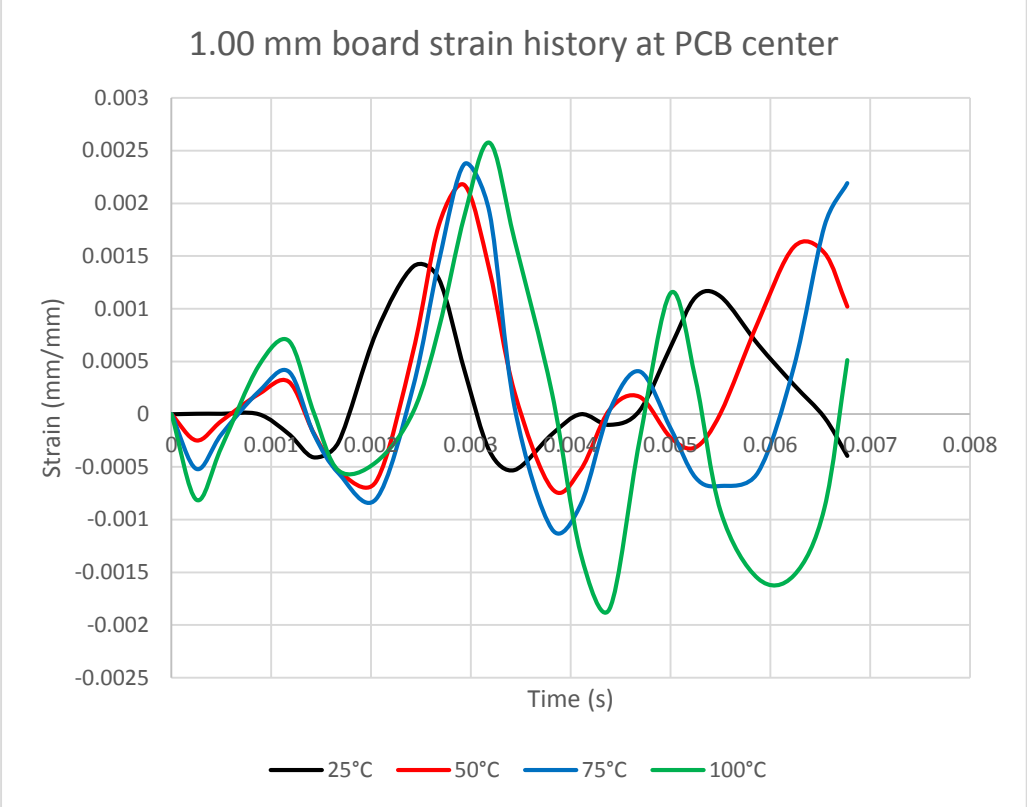

Figure 6.7: Strain Time History at the Center of the 1.00 mm PCB

From the above figure, at 75°C, for the 0.7 mm board the maximum strain was 0.0017 (mm/mm) and 0.00237 (mm/mm) for the 1.00 mm board. The maximum strain for 0.7 mm board took place at 0.00679 s and for 1.00 mm board was at 0.00293 s. For this location also increasing the temperature resulted in increased strain values for both the boards. But it should be noted that 1.00 mm board resulted in higher strain rate and magnitude than the 0.7 mm board.

6.3 Stress Variation Due to Elevated Temperature

The maximum stresses at the critical solders are shown in Figure 6.8. With increasing deformation, stresses induced in the solder interconnects for both the PCBs was increased. These stresses are calculated from the local model as before.

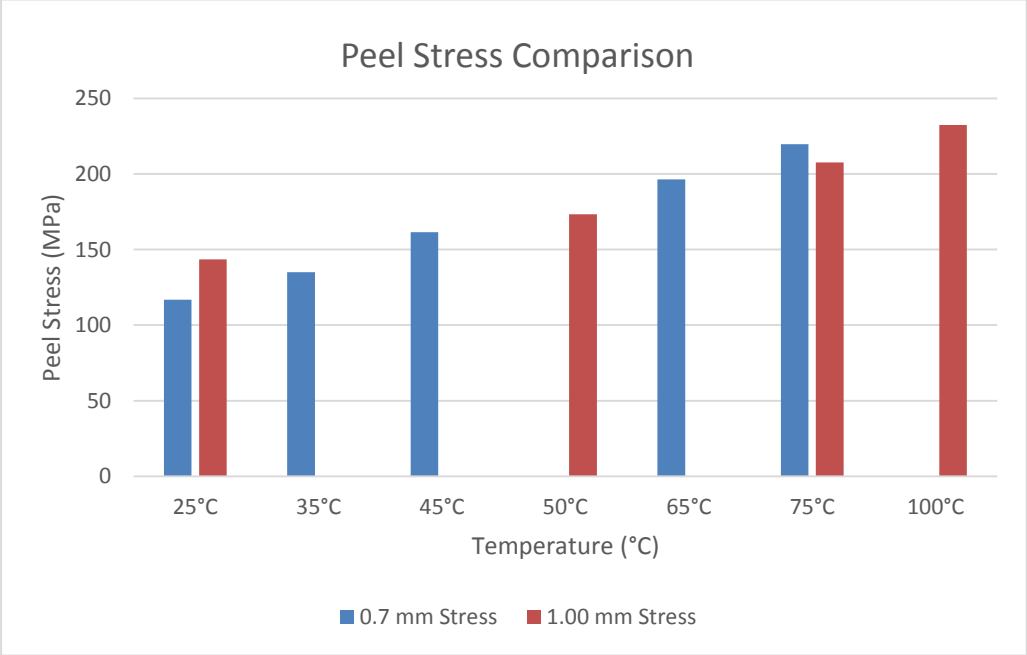

Figure 6.8: Peel Stress Comparison at Elevated Temperatures

At the highest temperature for 0.7 mm board the maximum stress was 219.69 MPa and for the 1.00 mm board the maximum stress was 232.54 MPa at 100°C. From the room temperature to 75°C the stress was increased for the 0.7 mm board was about 87.98% but for the 1.00 mm board the stress increased only 62.09% to the 100°C which is much less compared to the thinner board. These changes in stress at high temperatures are not exact as this simulation deals only with the linear elastic model for the solder interconnects whereas to get an accurate result plasticity is needed to be considered in the simulation.

But this helps us to understand the stress growth behavior of the thin and thick boards with the change of temperature. It is noteworthy that with increasing temperature the thick board generates more stress than the thin board as well as the percentage change is lower than the thin board.

Figure 6.9 and 6.10 show the peeling stress location for 0.7 mm and 1.00 mm board at 45°C and 50°C respectively.

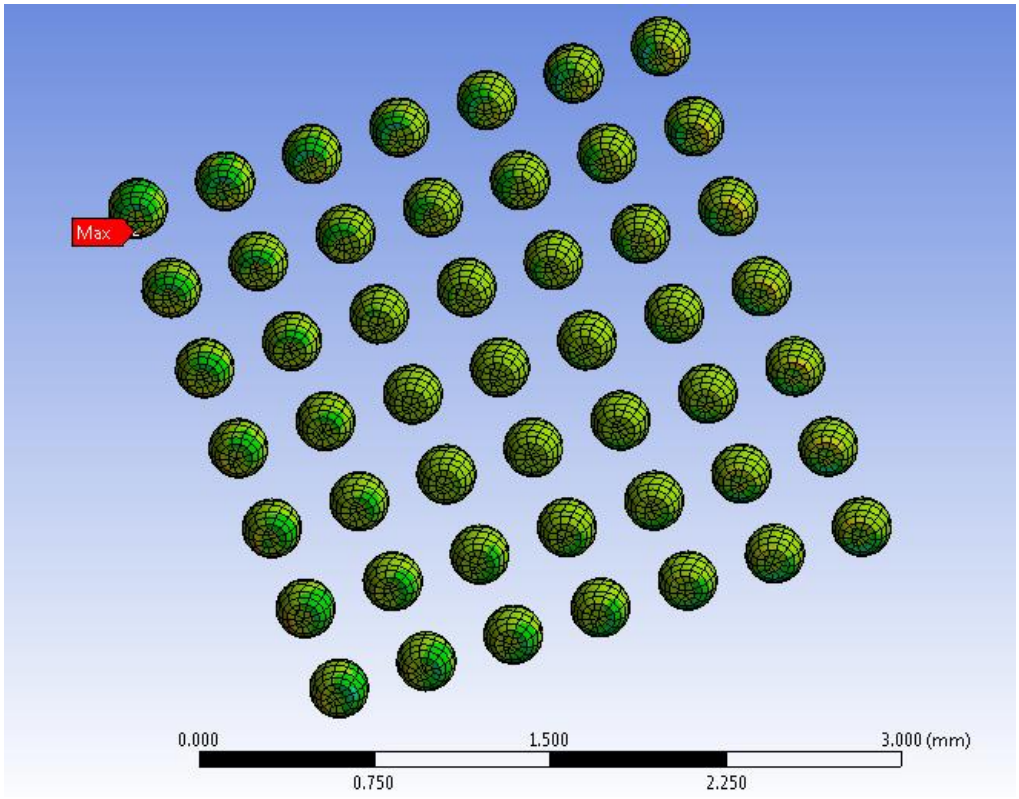

Figure 6.9: Peel Stress Location for the 0.7 mm Board at 45°C

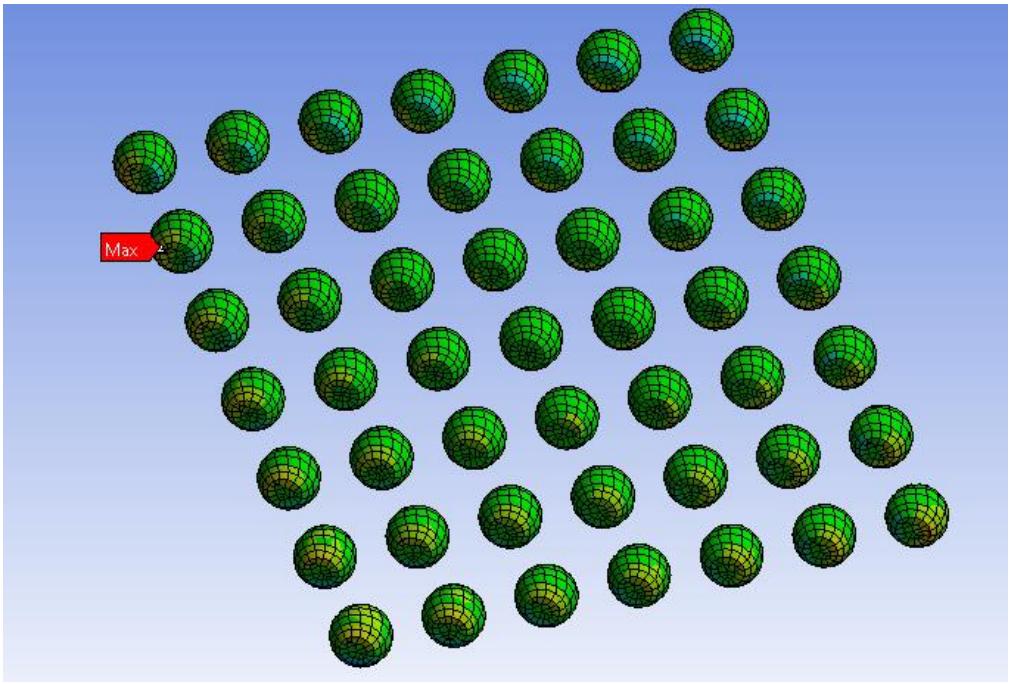

Figure 5.23: Peel Stress Location for the 1.00 mm PCB at 50°C

The maximum stress occurred at PCB side for all the temperatures for both the boards. The stress generation is always higher at the corner solder joints but for the 1.00 mm board, the maximum stress was generated at the 2nd solder from the right side of the corner ball as before at regular temperature analysis.

Chapter 7

SUMMARY & CONCLUSIONS

In this research, effort has been made to investigate the transient dynamic behavior of the board level assemblies due to drop test. The main focus of the research was to understand the boards behavior and solder joint reliability due to the change of

- Material properties
- Board Dimensional/Geometrical changes
- Thermal conditions

For that purpose, experimental technique was adopted to find out the required material properties of the interested boards. Then finite element modeling techniques was implemented to examine the dynamic behavior of the boards due to the impact load and generation of stress at the solder interconnections. To do that all the boards used in this research was followed by the JEDEC standard, but the packages was customer provided and was much smaller than the JEDEC defined IC packages.

First of all, the material properties were experimented maintaining experimental standards. For all the experiments multiple samples were selected and the mean results were taken. After that, FEM modeling was approached for the different boards and for different temperatures to analyze them due to the drop impact. In this effort, modeling techniques have been used to capture the transient strain of the boards and the transient stress of the solder interconnects. The models used to perform the FEM was used as symmetry model. And the technique was used is new and faster than previous ones as called Direct Acceleration Input (DAI) technique. Using this technique makes the simulation to run take less time than earlier techniques. The model used in this simulation was simple model

regarding the geometric details in the Global Model and full details in the Local Model. But the material properties were used was simple linear elastic material properties considering the structures material behavior as isotropic in nature. The results were found in the end is that the most better performance is given by the 1.00 mm board in environmental temperature and as well in the elevated temperatures. This was found in this study, by changing the above mentioned conditions in the simulation. As peel stress is proven to be the main cause of failure so that focus was made on the peel stress and, for all the local models the less peel stress was generated on the 1.00 mm board because of its elastic modulus and density combination. It is seen from the results, 0.7 mm has the highest peeling stress and strain generation. The acceleration response is also higher for it. 0.7 mm has a very high density compared to its thickness. This high density with less thickness is generating a lot of stress.

The effect of temperature was taken into account by evaluating the deformation of the PCB, normal strain along the x-axis and the peeling stress at solder interconnects. With increasing temperature, deformation increases for both the boards but for the thick board the maximum deformation was much higher than the thin board due to the variation in elastic modulus, CTE, and the dimensional difference. The stress generation on the solder interconnects increases with the increasing temperature due to external thermal load in addition to impact load but for the thin PCB, the percentage increase of stress generation is more critical than the thick PCB which may indicate the possibility of early failure of thin PCB instead of the thick one at elevated temperatures.

In this study, due to lack of resources, plastic model with orthotropic material properties could not be evaluated. In future, z-directional properties can be evaluated and can be put

in the model. This would give more accurate results and give a better understanding. Effective plastic strain can be measured for all the boards and can be compared. The simulation work can be compared and correlated with in-house experimental work in future. The results from the experiment can be used to create correlation parameters to get the life time of the boards.

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BIOGRAPHICAL STATEMENT

Anik Mahmood received his Bachelor's degree in Naval Architecture & Marine Engineering from the Bangladesh University of Engineering and Technology (BUET) in the year of 2012. He then joined in a heavy industry Ananda Shipyard & Slipways Ltd. as a Project Engineer and gained hands on experience in real life engineering problems in different fields. Then he worked as a Product Development Engineer in an Air Conditioner Manufacturer Company. Then he decided to pursue his Master's in Mechanical Engineering in the University of Texas at Arlington in Spring 2014. He joined the Electronics MEMS and Nano electronics Systems Packaging Center (EMNSPC) and started working as a Graduate Research Assistant. He has been actively involved in the research and his interest is in thermo-mechanical reliability, material characterization, simulation and analysis. He also worked as an Intern at the University of Texas at Arlington Research Institute for 6 months. During his time in the EMNSPC lab, he was an integral part of the SRC funded project with Texas Instruments and closely worked with the team. Upon graduation, he plans to pursue his career in the direction where his experience and expertise are utilized most.