EVALUATE THE USE OF FPGA SoC FOR REAL TIME DATA ACQUISITION AND AGGREGATE MICRO-TEXTURE MEASUREMENT USING LASER SENSORS.

By

MUDIT PRADHAN

Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE IN COMPUTER SCIENCE

THE UNIVERSITY OF TEXAS AT ARLINGTON

AUGUST 2016

Copyright © by Mudit Pradhan 2016

All Rights Reserved

Acknowledgements

I would like to extend my deepest regards and gratitude towards my thesis committee chair, Dr. Roger Walker who has been a continuous source of motivation to me throughout this thesis work. His deep knowledge, patience and enthusiasm have always encouraged me to perform better and working with him at Transport Instrumentation Laboratory has been truly a great learning experience. This thesis would not have been successful without his guidance and support.

I wish to express my thanks to my committee members, Dr. Ramez Elmasri and Dr. Bob Weems for their continuous support and guidance.

A special thanks to Mr. Wenming Kuo for his advices and technical discussions which helped me a lot to improve my understanding in all aspects.

Finally, I would like to thank my family and friends for extending their support throughout my Master's degree program.

July 20, 2016

Abstract

EVALUATE THE USE OF FPGA SoC FOR REAL TIME DATA ACQUISITION AND AGGREGATE MICRO-TEXTURE MEASUREMENT USING LASER SENSORS.

Mudit Pradhan, MS

The University of Texas at Arlington, 2016

Supervising Professor: Roger Walker

Aggregate texture has been found to play an important role in improving the longevity of highways and pavements. Aggregates with appropriate surface roughness level have an improved bonding with asphalt binder and concrete mixture to produce a more durable road surface. Macro-texture has been found to effect certain other important features of the road surface for example, the skid resistance, flow of water on the surface and noise of the tyre on road. However, more research need to done to access the impact of surface texture at micro-meter level. Accurate measurement of the micro-texture at high resolution and in real-time is a challenging task. In the first part, this thesis work presents a proof of concept for a laser based micro-texture measurement equipment capable of measuring texture at 0.2 micro-meter resolution, supporting a maximum sampling rate of up to 50 KHz with a precision motion control for aggregate movement at a step size of 0.1 micro-meter. In the second part, usability of field programmable

gateway array (FPGA) System on chip has been evaluated against the need for high speed real time data acquisition and high performance computing to accurately measure micro-texture. Hardware architecture is designed to efficiently leverage the capabilities of FPGA fabric. Software is implemented for dedicated multi-softcore operation, concurrently utilizing the capabilities of the on-board ARM Cortex A9 applications processor for real-time processing needs and a high throughput Ethernet communication model for remote data storage. Evaluation results are presented based on effective use of FPGA fabric in terms of data acquisition, processing needs and accuracy of the desired measurement equipment.

Table of Contents

List of Illustrations

List of Tables

Chapter 1

INTRODUCTION

Texture is considered to be a crucially important feature of aggregates used to develop a high quality adhesive system with asphalt binder and concrete mixture for the construction of road infrastructure and pavement. Texture features have also been found to determine several other important road characteristics such as high speed and low speed skid resistance [3], noise of the tire and surface drain ability. Several measurement techniques have been devised worldwide to measure texture. A camera based measurement device is currently being used by Texas Department of Transportation which uses image data to measure aggregate shape, angularity and texture. However, a more accurate, higher resolution measurement system is required which could produce more reliable results based on the data acquired from the aggregate surface facilitating the measurement of macro-texture and micro-texture. The figure 1.1 shows an example of high accuracy laser based road surface profiling system developed at UTA transportation laboratory.

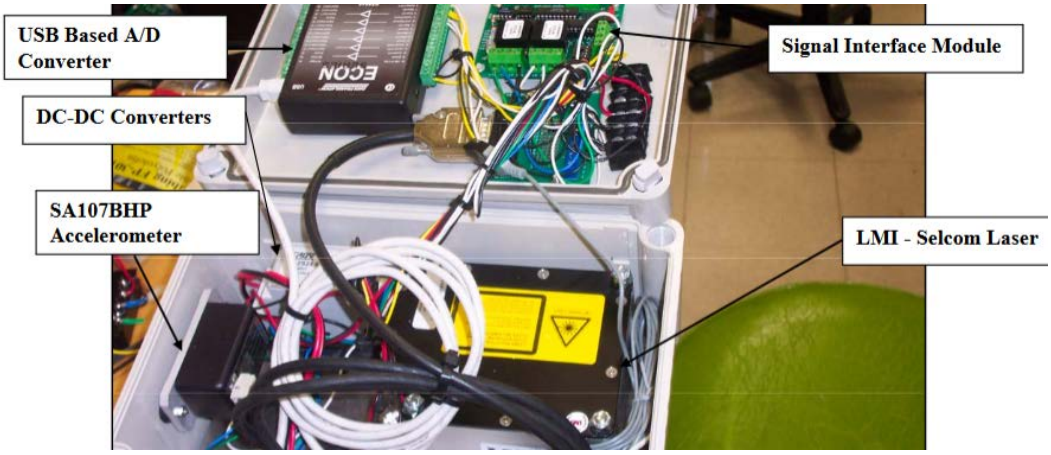


Fig 1.1 A laser based road profiler. [10]

Field Programmable Gateway Array (FPGA) have played a significant role in embedded engineering for more than three and a half decades now. These devices are best known for their on-demand configuration capability, which means that once manufactured with a definite

number of logic elements, these devices have the capability to be reconfigured an infinite number of times as long as the exact requirements of the desired integrated circuit are met. As opposed to Application Specific Integrated Circuits (ASICs) which need to be synthesized on the silicon each time an incremental circuit development is required, FPGAs serve as a rapid prototyping platform where every required incremental circuit/feature could be synthesized to FPGA logic using a suitable hardware definition language (HDL). This significantly reduces the cost of developing integrated circuits as new silicon synthesis is not required for every new hardware revision. In addition to this, a standard FPGA solution has been found to consume significantly less amount of power as compared to it ASIC.

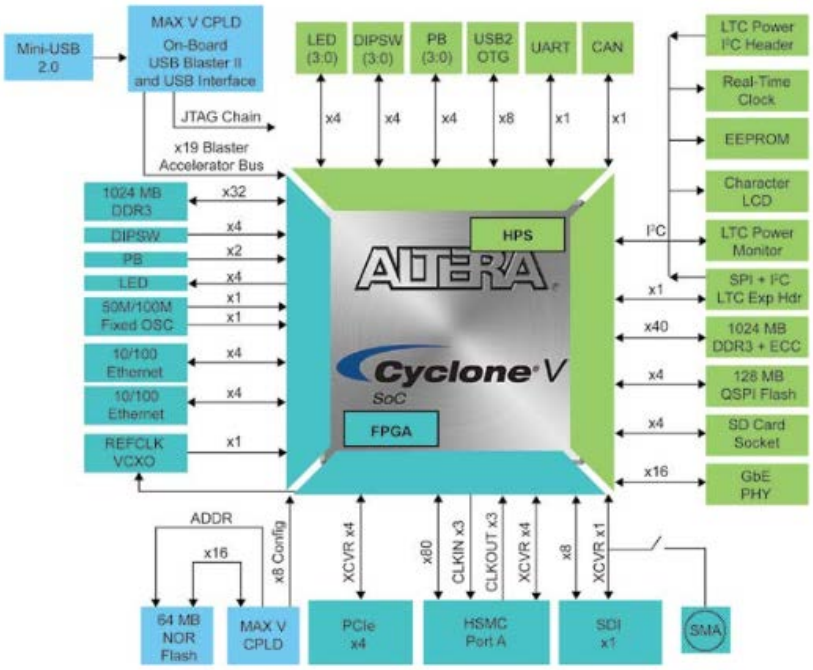


Fig. 1.2 Block diagram of Altera ARM based SOC chip. [11]

In modern-day computing infrastructure, FPGA manufacturing firms are continuously improving the products majorly by adding more peripheral support, increasing the number of logic elements, increasing memory blocks and reducing the power consumption to suit the increasing requirements of the market. This rapid growth has added to the exploration of FPGA capabilities and various new aspects of using FPGA have been found in recent times such as

using FPGA as real-time reconfigurable device which could adapt to the needs of environment, adding ability to design multiple softcore processors to support massively parallel processing architectures and designing hybrid system architectures of FPGA in addition to other advanced processing units to leverage FPGA capabilities along with the benefits of conventional hard processing system.

FPGAs have found applications in some of the most advanced computing machineries existing in the world today. Below is a list of few such examples:

1. Pattern recognition and data analysis for Large Hadron Collider where around 100K events are converted to analog pulse and sent to FPGA based solution to digitize the input at a rate of 3.4 GB/sec[2].
2. Radio astronomy at Center of Extraterrestrial Intelligence (SETI) project at University of California-Berkeley, where a system of 5 Xilinx FPGAs perform 29.4 GMACs (million multiply-add per second) [2] for astronomical data processing.

Few examples of ongoing future developments using FPGAs:

1. Intel® has announced a hybrid XEON® processor which uses FPGA fabric attached coherently for accelerating cloud workload [17].
2. Evolvable hardware using FPGAs for designing self-adaptive systems. [18]

FPGA based solution have their own proven benefits and the fact that it is finding application in many upcoming computing machineries, make FPGA a perfect evaluation candidate for any upcoming embedded platform.

1.1 Surface Texture Estimation

The texture is a combination of surface consistency and its roughness, it can be categorized into micro-texture, macro-texture and surface roughness. The measurement system should be capable of measuring at the level of micrometer resolution for accurately categorizing the aggregates into smooth, moderate and high texture samples.

- Micro-texture: The roughness characteristics of the surface which could be measured ranging approximately from 0 mm to 0.5 mm. Micro-texture of aggregate has been found to play an important role in deciding the road friction.
- Macro-texture: The roughness characteristics of the surface which could be measured ranging approximately between 0.5 mm to 50 mm. Macro-texture has been found to be responsible for tire wear, road friction as well as road noise.
- Mega-texture: Any feature or characteristic of the surface which could be measured approximately between 50 mm to 0.5 m is considered as mega texture. Mega-texture level has been found to affect towards the discomfort in the vehicle and vehicle wear.

1.1.1 Texture Estimation Technique, Mean Profile Depth(MPD)

MPD is a method which gives a single value result that can be used as a surface texture estimation and its roughness level. It is a good estimation but it does not describe the composition of the texture since it gives an estimate for the overall texture across a measurement range. The below figure shows MPD calculations along with the parameters used for the calculations.

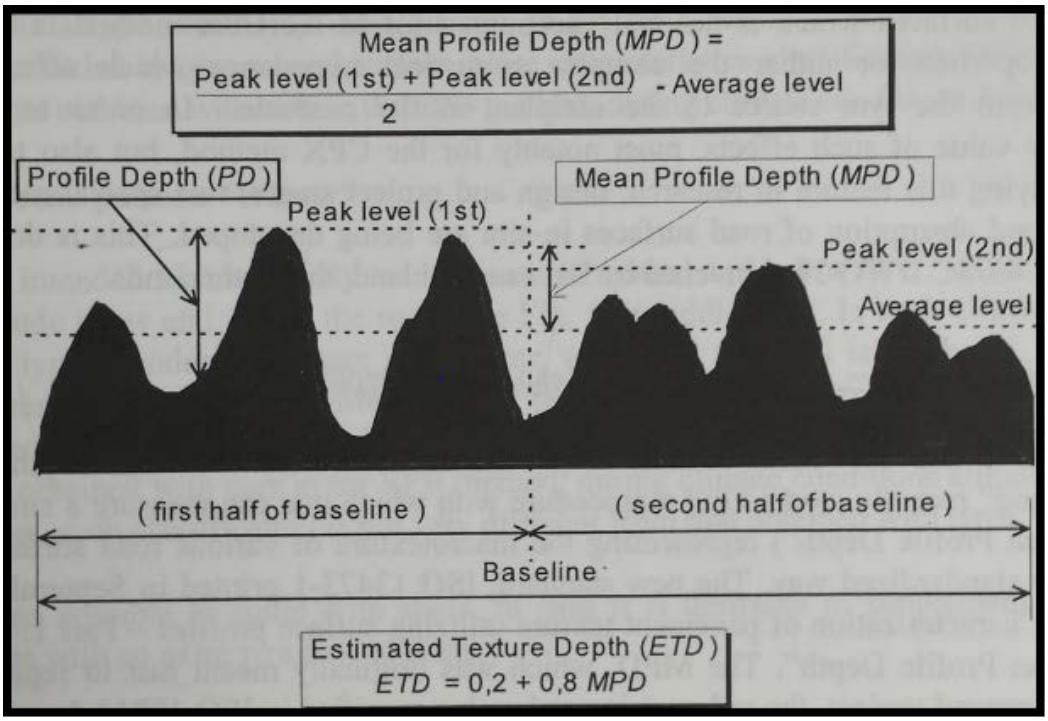


Figure 1.3 Profile Depth and Mean Profile Depth calculations. [12]

1.2 The Need For a High Resolution Laser Based System

For fine grained texture measurement and research study task, high resolution laser sensors which could be used to measure surface depth at micrometer level serve as a compelling platform. Some texture measurement systems have used high definition camera based approach to find the texture levels in past, but certain shortcomings and erroneous outcomes were observed due to the fact that a camera based system does not actually measure the surface depth level but uses image processing technique for predicting the surface properties. Laser sensors on the other hand, have been used in various profiling equipment including the state-of-the-art road profiler at UTA transportation laboratory and are proved to be standard measuring platforms in terms of accuracy and performance.

The current camera based measurement equipment used by Texas Department of Transportation to classify texture is called AIMS. It uses wavelet analysis to characterize

aggregate shape, angularity and texture. The AIMS provides misleading information sometimes when scanning aggregates of a varying colored surfaces. This is considered as a significant error as it results in incorrect categorization of the aggregates. So, there is a need to investigate the application of latest laser technology available for determining the texture and to compare these measurements with the existing AIMS system, Identify its shortcomings over laser based solution and create more advanced scanning techniques to improve the current aggregate surface analysis. The figures below illustrate a complete AIMS system and the groove for aggregate placement.

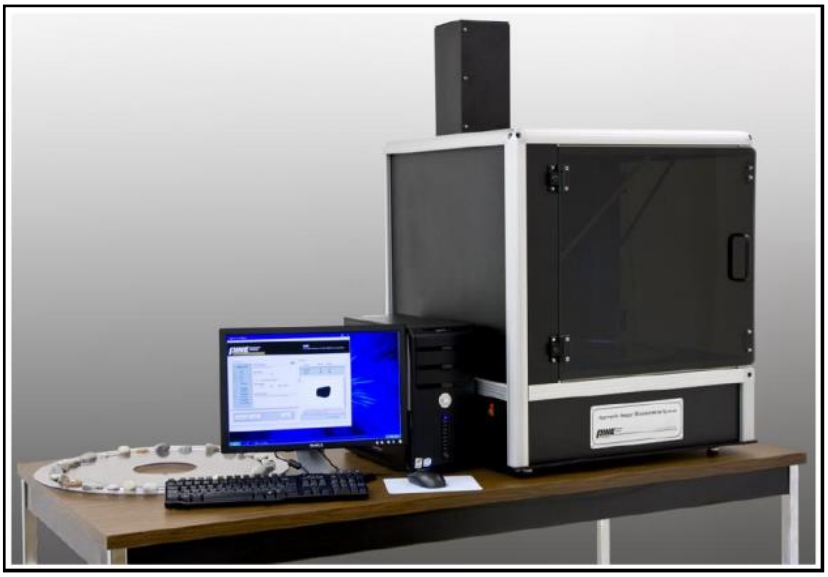


Figure 1.4 AIMS, Aggregate Imaging Measurement System. [13]

1.3 Objective and organization of thesis

In Chapter 2, a background study for a laser based texture measurement instrument has been discussed in details.

In chapter 3, the proof of concept established at embedded instrumentations lab, UTA for a laser based micro-texture measurement system. The hardware and software requirements were analyzed and results obtained were compelling.

In chapter 4, DE1-SOC FPGA board has been introduced, hardware and software programming techniques and main features of the board have been discussed in detail.

Chapter 5 is used to illustrate the hardware and the software design architecture and implementation for an advance multicore and multithread data acquisition and control system based on laser sensor.

Chapter 6 illustrates the results obtained, conclusion and future work.

Chapter 2

BACKGROUND STUDY

A pavement and surface measurement system was designed and implemented at UTA Transportation laboratory several years ago. This measurement system used non-contact laser sensors for the texture measurement at highway speeds. The measurement instrumentation was developed for both, micro-texture and macro-texture using single point high resolution laser sensor along with two translation stages for X-axis and Y-axis respectively. It was designed to capture raw measurement data readings from the analog laser sensor made by Selcom. The control system was made up of a power and interface module, a displacement control system from Newport and a data acquisition chip that directed the laser data to an embedded PC. The figure 2.1 shows block diagram of the control system.

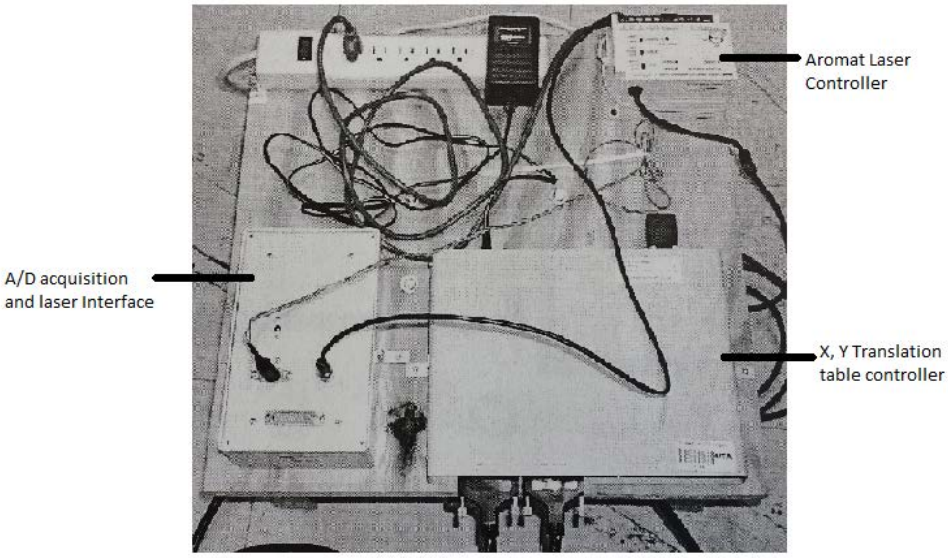


Figure 2.1 Block diagram of the laser based measurement system. [4]

2.1 Hardware components and description

2.1.1 Aromat Laser

Aromat laser manufactured by Matsuhita Electric Works, Ltd. was deployed for reading the surface data. This laser diode has a wavelength of 780nm, it is capable of making measurements close to 1 μm at 30Hz laser refresh rate.

2.1.2 Two Newport Translation tables

It consists of two translation tables which could traverse up to a range of 150 mm at a maximum speed of 2.5 mm/s, the translation tables used could step at a precision of 1 micrometer step size making it possible to collect laser data at every micrometer movement of the translation stage. The two translation stages are used to traverse in both X and Y-axis. The user specifies the distance to be traversed in X and Y axis respectively, the laser scans the target surface on X axis for all the specified Y axis positions.

2.1.3 The Controller

The controller consisted of a HC11 Motorola microprocessor, a 16 bit A/D converter, laser interface box and a LPT port for the embedded PC connectivity. The readings from Aromat laser scanner are read and digitized through the A/D converter and stored in 32 bit integer format into a FIFO buffer which is then read by the LPT port of the PC. The controller also sends and receives the commands for the operation through the LPT port.

2.2 Software design and flow control

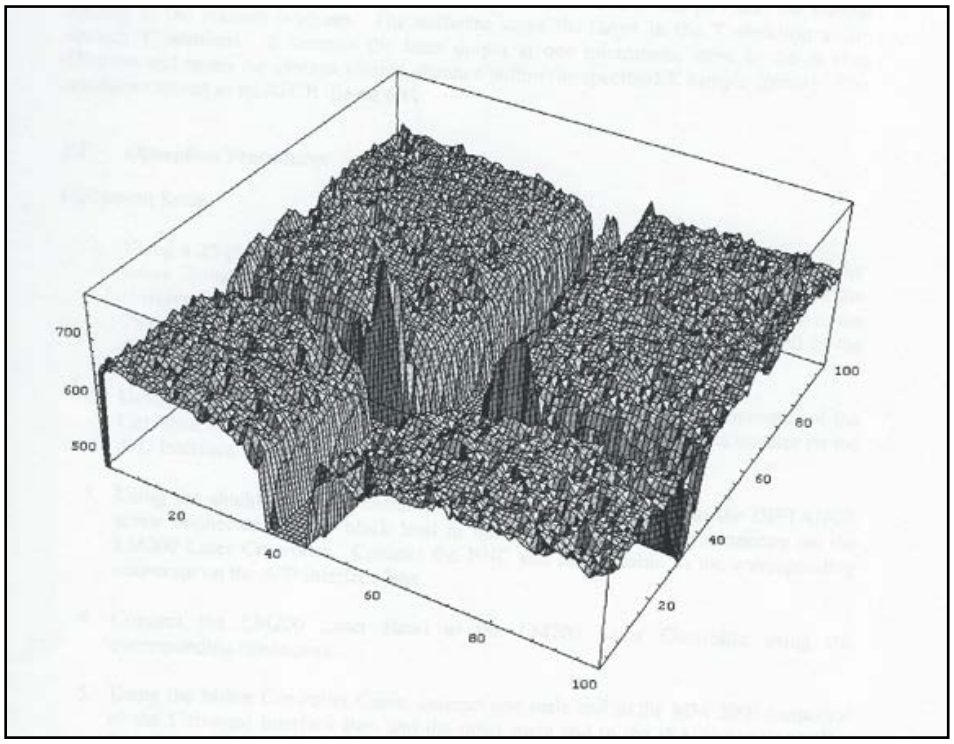
There were three modes of operation, read a single value, continuously read values, and data collection mode. The data collection mode required the user to input the data format, file name to store the data, translation distances in X and Y axis for the measurement and display the scanned information once the operations get finished.

The C program provided a user interface which could be used for sending commands to controller, read data from the controller and control the two translation stages. The commands

were used to start/ stop the data acquisition and also specify the mode of operation for the movement and data collection through the FIFO.

2.3 Sample Outcome

Figure 2.2 shows a three dimensional cross section scan of a commercial tile joint at the floor modelled from the data obtained through the above system. It provides a clear image of the surface depth and roughness distinguishable at micrometer precision level.



2.2 Figure three dimensional scan of a tile joint at UTA floor. [4]

Chapter 3

INITIAL SYSTEM AND PROOF OF CONCEPT

Initial study was performed on the hardware and software requirements of the texture measurement system and the ways in which its outcome could be processed to generate a meaningful result in the form of texture category identification. Various laser based equipment have been devised at the UTA transportation laboratory and therefore many considerable laser sensors and sensor controllers were available in the inventory for beginning with the conceptualization of the laser based measurement system initially. Since all the measurements required micrometer level precision, one of the most important component to be focused was the linear stage and the high precision motion controller. As the quality of the results obtained would heavily depend on data from the sensor, another area of careful investigation was the data acquisition chip required for digitizing the analog signals from laser sensor.
Identification of the major components needed careful study of the system requirements and the best techniques for the formulation of results. Investigations were made on all available components to identify the ideal specification of the system components for correct texture classification. Below listed are the major system components:

1) Laser Sensor and controller.
2) Linear stage and precision motion controller.
3) Data acquisition A/D convertor.
4) Embedded PC or board for data acquisition and system control.
5) Operating system for embedded PC.
6) Data acquisition device drivers and motion controller device drivers.
7) Software development environment for processing and visualizing the data.

This chapter would discuss about all the hardware and software considerations for the initial system which could be used to establish the proof of concept. Further it would discuss and

propose specifications of an advanced system based on the study and results obtained from the experiments performed.

3.1 Hardware

3.1.1 Laser Sensors and Controllers

Laser sensors being the most critical and expensive part of this measurement instrument, required detailed investigation and experimentations to proceed further. There are two categories of laser sensors available in the market.

- Single point laser
- Line laser

Single point lasers operate on the principle of triangulation. A laser beam is emitted through the laser emitting semiconductor element towards the target, the image of this laser beam is recorded by a receiver which is a position sensitive device or a line scan camera. Illuminated pixels on the received line are based on the distance between the object and the sensor, those pixels are evaluated by the digital signal processors and distance is predicted as a result. Measured values are transmitted as analog or digital signals based on the capabilities of the laser controller and then these values are communicated to a recording device such as PC or embedded system through a suitable interface like RS485, Ethernet or USB interface to further process the overall distance estimations on the target.

Line lasers could be considered as collection of single point lasers working together for measuring the entire line segment on X-axis. Distance between each laser spot making the line is called the X-axis resolution and it defines the precision with which the entire line is being recorded by the sensor scanner and the number of data points being obtained at each line profile.

Figure 3.1 shows the principle of triangulation being used in one of the laser sensors available at Transportation lab UTA.

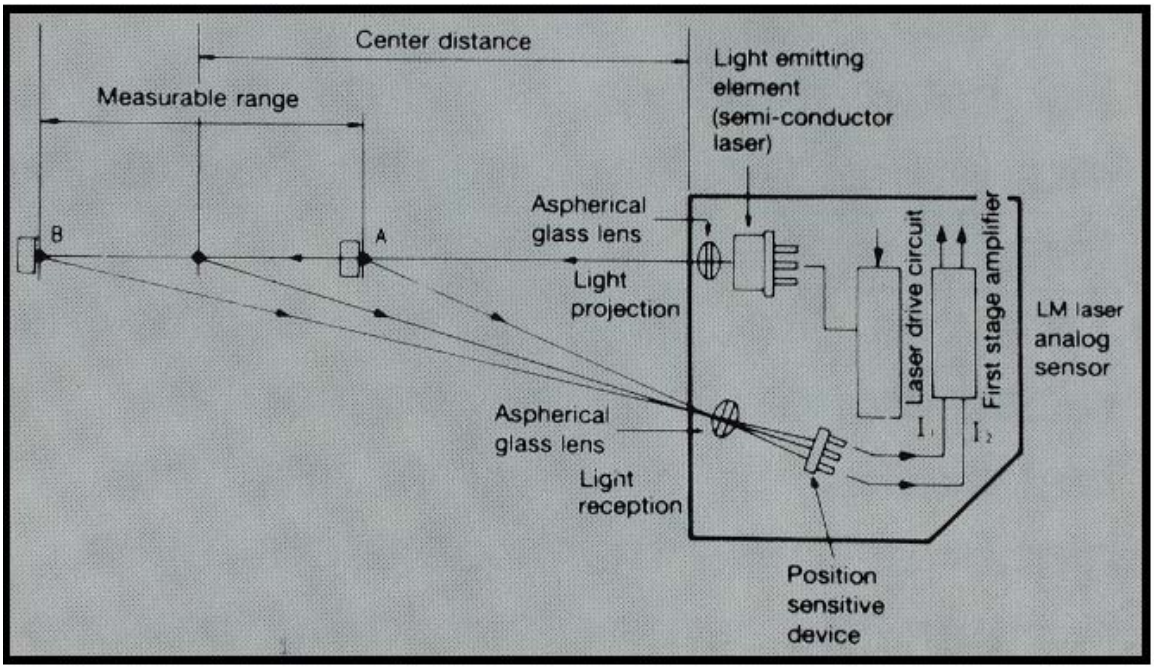


Figure 3.1 Laser triangulation technique for NAIS LM 200 Lase sensor [5]

After carefully examining various characteristics of the available laser sensors, a few most important selection criteria were identified and documented.

- Scan rate (also called laser refresh rate): This is the speed at which the laser sensor refreshes the readings from the target irrespective of the movement of target or the sensor. The synchronized Precision movement of object with the laser refresh rate would result into more accurate readings, a higher laser refresh rate is preferred for accurate measurements of a fast moving object.
- Resolution Z-axis: This defines the precision of measurement in the Z axis which estimates the difference between heights at two spots at the object. It is the most important characteristic of a laser sensor as an accurate estimation of object height at a particular point constitutes the measurement results.
- Clearance Distance: This defines the distance between laser head and the field of view at which the laser can start measurements. It is important to consider this characteristic

of the laser sensor as it provides the information which could be used to decide the distance between laser mount and the target, based on the system requirements.

- Measurement range X-axis (only for line laser): It is the length of horizontal laser beam. This specification could be used to determine the precision of measurement in X axis and the number of data points for each line profile.
- Measurement range Z-axis: The vertical range in millimeters for which the laser could successfully operate on the target. This would be helpful in deciding the maximum and the minimum dimensions of the target object supported by the laser sensor.
- Output interface: Communication interface for the output to the PC or embedded PC, ideal output communication interfaces are RS485 or Ethernet which are fast speed.
- Software support: Some Laser sensor manufacturers provide software support for image modelling and processing the laser data according to the needs of the customer. This is important to investigate as it gives an insight into equipment measurement capabilities and software development support for the laser based system.

  Figure 3.3 describes the various aspects of laser sensors in a diagrammatic way comparing the dimensions of a laser sensor along with its measurement range in Z and X axis.

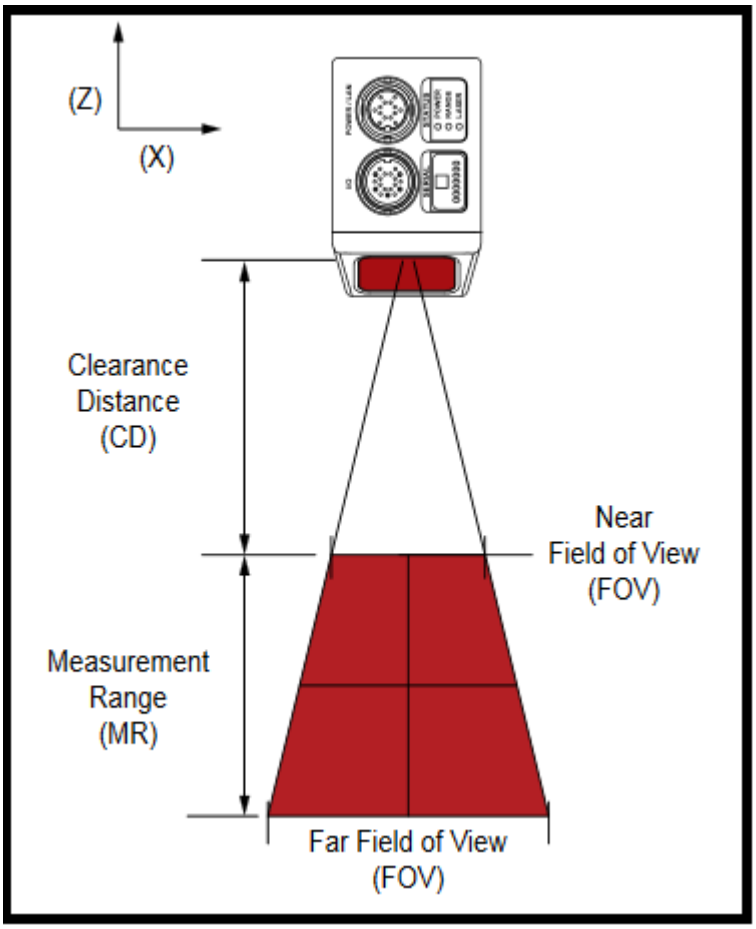


Figure 3.3 Measurement terminology for Line laser. [6]

Single point and line laser sensors both, operate on the same principles in terms of technology and data acquisition. Both can be considered for building a texture measurement system initially. However, both kinds of laser technologies have certain merits and de-merits which need assessment through experimentations. For example single point lasers have shown proven results and could be considered for highly precise measurements, but for this particular system, it would also require two linear stages for traversal in X and as well as Y axis for traversing over the target surface. On the other hand, line laser with a suitable X-measurement range could be easily used to read the line profile to determine entire surface feature using only

one linear stage but the level of precision and accuracy entirely depends on the manufacturer's specifications without giving any flexibility to modify the system to fit the requirement.
Some of the lasers initially considered for testing and experimentation purpose include single point laser sensors manufactured by Keyence, Panasonic and LMI, these are the sensors which were immediately available at the UTA Transportation lab and could be used to start with the basic analysis and to develop understanding of the accuracy level provided by different manufacturers, their precision range and to examine the quality standards.

- NAIS LM 200 Laser Sensor

  NAIS single point LM 200 laser manufactured by Matsuhita Corporation was considered first as it was easily available with specification which were good enough to start with and, had been used in one of the measurement projects at UTA Transportation lab. As per NAIS specs, it has high immunity towards reflectivity and color changes in the target surface which makes it a good candidate for initial testing. The below table shows the sensor specifications in detail.

Table 3-1 NAIS LM 200 specs

1	Scan rate and Resolution Z-axis	1) 3 µm resolution at 30Hz scan rate 2) 10 µm resolution at 300Hz scan rate 3) 30 µm resolution at 3KHz scan rate
2	Clearance Distance	30 mm
3	Measurement range Z-axis	6 mm
4	Output interface	Analog output +-3V
5	Software support	No software support

Figure 3.4 NAIS LM 200 Laser sensor and controller

- NAIS LM 300 Laser sensor and controller

This is an advanced version of LM 200 series of laser with even better quality precision measurement and greater scan rate. The sampling rate of this system is 20 KHz which could be increased up to 50 KHz. The laser controller offers more options such as measurement selection mode, Gain selection mode and calibration options. It has an additional RS 232 serial communication interface. Figure 3.5 shows the measuring system in detail based on LM 300 datasheet.

Table 3-2 NAIS LM 300 specs

	Resolution Z-axis	0.2 µm
1	Scan rate / response frequency	20KHz
2	Clearance Distance	30 mm
3	Measurement range Z-axis	6 mm
4	Output interface	RS 232
5	Software support	No software support

Figure 3.5 NAIS LM 300 laser sensor and controller

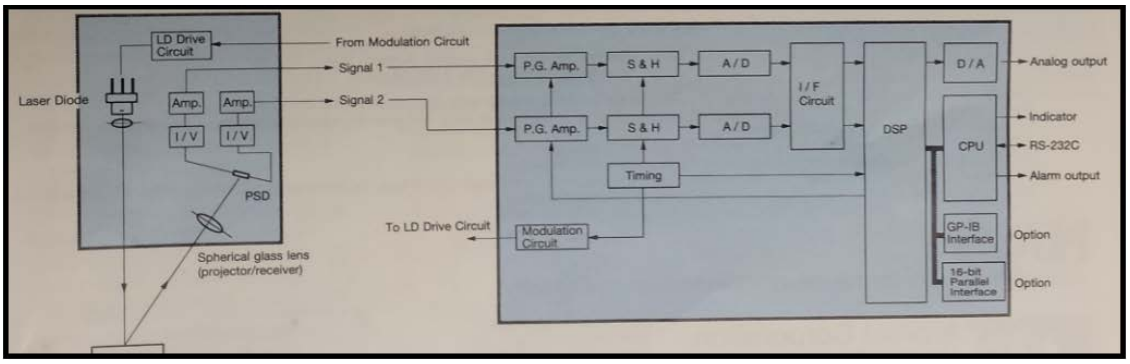


Figure 3.6 NAIS LM 300, inbuilt A/D conversion and measurement system. [20]

- Keyence LC-2400 series Laser Sensor

Keyence laser sensors are the most expensive systems available in market and are known for high quality measurement. It has maximum resolution up to 0.01 µm for the precise measurement, sampling frequency of 20 KHz which could be modified up to 50 KHz. The controller offers a wide range of laser intensity settings and gain settings. The measurement range is +-3 mm.

Table 3-3 Keyence LC 2450 specs

	Resolution Z-axis	0.01 µm
1	Scan rate / response frequency	20KHz
2	Clearance Distance	10 mm to 30 mm
3	Measurement range Z-axis	6 mm
4	Output interface	RS 232C baud rate: 75 to 19200 selectable
5	Software support	No software support

Figure 3.7 Keyence LC 2400 series Laser sensor controller

3.1.2 Data acquisition system and analog to digital conversion.

Laser sensors in consideration provide data readings in the form of analog voltages. Therefore data acquisition system is one of the most important sub system of the required measurement instrument as this component would be responsible for the result accuracy, deciding scan rate for the laser sensor and method of data transmission to the windows/Linux based embedded PC for further processing. DT 9816 data translation module is a low cost and fast sampling A/D converter chipset. The below key features were considered with respect to laser system compatibility and requirements making it a good candidate for an immediate adaptation into this test instrumentation for basic experimentation. Another reason for consideration of this A/D converter is its availability and good documentations from the manufacturers.

- USB based drivers for data acquisition.
- 6 analog channels input for simultaneous data acquisition
- 16 - bit data conversion for high accuracy
- Comparative low cost
- 50KHz sampling frequency per channel
- Availability of windows 10 drivers
- Signal range acceptable from -10V to +10V
- Gain adjustment from -5V to +5V

Figure 3.8 DT9816 module and OEM chipset. [8]

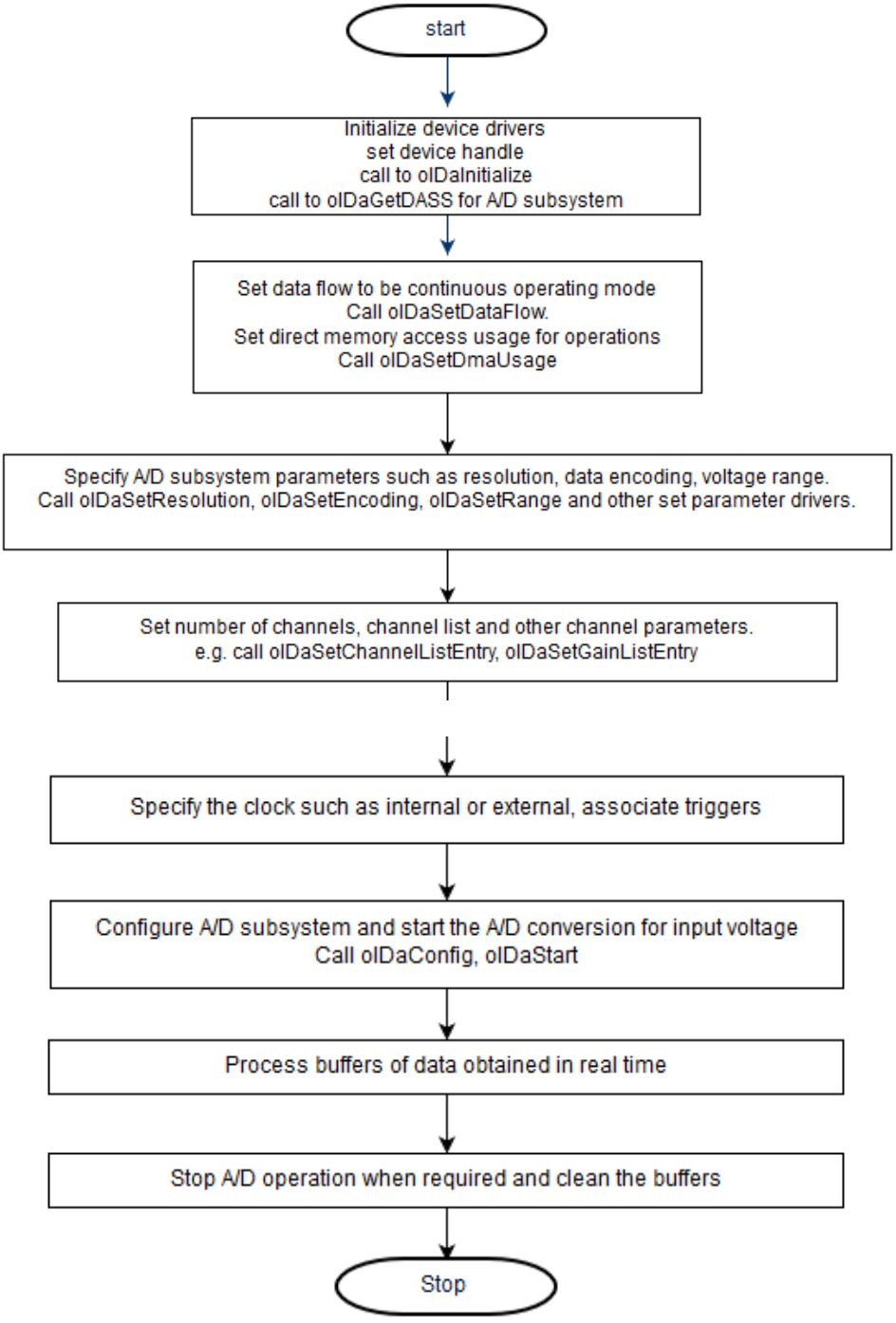


Figure 3.9 Data acquisition control flow using DT9816 module

Figure 3.9 shows the data acquisition flow using the DT9816 device drivers provided by the Data Translation® for 64-bit Microsoft Windows.

3.1.3 Linear Stage and Motion control System

A linear stage is a stepping motor or a DC motor which is accompanied with a motion controller which drives the motor upon receiving commands through the embedded PC using a device driver software. Currently, various technologies are being used to develop highly precise linear stages. Technologies like piezo Nano-positioning systems and magnetic levitation are provided by many vendors which can give precision up to a Nano meter and greatly surpass the precision of a conventional stepping motor. However, a precision and motion controlled linear stage capable of moving at one micrometer step size would provide enough precision for beginning with the tests on the laser based measurement system. A few important selection criteria for choosing the linear stage and controller are listed below.

- Minimal incremental motion: This is the maximum precision that a linear stage is capable of providing.
- Travel range: It specifies the maximum distance which could be covered by the linear stage in one direction. Size of target object must be considered before choosing the linear stage with best matching travel range.
- Load capacity: Motion of stage is mechanical and the precision would be effected by the weight of the object, therefore load capacity is an important feature.
- Repeatability: It is of two types, namely, unidirectional and bi-directional. It constitutes to the precision by which the motorized can handle repeated movements.
- Speed: Another very important feature. Laser refresh rate and measuring resolution should be synchronized with linear stage speed for optimal results without any redundancy.
- Computer interface for the controller: Ideal interfaces would be RS 232, Ethernet or USB. Embedded boards or FPGA boards have constrained resources to develop a

command interface with controller, hence availability of different command interfaces on the controller is important.

- Controller interface for the linear stage and its command compatibility with different kinds of linear stages from the same manufacturer for forward compatibility.
- Device driver software availability for 64-bit Windows, Linux, and ARM® based Linux systems.
- Time to accelerate and acquire a constant speed, time to decelerate and stop.
- Amount of vibrations on the linear stage due to motorized movement.

Since, linear stages and controller are expensive, there was a need to closely analyze the requirements for best possible result before making a purchase, and therefore a manually controlled linear stage was initially used as shown in figure 3.10 which was immediately available as well.

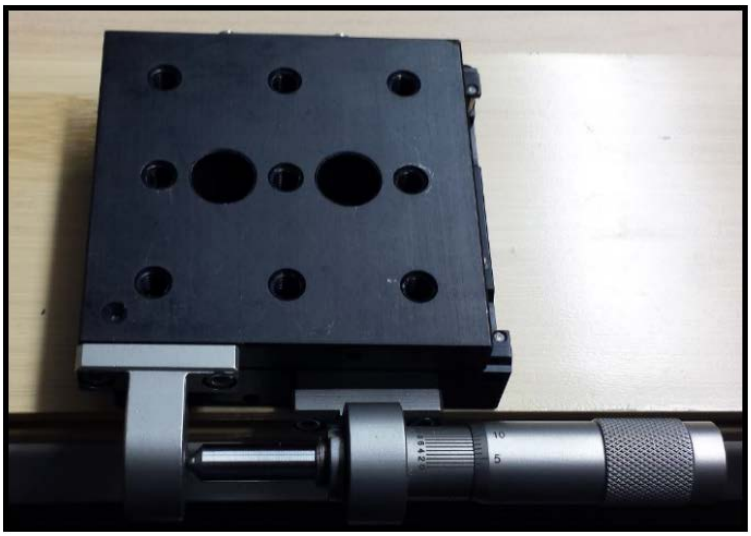


Figure 3.10 manually controlled linear stage, one micrometer step size

3.2 Software Requirements

A few software availability aspects and compatibility features were identified to be crucial in building the test equipment. For this initial test setup, 64-bit Microsoft® Windows operating system was best suitable for two reasons, the compatible DT9816 drivers were available from

the manufacturer only for Windows and a plenty of linear stage manufacturers also provided drivers for Windows. All required software were identified and enlisted for acquisition.

- Matlab® for image modelling and digital signal processing on the acquired data.
- Visual Studio 2012, for writing and modifying DT9816 or Motion controller drivers.
- A 64-bit Microsoft® Windows 7 operating system for device driver compatibility.
- Linux Ubuntu for evaluating the compatibility with DT9816 and linear stage drivers.

Using the laser technology and acquiring data at a high frequency would result into high volume of data which needs to be stored into files for further processing for texture characterization. Digital filtering was one of the software capabilities required to establish more meaningful results from the data. Matlab® provides an application programming interface for digital signal processing.

Device drivers for motion controller and Data Translation® module are only manufactured for Microsoft® Windows by the major manufacturers, therefore a suitable development environment was needed to modify and configure the drivers as per the system needs on Windows. One of the basic requirements in visibility was to synchronize the working of laser data acquisition, laser refresh rate and motion control system such that all the readings are obtained at constant speed without any motor vibration or environmental noise.

3.3 Structure of the complete system.

Figure 3.11 shows the block diagram of the complete laser based texture measurement system along with the major sub system components.

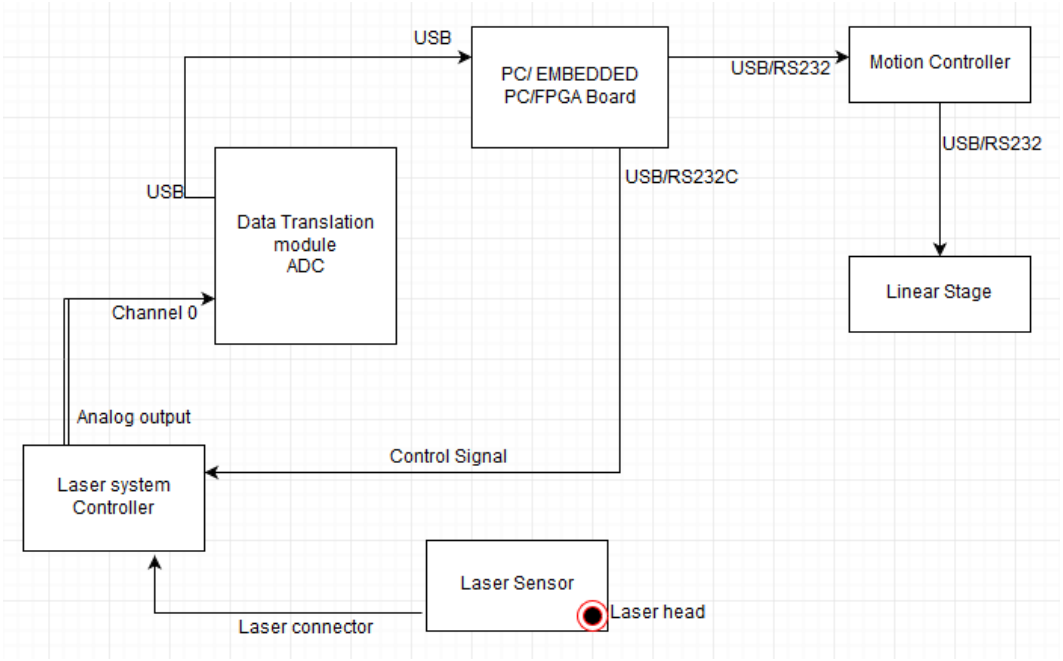


Figure 3.11 Block Diagram of Laser Measurement System and control flow

3.4 Experiments and Results

Based on specifications, a single point laser system passed the tests to provide standard measurement range which are adequate for the desired measurement equipment. The test setup was constructed using the NAIS LM 300 laser sensor due to its high resolution of up to 0.2 micrometers and a high laser refresh rate of 20 KHz, other sub systems included manually controlled linear stage and Data Translation board DT9816. Experiments were performed to investigate the use of single point lasers to measure micro-texture. The laser scans collected from the test setup were evaluated on the basis of following criteria keeping in mind the expected outcome of the system with respect to leveraging the advantages offered by laser sensors over the image processing techniques used for texture classification.

- To check how well the test equipment performs on different types of aggregate such as granite or limestone.
- To check how well the test equipment performs with color variations on the aggregates.

- To evaluate single point laser usability for micro-texture measurement and establish the level of details expected from a line laser based equipment for micro-texture measurement.
- To understand the equipment requirements with respect to maximum resolution required, compatibility of laser refresh rate with the sampling frequency of ADC board. For example, suppose the analog output of laser sensor ranges from -3V to +3V, the gain level of ADC device should be configured so that a more accurate voltage value gets digitized. The Data Translation® module has two selectable gain levels, +-5V and +-10V. In the above case, +-5V gain range would produce more accurate results as the conversion step size becomes shorter as compared to +-10V gain range and ADC could digitize +-3V input voltage range more accurately.
- To determine the type of readings that could be expected from each point along a line produced if a line laser sensor is used instead of single point laser. This could be done since a line laser uses same technology as single point lasers where multiple single point readings are collectively obtained across a line.
- To determine the statistical and predictive measures to summarize or classify an aggregate based on results obtained.

Figure 3.12 illustrates the complete laboratory setup for the test equipment including laser sensor, ADC module and manually controllable linear stage.

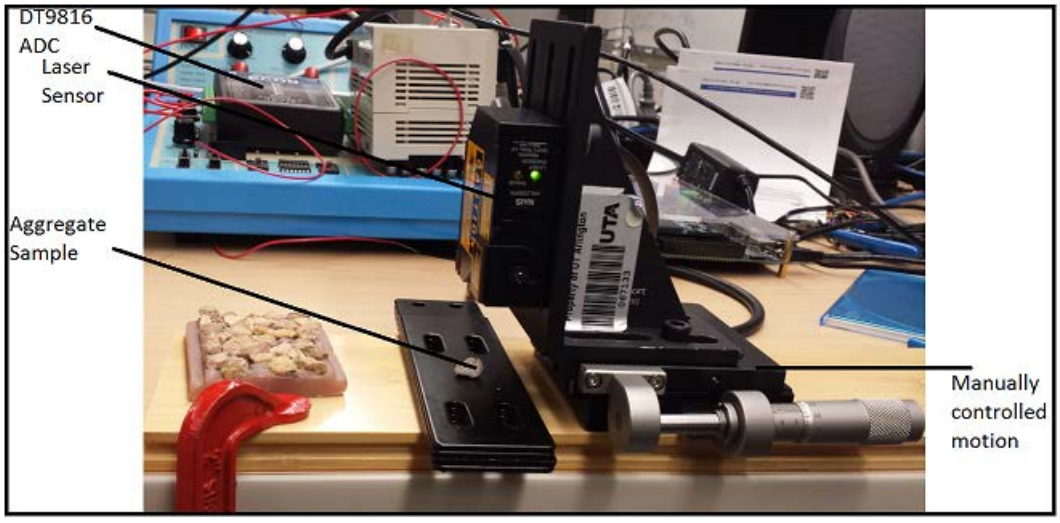


Figure 3.12 Laboratory setup for test equipment.

Figure 3.13 illustrates the plot created by data readings obtained by manually controlled motion with a step size of 100 micrometers. The next Figure 3.14 shows the data readings obtained by operating the linear stage at an approximately constant speed manually beneath the laser refreshing readings at a rate of 20KHz and ADC sampling frequency at 1KHz. Scans were made on limestone and granite samples.

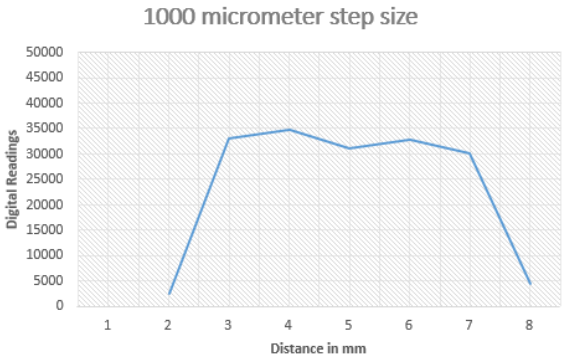


Figure 3.13 Plot showing readings using 1000 micrometer step size.

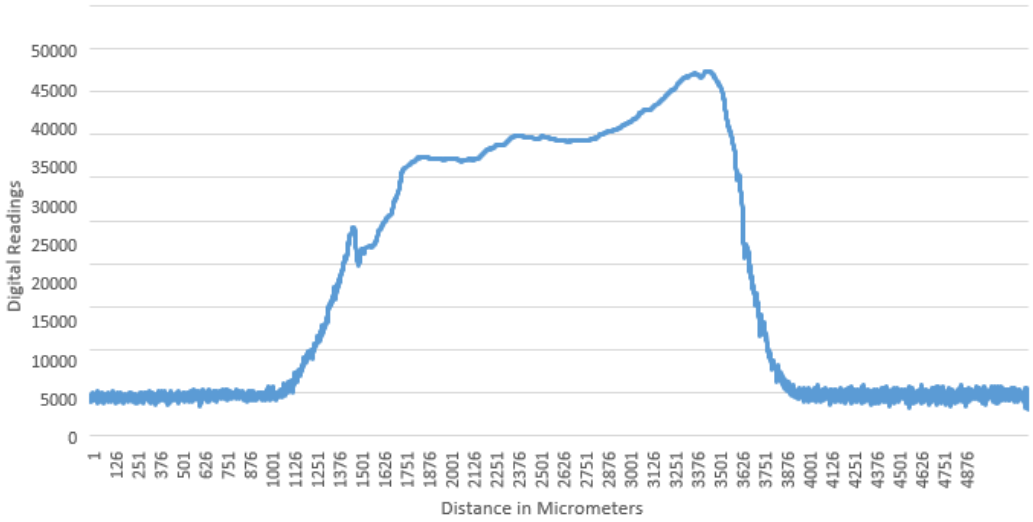


Figure 3.14 Manual motion at an approx. constant speed

Figure 3.15 Granite, limestone sample and a marked aggregate for analyzing the laser color immunity.

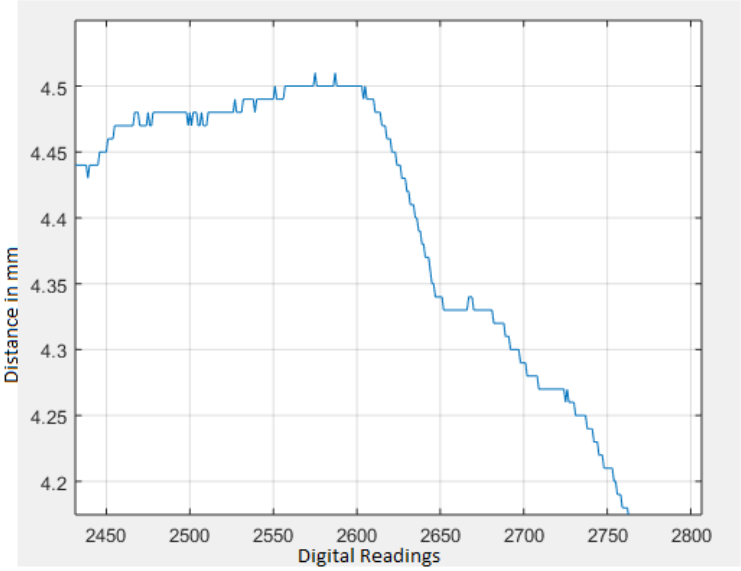


Figure 3.16 Fine grain detail level

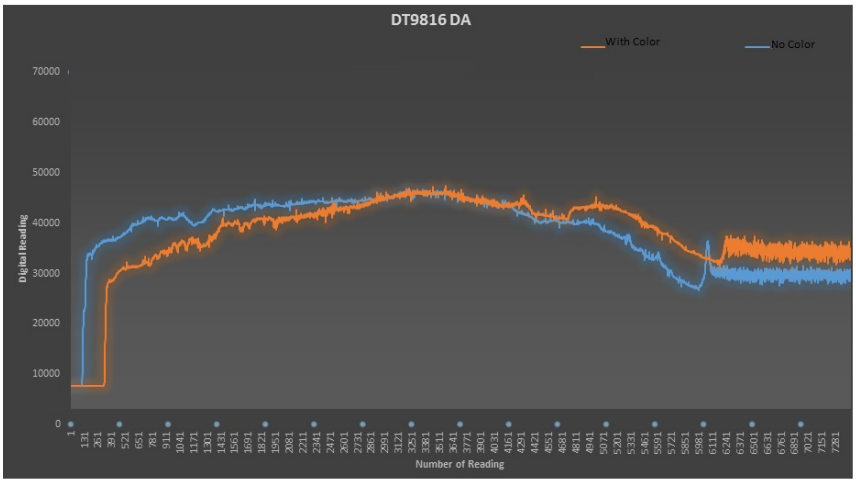


Figure 3.17 Plot comparison between marked and un-marked aggregates.

Statistical methods were investigated on the resulting data to characterize the micro-texture as opposed to the digital image processing techniques which uses wavelet analysis for the same. Digital filtering was used in different ways to address the following aspects of characterizing micro-texture features for a given aggregate sample.

- To filter the ambient noise due to light source or vibrations from the linear stage.
- Micro-texture measurements only needs to analyze the surface roughness index and therefore accurate readings along the surface +-0.5 mm height or depth are required, filtering out the true height of the aggregate was done using a high-pass filter. Also, statistical methods could be applied on the surface data; suppose standard deviation and sum of each texture line are used for characterizing the texture feature, a high pass IIR filter on the scan data with a cut-off frequency of approximately 0.5 mm results in an estimate of surface texture profile which is illustrated in figure 3.19.

Figure 3.18 illustrates a plot derived from the scan data of a granite sample and the corresponding filtered data plot using IIR filters at a cut-off frequency of 0.5 mm. The standard deviation and sum of absolute values for this granite aggregate was calculated to be 0.016 and 23.72 respectively.

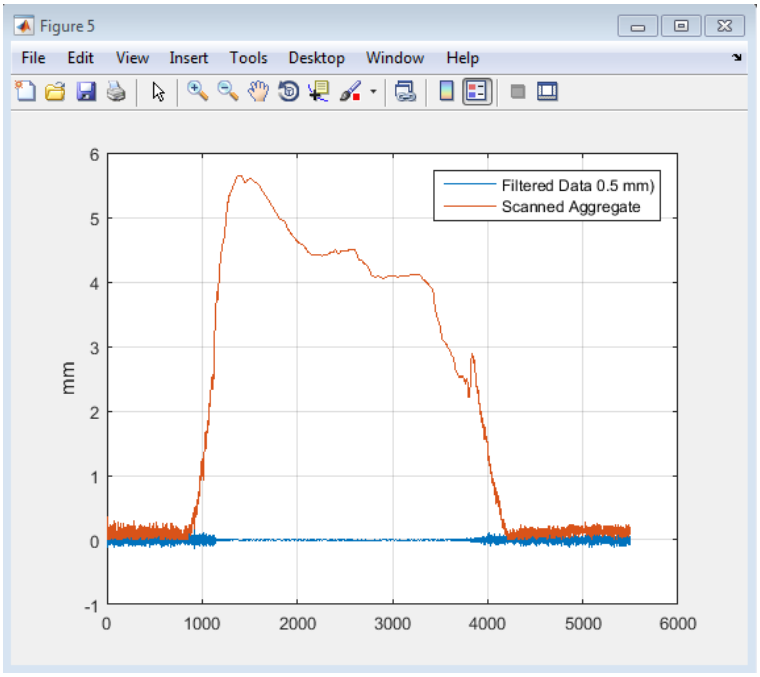


Figure 3.18 Data and IIR filter plot for granite sample.

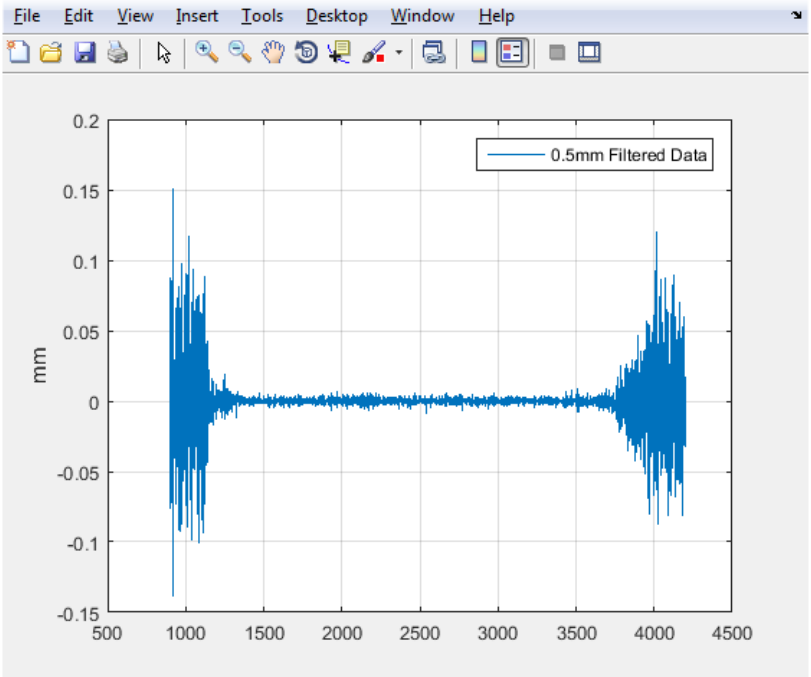


Figure 3.19 Surface estimation using high-pass IIR filter on scanned data.

Required Parameters for an ideal laser sensor, Analog to digital converter (ADC), linear stage and motion control system were thus determined and documented.

1) Total displacement capability required by the linear stage: 24 mm

2) Required time to perform the linear traversal from 0 to 24 mm: 3 seconds

3) So, the speed of motion controlled by linear stage controller is 8 mm/sec

4) Ideal laser resolution Z-axis was concluded to be 10 µm since resolution less than 10 µm was found to have negligible impact on the actual surface roughness and micro-texture.

Parameters for laser resolution, laser refresh rate and data acquisition sampling frequency were thus derived:

- If laser Z axis resolution is 10 µm, supported laser refresh rate should be 0.8 KHz or more and data acquisition system would capture 800 data points for 8 mm of traversal in 1 second, which means 100 samples per 1 mm traversal in 1/8 second time.

- Motion control system precision and speed requirements thus derived so far are as follows.

  If the required laser resolution is 10 µm, minimum laser refresh rate supported is 0.8 KHz, the required movement precision is 10 µm for the linear stage.

  So, 10 µm should be traversed every 0.00125 seconds.

Thus, properties of a linear stage required for the system having a laser sensor of 10 µm resolution supporting laser refresh rate of 0.8 KHz are illustrated in table 3-4.

Table 3-4 Desired properties of the motorized linear stage

Minimum Incremental Motion/ step size	10 µm or less
Range of traversal	0 mm to 24 mm
Minimum speed/ controllable linear stage speed	8mm/second or more
On axis accuracy	-2 to +2 µm

Based on the test equipment results and the requirement analysis, single point lasers proved to be adequate for micro-texture measurement, but more advantages were gathered for line laser sensors comparatively. For e.g., deploying a single point laser to our use would require additional task of creating a two dimensional controlled motion system which should be capable of taking precise steps in both X and Y axis. In addition to the extra expenditure on buying two linear stages and two axis motion controller, it would also need more time to traverse the entire surface of an aggregate scanning each single point on it, which is a great drawback. This would

also add an extra overhead on synchronizing, processing and controlling the system. Therefore, the idea of using a single point laser was discarded.

3.5 The Proposed System

Once the adequate system parameters were decided for the micro-texture measuring instrument, the components were proposed upon thorough investigation of the latest tools and cutting edge laser technology available in the market at present. Major equipment manufacturing companies were approached for providing the test data on an aggregate sample for further analysis. Acuity®, LMI® and Keyence® are the three companies which have good experience in manufacturing diverse and accurate laser sensor equipment. Sensor data gathered from these manufacturers was tested against the quality and accuracy obtained while testing with the single point laser system previously developed. Keyence laser sensor LJ V7080 was finally proposed as its features surpassed the system needs and offered extra advantages over the other manufacturers.

- Fastest Laser refresh rate for 64,000 profiles/second for more accurate results.
- The Z axis and Y axis resolution offered by this sensor was more precise than all other major competitors.
- Availability of Software tools for quality evaluation, data modelling and categorizing the scans.
- Availability of high speed interface such as Ethernet/USB for data transfer between the laser controller and the embedded PC.

Table 3-5 Keyence LJ - V7080

Scan Rate	64000 Hz
Data Points / Profile	800(claimed but not mentioned in the manual)
Resolution Z(micro meters)	0.5
Resolution X (micro meter)(Profile Data Interval)	10
Clearance Distance	80
Measurement Range - X Axis (mm)	32

Measurement Range - Z Axis (mm)	23
Communication Interface	Ethernet, USB, RS 232
Measurement Output	RS-232C (baud up to 115200 bits/sec)
Scanning Software	GUI based Software for 3D and 2D measurements and profiling

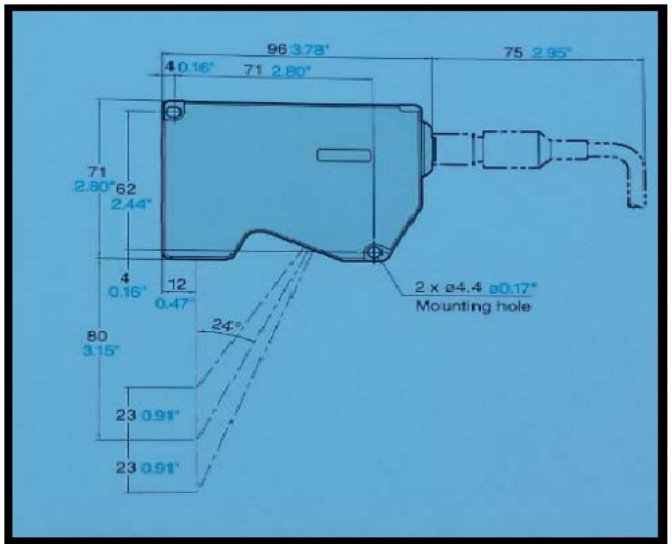


Figure 3.20 Keyence LJ - V7080 sensor head dimensions and measurement range. [19]

Aerotech® and Newport® on the other hand, are known to have experience in developing fast and highly precise motorized linear stages. Motion controller and linear stage manufactured by Newport® was finally proposed due to its compatible Windows drivers and a good match to the desired equipment requirements stated in table 3-4.

Figure 3.21 Newport SMC100 controller and UTS50PP linear stage

The proposed laser sensor and motion control sub-systems could be deployed to create a state-of-the-art shape, angularity and texture measurement system. In addition to these hardware components, a software solution would be required which could process the acquired data for accurate texture categorization, three dimensional image modelling and texture feature extraction.

Chapter 4

INTRODUCTION TO ALTERA DE1 SOC FPGA BOARD

In order to develop a high speed data acquisition system for measuring accurate micro-texture from aggregate surface, an embedded board capable of high performance and real time computing was a requirement. DE1 SOC is a system on chip embedded board designed to leverage the flexibility of hardware configuration on a Cyclone 5 FPGA along with the benefits of high speed real-time processing on a dual core ARM Cortex A9® processor (hard processor system). The device has a 12 bit on-board ADC module capable of sampling at the rate of 500 Ksps.

This chapter provides an introduction to DE1 SOC hardware components, software development tools, operating system platforms and software/hardware design process and strategies on DE1 SOC board.

The major system components of DE1 SOC board are listed below. Figure 4.1 shows its block diagram and system components. The chipset is composed of two parts, namely FPGA and HPS. The FPGA part has 85K logic elements supporting the design and re-configurability of most of the embedded peripherals on FPGA. To name a few for example, direct memory access controller, PLLs, on-chip memory, SPI interface and UART interface. Most of the required system components are provided by Altera in the form of intellectual property with a basic user license for a limited time without any charge.

FPGA components

- Cyclone V SoC
- 85K Programmable Logic Elements
- 4,450 Kbits embedded memory

Hard Processor system

- Dual-core ARM Cortex-A9 (HPS)

Memory device

- 64MB SDRAM on FPGA
- 1GB DDR3 SDRAM on HPS
- Micro SD Card Socket on HPS

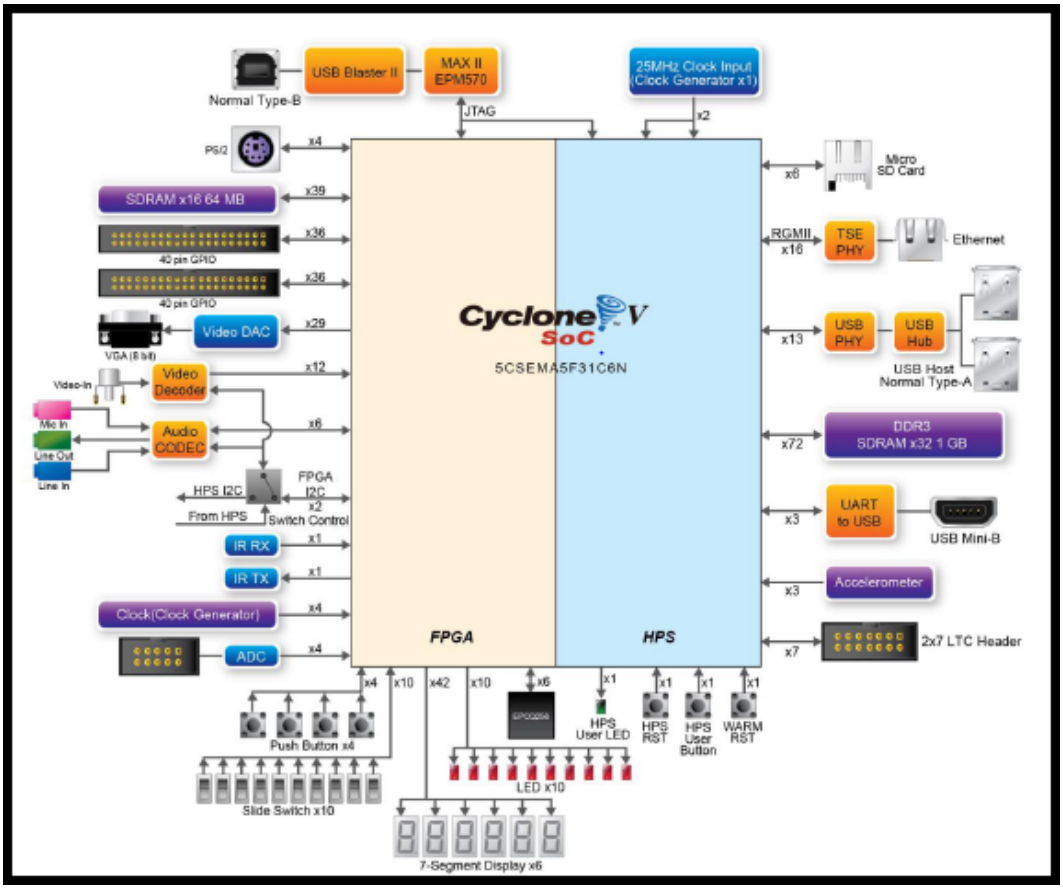


Figure 4.1 BLOCK Diagram of DE1 SOC Board [14]

Communication

- Two Port USB 2.0 Host
- USB to UART
- 10/100/1000 Ethernet

ADC

- sample rate: 500 KSPS

- Channel number: 8
- Resolution: 12 bits
- Analog input range : 0 ~ 4.096 V

GPIO

- Huge number of GPIO options are available in the form of switches, LEDs, and seven segment displays.

4.1 System Development Tools and Strategy

Device specific application hardware can be developed over the FPGA board and integrated on FPGA logic on the SOC board. Altera® provides tools and software development environment for developing the hardware and software separately. The software can be developed even before the hardware design is ready. Once the hardware is ready and configured over the FPGA fabric, the software can be easily tested for timing and performance constraints.

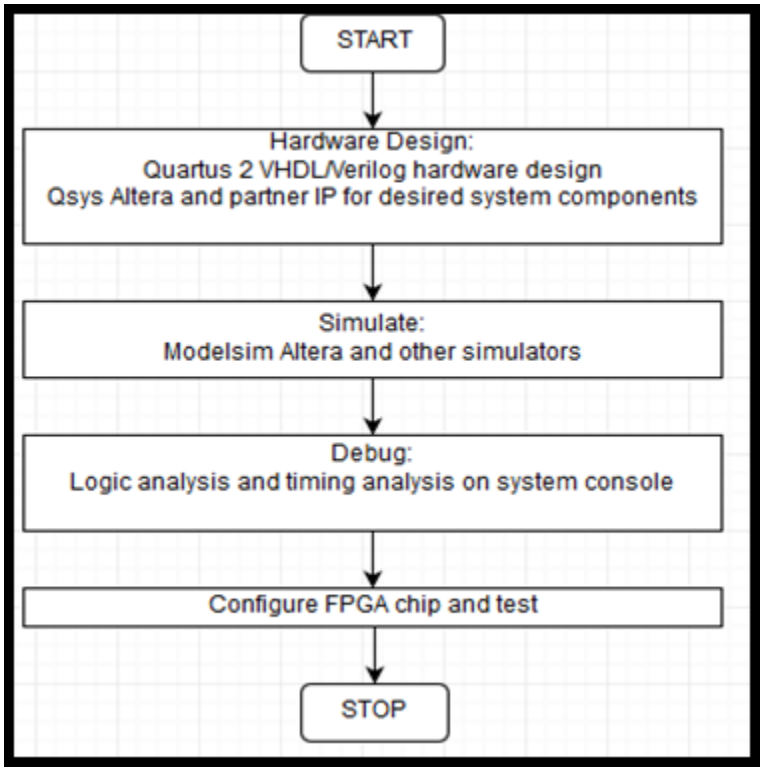


Figure 4.2 Hardware design flow diagram.

Following are the key points considered before beginning the software and hardware development for the surface measurement instrumentation on system on chip FPGA:

- FPGA hardware design for optimal performance acceleration.
- HPS use for efficient real-time computing.
- Data acquisition hardware and software using on-chip linear device ADC module.
- Ethernet connectivity for data communication between FPGA board and a Windows/Linux client.

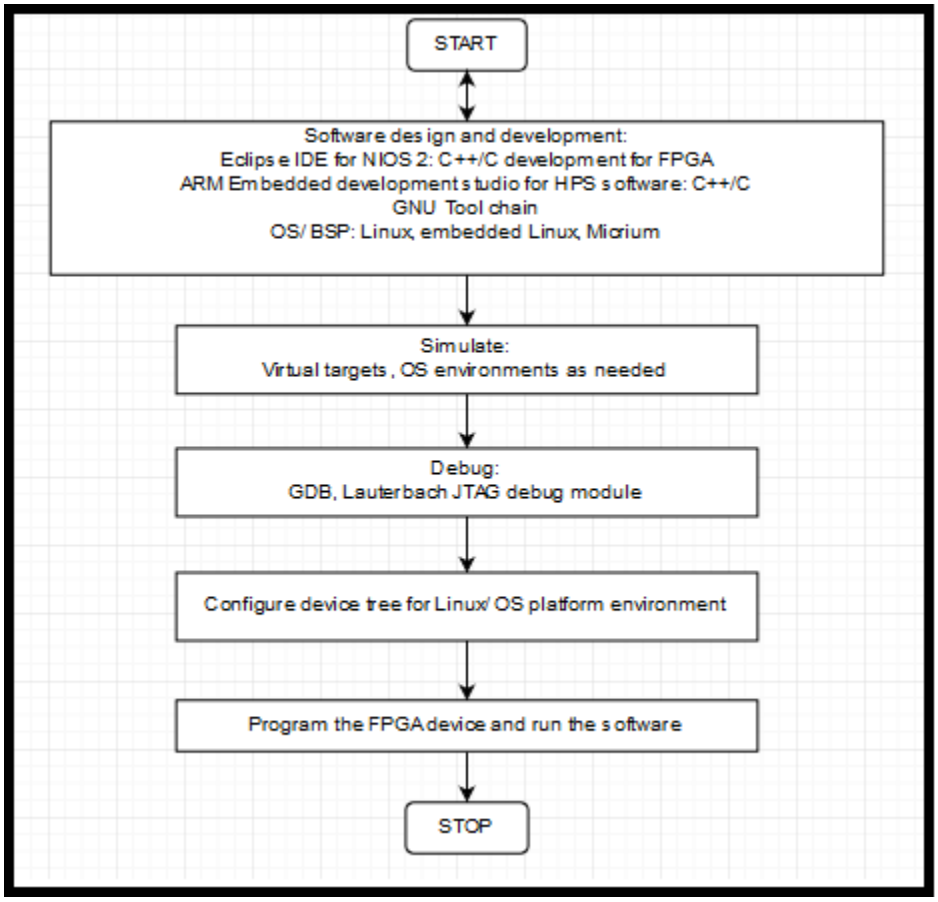


Figure 4.3 Software design flow diagram for DE1 SOC FPGA board

The dual core ARM® Cortex A9 processor sub system could be deployed for time critical operations involving real-time processing since these processors are 800 MHz and could be

used for operations such as low latency interrupts, high speed Ethernet throughput and real-time responses exploiting ARM® asymmetric multiprocessing technique. The two cores can be used separately to perform dedicated operations on each core, for example one core could handle the operating system and the other could be used for a real-time application.

NIOS 2 processors are Altera® intellectual property and could be configured on FPGA Cyclone 5. The speed of NIOS processors is constrained by the FPGA fabric performance being used for the hardware design, In case of Cyclone 5 FPGA, the clock frequency of NIOS processor ranges from 100 MHz to 150MHz. The NIOS processors have low interrupt latency, a number of NIOS processors could be deployed dedicatedly for executing a specific time critical job respectively to obtain a high performing system in real time using multi-core execution on a thread safe software architecture.

4.2 Operating Systems for HPS and NIOS 2 processors

Several operating system platforms could be deployed on the HPS subsystem based on the system processing requirements and task scheduling needs. Few most widely used real time operating system are VxWorks, Embedded Linux and MicroC/OS-II. Embedded Linux was considered for this application since it is available as an open source and the kernel could be modified if required in future. The Ethernet port is a part of HPS subsystem and needs to be accessed by the application software to communicate with other devices over the TCP/IP connection. Ethernet drivers are part of the embedded Linux provided by Altera development kit.

MicroC/OS-II operating system BSP could be built using Eclipse IDE for NIOS 2 processors, Altera provides support for developing MicroC/OS-II application on NIOS 2 processors. Since the ADC module is connected to the FPGA fabric, the high speed data acquisition software would require MicroC/OS-II support to be executed on a NIOS processor.

4.3 System Interconnect

To communicate data and feedback control to and fro between the HPS and FPGA fabric, SOC board contains the following HPS-FPGA AXI bridges:

- HPS to FPGA low weight AXI bridge(low speed 32 bit)
- FPGA to HPS bridge(high speed 32/64/128 bits)
- HPS to FPGA bridge((high speed 32/64/128 bits)

These high speed interconnect provide up to 100 GB per second processor to FPGA interconnect for data communication. The figure 4.4 demonstrates the FPGA fabric – HPS subsystem interconnect. FPGA-HPS interconnect is most important system component as it is the medium for the communication between two distinct parts of the system on chip without which it would be impossible to fully leverage the system capabilities.

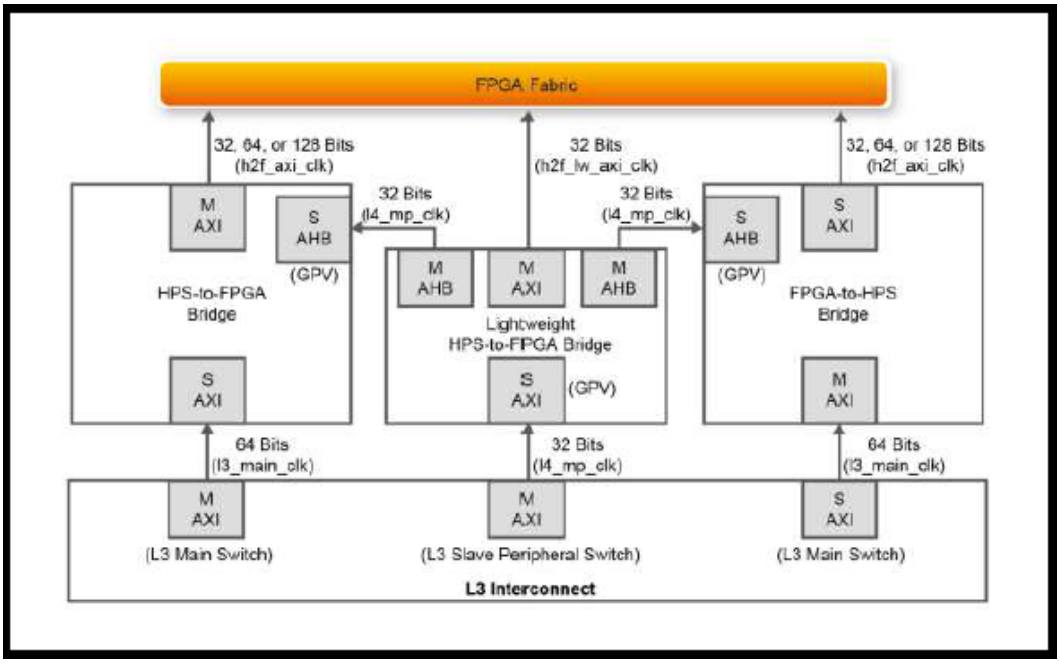


Figure 4.4 AXI Bridge interconnect for FPGA- HPS on System on Chip [15]

4.4 Linux Device Tree Blob

The Linux device tree blob could be generated using an open source tool. It is a data structure for the Linux operating system which tells the operating system about the system peripherals at

the system start up. It is important for embedded Linux to gather the description of the underlying hardware at the start-up, as in case of FPGA design implementations, the Linux device must be able to support multiple variations of the hardware as and when the FPGA is being re-configured.

A device tree typically contains the following information in the form of a tree data structure:

- Number and type of hard and soft-core CPUs in the system design.
- GPIO information.
- Interconnect busses and bridges on the system on chip with the respective base addresses.
- Peripheral connection information
- Device driver configuration information such as Ethernet MAC address
- Interrupt controller information

Device tree structure entry example for LED pin input output:

```
led_pio: gpio@0x100010040 {
                Compatible = "ALTR,pio-15.1", "ALTR,pio-1.0",
"altr,pio-1.0";
                reg = < 0x0000002 0x0001050 0x0000060 >;
                width = < 8 >;
                resetvalue = < 1 >;
                gpio-controller;
            };
        };
```

Device tree structure entry for HPS ARM® Cortex A9 processor core:

```
Cpus {
        hps_arm_a9: cpu@0x1 {
            device_type = "cpu";
            Compatible = "arm, cortex-a9-1.0", "arm, cortex-a9";
            reg = < 0x0000001 >;
            next-level-cache = < &hps_0_L2 >;
        };
```

For frequent changes in FPGA hardware or new component addition, the Linux kernel would require a recompilation. Device trees reduce the need to re-compile the kernel by feeding the hardware configuration to the OS kernel.

4.5 LTC2308 Analog to Digital Converter

The micro texture measurement application requires a high speed, multi-channel and high accuracy Analog to Digital converter (ADC). LTC2308 ADC module is provided in the Altera DE1 SOC board, connected to the FPGA fabric. It is 12-bit ADC, having conversion throughput rate at a maximum up to 500 Kilo samples per second which exceeds the requirements for the current application. The data input ranges from 0V to 4.96V. The 8 channels could be used for sampling data from multiple source simultaneously. It has a SPI compatible interface, the internal ADC clock allows the external data out clock to operate on any frequency up to 40 MHz. ADC module with Altera® SPI IP interface could be utilized to perform fast analog to Digital conversion on FPGA fabric.

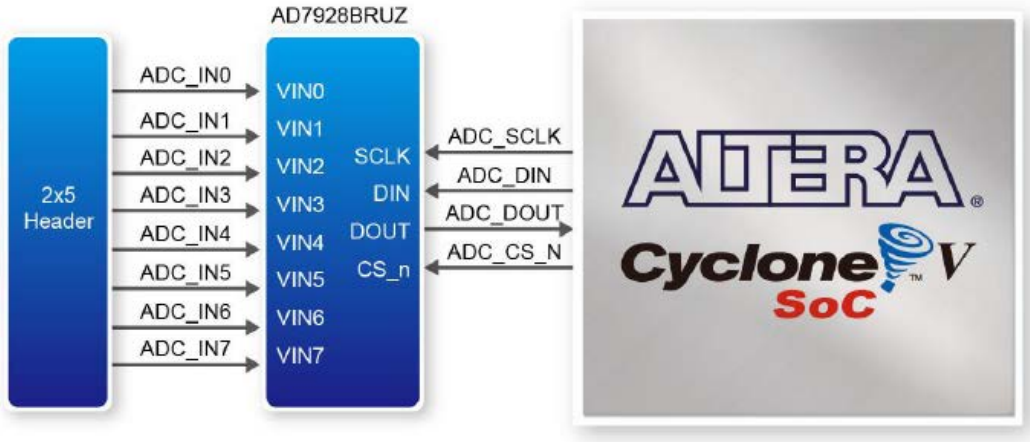


Figure 4.5 ADC LTE2308 and FPGA interface with connectivity pins. [15]

Chapter 5

HARDWARE AND SOFTWARE DESIGN ON FPGA SOC

FPGA based applications require design of the hardware architecture as well as the firmware software on top of the hardware configured on FPGA fabric. Therefore, this chapter begins with the details about developing a FPGA system architecture to evaluate how well the FPGA SoC could be utilized for the real time data acquisition and processing requirements in terms of power, efficiency and accuracy. Approach to develop system hardware and software to maximize the utilization of the system on chip resources would be discussed in detail. Software and hardware is designed to meet the current and future requirements of the micro-texture measurement instrumentation. Benefits of using the FPGA SoC against other embedded solutions have been discussed in Chapter 1 and 2, and the same aspects have been focused on, to evaluate the usability of this system on chip board for the application specific purpose.

5.1 Hardware Design and Implementation

5.1.1 Hardware design approach

The FPGA board has the option to start with the hardware development. The basic approach is to design a hardware circuit and configure it on to the FPGA fabric. However, for a complex design like real time ADC this approach is not very useful. The hardware needs to be a software programmable system which could be controlled and configured through a high level language such as C++.

NIOS 2 soft core processors could be configured on FPGA fabric and MicroC/OS-II operating system could be used to program the desired processes. A basic system to perform high speed data acquisition is described in figure 4.1 with the system interconnect structure on the FPGA board.

5.1.2 Basic FPGA component requirements – ADC

For interfacing a laser sensor with FPGA board, below FPGA hardware design components were identified.

- Input clock: An input clock is used to provide a single clock rate to the entire system. The input clock frequencies could be changed at the time of QSYS system generation
- System ID module: A system ID module is required to correctly identify a system device and check if the executable program was targeted for the current hardware image on the FPGA. If there is a mismatch, the FPGA device needs to be re-configured in order to execute the program.
- General purpose input output (GPIO): This hardware component is required in order to start and stop the data acquisition manually from a hardware switch. A hardware interrupt would be used from the GPIO switch to start/stop the ADC module.
- ADC module: The Linear technologies ADC model LTC2308 needs to be interfaced with SPI core to fetch the acquired data into the on-chip memory. Altera provides the LTC2308 module in the form of an intellectual property which could be used for a limited time. The ADC module needs to be integrated with all other components using QSYS system integration tool.
- Phase lock loop (PLL): A PLL is used to synchronize the clock frequencies of on- chip memory-SDRAM, GPIO and the processor with the output clock frequency of ADC converter module which allows the external data out clock to operate on frequencies up to 40 MHz.
- JTAG UART: A JTAG UART module is useful for executable program debugging and interfacing with the processor. The Eclipse IDE for NIOS 2 software development has a JTAG connectivity to the IDE console to fetch the program results on the system console.

- NIOS 2 Processor: A NIOS 2 processor is powerful enough to operate the ADC module to its full capability. The processor can be configured to be a slow or a fast processor at the time of system development in QSYS tool.

  Figure 5.1 illustrates the block diagram of the basic Analog to digital conversion system for real time data acquisition on FPGA board.

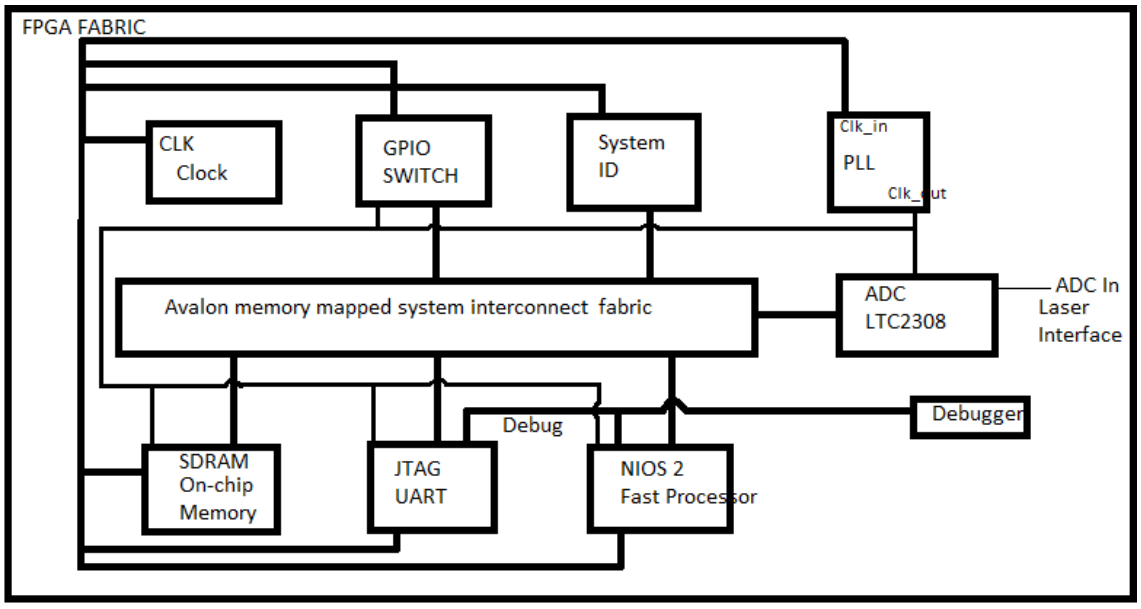


Figure 5.1 Block diagram of ADC data acquisition on FPGA fabric

Figure 5.2 is a snapshot of QSYS system generation tool. QSYS tool is provided by Altera® to integrate the system components together and define the components connectivity with each other. By using QSYS tool, Altera® and external hardware components could be synthesized into Verilog design files automatically. Once the system is generated, the top level Verilog design file was needed to be programmed to integrate all the system components used before the FPGA image could be compiled and generated.

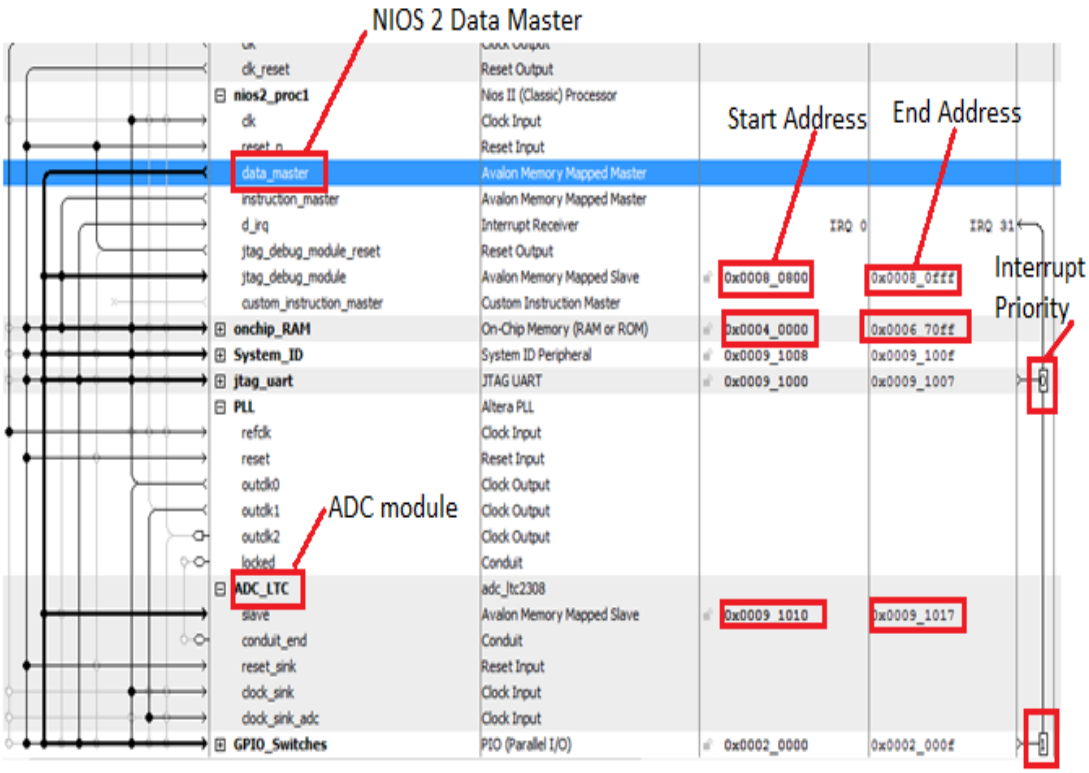


Figure 5.2 QSYS snapshot for FPGA fabric interconnect.

In figure 5.2, the data master is Avalon memory mapped master which is a QSYS system interface for providing connectivity to multiple slave components. A master typically controls a number of memory mapped slaves by using their base address for read/write operations. The slave in the above design include memory, UART and ADC module. The memory start address have been marked in figure 5.2, these base addresses would be used while programming the device for data acquisition. The hardware interrupts could be prioritized in the QSYS tool itself by providing the priority number to each interrupt enabled in QSYS system before the design Verilog code is generated. Figure 5.3 presents the top level design function for LTC 2308 ADC module along with the tHCONVST parameter which could be set to achieve high sampling rate from this ADC converter.

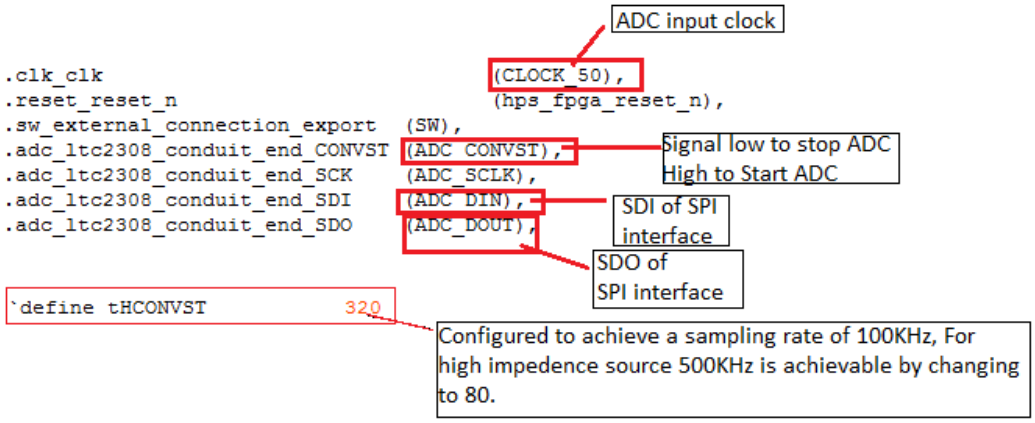


Figure 5.3 Design Verilog entry for ADC module.

Figure 5.5 describes the schematic diagram illustrating the individual wiring connections between the FPGA components. The Switch external connection and ADC conduit end connections are exported. Clk_in and Clk_reset connections need to be connected to an external clock source through the Verilog design code. Pin assignments need to done to attach a correct hardware PIN resource to the design. For example, ADC, HPS reset, FPGA reset, and clock source need to be correctly assigned in order to achieve the desired functionality from the hardware resource. Figure 5.4 shows a small example of PIN assignment scheme.

ADC_CONVST	Bidir	PIN_AJ4
ADC_DIN	Output	PIN_AK4
ADC_DOUT	Input	PIN_AK3
ADC_SCLK	Output	PIN_AK2
LEDR[7]	Output	PIN_W20
LEDR[6]	Output	PIN_Y19

Figure 5.4 Example of PIN assignment on FPGA board

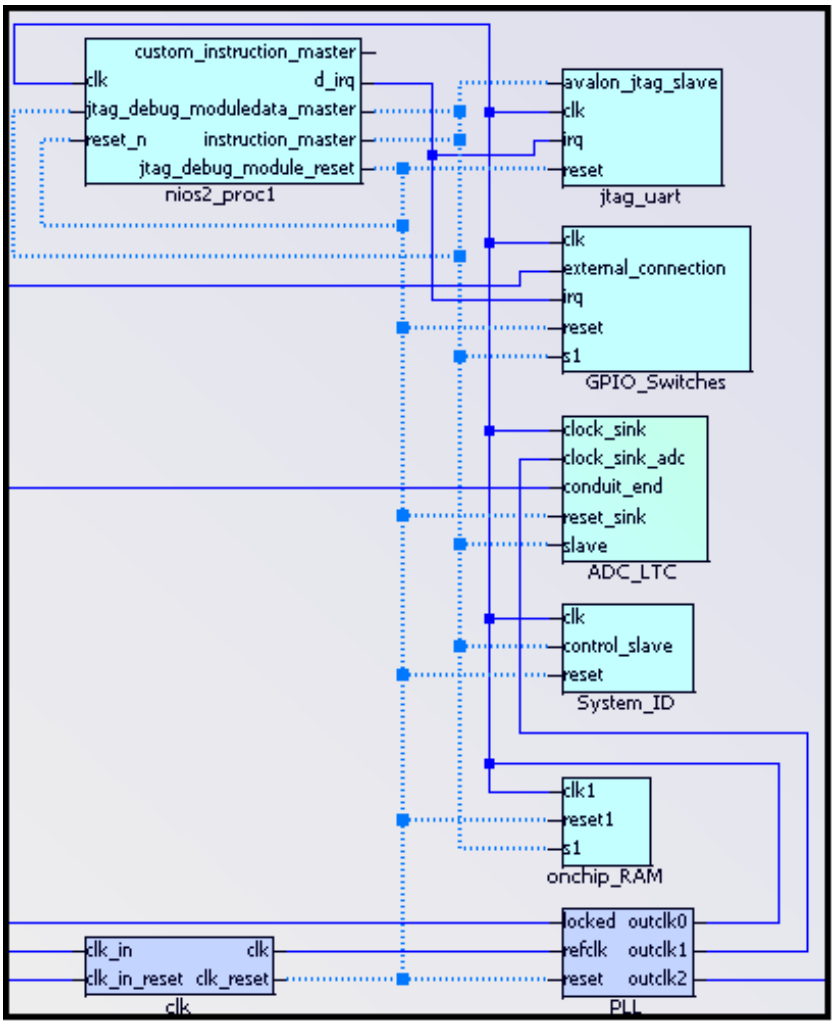


Figure 5.5 FPGA configuration schematic for basic ADC functionality

5.2 Advanced hardware requirements.

Below hardware requirements were derived for a real time micro-texture measurement Instrument.

- Data processing capability at a high sampling rate. The latest laser considered for this equipment has a refresh rate of up to 64,000 KHz. This requirement was derived from the specifications of the new laser controller.
- Real time digital filtering, using different filtering techniques such as FIR or IIR filters to reduce the noise from the data acquired from the laser system.

- Miscellaneous processing requirements such as mathematical calculations for micro-mean profile depth (MPD) or algorithms for improving the accuracy of the results such as identification of higher texture areas on the surface by linear regression analysis.
- Need for a multi thread environment to parallel process the data acquired, for example Posix threads over Linux operating system
- Getting the acquired data out of the FPGA physical storage. FPGA SOC board has a limited physical memory, the data needs to be stored in a separate storage server such as cloud storage. The data also needs to be processed by several other tools such as MATLAB in windows environment, this requires data to be available out of the FPGA device.
- Control operations such as switches to start and stop the ADC operations on the hardware and use of LED for indication of data acquisition states.

5.3 A Multicore Approach to Data Acquisition and Processing.

The processing needs of the application are more than what a single 100MHz – 150MHz processor could handle in real time. The FPGA SoC board has an on board dual core 800 MHz ARM® Cortex A9, which could be deployed by implementing a mechanism for inter processor communication between ARM HPS and NIOS 2 processors. Multi-softcore processors could be configured on the FPGA fabric to handle single dedicated operations by each processor. The number of multi – softcore processors supported by an FPGA depends on the capacity of FPGA fabric in use. Cyclone 5 FPGA could easily be used to build a dual core system utilizing only approx. 40% of the total logic elements on it.

5.3.1 Multicore architecture with inter-processor communication.

The Altera® way of performing inter-processor communication is a Mailbox core IP. The hardware design of Mailbox is packaged by Altera® and could be synthesized into a QSYS system design file. The figure 5.6 illustrates a multi-core design architecture using the dual core HPS and dual cores of NIOS processors. Mailbox core is discussed in detail later in this

chapter. The FPGA hardware design utilizes the Mailbox core for communication of data between ARM and NIOS processors using the AXI bridges.

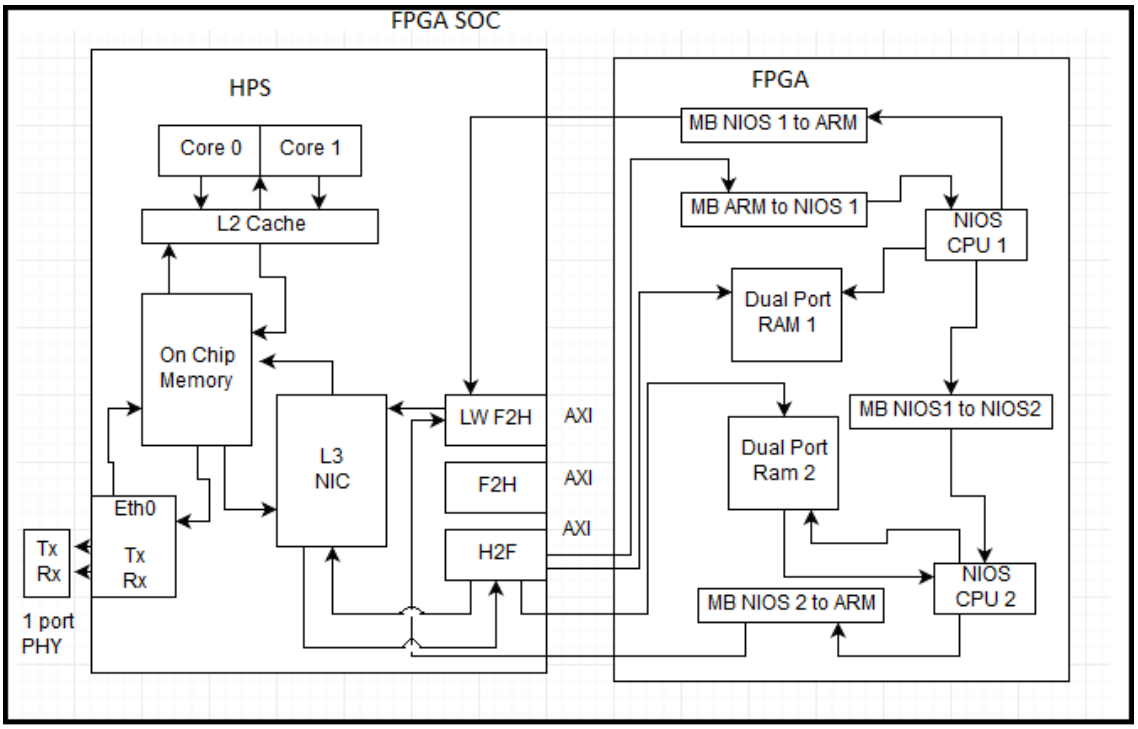


Figure 5.6 Multi-core hardware design and Mailbox inter-processor communication.

Dedicated operations to be performed by the individual subsystems are illustrated in the figure 5.7. It presents a complete SoC architecture model for data acquisition, processing and Ethernet communication to the remote client.

- NIOS CPU 1 is attached to ADC module, would be responsible for acquiring the data and communicating the data to the NIOS CPU 2 and the HPS through the dedicated mailbox cores. The software aspects of data communication would be discussed in the next chapter.
- NIOS CPU 2 would be dedicatedly used for miscellaneous data processing needs as discussed in section 5.2.

- Dual core HPS is connected to the Ethernet PHY and is a high speed applications processor which would be used for multi thread processing, high throughput Ethernet communication and digital filtering as required.

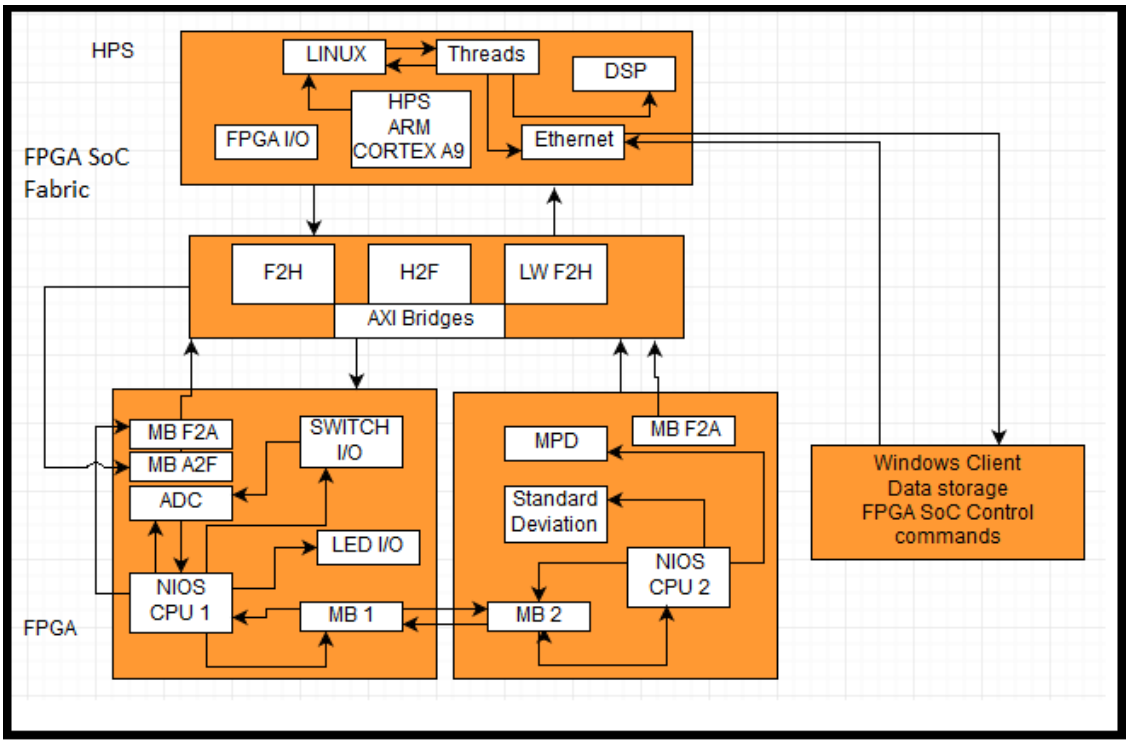


Figure 5.7 Complete Soc architecture for data acquisition, processing and Ethernet communication

The SoC fabric is programmed in to three sub system. Each subsystem is assigned a task to perform in real time.

Figure 5.8 displays all the QSYS system components used in creating the architecture design illustrated in figure 5.6.

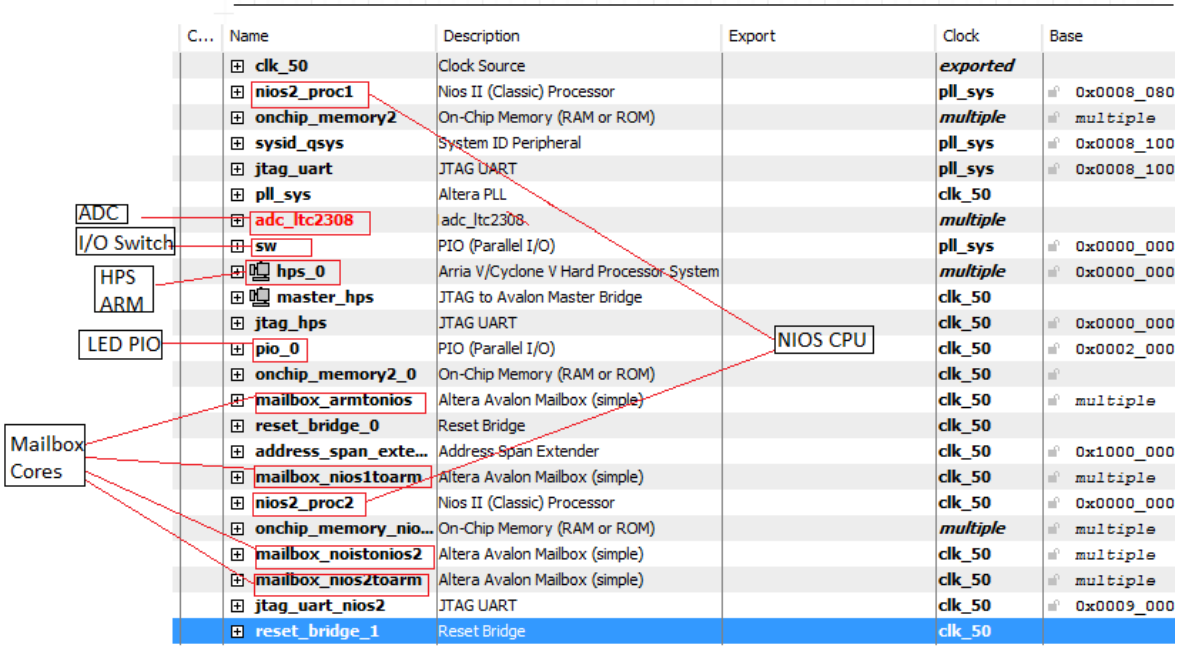


Figure 5.8 QSYS System Components for the designed hardware architecture.

Complete Schematic of this design is a large file, therefore HPS and NIOS CPU 1 sub system schematic diagram is illustrated in the figure 5.9. Only major components are shown in figure 5.9, individual connections seen in this figure were established between system components at the time of designing the QSYS system as illustrated by figure 5.8.

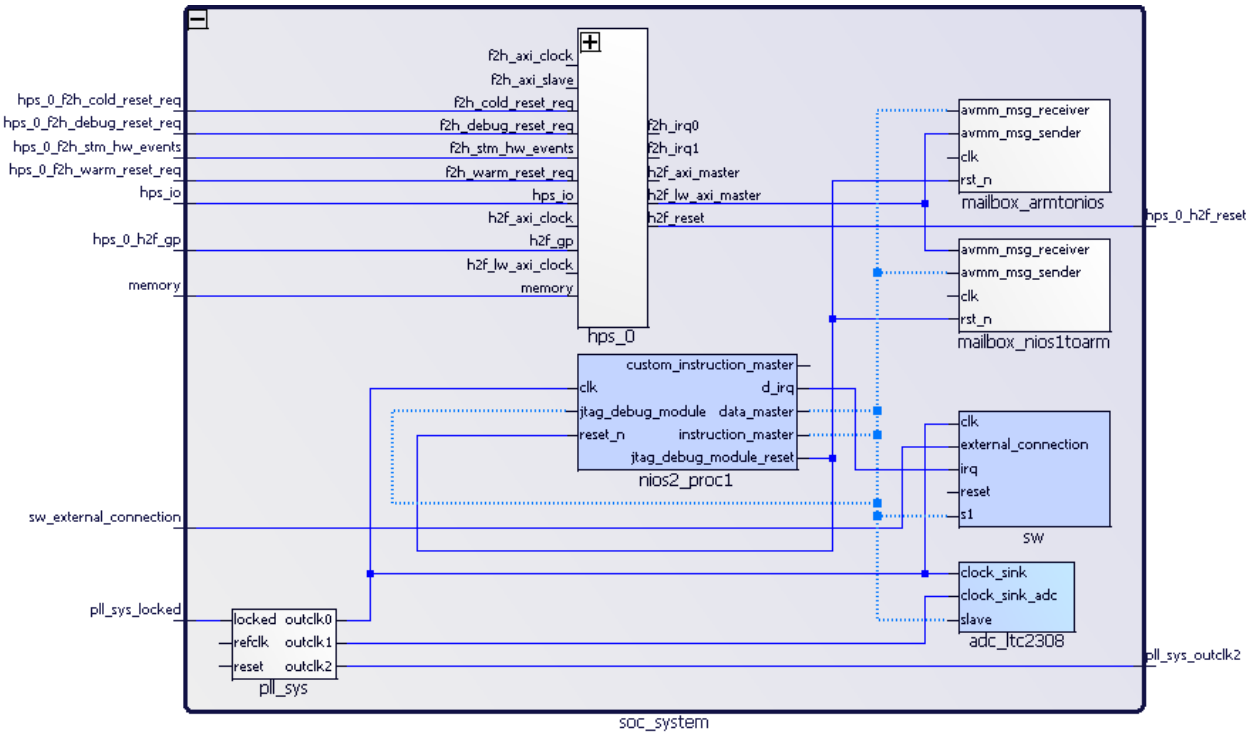


Figure 5.9 Reduced system architecture to illustrate NIOS and HPS connectivity through mailbox cores.

The Quartus 2 software tools performs analysis and synthesis of the FPGA system design at the time of project compilation. The timing analysis and pin fitting tests are performed during the compilation to check for any design related issues. Once the compilation is successfully complete, the FPGA configuration file is generated which could be programmed on to the FPGA fabric.

5.4 Software Design

The SoC board has HPS and FPGA Cyclone 5 fabric, Software needs to be developed separately for the two SoC sub-components. The following real time platforms were used as the software development environment.

- MicroC OS-II to develop software to be executed on NIOS 2 over the FPGA fabric.
- Embedded Linux to develop software for ARM Cortex A9 processors (HPS).

The FPGA fabric is used to accomplish the below tasks:

- ADC for data collection from the laser sensor.
- Control the data acquisition state through a hardware switch.
- MPD and standard deviation calculations in real time.
- Real time communication between the two NIOS cores and the HPS.

The HPS hardware component is used to accomplish the below tasks:

- Receive data acquired by the FPGA fabric
- Multithread data processing for real time digital filtering.
- Multi-thread real time data communication to remote client.
- Control LED indicators for to display server status.
- Control the data acquisition rate through the software.
- Manage the data collected in circular buffers.

5.4.1 ADC on FPGA fabric

ADC operation is the core of the data acquisition system for this application. The figure 5.10 shows the basic pin diagram of the ADC module and the figure 5.11 illustrates the software steps to start and stop the data acquisition, manage data into software buffers and make the buffers available to further processing for micro-texture measurement.

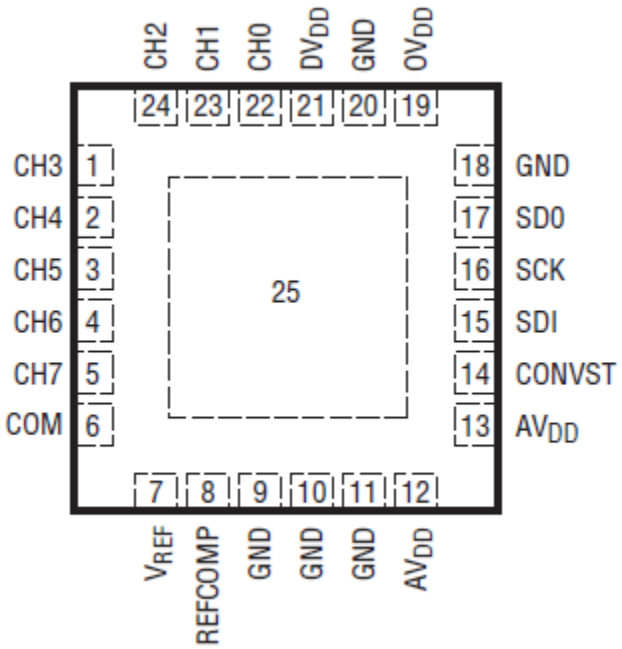
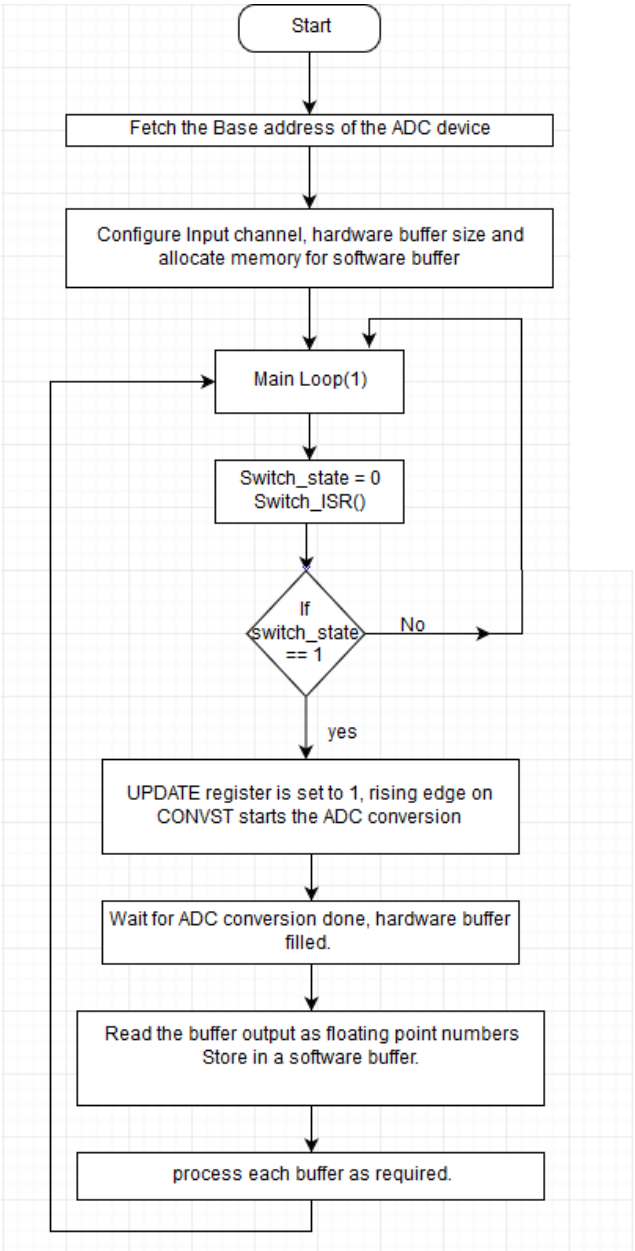


Figure 5.10 Pin diagram of Linear Technology LTC 2308 ADC converter. [16]

In the hardware definition, the ADC module was configured to perform operations at the rate of 100 KHz. It has 8 channels for simultaneous sampling and each channel has its configuration and output register. The hardware design supports reading the individual digital values into a hardware buffer of size up to 1024 for each software conversion cycle. Once a hardware buffer is full, the values are read into a software buffer for further processing.

- CONVST (PIN 14), a rising edge on this pin starts the ADC conversion.
- SDI (PIN15), configures the input channel and is latched on first 6 pulses of the clock (PIN 16).
- SDO (PIN 17) is the data out pin, data is shifted serially at each falling edge of the clock pulse
- CH0 to CH7 are the Analog input channels.


Start
Fetch the Base address of the ADC device
Configure Input channel, hardware buffer size and allocate memory for software buffer
Main Loop(1)
Switch_state = 0
Switch_ISR()
If switch_state == 1
No
yes
UPDATE register is set to 1, rising edge on CONVST starts the ADC conversion
Wait for ADC conversion done, hardware buffer filled.
Read the buffer output as floating point numbers Store in a software buffer.
process each buffer as required.

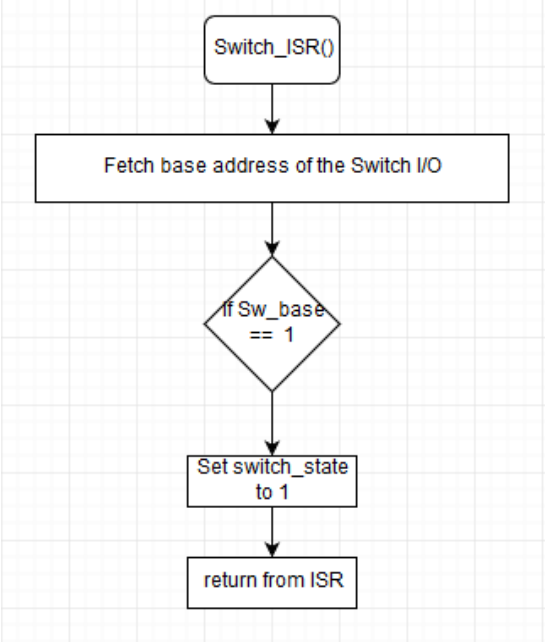


Figure 5.11 Flow chart for basic ADC operation controlled through the I/O switch.

5.4.2 Mailbox Core

In the software design, if multicore processors need to perform dedicated computations, inter-processor communication becomes a critical task. Mailbox cores provide a message passing interface between a sending processor and a receiving processor. For this application, the receiver polls the mailbox to fetch the messages. Polling and interrupts mechanism could be used to fetch the messages once available in the mailbox. It uses two registers each of size 32 bits for passing the messages between the sender and the receiver processor.

- Command register: 32 bit register, used to transfer user defined messages between the processors.
- Pointer register: instead of passing the message, 32 bit address is passed to the pointer register. The receiver processor could dereference the value pointed by pointer register.

- Status register: indicates mailbox full or empty status. Mailbox can message only one value at a time, if the value is not read by the receiver processor it must indicate a pending message in the mailbox and the mailbox remain full until it is read.

Flowchart in the figure 5.12 illustrates the working of a mailbox core.

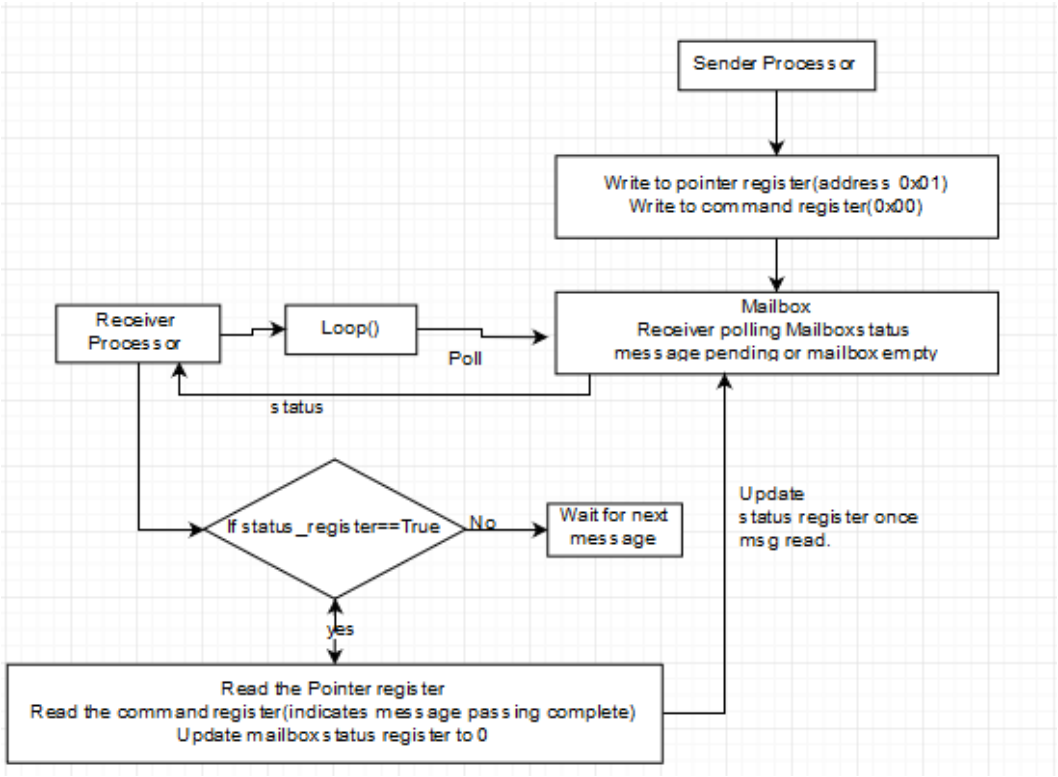


Figure 5.12 Flow diagram of Mailbox core send and receive message.

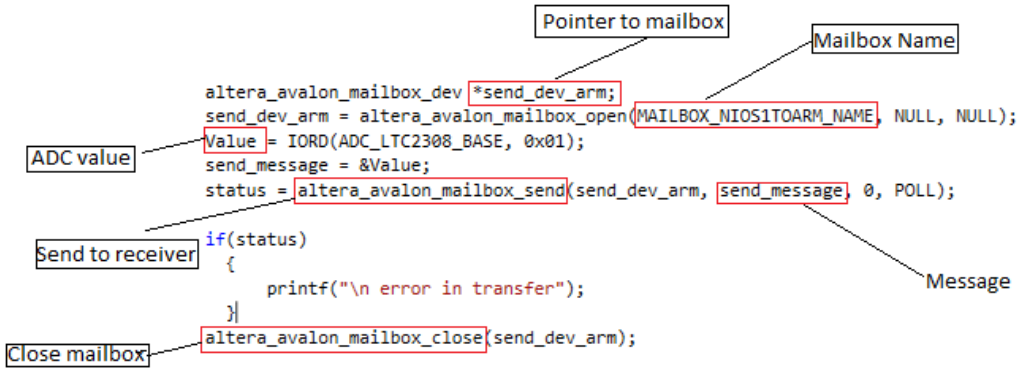


Figure 5.13 Mailbox example code to send message using Altera® HAL

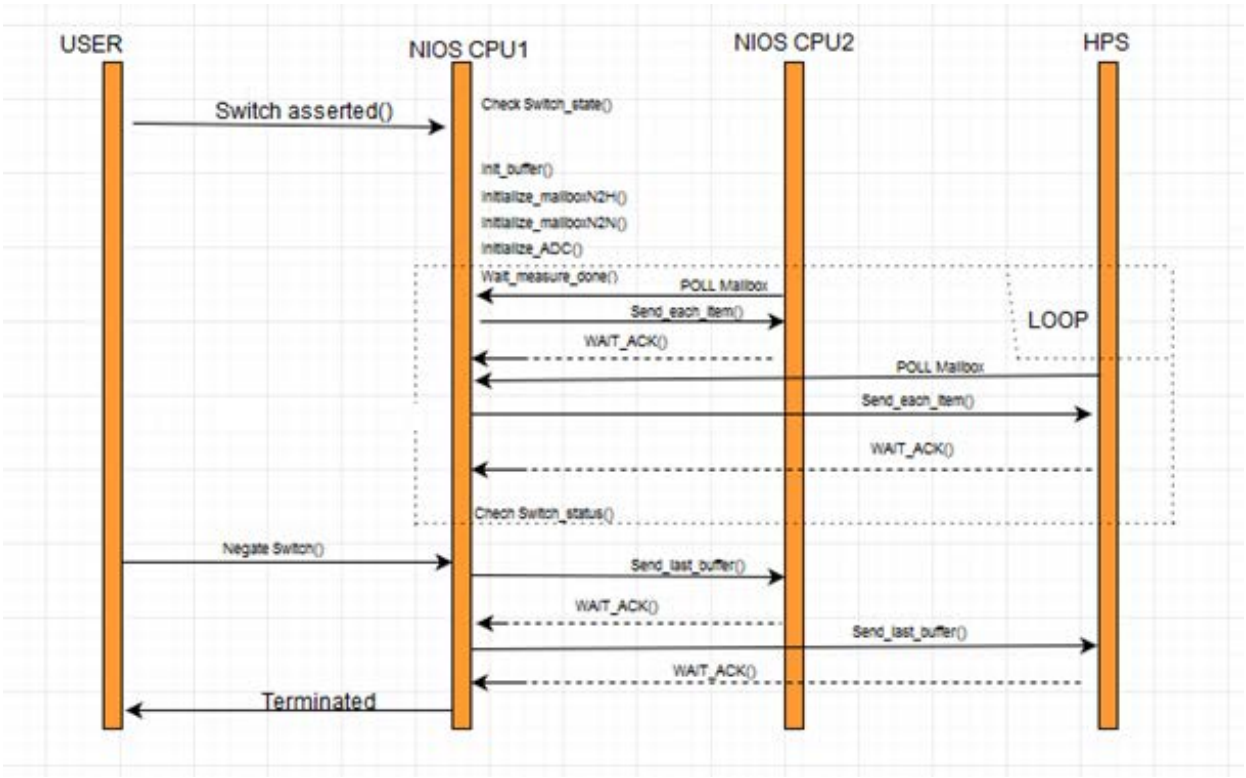


Figure 5.14 Time sequence diagram for FPGA side operations.

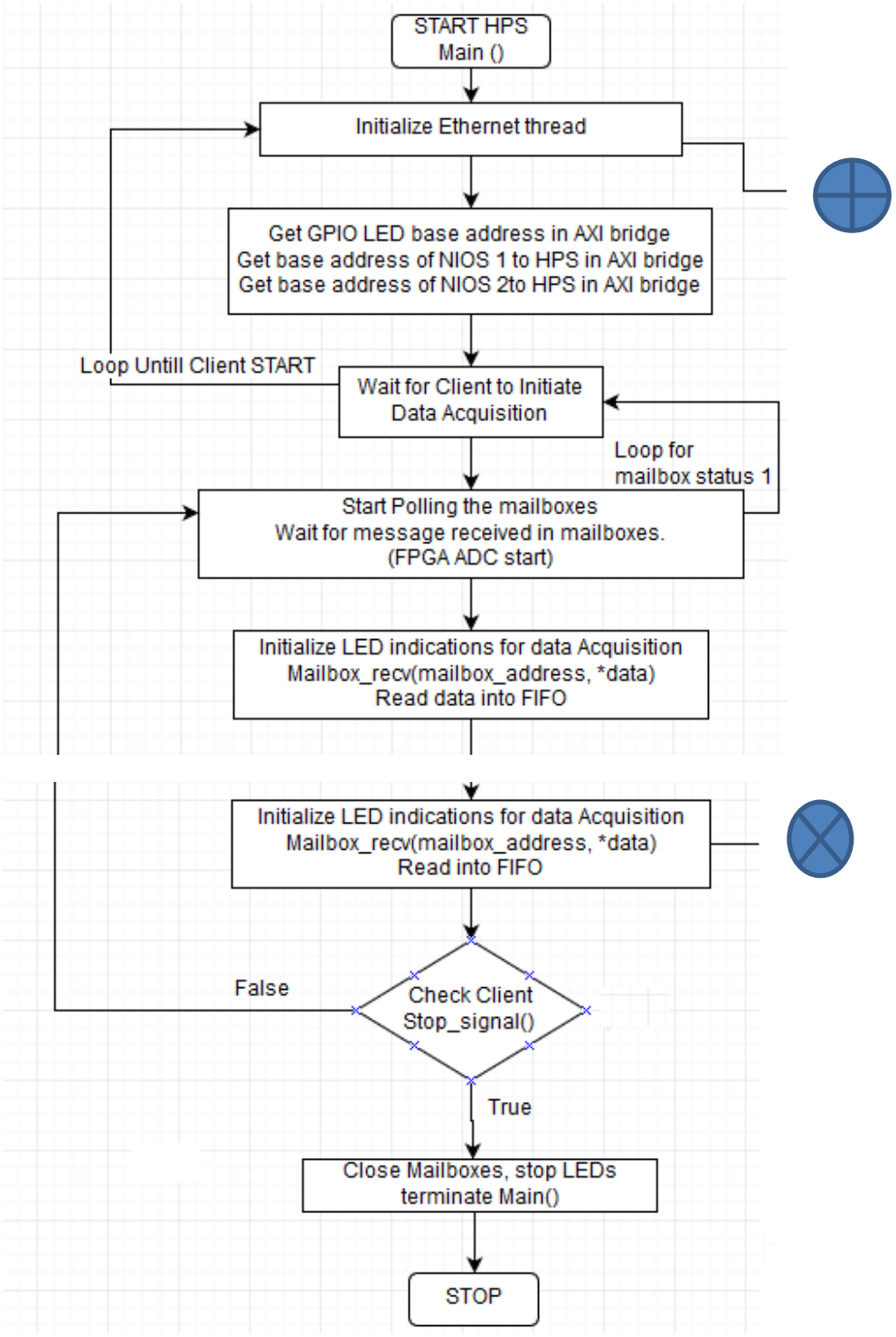


Figure 5.15 Flow chart for HPS multithreaded processing and Ethernet communication.

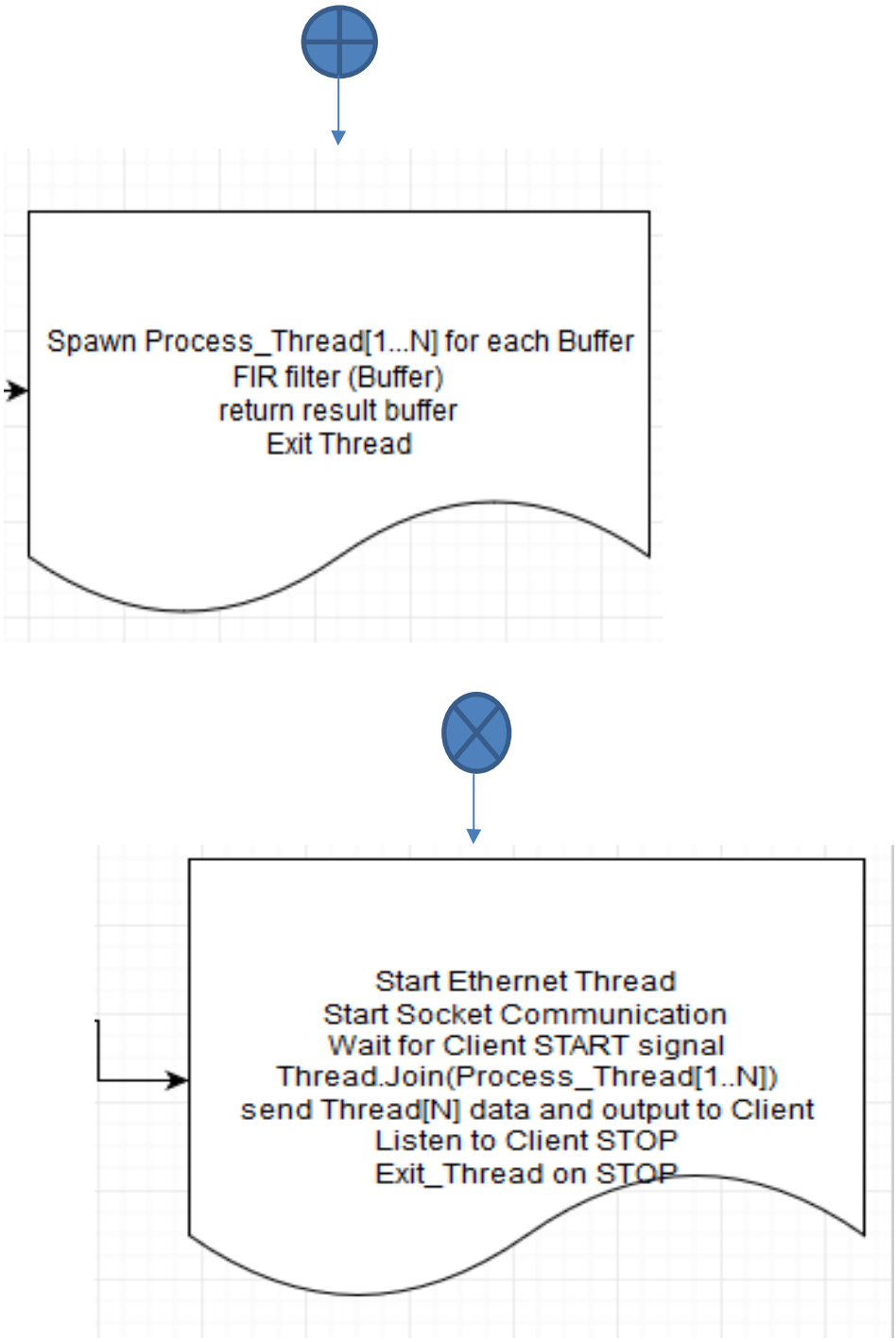


Figure 5.16 Flowchart for HPS multithreaded processing and Ethernet communication

CHAPTER 6

RESULTS AND CONCLUSION

The FPGA board was evaluated for the following parameters:

- Accuracy of Measurements (comparison with a standard device).
- Performance for real time computation (multi core and multi thread capabilities).
- Effect on data obtained by changing surface colour.
- Sampling Rate supported by the FPGA board.

FPGA
33530
33600
33600
33600
33570
33570
33610
33690
33690
33710
33710
33740
33720
33720
33690
33690
33690

Figure 6.1 Sample of data acquired from FPGA for a small portion of an aggregate.

The difference between the digital readings of DT9816 board and Linear Technology ADC on the FPGA board is evident as illustrated in figure 6.4. The two boards have significant difference between the digital outputs, DT9816 has a proven record of accuracy and hence more tests need to be performed with the Linear Technology ADC device w.r.t. environment and its sensitivity to conclude the reason for this incorrect result in the output.

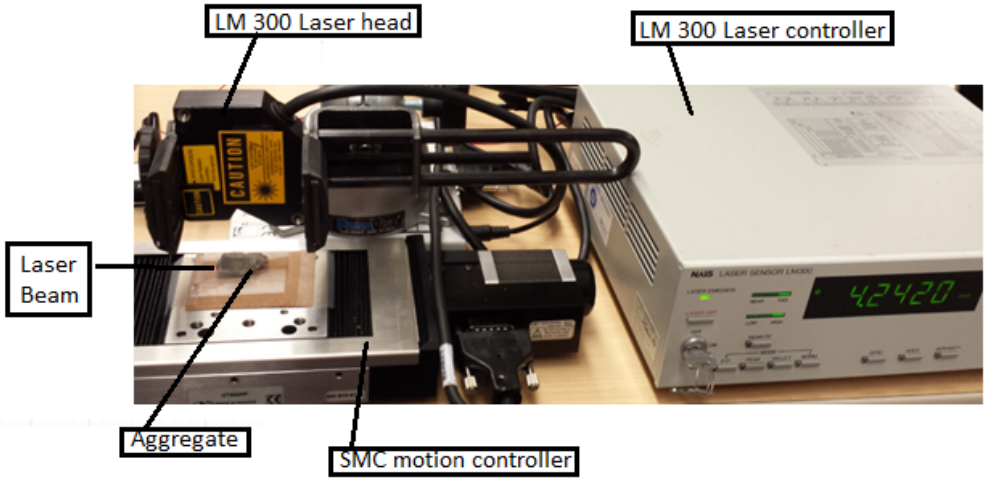


Figure 6.2 LM300 with SMC Motion control system

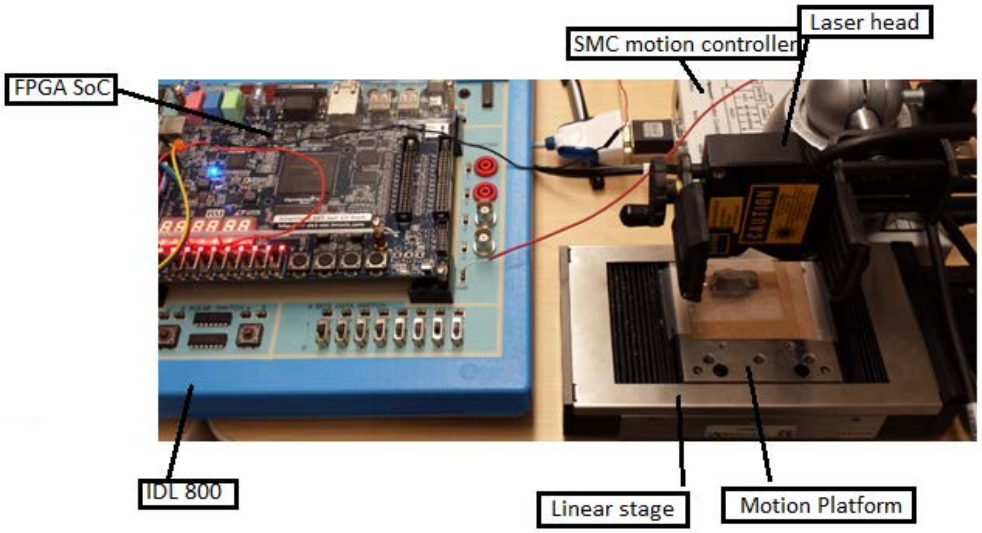


Figure 6.3 Complete FPGA Texture measurement instrument

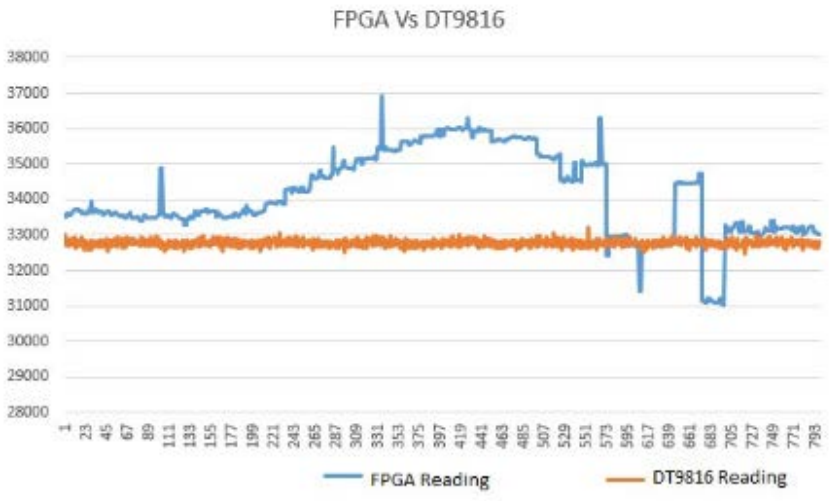


Figure 6.4 Comparison of Level of detail between 800 points obtained from DT9816 board and FPGA board.

The difference in DT9816 and FPGA digital readings could be seen from the figure 6.4, also the high peaks and low peaks are not the part of the aggregate surface, these highs and low peaks could be considered as the laser displacement noise or noise from ADC data. The exact reason for the noise is unclear, Linear Technology ADC on FPGA board should be thoroughly tested before the use for real time measurements.

Figure 6.4 Picture of laser with motion control for a Graphite sample.

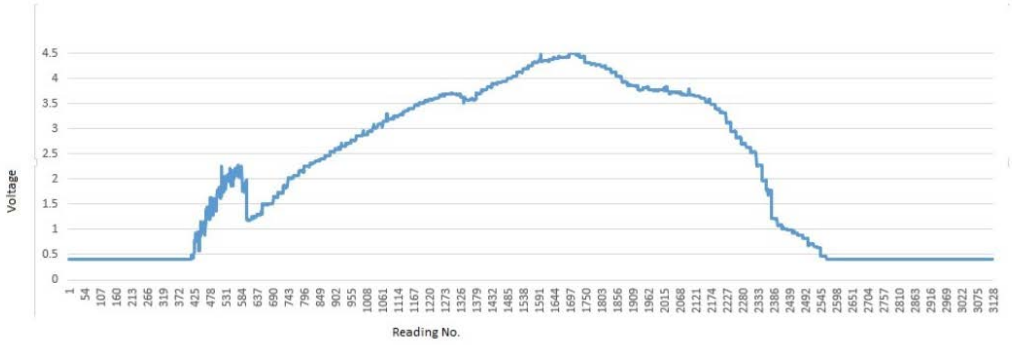


Figure 6.5 Single point laser data for Granite sample obtained through FPGA Linear Technology ADC device.

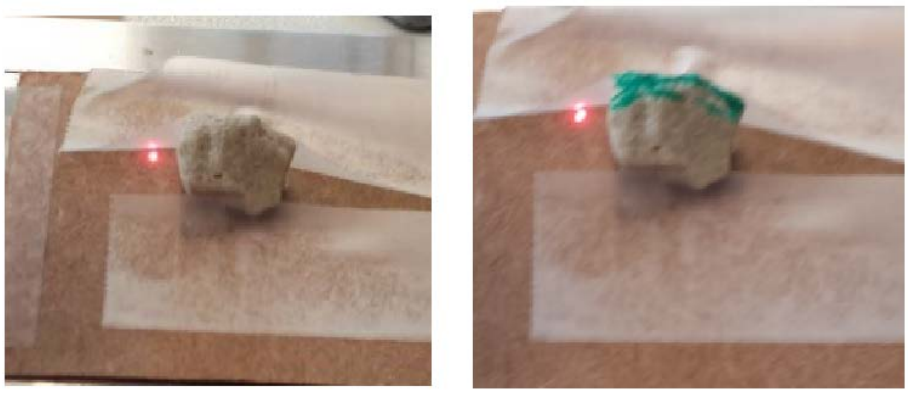


Figure 6.6 Laser measurements on a marked and unmarked aggregate.

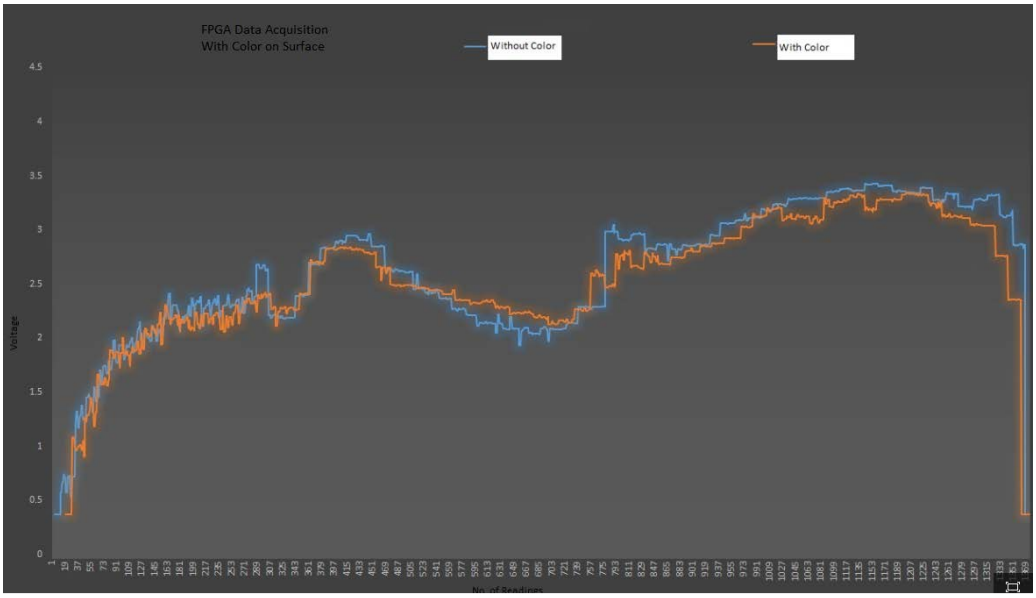


Figure 6.7 FPGA Data Acquisition with and without colour on the Aggregate Surface for a limestone sample.

The results obtained from FPGA ADC with and without the use of colors on the surface of the aggregate were similar to the results obtained using DT9816 board. The similarity could be used to conclude that colors on the surface of aggregate do not produce a significant change in the texture measured through laser sensor.

From the Hardware and Software designed using the FPGA board for real time ADC and high performance computing, the FPGA SoC has proved to be a good platform for embedded computing in real time use, especially because it provides a flexibility to use Embedded Linux on a high performance embedded applications processor such as ARM cortex A9 along with a FPGA chip which could be useful for performance acceleration and on demand reconfiguration capability of the hardware design. The following conclusions could be made for the use of FPGA SoC in real time applications:

- FPGA system on chip is a suitable platform for use in data acquisition and real time processing.
- The firmware and hardware is easily reconfigurable for numerous real time applications.
- Parallel processing infrastructure can be developed using multiple soft cores.
- Hard processor supports efficient multithreaded real time application.
- Soft processors could be dedicatedly used to parallel processing different peripherals.

6.2 Future Work

- Interface and synchronize a motion controller for precise motion with FPGA board and laser sensor. This would enable the precision motion control.
- Check if more efficient inter – processor communication can be achieved by using DMA and Mutex IP core. This would be useful to obtain higher performance by using the system on chip hardware.

References

[1] Impact of Changes in Profile Measurement Technology on QA Testing of Pavement Smoothness, Technical report 0-6610-1.

[2] Philip H.W. Leong, “Recent Trends in FPGA Architectures and Applications”, 4th IEEE International Symposium on Electronic Design, Test & Applications, IEEE 2008

[3] Mahone, D.C. 1975. An Evaluation of the Effects of Tread Depth, Pavement Texture, and Water Film Thickness on Skid Number: Speed Gradients. Virginia Highway and Transportation Research Council, Charlottesville.

[4] Development and implementation of a pavement and surface texture measurement system, Research Project # 2981.
http://library.ctr.utexas.edu/digitized/texasarchive/phase1/2981-1.pdf

[5] NAIS laser manual for LM100/LM200 models.
https://www.panasonic-electric-works.com/pew/eu/downloads/ds_x631_en_lm100_lm200.pdf

[6] LMI technologies Gocator 2300 series datasheet.
http://downloads.lmi3d.com/system/files/Gocator/documents/Gocator%202300%20Series/DATASHEET_Gocator_2300_WEB_EN.pdf

[7] Keyence LC 2400 series laser sensor datasheet.
http://www.artisantg.com/info/PDF__4B6579656E63655F4C43323430305F5365726965735F446174617368656574.pdf

[8] DT9816 Data Translation® module datasheet.
https://datatranslation.box.com/shared/static/aabdc787ad5cbd7d1f91.pdf

[9] DT9816 Data Translation® module user guide.
https://datatranslation.box.com/shared/static/9c7ad0d414e6a3f67795.pdf

[10] A portable profiler for pavement profile measurement. Research Project # 0-6004

http://ranger.uta.edu/~walker/Reports/Final_0-6004-1.pdf

[11] Alter user customizable ARM based SOC, white paper.

https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/br/br-soc-fpga.pdf

[12] Ulf Sandberg 1998. Influence of road surface texture on traffic characteristics related to environment, economy and safety.

[13] Gates, L., Masad, E., Pyle, R., and Bushee D. (2011). “Aggregate Imaging Measurement System 2 (AIMS 2), Report# FHWA-HIF-11-030

[14] DE1-SOC user manual, available at Altera® website.

[15] My First HPS-FPGA document available at Altera® website.

[16] Linear technology LTC 2308 datasheet.

[17] PK Gupta, Director of Cloud Platform Technology, DCG/CPG, Intel® Xeon®+FPGA Platform for the Data centre[online]:

http://reconfigurablecomputing4themasses.net/files/2.2%20PK.pdf

[18] Garrison W. Greenwood, Andrew M. Tyrrell, “Introduction to evolvable hardware”, IEEE press

[19] Keyence Laser systems manual.

[20] Laser NIAS LM 300 user manual.

Biographical Information

Mudit Pradhan did Bachelors in computer science from Uttar Pradesh technical university, India, in Computer Science and Engineering in the year 2008. He then pursued his career in Thin Computing and Mobile computing technologies working with DELL Wyse and Qualcomm in India. He started his Master's program in the year 2014 in Computer Science at University of Texas at Arlington where he worked as a Graduate Teaching Assistant and Graduate Research Assistant for Dr. Roger Walker, developing Embedded and real-time systems for Texas Department of Transportation. He plans to pursue his career as an embedded engineer and machine learning enthusiast.