STUDY OF CRACK PROPAGATION UNDER THERMAL LOADING ON A 3D TSV PACKAGE

by

SUBRAMANIAN R GOWTHAMAN

Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements for the Degree of

MASTER OF SCIENCE IN MECHANICAL ENGINEERING.

THE UNIVERSITY OF TEXAS AT ARLINGTON

August 2016

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Acknowledgements

I would like to sincerely thank my parents for providing me everything to pursue my Master's degree. I would like to thank Dr. Agonafer for all his support and opportunity he gave me to pursue my research work and successfully carry it out.

I am thankful to my guide Dr. Fahad Mirza for his support, suggestions and guidance he had provided. I would like to thank my close friend Mr. Mohammed Shahid Ali for his support throughout my research and for playing a big part in my research.

Thank you Sally Thompson and Debi Barton for all the good works that you are doing to help all the students grow.

August 10, 2016

Abstract

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Subramanian R Gowthaman, MS

The University of Texas at Arlington, 2016

Supervising Professor: Dereje Agonafer

Today, there is a revolution in going for miniaturization in size of electronic packages. More thinner, lighter and complex packages are in use for almost every electronic device. This initiation was taken to the next level and gives us a whole new ideology called 3D packaging. Currently, 3D packaging is the on-going research in almost all the electronic packaging related industries. 3D package uses Through Silicon Via (TSV) technology that gained momentum in the development and helped packaging system for significant miniaturization and power reduction, which result in increased performance. However, the reliability assessment is needed to evaluate the critical areas in TSV based 3D ICs. In electronic packages, reliability is the most important issue for electronic device manufacturing company and in any research institutes. In this paper, the different types of crack that can happen along the TSV/Si interface has been determined with the study of behaviors of crack. Finite element method is used for the analysis of TSV region and calculation of stress intensity factor (SIF). Stress Intensity Factor (SIF) is a function of applied load, component dimensions and the length of the crack. Analyzing all these functions will help us to give more ideas about crack propagation and thereby help us to take preventive measures.

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Chapter 1

Introduction

1.1. Microelectronics industry

Due to the technological advancement, electronics are undergoing miniaturization to become denser, smaller and lighter for maximum portability in today's digitalized industry. And at the same time, efficiency and quality should be improved with lower cost and reduced power loss to supply problem-free computing and also perform top notch functions for the requirements. For this, an effective communication has to be established between the IC's and the electronic systems without affecting the cost and form factor by the increased complexity [13]. Therefore, various other issues arising because of the factors such as cooling within the devices, signal processing time, heat dissipation, chemical and other reliability problems has to be effectively addressed by electronic packaging.

Figure 1-1 Trends in Packaging Technology [15]

1.2. The Basics of Electronic Packaging

As per the definition, Electronic packaging is the science of creating a suitable condition to the electronic product, to function reliably, for a long time period. Creating a suitable conditions includes, but not limited to, electrical, thermal and other green issues. It comprises all of the technologies related between IC and the system [16]. The function of electronic packaging is critical here as the function of the IC's and the system can be regulated only when the electronic product is packaged properly. The different levels in electronic packaging are classified into three types:

1. Chip-Level.
2. Board-Level.
3. System-Level.

Chip-Level Packaging: It is the lowest level of packaging and it consists of procedures to conveniently handle and do packaging of bare die to the boards. Earlier, it is impossible to use bare dies directly, though now it has become possible as well because of this system implication.

Figure 1-2 Process in Chip Level Package [16]

Board-Level Packaging: The bare dies that are packaged in Chip – Level Packaging are assembled and mounted together on system level boards in this packaging to perform system level functions.

System-Level Packaging: In this level, it is the integration as well as the combination of both chip level and board level packaging to make together as a system to function specific performance, per user requirements. E.g., Personal Computers, Cameras, Cell Phones, etc.

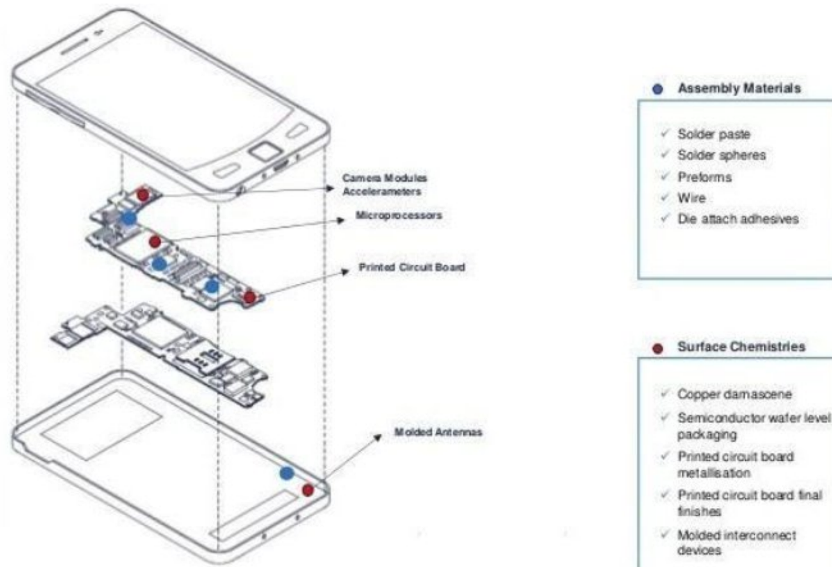

Figure 1-3 Packaging Application of a Mobile Device in System Level [17]

There was a trade-off with size, performance of the device and its cost in electronic packages, as the buyer always needs a product that is cheaper, smaller and does high functions. As we increase the performance and reduce the form factor product, the cost that is in the play tends to increase. Therefore, there needs to be an establishment of productive trade among these factor to create and produce an optimum system. Due to the miniaturization, reliability and testing of the product has to be vital so that it is thermo-mechanically strong, properly dissipates heat and has long life span while withstanding real life situations without compromising anything.

1.3. Packaging Levels

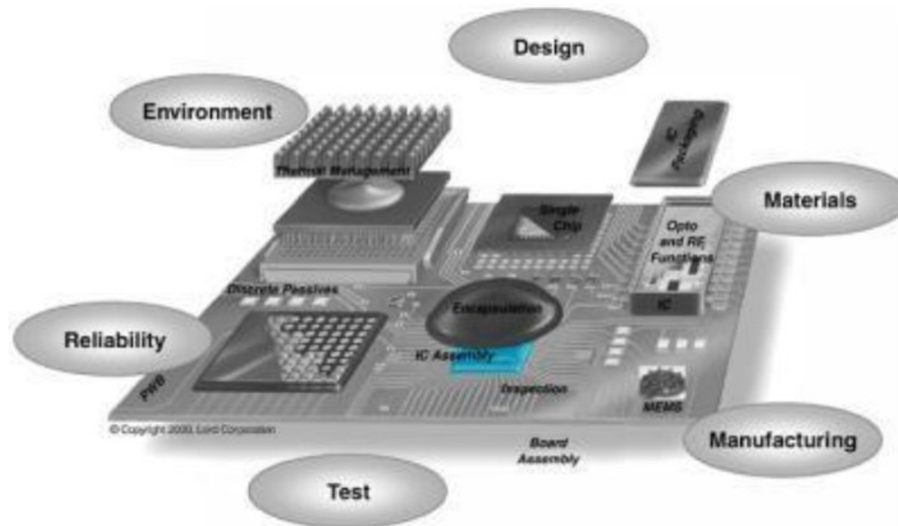

Figure 1-4 Considerations in Electronic Packaging [15]

The various stages in electronic packaging are noted below:

Stage 0: Inter-connections in a monolithic silicon die.

Stage 1: Packaging silicon dies into single chip package.

Stage 2: Multi-chip modules based on chip set technology.

Stage 3: Printed wiring cards and board.

Stage 4: Complete electronic system containing multiple subassemblies (boards, racks and frames).

Chapter 2

Current Works in 3D Packaging

The roadmap of electronic packaging is driven in such a direction that chips with more input/output terminals (I/Os) and state-of-the-art multi-functionality is going to take over [18]. Immediate changes have to be made regarding the design, methods of manufacture and selection of materials in order to meet such requirements.

Wafer Level Packaging, 3 Dimensional (3D) Stacking using wire bonds and flip chips, 3D System-in-Package (SiP), Package-On-Package (PoP), 2.5D interposer are few of the latest trends that are making way for emerging technologies.

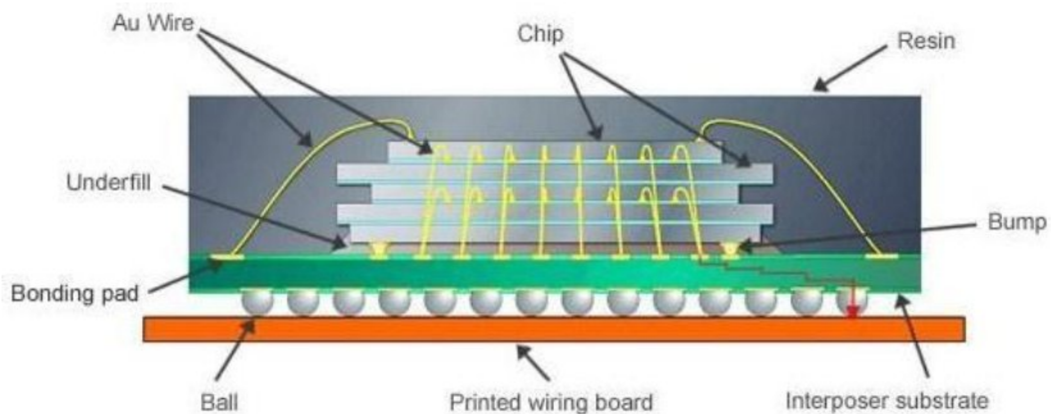

Figure 2-1 SiP Package using Stacked Chips [20]

As the chip packaging research reaching its limits, the researchers are continuously trying to find out new methods and one of those technologies is 3-Dimensional arrangement in vertical direction. There are various methods of packaging in 3D packaging technology that helps in plane stacking of the dies, thereby, helping us to use the real estate of PCB more effectively.

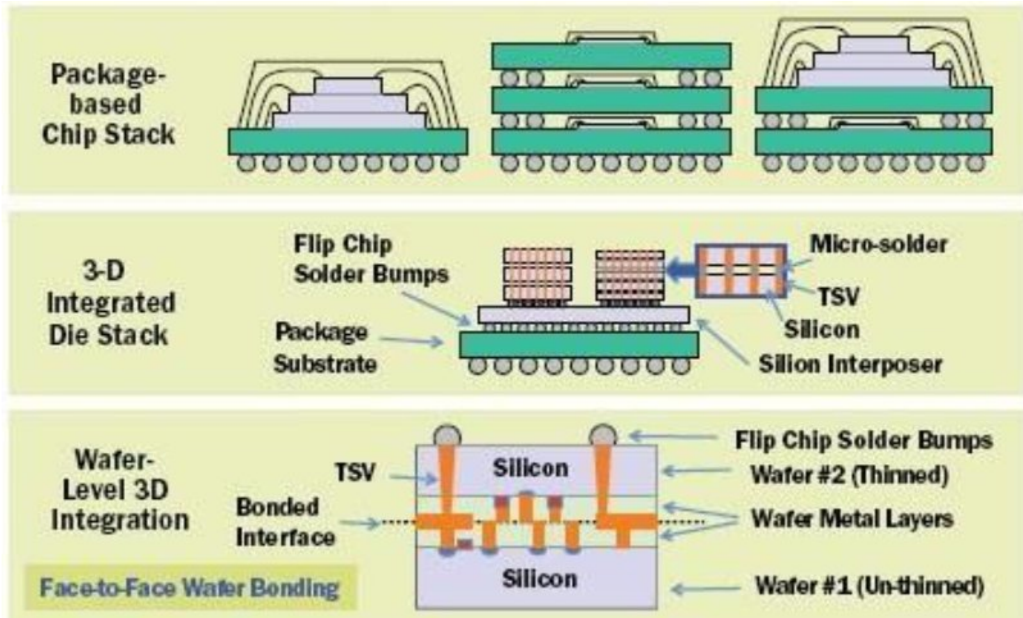

Figure 2-2 Technologies of 3D Packaging [21]

1. Wafer-Level Packaging (WLP): In WLP, at wafer level, all the packaging is made, and only after wafer fabrication, the where-in packaging, testing and burn-in is made [19]. WLP packages has an advantage of low cost than CSP and BGA packages. Also, it has smaller chip size and suitable for mobile devices, while there is no need of under fill during assembly.

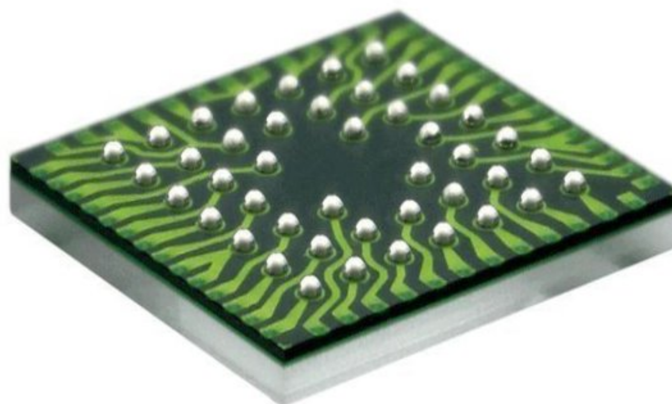

Figure 2-3 Ball Grid Array Interface in WLP Package [22]

2. System-in-Package (SiP): Many number of ICs enclosed within a single module package as a system is called SiP [23]. Music Players, mobile camcorders uses this system. Interconnects uses wire-bonding technology and it is used for functioning all the performance of an electronic system, by vertical stacking or horizontal tiling [24]. Though it has many advantages, if a single chip becomes defective then the whole package becomes non-functional.

2.1. Issues with 3D Packaging

The complete usage of the Chip Real Estate (CRE) in 3D packaging is still a challenge. Though wire bonding helps in interconnectivity, it only uses the peripheral of the silicon area. Issues like power loss, RC delay and the usage of peripheral area alone are the drawbacks of wire bonding. Though the above packages are the realistic solutions for 3D packaging, the implication of TSV provides more functionality and eliminates all the drawbacks in wire bonding.

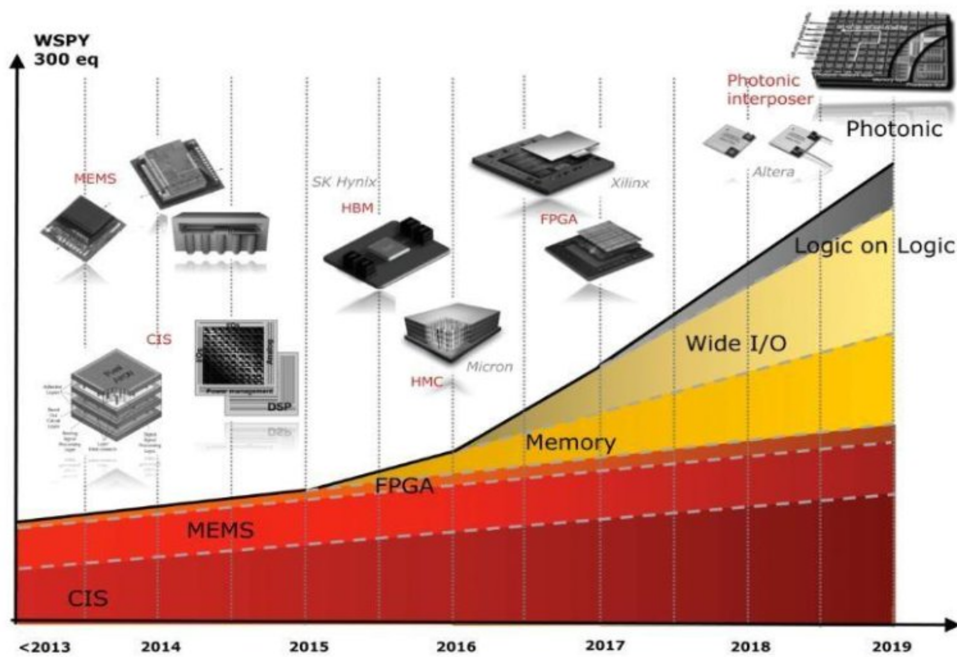

Figure 2-4 TSV Wafer Breakdowns [Source: Yole Development]

In 3D IC technology, we have the flexibility of design, more bandwidth, smaller footprint, complete utilization of CRE (Chip Real Estate), functional integration, etc. using TSV technology, as it is possible to achieve shorter interconnects, thereby having low RC delay and resistance. When two chips are connected by wire-bonding technology, not all the I/Os are fully utilized, as it is one of the challenges in 3D wire-bonding technology. The powerless and RC delays are also some of the drawbacks in 3D wire-bonding.

To overcome this problem, 3D TSV technology provides an excellent alternative and it is considered as the prime technology in integrating and stacking of dies. In a 3D TSV package, a hole is drilled through the thin silicon wafer and dielectric SiO_2 is deposited

inside the hole along the wall and it is filled with Copper. As the interconnect length is less, the processing time, resistance and the power loss is also reduced. Also, the increased number of I/Os in TSV facilitates improvement in functionality. In a very small area, we can incorporate TSV's to have thousands of inputs and outputs. TSV is the next generation technology that drives the current 3D packaging. Amidst of all these advancements, there are some issues like heat formation, structural integrity, interaction in TSV chip package, that are currently in research and development.

2.3. Limits in TSV Technology

The major issue with implementing TSV technology is its limitation to remove heat from the system (taking heat out of the stacked chips). Thermal stresses will be developed in the Silicon, Copper because of the CTE mismatch in those areas, if the heat is not properly removed from the system.

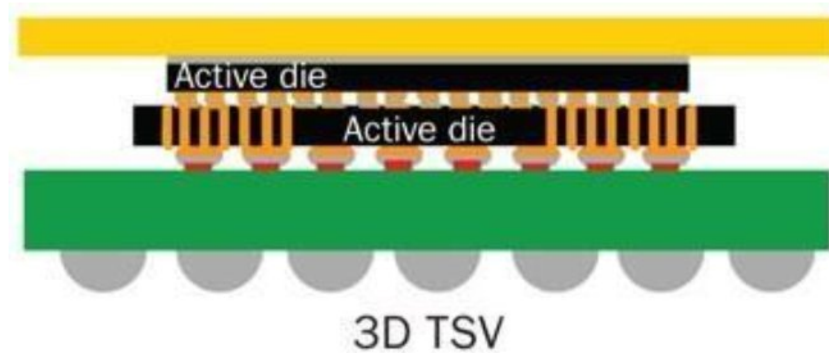

Figure 2-5 TSV Package

There is a space called 'Keep Out Zone (KOZ)' which is created around the TSV, and because of the thermal stress developed in that space, no active transistors can be placed and therefore, this area is not efficiently used. As the TSV's go through chips have transistors, it cannot be placed in the areas that has thermal stress. It is hard to eliminate

heat from the stacked chips. Thermal stresses have been developed between different materials at their interface because of the developed heat, and it creates structural integrity problems such as cracking, warpage, etc. Various materials expand and contract based on their CTE values. Silicon/silicon dioxide interface is very brittle and hence cracks will be easily formed in that region. One of the methods to reduce this problem is to find the critical areas along the length of the TSV and by using fracture mechanics, the types of cracks that are prevalent in those regions should be determine.

Material	Young's Modulus [Gpa]	Poisson Ratio	Coefficient of Thermal Expansion (CTE) [ppm/°C]
Silicon	169	0.26	2.3
SiO2	75	0.17	0.5
Copper	117	0.3	16.7

Table 2-1 Material Properties of Si and Cu

The main reason fracture mechanics is used here is because of the limitation that sharp corners that has flaw cannot be used in the stress concentration equation. Stress concentration is present in elliptical and square holes and linear elastic theory addresses this subject. Fracture mechanics is used here because the stress becomes infinity at the crack tip. Therefore, Stress Intensity Factor is being used here.

This research is primarily narrowed to analyze the structural integrity of a two die 3D TSV package during chip attachment to find the stress intensity factors in the interface of TSV/Silicon and thereby showing the prevalent types of cracking in TSV. Secondly the research is focused on finding the relation between the geometry of the die and substrate and how it affects the stress intensity factor arising in the TSV.

Chapter 3

Application Fracture Mechanics in TSV Package

It has been studied that the crack formation is the main reason why structures and components begins to fail [25]. Griffin introduced how the fracture, stress and toughness affects each other in the year 1920. Irwin proposed his research about the release of strain energy in the year 1950. Crack propagation occurs when the strain energy release rate attains a critical value. The stress intensity factor (K) is also calculated using similar method as the strain energy release rate. This is used to find the amount of stress present at the crack tip because of the developed stress [26]. The value of stress intensity factor K will be mainly affected by the size and location of the crack.

$$\sigma_x = \frac{K}{\sqrt{2\pi r}} \cos\frac{\theta}{2}\left[1 - \sin\frac{\theta}{2}\sin\frac{3\theta}{2}\right]$$

$$\sigma_y = \frac{K}{\sqrt{2\pi r}} \cos\frac{\theta}{2}\left[1 + \sin\frac{\theta}{2}\sin\frac{3\theta}{2}\right]$$

$$\sigma_{xy} = \frac{K}{\sqrt{2\pi r}} \sin\frac{\theta}{2}\left[\cos\frac{\theta}{2}\cos\frac{3\theta}{2}\right]$$

[28]

3.1 Introduction to J-integral

The fundamentals and the foundation of fracture mechanics have been established in 1960s. Rice invented a method called J-integral which is used to calculate the energy release rate of the non-linear materials described as a path independent line integral.

The equation for a cracked body with a cracked tip, under Mode-I condition is given as:

$$J = \int_{\Gamma} \left(w dy - T_i \frac{\partial u_i}{\partial x} ds \right)$$

[27]

Where, w is the strain energy density that includes stress and strain tensor components.

Ti = σij*n (i^{th} components of vectors of traction and displacement), n is the j_{th} component of unit outward normal to integration path, ds is the differential length along the contour C, and u_1 is the differentiation of displacement with respect to x_1 [26]

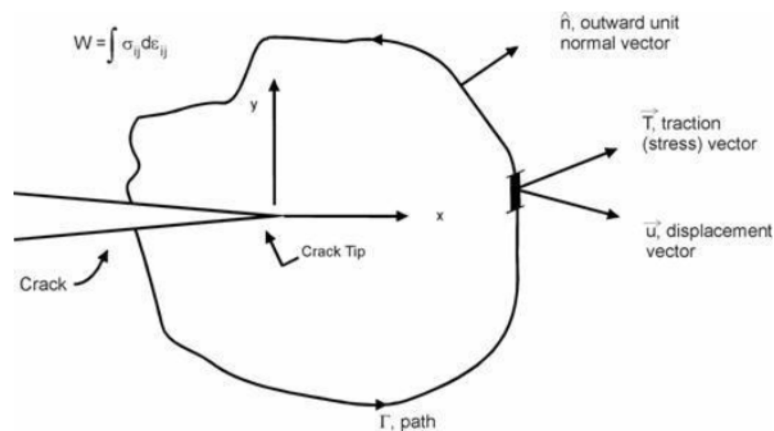

Figure 3-1 Parameters of J-Integral [28]

3.2. Types of Cracking

Using linear independent cracking modes, fracture phenomenon is analyzed by Fracture mechanics. These crack types are divided into three types as Mode I, II, or III as represented in the figure.

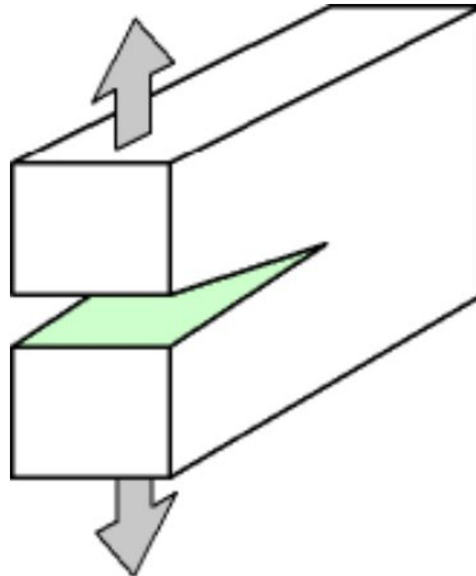

Figure 3-2 Type I Cracking [30]

In Mode I, the opening (tensile) mode is created in which the crack surfaces drifts apart in the opposite direction to each other due to tensile load. In Mode II, the crack (in-plane shear) mode is created by the surfaces sliding over each other in a way right-angled to the outer edge of the crack [29]. In Mode III, the crack is in a tearing (anti-plane shear) mode in which the surfaces of the crack move parallel and relative to each other with respect to the outer edge of the crack. Mode I type of crack is more prevalent in engineering design. Fracture is the combination of crack and its propagation.

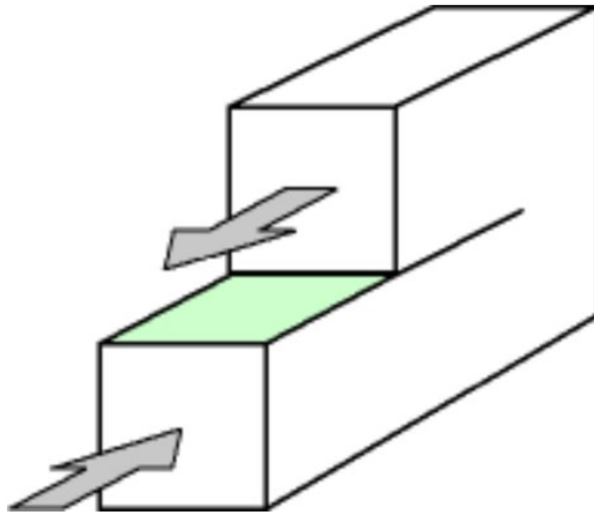

Figure 3-3 Type II Cracking [30]

By studying the crack propagation dynamics inside the material, deep knowledge can be attained about the different types of fracture modes. By research, it is shown that the crack slowly propagates in ductile materials with high plastic deformation rate, and continues to propagate as long as the stress is induced. Whereas in brittle materials that has little to no plastic deformation, the crack propagation is very rapid and its magnitude increases after its initiation.

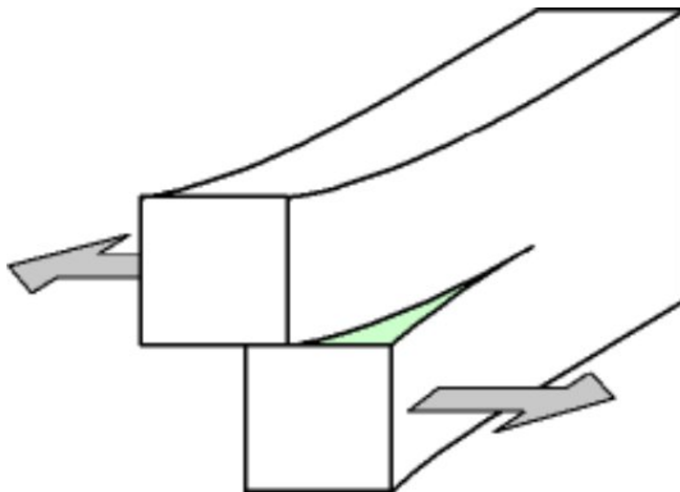

Figure 3-4 Type III Cracking [30]

3.3. Stress Intensity Factor and Fracture Toughness

For every material, there is a critical stress intensity factor which is the threshold value above which the material will result in producing fracture. [28]. This acts in the same way of yield strength. Fracture toughness is the value of stress intensity factor where the crack propagates in the material and it is denoted by K_C, and it can be expressed using the mathematical expression as below:

if K = Kc,

Then crack propagation occurs.

During the propagation, it provides information about the stress intensity field at the location of the crack. The factors affecting the fracture toughness are the rate of strain, temperature and thickness of the material. Based on the thickness of the material, the way at which the crack may propagate is related.

The stress intensity factors designations are given by the subscripts which are given below. For the opening crack mode, K_{I} is the subscript given to indicate the stress intensity factor for mode I. For the crack sliding (shearing) mode, K_{II} is the subscript given to indicate the stress intensity factor for mode II. For the out of plane (tearing out) mode, K_{III} is the subscript given to indicate the stress intensity factor for mode III. The 3 designations with their corresponding relations are shown below:

$$K_{\mathrm{I}} = \lim_{r \to 0} \sqrt{2\pi r}\, \sigma_{yy}(r, 0)$$

$$K_{\mathrm{II}} = \lim_{r \to 0} \sqrt{2\pi r}\, \sigma_{yx}(r, 0)$$

$$K_{\mathrm{III}} = \lim_{r \to 0} \sqrt{2\pi r}\, \sigma_{yz}(r, 0)$$

[26]

Chapter 4

Modeling and Analysis

The model of the crack was created using ANSYS 16 and as of now only semi-elliptical crack model can be created. Therefore, a global TSV package has been created, and by quarter symmetry method, the model is simulated for reflow conditions in order to analyze the different types of stresses that develops in the TSV package because of the thermal reflow boundary conditions varying from 200 degree Celsius to 25 degree Celsius (room temperature). And also, sub-modeling method is also been used to analyze the TSV Si/Cu interface. It is analyzed in depth by using the corresponding imported cut boundary conditions. As the crack can be created only on the open surface of the model (as of ANYSYS 16), the sub-model has to be cut into two equal halves. One of the halves is used from the sub-model to model the cylindrical silicon interposer crack (with the cut boundary constraints imported). The characteristics of stress intensity factor and J-integral have been studied by varying the die, substrate thickness, changing the crack dimensions. Finally, the SIF is compared to the silicon fracture toughness.

4.1. Model Description

A 2 die, 3 D flip-chip package model with TSV was taken from [6], and is attached to the substrate in order to study its response. The TSV in the package has a diameter of about 10μm, with the die electric thickness of 0.5μm. The chip real estate (CRE) of the TSV is about 1.5% of the total CRE, so the efficiency of the silicon is not affected, since the area of the TSV is limited to less than 4%. A compact modeling technique as performed by Mirza et al. [8] and Chirag et al. [11], is also implemented so the computational timing is maintained to a reasonable amount.

A three step simulation is performed. In the first step, a formulation of compact global model is done and solved. In step two, a sub-model 1 is taken from the far corner region of the global model which includes detailed features such as TSVs and the μ-bump interconnects, and gets its boundary conditions from the compact global model. In step three, a sub-model 2 which is the half of sub-model 1 is created on which the cut boundary conditions are applied and crack is designed. The confinements of the normal displacement towards the symmetric faces are the applied boundary conditions here in addition to fixing the bottom center node. This procedure is made in order to prevent rigid body motions. Linear elastic properties are used to model the materials with the exception of Cu metal and solders. The plastic deformation and the creep are taken into account in solder so its secondary creep can be included. As a rate dependent visco-plastic material, Anand's model is used. And to describe in-elastic characteristics of lead free solder, Anand's visco-plastic constitutive law was used. The material constants for Anand's visco-plastic laws are, $\hat{s}$, A, ξ, m, h, a, n, s, Q are used to describe the sensitivity of temperature in solder and rate of strain. These are determined through curve fitting the data gained from the test results.

In this method, the crack is placed along the cylindrical silicon die interface where the TSV and copper pass through, and the propagation of the crack is explained at different equally spaced positions in the interface. The critical region in the TSV is the interface of silicon and silicon di-oxide. Therefore, the crack is modeled in that interface as there were high chances of critical stresses to be developed in that area.

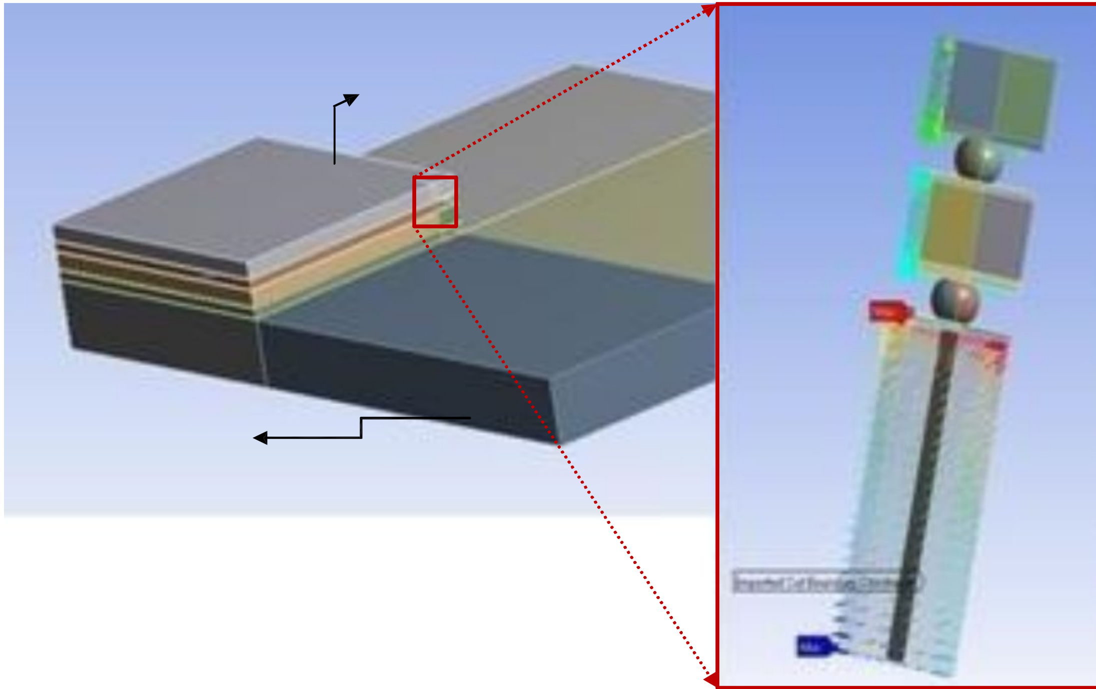

Figure 4-1 Global Model with Exploded Submodel

S. No.	Anand's Constant	Units	Value
1	s_0	Mpa	1.3
2	Q/R	1/K	9000
3	A	sec^{-1}	500
4	ξ	Dimensionless	7.1
5	m	Dimensionless	0.3
6	h_0	Mpa	5900
7	ŝ	Mpa	39.5
8	n	Dimensionless	0.03
9	a	Dimensionless	1.5

Table 4-1 Anand's Constants for SAC305 [6]

S. No.	Anand's	Units	Value
1	s	Mpa	0.15
2	$Q/\hat{R}$	1/K	9000
3	A	-1	500
4	ξ	Dimensionless	7.1
5	M	Dimensionless	0.3
6	h	Mpa	5900
7	$\hat{S}$	Mpa	3
8	N	Dimensionless	0.03
9	A	Dimensionless	1.5

Table 4-2 Anand's Constant for Effective Block in the Compact Model [6]

4.2. Method of Crack Formulation

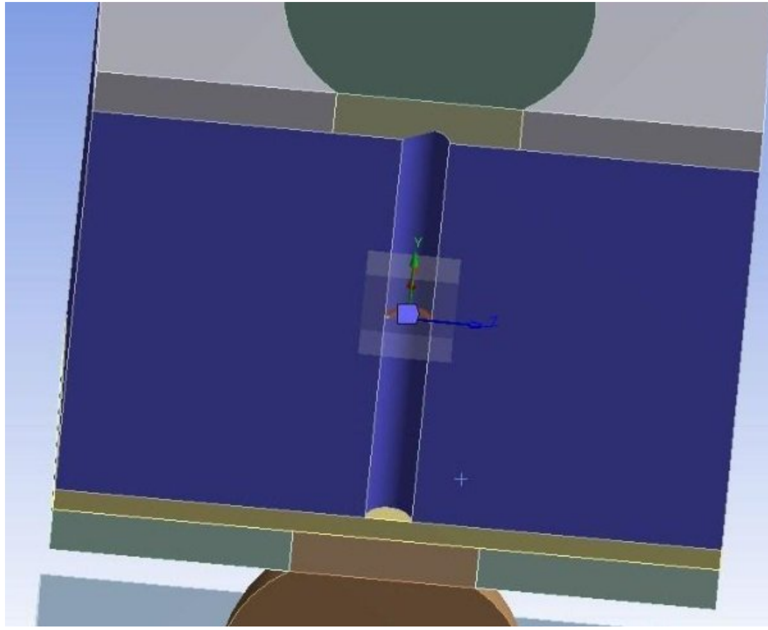

Figure 4-2 Crack formulation in the Silicon die at the mid-section of Sub model 2.

ANSYS 16 bundle is used to create, formulate and model the crack on the TSV Package. There are certain restrictions in ANYSYS 16 such as the crack model can be created only using tetrahedron mesh type and only semi-elliptical cracks can be designed. Therefore, first, the reflow conditions were applied to the global model and solved, followed by the sub-model 1 getting cut into two halves, and finally subjected to the original reflow conditions as a whole model. The sub-model 2, where the crack was placed, contains symmetrical half of sub-model 1, and then the reflow conditions were applied to it, with cut boundary confinements are imported and applied systematically from the sub-model 1.

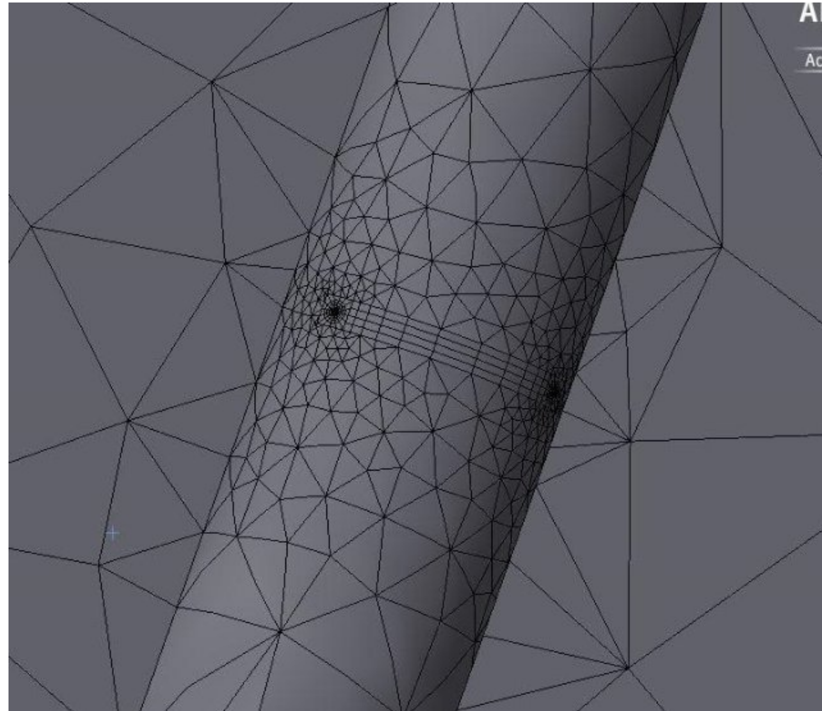

Figure 4-3 Crack Mesh in the Si/TSV interface of Silicon Die

Each simulation has been performed on the crack with equal distance of 9.5 μm in order to make 10 divisions that are equally placed apart in the total TSV length of 95μm. It takes 200°C to attach the 3D package to the substrate, so the thermal load of reflow condition is applied from 200°C to room temperature. The SIFs (K_1, K_2, K_3) and the J integral are calculated at different positions on the crack and at different modes, and the factors which alters the result are studied with the help of graphs. Using analysis it is figured out that which area will be more possible to experience one of the three types of cracking in the TSV. According to the linear elastic fracture mechanics, the condition in which the radial crack wont propagate is when, $K < K_C$, where K_C is the silicon's fracture toughness.

Chapter 5

Results and Discussion

5.1. Simulation and Validation

The analysis result shows that the normal stress (in Z direction in our case) is positive across the middle area of the silicon/copper interface. The stress distribution data is obtained after simulating under reflow conditions. The middle area of TSV is influenced to Mode 1 fracture, which is determined from the plot shown. The value K1 increases at the start and then decreases as it progresses and positive at the middle region. Crack on mode 2 is predominant on the top region of the interface. From the plot between K3 and the crack location, the top and bottom portions of the TSVs are more susceptible to mode 3 fractures, as the value of K3 is lower in the middle region.

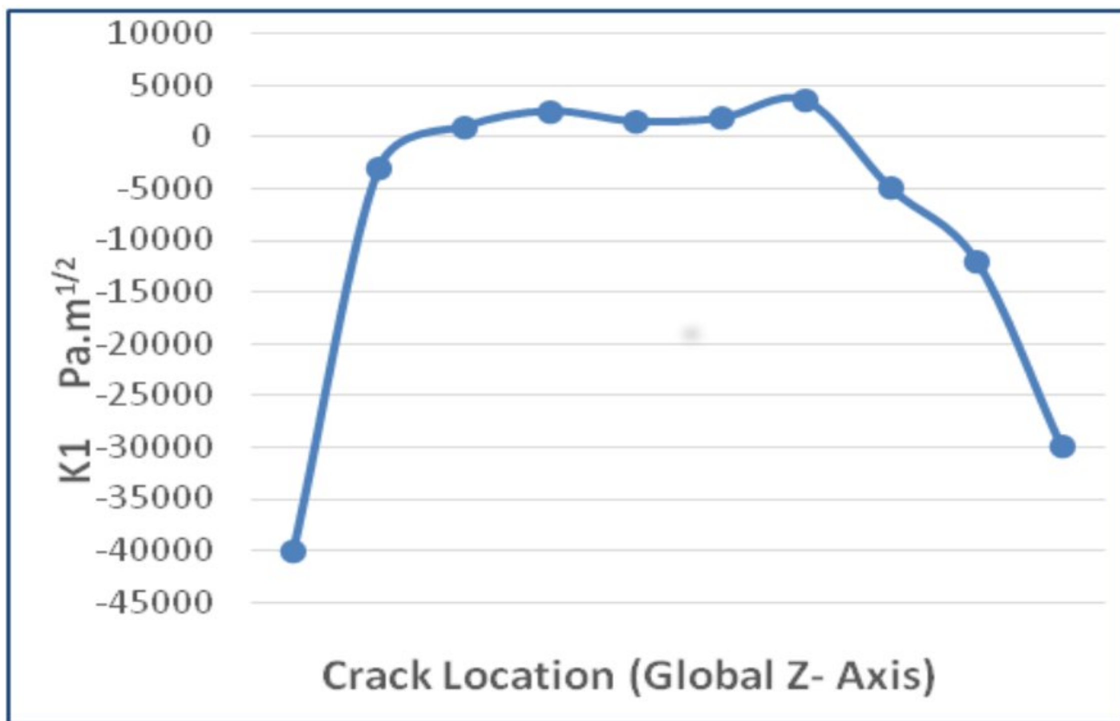

Figure 5-1 Stress Distribution at Silicon Die/Cu by K_1 Plot

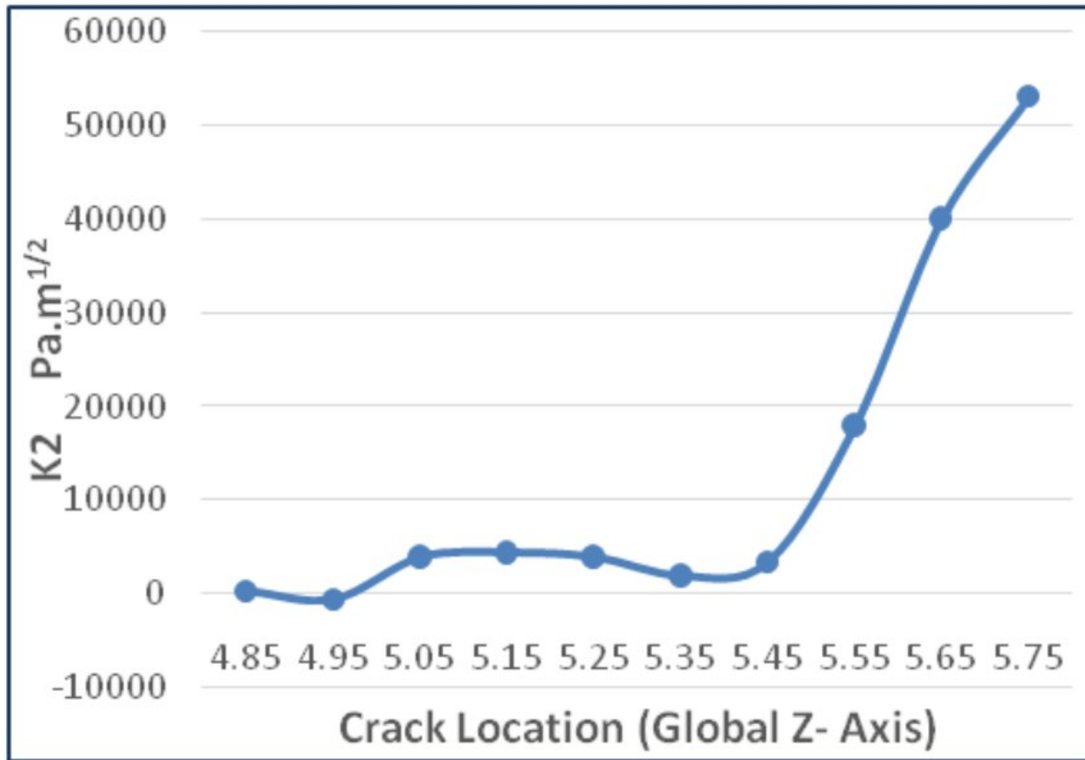

Figure 5-2 Stress Distribution at Silicon Die/Cu by K_2 plot

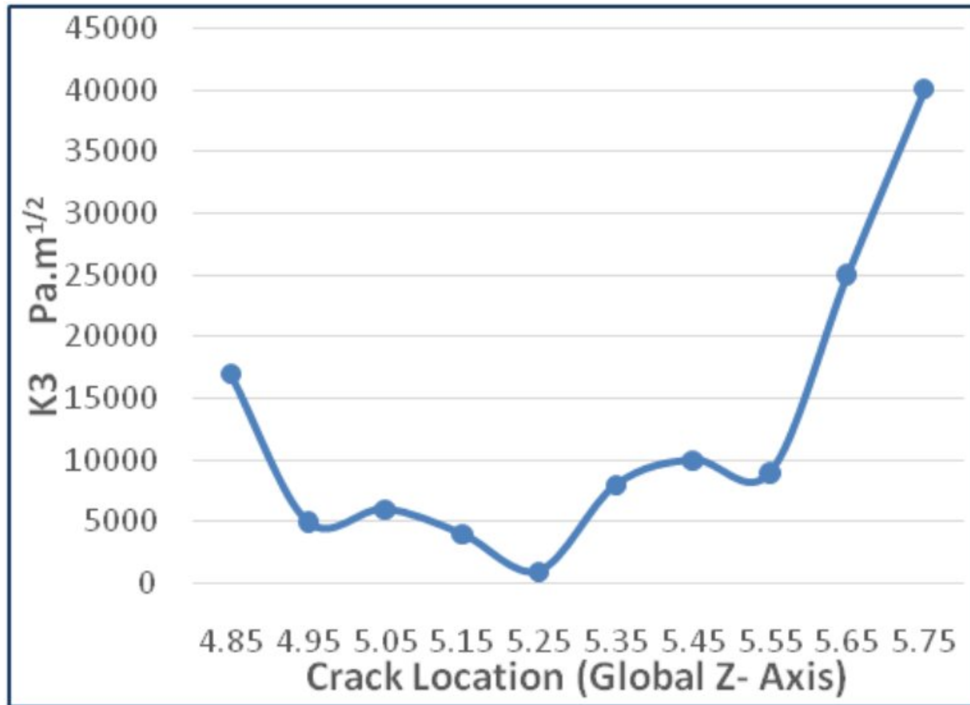

Figure 5-3 Stress Distribution at Silicon Die/Cu by K_3 plot

5.2. Relation between J-integral and different dimension parameter

The study of crack behavior with change in different dimensional parameter is done in this paper. This plot incorporate variation of J- integral with substrate thickness, die thickness, crack size and length of the crack. The analysis showed the significant change in J- integral values as die and substrate thickness increases and crack geometry changes.

The J- integral has indirect proportional relationship with substrate thickness that causes crack formation. The substrate thickness was varied from 0.2mm to 1mm with 0.2mm intervals and the corresponding J-integral value is noted. The data is plotted in graph and it has been observed that the value of J-integral decreases as the value of substrate thickness increases. After a certain limit the J-integral value starts to increase at a lower rate.

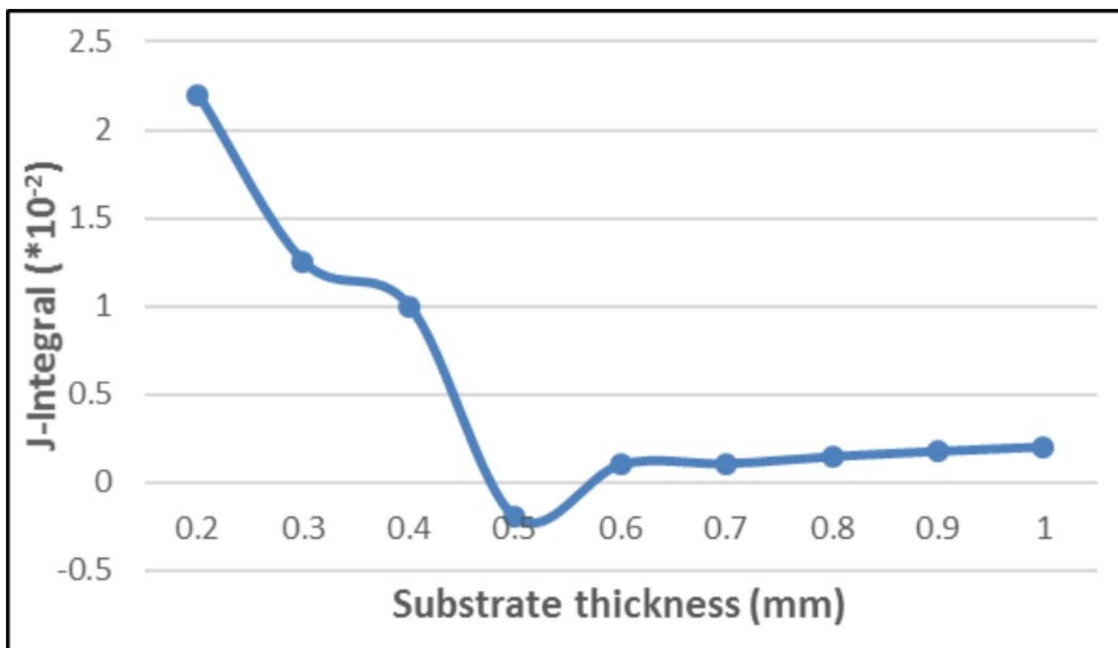

Figure 5-4 J-Integral vs substrate Thickness Plot

Similarly, the top die variation has been done by varying the thickness in equal increments of 0.1mm and the corresponding J- integral is noted. The value of J-Integral decreases drastically up to a certain limit and then remains the same even when the top die thickness increases.

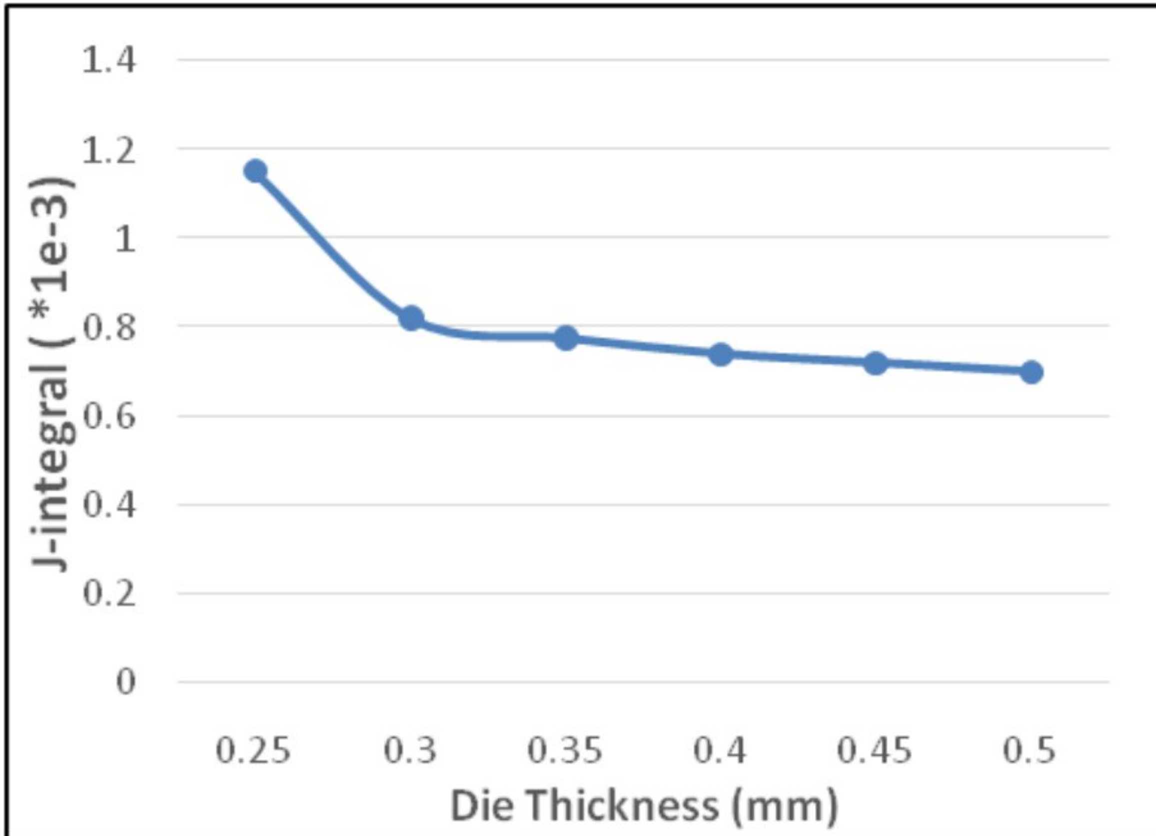

Figure 5-5 J-Integral vs Die thickness Plot

The crack size increase from 0.3 microns to 1.5 microns in the interval of 0.3 microns and the corresponding J- integral is noted and tabulated. The variation of J- integral with crack size is shown where the J-integral increases as the crack size increases.

Crack Size (E-07m)	J-integral (J/mm^2)
3	0.29643
6	0.37719
9	0.56732
12	0.83614
15	1.2012

Table 5-1 Variation of J integral with crack size

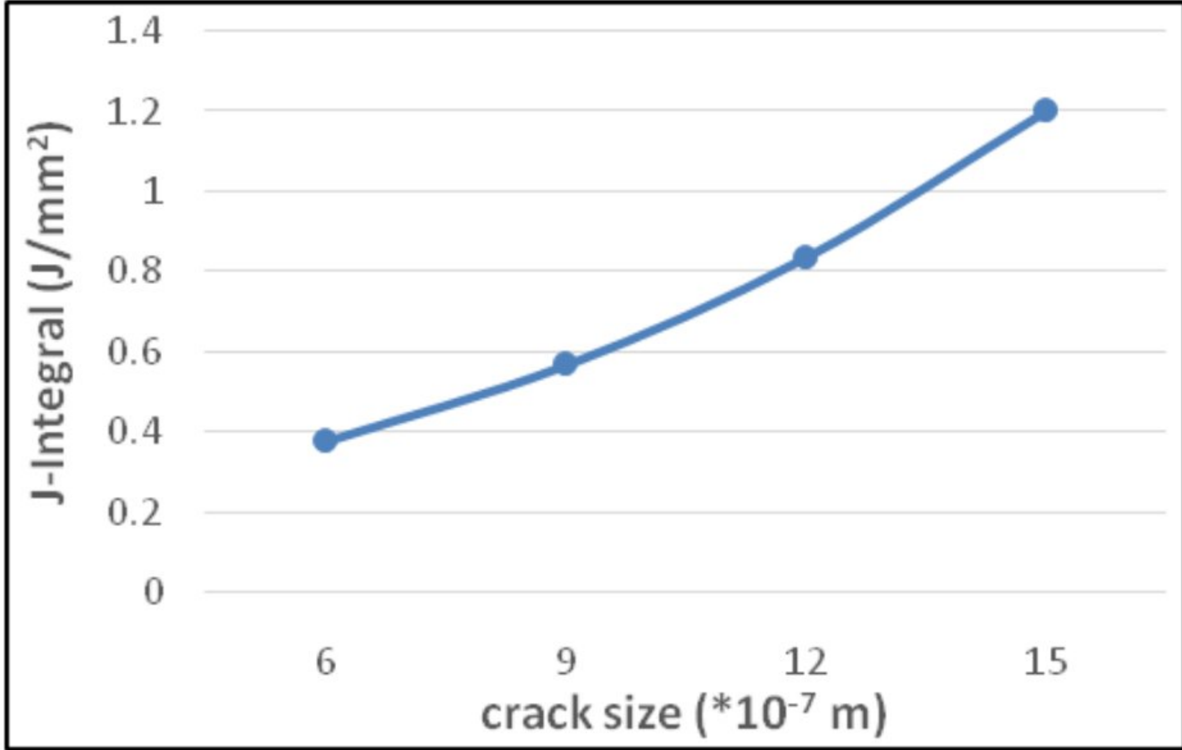

Figure 5-6 J-Integral vs Crack size plot

The radius of the crack is increased from 1 micron to 35 microns with 5 microns interval and the corresponding J-integral is noted. The variation of the values of J-integral with respect to length of crack is tabulated and the J-integral increases as the length of crack increases.

Length of the crack (microns)	J-integral (J/mm^2)	Increasing Percentage
1	.12303	
5	.38334	211.58%
10	0.90246	135.42%
15	1.2012	33.10%
20	1.5078	25.52%
25	1.8385	21.93%
30	2.0917	13.77%
35	2.3412	11.93%

Table 5-2 Variation of J integral with crack length

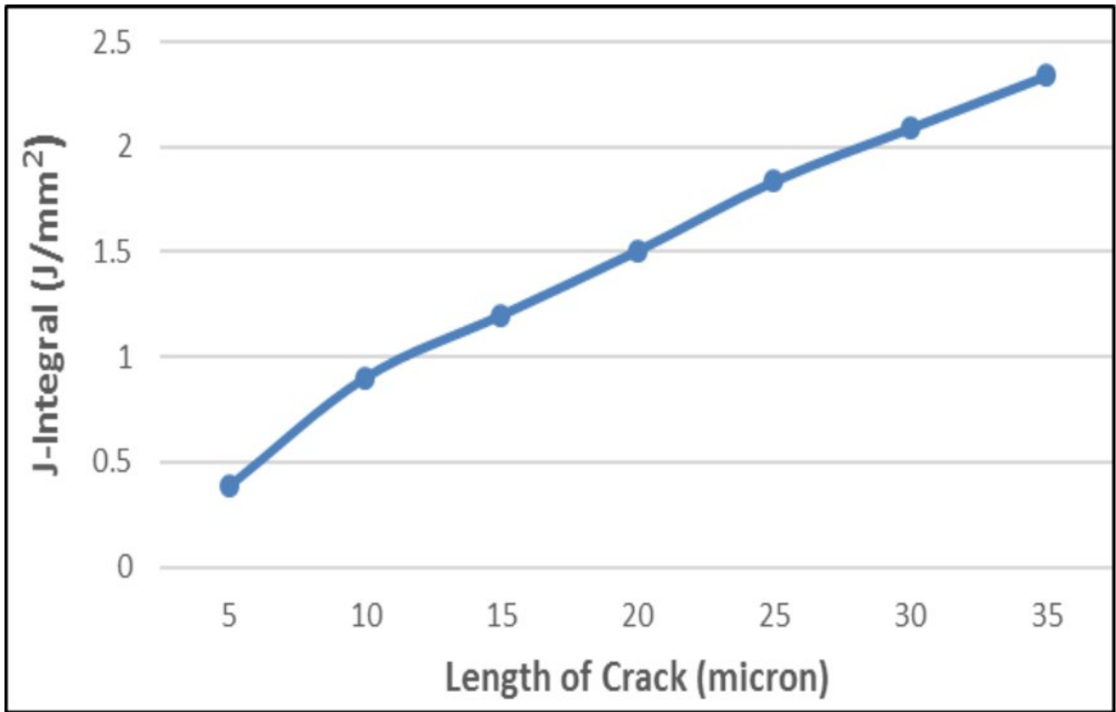

Figure 5-7 J-Integral Vs Crack length plot

Chapter 6

Conclusion

The variation of radial crack or crack propagation along the length of the silicon die has been successfully studied, through the TSV passage. The crack is modeled successfully and checked for different dimensions of crack. The cut boundary condition from the global model and sub model where used for simulation. The variation of J – integral value is used in calculating strain energy release rate per unit fracture surface and is determined with respect to crack size, die – substrate thickness and length of crack. The variation of crack length and size has also been successfully leveraged to investigate its effect on stress distribution and found that it is directly proportional to J-integral, whereas the relation between J-integral and die-substrate thickness shows an inversely proportional relational property up to certain limit of thickness.

All the results are in congruence with the hypothesis that "if the geometry of the crack increases with respective to the geometry of the model, then the J-integral value also increases".

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Author's Biography

Subramanian R Gowthaman has completed his Undergraduate degree in Mechanical Engineering from Anna University, Tamilnadu, India. He started pursuing his Master's degree in Mechanical Engineering at The University of Texas at Arlington in Spring 2014. He worked under Dr. Dereje Agonafer under the reliability team for electronic packages in the EMNSPC Lab (Electronics MEMS & Nano electronics Systems Packaging Center) from 2014 to 2016. He has also worked as a Design Engineer during his intern in Peak Energy Technology, Texas, USA to analyze and design a prototype for their company.