

SOLDER BALL RELIABILITY ASSESSMENT OF WAFER LEVEL CHIP SCALE
PACKAGE (WLCSP) THROUGH POWER CYCLING

by

BHAVNA CONJEEVARAM

Presented to the Faculty of the Graduate School of
The University of Texas at Arlington in Partial Fulfillment
of the Requirements
for the Degree of

MASTER OF SCIENCE IN MECHANICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

December 2016

Copyright © by Bhavna Conjeevaram 2016

All Rights Reserved



Acknowledgements

I would like to thank god for giving me the courage and wisdom to face all obstacles which came my way.

I thank my parents for giving me a bright life and motivating me throughout my journey.

I would like to thank Dr. Dereje Agonafer for believing in me and supporting me in all aspects of this journey. He was the best mentor who guided me through all difficulties with great optimism.

I show my sincere gratitude and respect to Dr. Haji Sheikh and Dr. Fahad Mirza for being panel members during my Thesis defense. I also thank Texas Instruments for providing the WLCSP boards.

I am grateful to Sally Thompson and Debi Barton for helping me with the paperwork throughout my degree plan.

Nothing would have been possible without the love and support of my EMNSPC team. It was a pleasure working with you all.

November 21, 2016

Abstract

SOLDER BALL RELIABILITY ASSESSMENT OF WAFER LEVEL CHIP SCALE PACKAGE (WLCSP) THROUGH POWER CYCLING

Bhavna Conjeevaram, MS

The University of Texas at Arlington, 2016

Supervising Professor: Dereje Agonafer

Failure analysis and its effects are major reliability concerns in electronic packaging. More accurate fatigue life prediction can be obtained after the consideration of all affecting loads on the electronic devices. When an electronic device is turned OFF and then turned ON multiple times, it creates a loading condition called Power Cycling. The die is the main heat source causing non-uniform temperature distribution. The solder ball reliability assessment of wafer level chip scale package (WLCSP) is done through computational methods such as Finite element analysis. WLCSPs use wafer level package technology which is an extension of the Wafer Fab process, where the final device is a die with an array pattern of the solder interconnects.

In this paper, the reliability of solder balls is determined by subjecting the board to Power Cycling and estimating the stress and failures. The mismatch in Coefficient of Thermal Expansion (CTE) between components used in WLCSP and the non-uniform temperature distribution between them, leads to the deformation of the package. Analysis is done on different thicknesses of the board to study its effect on reliability.

Table of Contents

Acknowledgements.....	iii
Abstract	iv
List of Illustrations	vii
List of Tables.....	viii
Chapter 1.....	9
1.1 Electronic Packaging	9
1.2 Classification of Packages.....	11
1.3 Wafer Level Chip Scale Package (WLCSP).....	12
1.4 Board Level Reliability	14
1.5 Power Cycling.....	18
1.6 Motivation and Objective	19
1.6.1 Motivation	19
1.6.2 Objective.....	21
Chapter 2	22
Chapter 3	25
3.1 Thermo Mechanical Analyzer:	27
3.2 Shimadzu Universal Testing Machine	31
3.3 Results of the Material Properties Obtained.....	33
Chapter 4	34
4.1 Introduction to FEA.....	34
4.2 Solving FE problems.	36
4.3 Considerations for Modelling.....	38
4.3.1 Considerations for Meshing.....	38

Chapter 5	39
5.1 Package Geometry	41
5.2 Anand's Viscoplastic Model	45
Chapter 6	47
6.1 Meshing	48
6.2 Boundary Conditions	50
Chapter 7	52
7.1 Temperature distribution	52
7.2 Stress distribution	54
7.2.1 Stress Distribution in 0.7mm board	54
7.2.2 Stress Distribution in 1mm board	55
7.2.3 Comparison of Maximum Equivalent Stress in two Boards	56
7.3 Directional Deformation	57
7.3.1 Directional Deformation in 0.7mm board	57
7.3.2 Directional Deformation in 1 mm board	59
7.3.3 Comparison of Directional Deformation of 0.7mm & 1mm boards	61
7.4 Plastic Work	62
7.4.1 Plastic Work in 0.7mm Board	62
7.4.2 Plastic Work in 1mm Board	62
7.5 Number of cycles to failure	64
Chapter 8	65
8.1 Conclusion	65
8.2 Future Work	66
References	67
Biographical Information	69

List of Illustrations

Figure 1-1 Moore's law	9
Figure 1-2 Microsystems Technologies.....	10
Figure 1-3 Classification of printed circuit boards.....	11
Figure 1-4 Wafer Level Chip Scale Package Cross Section.....	13
Figure 1-5 Wafer Level Chip Scale Package.....	13
Figure 1-6 Bathtub Curve.....	16
Figure 1-7 Board Cross-Section of 1mm WLCSP	20
Figure 2-1 Cross-Sectioned Sample in an Epoxy.....	24
Figure 2-2(a) Magnified image of 0.7mm board.....	24
Figure 2-2(b) Magnified image of 1mm board.....	24
Figure 3-1 TMA SS6000.....	27
Figure 3-2 Sample placement in TMA.....	28
Figure 3-3 TMA sample.....	29
Figure 3-4 CTE Measurement.....	30
Figure 3-5 Dog-bone sample of WLCSP.....	31
Figure 3-6 Shimadzu Testing Machine.....	32
Figure 5-1 Package Geometry of WLCSP.....	41
Figure 5-2 (a) and (b) Symmetry Boundary Conditions.....	43
Figure 6-1 Modelling Methodology.....	47
Figure 6-2(a) and (b) meshing of WLCSP.....	48
Figure 6-3 Quarter symmetry of WLCSP.....	49
Figure 6-4 Convective Boundary Condition.....	50

Figure 6-5 Internal Heat Generation on the die.....	51
Figure 6-6 Power cycling plot.....	51
Figure 7-1 (a) and (b) Temperature Distribution	52
Fig. 7-2 (a) (b) (c) Maximum Equivalent Stress Distribution 0.7mm board	54
Fig 7-3 (a) and (b) Maximum Equivalent Stress Distribution 1mm board.....	55
Figure 7-4 (a) (b) and (c) shows Directional Deformation of 0.7mm board.....	57
Figure 7-5 (a) (b) and (c) shows Directional Deformation of 1mm board.....	59
Figure 7-6 Plastic work in 0.7mm board.....	62
Figure 7-7 Plastic work in 0.7mm board.....	62

List of Tables

Table 1-1 Thermal environments for electronic products.....	15
Table 3-1 Dimensions of a dog bone sample.....	31
Table 3-2 Material Properties of WLCSP.....	33
Table 5-1 Dimensions of WLCSP.....	42
Table 5-2 Anand's constant.....	46
Plot 3-1 Young's Modulus Measurement.....	32
Plot 7-1 Temperature Distribution Plot.....	53
Plot 7-2 Max Equivalent stress in 0.7mm and 1mm board.....	56
Plot 7-3 Comparison of Directional Deformation in all directions.....	61
Plot 7-4 change in plastic work(ΔW).....	63
Plot 7-5 Plastic work at the end of third cycle.....	63
Plot 7-6 Number of Cycles to Failure of 0.7mm board and 1mm board.....	64

Chapter 1

INTRODUCTION

1.1 Electronic Packaging

Scientific development and progress has made a huge leap in the recent years. Microelectronics has been a quintessential element in this progress. It has a great influence in our mundane life. From common devices like MP3 players to complicated objects like satellites depend on Microelectronics.

According to Moore's law, "The number of transistors will double every 18 months". It is because of this law that Microprocessor industry has shown such exponential growth over the past few decades. [1]

Fig. 1-1 shows an example for Moore's law for different processors.

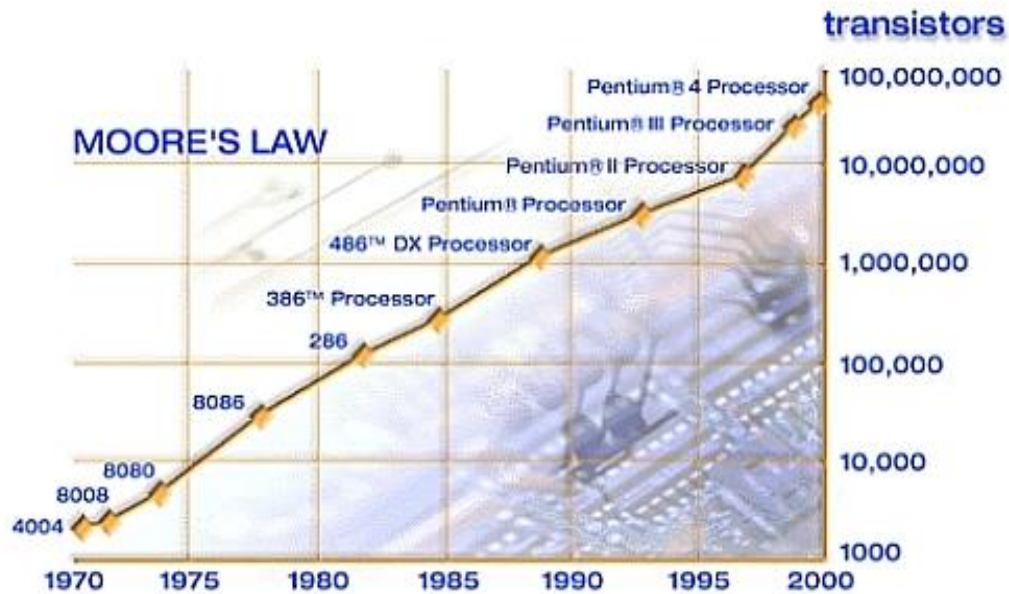


Figure 1-1 Moore's law [1a]

Electronic packaging is the backbone for all electronic equipment like personal computers, laptops, mobile phones, industrial robots, air conditioners, television and medical equipment.

Major components of electronic packages include integrated circuit chips, flat-panel, cathode-ray tube displays, loud speakers, diodes and so on. These components are interconnected with electric power supply and are assembled together in packaging. [2]

Due to the rapid improvement in technology, packaging has shown a tremendous growth posing great advantages in the industry. The key to success in such competitive and continuously changing market depends mainly on two important factors:

- Performance
- Cost

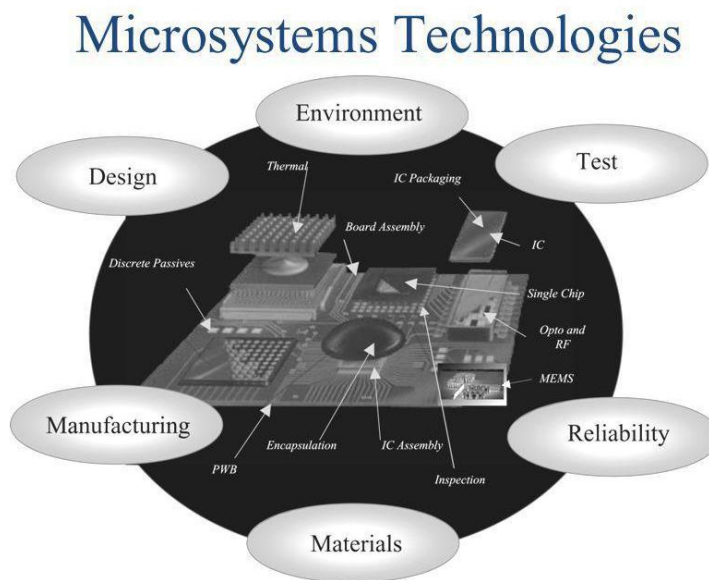


Figure 1-2 Microsystems Technologies [1b]

Fig. 1-2 explains Microsystems Technologies and the factors that affect it.

1.2 Classification of Packages

There is a high competition and pressure in the industry to make life easier for individuals. This can be attained by challenging the traditional methods and bringing out different types of packages which meet the requirement of the customers.

There are different types of PCB's which are classified on the basis of material, wiring, rigidity, additives, structure and its manufacturing process. [3]. Fig. 1-3 shows the classification of PCB's.

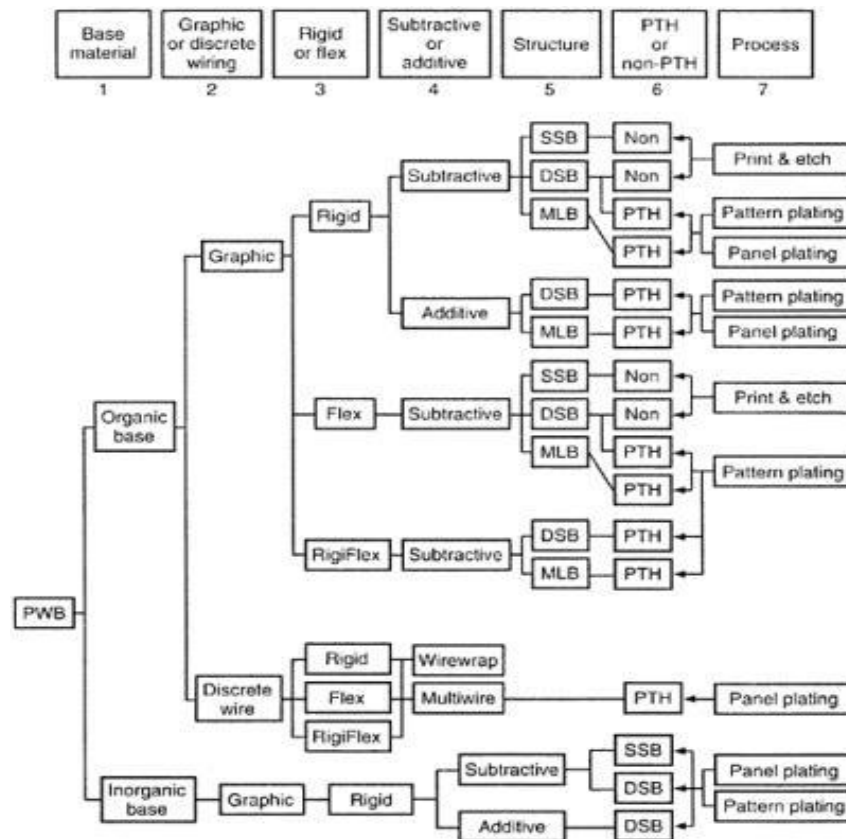


Figure 1-3 Classification of printed circuit boards [3]

1.3 Wafer Level Chip Scale Package (WLCSP)

Wafer level chip scale package is packaging an integrated circuit at wafer level instead of assembling different components at a later stage. The size of the package is approximately the same as that of the die. [4] WLCSP has minimized production time and usage of materials which in turn reduces the total cost of manufacturing. The different advantages of WLCSP include:

- Small form factor
- High efficiency
- No usage of underfills
- Less expensive [5]

From Paek, Jong Sik, et al "Wafer level Chip Scale Package", Wafer level package consists of a semiconductor die which connects a substrate electrically, an encapsulant and a solder ball mounted on the external apparatus. A method for producing the wafer level package consists the operations of bonding a substrate having a number of wiring patterns formed thereon to a wafer while electrically connecting each semiconductor die of the wafer to each unit of the substrate, forming a solder ball on a side of the substrate, encapsulating each semiconductor die of the wafer and the substrate, and sawing the semiconductor die and the substrate together from the wafer into a separate package. [6]

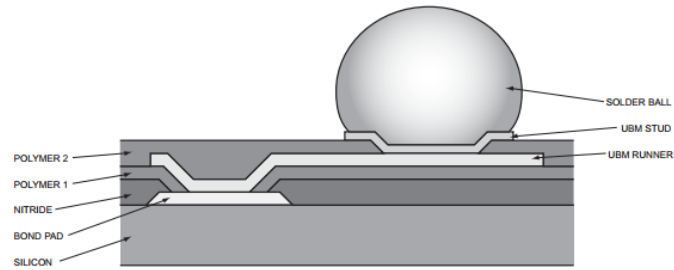


Figure 1-4 Wafer Level Chip Scale Package Cross Section [1c]

Fig. 1-4 show the cross section of WLCSP. The solder used in the package is SAC396.

Paek, Jong Sik, et al state that “Such a conventional wafer level package and a method for manufacturing the same have a problem in that only one semiconductor die is positioned on a package and the memory capacity or functions cannot be improved dramatically.”

A typical Wafer Level Chip Scale Package as shown in Fig. 1-5 uses a high cost substrate which in turn increases the production cost. Also, the semiconductor die and the substrate should be accurately aligned with respect to each other during production to acquire a strong bond with an adhesive. This is a tedious process and makes it complicated. [6]

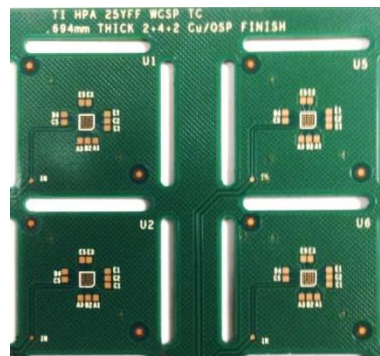


Figure 1-5 Wafer Level Chip Scale Package

1.4 Board Level Reliability

When a system or a component performs as per its requirements and fulfils all the checklists, it is said to be reliable. Most products have a definite lifespan, but they all come with a probability of failure and this is true for IC's as well.

Reliability estimation is based on environmental stresses, which can be simulated to test the working conditions of the said item and unravel the specific materials and process related marginalities that may be experienced during operational life.

Stress is not only restricted to temperature changes but can be of different types depending on the environmental conditions, geometry, reversibility, material properties etc. The severity of stress levels varies considerably. Different types of stresses include:

- Temperature
 - a) Constant
 - b) Varying
 - c) Shock
- Humidity
 - a) Noncondensing
 - b) Condensing
- Mechanical stresses
 - a) Shock/drop
 - b) Vibration
 - c) Bend
 - d) Torque

- Corrosive gases
- Dust
- Radiation
- Pressure
- Electrical [7]

Table 1-1 shows different Thermal environments to which the electronic products are exposed.

Use condition	Thermal excursion (°C)
Consumer electronics	0 to 60
Telecommunications	-40 to 85
Commercial aircraft	-55 to 95
Military aircraft	-55 to 125
Space	-40 to 85
Automotive-passenger	-55 to 65
Automotive-under the hood	-55 to 160

Table 1-1 Thermal environments for electronic products [5]

Reliability is usually represented graphically by specialists using a bathtub curve as shown in Fig. 1-6. Bathtub curve consists of three phases:

- An infant mortality phase (Usual life)
- Useful life
- Failures due to wear out

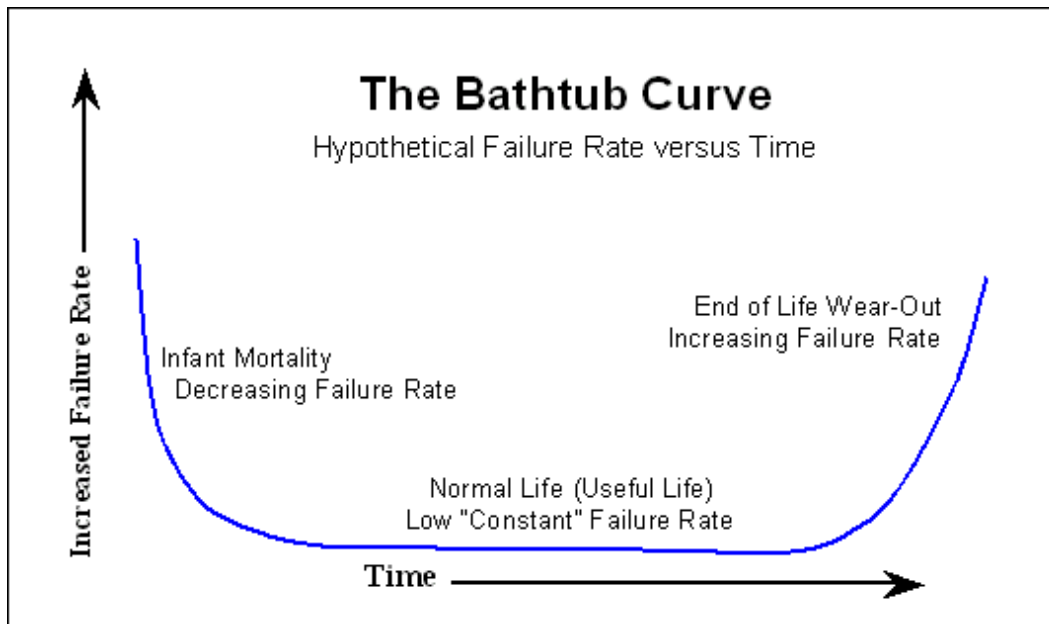


Figure 1-6 Bathtub Curve [1d]

The failures during the first phase are due to defects in manufacturing and assembly. Failure rate in the second phase is constant. Products fail as poor parts are screened out and removed from the system. The remaining parts fail in the last stage due to wear-out. In this phase, thermal and mechanical stresses cause permanent defects in the product. [8]

Few consortiums such as Joint Electronic Device Engineering Council (JEDEC) and Institute for Printed Circuits (IPC) have adapted, documented and standardized many of the reliability tests.

These tests come in two flavors – package level and board level. Package levels are directed to test the robustness of the device to deal with environmental conditions paying no consideration to interconnects when mounted on a board. Whereas for the board level or 2nd level reliability tests, stresses are examined on the solder joint of the surface mount package when mounted on board. [9]

1.5 Power Cycling

When a device is switched on and switched off several number of times, stresses are induced in the system. This loading condition is called Power Cycling.

Fatigue is the major factor affecting failure of solder interconnects and prolonging its life is the major concern for package designers and consumers. Generally, fatigue life is approximated by using accelerated thermal cycling (ATC) with hundreds of parts.

Various numerical integration tools like Finite Element Analysis are used for virtual qualification in an attempt to reduce development time and expenses. ATC conditions assume that the temperature is uniform throughout the assembly for predicting the life of the module.

However, in practical conditions the assembly is subjected to power cycles which results in temperature being non uniform throughout assembly as the die is the only source of heat generation. The difference in coefficient of thermal expansion between components results in the deformation of the package. This deformation is different when the package is subjected to Accelerated Thermal Cycling (ATC). [10]

1.6 Motivation and Objective

1.6.1 Motivation

Reliability of the package plays an important role in the field of Electronic Packaging. Every product has a particular life span and is subjected to various stresses under different environmental condition.

Reliability of a product or its life span is usually determined using Accelerated Thermal Cycling (ATC). This method is considered to be a traditional and conservative. Accelerated Thermal Cycling (ATC) is conducted with the assumption of uniform temperature distribution throughout the assembly.

However, in practical scenario, the package undergoes Power Cycling which consists of non-uniform temperature distribution throughout the assembly. The mismatch in Coefficient of Thermal Expansion (CTE) causes the package to deform. [10]

Literature review suggests that thicker boards fail faster. Reliability is inversely proportional to thickness. Thickness plays a huge role determining the reliability of the package. Thinner board on the other hand is more flexible and takes a longer period to fail when compared to the thicker board. [11]

Two Wafer Level Chip Scale Package (WLCSP) boards of 1mm and 0.7mm were subjected to Power Cycling. However, 0.7mm board failed faster under Power Cycling.

Fig. 1-7 shows the Board Cross-Section of 1mm Wafer Level Chip Scale Package.

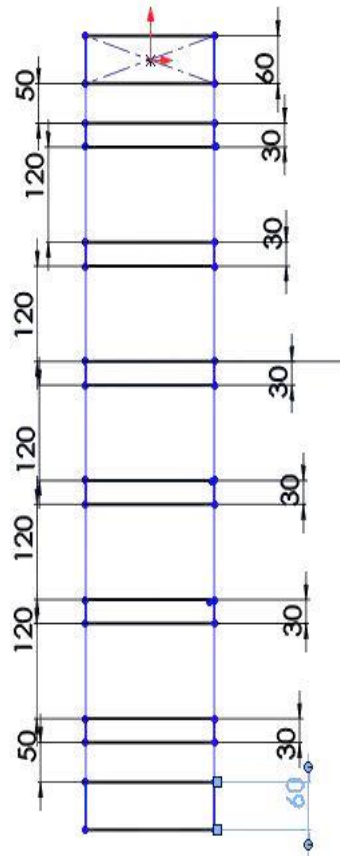


Figure 1-7 Board Cross-Section of 1mm WLCSP

1.6.2 Objective

Literature review states that thicker boards fail faster and it accounts for a major portion in Reliability. Following this, simulations were carried out using Finite Element Analysis (FEA) on boards with different thicknesses.

Fascinating enough, it was found that the results from the simulations were contradicting the above mentioned review. Hence, further study was necessary to determine factors accounting to reliability to get clarity.

The main objective was to analyze, determine and compare the number of cycles to failure of Wafer Level Chip Scale Packages (WLCSP) under Power Cycling. The comparison was carried out using two WLCSP with thickness of 0.7mm and 1mm. FEA simulations on the two boards were done to identify the critical solder joints and the root cause of their failure was determined.

Plastic Work also plays a major role in determining the number of cycles to failure. Thus, Plastic work, Equivalent (Von-Mises) stress and Directional Deformation in x-direction, y-direction and z-direction were also obtained to further quantify their effect on reliability.

Summarizing, it is evident that not one single factor alone affects the reliability. Hence, the determination and study of these variables was the key to figuring out what factors solely play major role in determining the reliability of WLCSP under power cycling.

Chapter 2

LITERATURE REVIEW

Advancement in Technology has led to Electronic packages production with an extensive emphasis on economy, performance, size and reliability. Efforts have been made to develop packages with high reliability under power cycling. But sadly, the research done on power cycling as opposed to thermal cycling modeling is very limited.

Work done based on solder joint reliability and power cycling can be summarized as follows: Darveaux [12] (2000) worked on the Effect of simulation methodology on solder joint crack growth correlation. Ahmed, Izhar Z and S. B. Park [10] (2004) published “An accurate assessment of interconnect fatigue life through power cycling”.

DEH Popp, A Mawer, G Presas [13] (2005) published “Flip chip PBGA solder joint reliability: Power Cycling versus Thermal Cycling”. In this paper, he has explained the design of a power cycling system. He determined the reliability of a flip chip plastic ball grid array (FC PBGA) by subjecting it to power cycling and thermal cycling. On comparison, the solder life oh FC BGA was 45% longer in power cycling. In thermal cycling, solder joint failure occurs in the center due to package flexing and in power cycling, solder joint failure occur along the die edge. [13]

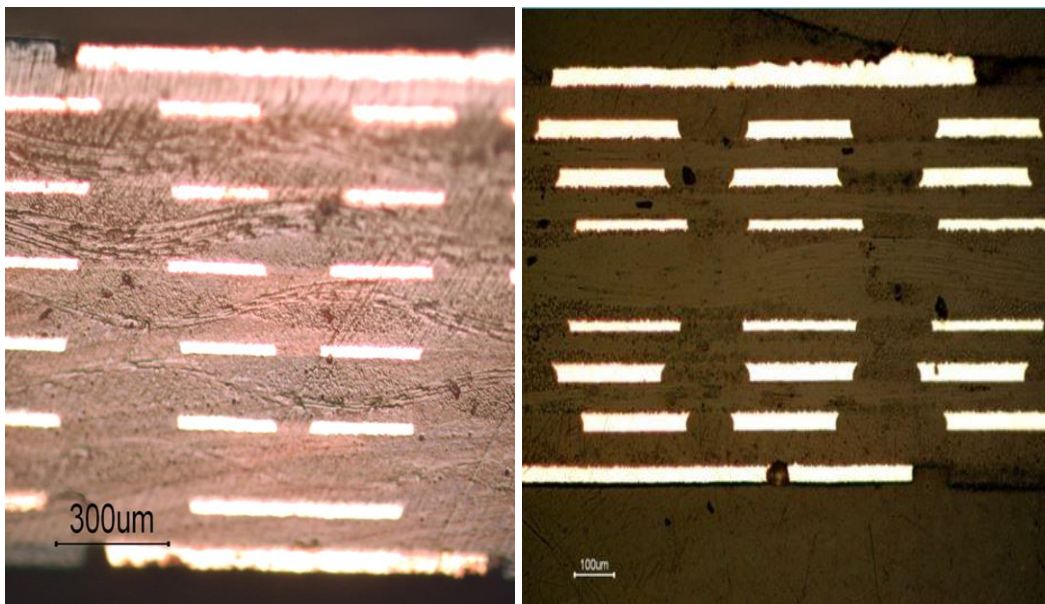
Park, S.B., and Izhar Z Ahmed later published “Shorter field life in power cycling for organic packages” (2007) [14]. They stated that “Higher substrate CTE in a plastic package generates double curvature in the package deformation and transfers higher stresses to the solder interconnects at the end of die. This mechanism makes the solder interconnects near the end of die edge fail earlier than those of the highest distance to neutral point. This phenomenon makes the interconnect fail earlier in power cycling than ATC.”

They proposed a proper analysis procedure for power cycling to predict the solder life. They made an effort to show that FC-PBGA had the possibility of shorter solder life in power cycling than ATC. Transient heat transfer coefficients were obtained by conducting Computational Fluid Dynamics (CFD) analysis while the temperature distribution and strain energy density were obtained from FEA-thermal and FEA structural analysis respectively. [14]

Hassaan Ahmad [8] conducted a detailed study of the board by placing a cross-sectioned sample in an epoxy which was left to solidify. The sample was under a 10x magnification lens to study the layers of the board. Fig. 2-1 shows the Cross-sectioned sample of WLCSP.



Figure 2-1 Cross-Sectioned Sample in an Epoxy



(a)

(b)

Figure 2-2 shows magnified image of the layers of the board. It shows (a) is a 1mm board (more FR4/Vol. of the board) and (b) is a 0.7mm board (more Cu/Vol. of board) [8]

Chapter 3

MATERIAL CHARACTERIZATION

Material Properties or characteristics, becomes an important aspect in determining the fatigue correlation parameters using Finite Element Analysis. By providing actual material properties for each material we can get accuracy in our results. The apparatus that were used to determine the material properties were:

- Thermo-Mechanical Analyzer (TMA)
- Shimadzu Universal Testing Machine

The following material properties were considered to characterize the WLCSPs that were used in the study:

- Young's Modulus.
- Co-efficient of Thermal Expansion (CTE).

The Coefficient of thermal Expansion in all the three directions was obtained using the Thermo-Mechanical Analyzer. Young's Modulus (E_{xy}) was obtained using Shimadzu Testing Machine.

Understanding of Young's Modulus and Coefficient of Thermal Expansion (CTE) as stated is very essential. The definitions of the same are as follows:

Young's Modulus (E):

The ratio of stress to strain of a material gives the Young's Modulus of that material.

Young's Modulus is basically an elastic property of the material.

Mathematically,

$$E = \frac{\sigma}{\varepsilon}$$

Where,

E – Young's Modulus (N/mm²)

σ – Stress (N/mm²)

ε – Strain

Coefficient of Thermal Expansion (CTE):

The change in volume or length of a material over a unit change in temperature is the Coefficient of Thermal Expansion (CTE). This gives us the Linear Thermal expansion per degree Celsius or Fahrenheit of the material. It is obtained as a ratio of strain at room temperature over the change in Temperature.

Mathematically,

$$\alpha = \frac{\varepsilon}{\Delta T}$$

Where,

α – Coefficient of Thermal Expansion (CTE) (ppm/°C)

ε – Strain (mm/mm)

ΔT – Change in Temperature (°C). [5]

A brief description of the apparatus, equipment and methods that were used in the study of the above mentioned properties:

3.1 Thermo Mechanical Analyzer:



Figure 3-1 TMA SS6000

Abbreviated as TMA, TMA measurements record changes caused by changes in the free volume of a polymer. TMA as shown in fig. 3-1 has the capability to measure from single fiber to stiff bulk compositions. This attribute gives an advantage to test and

measure great number of materials. It has high resolution and accuracy which helps in the measurement of samples with low expansion. [15]

The TMA consists of a probe which measures displacement, a motor to control a probe, an LVDT and a sample cylinder made of quartz. The force generated by the motor is transferred to the sample with help of the probe as shown in fig.3-2. When the sample expands, the probe moves and the displacement is measured by the LVDT which is placed on the top. TMA/SS6000 in specific was used to obtain the CTE.



Figure 3-2 Sample placement in TMA

The sample on the TMA is small as shown in fig. 3-3. The maximum permissible length of the sample is 20mm with diameter of 8mm. Due to smaller thickness of the sample; the length was taken as 10-12 mm to avoid bulking effect. High speed cutters

should not be used during the preparation of the sample as it would leave a heat residual. This heat residual might interfere in the measurement of CTE and might result in errors.



Figure 3-3 TMA sample

The TMA contains an analytical train which provides the access for an accurate measurement of position and it can be calibrated to known standards. The square sample used is $8 \times 8 \text{ mm}^2$. The sample is placed in the quartz cylinder. Quartz Fixtures are used to hold the sample during the test. Quartz has low CTE. To measure the CTE in z-direction, the sample was placed on its thickness. To measure CTE in xy-direction, the sample was placed along its length. A constant load of 100mN was applied. Ramp input is $5^\circ\text{C}/\text{min}$. Temperature difference is given from room temperature to 170°C . CTE measurement data is provided below.

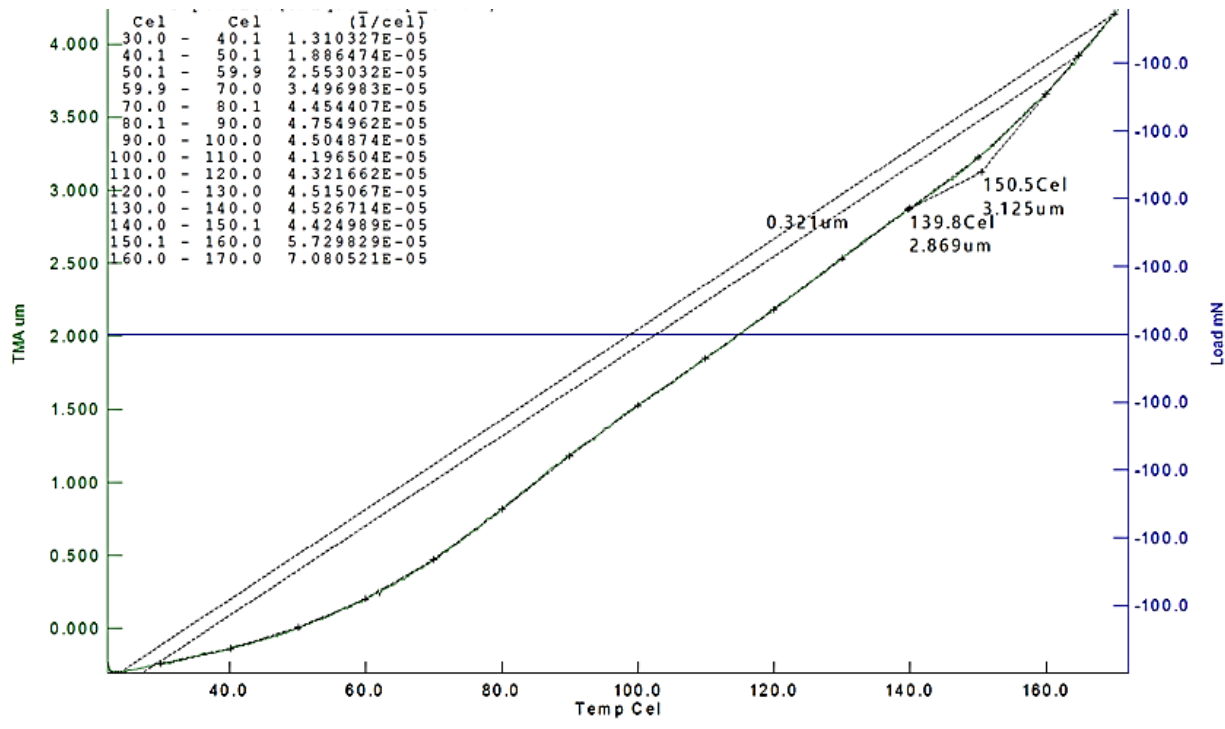


Figure 3-4 CTE Measurement

Fig. 3-4 shows the values obtained for Coefficient of Thermal Expansion using Thermo Mechanical Analyzer.

3.2 Shimadzu Universal Testing Machine

Sample used to measure Young's Modulus is in the shape of a dog bone as shown in fig.3-5 in order to create necking in the reduced section. There is a curvature between two sections to avoid stress concentration. The dimensions were chosen according to ASTM standards. Samples have to be properly aligned to avoid errors. The dimensions of the sample are given below in Table 3-1.

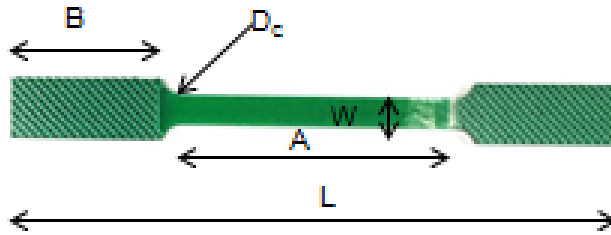


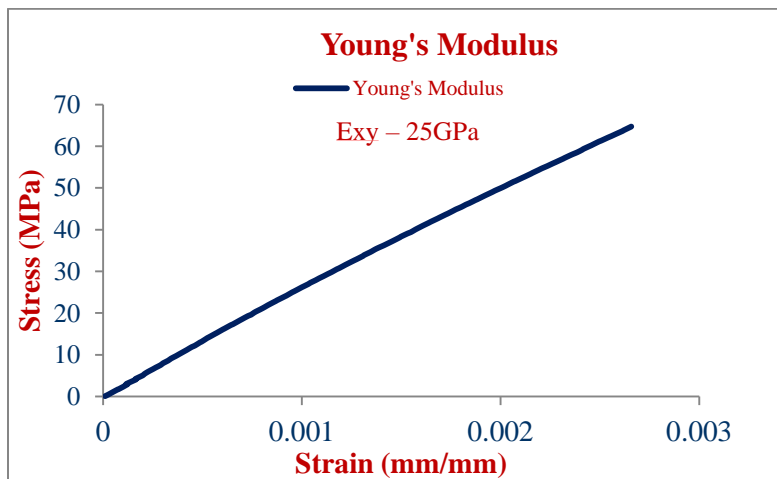
Figure 3-5 Dog-bone sample of WLCSP

Dimensions	Length(mm)
L	100
W	6
A	32
B	30
D _c	4

Table 3-1 Dimensions of a dog bone sample



Figure 3-6 Shimadzu Testing Machine



Plot 3-1 Young's Modulus Measurement

Shimadzu Machine as shown in Fig.3-6 is an AGS-X series machine which uses Trapezium software. This software was used to measure Young's Modulus of the sample as shown in Plot 3-1. The dog-bone sample was placed inside the jaws. A force of 2N/m was applied on the sample.

3.3 Results of the Material Properties Obtained

The following material properties were determined.

Boards	CTE (ppm/°C)			Young's Modulus E (GPa)
	x-dir	y-dir	z-dir	
1mm	20	20	60	25
0.7mm	23	23	50.5	30

Table 3-2 Material Properties of WLCSP.

Table 3-2 shows the material properties obtained for WLCSP using the Thermo Mechanical Analyzer and Shimadzu Testing Machine.

Chapter 4

FINITE ELEMENT ANALYSIS

4.1 Introduction to FEA

History is a testament to many instances where discretization has solved many complex problems. If you discretized a circle with polygons of many sides, you get a very accurate value of π , which has seen many applications and even philosophical discussions in popular cultures. This concept has met with open arms in many engineering applications.[16]

Mechanics itself is characterized by its branches being: Theoretical, Applied, Computational and Experimental. The Finite Element Methods are shelved under the computational branch. FEA are used to applications like:

- Aerospace
- Automotive
- Bio-mechanics
- Nuclear Engineering
- Mechanical/Civil

By taking a system as a whole, it's always hard to analyze it and solve its complexity. If we discretize it, reduce it to its elements connected by nodes, it is possible to solve many problems. FEA helps us solve these issues in a more simplified manner than brute force practical methods. These processes provide an approximate method of solving problems. [17]

Local equilibrium is established at the nodes and the unknown displacements are solved solving these equations. The general equation for solving the unknowns is

$$\{F\} = [K] \{u\}$$

Where,

$\{F\}$ = Forces at the nodes

$[K]$ = stiffness matrix

$\{u\}$ = Displacement at the nodes

The only unknowns are displacements due to the fact that the forces are externally applied. The stiffness are dependent on the geometry and the materials used. The displacements are determined at the nodes and meshes are generated to increase the number of nodes. So finer the meshes, higher the accuracy, which also invariably means that the computational time is considerably more. [5]

4.2 Solving FE problems.

- Determine the element properties from the geometric and loading data.
- Assemble all equations. All the non-zero coefficients in the matrix can be grouped together in a band. This eliminates usage of large space while computing.
- The third step is to provide all boundary conditions.
- Use many different methods to solve the equations. [18]

For most applications, we use a general purpose software called ANSYS. The objectives, physical systems and mesh are some of the considerations that must be made before the usage of ANSYS.

- Type of Problem
- Time Dependence
- Nonlinearity
- Modeling simplifications

From the analytical standpoint, this is a structural analysis where the stress/strain, deformations are determined of a solid body.

Evaluated quantities include:

- Displacement
- Stress
- Strain
- Reaction Forces

Degree of Freedom (DOF) or the unknown is the displacement. Many structural problems find themselves home to the moniker of static analysis.

The loads that are applied and the conditions of support are time invariant in nature. Non-linear material and geometrical properties like creep, plasticity are also in availability.

There are many non-linear properties defined in ANSYS. They are:

- Plasticity: Permanent deformation but not time dependent
- Creep: Permanent deformation but time dependent
- Viscoelasticity: Non-permanent deformation but time dependent [19]

4.3 Considerations for Modelling

The minor details that affect and influence the results should not be simulated. For symmetric conditions, it is better to take a portion like half, quarter or quadrant models. This technique saves some time during simulations.

There is no way around the symmetry condition requirements.

- Geometry
- Material Properties
- Loading
- Degree of Freedom

4.3.1 Considerations for Meshing

It is a well-known fact that finer meshes offer better approximations. But in some cases, finer meshes can cause errors. It's more to do with context and situations. Some regions may need coarse mesh and some regions may need fine mesh. However, there are some techniques that can be applied to have a better understanding of the mesh. They are:

- Adaptive Meshing
- Mesh Refinement Test within ANSYS
- Sub-Modeling [19]

Chapter 5

WLCSP MODELLING AND SIMULATION

The basic goal of computations is to analyze how the system responds to the imposed conditions. The solutions obtained can then be used to make engineering decisions in real life. The computations also transform one form of data to another form which satisfies the need of the decision making process. [16]

When the system involves complicated geometry, material properties and loadings, mathematical approach cannot be used. Hence, numerical methods like Finite Element method come to the rescue. This process involves modelling a body by dividing it into equivalent number of smaller bodies which are known as finite elements. These finite elements are interconnected at points connected to two or more elements which are known as nodes.

Finite Element Method works on the principle of formulating equations for each finite element and combines them to obtain the solution for the whole body instead of solving for the whole body in one operation. [17]

Finite Element Analysis consists of three steps:

- Preprocessing:
 - a) A geometric model is created according to the requirements
 - b) The body is divided into finite elements and meshing is done
 - c) The material properties of the body are assigned.

- Solution
 - a) The body is subjected to appropriate loads and the boundary conditions are given.
 - b) Output control and load step control are selected
 - c) Solver is selected
 - d) Desired solution is obtained
- Post Processing
 - a) The results are reviewed and used to make engineering decisions.

Assumptions:

- All materials are considered as linear elastic except solder
- PCB is considered as orthotropic
- Solder is modeled as rate-dependent viscoplastic material using Anand's viscoplastic model

5.1 Package Geometry

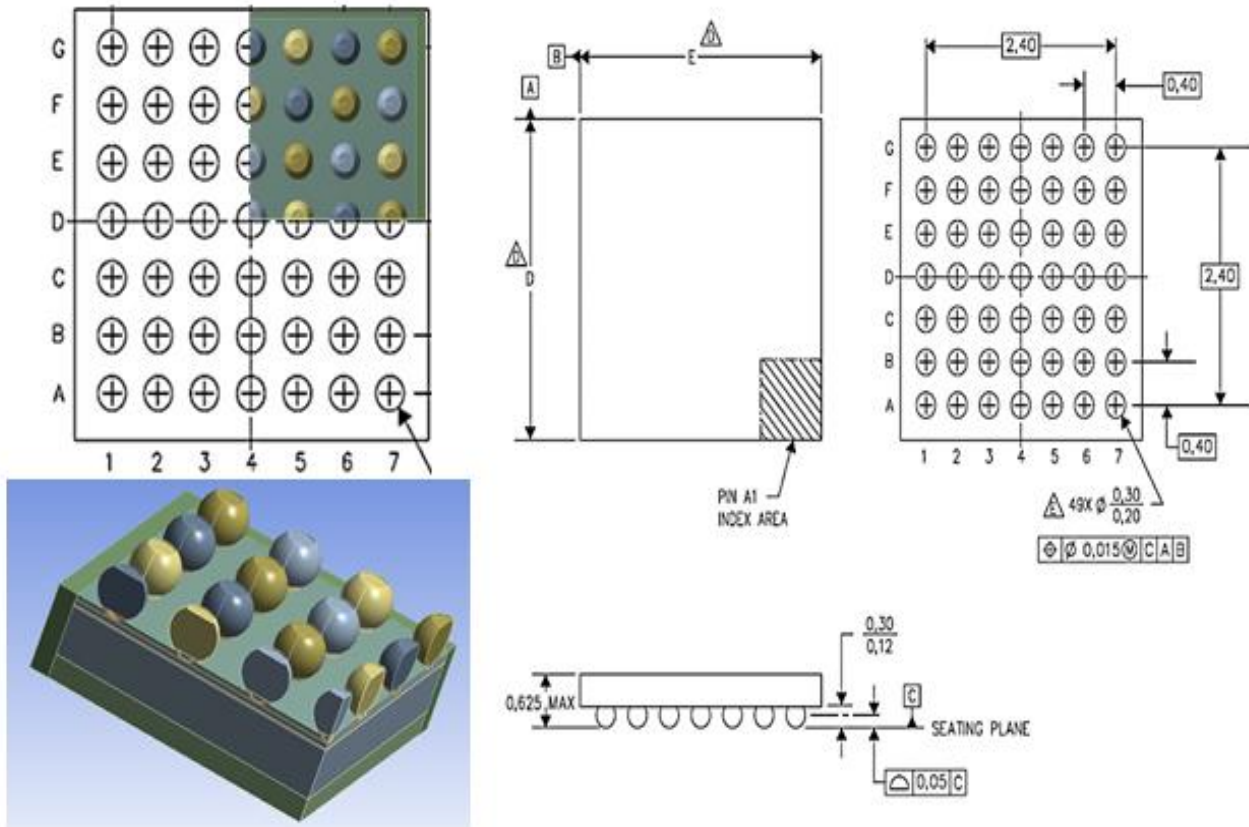


Figure 5-1 Package Geometry of WLCSP[5]

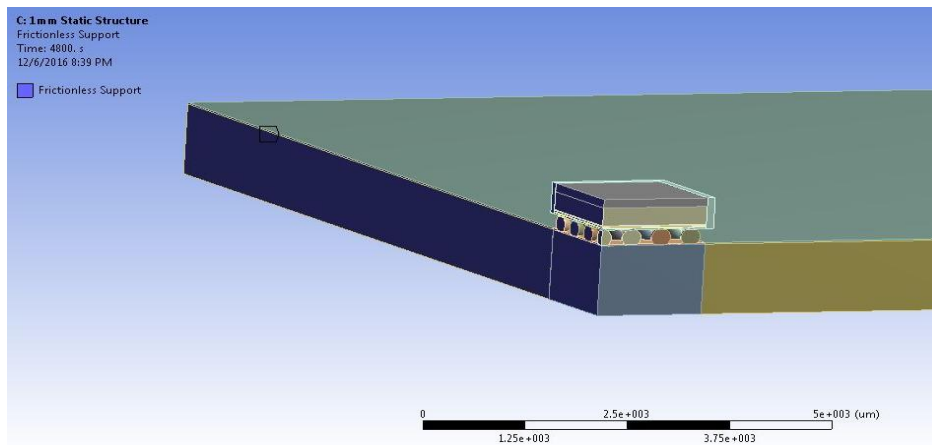
Figure 5-1 shows the detailed geometry of WLCSP. This is modeled using ANSYS v16.1

Table 5-1 shows the dimension of the package. Package dimensions influences the results obtained.

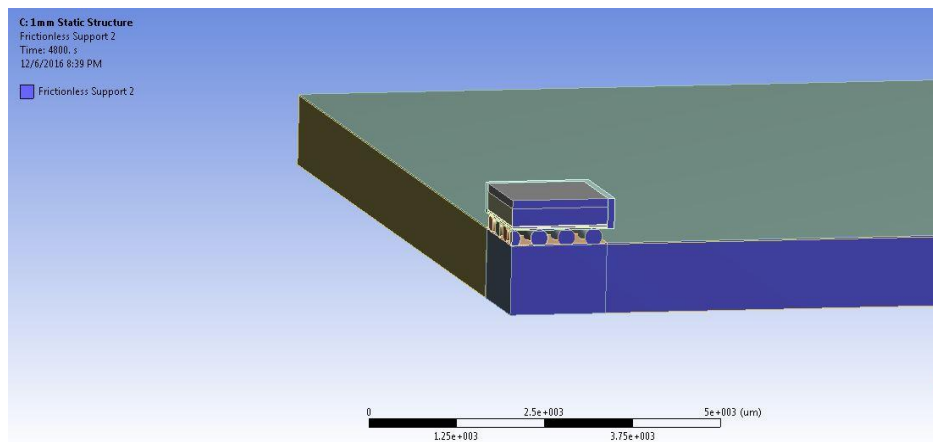
Component	Dimensions (mm)
Package	2.8 x 2.8 x 0.43
Die	4.315 x 3.245 x 0.19
PI Layer	2.8 x 2.8 x .02
Die Attach	4.15 x 4.15 x 0.01
UBM	.07 x 0.03
Pitch	0.4
PCB	24 x 24 x 1.00
	24 x 24 x 0.70

Table 5-1 Dimensions of WLCSP

Quarter geometry of WLCSP is used for computational purpose. Quarter geometry is considered for simulation as it saves computational time. Symmetric boundary conditions are applied on the 2 faces towards the inside where the geometry is split. Using quarter geometry does not affect the accuracy of the result.



(a)



(b)

Figure 5-2 (a) and (b) shows the symmetry boundary conditions on two surfaces.

The nature of all the properties were linear elastic, except the solder balls and the PCB. The solder balls were considered as visco-plastic and so Anand's model was used to explain the behavior of the solder balls. SAC 396 where the material composition is 95.5% Tin (Sn), 3.9% Silver (Ag) and 0.6% Copper (Cu) is what made up the solder ball. The Anand's constants are given in the Table 5-2. The PCBs were taken as linear orthotropic in nature. [20]

In the simulations, a 2.8x2.8 mm² WCSP is taken with a solder ball array of 7x7. The distance between the solder balls was 0.4 mm and the distance between the balls from one side to another is 2.4 mm. One thing to note is that it is very important to mention the dimensions of the components as they influence the results and affect the behavior of the assembly as whole.

5.2 Anand's Viscoplastic Model

As mentioned in the assumptions, Solder is modeled as rate dependent viscoplastic material which uses Anand's viscoplastic model. It takes both creep and plastic deformation into consideration to represent secondary creep of the solder. Anand's viscoplastic constitutive law best describes the inelastic behavior of lead-free solder. Anand's law consists of nine material constants A, Q, ξ , m, n, hu, a, su, \hat{s}

Anand's viscoplasticity for solder is described as:

$$\frac{d\varepsilon_p}{dt} = A \sinh \left(\xi \frac{\sigma}{s} \right)^{\frac{1}{m}} \exp \left(-\frac{Q}{kT} \right)$$

$$\dot{s} = [h_0 (|B|)^{\alpha} \frac{B}{|B|}] \frac{d\varepsilon_p}{dt}$$

Where,

$$B = 1 - \frac{s}{s^*}$$

and

$$s' = \hat{s} \left[\frac{1}{A} \frac{d\varepsilon_p}{dt} \exp \left(-\frac{Q}{kT} \right) \right]^n$$

[20]

Table 5-2 lists Anand's constant for SAC396 [8]

S.No.	Constant	Unit	Value
1	s_0	MPa	3.3
2	Q/R	1/K	9883
3	A	sec-1	15.7E+06
4	ξ	Dimensionless	1.06
5	m	Dimensionless	0.3686
6	h_0	Mpa	1077
7	\hat{s}	Mpa	3.15
8	n	Dimensionless	0.0352
9	a	Dimensionless	1.6832

Table 5-2 Anand's Constants

Chapter 6

MODELLING METHODOLOGY

- Based on the physical dimensions of the board, geometry is created on ANSYS. Material properties are assigned and mesh is created.
- A transient thermal analysis is performed on WLCSP. A power cycling loading is given to the die of the package.
- The solution gives the temperature distribution along the package. This solution is extracted and given as an input to static structural.
- The imported thermal load from transient thermal is used to calculate plastic work and Equivalent (Von-Mises) stresses. Critical solder joint and the Directional Deformation is also obtained. Fig. 6.1 shows all the steps.

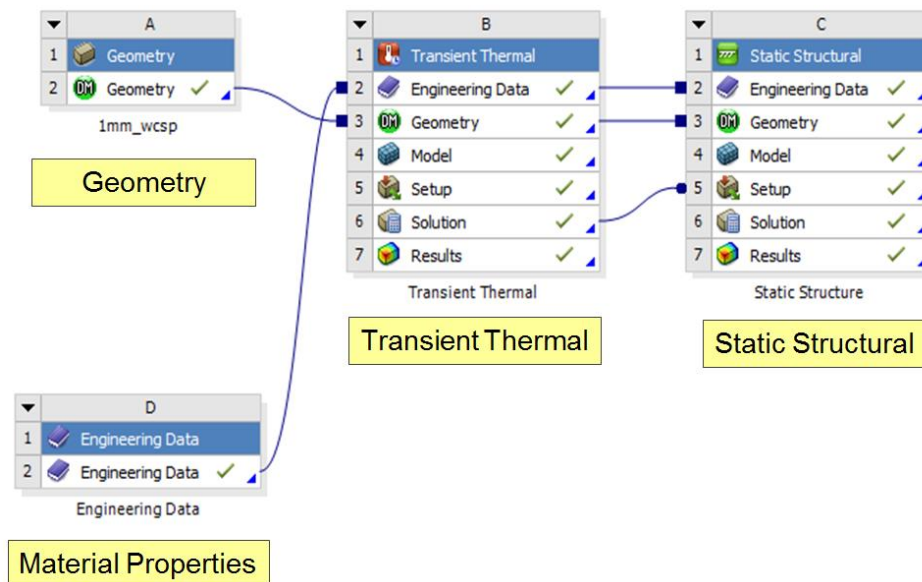
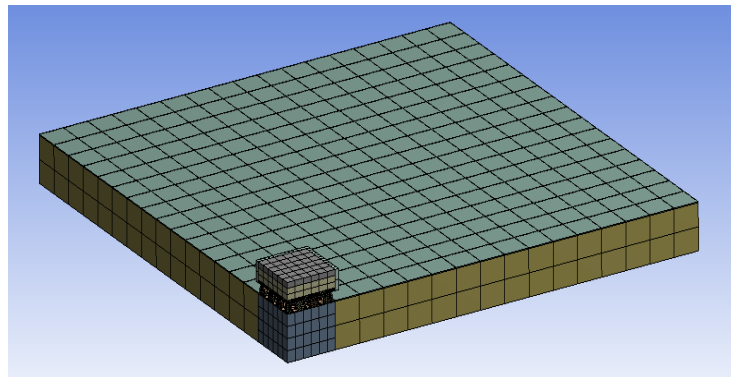


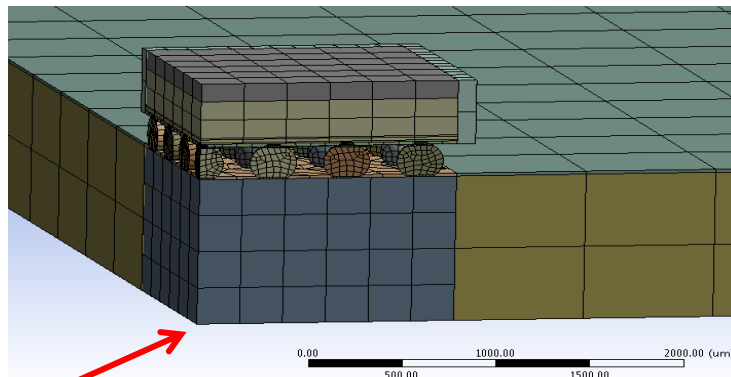
Figure 6-1 Modelling Methodology

6.1 Meshing

The meshing used in the simulations in ANSYS 17 was not very complicated and this helped to reduce a lot of computational time. Mesh sizes were assumed to be medium and caused no observable variance from the coarse mesh. Special meshing operations were carried out in regions where it was needed. Edge sizing was needed for very thin sections to have at least two parts in the mesh. Solders underwent body sizing to match the mesh of the solders to the rest of the body.



(a)



(b)

Fixed node in z-dir

Figure 6-2(a) shows the meshing of WLCSP and (b) shows the node constrained.

Quarter symmetry is shown below in Fig. 6-3. The meshing was done using hex dominant method. Number of elements in the mesh is 49640.

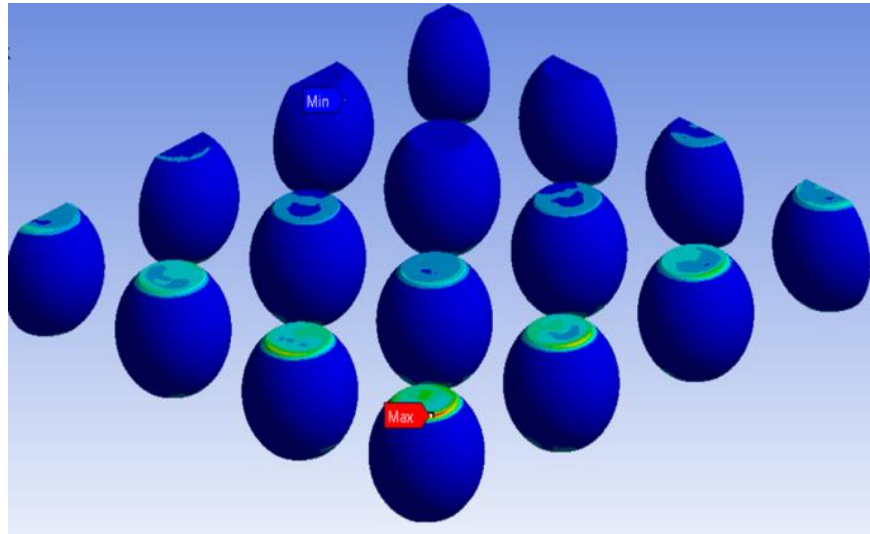


Figure 6-3 Quarter symmetry of WLCSP

6.2 Boundary Conditions

- Convective boundary condition is applied on surfaces of the package which are exposed to the environment.
- Symmetry boundary conditions are applied on the surfaces where the package is cut. Fixed support is given to the two surfaces.
- The center node is constrained in z-direction.

The convective heat transfer co-efficient used for this analysis is $23\text{W}/(\text{m}^2/\text{C})$.

This co-efficient is chosen with the assumption that the package does not exceed 1250

C.

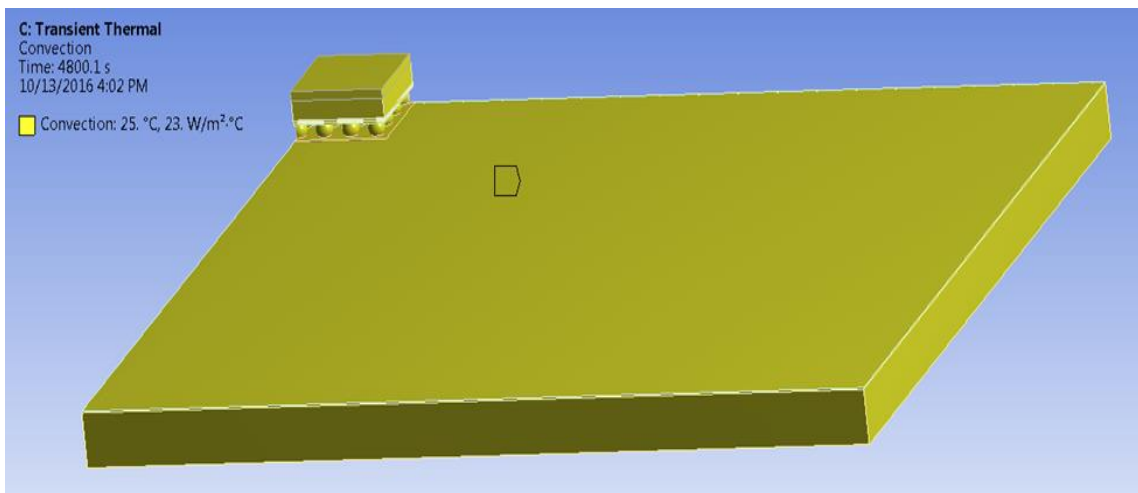


Figure 6-4 Convective Boundary Condition.

Figure 6-4 shows the convective boundary condition applied on the WLCSP.

Loading

Three cycles of $0.5\text{W}/\text{mm}^3$ is applied to the die of WLCSP for 4800 seconds. One cycle includes 800 seconds ON and 800 seconds OFF as shown in Fig. 6-5 and Fig.6-6

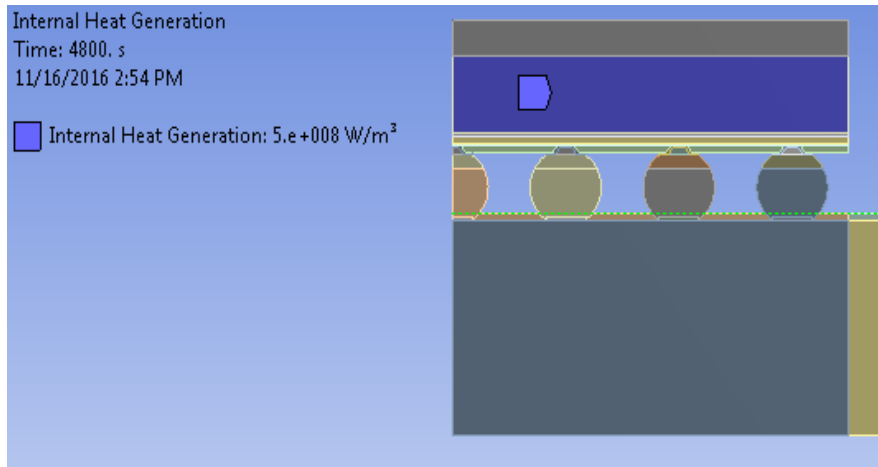


Figure 6-5 Internal Heat Generation on the die

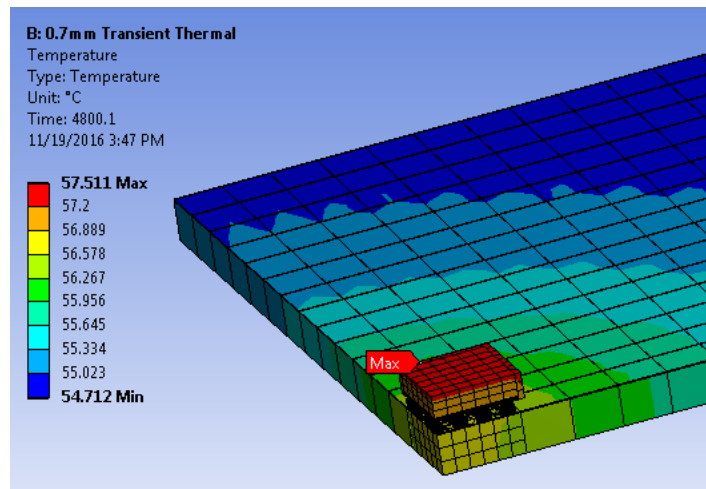


Figure 6-6 Power cycling plot

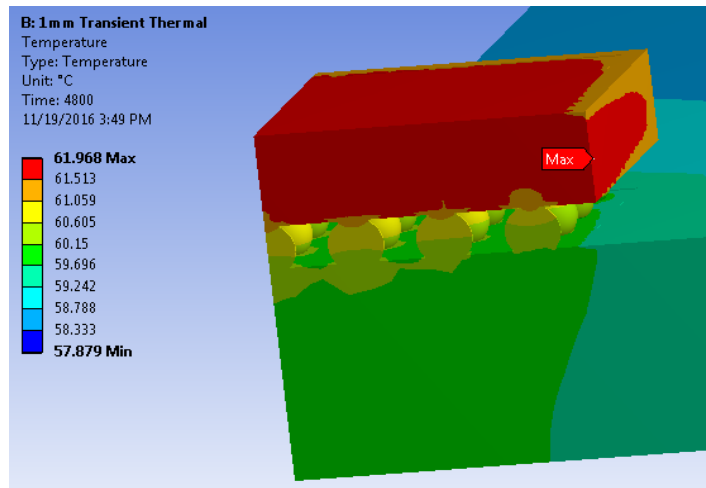
Chapter 7

RESULTS

7.1 Temperature distribution

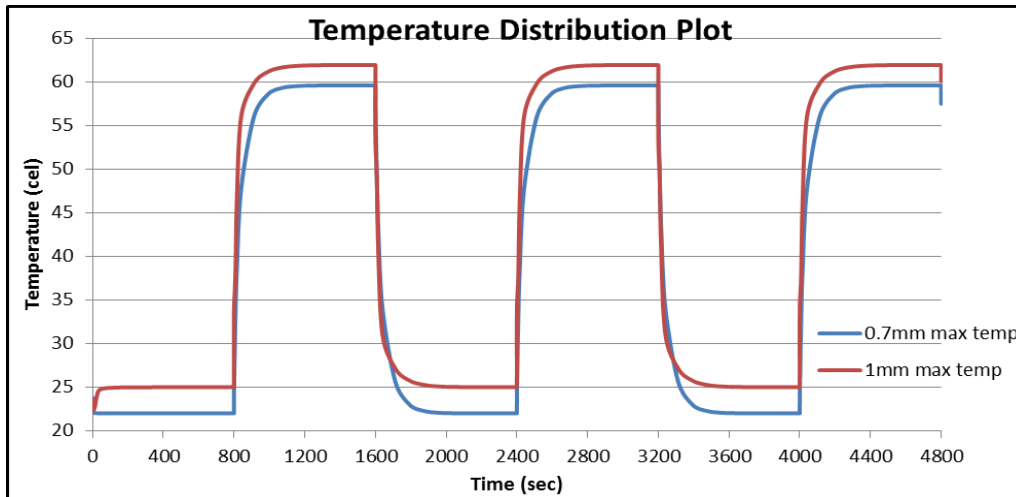


(a)



(b)

Figure 7-1 (a) shows temperature distribution of 0.7mm and (b) shows temperature distribution of 1mm board. The maximum temperature in 0.7mm board is 57.511°C . The max temperature in 1mm is 61.968°C .

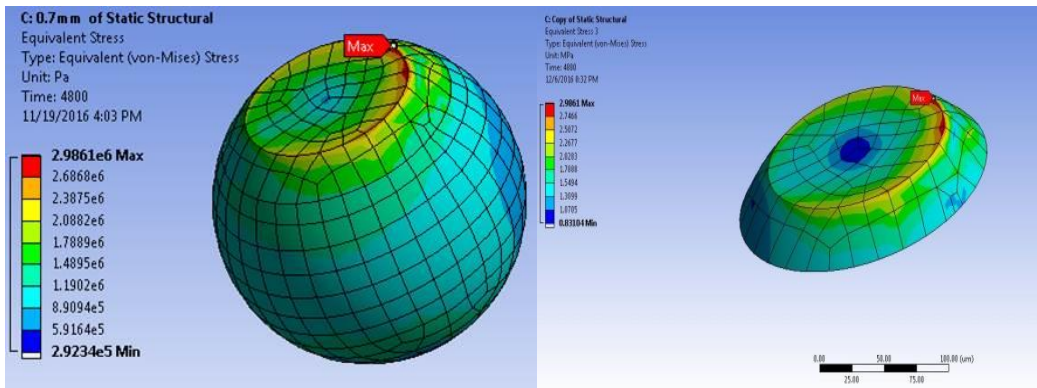


Plot 7-1 Temperature Distribution Plot

- Plot 7-2 shows temperature distribution in 0.7mm and 1mm package after 4800 seconds when 3 power cycles of 0.5W/mm³ is applied.
- The maximum and minimum temperature in the package is obtained.
- The non-uniform temperature distribution is transferred to static structural module

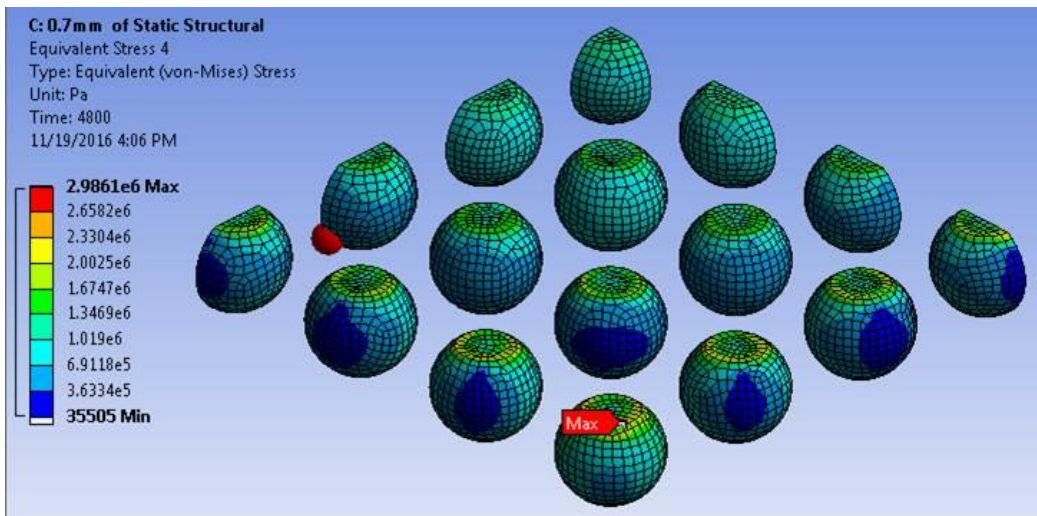
7.2 Stress distribution

7.2.1 Stress Distribution in 0.7mm board



(a)

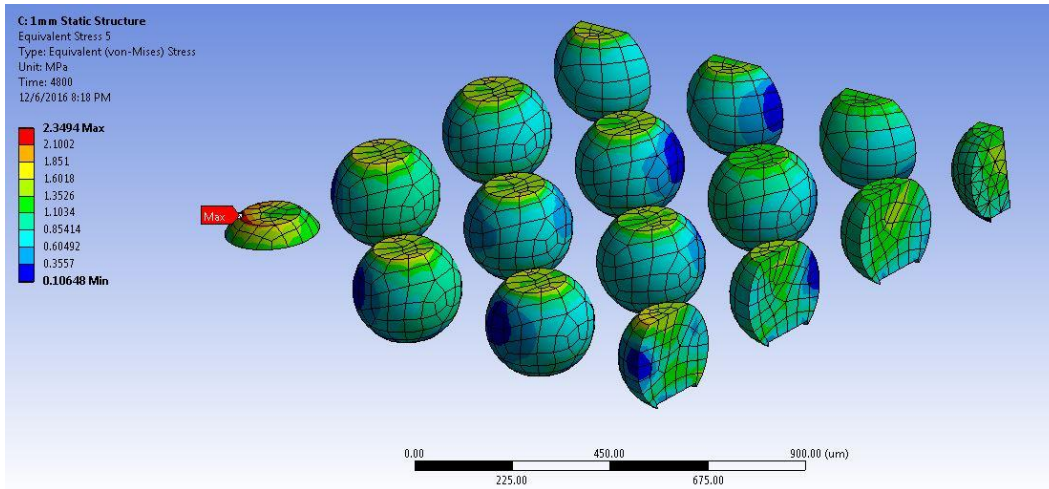
(b)



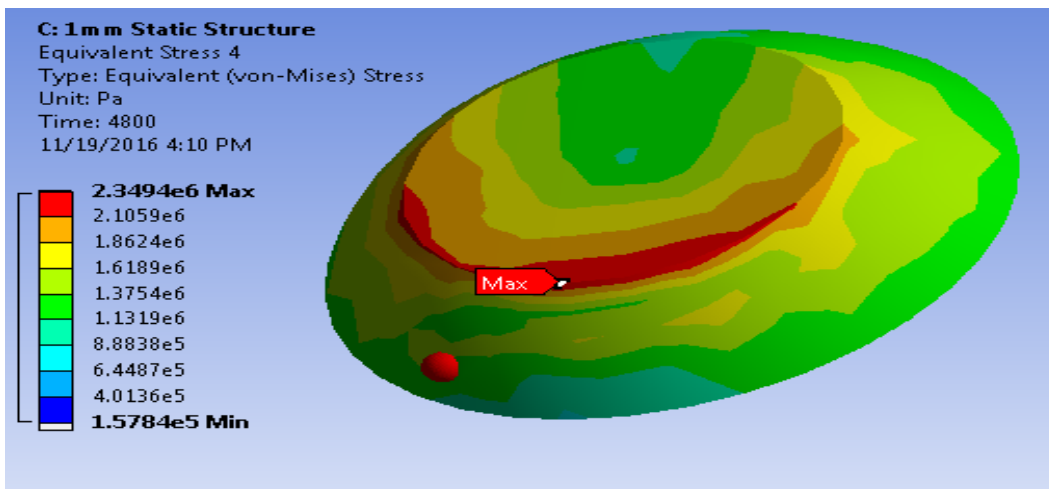
(c)

Fig. 7-2 (a) (b) and (c) shows the maximum equivalent stress in 0.7mm solder ball. The Max Equivalent stress is 2.9861Mpa.

7.2.2 Stress Distribution in 1mm board



(a)

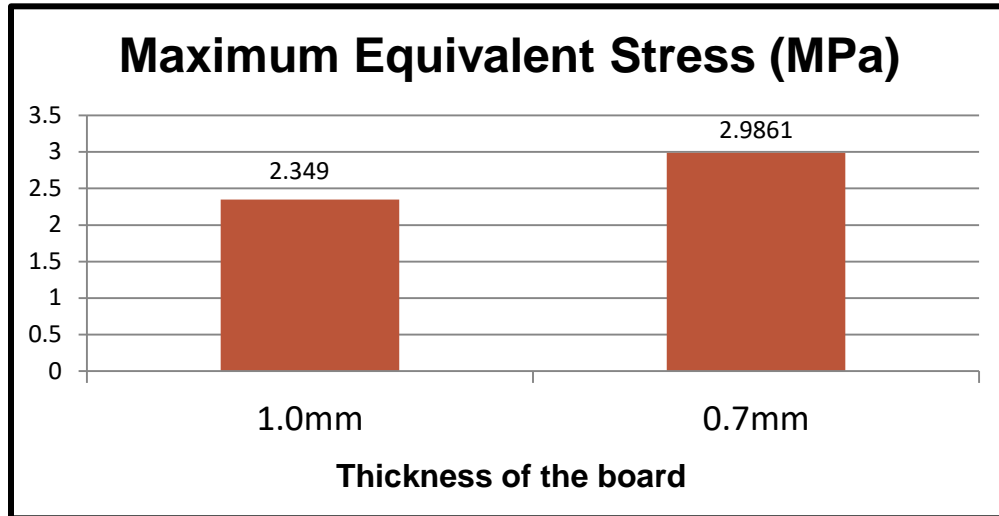


(b)

Fig 7-3 (a) and (b) shows the maximum equivalent stress in 1mm solder ball.

The Max Equivalent stress is found to be 2.349Mpa.

7.2.3 Comparison of Maximum Equivalent Stress in two Boards

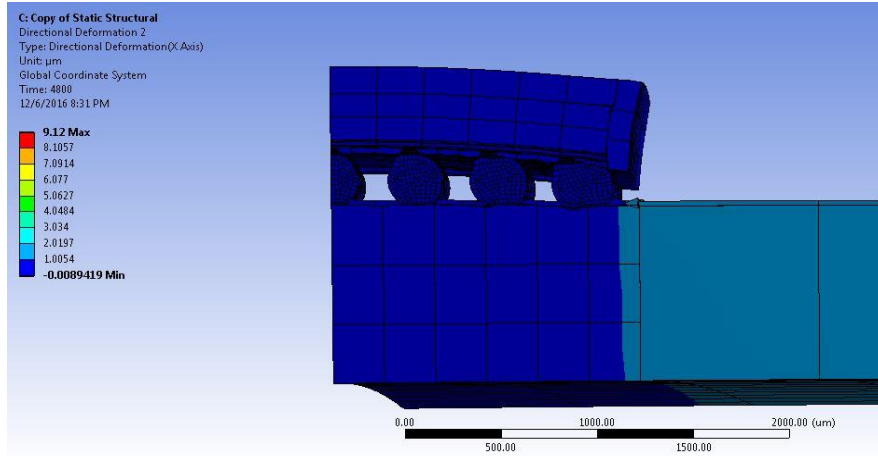


Plot 7-2 Max Equivalent stress in 0.7mm and 1mm board

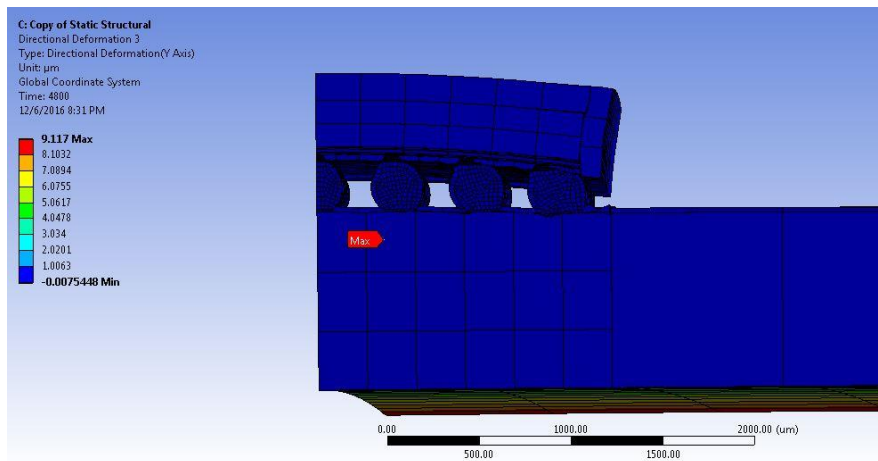
Plot 7-2 shows the comparison of Maximum Equivalent Stress between 2 boards. It reveals that 0.7mm has higher Equivalent stress as opposed to 1mm board.

7.3 Directional Deformation

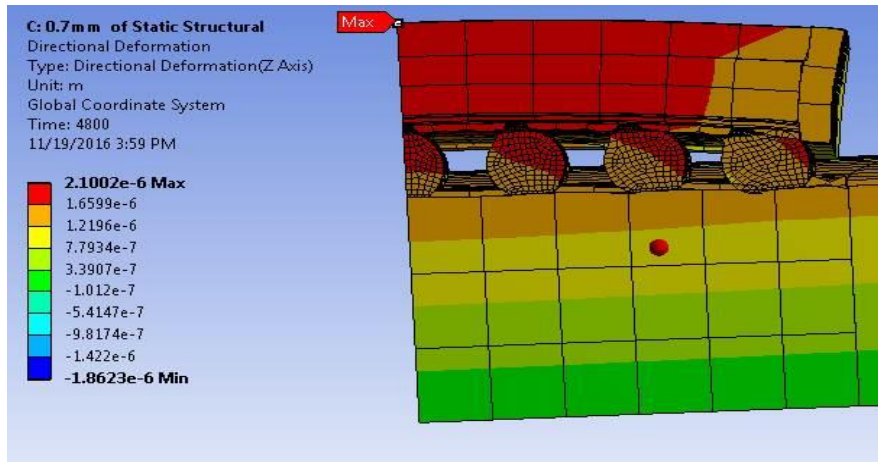
7.3.1 Directional Deformation in 0.7mm board



(a)



(b)



(c)

Figure 7-4 (a) (b) and (c) shows Directional Deformation of 0.7mm board in x-direction, y-direction and z-direction respectively.

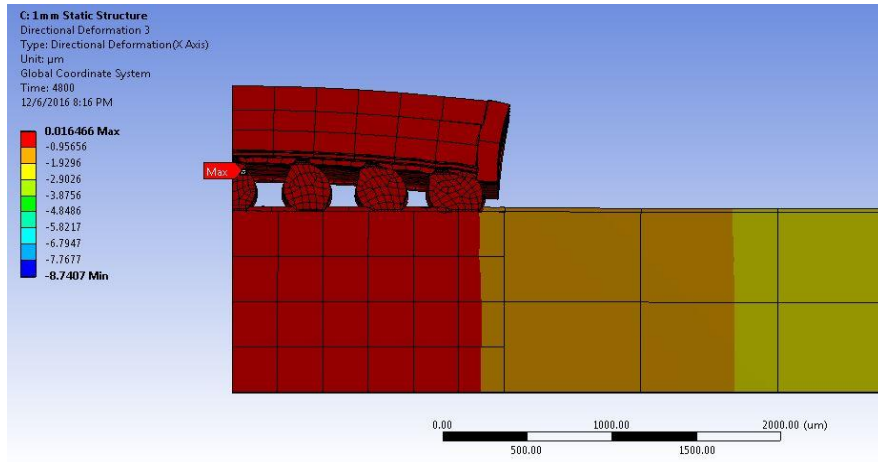
Directional Deformation of 0.7mm board in:

x-dir- 9.12 μm

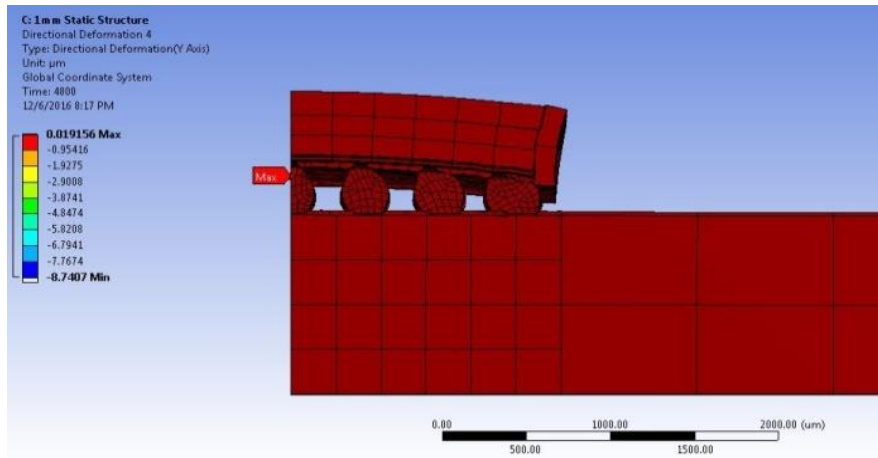
y-dir- 9.117 μm

z-dir- 2.1 μm

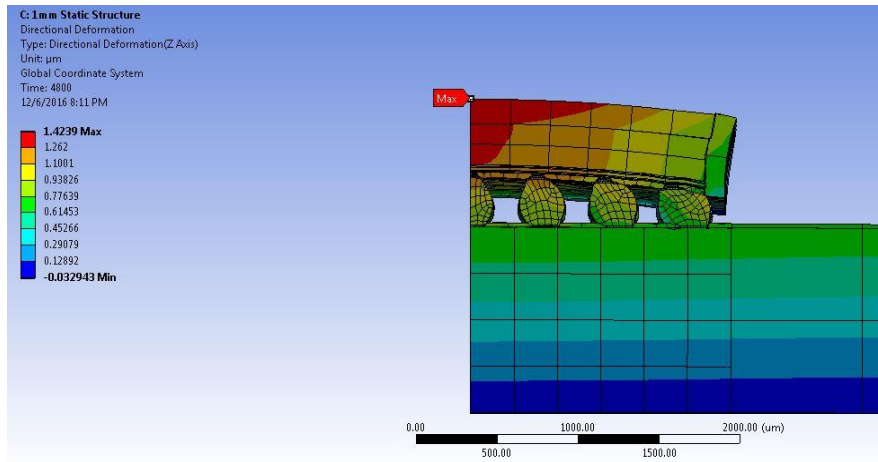
7.3.2 Directional Deformation in 1 mm board



(a)



(b)



(c)

Figure 7-5 (a) (b) and (c) shows Directional Deformation of 1mm board in x-direction, y-direction and z-direction respectively.

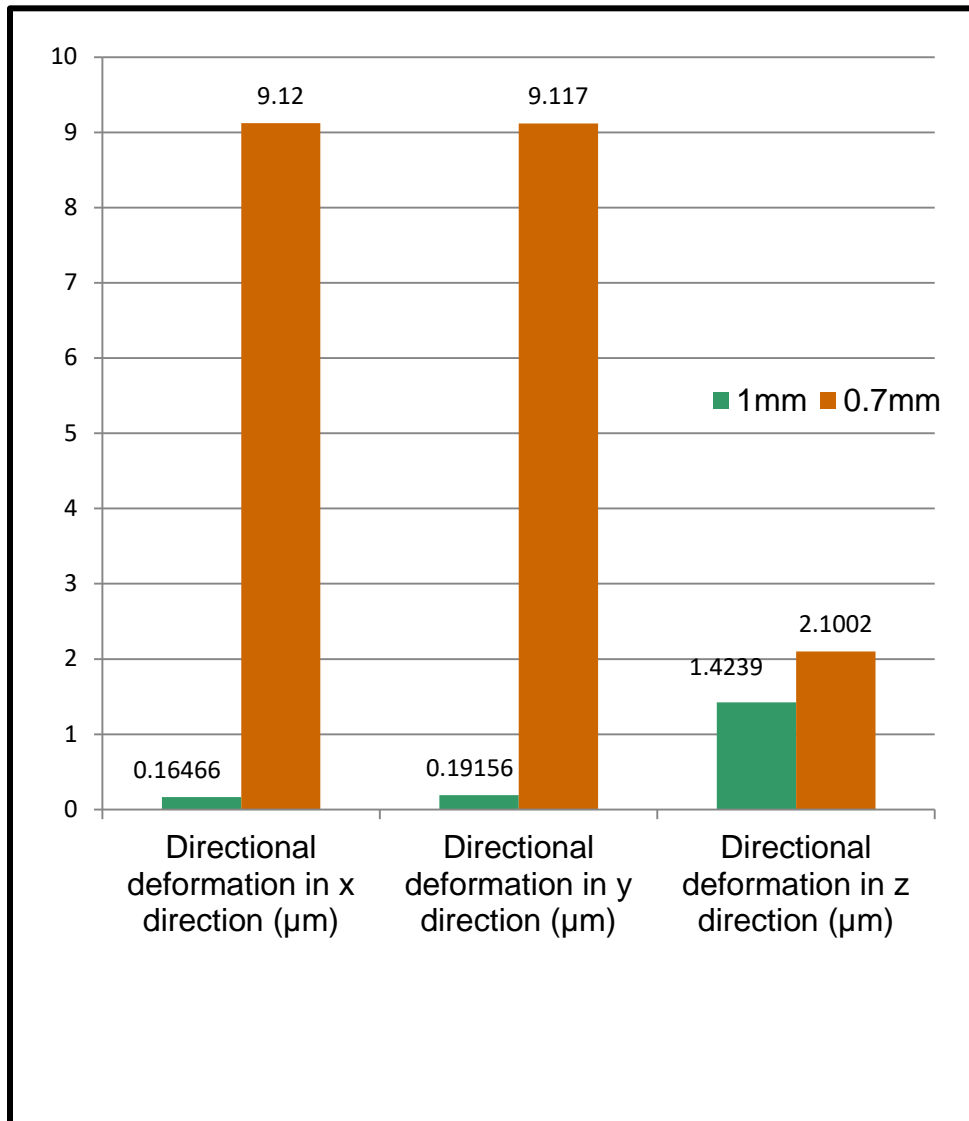
Directional Deformation of 1mm board in:

x-dir- 0.19 μm

y-dir- 0.16 μm

z-dir- 1.42 μm

7.3.3 Comparison of Directional Deformation of 0.7mm and 1mm boards.



Plot 7-3 Comparison of Directional Deformation in all directions of 0.7mm and 1mm board.

Graph represents the directional deformation of 1mm and 0.7mm boards.

Thinner board (0.7mm) has more deformation in all directions.

7.4 Plastic Work

7.4.1 Plastic Work in 0.7mm Board

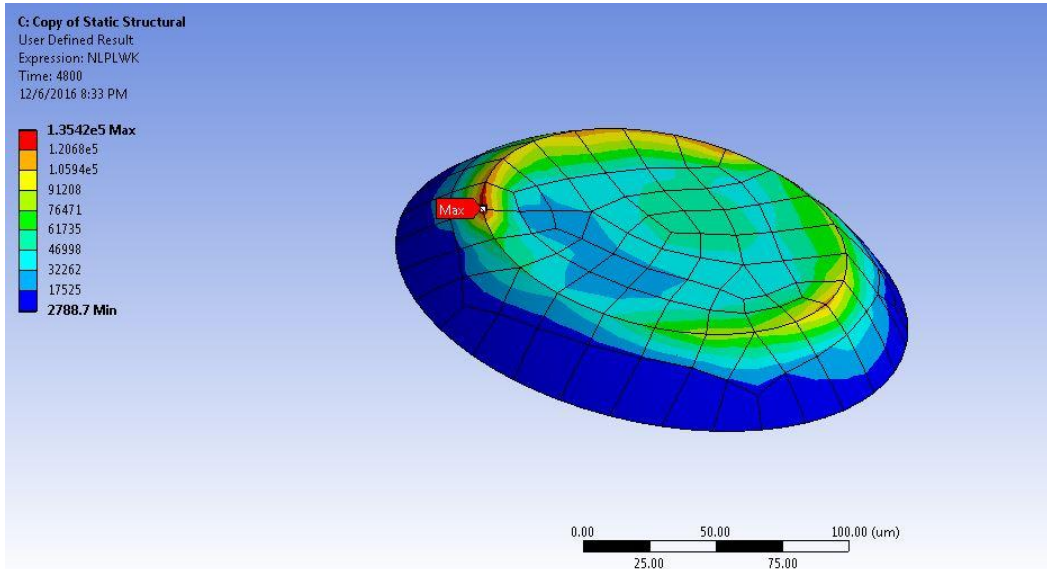


Figure 7-6 Plastic work in 0.7mm board

7.4.2 Plastic Work in 1mm Board

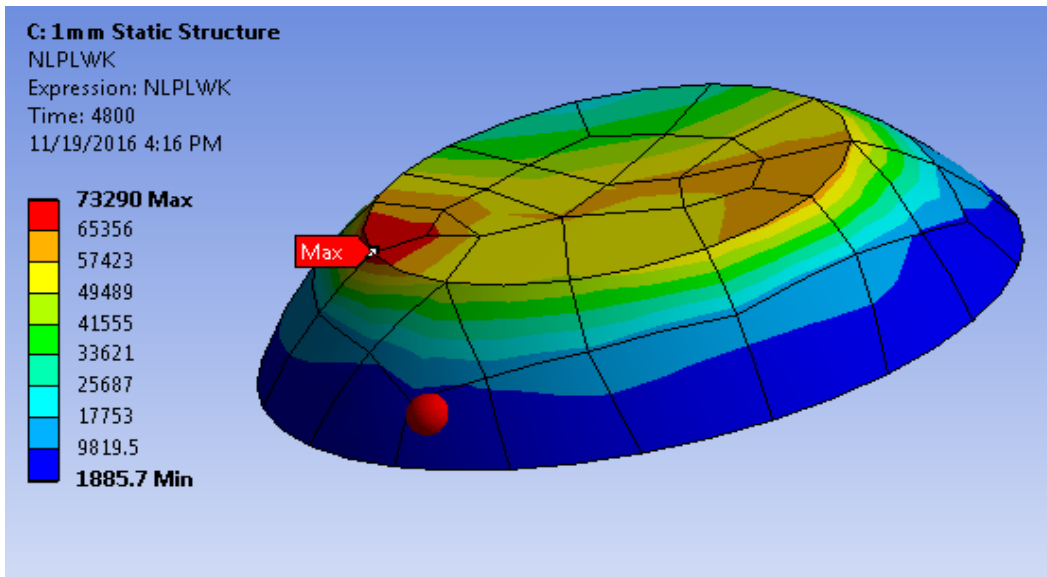
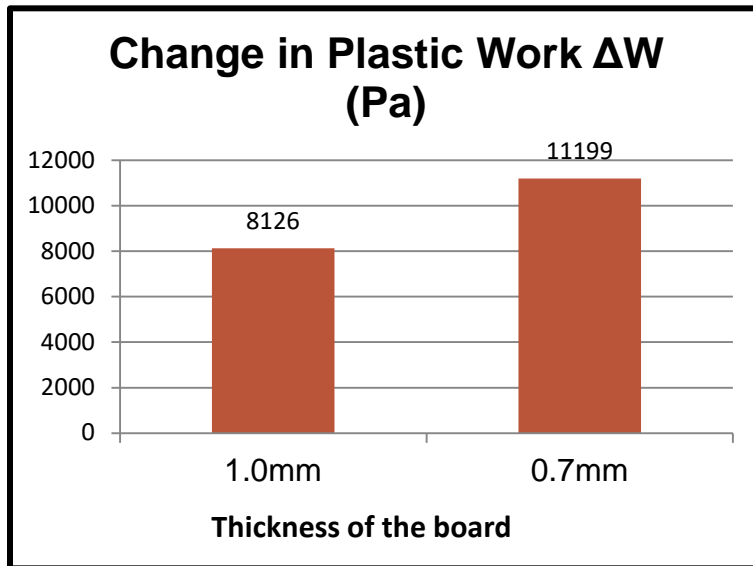
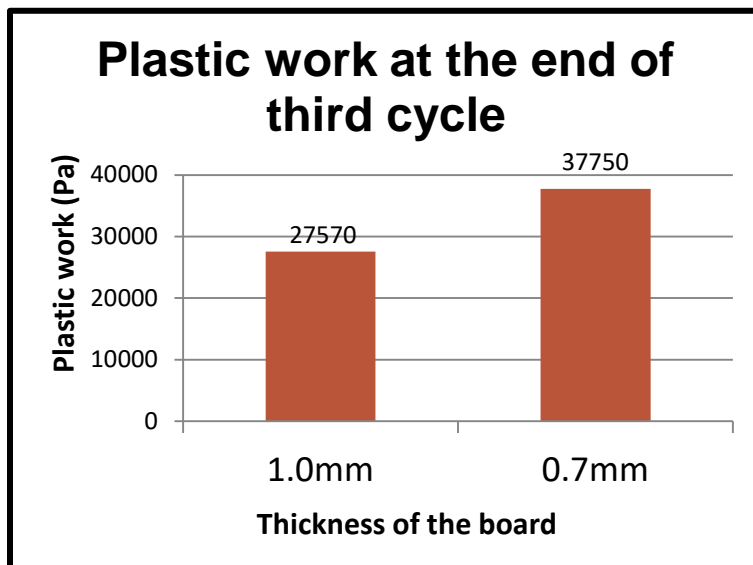


Figure 7-7 Plastic work in 0.7mm board



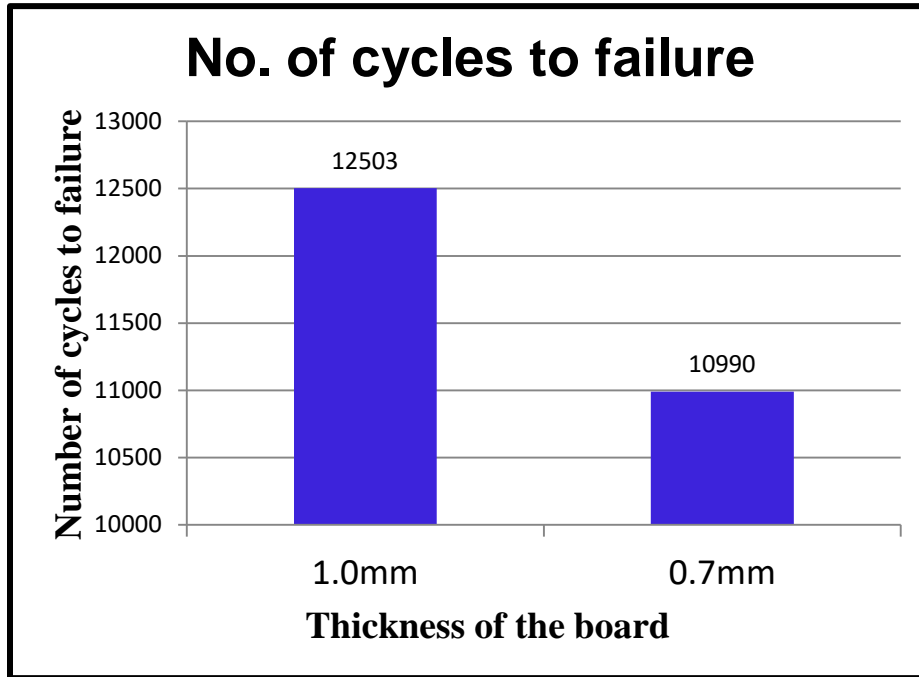
Plot 7-4 Change in plastic work(ΔW)



Plot 7-5 Plastic work at the end of third cycle

From Plot 7-4 and 7-5, it is seen that 0.7mm board has higher plastic work.

7.5 Number of cycles to failure



Plot 7-6 Number of Cycles to Failure of 0.7mm board and 1mm board.

Plot 7-6 shows the number of cycles to failure of 0.7mm board and 1mm board.

It is seen that 0.7mm board takes lesser number of cycles to fail. The plastic work ΔW obtained was used to calculate the number of cycles to failure using Schubert et. al [21] & Che and Pang[22] correlation:

$$N_f = \left(\frac{A}{\Delta W}\right)^k$$

Where,

N_f = Predicted life cycles to failure

$A = 1.256 \times 10^8$ MPa

$k = 0.4021$ [8]

Chapter 8

CONCLUSION AND FUTURE WORK

8.1 Conclusion

Studying Finite Element Analysis on two Wafer Level Chip Scale Packages of different thickness in specific a 0.7mm board and 1mm board under the influence of Power Cycling proved to be fruitful and an eye opening attempt at figuring out Solder Ball Reliability. Furthermore, analysis of Equivalent Stress (Von-Mises) Distribution, Directional Deformation and Plastic work were obtained and compared between the two boards. In doing so, number of cycles to failure was determined. On comparison, the results showed that 0.7mm board failed faster as opposed to the 1mm board.

The literature review and analysis show that the 0.7mm board has 38% more Copper per unit volume of the board and 1mm board has 38% more FR4 per unit volume of the board. Copper is stiffer than FR4 hence 0.7mm board is much more rigid. This makes it transfer more rigidity and stresses to the solder balls during Power cycling. The 1mm board is much more compliant because it sustains strain as observed in the Power cycling. [8]

The thinner board cannot sustain high stress and hence has a lower life cycle and fails faster. This confirms the claim that rigidity has a major role to play in a board's life cycle. The solder ball with experience higher stresses due to rigidity and eventually the solder will fail quicker.

8.2 Future Work

- Further study and simulations can be carried out for different thickness of the boards by implementing layer removal method and observe if there exists a pattern. Furthermore, simulations can be carried out for different types of boards with varying loading condition.
- Practical experimentation of Power cycling can be a suggestion to validate results.
- Reverse Engineering- Can the package attain Reliability if a number of cycles to failure is given?

References

- [1]. Datta, Madhav, Tetsuya Osaka, and J. Walter Schultze, eds. *Microelectronic packaging*. CRC press, 2004.
- [1a] <http://www.singularitysymposium.com/moores-law.html>
- [1b] <http://slideplayer.com/slide/1555508/>
- [1c] <http://www.atmel.com/Images/doc42007.pdf>
- [1d] <http://www.weibull.com/hotwire/issue21/hottopics21.htm>
- [2]. Tummala, Rao, Eugene J. Rymaszewski, and Alan G. Klopfenstein. *Microelectronics packaging handbook: technology drivers*. Springer Science & Business Media, 2012.
- [3]. S.W. Ricky Lee, "Types of Printed Circuit Boards"
- [4]. Ho, Kai-Kuang, and Te-Sheng Yang. "Wafer-level chip scale package." U.S. Patent No. 6,204,562. 20 Mar. 2001.
- [5]. Trina Barua. "A comparative study of the thermo-mechanical behavior of WCSP assembly due to difference in PCBS' layer thickness." May 2014.
- [6]. Paek, Jong Sik, et al. "Wafer level chip scale package." U.S. Patent No. 7,335,986. 26 Feb. 2008.
- [7]. Viswanadham, Puligandla. *Reliability of Electronic Packaging*. ASME Press, 2011.
- [8]. Hassaan Ahmad Khan. "Experimental and Simulation Board Level Reliability Assessment of Wafer Level Chip Scale Packages (WCSPs) Under Thermal Cycling" August 2015
- [9]. R. Rodgers, "Cypress Board Level Reliability Test for Surface Mount Packages", Cypress Semiconductor White paper, 2012.
- [10]. Ahmed, Izhar Z., and S. B. Park. "An accurate assessment of interconnect fatigue life through power cycling." *Thermal and Thermomechanical Phenomena in Electronic Systems, 2004. IThERM'04. The Ninth Intersociety Conference on*. Vol. 2. IEEE, 2004.

- [11]. D. Edwards, "PCB Design And Its Impact on Device Reliability," Electronic Design, [Online]
- [12]. Darveaux, Robert. "Effect of simulation methodology on solder joint crack growth correlation." *Electronic Components & Technology Conference, 2000. 2000 Proceedings. 50th.* IEEE, 2000.
- [13]. Popp, DE Hodges, Andrew Mawer, and Gabriel Presas. "Flip chip PBGA solder joint reliability: power cycling versus thermal cycling." *Motorola Semiconductor Products Sector, Austin, TX* (2005).
- [14]. Park, S. B., and Izhar Z. Ahmed. "Shorter field life in power cycling for organic packages." *Journal of Electronic Packaging* 129.1 (2007):.
- [15]. E. s. T. Analyzer, Thermomechanical Analyzer/Stress Strain, TMA 6100 Brochure and Optional Accessories.
- [16]. Szabo, Barna Aladar, and Ivo Babuška. *Finite element analysis*. John Wiley & Sons, 1991.
- [17]. Daryl L. Logan, "A First Course in Finite Element Method", Fifth Edition
- [18]. O. C. Zienkiewicz, R. L. Taylor and J. Z. Zhu, *The Finite Element Method: Its Basis and Fundamentals*, 2005.
- [19]. E. Madenci and I. Guven, "Fundamentals of ANSYS," in *The Finite Element Method and Applications in Engineering using ANSYS*, Springer, 2006, pp. 15-35.
- [20]. J. Pang, *Lead Free Solder: Mechanics and Reliability*, X ed. Springer, 2012.
- [21]. A. D. R. A. E. G. A. M. B. a. R. H. Schubert, "Fatigue Life Models for SnAgCu and SnPb Solder Joints Evaluated by Experiments and Simulation," in *Electronic Components and Technology Conference (ECTC)*, 2003.
- [22]. F. a. P. J. Che, "Thermal Fatigue Reliability Analysis for PBGA with Sn-3.8Ag-0.7Cu Solder Joints," in *Electronic Components and Technology Conference*, 2004.

Biographical Information

Bhavna Conjeevaram graduated with a Bachelor's degree from Nitte Meenakshi Institute of Technology, Bangalore, KA, India in 2014. She did her summer internship in L&T Komatsu Pvt Limited in 2012 during her Undergraduate. She pursued her Masters in Mechanical Engineering at University of Texas at Arlington from August 2014. She got the opportunity to work under Dr. Agonafer's Electronics MEMS & Nano electronics Systems Packaging Center (EMNSPC) group. She developed keen interest in studying the Reliability of packages. She has won the 'Best Student Poster' award for "*Solder Ball Reliability Assessment of WLCSP through Power Cycling*" at the 42nd International Symposium for Testing and Failure Analysis (ISTFA) conference held in Fort Worth Texas on November 9, 2016. She successfully completed her internship for 7 months in Imperial Manufacturing Group, Decatur, TX from February 2016 to August 2016.