EFFECT OF SOLDER VOIDS AND DISTANCE TO NEUTRAL POINT (DNP) ON SJR OF WCSP UNDER REFLOW CONDITION AND THERMAL CYCLING

by

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Abstract

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Since the introduction of Chip Scale Packages (CSP's) in the early 2000s, they have become one of the biggest packaging trends in recent history. There are currently over 50 different types of CSP's available throughout the industry and the numbers are increasing almost daily. Wafer Level Chip Scale Package's (WCSP) is kind of CSP's used widely due to its small form factor which offers efficient use of limited space and miniaturization of the electronic device. On the other hand, small form factor typically incurs greater initial cost in product design and development. In an electronic device, it is equally important to design a device with greater mechanical stability, with electrical stability as well. In this study, I am going to optimize the design of WCSP to enhance the thermo-mechanical reliability of the package by studying the effect of DNP. Further, the attempt has been made to study the effect of a void on BLR and SJR in the critical solder joint during thermal cycling and reflow condition. For this study PCB of 1 mm was leveraged. Thermo-Mechanical Analyzer (TMA), Dynamic Mechanical Analyzer (DMA) and, Oven were used to characterize material properties. PCB cross-sectioning was done using a cutter and Optical Microscopy was used to study voids and layer by layer composition of PCB. ANSYS Workbench 18.0 was leveraged to model 3D CAD of the quarter geometry of PCB and it was used to do the computational study.

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Chapter 1

INTRODUCTION

1.1 Electronic Packaging

The importance of Electronic packaging is being identified by industry but advancement and development in this filed is lagging the advances in Microelectronics. This is because it is a multi-disciplinary field which needs a study of traditional sub-areas like mechanics, electronics, physics, and chemistry. The most prominent areas to work are heat transfer, material science, electrical and mechanical stability and manufacturing.

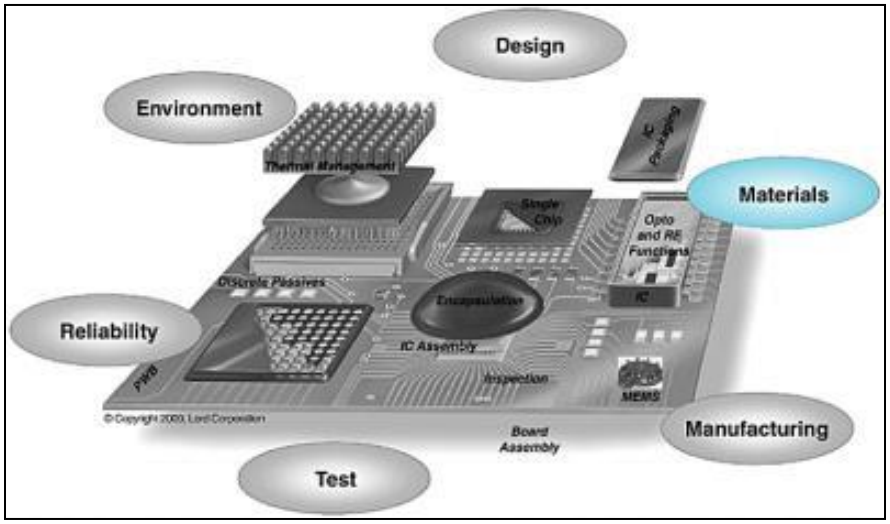

Figure 1- 1 Fundamentals of Electronic Packaging

The basic requirements to manufacture reliable electronic package are as follows-

1. Mechanical requirements
2. Environmental requirements
3. Reliability requirements
4. Interconnection requirements
5. Input/ Output (I/O) requirements

1.2 Wafer Level Chip Scale Package

WCSP is one of the most famous packages in the recent history of electronic packaging. WCSP refers to the technology of packaging an integrated circuit at the wafer level, instead of the traditional process of assembling individual units in packages after dicing them from a wafer. This process is an extension of the wafer Fab processes, where the device interconnects and protection are accomplished using the traditional fab processes and tools. In the final form, the device is a die with an array pattern of bumps or solder balls attached to an I/O pitch that is compatible with traditional circuit board assembly processes.

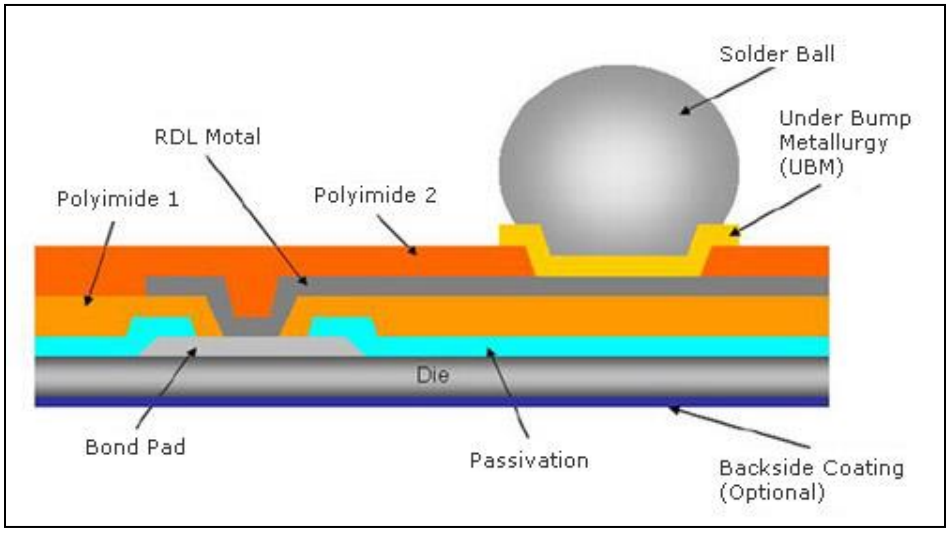

Figure 1- 2Typical WCS Package with solder bump

WCSP is a true chip-scale packaging (CSP) technology since the resulting package is of the same size of the die. WCSP technology differs from another ball-grid array (BGA) and laminate-based CSPs in that no bond wires or interposer connections are required. The key advantages of the WCSP are the die to PCB inductance is minimized, reduced package size, and enhanced thermal conduction characteristics. The advance in semiconductor technology has created chips with transistor counts and functions that were

unthinkable a few years ago. Portable electronics, as we know it today, would not be possible without equally exciting developments in IC packaging. Driven by the trend towards smaller, lighter, and thinner consumer products, smaller package types have been developed. WCSP has a smaller form factor which helps in more efficient use of limited space, greater flexibility in the placement of components in the assembly, reduced use of materials and ease of transport.

1.3 Literature review

WCSP is one of the packages which still need improvement and it can be optimized for the betterment of reliability. Tung Ching Lui et al. [1] introduced the study of Reliability assessment of WCSP based on DNP and scribe line width. Khan et al. [2] studied failure mechanisms in WCSP with 1 mm and 0.7 mm PCBs. In which WCSP with 0.7 mm PCB failed earlier than 1 mm PCB, this contradicts the previous studies based on the effect of varying PCB thickness on the thermo-mechanical reliability of a package. It was concluded that 0.7 mm PCB was less reliable that 1 mm PCB because of more copper content in 0.7 mm compared to 1 mm. Both studies can be used to optimize WCSP and get most out of it. Distance to neutral point is the distance from the center of the package to the center of the critical corner solder ball. DNP plays an important role when you are designing a WCS Package and on the other hand, it is equally important to consider the designing concerns of PCB. Pitch is the distance between two consecutive solder balls. Scribe line width is the distance from the center of the corner ball to the end of the package.

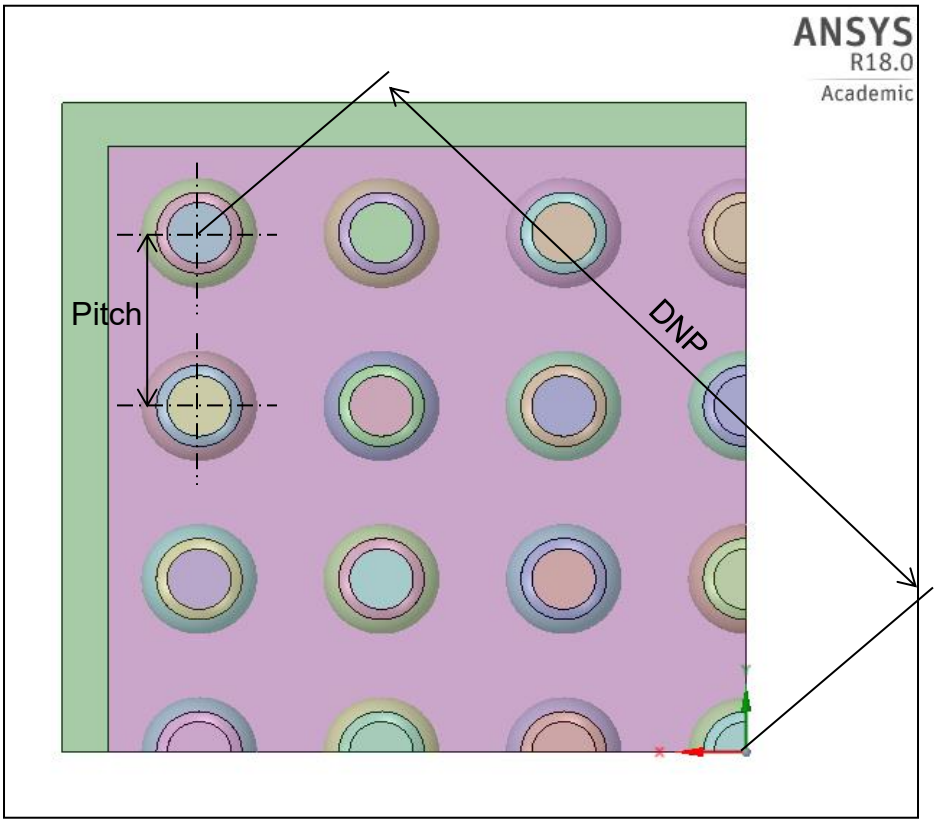

Figure 1- 3 WCSP showing DNP and pitch

Voids in the Sn-Pb and Pb-free solder are a really important issue because researchers always found conflicting results. Ladani et al. [3] studied the effect of the process-induced voids on the durability of a package.

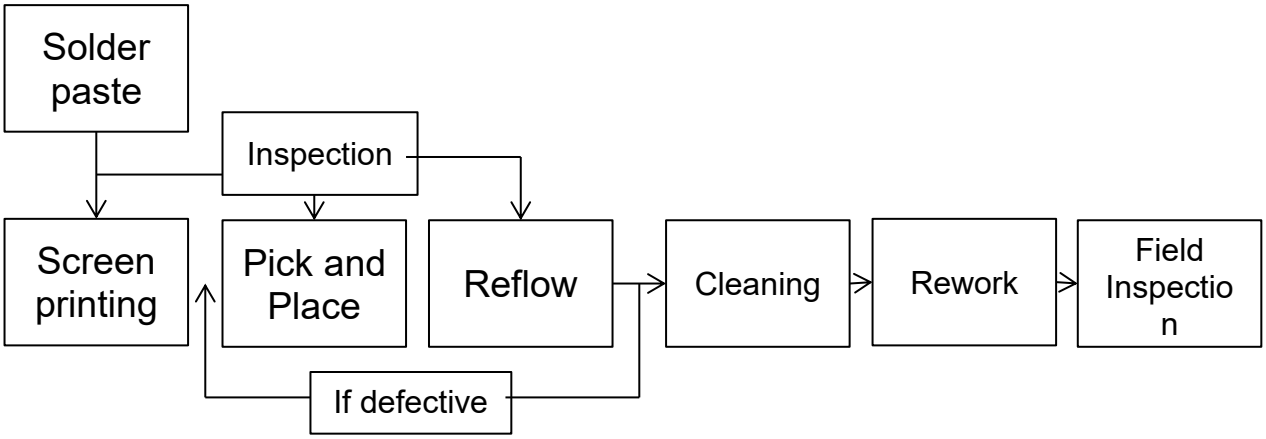

Figure 1- 4 Reflow process flow chart

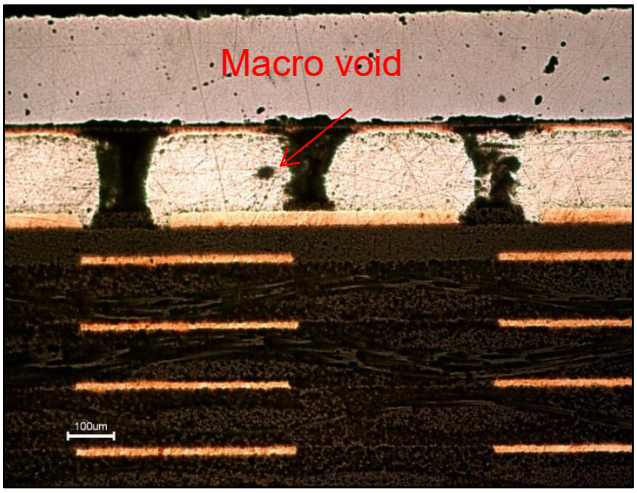

Figure 1- 5 Cross-sectioning showing void (Using optical microscopy)

Many defects in the assembly of SMT electronics assembly is introduced during the reflow and printing process. Studies have shown that 60% of defects identified after the reflow originated during the solder paste printing process. Cross-sectioning is done to study the layer by layer architecture of PCB and a package. Above figure shows the macro-void in the solder ball. In cross-sectioning PCB with a package is cross-sectioned using the cutter. Then the cross-sectioned face is polished and set in epoxy. When epoxy resin hardens the sample is then observed under optical microscope. There are different types of voids observed in the manufacturing of electronic packages.

1. Macro-voids
2. Micro-voids
3. Pinhole micro-voids

Chapter 2

MATERIAL CHARACTERIZATION

Material Characterization is one of the important parts in the reliability assessment of electronic package. For performing FE analysis to predict the number of lifecycles to failure it is crucial to determine mechanical properties of the electronic package and the printed circuit board (PCB). For this study following mechanical properties where determined-

1) Coefficient of Thermal Expansion (CTE)
2) Young's Modulus (E)
3) Poisson's ratio (υ)

To determine the mechanical properties, the equipment and technique used are as below-

1) Sun Microsystems Oven
2) Thermo-Mechanical Analyzer
3) Dynamic Mechanical Analyzer
4) Instron Universal Testing Machine

All sample preparation and testing were done in the lab. Procedure for preparation and testing will be explained in the sections below.

2.1 Coefficient of Thermal Expansion (CTE)

The coefficient of thermal expansion is the mechanical property of the material which tells us how the material will expand or contract as a function of the change in the temperature.

$$\alpha = \frac{\epsilon}{\Delta T}$$

Where,

α – Coefficient of Thermal Expansion (CTE) ppm/°C

ϵ - Strain (mm/mm)

ΔT – Difference in Temperature (°C)

2.1.1 Thermo-Mechanical Analyzer

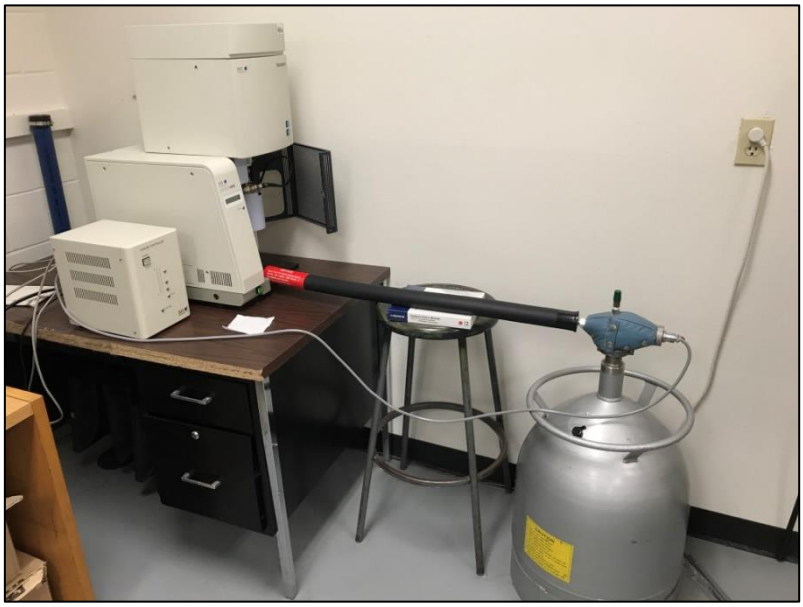

Figure 2- 1 Thermo-Mechanical Analyzer

Shown in the above figure is the Thermo-mechanical analyzer with a cooling unit on the right. Buehler cutter was used to prepare a sample for TMA experiment of 1mm thick PC Board. Sample dimensions were 8 X 8 mm. With the help of cooling unit, it is possible to determine CTE from -65°C to 260°C (a thermal cycle is from -40°C to 125°C).

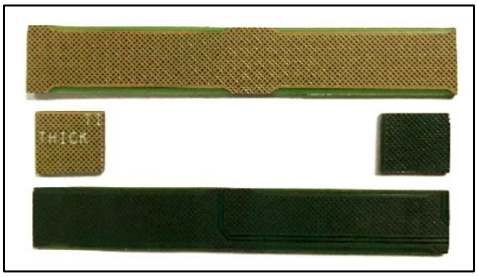

Figure 2- 2 TMA and DMA samples

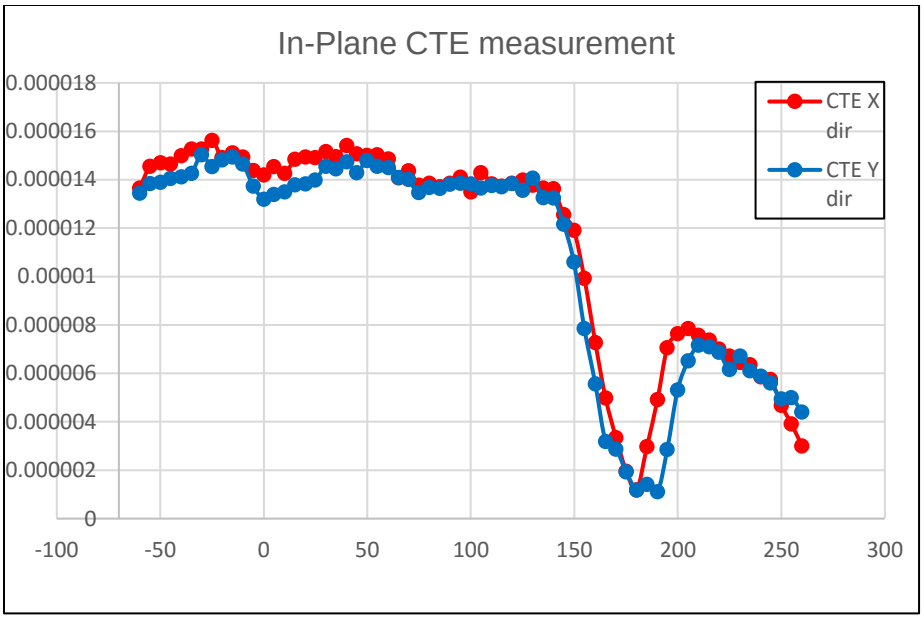

Figure 2- 3 In-Plane CTE for 1mm thick PCB

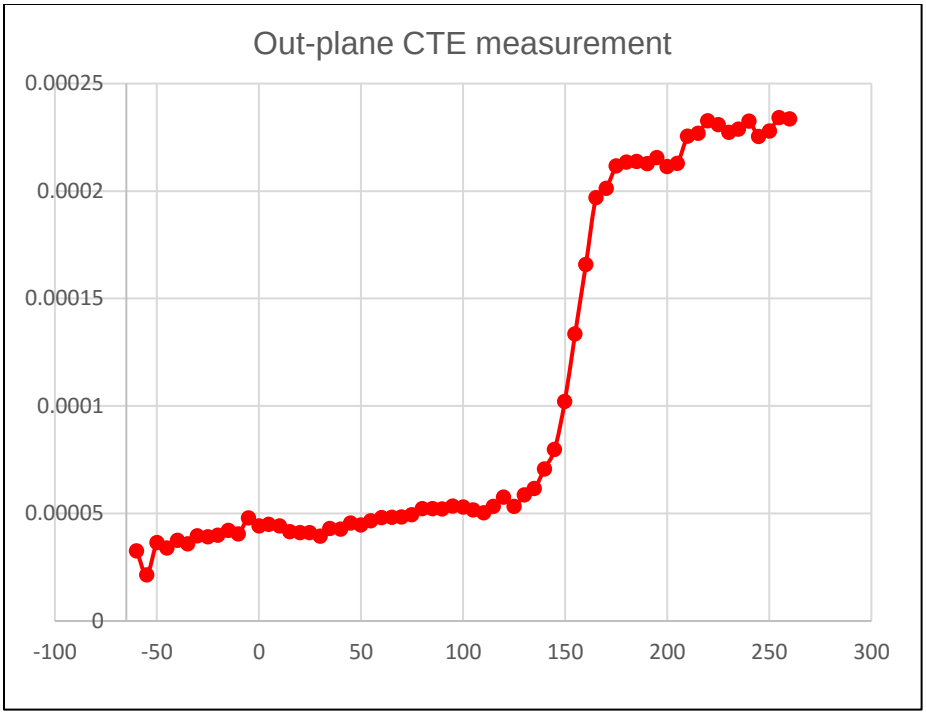

Figure 2- 4 Out-plane CTE for 1mm thick PCB

For both, CTE plots X-axis is temperature (°C) and Y-axis is CTE (ppm/°C)

Figure 2- 5 Sun Microsystems Oven

The oven was used to bake samples at the temperature of 125°C. Baked samples were used to determine CTE, Storage, and Loss Modulus values.

2.2 Young's Modulus (E)

Young's modulus in a numerical constant that describes the elastic property of the material when stretched or compressed in only one direction. Mathematically it can be defined as the stress produced in the material when some strain is applied to it.

$$E = \frac{\sigma}{\epsilon}$$

Where,

E - Young's Modulus (MPa)

σ - Stress (MPa)

∈ - Strain (mm/mm)

2.2.1 Instron Universal Testing Machine (UTM)

To determine Young's Modulus of 1mm thick PCB, an Instron UTM of 2 kN load cell was used to apply tensile loading to the bog-bone samples. Dog-bone samples were prepared as per the ASTM Standards [4]. An extensometer is placed on the sample to measure strain during sample extension. The extensometer is connected to a software to while the Instron is also connected and it gives in-situ force-displacement graph during the test. Stress is calculated by dividing the stress from the cross-sectional area of the sample and strain is measured using the extensometer. From the stress and strain, Young's Modulus is calculated for a sample.

Figure 2- 6 Instron Universal Testing Machine (UTM)

The length of the dog bone sample was 100mm with the width of 16mm. The length in the middle section was 33mm and the grip section was 30mm. A force per unit length of magnitude 2 N/m is applied to the samples.

2.2.2 Dynamic Mechanical Analyzer

Dynamic Mechanical Analysis measures the mechanical properties of materials as a function of time, temperature, and frequency. The term is also used to refer to the analyzer that performs the test. The amount of deformation is related to its stiffness. A force motor is used to generate the sinusoidal wave and this is transmitted to the sample via a drive shaft. One concern has always been the compliance of this drive shaft and the effect of any stabilizing bearing to hold it in position.

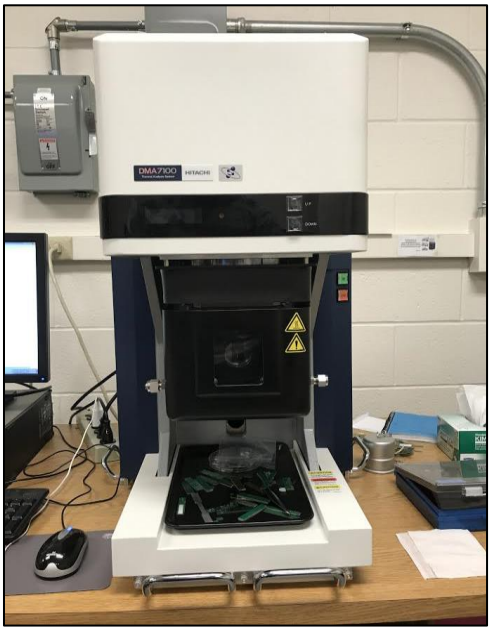

Figure 2- 7 Dynamic Mechanical Analyzer

For the DMA experiments, 3-point bend attachment was used for all the experiments.

All the measured values were temperature dependent. For computational analysis, all values for PCB was taken as temperature dependent for accuracy. The average fit value for CTE and Young's modulus are given in table 2-1.

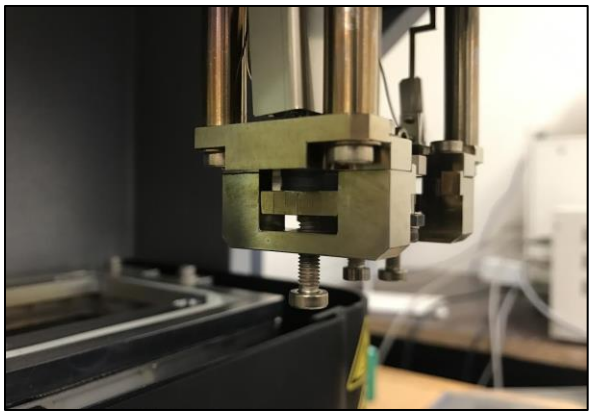

Figure 2- 8 DMA 3-point bending attachment

Table 2- 1 WCSP 1 mm thick board material properties

Board	Young's Modulus (GPa)	Poisson's ratio	CTE (ppm/°C)		
WCSP 1 mm PCB	15	0.39	X-dir	Y-dir	Z-dir
			15	14.5	50

Viscoelasticity is the property of materials that exhibit both viscous and elastic characteristics when undergoing deformation. The viscoelastic material properties of PCBs are characterized using dynamic mechanical analyzer (DMA). The frequency and temperature dependent complex moduli are obtained from the DMA.

Table 2- 2 WCSP material properties

Material	E (GPa)	CTE (ppm/°C)
Solder mask	4	60
Die	131	3
Mold	24	20
Cu Pad	110	17
UBM	50	16

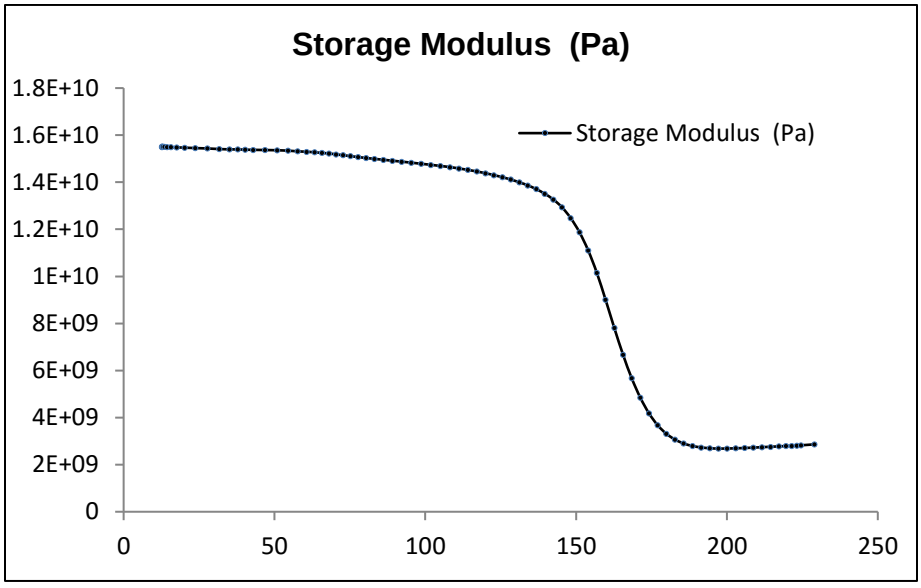

Figure 2- 9 Temperature and frequency dependent Storage Modulus of 1mm thick PCB

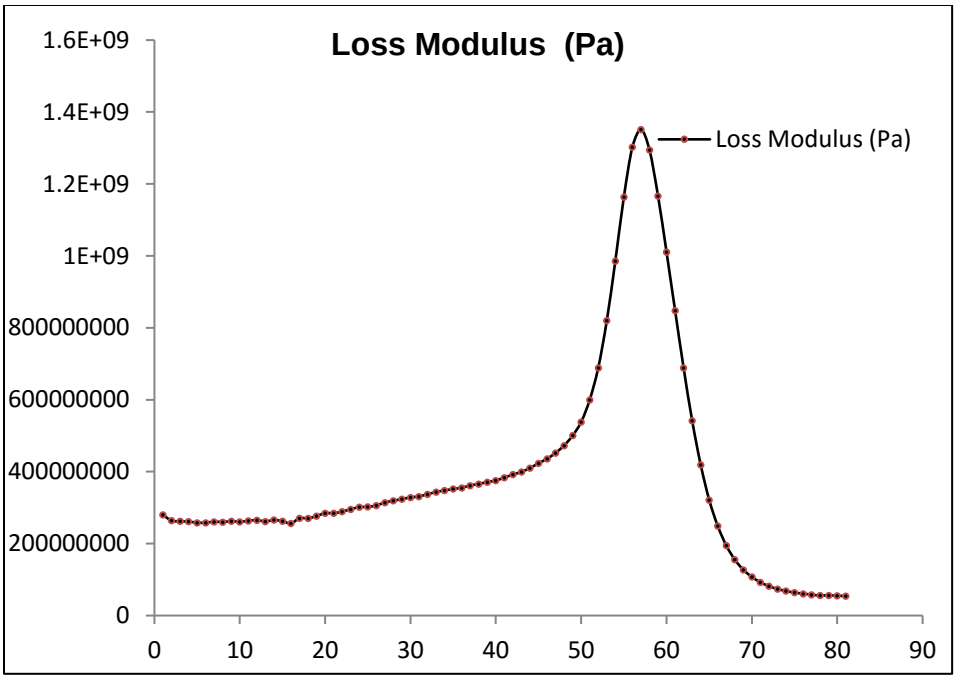

Figure 2- 10 Temperature and frequency dependent Loss Modulus of 1mm thick PCB

For the Solder balls of the WCSP, we used Anand's Viscoplastic Model because SAC396 has viscoplastic behavior. Solder ball properties are used for the computational study.

Table 2- 3 Anand's Viscoplastic Constants for SAC396

Sr. No	Constant	Unit	Value
1	s_0	MPa	3.3
2	Q/R	1/K	9883
3	A	sec^{-1}	15.7E+06
4	ξ	Dimensionless	1.06
5	m	Dimensionless	0.3686
6	h_0	MPa	1077
7	ŝ	MPa	3.15
8	n	Dimensionless	0.0352
9	a	Dimensionless	1.6832

Chapter 3

MODELING AND COMPUTATIONAL ANALYSIS

3.1 Outline

ANSYS 18.0 is being leveraged for modeling square WCSP. Quarter symmetry WCS package is modeled in same software, which was used to simulate the reflow condition and thermal cycling to analyze the various stresses developed within the critical solder joint and to predict the number of lifecycles to failure. The temperature boundary condition subjected to the model was 200°C. Four different square packages were modeled to study the effect of a change in a DNP. Die size varied for the all four different packages.

The void study was done on 7 X 7 array package for four different cases. Voids were modeled using the same software. Two independent loading conditions were tested to study thee developed strain and stress in the critical solder joint. Two independent loading conditions are Reflow condition and Thermal Cycling.

3.2 Modeling Methodology

3.2.1 Effect of change in DNP

To study the effect of a change in DNP and how will that affect the life of a package, ANSYS Design Modeler 18.0 was used to model 4 square packages. Jie-Hua Zhao et al. shown the different packages with a square and rectangular array of solder balls [5]. All the solder balls for different packages had the same dimensions. The PCB was modeled as a whole where the material properties were assigned to the block of PCB. Solder balls were modeled as viscoplastic material.

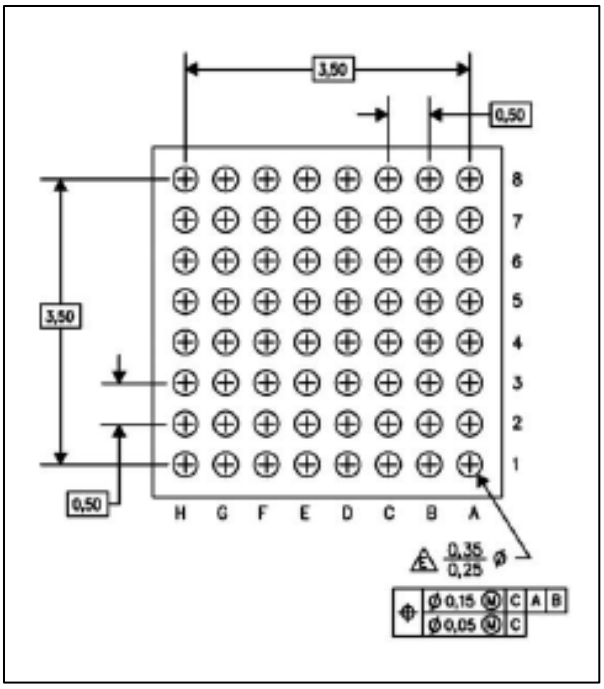

Figure 3- 1 Typical square package with 8 X 8 array of solder balls

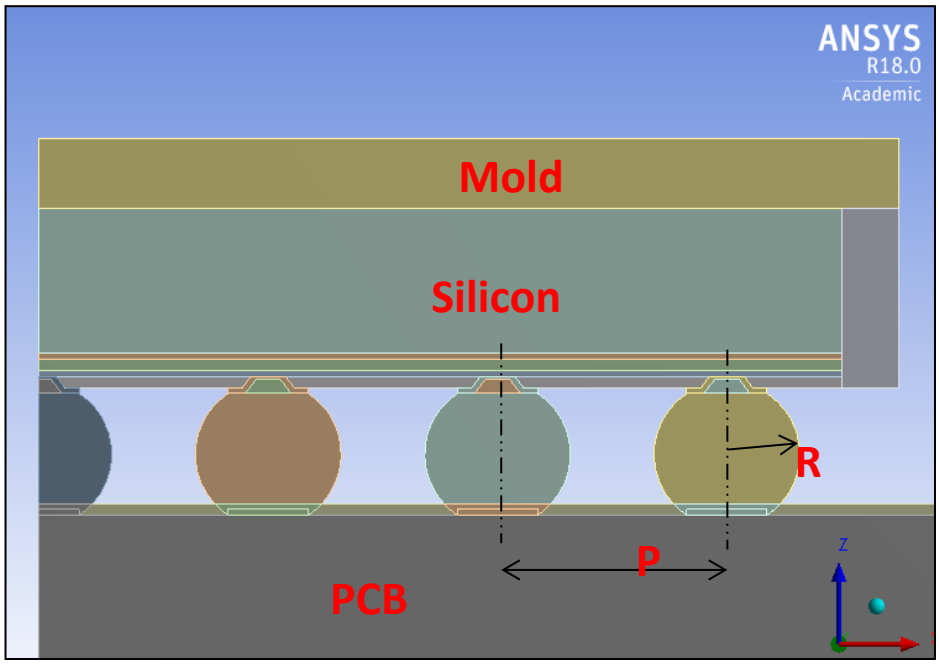

Figure 3- 2 WCSP modeled in ANSYS Design Modeler 18.0

Table 3- 1 Package and Solder ball dimensions

Component	Dimensions (mm)
Solder mask thickness	0.02
Cooper pad thickness	0.01
Solder ball pitch	0.14
Solder ball radius	0.12
Solder ball height	0.19

3.2.2 Void modeling in ANSYS

For the void study, three different cases were modeled in ANSYS Design Modeler 18.0 Void was modeled as Macro voids and Pinhole voids.

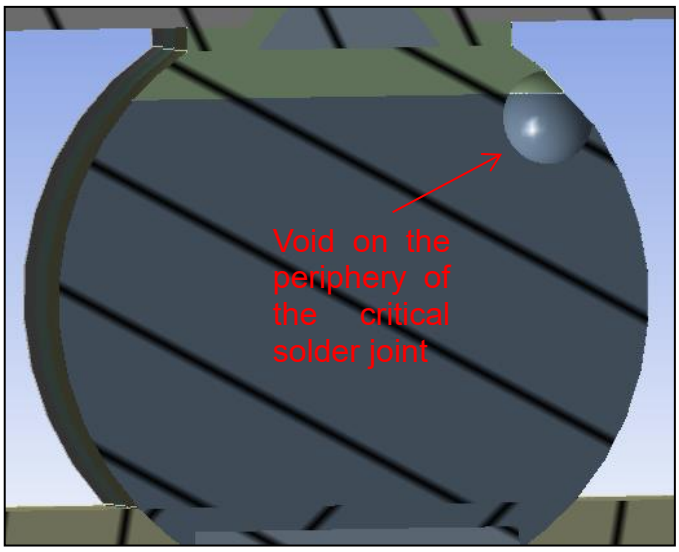

Figure 3- 3 Case I Void at the corner of critical solder joint

Case I- A macro void with spherical shape was modeled on the periphery of the critical solder joint. Spherical void has the diameter of 0.04 mm

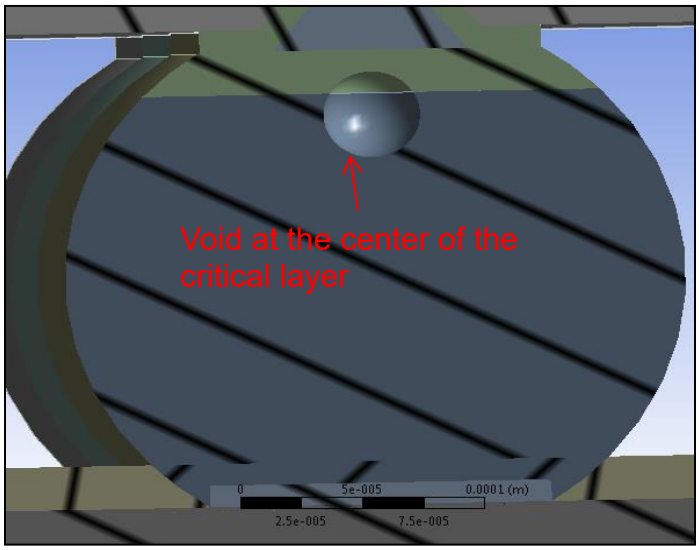

Figure 3- 4 Case II Macro void at the center of the critical layer

Case II- A spherical macro void was modeled with a diameter of 0.04 mm at the offset of 0.025 mm from the top of the solder ball.

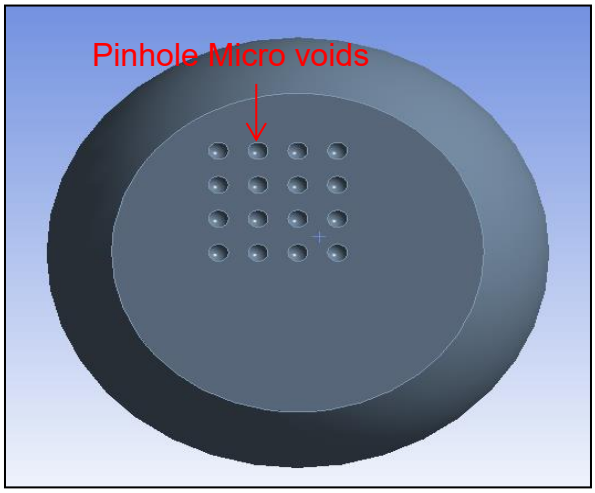

Figure 3- 5 Case III Pinhole micro voids at the top of the solder ball where it connects with critical solder layer

Case III- Pinhole micro voids are also spherical in shape. They were modeled in same software with the diameter of 0.01 mm.

Case IV- Macro void at the center of critical corner solder ball

3.3 Contact Summary and Meshing

3.3.1 Contact Summary

The geometry of WCSP with PCB is a complex geometry. ANSYS Workbench will assign the bonded contacts automatically. Many time automatic contacts are far open still they will be shown as bonded in the contact section. Due to this, it makes geometry rigid and which may affect results.

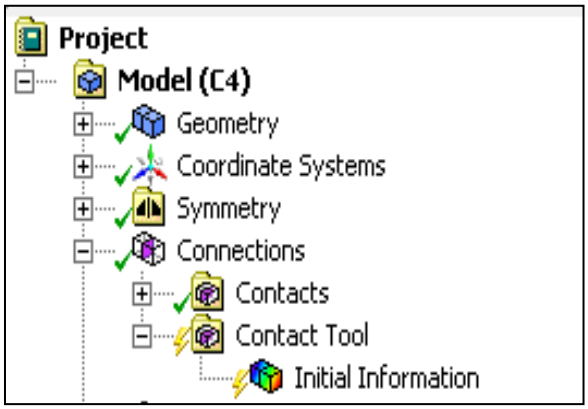

Figure 3- 6 Model tree showing Contact Tool

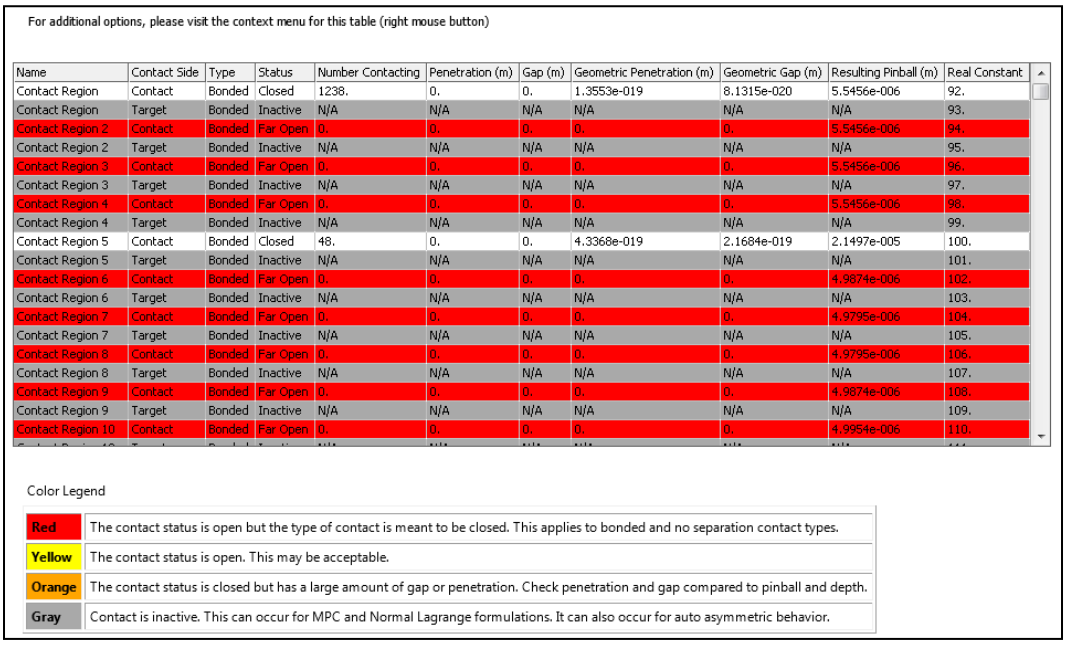

Figure 3- 7 Contact regions showing different contacts

Contact tool was used to generate initial information for all the contact regions in the geometry. Far open contacts were deleted and manually contacts were assigned where ever necessary.

3.3.2 Meshing

The meshing of the complex geometry is a crucial part of the computational study. Meshing is one of the most critical steps in the FEA. Larger the number of elements results in the better approximation in the solution. An excess number of elements may cause around off error in some of the cases. To avoid this error the meshing should be fine or coarse inappropriate region. Mesh sensitivity analysis can be considered to reduce the computational time while maintaining the accuracy of the solution [5]. An attempt is made to use hex-dominant mesh where ever possible in the geometry. Mesh sensitivity analysis was carried on one of the square packages to predict what should be the maximum number of elements in the geometry.

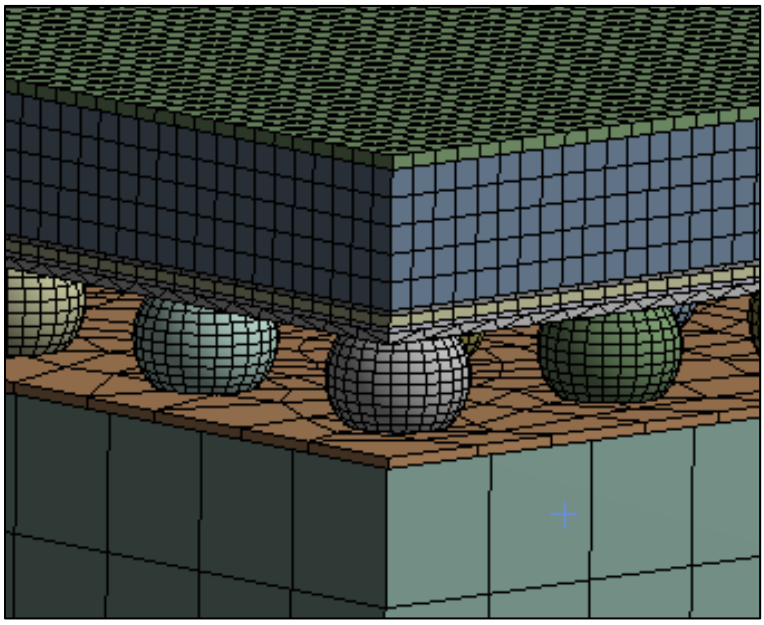

Figure 3- 8 Meshing of 8 X 8 array square WCS Package

Mesh sensitivity analysis carried out on 2 X 2 square package was an attempt to predict the maximum number of elements. This made easier to mesh differently sized package geometries.

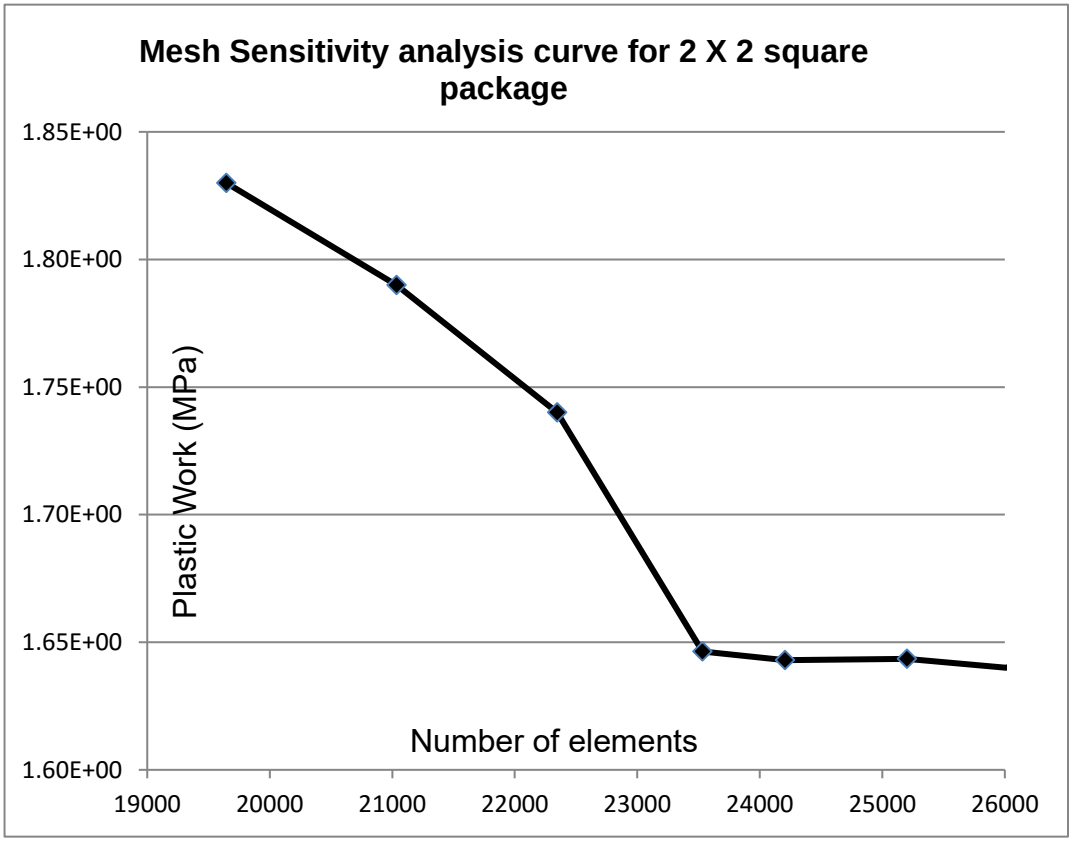

Figure 3- 9 Mesh Sensitivity analysis curve

Mesh sensitivity is an index to show how the mesh quality influences the calculation results. You can use the different dimension mesh to calculate, then analyze the differences. The best mesh is that it has the same calculation resolution as the smaller mesh and this mesh bigger than its have worse resolution than it.

3.4 Loading and Boundary Conditions

Loading and Boundary condition are the pillars of FE analysis. Loading and boundary conditions should be accurate to simulate realistic results. All the different sized packages were tested for two loading conditions Thermal Cycling and Reflow condition [8]. Boundary conditions for all the simulations were same.

3.4.1 Assumptions

- Each layer in the package is perfectly bonded to other.
- All materials except solder alloy (SAC396) are modeled using linear elastic material properties.
- Time and temperature dependent material properties were used from Anand's Viscoplastic Model to capture the inelastic behavior of SAC396.
- All components considered stress free at 200°C (reflow temperature).

3.4.2 Boundary Conditions

- Symmetry boundary conditions were taken at the Quarter symmetry faces.
- The common vertex of the PCB was fixed (All DOF zero) to restrict any rigid body motion.

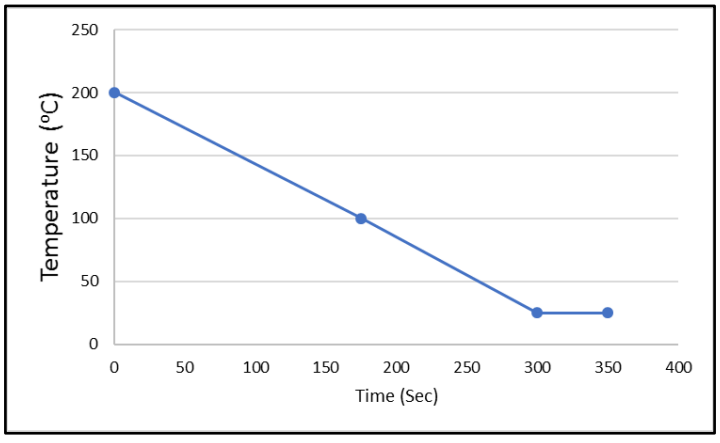

Figure 3- 10 Reflow condition

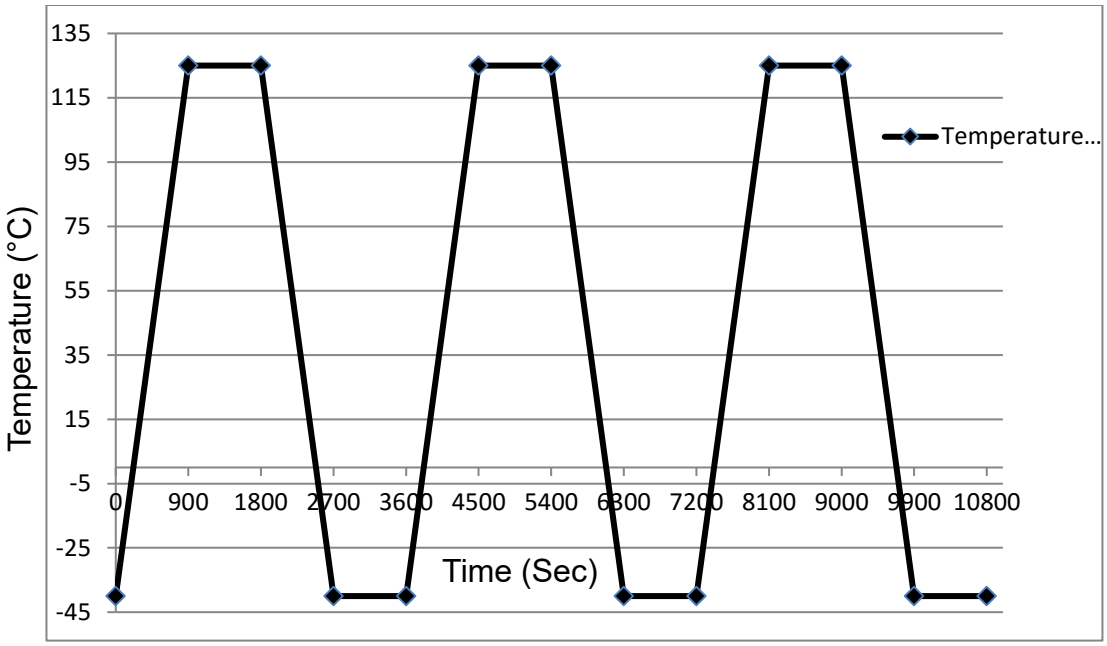

Figure 3- 11 Thermal cycling temperature profile

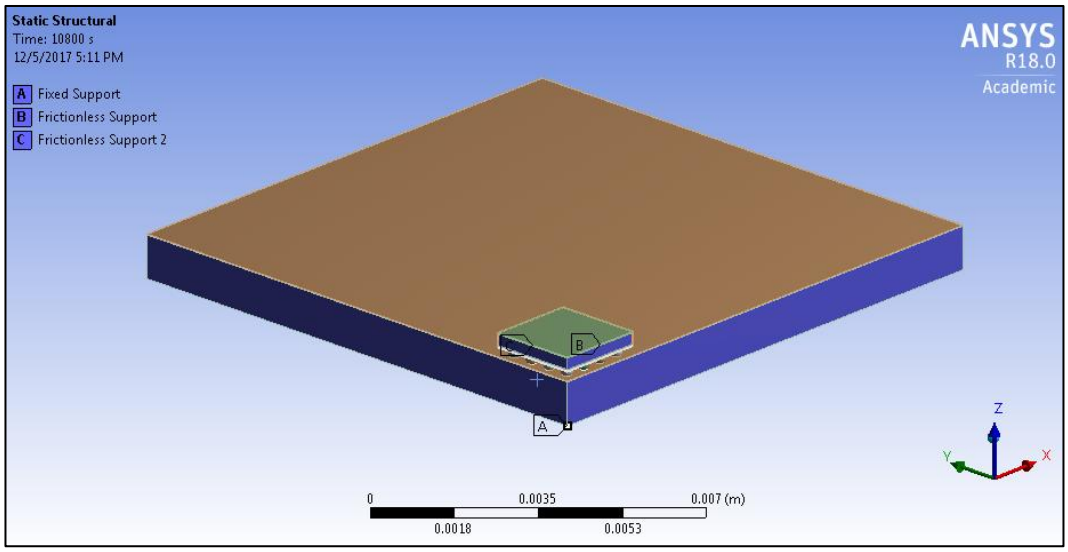

Figure 3- 12 WCSP showing fixed and frictionless supports

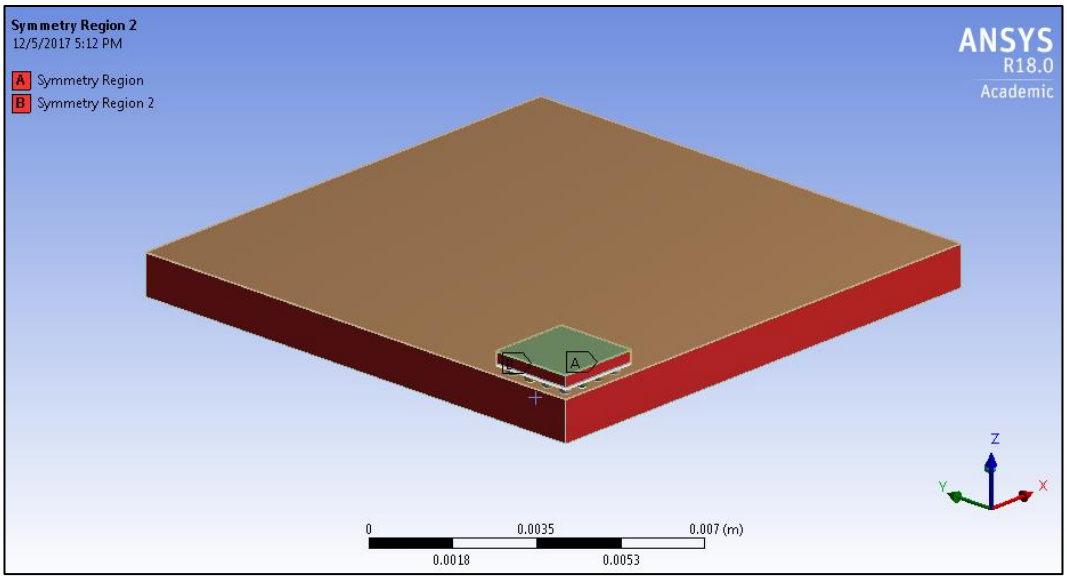

Figure 3- 13 Symmetry regions applied to quarter geometry

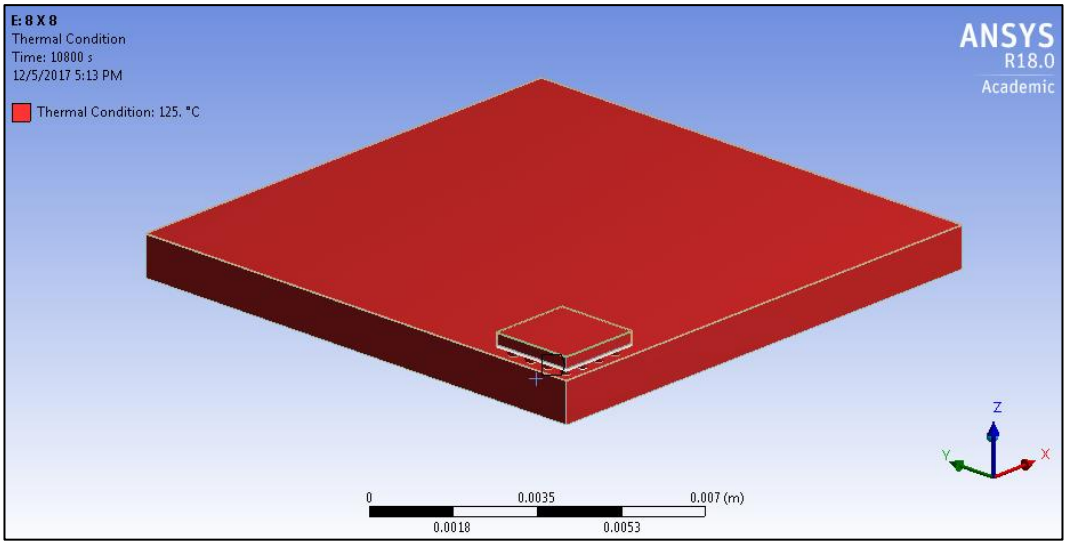

Figure 3- 14 Uniformly distributed thermal load throughout the body

Chapter 4

RESULTS AND CONCLUSIONS

4.1 Results

4.1.1 Results for effect of change in DNP

To study the effect of a change in DNP we studied four different square packages. The comparison was done by predicting the number of lifecycles to failure for all the different packages. Total inelastic strain and von-mises stress in the critical (corner) solder ball were used as correlation parameters to predict the number of life cycles to failure. The total strain and equivalent von-Mises stress in the critical ball as determined from the ANSYS model. Volume averaged plastic work was calculated by writing an APDL script in the ANSYS commands using the stress and strain values from the FEA model. This volume averaged plastic work was related life cycles to failure using Schubert et al. [6] and Che & Pang [7] correlation

$$N_f = \left(\frac{A}{\Delta W}\right)^k$$

Where N_f is the characteristic life. A (in MPa) and k (unitless) are two empirical fatigue parameters that were used from Jie et al. work on chip scale packages [8]. The values of A and k used were A = 8.783 x 106 (MPa) and, k = 0.4701

Table 4- 1 FE analysis results for 4 different packages

Package array	I/Os (interconnects)	DNP (mm)	Number of lifecycles to failure (N_f)	Plastic Work (ΔW)
2 X 2	4	0.35	2113	0.7421
5 X 5	25	1.14	1859	0.9747
7 X 7	49	1.7	1519	1.4982
8 X 8	64	2.48	1453	1.6464

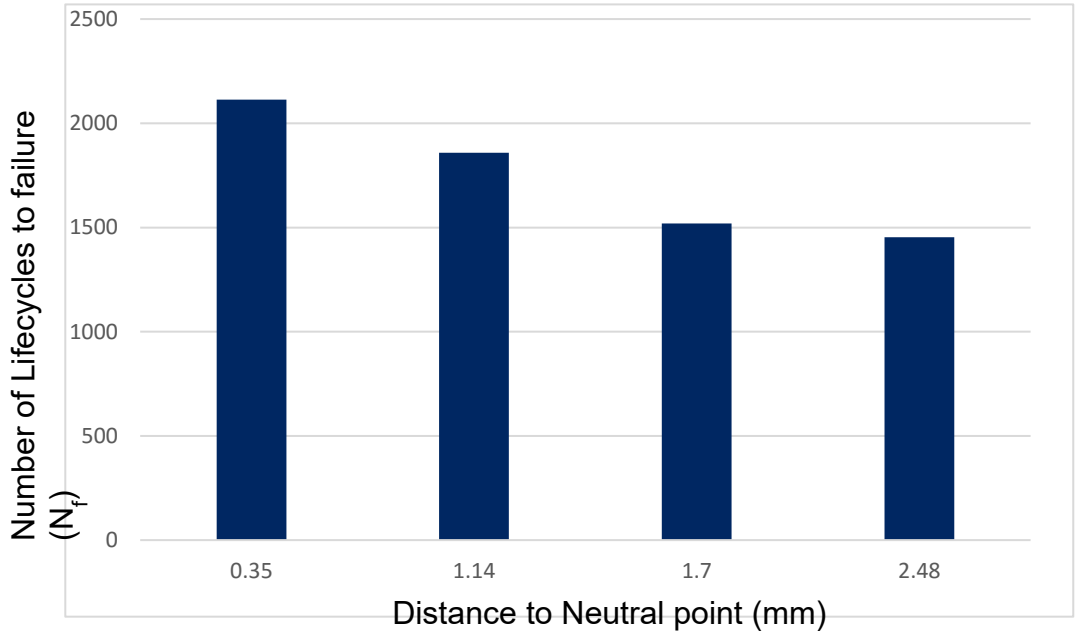

Figure 4- 1 Graph showing decrease in the number of lifecycles to failure with increase in DNP

MATLAB code was developed to solve multiple linear regression to find out the correlation between N_f, I/Os, and DNP.

```
Number of observations: 4, Error degrees of freedom: 1
Root Mean Squared Error: 31.7
R-squared: 0.997,  Adjusted R-Squared 0.99
```

Figure 4- 2 Linear regression equation was solved using MATLAB code

R Square shows 0.997 which is a very good fit. 99% of the variation in the life cycle is explained by the in depended variables I/Os and DNP. It shows a strong relationship and influence from I/Os and DNP. Also, the linear regression equation of life cycle involved I/O and DNP could be approximately

Number of lifecycles to failure (N_f) =2066.2 – 23.516(I/Os) +354.91(DNP)

Table 4- 2 Comparison of FE analysis and Linear regression equation

Package array	I/Os	DNP (mm)	N_f(FE Analysis)	N_f(Regression equation)	% error
7 X 7	49	1.7	1519	1517	0.01

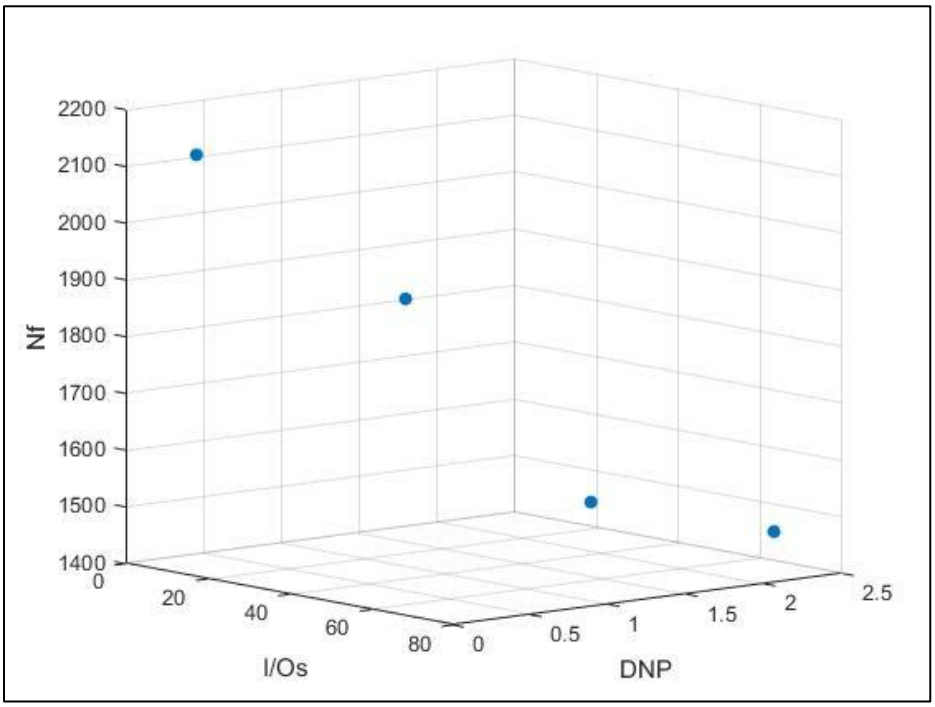

Figure 4- 3 Curve fitting for linear regression (MATLAB output)

4.1.2 Results for Void study

Table 4- 3 Results for four different cases

	Plastic Work (MPa)	Equivalent strain (mm/mm)
Case I	0.17	4.45e-4
Case II	0.19	4.46e-4
Case III	0.21	4.53e-4
Case IV	0.19	4.77e-4

Table 4- 4 Results for Maro-void at the center of critical solder ball

Volume % of critical solder ball with void and void radius (mm)	Thermal Cycling			Reflow condition	
	Plastic Work (MPa)	von-Mises Stresses (MPa)	Equivalent Strain*10^-4 (m/m)	von-Mises stresses (MPa)	Equivalent Strain*10^-4 (m/m)
98% and 0.06 mm	0.18	23.79	4.8	10.95	2.38
96% and 0.08 mm	0.17	23.25	4.7	10.61	2.305
93% and 0.10 mm	0.15	22.63	4.62	10.08	2.19
88% and 0.12 mm	0.13	21.87	4.46	9.42	2.04
81% and 0.14 mm	0.11	21.12	4.31	8.93	1.94
72% and 0.16 mm	0.1	20.38	4.16	8.85	1.92

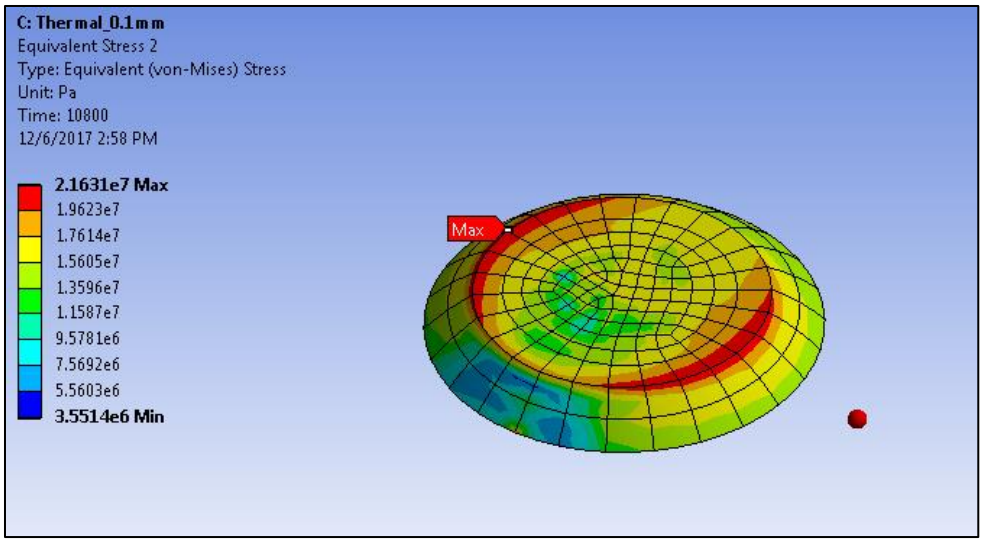

Figure 4- 4 Equivalent stress on the critical layer of the corner solder ball under Thermal Cycling

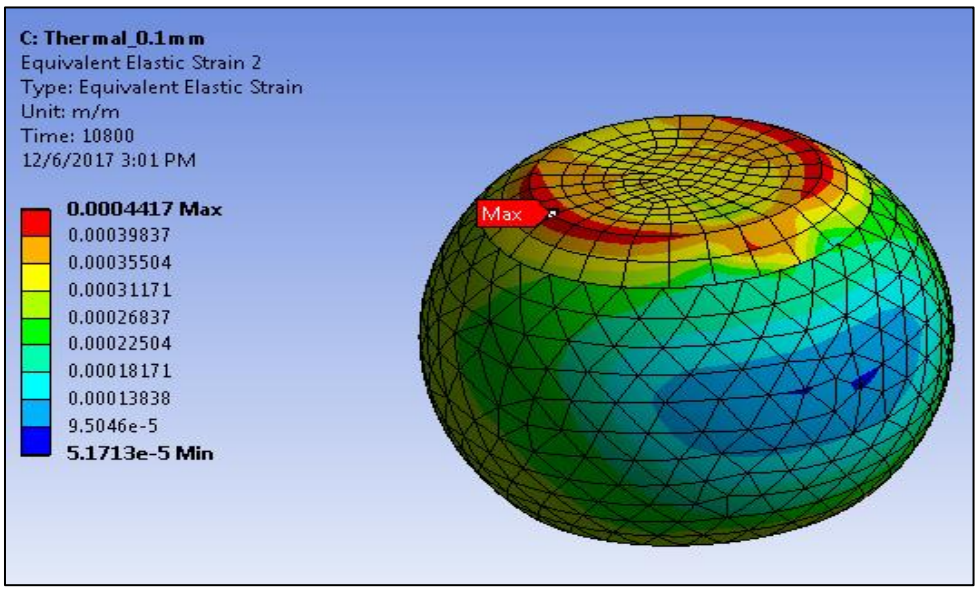

Figure 4- 5 Equivalent strain on the critical solder ball under Thermal Cycling

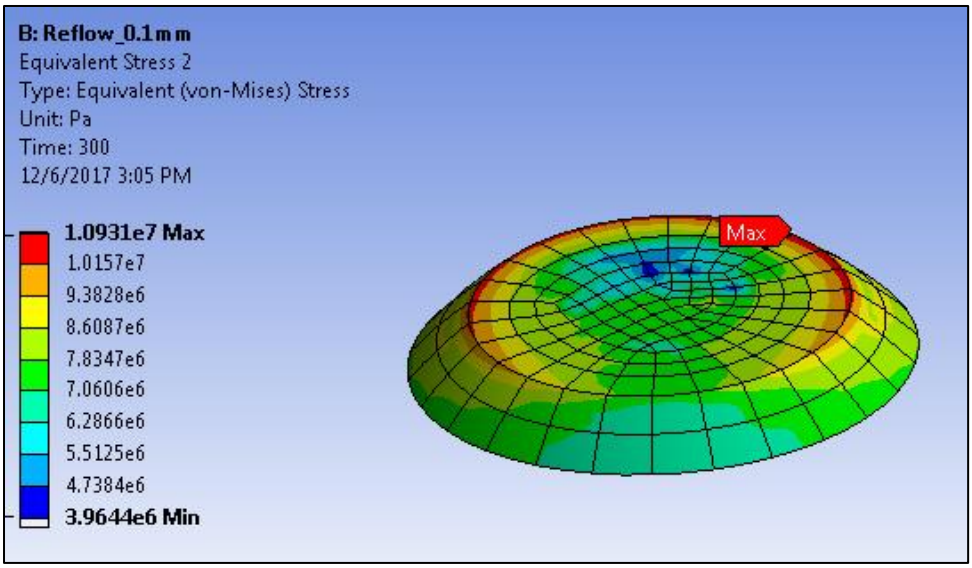

Figure 4- 6 Equivalent stress on the critical layer of the corner solder ball under Reflow Condition

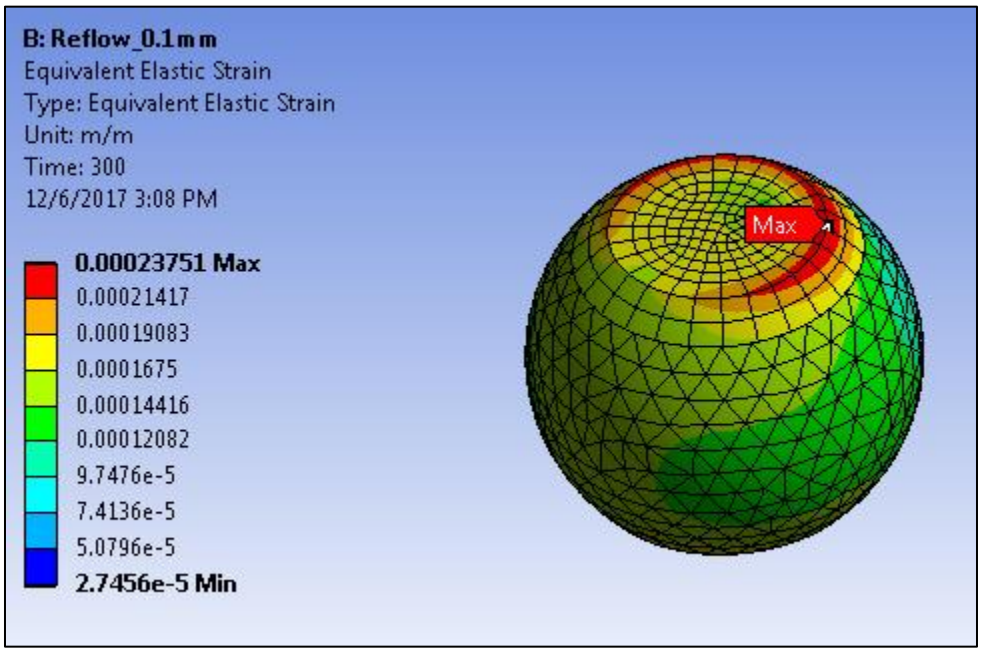

Figure 4- 7 Equivalent strain on the critical solder ball under Reflow Condition

4.2 Conclusion

We can conclude that successful characterization of PCB to predict its reliability via FEA. UTM, DMA, and TMA were leveraged to find Young's Modulus and temperature dependent CTE. Von Mises equivalent stress, and equivalent elastic strain are obtained from FEA and results were studied. Successfully studied the effect of a change in the DNP and voids on SJR of WCSP. DNP study clearly shows that with a decrease in DNP we get an increase in the number of cycles to failure. DNP can be reduced to considerably number but the cost to design and manufacturing should be considered on another hand. Linear regression was used to find out the correlation between N_f, DNP, and I/Os which showed 0.01% error compared to the FE results. Successfully modeled voids at different locations of the solder ball, including at different locations in the critical layer. It has been identified that the failure due to void depends on the location and its size. The probability of maximum failure due to void can occur from a macro void in the center of the critical layer.

Chapter 5

FUTURE WORK

- Effect of Scribe width length can be studied for different square packages as well as rectangular packages

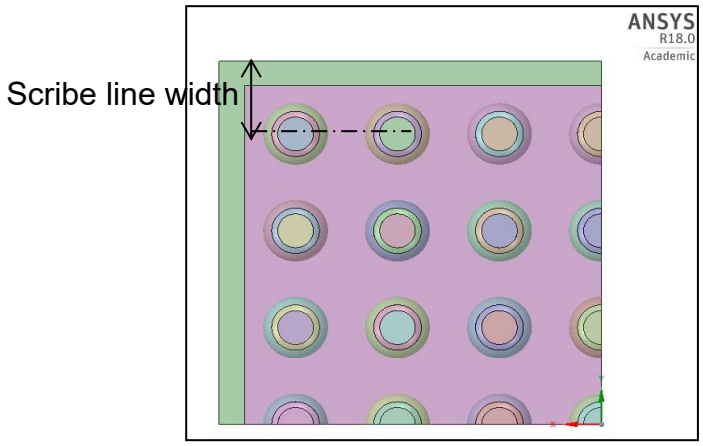

Figure 5- 1 Scribe line width for the WCSP

- More differently sized packages should be used to predict N_f for square and rectangular packages
- A parametric study conducted to evaluate the effect of voids only assesses the effect of voids on the durability of WCSP interconnects under thermo-mechanical loading. The effect of voids has not been investigated in other types of interconnects and other types of loading such as shock, drop, or vibration and remains for future investigations
- Crack propagation study due to voids in solder interconnects can be done
- Different shapes of voids can be studied for different loading conditions as we know shape of void will not be always spherical

Appendix A

MATLAB Code for Linear Regression equation

```
% The University of Texas at Arlington
% EMNSPC Lab
% Author- Aniruddha Doiphode, MS Mechanical Engineering
clear all;
clc;
x1= [4; 25; 49; 64]; % IO
x2= [.35; 1.14; 1.7; 2.48]; %DNP
y= [2113; 1859; 1513; 1453]; %Nf



X= [ones(size(x1))  x1 x2];
b= regress(y,X);


scatter3(x1,x2,y,'filled')
hold on

x1fit = min(x1):10:max(x1);
x2fit = min(x2):10:max(x2);
[X1FIT,X2FIT] = meshgrid(x1fit,x2fit);

YFIT = b(1) + b(2)*X1FIT + b(3)*X2FIT;

xlabel('I/Os')
ylabel('DNP')
zlabel('Nf')
view(50,10)


mdl = fitlm(X,y)
```

Appendix B

APDL Script to calculate the plastic work

```
!APDL SCRIPT TO CALCULATE PLASTIC WORK
/post1
allsel,all
!CALC AVG PLASTIC WORK FOR CYCLE1
set,4,last,1 !LOAD STEP
cmsel,s,Critical,elem !ELEMENT FOR VOL AVERGAING
etable,vo1table,volu
pretab,vo1table
etable,vse1table,nl,plwk !PLASTIC WORK
pretab,vse1table
smult,pw1table,vo1table,vse1table
ssum
*get,splwk,ssum,,item,pw1table
*get,svolu,ssum,,item,vo1table
pw1=splwk/svolu !AVERAGE PLASTIC WORK
!CALC AVG PLASTIC WORK FOR CYCLE2
set,8,last,1 !LOAD STEP
cmsel,s,Critical,elem
etable,vo2table,volu
pretab,vo2table
etable,vse2table,nl,plwk !PLASTIC WORK
pretab,vse2table
smult,pw2table,vo2table,vse2table
ssum
*get,splwk,ssum,,item,pw2table
*get,svolu,ssum,,item,vo2table
pw2=splwk/svolu !AVERAGE PLASTIC WORK
!CALC DELTA AVG PLASTIC WORK
pwa=pw2-pw1
!CALC AVG PLASTIC WORK FOR CYCLE3
set,12,last,1 !LOAD STEP
cmsel,s,Critical,elem
etable,vo3table,volu
pretab,vo3table
etable,vse3table,nl,plwk !PLASTIC WORK
pretab,vse3table
smult,pw3table,vo3table,vse3table
ssum
*get,splwk,ssum,,item,pw3table
*get,svolu,ssum,,item,vo3table
pw3=splwk/svolu !AVERAGE PLASTIC WORK
!CALC DELTA AVG PLASTIC WORK
pwb=pw3-pw2
my_pwb=pwb
my_pwa=pwa
my_pw1=pw1
my_pw2=pw2
my_pw3=pw3!   Commands inserted into this file will be executed immediately after
the ANSYS /POST1 command.
```

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Biographical Information

Aniruddha Doiphode received his Bachelor's degree in Mechanical Engineering from University of Pune, Pune, India, in May 2014. He worked as CAE Trainee at F. E. Solutions Pvt. Ltd., Pune. During his work at F. E. Solutions, he worked on different Mechanical design and analysis projects. He started studying Master's in Mechanical Engineering at the University of Texas at Arlington from Fall 2015. He joined the Electronics MEMS & Nanoelectronics Systems Packaging Center (EMNSPC) under Dr. Dereje Agonafer in 2015 and developed a keen interest in reliability and design of electronic packages. His research interest includes reliability, design, thermo-mechanical simulation and material characterization.

During his graduate studies, he was an integral part of the SRC-funded project where he worked closely with the industry liaisons. As a Treasurer of Surface Mount Technology Association (SMTA) UT Arlington student chapter, he was actively involved in all the events and a technical meeting of SMTA. Aniruddha Doiphode is a co-author of research papers published in well-known technical conferences. Upon graduation, Aniruddha Doiphode plans to pursue his career in the field of Mechanical Design Engineering. He will be working as a Product Design Engineer with Cummins Inc. starting from January 2018.