RELIABILITY ASSESSMENT OF SOLDER JOINT USING BGA PACKAGE – MEGTRON 6 VERSUS FR4 PRINTED CIRCUIT BOARDS USING DROP TESTING

by

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Abstract

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In electronic industry Ball grid array (BGA) package, surface mount technology has been used widely, due to its robust design, high density connections and improved performance. In surface mount technology, solder joints are used to interconnect package and PCB board assembly. High frequency laminates use in PCB boards provides excellent performance for high speed, frequency devices. Nelco 4000-13EPSI, Panasonic Megtron 6, and Rogers 4350B are few popular laminates. Component size reduction and structural complexity because of increasing number of transistors are making it very difficult to protect the packages from mechanical, thermal, and electrical damage. Difference in material properties between PCB board and package like coefficient of thermal expansion(CTE) generates excessive warpage, solder mask cracking, and bump cracking generally at the solder ball and package or solder ball and PCB board interface. Therefore, board level reliability(BLR) testing of these devices under thermal, and mechanical loading has because most important task. It includes temperature cycling, thermal shock, drop test, vibration, and mechanical bending test. The percentage of failure due to mechanical stress generation is much more then thermal loading. Board level drop testing has been used widely to study effect of mechanical impact loading. Finite elemental modeling software Ansys 16.1 is use because of complexity, high cost and time requirement of experimental method. Input G method is used for dropping testing analysis imitates all the conditions of physical test model. In this study performance of high frequency laminates FR4 and Megtron6

board with BGA package has been compare based on maximum peeling stress, strain rate and deformation magnitude.

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Chapter 1

INTRODUCTION

1.1 Electronic Packages

In electronic field, packages used for the manufacturing of printed circuit board(PCB) has been used widely with high demand of high frequency high speed devices. Advancement of integrated circuit (ICs) from transistors, and vacuum tube made major transformation in packaging industry. PCB are the physical devices mainly called as brain of the power device, It Protects ICs from external environment, accelerate heat dissipation, and ease handling. PCB comes into two variety e.g. single or double-sided also called as multi-layered PCB. Multi-layer PCB offers high assembly density, flexibility, controlled

impedance features, good EMI shielding, and less weight eliminating interconnection wiring harness. The cross-section view of a multi layered PCB is shown in the figure 1.1.

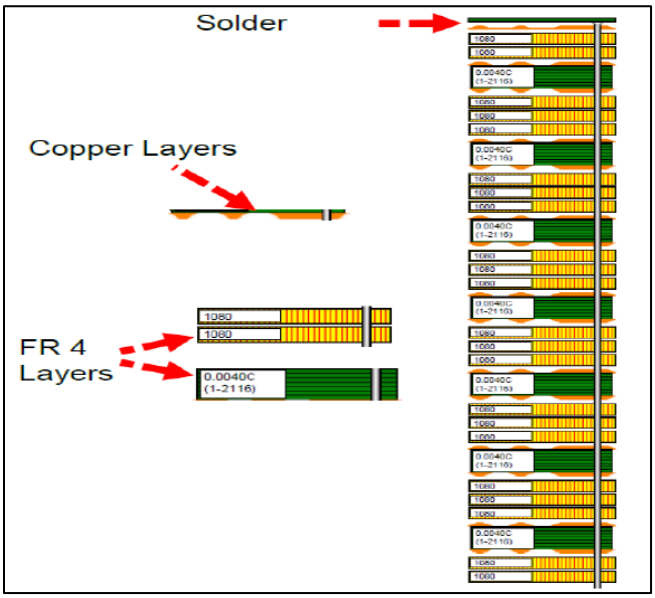

Figure 1.1: Cross-section of a 16 layered PCB

1.2 High Frequency Laminates

According to Moore's law, "The overall processing power for computers will double every two years" i.e. the number of transistors in a CPU would double in every two years. With increase in functions and pin count, size of ICs is getting smaller and complex day by day with Progression of ICs into LSIs, VLSIs, and to ULSIs. It necessitates the use of high frequency laminates for better and improved electrical performance. Epoxy-based FR-4 laminate has been used widely for the PCB production because of good reliability, low cost, excellent mechanical and electrical characteristics. But, as the frequency increases dissipation factor (Df), insertion loss, impedance loss increases which necessitates the innovation of high frequency material. High speed, high frequency laminates like Nelco N4000-13, Isola FR408, and

Panasonic Megtron 6 are replacing FR-4 laminate day by day (mugdha 1). The improved electrical performance, better impedance control, low moisture absorption, good thermal management are few advantages of high frequency laminates over FR4 (Coonrod 3).The FR-4 laminate used in the study has 8 layers (1-6-1) of copper, and the Megtron 6 has 18 layers (1-16-1) of copper, with 2mm of thickness.

Component	**Dimensions (mm)**
Package	6 x 6 x 0.74
Die	4.5 x 4.5 x 0.28
Solder ball pitch	0.5
Solder ball diameter	0.3
Solder ball height	0.2
Solder mask thickness	0.05
Substrate thickness	0.05
Copper pad thickness	0.04

Table 1.1 Package Dimensions

In Ball grid array(BGA) solder ball which are used to interconnect the printed circuit board(PCB) and integrated circuit(ICs) are arranged in grid pattern. The copper pads on PCB allows conduction of electric signal from ICs to PCB through solder balls. Instead of perimeter, In BGA whole bottom surface of ICs used for the solder ball interconnections also called as area array package. Figure 1.2 shows outline of Ball grid array package.

Figure 1.2 Ball grid array package

For the assembly of solder ball, ICs along with BGA solder balls place on top of PCB. Heat generated by reflow over or infrared heater used to melt solder balls, and surface tension helps to hold the package in alignment with solder ball.

BGA packages are available in various types

- HSBGA – BGA with heat spreader
- FCBGA – flip chip BGA
- CSBGA – cost saving BGA
- FCHSBGA – flip chip BGA with heat spreader
- FBGA: fine pitch ball grid array, with a square or rectangular array of solder balls on one surface
- LBGA : Low Profile Ball Grid Array
- TEPBGA: Thermally Enhanced Plastic BGA
- CBGA: Ceramic Ball Grid Array
- OBGA: Organic Ball Grid Array

- TFBGA – thin fine pitch BGA.
- PBGA: Plastic Ball Grid Array
- μBGA – micro-BGA, with ball spacing less than 1 mm
- LFBGA – low profile fine pitch ball grid array
- TBGA: Thin Ball Grid Array

For the study purpose, FCBGA flip chip ball grid array has been selected because of advantages like reduced signal inductance, power/ground inductance, and package footprint, along with higher signal density and die shrink (Texas Instruments 13). Two-metal layer or multi-layer are two basic types of flip chip BGA packages, where high-density organic laminate or ceramic substrates are generally used for assembling. Figure 1.3 shows A flip chip ball grid array package (FCBGA) (Texas Instruments 13)

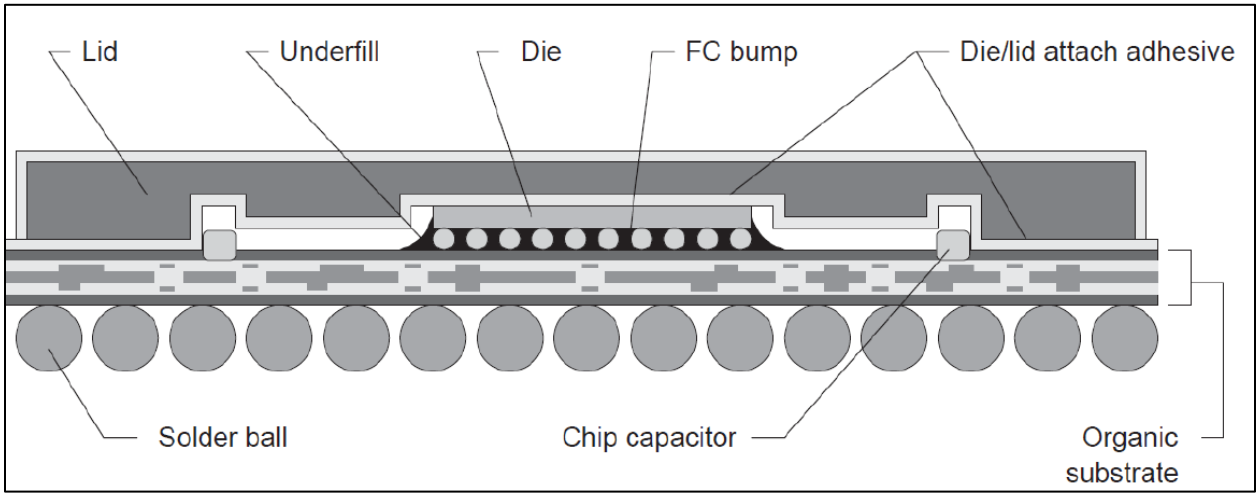

Figure1.3 Flip Chip Ball Grid Array Package (FCBGA) [Texas Instruments]

Higher pin counts or smaller package size plus high rate of manufacturing are the major reason behind replacing QFPs with BGAs. Additionally, BGA also Increases electrical performance because high grid density, higher power dissipation, Lower overall production costs (Swedish National Research Program 2).

1.3 Motivation

With increase in recent trend of miniaturization of the portable electronic devices such as digital cameras, calculators, cell phones, palm size PCs, the useful service life is decreasing because of drop impact on comparatively hard surface. Portable telecommunication industry, failure due to drop impact is one of the most prevalent failure modes of portable telecommunications (Wu, Guosho, Yeh, and Wyatt 11). In drop impact, vibration causes bending of board which produces stress in solder interconnects. This causes failure of solder joints, intermetallic layers or solder-pad interface. Several experiments have been performed to detect the effect of drop on performance of electronic packages (Tee et al. 7). The reliability of IC package depends board design, construction, material, thickness, and surface finish, interconnect material and the component size. Product level or board level test are performed to measure reliability of an electronic package. Board level reliability performance tests are widely used considering the scope for the improvement before building the complete product.

Computer-aided software finite element modeling (FEM) have become very popular to analyze the reliability performance of electronic package because of less computation time, low cost solution, user friendly methodology, accuracy of result. Nowadays, it is also replacing traditional experimental analysis methods. Finite element modeling involves the steps like validated FEM models, the Design of Experiment (DOE), material properties, geometry, and test conditions (Tee et al. 7).

1.4 Objective

The present work of this thesis focuses on the finite element modeling of the dynamic behaviors for BGA packages under impact loading on a JEDEC Standard test board. The main objectives of this study are followings:

Study of the dynamic behaviors of FR4, Megtron boards under the JEDEC drop test.

- Perform the modal analysis on the boards.
- Application of sub-modeling technique to study the local dynamic stress behaviors.
- Compare equivalent stresses, equivalent strains, and directional deformations.

Chapter 2
LITERATURE REVIEW

Reliability of solder joint of a BGA package on FR4 and high frequency Megtron series laminates under accelerated thermal cycling in her thesis work (Chaudhari 1). Her results showed that under accelerated thermal cycling high frequency Megtron series perform well over FR4. Her work gave insight to perform similar reliability analysis on high frequency laminates under impact loading. A step by step guide on drop impact test has been published by JESD22-B111 (1) to perform drop level reliability testing of PCB. John Coonrod (3) has compared FR4 and high frequency laminates based on material properties,

circuit fabrication issues, reliability issues, electrical performance, and its application. Unique Rahangdale (4) worked on reliability of RCC and FR4 BOARDS which helped to list down its advantages based on directional deformation, equivalent stresses and strains, change in plastic. The product level drop impact tests at different impact orientations, drop height conducted by Liam and Low presented contribution of each parameter on reliability of electronic packages. Drop impact simulation life prediction model by Tee, et al. (15) correlated analytical and experimental reliability failure results. Sub-modeling technique to perform BGA drop testing has performed by Zhu (18).

2.1 JEDEC Drop Test Method

Joint Electronic Device Engineering Council (JEDEC) is an organization works on microelectronic technologies, they have provided standards to measure performance of electronic package in case of board level drop testing. The standard test set up consists of PCB assembly, test apparatus. The detail representation of experimental drop testing setup shown in figure 2.1.

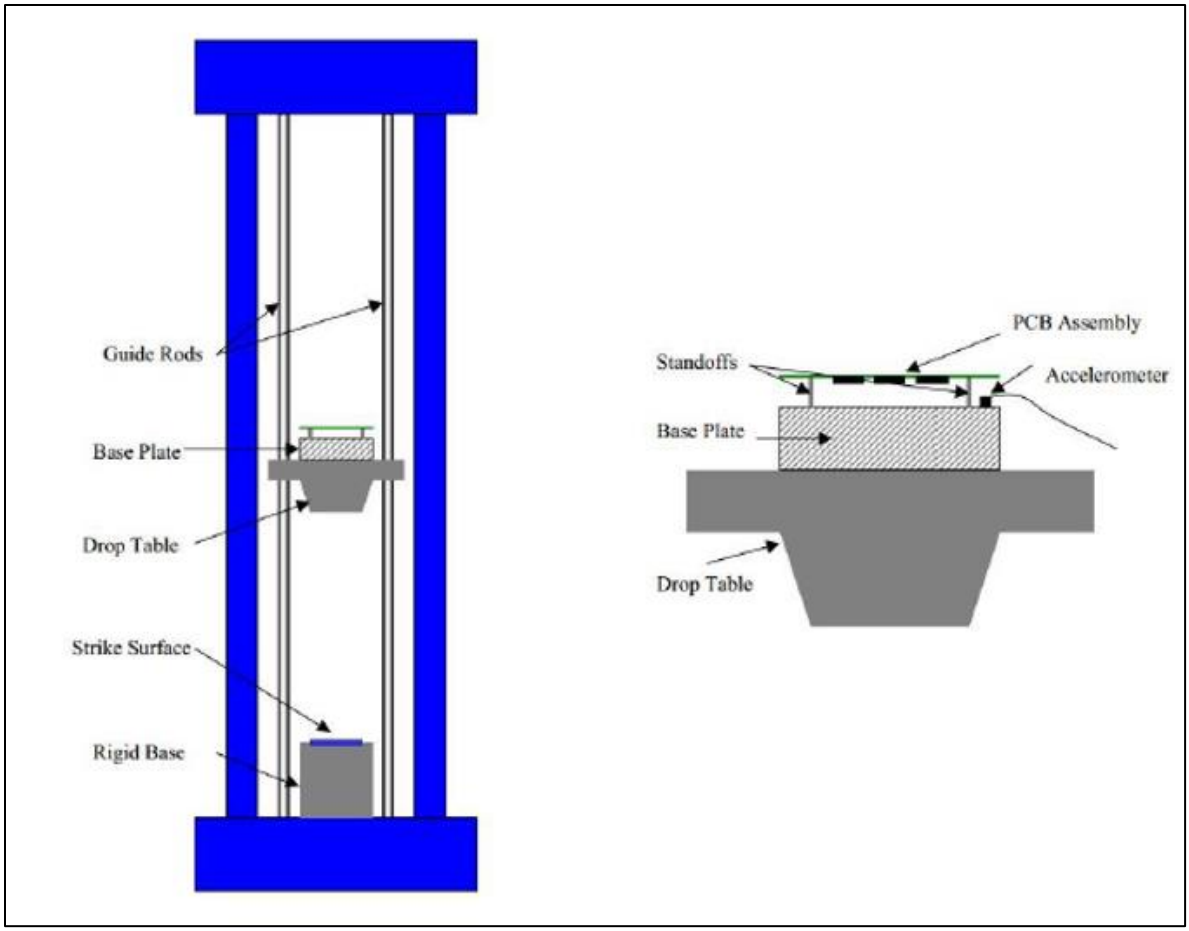

Figure 2.1 Schematic of JEDEC drop Experimental Setup

The PCB assembly is mounted to the base plate standoffs using four screws, one at each corner of the board. The experiment adopted horizontal orientation with components facing down in the cause of PCB flexure. An accelerometer may also be mounted on the board assembly at or near one of the support locations to ensure that the input pulse to the base plate is transmitted to the PCB without any distortion. Multiple drops were required while adjusting the drop height and strike surface to achieve the specified G levels and pulse duration in accordance with the JEDEC standard

To prevent relative movement between drop table and other part of base plate, the PCB assembly is attached to base plate at four corners with screws, one at each corner of the board. Figure 2.2 gives clear idea about the orientation of PCB assembly on base plate (Chen et al. 5). According to JEDEC drop test

specification, dimension of BGA package used for the experiment is 132mm X 66mm X 1mm, and has 15 components on it.

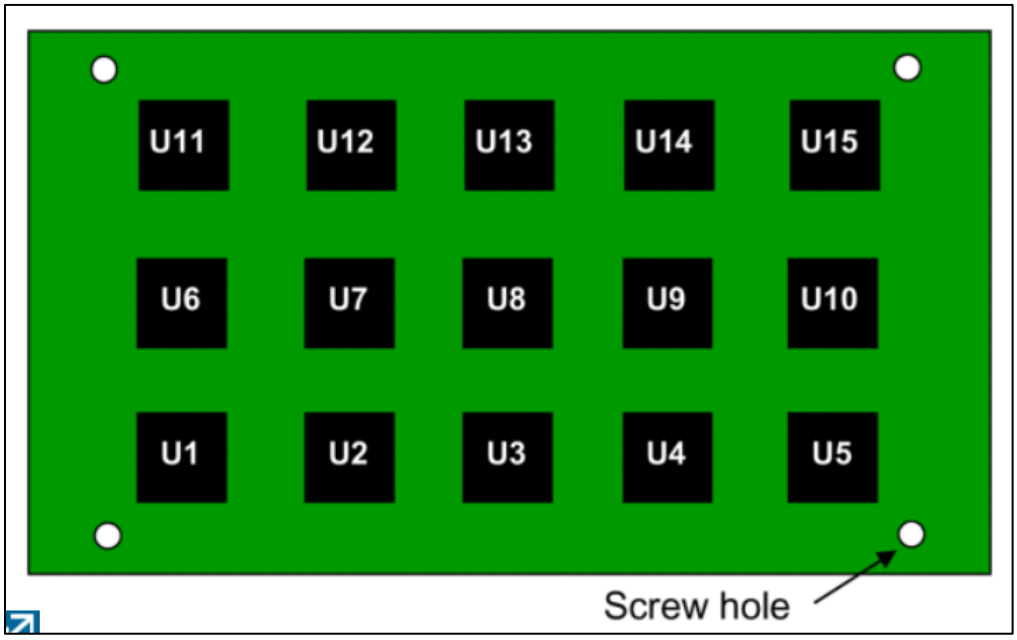

Figure 2.2 JEDEC Drop Board Schematic

The orientation of component board should be horizontal with ICs in downward direction. Input half sine waves are generated into the PCB board with help of accelerometer for 0.5ms duration, and drop height is adjusted to achieve 1500Gs drop impact shown in Figure 2.3 (Syed et al. 12).

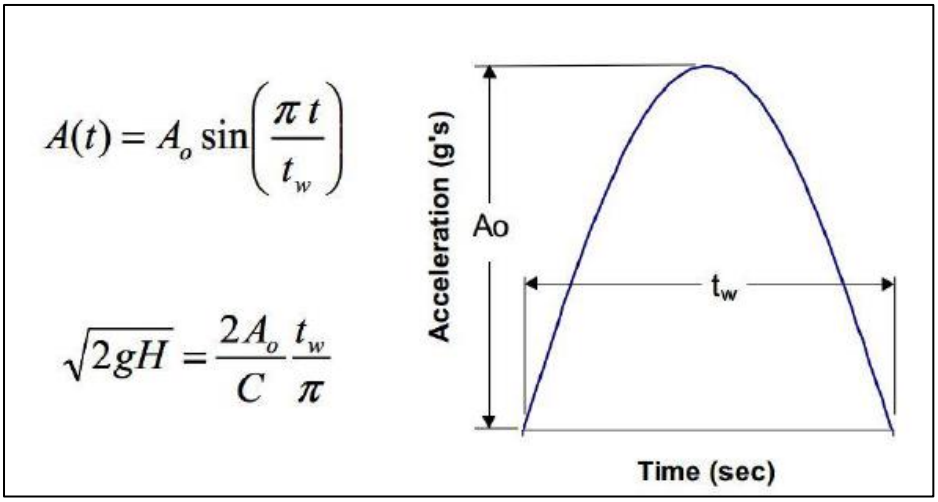

Figure 2.3: Drop Acceleration Input

Figure 2.4 shows the impact pulse measured in terms of peak acceleration 1500G for the duration of 0.4ms under a drop height 1.5m (Luan and Tee 14)

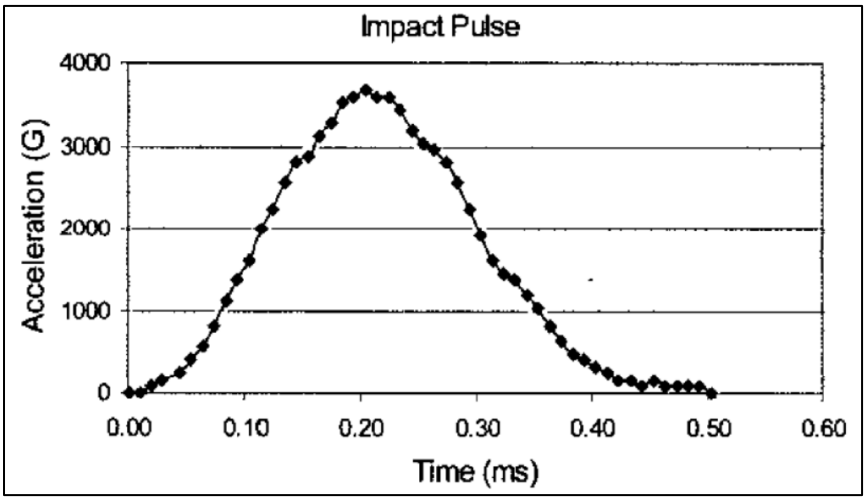

Figure 2.4. Input acceleration curve

According to Wong, et al. [31] principal reasons behind failure of the interconnections are as follows:

1. Elongation and bending of interconnection between PCB and package.

2. Large inertia of IC packages

3. Stress wave generated by impact force.

Different modes of failure between PCB and package interconnections are listed below.

1. Package-solder interconnect interface failure

2. Board-solder interconnect failure

3. Board via crack

Figure 2.5 gives clear picture of interconnect failure between PCB and package interface.

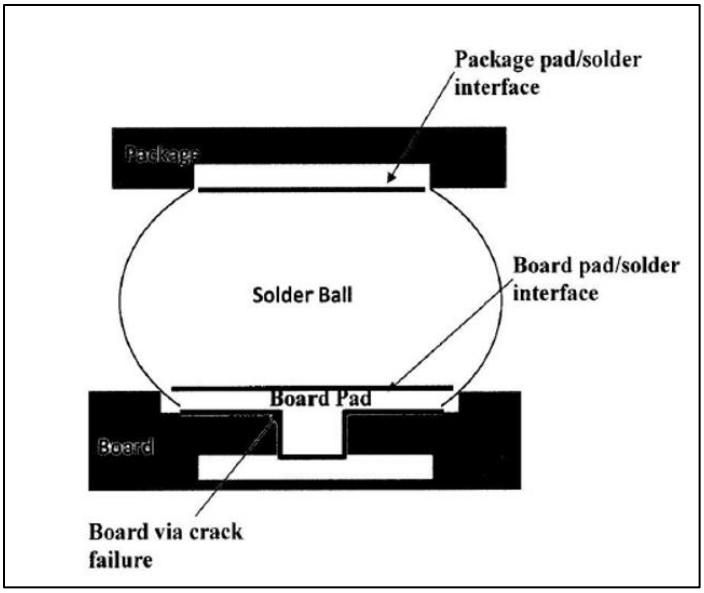

Figure 2.5 Package – PCB interface failure modes.

2.2 Finite Element Modelling

Methodologies for dynamic response of drop impact test. Figure 2.6 shows various methods to perform dynamic analysis (Aaue, 15)

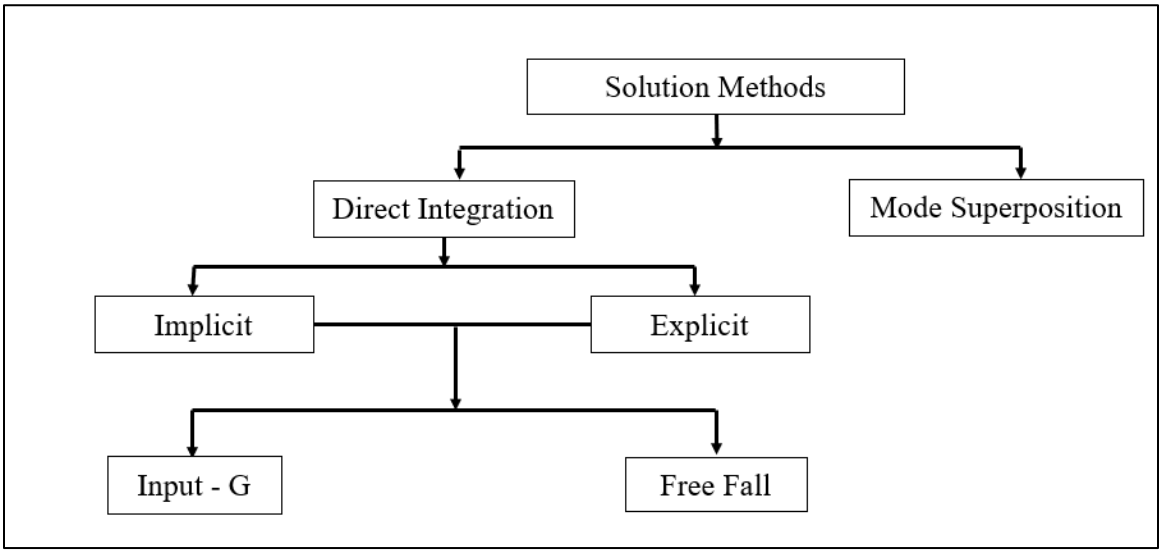

Figure 2.6 Method to determine Dynamic Response of the System

Figure 2.5 shows various finite element methods for dynamic response of the system. Direct integration and mode superposition are two basic classification, out of which direct integration is used widely. In this

work, direct integration technique has been used to solve the dynamic system. Problem can be solved by Implicit and Explicit algorithm in direct integration method. Implicit method further classifies into two types i.e. full system matrices and reduced matrices, which can be solve by input G method or free fall.

Board level simulation modelling

2.2.1 Free Fall Method

The free fall method simulates real drop test scenario, which includes modelling of drop block, board guiding rod etc. Figure 2.7 shows schematic of Free Fall Method (Tee et al. 10). As shown in figure 2.6 PCB assembled with package/s is mounted on a metal block through connectors which allows flexing of the PCB (Tee et al. 10). The entire assembly is guide-dropped from a height to produce the certain level of G's. The value of G depends on the contact surface condition and material properties used for the contact surface, drop height, and the felt material properties of felt (Tee et al. 10). The velocity of impact calculated from the empirical equation given below (Ren and Wang, 16)

$$v = \sqrt{2gH} \qquad 2.21$$

Where,

V is the velocity of the assembly before impact

g is the gravitational acceleration.

H is the drop height where

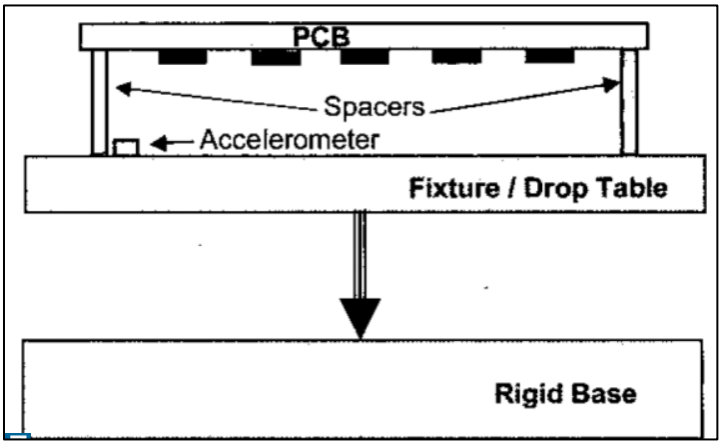

Figure 2.7 Schematic of Free Fall Method

Free fall method follows explicit time integration for the problem solving, where time step to perform model analysis is given by

$$\Delta t = l\sqrt{\frac{\rho}{E}} \tag{2.22}$$

Where,

l is the characteristic length

ρ is the density

E is young's modulus

Computation time for the free fall dynamic modelling is very high since it consumes large amount of time for finely refined mesh geometry.

2.2.2 Input G Method

Input G Method displacement derived from input acceleration (Luan and Tee 14). Additionally, in these methods the drop table, fixture, contact surface, and friction of guiding rods are not simulated, however their effects are considered to generate impact pulse. So, input acceleration 1500G given to board-package assembly for the duration of 0.4ms under a drop height of 1.5m to simulate experimental input impact pulse. Refer to Luan and Tee, "This standard numerical drop test will produce consistent and realistic testing results" (14). Because of simple experimental methodology of input G method, for same element mesh size of PCB and package in finite element modelling it takes considerably less computation time. Figure 2.8 shows schematic experimental set up of input G method.

The formulation of input G method given as below.

$$[M]\{\ddot{u}\} + [C]\{\dot{u}\} + [K]\{u\} = \begin{cases} -[M]1500g\ sin\frac{\pi t}{t_w},\ t \le t_w,\ t_w = 0.5 \\ 0,\ t > t_w \end{cases}$$

$$\{u\}|_{t=0} = 0$$

$$\{u\}|_{t=at\ hole} = 0 \tag{2.23}$$

where [M] is the mass matrix, [C] is the damping matrix, [K] is the stiffness matrix,

g is acceleration due to gravity, $\{\dot{u}\}$is the velocity, {u} is the displacement, t is time after impact.

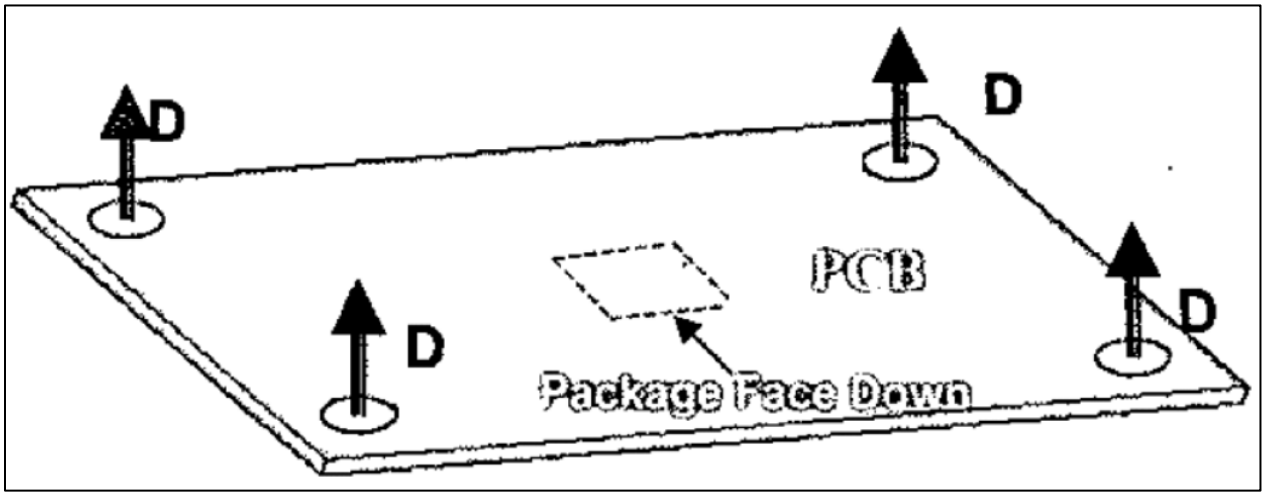

Figure 2.7 Schematic experimental set up of input G method.

For finite element modelling both full model and sub model are used with detail dynamic loading conditions, boundary conditions. To apply dynamic loads to the board structure input acceleration method is used.

Chapter 3

FINITE ELEMENT MODELING

3.1 Sub-modeling

The sub-modeling approach has been very widely used in the electronic packaging industry (Syed et al. 12). According to him this approach it is used to investigate the dynamic behavior of different components on a JEDEC board. Input G technique poses challenges when the package and the solder ball size is too small compared to the board dimension. In sub-modelling according to St. Venant's principle, the cut-boundary interpolation displacement method is applied to coarse model in interested region. Usually sub-modelling utilizes two separate models global model/full model and local model/sub-model. A global model is full geometry of the object under study. And the local model is part of global model under study with fine mesh.

According to following steps should be followed to solve sub-model (Hsu et al. 17)

1. Create and analyze global model.
2. Create the local model from global model of the specific region of interest and perform cut boundary interpolation.
3. Apply boundary loads and analyze the local model.

3.1.1 Global Model

Global model is board level modelling contains of shell element (Dhiman 8). Properties of all the material are classified into two categories one for elements in the non-component region and other for component region refers Figure 2.8 (Lall et al. 9). Based on component stiffness and mass, component region has the effective modulus and mass density. The dimensional size of solder ball is very small compare to package, which is of the ratio 10^6 (Dhiman 8). Because of this dimensional mismatch, board

level simulation becomes very challenging. Refer to Syed, et al., sub-modeling technique helps to boost the efficiency of the solution

(12). He suggested following steps to investigate the dynamic behavior of different components in board level simulation.

1. Calculate component stiffening effect.

2. Global modelling with the component stiffness effect

3. Sub-modeling approach to transfer boundary conditions to local/sub-model

4. Detailed solder joint model including calculations of intermetallic layer

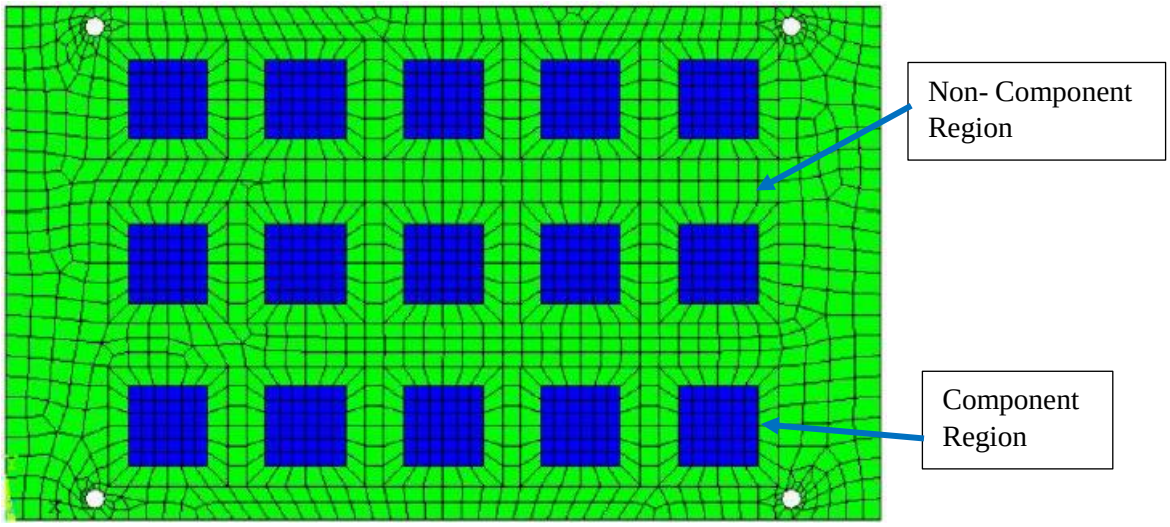

Figure 3.1: Global level modeling (15)

The quarter finite element model of the PCB board is used for the analysis because of symmetry. The quarter model of dimension 66mm X 38.5mm X 1mm created for analysis. Solder bump model is created for the analysis purpose.

3.2.2 Solder Bump Model

To simplify geometrical modelling and to save computational time solder balls are modeled as rectangular blocks. Optimized meshing consists of 242456 nodes and 89590 elements. The quarter symmetry model is shown in figure 3.2

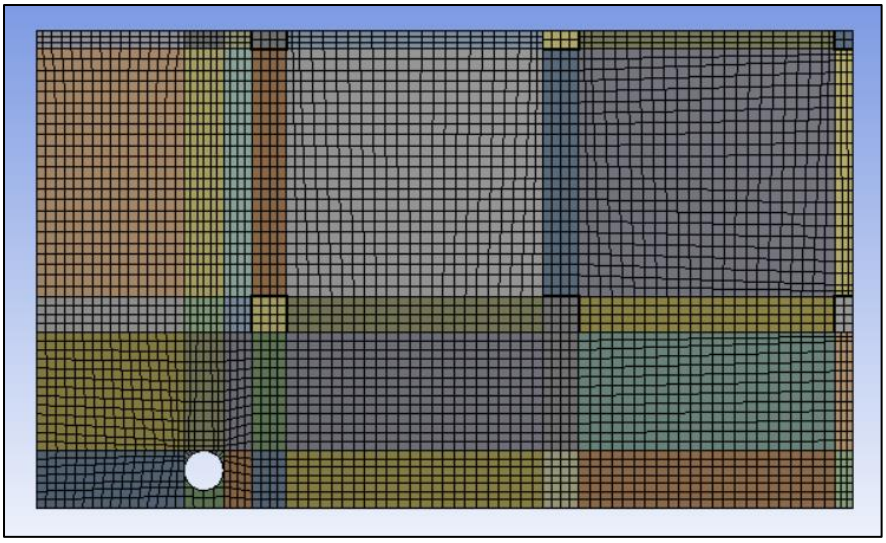

Figure 3.2 Quarter symmetry global model

3.3 Local Model

Local model also called as Sub-modeling where full model/global model displacement results are applied to local model. Local model at package 1 location shown in figure 3.3. The size for the global model is 3mm x 3mm.

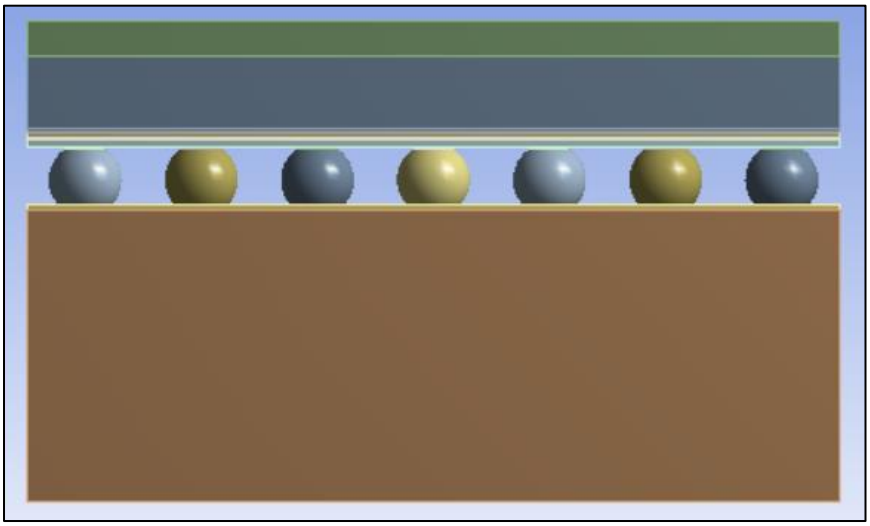

Figure 3.3 Local model at location 1

Local model contains only one chip, so the model size reduces significantly. The refined mesh pattern for the local model is shown in figure 3.4.

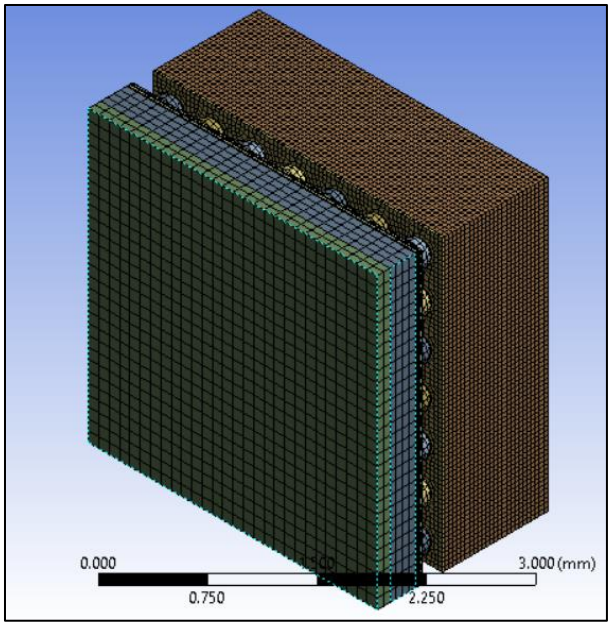

Figure 3.4 Refined mesh pattern

Component stiffening effect calculated for rectangular solder interconnects in global model are not very accurate though it saves computation time (Dhiman 8). Therefore, to achieve accuracy in solder interconnect displacement additional detail layer is added in corner joint with corresponding intermetallic layers which replaces the coarse corner joint in the global model (Dhiman 8). Figure 3.5. shows solder interconnect and intermetallic layer in detail (Syed et al. 12)

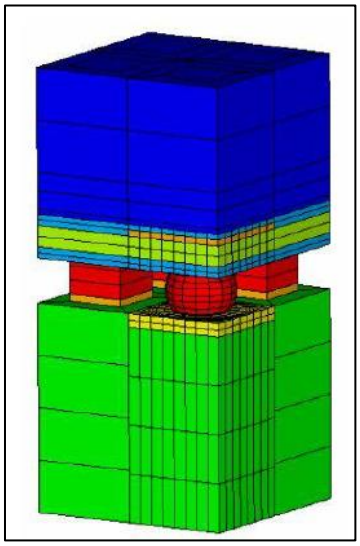

Figure 3.5 Local Model

Figure 3.6 represents stress distribution in the intermetallic layer. (Syed et al. 12)

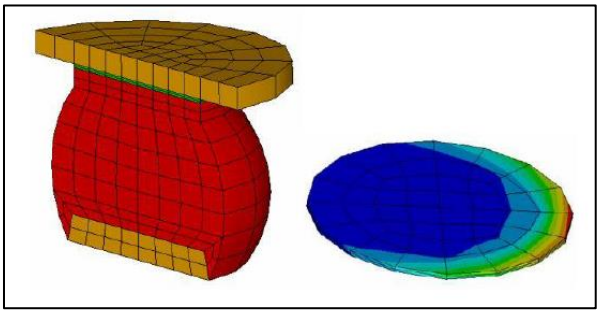

Figure 3.6 Detailed Solder Joint

Chapter 4

MATERIAL CHARACTERIZATION

Properties of material used for the PCB board is important parameter to perform finite element modelling are listed below.

- Coefficient of thermal expansion(CTE)
- Youngs Modulus
- Shear Modulus
- Poisson's ratio

Each of this property has described below one by one.

4.1 Thermo-Mechanical Analyzer

4.1.1 Coefficient of thermal expansion(CTE)

Coefficient of thermal expansion is change in degree of expansion per degree change in temperature.

$$\alpha = \varepsilon/\Delta T \tag{4.1}$$

Where,

α - Coefficient of Thermal Expansion (CTE) ppm/°C

ε - Strain (mm/mm)

ΔT- Difference in Temperature (°C)

The Thermal mechanical analyzer is used to measure In plane and out of plane coefficient of thermal expansion.

Figure 4.1 Thermo-Mechanical Analyzer (TMA-S6600)

8x8 mm BGA package sample shown in figure 3.4 is used for the TMA experiment.

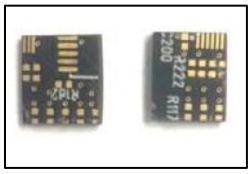

Figure 4.2 Samples used for TMA experiment

In thermal mechanical analyzer(TMA), quartz probe enclosed in the thermal chamber detects relative movement taking place with expansion or contraction of BGA sample due to change in temperature. The BGA sample is subjected to change in temperature from of -650C to 2600C with a ramp rate of 50C/min. The load applied in the start and end is 100 mN. The in-plane and out of plane CTE are obtained by changing the position of the PCB sample.

The figure 4.3 shows the plot for the in-plane of the Megtron 6 and the FR-4 samples.

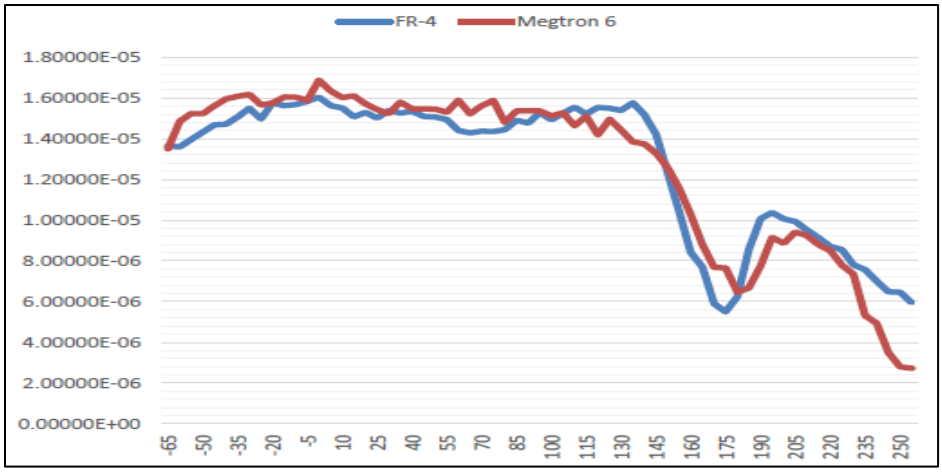

Figure 4.3 Plot for In-Plane CTE

The figure 4.4 shows the out of plane CTE of the PCB samples.

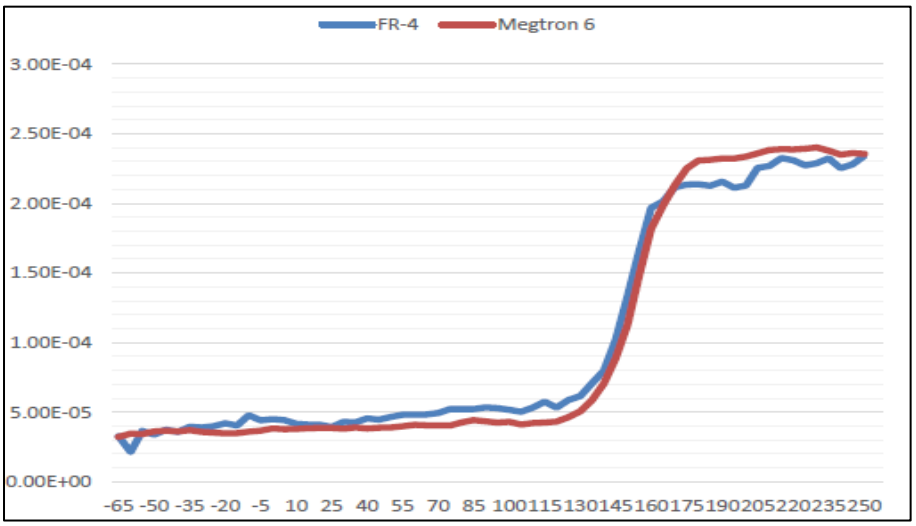

Figure 4.4 Plot for Out of Plane CTE

Poisson's ratio

Poisson's ratio is the measure of material expansion in directions perpendicular to the direction of compression. In short it is the ratio of material contraction to expansion. The empirical equation of Poisson's ratio is given by

$$\nu = -\frac{\varepsilon_{lateral}}{\varepsilon_{axial}} \qquad 4.2$$

Where,

$\varepsilon_{lateral}$ = transverse strain

ε_{axial}= axial strain

The table 4.1 shows the CTE values of the PCB materials in 3 directions.

Boards	CTE(ppm/0C)			E(GPa)	υ
	X-direction	Y-direction	Z-direction		
FR4	15.3	13.1	41.1	15.46	0.39
Megtron 6	15.39	13.2	43.1	13.8	0.2
Megtron 2	15	15	34	16.7	0.2
Megtron 4	14.5	14.5	35	15.9	0.2
Megtron 4s	14	14	32	15.1	0.2
Megtron 7	16	16	42	13.5	0.2
Megtron GX	10	10	22	29	0.2

Table. 4.1 CTE measured using TMA

The table 4.2 shows the CTE values of other components of the PCBA obtained from the literature. (Pallapothu 6)

Material	CTE (ppm/^{0}C)	E (GPa)
Copper Pad	17.78	110
Die Attach	65	154
Die	2.94	150
Mold	8.43	24
Polyimide Layer	35	3.3
Solder Mask	30	4.6

Table. 4.2 Material properties of BGA package.

Chapter 5

EXPERIMENTAL VALIDATION

5.1 Modal Analysis

This chapter describes modal analysis performed on global model to find out natural frequency of vibration PCB board and package during impact, where board is fixed in z direction at pin hole (Dhiman 8). Global model used for the modal analysis includes solder bump model, solder layer model and shell model. The purpose of modal analysis is to find highest mode of interest to calculate initial time step for the transient dynamic analysis (Morgan 18). He has also given the experimental formula to calculate initial time step given by equation 4.1.

$$\Delta t_{initial} = 1/20 f_{response} \quad (5.1.1)$$

Where,

$f_{response}$ is the frequency of the highest mode

Highest mode of frequency for all variety of PCB board using variety of laminates is obtained through modal analysis. Table 4.1 shows 5 modes of natural frequency of vibration.

Mode	FR4	Megtron 2	Megtron 4	Megtron 6	Megtron 7
First Mode	230.6	228.98	223.53	208.69	206.32
Second Mode	599.06	607.39	592.92	553.52	547.21
Third Mode	866.59	881.39	860.43	803.38	794.23
Fourth Mode	1290	1272.8	1242.6	1160.1	1146.9
Fifth Mode	2095.6	2131.1	2080.4	1942.5	1920.4

Table 5.1 Natural Frequencies of a JEDEC Board

The Figures 5.2 and 5.3 shows five mode shapes of natural frequency of vibration of FR4 board.

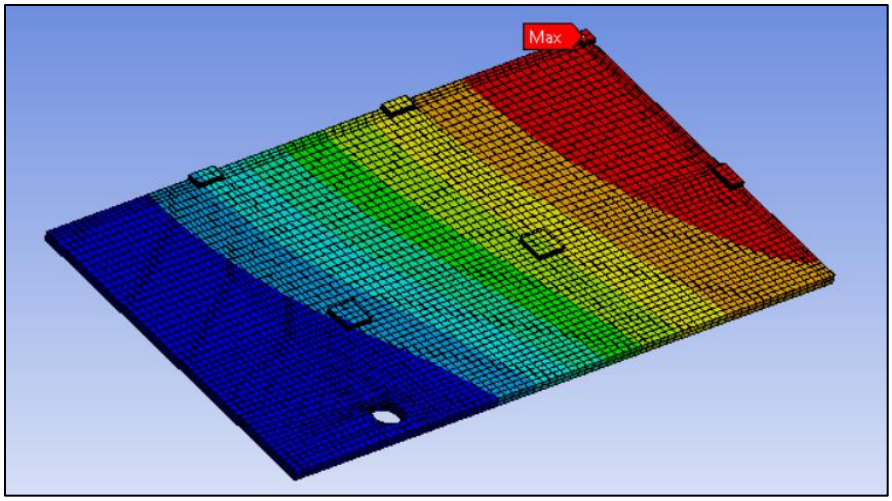

Figure 5.1 First Mode Shapes of a Quarter FR4 Board: Mode - 230.6 Hz

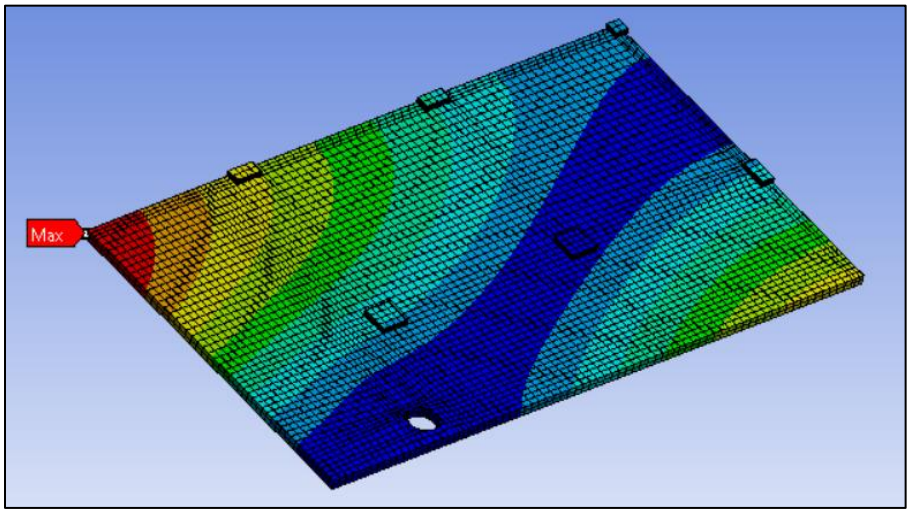

Figure 5.2 Second Mode Shapes of a Quarter FR4 Board: 599.06

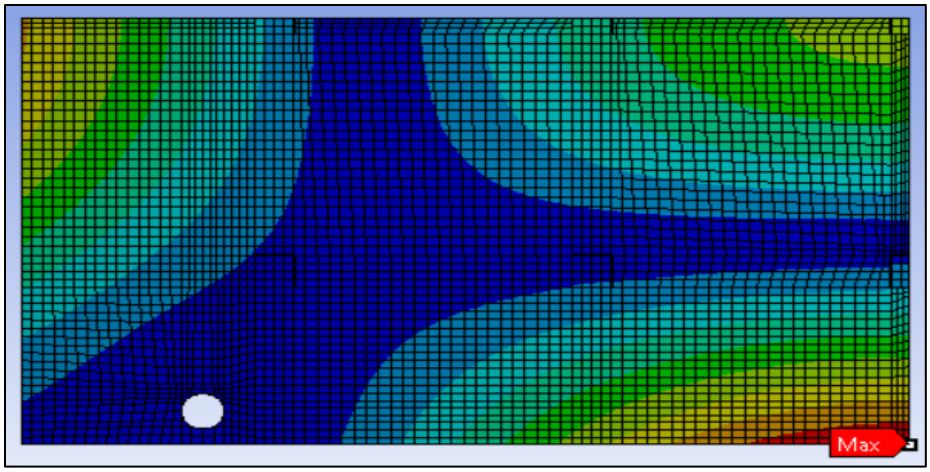

Figure 5.3 Three Mode Shapes of a Quarter FR4 Board: Mode 866.59 Hz

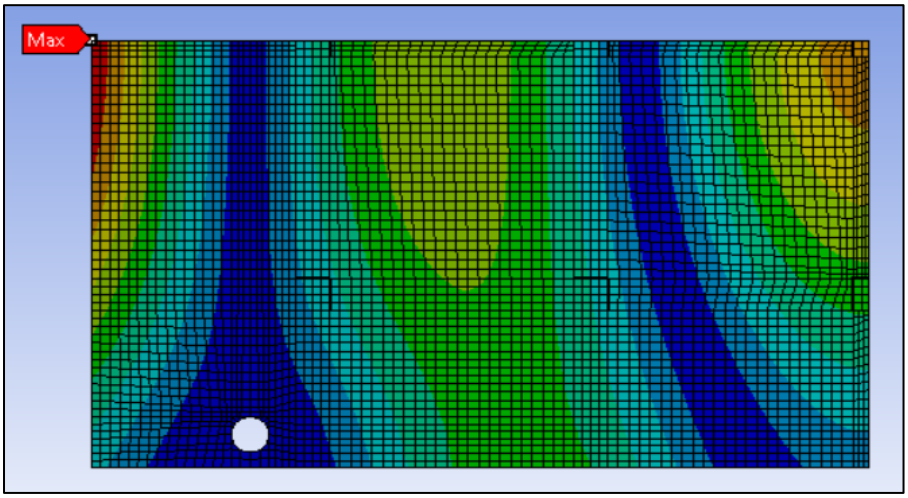

Figure 5.4 Four Mode Shapes of a Quarter FR4 Board: Mode 1290 Hz

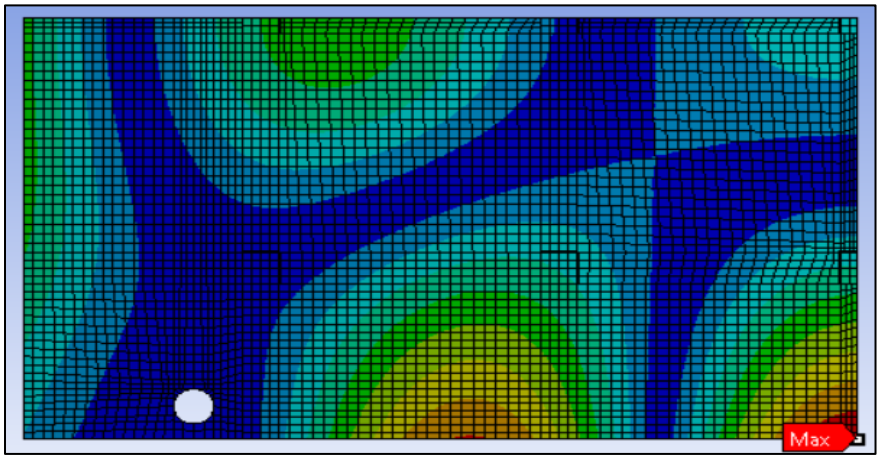

Figure 5.5 Five Mode Shapes of a Quarter FR4 Board: Mode 2095 Hz

Chapter 6

RESULTS AND CONCLUSION

6.1 Dynamic Analysis of PCB Board

Drop impact on PCB board will tensile stress in solder joint when it bends downwards and compressive stress when bending in upward direction. This bending movement will generate stresses and strain in solder interconnects, and the magnitude of stress will depends upon location of component and intensity of bending force. Figure 6.1 shows schematic of PCB bending.

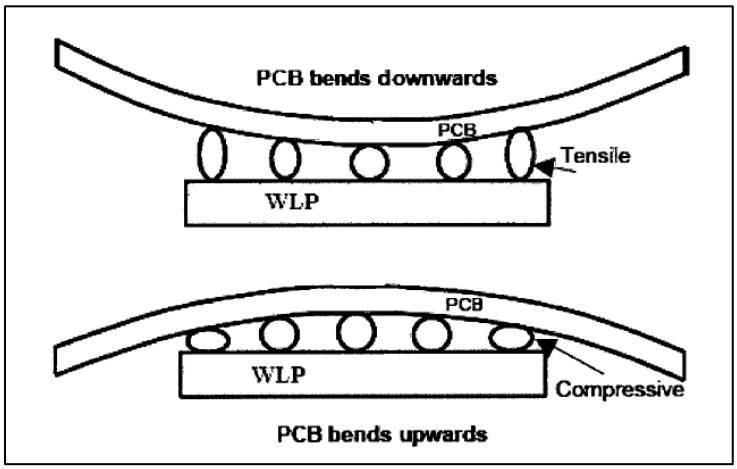

Figure 6.1 Schematic of PCB bending

6.2 Transient Structural Analysis

Transient structural analysis shows that first failure due to drop impact will occur in the corner solder ball away from the neutral point. This location of failure depends on material property of board and bending frequency mode.

6.2.1 Stress Analysis/ Peeling Stress Analysis

Contour diagram of normal stress shows that solder ball always fails from the package side. In this chapter maximum normal stress and stain is calculated to measure reliability of JEDEP board under drop impact.

Maximum stress distribution on the array of solder ball showed in figure 6.1.

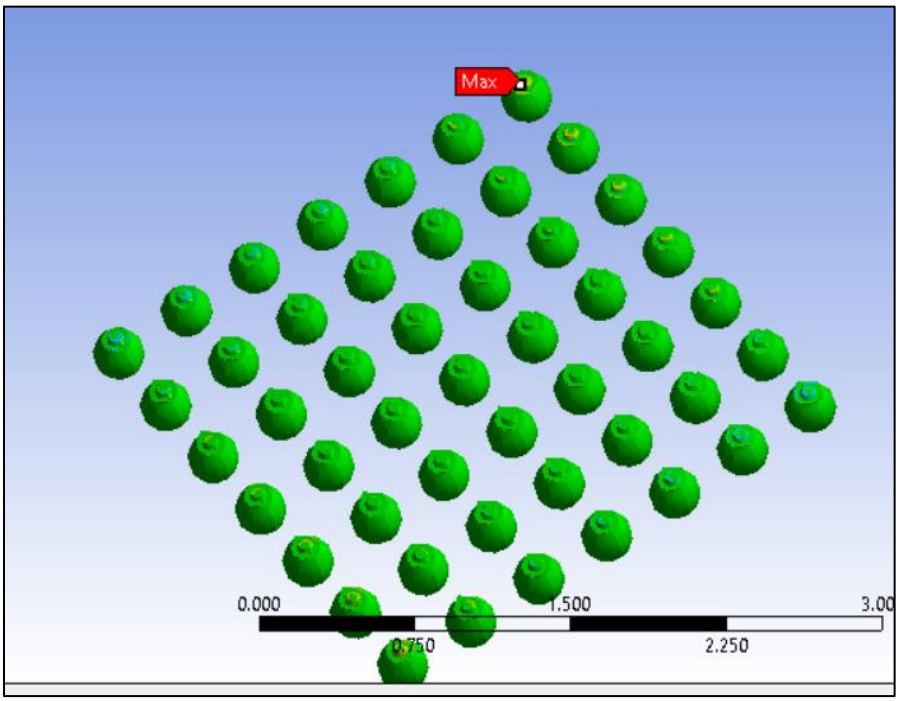

Figure 6.2 Maximum stress distribution on corner solder ball

Figure 6.3 shows maximum stress generation on the corner ball from the package side.

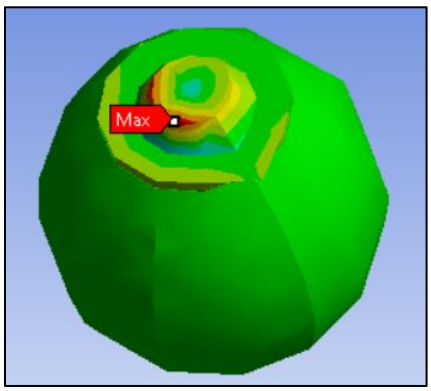

Figure 6.3 Maximum stress generation on corner solder ball from package side

Figure 6.4 shows maximum stress/peeling stress developed on all types of boards, the stress generated in FR-4 board is less than any other high frequency Megtron series board.

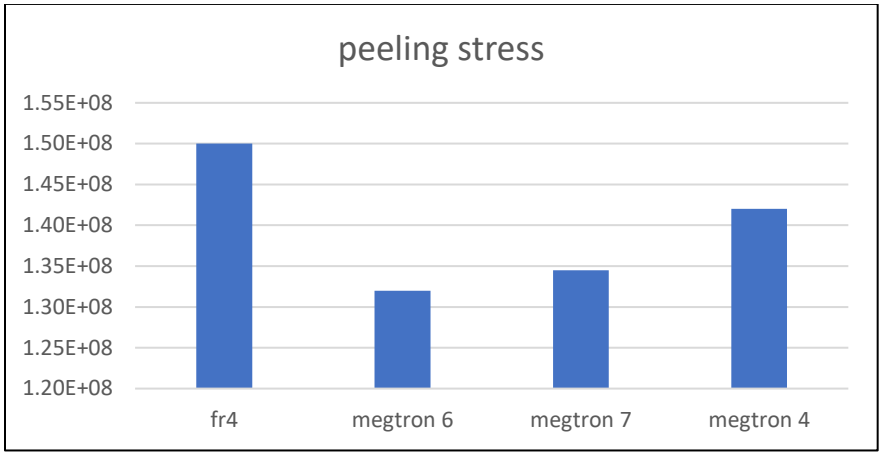

Figure 6.4 Peeling stress on corner solder ball.

6.2.2 Strain Analysis

Bending movement generates strain at each component. For the analysis purpose strain at the two locations i.e. strain at package center and strain at package corner. It showed that the maximum strain at the corner of the ball is more than maximum strain at the center of the ball. Figure 6.5 presents that maximum strain developed in Megtron 6 board is less than FR-4 board, which shows that stiffness of FR-4 board is more.

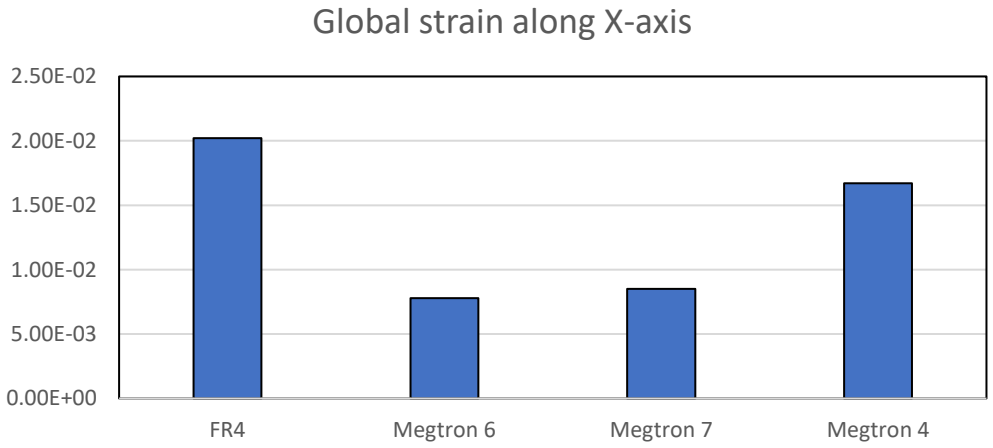

Figure 6.5 Equivalent elastic strain on the corner solder ball

6.2.3 Deformation Analysis

The PCB board undergoes deformation under the sinusoidal bending mode. The stress generation, bending mode, and the property of material. Figure 6.6 shows bending deformation of various types of PCB board laminates. The bending deformation in FR-4 laminate is highest than entire Megtron family.

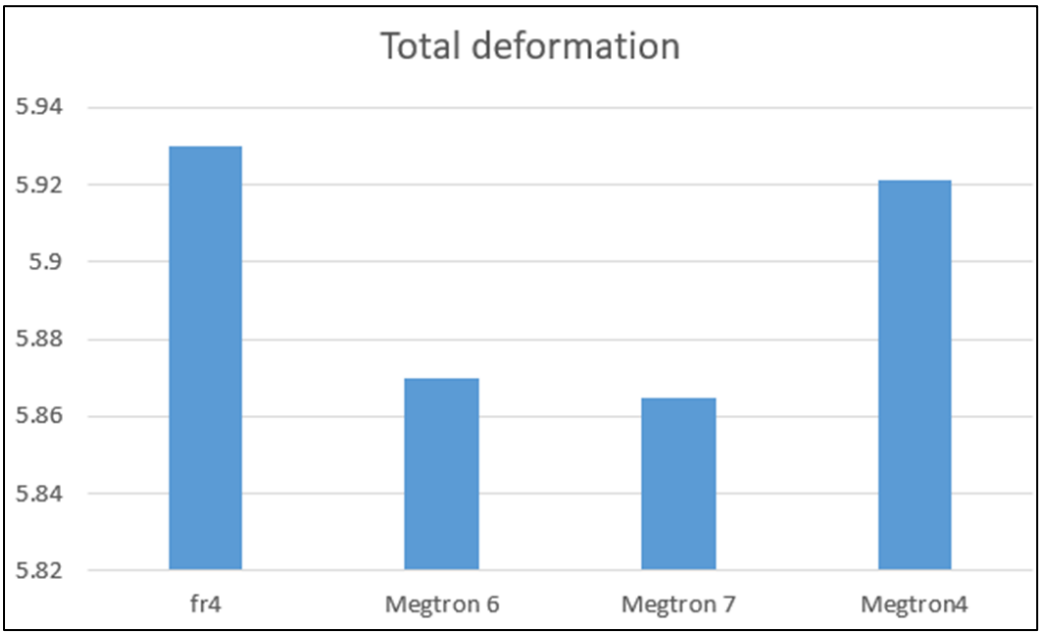

Figure 6.6 Maximum total deformation on corner solder ball

Chapter 7

CONCLUSION AND FUTURE WORK

7.1 Conclusion

The finite element modeling of dynamic behaviors of JEDEC drop test board with BGA package performed under impact loading. Input G acceleration method is used for finite element analysis. Sub-modeling approach has been followed for accurate results and less computation time. Modal analysis was performed to find out highest mode of frequency, which gave the initial time step during the impact. Transient dynamic analysis has been carried out to perform dynamic structural analysis. In sub-modeling approach board strains were extracted from package corner and center of each component and applied to local model. Model analysis showed that higher strains induces higher stress in solder joint, causing first failure at solder interconnect. During impact loading board undergoes bending movement, which develop tensile and compressive force causes failure of solder interconnect on package side. To perform reliability analysis of FR-4 and Megtron series board properties like total deformation, maximum equivalent strain, and maximum peeling stress have taken into consideration. The analysis results indicate that the performance of Megtron series is much better than FR-4 under peeling stress, strain, and deformation testing. Among all Megtron series Megtron 6 gives exceptional performance in all tests. So, for high frequency applications it is recommended to use Megtron 6 boards considering other favorable factors like Low dielectric constant, low dissipation factor, low moisture absorption capacity, better impedance control, and better thermal management.

7.2 Future Work

In future, a temperature dependent reliability drop testing can be perform on high frequency Megtron series board. In addition to this, detail layer by layer analysis can be done to study the reliability effect. Validation of simulation results can be done by experimental free fall gravity testing.

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BIOGRAPHICAL INFORMATION

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