OPTIMIZATION OF BOARD LEVEL RELIABILITY OF MICROELECTRONIC PACKAGES AND MODULES

by

ALOK KUMAR LOHIA

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To my beloved family:

My wife Lisa Lohia and son Jay Lohia,

My Father Purushottam Lal Lohia, my mother Poonam Lohia,

my two brothers Avinash and Ashish.

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I would like to acknowledge my wife support and constant motivation during this long journey. My son Jay Lohia came during this journey and brought so much joy which helped a lot. I am also indebted to my parent for giving me lessons to always strive for the better education.

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ABSTRACT

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Alok Kumar Lohia

The University of Texas at Arlington, 2018

Supervising Professor: Dr. Dereje Agonafer

Thermo-mechanical reliability estimation of electronic packages and modules provides an opportunity to predict the function life of semiconductor devices. The problem complexity lies in the fact that there are variety of electronic packages with different form factors, materials and manufacturing technology for various applications. The custom PCB ranges from very thin for portable application to very thick for power application. Despite conventional understanding and prior studies, some of the failures were not explained. This study reviews three failure problems for QFN, WCSP and BGA packages by characterizing the properties of custom PCB materials by layer removal process. Due to layup of the prepreg and copper material in the PCB, the bulk mechanical properties changes and impacts the reliability of the various packages and modules. The material properties of the PCB were determined using Instron Micro tester, Digital Image Correlation technique (DIC) and Thermal Mechanical Analyzer (TMA). The experimental data is then correlated with a FEM model to understand the mechanism. Next, several material/dimensional parameters affecting reliability of three problems were studied and

chosen for optimization. The study proposes a methodology to optimize the overall system to mitigate the failure and prolong the usable life of packages.

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Chapter 1 Introduction

1.1 Introduction

Semiconductor Packages are designed for various applications and are based on different manufacturing technologies and are in different geometry, pin count and materials [1].

Figure 1-1 Semiconductor Packages

1.2 Systems

The application can range from PCB as thin as 0.5mm for mobile application to more than 3mm for power module application materials.

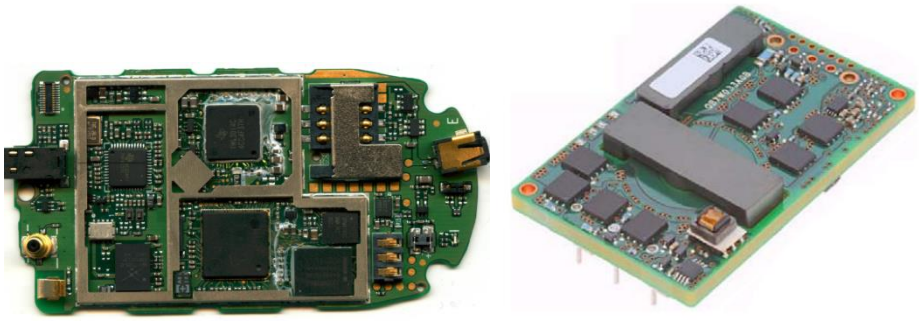


Figure 1-2 (a) Mobile system, (b) DC-DC Converter

1.3 Board Level Reliability (BLR)

Reliability can be defined as the ability of a system or component to perform its required functions under stated conditions for a specified period of time. To quantify reliability, “ability” should be interpreted as a “probability”. From this definition it is clear that all products always fail eventually. Indeed, a probability of zero failure during a certain amount of time is physically impossible, even for integrated circuit (IC) [2].

There are many indicators used to describe reliability and one of the most widely used is the failure rate. If a plot of failure rate versus time is depicted, a curve in the shape of a bathtub cross-section is obtained as shown in Figure 1-3. Hence it’s widely referred to as a bathtub curve.

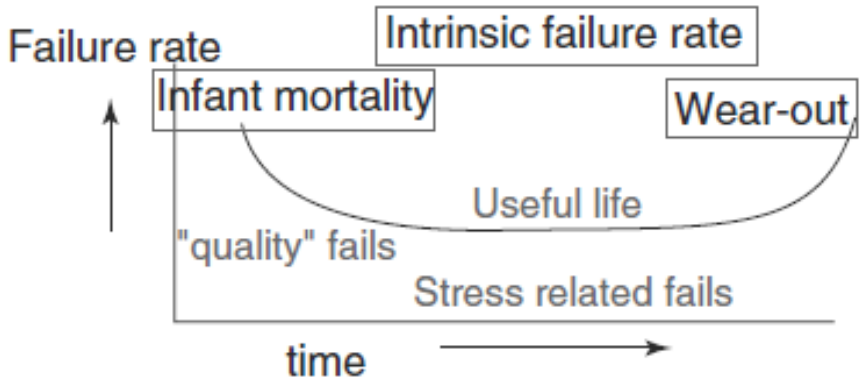


Figure 1-3 The bathtub curve: failure rate versus time

Three distinct phases of time can be seen in the bathtub curve: infant mortality, intrinsic failure and wear-out. Infant mortality or early failure is the period of time in which the product experiences failures also exclusively due to defects in the fabrication or assembly of the product. The intrinsic failure region has a near constant rate of failure since the poorly manufactured parts and defects were already screened out and eliminated and the majority of the population left are robust product which will enjoy long and sustained period where failures occur randomly. Finally, as the product ages,

chemical, mechanical, or electrical stresses begin to weaken the product's performance to the point of failure. This is called the wear-out region.

To estimate the reliability of the package, environmental stress test are used to simulate the end use environment conditions and to uncover specific materials and process related marginalities that may be experienced during operational life. Few consortiums such as Joint Electronic Device Engineering Council (JEDEC) and Institute for Printed Circuits (IPC) have adapted, documented and standardized many of the reliability tests. Since the scope of this work is only during thermal cycling, we'll briefly discuss about it. Table 1-1 shows different temperature ranges for various service environments for electronic products.

Thermal cycling is used to simulate both ambient and internal temperature changes that result during device power up, operation and ambient storage in controlled and uncontrolled environments. Due to difference in coefficient of thermal expansion between various package components, they warp and expand unevenly resulting in generation of internal thermal stresses which results in crack propagation in dielectric, fatigue and adhesion problems. These thermo-mechanical behaviors can be detected during thermal cycling tests. For reliability assessment, Weibull distribution is most commonly used to accurately reflect the behavior of the product in terms of failure rate.

Table 1-1 Thermal environments for electronic products

Use condition	**Thermal excursion (°C)**
Consumer electronics	0 to 60
Telecommunications	-40 to 85
Commercial aircraft	-55 to 95

Military aircraft	-55 to 125
Space	-40 to 85
Automotive-passenger	-55 to 65
Automotive-under the hood	-55 to 160

These reliability tests are either focused on package level or board level. Package level or 1st level reliability tests are dedicated to the robustness of the package component materials and design to withstand extreme environmental conditions and does not consider the interconnects when it is mounted on board. Whereas for the board level or 2nd level reliability tests, stresses are examined on the solder joint of the surface mount package when mounted on board [3].

1.4 Motivation

The motivation of this project can be outline as: a) To analyze the “physics of failure” for non-standard boards and SMT packages: QFN, WCSP and BGA b) Propose design/material changes to mitigate the failures observed during Accelerated Thermal Cycling (ATC).

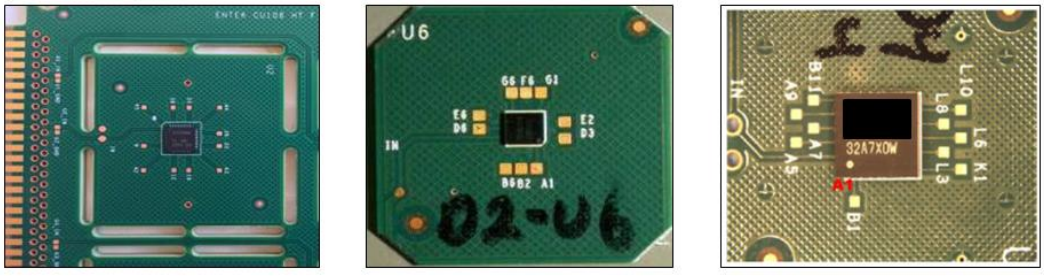


Figure 1-4 (a) QFN package (b) WCSP Package (c) BGA Package

1.5 Flow Chart of the work

Each of the three problems was understood using modular approach. The flow chart is shown below. In next chapters, each problem is outlined in detail.

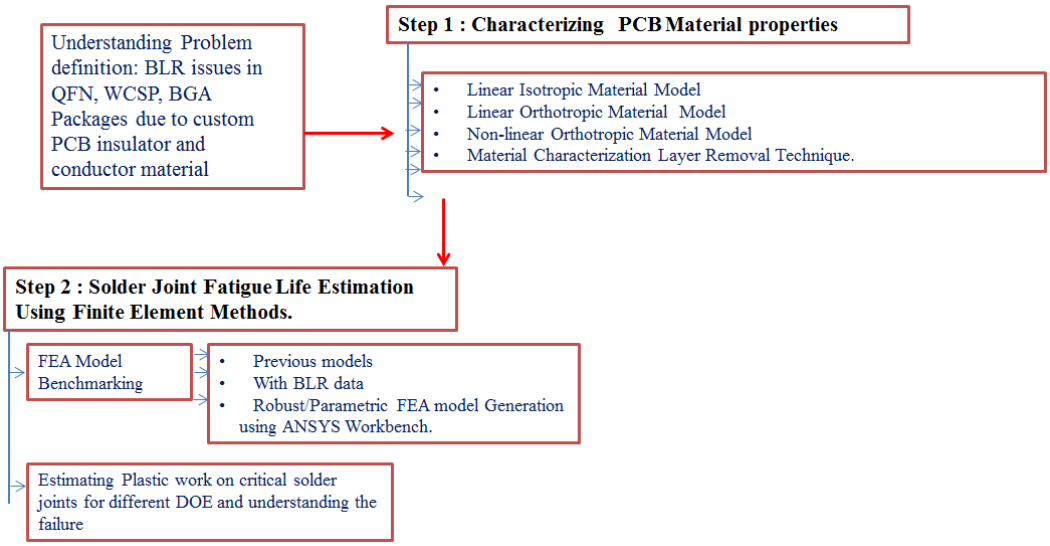


Figure 1-5 Flowchart for the Work

In next chapters, each problem is outlined in detail.

Chapter 2

Reliability of QFN package

2.1 Quad Flat No-Lead (QFN) Packages

Quad flat no leads (QFNs) and small-outline no leads (SONs) are thermally enhanced plastic packages that use conventional copper leadframe technology. This construction results in a cost-effective advanced packaging solution that helps to maximize board space with improved electrical and thermal performance over traditional leaded packages [1]. QFNs have solder lands on all four sides of the package. SONs typically have solder lands on two sides of the package. QFN/SONs are molded and mechanically singulated from a matrix leadframe or punched. Package size is determined by several key factors including die size, number of terminations, etc [4].

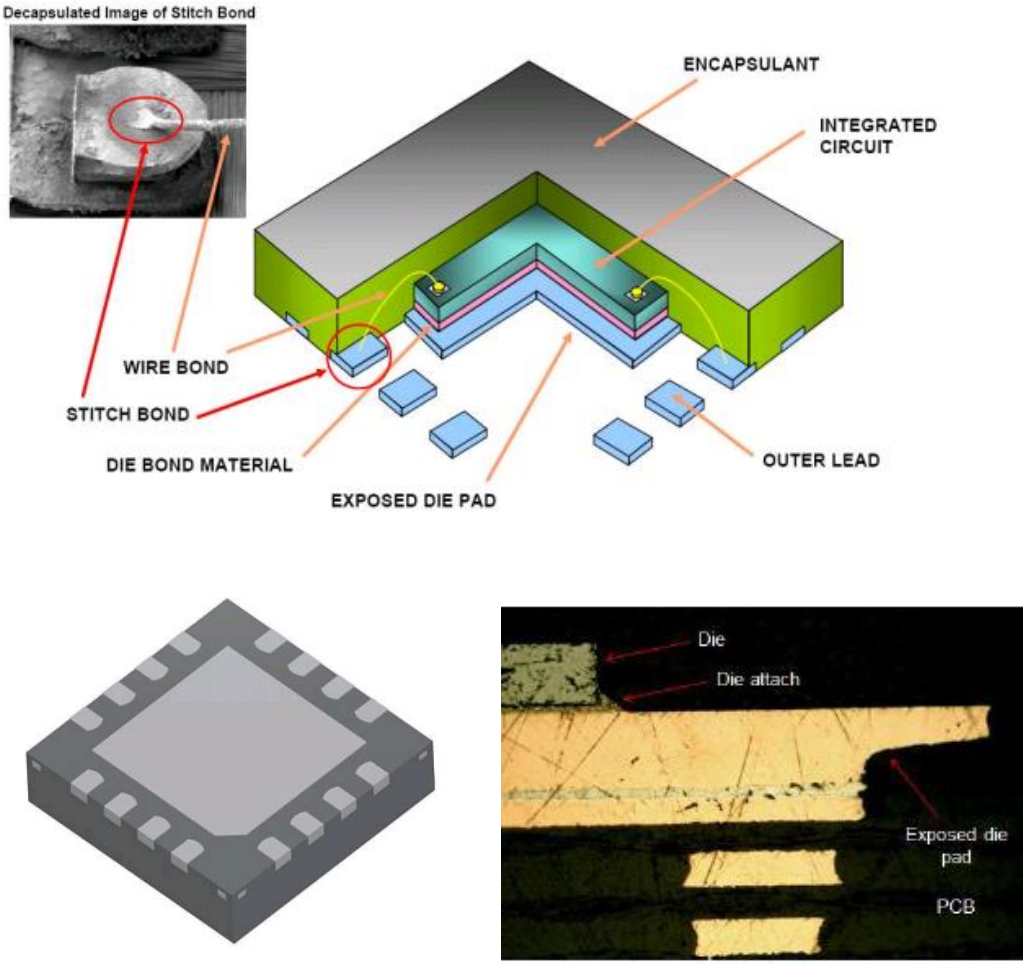


Figure 2-1 QFN Package Cross-section [5]

All QFN/SONs are leadless packages with electrical connections made via lands on the bottom side of the component to the surface of the connecting substrate [printed circuit boards (PCB), ceramic]. This enhances the thermal and electrical characteristics, enabling high-power and high-frequency applications. This configuration provides an extremely low resistance path resulting in efficient conduction of heat between the die and the exterior of the package. Due to its superior thermal and electrical characteristics, this device package has gained popularity in the industry during the last couple of years.

Because of its compact size, QFN package is an ideal choice for handheld portable applications and where package performance is required.

A printed circuit board (PCB), typically consists of alternate layers of copper and non-conductive laminate made up of glass fiber and resin (FR4). PCBs are available in different types based on its application E.g. Single sided (one copper and one laminate layer), double sided (two copper layers and laminate layers), multi-layered boards. Multi-layered boards are mainly used for high component density applications like defense and automotive. A thick printed circuit boards (PCB) consists of large number of Cu layers (>8) and large board thickness (>3 mm). Cross-section of a typical thick PCB with 16

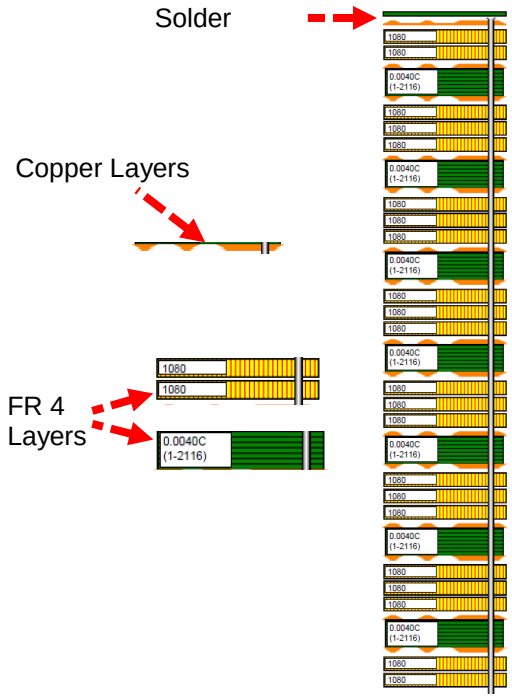


Figure 2-2 Cross-section of 16 Layered Board

copper layers, shown in the figure 2-2.

Primary reliability issues associated with the use of thick boards are because of the fact that as stiffness of the PCB increases with thickness leading to less deformation and compliance.

2.2 Problem Statement

QFN package gained popularity among the industry due to its low cost, compact size and excellent thermal electrical performance characteristics. Although QFN package is widely used in handheld devices, some customers require it for heavy industry application demanding thicker PCB. Literature suggests that as the thickness of PCB increases, the reliability and fatigue life of the package decreases since the board becomes stiffer and less flexible resulting in more transfer of stresses on the solder joint [6] [7] [8].

A 40 pin QFN board of thickness approx. 3 mm was tested under accelerated thermal cycling (ATC) conditions for failure analysis (FA). The board was tested under temperature load from -40°C to +125°C keeping the ramp and dwell time of 15min. The tests showed that some early fails. Some of the failures were observed to have insufficient joints, zero standoff or a combination of both (see Figure 2-3 and Figure 2-4). The requirement was to pass 700 cycles based on IPC9592 requirement.

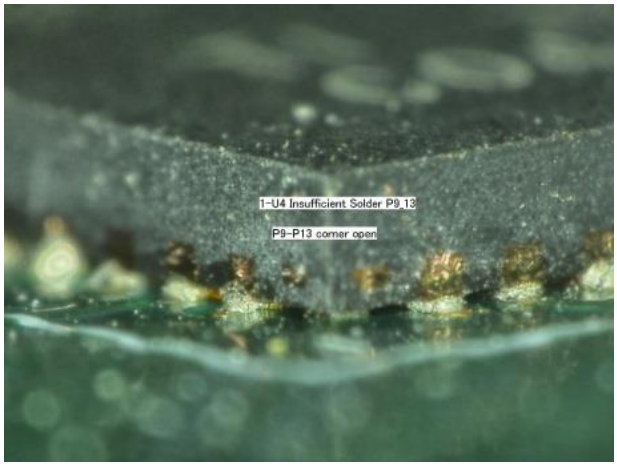


Figure 2-3 Typical fail unit showing insufficient joint

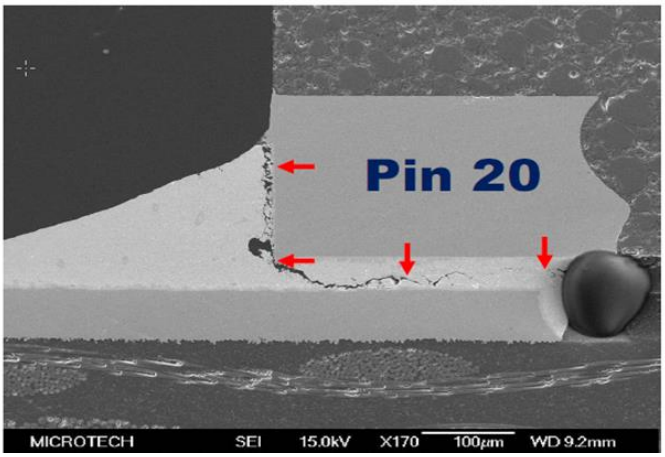


Figure 2-4 Crack propagation in a solder joint

From the test results, it was concluded that QFN package on the thicker board fails much earlier than thinner boards. This provides the motivation for this work. This work has made an attempt to study different package parameters that affect QFN reliability on thick boards, while keeping board parameters intact. The design parameters were then optimized to mitigate failure, thus improving its reliability.

The primary objective of this problem is to analyze different dimensional parameters affecting the reliability of QFN package on thick FR4 board under ATC

condition. Understand the root cause of the solder joint failures and methods to improve the mechanical reliability of the package thus making it to qualify the BLR industry standard for customers use.

Initially, in order to create a confident, accurate and reliable FEA model of QFN package, the workbench model was benchmarked with the existing TI's APDL version. Numerous mesh/analysis and solution controls like element size, type of elements, number of elements, number of load steps/sub steps, type of solver, etc. are studied for benchmarking. The thick PCB is then characterized using Instron and DIC to determine its elastic properties- Young's modulus and Co-efficient of thermal expansion. In the next step, the effect of several key package on the solder joint reliability is studied by performing a parametric analysis. The aim is to vary the parameters in an attempt to improve the board level reliability of the QFN package on thick FR-4 boards.

Finally, Multi Design Variable Optimization (MDVO) was performed using the critical parameters to find optimum set of design parameters thereby increasing board level reliability of QFN package on thick board.

2.3 MATERIAL CHARACTERIZATION

In order to accurately capture the material response generated in finite element model, it is imperative to assign actual material properties for each material. Since there is inadequate data available on the properties of thick PCB's, in this work, thick PCBs were characterized for finding following material properties given below-

- Coefficient of Thermal Expansion (CTE)
- Young's Modulus (E)
- Poisson Ratio (υ)

Some of the equipment's and techniques leveraged for characterization include-

- Sun Microsystems Oven with DIC
- Instron Micro tester with 2kN Load Cell

2.3.1 Coefficient of Thermal Expansion (CTE)

Coefficient of Thermal Expansion (CTE) is defined as volumetric dilation or contraction of a material in a particular direction as a function of the change in the material's bulk temperature. CTE is expressed as-

$$\alpha = \frac{\epsilon}{\Delta T}$$

Where,

α – Coefficient of Thermal Expansion (CTE) ppm/°C

ϵ - Strain (mm/mm)

ΔT –Temperature Difference (°C)

Since thermal cycling load applied on the package from -40°C to 125°C in the oven, it is necessary to know the CTE of the package so the FEA model of the package would complement the actual condition as closely as possible.

2.3.1.1 Digital Image Correlation Technique – CTE Measurement

Digital Image Correlation (DIC) is a full field optical non-contact technique to measure in-plane and out of plane deformations. The whole setup consists of a pair of 5MP cameras used to capture the images and oven to heat or cool the specimen. The cameras were positioned at an angle of 15~20deg from the vertical to have a view of package's in-plane as well as out of plane deformations. The cameras are connected to a software VIC Snap to view the image clearly on the screen and select area to be analyzed. Before, starting the measuring process, the test sample needs to be coated with white enamel paint and then speckled with black enamel paint. The size of the speckles should controlled and maintained in order to get accurate results. DIC requires

calibration each time the cameras are repositioned. The measurement test was benchmarked with aluminum sample to gain confidence in the test.

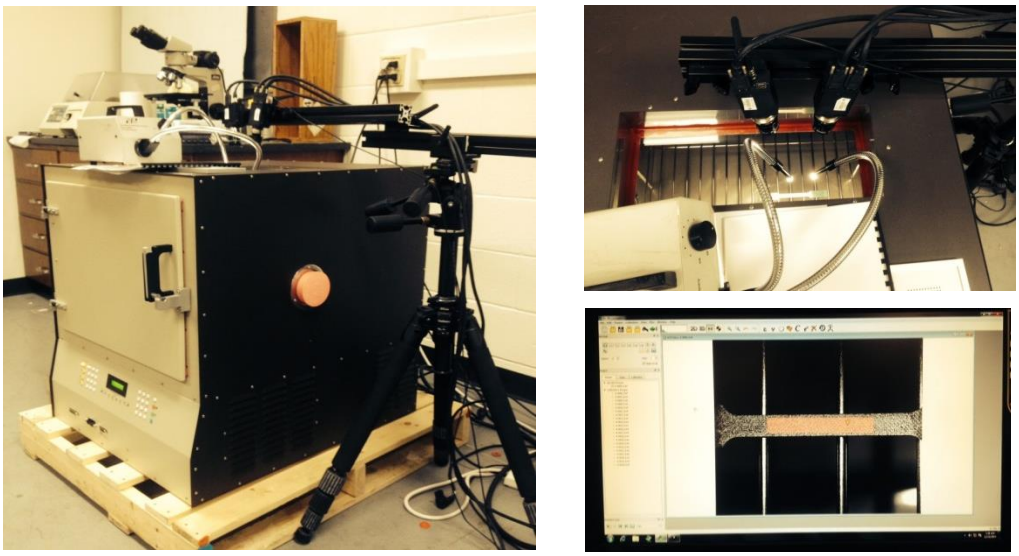


Figure 2-5 DIC Setup with Oven and Cameras

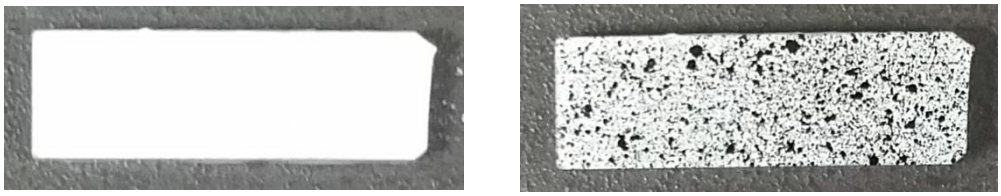


Figure 2-6 1. Test sample with white paint. 2. Speckled test sample

2.3.1.2 CTE Results

CTE measured using DIC are given in the graph below. In-plane and out-of-plane CTE was found to be 21 ppm/°C and 72.4 ppm/°C.

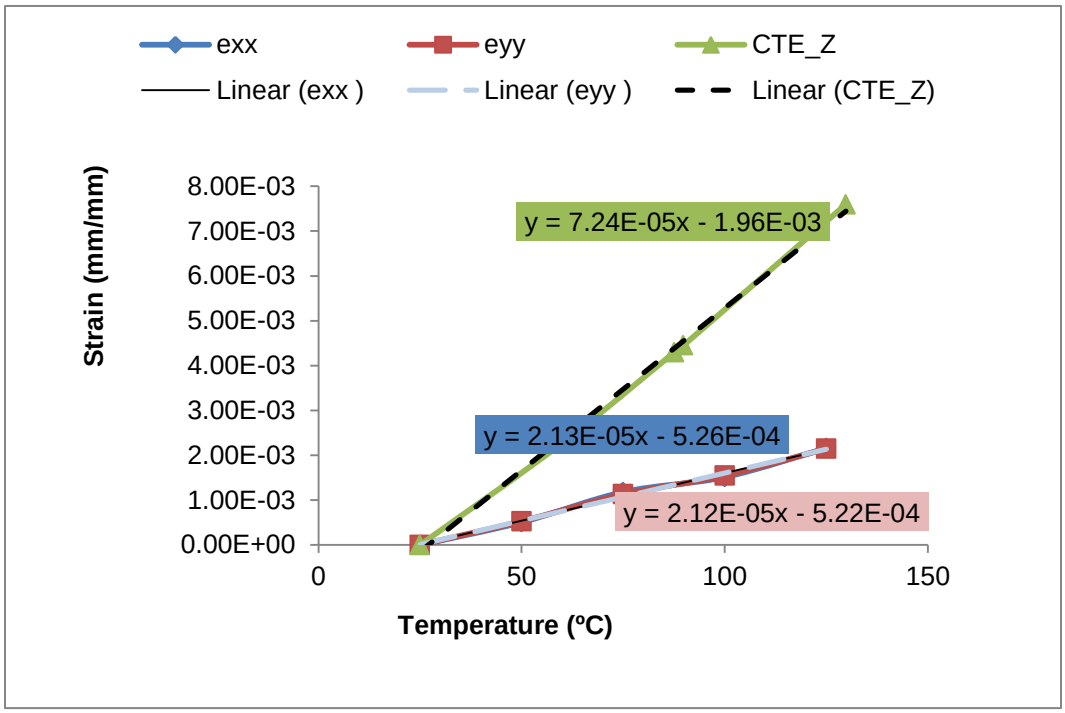


Figure 2-7 In-plane and out of plane CTE

2.3.2 Elastic Properties Measurement

Young's Modulus or Elastic Modulus defines the stiffness of compliance of a material when subjected to tensile or compressive loading. Materials that deform by a small amount when tensile load is applied to them are said to be stiffer as compared to the materials that deform by a considerable amount when tensile or compressive loading is applied to them. Mathematically, Young's Modulus is defined by the stress produced in a material when some strain is applied to it.

$$E = \frac{\sigma}{\epsilon}$$

Where,

E – Young's Modulus (MPa)

σ – Stress (MPa)

ϵ - Strain (mm/mm)

2.3.2.1 Instron Micro tester – Young's Modulus Testing

To conduct Young's Modulus measurement tests, an Instron Micro tester of 2kN load cell was used to apply tensile loading to the samples. An extensometer is placed on the sample to measure strain during sample extension. The extensometer is connected to software to while the Instron is also connected and it gives in-situ force-displacement graph during the test. Stress is calculated by dividing the stress from the cross-sectional area of the sample and strain is measured using the extensometer. From the stress and strain, Young's Modulus is calculated for a sample.

ASTM standard was followed to prepare dog bone samples for Instron test. The final shape of the sample is shown in the figure below

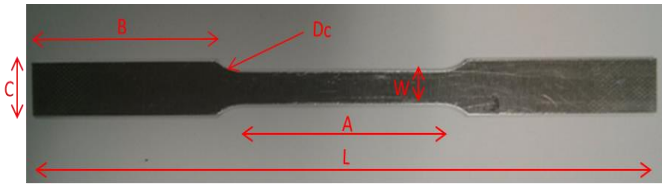


Figure 2-8 PCB dogbone sample

The dimensions of the sample as referred from the ASTM standards is given below

Table 2-1 PCB dog bone sample dimensions

Dimensions	Value (mm)
L - Overall Length	100
C – Width of grip section	10
W – Width	6
A – Length of Reduced Section	32

B – Length of Grip Section	30
Dc – Curvature Distance	4
R – Radius of Curvature	6

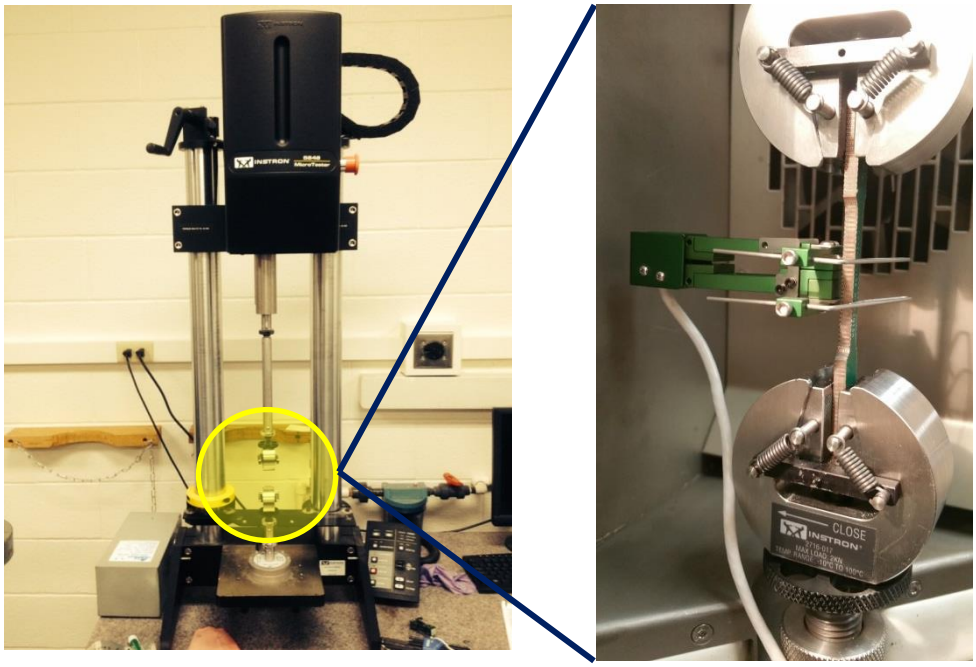


Figure 2-9 Instron Micro tester

The test setup and procedure as shown in fig 4 was benchmarked by testing an aluminum sample and calculating the Young's Modulus.

2.3.2.2 Test Results

After testing PCB, elastic modulus and Poisson's ratio of the PCB were found to be 30 GPa and 0.4. Following graph shows the stress-strain curve as determined by the Instron micro tester-

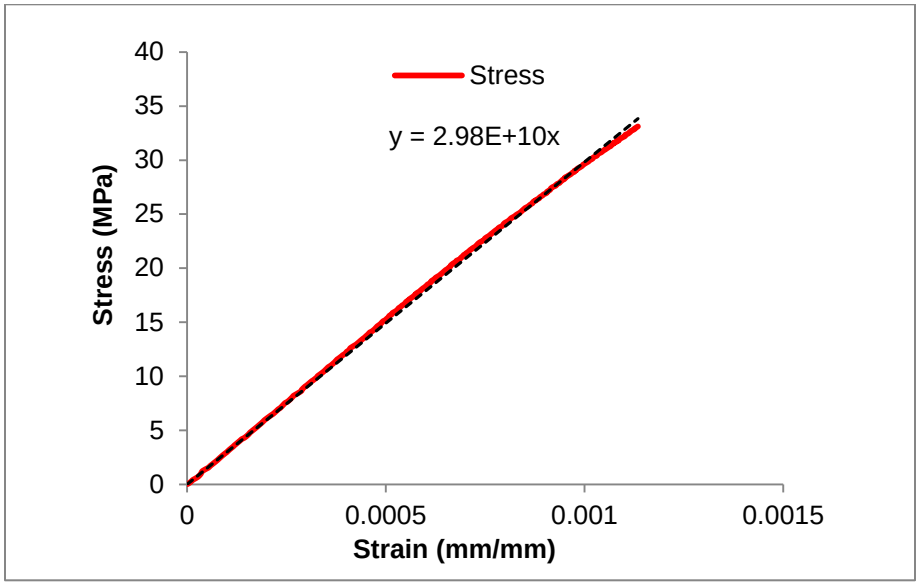


Figure 2-10 Elastic Modulus of PCB

2.3.3 Layer removal CTE analysis

A sample of 15mm x 5mm was used to perform layer removal using for thick board. The total layers distribution was 2 solder mask, 16 Cu layers and 15 FR4 layers as shown in figure 2-12.

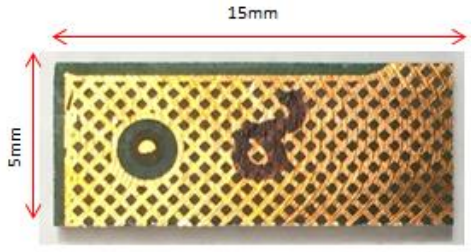


Figure 2-11 Sample of PCB after layer removal

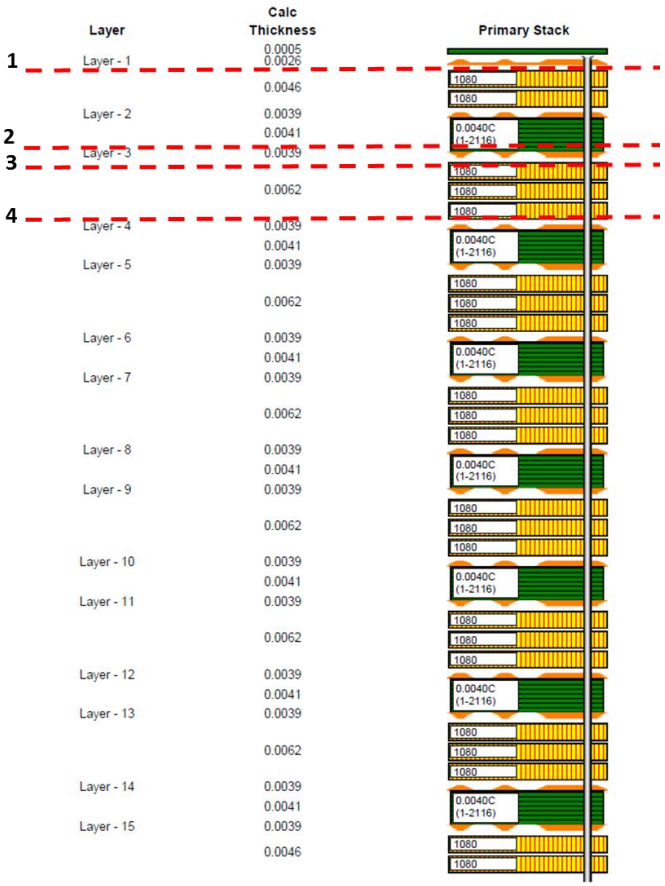


Figure 2-12 Thick board stack up for layer removal

The sample details on layer removal are shown as below in table 2-1:

Table 2-2 Layer removal samples detail

1	Removed SM + 1 Cu layer	35 um	One Side (Top / Bottom)
2	Removed 2 Cu layers + 2 FR4	375 um	
3	Removed 3 Cu layers+ 2 FR4	470 um	
4	Removed 3 Cu layers + 3 FR4	615 um	

a	Removed SM + 1 Cu layer	70 um	Both Side (Top and Bottom)
b	Removed 2 Cu layers + 2 FR4	375 um	
c	Removed 3 Cu layers+ 2 FR4	470 um	
d	Removed3 Cu layers + 3 FR4	615 um	

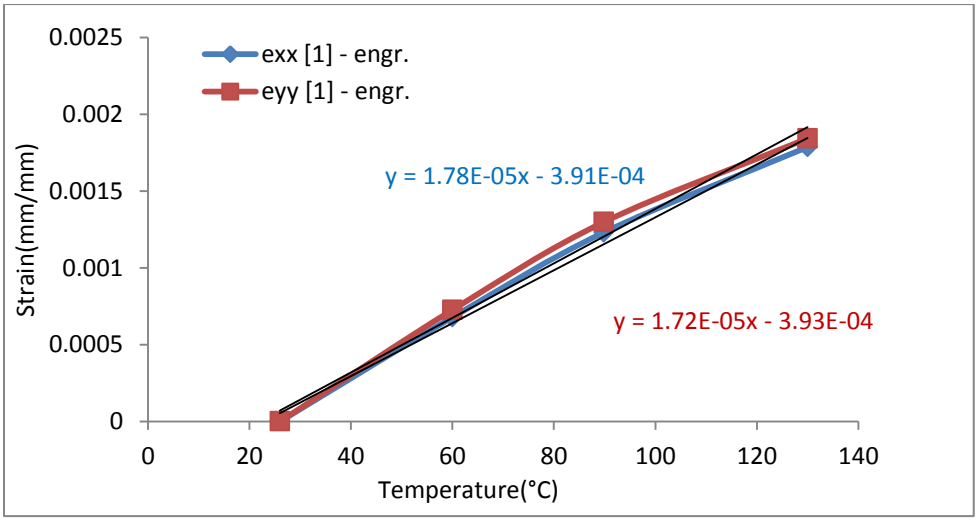


Figure 2-13 Removed SM + 1 Cu layer (Total 70µm)

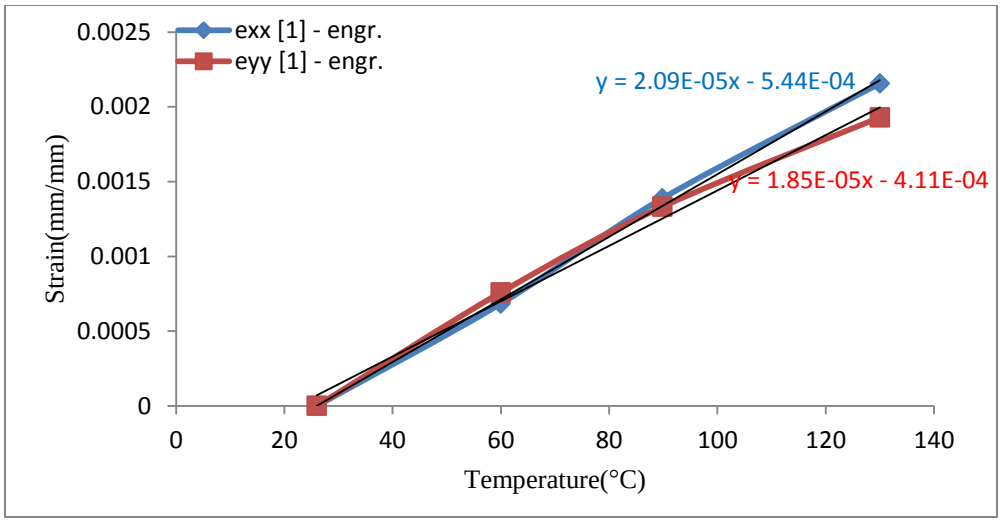


Figure 2-14 Removed 2 Cu layers+2 FR4(Total 375µm)

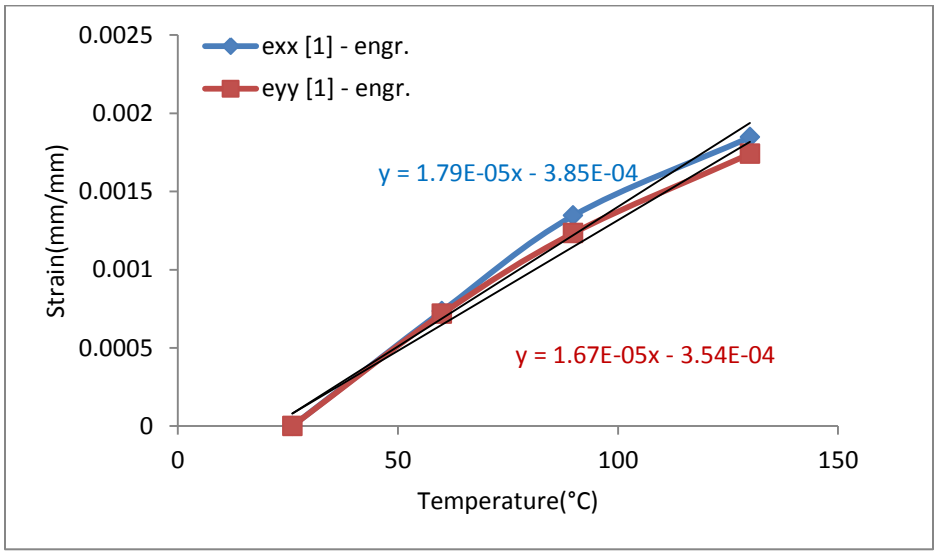


Figure 2-15 Removed 3 Cu layers+2Fr4 (Total 470µm)

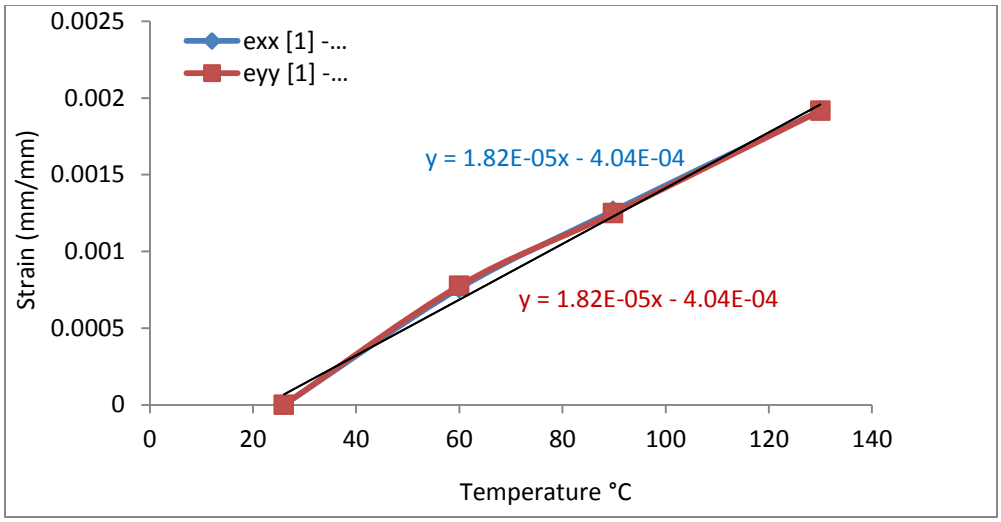


Figure 2-16 Removed 3 Cu layers + 3 FR4 (Total 615 µm)

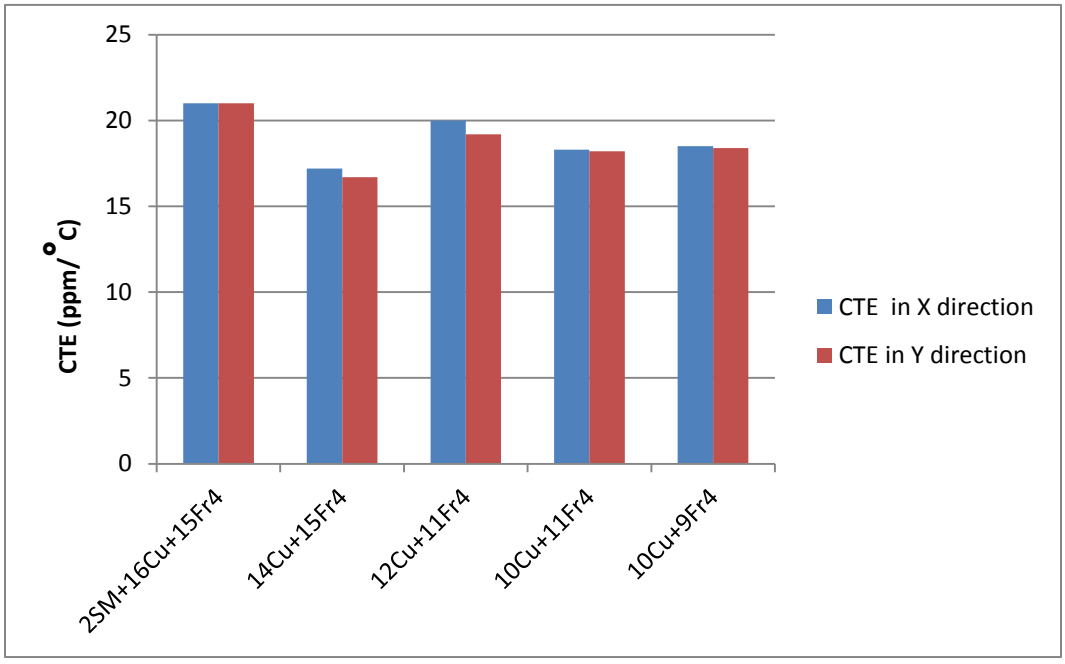


Figure 2-17 Summary - Layer removed from both sides

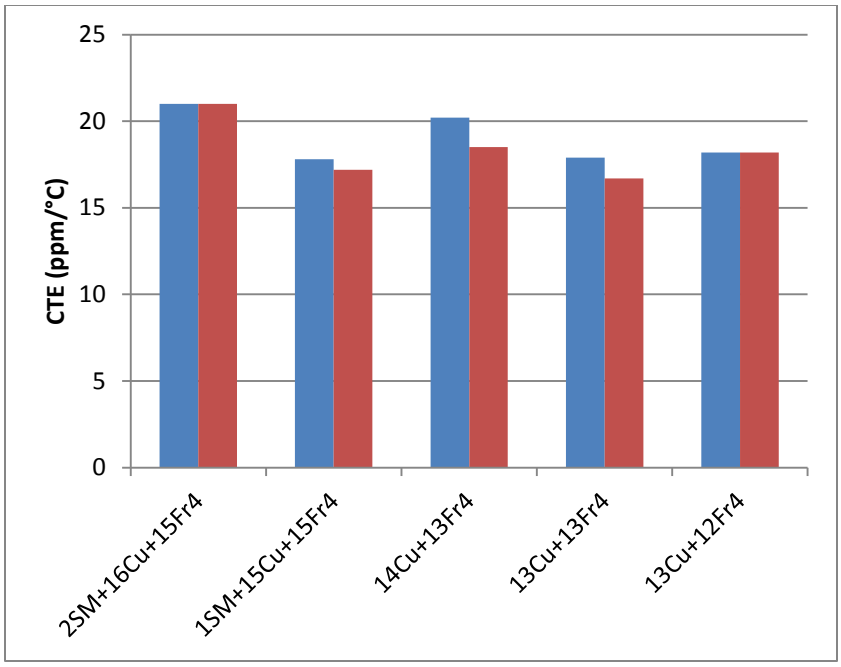


Figure 2-18 Layer removed from one side

CTE of Cu= 17 ppm/C; FR4 (without copper)= 12-14 ppm/C and SM= 30 ppm/C. It is found that in-plane CTE of PCB= 20-21 ppm/C with (CU, FR4 and solder mask). Removing Solder mask layer (either one side or both) causes in-plane CTE to decrease from 20-21 to 16-17 ppm/C. Preliminary investigation indicates, change in layers of PCB or no. of layers of FR4 and Cu has effects on in-plane CTE of PCB.

2.4

FINITE ELEMENT MODEL AND BENCHMARKING

2.4.1 Introduction to Finite Element Method

The Finite Element Method is a computational technique used to obtain approximate solution to boundary value problem in engineering. FEM is virtually used in almost every industry that can be imagined.

"The Finite Element Method is one of the most powerful numerical techniques ever devised for solving differential equations of initial and boundary value problems in geometrically complicated regions" [11]. Sometimes it is hard to find analytical solution of important problems as they come with complicated geometry, loading condition, and material properties. So FEA is the computational technique which helps in reaching the satisfactory results with all the complex conditions that can't be solved through analytical procedure. There are wide range of sophisticated commercial code available which helps in reaching the approximately close solution in 1D, 2D and 3D. In this FEA method, the whole continuum is divided into a finite numbers of small elements of geometrically simple shape. These elements are made up of numbers of nodes. Displacement of these nodes is unknown and to find it, polynomial interpolation function is used. External force is replaced by an equivalent system of forces applied at each node. By assembling the mentioned governing equation, results for the entire structure can be obtained.

$$\{F\} = [K]\{u\}$$

Where, {F} = Nodal load/force vector

[K] = Global stiffness matrix

{u} = Nodal displacement

Structure's stiffness (K) depends on its geometry and material properties. Load (F) value has to be provided by user. The only unknown is displacement (u). The way in

general FEA works is, it creates the number of small elements with each containing few nodes. There are equations known as Shape function in software, which tells software how to vary displacement (u) across the element and average value of displacement is determined at nodes. Those stress and/or displacement values are accessible at nodes which explains that finer the mesh elements, more accurate the nodal values would be. So there are certain steps that we need to follow during the modeling and simulation in any commercial code to reach approximately true solution, which would be explained [7]. In this study commercially available FEA tool, ANSYS Workbench has been leveraged.

2.4.2 FEA Problem Solving Steps

These five steps need to be carefully followed to reach satisfactory solution to FEA problem:

1) Geometry and Material definition
2) Defining Connection between bodies
3) Meshing the model
4) Defining load and boundary condition
5) Understanding and verifying the results

ANSYS is a general purpose FEA tool which is commercially available and can be used for wide range of engineering application. Before we start using ANSYS for FEA modeling and simulation, there are certain set of questions which need to be answered based on observation and engineering judgment. Questions may be like what is the objective of analysis? How to model entire physical system? How much details should be incorporated in system? How refine mesh should be in entire system or part of the whole system? To answer such questions computational expense must be compared to the level of accuracy of the results that needed. After that ANSYS can be employed to work in an efficient way after considering the following:

- Type of problem
- Time dependence
- Nonlinearity
- Modeling simplification

From observation and engineering judgment, analysis type has to be decided. In this study the analysis type is structural; to be specific out of different other structural problem focus in this study is on Static analysis. Non-linear material and geometrical properties such as plasticity, contact, and creep are available.

2.4.3 Finite Element Model of QFN package

The application of FEA modeling and simulation techniques used for the QFN package assembly is explained in this section. The ANSYS FEA procedures consist of three steps [8].

1) Preprocessing: Create geometric model, elements and mesh, input material properties.
2) Solution Process: Apply loads and boundary condition, output control, load step control, selecting proper solver, obtaining the solution.
3) Post processing: Review the result; list the result, contour map, result animation.

Certain assumptions have been made to carry out finite element analysis.

- All the parts in 3D package is assumed to be bonded to each other
- Temperature change in package during thermal cycling is assumed to be same throughout the package
- Except solder bump, all other materials are assumed to behave as linear elastic

2.4.4 Material Properties

Material properties used for FE model were linear elastic properties for copper pads/ lead frame, die, mold compound and solder mask. Linear orthotropic elastic

temperature dependent properties were used for PCB. SAC305 Solder was modeled as rate-dependent viscoplastic material using Anand's viscoplastic model, which takes into consideration both creep and plastic deformations to represent the secondary creep of solder. Through its material constants A, Q, ξ, m, n, h_0, a, s_0, ŝ, which are determined by curve-fitting the experimental data, Anand's law accounts for solder's strain-rate and temperature sensitivity. Anand's viscoplasticity model for solder can be described as follows- [15]

$$\frac{d\varepsilon_p}{dt} = A \sinh\left(\xi \frac{\sigma}{s}\right)^{\frac{1}{m}} \exp\left(-\frac{Q}{kT}\right)$$

With the rate of deformation resistance equation-

$$\dot{s} = \left[h_0(|B|)^{\alpha} \frac{B}{|B|}\right] \frac{d\varepsilon_p}{dt}$$

Where,

$$B = 1 - \frac{s}{s^*}$$

And

$$s^* = \hat{s}\left[\frac{1}{A}\frac{d\varepsilon_p}{dt} exp\left(-\frac{Q}{kT}\right)\right]^n$$

2.4.5 Package Geometry

A 3D 6 x 6mm QFN package was modeled in ANSYS v15.0 using the package drawings and optical microscope images. Figure 2-19 shows the cross-sectioning of the QFN package.

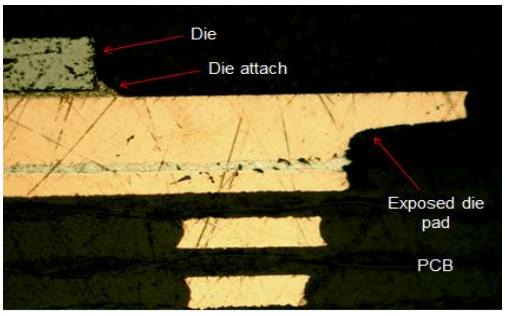


Figure 2-19 Cross section of QFN assembly

Figure 2-20 shows a 3D quarter geometry of 6 x 6mm QFN package. Quarter

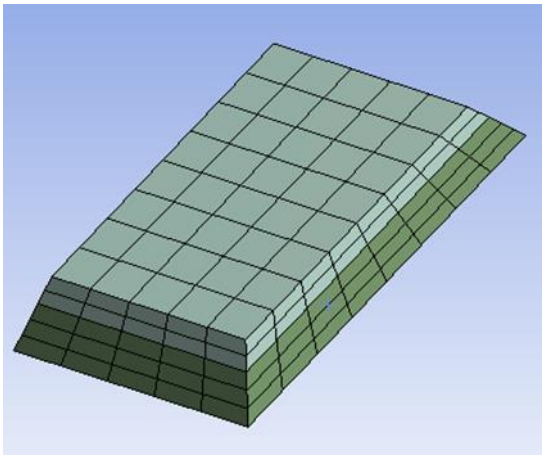
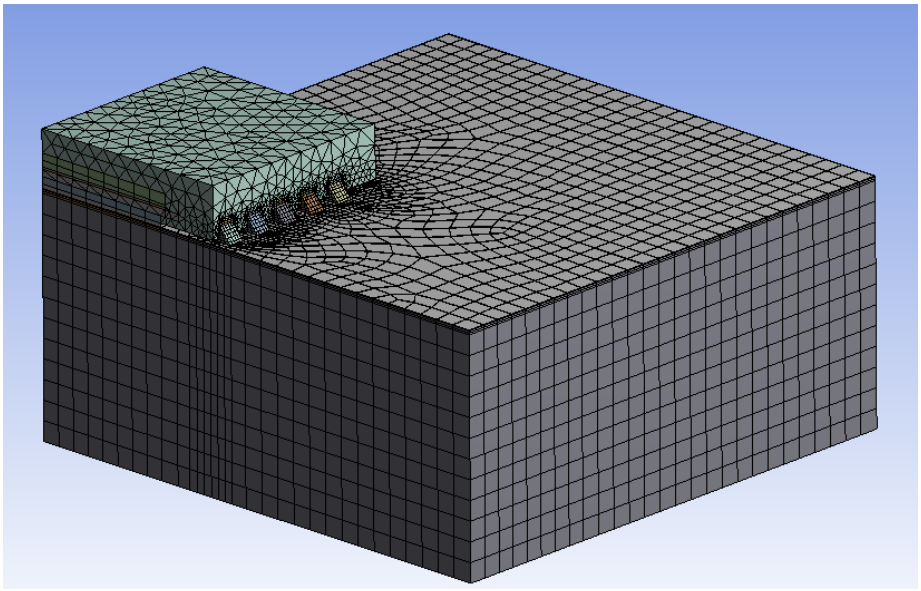


Figure 2-21 Mesh in solder layer

model is considered to save computational time without affecting the accuracy of the results. The model was discretely meshed using different meshing option in ANSYS Workbench v15.0. Mesh refinement and mesh sensitivity analysis was performed to

Figure 2-20 Meshed quarter symmetry QFN package



reach maximum accuracy with optimum solution time.

2.4.6 Loads and Boundary Conditions

Boundary conditions imposed on the global model can be seen in Figure 2-22. Symmetry boundary conditions are applied to the two boundary planes of the quarter symmetry model. The center node is fixed to prevent rigid body motion.

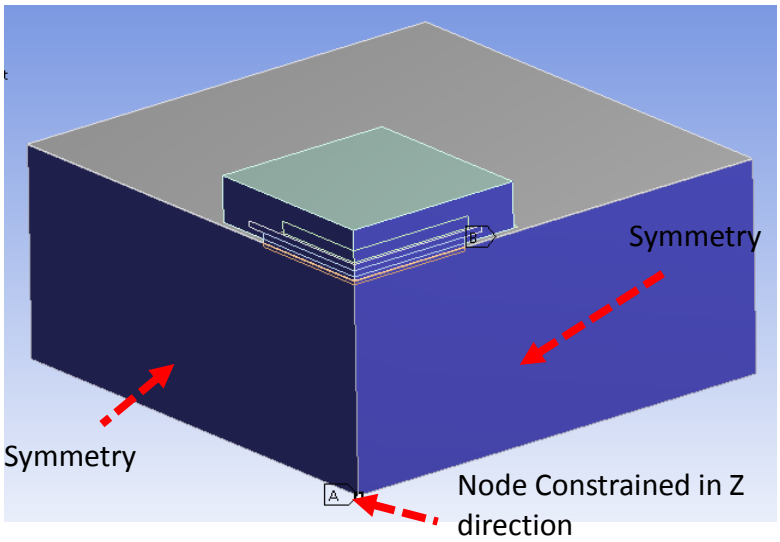


Figure 2-22 Boundary conditions in quarter symmetry model

Thermal cycling load of -40°C to 125°C ;15 min ramp/dwell was applied on the model as shown in the following Figure 2-24.Simulations are done over three complete cycles since most of the solder joints have reached a stable state after the end of third cycle. The initial stress-free temperature was set to be the maximum temperature in the cycle. Choosing the high dwell temperature of the BLR test as the stress-free

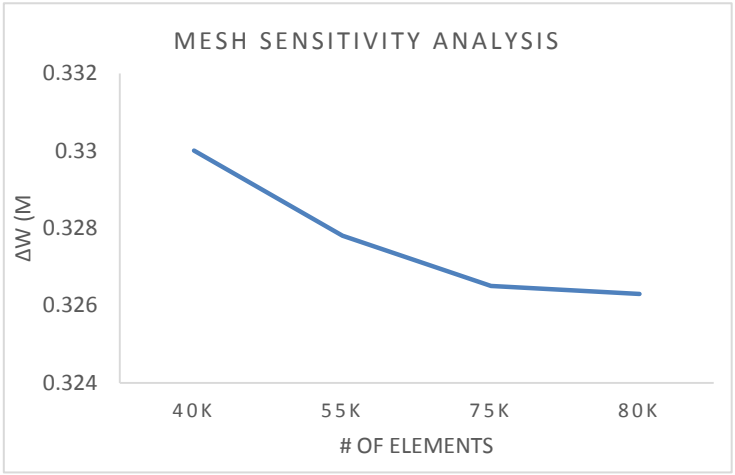


Figure 2-23 Mesh sensitivity analysis

temperature helps the system to reach the stabilized state faster.

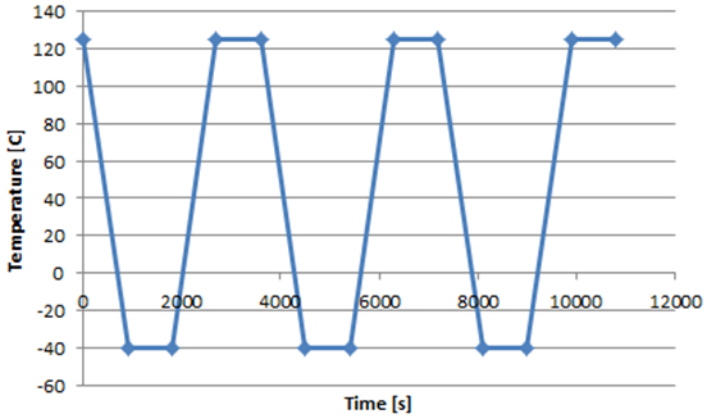


Figure 2-24 Temperature cycling profile

2.4.7 Post-Processing

Since solder is viscoplastic in nature, stress or strain based damage parameter may be accurate to quantify solder joint fatigue life. Hence, volume averaged plastic work accumulated between 3rd and 2nd cycle (ΔW_{avg}) is used a damage parameter. The results are volume averaged over 25µm layer thickness to minimize the effect of stress singularities in the model [16].

$$\Delta \mathrm{W}_{Avg.} = \frac{\sum W.V}{\sum V}$$

$$\Delta \mathrm{W}_{acc.} = \Delta \mathrm{W}_{Avg.3} - \Delta \mathrm{W}_{Avg.2}$$

Figure 2-25 Plastic Work

This damage parameter is then later used in parametric analysis and optimization.

2.4.8 Benchmarking

An FEA model to be reliable, accurate and to gain confidence in modeling, it needs to be benchmarked before using for solder joint fatigue life prediction. Therefore, a thorough study about the effect of different types of meshing methods, analysis/ solution controls was performed and later included in the workbench model used in this work.

Some of the key conclusions of the study which were included in the model are as follows-

1) Stress-free temperature - There are most commonly three types of stress free temperatures used in these analyses. First one is the melting temperature of solder approx. 200°C which assumes that solder starts providing mechanical support as soon as it solidifies. Second condition assumes that solder undergoes stress relaxation during storage and hence the stress free temperature is 25°C. Third condition assumes that solder is stress free at highest temperature (125°C) in the thermal cycle. Fan [10] demonstrated that use of high thermal cycling temperature as stress-free temperature leads to attain quickly stabilized strain energy density solutions which in turn significantly increases computational efficiency. Therefore, stress-free temperature of 125°C was chosen in this work.
2) Identical mesh (line divisions) in all solder volumes – It is imperative to provide identical mesh size/ divisions and element type in all the solder volumes on the periphery of the package to achieve consistent and accurate results. In this work, solder volume lines were divided as 8, 5 and 5 along its length, width and height.
3) Sub-steps - It is observed during the study that time discretization affects accuracy of the results. As the time divisions go on reducing, the solution reaches accuracy. But increasing time divisions, increases solution times

tremendously which makes it computationally inefficient. To overcome this problem, it is suggested to provide identical time divisions for each load step. In this study, all load steps are divided into 10 sub-steps.

4) Iterative solver used as opposed to direct solver – Iterative solver like Preconditioned Conjugate Gradient (PCG) solver is recommended for large models consisting of solid elements and fine mesh [14]. PCG solver is most robust solver, whereas direct solver is mostly recommended for small DOF linear analysis. Therefore, in this work PCG solver was used.
5) Large Deflection 'ON' and Rate 'ON' – These ANSYS commands are used in order to activate the effect of non-linear geometry and to include creep effect in the analysis.
6) Maintain equal thickness of critical solder layer for calculating plastic work – As the thickness of the solder regions on which the volume averaged accumulated plastic work (ΔWavg) is increased, the value of ΔWavg decreases. Hence, for consistent and accurate results, it is important to use same thickness layer for ΔWavg calculation. In this study, 25μ thick solder layer was chosen for calculating ΔWavg.

2.5

PARAMETRIC ANALYSIS OF QFN PACKAGE

In this design study, the effect of some of the key package parameters such as package geometry and material properties are investigated in an attempt to improve the solder joint reliability of the QFN. The parameters in focus are Die size, Die thickness, Solder stand-off height, Solder fillet length and Center solder under die pad. Only one package parameter is modified at a time to study its effect on the solder joint reliability. The analysis is done on QFN package with the same material properties but on thick board.

The main objective is to study the effects on these key parameters on the solder joint fatigue life to support package design for reliability in different applications.

2.5.1 Effect of Die Size and Die Thickness

Selecting smaller die size and die thickness is better for reliability because the die edge is farther from the peripheral solder joint thus resulting in less local CTE

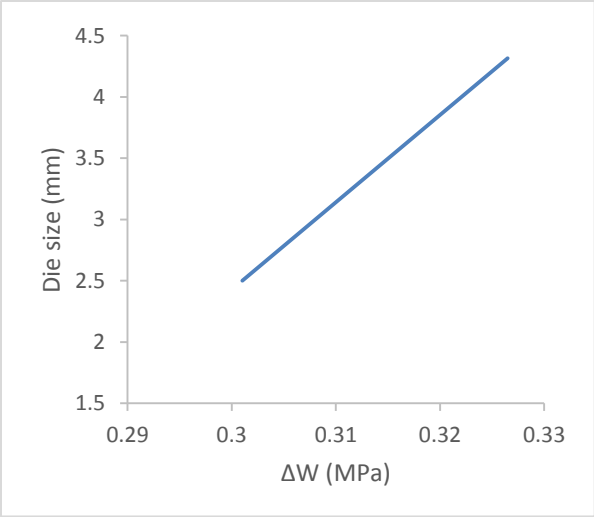


Figure 2-26 Graph of die size vs. ΔWavg

.mismatch.

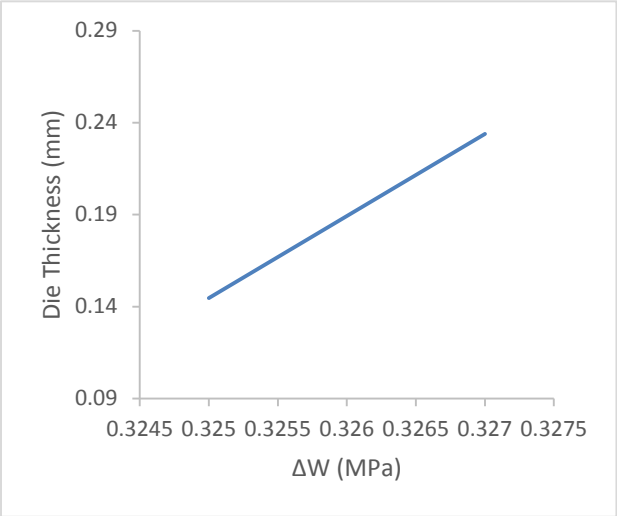


Figure 2-27 Graph of die thickness vs. ΔWavg

2.5.2 Effect of Solder Stand-off height

Generally, higher solder stand-off height has longer fatigue life. The larger solder thickness helps to reduce the plastic work induced during thermal cycling. Also, more solder volume means more resistance to the crack propagation in the solder joint.

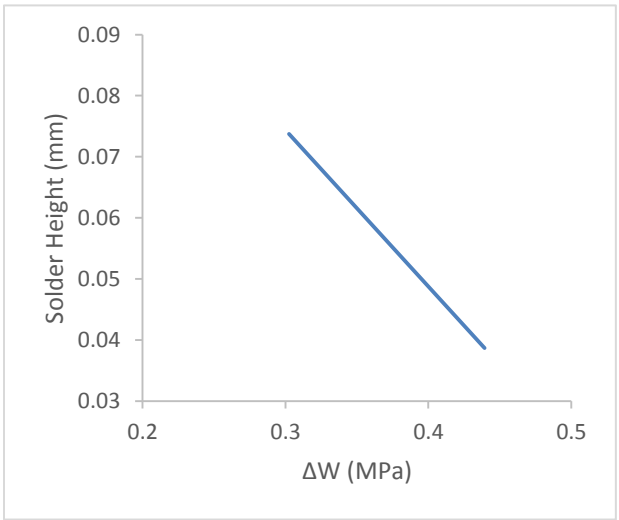


Figure 2-28 Graph of solder standoff height vs. ΔWavg

2.5.3 Effect of Center Solder under Die Pad

Amount of center pad soldering affects QFN reliability on thick board. As much as, 40% decrease in reliability is observed when there's no solder under die pad. This is associated with the reduced amount of solder volume thereby providing less support to the package.

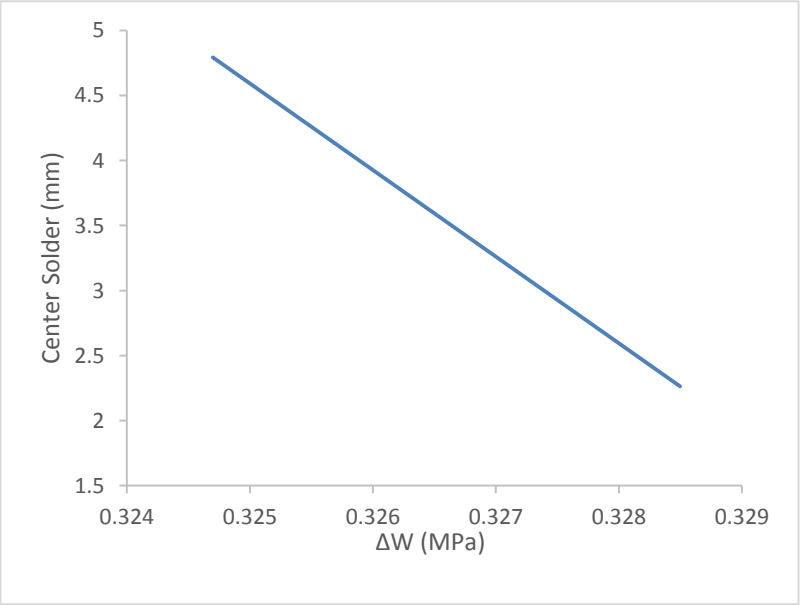


Figure 2-29 Graph of center solder vs. ΔWavg

2.5.4 Effect of Solder Fillet Length

More solder length has more solder volume and hence more solder available to absorb the damage. This strengthens the critical solder joint. The effect of different solder fillet length on plastic work is shown in the graph below

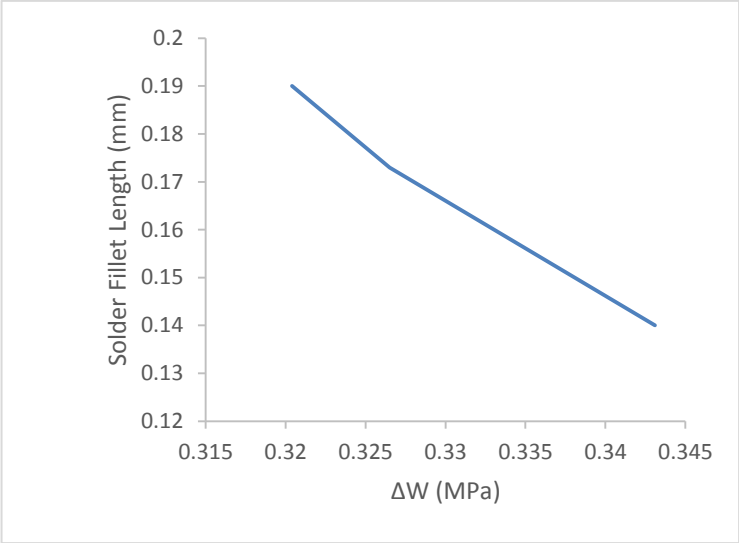


Figure 2-30 Graph of solder fillet length vs. ΔWavg

2.5.5 Effect of corner anchors and corner underfill

There were four sacrificial anchor pads added as shown in the figure 2-31. This improved the solder joint reliability by ~67% based on the FEM model. There was a matching CTE underfill selected which was dispensed only in corner area of the package. This was done to reduce the quantity of underfill used and help inspect the solder

underneath the package. This technique improved the reliability by another~70% from base model.

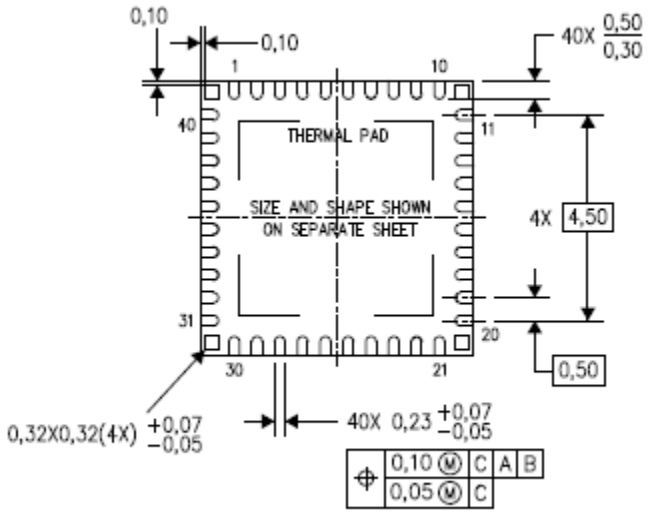


Figure 2-31 Corner anchors added to base QFN [5]

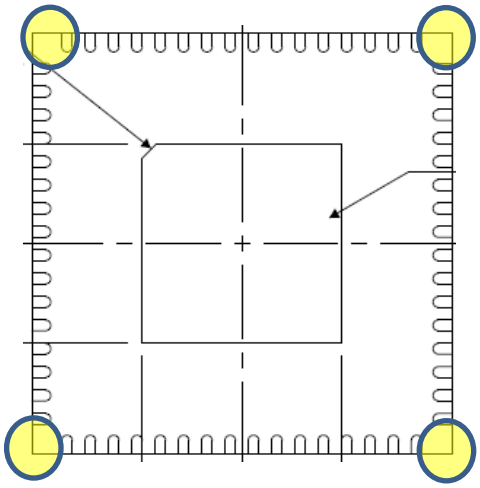


Figure 2-32 Underfill added in the corner to base QFN

2.6 Conclusion and optimization

In this work, QFN package was analyzed to assess the board level reliability under thermal cycling. First section involved understanding various meshing, analysis/solution controls to benchmark the FE model in ANSYS workbench. Benchmarking was necessary to create a reliable and accurate modeling methodology. In benchmarking process, it was observed that factors such as stress-free temperature, number of sub-steps, type of solver, type of mesh and thickness of solder layer used for calculating plastic work are the ones which affect volume averaged accumulated plastic work values.

Material characterization of PCB was performed using Instron micro-tester and Digital Image Correlation technique in the second section. All the measurement tests were first benchmarked with Al sample and results were found to be in close agreement. The in-plane Young's modulus and Poisson's ratio was found to be 30 GPa and 0.4, while in-plane and out-of-plane co-efficient of thermal expansion were 21 ppm/°C and 72.4 ppm/°C. Anand's viscoplastic constitutive law was used to describe the inelastic behavior of the lead-free solder alloy.

In the third section, a parametric design analysis was performed on QFN package mounted on thick FR-4 board to understand the effect of each parameter on reliability of the package. It was concluded that for better reliability it is recommended to have smaller die size and die thickness, larger solder stand-off height and longer solder fillet length, adding corner anchor and corner underfill.

Overall combination of thinner package with thinner die with corner anchor and corner underfill helped improve the reliability to pass IPC requirements.

Chapter 3 Reliability of Ball grid array package

3.1 Introduction

The role of electronic packaging is becoming more important and now constitute a much bigger percentage of the development of package with high evolution due to strong and competing demands for increased functionality and performance, further miniaturization, heightened reliability, and lower costs. Various types of packages like BGA and Quad Flat No-Lead (QFN) are widely used. Ball Grid Array package was developed out of the need to have a more robust and convenient package for integrated circuits with large numbers of interconnects. Moreover, BGA uses efficient board space, improved thermal and electrical performance, reduced package thickness and improved reworkability resulting from larger pad size. The different layers with different material properties inside the PCB (Printed Circuit board) make the PCB highly orthotropic. Additionally, prepreg materials are viscoelastic and they provide some sort of stress relaxation and creep characteristics. Currently, there are two types of boards that are used with BGA packages. One of the types has RCC film as the uppermost and lowermost prepreg substrate while the second type has FR4 film as the uppermost and lowermost prepreg substrate [11]. By using Dynamic Mechanical Analyzer (DMA), time and temperature-dependent viscoelastic properties of the board are obtained. Using Thermomechanical Analyzer (TMA), Coefficient of Thermal Expansion (CTEs) of the boards are obtained. In summary, in this study, the mechanical characterization of BGA PCBs with FR4 and RCC is presented along with the thermal cycling simulation results from ANSYS and the reliability of two types of boards were compared. The computational analysis includes lumped and layered model for detail analysis. The Volume averaging

technique is implemented to calculate the strain energy density. The Critical solder joint is determined from the static structural analysis under thermal loading.

BGA is a type of Surface Mount Technology packages. BGA is used extensively due to its robust design with many interconnects and improved connectivity with lower thermal resistance. Intensive research and development on BGA motivate us to study in detail about the layer stack up for the corresponding boards [15]. This variety of material in a single package results in building into a complex system and increasingly retains high levels of reliability. Reliability is dependent on various factors like the operation of the device, power consumption, heat dissipation and the environment (ambient temperature, temperature changes, environmental strains). The buildup layer of PCB affects the reliability of solder joints; it affects the creep strain range, stress range, creep strain energy density ranges and the thermal fatigue life . The solder balls on a populated PCB absorb all the strains due to the expansion of the package and by the PCB in thermal excursions. At high temperatures, there is a high possibility of the solder joint to fail due to the CTE mismatch between the PCB and the package [11]. Also, the stiffness of a PCB is higher than the package which affects the reliability of a solder joint. In this paper, the study of the effect of RCC and FR4 prepreg layers on solder joint failure for two different PCB is presented. To analyze the failure, we use ATC as the test. The simulations are run for the temperatures loading from -40^0 C to 125^0 C, and dwell and ramp time of 15mins. The work includes two types of BGA boards, using RCC and FR4 as the prepregs at the outermost layers. In this work, we have investigated the board level reliability of these two different boards. Finite Element Analysis (FEA) is used to determine the fatigue co-relation parameters such as elastic strain, stresses, directional deformation and accumulated volume average plastic work to predict the characteristic life of the package [13].

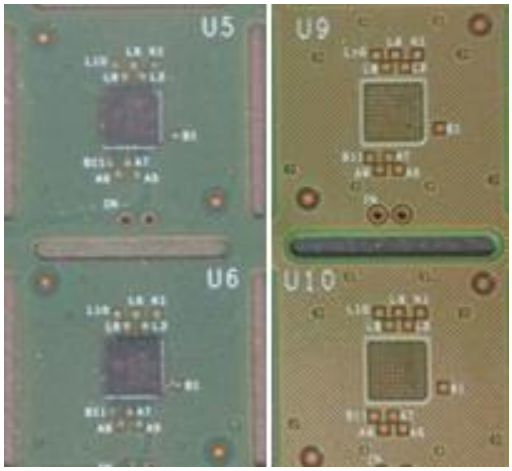


Figure 3-1 boards with FR4 (U5and U6) and RCC laminate (U9 and U10)

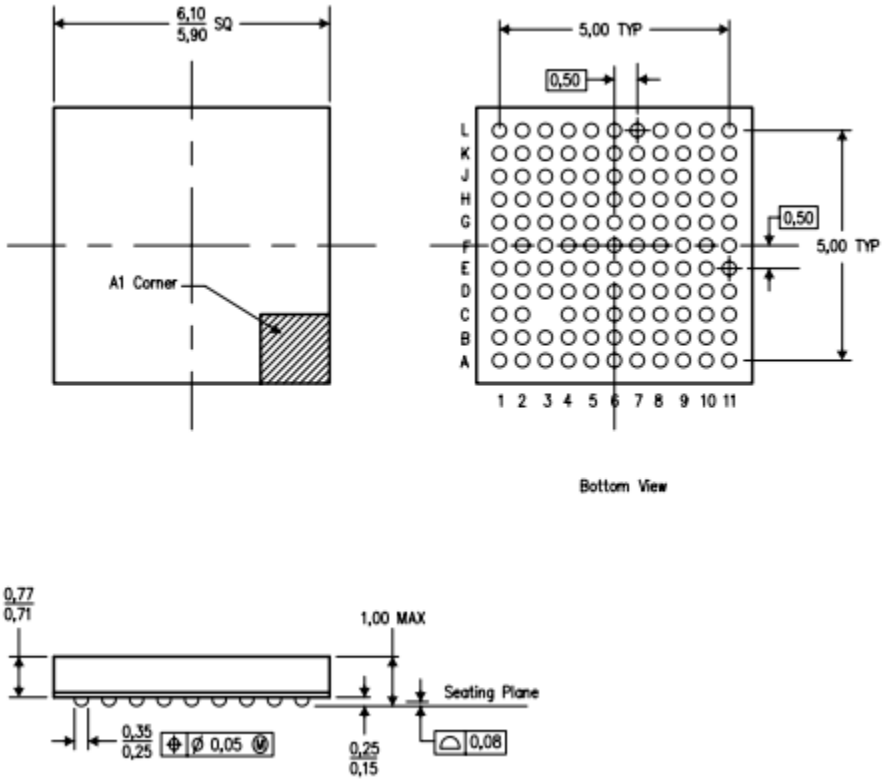


Figure 3-2 Layout and design for 120 pin BGA

The above layout is the package dimension of BGA with 120 solder ball. The correct dimension of the package and PCB is important for analysis.

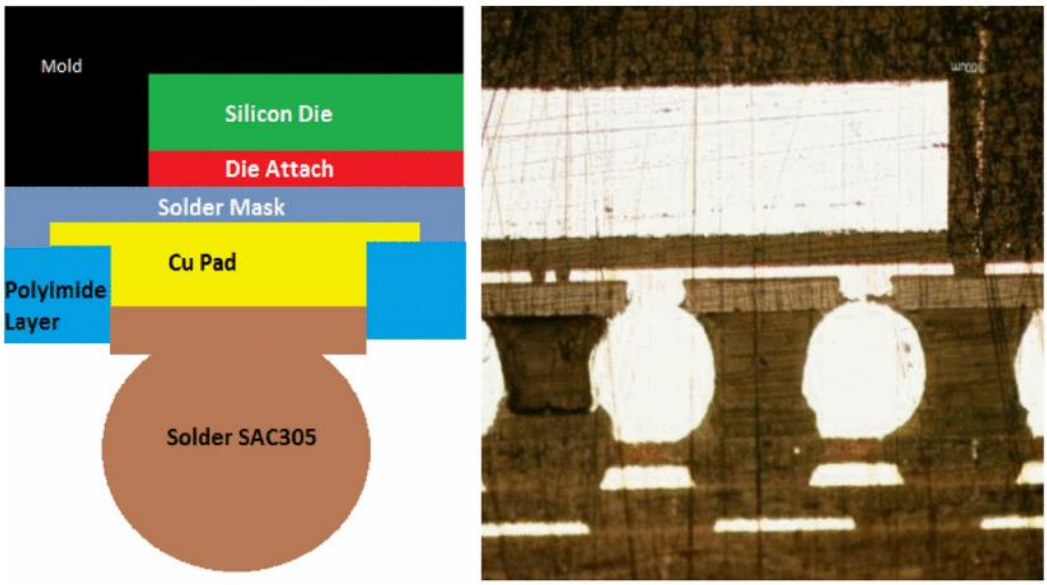


Figure 3-3 Package components (a) schematic drawing, (b) optical microscopy image

Figure 3-3 shows a clear picture of the components of the Ball Grid Package. The package basically comprises a copper pad on the top and bottom side of the solder bump. On the die side, the silicon die is attached which is further attached to polyimide layer with an adhesive layer in the middle. The solder mask in present both, the PCB side and the substrate side as shown in the schematic.

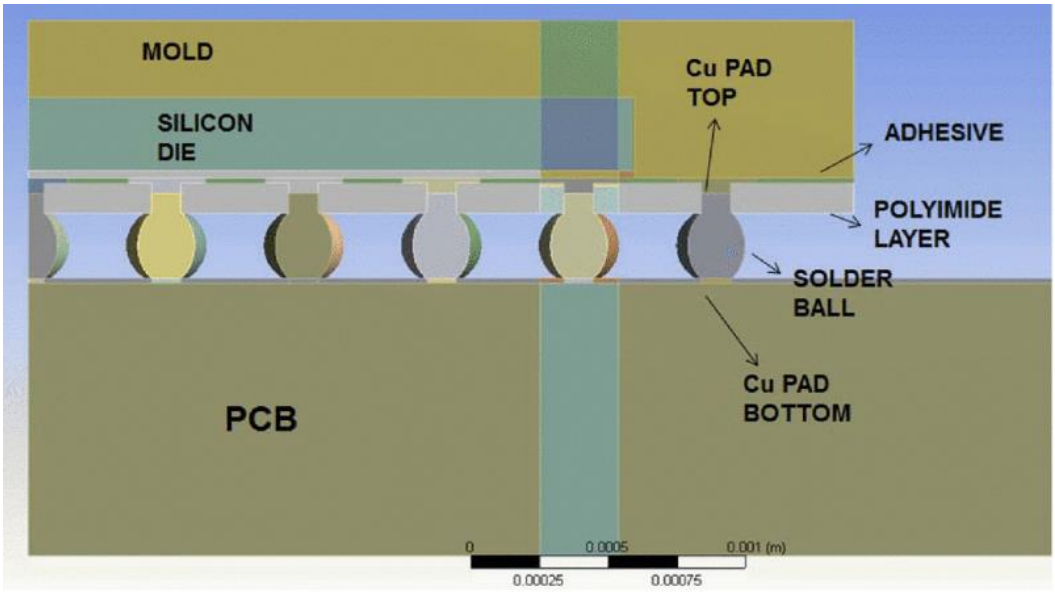


Figure 3-4 BGA assembly model with labeled component names

The dimension from the drawings, X-ray images, and the cross-section images are considered in creating a 3D model of the BGA package. The FE modeled BGA package is shown in figure 3-4. Symmetry allows for an octant symmetric model resulting in significant savings of computational time. The PCB layout (prepreg layer and the number of copper layers inside the pcbs) is determined by cross-sectioning the PCB as shown in figure 3-5 and 3-6. The detailed PCB with the layers is modeled inside a sub model. The PCB comprises of 1-6-1 configuration which means the PCB comprises of 8 copper layers where copper layers contribute to form a core layer of the pcb. The prepreg layer is present in between the PCB core layer and the outermost copper layer as shown in figure 5.

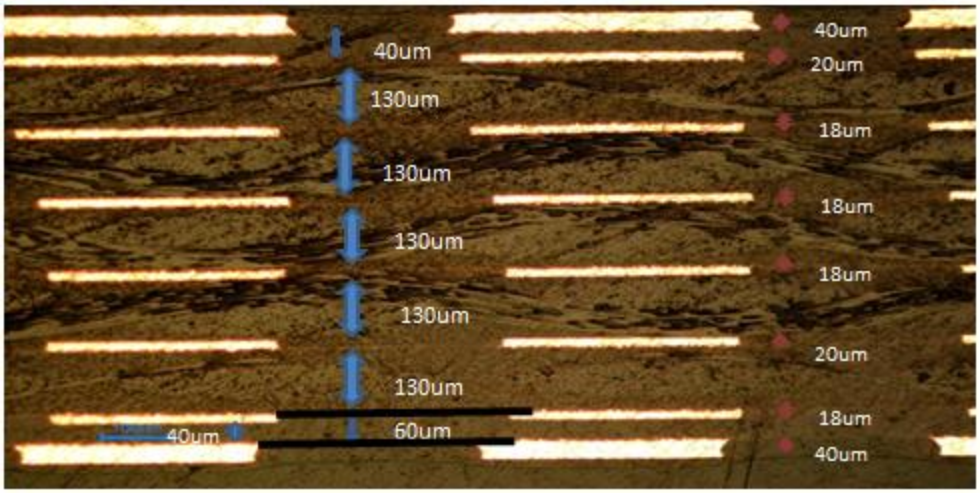


Figure 3-5 Layer stack-ups of 1 mm BGA board with RCC prepreg

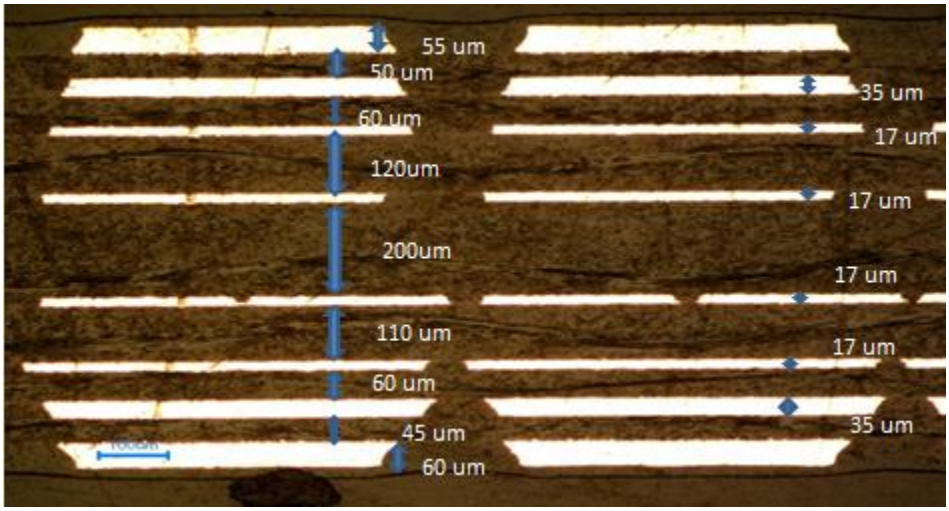


Figure 3-6 Figure 3 6 Layer stack-ups of 1 mm BGA board with FR4 on outer layers

11x11pin BGA package with PCB (two prepregs, FR4 and RCC) thickness of 1 mm were tested for temperature loading ranging from −40°C to 125C with 20 min dwell and ramp time [12]. It's important to test both the package and board sides of solder joint

for analysis. In this paper, plastic work is calculated in two sides, i.e. top and a bottom portion. To reduce simulation time, dwell and ramp time used for the analysis is 15mins which is considerable for the comparative study.

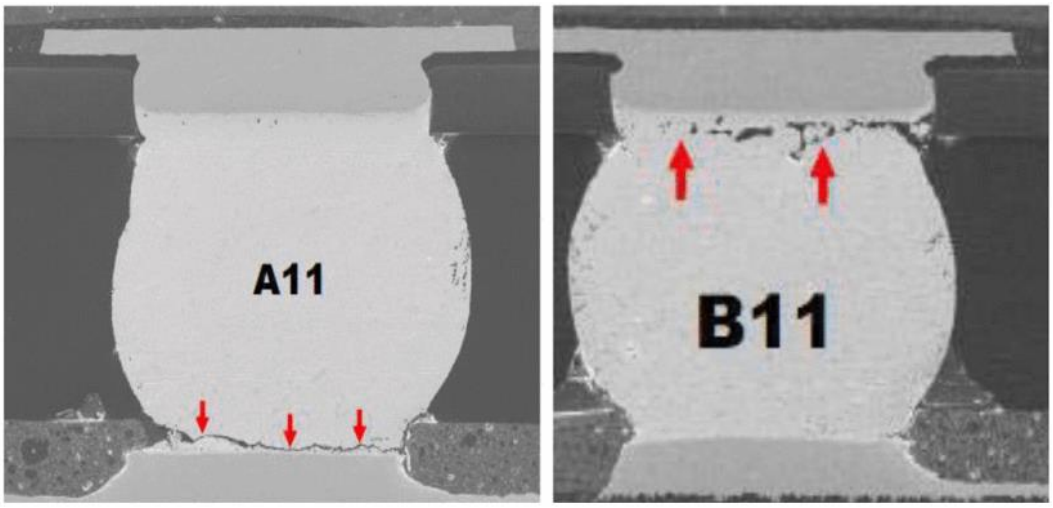


Figure 3-7 Solder joint failure occurred on the PCB side, (b) failure occurred on the substrate side of the package

3.2 Material Characterization

Material characterization is a very important step in FE Analysis of boards. For lumped analysis, it is necessary to predict precise material properties for the boards. Specifically, in this study, we are going to calculate CTE, Modulus of Elasticity and Poisson's ratio for the board using lumped approach. Various test setups were used to calculate material properties.

Figure 3-8 TMA and DMA sample

3.2.1 Thermo-Mechanical Analyzer (TMA)

TMA is a device with a thermal chamber which has a good working range of temperature. TMA is used to measure in-plane and out of plane CTE of the different boards. For this experiment sample is prepared using High-Speed Cutter, samples are typically cut into 8 by 8 mm of a square shape. The samples are cut to such a dimension that it should sit below the probe inside the thermal chamber. The probe of the TMA is of Quartz, which seats on the sample and relative movement of probe gives the CTE plot. CTE can be calculated for a temperature range of −65°C to 260°C, with a temperature increment of 3°C/min. Three experiments were performed for each measurement and the average value was taken.

Figure 3-9 (a) Thermomechanical analyzer (TMA), (b) universal testing machine (UTM)

CTE is measured using TMA in all direction. The out of plane CTE for both the PCB board. Placing PCBs sample in different orientation under TMA's quartz probe, we can measure CTE in a different direction. For example, in-plane CTE result is shown in . All measurements are done for temperature range −65°C to 260°C, so it can be used for all type of thermal loads. After 115°C, cold crystallization and recrystallization process occur due to which the sample shrinks and shows a significant dip in CTE values. Afterward, sample expands again after crystallite formation above 135°C and finally melts. The decrease in sample height and viscosity can be seen after 205°C which shows the beginning of melting process.

3.2.2 Universal Testing Machine (UTM)

UTM is a tensile testing machine which was used to calculate the modulus of elasticity and Poisson's Ratio of the boards at room temperature. Sample preparation was done by cutting the boards in dog-bone shaped as per the ASTM D412 Standards. The length of the dog bone sample was 100mm with the width of 16mm. The length in the middle section was 33mm and the grip section was 30mm. A force per unit length of magnitude 2 N/m is applied to the samples. Figure below shows how the sample was held in two jaws to carry out the experiment. Extensometer was placed at the center of dog bone sample during a tensile test and the lateral deformation was measured to calculate Poisson's ratio.

Table 3-1 Package Material Properties

Material	CTE (ppm/C)	E(Gpa)
Copper Pad	17	11
Die Attach	65	1.54
Die	2.9	150
Mold	8	24
PI Layer	35	3.3
Solder Mask	30	41.37

All the measured values were temperature dependent. For computational analysis, all values for PCB was taken as temperature dependent for accuracy. The average fit value for CTE and Young's modulus are given in table 3-2.

Table 3-2 PCB board Material Properties

Package	Exx (Gpa)	CTE (x) ppm/°C	CTE (z) ppm/°C	Tg (°C)
With RCC	28.5	15.6	74.1	100.4
With FR4	27.8	19	44.5	119.2

3.2.3 Layer Removal

The layers were removed using milling process on both boards. Cu layers and prepreg is removed from outer layers. The results show that after removing Cu and prepreg from outer layers, both samples are essentially the same with similar in-plane CTE values.

Table 3-3 Summary of Layer removal

	FR4 Board 1 mm		**RCC Board 1 mm**	
	Initial Board Configuration	Cu and Prepreg Layer Removed	Initial Board Configuration	Cu and Prepreg Layer Removed
CTE X-Direction(ppm/degree)	19	16.2	15.6	16.2
E (GPa)	27.8	30.4	28.5	28.9
No. of Cu Layers	8	6	8	6

3.3 Finite Element Model

Mechanics is characterized by its branches being: Theoretical, Applied, Computational, and Experimental. The Finite Element Methods are shelved under the computational branch. In this study, an octant symmetry exists and hence is utilized for savings computational time. Symmetric boundary conditions are applied to the two faces towards the inside where the geometry is split.

3.3.1 Material Properties

The nature of all the properties was linear elastic, except the solder balls and the PCB. The solder balls were considered as visco-plastic and so Anand's model was used to explain the behavior of the solder balls. SAC 305 where the material composition is 96.5% Tin (Sn), 3.0% Silver (Ag) and 0.5% Copper (Cu) is what made up the solder ball. The Anand's constants are given in Table 3. The PCBs were taken as linear orthotropic in nature. As mentioned in the assumptions, solder is modeled as rate dependent viscoplastic material which uses Anand's viscoplastic model. It takes both creep and plastic deformation into consideration to represent secondary creep of the solder. Anand's law consists of nine material constants A, Q, ξ, m, n, hu, a, su, s^.

$$\frac{d\varepsilon_p}{dt} = Asinh(\xi\frac{\sigma}{s})^{\frac{1}{m}}\exp\left(-\frac{Q}{KT}\right)$$

$$s = [h_0(|B|)^{\alpha}\frac{B}{|B|}]\frac{d\varepsilon_P}{dt}$$

$$B = 1 - \frac{s}{s^*}$$

$$s' = \hat{s}\left[\frac{1}{A}\frac{d_{\varepsilon_p}}{dt}\exp P(\frac{Q}{KT})\right]^n$$

3.3.2 Loading and BCs

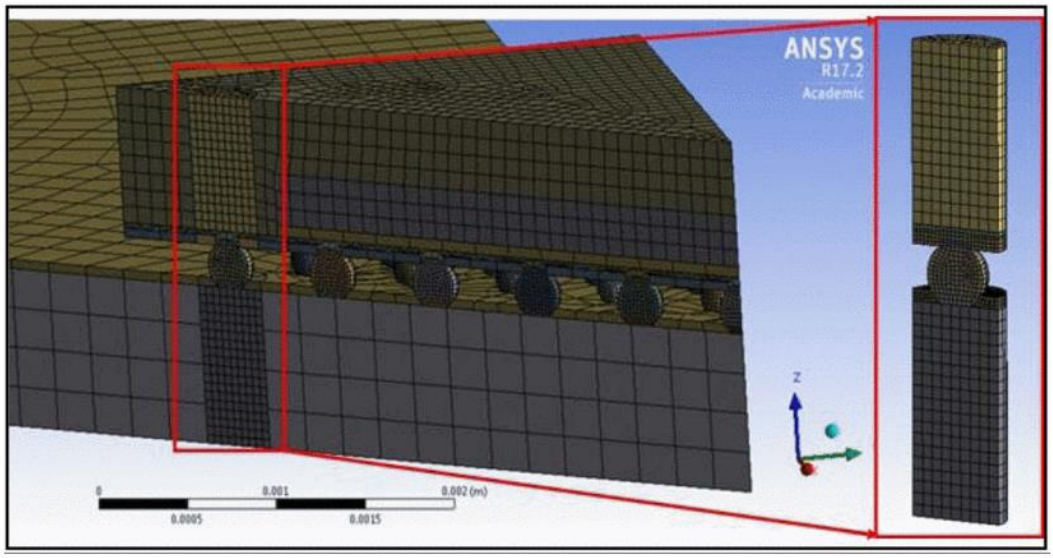


Figure 3-10 Global and sub model

Detailed stress-strain contours near the critical parts of the body sub modeling are done. In some cases, it may occur that the mesh is too coarse to provide the better results near the critical areas of the object where the stress is higher. Sub-modeling is also known as local global analysis or cut - boundary displacement method. The cut boundary is the method where the critical area is recognized or the part of the body where the stress is higher is determined and the part is sliced from the global model for further analysis. The boundary condition is imported from the global model for the analysis of the sub model. Here also, the sub-modeling technique was used for analysis. The detailed global model was created. A submodel from the global model is sliced as shown in figure 3-10. The impact of thermal load is highly active on the corner solder ball. The submodel was created as shown in figure 9 which includes half corner solder ball. Coarse mesh simulation is done for global model and cut boundary constraint is imported

to submodel where mesh sensitive analysis was done. The figure 3-11 shown below is the imported boundary condition on the connected surface [12].

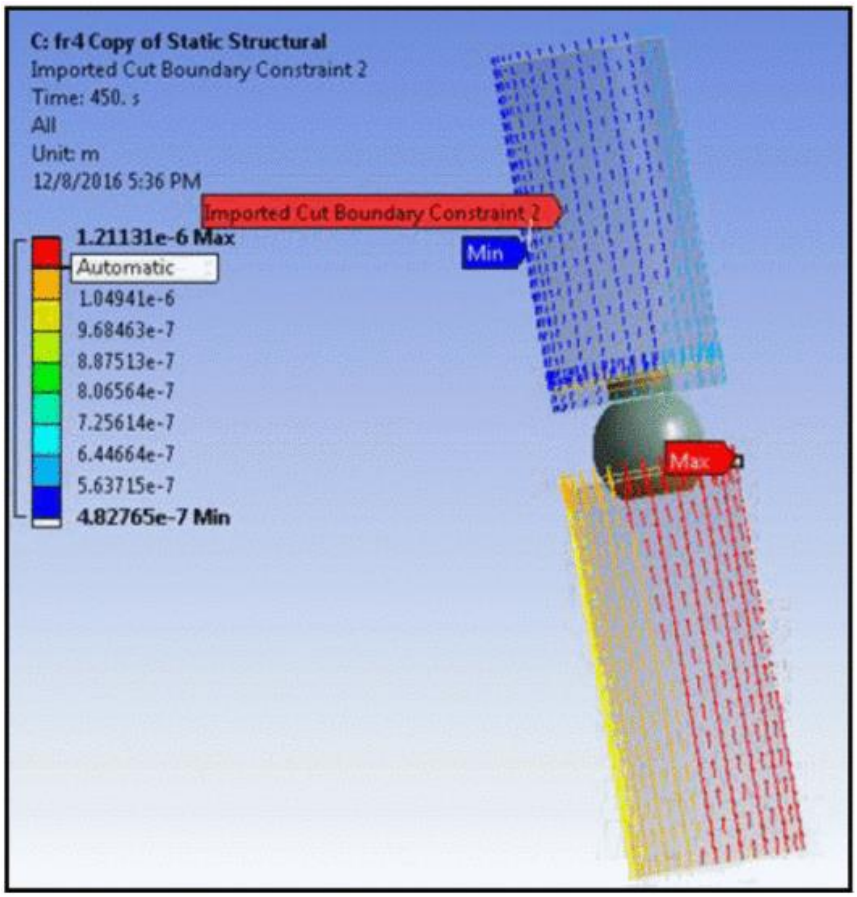


Figure 3-11 Cut boundary condition from global model

Thermal cycling loading was applied for −40°C to 125°C. A total of three cycles with a complete cycle of 60min, with 15min ramp and 15min dwell, were applied and the temperature profile is shown in Figure 3-12.

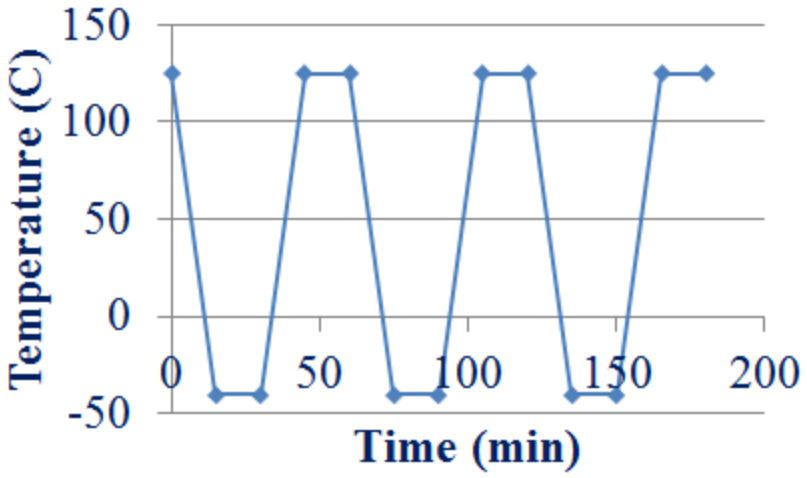


Figure 3-12 Thermal cycling

3.4 Results and Analysis

Lumped and layered model has been created on ANSYS 17.2 for computational analysis. Figure 9 shows the lumped model and figure 11 shows the layer by layer model referring PCB cross section measured under an optical microscope. Material properties for copper, RCC, FR4 and solder mask layer was defined separately and simulation is done keeping same meshing and one-part model for package component.

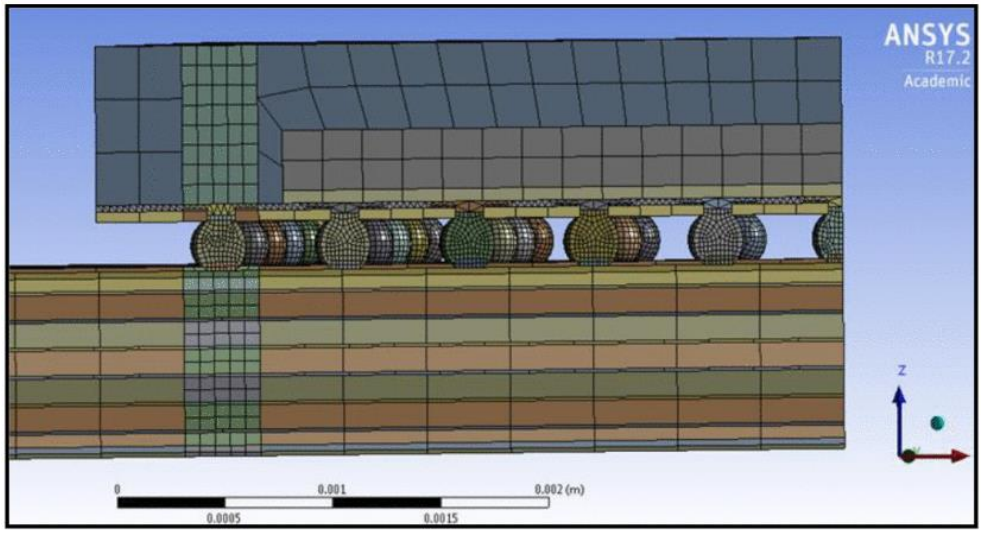


Figure 3-13 Layered Model

The equivalent stress distribution on the corner solder ball is shown in figure 3-14. It can be seen that the maximum stress developed on solder ball is maximized on the package side. In further analysis, life to failure has been compared between the top and a bottom portion.

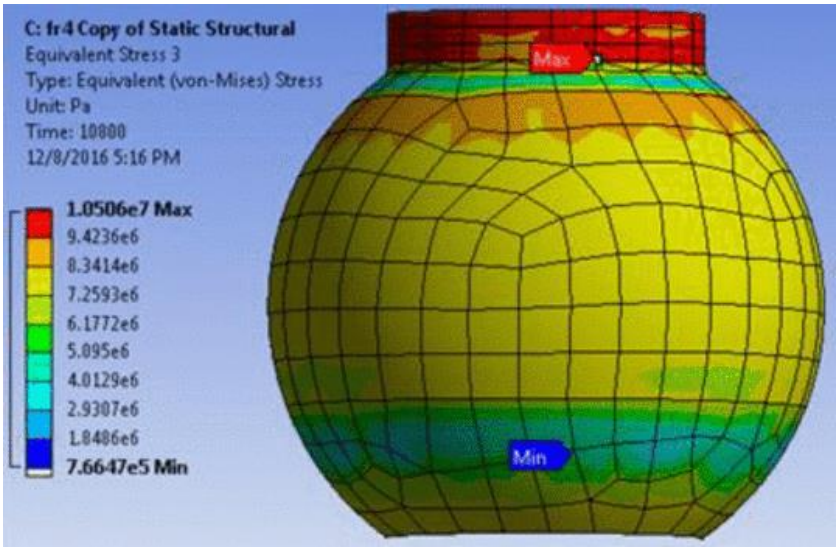


Figure 3-14 Equivalent stress on corner solder joint

Figure 3-15 is the comparison of Von Mises maximum equivalent stress developed on the corner solder ball for PCB board with RCC and FR4 prepreg. The chart also shows the comparison of lumped and layer by layer model. Layer by layer model is more defined due to consideration of PCB content, therefore it shows more stresses and accurate stress value. The developed stress is less in PCB with RCC prepreg and laminate. The same trend can be seen in the layered model also but the difference in the value is less.

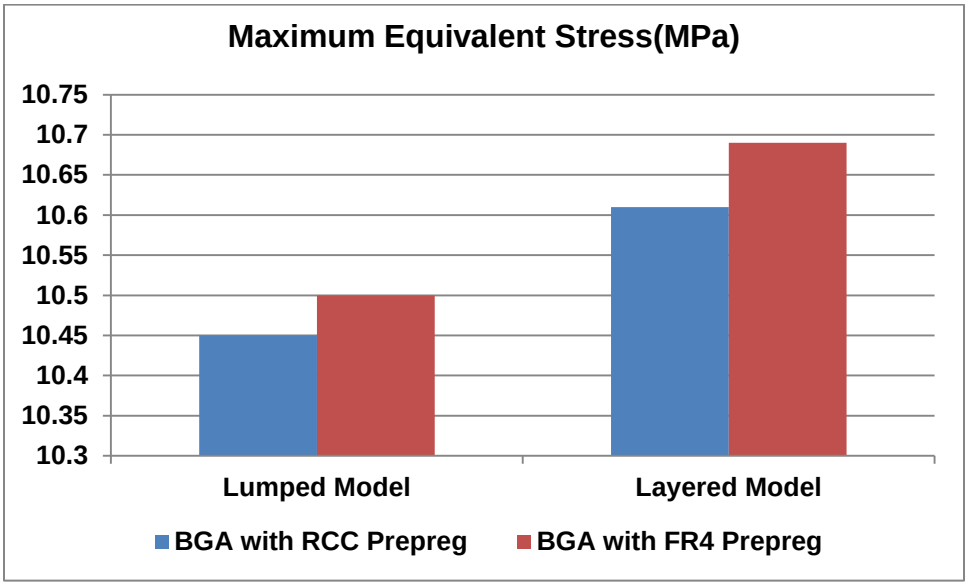


Figure 3-15 Max equivalent stress (MPa) comparison

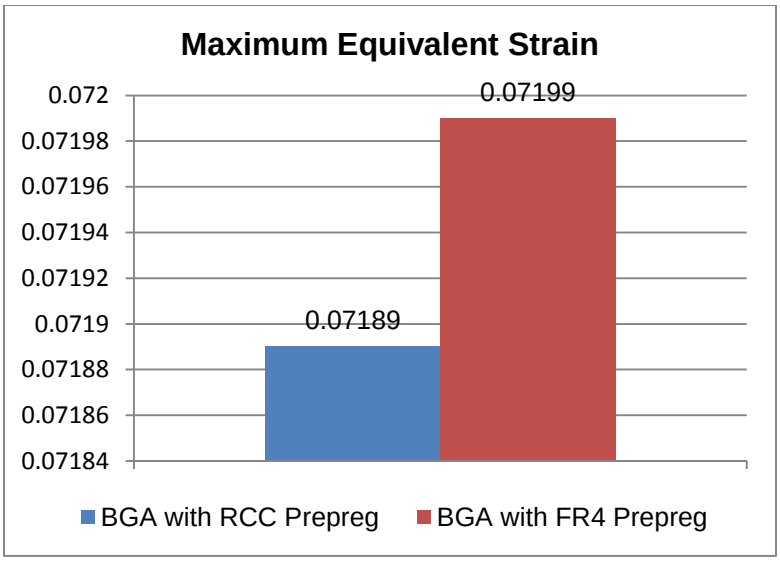


Figure 3-16 Max equivalent elastic strain comparison

Since solder demonstrates viscoplastic behavior, it was imperative to report the total equivalent strain in the corner solder to capture the effect of both elastic and plastic deformations. Figure 3-16 shows the maximum equivalent elastic strain comparison results for two boards. The board with FR4 prepreg show less strain compared to the board with RCC prepreg. The reason for the higher strain on the board with RCC prepreg is since it is less stiff than the board with the FR4 prepreg and consequently results in a higher strain.

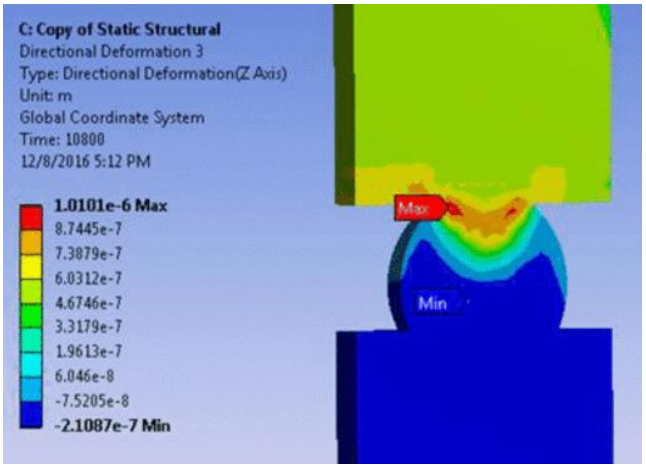


Figure 3-17 Directional deformation in z direction

The directional deformation along the z-axis is shown in figure 3-17. It is observed that the maximum deformation is at top of the corner solder ball. The lumped model is tested and maximum directional deformation is obtained. The values for RCC and FR4 prepreg board were compared. The board with FR4 prepreg shows less deformation in all direction compared to RCC prepreged board. Slit difference in deformation between x and y-direction is because temperature dependent CTE of the board in x and y are not identical.

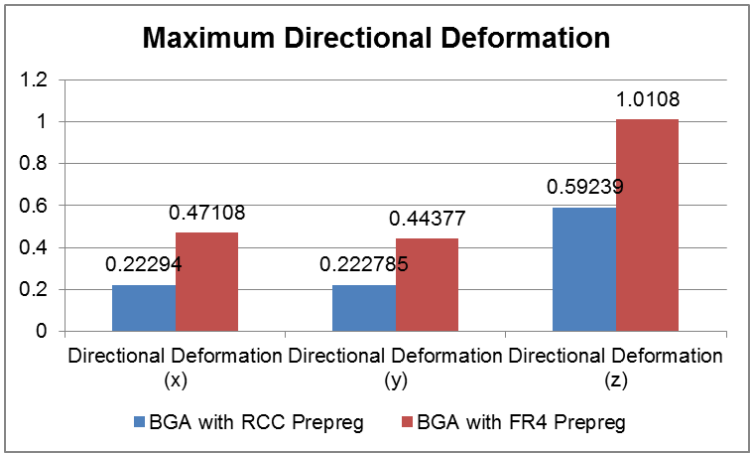


Figure 3-18 Maximum directional deformation (um) in all axis

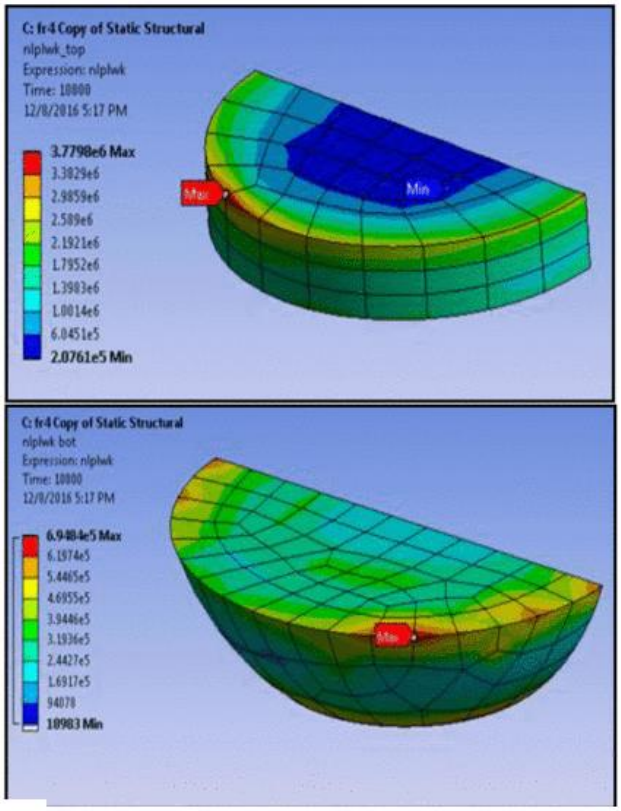


Figure 3-19 Non-linear plastic work distribution on (a) top portion of corner solder ball, (b) bottom portion of corner solder ball

Figure 3-19 shows two portions of corner solder ball. Fig 3-19(a) is the top portion which shows maximum stresses and Fig 3-19(b) is also considered for FEA, from experiments and literature review, it has been seen that even bottom portion has the possibility of crack propagation. So we have considered both top and the bottom portion of the corner solder ball to calculate average plastic work.

As seen from the results, the board with FR4 prepreg has less strain, but more Von Mises stress as compared to the board with RCC prepreg which has a higher strain and less Von Mises stress. Volume average change in Plastic work between cycle 2 and 3 was calculated for both the boards using Darveaux's APDL code [13]. The stiffness of

the board plays a significant role in reliability testing, the number of cycles to failure decreases as stiffness increases. [11]

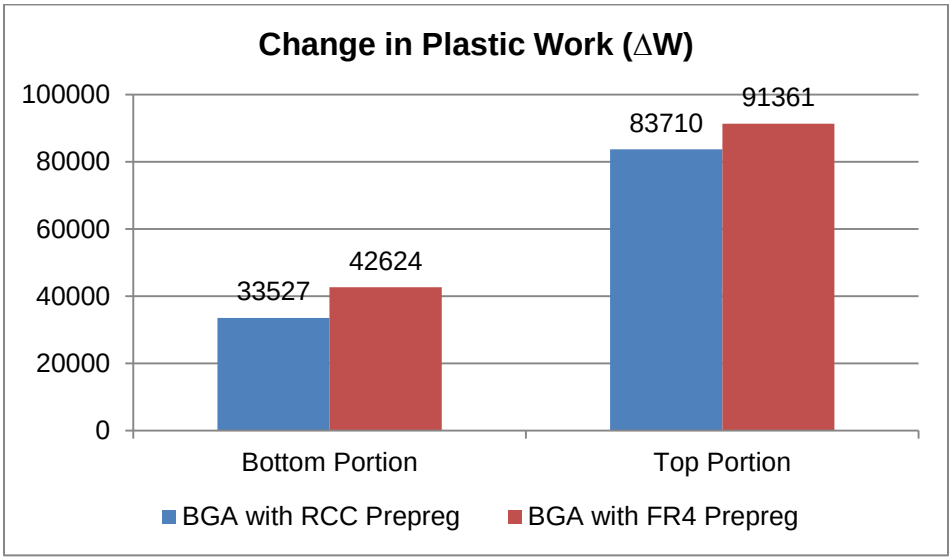


Figure 3-20 Change in plastic work (ΔW) for both boards

The fatigue indicator ΔW from the FEM analysis is used to calculate the number of cycles to failure using Schubert's model [14]. The ccorrelation is given below:

$$N_f = (A/\Delta W)^k$$

Where Nf= Predicted Life cycles to failure

The constant A and k varies with a package to package and can be calculated using experimental results. BGA PCB with FR4 prepreg shows more change in plastic work at the top and bottom portion compared to PCB with RCC prepreg. The top portion has less number of cycles to failure. As per Schubert's correlation, life to failure is inversely proportional to ΔW. Therefore, PCB with FR4 prepreg fails earlier.

3.5 Conclusion and optimization

Successful characterization of PCB to predict its reliability via FEA. UTM, DMA, and TMA were leveraged to find Young's Modulus and temperature dependent CTE. Directional deformation, Von Mises equivalent stress, and equivalent elastic strain are obtained from FEA and results were studied. From this work, it can be stated that after comparing the reliability of two available BGA boards, a board with RCC prepreg show better performance compared to a board with FR4 prepreg. The board with FR4 prepreg shows more Von Mises maximum equivalent stress and fails earlier. FR4 is still highly rated material used for PCB manufacturing because of its other benefits. RCC has high copper foil peel strength, high thermal resistance, and high glass transition temperature and highly demanded portable electronic equipment. FR4 has its special properties which are a high dielectric strength, high mechanical strength, light weight and high resistance to moisture. Depending on the demand and requirement both RCC and FR4 are used.

Chapter 4 Reliability of WCSP package

4.1 Wafer Scale Chip Package (WCSP)

WCSP is one of the most famous packages in the recent history of electronic packaging. WCSP refers to the technology of packaging an integrated circuit at the wafer level, instead of the traditional process of assembling individual units in packages after dicing them from a wafer. This process is an extension of the wafer Fab processes, where the device interconnects and protection are accomplished using the traditional fab processes and tools. In the final form, the device is a die with an array pattern of bumps or solder balls attached to an I/O pitch that is compatible with traditional circuit board assembly processes.

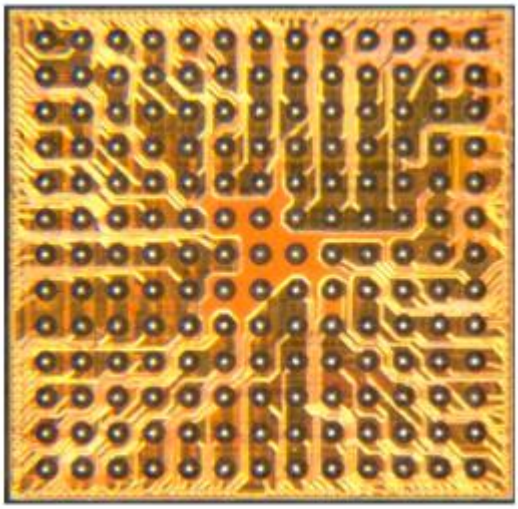


Figure 4-1 Wafer scale chip package

WCSP is a true chip-scale packaging (CSP) technology since the resulting package is of the same size of the die. WCSP technology differs from another ball-grid

array (BGA) and laminate-based CSPs in that no bond wires or interposer connections are required. The key advantages of the WCSP are the die to PCB inductance is minimized, reduced package size, and enhanced thermal conduction characteristics. The advance in semiconductor technology has created chips with transistor counts and functions that were unthinkable a few years ago. Portable electronics, as we know it today, would not be possible without equally exciting developments in IC packaging. Driven by the trend towards smaller, lighter, and thinner consumer products, smaller package types have been developed. WCSP has a smaller form factor which helps in more efficient use of limited space, greater flexibility in the placement of components in the assembly, reduced use of materials and ease of transport.

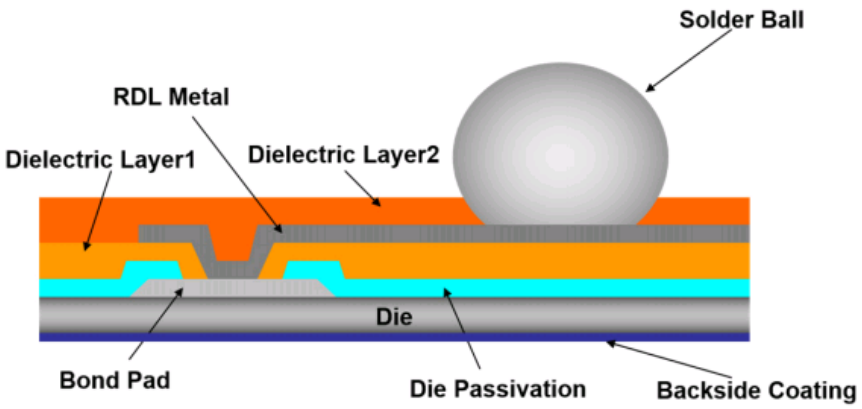


Figure 4-2 Cross-section of WCSP Package

4.2 Problem statement

Various studies have been conducted to study the effect of varying board thickness on thermo-mechanical reliability of BGA packages. Wafer level chip scale packages (WLCSP) have also been studied in this regard to determine the effect of PCB build-up thickness on the solder joint reliability. The studies clearly demonstrate that the

thinner Printed Circuit Boards (PCBs) result in longer thermo-mechanical fatigue life of solder joints for BGA. With the literature and past trends supporting the idea of thinner boards, manufacturer opted to move forward by decreasing the thickness of their PCBs to improve the reliability of their packages. The thickness was reduced from 1mm to 0.7mm by decreasing the thicknesses of individual layers and keeping the total number of layers constant. When subjected to thermal cycling, it was observed that 0.7mm board was failing earlier than the 1mm board. Since this behavior of a WLCSP contrasts with the past trends, it required extensive study to determine and understand the pre-mature physics of failure/causality of failure in 0.7mm board. In this paper, an effort is made to understand the mechanism which is causing an early failure in the thinner board. The effect of number & thicknesses of core layers, prepregs and Cu layers in the board has been studied through material characterization of both 1mm and 0.7mm boards. Further, a design optimization account has also been presented to improve the thermomechanical reliability of this package

In general, as the board thickness and overall stiffness decreases, the resulting stress, the solder joint experiences decreases. As much as a 2X increase in fatigue life can be realized by assembling CSPs on a thin board [15]. The primary reason for increase in solder life of a package mounted on a thinner board is basically the reduction in stiffness of the PCB caused due to reduction in its thickness. Based on this premise, thinner boards were used to mount CSPs for better solder joint reliability. Both 0.7 and 1 mm boards were subjected to thermal cycling tests from −40°C to 125°C and the results show that 0.7mm board failed in less no. of cycles as compared to the thicker board.

Three boards each of 0.7mm and 1 mm were subject to thermal cycling and then cross-sectioned into the solder balls of the failing daisy chains as confirmed by the curve trace analysis. The opens observed during curve trace analysis were caused by cracking

in the solder balls as a result of temperature cycle testing. The scanning electron microscopy (SEM) results for 0.7 and 1.0mm boards are shown in fig 4-3 and 4-4 respectively.

As it is seen from the figures below, the failure mechanism of both the boards is same i.e failure occurring at the interface of the solder and under metal bump (UMB), the cycles to failure of a 1 mm board are 3X the cycles to failure of a 0.7mm board. Since this behavior is in contrast to the industrial trends and basic mechanics which suggest that thinner boards are better for solder joint reliability, it was of considerable interest to study this behavior in a thin board [16].

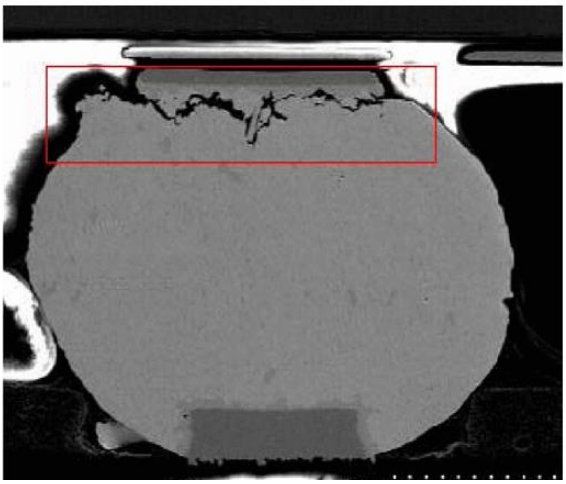


Figure 4-3 0.7mm Board Failure

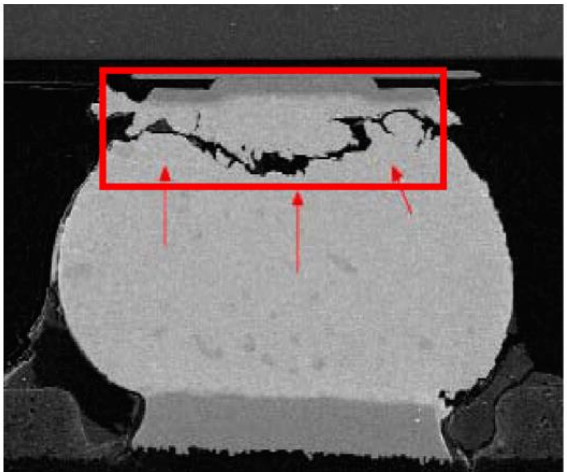


Figure 4-4 1mm Board Failure

To study the effect of number & thicknesses of cores, prepreg and Cu layers, both the boards were characterized to determine their material properties. The boards were cross-sectioned and their layout/layup was studied for of Cu and Prepreg stack details. Tensile testing of PCBs was conducted on the two boards using Instron tester to determine the Young's modulus. Coefficient of Thermal Expansion (CTE) was calculated using a Digital Image Correlation (DIC) technique which is a non-contact technique to measure in-plane and out of plane deformation. The experimental results were used as material properties of the model to predict the solder joint reliability. The warpage of the FEA model was validated against the experimental warpage of the package when subjected under thermal loading from 25°C to 125°C.

4.3 Material characterization

To come up with an effective FEA model which is a good approximation of the actual testing condition, it is imperative to have the right material properties. To determine

these properties, samples were taken from both boards and different tests were performed to determine their material properties. The tests performed are as follows:

4.3.1 Instron tensile test

Dog-bone samples were prepared as per ASTM standards for the tensile test. An aluminum sample is shown in fig. 3 and the standard dimension of the sample are given in table 1 below.

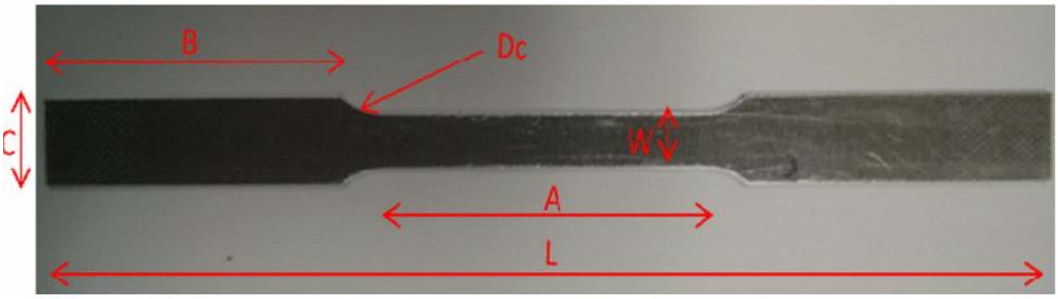


Figure 4-5 Dog Bone Sample

Dimensions	Value (mm)
L-length	100
C- Width of grip	10
W- Width	6
A- Length of reduced section	32
B- Length of Grip Section	30
R-Radius of curvature	6
Dc-Curvature Distance	4

Table 4-1 Dog-Bone Sample Dimensions

4.3.2 Experimental Set up

To measure the Young's modulus of PCB samples, Instron Micro Tester 5848 with a maximum load cell of 2KN was used to apply force. The grip section of dog-bone sample is clamped vertically between the two jaw faces of the Instron tester and an extensometer is placed on the samples with its pins gripping the sample tightly. The extensometer pins have an initial gap of 12mm between them. When tensile force is applied on the specimen, the extensometer pins which are tightly gripping the specimen open accordingly and the change in length is measured from where strain is calculated using Bluehill software.

The test setup and procedure as shown in fig. 4 was benchmarked by testing an aluminum sample and calculating the Young's Modulus. The experimental result was compared with the theoretical result and was found to be in complete agreement with the theoretical value. The Young's modulus values as measured by the Instron tester for 0.7 and 1 mm boards are shown in fig 5 and 6respectively.

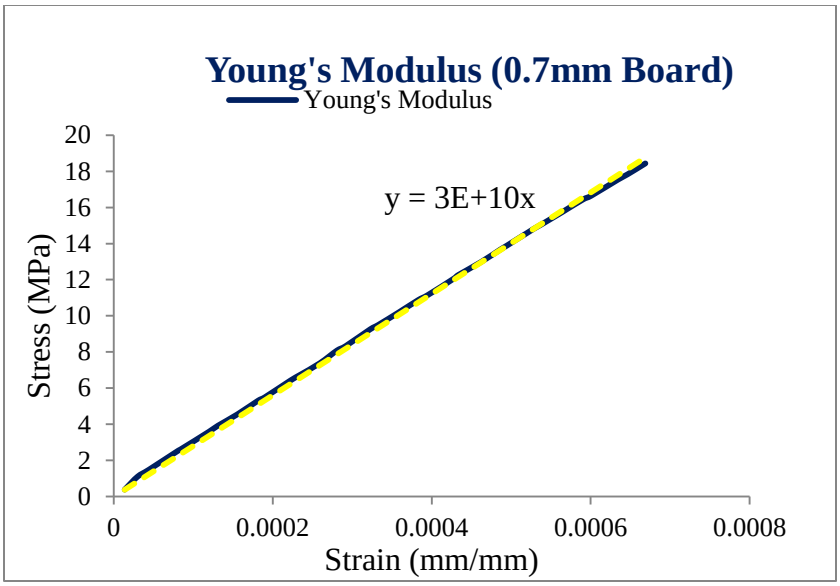


Figure 4-6 0.7mm Board Modulus

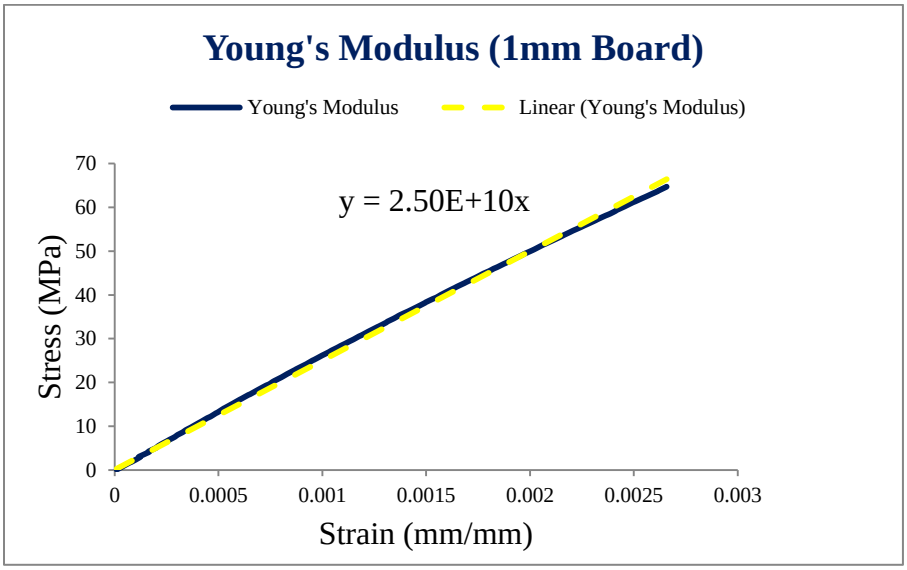


Figure 4-7 1mm board Modulus

4.3.3 DIC correlation with Oven

A digital image correlation technique was leveraged with a thermal cycling oven to determine the in plane and out of plane CTE of the packages. Samples were cut from

PCB and painted using spray paint. White paint was applied first to provide a good background followed by a spray of black paint. The DIC cameras trace movement of these black dots (speckles) on the samples and measure strain. CTE is calculated by dividing the strain by the change in temperature. The readings are taken at different temperatures i.e room temp, 50°C, 75°C, 100°C and 125°C. Each temperature reading gives a point for a temp Vs strain curve which gives CTE of the sample. The sample is then put in the oven and baked for 4~6 hours to remove moisture from the sample. The final prepared sample with black speckles is shown in fig 4-8 below:

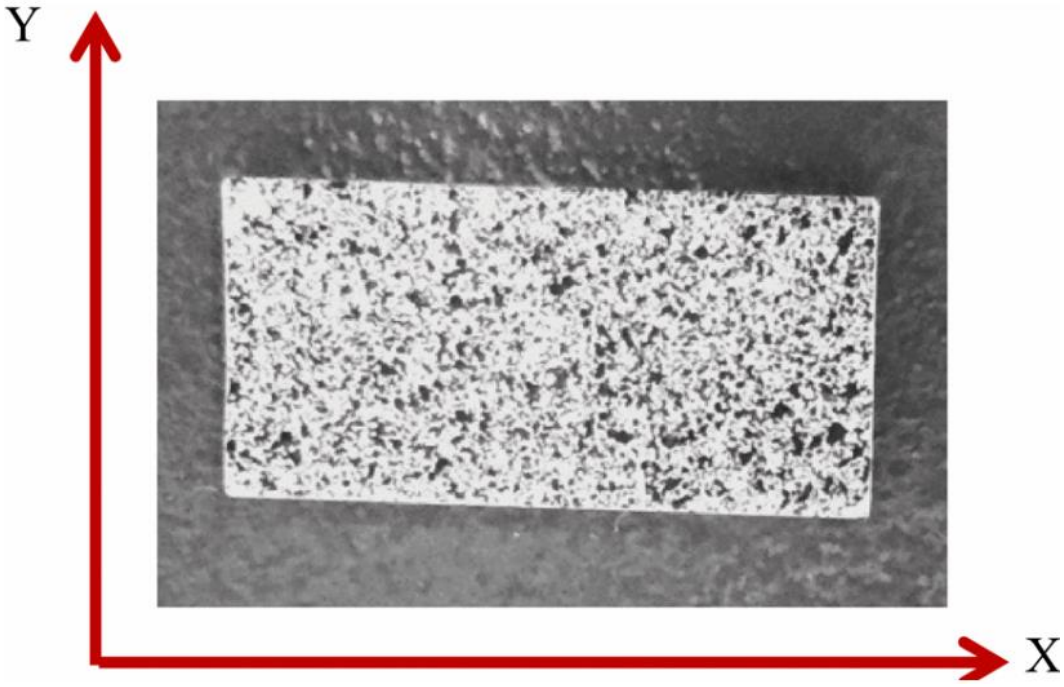


Figure 4-8 CTE Test Specked Sample

4.3.4 Experimental set up

To ensure that the whole sample is at the same temperature and there is no temperature difference along the thickness or along the surface of the sample, a dummy sample of same board and size was placed next to the test sample. Thermocouples were

attached to the dummy sample to monitor temperature of the sample at different locations. Since the thermocouples are attached to the sample using thermal tape, there is a possibility that the tape might restraint the sample from free expansion during heating. This is why a JEDEC standard was followed and thermocouples were attached to the dummy sample and not the test sample. The test setup inside the oven is shown in the fig 8 below:

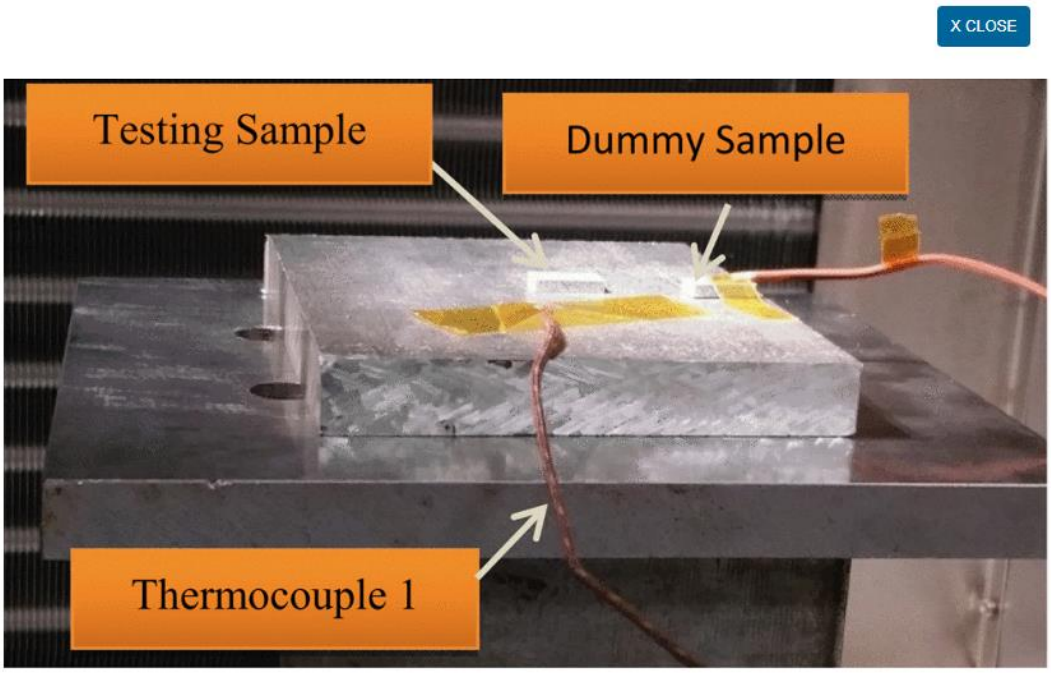


Figure 4-9 CTE set up

The other end of thermocouples was attached to a 20 channel Data Acquisition System (DAQ) which is connected to a computer which gives time vs temperature plot at any instant. 5MP cameras were used with a Digital Image Correlation (DIC) technique to monitor strain in the sample as it was heated from 25°C to 125°C. Images were captured at every 25°C change in temperature using VicSnap software connected with the cameras. The cameras see the sample through a boro silicate glass window at the top of

the oven. The boro silicate glass prevents any reflection of light into the cameras as the sample is kept illuminated at all times using a 15kW illumination beam focused on the sample. The DIC setup is shown in fig 4-10 below:

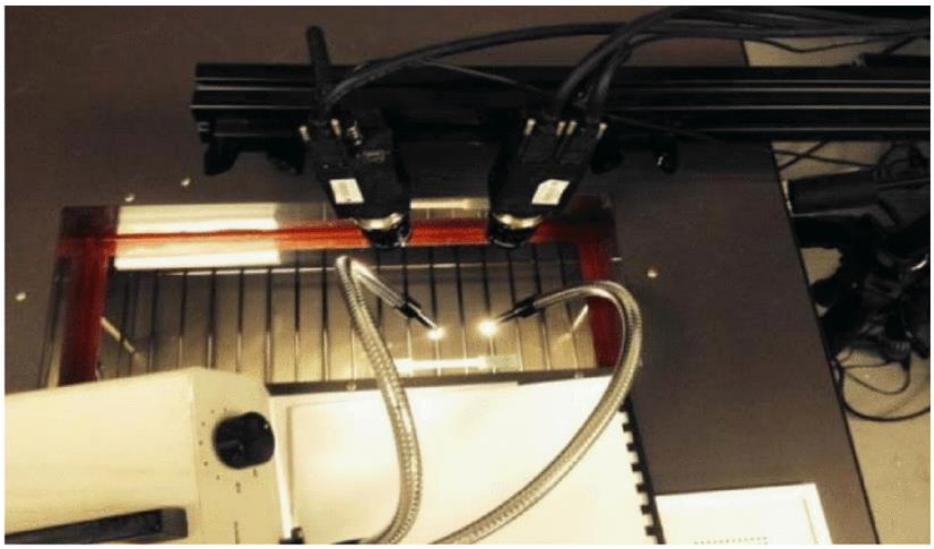


Figure 4-10 DIC set up

The Coefficient of thermal expansion (CTE) as measure with the DIC for 0.7mm and 1mm boards is given below in fig. 4-11 and 4-12.

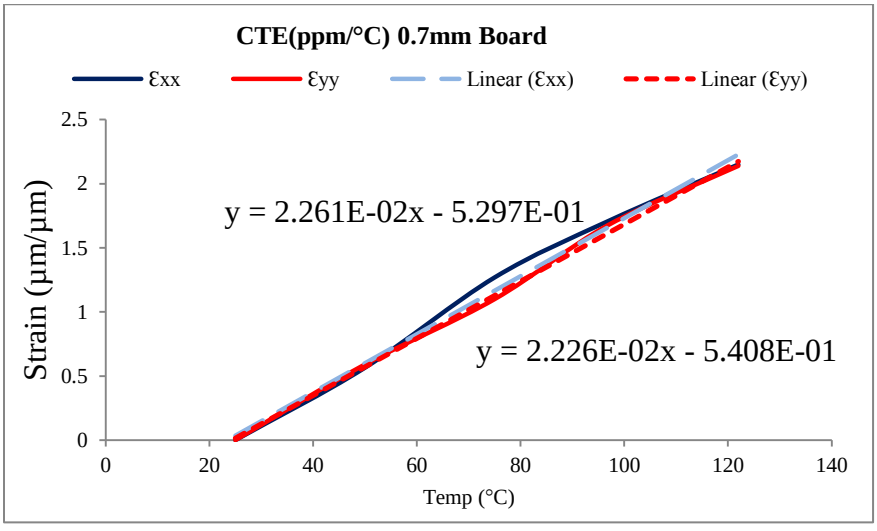


Figure 4-11 CTE 0.7mm board

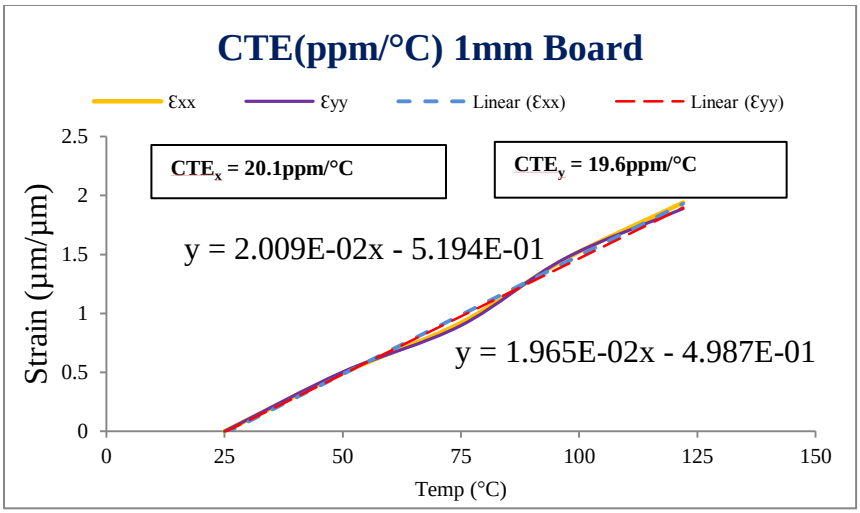


Figure 4-12 CTE 1mm board

4.3.5 PCB details

Since 0.7mm board was found to be stiffer than 1mm, it was worth looking deeper into the PCB layer-by-layer stack to find the reason behind the stiffness.

A cross-sectioning methodology was leveraged for this purpose where both the boards were cross-sectioned using a mechanical rotary cutter and small samples of 8x4mm were prepared. These samples were kept under an optical microscope to have a close look at the layers along the board thickness. The cross-section images from the optical microscope for 0.7 and 1mm boards are shown in fig. 4-13 and 4-14 respectively.

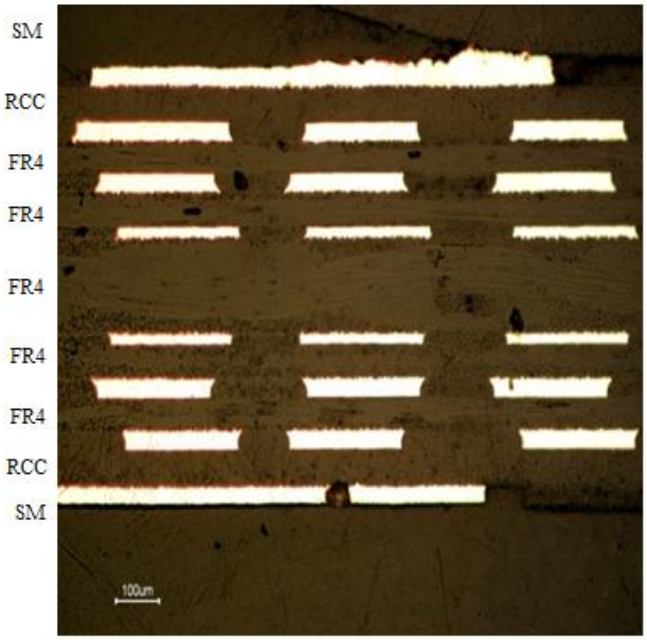


Figure 4-13 Cross-section of 0.7mm board

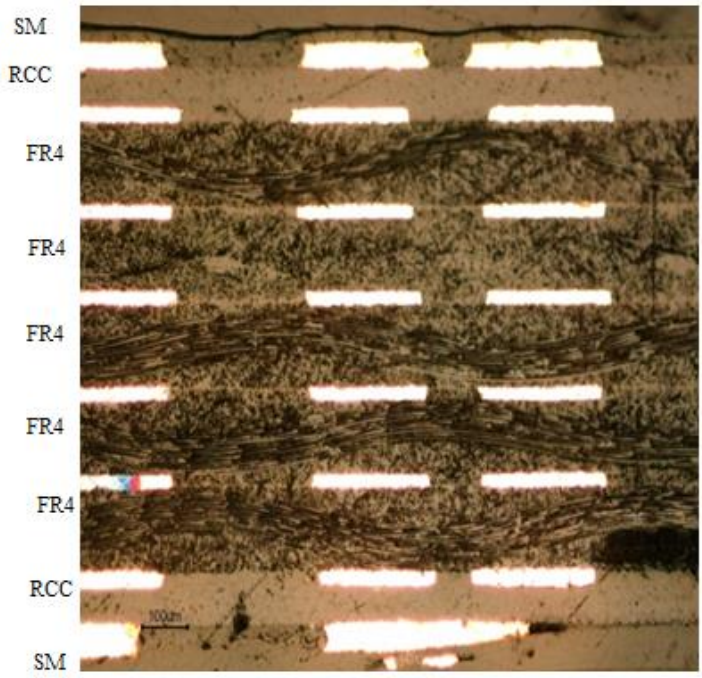


Figure 4-14 Cross-section of 1.0 mm board

Overall Cu thickness in 0.7 and 1 mm boards is 184um and 162um respectively.

4.3.6 Layer Removal

Layer was removed using milling process on 0.7 mm thick board and effect of some of the layer removal was investigated. In the first step only solder mask was removed, which reduced the stiffness of the board significantly as shown below to 21.9 GPa.

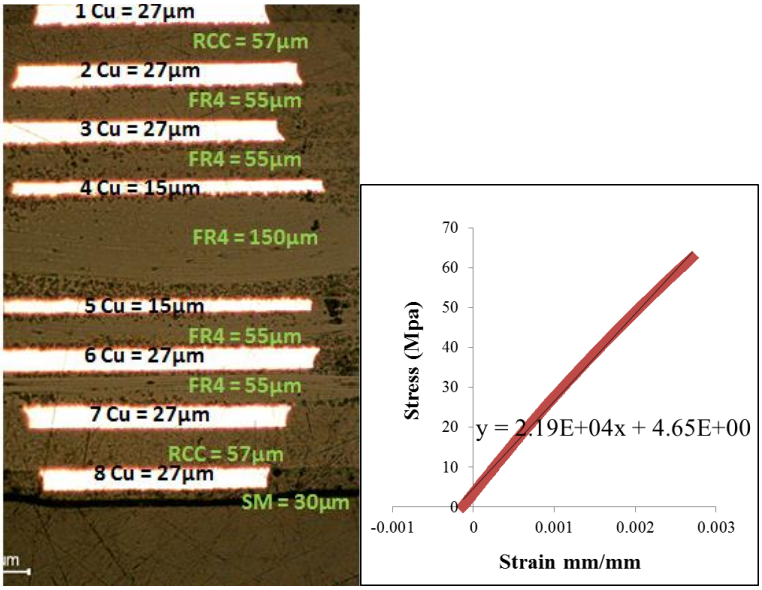


Figure 4-15 Solder mask removed -0.7mm board

On 1 mm thick board, layer 1 was removed. Removing Cu changed the thickness of the board to be 0.94 mm. The percentage of Cu decreased to 25% of the total volue and the percentage of prepreg became 75%. The change in Young's modulus was evident as the board became less stiff with a value of 24. The next layer to remove was RCC layer of thickness 0.05mm. The percentage copper went to 27%and FR4 had a percentage of 73 resulting in higher modulus of 24.8GPa.

Table 4-2 Summary of layer removal on 1 mm board

Package	Board Thickness (mm)	Board Layers	Exx(Gpa)
WCSP	1	2SM +8Cu+5FR4+ 2RCC	25
WCSP	0.94	7Cu+5FR4+ 2RCC	24
WCSP	0.89	7Cu+5FR4+ 1RCC	24.8

4.4 Finite Element Model

Commercially available ANSYS workbench [17] was used to model both the packages. Both the boards were cross-sectioned and viewed in a digital microscope using a 20 X lens to get the detailed layup of the board and the package.

Although the cross-section revealed details of every layer in the PCB as well as 1st level, the PCB was modeled as a block to reduce computational time and use bulk material properties as determined by experiments.

However, the RDL and Polyimide layers were modeled individually and the material properties were assigned from the literature. Quarter symmetry of the full model was used for faster computation. Fully meshed model with all the layers is shown in fig 4-16 below.

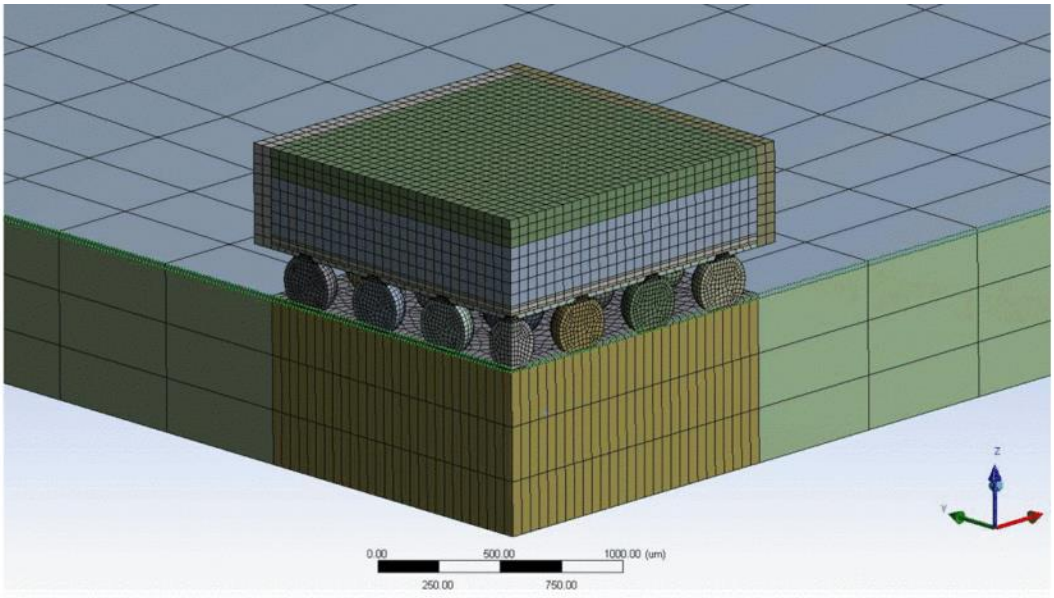


Figure 4-16 Meshed quarter model

The dimensions used for the models are given below. The only difference between the two models was the thickness of the PCB (0.7mm & 1mm), the rest is same for both the models.

Table 4-3 Package dimensions

Parameter	Dimensions(mm)
PCB(1mm/0.7mm)	24x24x1/0.7
Solder Array	7x7
Solder Dia	0.25
Solder Pitch	0.40
Die	2.8x2.8x0.25
RDL	2.8x2.8x0.02
Polyimide	2.8x2.8x0.01
Mold	3x3x0.43

4.4.1 Material Properties

All materials except SAC396 and PCB were modeled linear elastic. PCB was modeled linear orthotropic and SAC alloy was modeled viscoelastic using Anand's viscoplastic model for SAC396 [8].

The material properties used for different materials are given in table 4 below-

Table 4-4 Material Properties

Material	Property				
	E (GPa)	CTE (ppm/°C)	v		
			xy	yz	xz
PCB (0.7mm)	30	23	0.11	0.39	0.39
PCB (1mm)	25	20	0.11	0.39	0.39
Die	131	3	0.28		
RDL	130	16.8	0.34		
Polyimide	1.2	52	0.25		
Mold	24	20	0.3		
Cu	110	17	0.34		
Solder Mask	4	30	0.4		

The elastic part of the constitutive law of lead-free solder 396 can be described by a temperature-dependent Young's modulus and Poisson's ratio (v=0.40). The temperature-dependent Young's modulus is $E=100501-194T$ (MPa) in which the absolute temperature T is in Kelvin. The coefficient of thermal expansion of the solder is taken to be 23.5 ppm/K.

Anand's viscoplasticity for solder can be described as follows. There are nine material constants in Anand's viscoplasticity law which are given in table 4-5 [8]below for SAC396:

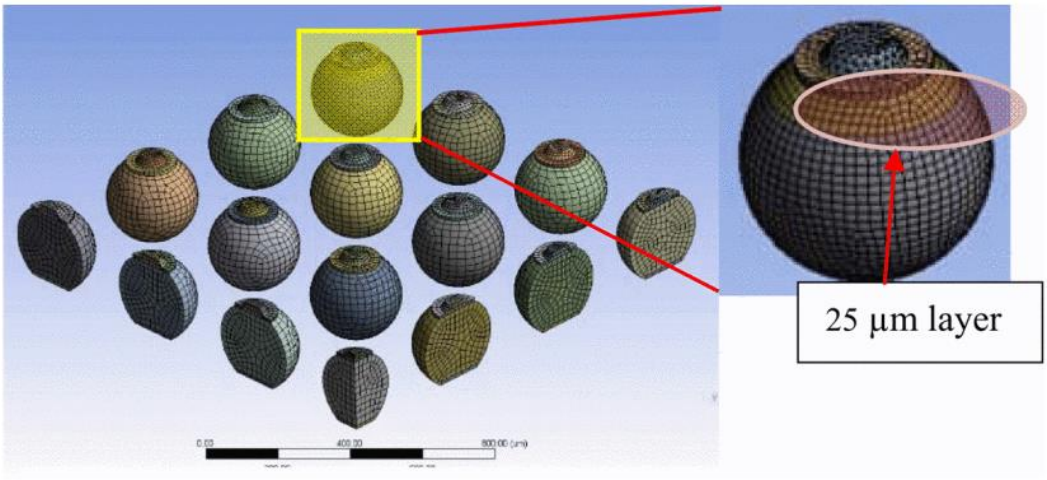


Figure 4-17 Corner solder ball and 25µm layer

Table 4-5 Anand's constant for SAC396

S. No	Constant	Unit	Value
1	s_0	MPa	3.3
2	Q/R	1/K	9883
3	A	sec^{-1}	15.7E+06
4	ξ	Dimensionless	1.06
5	m	Dimensionless	0.3686
6	h_0	MPa	1077
7	$\hat{s}$	MPa	3.15
8	n	Dimensionless	0.0352
9	a	Dimensionless	1.6832

To determine the life cycles to failure of both the boards, a 25umlayer starting at the interface of the solder and the Under Bump Metal (UBM) was sliced inside the solder ball as shown in fig 15above. The volume averaged plastic work was calculated at this sliced portion of the solder by writing an APDL script for calculating the plastic work. The calculated plastic work is then related to life cycles to failure using work based models.

4.4.2 Loading and BCs

when subjected to thermal cycling, therefore to replicate the original loading conditions thermal cycling loading was applied from −40°C to 125°C. A total of three cycles with a complete cycle of 60min with 15min ramp and 15mil dwell were applied as shown in fig 16 below.

The stress-free temperature of all bodies is 125°C, symmetric boundary conditions were applied to the two symmetric faces and the center node of the full model was fixed i.e all degree of freedom (DOF) were zero at the center node as shown below in fig 4-15.

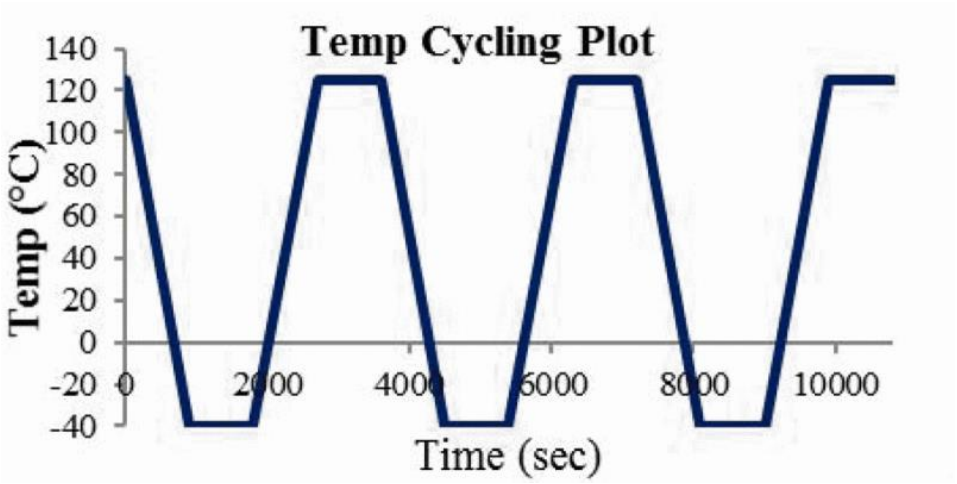


Figure 4-18 Temp cycling plot

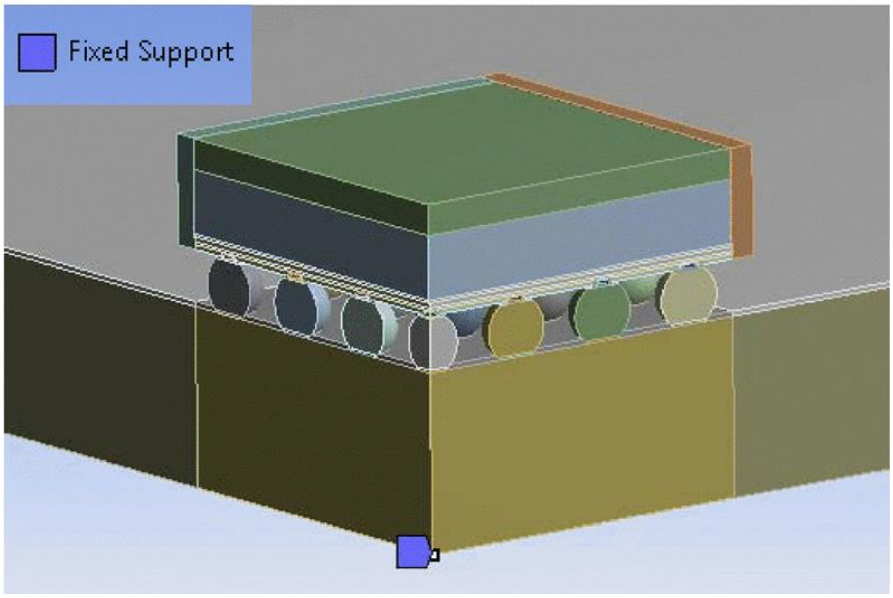


Figure 4-19 Symmetry faces & fixed node

4.5 Results and analysis

Total inelastic strain and von-mises stress in the critical (corner) solder ball were used as correlation parameters to predict relate life cycles to failure. The total strain and equivalent von-mises stress in the critical ball as determined from the ANSYS model are shown below in fig 4-20 & 4-1.

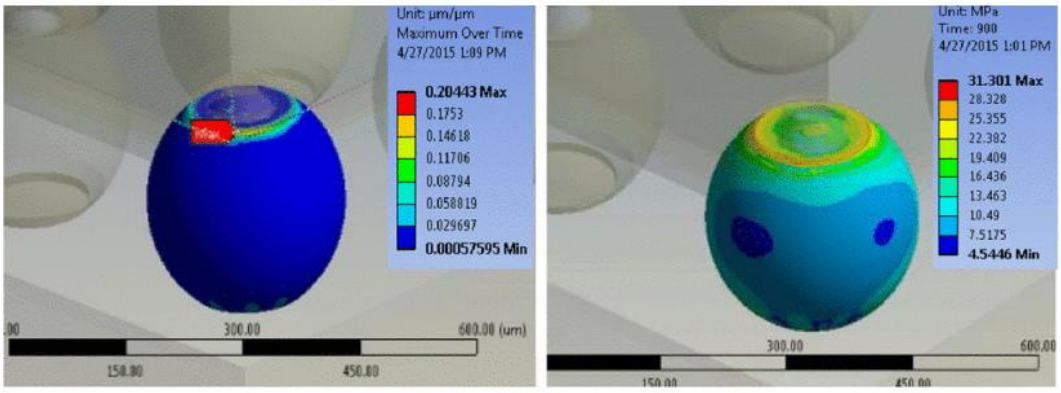


Figure 4-20 Strain & stress plots for l mm thick board

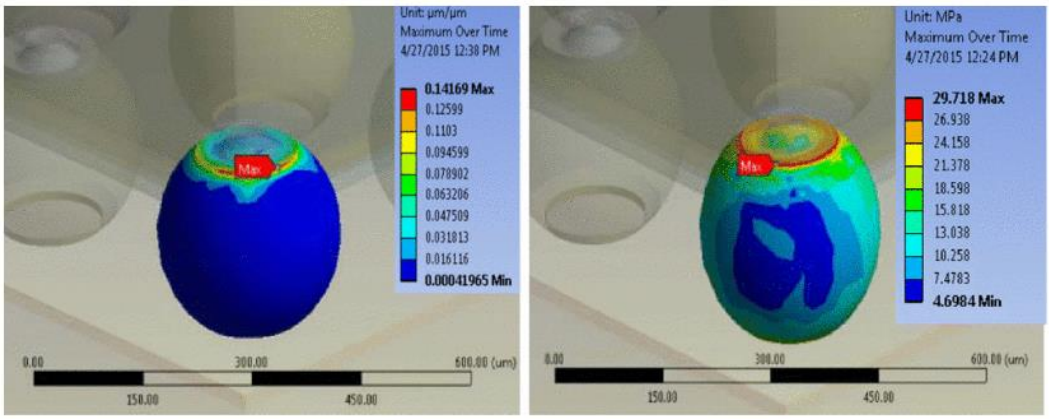


Figure 4-21 Strain & stress plots for 0.7mm thick board

Volume averaged plastic work was calculated by writing an APDL script in the ANSYS commands using the stress and strain values from the FEA model. The plastic work as for both the boards is given in table 4-5 below.

Table 4-6 Plastic work

Board Thickness(mm)	Plastic Work (MPa)
0.7	0.497
1	0.282

This volume averaged plastic work was related life cycles to failure using Schubert et al. [14] and Che & Pang [18] correlation:

$$N_f = \left(\frac{A}{\Delta W}\right)^k$$

where Nf is the characteristic life. A (in MPa) and k (unitless) are two empirical fatigue parameters that were used from Jie *et al*. work on chip scale packages [8]. The values of A and k used were A=8.783x106(MPa),k=0.4701.

The calculated life cycles to failure (Nf) as calculated from the above relation are given in table 4-7 below

Table 4-7 Life cycles to failure

Board Thickness(mm)	Cycles to Failure
0.7	2552
1	3330

As seen from the results above, the life cycles to failure in a 1mm board are 30% more than 0.7mm. The results from the FEA model are complementing the results obtained by experiments.

As shown from the results, 0.7mm board is experiencing a higher value of total strain and von-mises stress. This eventually accounts for lower life cycles to failure as compared to the 1mm board. Since these results are in line with the experimental data where 0.7mm board is failing earlier than the 1 mm counterpart, it needed some further investigation to find the reason behind this behavior.

Based on the results of cross-sectional study of both the boards, the total volume of Cu and FR4 was determined for both the boards. The purpose of this study was to determine the Cu content in both the boards, which contributes to the stiffness of the board.

Table 4-8 Copper & FR4 content in the boards

	0.7 mm	1mm
Total Cu (µm)	184	162
Volume of board (mm^3)	403.2	576
Cu/Vol of the board(µm/mm^3)	0.456	0.2815

4.6 Conclusion and Optimization

As shown from the table above there is 38.3% more Cu/mm^3 in 0.7mm board as compared to the 1mm board. Now, since Cu contributes to the stiffness and FR4 contributes to the compliance of the board, 0.7mm board is much stiffer as compared to the 1mm counterpart. The high volume of Cu in 0.7mm board is playing a significant role in its early failure as it is making the board stiffer and eventually generating more stresses in the critical solder ball. This indicates that reducing Copper layer would improve reliability of thinner boards. Reducing copper might create negative impact on electrical reliability and thermal performance.

Chapter 5

CONCLUSION

5.1 Summary and Conclusion

In this work, three problems were selected which were showing unconventional failure and the main goal was to understand the physics of failure.

For the first problem on QFN reliability on thick boards -Material characterization of PCB was performed using Instron micro-tester and Digital Image Correlation technique in the second section. All the measurement tests were first benchmarked with Al sample and results were found to be in close agreement. The in-plane Young's modulus and Poisson's ratio was found to be 30 GPa and 0.4, while in-plane and out-of-plane co-efficient of thermal expansion were 21 ppm/°C and 72.4 ppm/°C. A FEM model was generated and a parametric design analysis was performed on QFN package to understand the effect of each parameter on reliability of the package. . It was concluded that for better reliability it is recommended to have smaller die size and die thickness, larger solder stand-off height and longer solder fillet length, adding corner anchor and corner underfill. Overall combination of thinner package with thinner die with corner anchor and corner underfill helped improve the reliability to pass IPC requirements.

For the second problem on BGA package, the packages were mounted on similar board thickness and one package was failing earlier than the other. Again, characterization of PCB performed using UTM, DMA, and TMA to find Young's Modulus and temperature dependent CTE. Directional deformation, Von Mises equivalent stress, and equivalent elastic strain are obtained from FEA and results were studied. From this work, it can be stated that after comparing the reliability of two available BGA boards, a board with RCC prepreg show better performance compared to a board with FR4 prepreg. The board with FR4 prepreg shows more Von Mises maximum equivalent stress

and fails earlier. FR4 is still highly rated material used for PCB manufacturing because of its other benefits. RCC has high copper foil peel strength, high thermal resistance, and high glass transition temperature and highly demanded portable electronic equipment. FR4 has its special properties which are a high dielectric strength, high mechanical strength, light weight and high resistance to moisture. Depending on the demand and requirement both RCC and FR4 are used.

For the third problem of WCSP board on 0.7 mm and 1mm board, the packages were failing earlier on thinner board as compared to thicker board. The boards were cross-sectioned, which showed that there is 38.3% more Cu/mm^3 in 0.7mm board as compared to the 1mm board. Now, since Cu contributes to the stiffness and FR4 contributes to the compliance of the board, 0.7mm board is much stiffer as compared to the 1mm counterpart. The high volume of Cu in 0.7mm board is playing a significant role in its early failure as it is making the board stiffer and eventually generating more stresses in the critical solder ball. This indicates that reducing Copper layer would improve reliability of thinner boards. Reducing copper might create negative impact on electrical reliability and thermal performance.

Layer removal comparison was performed for all three problems which provided insight on how varying thickness of boards and different layer stack-ups might affect CTE and E and ultimately behavior of the boards under thermal loading conditions.

5.2 Future Work

The characterization and modeling work performed for all three problems could be used to further understand the failure mechanism in modular way. Because of applications needing more functionality, the boards will be thinner and thicker than what has been discussed in this study. To push the boundaries further, more study is needed to understand the details material behavior of PCBs on layer by layer using other techniques like nano-indentation over complete reflow temperature range. These data generated needs to be captured in the FEM model as material model to predict the reliability with more accuracy and prevent failures.

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BIOGRAPHICAL INFORMATION

Alok Lohia received his bachelor degree from Indian Institute of Technology Bombay in 2002 and Masters from SUNY Buffalo, NY 2003. He worked at IBM TJ Watson research center before joining TI in 2005 as semiconductor packaging engineer. He has 14 years of industrial experience in design, thermal and reliability of electronic packages and modules. He was industry Liaison from TI to support funding from SRC with Prof. Agonafer to understand the failure mechanisms of various packages on custom PCB board. He is currently senior mechanical engineer at ABB designing power electronics products. His research interest includes reliability, fracture mechanics, thermo-mechanical simulation and material characterization for electronic packages and modules.