ACCELERATED AGING OF A SWITCHING POWER SUPPLY PROTOTYPE

by

MICHAEL JAMES HIBBARD

Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

DECEMBER 2018

ACKNOWLEDGEMENTS

I would like to thank my parents, David and Karen Hibbard for their never ending encouragement and support through my long tenure as a student at UTA, without which I'm not sure I would have ever finished.

I want to thank my advisor Dr. Ali Davoudi for advocating on my behalf and providing me a path forward into the Electrical Engineering graduate department. I am very grateful of the continued support, advise and availability he always provided me.

I want to thank Dr. Haleh Hadavand for supporting and exposing me to the world of CERN and high energy physics. I am also grateful for the guidance from, and experience obtained while working with Dr. Seyedali Moayedi.

I also thank Dr. Bob Woods for providing me an outlet of inspiration and creativity in engineering while I was an undergraduate, and for encouraging me to peruse graduate school. I also want to thank my colleague Randy Long with whom I worked with on the FSAE all-electric car. Observing Randy pursue his M.S. in Electrical Engineering as a Civil Engineering graduate motivated me to do the same. I also want to thank all my friends from the Formula SAE race team for the companionship during my entire duration at UTA.

Lastly I want to thank my entire master's committee: Dr. Davoudi, Dr. Hadavand, Dr. Kenarangui and Dr. Madani and the entire administrative staff of the department of Electrical Engineering, especially Gail Paniuski.

November 30th, 2018

ABSTRACT

ACCELERATED AGING OF A SWITCHING POWER SUPPLY PROTOTYPE

MICHAEL JAMES HIBBARD, MSc

The University of Texas at Arlington, 2018

Supervising Professor: Dr. Ali Davoudi

The LVPS (Low Voltage Power Supply) is a switching power supply custom designed for the ATLAS Tile Calorimeter at the Large Hadron Collider in Geneva Switzerland. Over one thousand of these LVPS, also called 'bricks', will be produced for an upgrade cycle of all the detector electronics of the experiment. The responsibility of the technical design and manufacturing of these LVPS bricks has been supported by Dr. Hadavand's ATLAS group at UT Arlington. As part of supporting the manufacturing process, a test station has been designed and prototyped to accelerate the aging of these brick past their infancy period. The accelerated aging of these bricks is also referred to as a "burn-in" process.

In the accelerated aging, or burn-in station, a LVPS brick is subjected to a stressed environment where the load and temperature are both elevated. Different thermal systems were considered during the design, including utilizing the Peltier-Seebeck effect for the station. Previous legacy burn-in type stations utilized a water cooling circuit to maintain the temperature of the bricks and to sink power from the output load of the bricks. The new design has eliminated this water circuit and instead utilizes a forced convection-cooled electronic load. Each individual brick also

sits on top of its own heat sink, which is also force convection-cooled to regulate the temperature of each individual brick.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1

REVIEW AND ANALYSIS OF LVPS BRICKS

1.1 LVPS Application Environment

The LVPS bricks are apart of the electronics for the Tile Calorimeter of the ATLAS experiment of the LHC. The Tile Calorimeter, TileCal, samples the energy of hadrons as they interact with 500,000 scintillator tiles within the system. These tiles are composed of steel plates and plastic scintillators. TileCal consists of 4 barrel sections along the beam length, each comprising of 64 wedge-like segments. LVPS is positioned within each wedge segment of TileCal, inside of an electronics drawer to power all of the front-end detector electronics, which are also housed within the same drawer (Fig.1.1).

The Phase II upgrade of the LHC will raise the instantaneous luminosity by at least a factor of five. Due to the aging of the current electronics in the detectors and increased expected radiation from higher luminosity, all electronics of the TileCal will be upgraded. Improved prototypes of all the front-end detector electronics have been designed, manufactured and tested for the Phase II upgrade [1]. The new design of the LVPS is apart of this upgrade cycle.

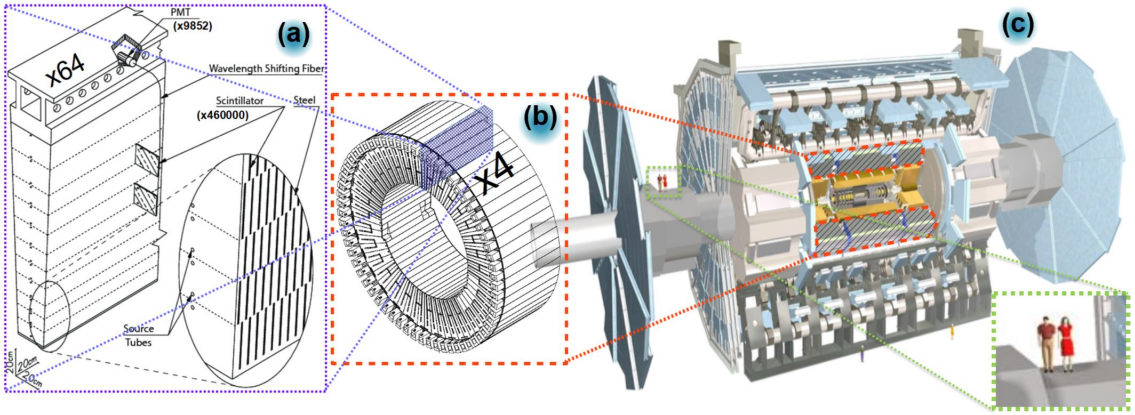


Figure 1.1: TileCal wedge-shaped module within ATLAS

1.2 About LVPS

The LVPS system of each TileCal wedge consists of an array of eight, nearly identical power supplies (bricks), configured in a parallel fashion (Fig. 1.2) [1]. It utilizes a custom galvanically isolated transformer with a 7:1 winding ratio. The LVPS brick steps down 200 V to 10 V and is nominally rated at 100 W. The LVPS brick is a dual-switch, forward-type high speed switching converter operating at 300 kHz. A dual switch topology is suitable for mid-power range switching converters with a high input to output voltage ratio [2]. A thorough analysis and understanding of this switch mode power supply is outside the scope of this thesis, but the technicalities necessary for the design of this burn-in station are presented below.

Figure 1.2: Four LVPS bricks arranged together

A functional block diagram of LVPS is represented in Fig. 1.3. On the primary side of the transformer, the power input consists of a 2nd order LC filter. Following the output winding of the transformer is half-bridge rectification followed by a 4th order LC filter. The commanded duty cycle signal is generated from a LT1681 controller [3] which is powered from an auxiliary winding of the transformer. After the brick is powered on and operating, all low voltage controls are powered from an auxiliary low voltage winding of the transformer. Additional control circuitry (with quick response time) has been synthesized outside of the main controller to shut down the brick in any event of excessive current, voltage or temperature.

Further, LVPS is controlled and monitored remotely by another system referred to simply as ELMB[1], which primarily adjusts the output voltage and switches the brick on and off. Since LVPS is paralleled on the output with seven other bricks,

the output voltage of each individual brick is tuned so that current is equally shared amongst the paralleled bricks. This tuning is accomplished by injecting a positive or negative DC signal (called "Vtrim") into the feedback error measurement of the controller. ELMB also turns on and off LVPS remotely through two signals: "Startup" and "RUN". The Run signal is a TTL 5V logic signal that must always remain high for the brick to be active. "Startup" is a 15V power source which is only required to power the control circuitry long enough until the brick is active for the auxiliary winding to power the control circuitry.

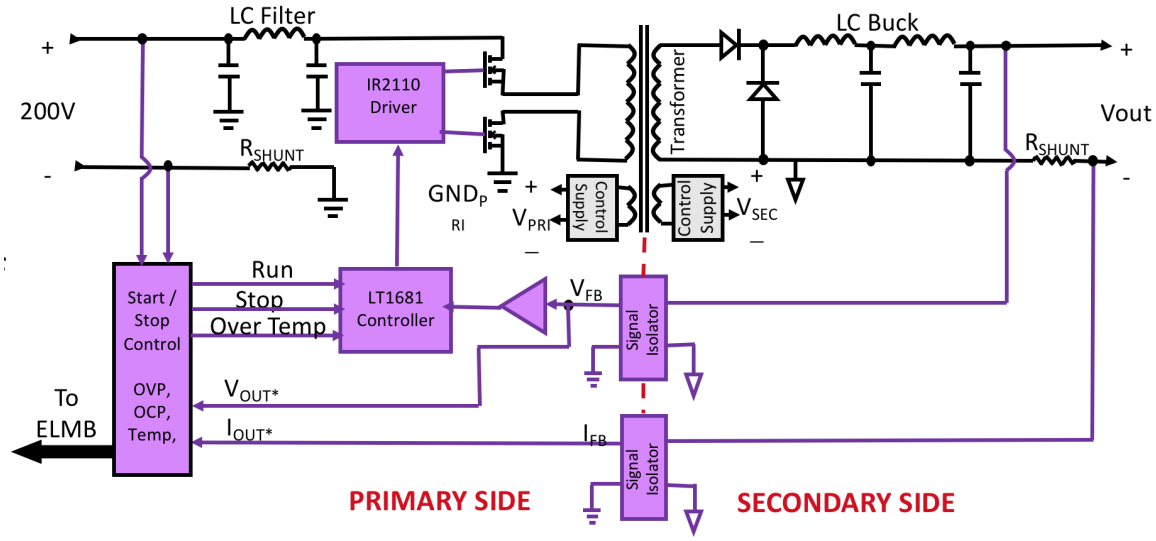


Figure 1.3: Brick diagram: dual-switch forward converter.

Some of the input and output is demonstrated in Fig. 1.4. The brick 200 V input, 10 V output and 20-conductor-signal ribbon connector are all shown. The silicon (MOSFETS and diodes) of the input and output side are also highlighted. The 20-pin ribbon connection carries analog values of the brick input voltage, output voltage, input current, output current, two thermistor voltages and the Vtrim signal.

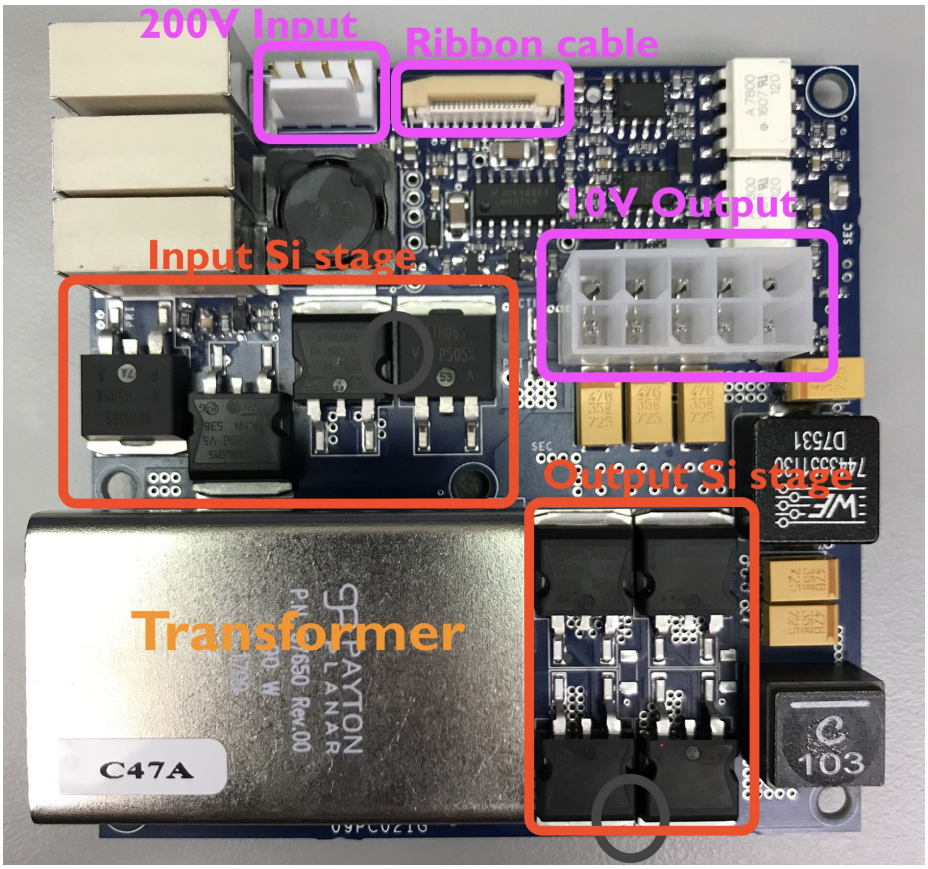


Figure 1.4: Brick diagram: component placement

LVPS also contains thermally conductive ceramic posts mounted on the bottom side of the PCB, directly underneath each power MOSFET or DIODE shown in Fig. 1.5 to conduct heat to a cooling-plate.

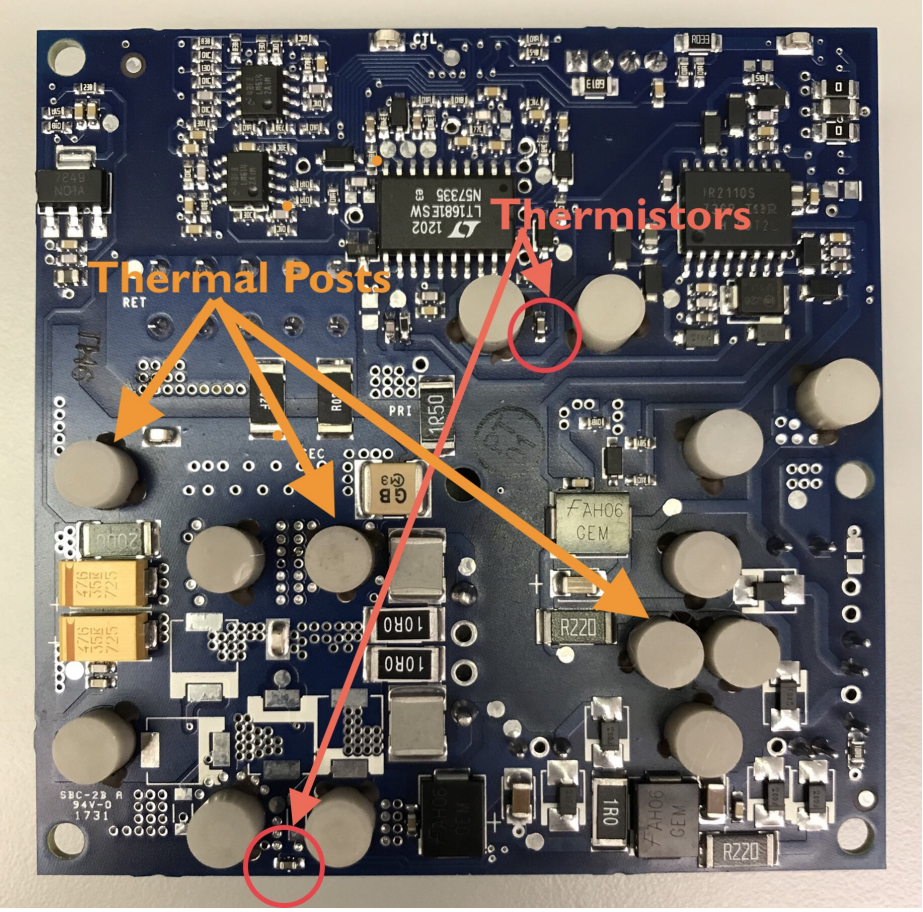


Figure 1.5: Brick diagram: thermal post and thermistor placement

1.3 Thermal Modeling: Heat Generation

The brick will operate in the burn-in station at near full load, 10 A at the output. The power losses of all the switching components of LVPS will now be determined at this load rating. The schematic function of these components are labeled in Fig. 1.6 and their layout placement is identified in Fig. 1.7. Components $T3$ and $T4$ are paralleled together, as well as $T5$ and $T6$.

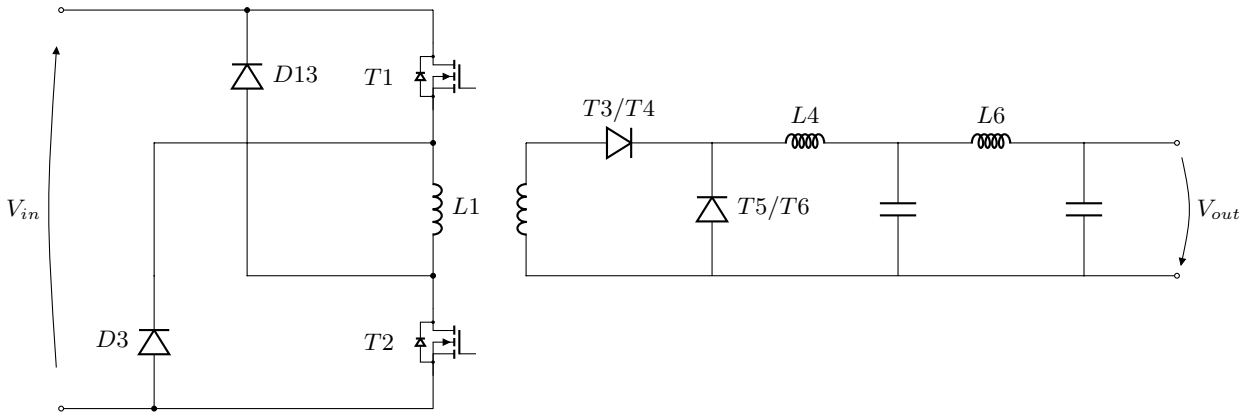


Figure 1.6: Schematic representation of power components of LVPS

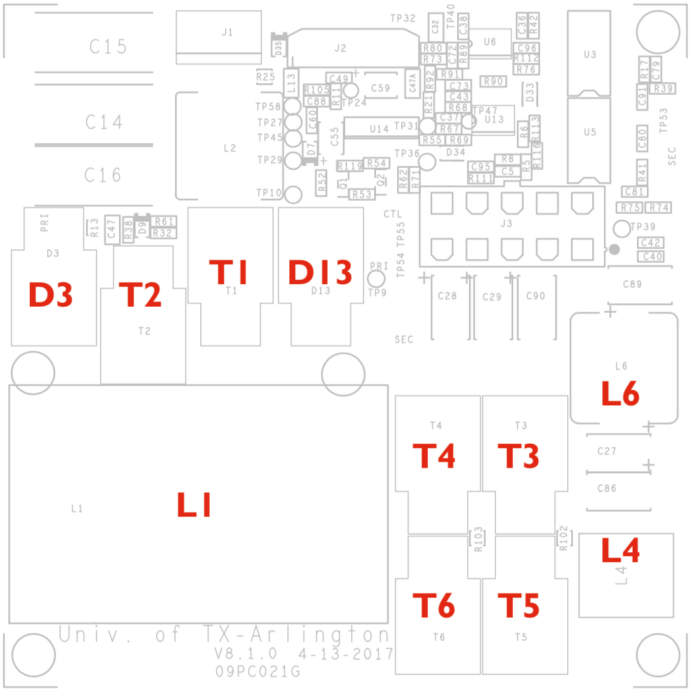


Figure 1.7: Layout of power components onto LVPS brick

The two modes of losses of importance in switching devices are the conduction losses and switching losses. At higher frequencies, the switching losses begin to dominate. Conduction losses were determined in the following way:

$$P_{ON} = I_O^2 \times R_{ON} \times D \tag{1.1}$$

where,

$$I_o: \text{ Output current} \tag{1.2}$$

$$R_{ON}: \text{ MOSFET on - resistance} \tag{1.3}$$

$$D: \text{ Duty Cycle} \tag{1.4}$$

The switching losses were calculated by:

$$P_{SW} = \frac{1}{2} \times V_{IN} \times I_O \times (t_r + t_f) \times f_{SW} \tag{1.5}$$

where,

$$t_r: \text{ MOSFET rise time [sec]} \tag{1.6}$$

$$t_f: \text{ MOSFET fall time [sec]} \tag{1.7}$$

$$f_{SW}: \text{ Switching frequency } [Hz] \tag{1.8}$$

To accurately model the heat generation determination of the switching devices, the switching times were measured on each of the power silicon devices of a LVPS brick operating at 100W.

Fig. 1.8 shows the voltage waveform for the flyback diodes, $D13$ and $D3$. The duration to become fully forward biased is 50ns and to fully reverse bias, 350ns.

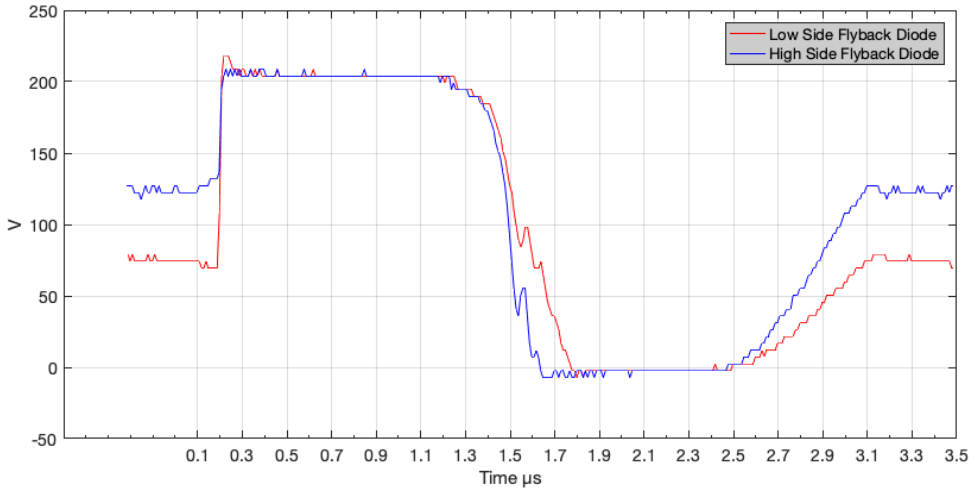


Figure 1.8: Transformer magnetizing inductance "flyback" diodes (high and low side), D3 & D14, small time division

Fig. 1.9 and Fig. 1.10 display the switching waveforms of $T1$ and $T2$. The duration to fully saturate, and then to turn fully off again is 25ns and 350ns.

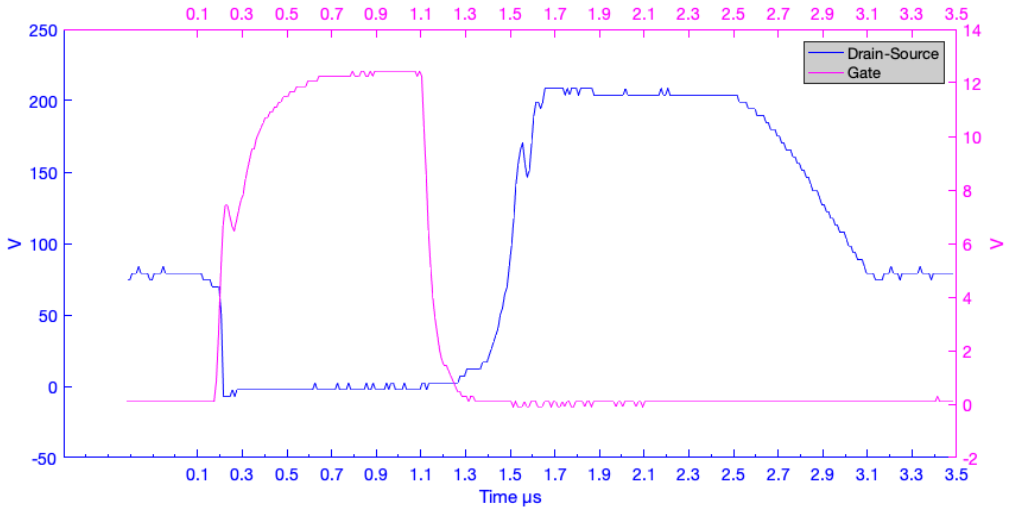


Figure 1.9: Low side MOSFET, T2, small time division

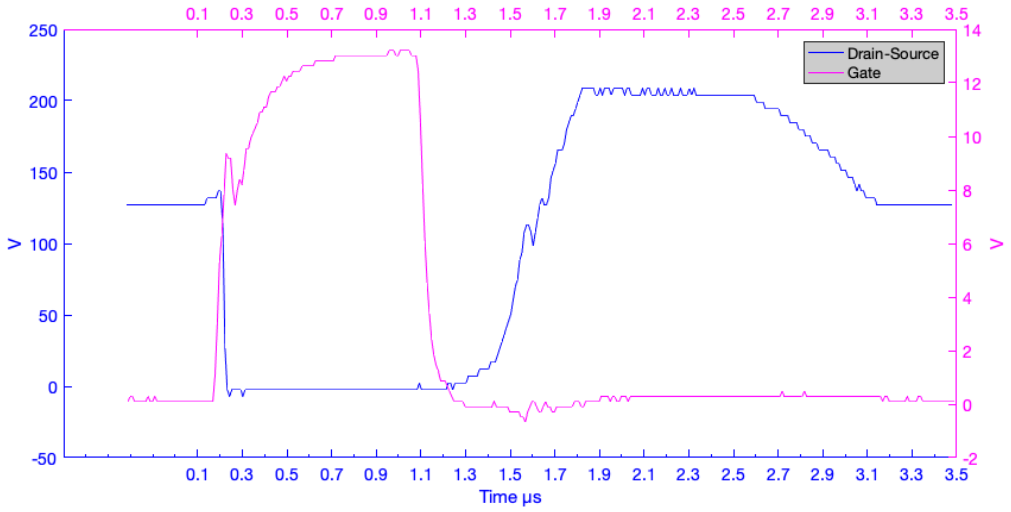


Figure 1.10: High side MOSFET, T1, small time division

Finally, Fig. 1.11 shows the voltage waveform for the output diodes, $T3/T4$ and $T5/T6$. The duration to become fully forward biased is 50ns and to fully reverse bias, 200ns for $T3/T4$ and 200ns and 500ns for $T5/T6$.

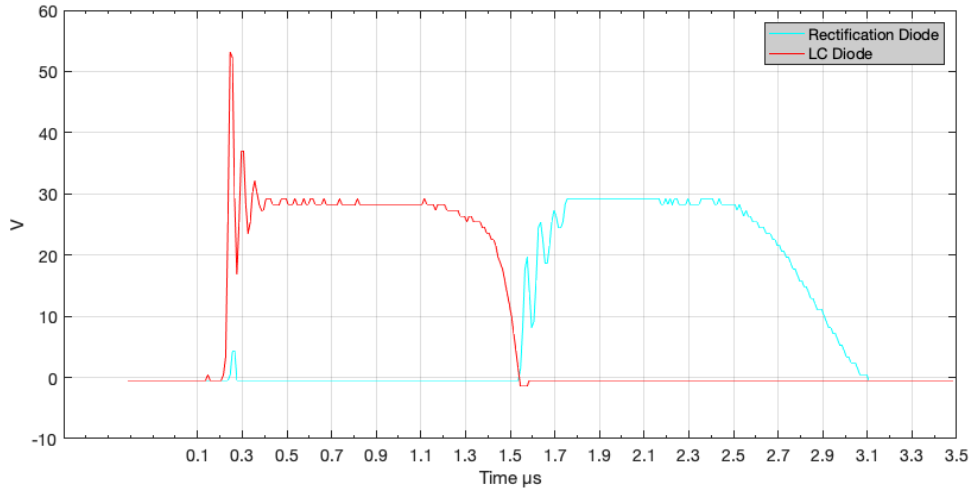


Figure 1.11: Output rectification and freewheeling diodes, T3/T4 & T5/T6, small time division

The component losses are quantified in Tab. 1.1 for the switching components and Tab. 1.2 for the magnetic components.

Component	Conduction	Switching	Total
T1+T2	0.011W	11.25W	11.261W
D3+D14	0.006W	1.8W	1.86W
T3+T4	0.011W	7.363W	7.374W
T5+T6	0.033W	3.682W	4.012W

Table 1.1: LVPS brick losses Silicon losses

Component	Conduction Loss
L1	5.3W
L4	0.57W
L6	0.18W

Table 1.2: LVPS brick inductor losses

The total losses of the brick is 19.7 W, while supplying 100 W on the output. The measured efficiency of the brick operating at 10 A in Fig. 1.12 (80.5%), which yields a high confidence in the losses determined analytically above.

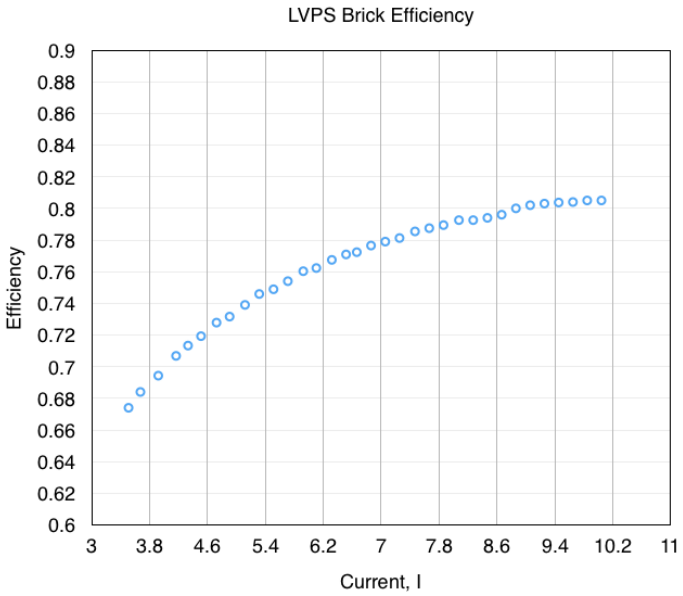


Figure 1.12: Efficiency of LVPS brick

1.4 Thermal Model: Temperature Rise

With the heat power generation known, the temperature rise of MOSFETs $T1$ and $T2$ are shown in Tab. 1.3. These two components generate the most heat.

	Temp. rise	C°/W
MOSFET, junction:	2.8C°	0.500
Solder pad:	0.5C°	0.092
Alumnium nitride	9.8C°	1.769
Thermal paste:	0.1C°	0.012
Temp. rise at junction:	13.3C°	
Temp. at junction:	**38.3C°**	

Table 1.3: Temperature rise of $T1$ & $T2$, ambient temp. 25C°

Similar results for temperature rise were also obtained from a FEA (Finite Element Analysis) including fluid dynamics and thermodynamics. LVPS was modeled with all conductive and dielectric layers (6 layer board), including the thermal posts

(Fig. 1.13) along with the final assembly including the cooling plate on which the LVPS is mounted. The maximum temperature and heat flux surface plots are displayed in model cross-sectional diagrams of Fig. 1.14a and Fig. 1.14b.

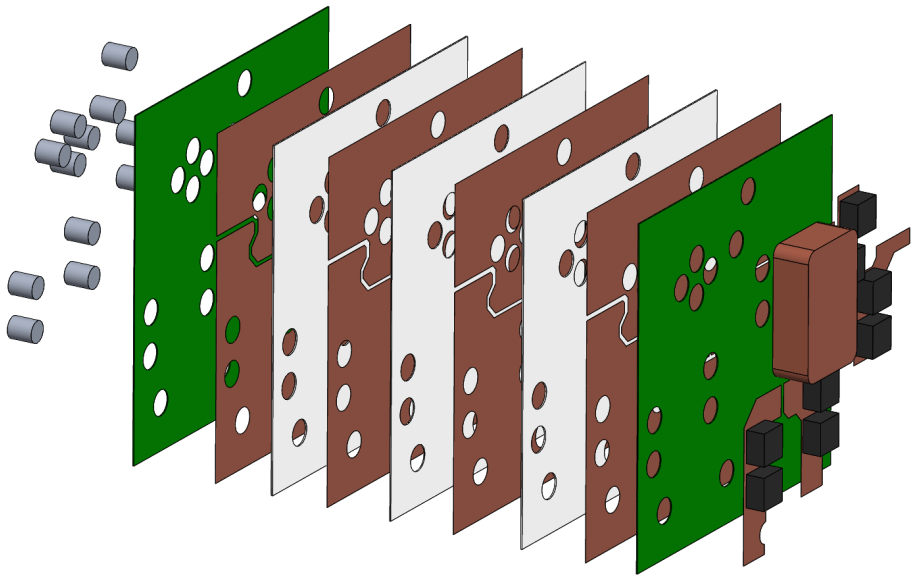
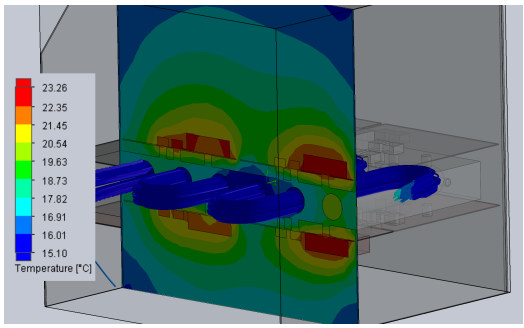
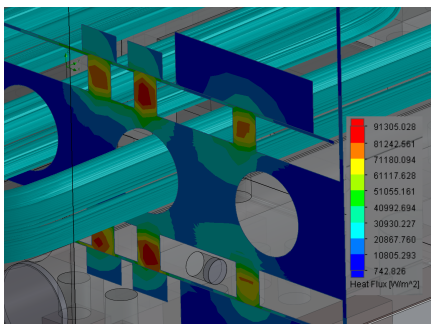


Figure 1.13: Parametric solid model of LVPS with all six layers and thermal posts



(a) LVPS Box Temperature Gradient



(b) Heat Flux Gradient

CHAPTER 2

BURN-IN STATION

2.1 Infant Mortality and Accelerated Aging

Accelerated aging, referred to as burn-in testing is a process to detect premature failure in components. During the burn-in process, components are stressed in an environment with an elevated temperature. This environment stresses the electronics under test and causes components that would fail prematurely, to fail immediately during the duration of this test before the newly manufactured electronics are deployed on the detector where access can be very limited. The type of failure that occurs early in the life of new electronics is referred to as "infant mortality failure". This period of early failure is shown in the failure rate plot of Fig. 2.1. This curve is called the "bathtub" curve [4].

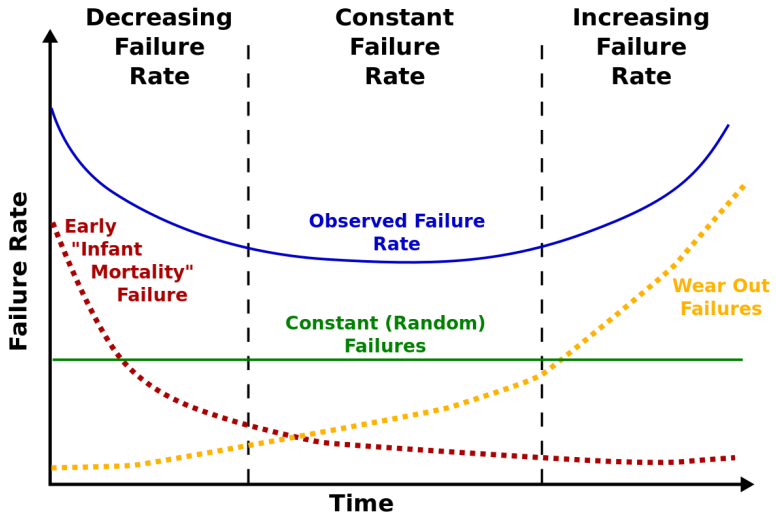


Figure 2.1: "Bathtub" curve of electronics lifespan

The three stages of failure that define the full life span of a population of electronics are described by the following:

- Stage 1, Infant Mortality: This is the period where early failures reveal themselves. This is possibly due to a lack of control in manufacturing processes. Components fail at a high rate, but this rate decreases with time.
- Stage 2, Normal Useful Life: This is the period where rate of failure is nearly constant, and due to randomly occurring faults.
- Stage 3, End of Life: Period marked by increase in failure rate due to aging of components; this period marks the end of the useful life span of a device.

The failure rate of any of these stages can be quantified in terms of the hazard function $h(t)$ which is the number of unit failures per unit of time.

$$h(t) = \frac{f(t)}{R(t)} \tag{2.1}$$

$f(t)$ is the time to (first) failure distribution (failure density function) and $R(t)$ is the probability of no failure before time t. $R(t)$ can be related to the failure distribution $F(t)$ through,

$$R(t) = 1 - F(t) \tag{2.2}$$

The Hazard function $f(t)$ depends on the existence of the a failure distribution $F(t)$ describing the probability of failure where T is time at which failure occurs.

$$\Pr(T \leq t) = F(t) = 1 - R(t), \quad t \geq 0 \tag{2.3}$$

The failure distribution $F(t)$ is also the integral of the failure density function $f(t)$:

$$F(t) = \int_0^t f(\tau) d\tau \tag{2.4}$$

For stage one, of infant mortality failure, I use the Pareto probability distribution function with shape parameter a for the failure density function $f(t)$.

$$f(t) = \frac{a}{t^{a+1}}, \quad t \geq 1 \tag{2.5}$$

The failure distribution then becomes,

$$F(t) = \int_0^t \frac{a}{t^{a+1}} = 1 - \frac{1}{t^a} \tag{2.6}$$

The hazard rate, or failures per unit time now becomes,

$$h(t) = \frac{f(t)}{R(t)} = \frac{at^a}{t^{a+1}} = \frac{a}{t} \tag{2.7}$$

This describes well the exponential failure rate seen in stage 1 of Fig. 2.1.

For stage two, of normal operation life, the exponential failure distribution function with rate parameter λ, is suitable for the failure density function $f(t)$.

$$f(t) = \lambda e^{-\lambda t} \tag{2.8}$$

The failure distribution then becomes,

$$F(t) = \int_0^t \lambda e^{-\lambda \tau} d\tau = 1 - e^{-\lambda t} \tag{2.9}$$

The hazard rate now becomes a constant, independent of time.

$$h(t) = \frac{f(t)}{R(t)} = \frac{\lambda e^{-\lambda t}}{e^{-\lambda t}} = \lambda \tag{2.10}$$

When data has been collected on many bricks early on in the manufacturing process, the parameters of this model can be selected to match the failure rate seen in production.

2.2 Burn In Test Procedure

During the production testing cycle of LVPS, each brick will be checked into a burn-in station which performs the accelerated aging. Here, a LVPS brick is subjected to a stressed environment where the load and temperature are both elevated. In this environment the expected operational life of the brick is slightly reduced, in order to get the run duration through the infant mortality state in a more timely manner. It is ideal to operate the test above 60°C, and slightly below the lowest maximum temperature of any device on the brick, which is 80°C. The following parameters have been selected for the burn in procedure.

Duration:	6 hours
Temperature:	80°C
Brick Load:	100 W (10 A)
Startup Cycles:	30+

Table 2.1: LVPS Brick Burn In Operating Parameters

2.3 Electronics

The electronics of the burn-in station consist of a desktop PC with software that controls eleven compartmentalized individual microprocessors located within the

burn-in station. The burn-in station is centrally controlled, and data is saved and presented on screen from the central PC. The main program that runs on the PC was created in the LabView[5] environment. The LabView program previous existed and was modified and maintained to function with this new burn-in station. Software used in the microprocessors local to the burn-in was custom created, although sections of legacy code was used for inspiration.

Since an external coolant refrigeration unit was not used in this design and forced-convection heat sinks was integrated in its place within the burn-in station, the total equipment necessary to operate the burn-in station, external to the burn-in station is a Windows-based PC and high voltage power supply. The data communication of this equipment is shown in Fig. 2.2. The high voltage power supply (PVS60085MR) normally supplies 1 kW of power at 200 V while the burn-in station is operating populated with eight bricks. The PVS60085MR supply is controlled by the PC LabView software via a VISA[6] communication link over Ethernet.

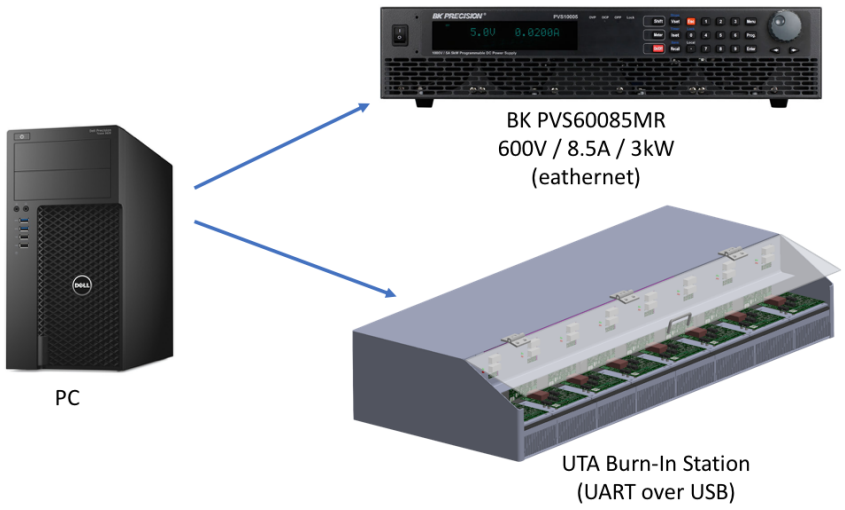


Figure 2.2: UTA Burn In Station Equipment

The PC LabView software communicates with all eleven microprocessors in the burn-in station through a single UART[6] layer link passed over a USB bus. UART communication is suitable for embedded system to PC-based microprocessor communications[6]. A FTDI IC is used to facilitate UART over USB.

The eleven microprocessors internal to the burn-in station perform specific function tasks. There are three types of PCBs (Printed Circuit Boards) within the burn-in station: x8 "Brick Interface" PCBs (one for each brick), two "Load Interface" PCBs and one "Supervisor". Only the Main Board physically communicates directly with the PC, and communicates itself directly to every other interface board. Its primary function is to multiplex between the PC and the ten other interface boards. This way, the LabView software on the PC communicates with only one microprocessor at a time. This communication diagram is shown in Fig. 2.3 where the black-colored paths are UART buses. Note that these buses do not represent traditional UART over a RS232 bus (+/-15 V), but over a USB bus from the PC to the Main Board, and then from the main board to the various interface boards over TTL logic. Each interface board for the brick and load contains a 16 bit PIC16F883 microcontroller.

All the other colored paths carry power. The orange path carries 200 V to each brick, red path carries 12 V to power each interface PCB, and the purple path is the 12V output from each individual brick to the electronic load.

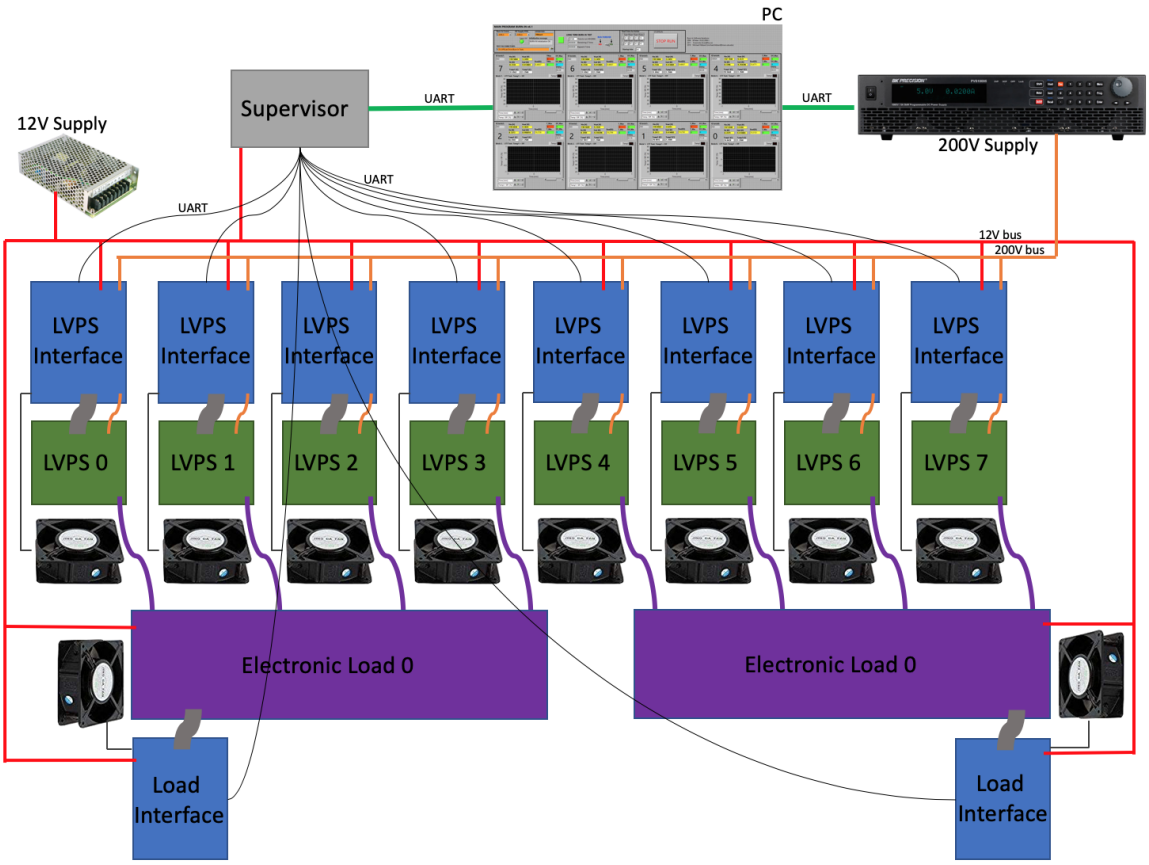


Figure 2.3: Burn-in station internal electronics communication diagram

The purpose and functionality of each interface PCB is presented in the next few section.

2.3.1 Main Board

The LabView software on the PC communicates directly via UART to each individual microprocessor. The communication is established by means of a serial link (RS232) over a USB virtual COM port using a FTDI IC[7]. This is accomplished by having the main board function purely as a multiplexer to each individual read out board. LabView on the PC accomplishes this multiplexing by asserting the RTS (Request to Send) flag on the UART level, transmitting the address of the desired

interface board the PC wished to communicate with (0-9), and then un-asserting the RTS flag. All bytes sent from the PC after this address initialization are then passed directly to the corresponding read out board with no work or interference done by the main board at all. Note that the UART TX of each interface board are all bussed together (Fig. 2.4).

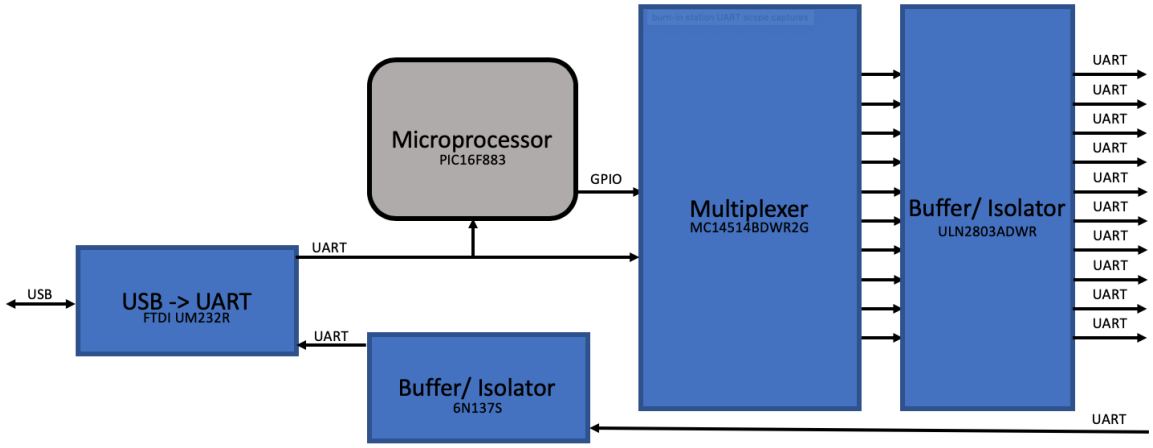


Figure 2.4: Supervisor functional block diagram. Left paths communicate with the PC. Right paths communicate with interface boards.

2.3.2 Brick Interface Board

The primary job of the brick interface board is to digitize and transmit data to the PC from various analog inputs of each brick's 20-pin ribbon cable. A 16-channel ADC from Linear Technology (LTC2449) [8] is the heart of the brick interface board. All behavioral parameters of the brick are measured, such as "Vin", "Iin", "Vout", "Iout" and two brick temperatures. Each brick has its own identical and corresponding interface board to control and monitor each brick. Beside digitizing all analog signals. The interface board also turns on and off the 200 V input supply via a high side MOSFET, and controls the state of the Run_IN signal (5 V) and 15 V startup pulse. The interface board also contains the voltage dividers for the

thermistors located on the brick to avoid temperature drift of the thermistor voltage divider circuit (Fig. 2.5).

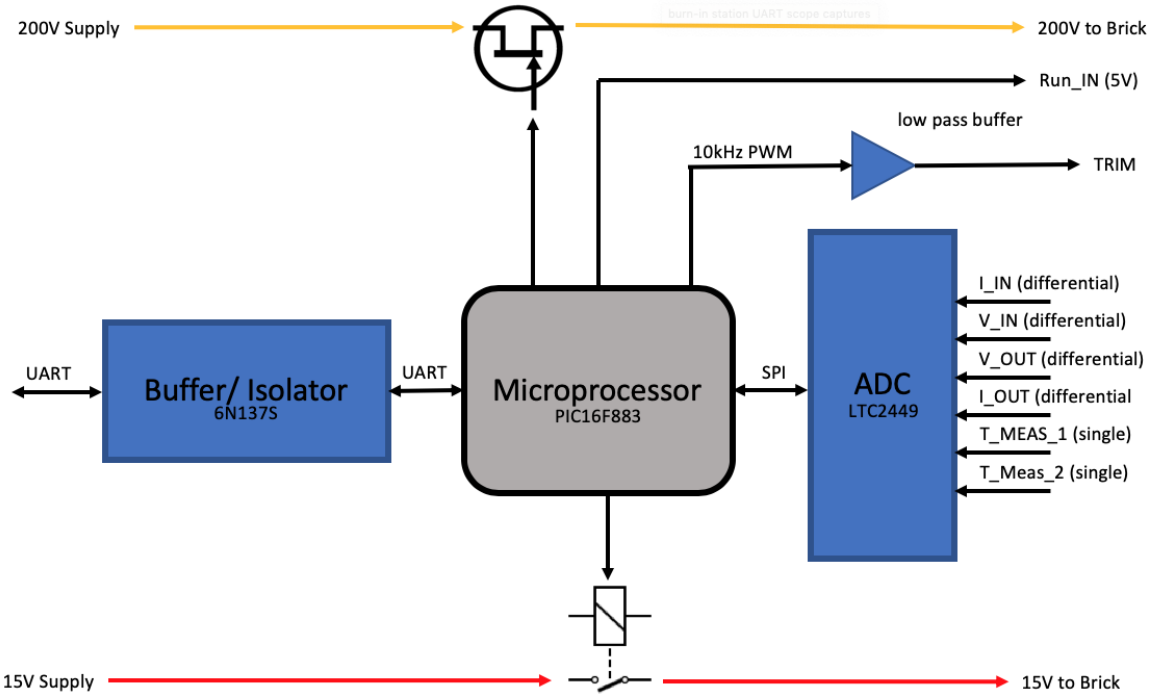


Figure 2.5: Brick Interface Board: Left paths communicate with Main Board. Right paths communicate with bricks.

2.3.3 Electronic Load

Each burn-in test station contains two electronic load boards. Each load board is equipped with four independent programmable current loads for four bricks (currents of 0.5 A – 10 A, maximum input voltage of +32 V). The energy of the load is shunted through a MOSFET, operating in the ohmic or triode region. This ohmic MOSFET is driven by an op-amp, which compares the value of the shunt voltage (negative input) with the value on the positive input from a DAC. This configuration is inherently current-mode control, and the opamp will always track the brick load current against the DAC output voltage (Fig. 2.6).

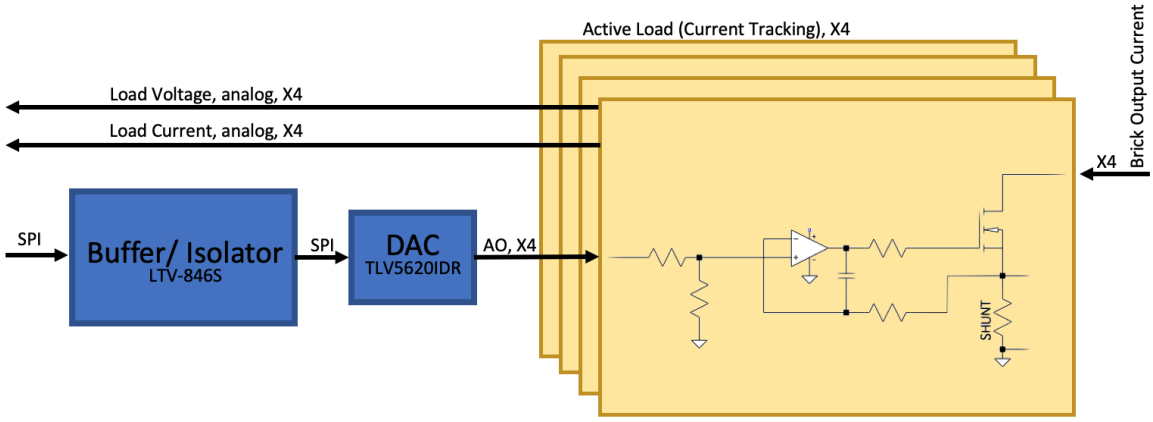


Figure 2.6: Electronic Load: Left paths communicate with Load Interface Board. Right paths communicate with brick output.

2.3.4 Load Interface

The load interface board is very similar to the brick interface board, in that the heart of this PCB is the same LTC2449 ADC which samples the voltage and current of the brick output measured at the electronic load. The second task of the load interface is to shift bits into the registers of the DAC contained on the electronic load to command the load current (2.7).

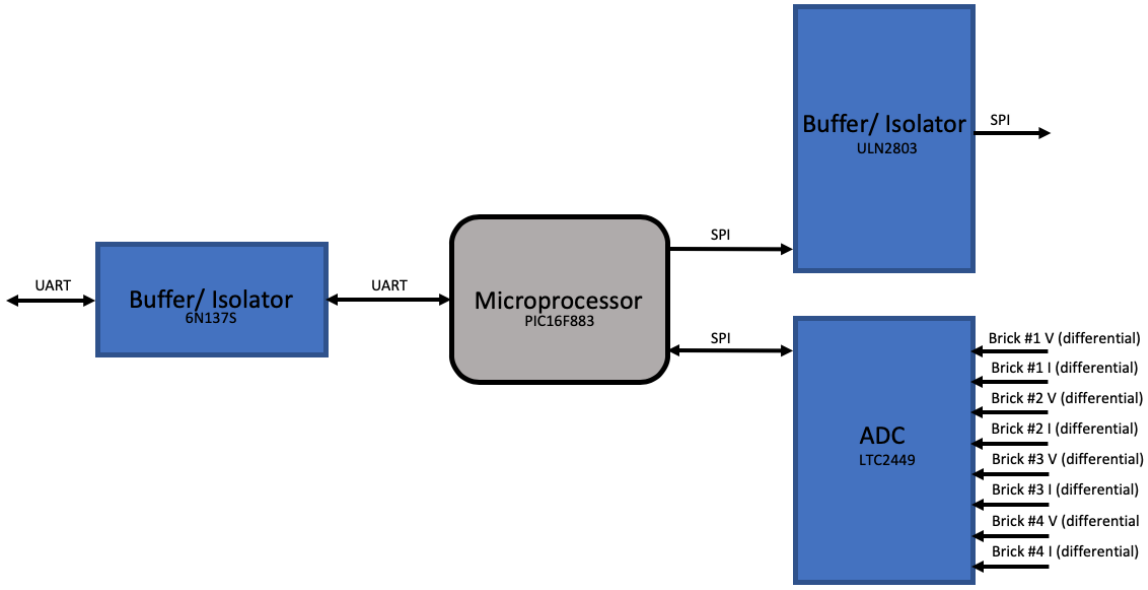


Figure 2.7: Load Interface: Left paths communicate with Main Board. Rights paths communicate with Electronic Load.

2.4 Hardware Design

The sizing of heat sinks and the design of the mechanical enclosure are now discussed in the new few sections.

2.4.1 Heatsink Cross Sectional Selection

Because bricks are capable of over heating (operating well above 80°C) with just moderate load, the waste heat of the bricks will be used to elevate the temperature of the bricks. The temperature of the bricks will be maintained by sinking heat out of them, through the thermal ceramic posts to heat sinks located below them. Heat sinks will also be utilize to sink heat away from the ohmic-MOSFETs used in the electronic load. The forced air convection approach will now be used to synthesize a solution to meet the temperature and heat flux sinking requirements of both the load and the brick.

Extruded fins from a surface can increase the heat transfer from that surface, by several fold. This section studies the optimal arrangement of external extruded fins over a base surface in order to obtain the maximum heat transfer allowable at a given temperature and heat convection rate. The area of the surface being considered is 10 cm by 10 cm. Certain design restriction have been imposed for simplicity and packaging constraints. First, the height of the fins are to be no taller than 100 mm. The material for the fins of the heat sink will be aluminum. Aluminum is a desirable due to its high thermal conduction, reasonable price, and corrosion resistance to many different environments. The fins are also to be straight and of constant cross sectional area. First the configuration of a singular fin will be studied to determine what parameters are important in determining the optimal configuration, then an array of fins will be studied with regard to their efficiency combined to determine the optimal configuration of an array of fins.

It is desirable to have as minimal temperature gradient as possible across the length of a fin; to accomplish this the fin must grow larger in thickness. However the number of fins on the surface will decrease as a result. The consequence is that the total surface area of the combined fins is reduced. Herein lies the topic of study. An optimal fin thickness must be chosen which maintains the minimal temperature gradient across a fin while maintaining the maximum total fins surface area on a finite base space.

An individual fin's performance can be quantified as below:

$$\varepsilon_{\mathrm{f}} = \frac{\mathrm{q_f}}{\mathrm{hA_c}\theta_{\mathrm{b}}} = \sqrt{\frac{\mathrm{kP}}{\mathrm{hA_c}}} \tag{2.11}$$

Where A_c is the fin cross-sectional area at the base, k is the thermal conductivity, h is the convection coefficient, q_f is the heat transfer rate, θ_b is the temperature at the

fin base, P is the fin perimeter and A_c is the fin cross sectional area. Notice in the statement of the fin performance, performance increases with increasing perimeter and decreasing cross sectional area. This is a key design consideration. The use of fins are also normally justified when $\varepsilon_{\mathrm{f}} > 2$ [9]. Therefore in order to justify our use of fins, the following condition must be true:

$$\frac{kP}{hA_c} > 4 \tag{2.12}$$

Since the thermal conductivity k is known (aluminum) and the heat transfer coefficient h for forced convection over a surface is be assumed ($150 W/m^2K$).

Now that I have considered the optimal configuration of an individual fin, the conditions for the optimal configuration of fins into an array will be studied. The optimal configuration of an arrays of fins is,

$$\eta_o = 1 - \frac{NA_f}{A_t}\left(1 - \eta_f\right) \tag{2.13}$$

$$A_t = NA_f + A_b \tag{2.14}$$

where N is the number of fins, A_f is the surface area of a fin, A_t the combined surface area of the fin and base and A_b is the prime surface of the base, in-between fins. From this relation I can identify that the highest optimal configuration of an array of fins results when fin performance is highest (no surprise) and the number of fins increases.

Now the heat transfer can be quantified based upon the fin performance. The heat transfer rate is given by:

$$q_t = hA_t \left[1 - \frac{NA_f}{A_t}\left(1 - \eta_f\right)\right]\theta_b \tag{2.15}$$

Notice that for the same system, (θ_b,h held constant), the heat transfer rate increases linearly with increasing number of fins and increasing fin performance. Therefore when designing an array of fins, it is optimal to set the number of fins and fin performance as large as possible.

There is an important consideration that this system of equations does not account for, which is boundary layer thickness. If there is interaction between the boundary layers that develop on opposing surfaces of adjoining fins, performance will suffer. Therefore the thickness of the fins should be configured such that the boundary layer on one side of a fin never exceeds half of the spacing between fins. The boundary layer thickness is what will essentially prevent the number of fins from approaching infinity.

Through an iterative process between determining the optimal fin arrangement, the physical mechanical packaging constraints, and the constraint of what is current available for purchase, the Wakefield-122547[10] was selected (Fig. 2.8).

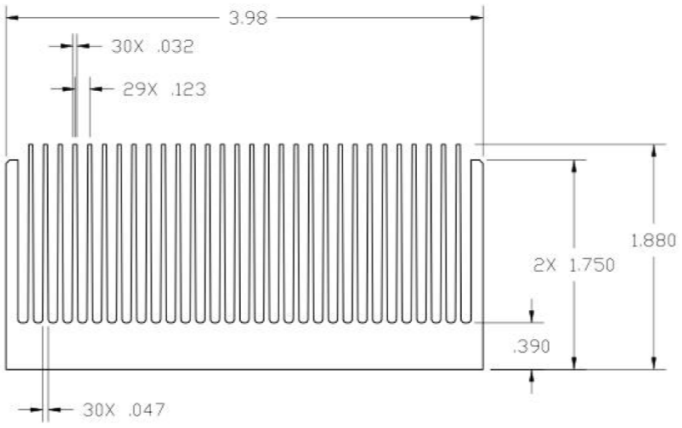


Figure 2.8: Heat sink profile

2.4.2 Heatsink for Electronic Load and Brick

With a heat sink cross section selected. The length, volumetric flow rate and pressure required for fan selection will be studied.

The heat sink for the electronic load was sized appropriately so that the full power output of the brick at 10A could be dissipated while allowing a sufficient temperature margin. The selected MOSFET for use as the current sink from the bricks is the IRFP260NPbF[11]. The fan selected is the SanAce 9GV1212P1J01. The performance of this fan is shown in Fig 2.10. The heat sink length is 19 cm. The manufacturer for this heat sink only provides thermal data for free convection. Since we are utilizing forced convection, computation fluid dynamics are utilized to determine the performance of this heat sink applied to the electronic load[12] [13].

Below are the specs which the electronic load was designed.

Parameter	Value	Unit
Ambient Temperature	35 °	C
Output power per brick	100	Watts
MOSFET Thermal Resistance, Junction to case	0.74	°C/Watt

Table 2.2: Electronic Load specifications

Because of thermal coefficient of the selected MOSFET is so high ($0.74°C/W$), two FETs were selected to operate in parallel for each brick. Due to the packaging constraints and layout, one heat sink 19 cm long was determined to be appropriate to dissipate the load of two bricks (100W, amongst 4 FETs). The packaging of the power MOSFETs onto the heatsink is shown in Fig. 2.9.

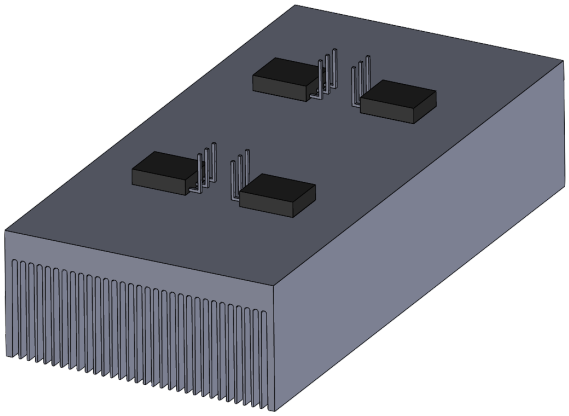


Figure 2.9: Electronic load heat sink

The pressure vs volumetric flow plot for the selected fan is shown in Fig. 2.10.

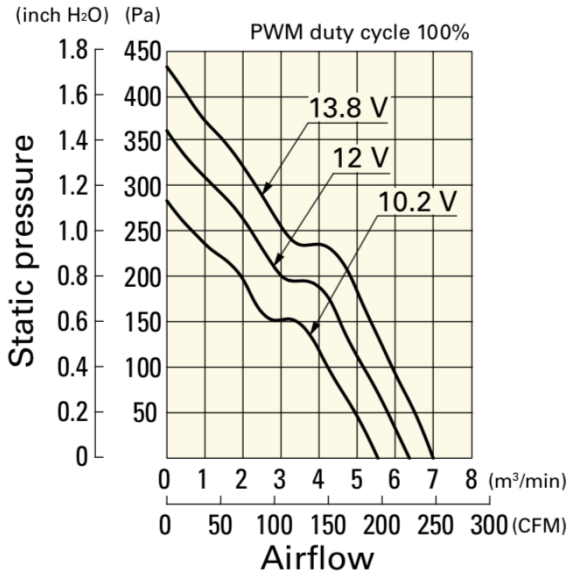


Figure 2.10: Electronic load fan pressure vs volumetric flow rate

The ambient air temperature initial condition for which the CFD plots were generated from is 25°C, with a volumetric flow rate of 0.066 m^3/s (air, 50% relative humidity). The temperature rise of the heat sink in Fig. 2.11 is 2.85°C.

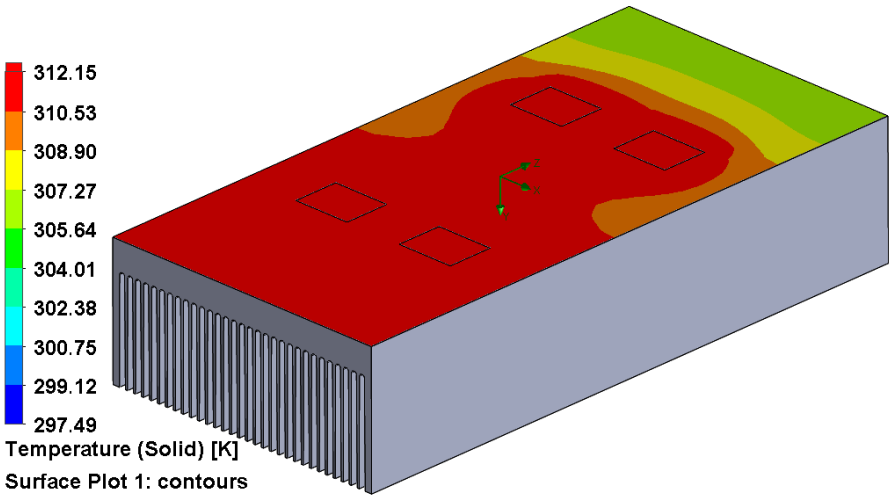


Figure 2.11: Electronic load heat sink temperature surface plot

For the stated volumetric flow rate, a pressure rise of across the heat sink (239 Pa) in Fig. 2.12 is under the plot line for the performance plot of the fan in Fig. 2.10.

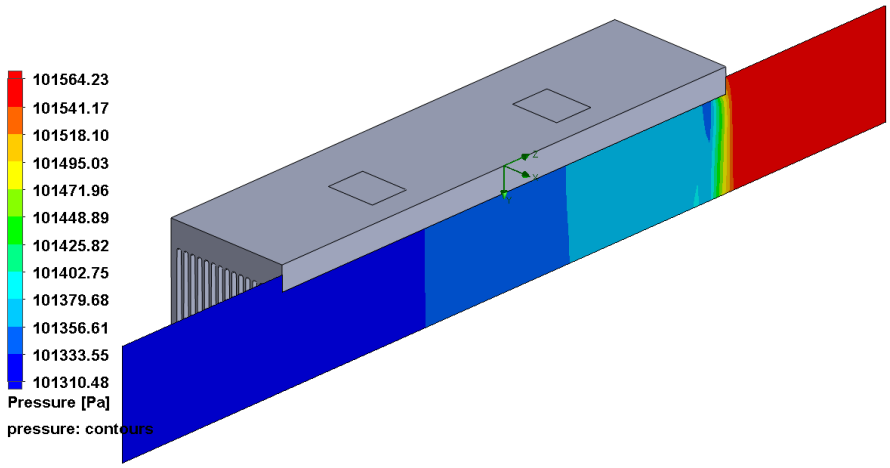


Figure 2.12: Electronic load heat sink pressure plot

The temperature rise of the fluid (air) across the heat sink rose in temperature 10.33°C (Fig. 2.13).

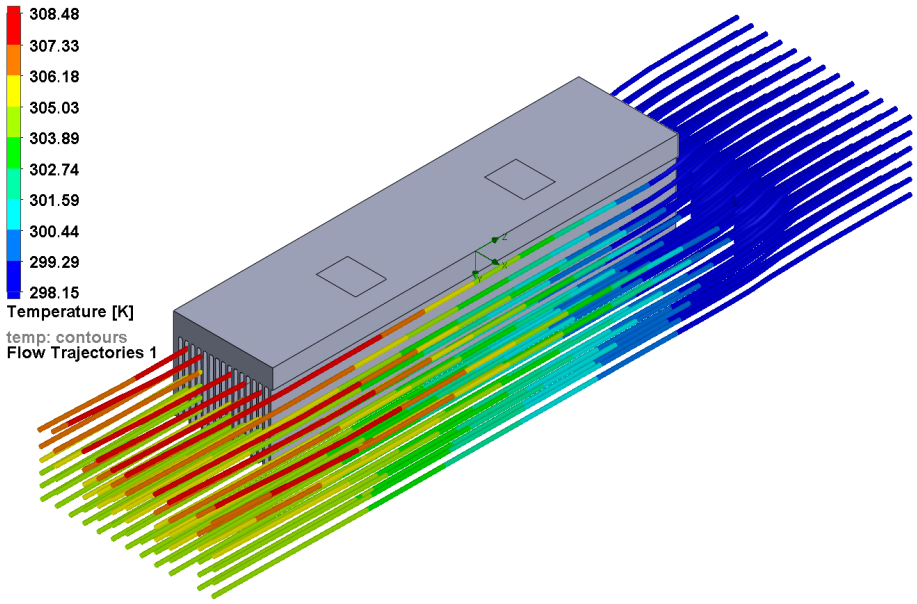


Figure 2.13: Electronic load heat sink fluid temperature rise

Similarly for the heat sink used to prevent the brick from damaging itself during the burn-in process (reaching an excessive temperature), a CFD was utilized to determine the heat sink length, volumetric flow rate and pressure required for the fan selection.

The heat sink for the brick was sized appropriately so that the full power dissipated by the brick due to its inefficiency at 10 A output (20 W) could be dissipated while allowing a sufficient temperature margin. The fan selected is the SanAce 9G0612G1011. The performance of this fan is shown in Fig2.14. The heat sink length is 10 cm.

The pressure vs volumetric flow plot for the selected fan is shown in Fig. 2.14.

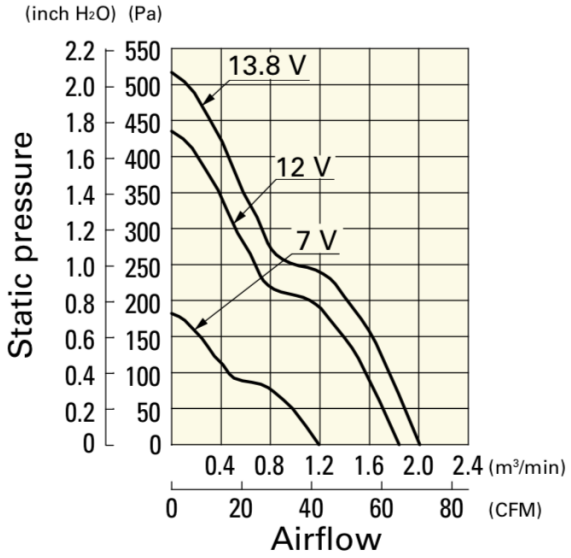


Figure 2.14: small fan pressure vs volumetric flow rate

For the CFD study in the next plots, the ambient air temperature was selected to be 25°C with a volumetric flow rate of 0.016 m^3/s (air, 50% relative humidity). The temperature rise of the heat sink in Fig. 2.15 is 2.85°C.

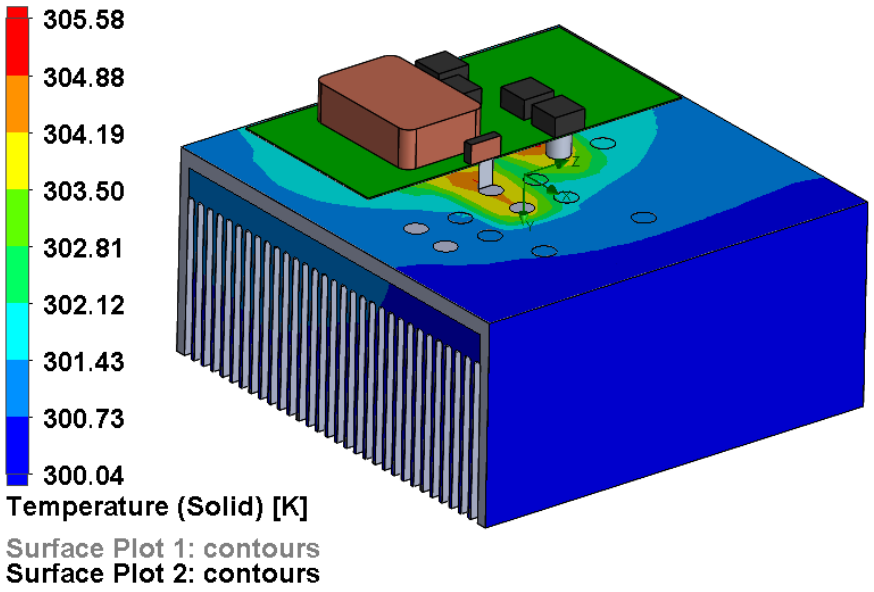


Figure 2.15: Brick load heat sink temperature surface plot

For the stated volumetric flow rate, the pressure rise across the heat sink is 65 Pa (Fig. 2.16), which is under the plot line for the performance plot of the fan in Fig. 2.14.

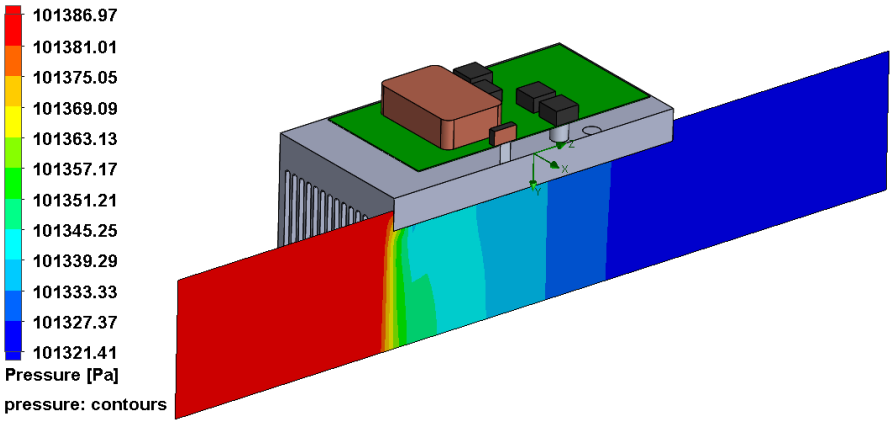


Figure 2.16: Brick load heat sink pressure plot

The temperature rise of the fluid (air) across the heat sink rose in temperature 5.54°C (Fig. 2.17).

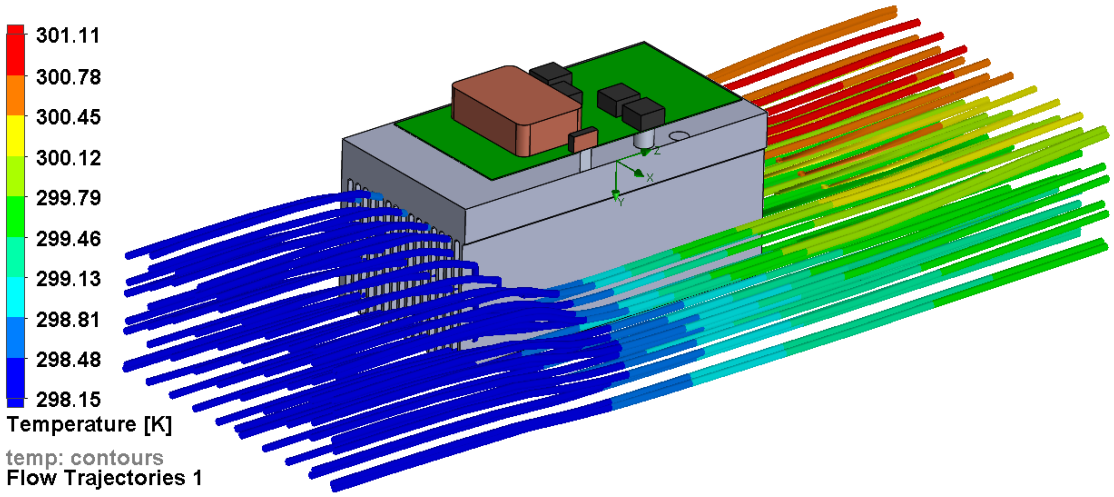


Figure 2.17: Brick load heat sink fluid temperature rise

The HVAC system of the lab environment must be able to sink the heat generated by the burn-in station out of the lab space. At UTA, room 001 of Science Hall is rated for "2tons" of heat capacity, which is the capacity to melt two imperial tons of ice within 24 hours, which is also 7 kW. With the lights (1.3 kW), 8 computers, four people and 3 burn-in stations operating in the lab, that totals just under 7kW (assuming lab walls are adiabatic). Therefore, the lab should ideally not be loaded up to this condition.

2.4.3 Enclosure Hardware

The 3D parametric solid model of the burn in station is displayed below in Fig. 2.18. The final exterior dimensions of the footprint are 46 cm x 87 cm by 21 cm tall.

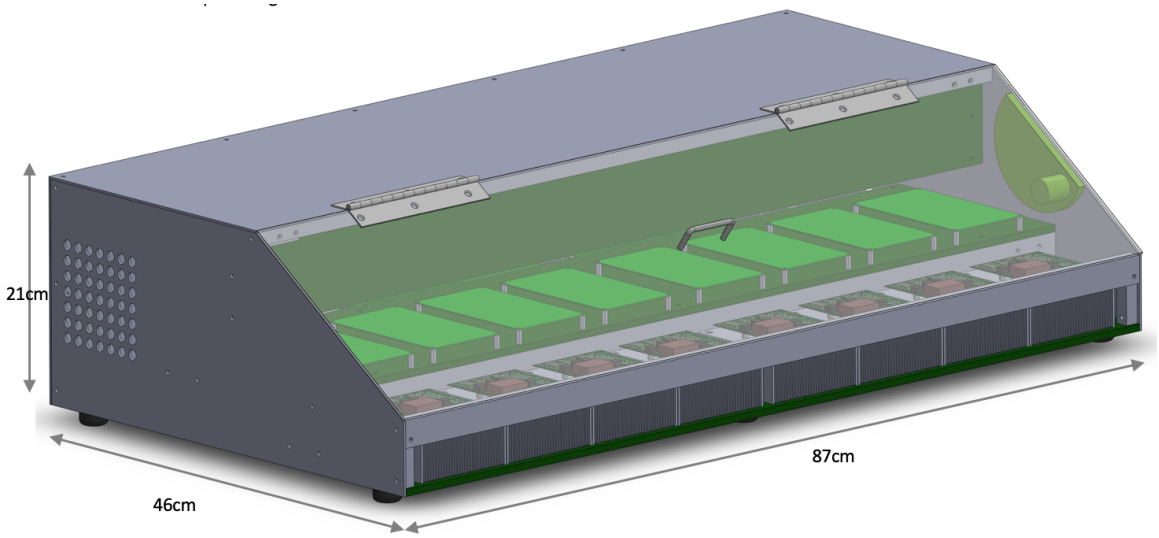


Figure 2.18: Burn in exterior dimensions

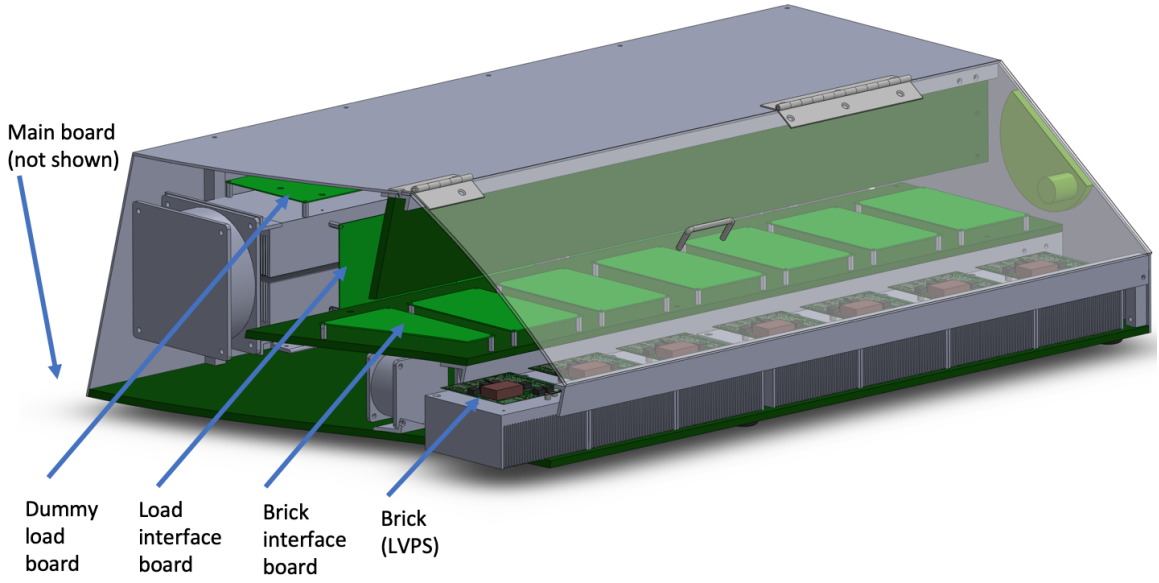


Figure 2.19: Burn in cross sectional view displaying internals

Fig. 2.19 and 2.20 displays how the electronic load was packaged. Four heat sinks were used in the dissipation of the brick load, with two bricks sourcing their

load into each heat sink. The air intake is pulled into the middle and exhausted out to the left and right sides through the heat sinks (Fig. 2.21). The short-length heat sink underneath the brick (only one brick shown) in Fig. 2.20 maintains the brick temperature by the fan placed behind it exhausting air forward of the burn in station.

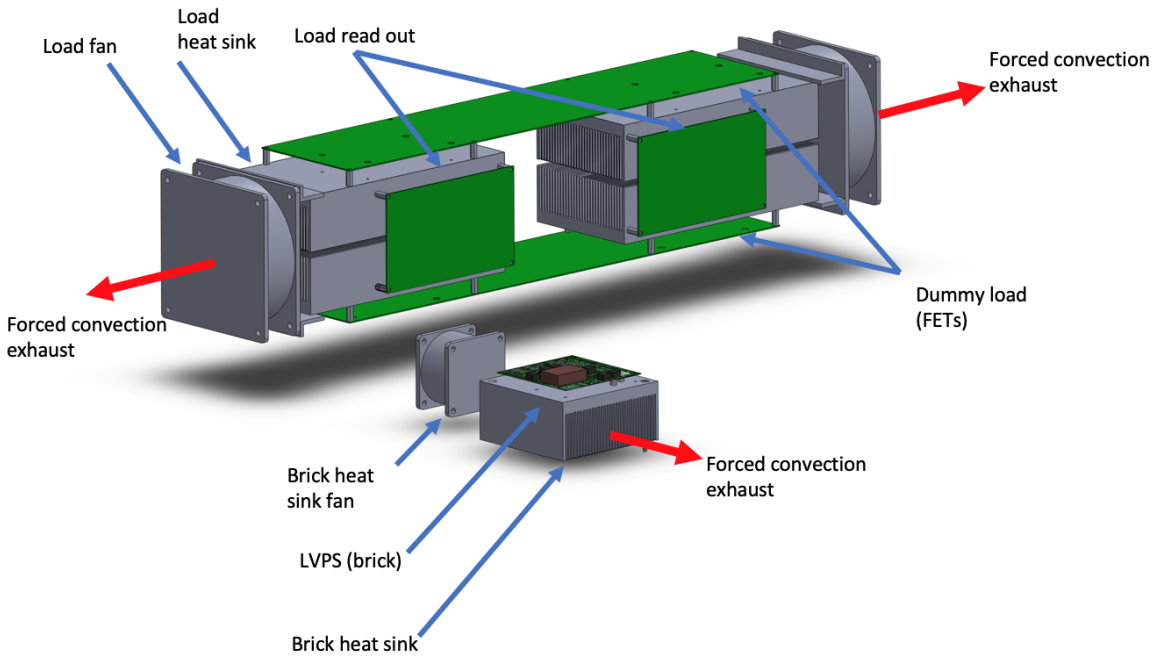


Figure 2.20: Burn in enclosure hidden away, displaying electronic load in back, and brick in front (only one brick shown)

In Fig2.21, the rear intake for the electronic load, and air exhaust of the the electronic load are shown.

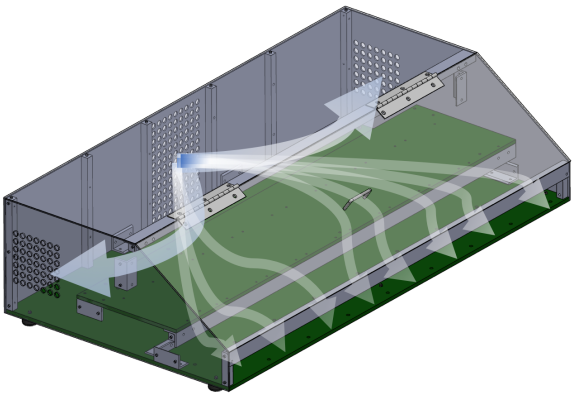


Figure 2.21: Air flow for electronic load and brick heat sinks

Several copies of the burn in station will be produced, and possibly shipped to different nations. With this in mind the construction was designed to be stiff and rugged to survive shipment. The primary structure consists of 3/8th inch fiber glass board with 1/2 inch thick aluminum columns used to attach the exterior panels (Fig. 2.22).

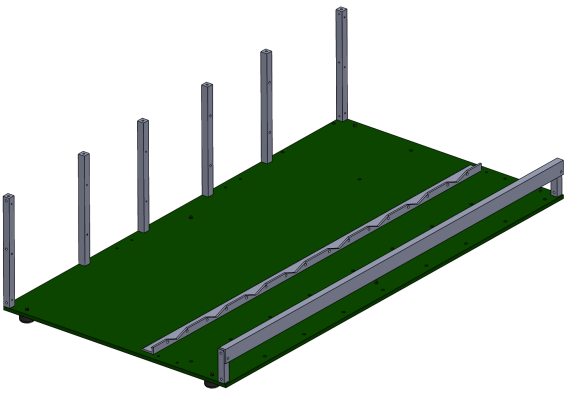


Figure 2.22: Burn-In enclosure structure

In Fig2.23 the exterior panels are attached and are partially transparent. The panels consist of 33 mil thick 6061 aluminum sheet.

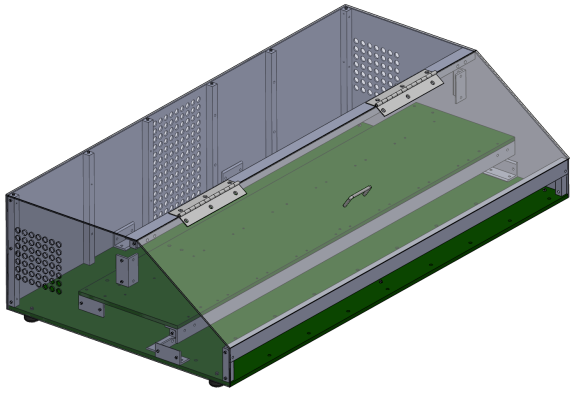


Figure 2.23: Burn-In enclosure with exterior panels (panels transparent)

In Fig2.24, the interior of the burn in station is populated with all internal electronics.

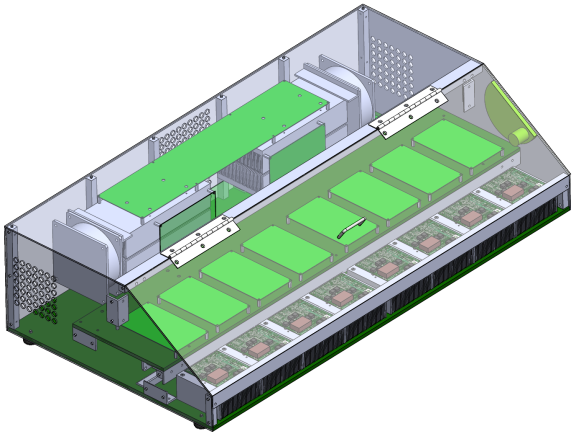


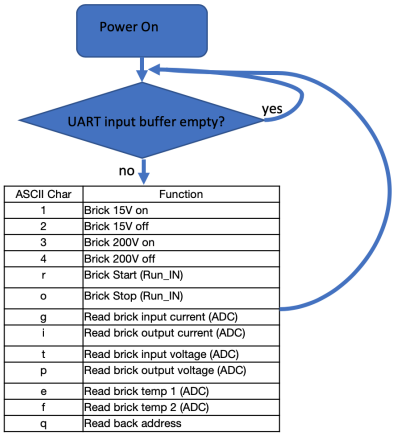
Figure 2.24: Burn-In: electronic load & and brick thermal management

2.5 Software

The creation and documentation of the software utilized within the electronics of the burn-in station, and in the central controlling PC are discussed in the next few sections.

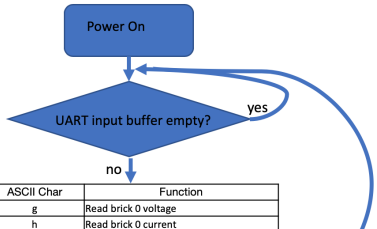
2.5.1 Embedded Software

The firmware of all the interface boards was written in embedded-C. A state machine was employed in both the brick interface board and the load interface board. Representative diagrams for each are displayed in Fig. 2.25 and Fig. 2.26.



ASCII Char	Function
1	Brick 15V on
2	Brick 15V off
3	Brick 200V on
4	Brick 200V off
r	Brick Start (Run_IN)
o	Brick Stop (Run_IN)
g	Read brick input current (ADC)
i	Read brick output current (ADC)
t	Read brick input voltage (ADC)
p	Read brick output voltage (ADC)
e	Read brick temp 1 (ADC)
f	Read brick temp 2 (ADC)
q	Read back address

Figure 2.25: Brick interface state machine diagram



ASCII Char	Function
g	Read brick 0 voltage
h	Read brick 0 current
i	Read brick 1 voltage
j	Read brick 1 current
k	Read brick 2 voltage
l	Read brick 2 current
m	Read brick 3 voltage
n	Read brick 3 current
z	Set load current brick 0
x	Set load current brick 1
c	Set load current brick 2
v	Set load current brick 3
q	Read back address

Figure 2.26: Load interface state machine diagram

2.5.2 Desktop Software

The central software on the PC, which communicates to all the interface boards and graphically displays and logs data points, was created in the LabView programming environment. Parts of legacy software at CERN was able to be recycled for the front panel graphics. A custom LabView driver was also created to communicate with the high voltage source via the VISA communications layer, over eathernet. The block diagram displaying the execuition path of the program is shown in Fig. 2.27.

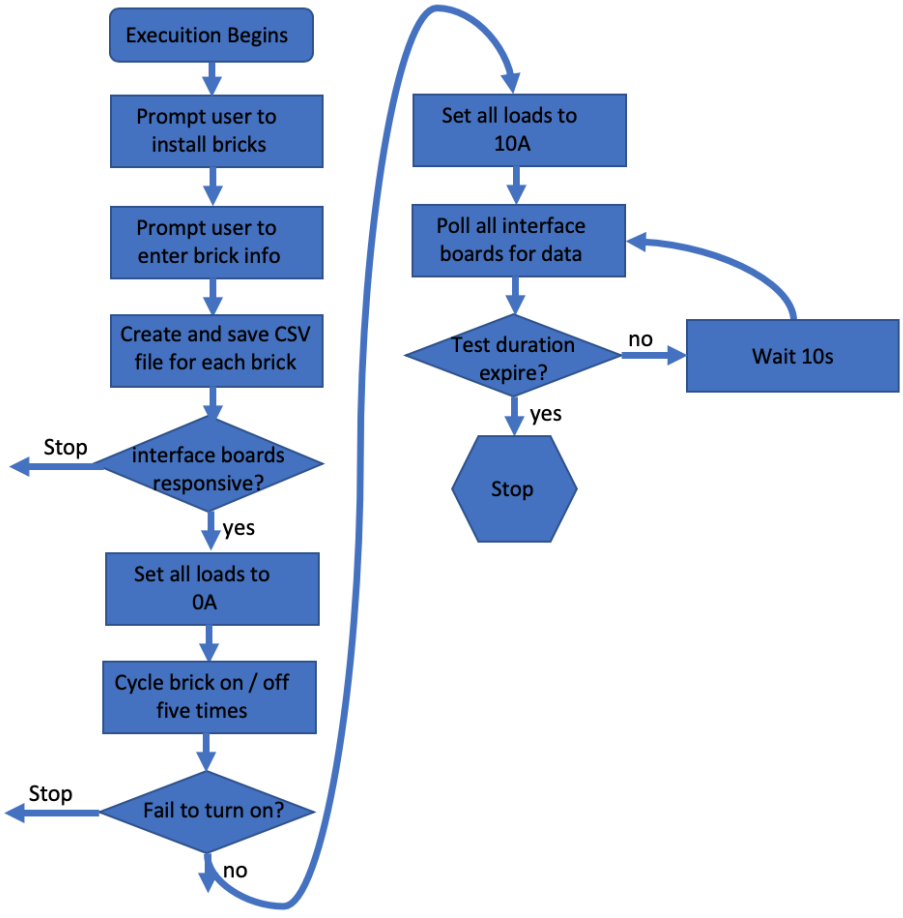


Figure 2.27: LabView Execution Diagram

A diagram displaying the front graphical panel of the LabView program is shown in Fig. 2.28. The front panel plots the efficiency and temperature of the brick in real time. The input and output voltages and currents are also displayed for each brick. The front panel panel also allows the user to halt the test at any time.

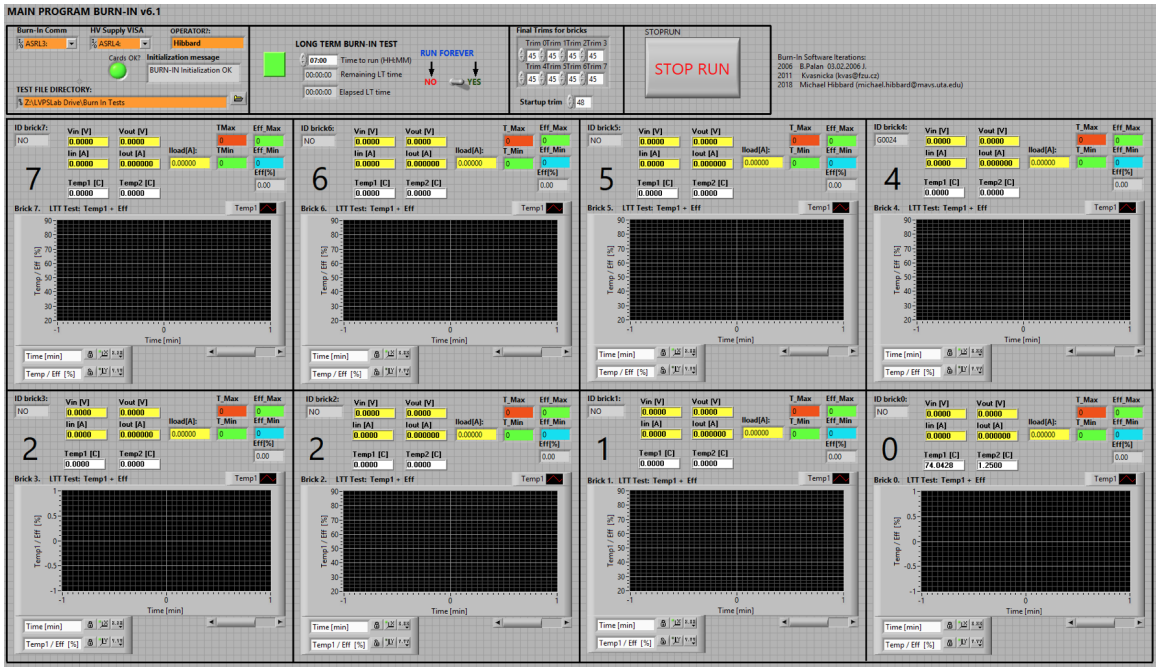


Figure 2.28: LabView desktop front panel read out

CHAPTER 3

BURN-IN STATION TEST RESULTS

3.1 Final Construction and Operation

Machining processes were performed on all of the heat sinks, angle aluminum and aluminum square columns. The assembly of the enclosure required a week to complete and few minor fitment issues were resolved. Fig. 3.2 shows the burn-in station fully assembled with the high voltage supply to the right.

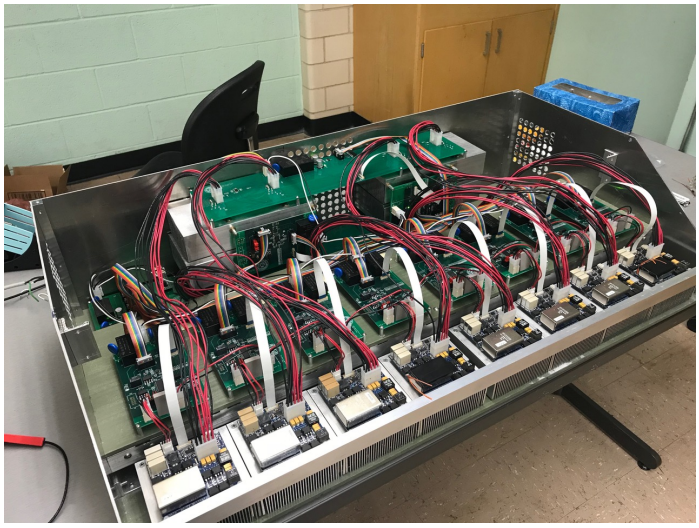


Figure 3.1: Completed and operational burn-in station (cover removed)

Assembly of the enclosure with all the electronics installed and wired inside the station is shown in Fig. 3.1. Here, the burn-in station is populated with eight bricks produced by UTA. The bricks were only retained in the lab long enough to debug all of the electronics of the burn-in station.

Figure 3.2: Completed and operational burn-in station (HV Supply shown to right)

Fig. 3.3 is a thermogram of one brick operating in the burn-in station. The brick is operating in steady state (full temperature reached) at near 75°C measured on the thermistor. The brick requires about 20 minutes of operation before it reaches its elevated temperature for the burn-in process.

Figure 3.3: One brick operating in burn in station

CHAPTER 4

CONCLUSION

The burn-in station will be used in the ATLAS experiment for the Low Voltage Power Supply bricks of TileCal to accelerate the age of the brick past their infancy period. The final produced burn-in station is capable of accelerating the aging of eight bricks at a time for any duration, typically six hours at a time. Custom software and hardware was design for the burn-in station to control and acquire data from the bricks, and to interface to the LabView program on the PC. Computational fluid dynamics was utilized for the sizing and integration of the heat sinks into the burn-in station. Sections of the LabView program were recycled form legacy software, but most of it was heavily modified to interface with the new electronics.

REFERENCES

[1] ATLAS collaboration, *Technical Design Report for the Phase-II Upgrade of the ATLAS Tile Calorimeter*. Hoboken, NJ: CERN-LHCC-2017-2019, 2011.

[2] Marty Brown, *Power Sources and Supplies World Class Designs*. Burlington, MA: Elsevier, 2008.

[3] Linear Technologies. (2001) Dual transistor synchronous forward controller. [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/1681f.pdf

[4] G.A. Klutke, P.C. Kiessler, M.A. Wortman, "A critical look at the bathtub curve," *IEEE Transactions On Reliability*, vol. 52, no. 1, pp. 125–129, 2003.

[5] National Instruments. (2001) Laboratory virtual instrument engineering workbench (labview). [Online]. Available: http://www.ni.com/en-us/shop/labview/labview-details.html

[6] Louis E. Frenzel Jr, *Serial Communications Interfaces, A Comprehensive Compendium of Serial Digital Input/Output (I/O) Standards*. Burlington, MA: Elsevier, 2016.

[7] FTDI. (2018) Ft232r - usb uart ic. [Online]. Available: https://www.ftdichip.com/Products/ICs/FT232R.htm

[8] Linear Technologies. (2018) Ltc2449. [Online]. Available: https://www.analog.com/en/products/ltc2449.html

[9] Theodore L. Bergman, Adrienne S. Lavine, *Fundaments of Heat and Mass Transfer, 7e*. Hoboken, NJ: John Wiley and Sons, 2011.

[10] Wakefield. (2018) Wakefield part number 122547. [Online]. Available: http://www.wakefield-vette.com/Portals/0/Short%20Length%20Thermal%20Extrusions/122547%20Thermal%20Extrusion.pdf

[11] Infineon. (2018) Irfp260npbf. [Online]. Available: https://www.infineon.com/dgdl/irfp260npbf.pdf?fileId=5546d462533600a401535628a2ef1fe4

[12] Jiyuan Tu, Guan Heng Yeoh, Chaoqun Liu, *Computational Fluid Dynamics A Practical Approach*. Burlington, MA: Elsevier, 2016.

[13] J. Tu, G. Yeoh, C Liu, *Concepts and Applications of Finite Element Analysis*. Hoboken, NJ: Wiley, 2001.

BIOGRAPHICAL STATEMENT

Michael Hibbard was born in North Texas in 1989. He completed his B.S. degree in Mechanical Engineering and later his M.S. in Electrical Engineering, both at the University of Texas at Arlington. While an undergraduate, Michael worked on the Formula SAE racing team at UTA, designing and developing a hybrid combustion-electric race car and an all wheel drive electric race car. While a graduate, Michael worked as a researcher in Dr. Hadavand's ATLAS group at UT Arlington under the guidance of Dr. Davoudi.