STUDY OF CONDUCTION BEHAVIOR IN DIELECTRICS IN CHIP LEVEL INTERCONNECTS:

DETECTION OF DEFECTS IN AL/SIO_2 INTERCONNECTS

by

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ABSTRACT

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DETECTION OF DEFECTS IN AL/SIO_2 INTERCONNECTS

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The University of Texas at Arlington, 2018

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This dissertation presents four different electrical measurement techniques to detect structural defects in Al/SiO_2 interconnects. These techniques, namely 1) polarity dependence measurement, 2) current voltage measurement, 3) two-point measurement and 4) discharge transient current measurement, can provide simple electrical parameters having direct relationship to defects state (type and quantity) in interconnect structure. All these measurement techniques use the MIM (metal-insulator-metal) structure such as the comb-serpentine structure commonly existing in integrated (IC) devices. This study also presents a newly discovered dielectric failure mechanism, that is the failure by a process of partial discharge dielectric breakdown phenomenon.

The goal of the charging polarity dependence measurement is to obtain a self-referenced parameter indicative of structural defect distribution in metal lines. Electrical bias from two opposite direction is applied to sample (one direction is refer to positive bias, while opposite direction is refer to negative bias) in sequence and resulting leakage current is measured. In an ideal situation where metal/dielectric interface is defect free,

the leakage current from both bias directions is expected to be identical because leakage current is proportional to electron injection area between metal and dielectric. With no defect, electron injection area from both electrodes are the same. However, if there exist defects in one side of metal line (either comb or serpentine side) more so than the other, electron injection area from both directions will be different, which will result in a net difference in leakage current. Based on this principal, by measuring leakage current difference under different bias direction, uneven distribution of interface defects can be characterized. This measurement can be extended to quantify the interface defect density, more specifically the voids in metal line, by conducting I-V measurement and comparing the forward and reverse current. The voids have two effects. Firstly, it reduces the interface area where electron injection occurs. Hence, injection of electron from this interface makes the leakage current to be smaller. On the other hand, since the void increases the local electrical field, it enhances the electron injection and thus current. Our study finds that the first effect is dominant when the field is low and the latter is more dominant when the field is high. Therefore, IV characteristics of the forward and reverse current shows that the interface with defect produces lower current (than the other direction) at low filed while the opposite happens when the field is high.

As for discharge transient current measurement, it gives a simple parameter that indicates the amount of structural defects in dielectric layer. Source of transient current observed in the research is likely impurities trapped in dielectric during deposition process. Upon bias, impurities are ionized and become mobile ions drifting in the direction of field to reach steady state (full polarization). When electric field is removed

(short to ground) during discharging process, mobile ions return to equilibrium and generate discharge transient current. If there exist structural defects in dielectric, ion migration is hindered, resulting in a smaller amount of ion drift and thus the transient current. It is therefore reasonable to relate the total amount of transient charge (Q) to the defect density in dielectric layers. Our study confirms that there exists such a relation and that Q can be used as an indicating parameter for TDDB (time dependent dielectric breakdown) reliability of the dielectrics.

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INTRODUCTION

1.1 Research Motivation and Achievements

Al/SiO_2 interconnect has been used widely in IC devices due to its low resistivity, excellent adhesion between metal lines/dielectrics and easy deposition process. As interconnects continues to scale down, achieving defect-free interconnects is increasingly difficult, becoming of a major concern. Defects in interconnect can be created during interconnect processes but also can develop at use condition by processes like electromigration, stress migration, time dependent dielectric breakdown, and a few others. Regardless of the processes, defects in either metals or dielectrics lead to a device failure and need to be eliminated or reduced.

Equally challenging to integrating interconnects without defect is their detection when they are present in either metal lines or dielectrics. In IC industry, conventional methods of detecting defect in interconnect are microscopic detections and electrical measurements. The advantage of SEM and TEM detections is that number of defects per area can be calculated and used as a parameter to determine the quality of interconnects. However, it is time inefficient, resource consuming and, most importantly, destructive to test devices. The advantage of electrical measurements are their simplicity and time efficiency. However, electrical measurement done by industry such as pattern capacitance and voltage ramp are influenced by many factors other than the defects, making the measurements to be prone to error in terms of detecting defects under

concern. Furthermore, electrical measurement is insensitive to defects in Al/SiO_2 interconnects, often yielding very weak or no relationship between electrical parameter and defects in interconnects.

The objective of this research is to find alternative electrical detection methods that provide simple electrical parameters which have a direct relationship to defects in interconnects. Therefore, several types of electrical measurement techniques including polarity dependence measurement, current-voltage curve (I-V curve) measurement, two-point measurement and discharge transient current measurement are proposed and their capabilities to detect defects in interconnects are developed in this study.

In this research, several measurement techniques are proposed and studied, and found a few electrical parameters indicative of defects in Al/SiO_2 interconnects, which is far more sensitive than the conventional techniques. Specifically, polarity dependence of the leakage current is found to be effective in revealing voids in Al metal lines. In case of I-V curve measurement with polarity change in bias, it is found to be very sensitive to structural defects (voids) in Al metal lines. We simplified the IV method to make it to be more practical by taking two-point leakage current as a parameter. Although the parameter does not reveal much about the physics behind the condition in given structure and materials, it does provide a simple parameter that can be used for detection of voids in metal lines. Our study also finds that structural defects in dielectrics can be characterized by the use of the discharge transient current measurement. The total stored charge developed during charging state can be measured accurately during

discharging process and the total charge (Q) is found to be extremely sensitive to defects locating in SiO_2 dielectrics.

In order to shed light on the physics behind our techniques, background information related to Al/SiO_2 interconnects structure/processing, defects and conduction mechanism are briefly introduced in this chapter. What is also discussed is the pros and cons of the conventional characterization techniques used in IC industries.

1.2 Technology of Al/SiO_2 Interconnects

1.2.1 Al/SiO_2 Interconnects

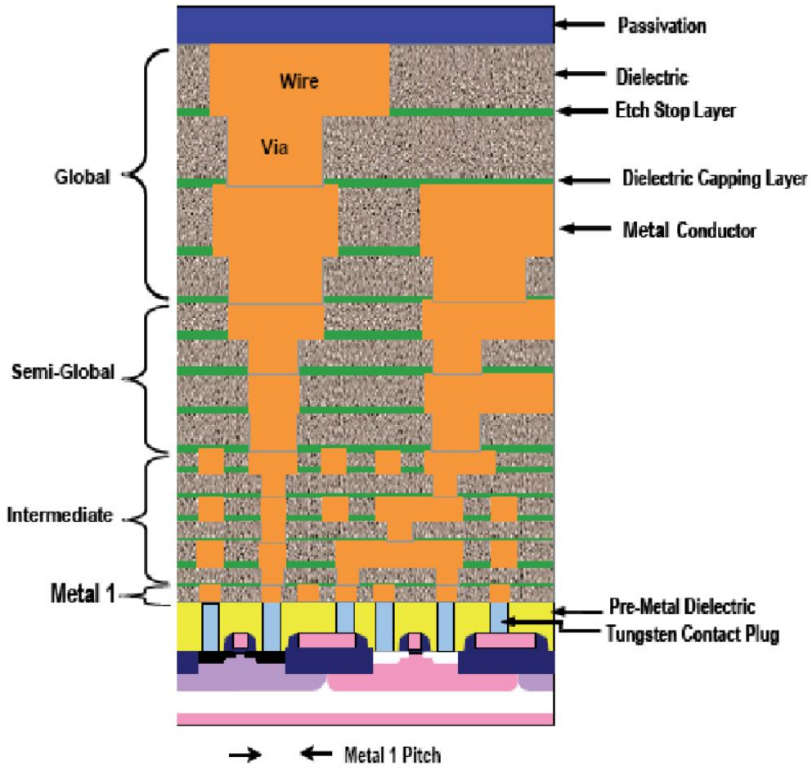

Figure 1.1 Typical cross-section of interconnect structure in IC chip [1]

IC (integrated circuit) chip is made of a set of compact electronic devices (transistor, resistor, capacitor, etc.) that are interconnected and located on semiconductor substrate. Therefore, interconnects refer to wires that connect each electronic devices in a chip. Conventional interconnects consists of Al as metal lines and SiO_2 as inter/intra layer dielectrics. Al/SiO_2 interconnect structure contains two essential parts: metal wires (Al-Cu alloy where Al is >97.5%, Cu is added to improve electromigration resistance [19,23]) that connect individual electronic devices and insulating dielectrics (SiO_2) that isolate and mechanically support metal wires. A typical interconnect structure is demonstrated in Figure 1.1.

There is a constant demand for IC device miniaturization because performance improvements depend on the size of the devices in a chip. Working speed of IC chip is essentially determined by the delay in two places: the gate of transistors and interconnects (by RC delay), as seen in Figure 1.2. When device size is large, gate delay is the dominant factor that affects the device operation speed. However, reduction in devices size makes the gate length to be smaller, results in the delay caused by the interconnect to be more dominant because it makes the resistance to increase in metal lines and capacitance to increase in dielectric layers [2]. To overcome RC delay limit, Cu/PLK interconnects have been developed and implemented to a few advanced devices like microprocessors [3-6]; yet majority of IC devices still use Al/SiO_2 interconnects [7] to take advantage of their superior reliability and processability.

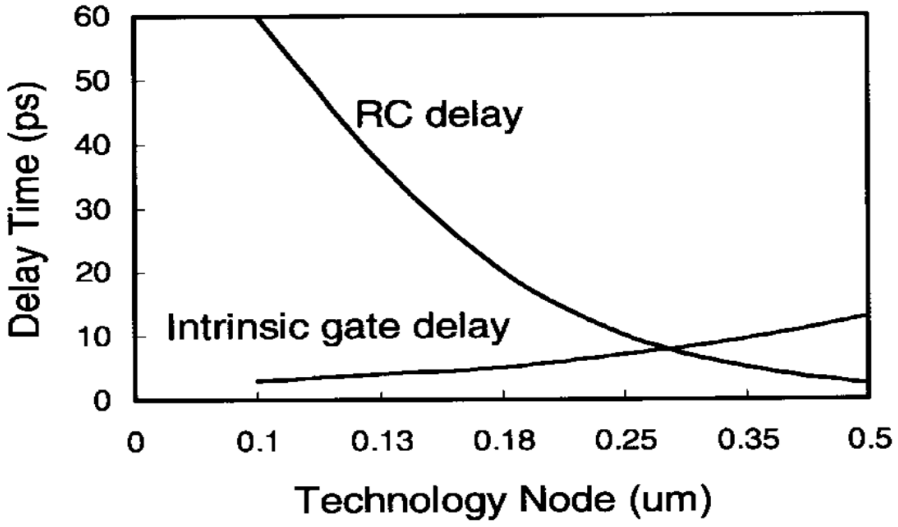

Figure 1.2 Gate delay versus interconnect RC delay [2]

1.2.2 Al/SiO_2 Interconnect Processing

There are three types of fabrication process in Al/SiO_2 metallization: cloisonné fabrication process [8], damascene fabrication process [9,10] and dual damascene fabrication process [11]. For cloisonné fabrication process and damascene fabrication process, vias and lines are fabricated separately, but for dual damascene fabrication process, vias and lines are fabricated through a single process.

Cloisonné fabrication process is the most common process used in Al/SiO_2 metallization. In the process, vias are fabricated first and lines are fabricated later. Figure 1.3 is a schematic of a typical cloisonné fabrication process. Process starts with SiO_2 depositing onto substrate through chemical vapor deposition (CVD) process (step 1).

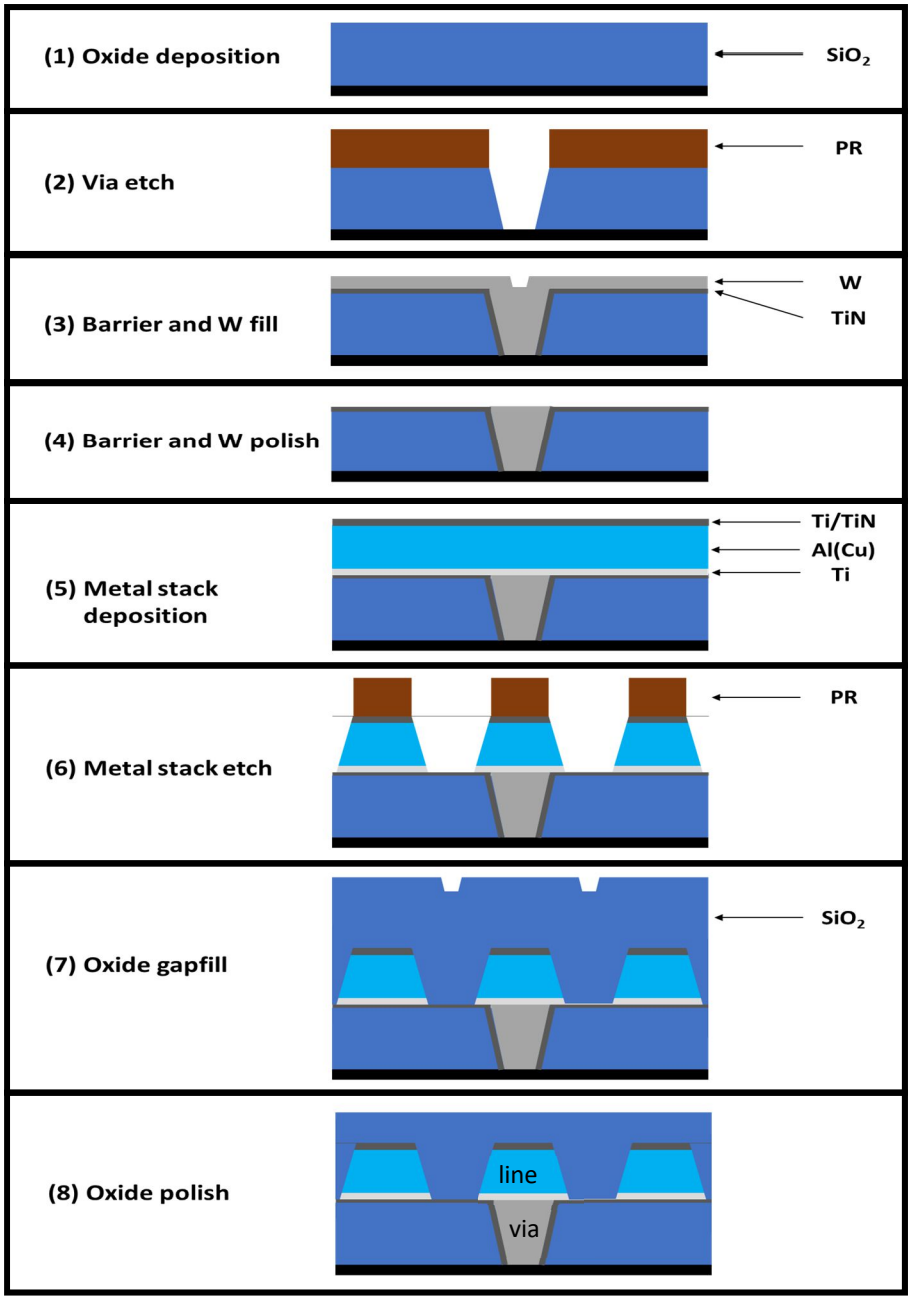

Figure 1.3 Schematic of cloisonné fabrication process

Then photoresist (PR) is coated onto oxide layer and patterned through lithography process. After that, area without PR is removed by reactive ion etching (RIE) process (step 2). Once trench of via is produced, PR is removed by cleaning process. Barrier layers like

(TiN) and Tungsten (W) are then deposited onto oxide layer through CVD process (step 3), followed by chemical mechanical polishing (CMP) process to result in via fabrication (step 4). After the via, Ti, Al and TiN (or Ti) are deposited by physical vapor deposition (PVD) or CVD process in sequence to create metal stack (step 5). The metal stack is then patterned with PR and etched through RIE process to create desired trench (step 6). After removal of PR, dielectric layer (SiO_2) is deposited through CVD process to isolate Al metal lines (step 7). After CMP planarization, lines are fabricated (step 8).

Damascene process is used to fabricate Cu/PLK interconnects [12]. In actuality, damascene process is initially developed for Al/SiO_2 interconnects and is still used in the industry. First step of the process is via fabrication and it is identical to cloisonné fabrication process. Second step of the process is line patterning. Figure 1.4 is the schematic of typical damascene process for line fabrication.

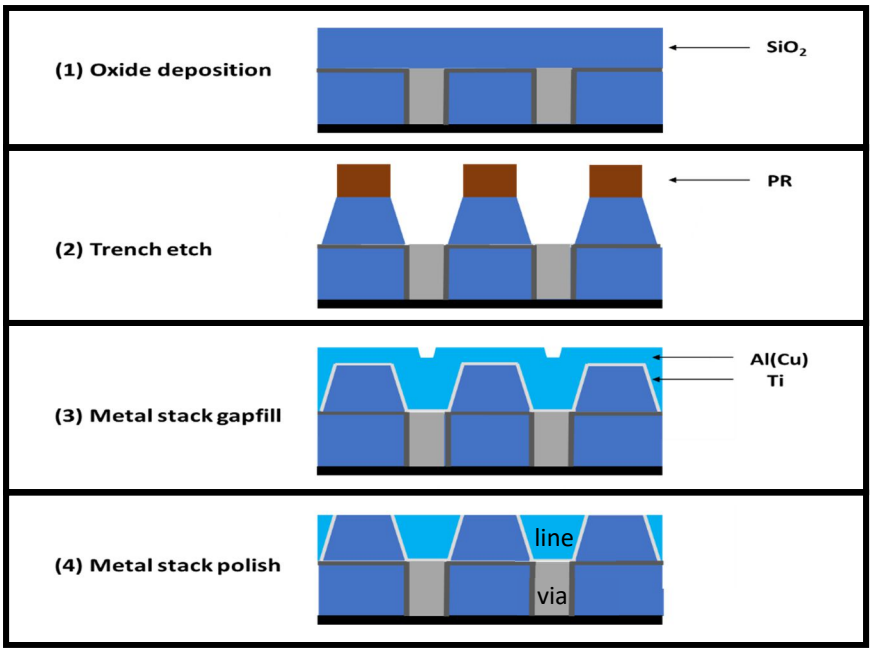

Figure 1.4 Schematic of damascene fabrication process for line

As is shown in Figure 1.4, the process starts with deposition of dielectric layer (SiO_2) through CVD process (step 1). Wafer is then patterned with PR through lithography process and etched by RIE process to create desire trench (step 2). It is then followed by the deposition of Ti and Al onto wafer by PVD or CVD process in sequence (step 3). After CMP planarization, Al metal lines are created (step 4).

As is previously discussed, cloisonné and damascene process require approximately the same number of steps to fabricate a planar interconnect level. Therefore, the cost of both processes does not show significant difference. However, cost of damascene process can be further reduced by the improved procedure known as the dual damascene which vias and lines are fabricated in a single step. Figure 1.5 shows the typical trench-first dual damascene fabrication process.

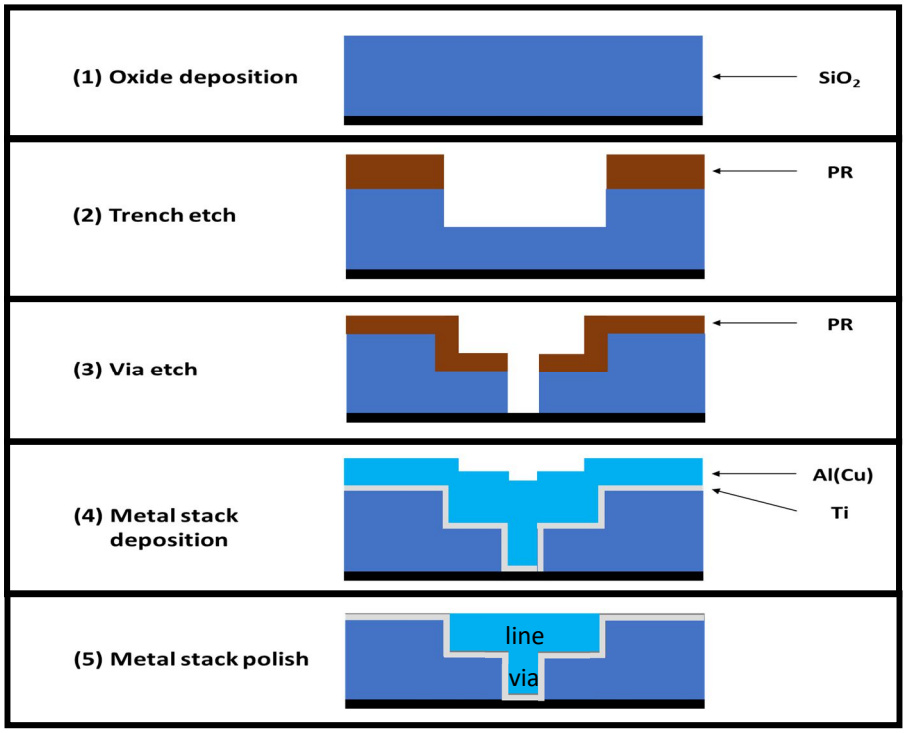

Figure 1.5 Schematic of trench-first dual damascene fabrication process

According to Figure 1.5, first step is to deposit oxide layer onto substrate (step 1). Wafer is then patterned with PR through photolithography process and etched by RIE process to create trench for metal line (step 2). Once trench is formed, another set of PR is patterned onto wafer and trench of via is produced by RIE etching (step 3). Deposition of Ti and Al by PVD or CVD in sequence complete the metal layer process (step 4). After CMP, via and line are fabricated (step 5).

1.3 Common Failure Mechanisms Seen in Al/SiO_2 Interconnects

As size of interconnects is scaling down to increase the performance of IC chips, defects in interconnects has become a major reliability concern in industry. Defects in interconnect can result from different mechanisms but can be categorized into two. The first is process related such as trapping voids and cracking. The second is the defects developed at use condition that includes the mechanism like electromigration in metal lines, stress migration induced voiding in metal lines, time dependent dielectric breakdown in dielectrics. These defects reduce the lifetime of interconnects and limit the reliability of the IC devices. Some of the common failure mechanisms seen in Al/SiO_2 interconnects are briefly introduced in this section.

1.3.1 Cracking

Cracking is one of the common failure mechanisms seen in interconnects and is known to result in delamination of capping layer and Al/SiO_2 interconnects [13] or facture of SiO_2 dielectric [14]. Capping layer (usually SiN) refers to the protective layer deposited

on top of interconnects to protect them from the environment. Crack can initiate at the flaws in capping layer thin film or SiO_2 dielectric and propagate through metal/dielectric interfaces (delamination) or dielectrics (cracks). This process is driven by thermal expansion mismatch in materials in the structure. There are three cracking modes [15,16]. Mode I crack is also known as the crack opening mode where a tensile stress normal to the plane of crack is applied. Mode II cracking is also known as the in-plane shear mode where a shear stress is parallel to the plane of crack and perpendicular to crack tip. Mode III cracking, also known as out-of-plane shear mode, occurs by a shear stress that is parallel to the plane of crack and crack tip. Among all different crack modes, mode I is

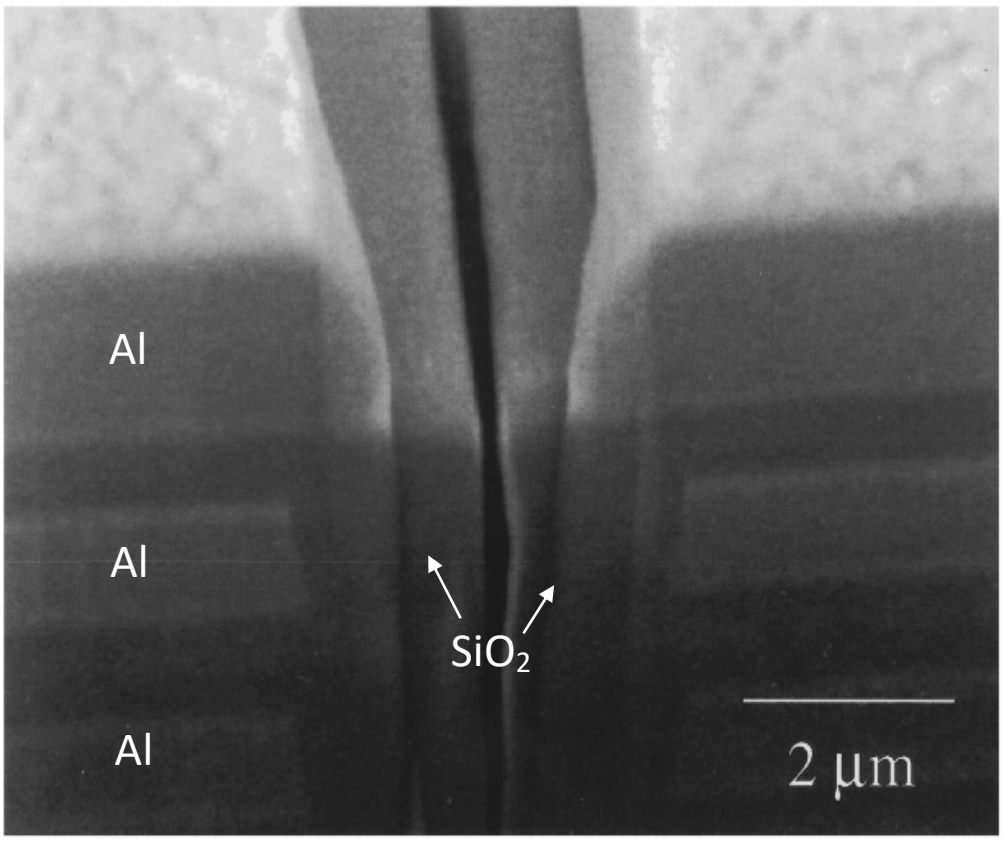

Figure 1.6 SEM image of Al/SiO2 interconnect with crack propagating inside dielectric [14]

most commonly seen in interconnects [13] and Figure 1.6 is a SEM image of Al/SiO_2 interconnect with crack propagating inside SiO_2 dielectric.

1.3.2 Electromigration

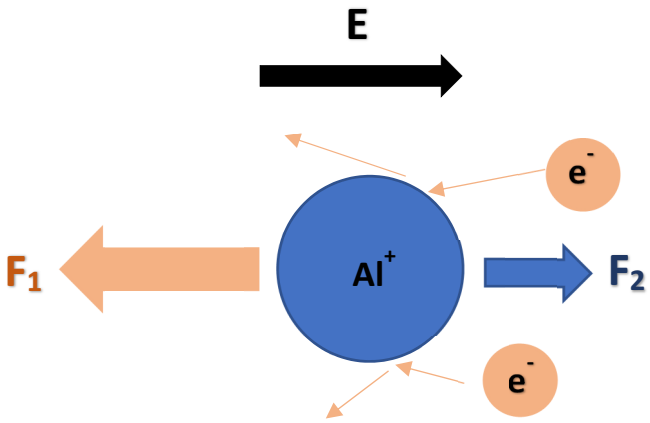

Figure 1.7 Schematic of electromigration

Electromigration (EM) is a phenomenon which metal ions are migrating towards opposite direction of applied electric field due to collision with electrons flowing inside metal lines [17-21] and Figure 1.7 is a schematic of electromigration in Al metal lines. As indicated by Figure 1.7, Al ions are subjected to two opposite driving forces (F_1 and F_2). F_1 is created by momentum transfer between electrons and Al ions. This force is known as wind force with same direction to electron flow. F_2 is created by effect of external electric field on Al ions. This force is known as field force with direction opposite to electron flow. When current density is high enough (10^5~10^6 A/cm^2) [22], F_1 is much larger than F_2 and Al ions will move in same direction as electron flow. Therefore, EM can be considered as a diffusion induced by wind force and diffusion flux of EM is governed by equation

$$J = \frac{D*C}{k*T} * z * e * \rho * j \qquad (1)$$

First part of equation (1) governs kinetics where *D* is diffusion coefficient, *C* is concentration, *k* is Boltzmann constant and *T* is temperature. Second part of the equation (1) governs driving force where *z* is effective valence, *e* is electron charge, ρ is flux density and *j* is current density.

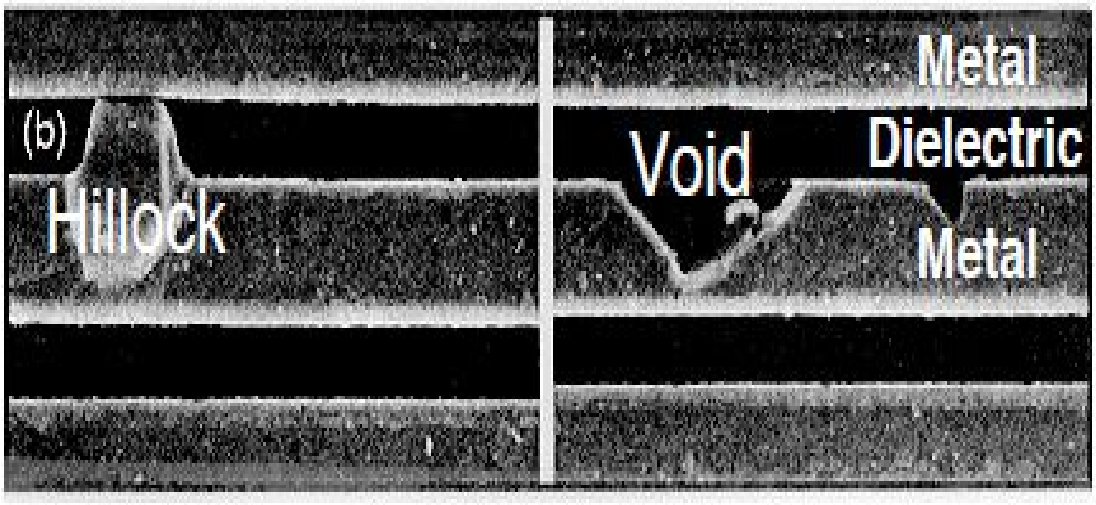

Figure 1.8 Hillock/voids in metal line due to EM [7]

In Al/SiO_2 interconnects, during electromigration, Al ions will migrate towards direction of electron flow and accumulate at anode. Therefore, hillocks will grow on anode side and voids will develop on cathode side, as seen in Figure 1.8. Since hillocks are deposition of conductive Al atoms, development of hillocks will lead to short circuit between different metal wires. Voids are empty spaces that are lacking atoms and do not conduct electric current. Therefore, as voids develop, cross-section of conduction path is reduced and this will increase current density and joule heat created by current. This will further accelerate growth rate of voids and eventually lead to open circuit of metal wires.

In either case, EM will decrease reliability of Al/SiO_2 interconnects and mean time to failure (MTTF) is govern by equation [20,21]

$$MTTF = \frac{A}{j^n} * \exp\left(\frac{E_a}{k*T}\right) \qquad (2)$$

where *A* is a constant that is related to properties and geometry of metal lines, *j* is current density, *n* is current exponent, E_a is activation energy, *k* is Boltzmann constant and *T* is temperature.

1.3.3 Stress Induced Voiding

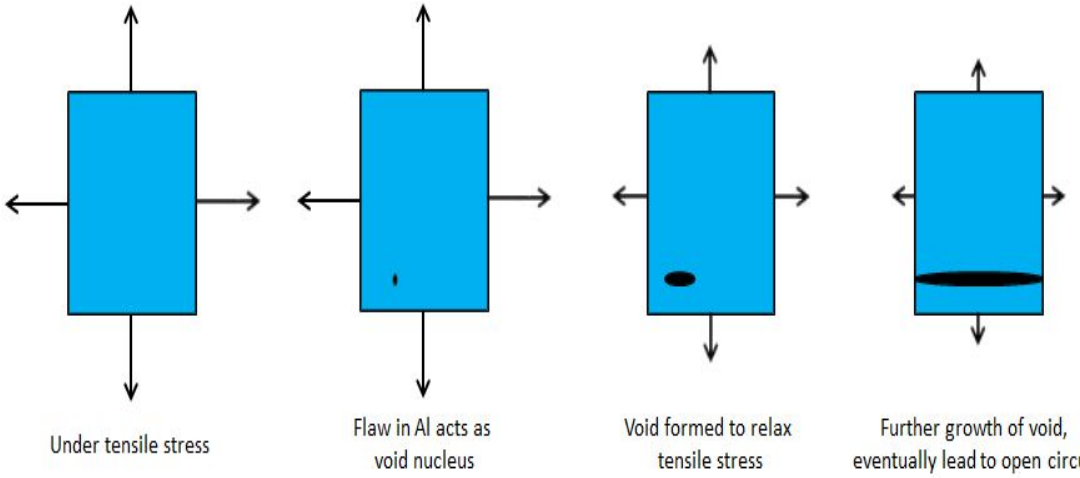

Figure 1.9 Schematic of void developed by stress migration in Al line

In 1980s, in order to further scale down interconnects to improve performance, narrow Al lines with line width comparable to line thickness were introduced. Soon it was discovered that voids can develop in wafers that were put in oven at high temperature, or even on shelves at room temperature [24-26]. This void formation mechanism is

known as stress induced voiding or stress migration. As Al line width and line thickness decreased, stress induced voiding will occur more easily.

Basic mechanism of stress induced voiding is related to the difference in coefficient of thermal expansion (CTE) between metal lines and surrounding dielectric materials [27-31]. For Al/SiO_2 interconnect, aluminum line has a much larger CTE than SiO_2. During fabrication of lines, aluminum lines are encapsulated in dielectrics at high temperature. This temperature is known as stress free temperature because there is no stress associated with Al lines and surrounding dielectrics. After cooling down to room temperature, due to huge CTE misfit of Al and SiO_2, Al lines are subjected to a triaxial tensile stress that is larger than yield strength of Al. However, under uniform tension, aluminum lines are in equilibrium state and no atom diffusion will occur. But if any flaw exists in aluminum line, it can serve as void nucleus. Since stress around nucleus is lower, aluminum atom will diffuse away from nucleus. Therefore, by growing the void, tensile stress can be relaxed (as shown in Figure 1.9).

There are two factors that can affect the speed of void formation and the size of voids. The first factor is the tensile stress that is proportional to difference between operating temperature T and stress free temperature T_0. As discussed in previous paragraph, due to CTE mismatch of metal lines and dielectrics, lower operating temperature will create to a higher CTE mismatch, which leads to higher tensile stress for Al lines. The second factor is diffusivity of atoms, which is proportional to operating temperature. Atomic diffusivity *D* is governed by equation

$$D = D_0 * \exp\left(\frac{-E_a}{kT}\right) \qquad (3)$$

where D_0 is temperature independent preexponential, E_a is activation energy for diffusion, k is Boltzmann's constant and T is temperature.

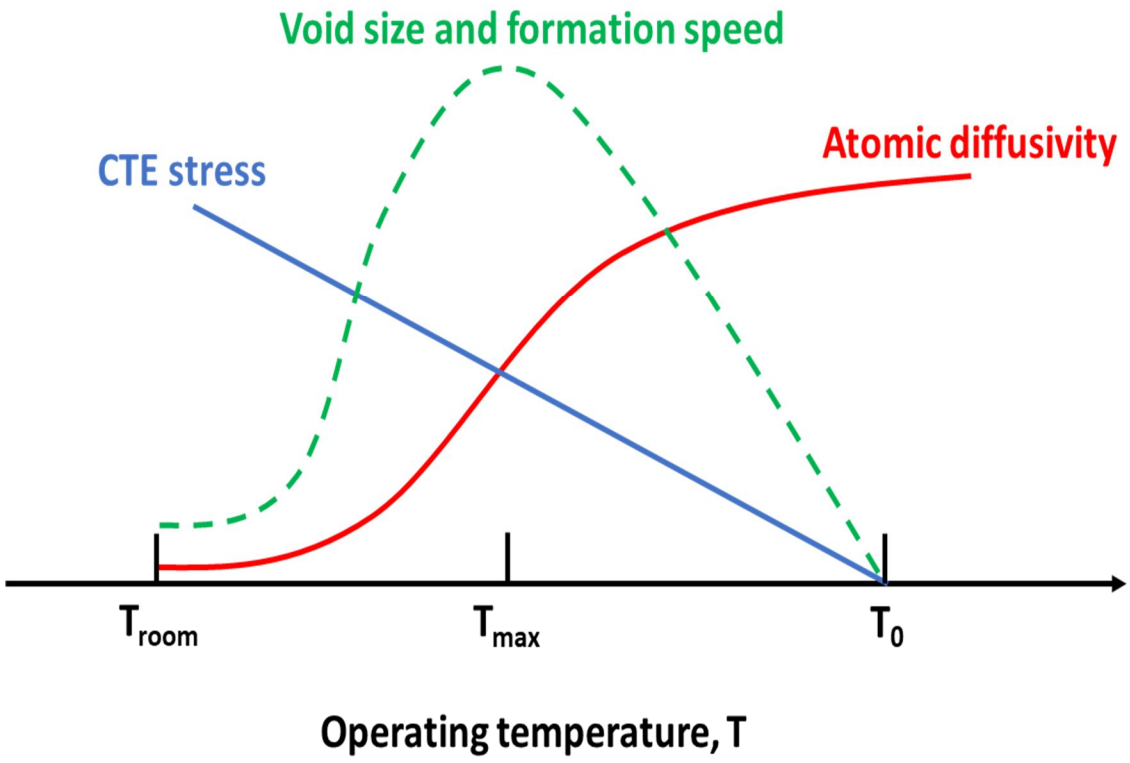

Figure 1.10 Schematic of temperature effect on void size and void formation speed [13]

Figure 1.10 is a schematic that represents relationship between operating temperature and the two factors that are affecting void size and formation speed. Figure 1.10 indicates that these two factors are working against each other, CTE stress decreases as operating temperature increases and atomic diffusivity increases when temperature decreases. However, there is a middle point (150°C to 200°C) where void size and formation speed can reach their maximum value.

Conventional method used to monitor stress induced voiding activity is to measure the electrical resistances of metal lines as a function of time. Failing criterial is set to be 20% increase in resistance compares to time zero value. Median time to failure (MTF) of stress induced voiding is then governed by equation [32]

$$MTF = \frac{C}{(T_0 - T)^N} * \exp\left(\frac{E_a}{kT}\right) \qquad (4)$$

where *MTF* refers to average time needed for half of the test wafers to fail, *C* and *N* are fitting parameters, T_0 is stress free temperature, T is operating temperature, E_a is activation energy and k is Boltzmann's constant.

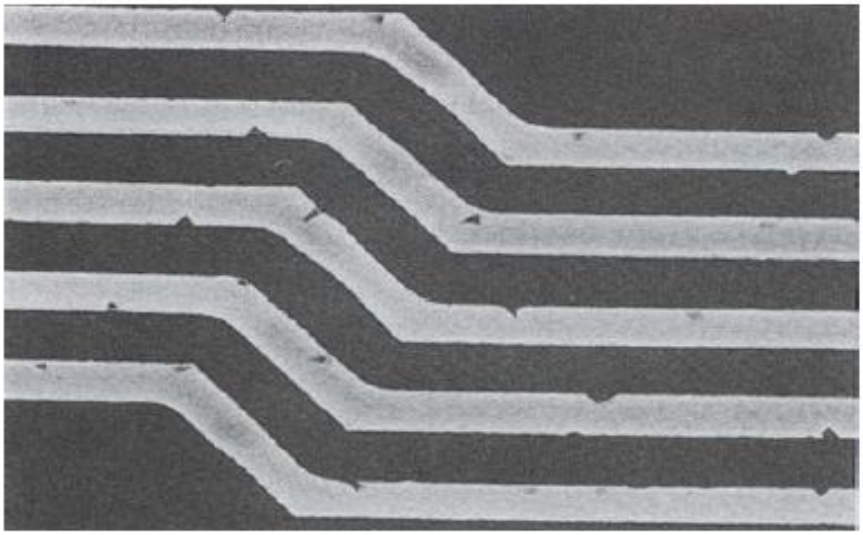

Figure 1.11 SEM image of interconnect with stress induced voids [32]

Figure 1.11 is the SEM image of an interconnect that is in the early stage of stress induced voiding activity. As voids further develop, metal lines will be discontinued and interconnect will experience open circuit failure. However, stress induced voiding activity can be mitigated by several methods that were originally developed to improve EM failure

resistance. First method is to add tiny amount of Cu into Al to from Al-Cu alloy, it is reported that by doing so, diffusion rate of Al atoms can be reduced by two orders of magnitude [19]. Second method is to implement materials with low diffusivity, such as W and TiN, into the interconnects as adhesion layer between metal lines and dielectrics [33]. If metal lines are opened due to voids, these materials can act as shunts and still conduct electric current (Figure 1.12). Third method is to replace long Al lines with short Al lines. Since volume of metal lines that needs to be relaxed is reduce, stress migration effect is less severe [34].

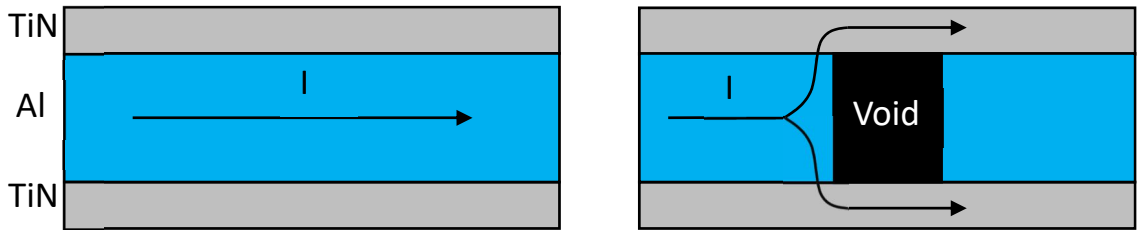

Figure 1.12 Schematic of TiN acting as shunts to prevent open circuit of Al metal line

1.3.4 Time Dependent Dielectric Breakdown

Time dependent dielectric breakdown (TDDB) refers to the breakdown that occurs after a long-time application of relatively low electric field (lower than dielectric strength of materials) due to the degradation of dielectric overtime [35-39]. Initially, TDDB is a phenomenon mostly seen in front-end-of-line transistors due to high electric field associated with thin gate oxides. However, as integrated circuit continue to scale down, electric field across interconnect has greatly increased and TDDB has become major concern in back-end-of-line interconnects as well.

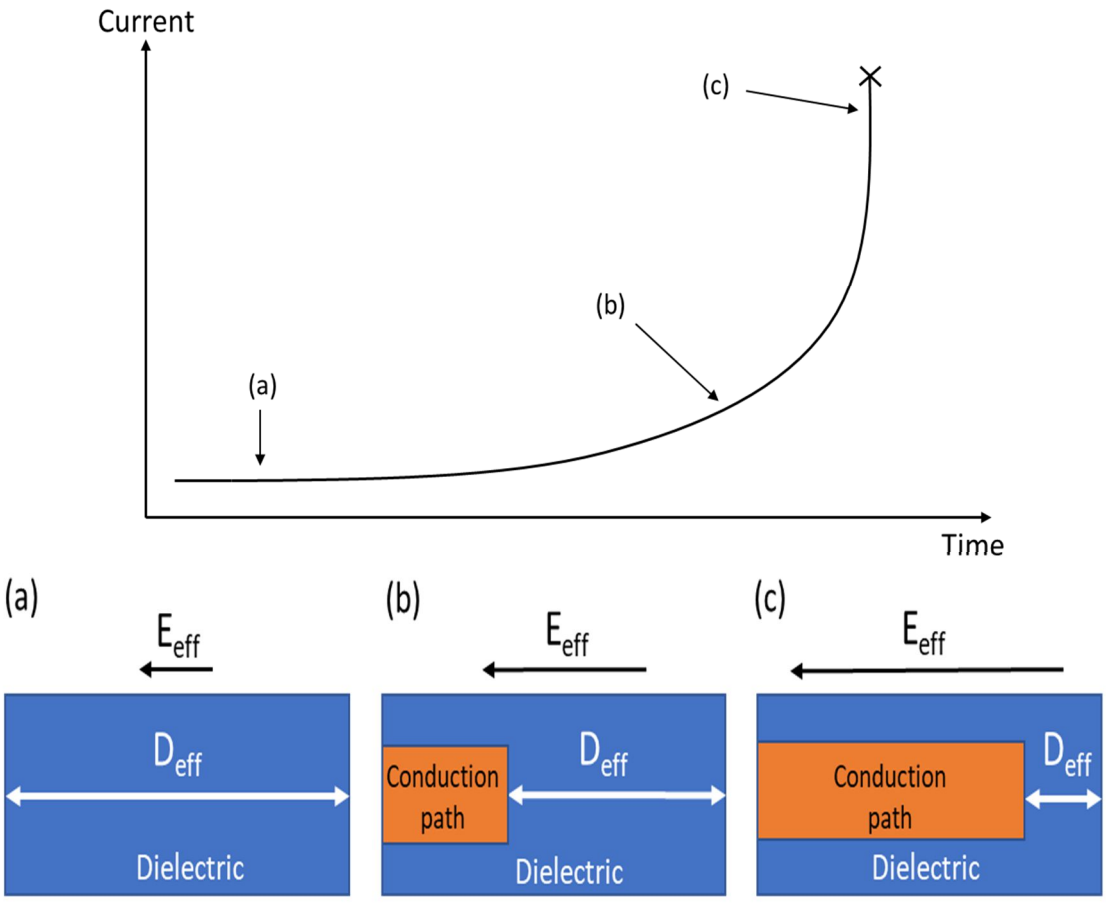

Figure 1.13 Schematic of a typical TDDB failure

Figure 1.13 is the schematic of a typical TDDB failure. In the figure, leakage current of dielectric is plotted as function of operation time. Based on leakage current, TDDB development can be divided into three stages: (a) early stage (b) short circuit development stage (c) final breakdown stage. Initially, SiO_2 dielectric is intact and effective dielectric width D_{eff} is equal to dielectric width D (Figure 1.13a). At this stage, leakage current does not vary with operation time. However, after operated for a long time, part of dielectric starts to degrade and lose its insulating properties. Therefore, a conduction path starts to form inside dielectric and D_{eff} is reduced. Since electric field

equals to voltage divided by width, with D_{eff} reduced, E_{eff} is increased and leakage current increases (Figure 1.13b). As dielectric degrades over time, conduction path is further elongated and leakage current continue to increase until a critical point where E_{eff} is larger than dielectric strength of SiO_2 and dielectric breakdown will occur, resulting in a spike increase of leakage current (Figure 1.13c). To understand and prevent TDDB, source of dielectric degradation has to be investigated. Several different mechanisms had been proposed to explain the phenomenon of dielectric degradation and these mechanisms will be discussed in chapter 4.

1.4 Conventional Defect Detection Methods

1.4.1 Line Resistance Measurement

Line resistance measurement is a common technique used to evaluate stress induced voiding and electro migration void formation. Resistance of metal lines is monitored during operation and if resistance is increased by 20% compares to its original value, metal line is considered as failure. Advantage of this technique is its simplicity. However, this technique is not very sensitive to defects as measured resistance is an average value of the whole metal line but no only the area that contains voids.

1.4.2 Voltage Ramp Test

Voltage ramp test is conducted by the industry as it reveals dielectric properties through measurement of breakdown voltage. As indicated by Figure 1.14, basic

procedure is to apply voltage to sample for certain amount of time, then increase voltage step by step until sample breaks down. The applied voltage that breaks the sample is known as breakdown voltage and it is proportional to the physical properties of dielectrics [40]. However, there are many factors that contribute to breakdown voltage, which makes it insensitive to structural defect in dielectric

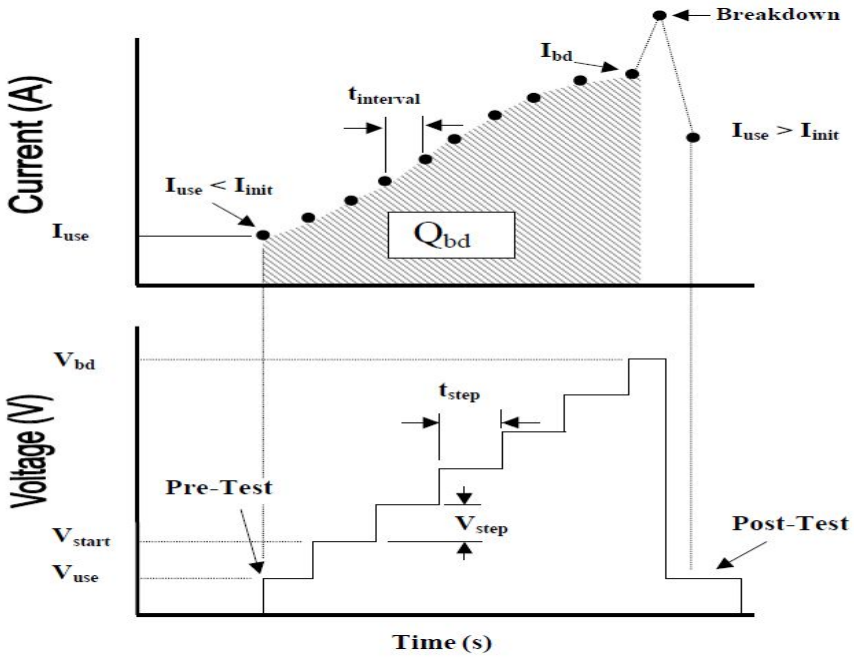

Figure 1.14 Schematic of voltage ramp test [40]

1.4.3 Scanning Electron Microscope Inspection

Scanning electron microscope (SEM) inspection can reveal the quality of interconnects. There are two types of SEM inspections: top-down view SEM and cross-section view SEM. Figure 1.15 is a schematic of both SEM inspections. Based on SEM view direction, either capping layer (top down view) or excessive interconnect (cross

section view) needs to be removed. It can be done through chemical etching, focus ion beam etching, ion milling, chemical mechanical polishing, etc.

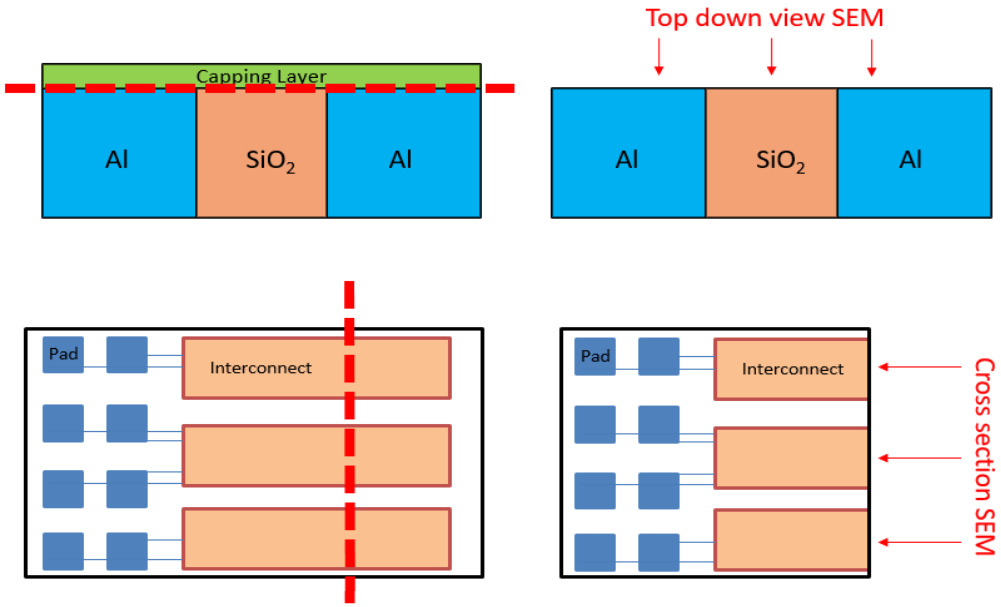

Figure 1.15 Schematic of top-down view and cross-section view SEM inspection

Top-down view SEM images gives better overview of defect distribution in single metal layer while cross-section view SEM images can show multiple metal layers simultaneously (Figure 1.16 and 1.17). Despite all the advantages that SEM inspection has, it is a destructive and time-consuming technique.

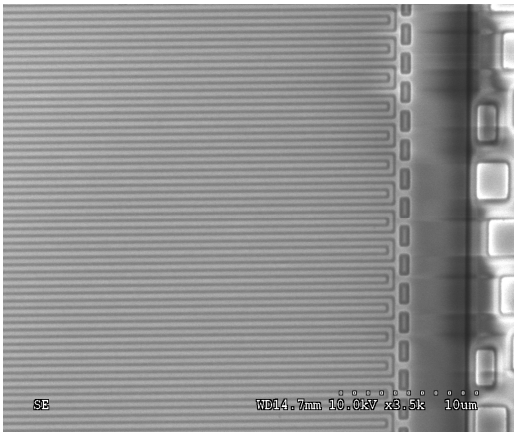

Figure 1.16 Top-down view SEM of Al/SiO_2 interconnect

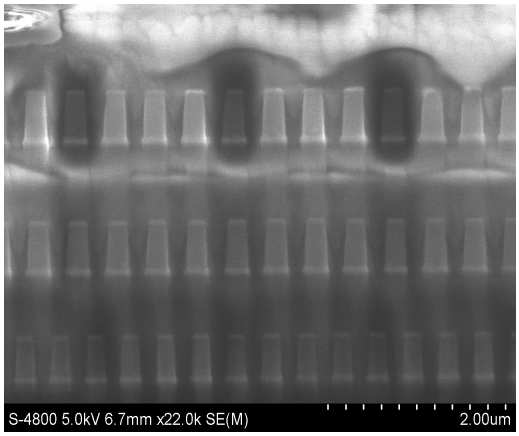

Figure 1.17 Cross-section view SEM of Al/SiO_2 interconnect

CHAPTER 2

POLARITY DEPENDENCE MEASUREMENT AND ITS SENSITIVITY TO STRUCTURAL DEFECTS IN ALUMINUM LINES OF AL/SIO_2 INTERCONNECTS

2.1 Background

The purpose of this measurement technique is to provide a self-reference parameter (*polarity difference*) that can be used to determine defect distribution in metal line (Figure 2.1). This detection technique is based on measuring leakage current of dielectrics under electric field. Leakage current refers to current that flows through insulating dielectrics under applied electric field due to different conduction mechanisms. Samples with and without defect are expected to show different level of leakage current

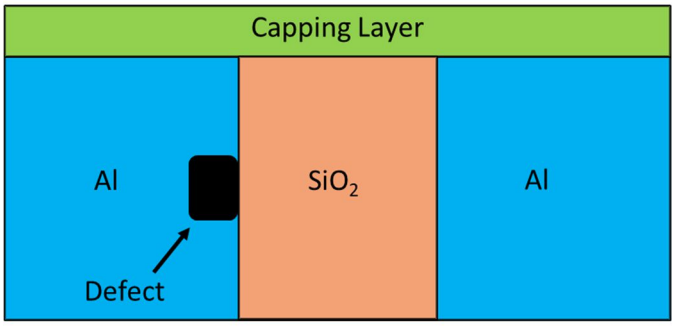

Figure 2.1 Schematic of defect in metal line at metal/dielectric interface from cross section view

Based on how current is transported, conduction mechanism can be divided into two categories: bulk-limited conduction mechanisms and electrode-limited conduction mechanisms [41-50]. If current transportation is determined by properties of dielectric bulk, the conduction mechanism is bulk controlled. If current transportation is determined by properties of metal/dielectric interface, the conduction mechanism is

electrode controlled. Figure 2.2 shows typical conduction mechanisms under different categories.

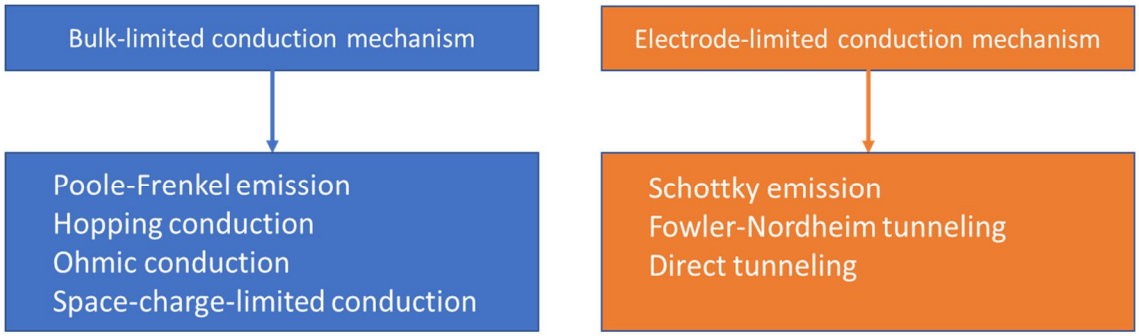

Figure 2.2 Classification of conduction mechanisms in dielectric

Since this measurement technique are focusing on detecting defects at interface of metal/dielectric, bulk-limited conduction mechanisms are considered to have similar effect on samples with/without defect at interface as intrinsic dielectric properties of samples should be the same. Therefore, in this measurement technique, electrode-limited conduction mechanisms are much more important and the conduction mechanism that is major contributor to leakage current must be determined.

2.1.1 Schottky Emission

Schottky emission occurs when electron obtains enough energy through thermal activation to overcome potential barrier at metal/dielectric interface and emits into dielectric [51, 62]. Besides electron obtaining enough energy to overcome potential barrier, barrier height can also be reduced by image force. When electron in dielectric is close to metal/dielectric interface, it will sense an electrostatic field that acts as if an equal but opposite charge is locating at metal side of metal/dielectric interface at mirror image

position. Electron and its image charge will attract each other and reduce potential barrier height, which will allow more electron to overcome barrier. Therefore, there are three factors that will strongly affect current density of Schottky emission: potential barrier height of metal/dielectric interface, applied electric field and temperature. Figure 2.3 is a schematic of Schottky emission at metal/insulator interface. The difference in Fermi level of two metals is due to applied electric field.

Current density of Schottky emission is [52-54]

$$J = A^* T^2 \exp\left[\frac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0}\right)}{kT}\right] \quad (5)$$

$$A^* = \frac{4\pi q k^2 m^*}{h^3} = \frac{120 m^*}{m_0} \quad (6)$$

where J is current density, A^* is effective Richardson constant, m_0 is free electron mass, m^* is effective electron mass in dielectric, T is absolute temperature, q is electron charge, $q\emptyset_B$ is barrier height, k is Boltzmann's factor, h is Planck's constant, ε_0 is permittivity in vacuum, ε_r is optical dielectric constant and E is electric field across dielectric.

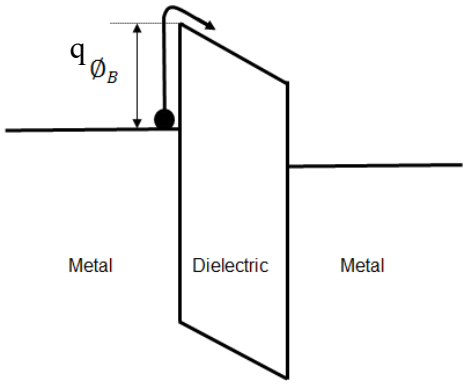

Figure 2.3 Schematic of Schottky emission

2.1.2 Fowler-Nordheim Tunneling

F-N tunneling occurs when electron penetrates energy barrier at metal/dielectric interface even if it does not have sufficient energy [55,59-61]. According to quantum physics, even if electron does not have enough energy to overcome potential barrier, it still has a chance to penetrate the triangular area of potential barrier created by high electric field [56]. The most impactful factor in F-N tunneling is applied electric field while temperature has little effect. Typical electric field for F-N tunneling to occur is >2MV/cm [57]. Figure 2.4 is a schematic of F-N tunneling.

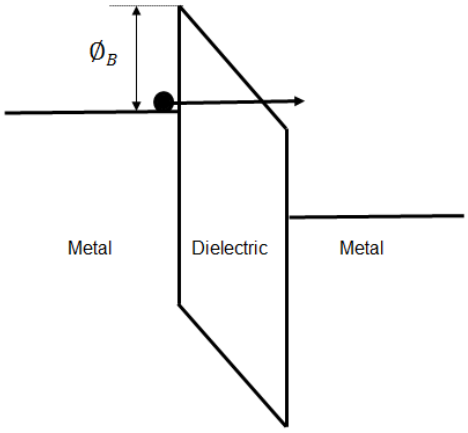

Figure 2.4 Schematic of Fowler-Nordheim emission

Current density is of F-N tunneling is [52]

$$J = \frac{q^3 E^2}{8\pi h q \phi_B} \exp\left[\frac{-8\pi(2qm_T^*)^{1/2}}{3hE}\phi_B^{3/2}\right] \qquad (7)$$

where J is current density, q is electron charge, $q\emptyset_B$ is barrier height, h is Planck's constant and E is electric field across dielectric.

2.1.3 Direct Tunneling

Direct tunneling is another tunneling mechanism which electron penetrates through rectangular area of potential barrier directly. It happens when dielectric width is extremely narrow (<3.5nm for SiO_2 dielectric) [52]. Figure 2.4 is a schematic of direct tunneling.

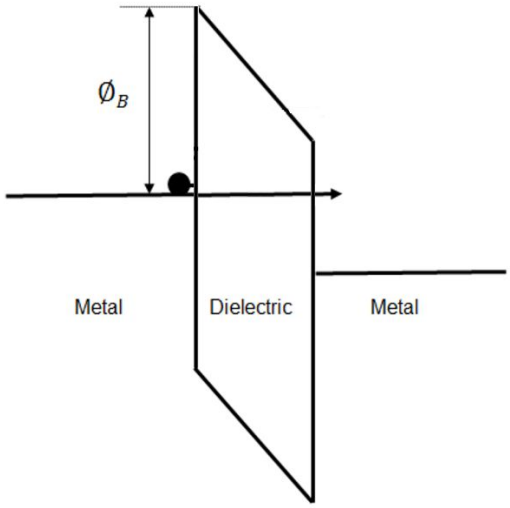

Figure 2.5 Schematic of direct tunneling

2.1.4 Charging Behavior of Dielectric

Leakage current is the current that flows through dielectric when an external electric field is applied to the dielectric. The process of applying an electric field to dielectric is called dielectric charging process. Figure 2.6 is a schematic of typical charging behavior of dielectric. As shown in the figure, charging behavior of dielectric can be divided into three regions. Initially current is high, then it will gradually decrease over time and eventually become stable at certain level. When electric field is first applied to

dielectric, polarization current will arise. Polarization current is generated by dipole movement, namely electronic, ionic and orientational polarization, due to external electric field. However, once dipole is fully aligned by electric field, polarization current will disappear. Therefore, this type of current is undetectable by regular instrument as dipole align time is $<10^{-6}$ S. Second region of charging behavior is where relaxation current is dominant. This type of current is created by the movement of mobile charge inside dielectric. When an electric field is applied, mobile ion with positive charge will migrate to the cathode side of dielectric and mobile ion with negative charge will migrate to the anode side of dielectric. Once all mobile ions drift to certain position, they will reach equilibrium state and migration stops. The last region of dielectric charging is mainly leakage current. At this stage, all dipoles and ions are in equilibrium state and do not contribute to current flowing through dielectric. Based on applied temperature, electric field and dielectric properties, one or multiple conduction mechanisms may be contributing to leakage current simultaneously.

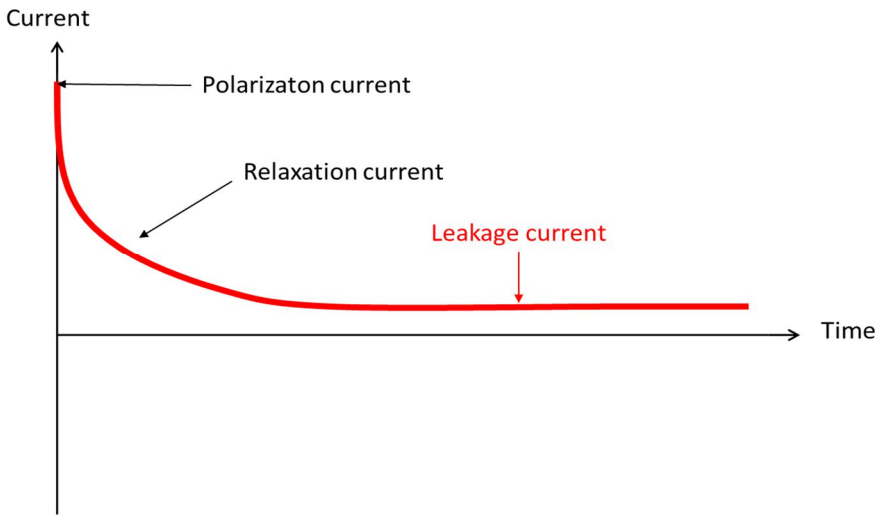

Figure 2.6 Schematic of dielectric charging behavior

2.1.5 Principle of Polarity Dependence Measurement Technique

Key idea of this measurement technique is to measure the difference in leakage current under different bias. Leakage current can be calculated from equation

$$I = A * J(E) \qquad (8)$$

Where A is electron injection area from electrode and J(E) is current density created by electric field. For samples with same fabrication process, conduction mechanism is expected to be the same as metal and dielectric properties are identical. Therefore, J(E) is expected to be similar for samples with same fabrication process. On the other hand, electron injection area may be different for samples with same fabrication process due to defects existing in metal lines. In ideal scenario where interconnect structure is defect free, under same electric field intensity, leakage current from both bias directions is expected to be identical in terms of quantity (Figure 2.7). This is because in defect free interconnect, electron injection area from both electrodes are identical.

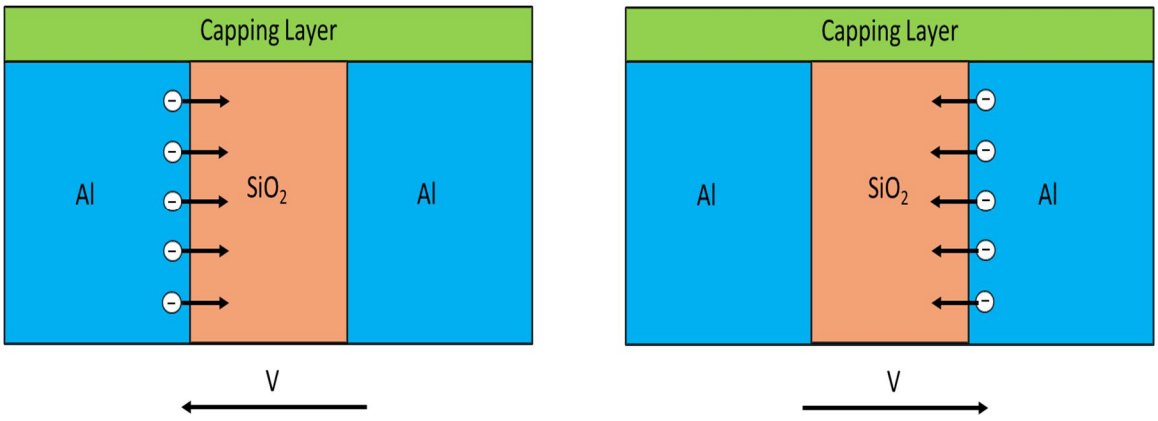

Figure 2.7 Schematic of leakage current in idea condition

However, if one of the electrodes has defects such as voids, injection path will be blocked and therefore electron injection area from both electrodes will be different, which will result in different amount of leakage current based on bias direction (Figure 2.8). Based on the mechanism, electrode which contains defects is expected to have smaller amount of leakage current.

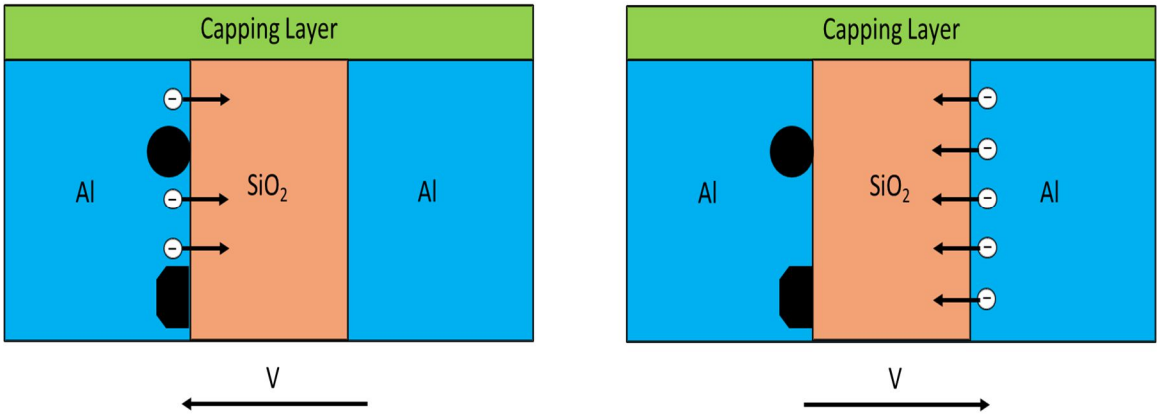

Figure 2.8 Schematic of leakage current when one electrode contains defects

Polarity difference is then calculated by equation

$$\text{Polarity difference} = [\,(\,|I_{negative}|\,/\,|I_{positive}|\,) - 1\,] * 100 \qquad (9)$$

Where $I_{negative}$ is leakage current under negative bias and $I_{positive}$ is leakage current under positive bias. Compare to sample with no defect (ideal scenario polarity difference should be 0%), sample with defects at electrodes will have higher polarity difference. Polarity difference can show not only difference in defect amount, but also defect distribution. Samples with more defect concentrated at one electrode is going to have a higher polarity difference compare to sample with defect evenly distributed at two electrodes.

2.1.6 Aging Treatment

Aging treatment (also known as heat treatment) are known to create stress induced voids inside Al metal lines due to CTE mismatch between Al and surrounding SiO_2. As sample went through aging treatment, it is expected to develop defects in metal lines over time. Therefore, sample's polarity difference is expected to increase with aging time. By comparing result from as-received samples and aging samples, a better understanding of the mechanism can be achieved.

2.2 Samples and Measurement System

2.2.1 Test Samples

Wafers provided by Texas Instruments were used in the research. Samples taken from wafers contain Al/SiO_2 interconnects (dielectric width = 0.21um, metal line thickness = 0.19um) which were patterned in a specific way known as comb-serpentine pattern (Figure 2.9).

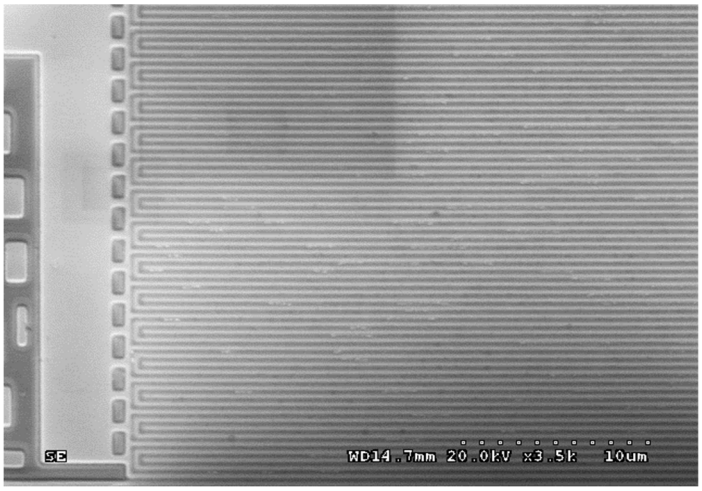

Figure 2.9 Top-down view of test pattern with capping layer removed

Comb and serpentine Al lines are isolated by SiO_2 dielectrics. In Figure 2.10, comb 1 and comb 2 are electrically connected. Therefore, a simplified metal-insulator-metal (MIM) structure as Figure 2.11, which both metal lines can be considered as electrodes, can be used for all the discussion in later paragraph. When a positive electric bias is applied to serpentine electrode and comb electrode is shorted to ground, an electric field with direction from serpentine electrode to comb electrode is formed.

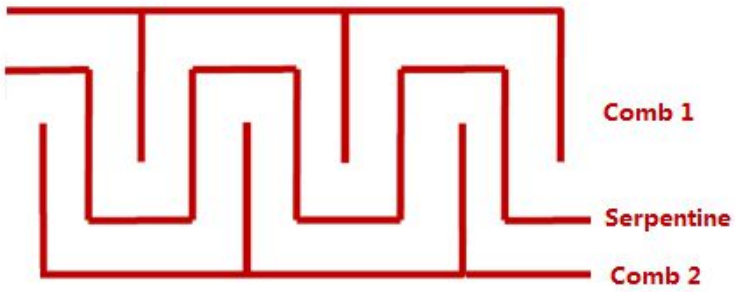

Figure 2.10 Schematic of top-down view comb-serpentine structure

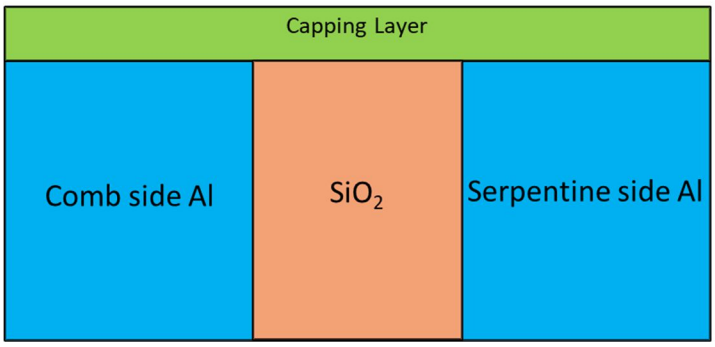

Figure 2.11 Schematic of cross section view MIM structure

2.2.2 Measurement System

Figure 2.12 is the data acquisition system which contains a HP 4140B PA meter/DC source, probe station and a PC with LABVIEW DAQ system. HP 4140B unit generates DC voltage from -100 to 100V and collect leakage current from DUT (device under test) with

picoampere (10^{-15}A) resolution. Probe station is where DUTs are tested during measurement.

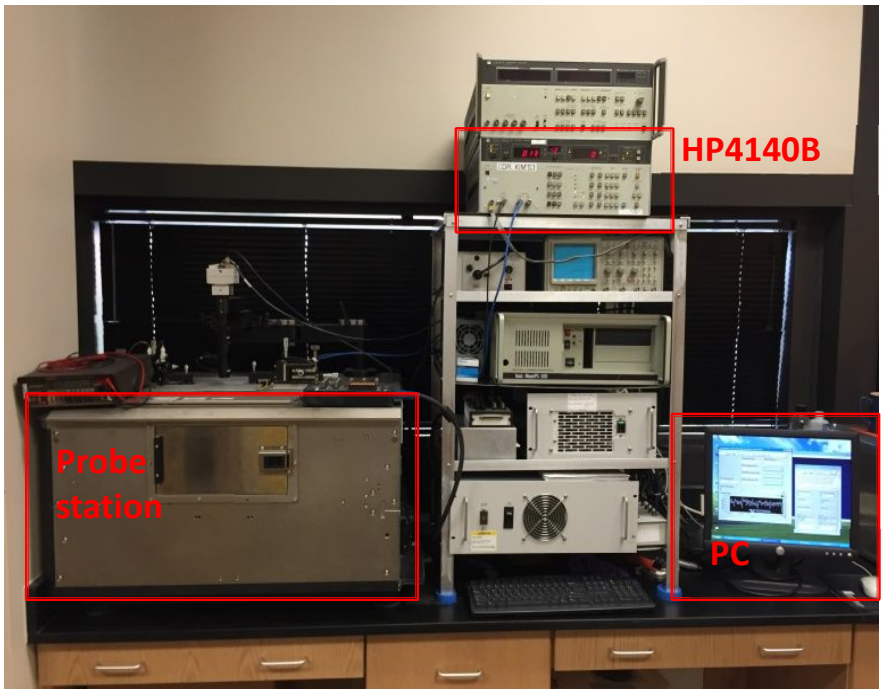

Figure 2.12 Measurement system

Figure 2.13 shows a schematic of electric connection between probe station and HP 4140B unit. Probe station is made of aluminum which acts as a shield blocking electrical noise from environment. Thermo plate below sample stage can heat up to 250^{o}C. LABVIEW DAQ software is used to translate analog data output from HP4140B unit to digital data which is readable by PC. Besides electrical measurement system, there are some conventional instruments used in the research due to the need to confirm the result obtained from electrical measurement, such as high temperature oven, focus ion beam and SEM.

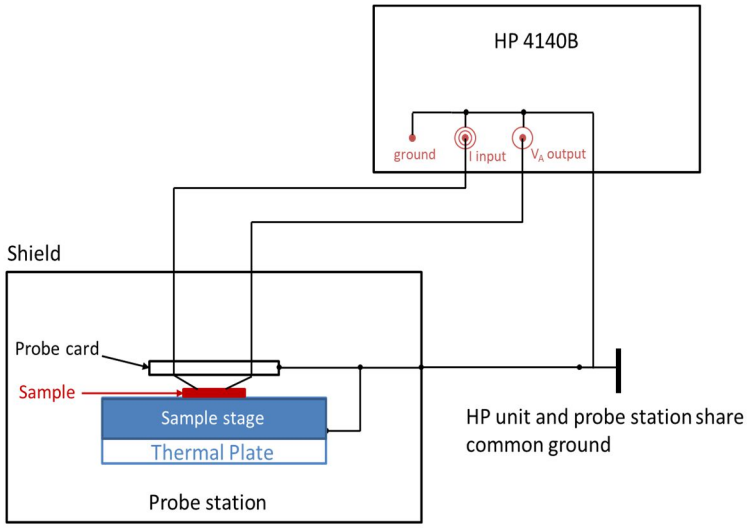

Figure 2.13 Schematic of electric connection between probe station and HP 4140B unit

2.3 Test Strategy

2.3.1 Sample Selection

Purpose of this research is to determine if proposed electrical measurement technique can detect defect in metal lines at metal/dielectric interface. Therefore, is it important to test both samples with defect and samples without defect to compare to results. When a whole wafer is considered, usually dies from edge position of the wafers has worse properties compare to center dies [63,64]. By comparing dies from different locations, leakage current difference may be observed. Figure 2.14 is a schematic of sample selection based on wafer location. Coordinate of the samples taken from wafer is marked as (x,y). For example, center samples in Figure 2.14 is marked as (11,9) and

(12,9). For this research, several different wafers were chosen. Therefore, it is important to select samples from same coordinate to give a meaningful comparison.

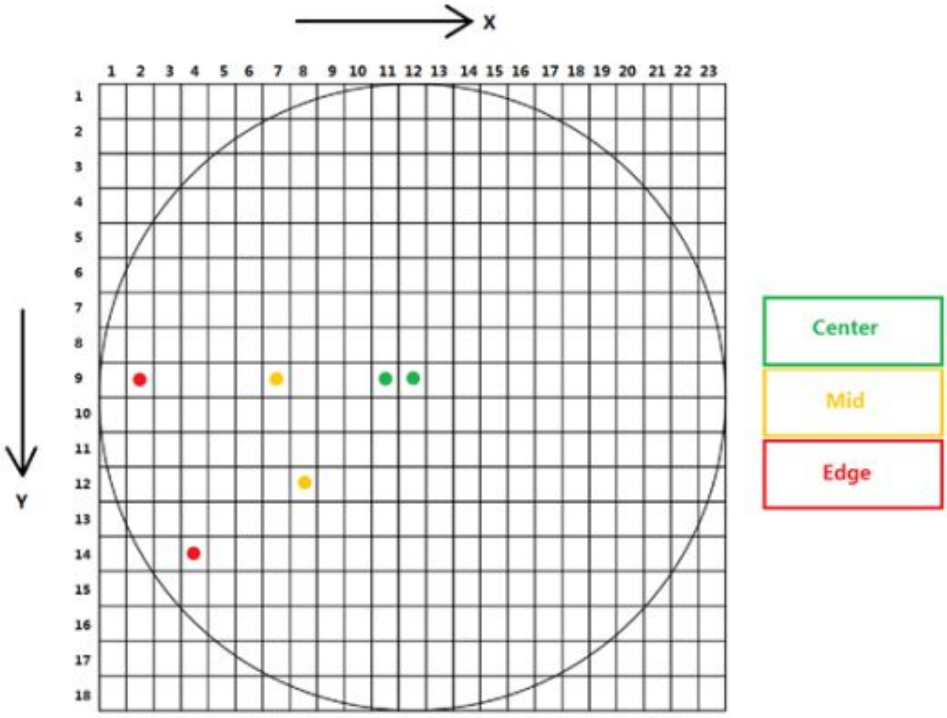

Figure 2.14 Schematic of sample selection based on die location

2.3.2 Test Procedure

As mentioned in previous paragraph, test structure contains comb metal line (comb Al electrode), serpentine metal line (serpentine Al electrode) and dielectric. During measurement, serpentine electrode is always connected to electrical bias source while comb electrode is connected to ground (Figure 2.15). In future discussion, positive bias refers to applying a positive voltage to serpentine electrode and the direction of electric field/current flow is from serpentine electrode to comb electrode (electrons are flowing in opposite direction). Negative bias refers to applying a negative voltage to serpentine

electrode and the direction of electric field/current flow is from comb electrode to serpentine electrode.

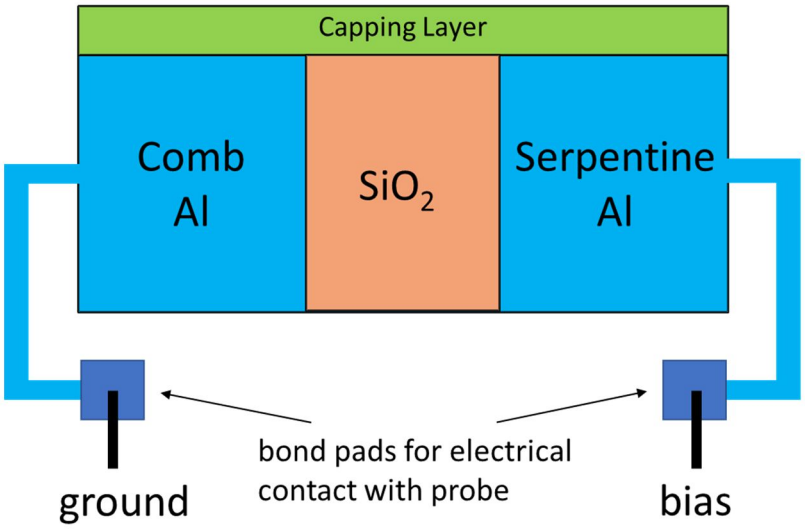

Figure 2.15 Schematic of electrical connection between sample and probe

A typical polarity dependence measurement contains four phases: positive charging, discharging, negative charging and then another discharging. Figure 2.16 is a schematic of the procedure. During positive charging phase, a positive bias is applied to sample for certain amount of time and current data is collected simultaneously. Once current stops to decay and remains at a stable level, that current level is considered as the level of leakage current. During discharging phase, bias is removed and both electrodes are connected to ground. Dielectric is then discharged and returned to equilibrium state. During negative charging phase, a negative bias is applied to sample and leakage current data is collected. After that, sample went through another discharging phase.

After samples go through polarity dependence measurement at as-received condition, they are sent into oven for aging treatment to create stress induced voiding. Temperature of the oven is set to 185°C and aging time is 100 hours. After 100 hours samples are taken out and cooled to room temperature. Another polarity dependence measurement will then be conducted on the samples. Repeat this process for several times and collect leakage current data and polarity difference data.

In this research, 2 wafers are selected (wafer P02 and P25). On each wafer 3 locations are picked (center, mid and edge). At center location 4 samples are tested, at mid and edge locations 8 samples are tested. A total of 8 center samples, 16 mid samples and 16 edge samples are tested in the research. Applied voltage is +/- 100V, charging time is 10 minutes, discharging time is 3 minutes and test temperature is 50°C

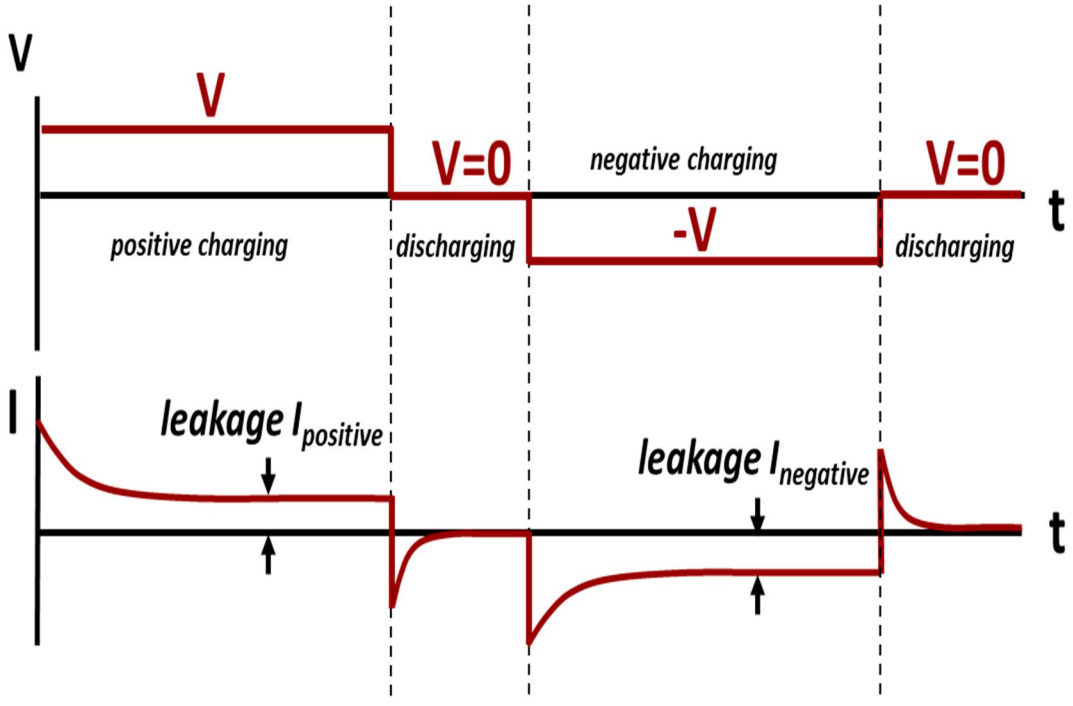

Figure 2.16 Schematic of polarity dependence measurement procedure

2.4 Result and Discussion

2.4.1 Leakage Current Seen in Research

Under applied electric field, leakage current data from dielectric is collected. Figure 2.17 is a current versus charging data collected from one of the samples from wafer P02. Current decays over time rapidly in the first 10 seconds. During this period, relaxation current created by movement of mobile ions is the dominant current seen in measurement. Initially current level is high because all mobile ions are drifting inside dielectric under electric field, ions with positive charges are drifting towards negative electrode while ions with negative charges are drifting towards positive electrode. But once mobile ions start to reach side wall of dielectric, movement of ions will be reduced and relaxation current starts to decay.

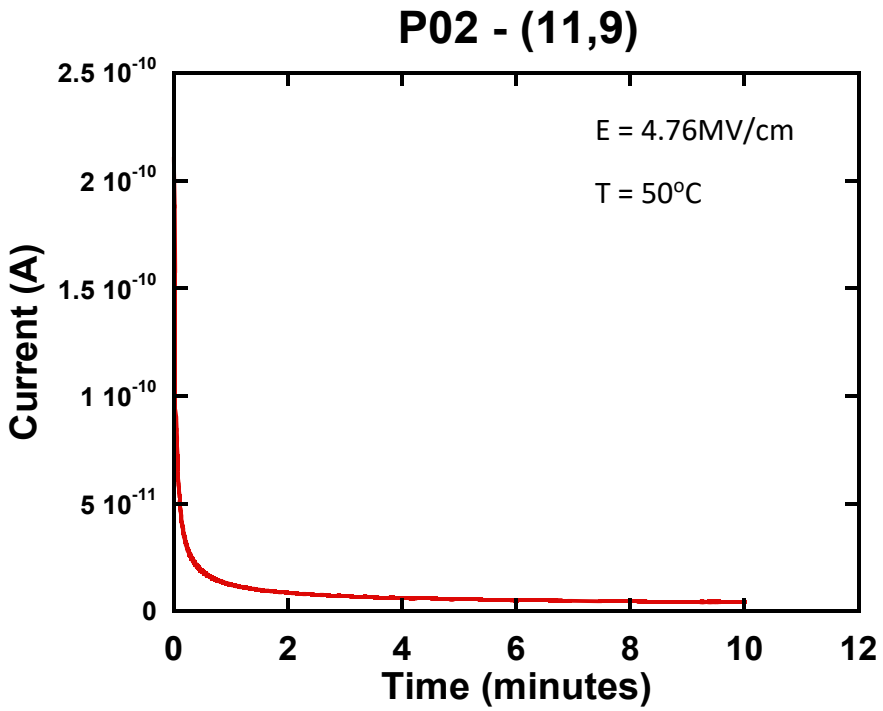

Figure 2.17 Current data from P02 center sample

From 10 seconds to 6 minutes, current seen in the measurement is a mixture of relaxation current and leakage current. Relaxation part of the current is the reason why current is still decaying at a relatively slow speed. After 6 minutes, most of the relaxation current are fully decayed and current seen in the measurement is mostly contributed by leakage current. Therefore, average current collected when charging time reaches 10 minutes is considered as leakage current of the sample in this research.

2.4.2 Conduction Mechanism Confirmation

As mentioned in previous paragraph, there are several conduction mechanisms that might contribute to leakage current. Therefore, it is important to identify which mechanism is the main contributor to leakage current difference seen in the samples.

Since samples are from wafers with identical fabrication process, dielectric properties of samples should be identical. This means bulk limited conduction mechanisms have same contribution to all samples. On the other hand, electrode limited conduction mechanisms are affected by metal/dielectric interface properties. Defects existing in metal lines near metal/dielectric interface is going to impact interface properties. Therefore, electrode limited conduction mechanisms are more likely to contribute to the polarity difference seen in samples.

Typical electrode limited conduction mechanisms include: Schottky emission, F-N tunneling and direct tunneling. Direct tunneling is not likely to contribute to leakage current in this case because it only occurs when thickness of SiO_2 dielectric is narrower than 3.5nm [52] while samples measurement in this research has a dielectric thickness of

210 nm. Schottky emission is affected by temperature and applied electric field. It is commonly seen in dielectric with higher operating temperature (>300K) [52, 65]. F-N tunneling is affected by electric field but not temperature, and thus more commonly seen in dielectric under high electric field and low temperature [52, 66].

To identify which mechanism is the main contributor to current difference seen in polarity dependence measurement, a simple curve fit measurement can be done. According to Chiu *et al.* [65, 66], when main contributor of leakage current is Schottky emission, ln (I/T^2) should have a linear relationship with $E^{1/2}$. When main contributor of leakage current is F-N tunneling, ln (I/E^2) should have a linear relationship with 1/E.

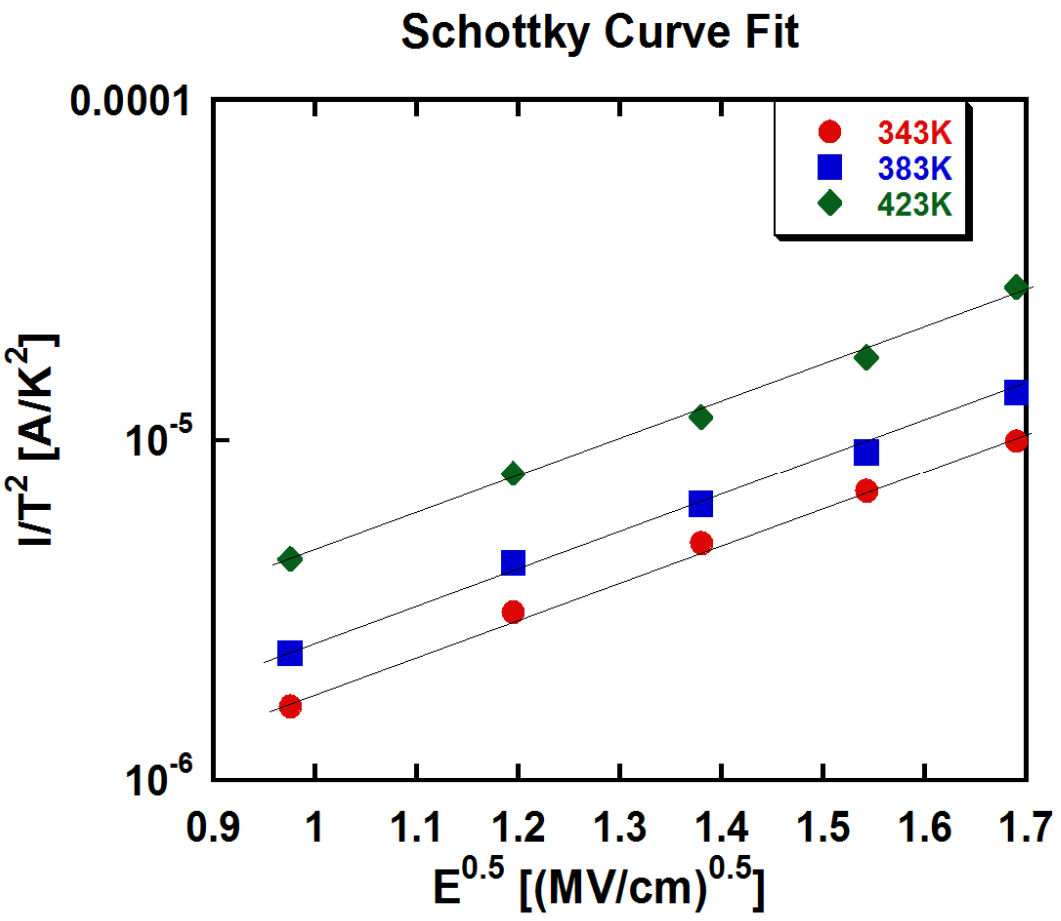

Figure 2.18 Schottky emission curve fit

Figure 2.18 and 2.19 are curve fit for Schottky emission and F-N tunneling, respectively. Y axis of both curve fits are logarithmic scale of ten. Curve fit of Schottky emission does show a linear relationship between I/T^2 and $E^{1/2}$ under log scale. F-N curve fit, on the other hand, does not show a liner relationship between I/E^2 and $1/E$ under log scale. Curve fit of F-N tunneling appears to have two different components, first components is from 0.2 to 0.35 * 1/E where I/E^2 decreases with 1/E and second component is between 0.35 to 0.7 * 1/E where I/E^2 increases linearly with 1/E. Curve fit result indicates that main contributing conduction mechanism of leakage current seen in the measurement is Schottky emission.

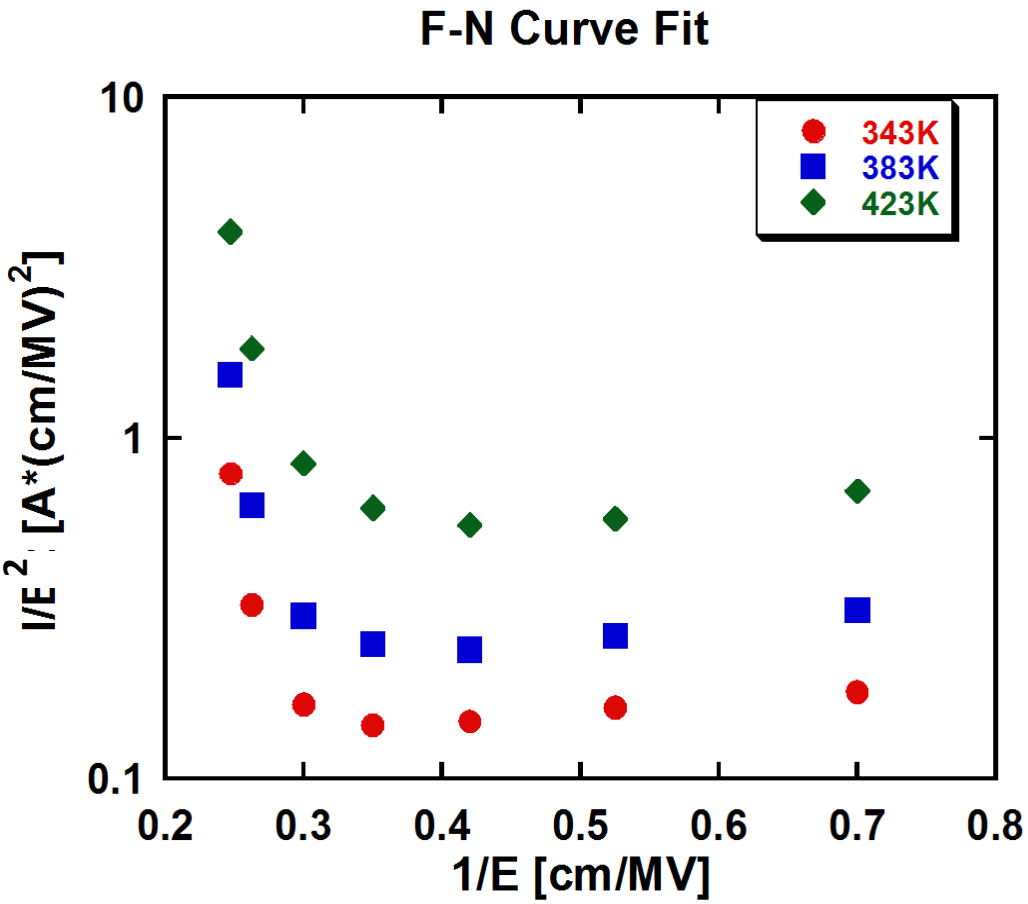

Figure 2.19 F-N tunneling curve fit

This result is as expected. According to Chiu *et al.* [52], contribution to leakage current from F-N tunneling mechanism will only be significant when potential barrier thickness is smaller than 10 nm. Since dielectric width of sample is 210 nm, to reduce the thickness of triangular area of potential barrier to 10nm will require an extremely high electric field (>10 MV/cm). It is likely that dielectric breakdown will occur before F-N tunneling starts to have a significant effect on leakage current.

2.4.3 Average Leakage Current of As-received Samples

Average leakage current is

$$\text{Average leakage current} = (|I_{negative}| + |I_{positive}|) / 2 \qquad (10)$$

where $I_{negative}$ is leakage current under negative bias and $I_{positive}$ is leakage current under positive bias. When sample contains a huge number of defects at metal electrodes, it is expected to show lower average leakage current compare to sample contains no defect. This is due to electron injection area difference mentioned in previous paragraph. When sample contains no defect, electron injection area from both metal electrodes is identical and leakage current level is high. But when a huge number of defects exist at metal electrodes, electron injection area is greatly reduced, and thus current reduced. Therefore, average leakage current can serve as an indicator of interconnect properties. However, leakage current is not only affected by interface injection area, other factors such as dielectric properties and interface roughness will have impacts on current as well, and thus average leakage current is only sensitive to huge number of defects. When samples are at as-received condition, it is not likely for them to develop enough defects

for average leakage current to show huge difference, hence average leakage current level is expected to be similar for samples from different location at as-received condition.

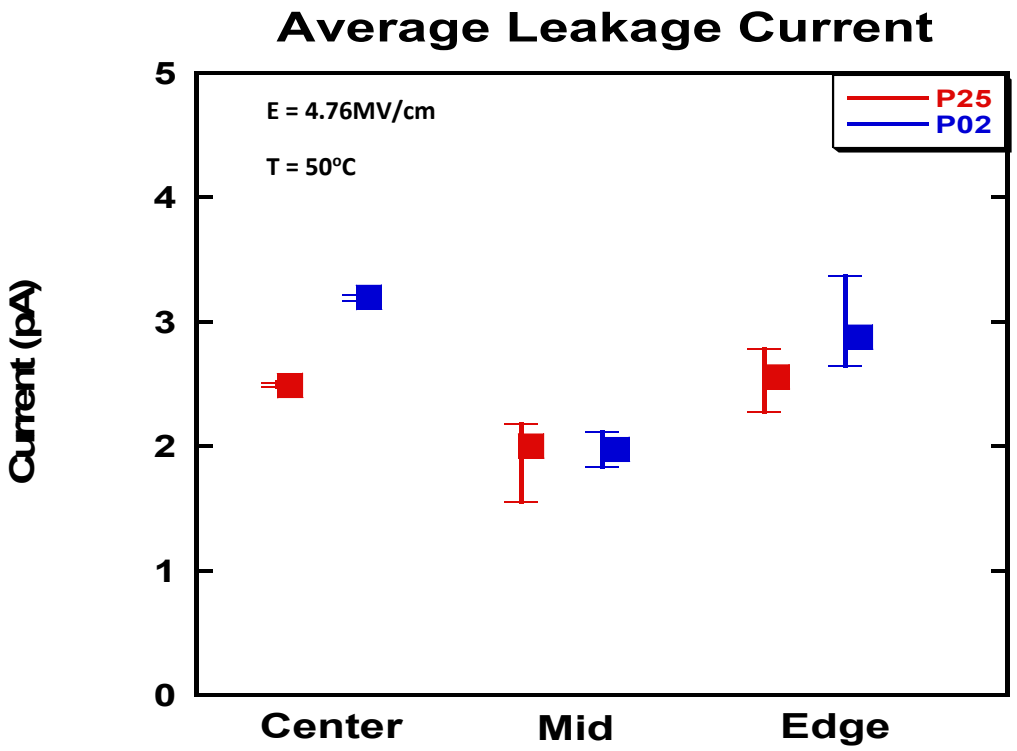

Figure 2.20 Average leakage current versus sample location

Figure 2.20 is average leakage current data collected from as-received samples. Each data point in center location represents the average of 4 samples and each data point in mid and edge location represents the average of 8 samples. Average leakage current data from different location does not show a huge difference, which indicates this measurement may not be sensitive enough to defects in metal lines.

2.4.4 Polarity Difference of As-received Samples

Polarity difference is the difference between leakage current under positive bias and negative bias. Unlike average leakage current measurement which is only sensitive

to huge number of defects in metal electrodes, polarity dependence measurement is designed to detect tiny amounts of defect. Difference between average leakage current measurement and polarity dependence measurement is that previous measurement provides a parameter (average leakage current) that is affected by lots of factors while later measurement provides a self-reference parameter (polarity difference) which is only sensitive to defect distribution at metal electrodes. Therefore, polarity dependence measurement is expected to capture difference in defect distribution even when number of defects is small.

Figure 2.21, 2.22 and 2.23 are example leakage current data collected from as-received samples taken from center, mid and edge location, respectively. In figures, only 6~10 minutes data are shown as it is where leakage current is dominant.

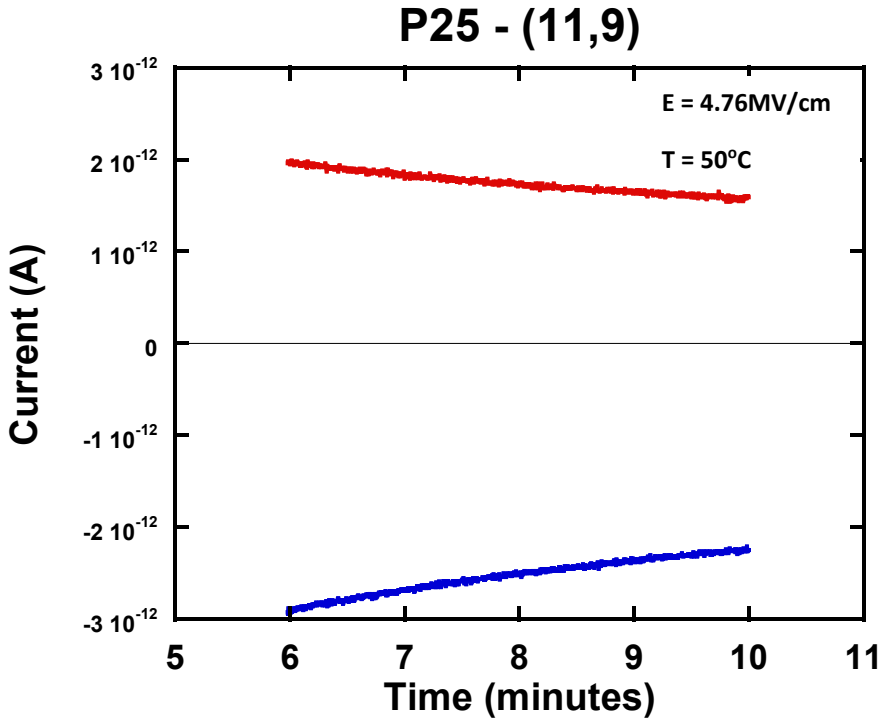

Figure 2.21 Leakage current under positive and negative bias from a center sample

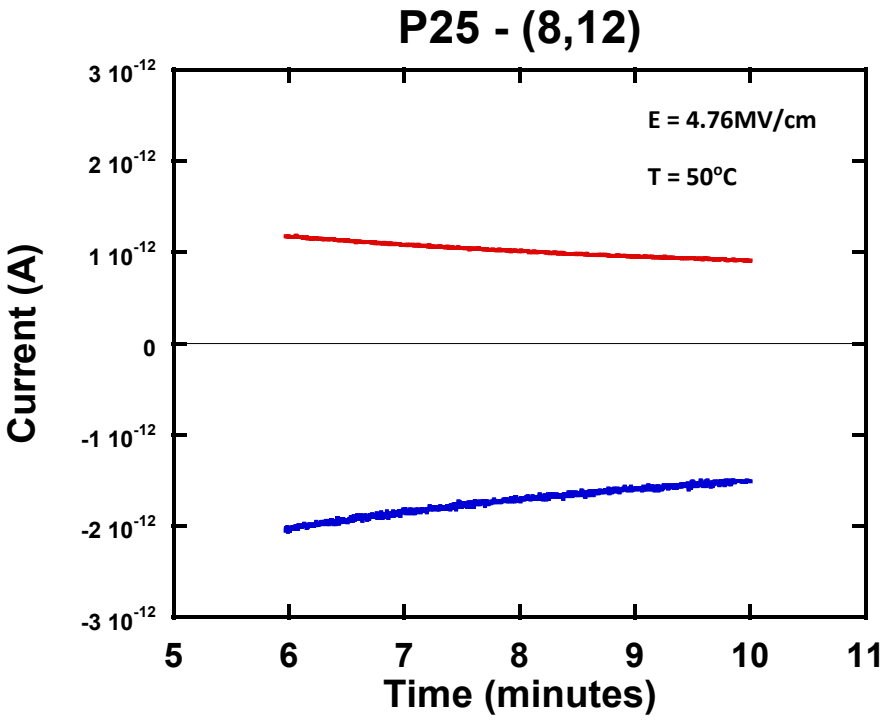

Figure 2.22 Leakage current under positive and negative bias from a mid sample

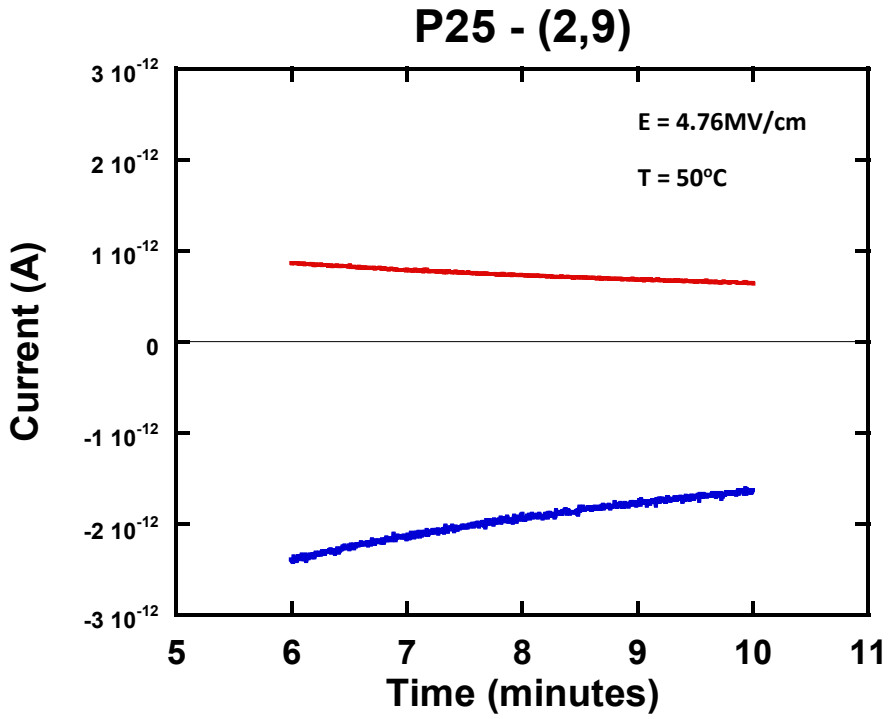

Figure 2.23 Leakage current under positive and negative bias from an edge sample

Example data from Figure 2.21, 2.22 and 2.23 can represent the current difference between samples taken from different locations during measurement. Overall, absolute leakage current under negative bias are larger than absolute leakage current under positive bias. According to the mechanism, it indicates that defect might already exists in metal lines even at as received condition, also comb side electrode might have more defects compares to serpentine side electrode. As discussed in previous chapter, it is possible to have stress induced voiding defect even when samples are stored in room temperature. Therefore, the pre-existing defects might be stress induced voids.

From Figure 2.21, leakage current under negative bis is ~30% larger than leakage current under positive bias. According to equation (9), Polarity difference is ~30% in this case. Compare to Figure 2.22 and 2.23, where polarity difference is ~50% and ~130%, center sample shows smallest polarity difference. This indicates that center sample might have least defects in metal lines compare to mid and edge sample at as-received condition. This corresponds well with the fact that edge sample tends to have worse properties [63,64] and possibly more defects in metal lines. This result shows that polarity dependence measurement is sensitive to defects existing in metal lines.

Figure 2.24 is average polarity difference data collected from as-received samples taken from center, mid and edge location. Each data point in center location represents the average of 4 samples and each data point in mid and edge location represents the average of 8 samples. From figure, center samples showed a lower average polarity difference (~30%) compare to mid samples (~45%) and edge samples (~55%). Two wafers showed a substantial difference at polarity difference even when samples are picked from

identical location on wafer. This is possibly due to the different fabrication process that two wafers went through as P25 and P02 wafers are fabricated with different CVD process. But overall trend is similar, center samples have lowest polarity difference while edge samples have highest polarity difference.

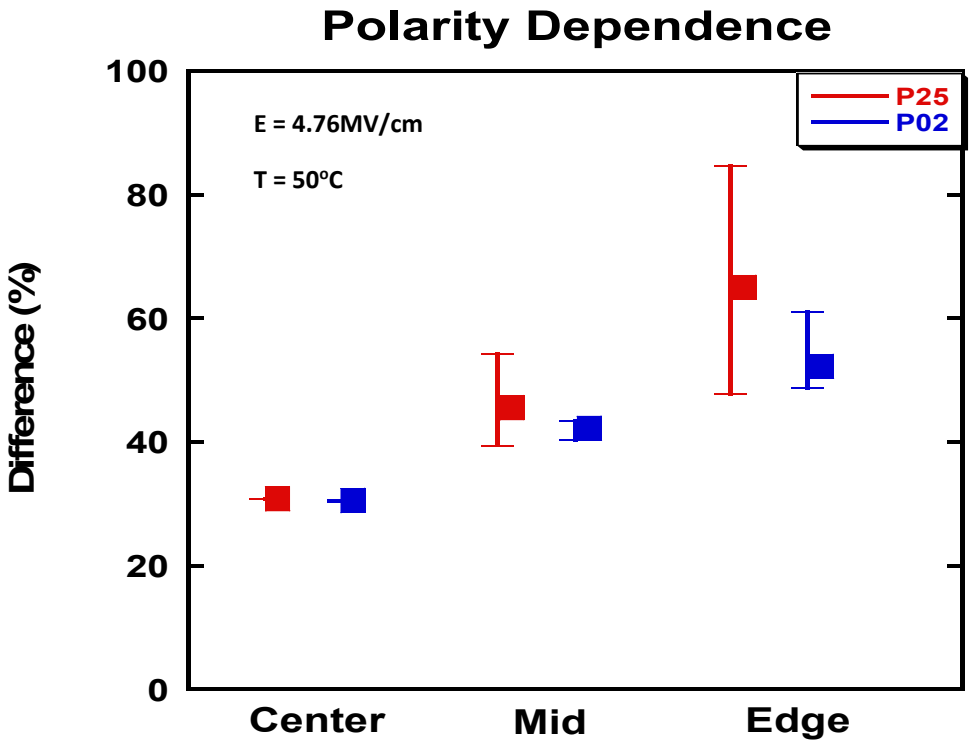

Figure 2.24 Polarity difference versus sample location

2.4.5 Resistance of As-received Sample

Resistance measurement of serpentine metal line is another indicator that can be used to detect defects in metal electrode. Resistance is

$$R = \rho * l / A \quad (11)$$

where R is resistance, ρ is electrical resistivity, l is length of conductor and A is cross section of conductor. When there are defects, such as voids, in metal lines, a part of

conductor is replaced by voids which is essentially insulator with high resistance. Therefore, overall resistance is expected to increase as more defects exist in metal lines. However, like average leakage current measurement, for resistance to show a noticeable change, amount of defects has to be very large. In another word, resistance will not change much unless metal lines are about to fail (open circuit). For samples tested in this research, minor resistance difference is expected as samples at as-received condition should have similar defects distribution.

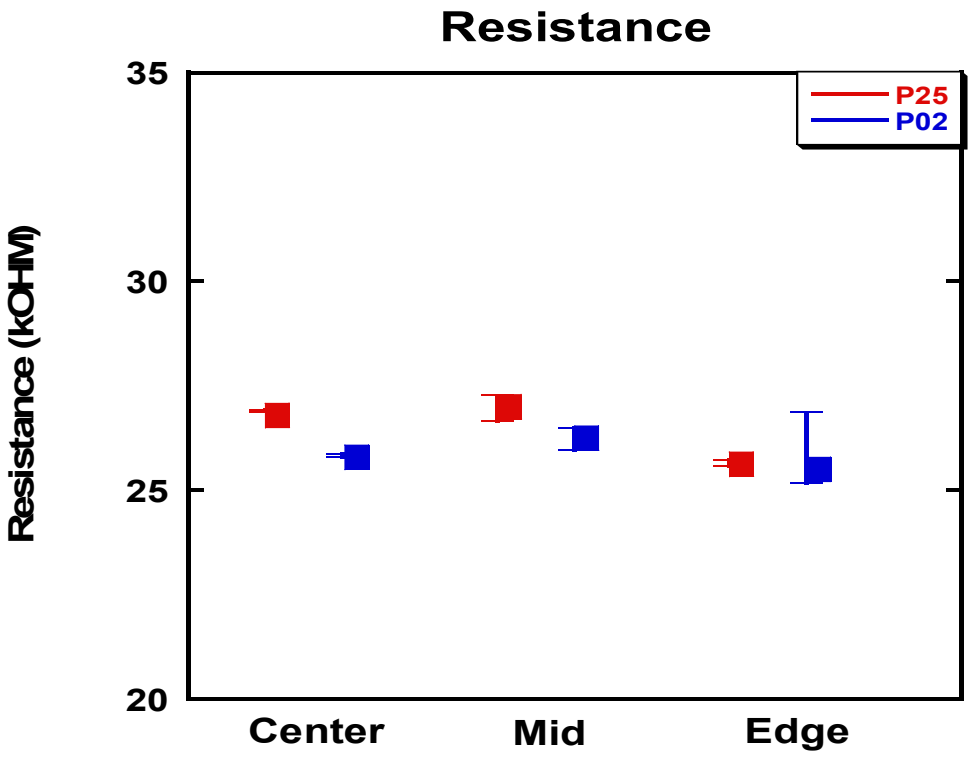

Figure 2.25 Resistance versus sample location

Figure 2.25 is resistance data collected from as-received samples taken from center, mid and edge location. Each data point in center location represents the average of 4 samples and each data point in mid and edge location represents the average of 8

samples. As seen in figure, resistance does not show noticeable between samples from different location. This indicates that resistance measurement is not very sensitive to defects in metal lines.

2.4.6 Average Leakage Current of Aging Samples

After samples are tested at as-received condition, aging treatment is applied to all samples. Figure 2.26 is average leakage current data collected from samples that go through aging treatment. The plot shows that average leakage current does not vary much over aging time. This might suggest that either defects do not develop rapidly during 600 hours of aging or the measurement is not sensitive to defects.

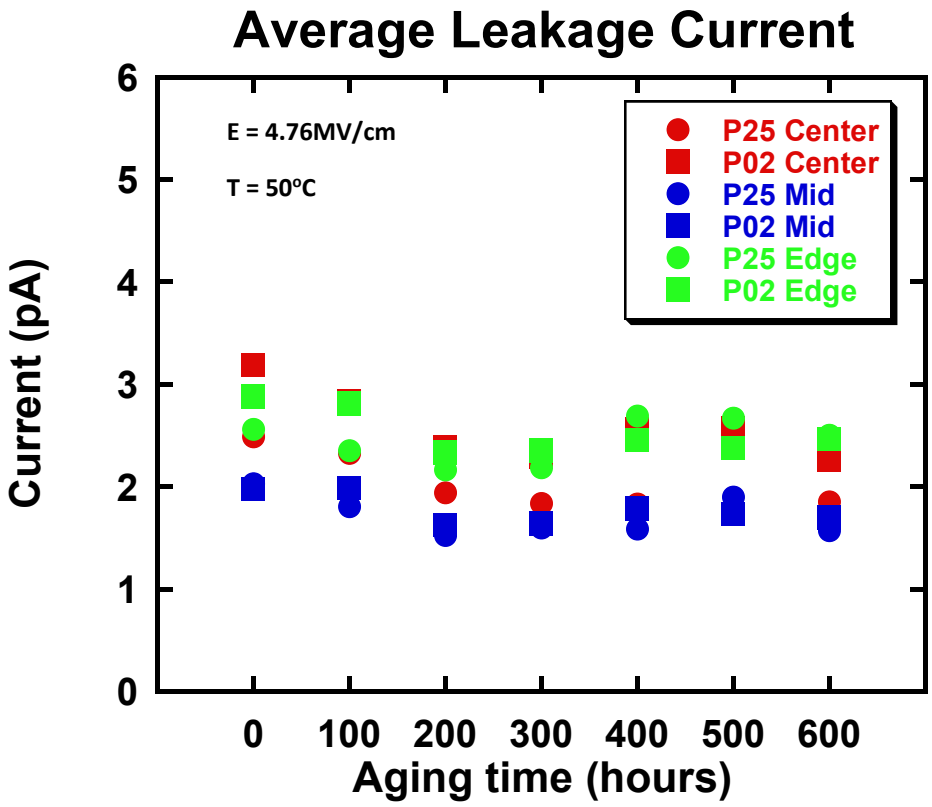

Figure 2.26 Average leakage current versus aging time

2.4.7 Polarity Difference of Aging Samples

As samples go through aging treatment, polarity difference of samples showed a noticeable change. Figure 2.27 is polarity difference data collected from aging samples. From the plot it can be observed that polarity difference of all samples decreases at 100 hours aging, it may be due to the annealing effect which improves crystal lattice structure [67,68] of Al, and thus defects such as dislocation can be removed. This will cause overall number of defects to be reduced and polarity difference is expected to decrease. After 100 hours, stress induced voids start to develop inside metal lines. Polarity difference of center samples remains steady while polarity difference of mid samples and edge samples gradually increases over aging time. Compare to mid samples, edge samples have a

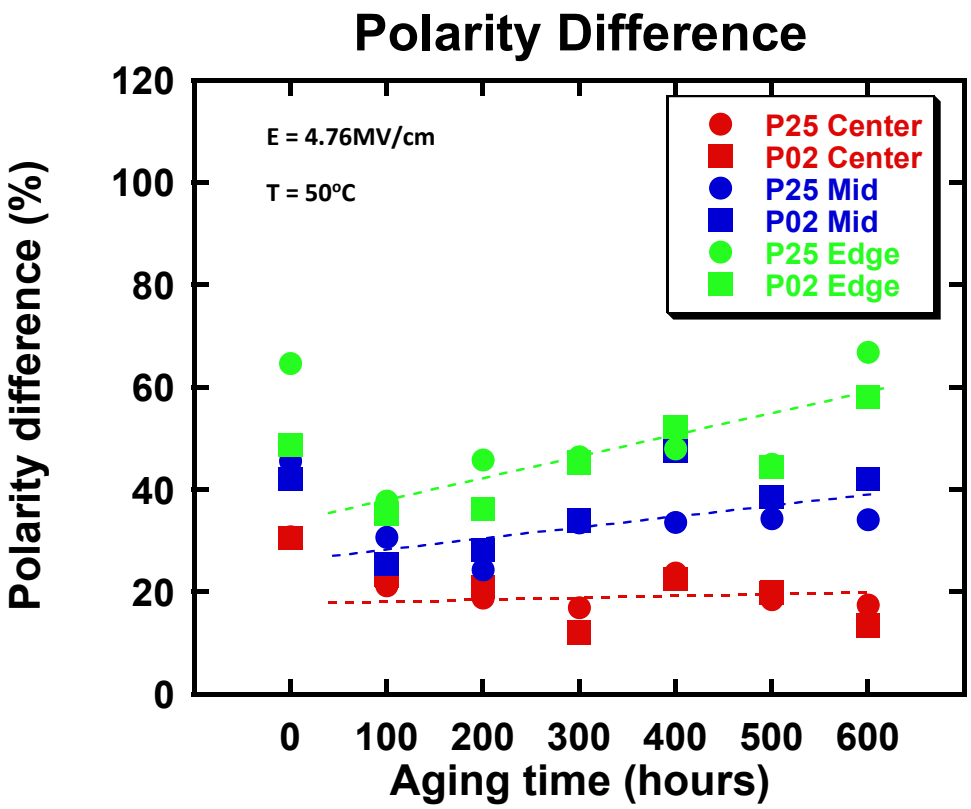

Figure 2.27 Polarity difference versus aging time

higher polarity difference slope. This result may suggest that edge samples developed highest amount of defects while center samples developed lowest amount of defects during aging treatment. Plausible explanation of mid and edge samples developing more defects is that mid and edge samples have worse properties [63,64] and are more prone to stress voiding activity. The plot also shows that samples with high polarity difference at as-received condition tends to have higher polarity difference over aging time. Therefore, polarity difference may serve as a predictive parameter which can identify samples that are more likely to develop defects over time.

2.4.8 Resistance of Aging Samples

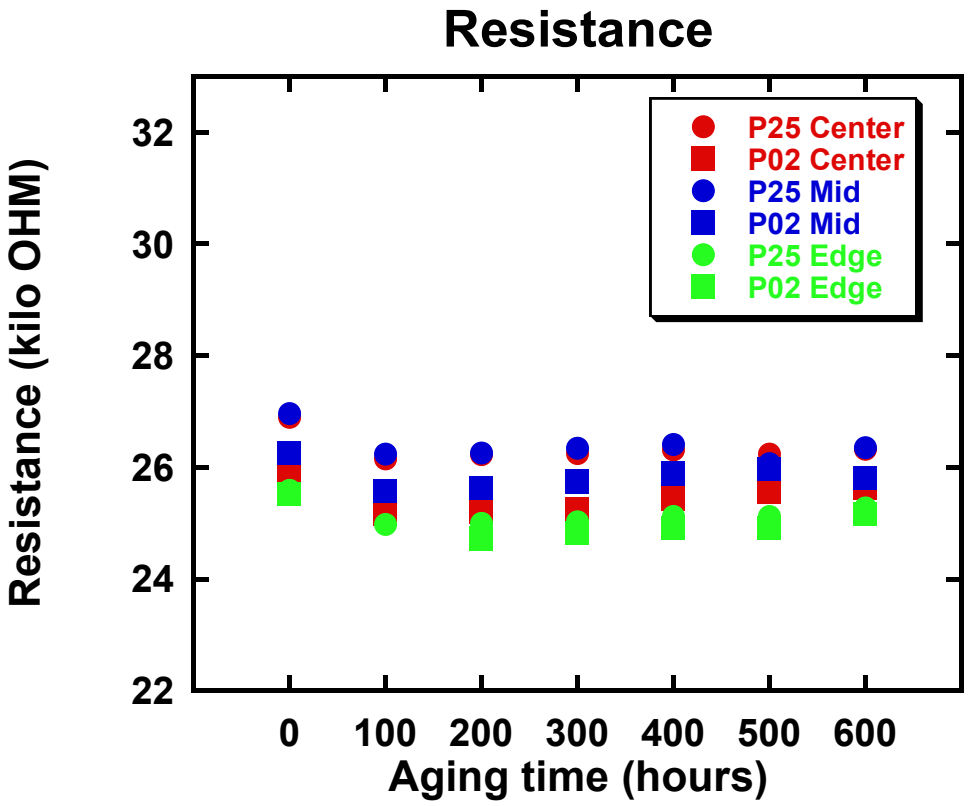

Figure 2.28 Resistance versus aging time

Resistance does not vary much during aging treatment. Figure 2.28 is resistance data collected from aging samples. Samples from all locations are having similar resistance from as-received condition to 600 hours aging. This is similar to the result of average leakage current measurement. Therefore, result indicates that polarity dependence measurement might be able to capture defect developing during aging treatment while average leakage current and resistance measurement cannot.

2.4.9 SEM Inspection on Aging Samples

To confirm if there are defects existing in metal lines, conventional SEM inspection are done on samples (600 hours aging) from edge location. Figure 2.29, 2.30 and 2.31 are top-down view SEM images with capping layer removed by focus ion beam.

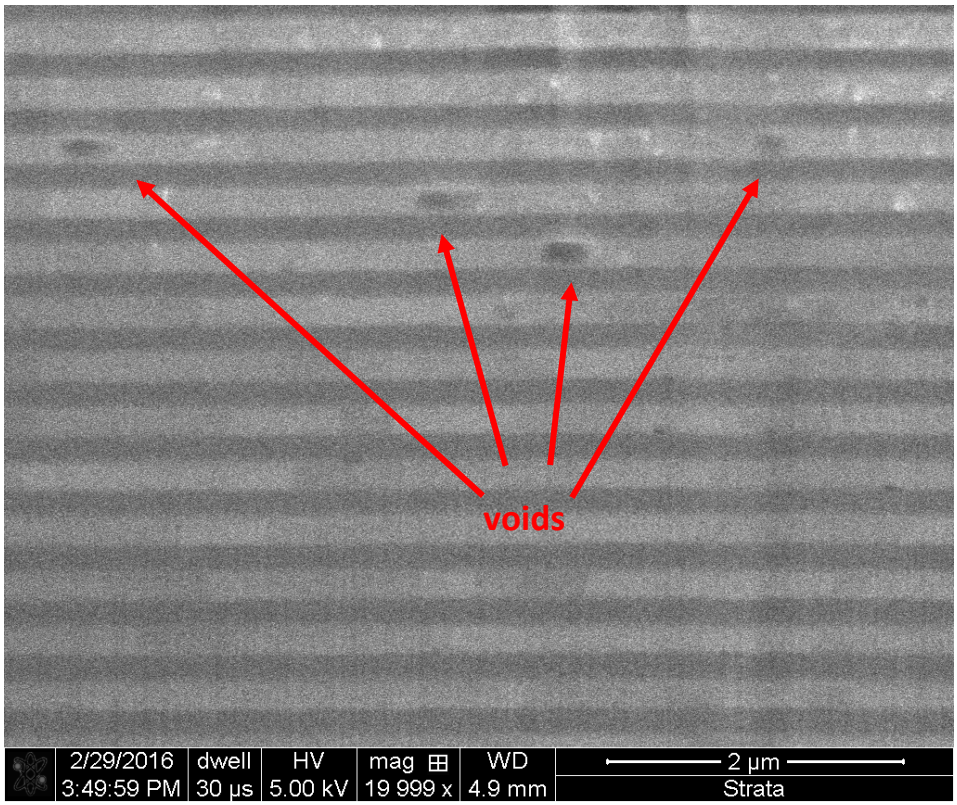

Figure 2.29 Top-down view SEM on edge sample (600 hours aging)

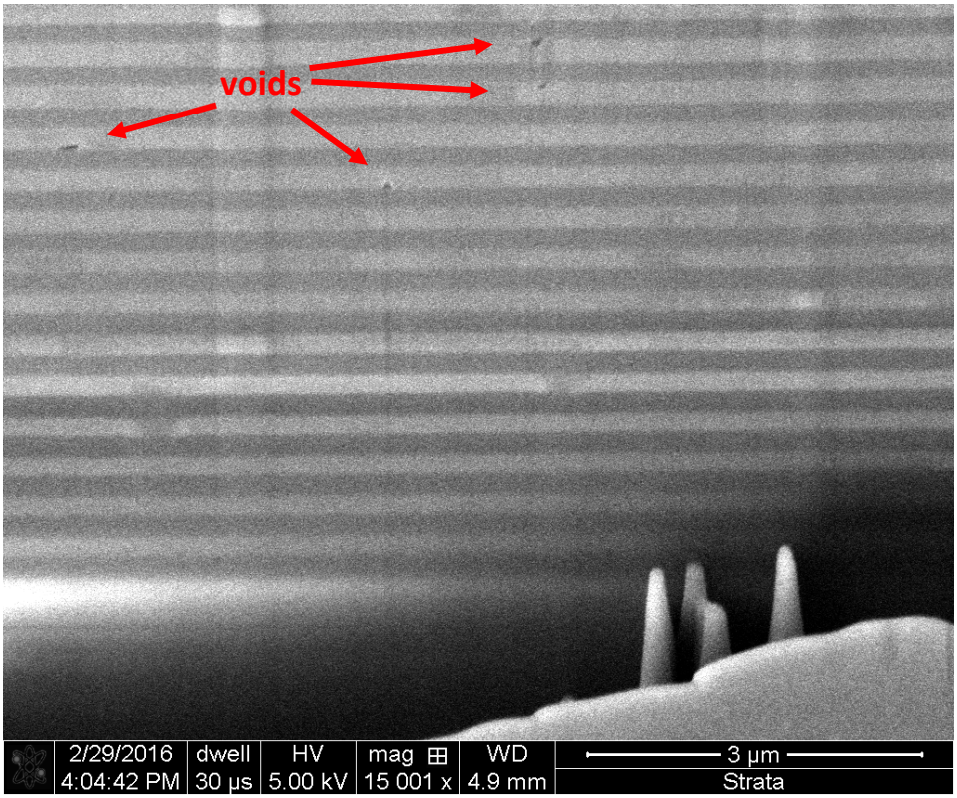

Figure 2.30 Top-down view SEM on edge sample (600 hours aging)

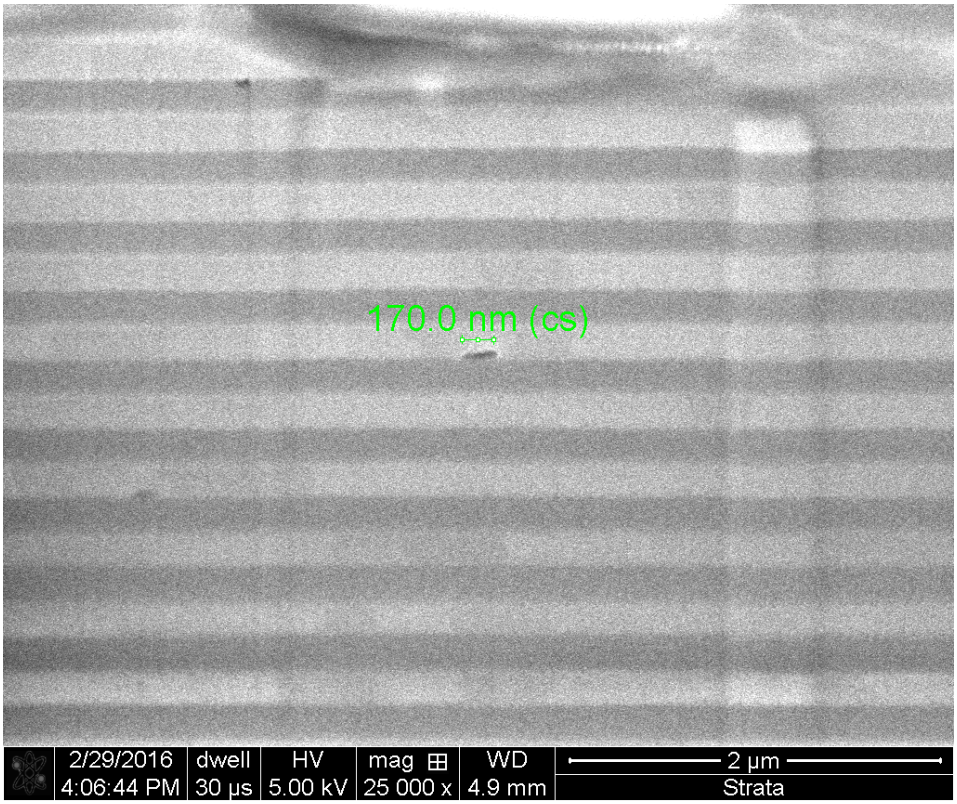

Figure 2.31 Top-down view SEM on edge sample (600 hours aging)

In SEM images, lines with brighter contrast and darker contrast are Al metal and SiO_2 dielectric, respectively. In Figure 2.29, several voids with length ~200nm can be observed. Those voids are ~60% the width of Al lines. If voids are fully developed, they might cut off metal lines and create open circuit. Voids seen in Figure 2.30 and 2.31 are smaller than those seen in Figure 2.29. These voids are likely at the early stage of stress migration. From the SEM images, it is clear that defects exist in edge sample after 600 hours aging.

2.5 Summary

In this chapter, leakage current measurement, resistance measurement and polarity dependence measurement have been introduced and the mechanism of these measurements have been studied. While average leakage current and resistance does not show direct relationship with defects located at Al metal lines in Al/SiO_2 interconnects, polarity dependence measurement shows a promising result and polarity difference might be able to serve as a simple parameter that can predict the properties of Al metal lines.

Samples used in the study are chip-level Al/SiO_2 interconnect (dielectric width = 0.21um) with comb-serpentine structure from Texas Instruments. Usually samples taken from edge location of wafer have worst properties while center samples have best properties. Therefore, by performing polarity dependence measurements on samples

taken from center, mid and edge location, polarity difference is expected to be different and can show some meaningful prediction as to the properties of Al metal lines.

Leakage current measurement collects current that flow through dielectric under applied electric field. There are several conduction mechanisms (bulk-limited and electrode-limited) that contribute to leakage current. In this chapter, main conduction mechanism that contributes to the leakage current seen in research is Schottky emission. Average leakage current of center, mid and edge samples at as-received condition or aging condition do not show significant difference. When defects exist in metal lines, electron injection area is reduced and leakage current should reduce as well. However, since leakage current is only sensitive to large number of defects in metal lines, when amount of defects in metal lines is not distinguishably different, average leakage current is going to be similar. Therefore, average leakage current measurement might not be an idea method to monitor defects in Al metal lines.

Resistance measurement collects resistance value of serpentine metal lines in Al/SiO_2 interconnects at as-received and aging condition. Resistance of center, mid and edge samples at as-received condition does not show noticeable difference. This is likely due to resistance of metal lines is not sensitive to defect unless metal lines are about to fail. For samples that go through aging process to create stress induced voids, resistance does not vary with aging time. This is another evidence that resistance is not sensitive to defects. Therefore, resistance measurement is not suited for defect detection in Al metal lines.

Polarity dependence measurement applied two voltage with same amount but different direction to samples and collect corresponding leakage current ($I_{positive}$ and $I_{negative}$). Polarity difference parameter is the ratio of positive and negative leakage current. For samples at as-received condition, center samples show a lowest polarity difference while edge samples show a highest polarity difference. According to the mechanism of polarity dependence measurement, it indicates that edge samples contain defects even at as-received condition. As samples go through aging process, polarity difference of samples increases gradually and edge samples show a higher increase rate in polarity difference compare to center samples. This indicates that edge samples might be more prone to stress induced voiding activity. To confirm that edge samples do contain defects, SEM inspections were done and result indicates that edge samples contain voids after aging process. Result of polarity dependence indicates that polarity difference might serve as a simple parameter that can predict Al metal lines properties.

CHAPTER 3

CURRENT VOLTAGE MEASUREMENT AND ITS SENSITIVITY TO STRUCTURAL DEFECTS IN ALUMINUM LINES OF AL/SIO_2 INTERCONNECTS

3.1 Background

Current voltage measurement (I-V test or J-V test) has been implemented as a quality and reliability test method to determine the properties of semiconductor devices, such as dielectric properties of transistors and characteristic of diodes [69-73]. However, using current voltage measurements to determine the properties of metal lines in interconnect has not been studied. The purpose of this study is to propose two current voltage measurement techniques that can provide simple parameters to predict the properties of Aluminum metal lines in Al/SiO_2 interconnects.

First measurement technique is I-V curve measurement. In this research, 12 voltage levels (from 5V to 85V) are applied to sample and leakage current data of each voltage level is collected and plotted as I-V curve. I-V curve can serve as an indicator of defect distribution in Al metal lines at metal/dielectric interface. As discussed in previous chapter, two factors are affecting leakage current: current injection area and current density which is affected by electric field (I = A * J(E)). When there is a defect in metal line, current injection area is reduced because electrons cannot inject into dielectric through defect. However, current density is increased because the sharp corner created by defect can induce highly concentrated electric field. Therefore, these two factors are competing against each other and under different voltage level, one factor is expected to

be more dominant than the other factor. Samples with defects located at metal/dielectric interface is expected to show different I-V curve compare to samples with no defect.

Second measurement technique is two-point measurement which only two different level of voltage (45V and 85V) are applied to sample and leakage current data is collected. Two-point measurement is developed based on the concept of I-V test that different voltage level might have different effect on leakage current. This measurement technique can yield a simple parameter ($I_{high\ voltage}/I_{low\ voltage}$) that might be able to reflect the number of defects existing inside metal lines.

3.2 Experimental Setup and Test Strategy

3.2.1 Test Samples

Wafers provided by Texas Instruments were used in the research. Samples taken from the wafers contain Al/SiO_2 interconnects (dielectric width = 0.21um, metal line thickness = 0.19um) which were patterned in a specific way known as comb-serpentine pattern, as discussed in previous chapter.

3.2.2 Measurement System

For I-V curve measurement and two-point measurement, data acquisition system (HP4140B pA meter/DC source, probe station and PC with LABVIEW DAQ system) introduced in previous chapter was used. SEM inspections were done by Hitachi 4000 and 5000 SEM.

3.2.3 Sample Selection

Purpose of this research is to determine if proposed electrical measurement technique can detect defect in metal lines. Therefore, is it important to test both samples with defect and samples without defect to compare to results. When a whole wafer is considered, usually dies from edge position of the wafers has worse properties compare to center dies [63,64] and there is a possibility that edge dies have pre-existing defects. By comparing dies from different locations, a difference in leakage current might be observed. In this research, samples from center and edge location are selected.

3.2.4 I-V Curve Measurement Procedure

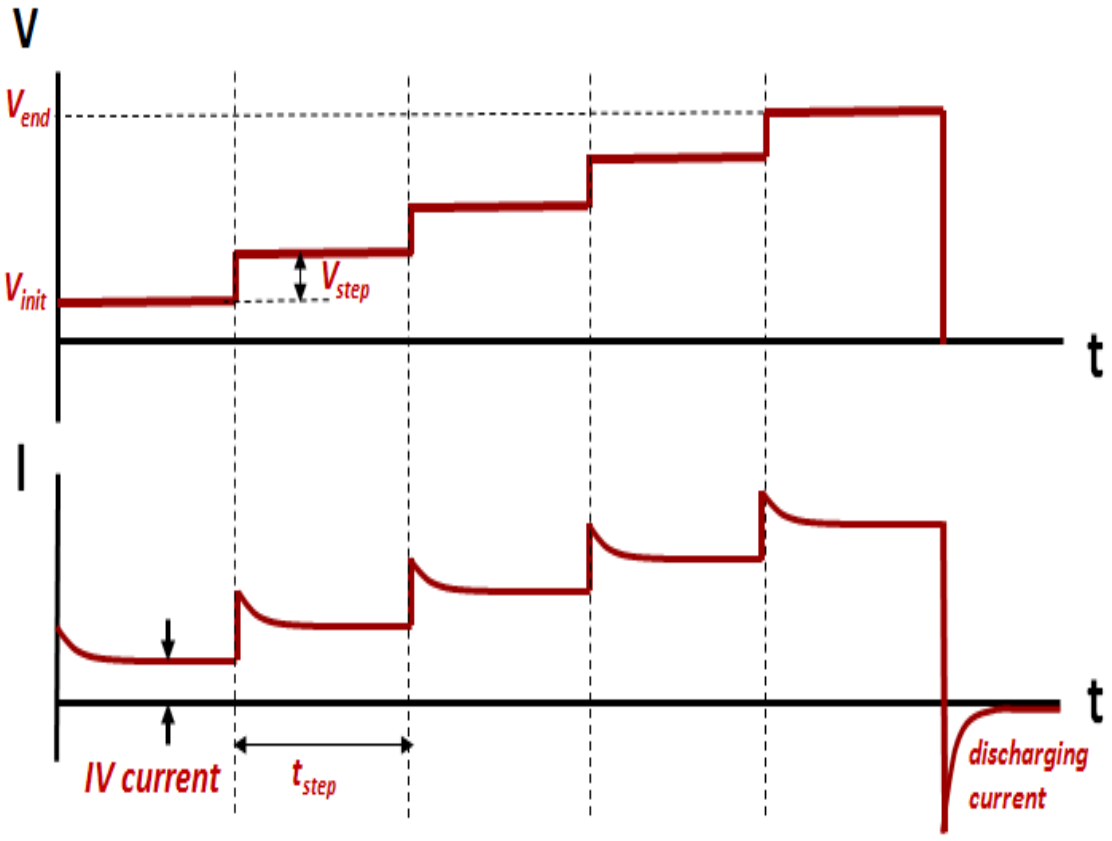

Figure 3.1 Schematic of I-V curve measurement

Figure 3.1 is the schematic of I-V curve measurement. Basic procedure of I-V curve measurement is: First apply an initial voltage (V_{init}) to sample for certain amount of time (t_{step}) and collect corresponding leakage current data. Applied voltage is then increased by certain amount (V_{step}) and sample is charged for same amount of time (t_{step}) to collect another corresponding leakage current data. Repeat the process until maximum voltage (V_{end}) is reached. In this research, measurement condition is V_{init} = 5V, V_{step} = 5V, V_{end} = 85V and t_{step} = 1 minutes. By plotting current versus voltage data into KaleidaGraph software, I-V curve can be observed.

3.2.5 Two-point Measurement Procedure

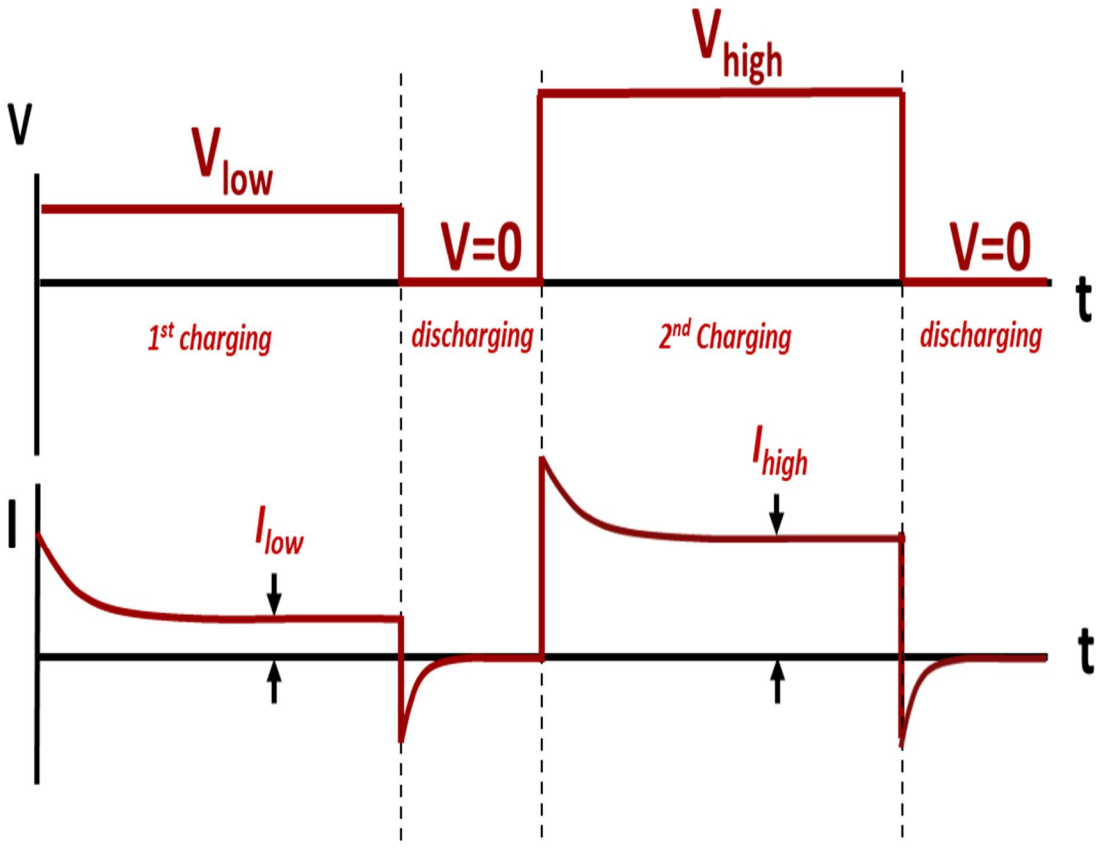

Figure 3.2 Schematic of two-point measurement

Procedure of two-point measurement is similar to I-V curve measurement except only two level of voltage are applied to the sample. Figure 3.2 is a schematic of two-point measurement. During first charging process, a lower voltage V_{low} is applied to the sample for certain amount of time ($t_{charging}$) and leakage current data I_{low} is collected. After that, voltage is removed and sample is shorted to ground for certain time period ($t_{discharge}$) to discharge. During second charging process, a higher voltage V_{high} is applied to the sample for same amount of time and leakage current data I_{high} is collected. Ratio of I_{high} /I_{low} is then calculated and used as a parameter to determine properties of Al metal lines. In this research, V_{low} = 45V, V_{high} = 85V, $t_{charging}$ = 10 minutes, $t_{discharing}$ = 3 minutes and test temperature is 50^{o}C.

3.2.6 Chemical Etching

To do top-down view SEM inspection, capping layer (mostly SiN) of samples need to be removed. HF is a known wet etchant that can remove SiN. However, etch rate of HF on SiN is too fast and hard to control. Therefore, etchant used in the research is 6:1 buffer oxide which is a mixture of 40% NH_4F and 49%HF at 6:1 volume ratio and NH_4F can slow down and control the etch rate of HF. Chemical reaction of SiN and buffer oxide is

$$Si_3N_4 + 16HF \rightarrow 2(NH_4)_2[SiF_6] + SiF_4$$

In this study, etch temperature is set to 50^{o}C. Since etchant can also attack Al metal lines beneath capping layer, to rule out the possibility of seeing voids created by etching, a thin layer of capping layer needs to remain on the surface. This requires a precise control on the etching time (~5 minutes, depends on the sample).

3.3 Result and Discussion

3.3.1 I-V Curve Measurement of As-received Samples

As discussed in previous paragraph, samples from center and edge location are expected to show some difference in I-V curve and the result indicates that there does exist noticeable difference in the curve. A set of I-V data has been plotted into Figure 3.3 as an example to show the distinct difference between center and edge sample at as-received condition. Voltage applied to the sample is 5–85V, dielectric width of sample is 0.21um and test temperature is 50^{o}C.

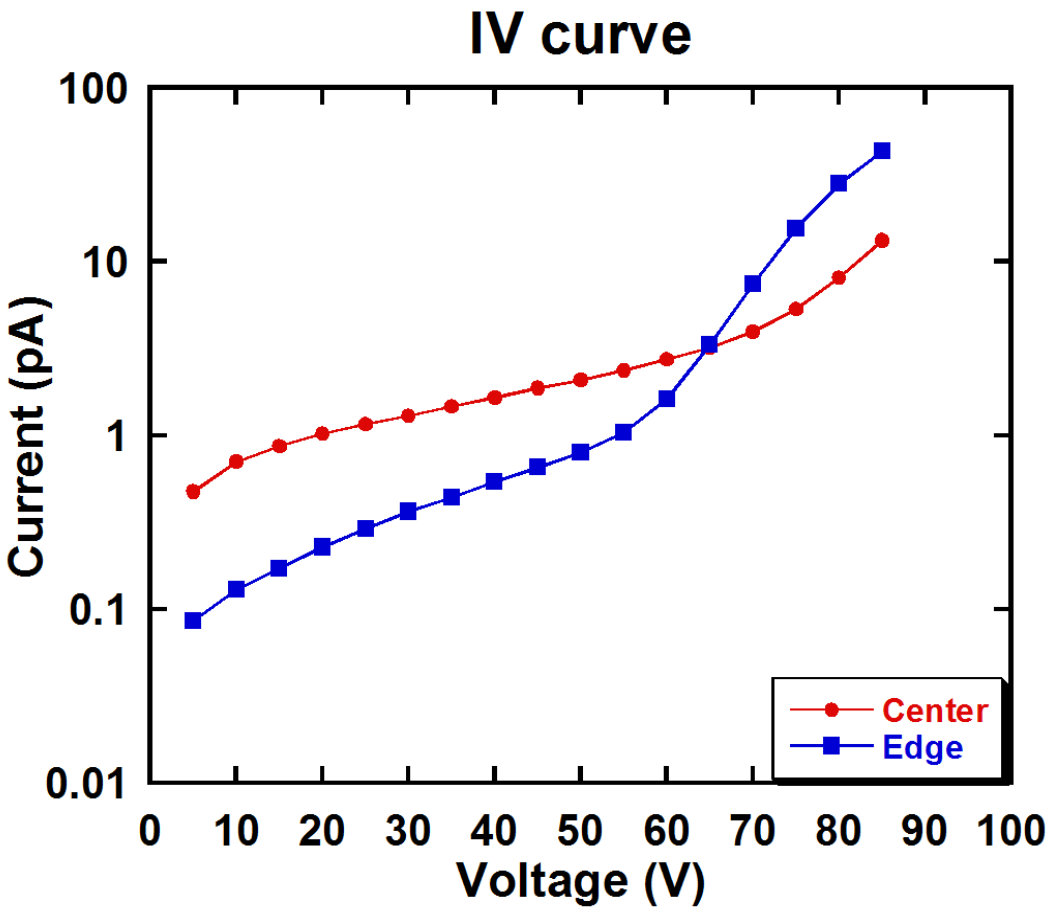

Figure 3.3 Typical I-V curve data from center and edge sample

Figure 3.3 indicates that at low applied voltage (5-60V), center sample shows higher current compare to edge sample. However, as applied voltage continuous to increase (70-85V), center sample shows *lower* current compare to edge sample. Based on current understanding, this significant I-V curve difference might be coming from the defects existing in Al metal lines.

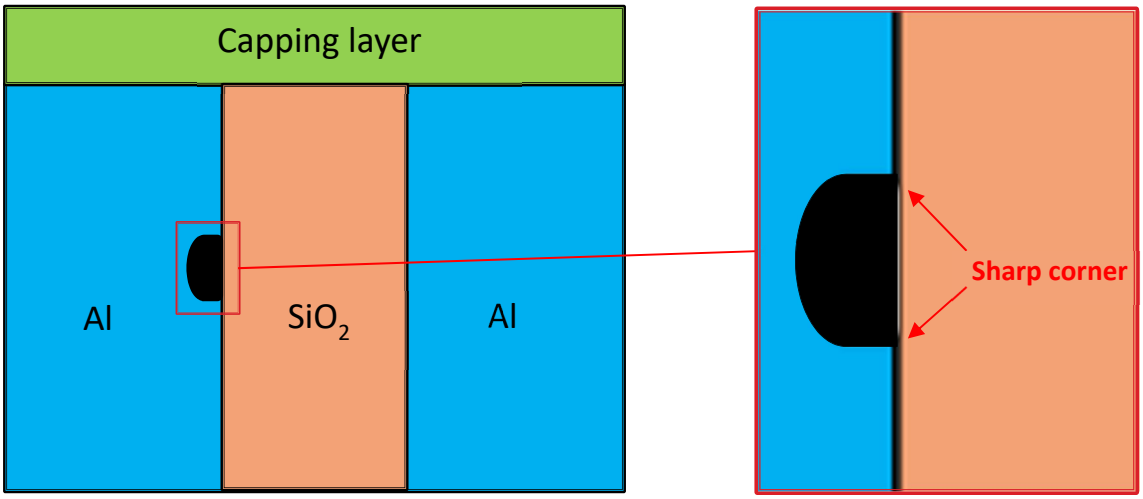

Figure 3.4 Schematic of defect existing in metal line

Figure 3.4 is a schematic of void existing inside Al metal lines at Al/SiO_2 interface. As discussed in previous chapter, two factors are affecting leakage current:

$$I = A * J(E) \qquad (8)$$

where *A* is current injection area and *J(E)* is current density which is exponentially affected by electric field. When defects, such as voids, exist in Al metal lines, electron injection area is reduced because electron cannot inject into dielectric through voids. However,

when there is a void in metal lines, sharp corners are created due to the shape of void (zoomed image of Figure 3.4) and high local electric field will concentrate at sharp corners [74]. Electric field distribution of a void locate inside meta line is simulated by COMSOL during the study. As seen in Figure 3.5, simulation indicates that when average applied electric is 4MV/cm, local electric field at sharp corner of void can reach 11.7MV/cm. Based on the shape of the void, local electric field around void can vary. But this shows

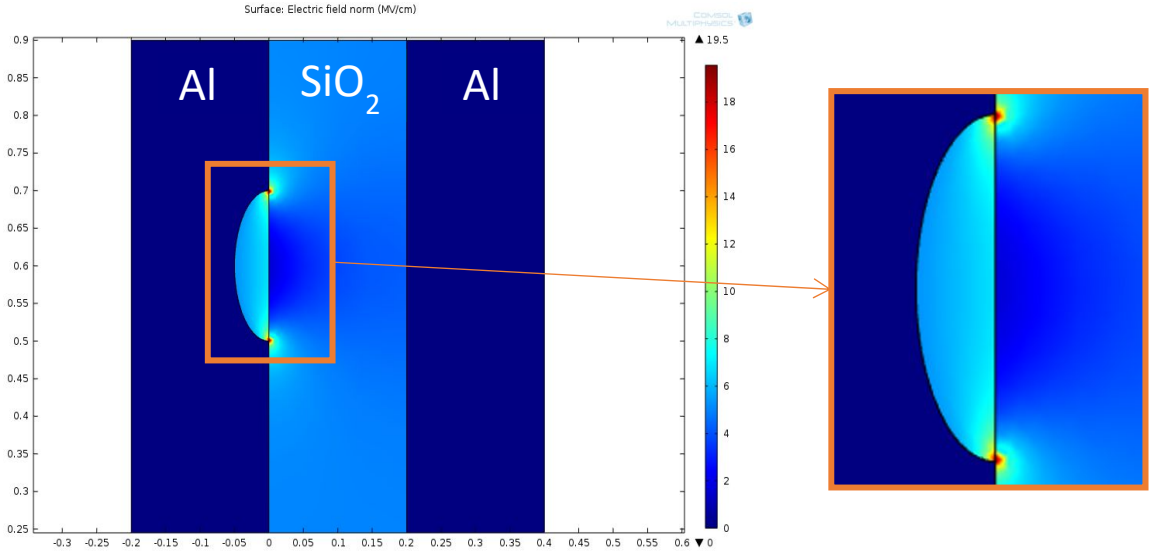

Figure 3.5 Simulation of electric field distribution around void

an overall trend that electric field at sharp corner created by voids tend to have much higher local electric field than smooth Al/SiO_2 interface. Since current density is exponentially affected by electric field, with defect existing at metal line, current density is expected to be higher due to high local electric field. Therefore, compare to samples without defects, samples with defects in metal lines are having smaller electron injection area and larger current density. As these two factors are competing against each other,

at low voltage (electric field), electron injection area is the dominant factor and leakage current is reduced. However, at high voltage (electric field), current density is dominant factor because it is increases exponentially with electric field, which will lead to higher leakage current. Therefore, I-V curve result indicates that edge sample might have defects in metal lines.

3.3.2 SEM Inspection on As-received Samples

To confirm the result from I-V curve measurement, a series of SEM inspection were done on samples from edge locations at as-received condition. As mentioned in previous paragraph, capping layers that were on top of Al/SiO_2 interconnects were removed by chemical etching method and it is important to have a thin layer of capping layer remaining on samples that serves as a protective layer from etching so that voids seen in the metal lines do not come from etching.

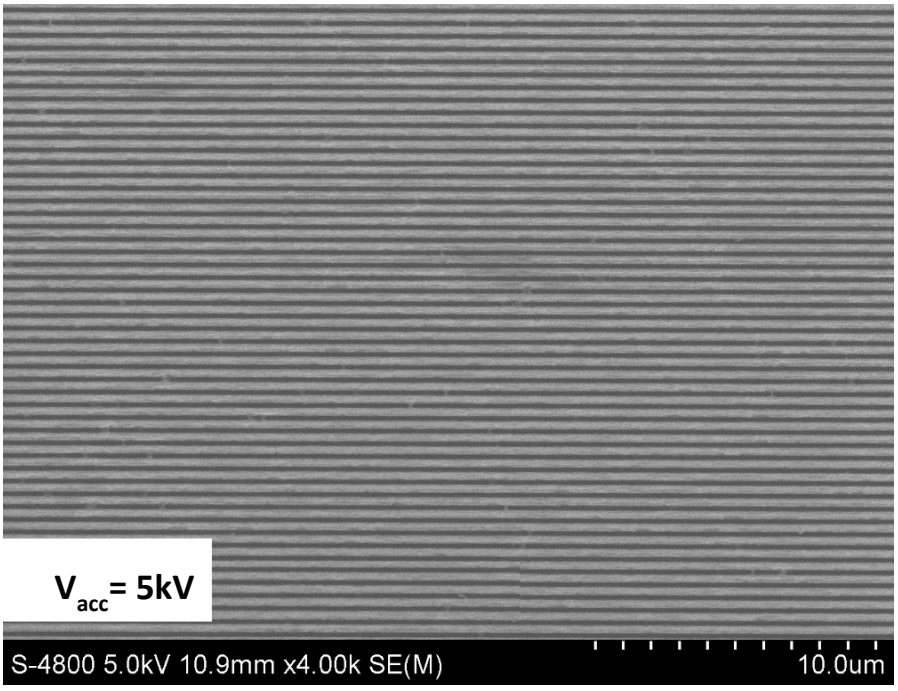

Figure 3.6 Top-down view SEM on edge sample at low acceleration voltage

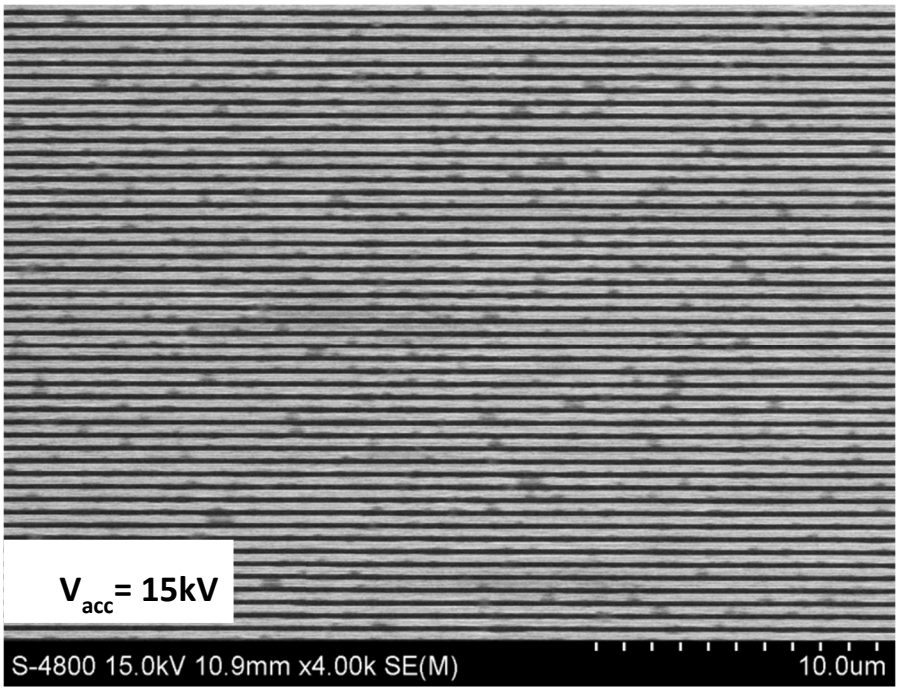

Figure 3.7 Top-down view SEM on edge sample at high acceleration voltage

To prove that etching does not create voids in metal lines, a set of SEM images that were taken from an edge sample at exact same location under different acceleration voltage are shown in Figure 3.6 and 3.7. In the images, lines with bright contrast are Al and lines with dark contrast are SiO_2. In Figure 3.6, when acceleration voltage is 5kV, no voids can be seen in metal lines. However, in Figure 3.7, when acceleration voltage is 15kV, voids (dark contrast in Al metal lines) can be seen all over the patterns. Since the penetration depth of SEM detection is proportional to acceleration voltage, no voids seen at low acceleration voltage indicates that voids are not on the surface of sample, instead voids are beneath capping layer because they can only be seen under high acceleration voltage. Since chemical etchant can only contact the surface of metal lines during etching

process, voids seen in the research are pre-existing defects that do not come from chemical etching.

Figure 3.8 Top-down view SEM on edge sample at as-received condition

During SEM inspection, center samples contained few or no defect in metal lines while edges contained a noticeable amount of voids in metal lines. Figure 3.8 is a top-down SEM images taken from an edge sample at as-received condition. In the image, voids and the sharp corners created by them can be seen in metal lines. This corresponds well with the result from I-V curve measurement indicating that edge samples have pre-existing defects in Al metal lines.

3.3.3 I-V Curve Measurement of Aging Samples

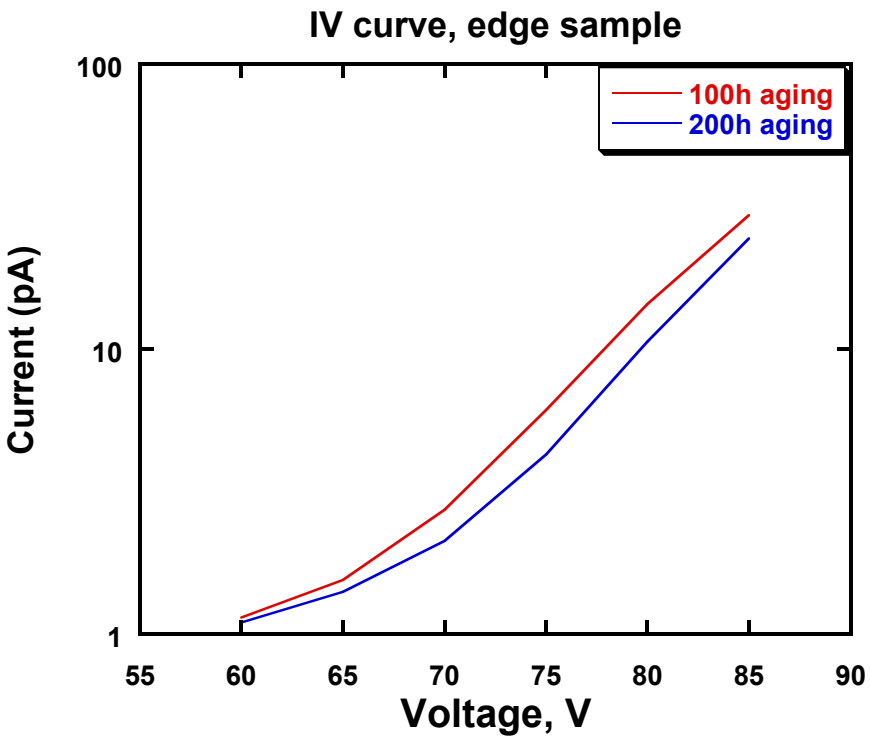

Figure 3.9 Typical I-V curve of edge sample after 100 and 200 hours aging

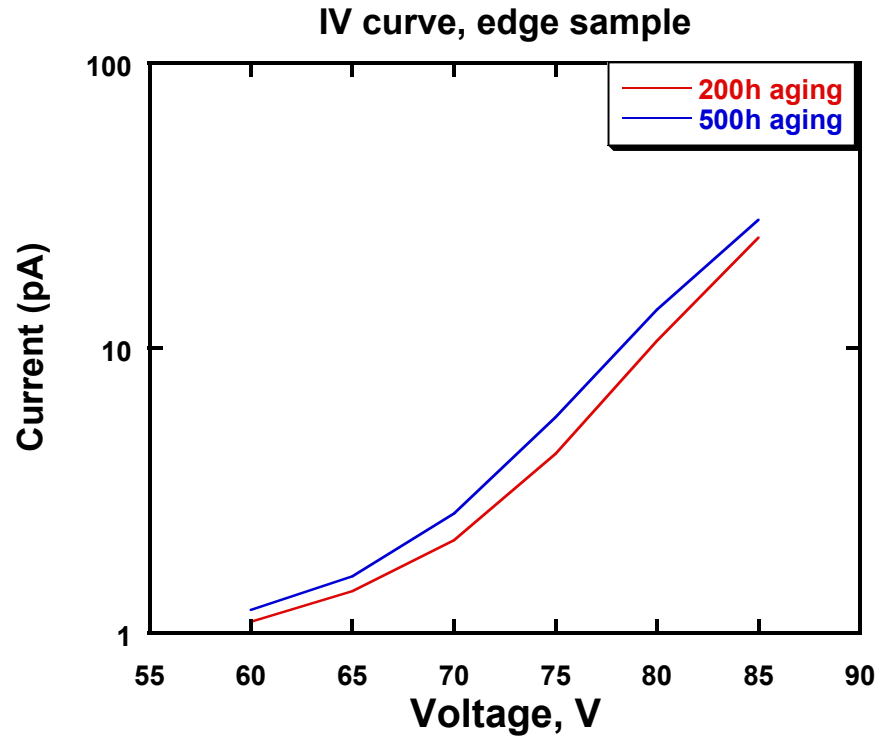

Figure 3.10 Typical I-V curve of edge sample after 200 and 500 hours aging

To understand the relationship between I-V curve and stress induced voiding activity, a series of I-V curve measurements have been done on samples that go through aging procedure. During measurement, center and edge samples all showed a certain trend in I-V curve and a set of data has been plotted in Figure 3.9 and Figure 3.10 as an example. Dielectric width of samples is 0.21um, test temperature is 50^{o}C and aging temperature is 185^{o}C. Since 5V to 45V data does not show much variation over aging time, plots are focused on 50 to 85V where noticeable change in I-V curve can be observed.

Figure 3.9 indicates that from 100 hours to 200 hours aging, I-V curve decreases at high voltage domain (50 – 85V). However, Figure 3.10 indicates that from 200 hours to 500 hours aging, I-V curve increases at high voltage domain (50 – 85V). According the current understanding on the mechanism of I-V curve, this indicates that the amount of defects are first decreased and then increased during aging treatment. Plausible explanation is during early aging process, defects such as small voids are merging into larger voids to release tensile stress [75] and overall amount of voids are reduced. But as aging process continues, more voids are developed and therefore overall amount of voids are increased. In order to confirm this assumption. SEM inspections were done on samples with capping layer removed by FIB. Figure 3.11 and Figure 3.12 are SEM images of edge samples at as-received condition and after 500 hours aging, respectively. Figure 3.11 indicates that at as-received condition, there exist fewer voids and the size of voids is smaller. Figure 3.12 indicates that after 500 hours aging process, more voids are developed in Al metal lines and the size of voids is increased. This corresponds well with the indication from I-V curve measurement.

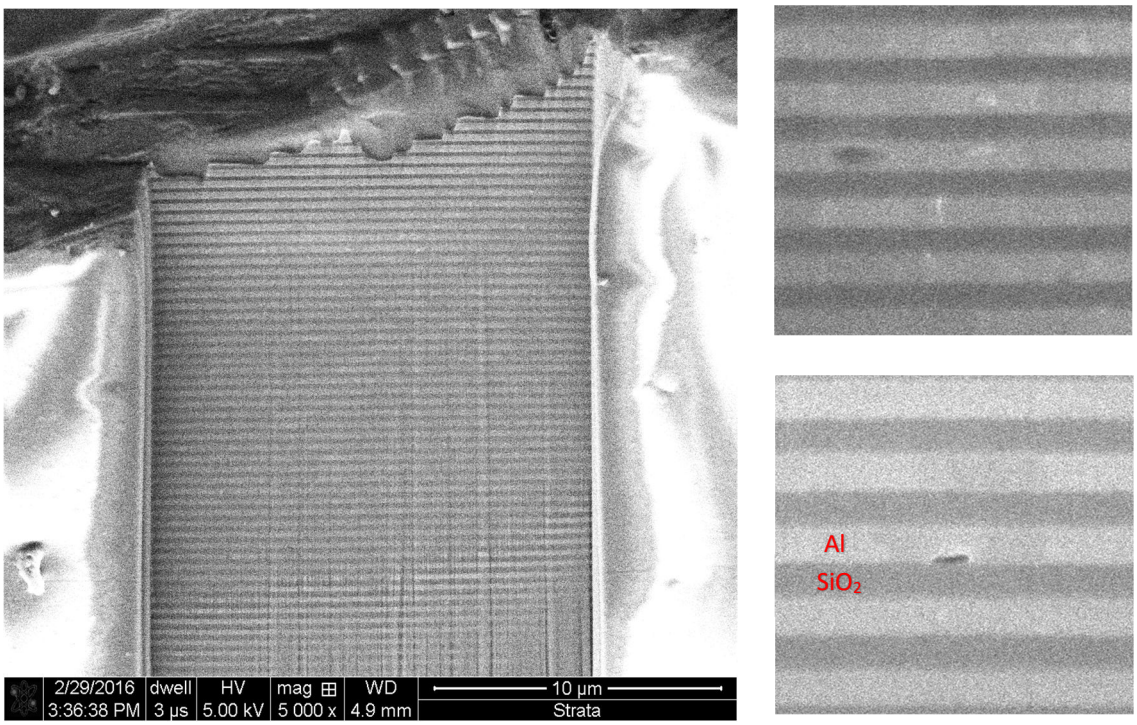

Figure 3.11 Top-down view SEM of edge sample at as-received condition

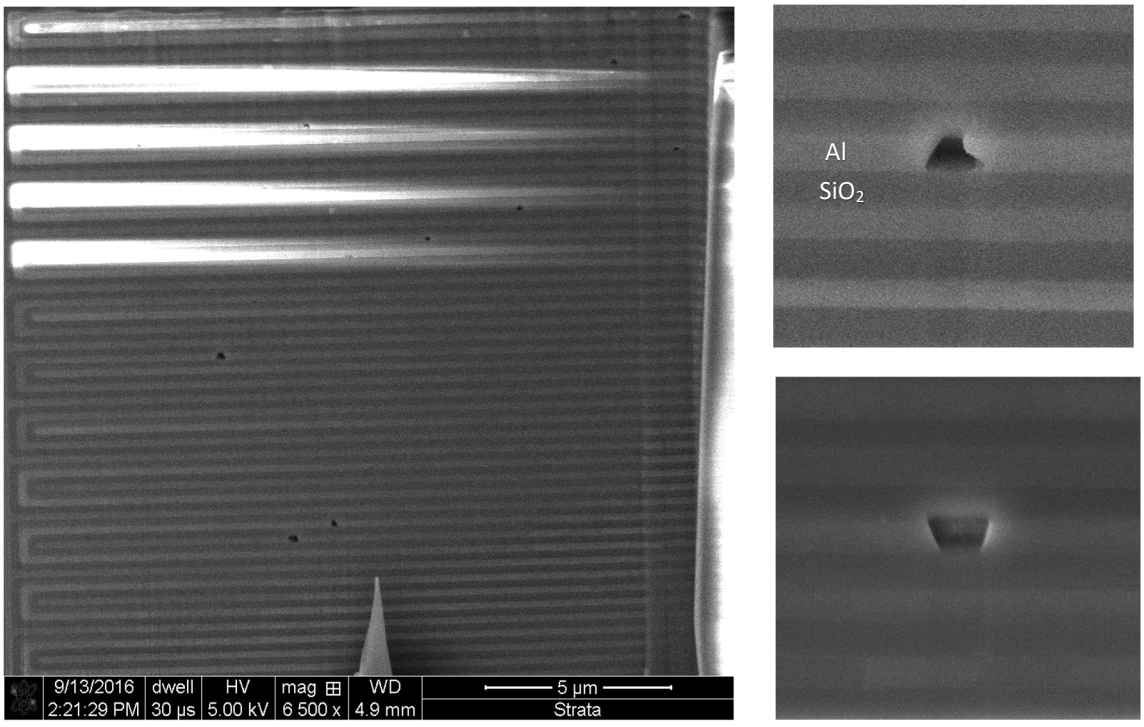

Figure 3.12 Top-down view SEM of edge sample after 500 hours aging

3.3.4 Two-point Measurement of As-received Samples

The purpose of two-point measurement is to provide a simple parameter, two-point current ratio (I_{high}/I_{low}), that can be used as an indicator for properties of metal lines in Al/SiO_2 interconnect. As discussed in previous paragraph, to larger amount of sharp corners creating higher local electric field. Therefore, compare to sample with no defect, sample with defects in metal lines is expected to show lower leakage current at low voltage due to smaller injection area and higher leakage current at high voltage due sample with defects is expected to show higher current ratio due to the larger difference between I_{low} and I_{high}.

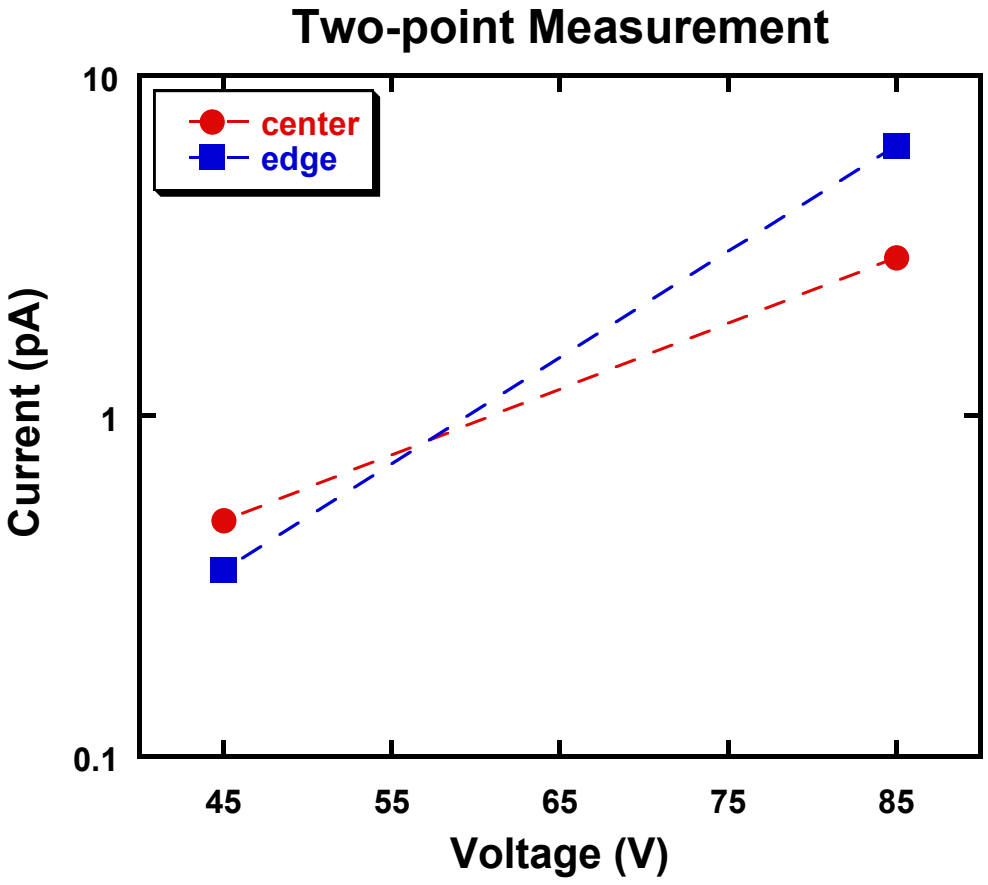

Figure 3.13 Two-point measurement of center and edge sample at as-received condition

A set of center and edge samples at as-received condition are tested and two-point measurement data has been plotted in Figure 3.13 as an example. Dielectric width of sample is 0.22um, applied voltage is 45V and 85V and test temperature is 50°C. A set of center and edge samples at as-received condition are tested and two-point measurement data has been plotted in Figure 3.13 as an example. Dielectric width of sample is 0.22um, applied voltage is 45V and 85V and test temperature is 50°C. Figure 3.13 indicates that edge sample has lower leakage current at 45V and higher leakage current at 85V compares to center sample. This result is expected and corresponds well with the result of I-V curve measurement. After calculation, current ratio of center sample is (2.92pA / 0.49pA) = 5.96 and current ratio of edge sample is (6.23pA / 0.35pA) = 17.8. This approximately 3 times difference in current ratio might indicate that edge sample has more defects in Al metal lines.

3.3.5 Two-point Measurement of Aging Samples

To further understand the relationship between two-point current ratio and stress induced voiding activity, two wafers were selected (P04 and P23) and a set of measurements were done on samples taken from center and edge locations of wafers. Dielectric width of sample is 0.22um, applied voltage is 45V and 85V (E = 2.05MV/cm and 3.86MV/cm), test temperature is 50°C, charging time is 10 minutes, discharging time is 3 minutes and aging temperature is 185°C. Two-point current ratio data has been collected from test samples (32 samples) and plotted into Figure 3.14 where each data point represents the average value of 8 samples.

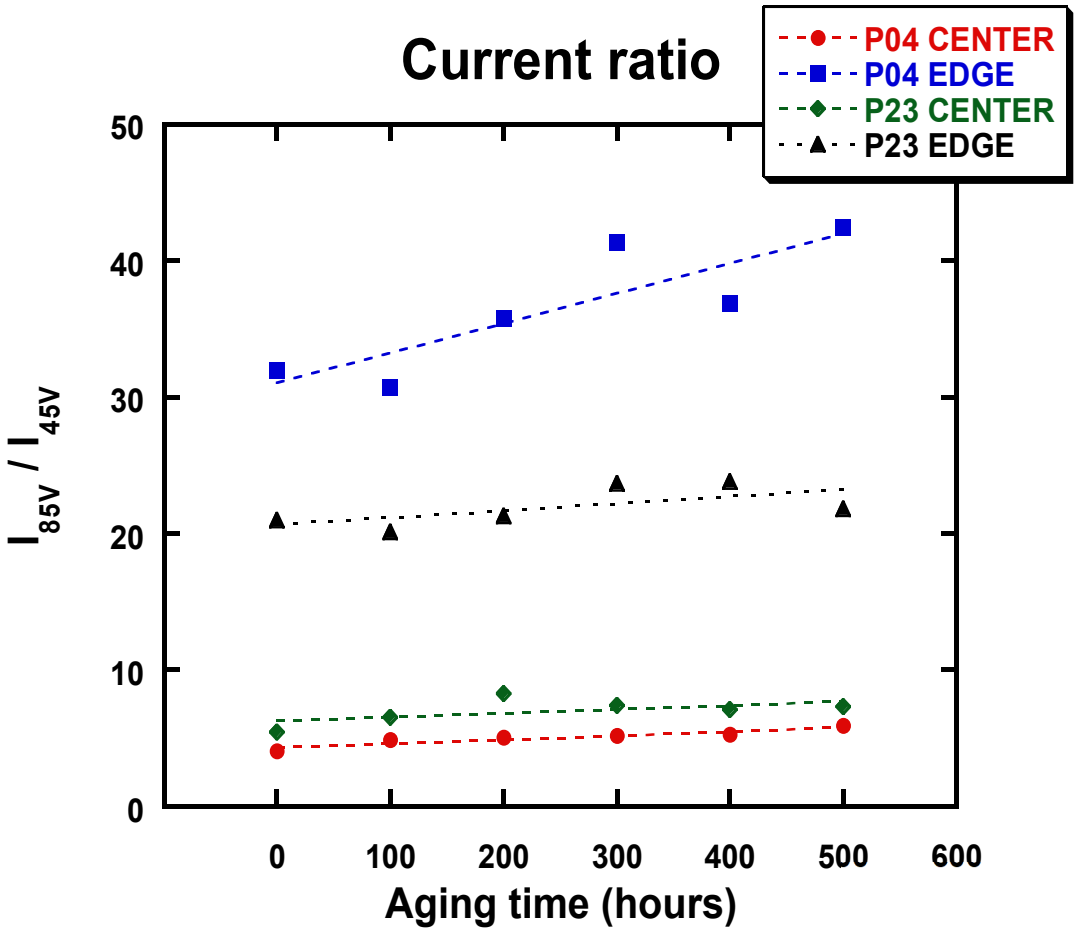

Figure 3.14 Current ratio versus aging time of center and edge samples

As seen in Figure 3.14, at time zero, current ratio of P04 center samples, P04 edge samples, P23 center samples and P23 edge samples are 4.06, 31.95, 5.42 and 20.97, respectively. Center samples have a much lower current ratio compare to edge samples. This indicates that at as-received condition, edge samples contain more defects in Al metal lines than center samples. As samples go through aging process over time, current ratio increases gradually. This indicates that stress induced voids might be developing inside metal lines. However, the increase rate of each set of samples is different. While P04 center samples, P23 center samples and P23 edge samples have more or less similar

current ratio increase rate, P04 edge samples show a higher increase rate. Based on current understanding, increase rate is related to the speed of voids developing in metal lines. It indicates that P04 edge samples might be more prone to stress induced voiding activity and the predicted metal line quality is: P04 center > P23 center > P23 edge > P04 edge.

In order to confirm the result from two-point measurement, a series of SEM inspections were done on center and edge samples from wafer P04. 3 aging conditions (o hour, 200 hours and 500 hours) were selected to show the stress induced voids development over aging time. SEM inspection result indicates that edge samples have more voids in metal lines compare to center samples at time zero, 200 hours aging and 500 hours aging. Some of the SEM images are shown in Figure 3.15, 3.16 and 3.17. Figure 3.15a and 3.15b are center and edge samples at time zero (as-received condition), Figure 3.16a and 3.16b are center and edge samples after 200 hours aging process and Figure 3.17a and 3.17b are center and edge samples after 500 hours aging process. In the images, lines with bright contrast are Al metal lines, lines with dark contrast are SiO_2 dielectric and areas with dark contrast within Al lines are voids. SEM images indicate that: 1. Edge samples develop voids at a faster rate compare to center samples over aging time. 2. Edge samples have more voids in every aging stage 3. Edge sample at time zero (as-received condition) has already developed more voids than center sample at 200 hours and 500 hours aging condition. These three observations correspond well with what two-point measurement predicted, and thus two-point current ratio might be able to serve as parameter that indicates metal lines properties.

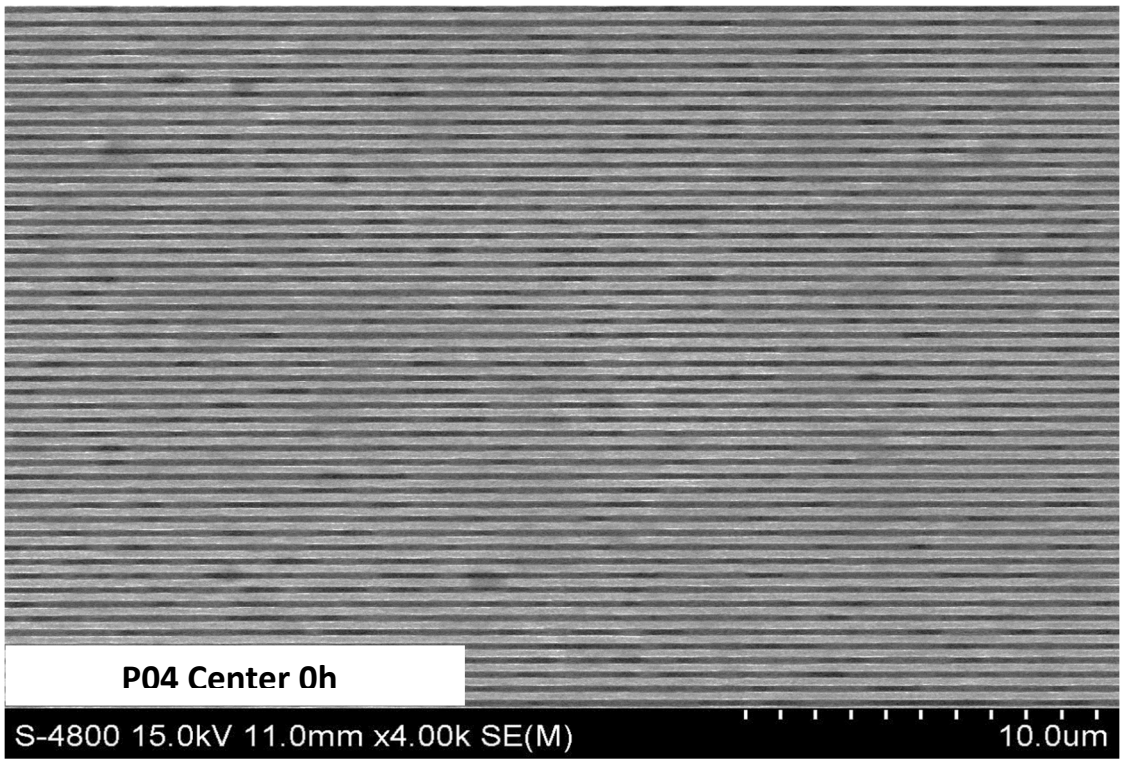

Figure 3.15a SEM of center sample at as-received condition

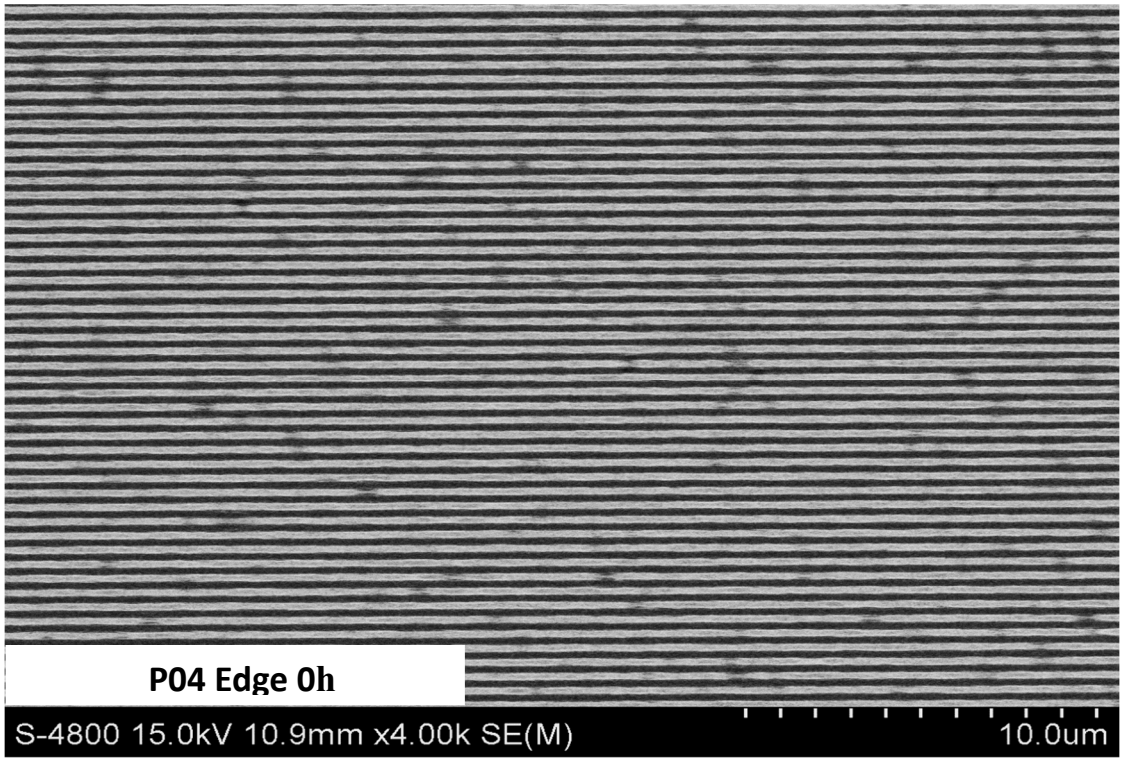

Figure 3.15b SEM of edge sample at as-received condition

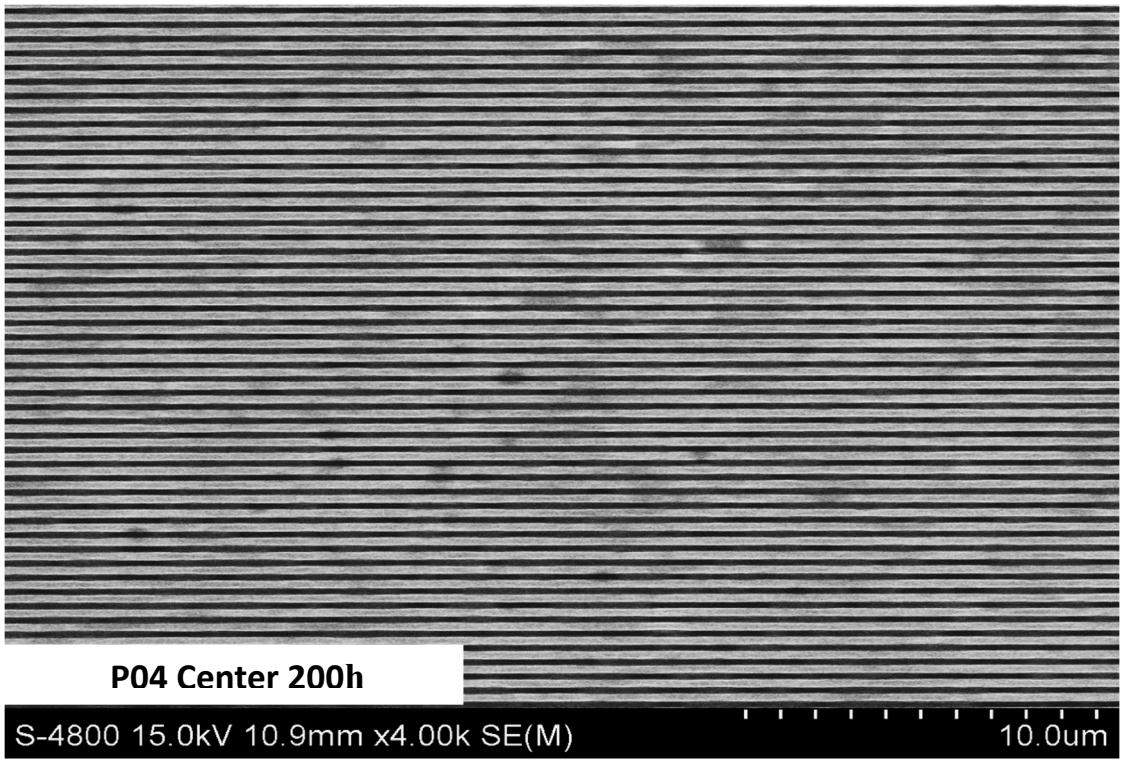

Figure 3.16a SEM of center sample after 200 hours aging

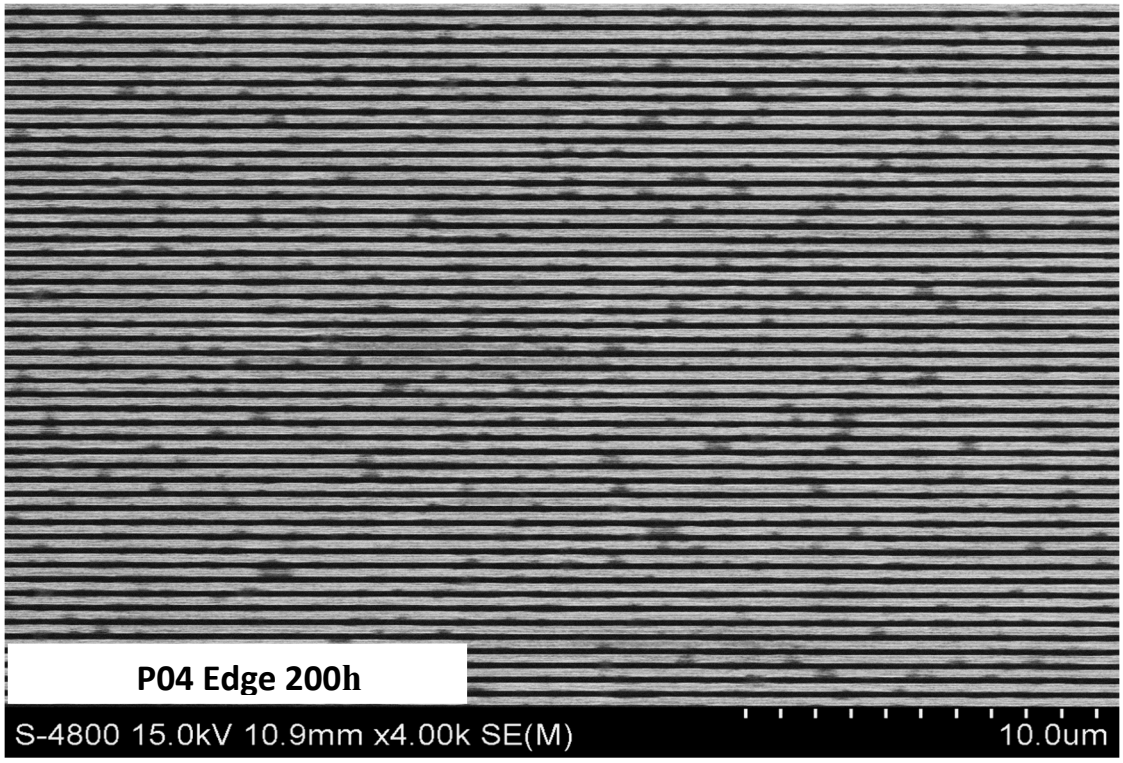

Figure 3.16b SEM of edge sample after 200 hours aging

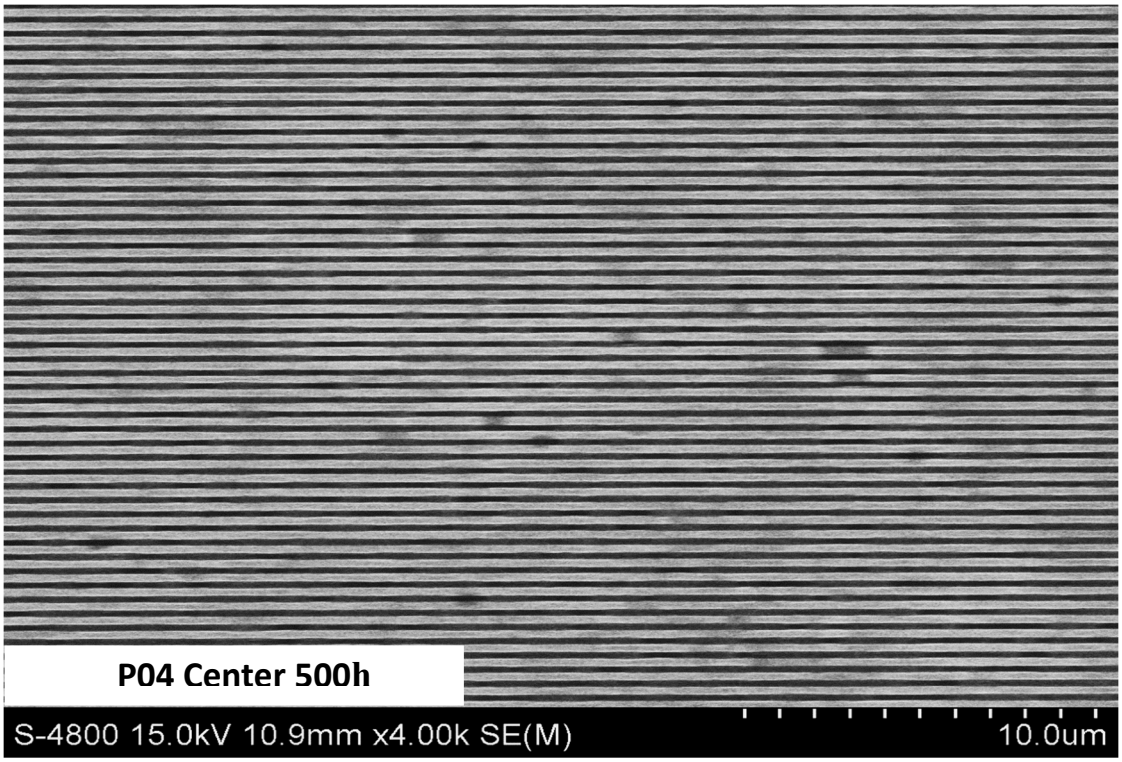

Figure 3.17a SEM of center sample after 500 hours aging

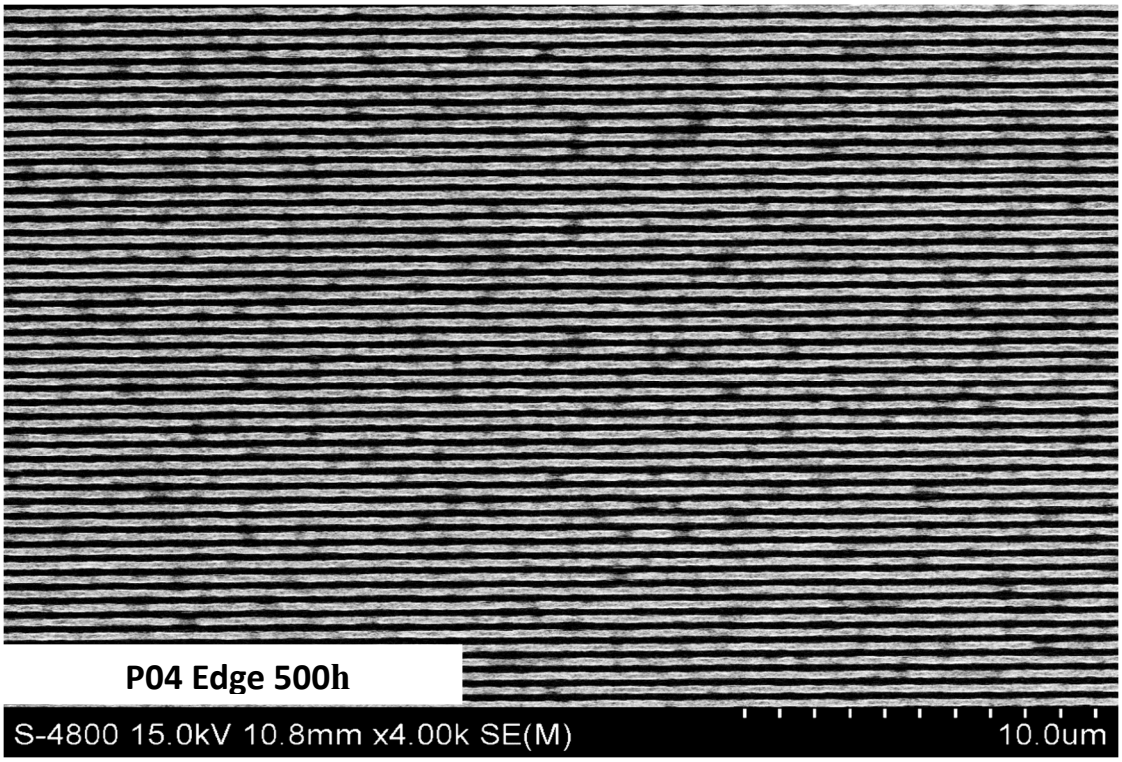

Figure 3.17b SEM of edge sample after 500 hours aging

3.4 Summary

In this chapter, I-V curve measurement and two-point measurement have been introduced and the mechanisms of I-V curve measurement and two-point measurement have been studied. These two methods have been proven by SEM inspection to be effective at detecting defects located at Al metal lines in Al/SiO_2 interconnects and a simple parameter two-point current ratio can be used to predict the properties of Al metal lines.

I-V curve measurement applies different voltage (5V to 85V) to samples and collects corresponding leakage current. I-V curve measurement data of samples at as-received condition indicates that, compare to center samples, edge samples have lower leakage current at low voltage and higher leakage current at high voltage. According to the mechanism of I-V curve measurement, it might be due to the defects locating in Al metal lines. When defects exist, they have two effects to leakage current, electron injection area is reduced but current density is increased because of high local field at sharp corners created by defects. At low voltage, effect of electron injection area is dominant and therefore leakage current reduces. At high voltage, effect of current density is dominant, and thus leakage current increases. Therefore, result of I-V curve measurement predicts that even at as-received condition, edge samples might already contain defects in Al metal lines and this is prediction is proven by SEM inspection. As for samples that go through aging process to develop stress induced voids, I-V curve measurement data indicates that both center and edge samples show a similar trend, which is I-V curve decreases at early stage of aging process and increases at later stage of

aging process. According to the I-V curve mechanism, this is due to tiny voids merging into large voids initially and then more voids are developed over aging process. This prediction is also proven by SEM inspection. Therefore, I-V curve measurement can serve as a measurement technique that can reveal the properties of Al metal lines.

Two-point measurement applies two voltage (45V and 85V) to samples and collects corresponding leakage current. For samples at as-received condition, two-point measurement data indicates that current ratio of edge samples is approximately 3 times larger than center samples. According two-point measurement mechanism, this is possibly due to defects that exist in Al metal lines. Edge samples that contain defect in Al metal line is expected to have lower leakage current at low voltage and higher leakage at high voltage, which gives a higher current ratio. This result corresponds well with what I-V curve measurement predicts. For samples that go through aging process, edge samples show a higher current ratio and higher increase rate of current ratio over aging time. This indicates that edge samples might be more prone to stress voiding and overall have worse properties compare to center samples. The prediction is then proven by SEM inspection, and thus current ratio collected from two-point measurement might serve as an indicator for Al metal lines properties.

CHAPTER 4

DISCHARGE TRANSIENT CURRENT MEASUREMENT AND ITS SENSITIVITY TO STRUCTURAL DEFECTS IN DIELECTRIC LAYERS OF AL/SIO_2 INTERCONNECTS

4.1 Background

Thin film SiO_2 are a crucial part of Al/SiO_2 interconnect as they serve as insulating materials to prevent Al metal lines from short circuit. Therefore, to achieve good interconnect integration, quality control of SiO_2 dielectrics is one of the key factors. However, the quality of dielectric layer is affected by many factors and can vary between different wafers and locations within wafer. This results in a significant variation in reliability performance, such as dielectric breakdown and high leakage current, for different wafers. As interconnects continue to scale down to improve communicating speed, variation in reliability performance has become more severe as high aspect ratio of interconnects can lead to impartial filling of the space between Al metal lines which will create voids [76], as shown in Figure 1.

Therefore, detection of trapping structural defects in dielectrics is critical for maintaining excellent interconnect properties. The most efficient way to detect defects is through electrical measurement due to its simplicity and efficiency. However, conventional electrical measurement techniques, such as pattern capacitance or voltage ramp to breakdown, are influenced by many factors and do not show clear indication to defects. In another word, conventional electrical measurement techniques are not sensitive enough to detect structural defects in dielectrics. Another type of defect

detection is through microscopic technique such as TEM and SEM. Microscopic techniques can reveal defects effectively (Figure 4.1) but with the downside of time consuming and destructive to samples.

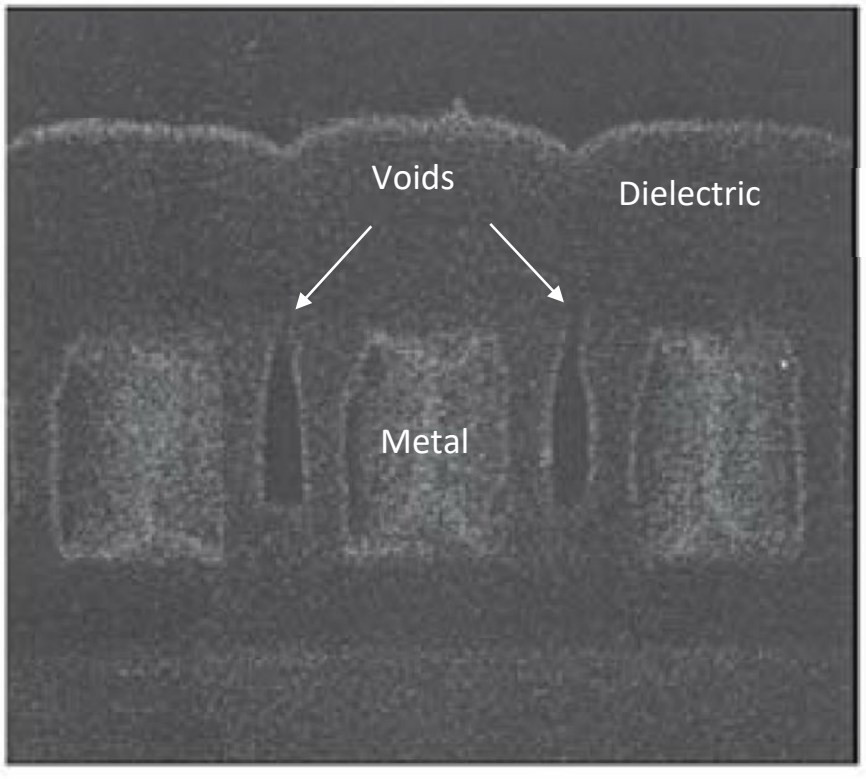

Figure 4.1 Voids in dielectric under SEM inspection [76]

The purpose of this study is to develop a detection technique that uses simple electrical measurements to obtain a single parameter which is sensitive to structural defects in dielectrics and can be used as parameter indicative of dielectric defects. Proposed technique is called discharge transient current measurement. During the research, discharge transient is quantified and found to be highly sensitive to structural defects in dielectrics.

Discharge transient current is also known as dielectric absorption current [77]. During charging process, charge carriers inside dielectrics will migrate based on applied electric field direction. When electric field is removed (short to ground) during discharging process, charge carriers displaced during charging process will back-diffuse to equilibrium state and generate discharge transient current. If there exist defects, such as voids, in dielectrics, charge carriers' back-diffusion path will be hindered and therefore transient current will decrease. Therefore, dielectric with more defects is expected to have smaller discharge transient current.

Unlike normal dipole polarization or depolarization, relaxation time of discharge transient current is much longer [77]. Relaxation time refers to the time required for charge carriers inside dielectric to return to their equilibrium state. Typical relaxation time of dipole polarization and depolarization process seen in this research is ~10^{-5}s (RC delay = 10^{6}ohm * 10^{-11}C) and is too fast for HP4140B pA meter to collect. Therefore, all discharge current data collected in the research is most likely coming from discharge transient current.

Besides discharge transient current measurement, thermally stimulated depolarization current measurement (TSDC), capacitance measurement and time dependent dielectric breakdown test (TDDB) are also implemented in the research to serve as aiding technique that helps to achieve better understanding of the mechanism of discharge transient current. In later paragraph, these three techniques will be briefly introduced.

4.1.1 Thermally Stimulated Depolarization Current

TSDC is an ideal method to reveal the nature of charge carriers [78,79] that contribute to discharge transient current. The basic principle of this technique is to "freeze" polarization dipoles by rapid cooling and "thaw" polarization dipoles by slow heating. Polarization dipole is referring to the charge carrier contributing to discharge transient current. Initially, sample is polarized under a constant electric field at an elevated temperature and dipoles inside dielectric will form a metastable polarization state. Then the temperature is rapidly cooled to a lower temperature and those polarized dipoles are frozen inside dielectric. Electric field is then removed and temperature is increased at a constant rate, eventually frozen dipoles will gain enough thermal energy and return to their equilibrium state. The process where dipoles return to equilibrium will generate a small amount of current and this is known as TSDC. Different types of polarization dipoles have different TSDC trend, and thus TSDC can be used to determine the source of polarization dipole.

Typically, there are three types of dipoles that might exist in dielectric and contribute to dielectric relaxation process: defect dipoles, trap charges and mobile ions [80]. Defect dipoles, created by impurities substituting cations or anions in dielectric crystal structure, are observed and studied by Bucci and Fieschi [78,79] with TSDC technique. Trap charges refer to electrons or holes that loss their energy and are trapped to defect sites or impurities. After gaining enough energy, these charges can escape from energy trap and become mobile charge carriers. Relationship between trap charges and TSDC was studied by Randall and Wilkins [81], they assumed that TSDC peak intensity is

proportional to the rate of trap charges being thermally activated at heating up process. Mobile ions are atoms or molecules with net electric charges due to the loss or gain of electrons. Under applied electric field, mobile ions will migrate towards electrodes and accumulate at the sidewalls of dielectrics. When temperature is rapidly decreased, mobility of mobile ions will be drastically reduced [82]. After external electric field is removed and temperature starts to increase, these mobile ions' mobility will recover and ions will be back-migrating due to the internal field created by uneven distribution of electrical charges inside dielectrics. This back-migration process will create TSDC peak.

4.1.2 Capacitance Measurement

Capacitance versus frequency measurement is another idea method of revealing the nature of charge carriers contributing to discharge transient current. Al/SiO_2 interconnect can be considered as a simple capacitor that has two electrodes (Al metal lines) and one dielectric (SiO_2). If capacitor is charged with DC bias, capacitance is a fixed value following equation

$$C = Q \,/\, V \qquad (12)$$

Where C is capacitance, Q is the charge held by capacitor and V is applied voltage. However, if capacitor is charged with AC bias, applied voltage signal is continually changing between positive and negative polarity with certain frequency and capacitance become a value dependent of AC bias frequency. This is due to capacitive reactance which acts as an opposition to the change of voltage applied to capacitor. Reactance follows equation

$$Xc = 1 / 2\pi fC \qquad (13)$$

Where Xc is reactance of capacitor, f is frequency of AC bias and C is capacitance. Reactance is not the only factor that determine the relationship between capacitance and AC bias frequency. Another key factor is the origin of the dielectric polarization in capacitor. Dielectric polarization is the reason capacitor can hold charges under applied electrical bias, it can be defined as the displacement of charged particles (atoms, molecule, ions, electrons or holes) under applied electric field. There are four types of dielectric polarization: electronic polarization, ionic polarization, dipolar polarization and space charge polarization.

Electronic polarization refers to the displacement of positively charged nucleus and negatively charged electrons of atom. When there is no external electric field, atom is in equilibrium state with nucleus surrounded by electrons (Figure 4.2a). When an external field is applied, negatively charged electrons will shift with respect to positively charged nucleus and atom become polarized because of the uneven distribution of nucleus and electrons (figure 4.2b).

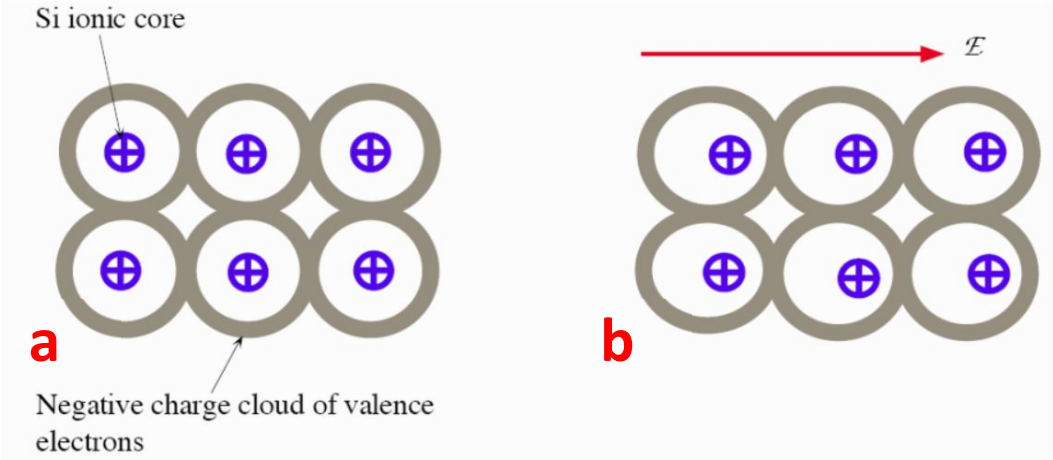

Figure 4.2 Schematic of electronic polarization [83]

Ionic polarization refers to the relative displacement of positive ion and negative ion in an ionic bond molecule. This type of polarization is usually observed in ionic crystal such as NaCl, KCl and LiBr. When there is no external field, dipole moments of positive ion and negative ion are canceling out each other because they have same value but opposite direction, as seen in Figure 4.3a. When an external field is applied, positive ion will displace towards negative electrode (or negative ion will displace towards positive electrode, depends on the type of ion) and relative position of positive and negative ion will be changed, as seen in Figure 4.3b.

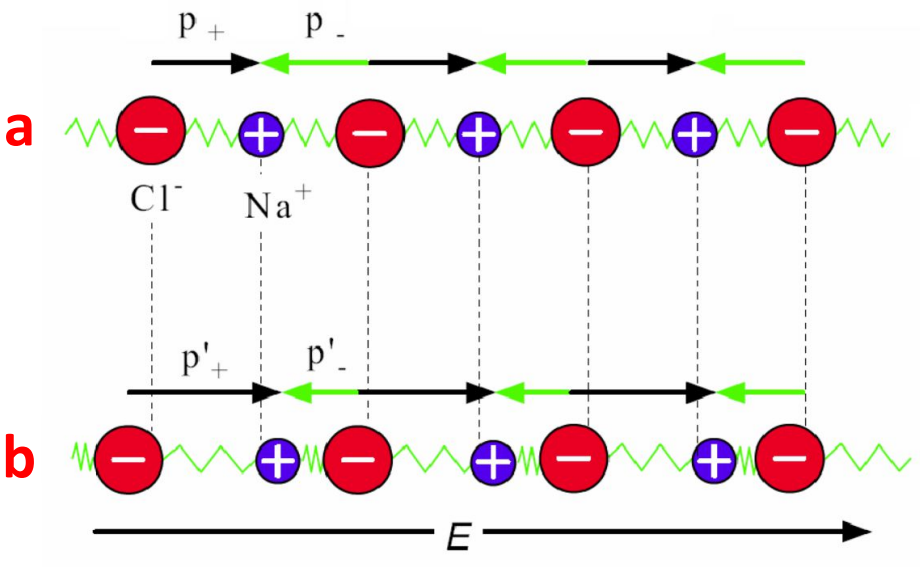

Figure 4.3 Schematic of ionic polarization [83]

Dipolar polarization, also known as orientational polarization, refers to the alignment of polar molecule under electric field. Atoms in polar molecule usually have different degree of attraction to electrons (electronegative) and if one atom attracts electrons more, it become more positive compare to another atom which attracts electrons less. This type of polarization is usually observed in covalent bond materials

such as H_20, CO and HCl. When external field does not exist, unlike other types of polarization, net dipole moment of each polar molecule is not zero. This is because charges are not evenly distributed among atoms, as seen in Figure 4.4a. However, in the dielectric, overall net dipole moment of all polar molecules combined is equal to zero due to thermal agitation, which mean average net dipole moment of each molecule is zero, as seen in Figure 4.4b. When an external field exists, molecule will rotate to align with the electric field, as seen in 4.4c. This will cause the overall net dipole moment of all polar molecules combined to be non-zero and average net dipole moment of each molecule is not zero, as seen in Figure 4.4d. Since SiO_2 is a non-polar molecule, it is not likely to observe dipolar polarization in Al/SiO_2 interconnects.

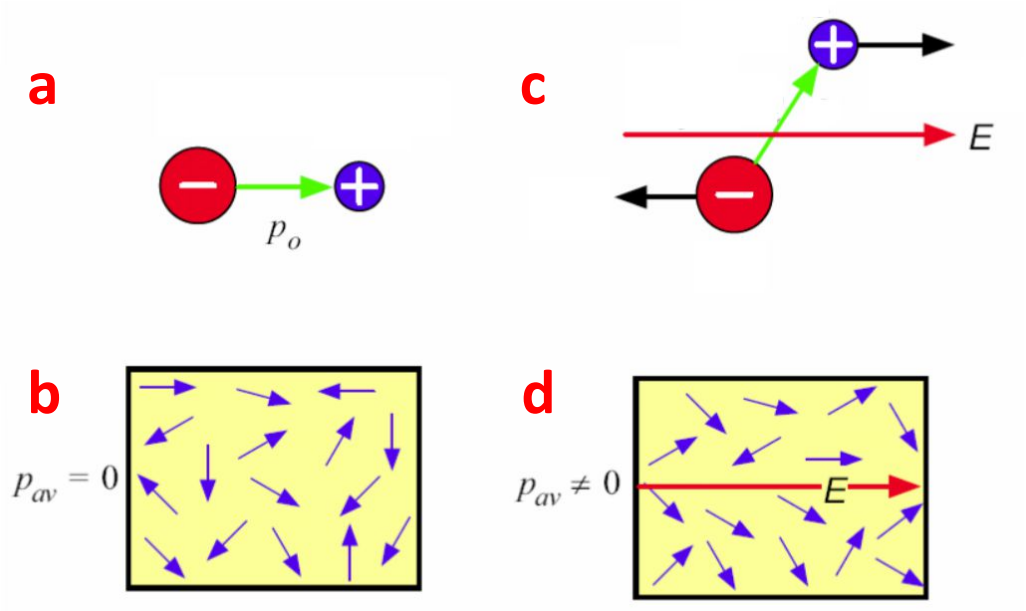

Figure 4.4 Schematic of dipolar polarization [83]

Space charge polarization refers to the displacement of mobile ions inside dielectrics. Mobile ion can be any particle that carries electrical charges, such electron, hole and atom or molecule that lost or gained electrons. Assume a dielectric with equal

number of mobile positive ions and fixed negative ions. Without external electric field, positive ions are randomly distributed inside dielectric to reach equilibrium state, as seen in Figure 4.5a. When an external field is applied to dielectric, positive ions will migrate to cathode electrode under field stress and accumulate at the sidewall of dielectric, as seen in Figure 4.5b. Space charge polarization is commonly seen in metal interconnect as impurities in dielectric can be ionized and become mobile ions, which can migrate inside dielectric under high electric field. Common impurities seen in dielectrics include H, N, H_2O and Si-OH groups [84].

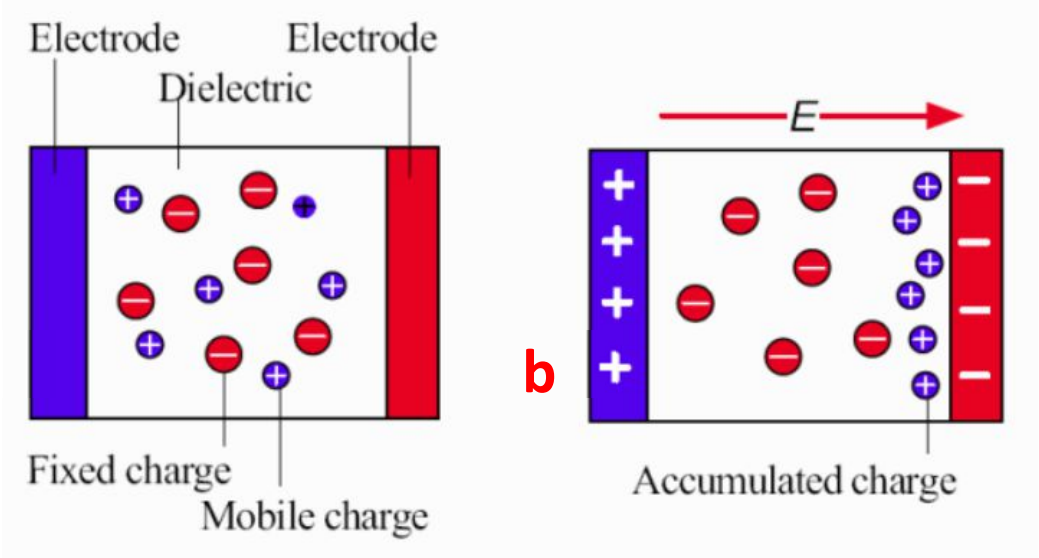

Figure 4.5 Schematic of space charge polarization [83]

4.1.3 Time Dependent Dielectric Breakdown

Time dependent dielectric breakdown (TDDB) test is one of the most common methods used to predict the reliability of electronic components, such as gate oxide of front-end-of-line transistor and dielectric oxide of back-end-of-line interconnect. Unlike

immediate breakdown which is caused by applying electric field that is higher than dielectric strength, TDDB refers to the breakdown that occurs after a long-time application of relatively low electric field (lower than critical value) due to the degradation of dielectric overtime. TDDB is a major concern in front-end-of-line transistor because high electric field is presented in the thin gate oxide. However, for back-end-of-line interconnect, it had not been a major concern until recent years. This is because SiO_2 dielectrics used in interconnects have good insulating properties and electric field across dielectric is much lower than gate oxide. But as integrated circuit on chip continuously decreases in size to reduce power consumption [92], electric field across dielectric can reach 1MV/cm and the chance of TDDB occurring in interconnect is greatly increased [37].

When considering the reliability of oxide TDDB, maximum failure rate accepted by the industry is that for 10 years of operation at normal voltage and temperature, at most 100 devices per million can be broken [94]. Apparently, it is not realistic to perform reliability test for ten years. Therefore, it is necessary to perform some kind of accelerated tests to speed up the failure process. Common method implemented to accelerate failure process is to apply a relatively high electric field and temperature [95]. Once TDDB data under harsh condition is collected, it will be extrapolated back to real operating condition and thus TDDB lifetime of electrical components can be obtained.

TDDB is a statistical phenomenon, meaning that two identical electronic components can be subjected to same operating condition but fail at different time [96]. Therefore, TDDB test usually requires a lot of samples to get any meaningful prediction. Common terms to describe TDDB includes: cumulative distribution function (CDF),

reliability function, probability function (PDF) and failure rate. CDF refers to percentage of samples that has failed before time *t* and can be described as *F(t).* Reliability function refers to percentage of samples that survived until time *t* and can be described as

$$R(t) = 1 - F(t) \qquad (14)$$

where *R(t)* is reliability function and *F(t)* is CDF. PDF refers to the percentage of sample failing at certain time t and can be described as

$$f(t) = dF(t) \,/\, dt \qquad (15)$$

where *f(t)* is PDF, *F(t)* is CDF and *t* is time. Failure rate refers to the chance that a sample will fail at given time t and can be described as

$$h(t) = f(t) \,/\, R(t) \qquad (16)$$

where *h(t)* is failure rate, *f(t)* is PDF and *R(t)* is reliability function.

TDDB can be divided into two categories based on origin of breakdown: extrinsic breakdown and intrinsic breakdown. Cause of extrinsic breakdown is metal diffusion from electrode into dielectric. This is not likely to happen in Al/SiO_2 interconnect as Al can react with SiO_2 to form a layer of Al_2O_3 which creates a barrier for metal penetration into SiO_2. Therefore, main cause of SiO_2 failure is intrinsic breakdown, which is related to defect generation inside dielectric. Intrinsic model includes: E model [97-101], 1/E model [102-105], V^N model [106-109]and $E^{1/2}$ model [110-113]. Intrinsic model can be divided into two categories: field-induced model and current-induced model.

E model [97-101] is also known as thermochemical model. This is a field-induced model that suggests Si-Si bonds and Si-O coordination in SiO_2 dielectrics might break under high electric field and temperature and become defects. When Si-Si bond or Si-O coordination is broken, oxygen vacancies will be created and act as defects. With enough defects, a percolation path between anode and cathode can be formed and dielectric breakdown will occur. Therefore, TDDB lifetime is affected by bond/coordination breakage rate and E model TDDB lifetime follows

$$ln(TTF) \propto \frac{\Delta H_0}{K_B T} - \gamma E_0 \qquad (17)$$

where TTF is TDDB lifetime, ΔH_0 is activation energy of bond/coordination breakage, T is temperature, γ is field acceleration parameter related to dipole polarization and E_0 is electric field.

1/E model [102-105] is also known as anode injection model. This current-induced model suggests that under high electric field, large amounts of electrons are tunneling through oxide with high kinetic energy due to F-N tunneling. Due to impact ionization, when electrons are migrating towards anode electrode, some defects will be formed and when electrons hit anode electrode, kinetic energy is transferred into thermal energy and holes are created. Holes will then tunnel back into dielectric and create more defects. TDDB lifetime of 1/E model follows

$$TTF = \tau_0(T) * exp[\frac{G(T)}{E_0}] \qquad (18)$$

where TTF is TDDB lifetime, $\tau_0(T)$ is temperature dependent factor, $G(T)$ is factor associated with electron and hole tunneling and E_0 is electric field.

V^N model [106-109], also known as anode hydrogen release mode, is a current-induced model similar to 1/E model except hydron ions are migrating through dielectric instead of electrons. This model is used to predict TDDB lifetime of ultra-thin (<4nm) metal-insulator-semiconductor (MIS) structure, such as Al-SiO_2-Si, instead of metal-insulator-metal (MIM) structure used in the study. Under high electric field, Si-H bonds at Si/SiO_2 interface will break and hydrogen ions will migrate into dielectric and break other weak chemical bonds during impact, which will create defects in dielectrics and eventually lead to breakdown. TDDB lifetime of V^N model follows

$$TTF = B_0(T) * V^{-N} \qquad (19)$$

where TTF is TDDB lifetime, $B_0(T)$ is factor associated with hydrogen ion migration, *V* is voltage and *N* is experimental value between 40 and 48. This model might not be applicable to Al/SiO_2 as it can only predict MIS structure with dielectric width smaller than 4nm (sample used in the research has MIM structure with dielectric width of 210nm).

$E^{1/2}$ model [110-113] is a current-induced model that was developed to predict the TDDB lifetime of low-k materials. Low-k materials refer to materials that has dielectric constant smaller than SiO_2 (k=4.2). This model assumes that dielectric breakdown is caused by current flowing through the dielectric. For high quality SiO_2 dielectric, main conduction mechanism is F-N tunneling, but for low quality SiO_2 or low-k dielectric, main

conduction mechanisms are either P-F emission or Schottky emission. TDDB lifetime of $E^{1/2}$ model follows

$$TTF \propto \exp\left(\frac{Q_{bh}-\lambda\sqrt{E}}{k_B T}\right) \qquad (20)$$

where *TTF* is TDDB lifetime, Q_{bh} is barrier height, λ is root-field acceleration parameter, *E* is electric field, k_B is Boltzmann constant and *T* is temperature.

4.2 Experimental Setup and Test Strategy

4.2.1 Test Samples

Wafers provided by Texas Instruments were used in the research. Samples taken from the wafers contain Al/SiO_2 interconnects (dielectric width = 0.21um, metal line thickness = 0.19um) which were patterned in a specific way known as comb-serpentine pattern.

4.2.2 Measurement System

In this research, several instruments were used. For discharge transient current and TSDC measurement, data acquisition system (HP4140B pA meter/DC source, probe station and PC with LABVIEW DAQ system) introduced in previous chapter was used. For capacitance measurement, a combination of data acquisition system and HP 4284A LCR meter with 20Hz to 1MHz were used (Figure 4.6). Top-down view SEM inspection were done on samples with capping layers removed by chemical etching which was introduced in previous chapter.

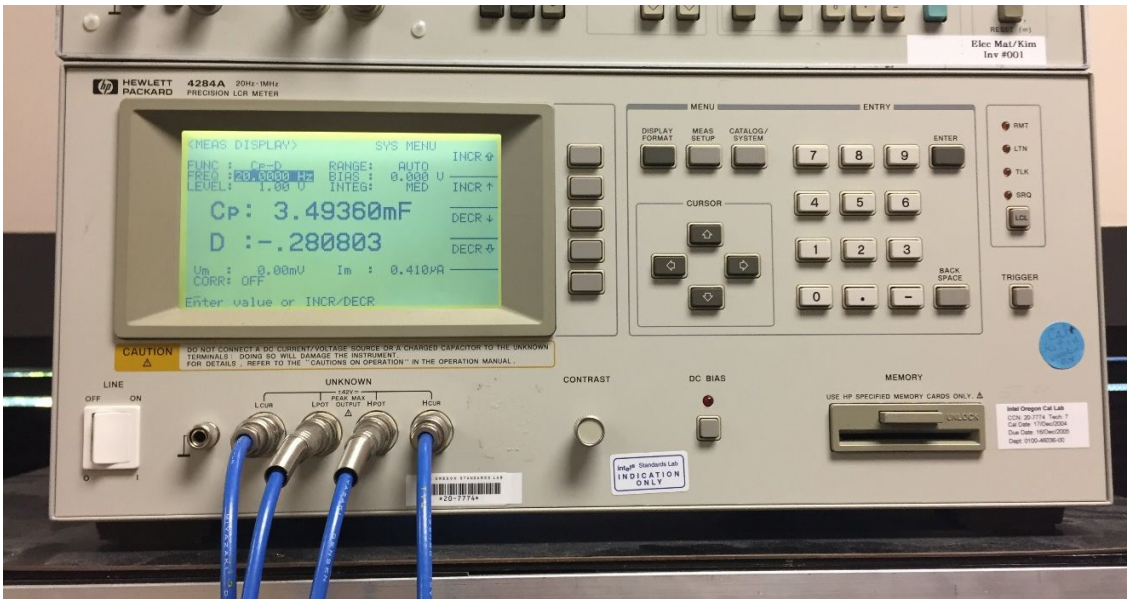

Figure 4.6 HP 4284A LCR meter

4.2.3 Sample Selection

Purpose of this research is to determine if proposed electrical measurement technique can detect defect in dielectrics. Therefore, is it important to test both samples with defect and samples without defect to compare to results. When a whole wafer is considered, usually dies from edge position of the wafers has worse properties compare to center dies [63-64]. By comparing dies from different locations, discharge transient current difference may be observed. In this research, samples from center and edge location are selected.

4.2.4 Discharge Transient Current Measurement Procedure

The goal of this measurement is to quantify amount and degree of charges stored during charging phase. Therefore, voltage (V) are applied to sample for certain amount

time (tcharge) to allow polarization, and then voltage is removed and both electrodes are grounded for certain amount of time(tdisch) and discharge current data is collected (Figure 4.7). As mentioned in previous paragraph, relaxation time of normal dipole depolarization current is in millisecond range and cannot be collected by instrument used in this research, therefore the main source of discharge current data is discharge transient current.

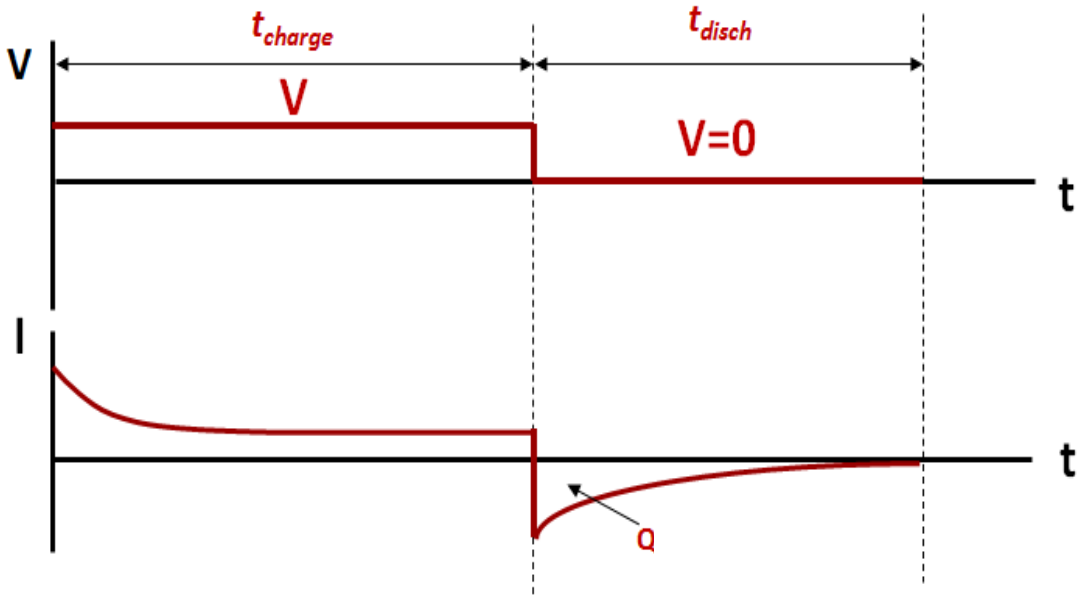

Figure 4.7 Schematic of discharge transient current measurement procedure

4.2.5 TSDC Measurement Procedure

Figure 4.8 is a schematic of the TSDC measurement procedure used in the study. Initially, applied temperature is increased to T_p from T_0, then an electric field F_p is applied to sample for certain amount of time (t_{charge} = 85 minutes). During this period, sample is cooled down gradually back to T_0. Then sample goes through discharging process for certain amount of time ($t_{discharge}$ = 6 minutes) to remove excessive charges. After that,

sample is heated up at constant rate and TSDC data can be collected by LABVIEW acquisition system. Peak of the current is defined as TSDC peak at temperature T_m.

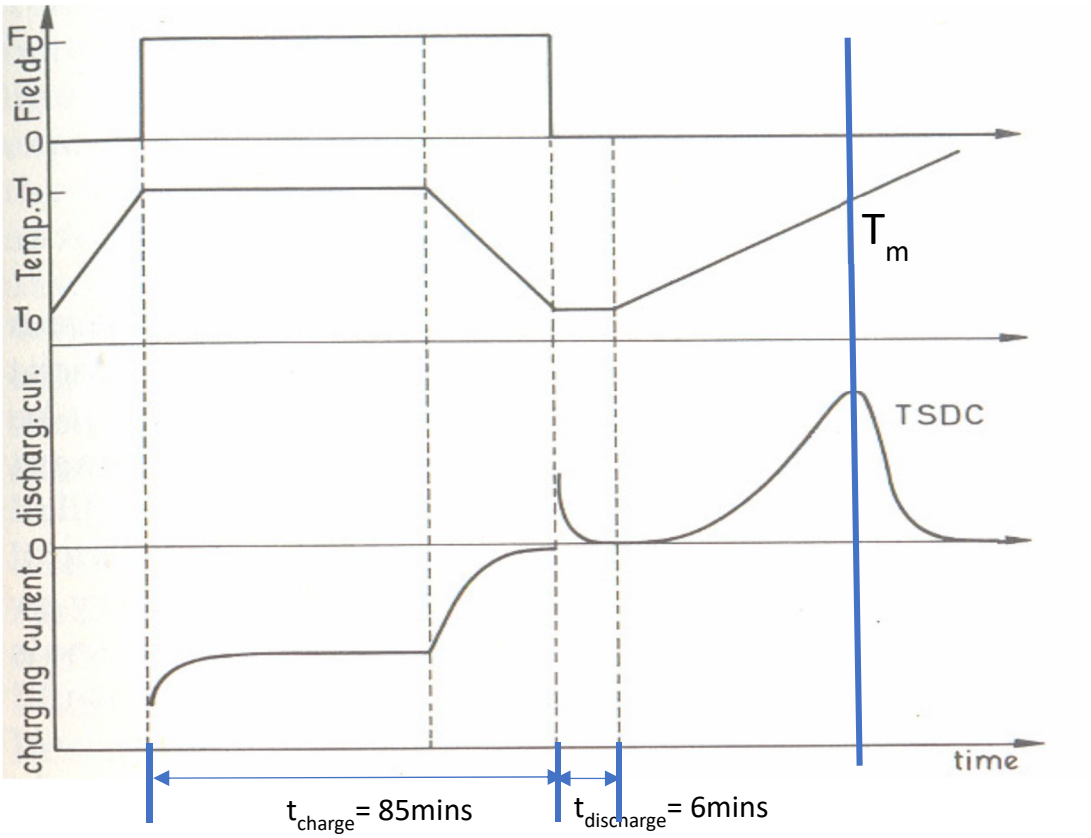

Figure 4.8 Schematic of TSDC measurement procedure [122]

4.2.6 Capacitance Measurement Procedure

Samples are tested under parallel capacitance mode with applied AC bias frequency from 20Hz to 1MHz. At low frequency (20Hz to 2kHz), scan per step is 10Hz. At mid frequency (2kHz to 10kHZ), scan per step is 100Hz. At high frequency (10kHz to 1MHz), scan per step is 1kHz. All capacitance data collected during measurement are then saved into txt file through LABVIEW DAQ system.

4.3 Result and Discussion

4.3.1 TSDC and Source of Charge Carriers

To understand the nature of charge carriers in discharge transient current, TSDC measurements have been done on samples taken from center and edge location. Figure 4.9 is a set of TSDC data collected during the study, with applied electric field Ep = 3.8MV/cm, polarization temperature Tp = 80°C, polarization time tp =85 min and heating rate β = 5°C/min.

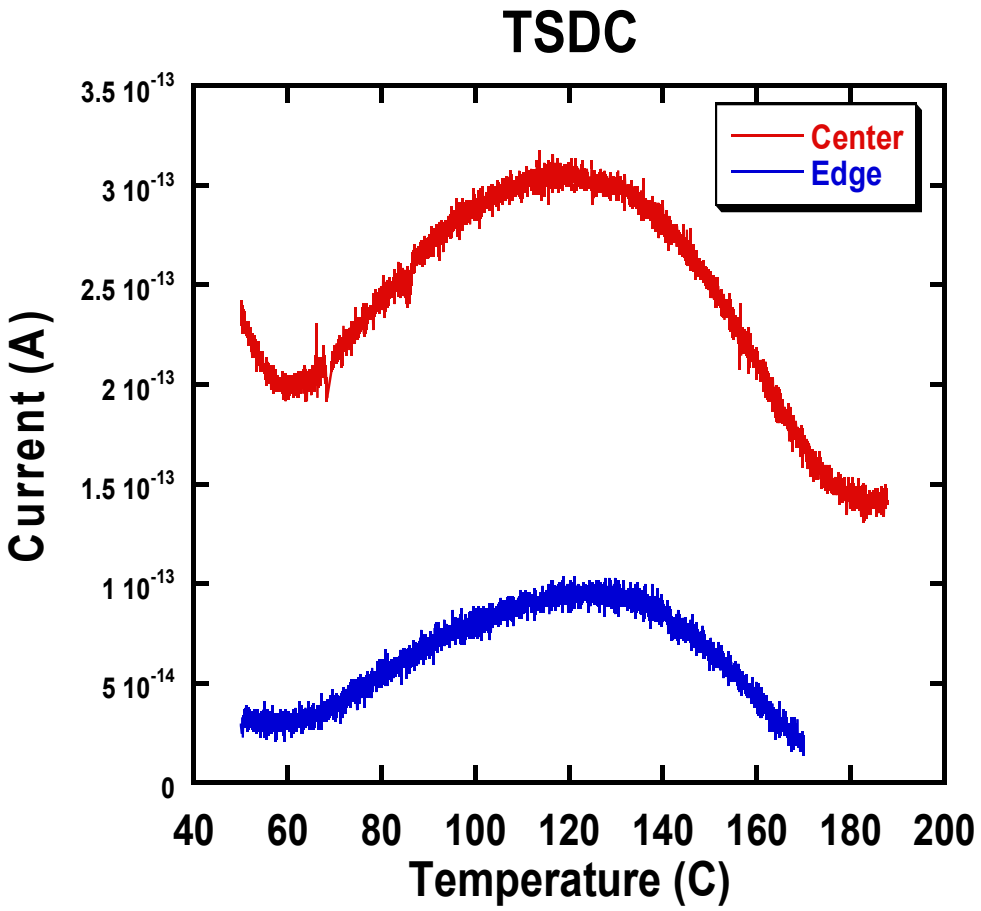

Figure 4.9 TSDC data of samples from center and edge location

From the plot, both samples indicate one clear peak at ~125^{o}C. Number of peaks represents how many types of charge carriers are contributing to the discharge transient current. Since only one peak is observed, it is likely that only one type of charge carriers is contributing to discharge transient current seen in the study. Also compares to edge sample (0.1 pA), center sample has a noticeable higher peak current (0.3pA). Since peak current is affected by number of charge carriers in dielectric, this result indicates that center sample might have more charge carriers compares to edge sample.

As discussed in previous paragraph, there are three types of charge carriers that might exist in dielectric and contribute to dielectric relaxation process: defect dipoles, trap charges and mobile ions. Defect dipoles are created by the attraction between positive and negative charges and they are the source of dipolar relaxation seen in dielectric [114-117]. Usually dipoles are created by impurities substituting cations or anions in dielectric crystal structure. Trap charges are referring to the immobilized electrons/holes that are bound to defects or impurities which act as energy trap. However, with addition of energy, such as heat or electric field, trap charges can escape from the energy trap and become mobile charge carriers. This type of charge carrier is commonly seen in dielectrics [118-120]. Mobile ions are atoms or molecules which carry positive or negative charges and will drift inside dielectric based on direction of applied electric field. This type of charge carrier is causing space charge relaxation seen in dielectric [90,91,121].

To identify which type of charge carrier is contributing to discharge transient current, a simple measurement can be done. Several research groups reported that for

each type of charge carrier, peak temperature Tm will shift to different direction when applied electric field Ep varies [121,123,124].

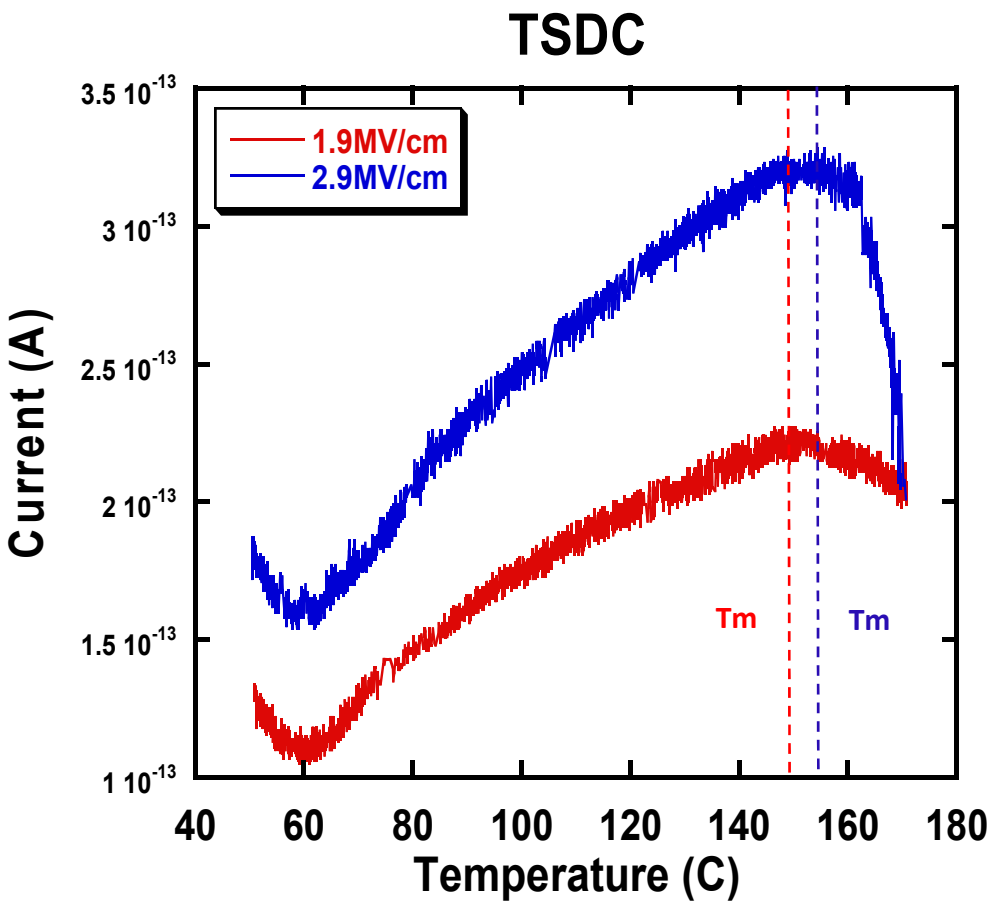

Figure 4.10 TSDC data of samples under different applied electric field

Figure 4.10 is a set of TSDC data collected during study with applied electric field Ep = 1.9MV/cm and 2.9MV/cm (sample dielectric width = 0.21um), polarization temperature Tp = 110°C, polarization time tp =85 min and heating rate β = 5°C/min. The plot indicates that as applied electric increases, peak temperature will increase. According to W. Liu [123], if the origin of charge carrier is defect dipole, applied electric

field is expected to have no effect on peak temperature. Therefore, the source of discharge transient current is not likely to be defect dipole. As for trap charge, according to Nadkarni *et al*. [124], peak temperature will shift to lower end as electric field increases. This is opposite from what the plot indicates, and thus trap charge is not likely the source of discharge transient current. Since the source of discharge transient current is not likely to be either defect dipole or trap charge, only possible source remains is mobile ion. However, this is not a sufficient evidence to prove that source of discharge current is mobile ion, and thus two measurements had been done to further confirm the hypothesis.

The first measurement was done to determine if source of discharge transient current is trap charge, with samples taken from center and edge location, applied voltage electric field Ep = 1.9MV/cm, 2.9 MV/cm and 3.8MV/cm (sample dielectric width = 0.21um), polarization temperature Tp = 100^{o}C, polarization time tp =85 min and heating rate β = 5^{o}C/min. Square of peak temperature of samples under 3 different applied electric field has been collected and plotted in Figure 4.11. The plot indicates that for center and edge samples, there is no clear relationship between square of peak temperature and applied electric field. According to Nadkarni *et al*. [124], when trap charge is the source of current, peak temperature decreases linearly as square root of applied electric field increases. In another word, square of peak temperature decreases linearly as applied electric field increases. However, from Figure 4.11 such relationship cannot be found, and thus trap charge is not likely to be the source of discharge transient current.

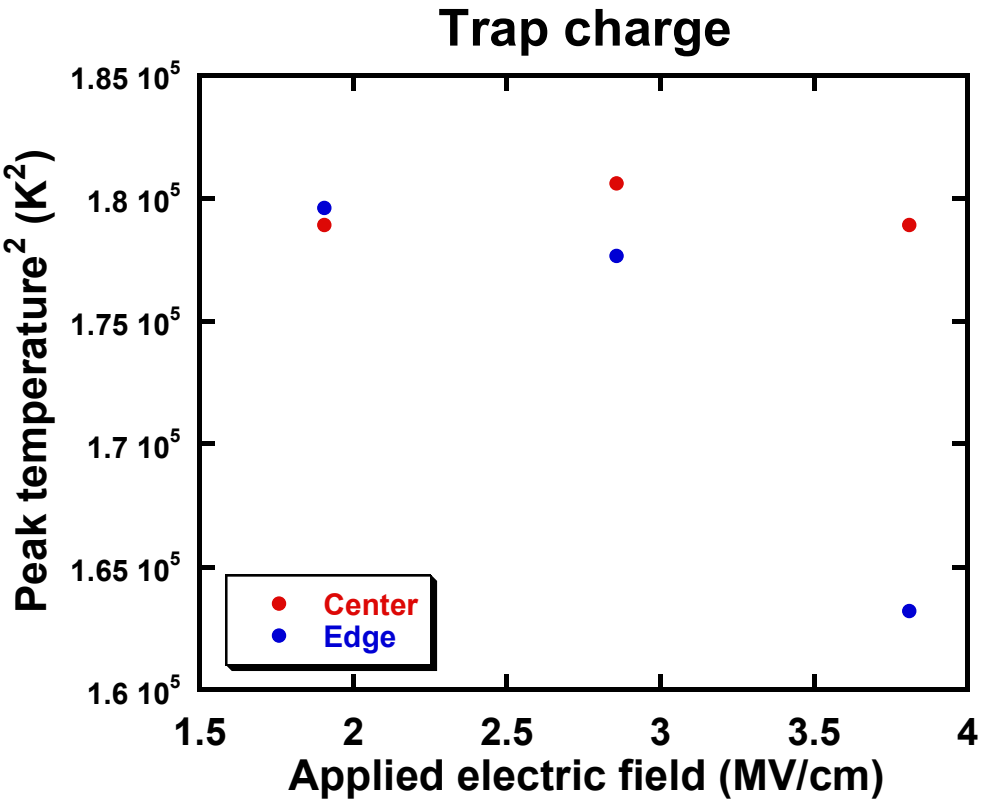

Figure 4.11 Temperature versus electric field plot for trap charges confirmation

The second measurement was done to determine if source of discharge transient current is mobile ion, with sample taken from center and edge locations, applied voltage Vp = 40V, 60V and 80V (sample dielectric width = 0.21um), polarization temperature Tp = 100°C, polarization time tp =85 min and heating rate β = 5°C/min. Peak current of samples under 3 different applied voltage has been collected and plotted in Figure 4.12. The plot indicates that for center and edge samples, as applied voltage increases, peak current increases linearly. According to Van Turnhout *et al.* [121], when mobile ion is the source of current, peak current decreases linearly as sample thickness increases under given electric field where electric field = applied voltage / sample thickness. Since the samples

have a fixed thickness, by increasing applied voltage, peak current should be increasing linearly. This corresponds well with what is indicated by Figure 4.12. Therefore, it is plausible that samples taken from center and edge have a common source of discharge transient current, which is mobile ion.

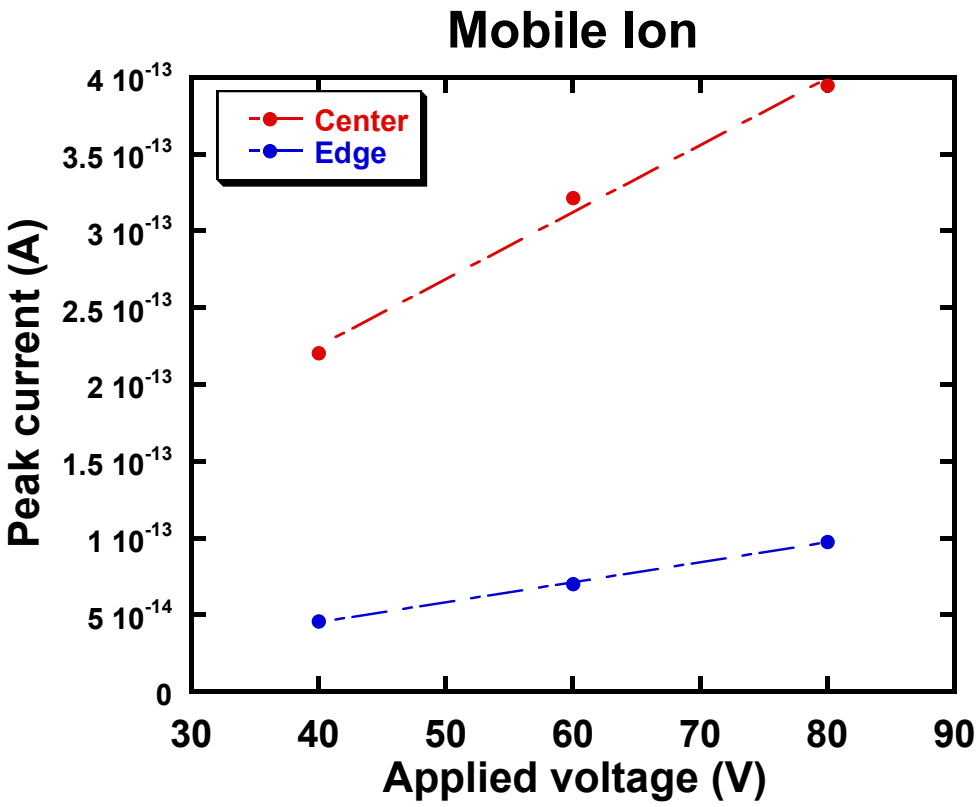

Figure 4.12 Peak current versus applied voltage plot for mobile ions confirmation

4.3.2 Discharge Transient Current and Factor Q of As-Received Samples

In this study, discharge transient current is used as an indicator of dielectric properties. Samples with better dielectric properties are expected to have higher discharge transient current while worse properties are expected to have lower discharge transient current. However, discharge transient current decays over time and it is difficult

to get a simple parameter that can indicate the level of current. Therefore, a data analysis technique is used to extract total charges that was returned to equilibrium state during discharging process. The amount of charges is factor Q, which can be used as a simple parameter that can determine the properties of dielectrics.

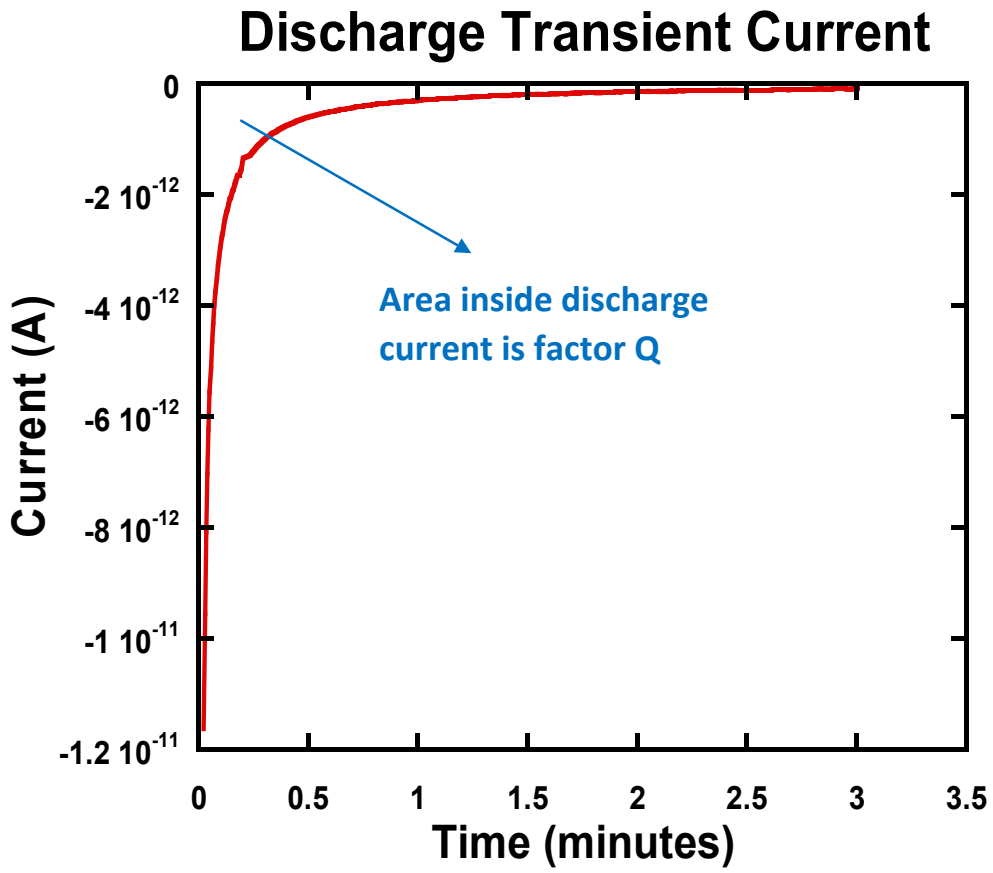

Figure 4.13 Typical discharge transient current and factor Q

Figure 4.13 is a typical discharge transient current data. As seen in the plot, discharge current varies with time and there is no simple data point that can represent current level. But for given amount of time, 3 minutes in this case, total charges that drifts inside dielectric is a fixed value, and can be extracted from

$$Q = \int (I_{\text{discharge}})dt \qquad (21)$$

Where Q is total amount and degree of charges that were drifted back to equilibrium state during discharging process, $I_{discharge}$ is the discharge current, t is time. Compare to samples with worse dielectric properties, samples with better dielectric properties are expected to show a higher Q.

Figure 4.14, 4.15 and 4.16 are typical discharge transient current data collected during study. Applied electric field is +/- 3.57MV/cm, charging time is 10 minutes, discharging time is 3 minutes and test temperature is 50°C.

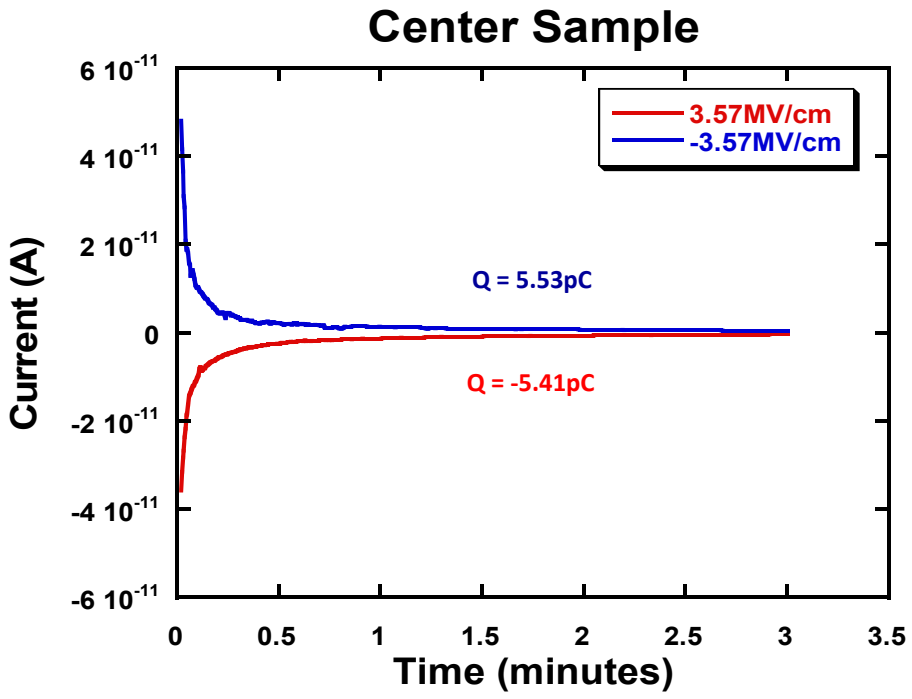

Figure 4.14 Typical discharge transient current and factor Q of center sample

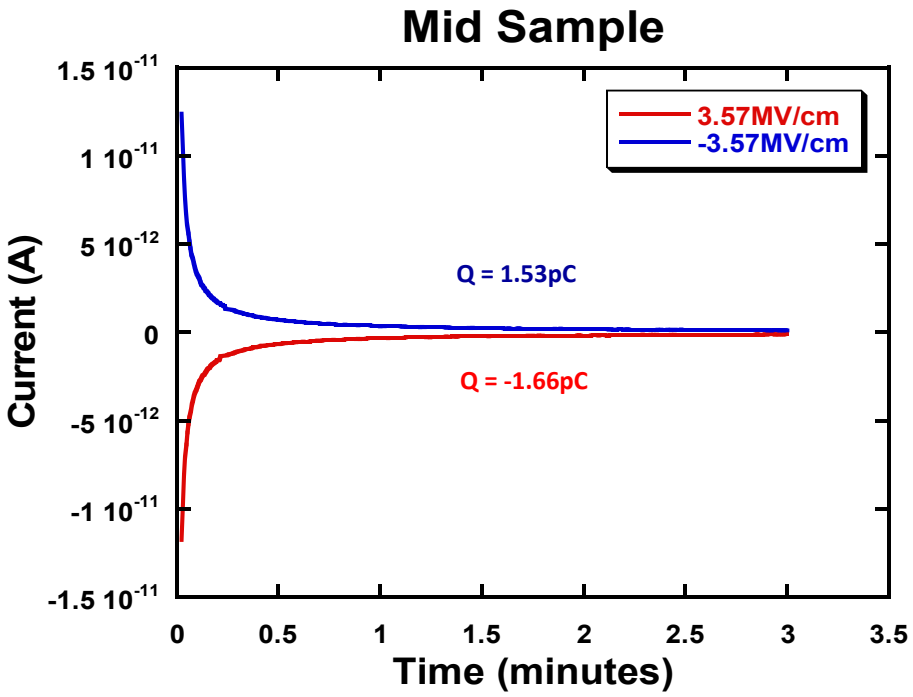

Figure 4.15 Typical discharge transient current and factor Q of mid sample

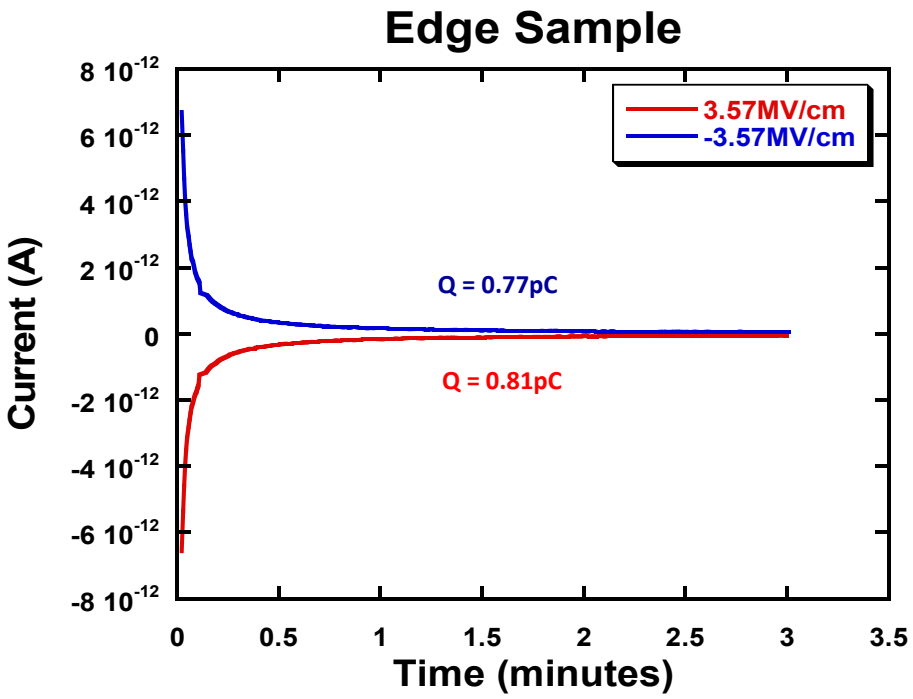

Figure 4.16 Typical discharge transient current and factor Q of edge sample

Figure 4.14, 4.15 and 4.16 indicate that discharge transient current and factor Q do not have electric field polarity dependence. This is because discharge transient current is sensitive to defects in dielectrics, but not to defects at metal/dielectric interface. Polarity dependence measurement introduced in previous chapter is an electrode limited technique where electrode/dielectric interface property is the key factor, and two electrodes with different properties (one with more defects and one with less defects) will create a difference in leakage current based on direction of electric field. Discharge transient current measurement, on the other hand, is a bulk-limited technique. Since bulk properties is always the same, direction of electric field is expected to have no effect on discharge transient current and factor Q.

Figure 4.14, 4.15 and 4.16 also indicate that there is a substantial difference in discharge transient current and factor Q of samples taken from different locations. Average Q of center, mid and edge sample is 5.47, 1.60 and 0.79 picocoulombs, respectively. Difference in center and edge sample is ~600% and this might be related to defects in dielectrics.

As discussed in previous paragraph, discharge transient current observed in the study is related to mobile ions. The source of mobile ions might be impurities that were trapped inside dielectric during deposition process [76,84-89]. Figure 4.17 is a schematic of charging and discharging process for samples with and without defects in dielectrics. During charging process, impurities will be ionized under high electric field and become mobile ions drifting inside dielectric. If there are positive ions in dielectrics as in Figure 4.17, they will drift to cathode electrode and accumulate at dielectric sidewall. If there is

no defect in dielectric, when electric field is removed during discharging process, mobile ions will return to equilibrium position and generate discharge transient current. If there exist defects in dielectric, ion drifting path will be hindered and discharge transient current will decrease. Therefore, dielectric with more defects is going to have smaller discharge transient current. Since edge samples are known to have worse properties, it is expected to show smaller discharge transient current and factor Q. Therefore, factor Q might serve as an indicator to determine dielectric properties.

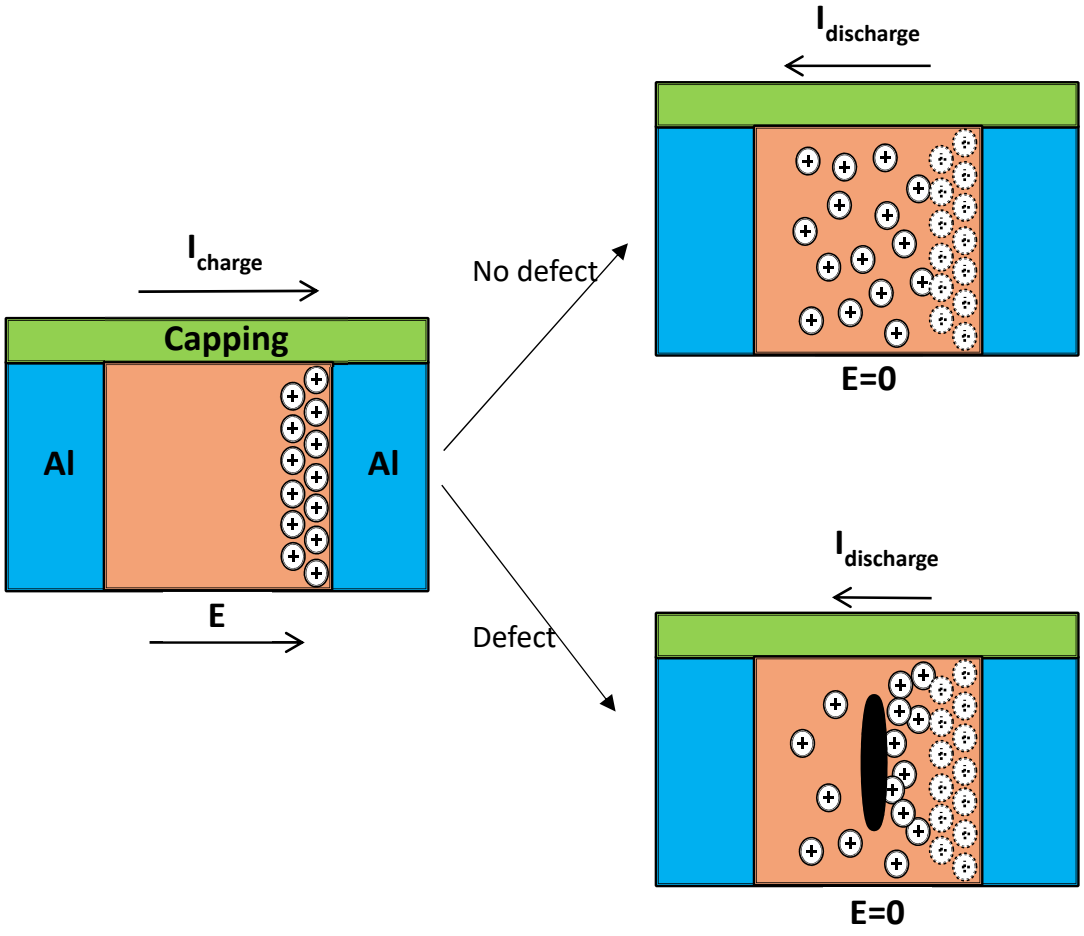

Figure 4.17 Schematic of charging/discharging process for sample with/without defects

As mentioned in previous paragraph, factor Q represents the total amount and degree of mobile ion charges that are returned to equilibrium state during discharging process. While defects exist in dielectric, mobile ions' migration path will be blocked and factor Q will be affected. Therefore, by following equations

$$Q = A[exp(\alpha V/kT) - 1] \qquad (22)$$

where Q is total charges, V is applied voltage, k is Boltzmann constant, A is geometrical constant that is mostly affected by interface area of metal/dielectric and α is parameter affected by valence of mobile ions [125], relationship between Q and applied voltage V can be determined. However, while defects exist in dielectric, mobile ions' drifting path will be blocked by defects and overall drifting length will be shorter. Therefore, voltage drop across dielectric can be calculated by equation

$$V = V[\sum(w_i/W) + \sum(w^v/W)] \qquad (23)$$

where W is total dielectric width, w_i is size of defect free dielectric and w_v is size of defect. By assuming size of defect is small and voltage drop across them is negligible, combining equation (4) & (5) gives equation

$$Q = A[exp\left(\frac{\alpha V}{kT}\frac{\overline{w}}{W}\right) - 1] \qquad (24)$$

where $\overline{w}$ is average size of the cluster encompassed by defects in dielectric. Therefore, Q is inversely exponentially proportional to amount of defects in dielectrics. Based on equation (6), data plotted in Figure 4.14 and 4.16 showed almost 6 times difference in Q

from center and edge samples is resulted by ~30% smaller cluster size at edge samples. Therefore, factor Q is extremely sensitive to defects in dielectrics.

To further understand the mechanism of factor Q, two wafers were selected (P02 and P25) and a set of measurements were done on samples taken from different wafer locations. Dielectric width of sample is 0.21um, applied voltage is +/- 75V (E = +/- 3.57MV/cm), test temperature is 50°C, charging time is 10 minutes and discharging time is 3 minutes. Factor Q is the average of absolute Q value under positive and negative bias. At each location 8 samples were selected and data was plotted into Figure 4.18. In the

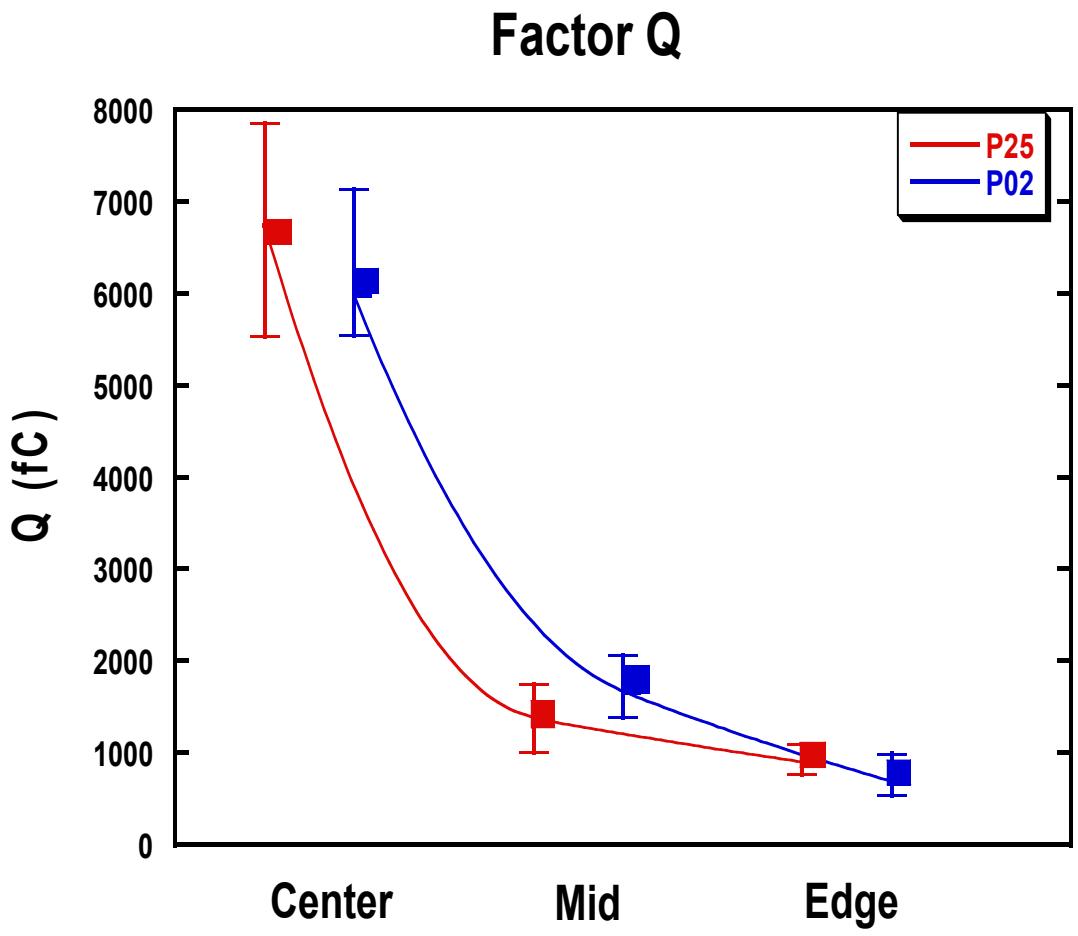

Figure 4.18 Factor Q data of samples from different locations

plot, little square represents the average value, high bar represents the maximum value collected from measurements and low bar represents the minimum value collected from measurements. Average value of P25 and P02 center is 6741fC and 5971fC, respectively. Average value of P25 and P02 mid is 1372fC and 1662fC, respectively. Average value of P25 and P02 edge is 900fC and 690fC, respectively. It clearly indicates that there is a huge difference between samples taken from different locations. Center samples have ~8 times larger Q compare to edge samples and ~4.2 times larger Q compare to mid samples. According to the mechanisms introduced in previous paragraph, this predicts that at as-received condition, edge samples and mid samples have developed a lot of defects, possibly voids, in the SiO_2 dielectrics.

To confirm this result, a series of SEM inspections have been done on samples taken from center and edge location at as-received condition. Figure 4.19 and 4.20 are some of the SEM images that were taken from center and edge location, respectively. Each figure contains three separate images, they are taken from different spots on the sample under different magnification. Capping layers of the samples have been removed and SEM images are taken from top-down view. In images, lines with darker contrast are SiO_2 dielectric and lines with brighter contrast are Al metals. Images in Figure 4.19 indicates that there are hardly any defects in dielectrics. However, from Figure 4.20 lots of voids (dark contrast in dielectric) can be observed in the dielectrics.

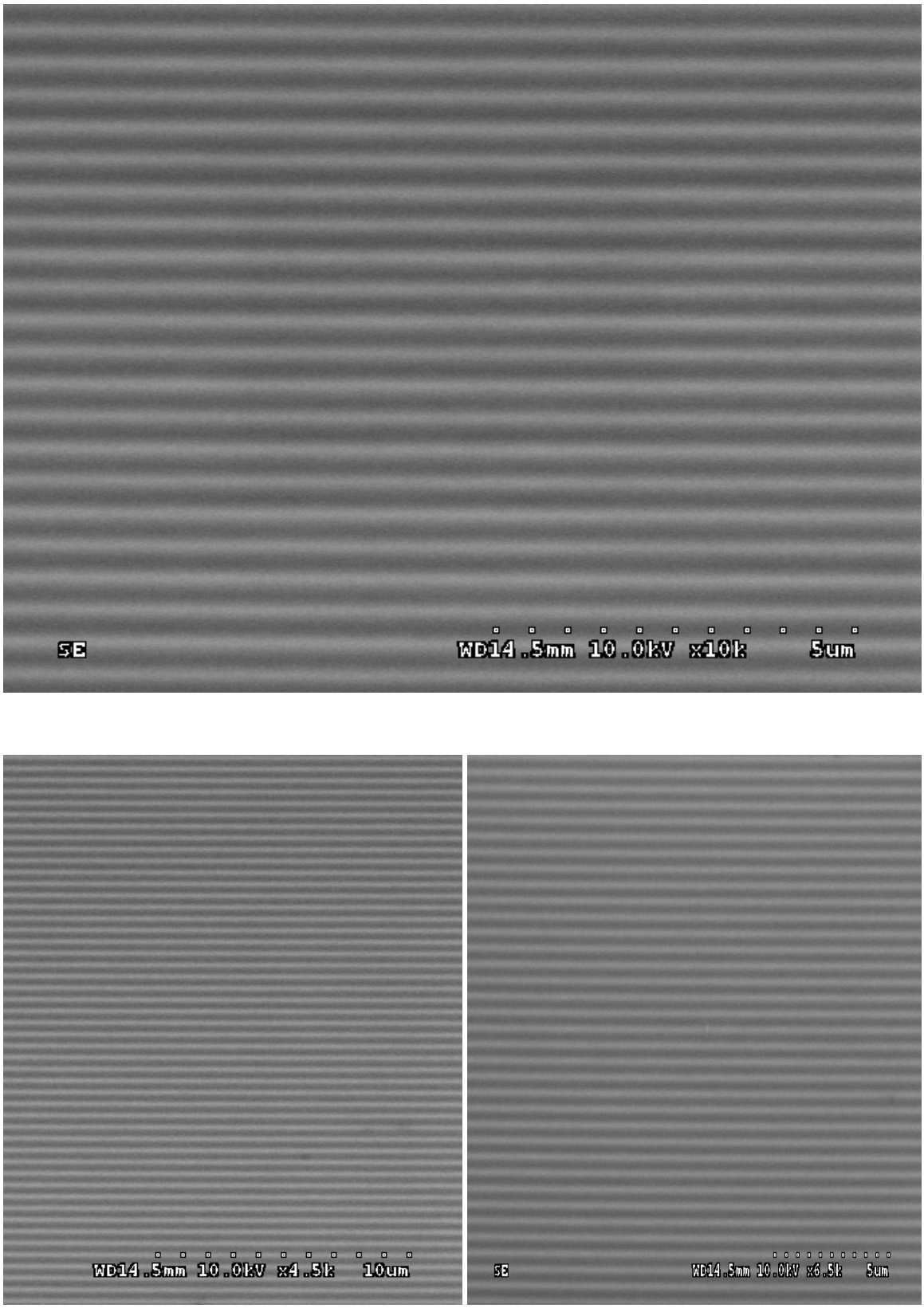

Figure 4.19 SEM images of sample taken from center location

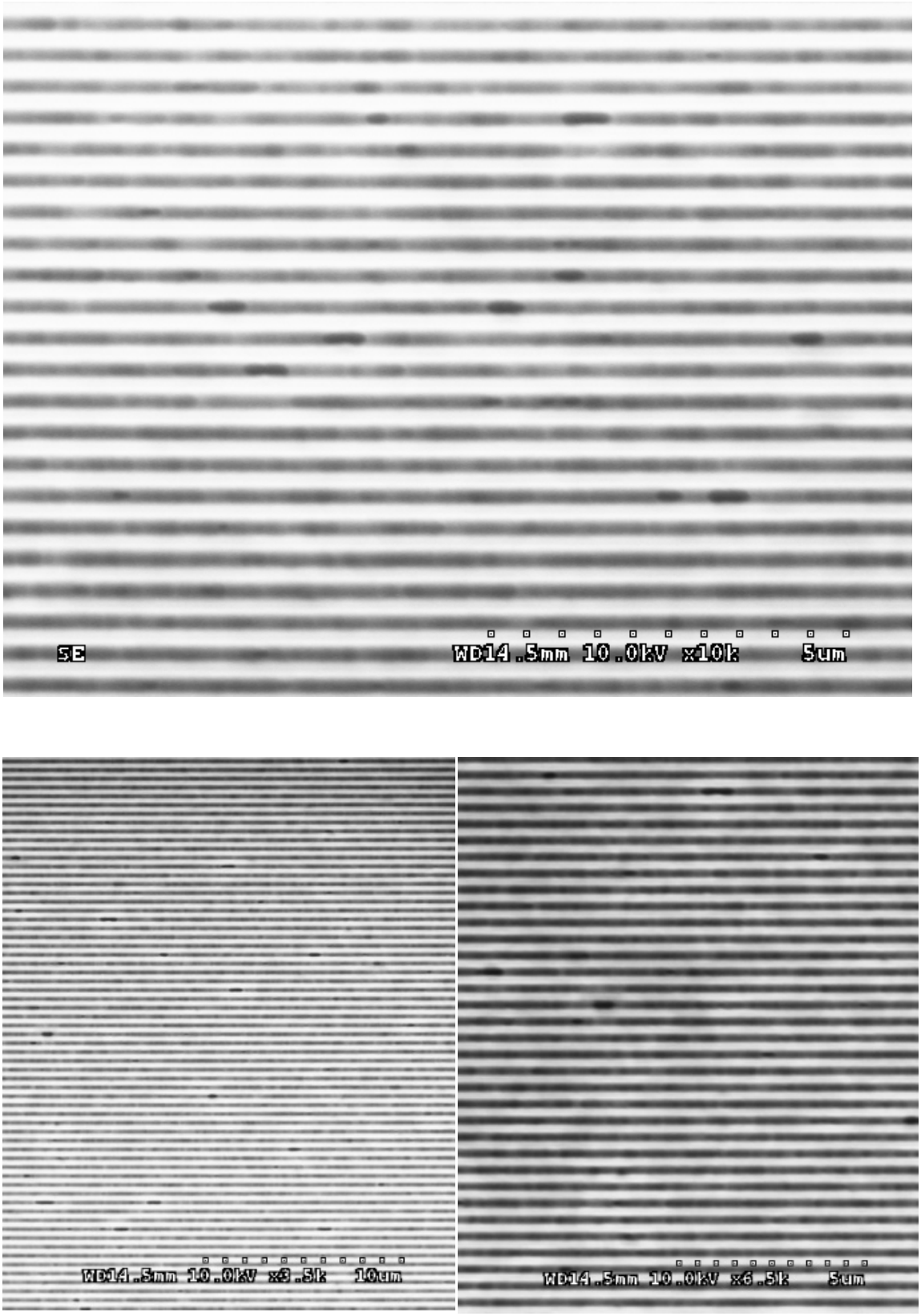

Figure 4.20 SEM images of sample taken from edge location

Result from SEM inspections corresponds well with prediction made from factor Q, which is edge samples have more defects existing in dielectric compare to center samples. Although difference in factor Q is huge, edge sample only contains a mediocre amount of voids in the dielectric. This indicates that factor Q is so sensitive to defects that even tiny amount of defects can create noticeable difference in factor Q.

Data collect from wafer P02 is further analyzed and plotted in Figure 4.21 as a cumulative probability distribution (CDF) function. Mean Q of center, mid and edge samples are 5964fC, 1648fC and 670fC, respectively. There exists a ~8.9 times difference

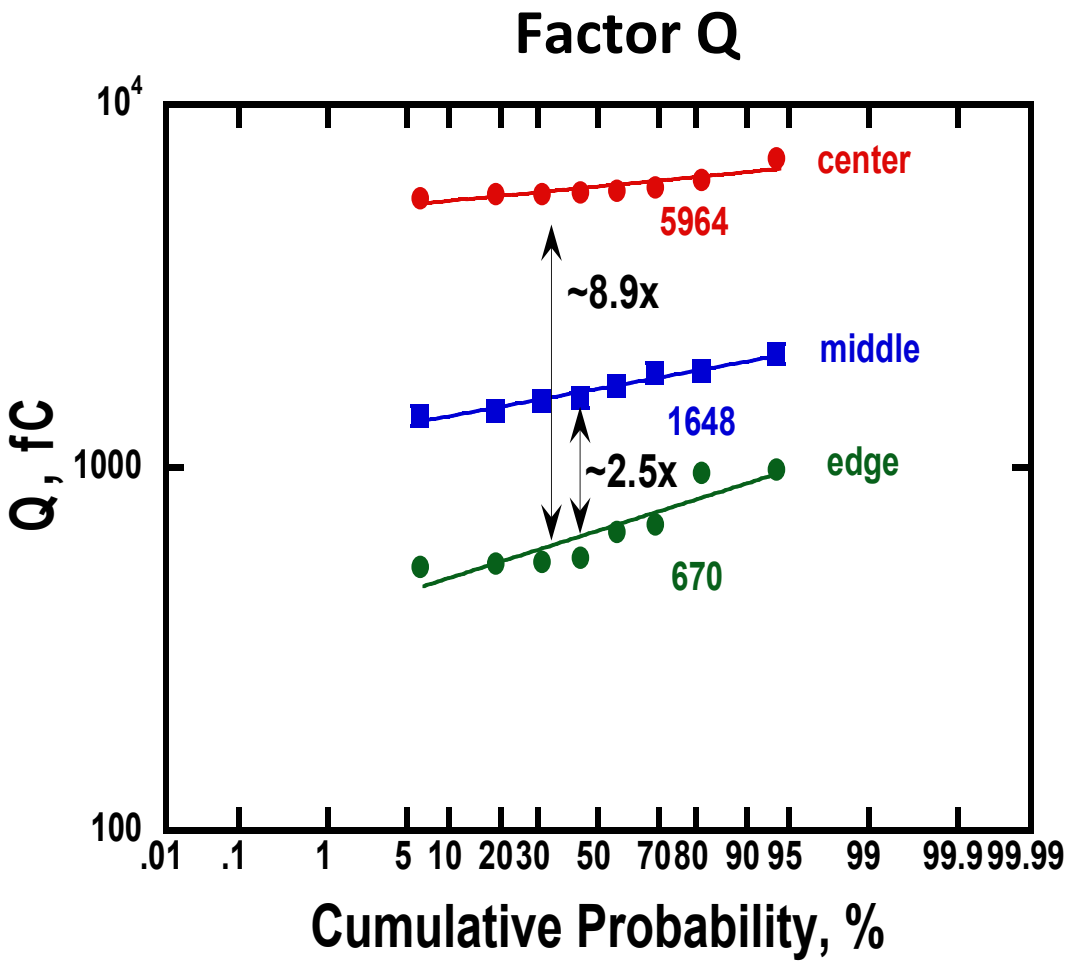

Figure 4.21 Factor Q versus cumulative probability of wafer P25 samples

in Q between center and edge samples and a ~2.5 times difference in Q between center and mid samples. According to equation (6), average cluster size of defect free dielectric from edge samples are ~40% smaller than center samples.

4.3.3 Discharge Transient Current and Factor Q of Aging Samples

To understand the effect of aging process on properties of dielectrics, a set of samples were tested at both as-received condition and aging condition. 8 samples (dielectric width = 0.21um) taken from each location (center, mid and edge) are tested. Applied voltage is 75V (E = 3.57MV/cm), charging time is 10 minutes, discharging time is 3 minutes, test temperature is 50^{o}C, aging temperature is 185^{o}C and aging time is up to 700 hours. Data collected during study is plotted in Figure 4.22. Plot indicates that factor Q does not vary much over aging time. At time zero (as-received condition), average factor Q of center, mid and edge samples are 7960fC, 2220fC and 920fC, respectively. After that, as samples went through aging process, factor Q remains at similar level. This result indicates that defects might exists in mid and edge samples at as-received condition and amount of defects does not vary much during aging process. It is as expected because defects in dielectrics are most likely created by inferior dielectric deposition process. Although aging process is known to create stress voiding defects, usually voiding activity are occurring in metal lines only because metal lines are softer than dielectrics and when coefficient of thermal expansion mismatch between metal lines and surrounding dielectrics occurs, voids will form inside metal lines to reduce the stress. This means the

number of defects in dielectric are most likely determined by deposition process and it is an independent factor from aging process.

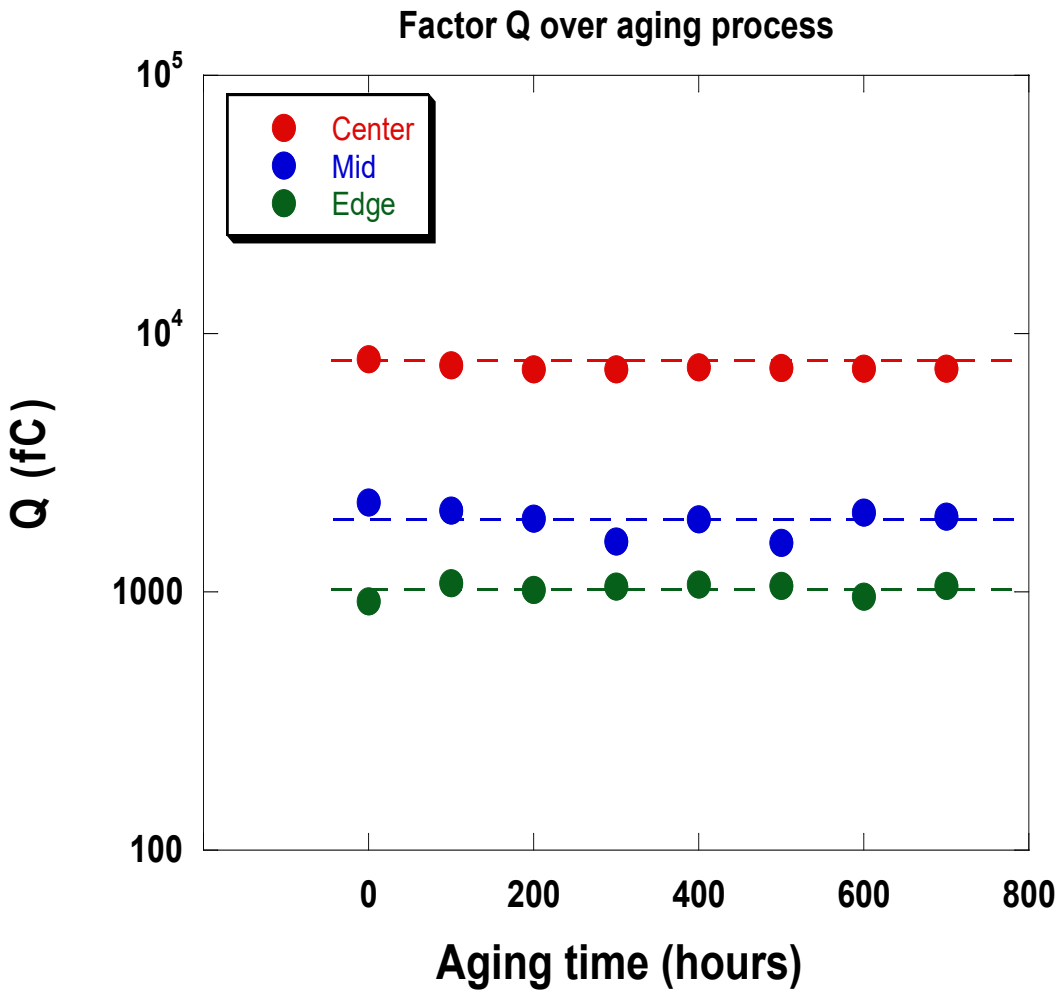

Figure 4.22 Factor Q versus aging time of center, mid and edge samples

4.3.4 Source of Mobile Ions

As discussed in previous paragraph, source of discharge transient current seen in the study is the displacement of mobile ions in the dielectric. However, the nature of mobile ion itself is unclear. To better understand the mechanism of discharge transient

current, a series of researches were done to identify the source of mobile ions. In another word, to determine what element or elements mobile ions are. An efficient way of doing this is to find the activation energy of mobile ions and cross reference to other researcher's publication and identify the source of mobile ions.

To find the activation energy*, Neel-Brown*-Arrhenius *equation can be used*

$$\tau_{av} = \tau_0 exp(\frac{Ea}{kT}) \qquad (25)$$

where τ_{av} is average relaxation time for mobile ions to return to equilibrium state during discharging process, τ_0 is relaxation time that is related to the characteristic of materials, Ea is activation energy of mobile ions, k is Boltzmann constant and T is temperature. According to equation (7), activation energy can be calculated through the slope of τ_{av} and 1/kT.

In order to obtain average relaxation time, first step is to collect factor Q value under different bias (electric field) and temperature. In this study, 5 different bias (40V, 50V, 60V, 70V and 80V) and 4 different temperature (50°C, 75°C, 100°C and 125°C) are used to generate a plot of factor Q versus applied voltage. Samples used in this study have a dielectric width of 0.21um and therefore applied electric field is 1.90MV/cm, 2.38MV/cm, 2.86MV/cm, 3.33MV/cm and 3.81MV/cm. Data collected from center and edge samples are plotted in Figure 4.23 and 4.24, respectively.

Figure 4.23 and 4.24 indicate that Q increases with both increasing bias and temperature. For center sample, factor Q shows a linear increase with increasing bias and temperature. The factor Q increase rate (the slope of Q versus applied bias) between

different temperature is similar. This indicates there might be a linear relationship between factor Q and applied bias / temperature. On the other hand, edge sample also shows a linear increase in factor Q when applied bias increases. However, factor Q increase rate is different for each temperature. As temperature increases, slope of factor Q versus applied bias increases. Another thing noticeable is that factor Q and temperature appears to have an exponential relationship instead of a linear relationship. These two differences seen in center and edge samples are likely due to edge samples having more defects in dielectrics.

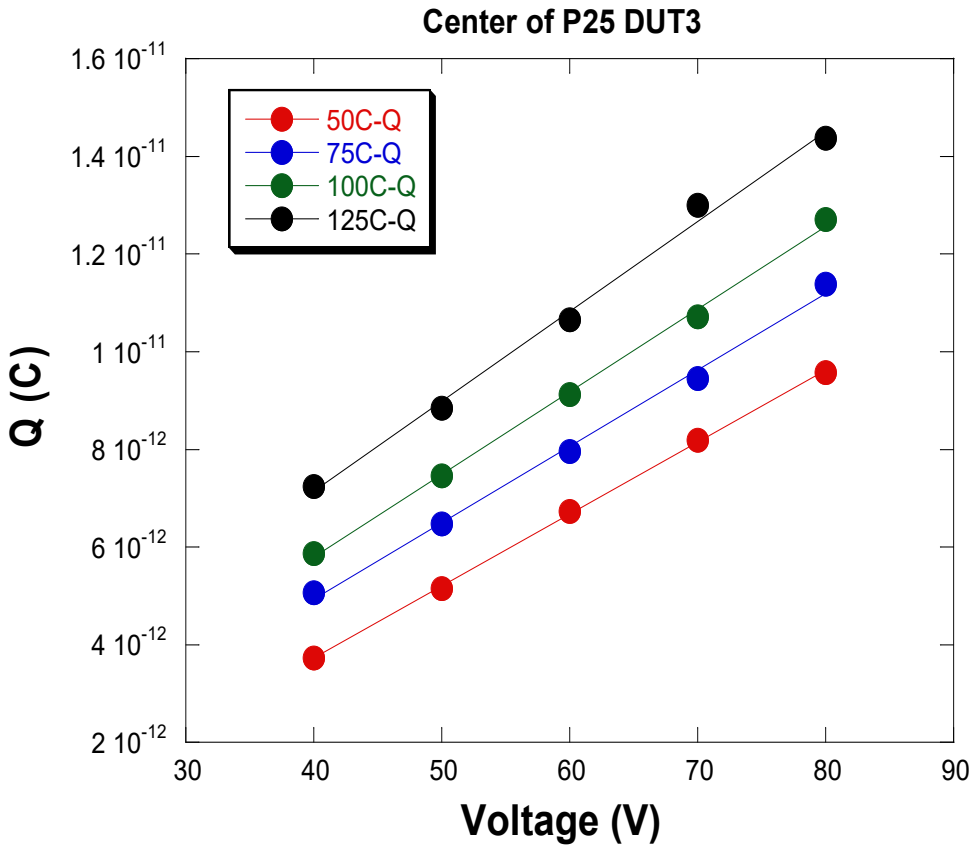

Figure 4.23 Factor Q versus applied bias from center sample

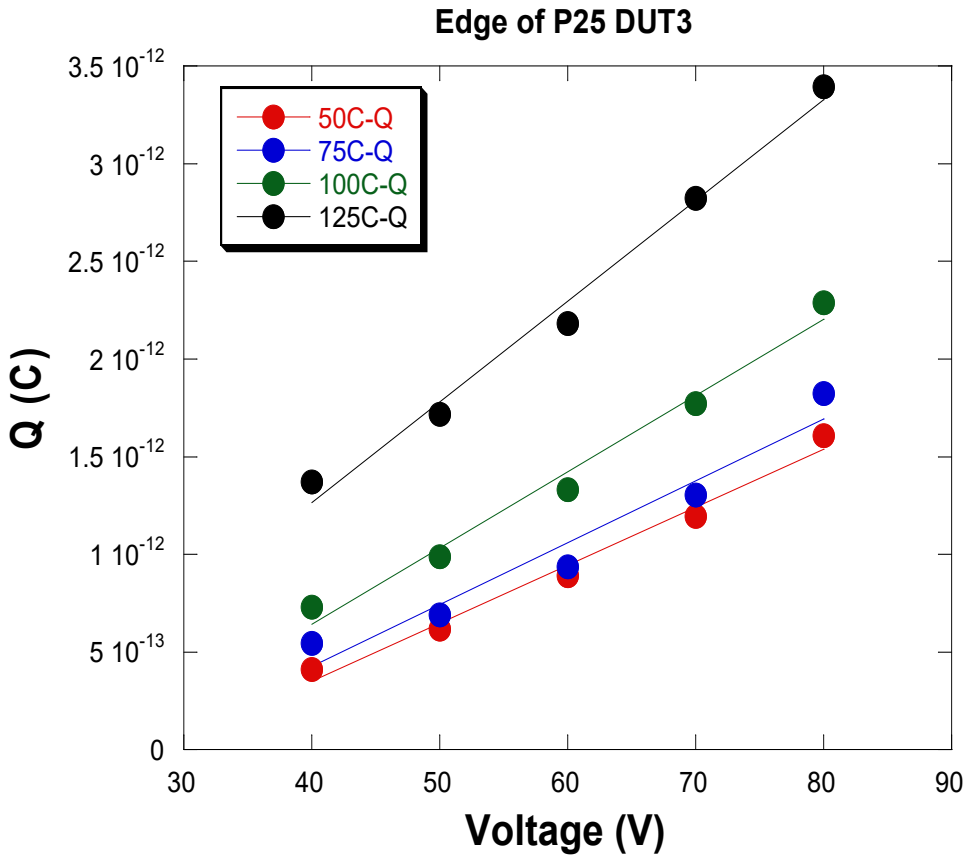

Figure 4.24 Factor Q versus applied bias from edge sample

Once factor Q versus applied bias data is collected, average relaxation time can be calculated through a series of calculations. Relation between factor Q and current is

$$Q = \int_0^\infty j(t)dt \qquad (26)$$

where Q is total amount of mobile ion charges drifting inside dielectric during discharging process, j(t) is current at given time. j(t) can then be defined as

$$j(t) \sim j(0)exp(-\frac{t}{\tau_{av}}) \qquad (27)$$

Where j(0) is current at time zero, t is given time and τ_{av} is average relaxation time. Combining equation (8) and (9), factor Q can then be defined as

$$Q = j(0)\tau_{av} \qquad (28)$$

Therefore, average relaxation time can be calculated by dividing factor Q with time zero current. After calculation, result of average relaxation time is plotted in Figure 4.25 and 4.26. Figure 4.25 indicates that for center sample, as temperature increases, average relaxation time decreases. This is as expected since relaxation time is proportional to how fast mobile ion can return to its equilibrium state during discharging process. As temperature increases, ion mobility increases, and thus is takes shorter time for ion to

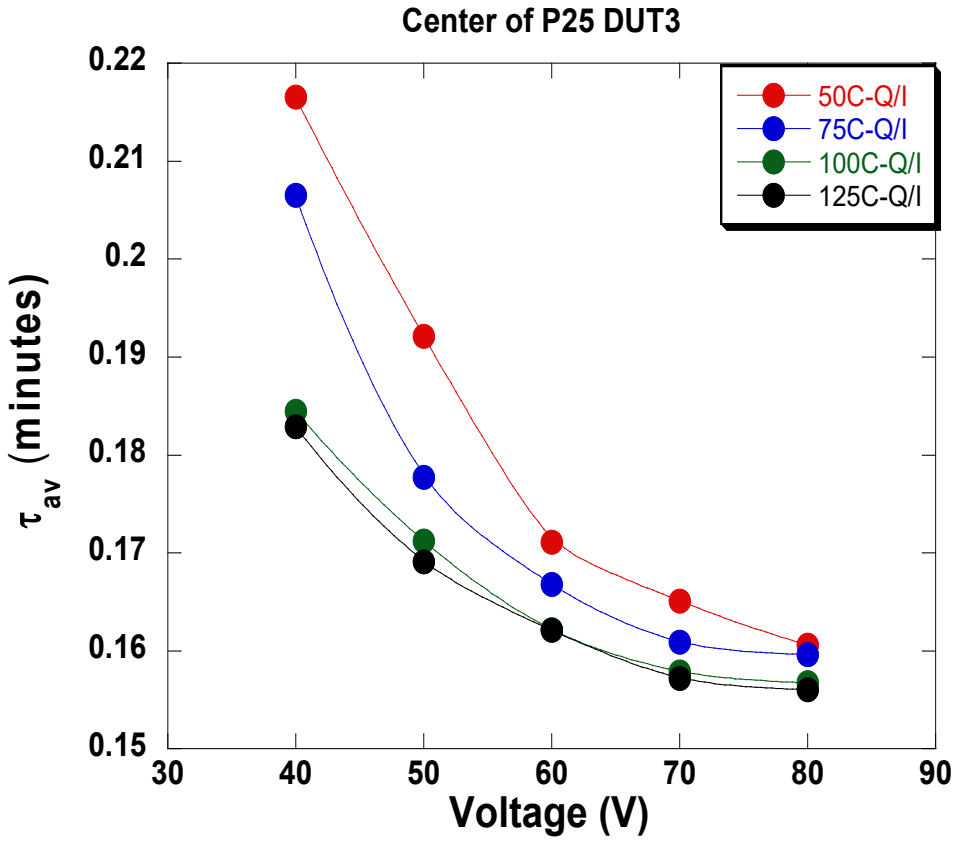

Figure 4.25 Average relaxation time versus applied bias from center sample

drift back to its equilibrium state. Figure 4.26 indicates that for edge sample, as temperature increases, average relaxation time increases and this is opposite from what center sample indicates.

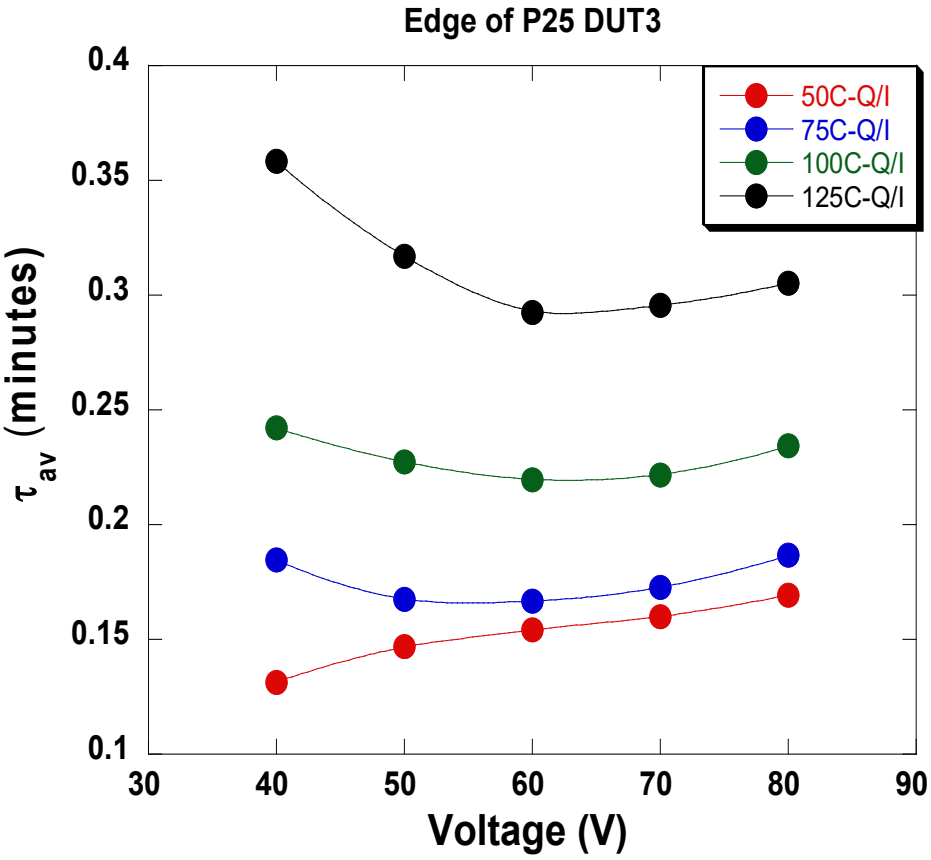

Figure 4.26 Average relaxation time versus applied bias from edge sample

As discussed in previous paragraph, activation energy can be calculated through the slope of τ_{av} and 1/kT. Therefore, the last step of calculation is to plot average relaxation time data against 1/kT and Figure 4.27 and 4.28 are the result of samples taken from center and edge locations. Boltzmann constant is removed from the plots for simplication. However, k is included in the calculation when computing for the slope.

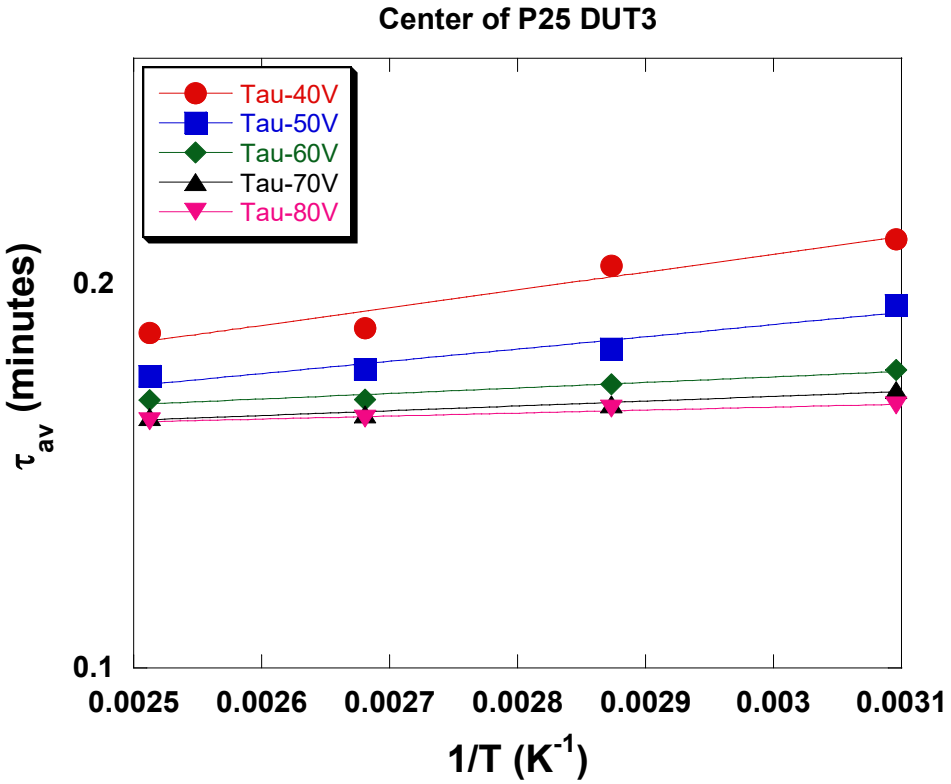

Figure 4.27 Average relaxation time versus applied bias from center sample

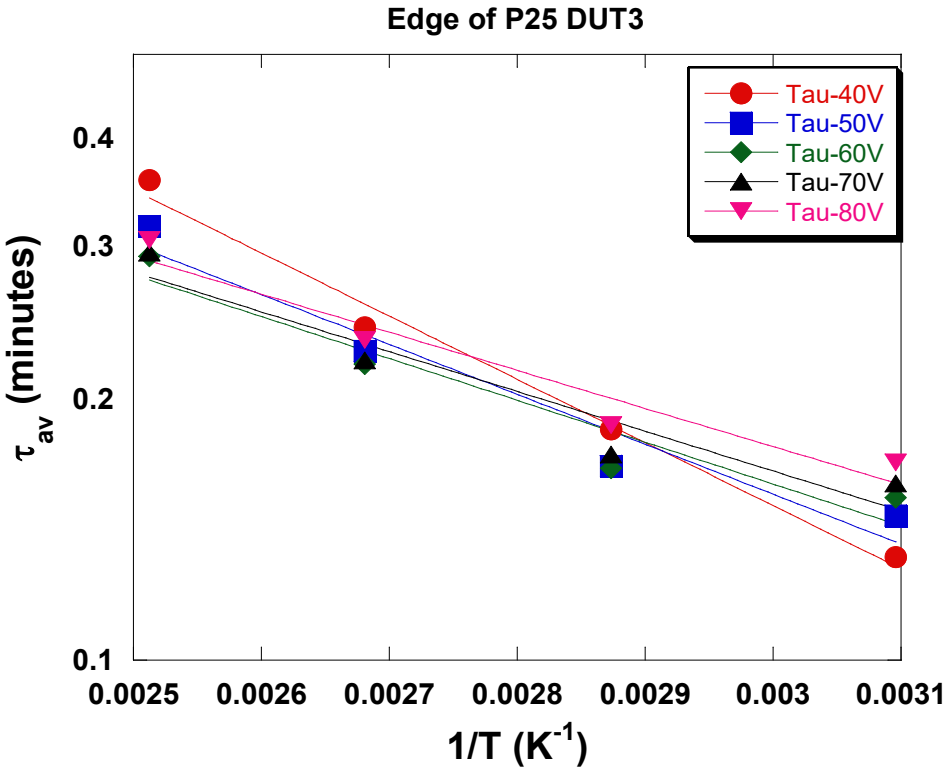

Figure 4.28 Average relaxation time versus applied bias from edge sample

Figure 4.27 indicates that for center sample, average relaxation time decreases as temperature increases and slopes vary with applied bias. Figure 4.28 indicates that as temperature increases, edge sample has longer average relaxation time. By calculating the slope of τ_{av} and $1/kT$, activation energy can be acquired and plotted in Figure 4.29. The trend of center sample is as expected because according to A. Pivrikas *et al*. [126], activation energy will decrease as applied electric field increases. Based on the plot, at E = 0MV/cm, activation energy can be extrapolated and Ea = 0.163eV. This is very similar to activation energy of H^0 in SiO_2 dielectric where Ea = 0.18eV [127] and hydrogen is a

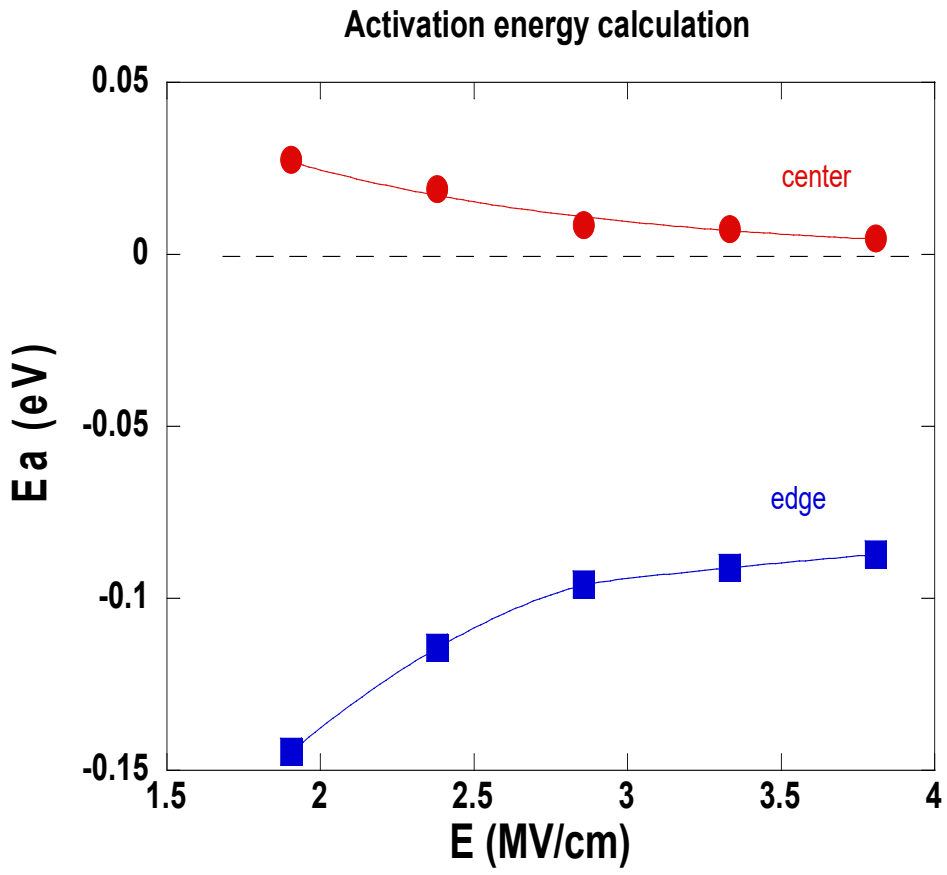

Figure 4.29 Activation energy versus applied electric field

common contamination seen in SiO_2 dielectrics deposited by PECVD process [76, 84-89]. Since all samples tested in the study are fabricated by PECVD process, it is likely that the source of mobile ion is hydrogen. On the other hand, edge sample shows a negative activation energy which is very uncommon. It indicates that as temperature and voltage increase, it is harder for mobile ions to return to their equilibrium state. This is likely due to defects in dielectrics. For center samples with no defect in dielectrics, mobile ions migrate to one side of dielectric sidewall under applied electric field and Q is stored during charging process. At discharging process, external electric field is removed but an internal field with direction opposite to external field exists inside dielectric due to the uneven distribution of mobile ions. This internal field will assist back migration of mobile ions until they reach equilibrium state inside dielectric. Therefore, as temperature increases, mobile ions mobility will be increased and can return to equilibrium state faster. As for edge samples with defects in dielectrics, during charging process, mobile ions are forced to migrate through microscopic defects and accumulate at one side of dielectric sidewall under high electric field and temperature. As electric field and temperature increases, more mobile ions are accumulated at side wall. During discharging process when external electric field is removed, internal field is much weaker compares to external field and the back-migration process will be impeded by defects. Therefore, the more mobile ions are displaced during charging process, the longer relaxation time is going to take for mobile ions to return to equilibrium state. In another word, for edge sample with defects in dielectrics, as temperature and applied electric field increases, amount and degree of

mobile ions displacement increases and it is harder for all mobile ions to back-migrate during discharging process because of the defects.

4.3.5 Capacitance Measurement of As-received Samples

In order to gain better understanding of how defects existing in dielectrics affect mobile ion migration, another series of measurements were conducted in the study. Capacitance measurement under AC bias with different frequency is an ideal way of revealing the nature of mobile ion migration inside dielectrics and the possible effects of defects.

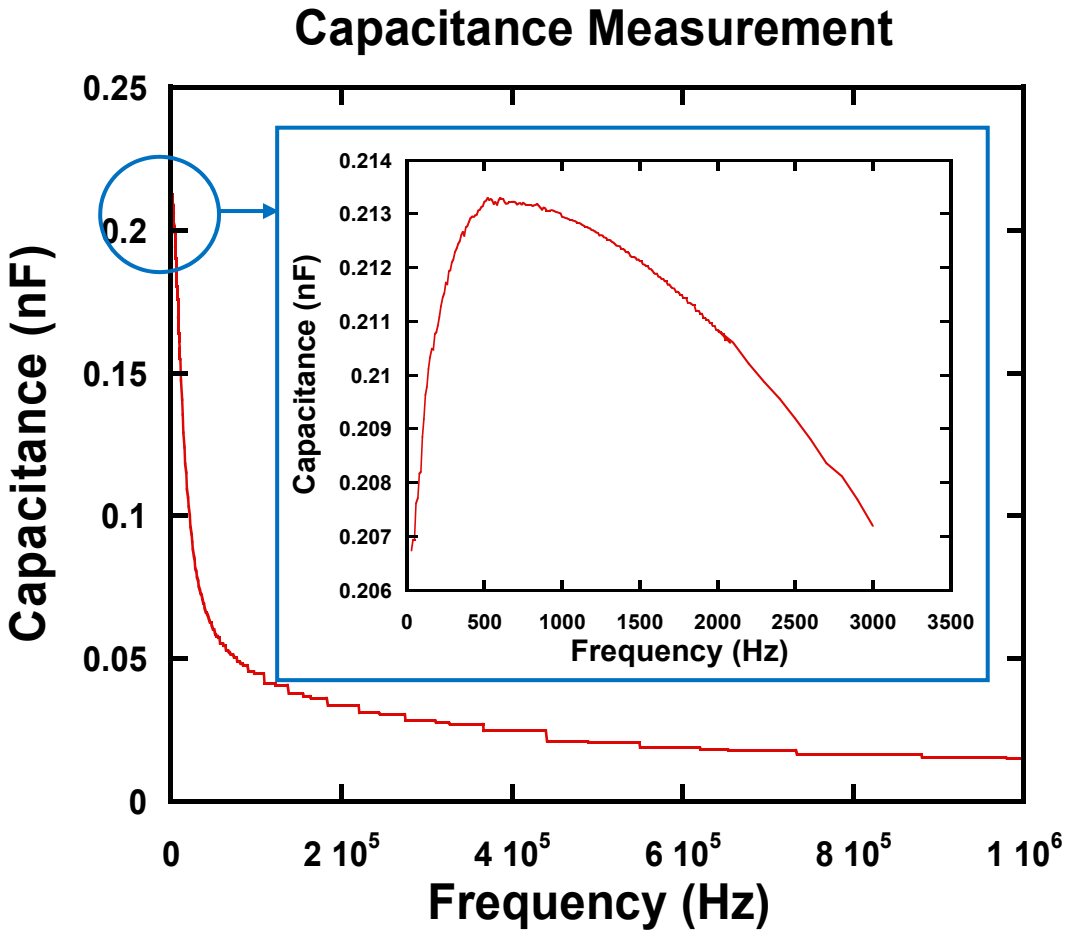

Figure 4.30 Typical capacitance versus AC frequency data seen in the study

Key parameter of capacitance measurement is peak frequency as it can provide important information such as the origin of polarization dipole and the relaxation time of dipole. As discussed in previous paragraph, peak frequency refers to a specific AC frequency that can produce a peak in capacitance due to the resonance of polarization dipole and AC frequency. Higher peak frequency is associate with faster movement of polarization dipole. A set of data obtained from capacitance measurement is plotted in Figure 4.30 as an example. In this measurement, applied AC bias is 17V (range from -17V to +17V), and test temperature is 50^{o}C. The plot indicates that from 0.1MHz to 1MHZ, there is no clear capacitance peak, but when zoomed into low frequency range, there is a clear capacitance peak observed at ~500Hz and this Is the peak frequency. Typical peak frequencies for space charge dipole, orientational dipole, ionic dipole and electronic dipole are ~1-10^{3}Hz, 10^{6}Hz, 10^{12}Hz and 10^{16}Hz, respectively [128]. Therefore, this result indicates that from 0 to 1MHz frequency, space charge dipole is the only type of polarization dipole contributing to the capacitance. Since space charge dipole is created by the migration of mobile ions, peak frequency data can serve as a good indication of mobile ions activity.

Based on current understanding, defect is expected to have effect on peak frequency. Figure 4.31 is a schematic of a mobile ion drifting under AC bias. When applied bias (electric field) is alternating direction, ion will oscillate inside dielectric with certain distance at certain velocity

$$D_{drift} \propto 1/ f_{peak} \qquad (29)$$

$$V_{drift} \propto f_{peak} \qquad (30)$$

where D_{drift} is distance of mobile ion drifting inside dielectric, V_{drift} is drifting speed of mobile ion and f_{peak} is peak frequency. Since ion drift distance and drift speed is proportional to AC bias level, for dielectric with no defect, higher AC bias level will lead to a higher D_{drift} and V_{drift}. When defects exist in dielectric, such as Figure 4.32, as AC bias increases, V_{drift} will increase continuously while D_{drift} can only increase to a certain extent before voids impede further displacement. According to equation (11) and (12), this indicates that as AC bias level increases, peak frequency is expected to increase as well.

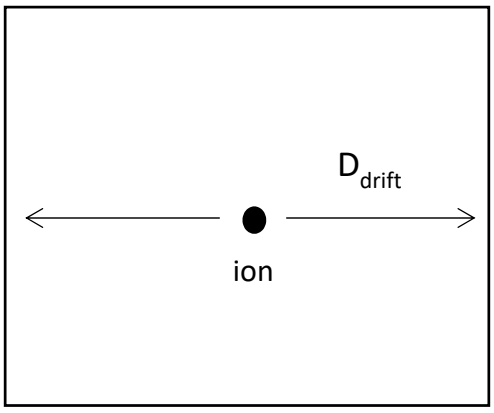

Figure 4.31 Schematic of ion under AC bias

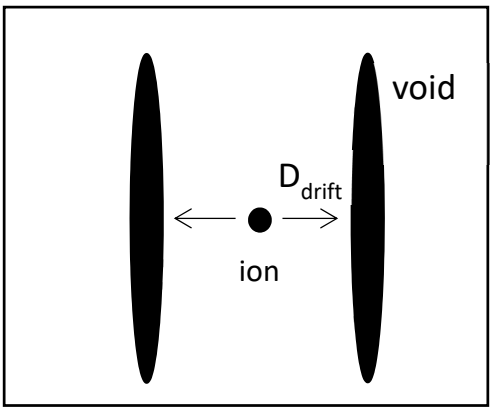

Figure 4.32 Schematic of ion with defects under AC bias

To confirm this assumption, a series of measurements were done. In the measurements, samples taken from center and edge location are selected and applied AC bias is 9V, 13V and 17V while test temperature is 30°C, 50°C, 75°C, 100°C and 125°C. Figure 4.33 and 4.34 are two sets of peak frequency data collected during the study.

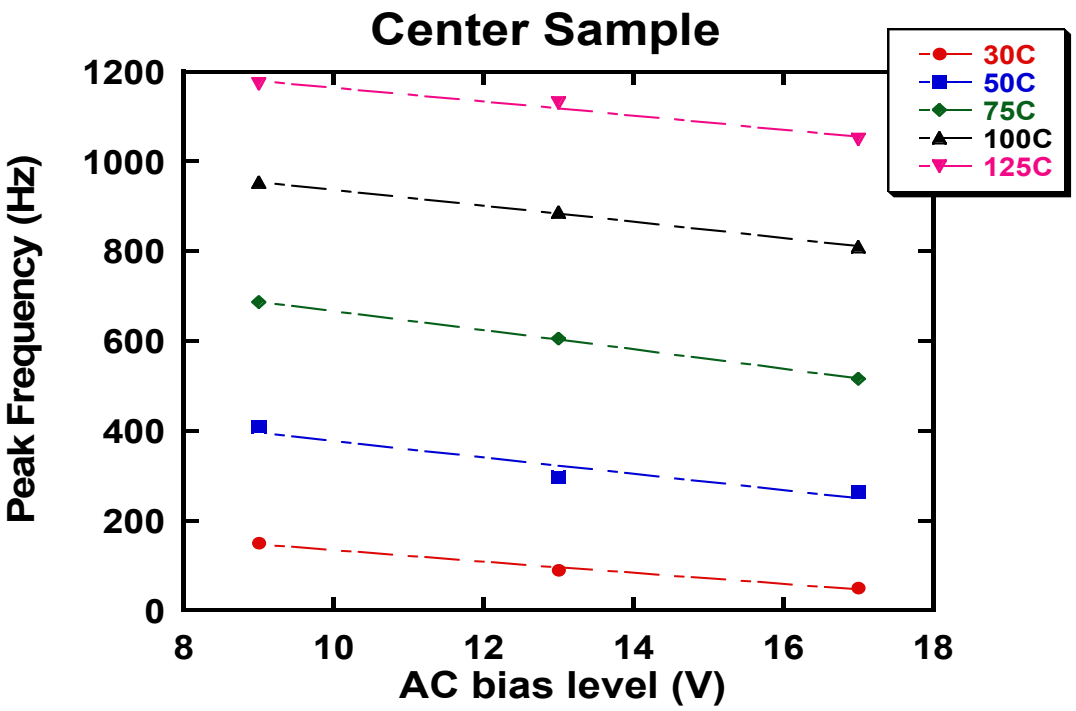

Figure 4.33 Peak frequency versus AC bias level for center sample

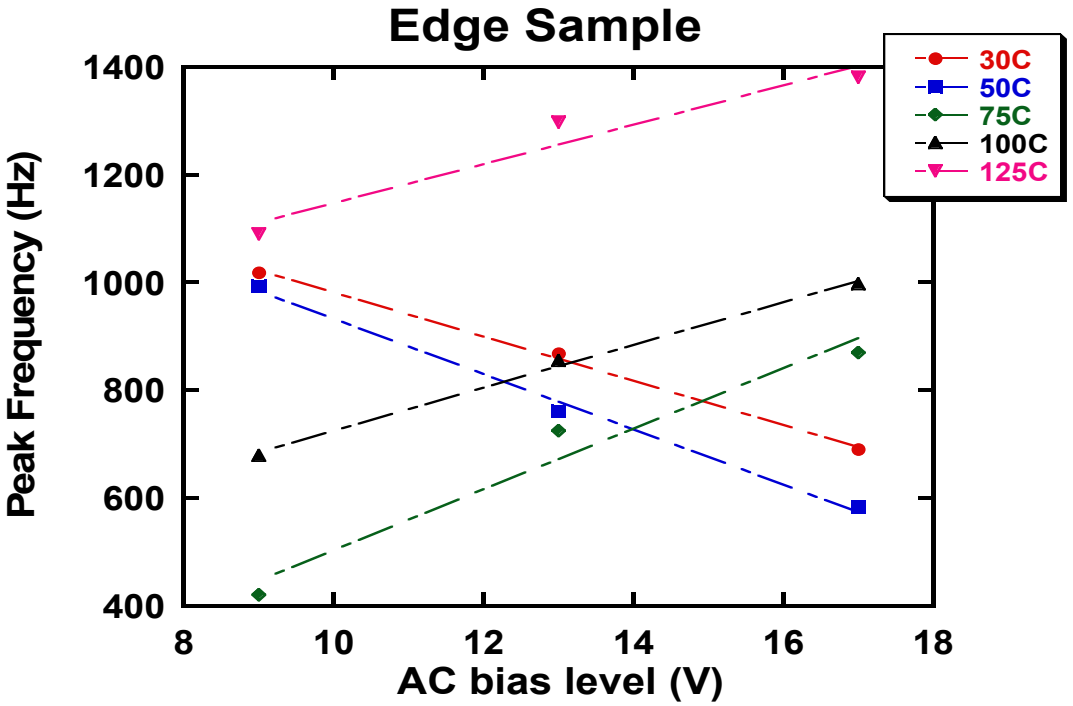

Figure 4.34 Peak frequency versus AC bias level for edge sample

Figure 4.33 indicates that for center sample, as temperature increases, peak frequency increases. Since ion mobility is directly proportional to temperature, V_{drift} is expected to increase with higher temperature, which leads to high peak frequency. Figure 4.34, on the other hand, indicates something unexpected. For edge sample, from 75^{o}C to 125^{o}C, as temperature and voltage increases, peak frequency increases. For temperature, it should have similar effect on both center and edge samples. As for voltage effect on peak frequency, when AC bias increases, peak frequency will increase as discussed in previous paragraph. However, from 30^{o}C to 50^{o}C, the plot shows an opposite trend compares to 75^{o}C to 125^{o}C. As temperature and voltage increase, peak frequency decreases. Plausible explanation is that at low temperature, energy traps (created by defects) are not fully activated [129]. When applied bias increases, more energy traps are activated through electrical energy. These energy traps will hinder the movement of mobile ions, and thus reduce V_{drift} which leads to lower peak frequency. This correspond well with the fact that when applied AC bias is 9V, peak frequency of 30^{o}C (1018Hz) and 50^{o}C (993Hz) is higher than 75^{o}C(420Hz) and 100^{o}C(679Hz), which is likely due to energy traps not fully activate at low temperature and thus ion mobility is high.

4.3.6 Time Dependent Dielectric Breakdown Test of As-received Samples

In previous paragraphs, mechanism and application for discharge transient current measurement has been studied. However, it is crucial to correlate factor Q with the result from conventional reliability test. One of the most common reliability tests for dielectric properties is time dependent dielectric breakdown test (TDDB). In the study, several series of tests have been done on samples taken from different wafers which are

expected to show different factor Q and TDDB failure time. Figure 4.35 is a typical TDDB data seen in research. Dielectric width of the sample is 0.21um, applied bias is 65V, applied electric field is 3.10MV/cm and test temperature is 125°C. As seen in zoomed plot, from time zero to ~300 minutes, dielectric exhibits a normal charging behavior (leakage current is ~10^{-12}A to 10^{-11}A) as discussed in previous paragraph. After 300 minutes, a noticeable uprising trend of leakage current can be observed (leakage current

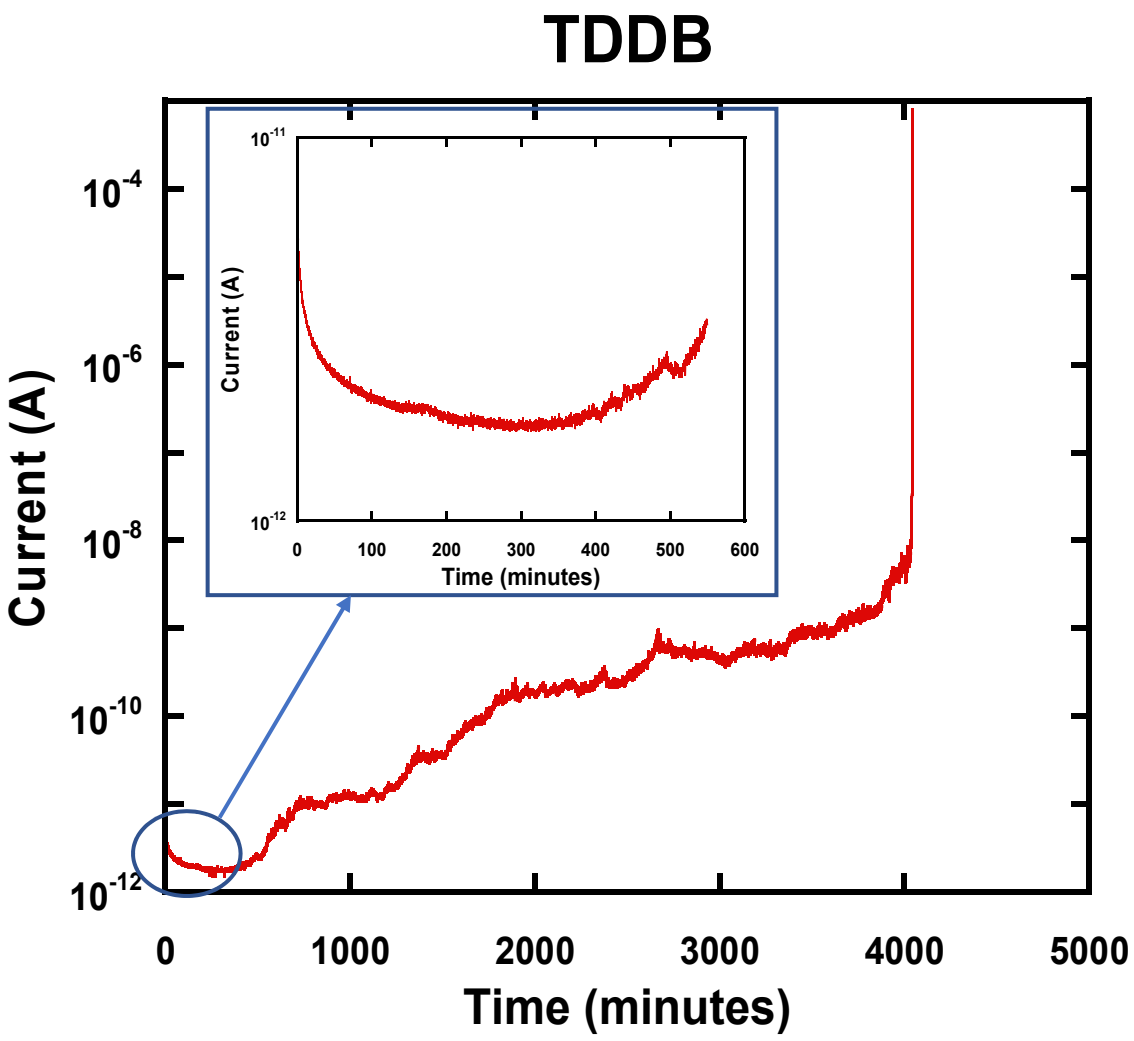

Figure 4.35 Typical TDDB data seen in the research

is ~10^{-11}A to 10^{-8}A). This is the period where short circuit path are forming inside dielectric under electric stress. As discussed in previous paragraph, there are many different mechanisms that can contribute to the formation of electrical short circuit, such as breakage of Si-Si bond in SiO_2 that creates oxygen vacancy or energetic electrons that create defect in dielectrics. As electrical short circuit continuously formatting inside dielectrics, effective dielectric thickness is reduced and effective electric field increases. This will further increase the short circuit formation speed and therefore the increase rate of leakage current become faster over time. At certain point, when effective dielectric thickness is reduced to critical value, a total electrical breakdown as seen in the plot, where current shoot up to 10^{-3}A (the current limit of HP 4140 pA meter), will occur. Amount of time required for final electrical breakdown of dielectric to occur is the time to failure (TTF), also known as TDDB lifetime. Higher TDDB lifetime usually means the properties of tested dielectric are better and lower TDDB lifetime means the opposite.

As discussed in previous paragraph, compare to center samples, edge samples tend to have worse dielectric properties due to defects existing in dielectrics. Therefore, TDDB test is expected to show different result for samples from different wafer locations. A set of TDDB date collected during the study is plotted in Figure 4.36. One sample is picked from each location (center and edge). Dielectric width of the samples is 0.21um, applied bias is 65V, applied electric field is 3.10MV/cm and test temperature is 125^{o}C. Factor Q is also measured during the test, applied electric field is 3.10MV/cm, charging time is 10 minutes, discharging time 3 minutes and test temperature is 125^{o}C.

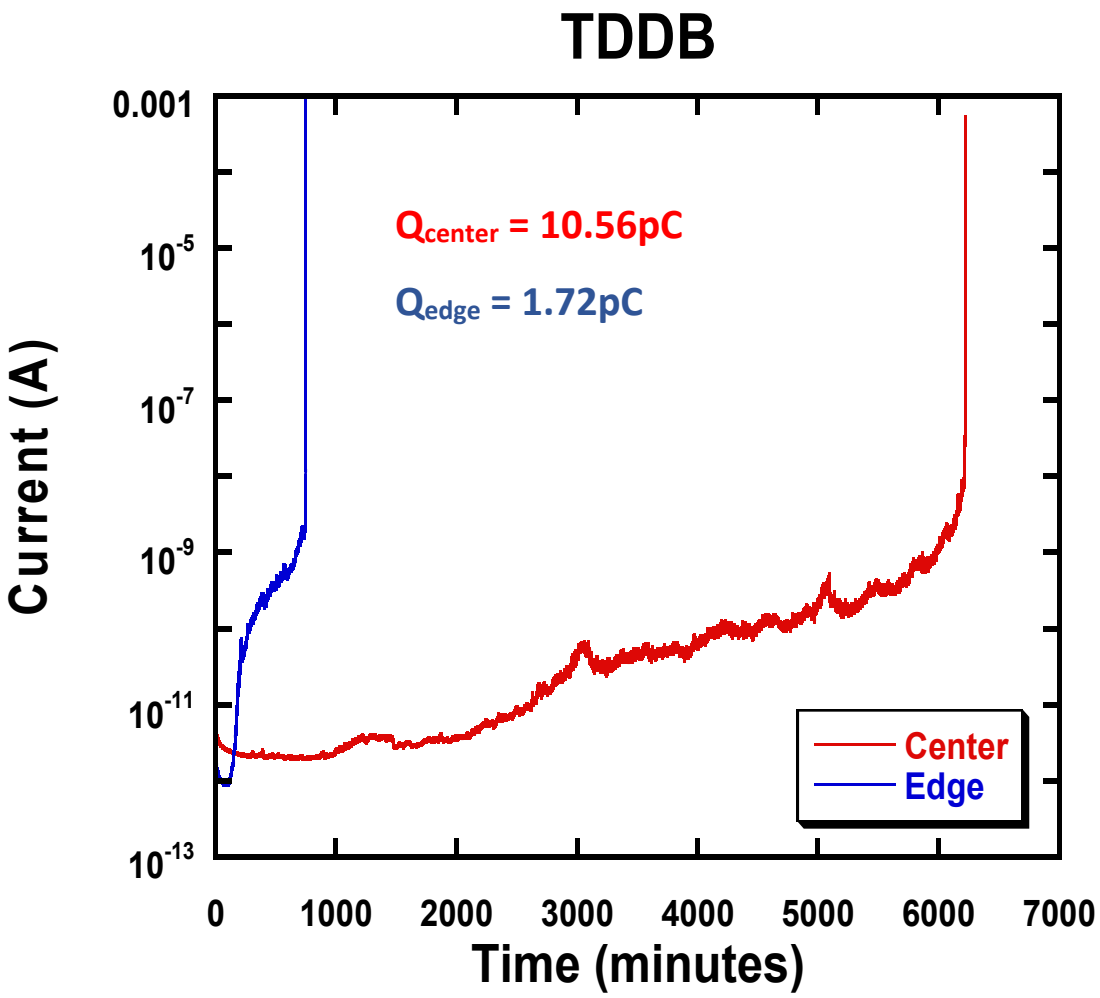

Figure 4.36 TDDB data of center and edge samples

As seen in the plot, center sample and edge sample showed a distinguished difference in TDDB lifetime. Center sample has a TDDB lifetime of 6222 minutes while edge sample has a TDDB lifetime of 748 minutes. Factor Q of center sample and edge sample is 10.56pC and 1.72pC, respectively. Center sample has a TDDB lifetime that is ~8.3 times of edge sample, while factor Q is ~6.1 times larger than edge sample. This indicates that factor Q and TDDB lifetime may have a non-linear relationship. Plausible explanation for the huge difference seen in the TDDB lifetime is the difference of dielectric

strength of SiO_2 and defects. Dielectric strength refers to the maximum electric field that insulating material can withstand without electrical breakdown. Dielectric strength of SiO_2 is typically >5MV/cm [58] and this is the reason TDDB failure does not occur immediately because applied electric field (3.1MV/cm) is well below SiO_2's critical electric field. On the other hand, defects such as voids can be considered as tiny vacuum pockets located inside dielectric. Since dielectric strength of vacuum is only 0.2 - 0.4MV/cm [93], when applied electric field is higher than 0.4MV/cm, electrical breakdown in defect sites will occur and defect sites will lose their insulating properties. This process reduces the effective dielectric thickness, and thus effective electric field is increased. For samples that contain more defects in dielectrics, overall effective electric field is higher. As discussed in previous paragraph, although there are many different theories proposed to explain TDDB behavior, all of them agreed that higher electric field will lead to a shorter TDDB lifetime, therefore samples with more defects in dielectrics are expected to have a shorter TDDB lifetime.

Another thing noticeable in Figure 4.36 is the difference of leakage current level before short circuit formation. Center sample has higher leakage current compare to edge sample, this is likely due to center sample has better metal line properties and as discussed in previous chapter, less defects at metal/dielectric interface will lead to a higher leakage current injection area, and thus higher leakage current.

Although Figure 4.36 indicates that there is a clear relationship between factor Q and TDDB lifetime, one set of data is not enough to make valid conclusion. Therefore, a total of 50 samples from different wafers (P12, 17, 20 and 25) and locations (center and

edge) are tested and data is plotted into Figure 4.37. Dielectric width of the samples is 0.21um, applied bias is 65V, applied electric field is 3.10MV/cm and test temperature is 125°C. Factor Q is also measured during the test, applied electric field is 3.10MV/cm, charging time is 10 minutes, discharging time 3 minutes and test temperature is 125°C.

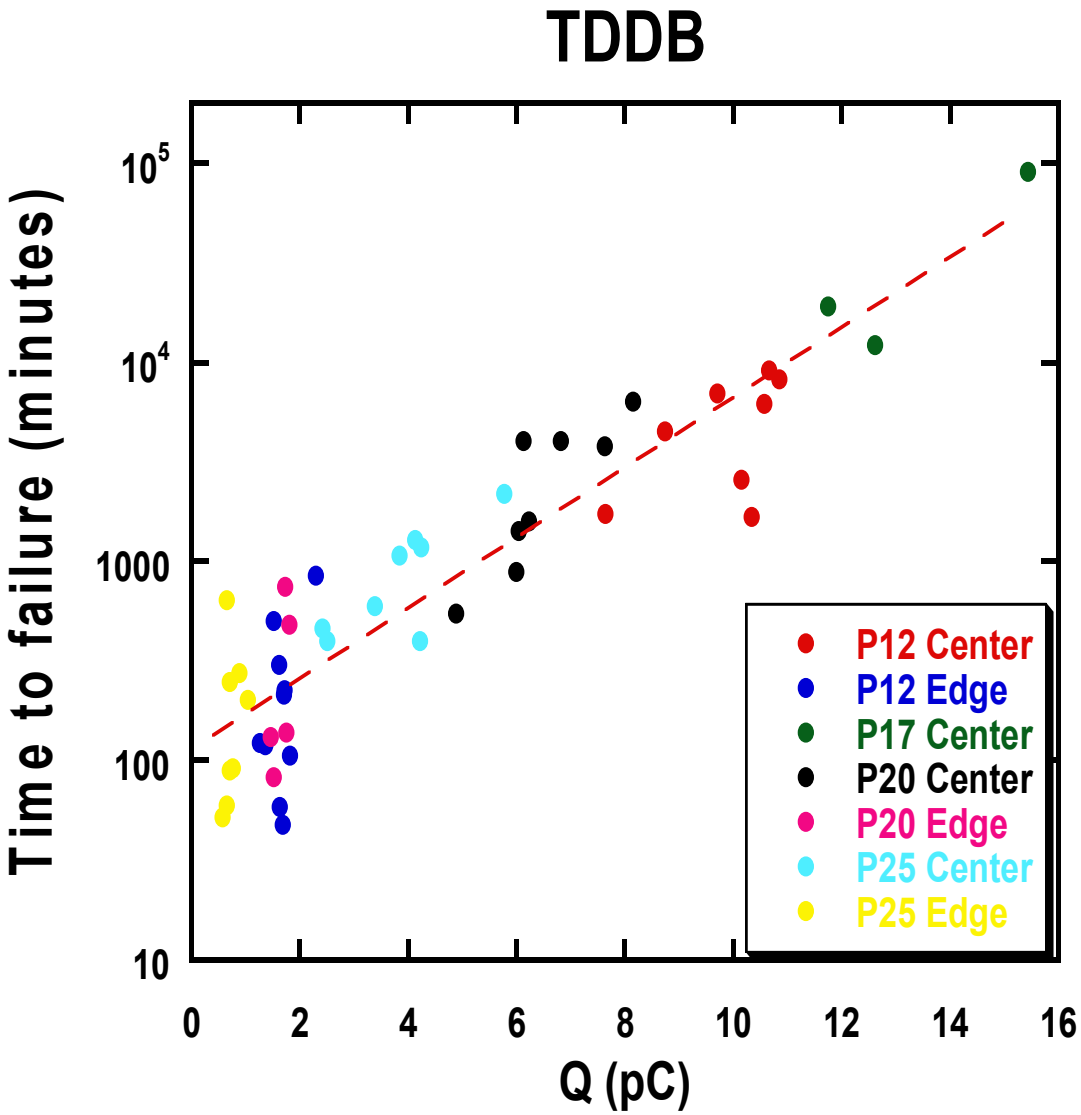

Figure 4.37 TDDB data of center and edge samples from 4 wafers

Figure 4.37 indicates that while factor Q of edge samples is in a narrow range (1 ~ 2pC), center samples showed a variety of factor Q (2pC ~ 16pC). This is because 4 tested wafers are fabricated through different PECVD condition, and thus dielectric properties are expected to be different. Based on factor Q, the plot suggests that P25 center samples (Q = 2 - 4pC) might have most defects in dielectric while P17 center samples (Q = 12 -16pC) have least defects and TTDB lifetime data supports this assumption. Average TDDB lifetime of P25 center samples and P17 center samples are 950 minutes and 40862 minutes, respectively. Figure 4.37 also indicates that as factor Q increases, TDDB lifetime increases exponentially and follow

$$TTF = A * exp(B * Q) \qquad (31)$$

where TTF is TDDB lifetime, A is geometrical constant, B is constant that is affected by temperature and Q is factor Q. This result indicates that factor Q might be able to serve as an indicator that can predict dielectric properties.

4.4 Summary

In this chapter, discharge transient current measurement has been introduced and the mechanisms of discharge transient current and its sensitivity to structural defects in SiO_2 dielectrics have been studied. Relationship between discharge transient current and conventional TDDB result have revealed and factor Q is proven to be able to serve as an indicator for dielectric properties.

To understand discharge transient current, source of the current has to be identified. According to several research groups, there are three possible candidates that can contribute to discharge transient current: defect dipoles, trap charges and mobile ions. TSDC measurement is implemented to determine which candidate is the dominant source and the result indicates that source of discharge transient current is mobile ions.

Discharge transient current is created by the back-diffusion of charge carriers that were displaced during charging process. If defects exist in dielectric, diffusion path will be hindered and current will be reduced. Therefore, discharge transient current of samples with defects in dielectrics is expected to be smaller than normal samples. However, discharge transient current is a parameter that varies with time and this will create difficulties when trying to correlate dielectric properties of samples with the parameter. Therefore, a technique is implemented to acquire a simple parameter factor Q to determine dielectric properties. Factor Q represents the total amount and degree of charges that were displaced during charging process and can be obtained by integrating discharge transient current over discharging time. Similar to discharge transient current, factor Q of samples with defects in dielectrics is expected to show smaller value compares to normal samples.

Discharge transient current measurements have been done on samples from different locations on different wafers at as-received condition. Result indicates that center samples have Q value that is much higher than edge samples. According to the mechanism, this indicates that edge samples might have more defects in dielectrics and this assumption is proven by SEM inspections. For samples that go through aging process,

factor Q does not show noticeable change. This is because discharge transient current measurement is only sensitive to defects in dielectrics and those defects are mainly created during dielectric deposition process but not aging process.

Although discharge transient current is proven to be very sensitive to defects, the source of mobile ions remains unknown. An ideal way of revealing the nature of mobile ions is through activation energy calculation. First, relaxation time of discharging is obtained by a series of measurements under different applied voltage and temperature. Activation energy can then be calculated through relaxation time versus temperature. According to the result, it is likely that the hydrogen contamination in SiO_2 is the source of mobile ions.

To further understand how defects affect mobile ion migration in dielectrics, another series of capacitance measurements are done on the samples. Result shows that peak frequency of samples with defects increases as AC bias level increases. The migration speed and distance of mobile ion is proportional to the AC bias level. If defects exist in dielectric, migration distance will be affected but migration speed will not. Therefore, as AC bias increases, migration speed will increase accordingly but not migration distance and this will reduce the time (relaxation time) it takes for ion to return to its equilibrium position. Peak frequency, which is inversely proportional to relaxation time, is then increased with increasing AC bias level. Therefore, result of capacitance measurement indicates that mobile ions' migration path can be hindered by defects in dielectric.

The last step of this research is to correlate factor Q with the result from conventional reliability test. One of the most common reliability tests for dielectric properties is TDDB test. In this study, TDDB tests are performed on samples from different locations on different wafers. The result indicates that factor Q is exponentially proportional to TDDB lifetime.

CHAPTER 5

PARTIAL DISCHARGE DIELECTRIC BREAKDOWN SEEN IN LOW VOLTAGE AL/SIO_2 INTERCONNECTS

5.1 Background

Partial discharge dielectric breakdown (PDDB) is a phenomenon commonly seen in high electrical voltage devices (typically in range of thousand volts) [130]. However, it is rare to observe partial discharge in microelectronic devices at relatively low voltage (in range of tens of volts). In this study, PDDB has been observed in Al/SiO_2 interconnect and the mechanisms behind PDDB will be discussed in this chapter.

Corona discharge, a gas discharge where atoms and molecules are ionized and become mobile ions under inhomogeneous electric field, is the first step of PDDB. Corona discharge is a phenomenon where gases around electrode is ionized by local electric field and form a conduction region [136,138]. An important aspect of corona discharge is that electric field at the surface of electrode is high enough to ionize gases, but lower than dielectric strength of dielectrics. Therefore, corona discharge will not induce complete dielectric breakdown.

Geometry of electrode is an important factor for corona discharge as electric field around sharp electrode is stronger than blunt electrode. Another important factor is the inception voltage (electric field), which refers to the minimum voltage required for corona discharge to occur. Cavities such as voids and cracks can be considered as air gapes locating inside dielectrics. With certain electric field, it is possible for air gapes to

experience corona discharge and charges will be built up in air gapes, eventually lead to PDDB.

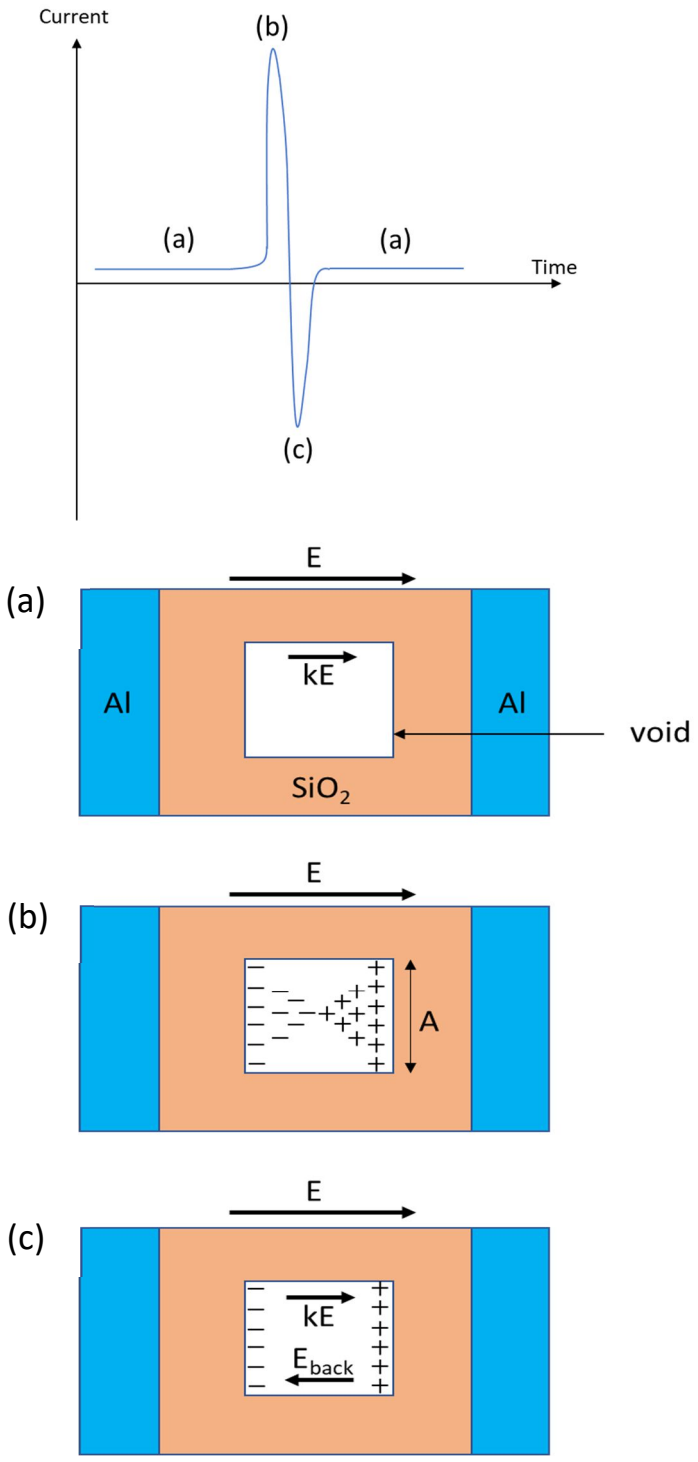

Figure 5.1 Schematic of PDDB in dielectric

Unlike complete dielectric breakdown, PDDB is a breakdown phenomenon where dielectric is partially bridged by discharges and electric current will swing up and down with high frequency [131,132,137]. A schematic of PDDB is shown in Figure 5.1. Assume an electric field E is applied to an Al/SiO_2 interconnect with a void exists inside dielectric, as seen in Figure 5.1a. The electric field across the void will be kE, where k is a factor related to geometry of void. When kE is larger than the inception electric field for corona discharge to occur, atoms and molecules inside void will be ionized around electrode [133] and a discharge channel with high conductivity is formed between two opposite void surfaces, as seen in Figure 5.1b. Therefore, electric current will increase as effective electric field is increased. As a result, electron will migrate to anode and accumulate at the interface while positive ions doing the opposite. This uneven charge distribution will create an internal field E_{back} that is opposite to the direction of kE [135] and electric field across void will then become $E_r = kE - E_{back}$, where E_r is the residual electric field across void. Since E_r is smaller than inception electric field, corona discharge will be terminated. Charges that are accumulate at surface of void will then discharge back and create an electric current with opposite direction, as seen in Figure 5.1c. Then next partial discharge will occur when electric field across void is higher than inception electric field and the cycle will continue. Amount of charges released during PDDB is governed by equation [133]

$$Q = \varepsilon_r * \varepsilon_0 * A * (E - E_r) \qquad (32)$$

where ε_r is dielectric constant of gases inside void, $\varepsilon_0$is dielectric constant of vacuum, A is discharge area of void, *E* is the electric field across void when PDDB occur and E_r is residual electric field.

5.2 Experimental Setup and Test Strategy

5.2.1 Test Samples

Wafers provided by Texas Instruments were used in the research. Samples taken from the wafers contain Al/SiO_2 interconnects (dielectric width = 0.21um, metal line thickness = 0.19um) which were patterned in a specific way known as comb-serpentine pattern.

5.2.2 Measurement System

For PDDB measurement, data acquisition system (HP4140B pA meter/DC source, probe station and PC with LABVIEW DAQ system) introduced in previous chapter was used. Samples were put in the oven introduced in previous chapter during aging process.

5.2.3 Experiment Procedure

Samples go through aging procedure (temperature=185^{o}C) to induce stress defect and leakage current of samples was measured every 100 hours. During measurement, electrical bias is applied to the sample and leakage current data is collected. Typical charging time is 10 minutes and discharging time is 3 minutes.

5.3 Result and Discussion

5.3.1 Abnormal Leakage Current Seen in Aging Samples

Around 80 samples are selected and tested at as-received condition and all samples show a typical charging behavior as introduced in previous chapter. However, after several hundreds of aging process, 10% of the samples start to show abnormal leakage current behavior and a set of data is plotted in Figure 5.2 as an example. This abnormal leakage current behavior might be related to PDDB due to: First, the signature high frequency current swing. Second, the current is too small to be considered as complete breakdown. For PDDB to occur, two key factors must be fulfilled: First, there are defects existing in dielectric. Second, there is an inception voltage for corona discharge to initiate.

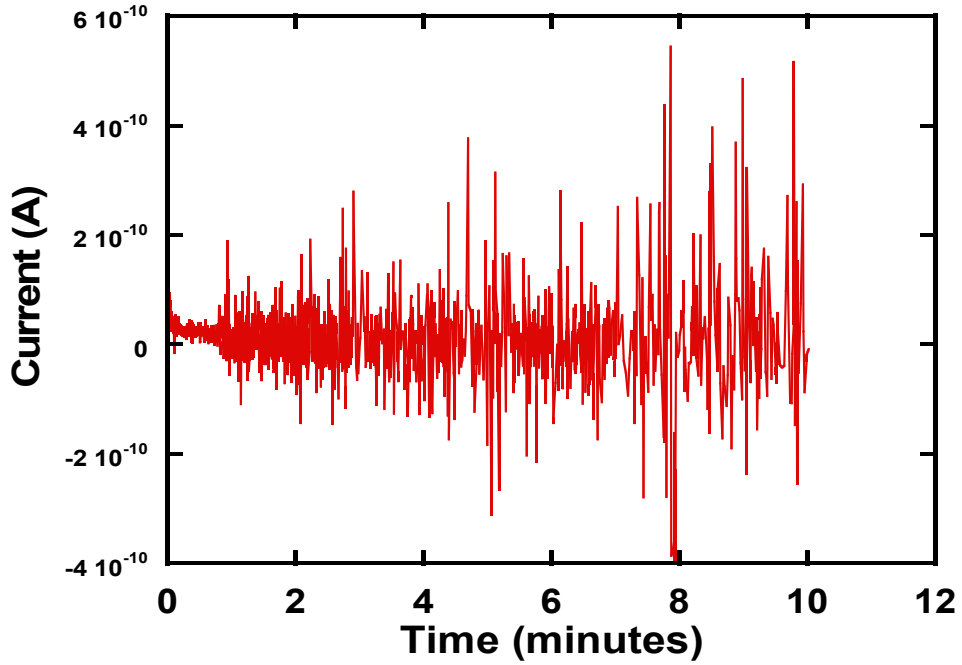

Figure 5.2 Abnormal leakage current data

5.3.2 Defects in Dielectrics

As discussed in previous chapter, it is known that aging process will create defects in interconnects due to different thermal expansion coefficient of aluminum and SiO_2. Most common defects seen in this scenario are void and extrusion. Since the source of PDDB is corona discharge in cavity, extrusion is not likely to be responsible for the abnormal current behavior seen in the research. On the other hand, void is the possible cause of corona discharge as it creates cavity in dielectric.

For PDDB to occur, there should be cavities existing inside dielectric. According to C. G. Karagiannopoulos [134], the cavities can either locate inside the dielectric or at the surface of dielectric. If cavities exist inside dielectric, there will be no polarity dependence

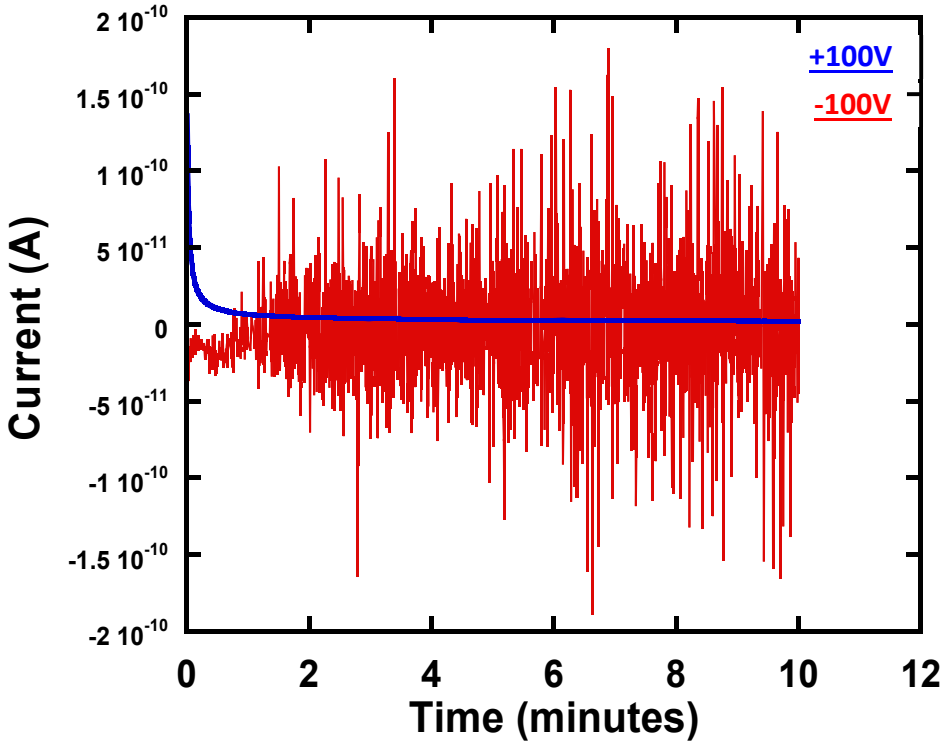

Figure 5.3 Abnormal leakage current data of sample under different bias direction

for PDDB to occur, in another word, if inception voltage is 100V, it is expected to see PDDB when applied voltage is either +100V or -100V. However, data from this research shows that in many cases, under same amount of electrical bias, abnormal leakage current occurs in one bias direction only. Figure 5.3 is an abnormal leakage current data of sample under different bias direction. It indicates that when applied voltage is +100V, sample shows a typical charging behavior. But when applied voltage is -100V, abnormal leakage current behavior occurs. Therefore, it is likely that the PDDB seen in the study is due to defects locating at interface of dielectric.

In previous chapter, a simulation of a void locating at the metal/dielectric interface has been done and result indicates that sharp edge at void can create highly concentrated electric field, which is able to initiate corona discharge. A series of SEM inspections were done on samples that showed abnormal charging behavior and many cavities can be observed at the surface of metal/dielectric interface.

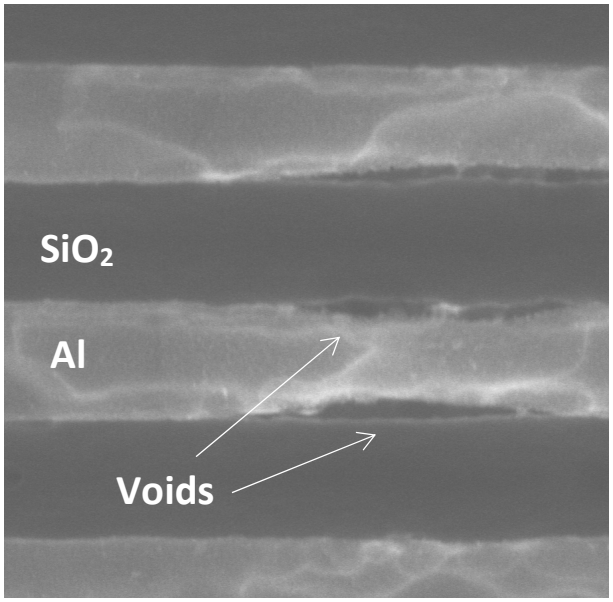

Figure 5.4 SEM image of sample showing abnormal charging behavior

Figure 5.4 is a SEM image of a sample with capping layer removed. Lines with dark contrast are SiO_2 and lines with bright contrast are Al. The darker contrast inside Al lines are voids. As the figure indicates, voids can be seen at interface of Al/SiO_2.

5.3.3 Inception Voltage for PDDB

For PDDB to occur, critical voltage is required for corona discharge to initiate. In order to find the inception voltage, electrical bias applied to sample is increased gradually (1V per step) until abnormal leakage current is observed. Figure 5.5 represents the leakage current data of a sample tested under 53V and 54V, in this example, 54V is the inception voltage for this specific sample. During the study, inception voltage is not a fixed value, but instead, it varies over different samples. This is likely due to the geometry of void. Void with sharp corner is expected to require a smaller inception voltage as the electric field across the void is larger than void with blunt corner.

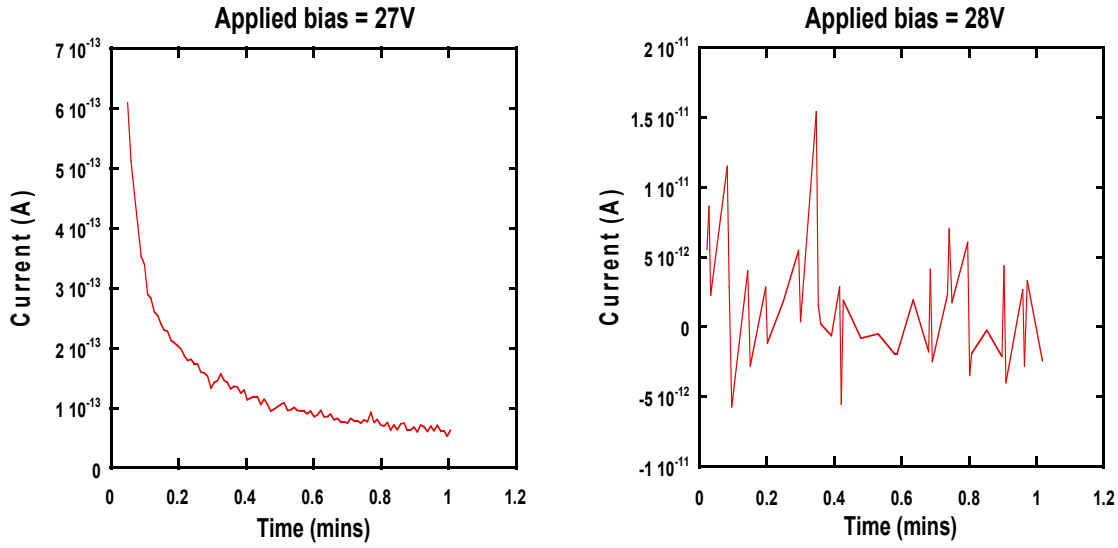

Figure 5.5 Leakage current data of a sample under different voltage

Inception voltage of samples is not only depending on geometry of defects, but also affected by operating temperature. Data of three samples is plotted into Figure 5.6. Figure indicates that as test temperature increases, inception voltage decreases. This matches with reports from several research groups indicating that inception voltage will decrease with increasing temperature [139-141].

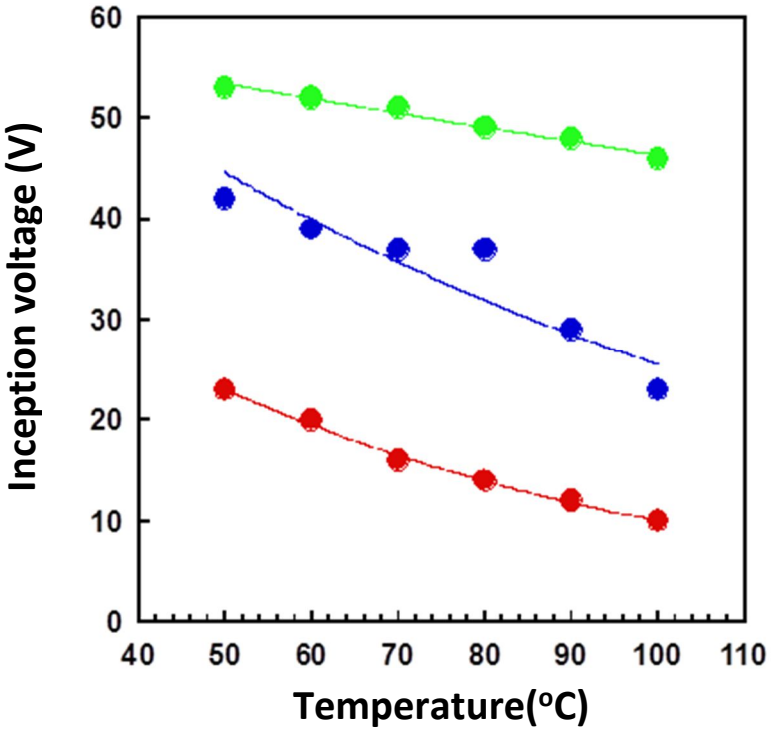

Figure 5.6 Inception voltage versus test temperature of three samples

5.4 Summary

In this chapter, abnormal leakage current behavior of samples that go through aging process has been studied. This leakage current behavior is believed to be partial discharge dielectric breakdown (PDDB), which is initiated by corona discharge. Corona

discharge occurs when gases around electrode is ionized by local electric field and form a conduction region. When defect such as void exists in dielectric, it can be considered as a cavity with gases in it. By ionizing the gases, a conduction path can form inside the void and effective electric field is increased, leading to a up-swing in current. Once ions and electrons migrate to sidewall of void due to applied electric field, an internal field with direction opposite to applied field will be created due to unevenly distributed charge carriers. This will reduce the electric field across the void and corona discharge will be terminated, leading to a discharge that allow charge carriers to return to their equilibrium state and result in a down-swing in current. This process can occur in cycle and can severely damage integrity of dielectric.

There are two key factors for PDDB to occur: Cavity for charges to build up and inception voltage to initiate corona discharge. Cavities such as voids can locate either inside dielectric or at the surface of dielectric. During the research, it was found that many samples showed polarity dependence in PDDB. This indicates that voids are more likely located at surface of dielectric and the prediction is proven by SEM inspection as voids have been observed in metal/dielectric interface. Inception voltage of test samples has been obtained and the result indicates that inception voltage of every sample is different. This is plausibly due to geometry of voids, where voids with sharper corner will require a smaller voltage to initiate corona discharge. With two factors fulfilled and the characteristic swing in current, the abnormal leakage current behavior seen in the research is very likely due to PDDB.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Polarity Dependence Measurement and Its Sensitivity to Structural Defects in Aluminum Lines of Al/SiO_2 Interconnects

Polarity dependence measurement technique has been implemented on chip-level Al/SiO_2 interconnect (dielectric width = 0.21um) with comb-serpentine structure provided by Texas Instruments. Key concept of polarity dependence measurement is to collect leakage current based on bias direction. In this research, main conduction mechanism contributing to leakage current is determined to be the Schottky emission. During polarity dependence measurement, two voltages with same amount but different directions are applied to samples and corresponding leakage currents ($I_{positive}$ and $I_{negative}$) are collected. When defects exist in metal lines, electron injection area is reduced and leakage current should reduce as well. Therefore, metal lines with defects are expected to show some polarity difference ($I_{positive}$ / $I_{negative}$). Result shows that samples taken from edge location of wafer show highest polarity difference while center samples show lowest polarity difference. This indicates that the edge samples contain more defects in metal lines than center and mid samples, and the assumption is substantiated by SEM inspection. Therefore, polarity dependence measurement might be able to serve as a detection technique that can predict the quality of Al metal lines.

Although polarity dependence measurement showed some promising result, the reason why samples always showed higher leakage current when electrons are injecting

from serpentine metal lines is still unclear. One of the possibilities is that the geometry of serpentine lines and comb lines is different and it might have some effect on electron injection area. Further studies are necessary to understand the geometrical effect of different metal lines.

6.2 Current Voltage Measurement and Its Sensitivity to Structural Defects in Aluminum Lines of Al/SiO_2 Interconnects

Key concepts of current voltage measurement (I-V curve measurement) and two-point measurement are to collect leakage current under different bias level. During I-V curve measurement, different level of voltage has been applied to samples and leakage current corresponding to each voltage has been collected. Basic mechanism of both measurements is that when defects exist in metal lines, they have two effects on leakage current, electron injection area is reduced but current density is increased because of high local field at sharp corners created by defects. At low voltage, effect of electron injection area is dominant and therefore leakage current reduces. At high voltage, effect of current density is dominant, and thus leakage current increases. Result of I-V curve measurement on as-received samples shows that edge samples have different I-V curve from center samples. Compare to center samples, edge samples have lower leakage current at low voltage but higher leakage current at high voltage. It indicates that edge samples have more defects in metal lines than center samples, which matches with the result from polarity dependence measurement. During Two-point measurement, two voltages (45V

and 85V) are applied to samples and corresponding leakage currents are collected. A simple current ratio (I_{85V} / I_{45V}) can then be used to evaluate the quality of Al metal lines as metal line with more defects is expected to show a higher current ratio. Result of two-point measurement on as-received and aging samples shows that edge samples have higher current ratio at time zero, and higher increase rate of current ratio over aging time. This indicates that edge samples might be more prone to stress voiding and overall have worse properties compare to center samples. The prediction is then proven by SEM inspection, and thus current ratio collected from two-point measurement might serve as an indicator for Al metal lines properties.

Although two-point current ratio is proven to be sensitive to structural defects located in Al metal lines, a combination of theory study and simulation still need to be done. More study is required to derive equation that can describe the relationship between current ratio, average defect size and defect amount. Equation should then be verified by actual SEM inspection or simulation. Since effect of defects is a 3-dimensional property and SEM inspection is a 2-dimensional inspection method, SEM might not be accurate in terms of calculating amount of defect and average defect size. Defect simulation, on the other hand, can simulate 3-dimensional property and it might be able to give a more accurate relationship between leakage current and defect properties.

6.3 Discharge Transient Current Measurement and Its Sensitivity to Structural Defects in Dielectric Layers of Al/SiO_2 Interconnects

Discharge transient current is created by the back-diffusion of charge carriers that were displaced during charging process. In the research, source of charge carriers has been confirmed to be mobile ions by TSDC technique. And based on activation energy calculation, source of mobile ions is likely to be hydrogen impurities inside dielectrics. Basic mechanism of discharge transient current measurement is that if defects exist in dielectric, diffusion path will be hindered and discharge transient current will be reduced. Therefore, samples with worse dielectric quality are expected to have lower discharge transient current. However, discharge transient current is a parameter that varies with time and this will create difficulties when trying to correlate dielectric properties of samples with the parameter. By integrating discharge current over time, factor Q, which represents the total amount and degree of charges displaced during charging process, can be obtained. Similar to discharge transient current, factor Q of samples with defects in dielectrics are expected to show smaller value compare to normal samples. Result of discharge transient current measurement on as-received samples shows that center samples have Q values that are much higher than edge samples. According to the mechanism, this indicates that edge samples might have more defects in dielectrics and this assumption is proven by SEM inspections. As for samples that go through aging process, Q value does not show noticeable change overtime. This is plausibly due to most defects in dielectrics are created during deposition process but not aging process. To understand how defects can affect ion migration in dielectric, capacitance measurements are done on samples from center and edge locations. Result shows that peak frequency of samples with defects increases as AC bias level increases. This indicates that ions'

migration path can be blocked by defects in dielectric. In the study, TDDB tests, which is one of the most common reliability tests for dielectric, have been performed on samples in order to correlate with factor Q. Result indicates that factor Q is exponentially proportional to TDDB lifetime. Therefore, discharge transient current measurement might be able to predict the quality and reliability of SiO_2 dielectrics by simple parameter – factor Q.

6.4 Partial Discharge Dielectric Breakdown Seen in Low Voltage Al/SiO_2 Interconnects

An abnormal leakage current behavior seen in samples that go through aging process has been studied. Due to the signature up and down swing in leakage current, the abnormal leakage current behavior is likely due to partial discharge dielectric breakdown (PDDB). For PDDB to occur, there are two key factors: cavity for charge to build up and inception voltage for corona discharge to initiate. Cavity can locate inside or at surface of dielectric. In the study, many samples only show abnormal leakage current behavior in one bias direction. This indicates that voids are more likely located at surface of dielectric and the prediction is proven by SEM inspection as voids have been observed in metal/dielectric interface. Inception voltage of each sample has been measured and it is different for every sample. This is plausibly due to geometry of voids, where voids with sharper corner will require a smaller voltage to initiate corona discharge. With two factors fulfilled and the characteristic swing in current, the abnormal leakage current behavior seen in the research is very likely due to PDDB.

Although the abnormal charging behavior is most likely to be related to PDDB, the reason why only some of aging samples are showing PDDB is still unknown. One of the plausible reason is that inception voltage of those samples are higher than 100V (the limit of HP 4140B unit). If this is the case, geometry of voids is the key factor that affects inception voltage. Therefore, by simulation, relation between geometry of voids and inception voltage might be obtained.

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BIOGRAPHICAL INFORMATION

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