MULTI-PHYSICS DESIGN OPTIMIZATION OF 2D AND ADVANCED HETEROGENOUS 3D INTEGRATED CIRCUITS

by

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I also would like to mention, without all my friends' constant annoyance, I would have completed my thesis much earlier.

August 09, 2018

I would like to dedicate my Ph.D. Dissertation
To

My parents
For their love, endless support and encouragement

My role model, my Brother
Whom I always wanted to chase in the race of knowledge but even after trying hard for years, he was always superior to me. This encouraged me to keep working hard towards the goal of my life.

My loving wife
Who always stood by me in ups and downs of my life and encouraged me to achieve the point at which I'm standing.

August 09, 2018

Abstract

MULTI-PHYSICS DESIGN OPTIMIZATION OF 2D AND ADVANCED HETEROGENOUS 3D INTEGRATED CIRCUITS

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The convergence and miniaturization of computing and communications dictate building up rather than out. As planar device miniaturization continues to its ultimate limits, the complexity of circuit interconnections for 2-D devices becomes a limitation for performance and drives up power dissipation [1]. Failure analysis and its effects are major reliability concerns in electronic packaging. More accurate fatigue life prediction can be obtained after the consideration of all affecting loads on the electronic devices. In this study, an attempt is made to analyze 3 types of packages i.e. Wafer Level Chip Scale Package (WCSP), Quad Flat No-Lead (QFN) Package and 2-Die 3D TSV package. This study will be divided into 2 sections, one will focus on reliability and design optimization of 2D planar packages which includes only one die and other section includes discussion about 3D packages in which multiple dies are stacked on top of each other. The

overall aim of this study is to analyze early failure mechanisms and mitigate problems faced by some assemblies. This includes material characterization, failure analysis, Finite Element Analysis, Design Optimization and proposes a better design to improve cycles to failure under reflow, thermal cycling and drop impact.

Wafer Level Chip Scale packages are widely used packages nowadays, due to the low cost and smallest size. WCSP is a combination of Flip Chip packages and Chip Scale Packages. As the name suggests, IC packaging is formed at the wafer level in the wafer foundry. This is how WCSP is distinguished with other packages where packaging is done into 2 parts Wafer and Singulation of wafers into IC's [2]. This is the reason manufacturer can save a lot of time during different stages of manufacturing and hence WCSP's are less expensive. This study focuses on failure analysis of early failure in the packages and change in design parameters for improved solder joint reliability and mitigation of early failure. Further, the effect of different parameters like underfill, Cu pillars, Block of solder balls etc. are studied on the reliability of WCSP packages.

Quad Flat No Lead Package is a Surface Mount Technology (SMT) also known as Micro Leadframe (MLF) and Small Outline No Leads (SON). This package is a near chip scale plastic encapsulated package made with a planar copper lead frame substrate [2]. In this study, a design optimization is performed to improve SJR for packages used with very thick PCB around 3.45mm. Different solder profile has been tested to observe the effect on SJR under thermal cycling.

Furthermore, QFN is tested under drop test at various temperatures. This is attempting to analyze the impact of drop at a different temperature as electronic devices will not be necessary at OFF condition during the drop situation in real life.

As the consumers demand more functions on their hand-held electronic devices, the need for more devices such as memory, CPU, and GPU in hand-held type footprints is increasing. Chip-stacking (3-D) is emerging as a powerful tool that satiates such IC package requirements [1]. A 3-D FPGA would overcome the interconnect limitations, resulting in greater silicon efficiency per function (number of used gates/total number of gates), faster signal/data throughput, and faster switching of the gate-level configuration. 3-D through-silicon-via (TSV) technology is being termed as the "***next big thing***" in the semiconductor arena and has the potential of revolutionizing the packaging industry but it has some inherent issues that need to be addressed before it could be implemented in the mainstream electronics industry. TSV fabrication process, thermal management of 3-D TSV packages, TSV joule heating, and chip package interaction (CPI), are some of the key issues in this technology.

In this dissertation, the thermo-mechanical chip-package-interaction (CPI) analysis is carried out and a full field compact 3D modeling methodology has been leveraged to assess the mechanical integrity of a 2 die 3D TSV package during attachment to the substrate. This modeling methodology would provide damage predictions caused due to global and local CTE mismatch between the different

package components. Mechanical interaction at the Si/TSV regions, back-end Cu/low-k stack and the inter-die μ-bumps during chip attachment is demonstrated in this study. Further, multivariable design optimization is carried out to improve the reliability of components under reflow and thermal loads. It is clear from this study that material used for mold and underfills plays important role in the reliability of the whole assembly.

Keywords- Solder Joint Reliability (SJR), Design Optimization, FEA, WCSP, QFN, Chip-Package-Interaction (CPI), 3D TSV, Copper Pumping, Underfill, Drop Test, Reflow Condition, Temperature Dependent Material Characterization.

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Chapter 1

INTRODUCTION

1.1 ELECTRONIC PACKAGING

Electronic Packaging is a multi-disciplinary subject which needs knowledge of all field i.e. Mechanical, Industrial and Electrical Engineering, Chemistry, Physics and Material Science Department. All these disciplines are equally important in Packaging. Electronic packaging provides housing and interconnections of integrated circuits to form an electronic system [3] [4].

Electronic Packaging must provide:

- Circuit support and protection
- Heat dissipation
- Signal distribution
- Manufacturability and serviceability
- Power distribution

Hierarchy of interconnections levels:

Level 0

- Gate-to-gate interconnections on the silicon die

Level 1

- Connections from the chip to its package

Level 2

- PCB, from component to component or to external connector

Level 3

- Connections between PCBs, including backplanes or motherboards

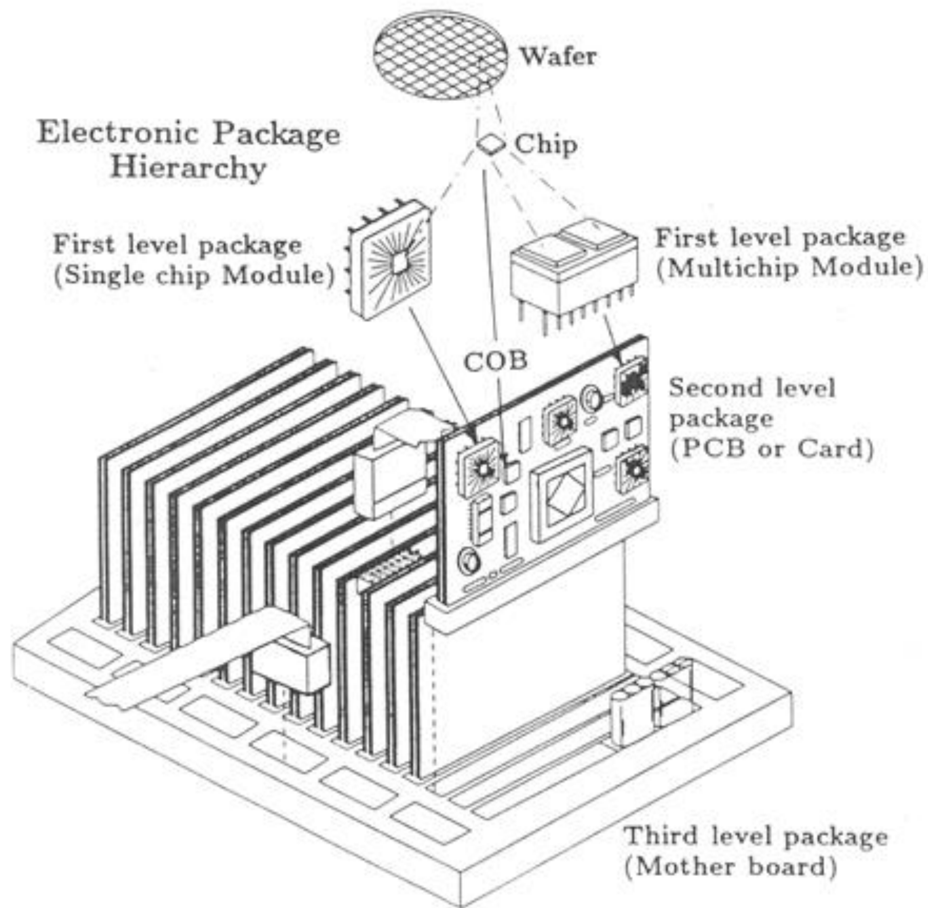

FIGURE 1-1 HIERARCHY OF INTERCONNECTIONS LEVELS

Level 4

- Connections between subassemblies, for example, a rack

Level 5

- Connections between physically separate systems, using, for example, an Ethernet LAN

1.2 PACKAGES CLASSIFICATION AND ASSEMBLY

Packages can be broadly classified as-

- Through Hole Mount IC Packages
  - Dual In-line Package(DIP)
  - Pin Grid
- Surface Mount IC Packages
  - Quad Flat Package (QFP)
  - Thin small outline package (TSOP)
  - Small outline J-leaded package (SOJ)
  - Ball Grid Array (BGA)
- Chip Scale IC Packages
  - Chip Scale Package (CSP)
  - Wafer Level

- Stacked Die (2.5D & 3D Packages)

The figure below shows a schematic diagram of the assembly process involving a typical lead frame package. Packages are manufactured after a series of process one at a time using polymers in various forms.

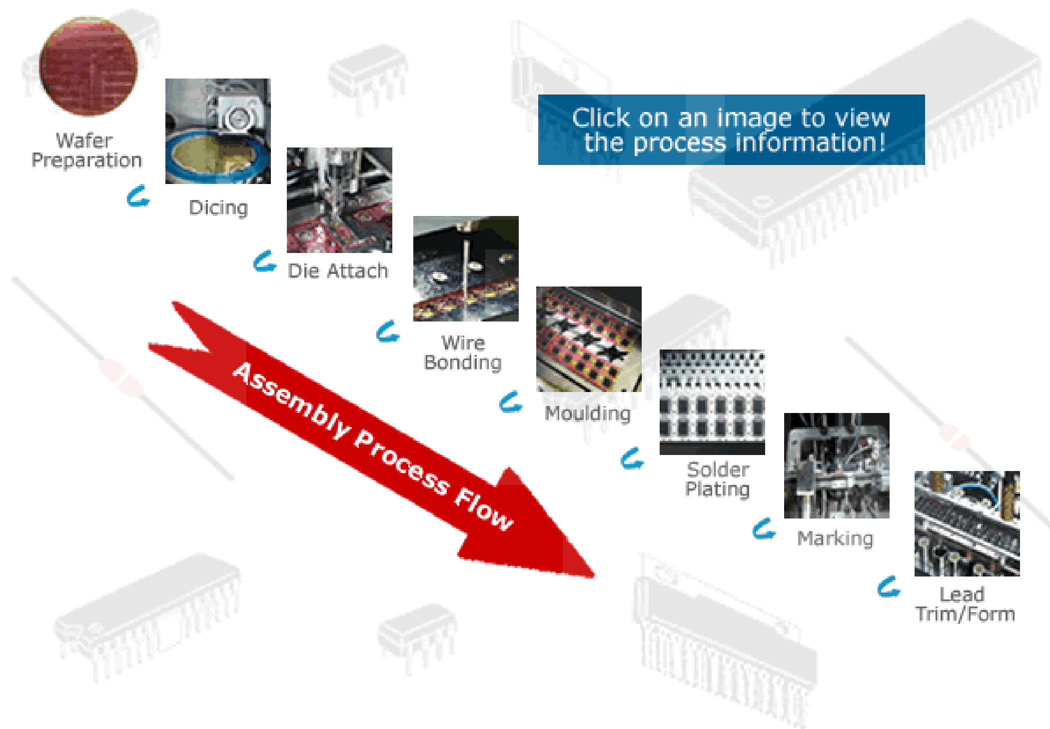

FIGURE 1-2 PACKAGE MANUFACTURING PROCESS

1.3 WAFER LEVEL CHIP SCALE PACKAGES

Wafer Level Chip Scale packages are widely used packages nowadays due to the low cost and smallest size. WCSP is a package is a combination of Flip chip and Chip scale packages. As the name suggests, IC packaging is formed at the wafer level in the wafer foundry. This is how WCSP is distinguished with other packages where packaging is done into 2 parts Wafer and Singulation of wafers into IC's. As a front end and back end, assembly is performed at foundry it saves a lot of time spent after the manufacturing process, which makes these packages very cheap. In this process, the wafer is taken out after the fabrication process before test and IC connections will be formed [2].

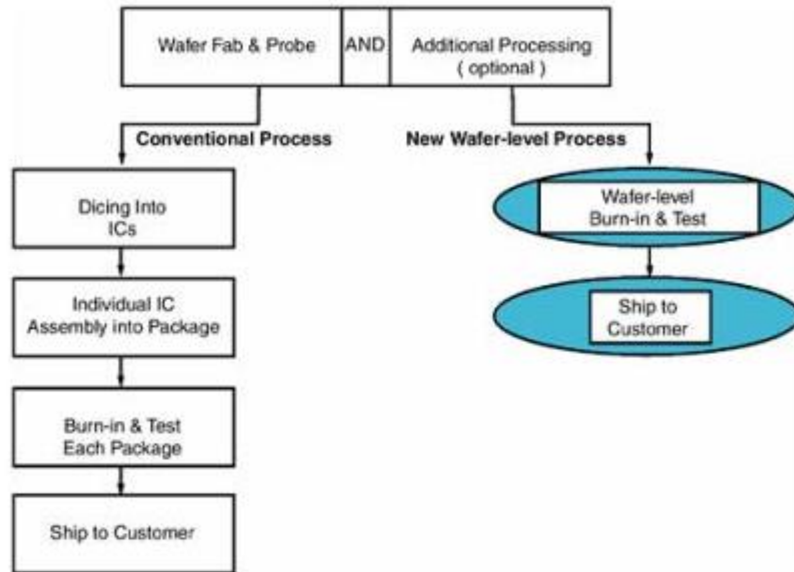

FIGURE 1-3 - COMPARISON OF WCSP WITH CONVENTIONAL PACKAGING [2]

WCSP packages have the advantage of this very low cost and smallest size. Freescale offers WLCSP size and thickness with various options of I/O and solder ball pitch of 0.4 and 0.5mm. The physical size of WCSP is dynamic since it depends on actual die size. [5]

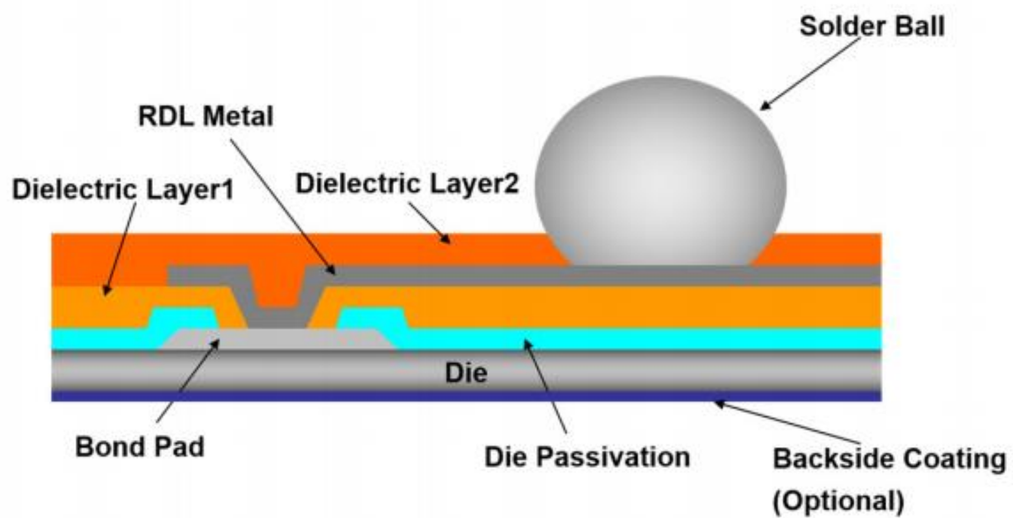

FIGURE 1-4 TYPICAL POLYMER-RDL WLCSP CONSTRUCTION [5]

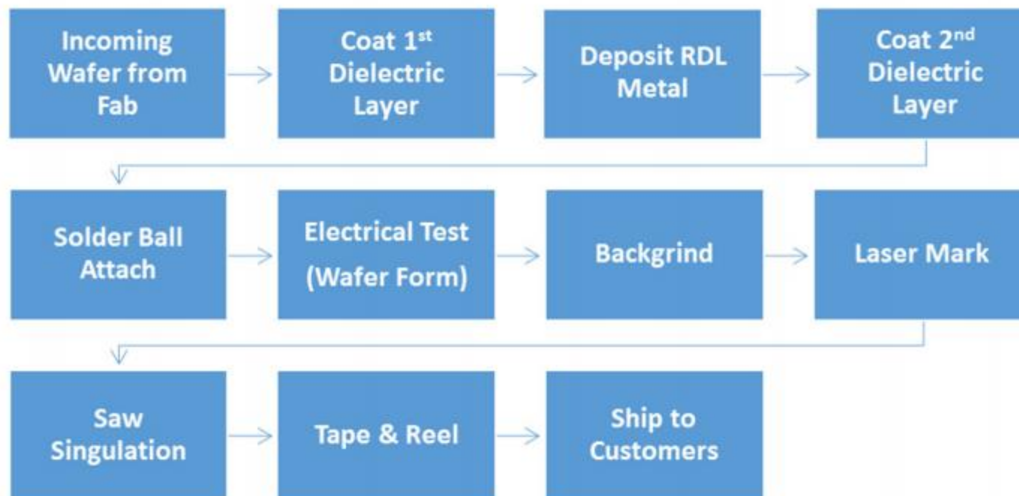

FIGURE 1-5 WLCSP PROCESS FLOW [5]

1.4 QUAD FLAT NO-LEAD PACKAGES

Quad Flat No Lead Package is also a Surface Mount Technology (SMT) also known as micro lead frame (MLF) and small outline no leads (SON). This package is a near chip scale plastic encapsulated package made with a planar copper lead frame substrate. The QFN (Quad Flat No-lead) package is probably the most popular semiconductor package today because of four reasons: low cost, small form factor and good electrical and thermal performance. The QFN can have single or multiple rows of a pin. For this study, I have considered 4 rows of pins, a total of 64 pins.

QFN have an exposed thermal pad on the bottom side of the package which can be soldered directly to the system PCB for optimal thermal transfer of heat from the die. The benefits that come from choosing the QFN packages include a decreasing lead inductance due to optimally short bond wires, lightweight, thin profile and small sized “near chip scale” footprint. Moreover, thanks to the exposed copper die pad, the QFN is perfect for many new applications that need better performance in size, weight and their thermal and electrical properties. Downsides of adopting QFN packages include a possible floatation of the 3×3 mm DFN packages on the on the pool of molten solder under the thermal pad during assembly; oxidation problems of the exposed chip contact pads; missing clearance of a soldering pencil to reflow pads under the chip if touch up is desired [6]. These issues can be mitigated by better control of the re-flow process and using QFNs which are plated (Tin common) to lessen oxidization issues [7]. Although a wire bonding is the most common method for the die to package connectivity, some packages are manufactured with flip-chip die due to its better electrical performance.

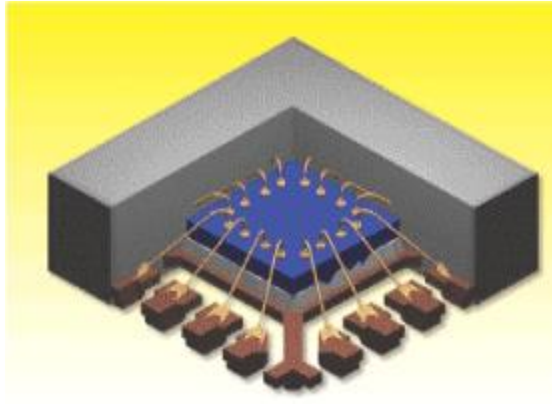

FIGURE 1-6 TYPICAL QFN CROSS SECTION

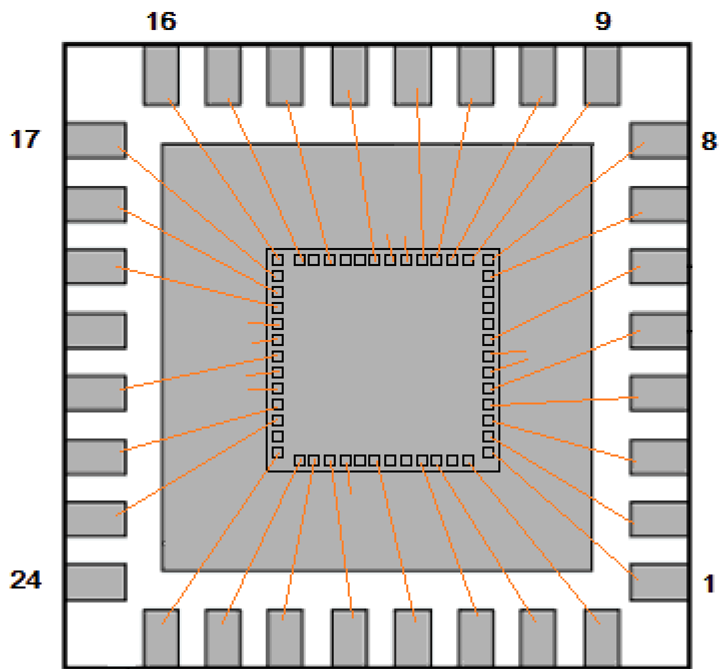

FIGURE 1-7 QFN WIRE BONDING CONNECTIONS [7]

1.5 3D TSV PACKAGES

Consumer electronic products such as digital cameras, personal digital assistants, cell-phones etc., require high functional integration in small footprints with low cost. Multi-chip packaging (chips packaged on the same plane) is one of the solutions. But, due to miniaturization, coupled with the requirements of high memory density, performance, and more features per cm^2 of Printed Circuit Board (PCB), engineers have been forced to think vertically. Stacking dies and interconnecting them vertically accomplishes all these goals. 3-D stacking of the processor and memory components in high computing applications reduces the communication delay in a multi-core system owing to reduced system size and shorter interconnects [8].

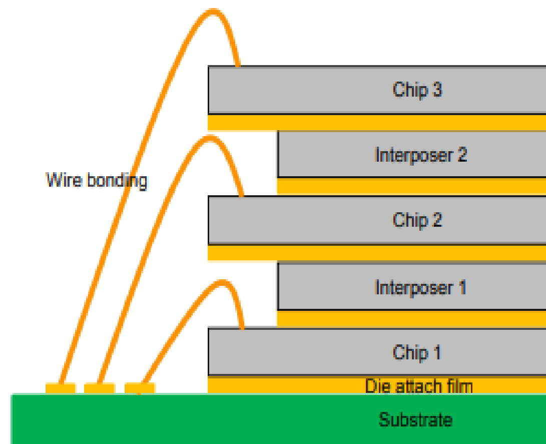

FIGURE 1-8 3 DIE STACKED 3D WIRE BONDED PACKAGE

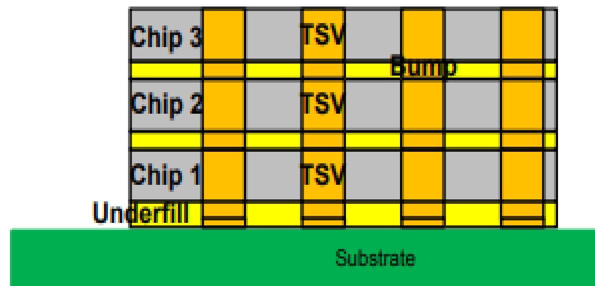

FIGURE 1-9 DIE STACKED 3D TSV PACKAGE

As shown in figure 1-8 & 1-9, 3d packages take same real estate as of 2D but it has more power generation than 2D packages as multiple dies are stacked on each other. High-density-interconnects (HDI), necessitates area array packaging with a much higher number of interconnects as well as reduced footprints leading to 3D TSV technology. Hybrid-memory-cube (HMC) is one such development [9]. HMC is a small, high-speed logic layer that sits below vertical stacks of DRAM die that are connected using through-silicon-via (TSV) interconnects. 3-D IC technology is a promising approach to reduce interconnection power, increase communication frequency, improve design flexibility and enable seamless system-level integration of heterogeneous technologies. The GLOBALFOUNDRIES 3D innovation roadmap for high- performance computing is shown below in Figure 1-8 [10].

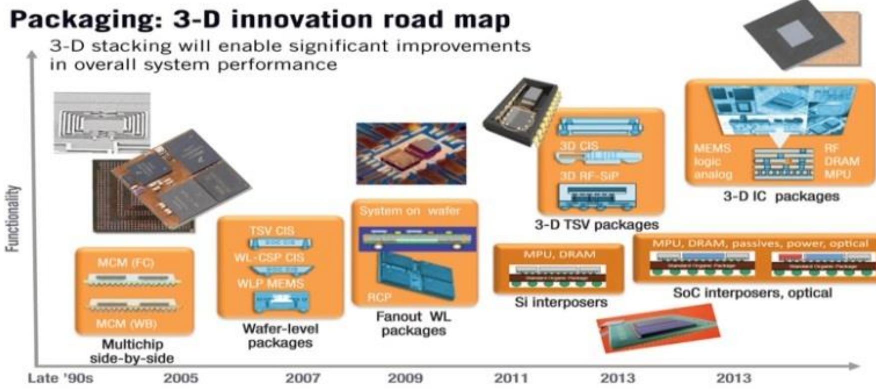

FIGURE 1-10 3D INNOVATION ROADMAP - GLOBALFOUNDRIES

In this dissertation, the thermo-mechanical chip-package-interaction (CPI) analysis is carried out and a full field 3D modeling methodology has been leveraged to assess the mechanical integrity of a 2-die 3D TSV package during attachment to the substrate. This modeling methodology would provide damage predictions caused due to global and local CTE mismatch between the different package components. Mechanical interaction at the Si/TSV regions, back-end Cu/low-k stack and the inter-die µ-bumps during chip attachment and under thermal loads are demonstrated in this dissertation.

Chapter 2

MULTHISICS DESIGN OPTIMIZATION OF WCSP

2.1 ABSTRACT

Various studies have been conducted to study the effect of varying board thickness on the thermo-mechanical reliability of BGA packages. Wafer level chip scale packages (WLCSP) have also been studied in this regard to determine the effect of PCB build-up thickness on the solder joint reliability [11] [12]. The studies clearly demonstrate that the thinner Printed Circuit Boards (PCBs) result in longer thermo-mechanical fatigue life of solder joints for BGA. With the literature and past trends supporting the idea of thinner boards, the manufacturer opted to move forward by decreasing the thickness of their PCBs to improve the reliability of their packages. The thickness was reduced from 1mm to 0.7mm by decreasing the thicknesses of individual layers and keeping the total number of layers constant. When subjected to thermal cycling, it was observed that the 0.7mm board was failing earlier than the 1mm board. Since this behavior of a WLCSP contrasts with the past trends, it required extensive study to determine and understand the pre-mature physics of failure/causality of failure in 0.7mm board. In the previous study in the publication [12], the failure mechanism is determined, and the solution is presented that the life of any assembly also depends on the copper content in PCB board. Cu volume in

the PCB is making PCB stiffer which results in the failure. In this dissertation, an effort is made to demonstrate the failure mechanism published earlier and provide results to support the study. The effect of number & thicknesses of core layers, prepregs and Cu layers in the board has been studied through material characterization of both 1mm and 0.7mm boards. Further, a design optimization and effect of different parameters like using underfill only to corner solder, replacing solder with Copper pillar and creating a block of corner solder has also been presented to improve the thermo-mechanical reliability of this package. Underfilling corner solder has shown a significant amount of decrease in plastic work and showed a better life. Cu pillars are very good for electrical connections as pillars are small in diameter the pitch can be reduced and hence increase in a number of interconnects, but this showed really bad performance in reliability.

2.2 INTRODUCTION

In general, as the board thickness and overall stiffness decrease, the resulting stress, the solder joint experiences decrease. As much as a 2X increase in fatigue life can be realized by assembling CSPs on a thin board [13]. The primary reason for the increase in solder life of a package mounted on a thinner board is basically the reduction in stiffness of the PCB caused due to a reduction in its thickness. Based on this premise, thinner boards were used to mount CSPs for better solder joint

reliability [14] [15]. Both 0.7 and 1mm boards were subjected to thermal cycling tests from -40°C to 125°C and the results show that 0.7mm board failed in less no. of cycles as compared to the thicker board.

Three boards each of 0.7mm and 1mm were subject to thermal cycling and then cross-sectioned into the solder balls of the failing daisy chains as confirmed by the curve trace analysis. The opens observed during curve trace analysis were caused by cracking in the solder balls because of temperature cycle testing [16]. The scanning electron microscopy (SEM) results for 0.7 and 1.0mm boards are shown in figure 2-1.

As it is seen from the figures above the failure mechanism of both the boards is same i.e. failure occurring at the interface of the solder and under metal bump (UMB), the cycles to failure of a 1mm board are 3X the cycles to failure of a 0.7mm board. Since this behavior contrasts with the industrial trends and basic mechanics which suggest that thinner boards are better for solder joint reliability, it was of considerable interest to study this behavior in a thin board.

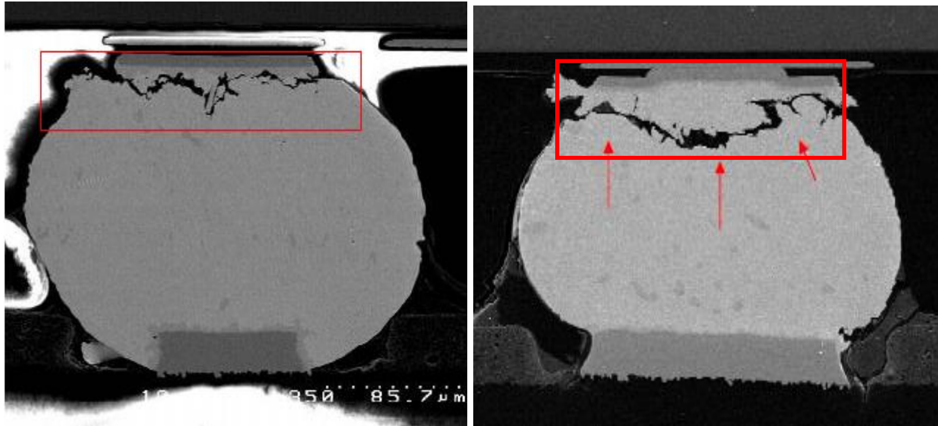

FIGURE 2-1- 0.7 AND 1MM BOARD FAILURE RESPECTIVELY

2.3 MATERIAL CHARACTERIZATION

Material characterization is a very important step in the process of failure analysis and design optimization. An accurate mechanical property is required to eliminate FEA simulation errors, so it was imperative to have all the required material properties of the WCSP provided by Texas Instruments. The material properties required to model a package in ANSYS workbench are given below

- The coefficient of Thermal Expansion (CTE)
- Young’s Modulus (E)
- Poisson Ratio (υ)

To determine these properties the equipment and techniques used are given below-

- Sun Microsystems Oven with DIC
- Instron Micro tester with 2kN Load Cell
- Thermo-mechanical Analysis
- Dynamic Mechanical Analysis

Sample preparation and test procedures for all the tests conducted for material characterization will be explained in this section.

2.3.1 The coefficient of Thermal Expansion (CTE)

The coefficient of Thermal Expansion (CTE) is defined as the tendency of a material which defines the amount by which it expands or contracts when heated or cooled

$$\alpha = \frac{\epsilon}{\Delta T}$$

Where,

α – Coefficient of Thermal Expansion (CTE) ppm/°C

ϵ - Strain (mm/mm)

ΔT – Difference in Temperature (°C)

Since the packages are tested under thermal cycling from -40°C to 125°C in the oven to predict the cycles to failure, it was necessary to know the CTE of the package. As the electronic assembly is made up of composite material, CTE is a critical parameter which induces bending of assembly and hence failures.

2.3.1.1 Heating/Cooling Oven

The oven used for heating the package was a Sun Microsystems Oven with a door for easy access to place and remove packages in the oven. The oven has a 12"x4" borosilicate glass at the top wall for the cameras to view the package clearly. The purpose of using a borosilicate glass is to avoid any reflection caused due to illumination from glass surface into the camera eye. There are two openings on each side wall of the oven which are covered with rubber corks. Thermocouple wires are connected to the sample through these openings which are closed with the rubber corks after the wires have been carefully passed through them.

FIGURE 2-2 SUN MICROSYSTEM OVEN

2.3.1.2 Digital Image Correlation Technique – CTE Measurement

Digital Image Correlation (DIC) is a non-contact and nondestructive technique to measure in-plane and out of plane deformations. A pair of 5MP high-speed cameras is used to capture the images. The cameras were positioned at an angle of 15~20deg from the vertical to have a view of package's in-plane as well as out of plane deformations. The cameras were connected to a software VICSnap to view the image clearly on the screen and select area of interest to be analyzed.

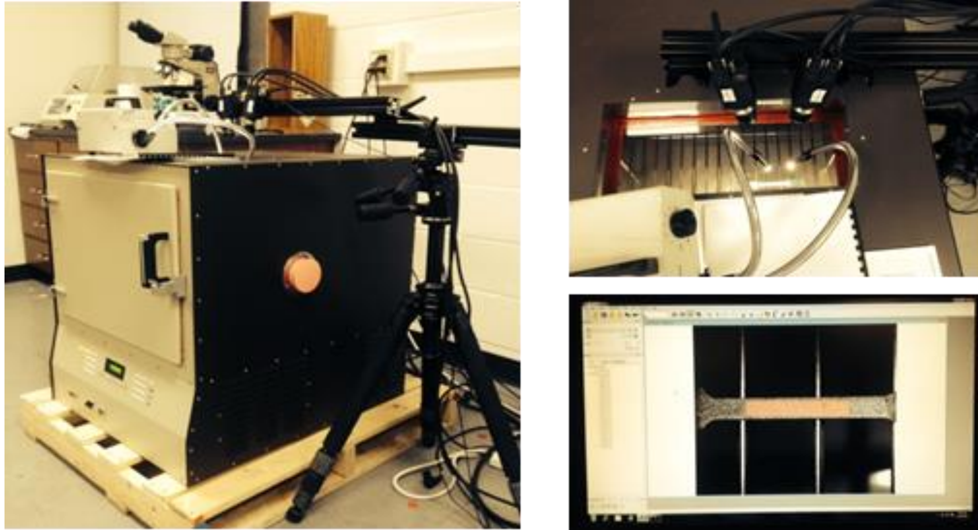

FIGURE 2-3 DIC EXPERIMENTAL SETUP

2.3.1.3 DIC Calibration

It is of utmost importance that before using DIC, the cameras have been calibrated properly so they can measure the smallest deformation correctly. To calibrate the DIC, a calibrating panel with a white base and black dots were used. The pitch between the dots was 4mm and the total number of dots was 108. First, the sample is focused so that the image on the software is clearly visible and sharp, then the calibrating panel is kept at the same height as of the sample and images are taken by the software at different angles of the calibrating panel. The panel is tilted in all directions to get a good focus of the DIC cameras from all directions and

angles. The software is then used to analyze the images of the panel and once the software can view the dots on calibrating panel clearly, the DIC is ready for testing.

2.3.1.4 Sample Preparation

Since the DIC works on the principle of tracking movements of small dots during heating or cooling, it is very important to prepare the testing sample in such a way that it has clearly visible dots on its surface. To achieve this, samples

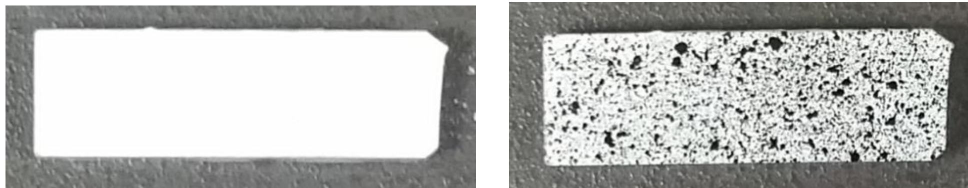

FIGURE 2-4 SAMPLE PREPARATION FOR CTE MEASUREMENT

of 15mmx51mm were cut out from PCB and painted using matt enamel paint. First, a layer of white paint is applied to the sample and left to dry. Once it has dried, black paint is sprinkled on the white layer carefully in such a way that the surface neither gets very large blots nor very few dots. There should be enough dots on the surface for the DIC to trace their movement during expansion. This sample is then kept inside the oven and thermocouples are then connected to it at 3 different locations to measure temperature during the test and avoid any temperature difference within the sample due to the thermal mass.

2.3.1.5 CTE Results

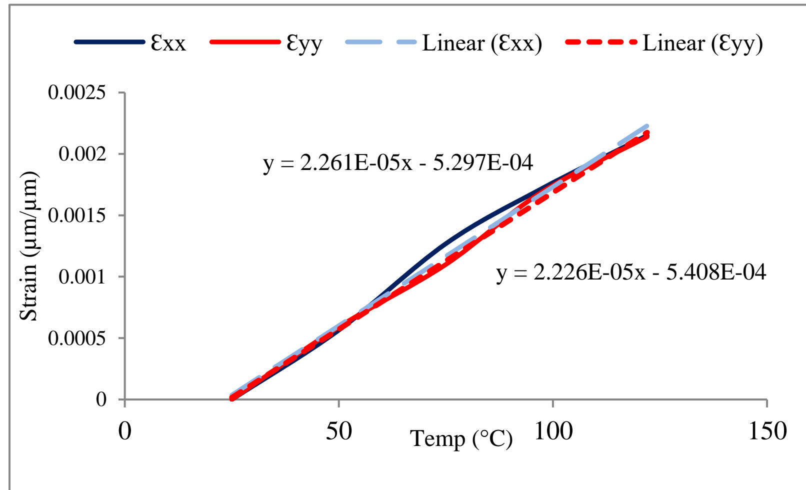

FIGURE 2-5 CTE 0.7MM BOARD

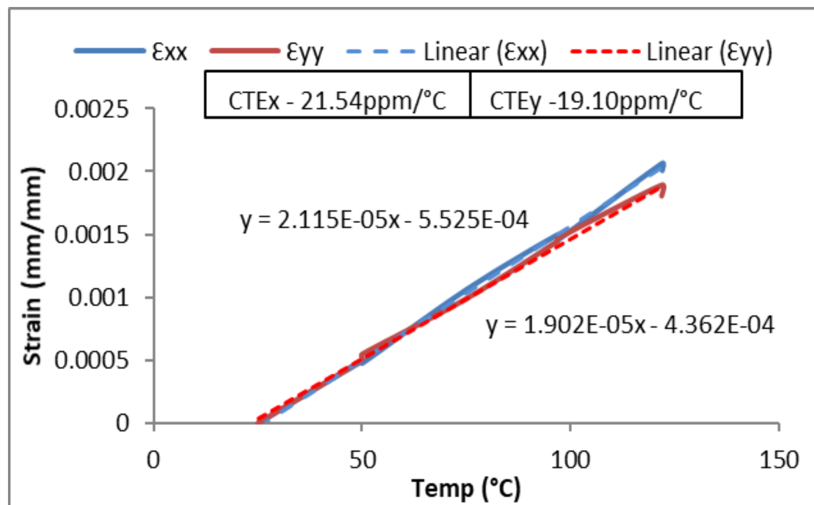

FIGURE 2-6 CTE 1MM BOARD

2.3.2 *Young's Modulus Measurement*

Young's Modulus or Elastic Modulus defines the stiffness of compliance of a material when subjected to tensile or compressive loading. Materials that deform by a small amount when a tensile load is applied to them are said to be stiffer as compared to the materials that deform by a considerable amount when tensile or compressive loading is applied to them. Mathematically, Young's Modulus is defined by the stress produced in a material when some strain is applied to it.

$$E = \frac{\sigma}{\epsilon}$$

Where,

E – Young's Modulus (MPa)

σ – Stress (MPa)

ϵ - Strain (mm/mm)

2.3.2.1 Instron Microtester – Young's Modulus Testing

To conduct Young's Modulus tests, an Instron Microtester of 2kN load cell was used to apply tensile loading to the samples. An extensometer is placed on the sample to measure strain during sample extension. The extensometer is connected to a software to while the Instron is also connected and it gives in-situ force-displacement graph during the test. Stress is calculated by dividing the stress from

the cross-sectional area of the sample and strain is measured using the extensometer. From the stress and strain, Young's Modulus is calculated for a sample.

2.3.2.2 Sample Preparation

ASTM standard [17] was followed to prepare dog bone samples for Instron test. The reason for preparing dog bone samples is to make sure there is enough grip section available for the instron grips to hold the sample tightly during the test. The final shape of the sample is shown in the figure below

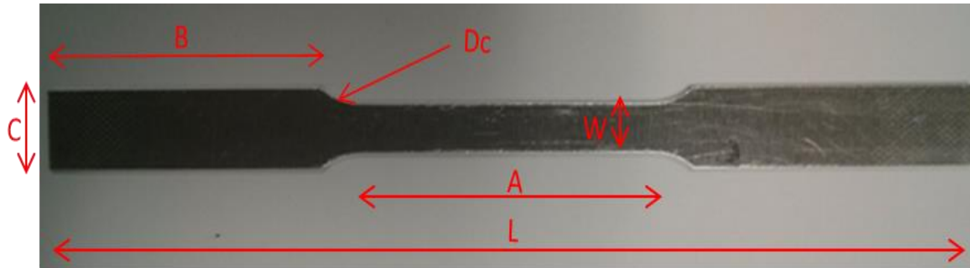

FIGURE 2-7 DOG BONE SAMPLE

The dimensions of the sample as referred from the ASTM standards is given below -

TABLE 2-1 DOG BONE DIMENSION

Dimensions	Value (mm)
L - Overall Length	100
C – Width of grip section	10
W – Width	6
A – Length of Reduced Section	32
B – Length of Grip Section	30
Dc – Curvature Distance	4
R – Radius of Curvature	6

2.3.2.3 Experimental Setup

To measure Young's modulus of PCB samples, Instron Microtester 5848 with a max. the load cell of 2kN was used to apply force. The grip section of the dog bone sample is clamped vertically between the two jaw faces of the Instron tester and an extensometer is placed on the samples with its pins gripping the sample tightly. The extensometer pins have an initial gap of 12mm between them. When a tensile force is applied to the specimen, the extensometer pins which are tightly gripping the

specimen open accordingly and the change in length is measured from where strain is calculated using Instron software.

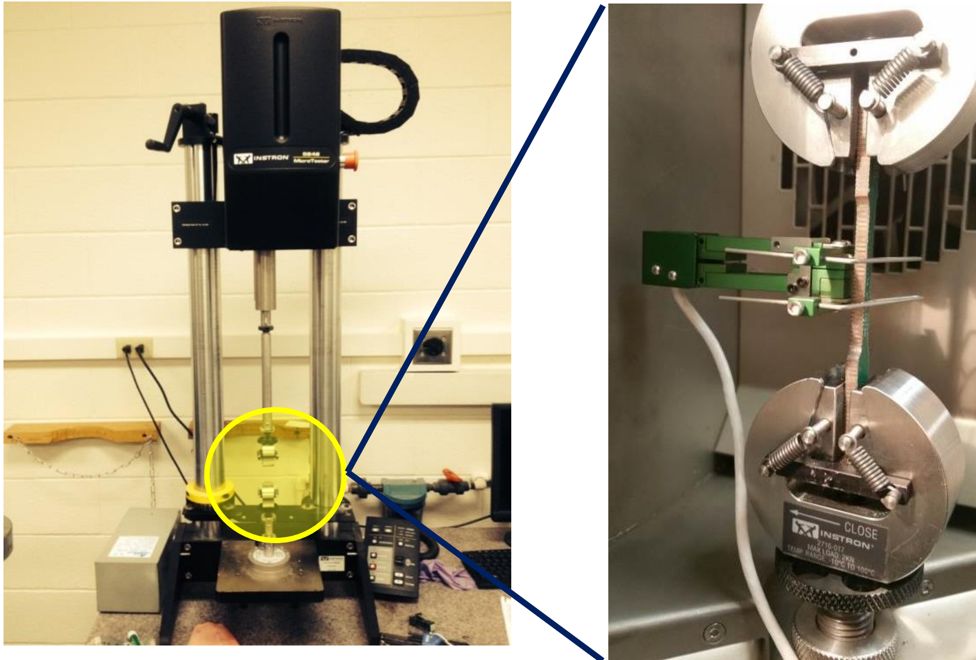

FIGURE 2-8 INSTRON EXPERIMENTAL SETUP

The test setup and procedure as shown in fig 2-8 was benchmarked by testing an aluminum sample and calculating the Young’s Modulus. The experimental result was compared with the theoretical result and was found to be in complete agreement with the theoretical value.

2.3.2.4 Instron Results

The Young’s modulus values as measured by the Instron tester for 0.7 and 1mm boards are shown in

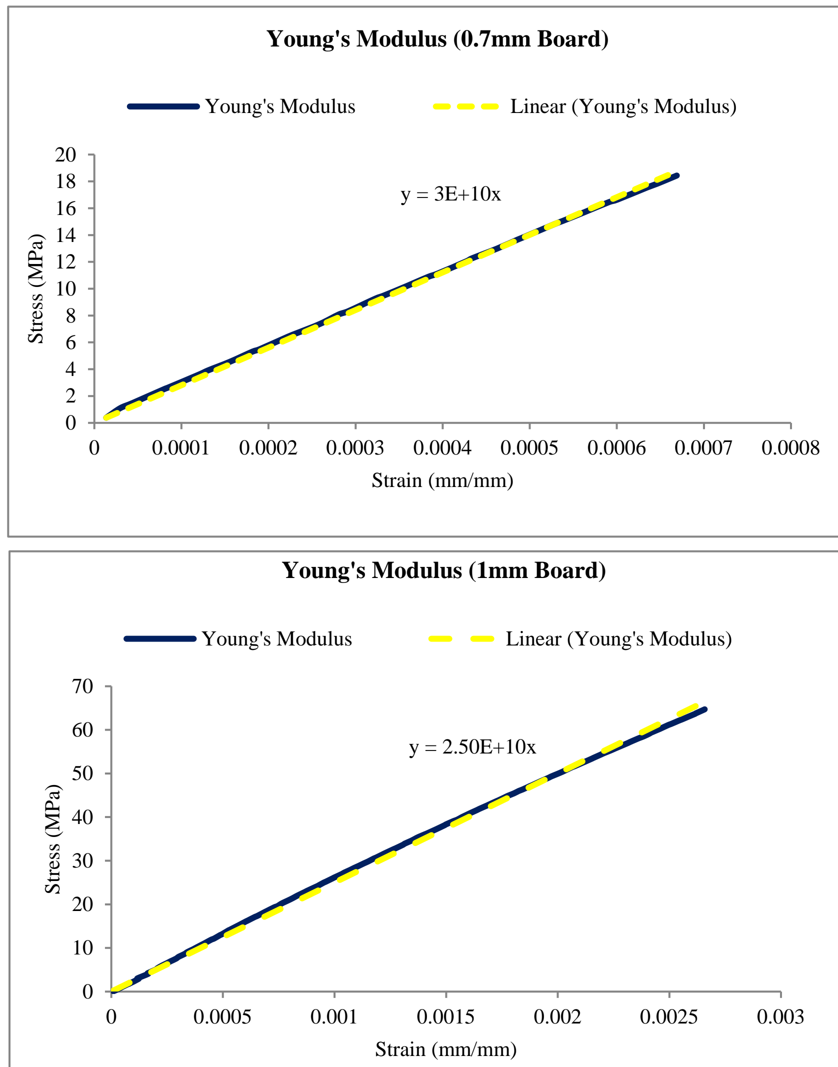

FIGURE 2-9 YOUNG'S MODULUS RESULTS FOR 0.7MM AND 1MM RESPECTIVELY

2.3.3 Storage and Loss Moduli Measurement

The storage and loss modulus in viscoelastic materials measure the stored energy, representing the elastic portion, and the energy dissipated as heat, representing the viscous portion [16]. The tensile storage and loss moduli are defined as follows

$$\text{Storage: } E' = \frac{\sigma}{\epsilon} cos\delta$$

$$\text{Loss: } E'' = \frac{\sigma}{\epsilon} sin\delta$$

2.3.3.1 Sample Preparation and Fixture

Rectangular samples of 40mm x 3mm were used for the test. Samples were mounted in a dual cantilever beam fixture as shown below

FIGURE 2-10 DMA BENDING FIXTURE

2.3.3.2 DMA Results

The results of both the thin and thick boards for storage and loss moduli are given below

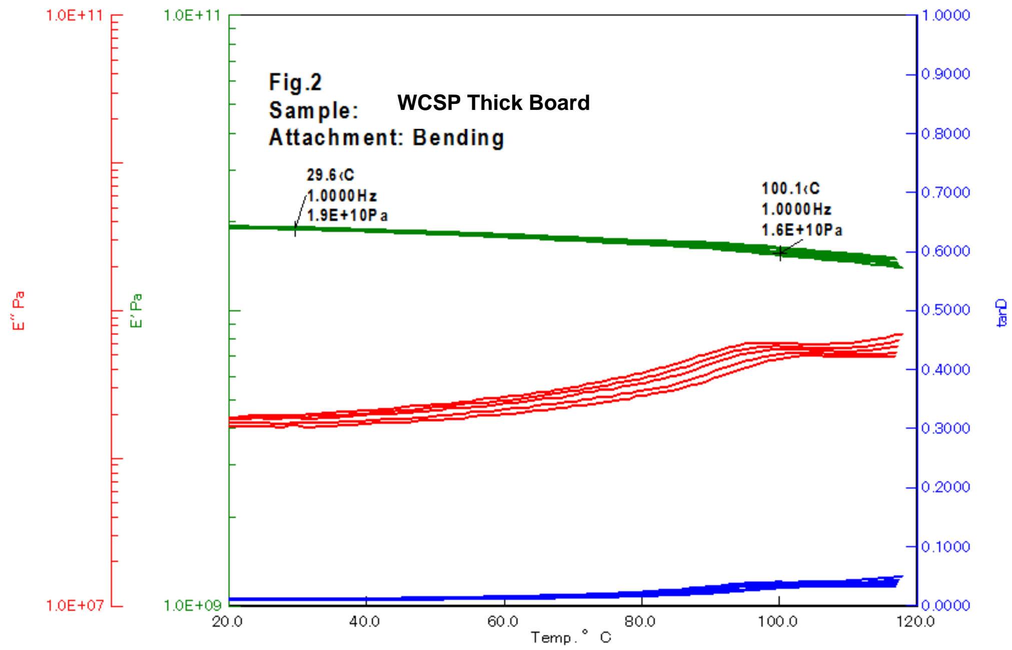

FIGURE 2-11 1MM BOARD TEMPERATURE DEPENDENT YOUNG'S MODULUS

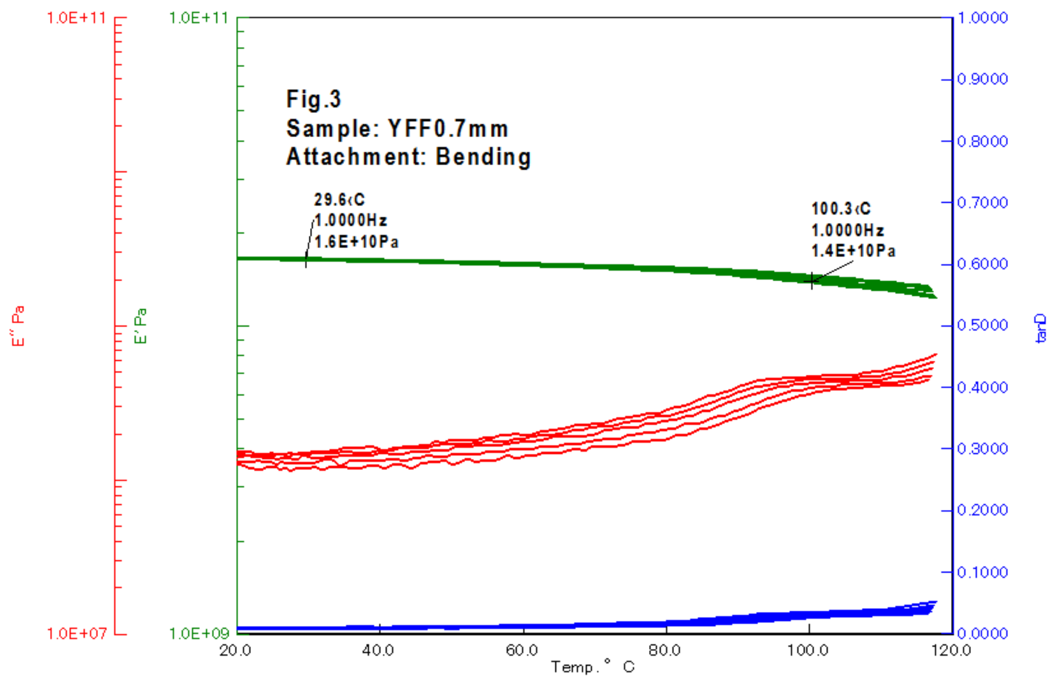

FIGURE 2-12 1MM BOARD TEMPERATURE DEPENDENT YOUNG'S MODULUS

2.3.4 PCB Cross-section

Since 0.7mm board was found to be stiffer than 1mm, it was worth looking deeper into the PCB layer-by-layer stack to find the reason behind the stiffness.

A cross-sectioning methodology was leveraged for this purpose where both the boards were cross-sectioned using a mechanical rotary cutter and small samples of 8x4mm were prepared. These samples were kept under an optical microscope to

have a close look at the layers along the board thickness. The cross-section images from the optical microscope for 0.7 and 1mm boards are shown in fig. respectively.

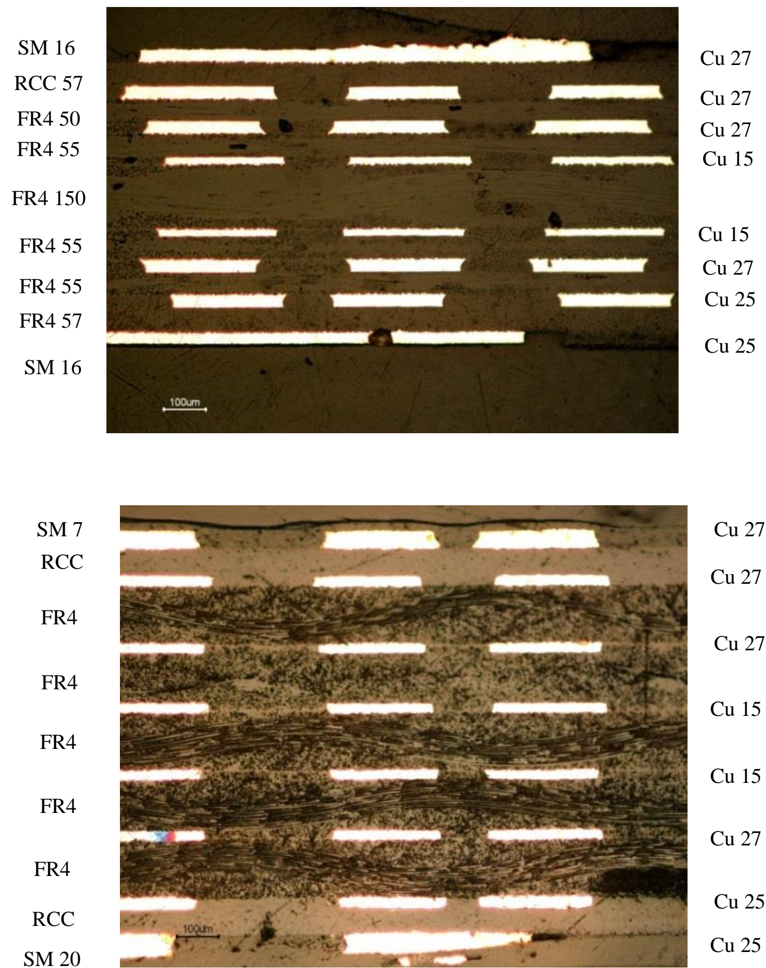

FIGURE 2-13 PCB CROSS-SECTION FOR 0.7MM AND 1MM RESPECTIVELY

As shown in the figures above the overall Cu thickness in 0.7 and 1mm boards is 184µ and 162µ respectively.

2.4 MODELING METHODOLOGY

Commercially available ANSYS workbench 19.0 was used to model both the packages. Both the boards were cross-sectioned and viewed in a digital microscope using a 20X lens to get the detailed layup of the board and the package.

Although the cross-section revealed details of every layer in the PCB as well as 1st level, the PCB was modeled as a block to reduce computational time and use bulk material properties as determined by experiments.

However, the RDL and Polyimide layers were modeled individually, and the material properties were assigned from the literature. Quarter symmetry of the full model was used for faster computation. Fully meshed model with all the layers is shown in fig 2-14 below.

The dimensions used for the models are given below. The only difference between the two models was the thickness of the PCB (0.7mm & 1mm), the rest is the same for both the models [18].

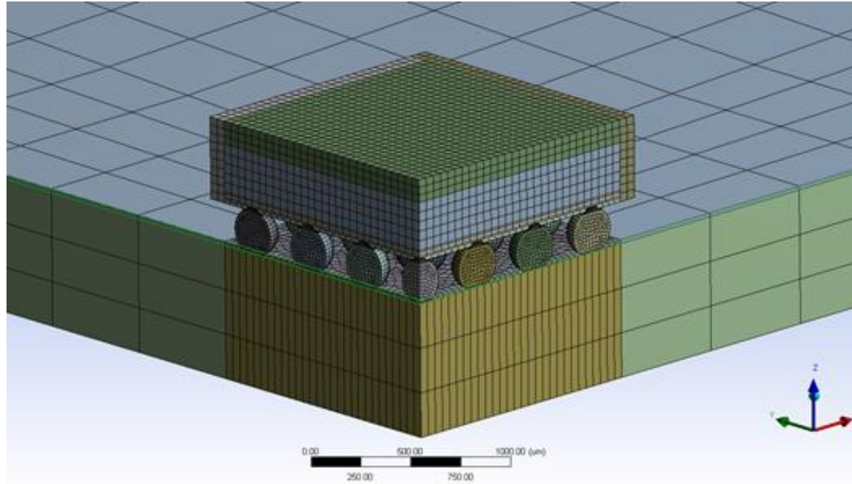
FIGURE 2-14 MESHED QUARTER MODEL

TABLE 2-2 PACKAGE DIMENSIONS

Parameter	**Dimensions(mm)**
PCB(1mm/0.7mm)	24x24x1/0.7
Solder Array	7x7
Solder Día	0.25
Solder Pitch	0.40
Die	2.8x2.8x0.25
RDL	2.8x2.8x0.02
Polyimide	2.8x2.8x0.01
Mold	3x3x0.43

2.4.1 Material Properties

All materials except SAC396 and PCB were modeled linear elastic [19]. PCB was modeled linear orthotropic and SAC alloy was modeled viscoplastic using Anand's viscoplastic model for SAC396 [20] [21].

The material properties used for different materials are given in table 2-3 below-

TABLE 2-3 MATERIAL PROPERTIES USED IN THE MODEL

Material	**Property**				
	E (GPa)	**CTE (ppm/°C)**	**ν**		
			xy	**yz**	**xz**
PCB (0.7mm)	30	23	0.11	0.39	0.39
PCB (1mm)	25	20	0.11	0.39	0.39
Die	131	3	0.28		
RDL	130	16.8	0.34		
Polyimide	1.2	52	0.25		
Mold	24	20	0.3		
Cu	110	17	0.34		
Solder Mask	4	30	0.4		

The elastic part of the constitutive law of lead-free solder 396 can be described by a temperature-dependent Young's modulus and Poisson's ratio (ν=0.40). The temperature-dependent Young's modulus is E=100501−194T(MPa) in which the absolute temperature T is in Kelvin. The coefficient of thermal expansion of the solder is taken to be 23.5 ppm/K

Anand's viscoplasticity for solder can be described as follows [1] [22]

$$\frac{d\varepsilon_p}{dt} = A \sinh\left(\xi \frac{\sigma}{s}\right)^{\frac{1}{m}} \exp\left(-\frac{Q}{kT}\right)$$

With the rate of deformation resistance equation

$$\dot{s} = \left[h_0(|B|)^{\alpha} \frac{B}{|B|}\right] \frac{d\varepsilon_p}{dt}$$

where,

$$B = 1 - \frac{s}{s^*}$$

and

$$s^* = \hat{s}\left[\frac{1}{A}\frac{d\varepsilon_p}{dt} exp\left(-\frac{Q}{kT}\right)\right]^n$$

There are nine material constants in Anand's viscoplasticity law which are given in table 2-4 below for SAC396

TABLE 2-4 ANAND'S CONSTANTS

S. No	**Constant**	**Unit**	**Value**
1	s_0	MPa	3.3
2	Q/R	1/K	9883
3	A	sec^{-1}	15.7E+06
4	ξ	Dimensionless	1.06
5	m	Dimensionless	0.3686
6	h_0	MPa	1077
7	$\hat{s}$	MPa	3.15
8	n	Dimensionless	0.0352
9	a	Dimensionless	1.6832

To determine the life cycles to failure of both the boards, a 25µm layer starting at the interface of the solder and the Under-Bump Metal (UBM) was sliced inside the solder ball as shown in figure 2-15 above. It was shown that the calculated strain energy density increases as element size in the solder joint decreases. Hence, a volume averaging technique was used to reduce this sensitivity to meshing. The strain energy value of each element is normalized by the volume of the element [23].

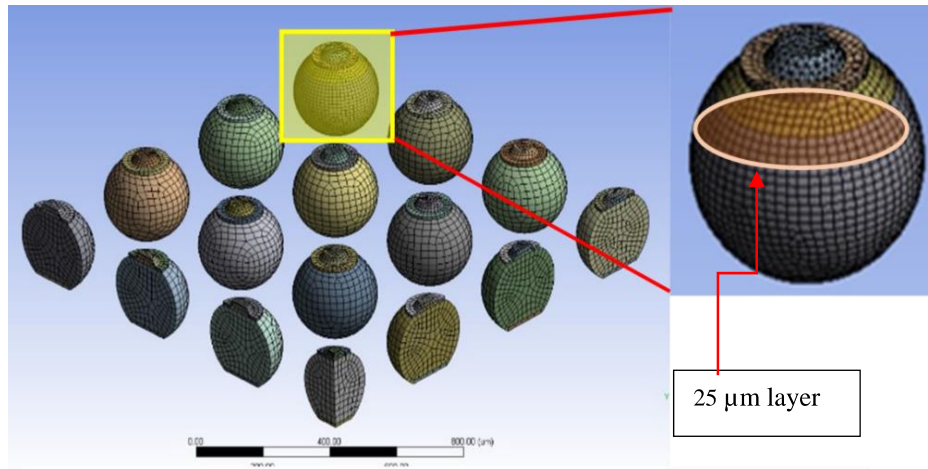

FIGURE 2-15 CORNER SOLDER AND 25UM LAYER

$$\Delta W_{ave} = \frac{\sum \Delta W \bullet V}{\sum V}$$

where ΔW_{ave} is the average viscoplastic strain energy density accumulated per cycle for the interface elements, AW is the viscoplastic strain energy density accumulated per cycle of each element, and V is the volume of each element. This technique helps make the analysis more robust [23]. The volume averaged plastic work was calculated at this sliced portion of the solder by writing an APDL script for calculating the plastic work. The calculated plastic work is then related to life cycles to failure using work-based models. Tin dendrites play important role in understanding SAC behavior [24]. Also, [25] et. al. discussed apparent solder joint

strengthening effect caused due to global stress triaxiality and simple analytical approach to find accurate properties when using such specimens

2.4.2 Loading and BCs

Since the boards were originally tested by TI when subjected to thermal cycling, therefore to replicate the original loading conditions thermal cycling loading was applied from -40°C to 125°C. A total of three cycles with a complete cycle of 60min with 15min ramp and 15mil dwell were applied as shown in fig 15 below. The stress-free temperature of all bodies is 125°C, symmetric boundary conditions were applied to the two symmetric faces and the center node of the full model was fixed i.e. all degree of freedom (DOF) were zero at the center node as shown below in fig 2-16

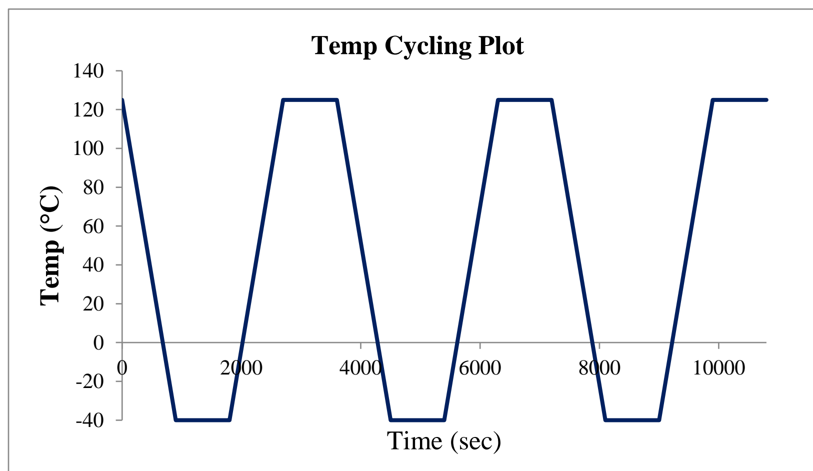

FIGURE 2-16 TEMP CYCLING PLOT

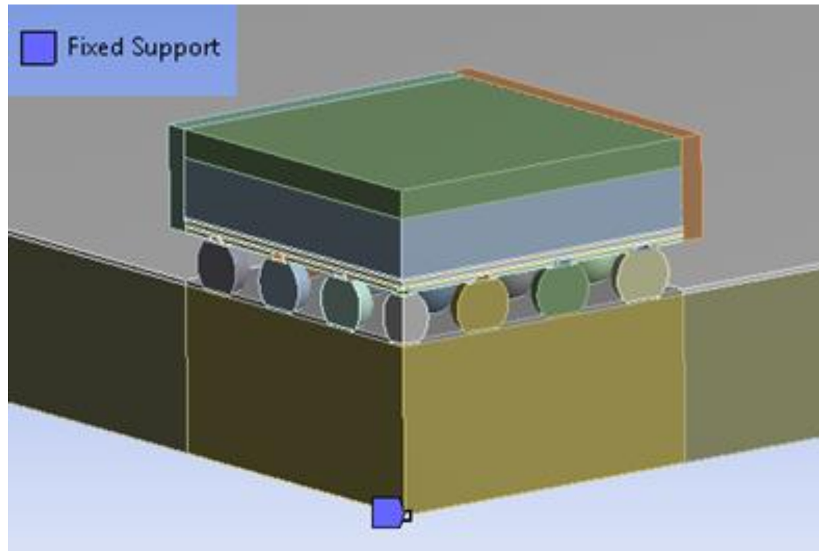

FIGURE 2-17 FIXED SUPPORT

2.5 RESULTS

Total inelastic strain and von-mises stress in the critical (corner) solder ball were used as correlation parameters to predict relate life cycles to failure. The total strain and equivalent von-mises stress in the critical ball as determined by the ANSYS model is shown below in figure 2-18 & 19

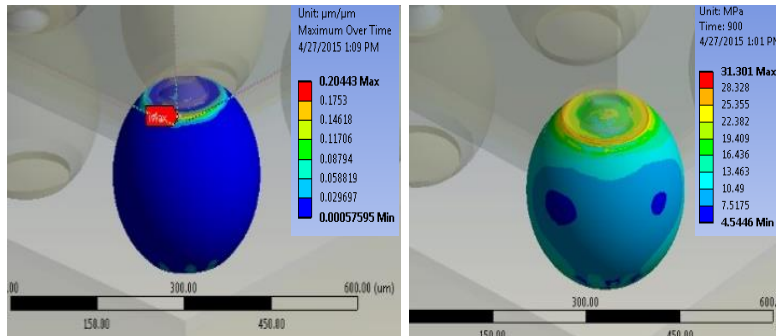

FIGURE 2-18 STRAIN AND STRESS PLOTS OF CRITICAL

SOLDER IN 1MM

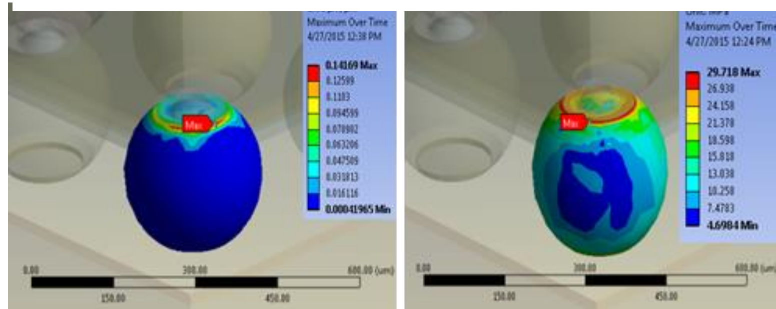

FIGURE 2-19 STRAIN AND STRESS PLOTS OF CRITICAL

SOLDER IN 0.7MM

Volume averaged plastic work was calculated by writing an APDL script in the ANSYS commands using the stress and strain values from the FEA model. The plastic work as for both the boards is given in table 6 below. From these results package with 0.7 board failing earlier as it has maximum plastic work.

TABLE 2-5 PLASTIC WORK COMPARISON OF 0.7MM AND 1MM

Board Thickness (mm)	Plastic Work (MPa)
0.7	0.497
1	0.282

This volume averaged plastic work was related life cycles to failure using Schubert et al. [26] and Che & Pang [27] correlation-

$$N_f=(A/\Delta W)\ \hat{}k$$

Where N_f is the characteristic life. An (in MPa) and k (unitless) are two empirical fatigue parameters that were used from Jie et al. work on chip scale packages [28].

The values of A and k used were

$$A = 8.783 \text{ x } 106 \text{ (MPa)},$$

$$k = 0.4701$$

The calculated life cycles to failure (Nf) as calculated from the above relation are given in table 7 below

TABLE 2-6 CYCLES TO FAILURE OF BOTH BOARDS

Board Thickness (mm)	Cycles to Failure (N_f)
0.7	2552
1	3330

As seen from the results above, the life cycles to failure in a 1mm board are 30% more than 0.7mm. The results from the FEA model are complementing the results obtained by experiments.

2.6 ANALYSIS

As shown from the results, the 0.7mm board is experiencing a higher value of total strain and von-mises stress. This eventually accounts for lower life cycles to failure as compared to the 1mm board. Since these results are in line with the experimental data where 0.7mm board is failing earlier than the 1mm counterpart, it needed some further investigation to find the reason behind this behavior. The reason behind failure could be the material used for solder as well [29].

Based on the results of a cross-sectional study of both the boards, the total volume of Cu and FR4 was determined for both the boards. The purpose of this study was

to determine the Cu content in both the boards, which contributes to the stiffness of the board.

TABLE 2-7 COPPER VOLUME COMPARISON

	0.7mm	**1mm**
Total Cu (μm)	184	162
Vol. of board (mm^3)	24x24x0.7=403.2	24x24x1=576
Cu/Vol. of board ($\mu m/mm^3$)	0.456	0.2815

As shown from the table above there is 38.3% more Cu/mm3 in 0.7mm board as compared to the 1mm board. This also means that 1mm board has 38.3% more FR4/mm3 as compared to the 1mm board. Now, since Cu contributes to the stiffness and FR4 contributes to the compliance of the board, 0.7mm board is much stiffer as compared to the 1mm counterpart.

It is the author's belief that the high volume of Cu in 0.7mm board is playing a significant role in its early failure as it is making the board stiffer and eventually generating more stresses in the critical solder ball. This indicates that reducing Copper layer would improve the reliability of thinner boards. To validate this theory

the author has taken a help of Ansys simulations. Also, the author will consider the effect on electrical performance and failures. Reducing Copper might create a negative impact on electrical reliability.

2.7 STUDY OF REDUCED COPPER VOLUME

In this study, layer removal experiment has been performed. For that, a special fixture is fabricated to hold sample tightly against the force of the CNC milling machine as shown below.

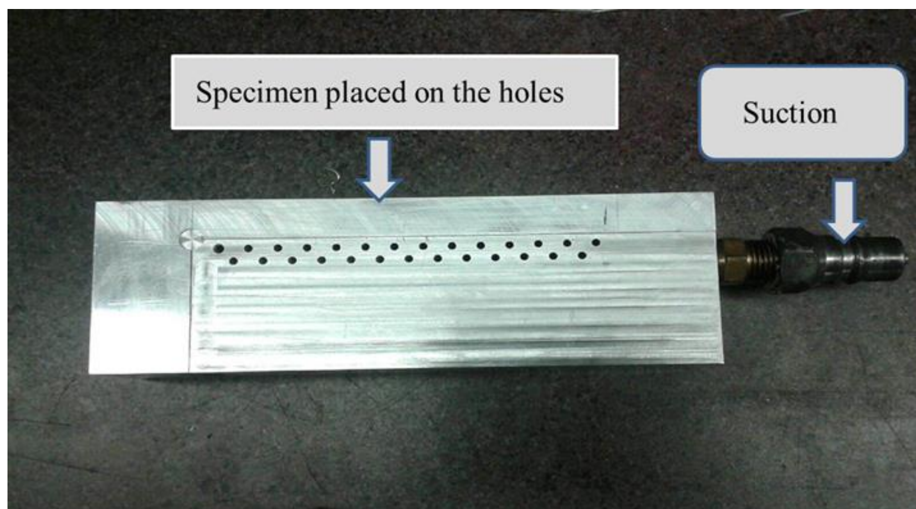

FIGURE 2-20 PNEUMATIC FIXTURE FOR LAYER REMOVAL

The holes in the area are provided to suck sample and hold tightly on the fixture against the force of CNC milling machine. There was some limitation to fixture that, if sample size goes below particular thickness, suction force suck sample inside the fixture. As per the cross-section details of each layer, layer by layers are removed and properties at different composition of PCB are measured. Those properties were imported in ANSYS and simulated for plastic work. This study is helpful in determining the effect of each layer in properties of PCB. The figure below shows the layer removal comparison of plastic work obtained through ANSYS simulation.

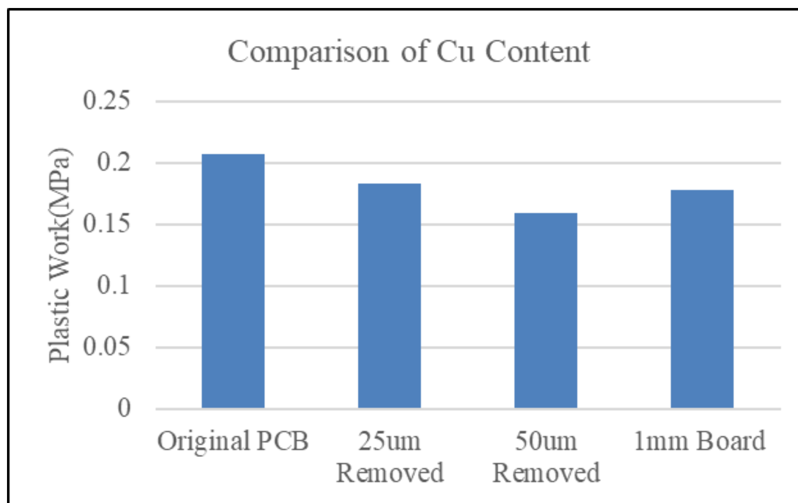

FIGURE 2-21 LAYER REMOVAL YOUNG'S MODULUS COMPARISON

From the above figure, it is very clear that as you go on removing Cu layers from the stack-up, the PCB become softer and flexible which results in better performance of the assembly. Figure 2-22 shows the effect of PCB stiffness on the warpage of assembly. It also shows the stresses developed on corner solders.

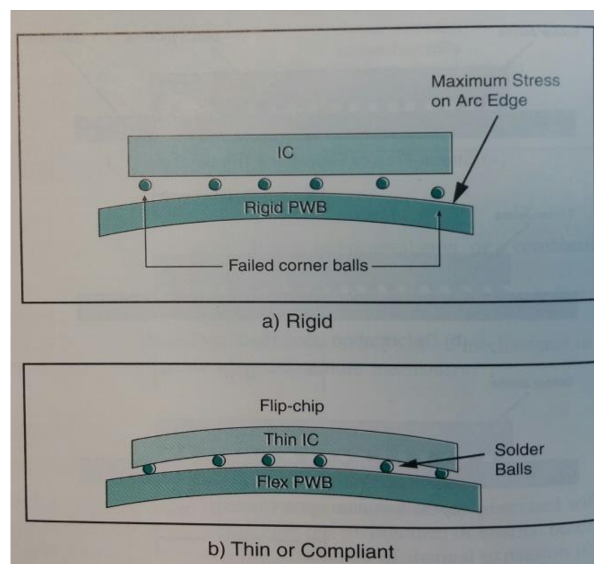

FIGURE 2-22 EFFECT OF PCB STIFFNESS [2]

Using these new properties obtained through layer removal study have shown a significant amount of change in Total strain and Plastic work of corner solder used with 0.7mm board. In the FEA when the amount of copper is removed, the same amount of FR4 is added in the PCB to maintain the thickness of PCB. This is to study the effect of reduced copper content in the same PCB and how copper affects the reliability. Reducing copper is possible if it can be reduced in the planar

direction and not in thickness side. Design optimization for improved reliability should not affect the electrical performance of the system. The figure below shows the results obtained by new properties with reduced copper contains.

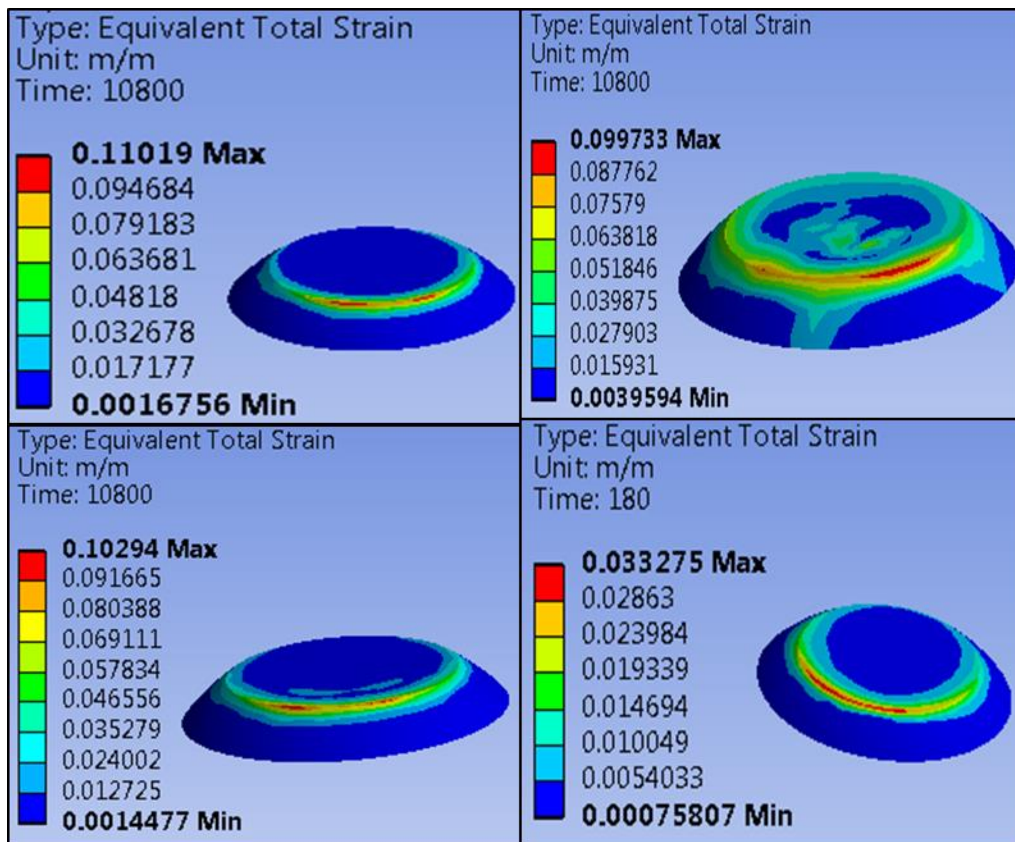

FIGURE 2-23 TOTAL STRAIN OBTAINED WITH ORIGINAL PCB, 25UM REMOVED, 50UM REMOVED, 1MM ORIGINAL PCB CLOCKWISE FROM TOP LEFT

So, copper is playing important role in deciding the life of a WCSP package. But reducing copper content may be challenging. We can reduce copper in the planar

directing but cannot reduce it in Z direction i.e. thickness. So, next study is designed to avoid playing with copper and affect our electrical performance, author has decided to analyze the effect of different parameters on the life of the package.

2.8 EFFECT OF UNDERFILL FOR ONLY CORNER SOLDER

IBM and Hitachi were credited with starting the journey of Flip chip to organic boards, Tsukada of IBM Japan, based on some observations, has discovered that underfilling the gap between Flip chip IC and PCB can tremendously improve reliability. `Underfilling work started in 1985. By 1988 Hitachi reported the use of polymer to underfill for improved reliability. The underfill encapsulates are applied between the chip and substrate to compensate for the coefficient of thermal expansion (CTE) difference between chip and substrate [2]. The CTE of Silicon is ~3ppm/°C and that of the substrate is ~17-21ppm/°C. CTE of ceramic substrates is ~7ppm/°C resulting lower stresses on interconnects, so there is no need of underfill. WCSP is a very cheap and small package with a very small stand of height. So, most of the WCSP's don't use underfill. But in this case to help improve poor life caused by the result of electrical requirement author has decided to use underfill to only corner critical solder. The figure below shows detail about corner underfill geometry.

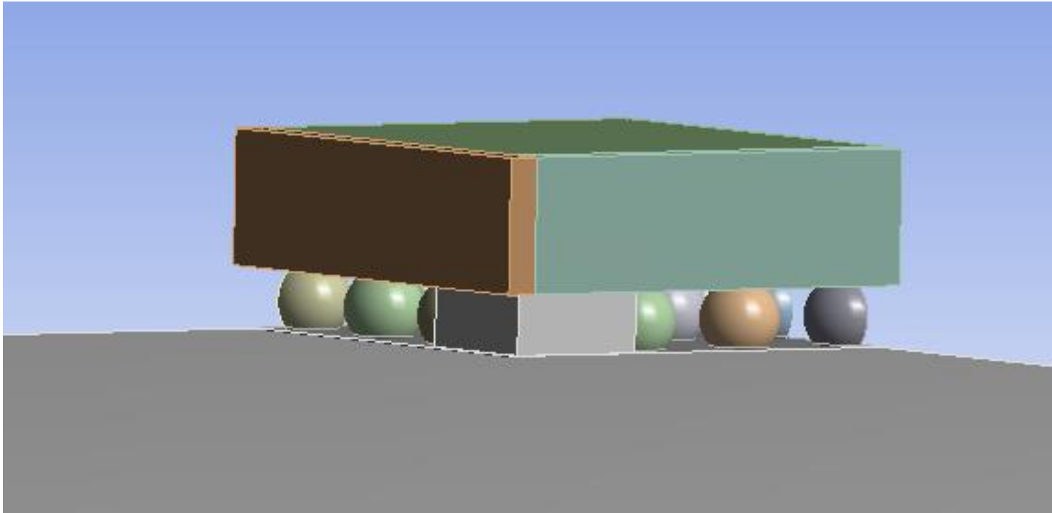

FIGURE 2-24 CORNER SOLDER UNDERFILL LAYOUT

Using corner underfill is to save time and cost of packages as well as it would make repair and reworking of interconnects very easy. The figure below compares the total strain difference between 0.7mm and 1mm board. Effect of underfill is observed with significant change in total strain and PW of critical solder. The use of underfill to only corner solder showed around 50% improved reliability.

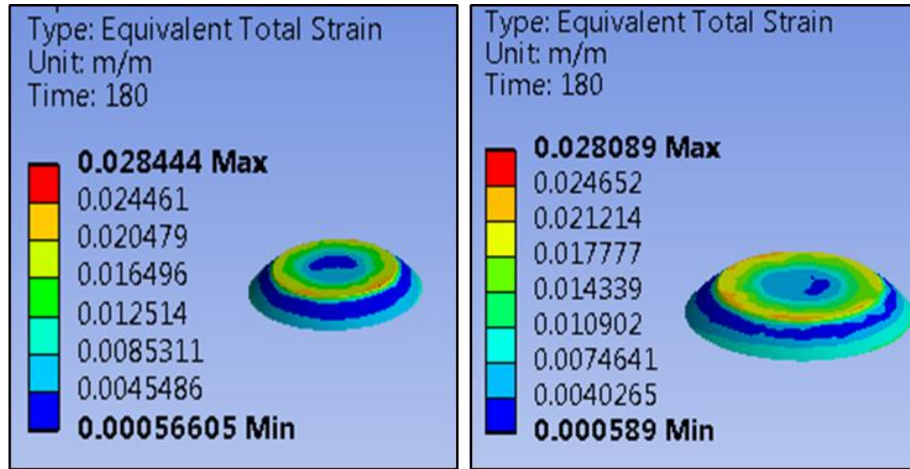

FIGURE 2-25 TOTAL STRAIN IN CORNER SOLDER WITH CORNER UNDERFILL IN 0.7MM AND 1MM BOARD RESPECTIVELY

TABLE 2-8 TOTAL STRAIN AND PW COMPARISON BETWEEN 07MM AND 1MM

Total Strain in 25µm Layer		
Type of Design	0.7mm	1mm
Total Strain	0.02844	0.02808

Plastic Work in 25µm Layer		
Type of Design	0.7mm	1mm
PW(MPa)	0.078	0.0663

.

So, using corner solder underfill improved reliability of both the packages on different boards tremendously, but 0.7mm board reacted to underfill significantly reducing cycles to failure difference between both the boards. Underfill is supposed to protect solder joints and make the product last longer. Previous research indicates that for some applications underfill may result in thermal-cycle failure sooner than if no underfill was used at all [30].

2.9 EFFECT OF CORNER COPPER PILLAR

Fine-pitch copper pillar bump (CPB) for flip chip assembly is expanding in package applications for mobile electronic devices due to the need for smaller form factor, thin thickness, and the demand for better performance and lower power consumption [31]. The C4 bumps gained wide acceptance in IBM devices because the bumps could be applied to a whole wafer by evaporation over a stencil mask. Manufacturing cost, therefore, was already a key factor that C4 prevailed over the more expensive copper ball joints. By the early 1980s, IBM was applying C4 in high-performance server systems with bump pitches about 250 µm. The bump diameters ranged between 100 and 125 µm; bump heights were between 70 and 85 µm [32]. Figure 2-26 show's TI's 40-µm Fine Pitch Copper Pillar Flip Chip Packages. Looking closer figure 2-26, we can see that the plugs are tapered with

some solder flow down the side, and it appears that the copper traces had been pre-coated with the same tin-based solder (likely SnAgCu) [33].

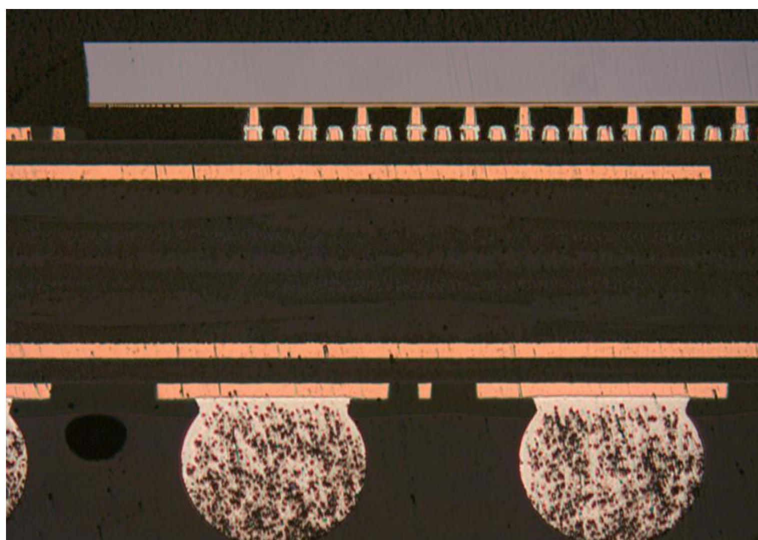

FIGURE 2-26 CROSS-SECTION OF TEXAS INSTRUMENTS XAM3715

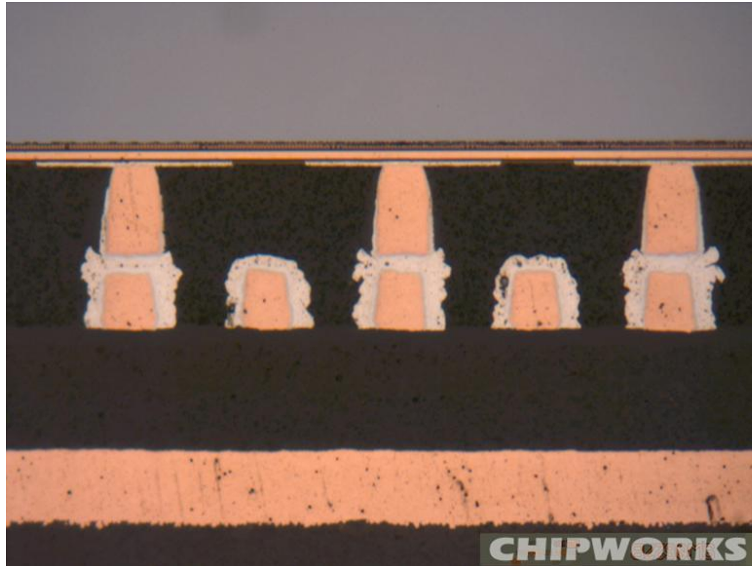

FIGURE 2-27 ZOOMED VIEW OF COPPER PILLARS CROSS-SECTION OF TEXAS INSTRUMENTS XAM3715

The concept of the copper pillar is leveraged from above-mentioned technologies, but the only change was made that, only corner SAC solder is replaced by a copper pillar. Figure 2-27 shows the design of corner copper pillar used in the analysis.

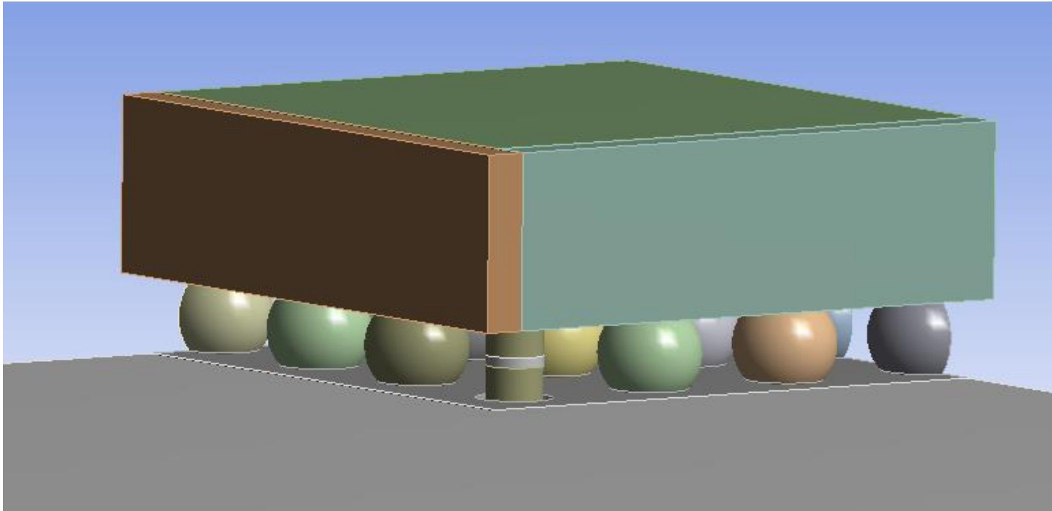

FIGURE 2-28 CORNER COPPER PILLAR DESIGN

Copper pillars were soldered at center with the same solder i.e. SAC 396. Figure 2-28 shows the results obtained by using corner copper pillar. Simultaneously, one more parameter was studied. Increasing the volume of corner solder ball and making it a rectangular block of solder. Previous studies have shown that increasing solder volume has shown improved life. Figure 2-30 shows results obtained by corner solder block. Several parameters must be evaluated before making a careful transition from a lead-based alloy to a lead-free alloy [34] [35] [36]. Any lead-free alloy replacing lead-based alloy should qualify with requirements such as low melting point, adequate wetting characteristics, comparable cost, consistent

manufacturability (at the component level and the board level), wide availability, acceptable reliability, ease of reworkability and reparability etc. [37] [30]. Among these parameters' reliability has probably become the most significant parameter.

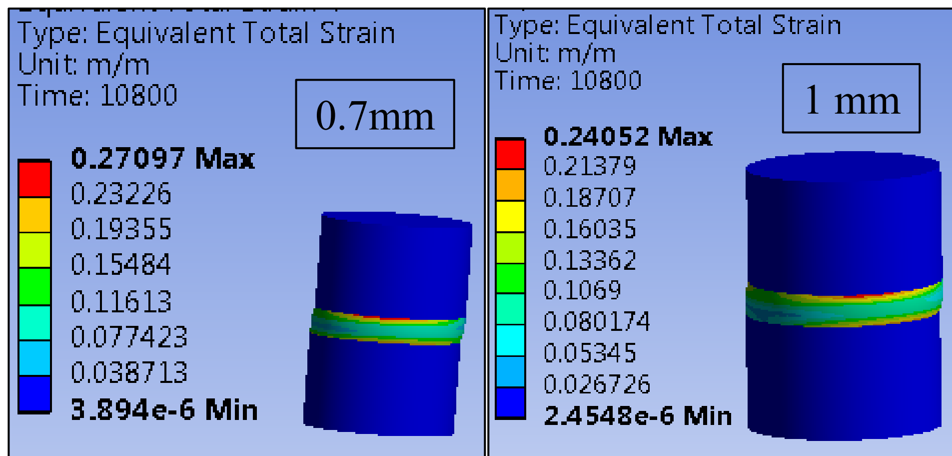

FIGURE 2-29 COMPARISON OF TOTAL STRAIN IN CORNER SOLDER

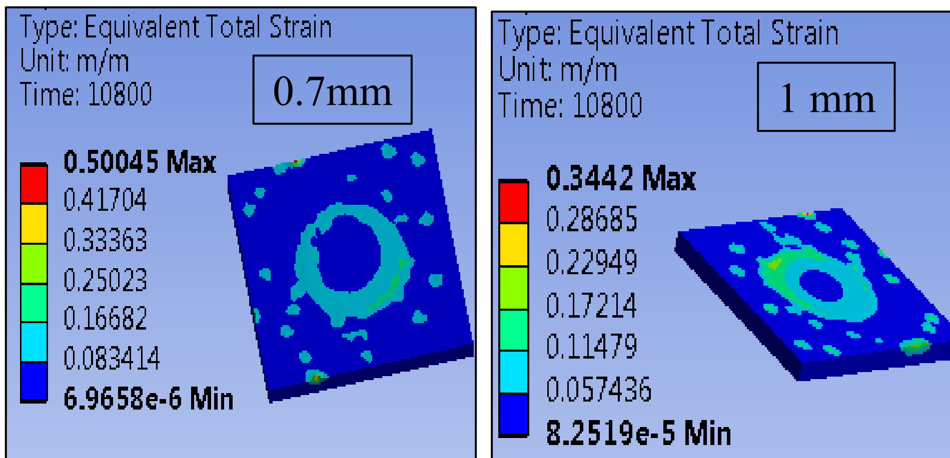

FIGURE 2-30 EFFECT OF CORNER SOLDER BLOCK

Copper Pillar as corner solder block did not work, as it significantly increases the plastic work, hence poor reliability. Both these designs are not suitable for WCSP.

TABLE 2-9 TOTAL STRAIN AND PLASTIC WORK OF COPPER PILLAR AND CORNER BLOCK

Total Strain In 25um		
Type of Design	0.7mm	1mm
Corner Block	0.50	0.342
Corner Cu Pillar	0.271	0.241

Plastic In 25um		
Type of Design	0.7mm	1mm
Corner Block	0.2822	0.215
Corner Cu Pillar	1.4	1.03

Table 2-9 shows the detailed results of corner block and copper pillar study. It can be said that the copper pillar and corner block cannot be used in this assembly as it can reduce the reliability and life of the package. A significant amount of increase in total strain and PW is observed if compared to PW with underfill 0.078MPa which is almost 3X time lower than as of copper pillar.

2.10 CONCLUSION

As shown from the results in the above sections there is 38.3% more Cu/mm^3 in 0.7mm board as compared to the 1mm board. This also means that 1mm board has 38.3% more FR4/mm3 as compared to the 1mm board. Now, since Cu contributes to the stiffness and FR4 contributes to the compliance of the board, 0.7mm board is much stiffer as compared to the 1mm counterpart.

It is the author's belief that the high volume of Cu in 0.7mm board is playing a significant role in its early failure as it is making the board stiffer and eventually generating more stresses in the critical solder ball. This study has also shown the effect of copper by performing layer removal study and analyzing the effect of copper present in PCB, which indicates that reducing Copper layer would improve the reliability of thinner boards. Due to the possibilities of affecting electrical performance and failures the author proposed new design parameters to improve solder reliability without affecting thermal performance. In this study, the effect of corner underfill is successfully studied and showed significant improvement in the cycles to failure. Other parameters like copper pillars and corner solder block models are also studied. But, other designs resulted in poor performance of assembly under thermal cycling.

Chapter 3

FAILURE ANALYSIS AND DESIGN OPTIMIZATION OF QFN

3.1 ABSTRACT

Increasing popularity of hand-held devices and big competition between rival companies invented smaller and faster devices. Miniaturization of electronic devices allowed to fit more electronic component to fit in a smaller area producing the risk of failure due to increasing thermal load or drop impact. It is very important to analyze and ensure the reliability of an electronic device under a different type of loadings. Not only the drop impact but also thermal load, moisture, and convection can affect the reliability of these devices. Most popular devices like cell phones, laptops, tablets are prone to accidental impact loads which will challenge the interconnects reliability and eventually will result in failure. As discussed in the previous chapter, increase in PCB thickness or stiffness results in early failure of packages. The initial part of this work demonstrates the design optimization of the solder joint. Several solder profiles were tested for improved reliability under Accelerated Thermal Cycling (ATC). Solder profile plays a very important role in when considering design optimization for improved reliability. As

solder profile can create favorable conditions for crack growth. After analyzing the best solder profile for an improved life, the assembly is tested for drop impact to analyze the robustness of design under drop impact. In this thesis, an attempt has been made to study a drop/shock impact test on Quad Flat No-lead (QFN) package assembled on two different boards with varying thicknesses. The uniqueness in this study is an analyzing effect of drop/shock impact on the QFN assembly in working condition i.e. at different temperatures- uniform as well as non-uniform temperatures. The Ansys Workbench 19 is leveraged to set up a computation model to provide a power to the chip to create non-uniform temperature distribution during the drop testing analysis. This study will help us understand close to the realistic effect of drop impact on the interconnect's assembly. Several material properties which affect the reliability of devices are Young's modulus, density, CTE, thermal conductivity, specific heat and Poisson's ratio. Thermal mechanical analyzer (TMA), the Dynamic mechanical analyzer (DMA) and Universal testing machine are leveraged to characterize all the temperature dependent properties of two boards to simulate. Finite element analysis (FEA) tool is used to analyze the effect of impact loading on solder joint reliability (SJR) of the package used on two boards with thickness and layer stack-ups as per JEDEC standards [38]. This study will help us understand the effect of thickness and layer stack-up of PCB on the reliability of QFN packages under drop test. The packages are susceptible to solder

joint failures, induced by a combination of PCB bending and mechanical shock during impact [39]. From the past work, the critical peripheral solder joint failure is observed to occur at the corner lead. Failure is initiated along the solder fillet/lead edge, and it propagates through the top solder/lead interface on the component side [40]. The focus of this work is to investigate the impact of drop test with the powered package and, how the reliability of any assembly changes with changing the stiffness of the printed circuit board. This comparative study will give us an insight into the effect of PCB layer stack-ups, thickness, and temperature effect on the reliability of solder interconnects under drop impacts

Keywords: QFN, Solder Joint Reliability, Drop Impact/Test, Temperature-dependent, Drop test simulation, Finite element analysis

3.2 INTRODUCTION

Electronic devices manufacturing industries are in demand of smaller, cheaper and high-performance semiconductor devices. Surface mount technology is the evolution of chip scale technology and the components of the surface mount package are further shrunk. These packages are mounted on the surface of the PCB as shown in figure 3-1 below and hence both the sides of the board are available for package mountings. The packages have more density and thicker pins as compared to through-hole packages.

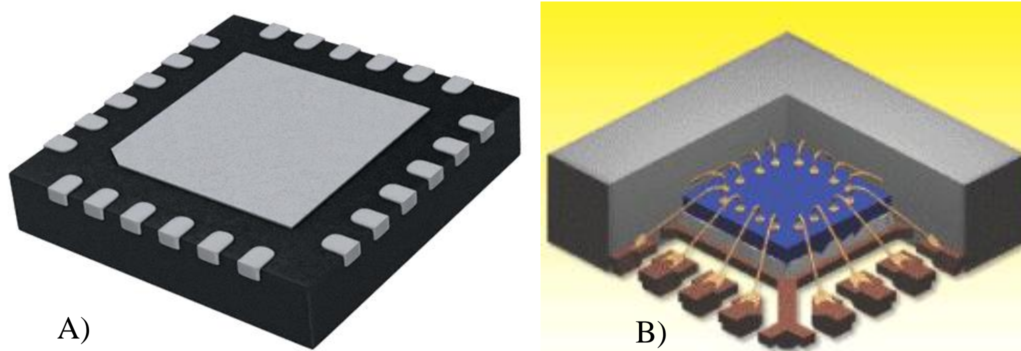

FIGURE 3-1: A) BOTTOM VIEW OF QFN PACKAGE B) INTERNAL VIEW OF WIRE-BONDING DETAILS

But, surface mount technology causes less solderability and repeatability. Components like a capacitor, integrated circuits and resistor are miniaturized for high-speed performance, which is difficult to manufacture or fabricate. During the long-term in working condition, these packages show failures from time to time and reliability becomes the major concern. One of the surface mount packages, QFN package has better thermal performance than the other surface mount technology package due to provided thermal pad. QFN which is also known as Micro Lead Frame (MLF) and small outline No-Leads (SON), uses SMT. It doesn't have through-hole connections to the PCB, but the exposed lands at the bottom of the package along the perimeter are soldered. Low inductance, capacitance, small package volume, smaller board routing area and no external leads are other benefits

of QFN packages. Thermally enhanced QFN is designed to eliminate the use of bulky heat sinks and slugs. This package can be easily mounted using standard PCB assembly techniques and can be removed and replaced using standard repair procedures. QFN package gained popularity in the industry due to it's excellent thermal and electrical characteristics [39] [41].

Multifunctional integrated electronic devices and new wearable modern electronics gadgets can subject to accidental drop impact during the day to day use. These handheld electronic devices are operated by the busy corporate worker, college students and even kids which create a high possibility of impact loading on it. The accidental drop damages the outer body of the devices and connected internal components. The shock wave gets transmitted through the support to PCB and other components like the packages, the capacitors, and the ICs. The board-level drop test has become an essential reliability evaluation methodology in recent years in developing mobile devices that involve electronic packages with lead-free solder joints [42]. Board level drop test is easier than product level drop test, the product design and other parameters play a vital role in deciding its reliability. At the board-level drop testing, the factor which is important is PCB properties, thickness, and its composition. From the previous research studies, it has been seen that the thinner board can also be more rigid compared to the thicker board due to its composition

[12]. When a package undergoes a sudden drop, the solder joints are subjected to maximum equivalent stress due to impact. According to the past studies, the location for the initiation of failure in the form of cracks, on the solder fillet or in the base of the joint [43].

Tee et al. [39] in his study performed drop test at room temperature and concluded that packages are susceptible to solder joint failures, induced by a combination of PCB bending and mechanical shock during impact. The critical peripheral solder joint is observed to occur at the corner lead. Failure is initiated along the solder fillet/lead edge, and it propagates through the top solder/lead

interface on the component side. Guruprasad et al. [44] investigated that in BGA package the failure modes observed for SAC305 were IMC fracture at the component side pad, which is the same as seen in the micro-impact fatigue tests. The failure mode for the SAC105 was either pad cratering or bulk solder fatigue

Song et al. [45] study were helpful to understand that the crack in the solder joint may close after the impact, resulting in an undetectable failure unless there is a high-speed real-time data acquisition system available for in-situ monitoring. Meng et al. [46] proposed that finite element analysis (FEA)-based methods can significantly improve the prediction capability and efficiency because they use the local dynamic response at the failure site to assess the damage severity. Douglas et. al. [47] the standards put in place by JEDEC for drop testing may seriously

underestimate the actual conditions in a drop event, especially when there are risks of secondary impacts between the internal structures in the test specimen. Clearances between the PWB and the fixture can be tailored to create very high or low acceleration amplifications by exploiting secondary impact between the test specimen and the fixture. The failure modes in the finite-clearance configuration were predominantly fatal cracks in the interfacial IMC layer near the PWB. In a few of these tests, partial or full pad peel out was another observed failure mechanism. The clearance, which produces an optimal impact, is clearly proportional to the drop height (impact amplitude). Kang et. al [48]. The solder ball interfacial failure is induced by a combination of mechanical shock and PCB bending. The bending stress is critical to solder joint reliability

In this study, depending upon the past work, I have modified the standard drop testing method by the providing power to all packages on PCB during drop testing. The idea behind this method is to analyze the drop impact during real time. When we are considering the accidental impact of handheld devices during daily work, the i.e device is in working condition. That means it's generating some internal heat which produces the non-uniform temperature distribution on the system. This non-uniform temperature distribution or temperature gradient produces a high junction temperature. This thermal load can cause solder joint failure, or it might play a

significant role in the impact or drop testing. Many researchers have shown that coupling power cycle with ATC shows a significant change in results and which is said to be more realistic [41].

3.3 MATERIAL CHARACTERIZATION

As discussed in the previous chapter, it's important to know the details of PCB stack up. Depending on the cross-section measurement, we could be able to to calculate the copper content of the PCB. More percentage of copper will result in more deformation and can show significant impact on results [12]. The epoxy mold is created for a PCB board sample to observe its cross section under an optical microscope. It has been observed that the percentage of copper in the 93mil board is 40% and the 134mil board has 43.7% of the total PCB stack-up. The percentage of copper in two QFN PCB boards increases with increase in thickness of the board which will result in more flexural stiffness. The detailed layer stack up of both the boards are shown in Figure 3-2. 93mils thick board has 10 copper layers and the 134mils board has 16 copper layers. Depending upon the thickness of the copper layer, the percentage of copper changes. Rigidity increases with an increase in the percentage of copper in PCB. [47]

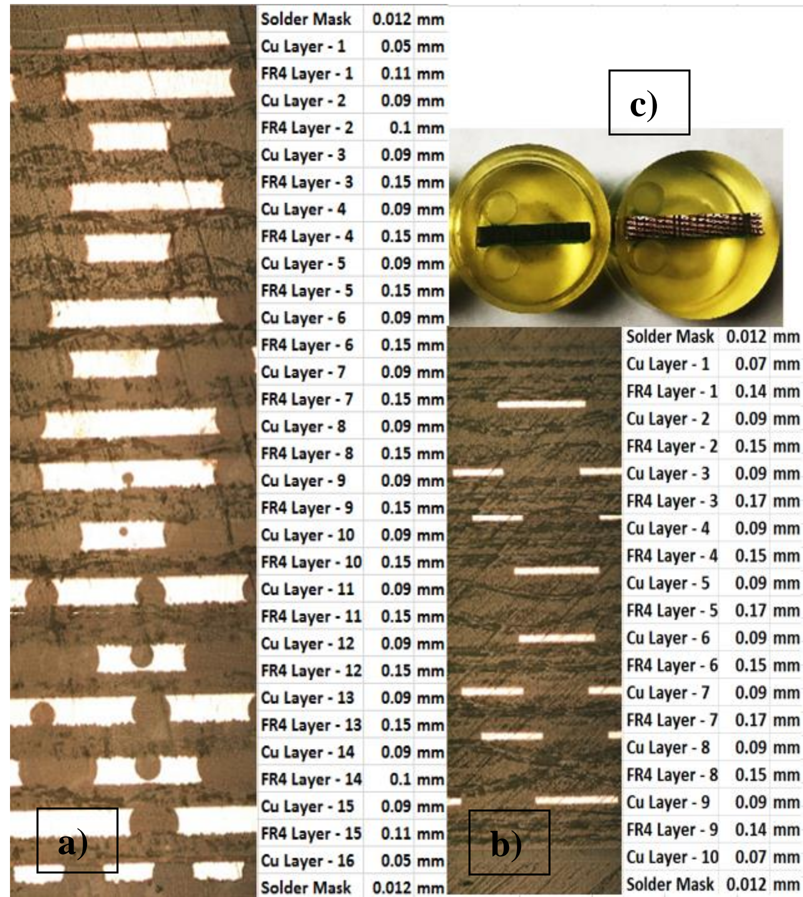

FIGURE 3-2: A) STACK UP DETAIL OF 134MIL BOARD. B) STACK UP DETAILS OF 93 MILS BOARD. C) EPOXY MOLD COMPONENT USED FOR CROSS SECTIONING

Material characterization has a critical importance in an FE Analysis of boards. For lumped PCB approach, it is necessary to predict the precise material properties for

boards. Specifically, in this study, we are going to measure Coefficient of Thermal Expansion (CTE), Modulus of Elasticity (E) and Poisons Ratio of the boards using a lumped approach. Various test setups have been used to measure material properties. Being highly non-uniform structure of PCB, minimum 5 tests with the samples from different location of PCB were used for the experiments.

3.3.1 Thermo-Mechanical Analyzer (TMA)

TMA is a device with a thermal chamber which has a good working range of temperature from -150°C to 450°C. TMA is used to measure in-plane and out-plane CTE of the different boards. For this experiment sample is prepared using the high-speed cutter, the sample is typically cut into 8×8 mm^2 of a square shape. The sample is cut in such a dimension that; it will seat below the probe inside the thermal chamber. The probe of the TMA is of quartz, which seats on the sample and relative movement of probe gives us the plot for CTE. CTE is measured for a temperature range of -40°C to 260°C, with a ramp rate of 3°C/min to achieve a uniform temperature throughout the sample during measurements.

FIGURE 3-3: (A) THERMAL MECHANICAL ANALYZER (TMA). (B) DYNAMIC MECHANICAL ANALYZER (DMA)

3.3.2 Dynamic Mechanical Analyzer

Dynamic Mechanical Analyzer measures the mechanical properties of materials as a function of time, temperature, and frequency. The term is also used to refer to the analyzer that performs the test. DMA is also called DMTA for Dynamic Mechanical Thermal Analyzer. DMA works by applying a sinusoidal deformation to a sample of known geometry. The amount of deformation is related to its

stiffness. 10mm*50mm sample size has been taken to measure Elastic modulus from a temperature range from 15°C to 260°C.

TABLE 3-1: MATERIAL PROPERTIES

Material	CTE (ppm/°C)	E (GPa)
Die	2-3	125-135
Die Attach	60-70	8-14
Lead Frame	15-20	125-135
Epoxy Mold	8-13	1-5
Epoxy die pad	15-20	125-130
93mil PCB	$\alpha_{x, y}$=16.3, α_z =37.8	13.7
134mil PCB	$\alpha_{x, y}$=17.5, α_z=32.8	16.1

3.4 COMPUTATIONAL ANALYSIS

The Finite Element Methods are said to be under the computational branch. FEA is used for applications like Aerospace, automotive, nuclear, mechanical, civil. By taking a system it's always hard to analyze it and solve its complexity. Ansys Workbench 19 is leveraged to model quarter geometry of QFN used for the computational purpose. Package component details are as shown in figure 3-4.

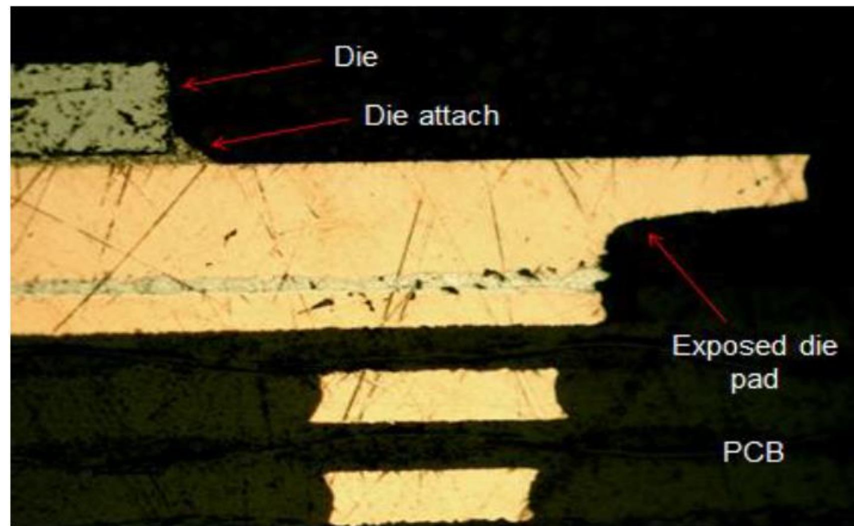

FIGURE 3-4: QFN PACKAGE COMPONENTS

Quarter geometry is considered for the simulation to reduce computational time. Symmetric boundary conditions are applied on the 2 faces towards the inside where the geometry is split. Using quarter geometry does not affect the accuracy of the

result. All the properties except the solder are modeled as linear elastic, [1] [49]. The solder is considered as viscoplastic and so Anand's model was used to explain the behavior of the solder joints. SAC305 is an alloy made of 96.5% tin, 3% silver and 0.5% copper. It is used as the material for solder. Anand's viscoplastic constitutive law is used to describe the inelastic part of the lead-free solder. The Anand's constants are given in Table 2 below. It takes both creep and plastic deformation into consideration to represent secondary creep of the solder. Anand's viscoplastic constitutive law best describes the inelastic behavior of lead-free solder [50]. Anand's law consists of nine material constants A, Q, ξ, m, n, hu, a, so, ŝ.

$$\frac{d\varepsilon_p}{dt} = A\sinh\left(\xi\frac{\sigma}{s}\right)^{\frac{1}{m}}\exp\left(-\frac{Q}{kT}\right)$$

$$\dot{s} = [h_0(|B|)^{\alpha}\frac{B}{|B|}]\frac{d\varepsilon_p}{dt}$$

$$B = 1 - \frac{s}{s^*}$$

$$s' = \hat{s}\left[\frac{1}{A}\frac{d\varepsilon_p}{dt}\exp\left(-\frac{Q}{kT}\right)\right]^n$$

TABLE 3-2: ANAND'S MATERIAL CONSTANTS FOR SAC 305

Consta	Name	Unit	Value
s_0	Initial Deformation Resistance	MPa	2.15
Q/R	Activation Energy/ Universal Gas Constant	1/K	9970
A	Pre-exponential Factor	sec^{-1}	17.994
ξ	Multiplier of Stress	Dimensionless	0.35
m	Strain Rate Sensitivity of Stress	Dimensionless	0.153
h_0	Hardening/Softening Constant	MPa	1525.98
$\hat{s}$	Coefficient of Deformation Resistance Saturation	MPa	2.536
n	Strain Rate Sensitivity of Saturation	Dimensionless	0.028
a	Strain Rate of Sensitivity of Hardening or Softening	Dimensionless	1.69

3.5 SOLDER PROFILE DESIGN OPTIMIZATION UNDER THERMAL CYCLING

Several solder profiles were designed to test the QFN assembly for improved cycles to failure. Three types of designs were selected as shown in the figure below. 1) Adding extra material to solder by changing fillet angle, 2) Keeping the amount of material same but changing fillet angles and 3) Using concave or convex design for

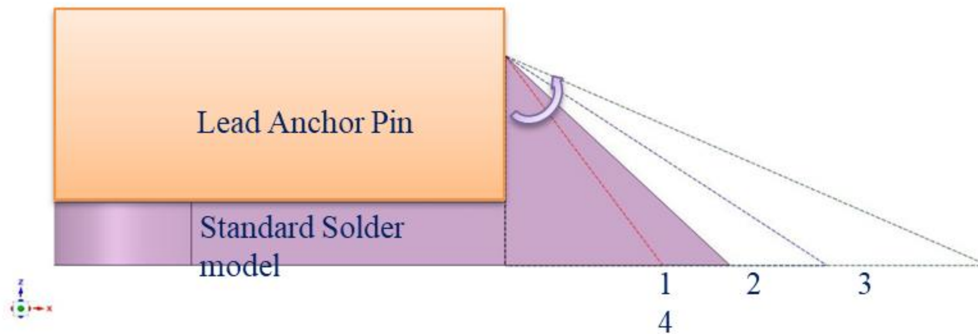

FIGURE 3-5 SOLDER PROFILE WITH DIFFERENT ANGLES

fillet. In the first case, the solder angle formed between lead anchor pin side and the

solder slope is varied, and the solder height is maintained constant as shown in figure 3-5. The solder height is selected to be the same as the standard model and the solder height is maintained at 0.2mm. The design constraints being that the maximum solder height is equal to the lead solder pin and the height being kept same as the one in the standard model to compare the results.

TABLE 3-3 SOLDER PROFILE FILLET ANGLES

Design	Solder Angle
1	35
2	45
3	55
4	65

The angles considered are an an interval of 10 degrees. The standard model has an angle of 45. So, the angles considered are 35, 45, 55, 65. As the solder angle increases, the solder volume also increases with the increased area of the triangle formed by lead solder anchor pin, the solder mask, and the solder slope.

In the second case, the design constraint considered was to check for a constant volume of SAC. The Tin-Silver-Copper is widely used solder material. The solder height in the model of the model was 0.2 mm. The width was also around 0.2mm for the standard model. The solder forms a triangle between the lead solder anchor edge and the solder mask side. The triangle formed by the sides is of an area half * 0.2 * 0.2 will become 0.02 sq.mm. The edge of the solder is 0.23 mm. The total

solder volume becomes 0.0046 cu.mm. The design was made in a manner that the solder volume remains constant for the study as shown in figure 3-6.

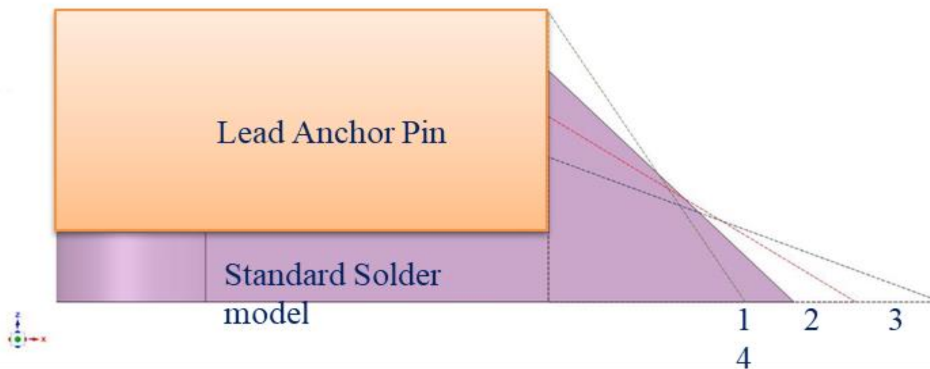

FIGURE 3-6 ADDING EXTRA SOLDER MATERIAL FILLET PROFILE

The possible dimensions for achieving the results are listed in Table 3-4. By the combination of increasing height to 0.25mm and reducing the base width to 0.16mm this constant volume is achieved. By these new dimensions, we get the triangle area same as the original at 0.02 mm^2. The assembly with these new solder profiles are tested under thermal cycling load and predicted cycles to failure.

TABLE 3-4 SOLDER PROFILE DETAILS

Model	Height (mm)	Width (mm)	Area (sq.mm)
1	0.25	0.16	0.04
2	0.2	0.2	0.04
3	0.16	0.25	0.04
4	0.125	0.32	0.04

For the third study, geometric variations are made on the profile of the solder. The solder height and solder base width are maintained the same as the standard model. Bulbous and shrunk profiles are created on the solder profile, with a radius of curvature varying from negative to positive values to study the effect of increasing solder mass of SAC on the solder joint reliability [51] [52]. Of the 4 models created for this study, first one is a shrunk profile with the curvature of negative 25-micron arc. The second model is the original standard model being used throughout the work to form the basis of the comparative study. The third model is a bulbous profile with a radius of the arc as the first model but in positive direction hence 25 microns. The fourth model, the arc is equal to the height of the lead anchor pin and

is equal to the height of lead solder at lead anchor pin side, of 20 micrometers as shown in figure 3-7 below. All these profiles were modeled and simulated in ANSYS 19. Thermal cycle was selected from -40℃ to 125℃.

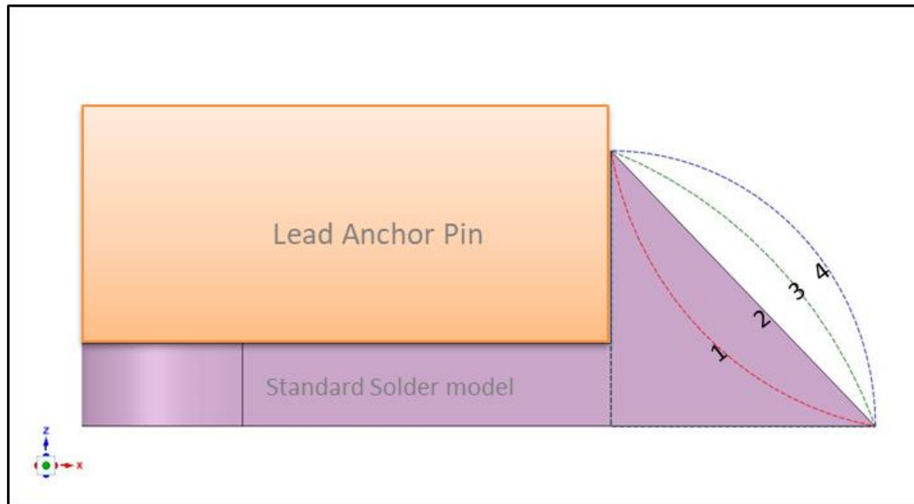

FIGURE 3-7 SOLDER FILLET WITH CONCAVE OR CONVEX PROFILE

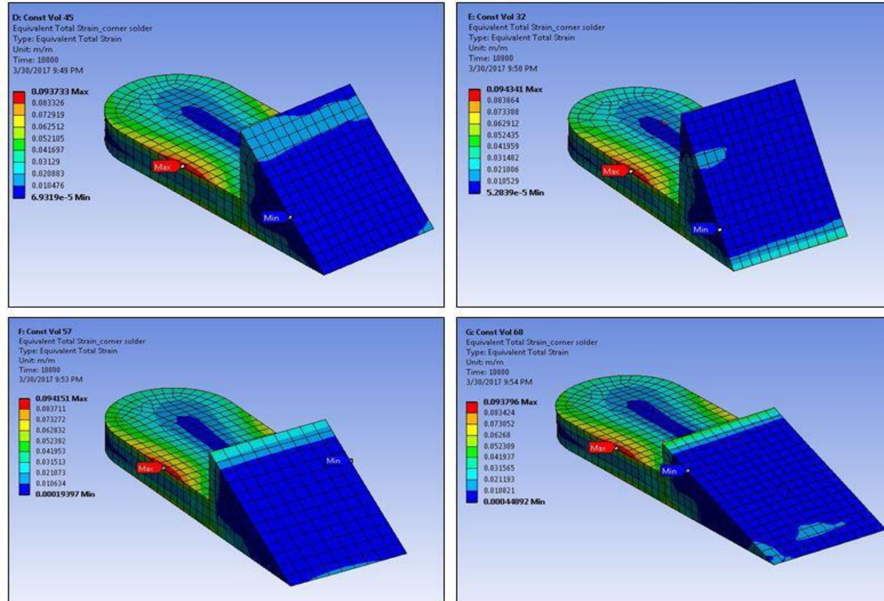

FIGURE 3-8 RESULTS OF DIFFERENT SOLDER PROFILES

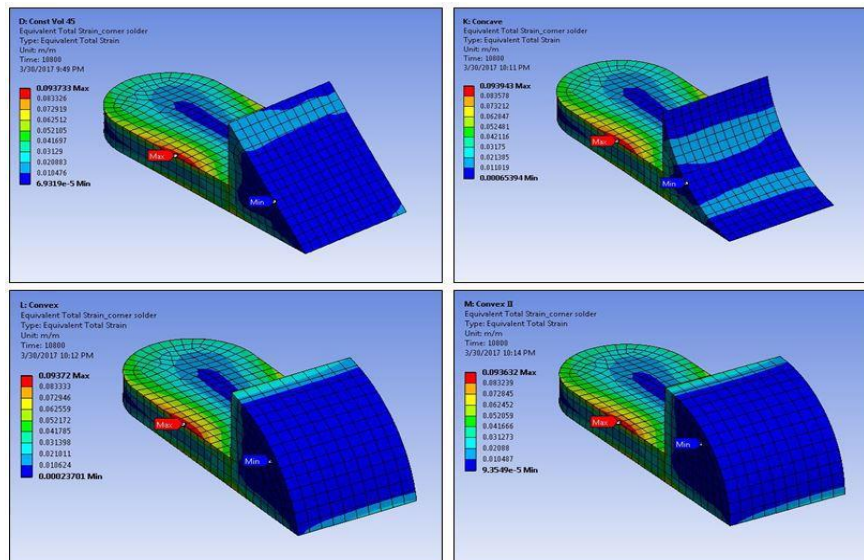

FIGURE 3-9 RESULTS OF DIFFERENT SOLDER PROFILE WITH

CONCAVE AND CONVEX PROFILES

By comparing all the obtained plastic work curves, it was seen that the plastic work is minimum when the solder angle is maintained around 45 degrees. When the solder on the lead anchor pin side and the base is maintained to be of the same dimension we see the least amount of plastic work. When the amount of solder is more on the lead anchor pin side than the base width the plastic work is seen to be the same at 7.35E+05 and 7.36E+05. It can be established that maintaining the solder angle at 45 degrees gives up minimum plastic work thereby, maximum life. The model from Texas instruments holds true and maintains the solder angle to near optimum and reduces the plastic work to the minimum possible.

The design constraint considered to increase the angle along the solder mask was maintained to a maximum of 65 degrees as the purpose of SAC is to solder the lead anchor pin onto the board and having more solder material does not serve the purpose of soldering the board. But, acts as redundant material on the board. Therefore, the angles were compared, and we see a very significant dip in the plastic work from 8.11 to 5.67 (e+05). It can be established that when the solder volume goes on increasing the plastic work reduces to the point of design constraint.

The data table with plastic work was generated for all the models. A significant reduction in plastic work is observed as the solder mass keeps on increasing from shrunk to bulbous profile. The reduction in plastic work continues up until the

solder profile’s curvature is become same as the height on the lead solder anchor side. Then, an upward trend in the curve is observed, it can be inferred that the reduction in plastic work due to added solder mass only continues up to a certain value and beyond it, the SAC material has no effect on the plastic work generated by the solder joint.

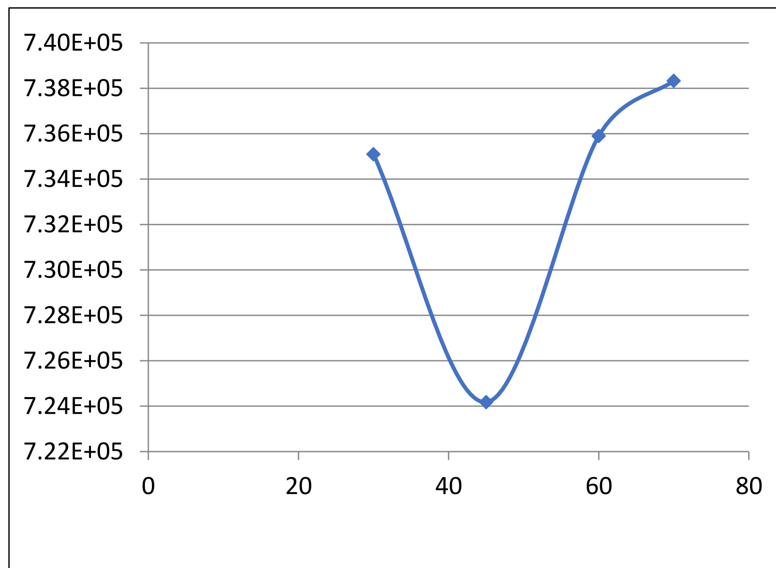

FIGURE 3-10 SOLDER ANGLE VS PLASTIC WORK

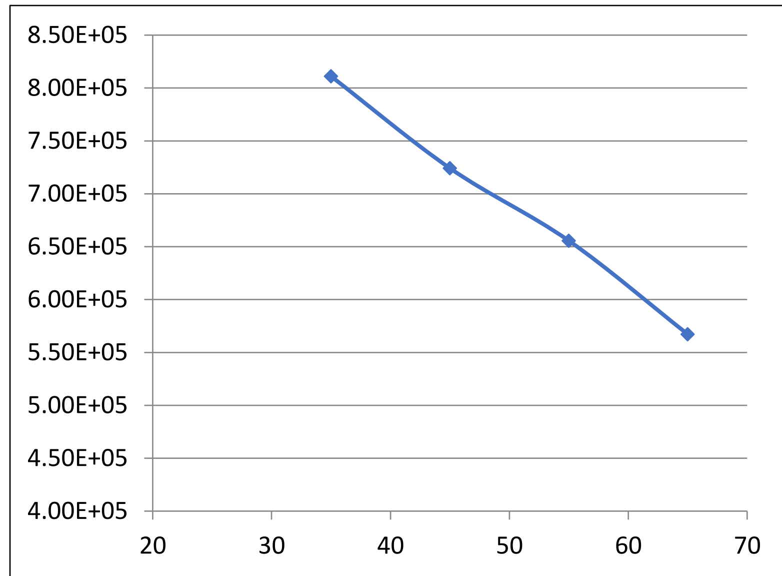

FIGURE 3-11 SOLDER ANGLE VS PLASTIC WORK

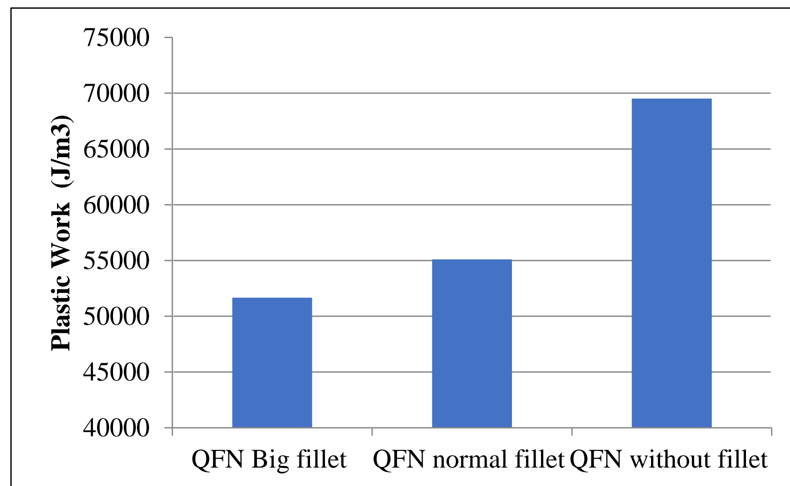

FIGURE 3-12PLASTIC WORK COMPARISON OF BIG, NORMAL AND NO FILLET

Finite element simulations and actual test data generated by the customer have shown that the fillets - if formed – can improve the board level reliability by as much as 2X for a package with a large die to package size ratio. The fillet extends the length of the solder joint and provides a longer path for the crack to go through the entire joint, thus improving the reliability [53].

3.6 FUNDAMENTAL & EXPERIMENTAL SETUP OF DROP TEST

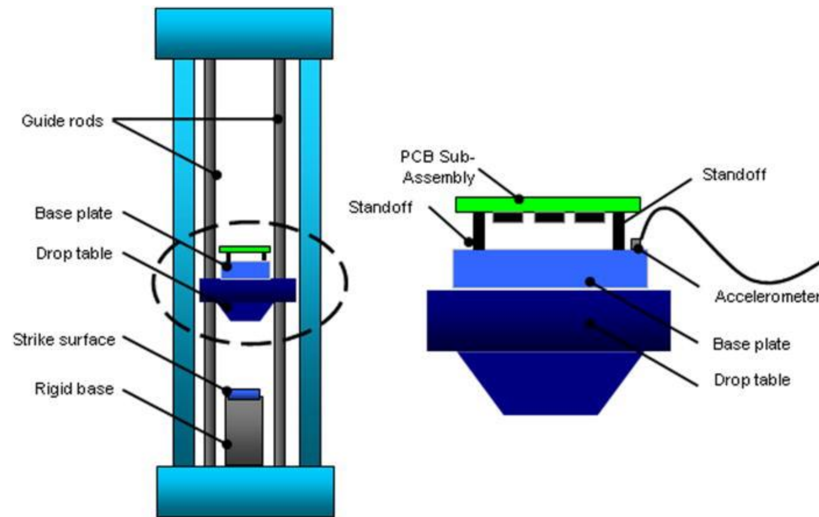

FIGURE 3-13: EXPERIMENTAL SETUP FOR THE DROP TEST [54]

The experimental setup of the drop test suggested by JEDEC is shown in Figure 3-13. The board is fixed to the base plate attached to the drop table with the help of four standoffs or screws. The drop table strikes the rigid base by gliding down the glide rods. The striking surface is covered by the layer of felt to maintain the contact constraints. The drop impact process includes multiple energy transformations as drop table falls freely from a height. The potential energy converts into kinetic energy and after striking at the end, impact pulse generated for the very short duration. In the experimental setup, this prescribed acceleration pulse can be

achieved by manipulating the fall height [43]. The impacting force is transmitted through the mounting screws to the PCB. The force applied to PCB assembly experience flexural movement which ultimately causes failure in solder joints. During the bending movement, the mismatch between elastic modulus of PCB and package creates tension and compression load. The failure in the solder joint could be a tensile rupture and a typical QFN solder joint rupture image is shown in Figure 3-14.

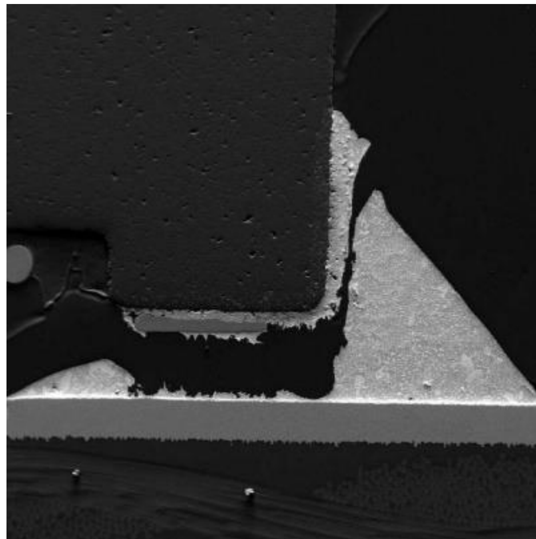

FIGURE 3-14: SOLDER JOINT FAILURE TENSILE RUPTURE (FRACTURE) [55]

As in this study, the internal heat generated thermal load is also considered therefore mismatch in CTE of PCB and package also becomes coupled failure factor with a drop test.

FEM tool is helpful in performing computational analysis, reducing the experimental time and expensive experimental setup. Simulation has done previously for performing a drop test which required exact material setups such as felt material, drop table material and all other component involved in the experiment. An alternative method was invented by tee et al. [56] which is a computational method involving term “Input G” method and which evolve with the advancement of the modeling and simulation methodology and software. Only the package and its components modeling are involved in this method which makes it computationally easy. Later an alternative of the Input G [43] method was described by Lianxi [57] as a ‘Direct Acceleration Input’ (DAI) method. For this study, DAI method is chosen for the simulation. This method applies the acceleration impulse as a body force to the assembly structure. The mathematical formulation for this method is:

$$\{M\}[\ddot{x}] + \{c\}[\dot{x}] + \{K\}[x] = -\{M\}1500\ g \sin(\Pi t/t_w) \quad \ldots.\ (4)$$

$$\text{where } t < tw, \quad t_w = 0.5\text{ms} \quad \ldots\ldots\ldots.\ (5)$$

$$= 0 \text{ where } t > t_w$$

The initial condition is:

$$[x]|_{t=0} = 0; \; [\dot{x}]|_{t=0} = \sqrt{2gh} \; \ldots\ldots\ldots\ldots \; \ldots\ldots \; (6)$$

And the boundary condition is

$$[x]|_{hole} = 0 \; \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \; (7)$$

Where {M}, {C}, {K} is the mass, damping coefficient, stiffness coefficient matrix respectively and $[\ddot{x}]$, $[\dot{x}]$, $[x]$ is the acceleration, velocity and displacement.

3.6.1 JEDEC Global Model

The dimension of the PCB we are considering is $132\times77\times2.4/3.4$ mm^3 boards with 121 solder joints i.e. 11*11 array on each package. JEDEC has a standard design of the board that must be followed for performing FEM drop test with the correct setup. 15 packages were mounted on the PCB and the layout of placing packages are shown in Figure 3-15.

FIGURE 3-15: JEDEC BOARD DESIGN LAYOUT [38]

The natural frequency of the two PCB and mode shapes are obtained from the modal analysis. It is very important for analyzing the natural frequency of any solid, liquid or gas. Like solid, the fluids also have natural frequency and can change its frequency when it experiences any force. The natural frequency of the PCB assembly increases with a decrease in temperature. There is indeed an effect of the temperature on Young's modulus of the materials used in assembly and especially the glass-epoxy-resin composite constitutive of the board. Young modulus of FR-4 tends to increase with the decrease in temperature which leads to more failure of the test assembly at low temperature. As we can observe from the Figure 3-16 that

the frequency increases from mode1 to mode 6. The 93mil board shows less frequency value compared to 134mil board. [58]

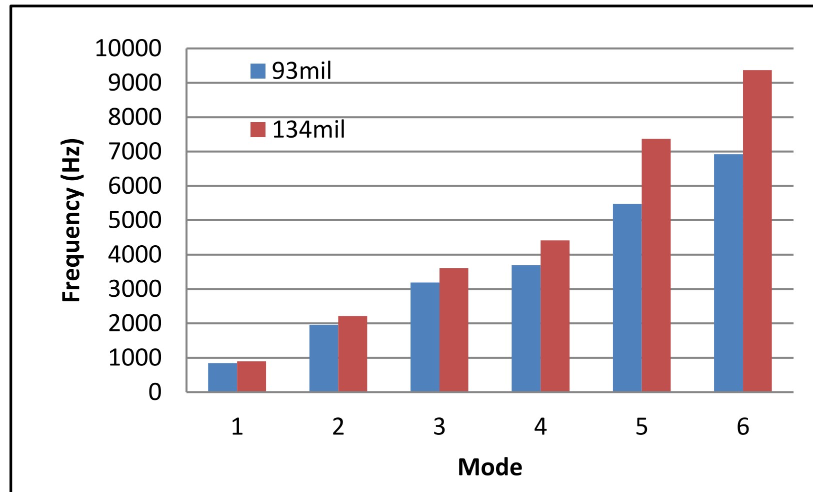

FIGURE 3-16: PCB'S NATURAL FREQUENCY AT DIFFERENT MODE

The magnitude of the 1500g accelerated pulse is applied to the system which is followed by JEDEC standard JESD22-B111. The small handheld devices are designed to withstand drops from a height of 1.5m. The acceleration pulse gives the exact value of the peak acceleration corresponding to the 1.5m height of the drop. The acceleration pulse used as input in this study has a peak value of 1500 g and duration of 0.5 milliseconds as shown in figure 3-17.

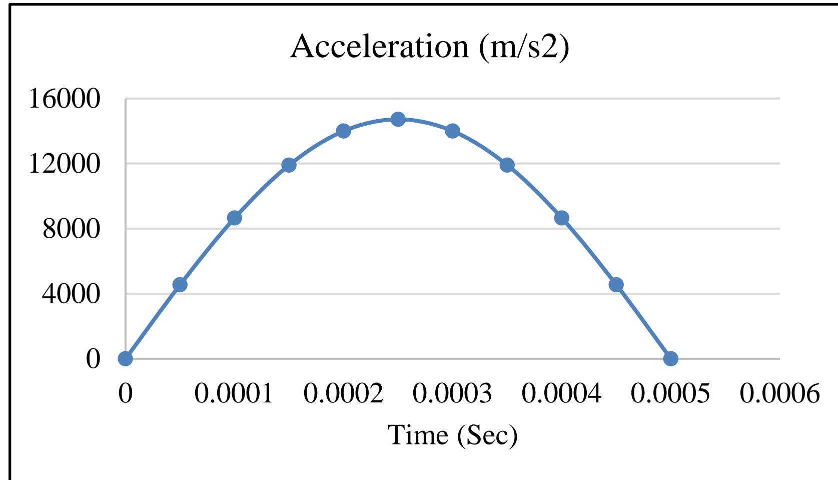

FIGURE 3-17: ACCELERATION PULSE INPUT

3.7 METHODOLOGY & RESULT

Steady-state thermal analysis has been done for obtaining the temperature distribution on PCB assembly during working condition. For efficient simulation, we have considered the quarter symmetric model of PCB assembly and Internal heat generation of power density 0.5W/mm^3 is applied to die of each package. The power density value depends on the package power and it can vary depending upon the application. The convective heat transfer coefficient considered for this analysis is 23W/m^2.°C. This value is chosen in such a way that it tries to match the computational analysis to experimental results. The convection is applied to the outer surface of the package and PCB board.

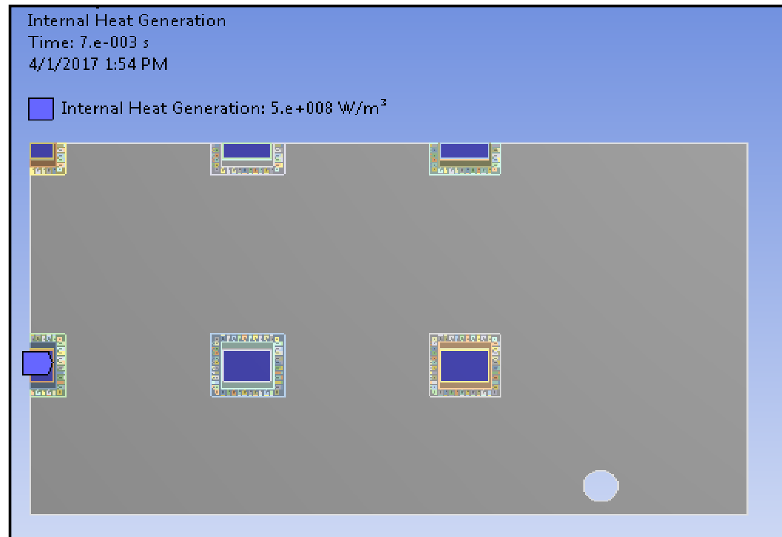

FIGURE 3-18: INTERNAL HEAT GENERATION

The global model of PCB assembly includes a detailed model of each package with all pins and other components. With all that components, meshing becomes a crucial part for performing the efficient and accurate simulation. The computational abilities for the analysis include ANSYS Workbench 19.0 on the server computer with 128GB RAM, 1TB hard drive and Xenon processor. Considering our computational abilities, the optimized meshing is done for a global model with 40k mesh elements. The mesh sensitive analysis is done for obtaining mesh independent model. Figure 3-19 shows a meshed quarter symmetric model. It has a total of 150 solder pins, therefore it’s important to assign correct mesh size to all pins.

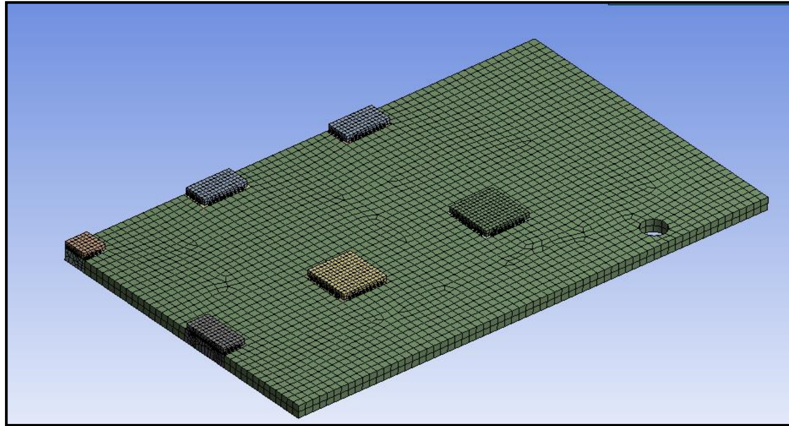

FIGURE 3-19: QUARTER SYMMETRY MESHED MODEL

Figure 3-20 is a contour plot of the temperature distribution of the global model with four screw holes from the steady-state thermal analysis. The obtained junction temperature of the package placed at the center is 66.34ºC. The center package is surrounded by other packages which are also generating power, therefore the junction temperature of the center package is higher than the other.

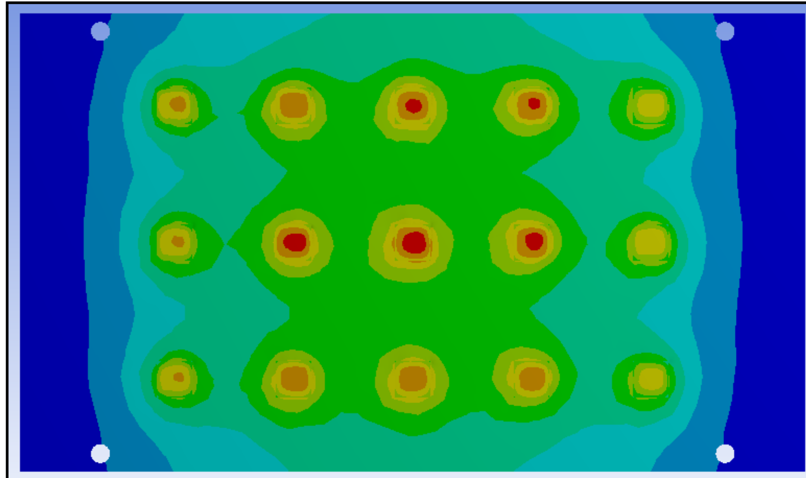

FIGURE 3-20: TEMPERATURE DISTRIBUTION ON GLOBAL MODEL

The temperature load from the steady-state thermal analysis is imported to transient structural analysis. The transient structural module was used for simulation since the simulation is time-dependent**.** The critical condition for failure, i.e., component face down, was considered while applying the acceleration input. The full model was provided with four fixed supports at the screw holes and input half sine acceleration pulse. Frictionless support boundary condition is applied to symmetric faces of quarter symmetry model and the fixed support is applied to the screw hole.

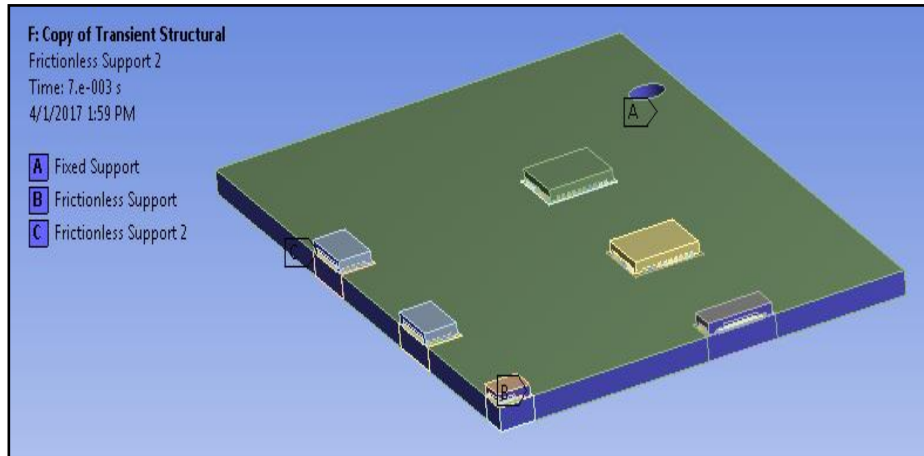

FIGURE 3-21: QUARTER SYMMETRY BOUNDARY CONDITIONS

With imported body temperature in the transient structural analysis, acceleration is applied to the whole system. The impact shows maximum deformation at the center of the PCB assembly. Figure 3-22 is the obtained total deformation for the model under drop testing with non-uniform temperature distributed the load. The maximum equivalent stress was observed at the fixed support i.e. screw hole.

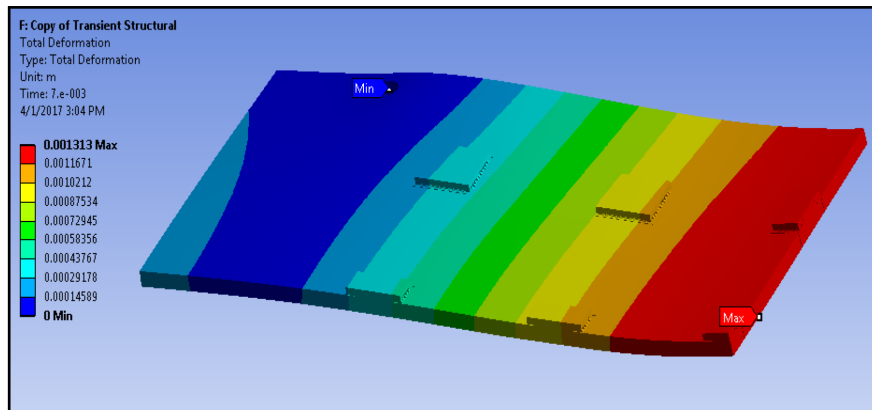

FIGURE 3-22: TOTAL DEFORMATION

The submodels technique was implemented for detailed analysis of critical package with maximum equivalent stress and strain. The temperature load was imported from a steady-state thermal analysis to the sub-model which is shown in Figure 3-23. The contour shows the distribution of temperature on sub-model, with maximum temperature at the die and minimum at the farthest point from the center. Similarly, cut boundary condition on all face is imported from transient structural analysis to sub-model, figure 3-24. Stress analysis with fine meshing is done in sub-model and the effect of drop test with package power is studied on solder joints. Fatigue and fracture failure could be possible due to this coupled load and it's important to study stress & strain on critical solder joint.

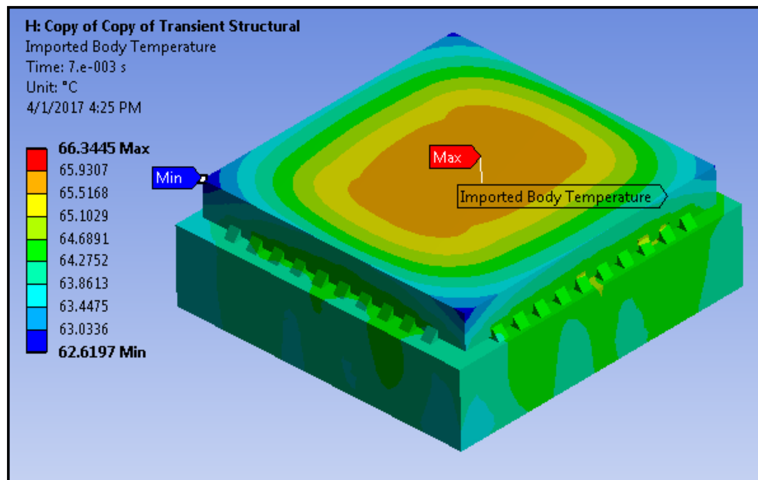

FIGURE 3-23: IMPORTED BODY TEMPERATURE

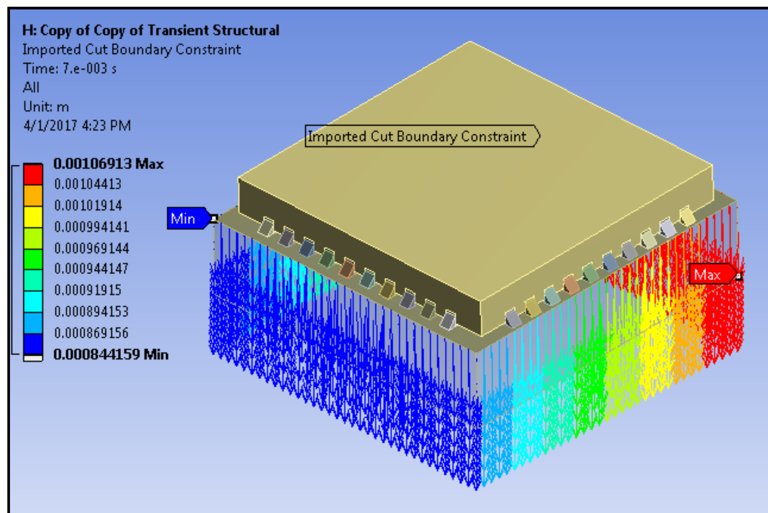

FIGURE 3-24: CUT BOUNDARY CONDITION FROM GLOBAL MODEL

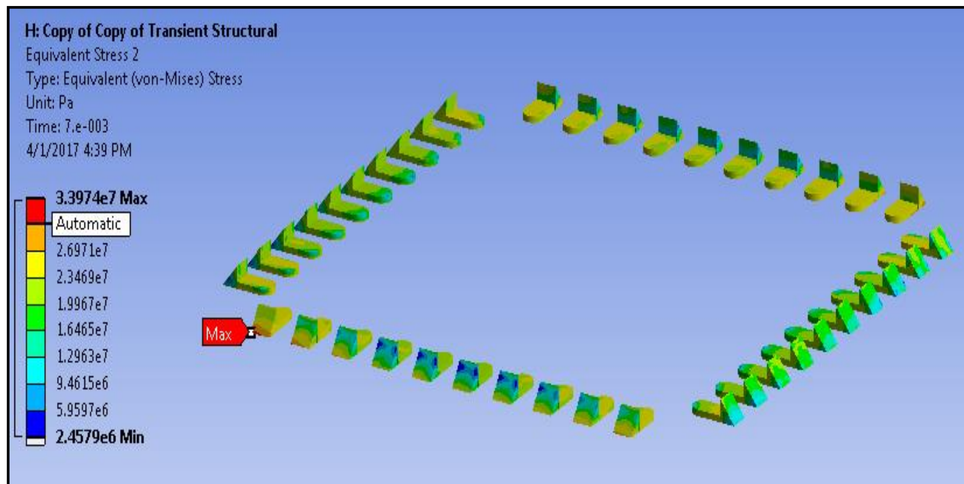

FIGURE 3-25: CRITICAL SOLDER JOINT

Critical solder joint was obtained for critical failure analysis. It was observed that the corner solder joint of the U1 (Corner package) package shows maximum equivalent stress. Figure 3-25 shows the critical solder pin with maximum von-Mises stress and maximum equivalent strain value. The computational drop testing was performed for both power off and power on. This will explain how the system can react under only drop testing and drop testing when the package is in a working state. Figure 3-26 shows the comparison of two cases by plotting time-dependent von-Mises equivalent stress on solder joints. The stress value is higher when the package is generating internal heat. The blue curve in Figure 3-26 is the time-dependent equivalent stress value on solder joints for the normal drop test. With the increase in time, the equivalent stress value keeps on vibrating and stabilizing.

The impact acceleration load is applied for only 0.5milliseconds and left unloaded for rest 6.5milliseconds. A similar trend was observed for the solder joint time-dependent equivalent strain.

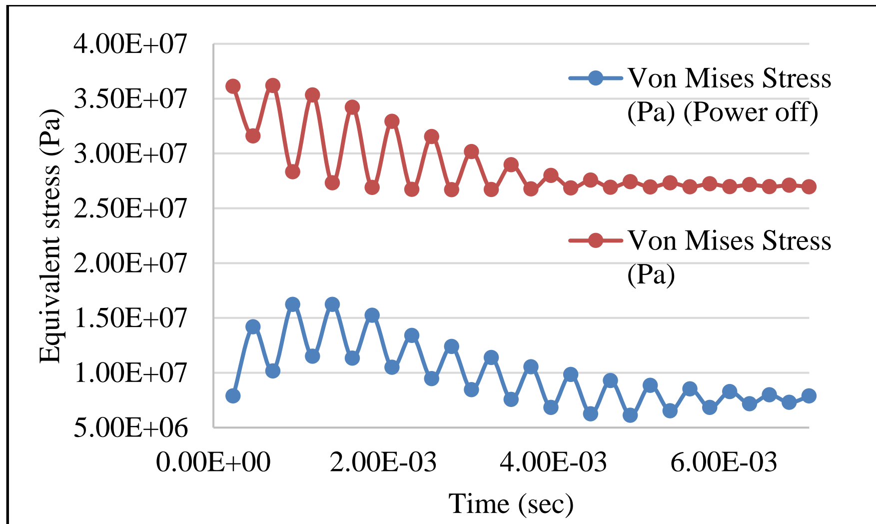

FIGURE 3-26: SOLDER JOINT VON MISES STRESS: POWER OFF & POWER ON

After studying the impact due to two loading case, the other motive of this work is the comparison of two thick PCB under drop test coupled with power load. Measured properties for two PCB are used for computation analysis. The similar methodology is leveraged for these two board i.e. 93mil and 134mil. Generally, the stiffness increases with increases in PCB thickness and in our case also we have observed the same. Regular composition trend in PCB stack up, thickness board with more copper content, helps in the comparison study. Figure 3-27 shows the

maximum von-Mises equivalent stress and equivalent strain on the solder joint. It can be observed that under the normal drop testing condition the package assembly with 134mil PCB shows more solder joint stress and strain value which is almost 25% more in the thicker board. PCB stiffness plays a significant role in drop testing and stiffer boards show more stresses at the solder joints. In the case, when the package is generating power and internal heat, we observed that stress and strain value increases by almost 3 times. The effect of mismatch in CTE and Young's modulus between PCB and package can be seen more in the second case.

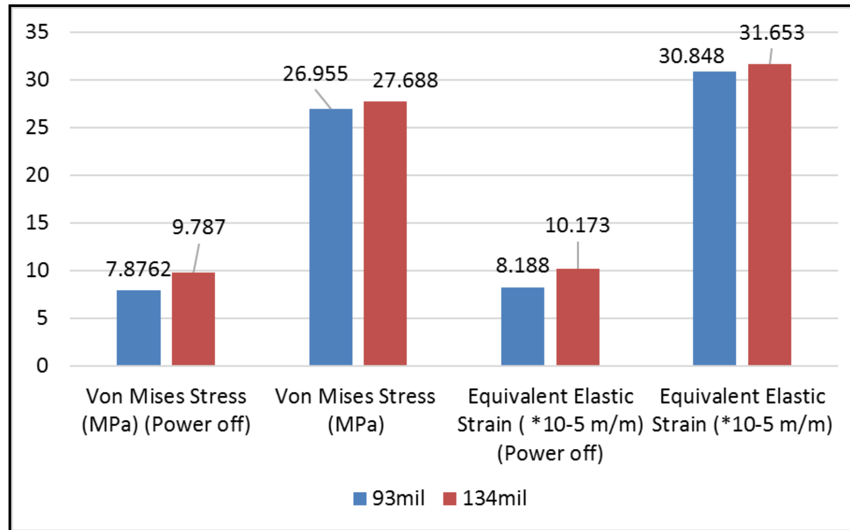

FIGURE 3-27: SOLDER JOINT ASSESSMENT OF TWO BOARDS UNDER DROP TEST

Stress on the boards depends on both the acceleration response and density. According to Che et al. [59], generation of high peeling stress is a good indication of high damage due to dropping test. The maximum peeling stress occurs on the PCB of the outer solder joint, and the stress induced by the bending moment is dominant. The numerical results show that only a few solder joints close to the edge of the component experience greater peeling stresses while the other majority is under quite a low-stress level. The bending deformation of the PCB and the component has great influence on the magnitude of the peeling stress [60]. As power cycling generates an uneven distribution of temperature throughout the study, I have considered performing uniform temperature distribution in the assembly.

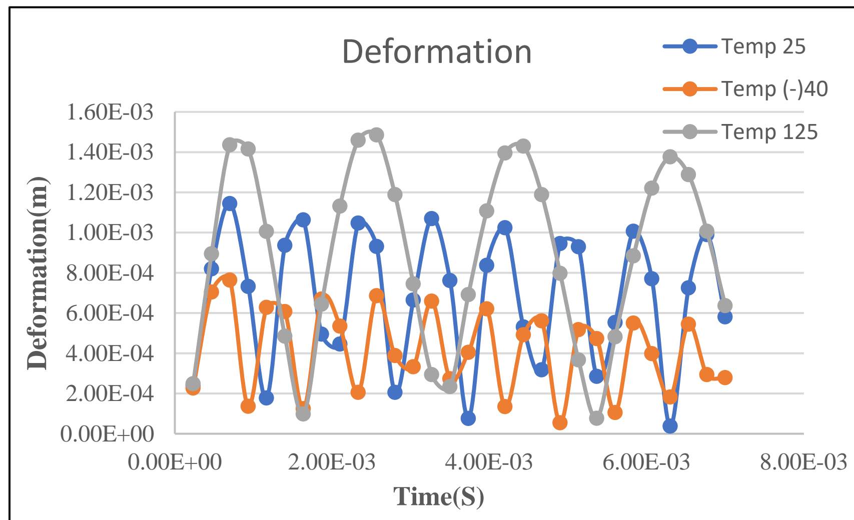

FIGURE 3-28 UNIFORM TEMPERATURE DEPENDENT DEFORMATION

Figure 3.28 & 3-29 shows the effect of uniform temp distribution in the assembly subjected to drop test. These results show that at higher temperature PCB shows flexible nature which results in more deformation at higher temperatures and hence the maximum peeling stress is observed at higher temperature assembly.

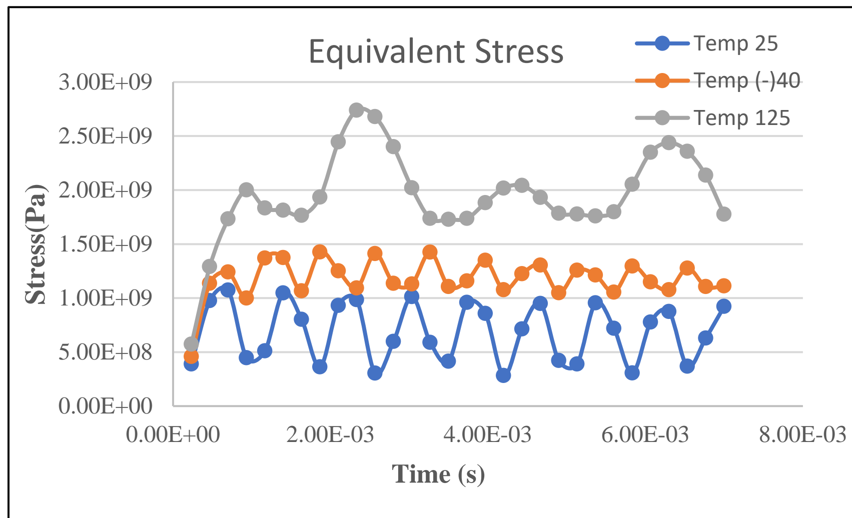

FIGURE 3-29 UNIFORM TEMPT DEPENDENT PEELING STRESS

Figure 3-30 shows the peeling stress comparison of two PCBs. The stiffer board show less deformation and less peeling stress under the given acceleration. 134mil board has 16 copper layers and the 93mil board has 10 copper layers. The critical solder (of U3 package) under peeling is different from the critical solder joint (of U1 package) observed in equivalent stress or strain value.

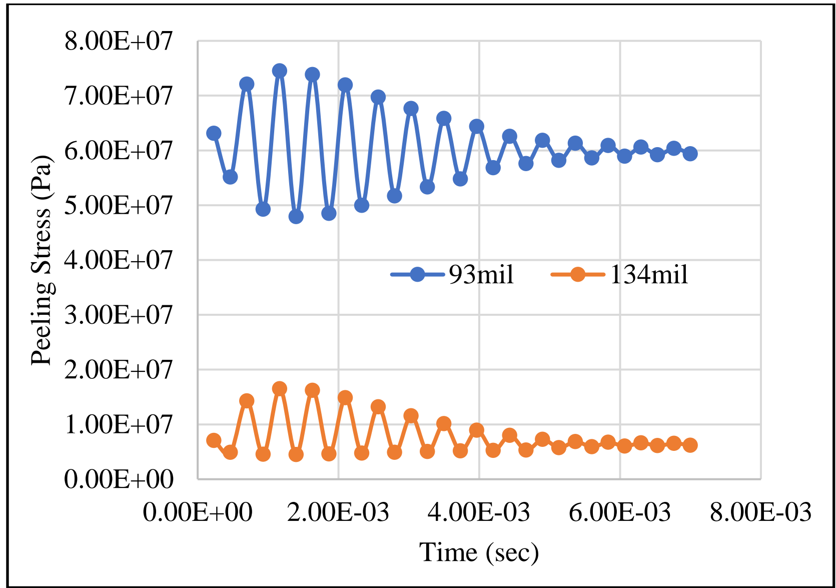

FIGURE 3-30: TIME-DEPENDENT PEELING STRESS

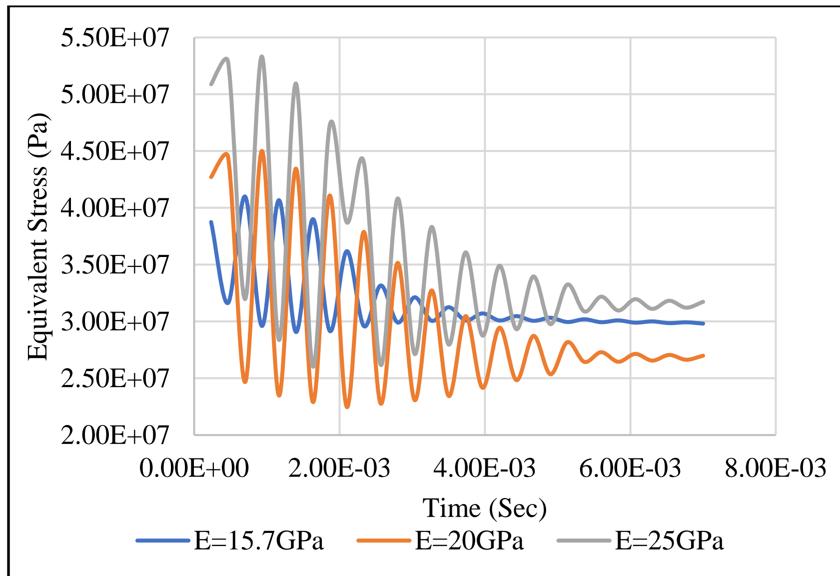

FIGURE 3-31: TIME-DEPENDENT SOLDER JOINT VON MISES STRESS

In the last part of the study, the PCBs with different stiffness were compared of the PCB with the same thickness i.e. 15.7GPa, 20GPa, and 25GPa. Figure 3-33 shows the comparison of time-dependent solder joint von-Mises stress. The solder joints are subjected to bending moment, axial force, and shear force when the PCB subjected to bending moment. The PCB and component bend under the act of G(t). However, the difference of the bending stiffness between the PCB and component make the solder joints deforming under tensile/compressive stresses during PCB bends upward/downward [60]. The board with higher Young's modulus show higher equivalent stress value. The rigidity of board or mismatch in elasticity between board and package creates a lot of stress on solder joints. This equivalent stress value decreases with a decrease in the thickness of the board. The similar trend can be seen with strain results. Figure 3-32 shows the flexural deformation of board assembly. The board with less elastic modulus are considered to be more flexible and deforms more under impact loading, in another way it shows more acceleration response.

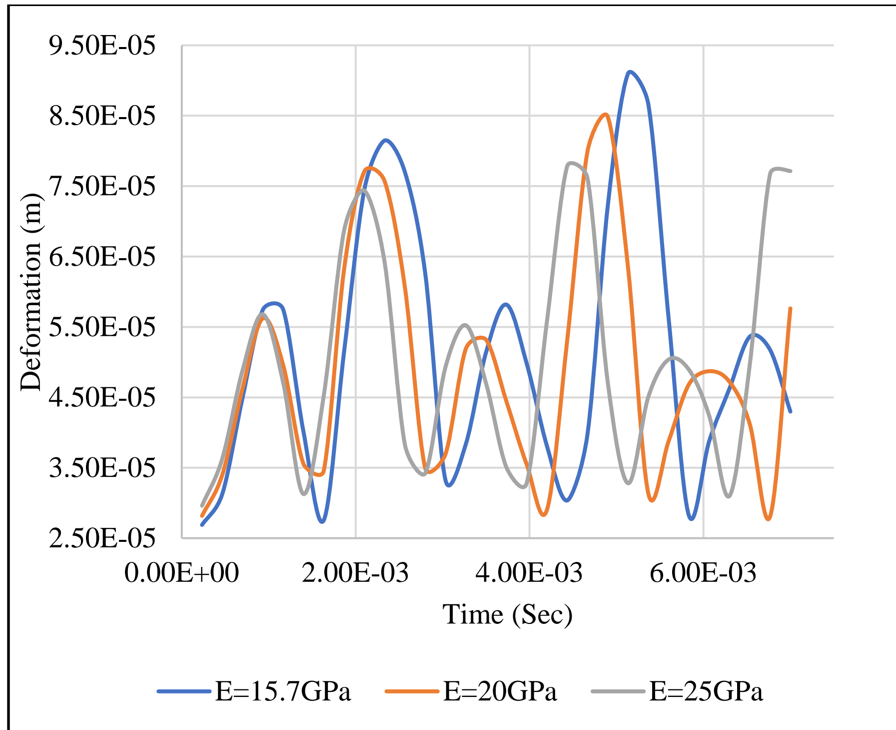

FIGURE 3-32: PCB (THICKNESS CONSTANT) FLEXURAL DEFORMATION

As we discussed, the rigidity of PCB is governed by the content of copper in it. Changing copper layer thickness significantly affect the reliability of the system. The results mentioned in figure 3-33 shows the variation of total deformation of the assembly versus thickness of the outermost copper layer in 134 mil PCB. The single copper layer thickness was varied from 0.025mm to 1.25mm and the total deformation was noted. It can be observed that with the increase in copper layer thickness, the total deformation of the assembly decreases. The amount of plastic

deformation reduces due to increases in an overall increase in the Modulus of elasticity. [3]

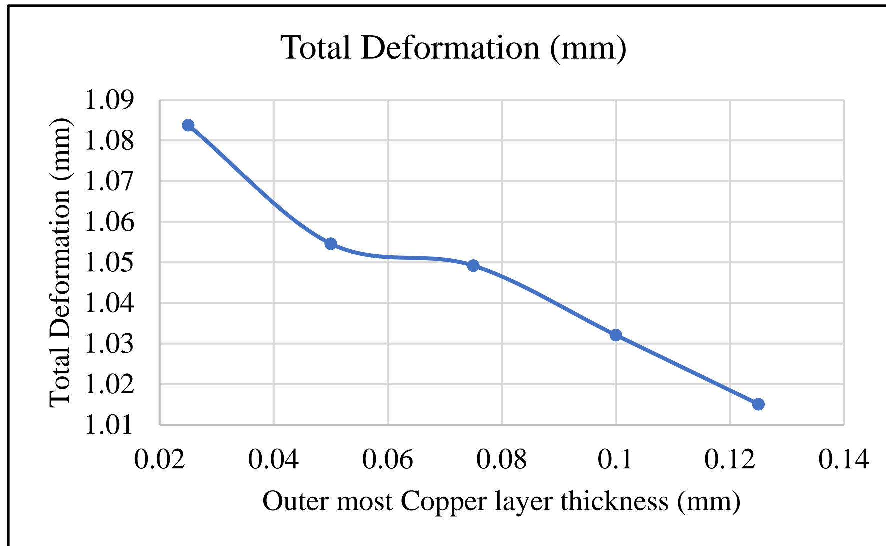

FIGURE 3-33 TOTAL DEFORMATION VS OUTERMOST COPPER LAYER THICKNESS

3.8 SUMMARY

Material characterization of two printed circuit boards was done using instruments like TMA and DMA. The composition of each board was observed to analyzed PCB stack-up and copper content. PCB assembly for QFN package was modeled on ANSYS Workbench 19.0 referring JEDEC standard for drop testing. The more realistic approach was tried to introduced by performing drop test when the package is in working condition. Temperature distribution on PCB assembly was obtained

on steady-state thermal analysis model of ANSYS. The time-dependent temperature profile was coupled with acceleration load in the transient structural analysis where drop testing is performed. It was observed that the failure due to coupled thermal and impact is more severe than the normal acceleration load. More than 30% of equivalent stress on critical solder was observed under coupled load. The motivation of any reliability assessment is to check failure rate and life to failure of an electronic component. Therefore, considering thermal impact due to package power during impact loading or drop testing could be the more realistic approach for reliability testing. In the second part of the paper, it was studied that the PCB with higher stiffness are more subjected to solder joint failure under drop testing coupled with power load whereas the deformation and peeling stress of PCB assembly were higher for thinner boards due to its flexible behavior. The mechanical material properties like stiffness and Poisson's ratio of the components are the main parameter for the drop test but when the thermal load was coupled with drop test, a mismatch in CTE of components becomes additional parameter which is considered here. The experimental data can provide significant strength to this work.

Chapter 4

MULTI-VARIABLE DESIGN OPTIMIZATION STRUCTURAL INTEGRITY OF 3D TSV PACKAGE

4.1 ABSTRACT

New electronic devices with small size and low power consumption are in demand in recent years. Miniaturization and complex product are required in modern electronics for more functionality in the smaller electronic package. To overcome such issues, 3D packages or package on package (PoP) are introduced. The 3D packaging is stacking of chip on top of another which is emerging as a powerful technology that satisfies such integrated circuit (IC) package demands. A 3D package using through silicon vias (TSVs) has emerged as an effective technology for future interconnection requirements. The mismatch of coefficient of thermal expansion (CTE) of the SiO2 and copper used in TSV can induce a lot of thermal stresses. The stress developed at interfaces results in the interfacial delamination of TSV, which is mainly driven by a shear stress concentration at the point. The developed thermal stresses are critical for the thermo-mechanical reliability of the 3D package. In this dissertation, the effect of package structure on the failure metric of the 3D package has been studied. J-integral has been used to quantify the crack driving force. The crack is modeled at the TSV and BEOL (Back End of the Line) and the die -substrate thickness is varied and studied during chip attachment process

and under thermal cycling load for optimizing the die and substrate thickness design [1]. Finite Element method has been used to analyze the thermo-mechanical stresses and fracture parameters in TSV structures 3D package. For this study, full field compact modeling methodology [2] has been leveraged for the ease of FEA using ANSYS Workbench 17.2. An optimized package assembly was obtained to reduce the crack driving energy at the TSV region and in the BEOL dielectric layer. The thermo-mechanical deformation and stress develop inside the package during assembly and subsequent reliability tests due to the mismatch of the coefficients of thermal expansion (CTE) between the chip and the substrate. The thermal residual stress causes many mechanical reliability issues in the solder joints and the underfill layer between die and substrate, such as solder fatigue failure and underfills delamination [61]. Moreover, the thermo-mechanical deformation of the package can be directly coupled into the Cu/low-k interconnect, inducing large local stresses to drive the interfacial crack formation and propagation [62].

The effect of different parameters like material properties of Mold and Underfill on warpage is studied. Also, crack propagation and delamination between Cu-SiO_2 interface is studied under thermal cycling load. As chip-package interaction is most critical or maximum at the time of die attach process during chip to package assembly, the crack propagation is studied at reflow condition. A sub modeling technic is leveraged to induce pre-existing virtual crack to investigate delamination

at Cu-SiO2 interface. A design approach has been proposed to mitigate brittle failure issues thus improving the thermo-mechanical reliability of the 3D package.

Keywords – TSV, BEOL, FEA, Crack propagation, J-integral, CTE, low-k dielectric, Thermal loads

4.2 INTRODUCTION

On the demand for greater portability of electronic devices, the electronics in today's digitized industry are undergoing integration and miniaturization to become smaller and lighter for ease of its application. The electronic packaging industry is driven by the chips with more I/O's and the state-of-the-art multi-functionality. On the other hand, the efficiency and quality with the reduced cost and power loss must be established, which inspires the manufacturer to do 3D stacking of chips. This necessitates an effective communication between the IC and the electronic system. Thus, due to low cost, small form factor and high-performance 3-dimensional integration have emerged as a boost to electronic packages manufacturing company. In 3-dimension packages, TSV technology is used. In TSV packages, a thin silicon wafer is drilled with holes and dielectric SiO_2 is deposited along the inside walls of the holes, which are further filled with copper. Removing heat from the system with TSV's is a challenge, which creates an issue. Else, the CTE

mismatch of different material will cause thermal stresses to be developed. Results in forming keep out zone where active transistors cannot be placed. TSV package has some critical stress areas like SiO_2/Cu interface, and Silicon, which may lead to crack. There will be reliability issues due to these cracks. Work is done to obtain a relation between crack location and K1, K2, K3. Also, the relation between J-Integral, substrate thickness and die thickness are obtained. ANSYS 19 bundle is used for modeling and simulation and finite element analysis (FEA) is used to calculate stress intensity factor (SIF) at the crack interface. [63] [64] [65]

4.3 LITERATURE REVIEW

Zheng et al. [66] introduced the development trends of 3-D stacked packages. The advantage of 3-D over the traditional 2-D or planar packaging (Multi-Chip-Module, MCM) and challenges faced by the 3-D technology have been discussed. Selvanayagam et al. [67] demonstrated the nonlinear stresses and strains in the μ-bumps between the silicon chip and copper filled TSV interposer (with and without underfill) for a wide range of via sizes and pitches, and various temperature conditions.

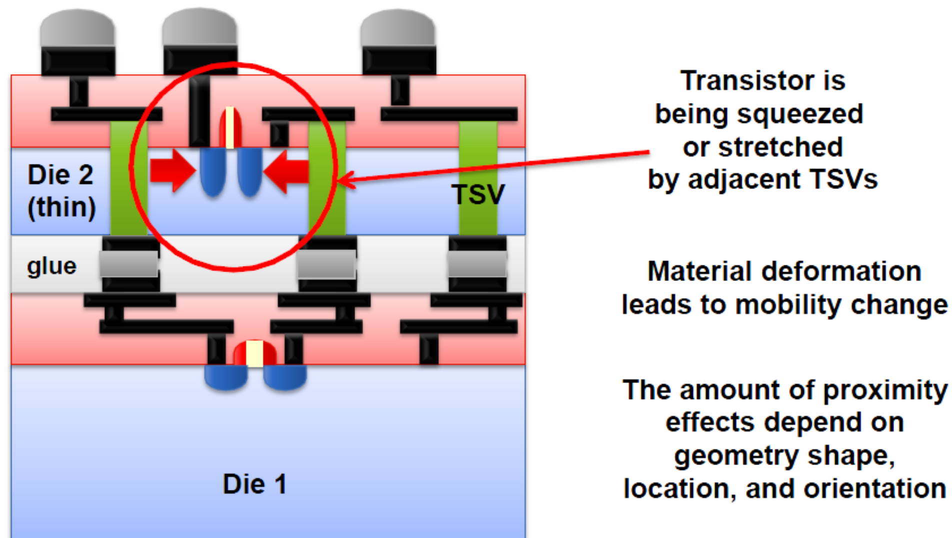

FIGURE 4-1 STRESS AFFECTS TRANSISTOR PERFORMANCE

Selvanayagam [67] results were useful for deciding if underfill is necessary for the reliability of μ-bumps and selecting underfill materials to minimize the stresses and strains in the μ-bumps. [68] et al. developed an analytical model for the three-dimensional state of stress in a periodic array of TSVs. The model accounts for Cu plasticity and predicts the out-of-plane protrusion that occurs in the TSV due to differential thermal expansion with the surrounding Si.

Excessive out-of-plane deformation of the top surface of the via has the potential to induce fracture causing stress in the brittle dielectric layers that lie above the via. Kawa et al. [69] studied the TSV related performance and reliability issues due to

thermal-mechanical stress using Fammos TX. He showed that the localized TSV/Si stress significantly affects the BEoL mechanical response/reliability and the transistor performance (see figure 4-2). Alam et al. [70] analyzed the parasitic characteristics of inter-die bonding techniques and materials.

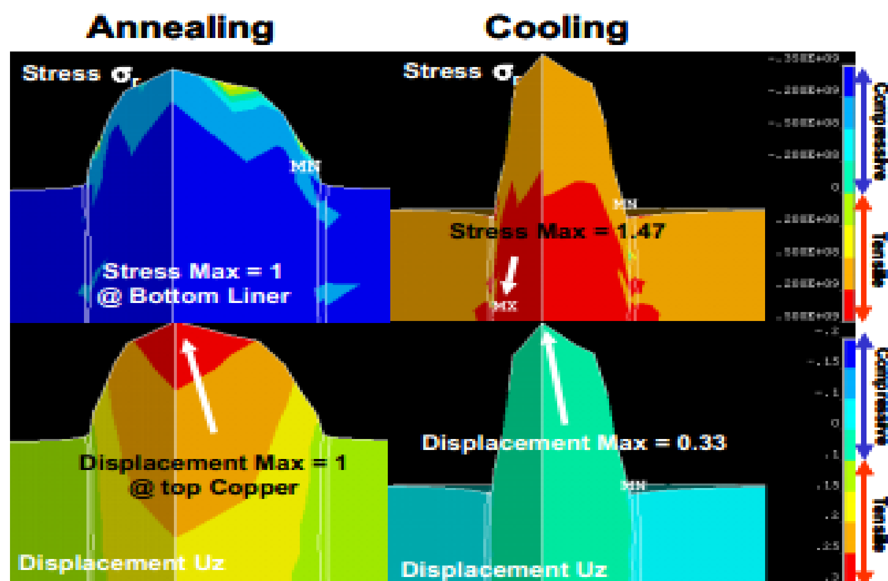

FIGURE 4-2 TSV CU PROTRUSION [KAWA ET AL] [69]

4.4 OUTLINE

ANSYS 19 is being leveraged for modeling all types of cracks. Quarter symmetry TSV package is modeled in the same software, which was used to simulate the reflow condition and thermal cycling to analyze the various stresses developed

within the TSV package. The temperature boundary condition subjected to the package was 200°C to room temperature for reflow condition and -40 to 125°C thermal cycling. The sub-modeling technique was used to analyze the copper-SiO2 interaction of the TSV. The cracks are modeled at a different position on TSV and different dielectric layers of BEOL to study crack behavior. Die and substrate thickness was varied to study the behavior of stress intensity factor and J-integral. Nine tracks were modeled along the TSV with the same direction. Two independent loading conditions were tested, and J-integral variation was studied by varying the substrate and die thickness. Two independent loading conditions are Reflow condition and Thermal Cycling.

4.5 MODEL DESCRIPTION

2 die 3-D flip chip package along with the TSV has been studied with respect to the crack propagation analysis. The response of this package after connecting substrate and the chip has also been studied. TSV has a diameter of 10μm including 9μm Cu diameter and 0.5μm thick SiO_2 layer for insulation. To avoid the adverse effects of silicon efficiency, the TSV is restricted to less than 4 percent of total silicon real estate. There are 2 steps that play a vital role in simulation. Initially, a global model with detailed assembly is formulated and solved. The results from this solution are

used to generate boundary conditions to the sub model 1 which is part of the critical region having detailed features (for example practical μ-bump interconnections and TSVs). To prevent rigid body motions, a center node at the bottom is fixed and normal displacement with respect to the symmetric faces are constrained. Using linear elastic material properties from Rajmane et al, all the materials except copper (TSVs and BEOL) and solder (SAC305) are modeled. [49] [1] Using Anand's viscoplastic model and considering the creep and plastic deformations (representing secondary creep), solder is modeled as rate dependent viscoplastic material. To describe the inelastic behavior of lead-free solder, Anand's viscoplastic constitutive law has been used. Anand's law has an impact on a total of nine material constants A, Q, ξ, m, n, h, a, s, $\hat{s}$ (all of which are extracted from the curve fitting experimental data) that are used throughout the solder strain-rate and temperature sensitivity.

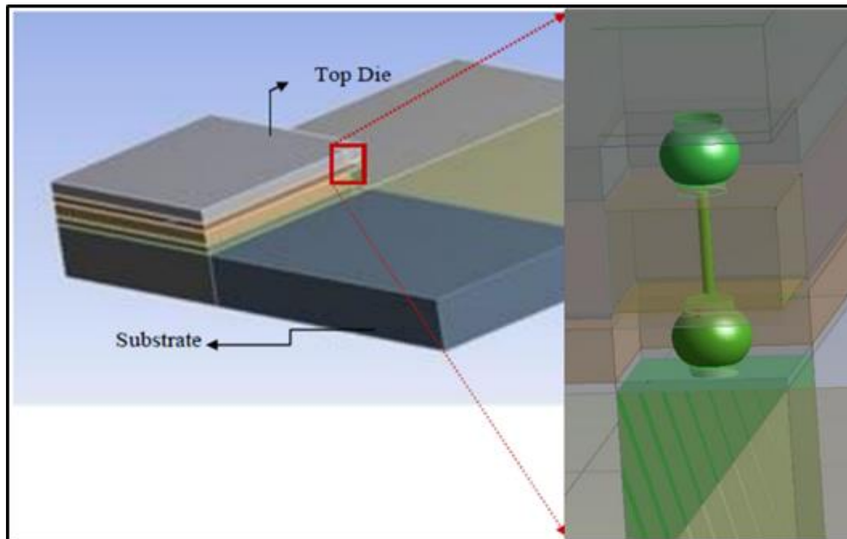

FIGURE 4-3 GLOBAL MODEL WITH HIGHLIGHTED SUB MODEL 1

TABLE 4-1 ANAND'S CONSTANTS

S. No.	Anand's Constant	Units	Value
1	s_0	MPa	1.3
2	Q/R	1/K	9000
3	A	Sec^{-1}	500
4	ξ	Dimensionless	7.1
5	m	Dimensionless	0.3
6	h_0	MPa	5900
7	ŝ	MPa	39.5
8	n	Dimensionless	0.03
9	a	Dimensionless	1.5

Crack propagation is placed in a different location along the cylindrical silicon die interposer where the TSV and copper passes. In this experiment, silicon and silicon

dioxide are covered as the critical area on the TSV interface. Therefore, the crack is modeled successfully along the silicon die/Cu interface. This is the prominent region for critical stresses acting where more chances of crack to be developed.

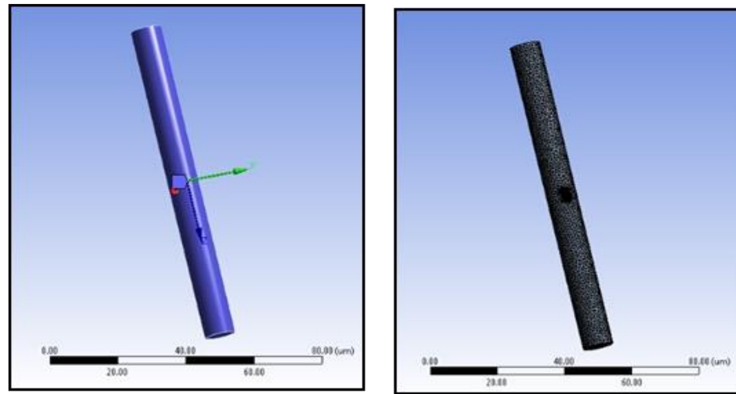

FIGURE 4-4 CRACK FORMULATION & MESHED BODY ON TSV OF SUB MODEL

All modeling and formulation of radial horizontal crack for the TSV package are done using ANSYS 19 bundle. The tetrahedron mesh profile is used here and only semi-elliptical cracks can be a model on the exterior surface using the software. The global model as a compressive model is subjected to same reflow conditions. The sub model 1 has been cut in two half and simulation is done with the same reflow conditions. The crack has been modeled in the sub model 2 which is one of the symmetrical halves of submodel 1. The sub model 2 was again subjected to the same reflow condition with importing cut boundary constraints from the sub

model 1.10 divisions with equal space have been taken for simulation of the crack where the total edge length of TSV is 95µm. All the simulations are done along the length of TSV in sub model 2 with an equal division of 9.5µm. When it is attached to the substrate, reflow condition is taken for thermal loading in 3D TSV package from 200ºC to room temperature (for Pb-free SAC305 Alloy). The plot for the relation between stress intensity factor (SIF) (i.e. K_1, K_2, K_3) and crack location have been shown in this paper. Also, the relation between crack size, crack length and J-integral is shown in the plot. The results show that the TSV area is much affected by mode 1, mode 2 and mode 3 cracking. To avoid radial crack, K should be less than K_c, i.e. $K<K_c$ where K_c is the fracture toughness of silicon.

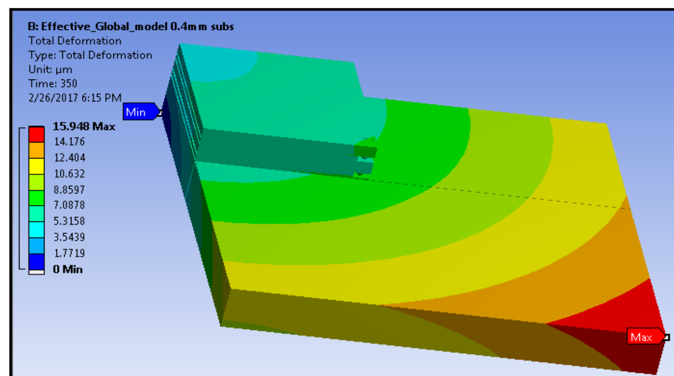

FIGURE 4-5 TOTAL DEFORMATION OF GLOBAL MODEL

4.6 SIMULATION AND VALIDATION

The analysis result shows that the normal stress (in the Z direction in our case) is positive across the middle area of the silicon/ copper interface. The stress distribution data is obtained after simulating under reflow conditions. The middle area of TSV is influenced to Mode 1 fracture, which is determined from the plot shown. The value K_1 increases at the start and then decreases. It is positive in the middle region (Figure 4-7). Crack on mode 2 is predominant in the top region of the interface (Figure 4-8). In figure 4-9, from the plot between K_3 and the crack location, the top and bottom portions of the TSVs are more susceptible to mode 3 fracture, as the value of K_3 is lower in the middle region. K depends on the load and cracks geometry

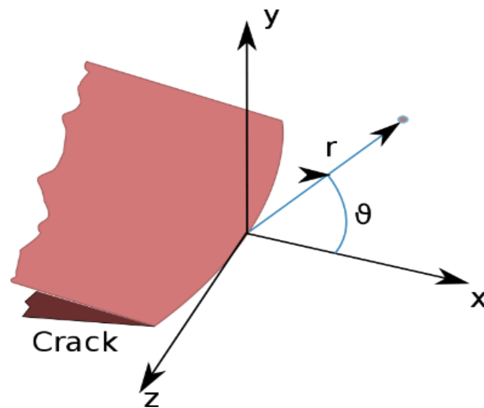

FIGURE 4-6 POLAR COORDINATE AT CRACK TIP

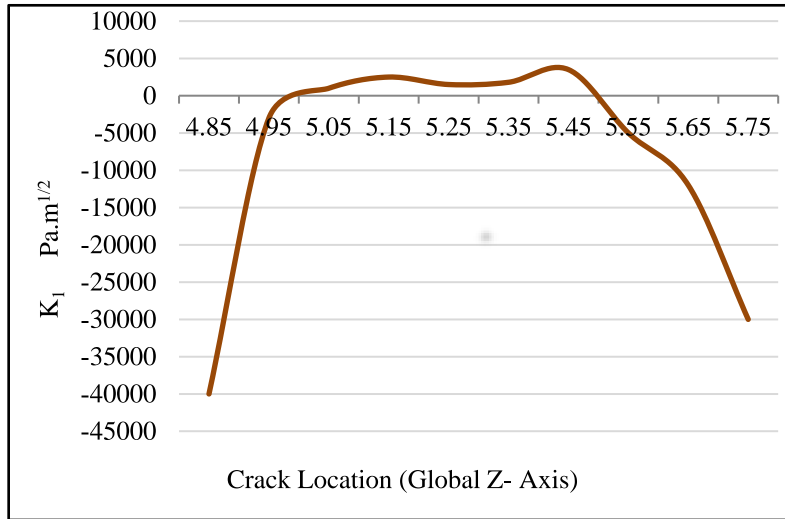

FIGURE 4-7 SILICON DIES/CU STRESS DISTRIBUTION WITH K1 PLOT

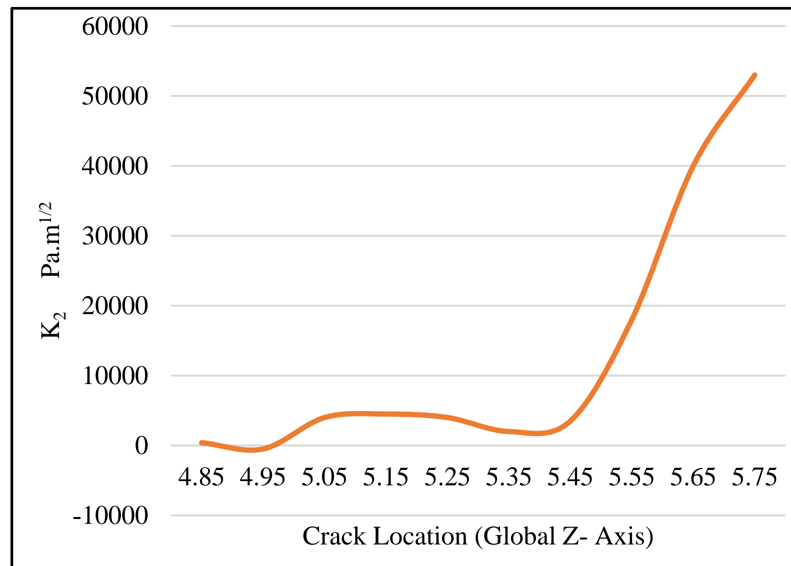

FIGURE 4-8 K2 CRACK LOCATION PLOT

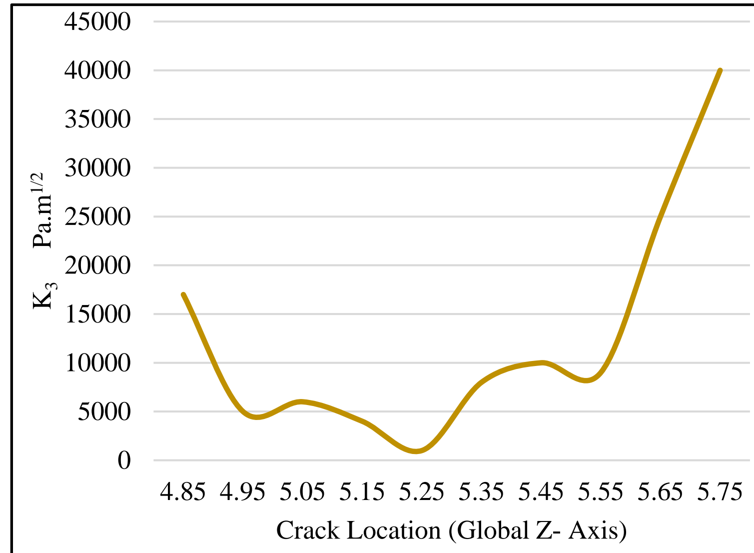

FIGURE 4-9 K3 CRACK LOCATION PLOT

J-integral is used to calculate the strain energy release rate per unit fracture surface. It is not path-independent of while loading elastic-plastic material. Rice J.R., 1968, showed that the J-integral is a path independent line integral and it represents the strain energy release rate of non-linear elastic materials. The value of J is determined by calculating the area under the load versus deflection curve which can be seen in figure 4-10. [71] [72]

$$J = \int_{\Gamma} \left(W dy - T \frac{\partial u}{\partial x} ds \right)$$

$$W = W(x, y) = \int_{0}^{\varepsilon} \sigma_{ij} \, d\varepsilon_{ij}$$

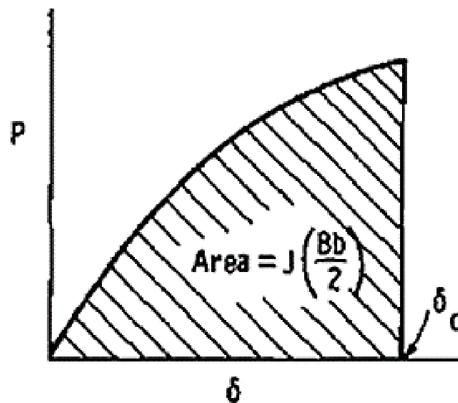

Figure 4-10 Load vs Deflection

Where W is the strain energy density per unit volume, ds is an infinitesimal element of the contour are length, Γ denotes any contour path surrounding the crack tip, and T and u are traction and displacement vectors along Γ Curve.

4.7 RESULTS

Maximum stresses were investigated at a different location of TSV copper core and deposited a layer of SiO_2. It has observed that the copper core has more deformation and von-mises stress which is shown in figure 4-11. So, for the further study, crack was modeled on the copper core and all analysis was done.

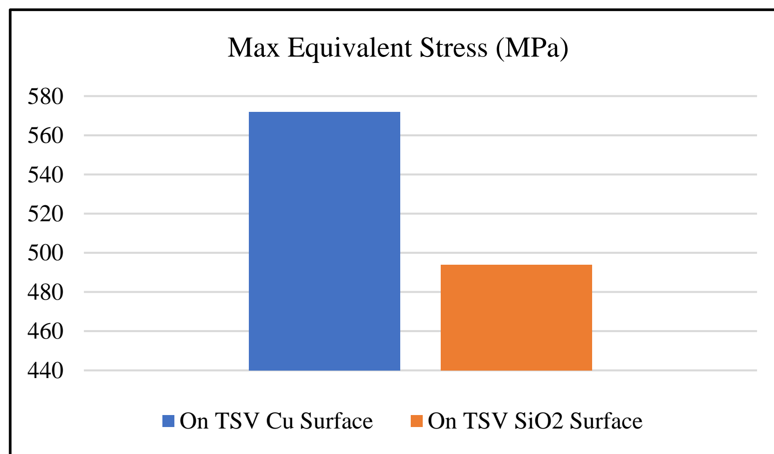

FIGURE 4-11 MAX VON MISES STRESS TEST ON TSV COPPER CORE AND SIO2 SURFACE

4.7.1 Reflow condition:

4.7.1.1 Die-Substrate thickness ratio

Reflow soldering is the common method of attaching microelectronic devices to the printed circuit board. Solder paste is used to attach the electronic component.

Reflow is the process when there are maximum stresses are developed in the solders and the assembly. To analyze peeling stresses and delamination, pre-existing virtual crack was modeled along the TSV and reflow thermal load was applied to the 3D package assembly. In the reflow condition, the initial thermal load is applied at $200^{O}C$ and in 350 seconds it brought to the room temperature i.e. $25^{O}C$. In this study, number cases were considered i.e. the effect of substrate thickness, the effect of Die thickness and the best combination of substrate and die thickness. Furthermore, best-selected combination used to analyze the effect of mold material on Cu-Sio_2 and studied peeling stresses. The variation of stress on TSV with respect to substrate thickness is demonstrated in figure 4-12 below. The figure shows the stress distribution when die thickness kept constant at 0.1mm and 0.4mm while substrate thickness is varied from 0.1mm to 0.6mm. From these results, it is very clear that 0.2mm thickness substrate shoed maximum stresses for both die thicknesses. So, 0.2mm substrate thickness would be the worst combination for die and substrate thickness to be used. After 0.4mm substrate thickness for both die thickness, the stresses stabilize and remain same with less value.

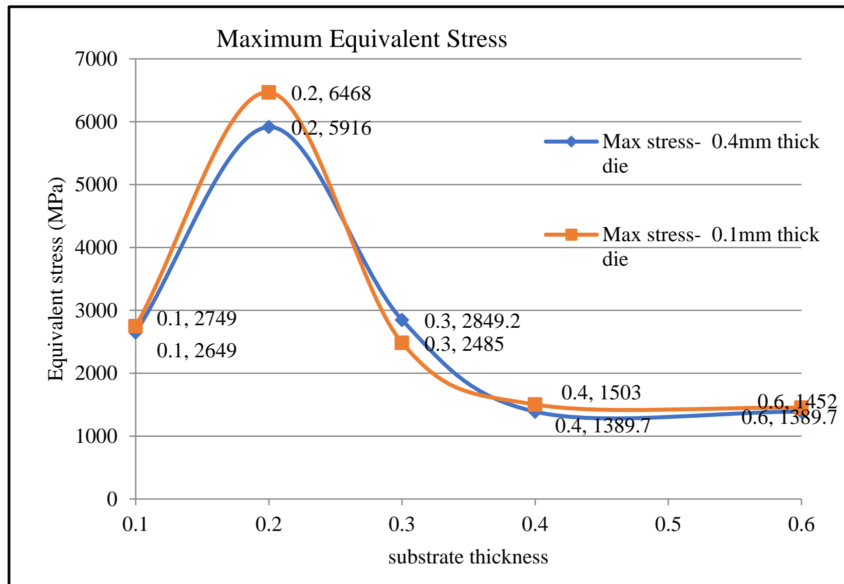

FIGURE 4-12 MAX STRESS VARIATION WITH SUBSTRATE THICKNESS

The aim of this work is to study the variation of J-Integral with package assembly structure. Figure 4-13 shows the change in the J-Integral value of horizontally oriented crack with a variation of substrate thickness keeping dies thickness constant at 0.1mm. The J-integral value decreases with the increase of substrate thickness and remains same after 0.4mm. Horizontally oriented cracks were modeled at 9 different locations on TSV but in figure 4-14 only cracks at three locations of TSV are shown

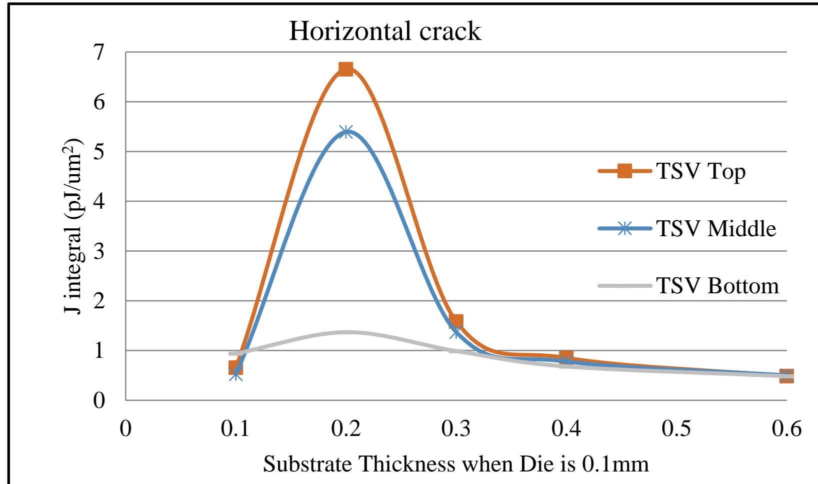

FIGURE 4-13 J-INTEGRAL VS SUBSTRATE THICKNESS FOR HORIZONTAL CRACK

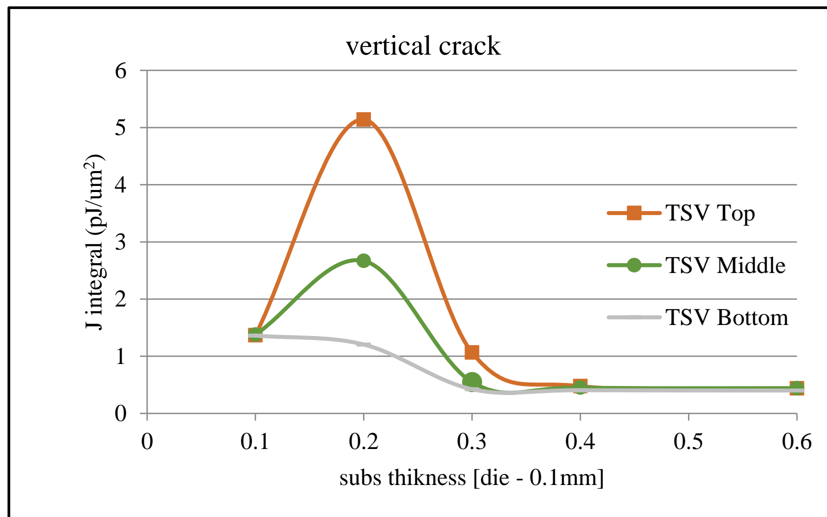

FIGURE 4-14 J-INTEGRAL VS SUBSTRATE THICKNESS FOR VERTICAL CRACK

and relation for vertical crack is shown figure 4-14. From both figures, we can conclude that crack located at the top side of TSV should be considered as a critical crack which will lead to failure. This means crack will propagate through the top part of TSV and propagated throughout the Cu-Sio2 interface. 0.2mm Substrate to 0.1mm die combination showed highest J-integral value, hence worst design choice. 0.4mm substrate thickness, which can be considered as the best design. Compared to stresses or J-integral values of 0.1mm thickness substrate, there is no significant decrease in the stresses. So, considering cost and all other factors 0.1mm die to 0.1mm substrate thickness combination is the best design to consider.

4.7.1.2 Effect of Mold component Material

Three packages with identical structure and properties were tested under reflow condition to analyze the effect of mold component material stiffness on the reliability of TSV interface. Table 4-2 shows how J-int value changes w.r.t. mold material. From this, we can conclude that materially contributes to TSV delamination.

TABLE 4-2 CHANGE IN J-INT W.R.T TO MOLD MATERIAL

Mold Type	J-Int (PJ/um2)
Stiff	0.0854
Original	0.065
Soft	0.054

4.7.2 Thermal Cycling

Thermal cycling is a most common method to test the strength of electronic device assembly against the low cycle fatigue load. Accelerated Thermal Cycling is performed to determine the working life of components and solder interconnects. The thermal cycling was performed as per the JEDEC standard - JESD22-A104D. Experimentally this test is done in an environmental chamber with the same condition mentioned in standards. Developed mechanical stresses and strain energy can be used to investigate the solder joints or assembly reliability. The temperature varies from -40°C to 125°C in a cycle and 3 cycles has been performed in ANSYS for 10800 sec. The dwell and ramp rates were 15mins for each step to induce creep strain in the solders. Like a reflow condition, crack was modeled on the TSV core at different location and variation of J-integral was studied with respect to substrate thickness and with changing top die thickness. Figure 4-13 shows the variation of J-integral value for the different size of the substrate for two different top die size. In this study, two cracks were modeled at the top and bottom of TSV. When the thickness of the top die is 0.1mm the variation of j integral values were noted. The J-integral value decreases with increase in substrate thickness and then increase to some extend and stabilize after 0.4mm thickness. Similarly, for 0.4mm die

thickness, j integral value decreases and then remain the same after some limit. The red circle in below figure is the optimized region where all design parameters show minimum j integral i.e. resistance to crack propagation.

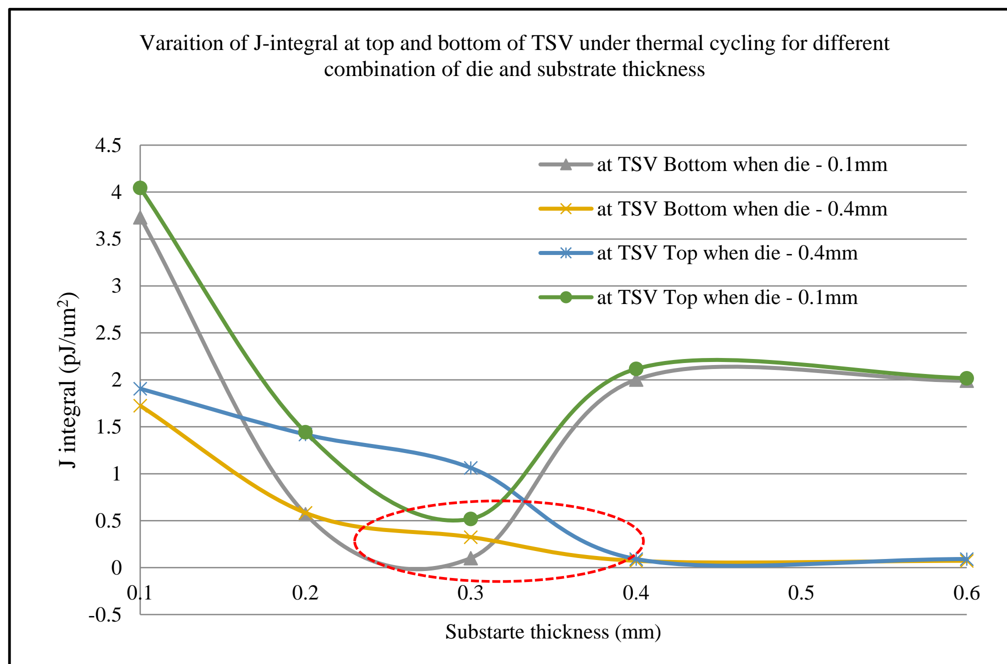

FIGURE 4-15 J INTEGRAL VARIATION ON TSV WITH SUBSTRATE THICKNESS

Nine cracks were modeled on the TSV core surface at distance of 11micron with the same dimension. The variation of j integral of each crack is shown in Figure 4-14. The j1, j2 … j9 is the different location of crack on TSV starting from the top to bottom. The red box shows the optimized value of substrate thickness for 0.1mm die thickness.

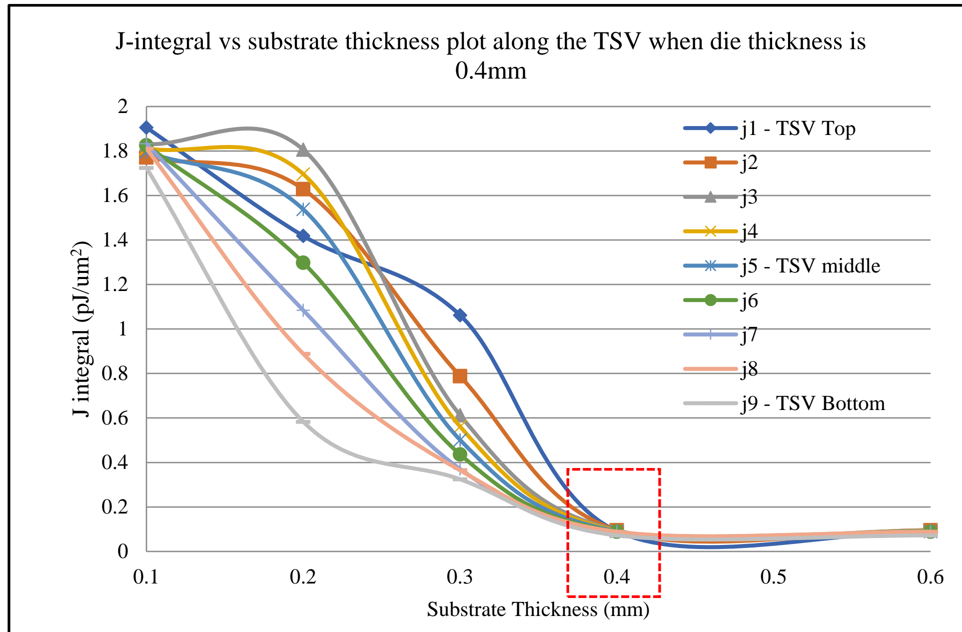

FIGURE 4-16 J INTEGRAL VS SUBSTRATE THICKNESS ALONG TSV CORE FOR TOP DIE THICKNESS 0.4MM UNDER THERMAL CYCLING

Similarly, for top die thickness of 0.4mm, j integral value has been noted for each crack by changing substrate thickness. It is observed that the 0.4mm substrate thickness is optimized value mentioned in figure 14 in the red box. J-integral value for each crack decreases with the increase of substrate thickness.

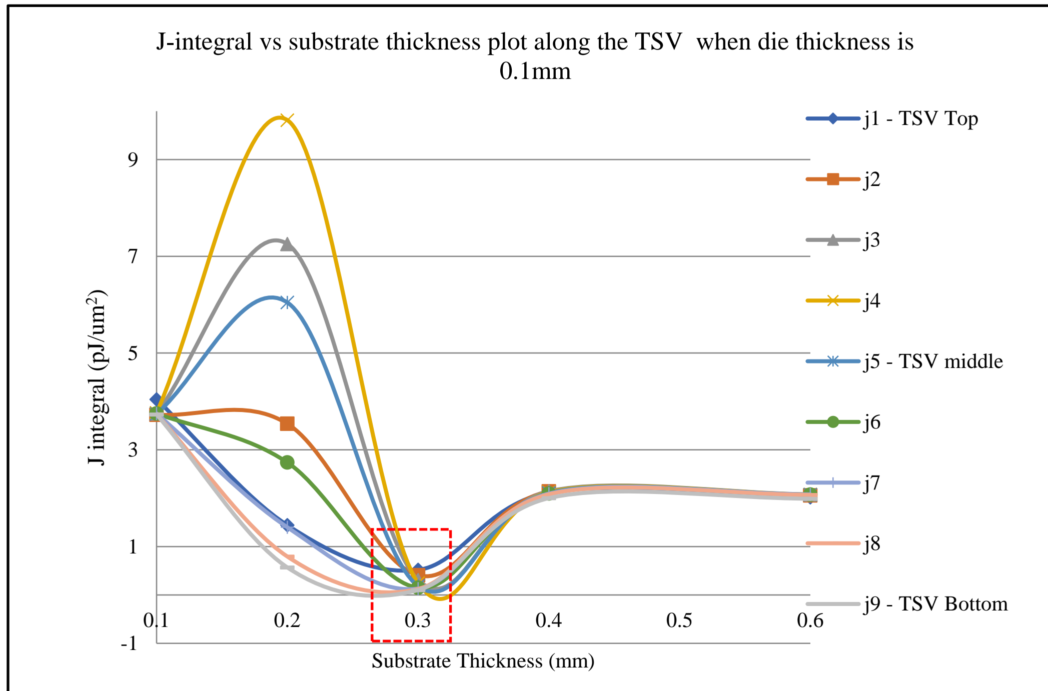

FIGURE 4-17 J-INTEGRAL VS SUBSTRATE THICKNESS ALONG TSV CORE FOR TOP DIE THICKNESS 0.1MM UNDER THERMAL CYCLING

J-integral value is line integral of the crack tip. So, per the literature survey, the value of J-integral should increase with an increase in crack size. For a detailed analysis of the study on 3D TSV package, crack size was increased, and the j integral value has been noted. Figure 4-16 shows the relation of crack perimeter and j integral value.

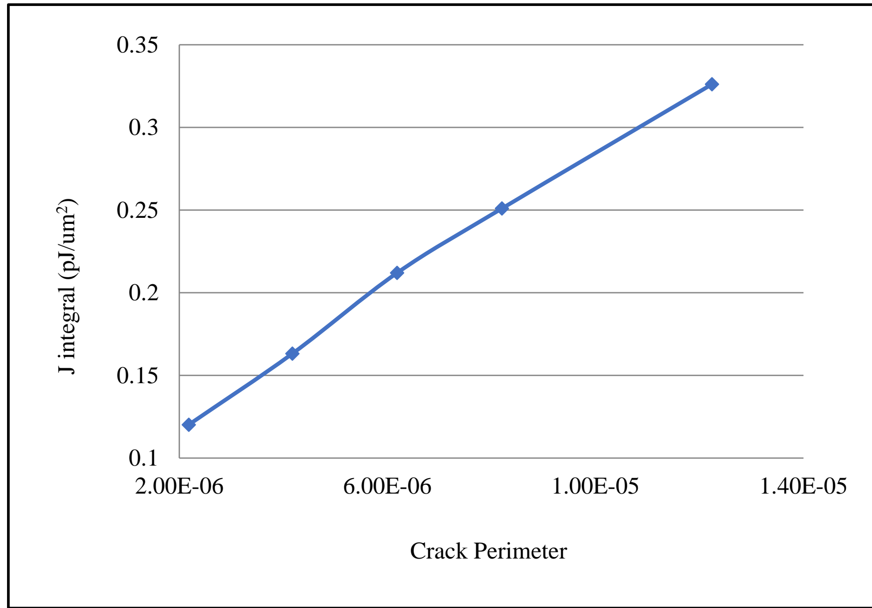

FIGURE 4-18 J-INTEGRAL VS CRACK PERIMETER

Also, the variation of maximum equivalent elastic strain value has been noted for different crack size. The relation between strain and the crack perimeter is shown in figure 4-18. The maximum strain value increases first and then decreases up to a certain limit. After 7-micron crack perimeter, the strain stabilizes and remain the same with an increase in crack size.

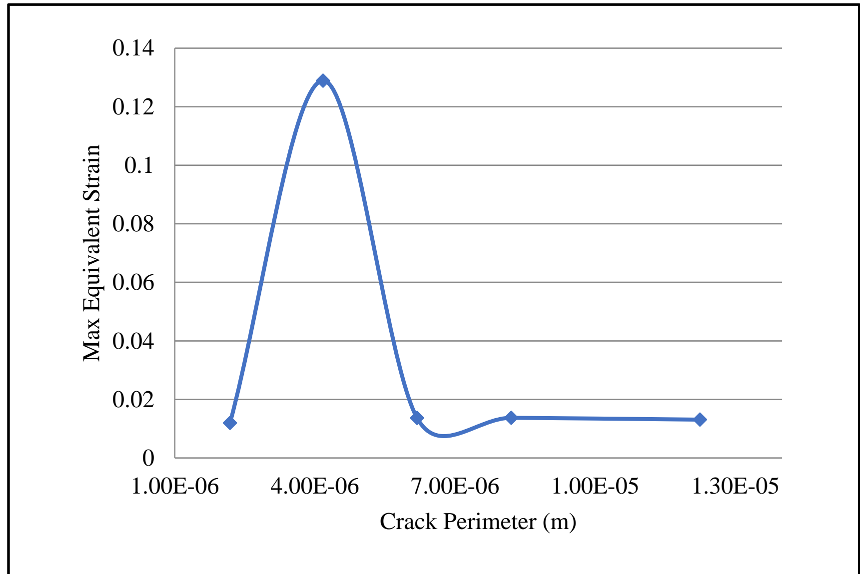

FIGURE 4-19 MAX EQUIVALENT STRAIN VS CRACK PERIMETER (MM)

The impact of the thermal load on J-integral for cracks on the TSV surface is also studied. The upper limit of thermal cycling has been changed and varied to create a new profile as shown in figure 4-19. The maximum or upper-temperature limit was taken from 105°C to 205°C with an interval of 20°C, therefore 6 different thermal cycling profile was created.

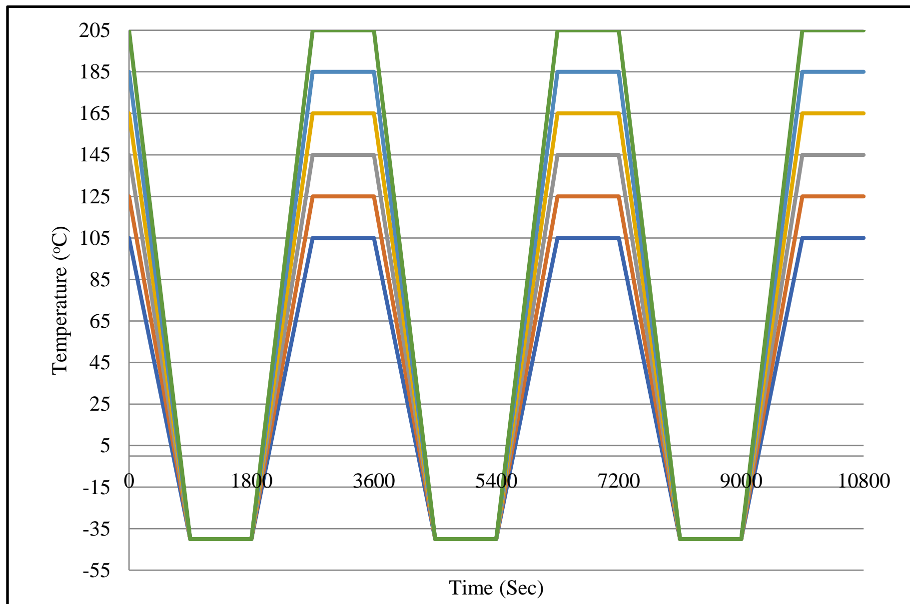

FIGURE 4-20 DIFFERENT THERMAL CYCLE PROFILE

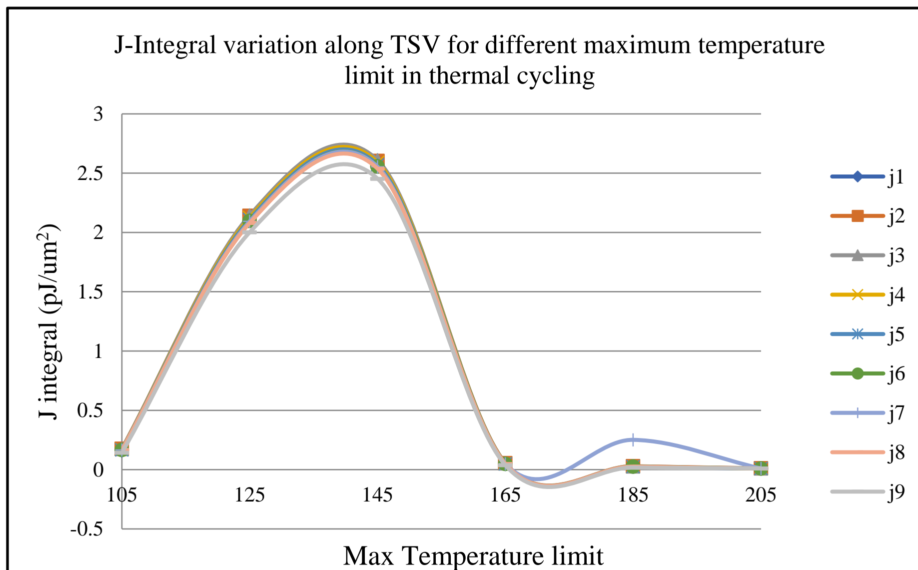

FIGURE 4-21 J-INTEGRAL VARIATION WITH INCREASING THERMAL LOAD

4.7.2.1 Effect of Underfill and Mold Material on Solder Joint Reliability

Underfill plays a very important role on the thermo-mechanical reliability of electronic components. Underfill is used to support solder interconnects as well as protect them from environmental conditions. Package structure kept identical and underfill with different stiffnesses is used to understand the effect of different material properties of underfill on the reliability and how could we improve reliability by not making any significant changes in packaging components. Using soft underfill showed significant warpage in the package than stiff underfill material. Material Properties of three types of underfill used are listed in Table 4-2.

TABLE 4-3 MATERIAL PROPERTIES FOR THREE MODELS

Underfill	A	B	C
Young's Modulus	3	6	9
CTE (ppm/°C)	20	25	30

Figure 4-20 shows the comparison of total strain of all three types of underfill. From this, we can say that soft underfill plays important role in resisting strain in solder. The underfill is the material which is used in between chip and substrate

and it support the package. So, properties of underfill should be in between the PCB and chip. At that point, we can see a significant change in results.

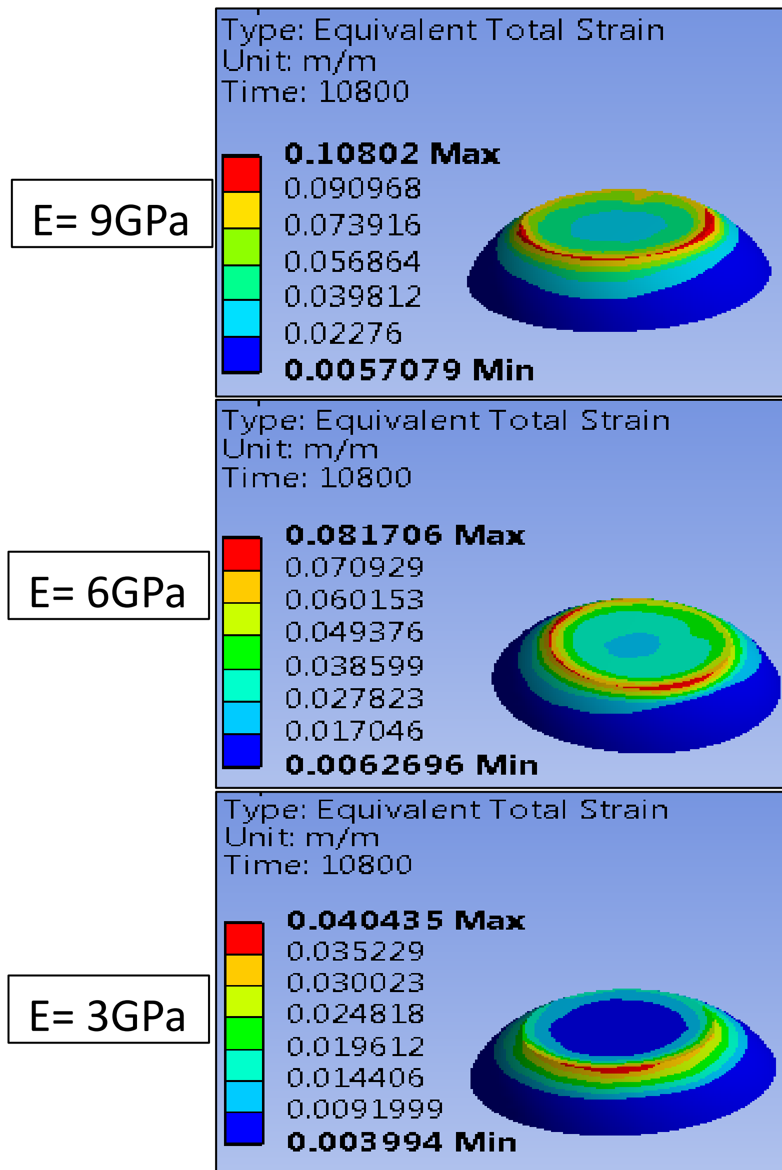

FIGURE 4-22 TOTAL STRAIN COMPARISON BETWEEN THREE TYPES OF UNDERFILL

Table 4-4 shows the results comparison between all three models and which parameter is affected by change in underfill properties. Use of underfill also reduced the delamination at the TSV interface and improved SJR as PW is decreased.

TABLE 4-4 RESULTS COMPARING J, PW, AND TOTAL STRAIN

Effect of Underfill Stiffness			
E (GPa)	J(pJ/um^2)	PW(MPa)	Total Strain
9	0.015	0.1999	0.108
6	0.008	0.182	0.082
3	0.0074	0.1565	0.04044

The peeling stress at the top surface, which is transferred into the silicon die via solder UBM and pad structure and is harmful to the silicon passivation layer and to

the BEOL low-k interconnects inside the chip. However, the stress level in the solder bumps can be reduced when the underfill material is incorporated [62].

4.7.2.2 INTEGRAL VARIATION DUE TO SEMIELLIPTICAL CRACK AT BEOL

BEOL reliability is a challenging part in today's microelectronic manufacturing industries. The bonding process of IC undergoes a large plastic deformation which requires a special attention from the modeling point of view.

FIGURE 4-23 BEOL DETAIL

The low-k material in BEOL is the mechanically weak but are important for reducing the electrical losses. In place of gold wire bonding, copper wire bondings are used. As copper has a higher yield stress than gold [73], higher forces act on a mechanical weak structure. The thermomechanical reliability of BEOL is as important as solder bumps, TSVs, and other components. The stability of the J-

integral value obtained from the FEA is important to avoid a misunderstanding of the cracking energy. To study the impact of thermal load on crack at different layers of dielectric, BEOL stack up is incorporated. In sub-model shown in figure 4-24 & 4-25, 11 layers consisting of 5 metal layer and 6 dielectric layers alternately stacked on each other. Each layer is 1.4micron in thickness. Similarly, to TSV, the same type of study has been done here. Leveraging finite element modeling, we have modeled semi-elliptical crack on a different dielectric layer of BEOL. The study will show the variation of J-integral of crack from the top dielectric layer to the bottom layer. The sub-modeling technique is used for analysis and fracture tool for modeling crack. Figure 4-24 shows all sub-models used and the cut boundary condition imported to it. [73]

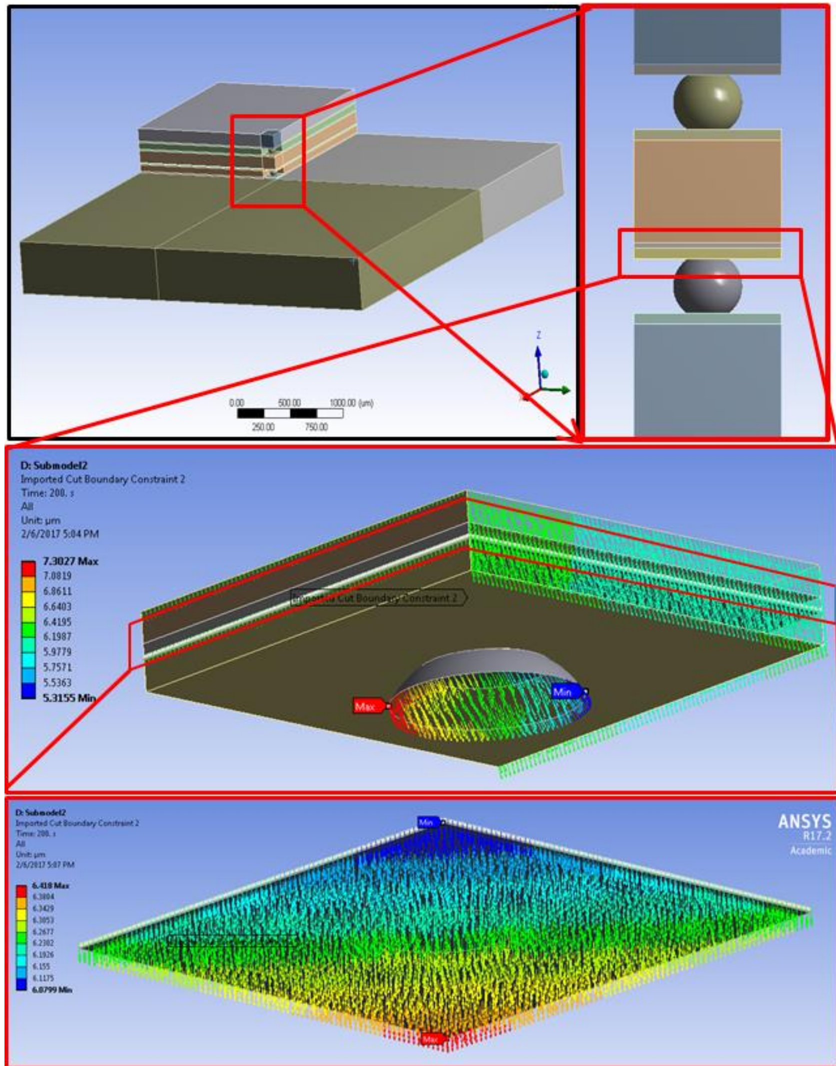

FIGURE 4-24 SUB-MODELING TECHNIQUE & CUT BOUNDARY CONDITION

Continuation of scale miniaturization of electronic components in semiconductor industries for improved device performance, multi-level interconnects of Copper/low-k stacked structures, adopting the damascene module, are being introduced into the next generation IC chip in order to meet the requirements of reducing high RC delay. The BEOL is comprised of copper and low-k dielectric stacked structures as shown in figure 4-25 which are regarded as a composition of Multi- thin films. The low-k material has a lower elastic modulus and poor adhesion compared to another dielectric material. When temperature loads are applied, there is a possibility of crack growth due to a mismatch in coefficient of thermal expansion (CTE) and the elastic modulus of the layers. [74]

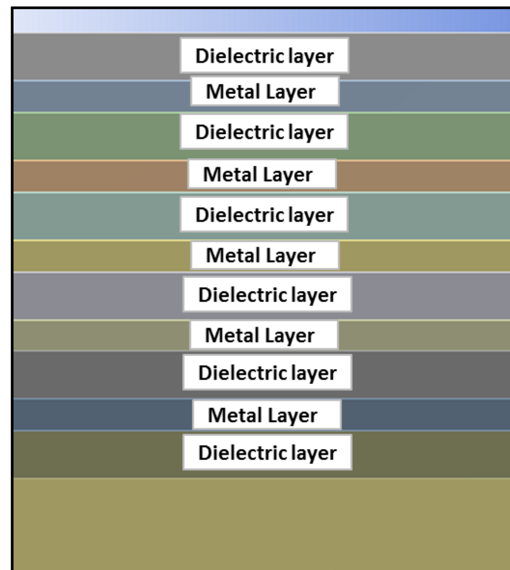

FIGURE 4-25 BEOL STACK-UP

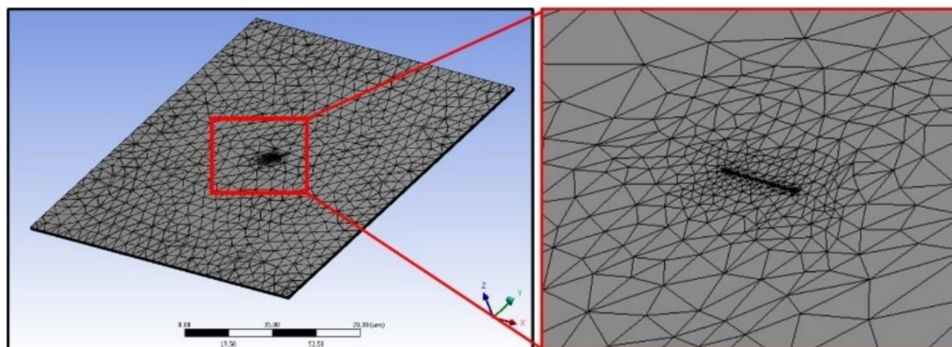

FIGURE 4-26 MODELING CRACK AT CENTER OF DIELECTRIC LAYER

Figure 4-23 shows the mesh modeling of the crack size on the top dielectric layer of BEOL. Similar crack location and size are done for other layers too. A semi-elliptical crack with 0.5micron major axis and 0.1micron minor axis was modeled. Further, the thermal load applied to the model is the reflow condition starting from 200°C to room temperature. Each dielectric layer shows a significant reaction to the thermal load from each other. Figure 4-27 shows the stress distribution on 4 different layers. It can be seen from the contour that the bottom dielectric layer (i.e. dielectric layer 6) shows minimum stress and dielectric layer 5 shows maximum.

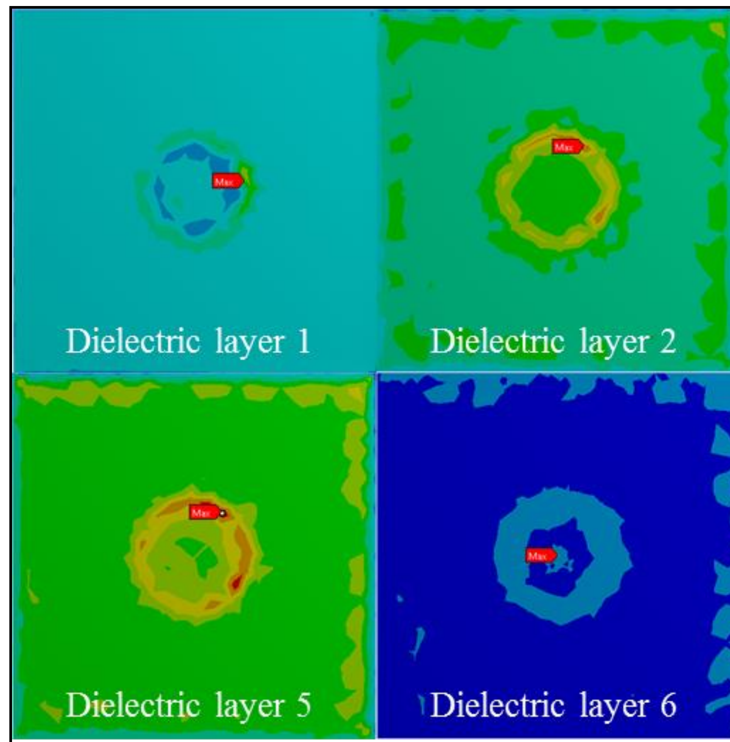

FIGURE 4-27 EQUIVALENT STRESS DISTRIBUTION

The j integral value has been noted for a crack at different layer and the variation is shown in figure 4-28. Crack at Low-k electric layer 1 show the maximum j integral value due to a CTE & E mismatch between dielectric and silicon die. The value increases as we go down to second last layer from the bottom low-k layer. Minimum j integral value has been noted for the bottom dielectric layer.

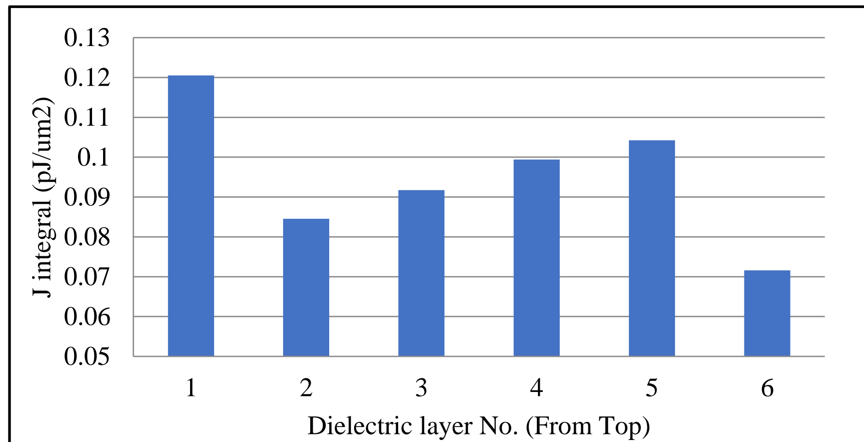

FIGURE 4-28 J-INTEGRAL FOR CRACK AT DIELECTRIC LAYERS

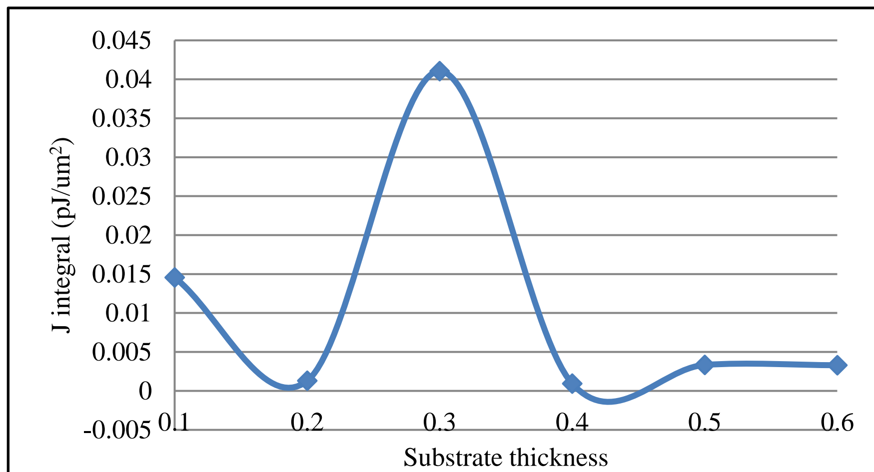

FIGURE 4-29 J-INTEGRAL VS SUBSTRATE THICKNESS

Further study includes the substrate thickness optimization and identifying the best dimension against crack propagation. We increased the substrate thickness from 0.1mm to 0.6mm by an interval of 0.1mm and noted j integral of crack at top

dielectric for each dimension. The plot between J-integral and substrate thickness is shown in figure 4-29. The J-integral value shows maximum for 0.3mm substrate thickness and after 0.4 mm substrate thickness, it gets stabilized. From the analysis, we can conclude that the substrate thickness of 0.4mm is the best fit against crack propagation at BEOL.

4.8 CONCLUSION

The package, PCB, and crack modeling were done successfully. The variation of radial cracks or crack propagation along the TSV Cu core and on low-k dielectric layers of BEOL has been successfully studied. The cut boundary condition from the global model and sub model were used for simulation. The variation of J-integral and other parameters were studied for a different combination of substrate and top die thickness. The J-integral value is used in calculating the strain energy release rate per unit fracture surface area and is determined with respect to crack size. Six different type of thermal cycle profiles were created, and variation of J-integral value has been studied. The variation of crack size has also been successfully leveraged to investigate its effect on stress and strain distribution and found that it was directly proportional to J- integral, whereas the relation between J-integral and top die-substrate thickness shows an inversely proportional relational property up to a certain limit of thickness. For 0.1mm die thickness, 0.3mm

substrate thickness is most reliable against crack propagation and for 0.4mm die thickness, 0.4mm substrate thickness is most reliable. This combination creates a zone of the reliable area of substrate thickness from 0.3mm to 0.4mm. In further, the impact of the reflow condition on crack at different low-k dielectric layer was studied. The relation between a substrate thickness and j integral of crack at a dielectric layer is obtained. This study is important for optimizing the package geometry under different loading condition and understanding of crack propagation depending on structural integrity. Different crack size at a different location can be studied as per requirement following the same concept.

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