DESIGN OF A CLC TESTBED TO STUDY HIGH VOLTAGE CAPACITORS

by

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THESIS

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ABSTRACT

Design of a CLC Testbed to Study High Voltage Capacitors

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Pulsed power systems rely on the interconnection of several unique stages for successful implementation. These stages can include, but are not limited to a prime power source, power conditioning circuit, intermediate energy storage, pulsed forming network, and the load. There are many possible intermediate energy storage devices that can be considered, two of which are inductive and capacitive. There are many advantages and disadvantages that each offer. Inductive energy storage is several times more energy dense than capacitive energy storage but most of the time, an opening switch is required to transfer the energy to the load and those are difficult to implement, especially repetitively. Capacitive energy storage is more power dense and often requires a closing switch for energy transfer which are easier to implement. Though inductive energy storage is occasionally used, capacitive energy storage is typically used more often.

Applications demanding voltages as high as 100 kV will often rely on film-type capacitors. In order to charge and discharge them repetitively at high frequency, they must be able to be charged and discharged at high current. High rate discharge is typically factored into the design, but repetitive high rate recharge is not. This brings into question how these types of capacitors will perform, age, and eventually fail when they are charged,

discharged, recharged, and discharged again rapidly at high current. Furthermore, the impact an elevated ambient temperature has on them is also of interest. To answer these questions, a capacitive-inductive-capacitive (CLC) circuit has been assembled and commissioned. In the circuit, the first capacitive element serves as a primary storage device and the second capacitor acts as the capacitor under test. The inductive elements are used to shape the recharge pulse. The capacitor under test is discharged into a low impedance water load, rapidly recharged from the primary storage capacitor, and then discharged again. The capacitor under test is housed in a thermal chamber so the ambient temperature can be adjusted as needed.

In this report, a brief introduction to capacitive energy storage, the design of the testbed, the construction of the testbed, some lessons learned, and some preliminary results will be documented.

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CHAPTER I

INTRODUCTION

Successful deployment of pulsed power systems relies on the interaction of several electronic stages that include but are not limited to the prime power, power regulation, intermediate energy storage, pulsed forming, and the load. There are a few different intermediate energy storage options, two of which are capacitive and inductive, each of which has advantages and disadvantages. Capacitive energy storage has high power density but lacks energy density. Inductive storage has higher energy density than capacitive energy storage, but it is difficult to implement practically due to the need for an opening switch in most cases. Interrupting the high current that many pulsed power systems demand is challenging, and repetitive operation is incredibly difficult to achieve using inductive energy storage. Because capacitive energy storage typically relies on closing switches, it is more often used, even though repetitive rate closing switches still introduce significant challenges.

There are different types of capacitors that are used in in high voltage pulsed power applications with ceramic, non-metalized film, and metalized film being the ones most commonly employed. Charge voltages in the 100s of kV have been achieved. Metallic and plastic casings are available with the type having a large impact on the capacitor's energy and power density, respectively. The demand for repetitive rate operation in pulsed power systems increases the stress of all the components significantly and large advances have been made in recent decades to make this mode of operation achievable using capacitive storage.

Though capacitive energy storage technology is quite mature, there are still many technical hurdles to overcome. The energy density of capacitors has increased dramatically over the years and this has made the compact pulsed power systems more feasible than ever. Because compact pulsed power devices will need to be fielded in challenging environmental conditions, it is critical that it be understood how film capacitors performance, ageing, and failure are affected in different environmental conditions. Though pulsed power capacitors are designed to supply high repetitive rate current, there is a need to study how they age, perform, and fail when they are recharged at high current rates between discharges in variable environmental conditions. The intent of the work performed here is to design, build, and commission a testbed that can be used in the future to study high voltage pulsed power capacitors at high rates of charge and discharge in a controlled ambient condition. It should be noted that some performance measurements have been made but no aging study will be documented here. The design of the testbed and some preliminary results obtained will be presented.

CHAPTER II

BACKGROUND

As highlighted in the introduction, capacitors play a pivotal role in pulsed power systems. Advances made in recent decades have made repetitive, compact pulsed power systems achievable and there is always a desire to understand them fundamentally and improve them technologically. In this background section, a light background on capacitor technology, as it applies to pulsed power systems will be described.

2.1 Pulsed Power Technology

Though it is largely assumed that reader is familiar with pulsed power technology, it never hurts to provide a brief background. The aim of pulsed power is to store energy over a moderately long period of time at modest power levels into some form of energy storage technology and then to release that energy quickly in the form a pulse(s) with a high peak to average power ratio. Of course, what one user considers a moderately long period of time, a moderate power level, or a high peak to average power ratio, may be very different than what another user considers and as a result there is no easy way to define those values and apply them to all systems. The graphic of Figure 1 can be considered as a reference but again should not be considered to fall within the ranges of all types of systems.

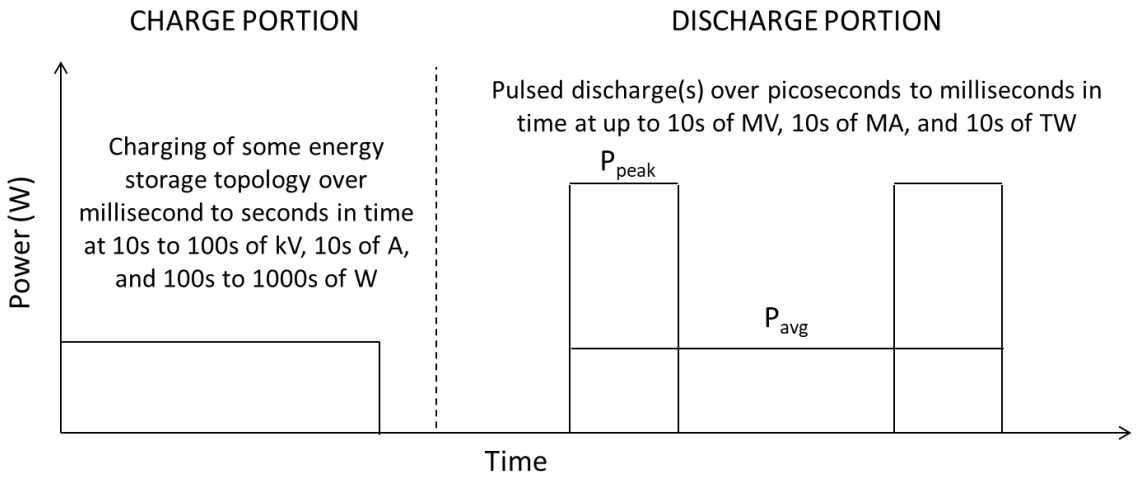

Figure 1: Simple illustration describing the storing up of energy over a long period of time and then compressing that energy into an output pulse that has a high peak to average current ratio.

What is shown in Figure 1 can be thought of simply as pulse compression and that compression can result in very high-power amplification. As a simple example, if one Joule of energy is stored using a power supply capable of supplying only 1 W of power and then that energy is released into a low impedance load within 1 μs, a megawatt of instantaneous power could be supplied. This results in a power amplification of 10^6 and this could never be achieved using a power supply of the same size and weight as the one used to initially charge the capacitor. Without an intermediate energy storage device that can store the energy and then release it quickly, this type of amplification is not achievable, and, in most systems, there are several electronic stages that must work together to make this possible. These include but are not limited to the prime power supply, intermediate energy storage, switch, pulsed forming network, and the load. A simple graphic is shown in Figure 2. Like

Figure 1, the graphic in Figure 2 is certainly not representative of all pulsed power systems but it is of many.

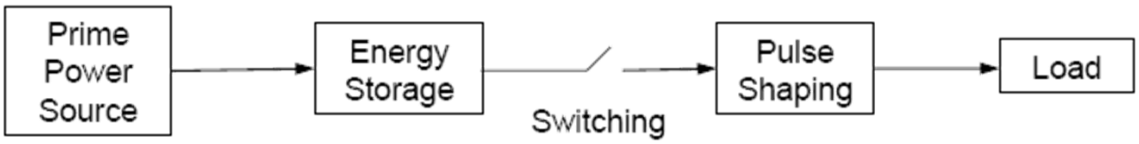

Figure 2: Simple graphic describing the interconnection of electronic stages required to make many pulsed power systems possible.

Since most of the pulsed power research and development (R&D) has been performed in a laboratory, the prime power supply is typically a grid tied power supply that converts AC mains to DC charge power. This is not always the case of course and as systems move away from the laboratory, the need for mobile prime power sources becomes a critical requirement. Alternative prime power sources include electrochemical batteries, fossil fuel driven electrical generator systems, and explosives, among others.

Storing energy, which is a focus of the work performed here, can be achieved many ways. A few include capacitive, inductive, and mechanical (flywheels) energy storage. Switching the energy out of the energy storage is often one of the hardest objectives to achieve. When capacitive energy storage is used, typically a closing switch is required, and this is usually easier than trying to get an opening switch to perform reliably. Closing switches that have been successfully demonstrated include, but are not limited to spark-gaps, ignitrons, thyratrons, thyristors, klystrons, vacuum contactors, mechanical contactors, and insulated gate bipolar junction transistors (IGBTs). When inductive energy storage is used, opening switches are typically required and those are much harder to

implement, especially repetitively, than closing switches. Since capacitive energy storage typically relies on closing switches and inductive energy storage relies on opening switches, capacitive energy storage is more often used when possible. Opening switches that have been developed include the plasma erosion opening switch (PEOS) [1], zero current commutating gas and solid-state switches, traditional fuses, or exploding opening switches, among a few others.

Pulsed forming is achieved a few different ways. One way involves using a combination of capacitive and inductive elements connected in a series/parallel network to form a resonant pulse. Examples of these would be Guilliman pulse forming networks. Another way of shaping the pulse involves using transmission lines and relying on transit times and switching to shape the pulse.

There are too many different types of pulsed power loads to go into any real depth here. Simply put there are many different loads that are designed for defense and civilian applications. A few defense applications include radar, electromagnetic pulse simulation and testing, nuclear fusion, nuclear radiation effects, electromagnetic acceleration, high power microwave generation, and compact and explosive flux compression generator systems. A few example civilian applications include radar, medical imaging, camera flash systems, magnetic forming of metals, materials and surface treatment, environmental gas breakdown, liquid shock wave studies, and algae decomposition.

2.2 Intermediate Energy Storage Devices

As highlighted a few times already, pulsed power relies on the slow storage of energy and then the quick release of that energy in a high peak to average power pulse.

Storage of energy is achieved in many ways with capacitive and inductive being among the most commonly used. Inductive energy systems are theoretically 100 times [2] more energy dense than capacitive energy storage systems, as seen in Figure 3. Despite being more energy dense, they are not as power dense as capacitors and the requirement of an opening switch to create high voltages is difficult.

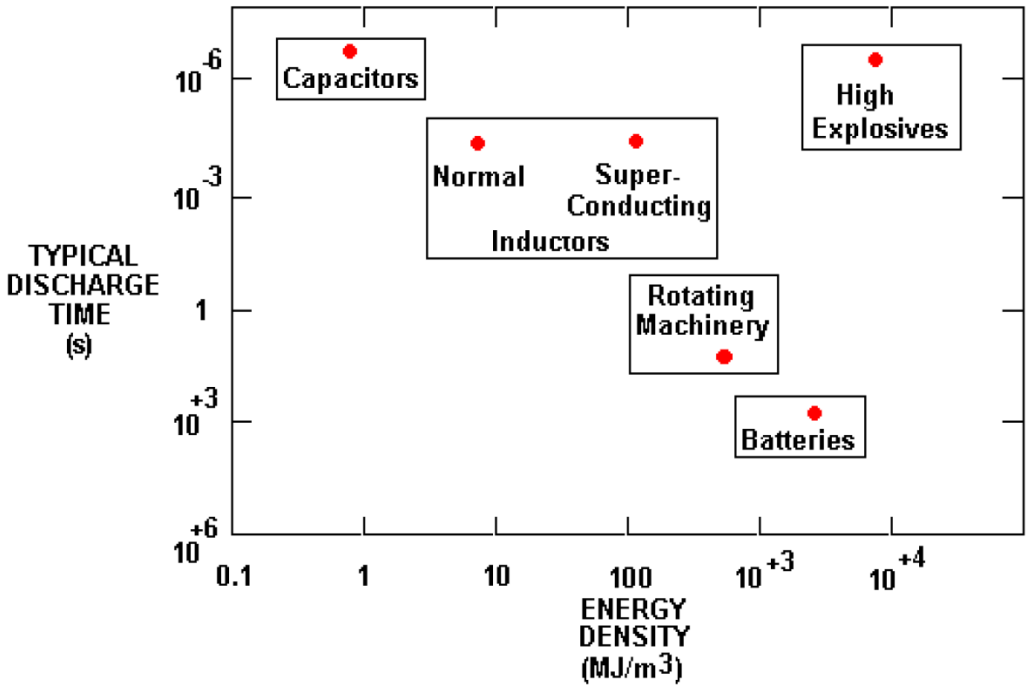

Figure 3: Ragone chart plotting the power and energy density of multiple energy storage technologies [3]. Of interest here is capacitive and inductive energy storage, respectively

2.3 Inductive Energy Storage

In its simplest form, an inductor is nothing more than a wire and, in any system, there are always wires that are used to interconnect devices introducing stray inductance. In most pulsed power applications, there is a strong desire to minimize stray inductance as it introduces loss and can slow down pulse rise times. Two wire inductors and coaxial

inductors are good examples of those that don't store a great deal of energy but can introduce inductance into a system. When it is beneficial to store energy in a magnetic field, higher value inductors are assembled in the form of solenoids and torroids, as shown in Figure 4.

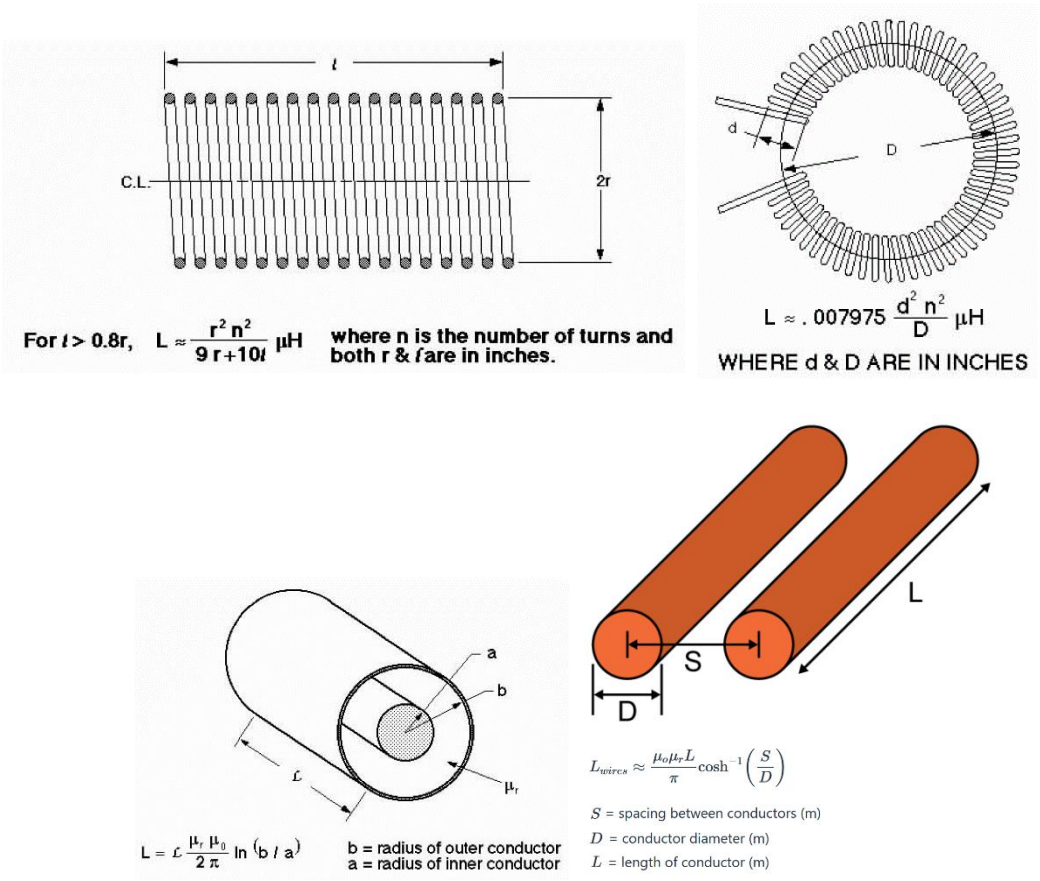

Figure 4: Examples of solenoidal (upper left) [3] and toroidal inductors (upper right) [3], coaxial (lower left) [3], and parallel wire (lower right) [7] inductors.

If they are wrapped around non-permeable cores, then the magnetic flux density is low, and they are unable to store as much as they are when magnetic cores are used. The choice of a magnetic core is critical to the successful implementation of inductive energy storage as the hysteresis curve of the material defines the ability to store energy in the core

or saturate it. The relative permeability constant, μ_r, of the core along with the shape of the hysteresis curve defines the materials ability to store magnetic flux. It is beyond the scope of this work to discuss it in depth but often an inductor can be used as a switch when the field is taken to the saturation level, causing the magnetic field to collapse quickly.

Since inductors are just wire carrying current, they can be quite resistive and therefore lossy. If the frequency of the system is high, then the skin effect can play a very large role in how the inductor is used. It is critical that the wire diameter be sized properly so that it can carry the electrical action and not fuse due to thermal melting. Litz wire, which is essentially a bundle of smaller insulated wires has been used to increase the effective surface area and reduce resistive and skin effect losses. Another factor to consider is the magnetic pressure induced when high currents are carried, seen in a few of the graphics in Figure 4. When the magnetic pressures are high, it is critical that the inductors be built structurally strong to prevent the forces from crushing them mechanically. Core material, structural fiber glass impregnated epoxies, and other enclosures must be carefully designed and chosen to withstand these forces and there are of course limits to what can be achieved. The magnetic pressure also affects the types of materials that can be used, and care must be taken to consider that when designing an energy storage inductor.

Conversion of energy in the inductor's magnetic field into a high pulsed voltage source is achieved by interrupting the flow of current using an opening switch. An example of a very simple inductive energy storage circuit is shown in Figure 5. In this circuit, current is passed through the inductor from the primary current source with the opening switch (S_o) initially closed. Once the magnetic field is established, S_o is opened interrupting the

flow of current inducing a voltage spike according to equation 2.1. When the voltage is induced, the closing switch (S_C) is closed transferring the energy into the load.

$$V = L\left(\frac{dI}{dt}\right) \quad \text{Eq 2.1}$$

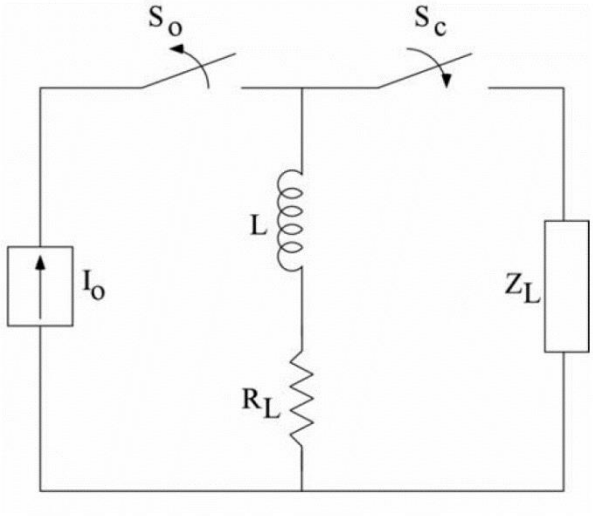

Figure 5: Simple inductive energy storage circuit

Advancements in semi-conductive opening switches, such as gate turn-off thyristors (GTOs), integrated gate-commutated thyristors (IGCTs), and insulated-gate bipolar transistors (IGBTs) has helped to make inductive energy storage more feasible. These types of switches are available and can briefly operate in the megawatt range but an array of them in parallel is needed to increase that further [5]. Timing of getting all the switches to open simultaneously and share the current is difficult at best and is still a hot topic of research. Protection of the switches is especially important and even when successful operation is achieved, the switch arrays quickly make the system expensive, heavier, and bulkier.

In order to relieve stress on opening switches, many researchers have implemented various circuit topologies to lower the requirements of the opening switch. The Institute for Advanced Technology (IAT) proposed a slow transfer of energy through capacitive hybrid (STRETCH) meat grinder circuit [6]. An implementation of this circuit topology is shown in Figure 6. As shown in the figure, IAT added a parallel capacitor to a traditional meat grinder circuit, which is an inductive current multiplication circuit. When the flow of current in the inductor L_1 is interrupted using an IGCT, all the magnetic flux initially contained within L_1 and L_2 is compressed into the L_2 resulting in current amplification. With the added capacitor, the circuit is still able to produce high current multiplication, but it has a slightly lower energy density compared to the purely inductive meat grinder. The purpose of the capacitor is to limit the voltage the opening switch sees due to imperfect coupling between inductors and induced back electromotive force (emf) that gets reflected from the load. Though this demonstrates a great example of how an opening switch can be deployed, later work by IAT found that in order to scale up the current, additional opening switches have to be placed in parallel and while possible, it requires all the switches to open with minimal jitter which is very difficult in practice. [6].

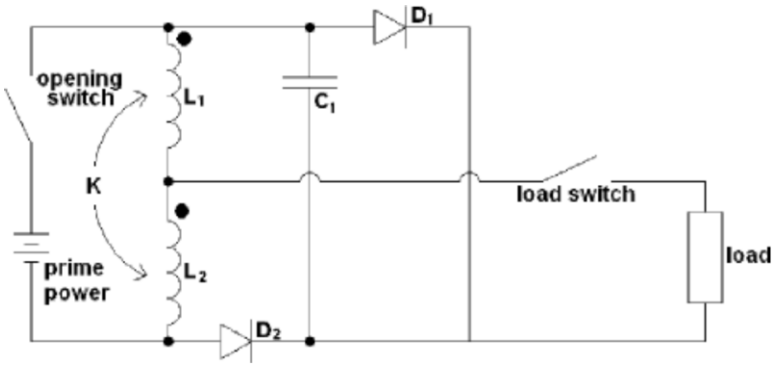

Figure 6: Single stage STRETCH meat grinder circuit [6]

Another opening switch topology that is employed is an XRAM circuit, which is shown in Figure 7. This was first proposed by Werner Koch at Marx' High Voltage Institute at Brunswick Technical University in 1967 [7]. An XRAM can be thought as an inductive counterpart to a MARX circuit. A MARX is fundamentally a voltage multiplication circuit that switches charged parallel connected capacitors into series connected capacitors. This allows the output voltage to be *n* (number of capacitors) times the initial parallel capacitor charge voltage.

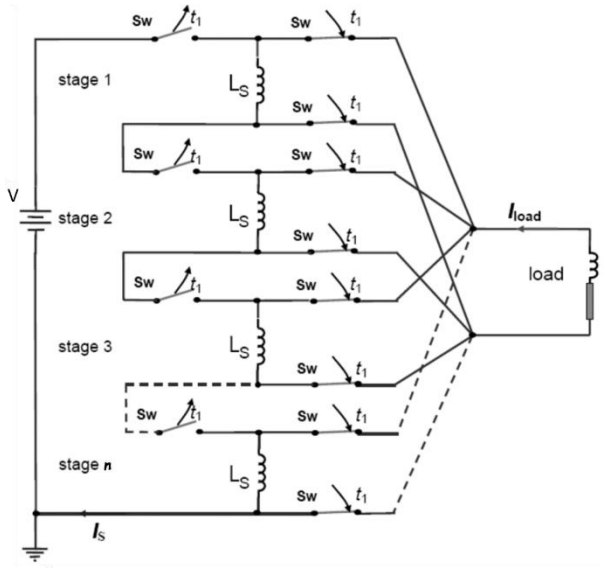

Figure 7: An n-stage XRAM circuit [7]

The XRAM circuit uses inductors that are energized in series from a current source and then discharged in parallel for current multiplication. At the French Institute of Saint Loius, Philipp Dedié and others developed a technique called the Inverse Current Commutation with Semiconductor devices (ICCOS), which is based on the counter current commutation principle. The ICCOS was applied to a high-powered thyristor opening switch, capable of interrupting currents up to 28kA. Their research led them to create an

eight-stage XRAM generator with an energy density of 60 MJ/m^3, a power output of 1.2 MW with each stage contributing a max of 4 kA for five seconds and capable of delivering a total of 32 kA to the load [7].

2.4 Capacitive Energy Storage

Capacitors are a more widely used and manageable form of energy storage. They can be charged to high voltage using conventional power supplies and are able to act as both high voltage and high current sources. In their simplest form, a capacitor is two metal plates separated by a dielectric material, as shown in Figure 8. When potential is applied across the plates, charge is separated establishing the electric field across the dielectric. The dielectric can be air or any other non-conductive material, each of which will have its own relative permittivity value, ε_r, that defines the ability of the material to store energy in an electric field. The dielectric breakdown strength of the dielectric is a critical part of the system that must be higher than the charge voltage to prevent the charge from conducting across it.

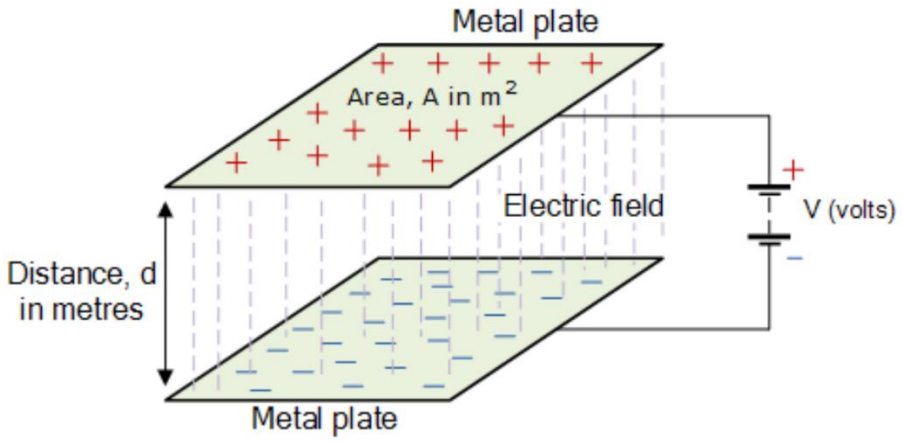

Figure 8: Simple schematic of a parallel plate capacitor [8]

There are many equations that govern the capacitor's capacitance, storage of energy, potential across the plates, and the current sourced in and out, respectively. A few of those are given below in equations 2.2 – 2.4, respectively. From these equations it is understood that the rate of change in the voltage is what drives the current the capacitor supplies. The capacitor voltage drops quickly when loaded into a low impedance load resulting a high current pulse. Because there is a voltage initially established in a capacitor during charge, a closing switch is used to dump the energy from the capacitor into the load. A very simple circuit describing this is shown in Figure 9. The capacitor is initially charged using the voltage source V_o up to the desired level. Once it is charged, the closing switch (S_c) is closed allowing current to flow to the load. Typical closing switches used in these applications are spark gaps, ignitrons, klystrons, thyratrons, thyristors, IGBTs, and mechanical switches among others. There will not be more detail given here about these, but the reader is encouraged to read more about these as needed. The construction of most capacitive energy storage circuits is more complicated than that shown in Figure 9 but it serves as a simple reference.

$$C = \frac{Q}{V} = \frac{\varepsilon_o \varepsilon_r * A}{d} \qquad \text{Eq 2.2}$$

$$V(t) = \frac{1}{C}\int i(t)dt + V(0) \qquad \text{Eq 2.3}$$

$$i(t) = C\frac{dv}{dt} \qquad \text{Eq 2.4}$$

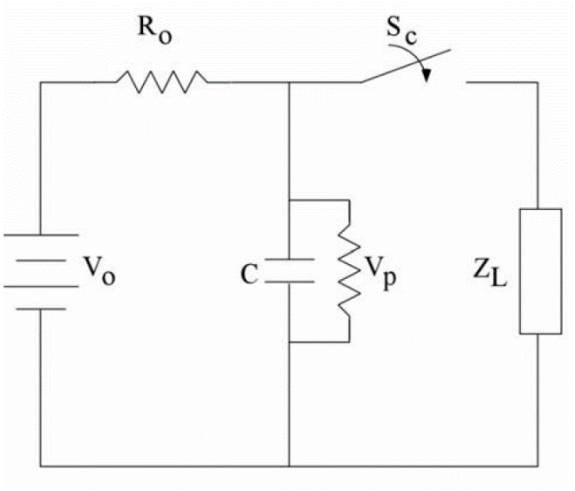

Figure 9: Simple capacitive energy storage circuit

2.5 Types of Capacitors used in Pulsed Power Applications

Over the last several decades, capacitor technologies developed for pulsed power applications have advanced considerably in terms of their performance, energy and power density, and reliability. Film-type capacitors have been the dominate choice for capacitive energy storage in pulsed power systems, due to the ability of metallized film capacitors to self-heal. Ceramic capacitors have also been employed in pulsed power systems, but due to their low breakdown strength, they are not as widely adopted.

2.5.1 Metalized Film Capacitors

As mentioned earlier, a capacitor is composed of two metal plates, or electrodes, with a dielectric separating the two. In film capacitors, metal foils are used as the electrodes and either Kraft paper impregnated with a suitable insulating fluid, or a polymer, such as polypropylene are used as the dielectric [9]. A general layout of a film capacitor is shown in Figure 10. Typically, the foil and dielectric are assembled flat and then get ‘rolled up’

together, where the foil is extended out and terminated by either soldering or welding the edges, forming the electrodes.

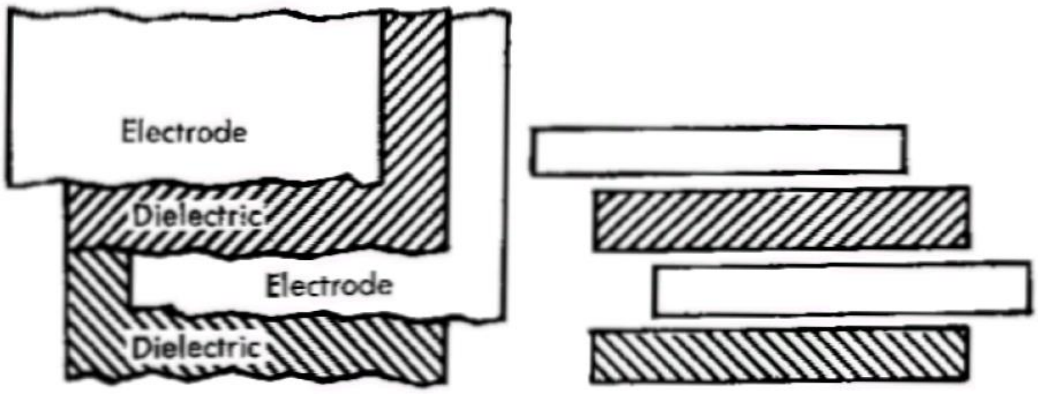

Figure 10: A general structure of a film capacitor [4]

These types of capacitors exhibit the ability to self-heal, when a breakdown occurs in the dielectric. Self-healing is the ability to recover from a small-scale, localized breakdown event inside the capacitor. This self-healing or clearing happens when defects in the film of the capacitor are present, which causes a breakdown to occur when operating under a high electric field [11]. This causes centralized heating and the metalized electrode to be vaporized at the site of the defect. The hole left in the electrode that is wider than the hole in the dielectric material it is deposited on leaving a stable insulation barrier in place that allows the capacitor to remain operational with a slightly lower capacitance after each clearing event. When clearing happens too frequently, the capacitor can exhibit catastrophic failure or possible a fire. The catastrophic failure is essentially the melting of the dielectric. In most cases the end of life is indicated when the capacitance has decreased by 5%.

Metalized film capacitors are most commonly composed of Kraft paper, polypropylene, or a polyester substrate for the dielectric. The electrode is either aluminum, zinc, or some other type of alloy that is sprayed onto the dielectric. A general structure of the metallized film capacitor is shown in Figure 11.

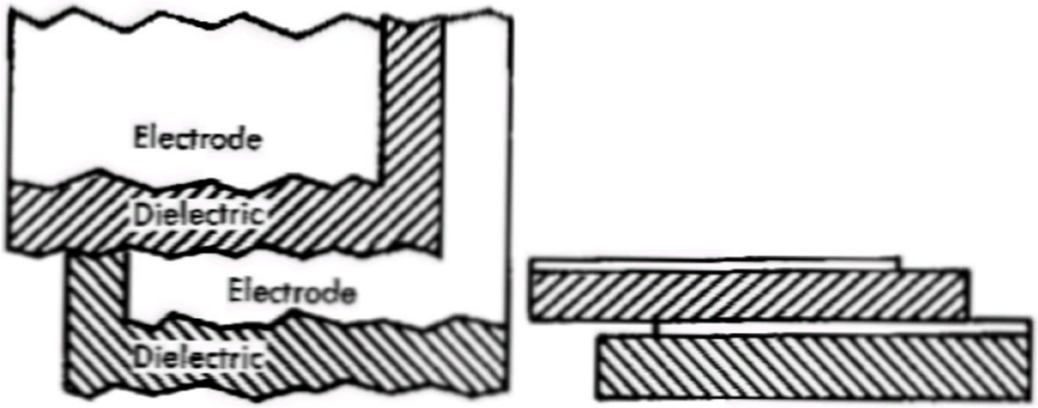

Figure 11: A general structure of a metallized film capacitor [3]

In more recent metalized film capacitors, a self-fusing technique has been used to extend the graceful aging. Self-fusing is another form of self-healing, which utilizes the metallized electrodes as segmented patterns that localize the self-healed area by fusible links as shown in Figure 12 [10].

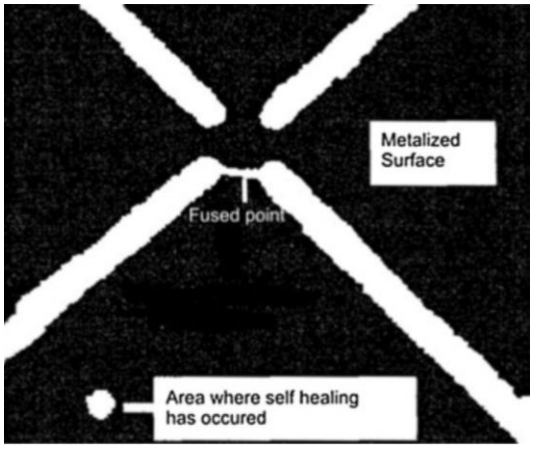

Figure 12: An illustration of the process of self-fusing [10]

Even though self-healing extends the lifetime of these capacitors, it has been shown that repetitive rate operation can impact lifetime significantly. A study conducted by Hua Li and others at State Key Laboratory of Advanced Electromagnetic Engineering and Technology, showed that the lifetime of metalized film capacitors operating at 5 kV had longer lifetimes as the repetition rate increased. A typical waveform of their study is shown in the Figure 13. In their experimental setup, the capacitor under test was charged to a pre-set voltage using a 30 kJ/s repetitive capacitor charging power source. Once charged, the capacitor was discharged into a load through a thyristor that was paralleled with a diode for freewheeling current.

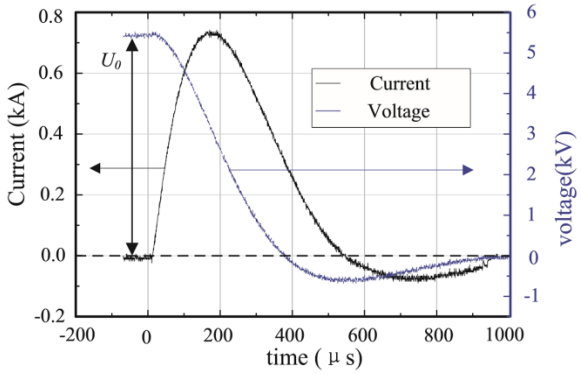

Figure 13: Typical waveform from the study conducted by Hua Li and others at State Key Laboratory of Advanced Electromagnetic Engineering and Technology [11]

They studied frequencies ranging from 0.08 Hz to 10 H and proposed that the increase in lifetime at higher rates was due to the self-healing induced gas that was more concentrated at higher rate than at lower ones. At lower rates the gas was able to disperse into the windings of the capacitor which would result in more defects. A table of their findings are displayed in Table 1.

Table 1: Lifetime results of metalized film capacitors. The study was conducted Hua Li and others at State Key Laboratory of Advanced Electromagnetic Engineering and Technology [11]

Repetitive rate/Hz	0.08	0.50	1	2	5	10
Charging time/s	10	1.6	0.80	0.40	0.16	0.08
Hold time/s	1	0.2	0.10	0.05	0.02	0.01
Interval time/s	1	0.2	0. 10	0.05	0.02	0.01
Lifetime/shot	4988	6849	8919	10553	12982	12707
Relative standard deviation	10.00%	4.74%	12.37%	5.40%	13.35%	6.68%

To study the lifetime and performance of a capacitor for pulsed power applications, the peak current needs to be accounted for. A study conducted by Guido Picci and Maurizio Rabuffi, found that pulses having high peaks of current and short duration produced the same degradation level in the capacitor as pulses having low peaks of current, but long duration [12]. They classified a short pulse duration as 20 μs to 40 μs, and a long duration as 200 μs to 300 μs. They studied over 300 capacitors that were divided into three separate categories as shown in Table 2.

Table 2: Three categories of the types of capacitors used in the experiment conducted by Guido Picci and Maurizio Rabuffi [12]

Capacitors type	Type of metallization
Cylindrical PP film capacitors	Al - Zn
Cylindrical PP film capacitors	Al
Flat PP film Capacitors	Al - Zn

All 300 capacitors were tested to 5,000 shots with two different circuit topologies. The exact topologies of the circuit weren't given, but they stated that a square wave generator was employed to produce an aperiodic pulse and an RLC circuit was designed to

produce an underdamped response. The typical waveforms of each circuit are shown in Figure 14. Both circuits were stated to be able to reach peak currents of 7000 A, 8000 A, and sometimes 10000 A. The study showed no difference between the affects that the two waveforms had on the capacitor's performance or degradation.

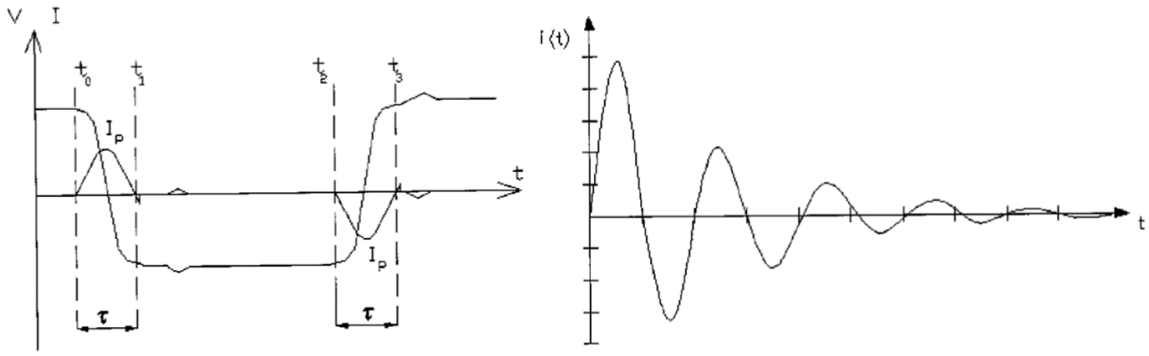

Figure 14: The left graph shows the response of the waveform generator used to produce an aperiodic pulse. The right graph shows the underdamped response of the RLC circuit [12]

The study showed that the thermal and mechanical stresses caused deterioration of the capacitor regardless of the duration and peak of the current pulse. They showed that the rise of temperature on the capacitor's windings would cause the dielectric to shrink, which reduces the capacitor's performance. The shrinkage results in the dielectric applying unwanted mechanical stresses on the capacitor's end connections.

2.5.2 Ceramic Capacitors

There are many kinds of ceramic materials that are suitable for producing high voltage and high energy dense capacitors. High voltage ceramic capacitors have a higher energy density than film capacitors, primarily due to having a significantly higher dielectric constant, ε_r or sometimes denoted as K, as shown in Table 3. As, shown in the table, high

voltage ceramic capacitors have a significantly lower voltage breakdown point than film capacitors limiting their applications in high voltage applications. Unlike metalized film capacitors, ceramic capacitors do not exhibit self-healing. Instead a crack usually occurs upon a breakdown, which leaves the capacitor unusable.

Table 3: Dielectric constants and breakdown strengths of various insulators [13]

DIELECTRIC CONSTANTS (K) AND BREAKDOWN STRENGTHS (V_b) OF SELECTED INSULATORS

Insulator	K	V_b(V/mil)
Air	1.000585	75
Aluminum oxide	7.0–10	250–380
Bakelite (general purpose)	6.0	300
Castor oil	4.5	350
Ceramics	5.5–7.5	200–350
Ethylene glycol	39	500
High-voltage ceramic (barium titanate composite and filler)	500–6 000	50
Kapton (polyimide)	3.6	7 000
Kraft paper (impregnated)	6.0	2 000
Lucite	3.3	500
Mylar	3.25	7 000
Paraffin	2.25	250
Polycarbonate	2.9	7 000
Polyethylene	2.2	4 500
Polypropylene	2.2	7 500
Polystyrene	2.5	600
Polysulfone	3.1	8 000
Pyrex glass	4.6	500
Quartz, fused	3.85	500
Reconstituted mica	7.8	1 600
Silicone oil	2.8	350
Sulfur hexafluoride	1.0	200
Sulfur	4.0	
Tantalum oxide	27	13 000[a]
Teflon	2.0	2 200–4 400
Titanium dioxide ceramics	15–500	
Transformer oil	2.2	300–500
Water	80	500[b]

[a]Across 5 500 A.
[b]Pulse charged in 7–10 μs.

There have been many studies conducted to understand how ceramic capacitors fail under various modes of operation. A combined effort between State Key Laboratory of Electrical Insulation and Power Equipment, State Grid Shaanxi Electric Power Research Institute, and State Grid Liaoning Electric Power Company investigated the lifetime of high voltage ceramic capacitors under repetitive frequency operation at 25 Hz and proposed improvement methods to extend the lifetime of these capacitors [14]. Their

researched explored and discussed three failure modes associated with these high voltage ceramic capacitors. These failure modes are inner breakdown of the ceramic dielectric, interface breakdown of the ceramic-epoxy, and an abscission to the capacitor's connection terminals.

All capacitors used in the study were made in a laboratory that strictly follows the manufacturer Xi'an Xiwuer Capacitor Co., Ltd's, design and fabrication process. The material used to fabricate the capacitors was strontium bismuth titanate (SrBiTi), whose relative dielectric constant is approximately 2500. The electrodes for the capacitor were formed by welding silver layers and brass terminals together [14]. The structure of their fabricated capacitor is shown in Figure 15. The fabricated capacitors came out to a capacitance of about 2.55 nF. It is important to note that Figure 15 shows copper as the terminal, but the researchers instead used brass terminals in their study.

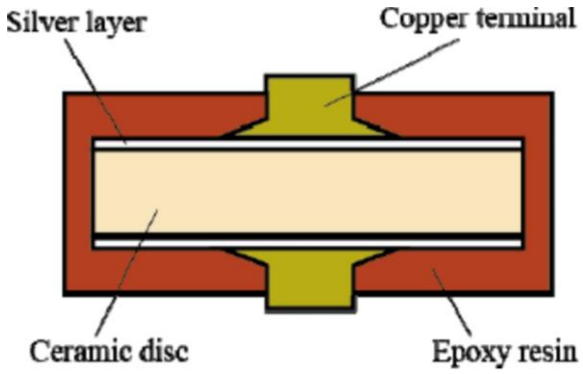

Figure 15: The structure of the high voltage ceramic capacitor [14]

To evaluate the capacitors a testbed was designed composing of three stages, which are a resonant charging circuit, a magnetic pulse compression network using pulse transformers, and a discharging cavity as shown in Figure 16. This platform can output a maximum of 70 kV and peak current over 15 kA [14].

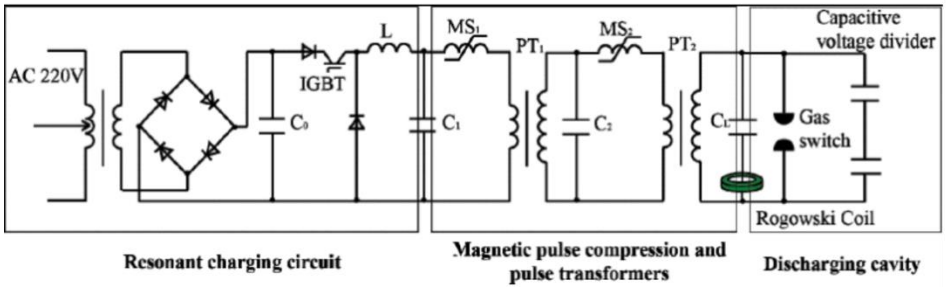

Figure 16: Circuit diagram of the repetitive pulse power generator testbed [14]

The occurrence of the inner breakdown of the dielectric ceramic often appears in overstress conditions, and the results of these conditions are shown in Figure 17. When the capacitor is operating under a high electric field, partial discharges occur within voids of the material. This is due to the limited techniques used during manufacturing, which inevitably leaves the capacitors with voids and other defects. The researchers proposed to add silicon carbide (SiC) powder and adhesive to the silver plating of the capacitor. The SiC was added to help decrease the electric field distortion [14]. Their results showed that at an electric field strength of 2 kV/mm, there was no difference in the performance of the capacitors with or without the SiC coating. However, it became apparent that increasing electric field strength to 2.5 kV/mm resulted in an increase in the lifetime of the SiC coated capacitors.

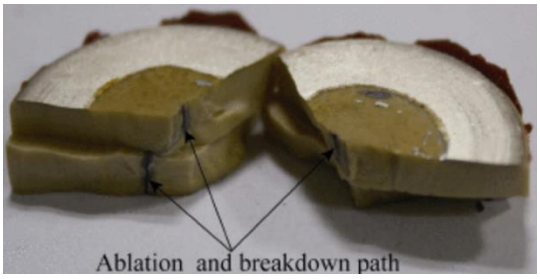

Figure 17: Dielectric failure of a ceramic capacitor [14]

The ceramic-epoxy interface breakdown is due to the associated fatigue and defects at the ceramic/epoxy interface. Results of this type of failure are shown in Figure 18. To help reduce the failure at this interface, a coupling agent was added. The coupling agent is used to enhance the connection between the ceramic discs and epoxy, due to micro slits or pores that occur during manufacturing and shrinkage of the epoxy during the curing process [14]. As a result, the added agent, was able to extend the lifetime of the capacitors. The graph in Figure 19 shows the results of this experiment. The four capacitors without the agent are labeled as F1-F4, while the added coupling agent capacitors are labeled as G1-G4.

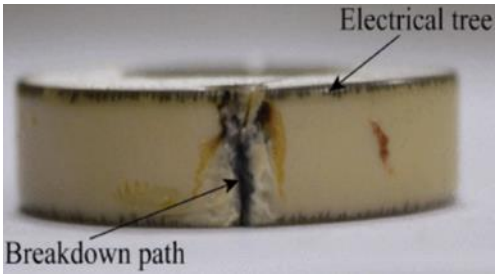

Figure 18: Ceramic-epoxy interface breakdown [14]

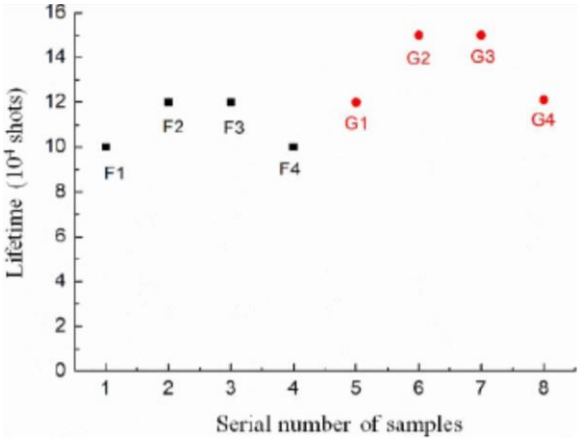

Figure 19: The lifetime comparison between capacitors with the coupling agent (G) and without the agent (F) [14]

The third failure mode mentioned was the abscission of the brass terminals as a result of high current densities and this type of failure is shown in Figure 20. The excess current density causes the considerable accumulation of heat between brass terminals and silver layers which deteriorates the welding end and lead to the abscission of the brass terminals [14]. To solve this problem work was done to change the structure of the brass terminals. The diameter of the terminal was increased, and the terminal was made to be porous such that the air gaps could be reduced during manufacturing. The lifetime results showed that the original manufactured terminals had higher capacitance and dielectric loss then the new terminal design structure, but both had the same amount of lifetime shots.

Figure 20: The brass terminals before and after lifetime tests [14]

CHAPTER III

EXPERIMENTAL SETUP

3.1 Circuit Design

The aim of the work being performed here is to design, setup, and commission, a testbed that can be used to evaluate the high rate charge and discharge of high voltage capacitors in controlled ambient conditions. There is not any one capacitor of interest, but the intent was to make a testbed capable of studying capacitors with charge voltages as high as 100 kV. Capacitances no higher than 10s of nF are most likely at these voltages. After a careful design study, the circuit topology chosen is a CLC resonant charging circuit. This circuit allows for the transfer of energy from one capacitor to another through a pulse shaping inductor. A general schematic of a CLC circuit is shown in Figure 21. The closing switch, SW, is used to release the energy stored in capacitor C_1, transferring it to capacitor C_2. Without a diode in the circuit, the two capacitors will resonate back and forth through the inductor until the energy is dissipated resistively. Adding a forward diode results in transferring energy to C_2 where it is held until it is either resistively dissipated or released into another load. This method of charging has been known to operate asynchronously and at high repetition rates [15].

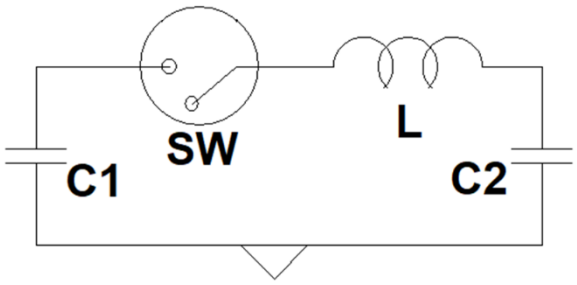

Figure 21: A CLC resonant charging circuit

Considering this topology, the circuit shown in Figure 22 was designed that allows for any capacitor under test to be charged by the power supply and then recharged by the intermediate capacitive energy storage elements C_1 and C_2.

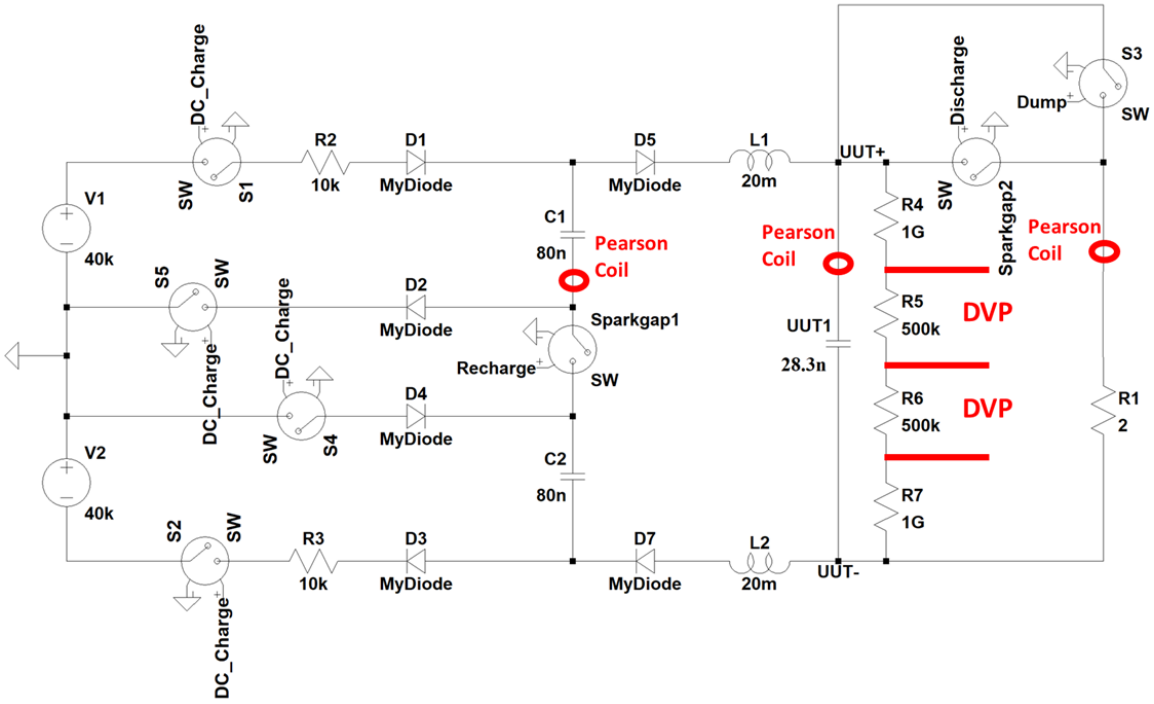

Figure 22: LTSpice circuit schematic of the CLC circuit.

In Figure 22, two 80 nF metallized film intermediate energy storage capacitors are seen. These capacitors are rated to 100 kV and act as the primary energy storage of the testbed. They are connected via a spark gap, labeled Sparkgap1, that enables them to be charged independently and then connected in series when the time is right. Each capacitor is charged by its own respective 40 kV TDK Lambda capacitor charging power supply. The upper power supply is rated to +40 kV and the lower power supply is rated to -40 kV. High voltage Ross Relay, electro-mechanical contactors, are used to connect the positive and negative terminals, respectively, of each power supply to its respective capacitor. High

voltage diodes, IXYS model UGE3126AY4, are used to connect the capacitors to its respective charge path while still allowing the common point to be broken by the spark gap. The diodes are each rated for 24 kV voltage hold off and 2 A conduction current making them well suited for this portion of the circuit. Three are connected in series in each location where a diode is shown to enable up to 72 kV holdoff. Though likely not needed because they are current limited supplies, each charge path is current limited using a 10 kΩ resistor. The unit under test (UUT), the target capacitor, is simultaneously charged through the two 20 mH inductors and high voltage diodes stacks, six in series this time. Because positive and negative polarity supplies are being used, the UUT is charged to a differential voltage as high as 80 kV.

Once all three capacitors are charged, the Ross relays that connect the supplies to the capacitors are opened to isolate them during the experiment. Once isolated, a trigger signal is sent from the host controller to a trigger transformer that drives the discharge spark labeled Sparkgap2. This connects the UUT to a low impedance, <25 Ω, water resistive load, whose construction will be discussed later. This causes the UUT to discharge at high current in a matter of a few hundred ns, with the waveform following a typical RC decay. Once discharged, a trigger signal is sent to 'Sparkgap1', connecting the common terminals of the two primary storage capacitors together, introducing them into the circuit. Once this occurs, the UUT is charged by the primary storage capacitors at a rate determined by the two 18 mH inductors that are connected between them. The two inductors were commercially procured and were sized such that the device under test would be recharged in roughly 80 to 100 μs with a peak current of roughly 60 A, depending on the UUT being

evaluated. The high voltage diode stacks connected within that series path prevent the two capacitors from oscillating causing the UUT to remain charged.

Once the capacitor is charged, Sparkgap2 can be triggered again to discharge it into the low impedance water load again. This type of operation emulates a charge, discharge, recharge, discharge test sequence of the UUT, in a manner like how it might be expected to perform in a pulsed power system. As shown in the schematic, there are several voltage and current diagnostics implemented in the design and safety dumps that are used to abort the process as needed. More detail will be provided about each part of the testbed in the sections that follow but this briefly summarizes its overall operation.

3.2 The Physical Testbed

The physical construction of the CLC circuit is shown in Figure 23. There were many implementations of the construction that led to this final design. Most of the testbed is assembled within a 45” x 45” x 24” aluminum enclosure that is lined with two 45 mil thick sheets of PVC so that it can be filled with a transformer oil dielectric. What is not shown in Figure 24 are the two inductors and the resistive voltage dividers, which are underneath the pulse transformers. A primary design element of the testbed is that the UUT be able to be placed in a controlled but variable ambient thermal environment. This is accomplished by placing the UUT in a temperature chamber as shown in Figure 25. The UUT is housed in a plastic container within the chamber that is filled with transformer oil.

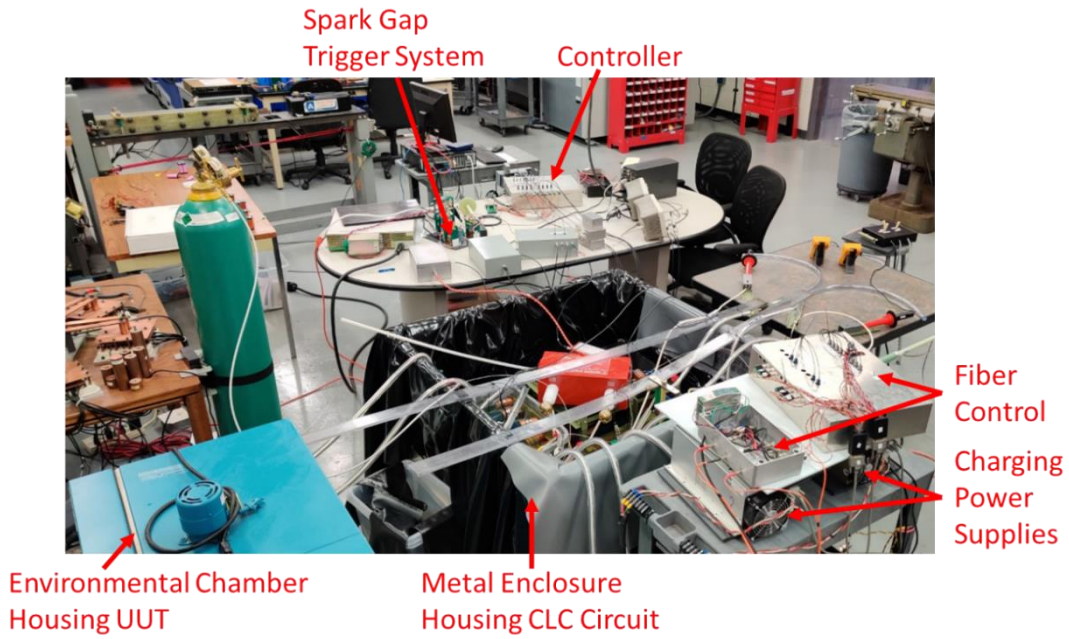

Figure 23: Physical Testbed Setup

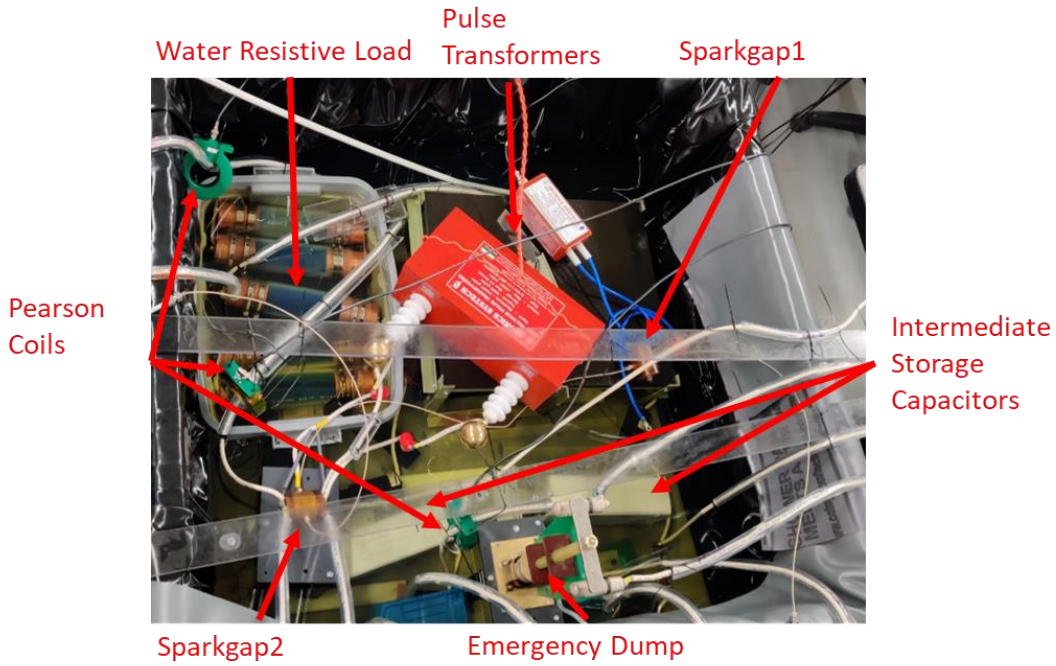

Figure 24: The layout of the circuit, excluding the power supplies and the capacitor under test.

Figure 25: The Unit Under Test (UUT) capacitor will be placed inside a temperature chamber and will be submerged in oil. While in the temperature chamber, the UUT will be under various ambient conditions.

3.3 Water Resistive Load

Resistive loads capable of 100 kV and high current operation are not trivial or cheap, therefore the easiest and most effective way of accomplishing this is to use custom made water resistors, shown in Figure 26. The resistors are constructed using two copper electrodes that plug both ends of a piece of Tygon tubing. The tube is filled with a mixture of de-ionized water and cupric sulfate crystals dissolved to obtain the desired resistivity. In this case, the diameter of the tubing was chosen to be 2.5". This was chosen as low impedance was desired and that is of course achieved by either a large cross-sectional area or a short length. Since a short length will breakdown at 100 kV, the larger area is desirable. A load impedance of a few Ohms was needed so it was determined early that a few resistors would have to be paralleled to achieve that. At room temperature, the expected resistance of each resistor was estimated to be roughly 21Ω and it was assumed that as many as nine would be paralleled to achieve a few Ohms of resistance. The resistance value was

calculated using equation 3.1 [16], where ρ is the resistivity of the saturated solution, R is the resistance, A is the cross-sectional area, and L is the length of the water filled portion of the tube.

$$\boldsymbol{\rho = \frac{RA}{L}} \qquad \text{Eq. 3.1}$$

Figure 26: Pictured are the water resistors that will act as part of load the for the CLC charging circuit.

Once filled, the resistor values of each resistor were validated using the RC circuit shown in Figure 27. The setup shows a 2900 pF capacitor in series with a park gap and the water resistor under test. The spark gap was setup to breakdown at roughly 2.7kV. The capacitor was charged until the spark gap broke down and the voltage and current through the resistor under test was measured. Knowing the capacitor value, the RC time constant was used to measure the resistor value. An LTspice model was created to validate the measured values, shown in Figure 27.

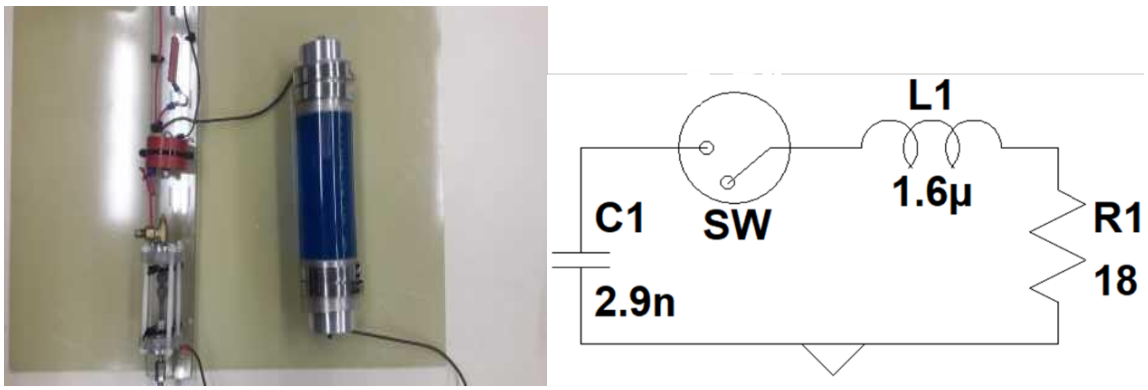

Figure 27: Displayed is the RC circuit and LTspice model created to validate the water resistor value. The circuit is composed of a 2900pF capacitor in series with a spark gap and water resistor.

A sample of the data collected, shown in Figure 28, shows an underdamped RLC series circuit. An estimated 500nH inductance was assumed as an initial guess in the simulation to resemble the underdamped system. With this estimated inductor value, equation 3.2 used to calculate the resistance value [17]. From this, the resistance of the resistor was found to be roughly 18 Ω.

$$I_{peak} = \frac{V_0}{L\omega_o} e^{\frac{-R\pi}{4L\omega_o}} \qquad \text{Eq. 3.2}$$

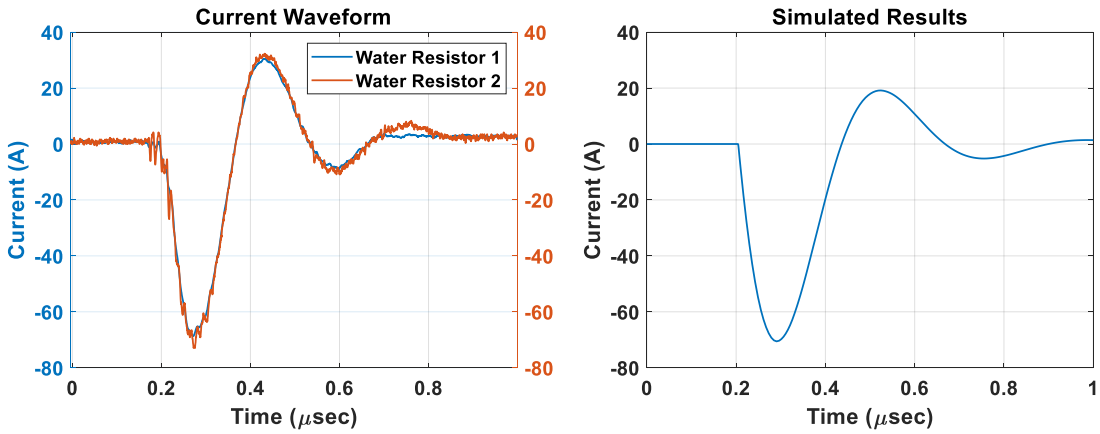

Figure 28: The left displays the experimental results of two water resistors. The simulated results are shown on the right. The results of the simulation match closely with experimental measurements.

3.4 Spark Gap Trigger System

Spark gaps are used to initiate a discharge of the UUT as well as the recharge from the primary storage, respectively. Triggering of the spark gaps proved to be one of the most difficult portions of the project. The trigger must be initiated from the low voltage control system but stepped up to a 10s of kV pulsed voltage to initiate the breakdown event in an isolated manner. This is typically achieved using high voltage step-up pulsed trigger transformers. Though these are commonly used, they are nearly always custom designed and are not readily available as a commercial off the shelf component.

The first attempt at a triggering system utilized an automotive spark plug trigger circuit and transformer, shown in Figure 29. This design had a great deal of promise as the spark gap trigger box cost roughly $450, driving a roughly 450 V output pulse using a 12 VDC input source. The transformer is a step-up transformer that converts the 450 V output pulse into a roughly 45 kV output pulse, perfect for triggering the spark gaps.

Since these were designed for automotive use, there was little documentation available from the manufacturer about the generation of the pulses, isolation rating, or its general operation beyond how to install it in an automotive vehicle. Spark plug triggers will typically send pulse bursts rather than a single pulse so special effort was made to find a trigger system that would be capable of sending a single trigger on command, or so it was thought after conversations with the manufacture. As will be shown later, the information gathered from the manufacturer was not entirely correct and the trigger generator sent bursts of pulses that overlapped with the discharge and recharge commands thereby preventing them from being able to be used properly.

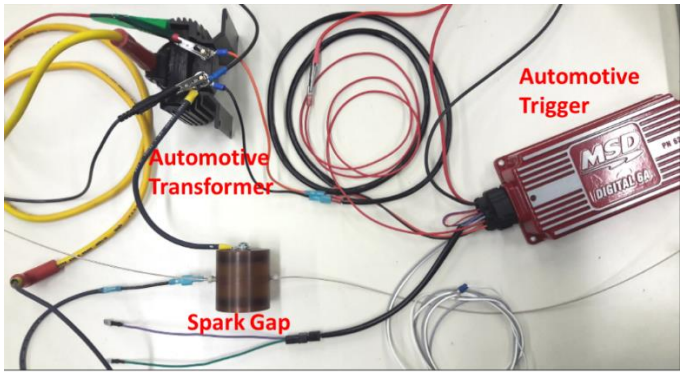

Figure 29: The automotive spark plug trigger, transformer and spark gap.

Another problem was found with respect to the transformer. Rather than having isolated grounds on the primary and secondary coils, they were commonly grounded and designed to ground to an automotive chassis. This of course was very unfortunate as it prevented the low voltage control ground from being able to be isolated from the high voltage output ground. Calls to US transformer manufacturers for a custom solution were either unanswered or the cost of a few transformers exceeded $10,000 which was well in excess of the allowable budget. Therefore, the second attempt involved using the same

automotive transformer and a custom primary drive circuit. The drive circuit was replaced with a simple capacitive discharge circuit that discharges a 330 µF capacitor into the primary of the step-up automotive transformer through a low side SCR switch, shown in Figure 30. The SCR was driven using a 5 V logic circuit from a controller. This circuit worked great for triggering the spark gaps on the bench however when they were introduced into the high voltage CLC circuit, the inability to isolate the primary ground allowed noise to be coupled into the system that damaged portions of the low voltage National Instruments controller. It was determined quickly that a cost effective, isolated transformer method had to be identified.

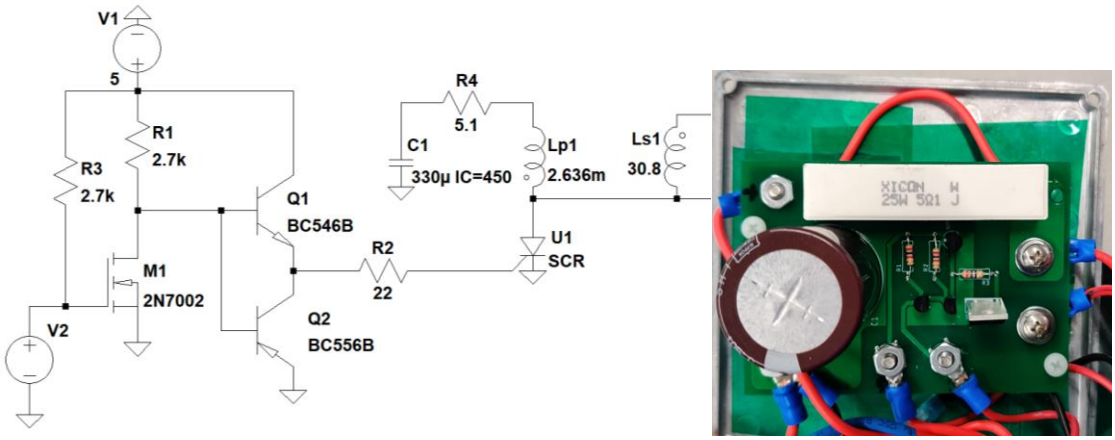

Figure 30: The left is the circuit schematic of the capacitive discharge circuit into an automotive transformer circuit with a low side SCR switch. The right is the professional PCB of the circuit.

The next attempt involved making custom 1:1 transformers that could be used to isolate the secondary of the automotive transformer from the spark gaps. A few ferrite cores typically used to reduce EMI on data acquisition cables were used first. The BH curve of the ferrite rings was unknown but there was extras around the lab, so they were tried. When

experimented, there is not enough impedance in the 1:1 transformer's primary to drive the voltage needed so it would not work; even after adding additional turns to its secondary. The second approach was to use extra Metglas cores from the lab, shown in Figure 31. Using these cores, an attempt was made to make step-up transformers, but they saturated at 5 kV on the secondary meaning the magnetic properties were not well matched to the requirements.

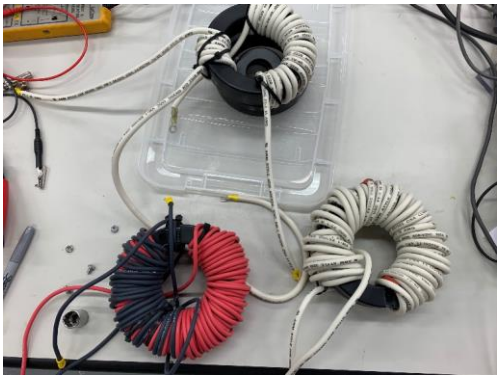

Figure 31: Photograph of the few transformers attempts made using the Metglas cores.

These unsuccessful attempts using parts around the lab meant that a more careful design was needed. In the process of researching core materials, an Indian company called Zeonics was found who offered a pulse transformer that required a roughly 1 kV input, produces 100 kV output, has isolated grounds, and that has 130 kV of DC isolation. This transformer is shown in Figure 32. The cost was well within the budget and therefore it was procured as a simple solution. They also offered a pulse transformer that required and 800 V input, has a 40 kV output, has isolated grounds, and has 50 kV of DC isolation. This one is seen in Figure 32. One of each was procured with the former being used to trigger the discharge sparkgap and the latter used to trigger the recharge sparkgap.

Figure 32: Left is the 1 kV input/ 100 kV output pulse transformer and the right is the 800 V input/ 40 kV output pulse transformer

Once those were obtained and a new capacitive discharge circuit was designed that used higher rated SCRs, diodes, and transistors shown in Figure 33, evaluation of the triggering system was performed successfully, and experiments were finally able to be performed to commission the testbed.

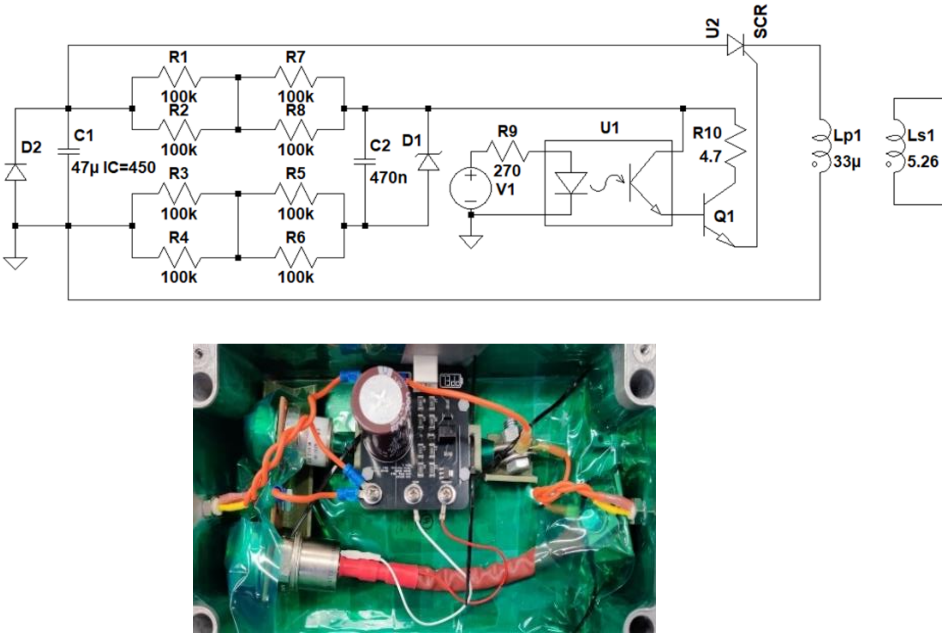

Figure 33: Top is the circuit schematic of the capacitive discharge circuit and the bottom is the encased capacitive discharge circuit, SCR, and flyback diode

3.5 The Control System

This section will discuss the many software, data acquisition, and fiber optic isolation methods used to safely control and operate the system.

3.5.1 National Instruments cDAQ Chassis

A National Instruments (NI) cDAQ chassis, which is shown in Figure 34, is used to control the power supplies, actuate all relays, trigger the spark gaps, and for status and fault monitoring. As shown in the figure, the chassis houses four cDAQ cards. These cards are a NI 9225 analog input card, a NI 9263 analog out card, a NI 9476 digital out card, and an NI 9425 digital input card. The NI 9476 card is powered by an external 15V/1A power supply also shown in Figure 34.

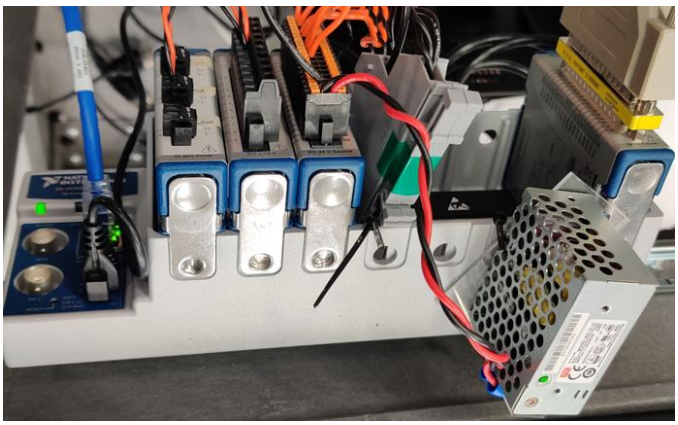

Figure 34: The right shows the NI cDAQ chassis to control the power supplies, actuate all the relays, trigger the spark gaps, and for status and fault monitoring.

The NI 9225 analog input card is used to measure a scaled version of the power supply output voltage and therefor the capacitor charge voltage. This measurement is on a scale from 0 to 10 V; where 10 V is equivalent to 40 kV. The NI 9263 analog output card is used to set the output voltage level of the power supplies. This card outputs a 0 to 10 V

analog signal, that the high voltage power supplies convert internally to the range of 0 to 40 kV. The NI 9476 digital out card is used to send the inhibit and enable signals to both supplies when commanded. This output card is responsible for sending the trigger signals to the spark gap trigger system as well. The last card in the chassis is the NI 9425 digital out card, which is used for status and fault monitoring of the high voltage power supplies

3.5.2 National Instruments LabVIEW

Communication between the NI cDAQ cards and the hardware is controlled using a custom designed LabVIEW virtual instrument (VI) panel, shown in Figure 35. The VI controls the output voltages of the power supplies either independently or using a common set point. The VI also has an automatic inhibit feature that stops the power supplies from charging the capacitors once the desired charge voltage is reached. This is accomplished by using the end of charge status that the high voltage power supplies send to the cDAQ card. The power supplies can be commanded to immediately set the output voltage to the desired charge voltage, or the voltage can be ramped from 0 V to the desired charge voltage using a ramp function. The speed of the ramp function is an arbitrary value that was selected to reduce the charge speed of the supplies and reduce potential LdI/dt spikes. This value can be manually changed on the front panel of the VI to make the ramp slower or faster.

‘LEDs’ on the front panel are used as indicators to indicate the status and faults of the supplies. These indicators represent the load fault, summary fault, end of charge, and inhibit. The load fault represents a shorted output or a very large output capacitor. Below the load fault LEDs, are the summary fault LEDs, that show if there is an output

overvoltage, a temperature fault, or low input voltage. Then there is the end of charge LEDs, which indicate when the power supplies reach the desired set voltage. The status of the charge indicators is used in the auto inhibiting functionality mentioned earlier. The last set of LEDs for status and fault monitoring is the inhibit LEDs which indicate when the unit can be enabled. Essentially, the power supply requires inhibit to be off and enable to be on for operation, or charging, to occur. In simpler terms, if inhibit is on, then the output is always off; and if inhibit is off then the output can be enabled. Inhibit is a state that is auto enabled by the supply in a fault case but is otherwise controlled via a button on the front panel. Finally, the front panel plots the voltage returned from each respective power supply in the two black plots on the right-hand side and has the ability to record those waveforms as .csv files for later processing and analysis.

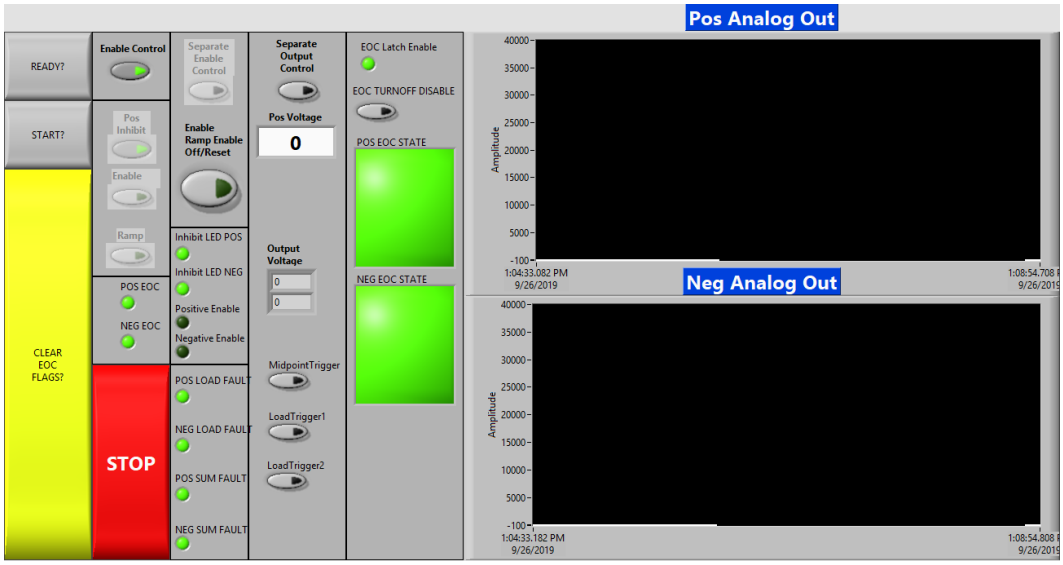

Figure 35: The front panel of the LabVIEW VI used for controlling the cDAQ. The VI can control the power supplies separately or together with a numerical input value. In addition, the VI can control when the spark gaps will be triggered.

3.5.3 Fiber Optic Control

The power supplies have control signals, both analog and digital, that are sent from and transmitted to the control system, which is floated using a UPS. In other words, the UPSs are used to power the low voltage equipment in the system. The output ground of each supply is earth grounded. To isolate the NI controller from the high voltage testbed; fiber optic transmit (Tx) and receive (Rx) boards were designed and fabricated to interface with the low voltage NI controller and the high voltage testbed and are shown in Figure 36. The eight channel boards are designed such that each independent channel can interface with either 15 V or 5 V logic; where the user is able to select which voltage is used. This is critical as the high voltage power supplies require 15 V logic as an input while the NI controller requires 5 V. The power supplies also use an open-collector as an output to send its status and fault signals. The Tx board was designed and validated to work with an input of either a grounded 15 V signal, grounded 5 V signal, or an open-collector using user controlled switches.

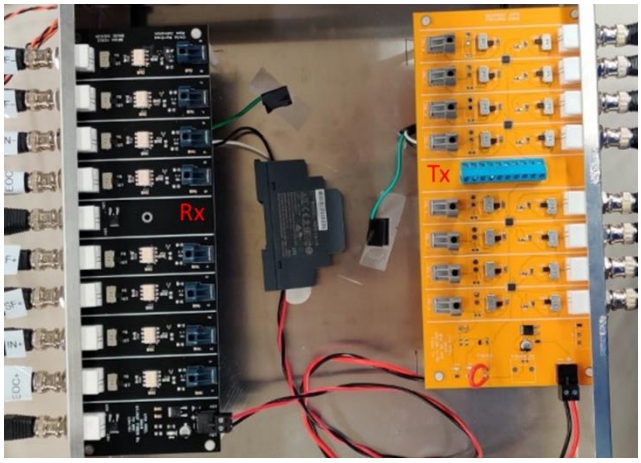

Figure 36: The fiber optic transmit (Tx) and receive (Rx) boards. The black board is the receive and the yellow board is the transmit board

Fiber optic isolation of the analog control signals is a little bit more difficult. To achieve this, low-cost analog/fiber converters were procured by a company called AA Labs. These boards are called the AFL-200 and are a single channel analog boards that transmit and receive 0 – 10 V analog signals over fiber. The 0 – 10 V analog voltage signals are sent by the controller to the power supplies to set the output voltage of the power supplies. Similarly, 0 – 10 V analog signals are sent by the power supplies back to the controller to report their respective output voltage. The boards use frequency modulation to achieve this task. Each board also has two digital transmit/receive channels on them but due to the 0 – 10 V logic level, they are being used here. There are two sets of four AFL-200 channels assembled into two control enclosures to interconnect the supplies to the NI controller. Each enclosure has two transmit boards and two receive boards and one of the enclosures are shown in Figure 37.

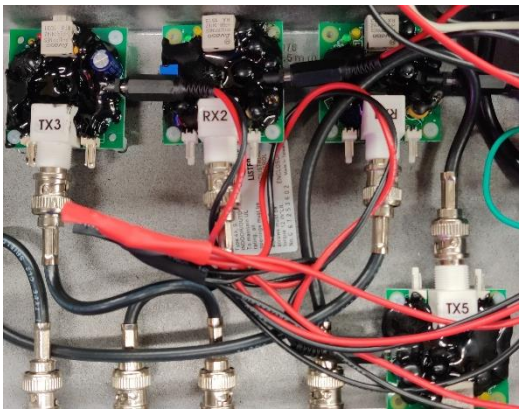

Figure 37: One enclosure containing two transmit and two receive analog/fiber boards.

3.5.4 Control Setup

The diagram in Figure 38 showcases how the fiber isolation boards and the AFL-200 analog/fiber converters are implemented between the NI cDAQ, the power supplies, and the trigger system, respectively.

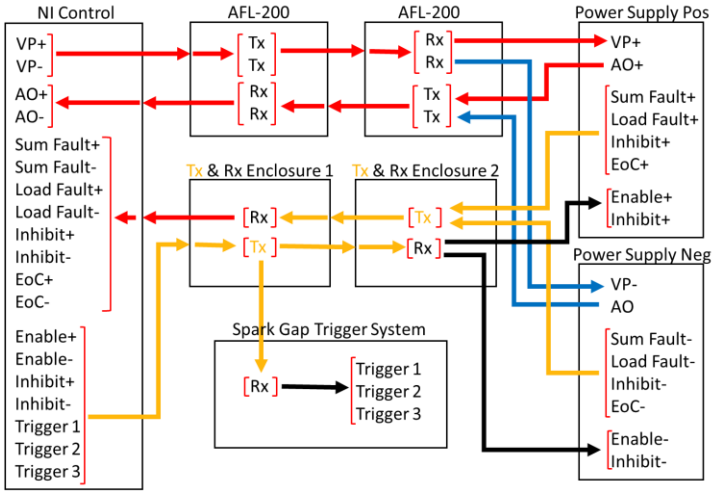

Figure 38: Diagram of how the fiber boards are connected within the system.

On the controller end, the two analog transmitters send out Vprogram+ (VP+) and Vprogram- (VP-) that are 0 – 10 V analog signals that set the voltage point of each respective power supply; with 10 V being equivalent to a 40 kV output from the power supplies. The two receivers receive the Analog Out+ (AO+) and Analog Out- (AO-), that are 0 – 10 V analog signals from each respective power supply that reports their respective output voltage. The enclosure at the power supply side will of course perform the opposite function. The Tx and Rx enclosures are used to transmit the enable and inhibit signals from the controller to each power supply and all the status/fault indicators from the power supplies back to the controller. The Tx board in the TX and Rx enclosure 1, is responsible for sending three trigger signals to another Rx board in the spark gap trigger system.

Trigger 1 is for a discharge of the capacitor, trigger 2 is for a recharge, and trigger 3 is for another discharge.

3.6 Electrical Diagnostics

In this section, the implementations of the voltage and current diagnostics are discussed.

3.6.1 Voltage Monitor

Given the high voltage nature of the circuit, voltage monitoring is not easy to achieve. Two voltage dividing circuits are used to monitor/measure the voltage across the unit under test (UUT). Each divider is made up of a 1 GΩ high voltage resistor in series with a 500 kΩ potentiometer that can be used to tune the voltage divider ratio, shown in Figure 39 and labeled as 'DVP' in Figure 22. The low side and high side labels are above each respective potentiometer that can be adjusted to tune the divider ratio. On the right side are four BNCs labeled I_1, V_1, I_2, and V_2. I_1, and I_2 are used to carry in one leg of each respective 1 GΩ resistor for connection to its respective potentiometer. The V_1 and V_2 BNCs are across each respective potentiometer and each is monitored by its own respective differential voltage probe (DVP) for data acquisition.

Figure 39: The enclosure for the two 500 kΩ potentiometers that are used for tuning the voltage divider ratio.

3.6.2 Pearson Current Monitor

With current risetimes on the order of 100's of nanoseconds, high slew rate current diagnostics are required. Current monitors manufactured by Pearson Electronics Inc., model 110A, are used to monitor the discharge and recharge currents, respectively of the system. Three of these coils are placed inside the enclosure. The placement of these coils in the circuit can be seen in Figure 22. These monitors have a sensitivity of 0.1 V/A, maximum peak current of 10 kA, and a usable rise time of 20ns when terminated into a 50 Ω impedance [18]. A graphical description of the coil is shown in Figure 40.

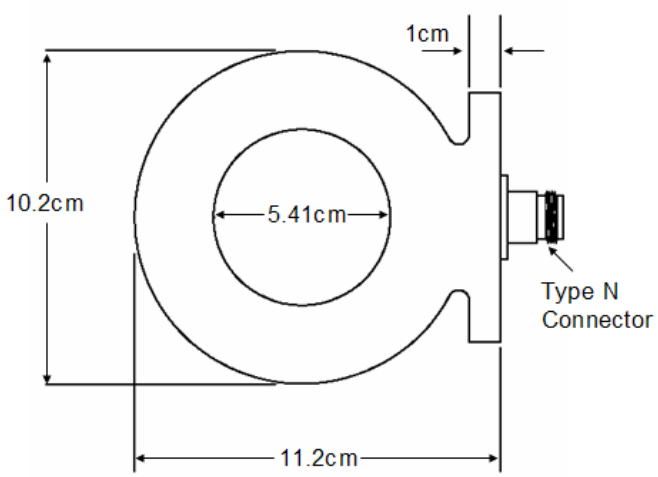

Figure 40: Pearson current monitor (model 110A) [18].

CHAPTER IV

Preliminary Results

The focus of this chapter is to discuss the testing procedures employed to date. This chapter will also briefly discuss preliminary waveforms collected, which will be compared to simulations conducted in LTspice.

4.1 Testing Procedure

When conducting experiments, each part of the system needs to be checked before any experiments begin. The inspections include checking the fiber circuit boards as well as the spark gap air pressure and air left in the compressed air cylinders. A safety check list appears on the front panel of the VI and must be filled out by the user before the user can control the high voltage power supplies. This checklist ensures all the relays are in the correct position and that the UPSs are disconnected from earth ground before any testing can be conducted. After testing is completed, all dumps are closed and all relays connecting the power supplies to the system are opened, in case there is a malfunction in the power supplies before they are disconnected from the wall. After experiments are completed, a 120 kV shorting stink is used to short each capacitor in the system to ensure they have fully discharged, and a shorting strap is then connected across each one for safe storage.

4.2 Typical Voltage and Current Waveforms

The testbed has been able to repeatedly perform charge, discharge, and recharge sequences at 20 kV (±10 kV), 40 kV (±20 kV), and 60 kV (±30 kV). Though it should be capable of operation above 60 kV, it has not been attempted just for a lack of needing to so far. Figures 41 - 46 showcase the discharge and recharge waveforms at each voltage

level and how it compares to simulation results. It is important to note that the resisitve voltage divider was not used to measure the voltage across the UUT, and a 100 kV grounded probe was used in limited circumstances only. One thing to notice about the voltage probes measurement is the negative portion on the discharge sequence at each voltage level. It is confident to say that the negative portion of the votlage waveform in the discharge plots is not real and it is due to the nature of the non-isolated votlage probe. It should be noted that the capacitor used for these sets of test was not characterized, which means the simulation did not have the exact model to simulate the capacitor. The decision to not characterize the capacitor was due to conducting these experiements to test the capabiltiies and reliabilty of the testbed and not the capacitor yet.

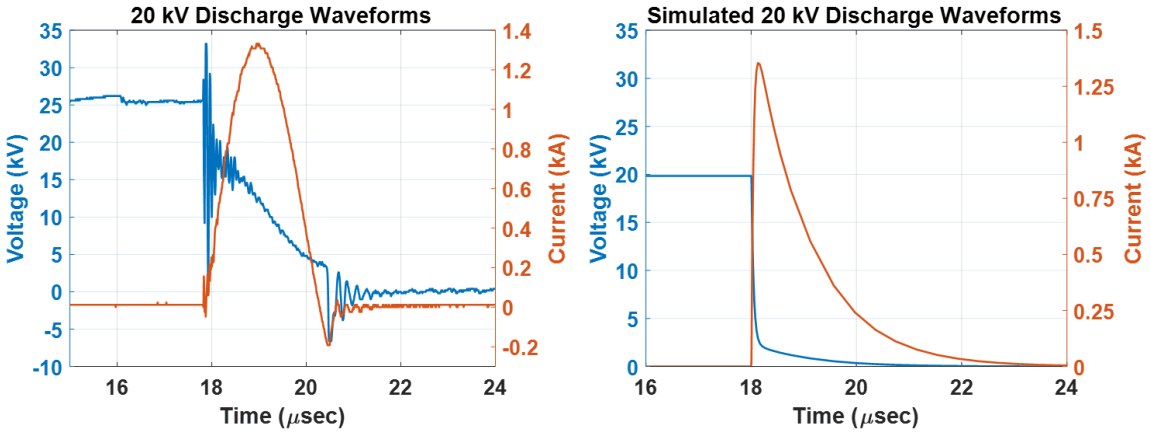

Figure 41: Measured (left) vs Simulated (right) results of a 20 kV (±10 kV) discharge.

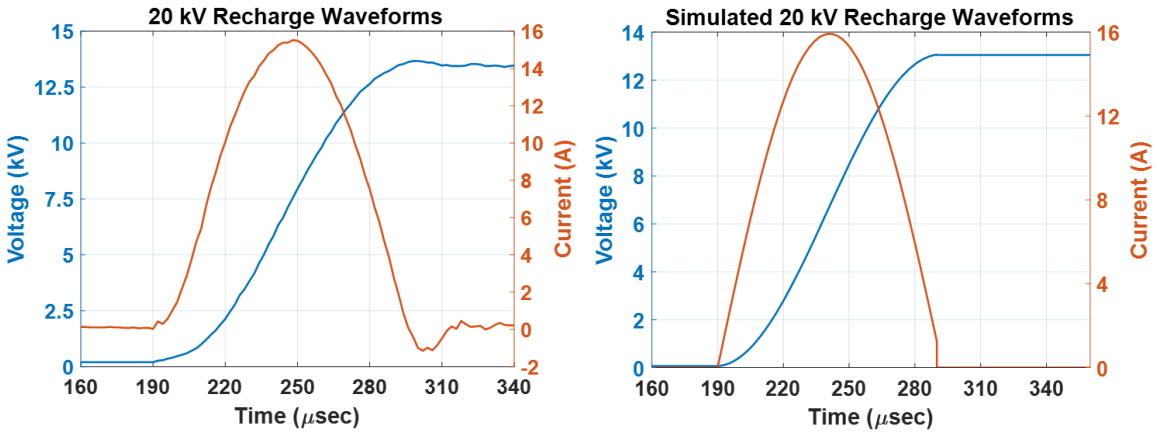

Figure 42: Measured (left) vs Simulated (right) results of a 20 kV (±10 kV) recharge.

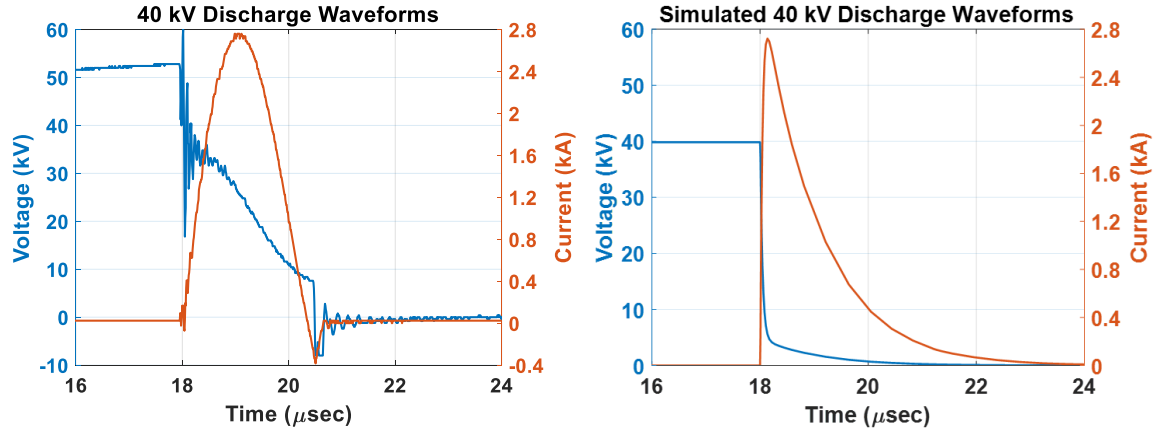

Figure 43: Measured (left) vs Simulated (right) results of a 40 kV (±20 kV) discharge.

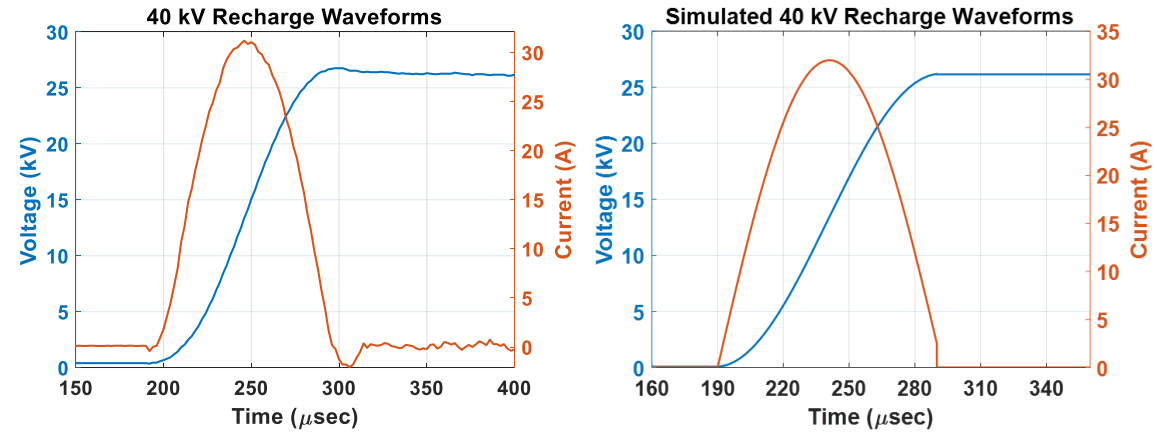

Figure 44: Measured (left) vs Simulated (right) results of a 40 kV (±20 kV) recharge.

It is important to note the reason why the resisitve voltage divider was not used to measure the voltage across the UUT up to this point. Because the divider is resistive, it will allow the capacitor under test to discharge and since the timing of the spark-gaps is all manual at this point, leaving the capacitors too long would allow them to discharge.

As reliability experiments of the testbed continued, it was believed that the non-isolated voltage probe would be an acceptable measurement. During an experiment at 50 kV (±25 kV), an arc occurred between the UPS ground, which is floated up to -25 kV, and the concrete floor causing a bit of damage to the floor. As stated earlier, UPSs are used to float the low voltage system, which includes the oscilliscopes; which results in the ground connection being floated up to ground of the capacitor under test due to the non-isolated voltage probe. To ensure that the system was kept safe, the voltage probe was removed.

Additional experiments were performed at 20 kV (±10 kV), 40 kV (±20 kV), and 60 kV (±30 kV), without the voltage measurement of the UUT to demostrate the repeatability of the system from current measurements alone. The results of the 20 kV and 40 kV experiments are identical to those shown in Figures 41 - 46. The results of the 60 kV waveforms are shown in Figure 47. A comparison of the recharge voltage of four different shots at 60 kV are compared in Figure 48. Also, a second discharge was conducted and recorded afer the recharge and it is compared to the first discharge in the sequence in Figure 49. Since, the UUT has a capaciotance of 80 nF, where as the primary storage is only 40 nF when connected in series, it is expected that the UUT is charged to roughly 2/3 of the initial charge votlage, resuting in less current in the second discahrge. The math justifyign this is found in equations 4.1, 4.2, and 4.3 [19]. From the equations it can be

shown that as the capacitance of C_2, which is the UUT, is decreased; the voltage and current peak values are increased.

$$V_{c2}(t) = \frac{V_o}{1+\frac{C_2}{C_1}}[1 - \cos(\omega_o t)] \qquad \text{Eq. 4.1}$$

$$I(t) = \frac{\omega_o V_o}{\frac{1}{C_1}+\frac{1}{C_2}} \sin(\omega_o t) \qquad \text{Eq. 4.2}$$

$$\omega_o = \sqrt{\frac{1}{L}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)} \qquad \text{Eq. 4.3}$$

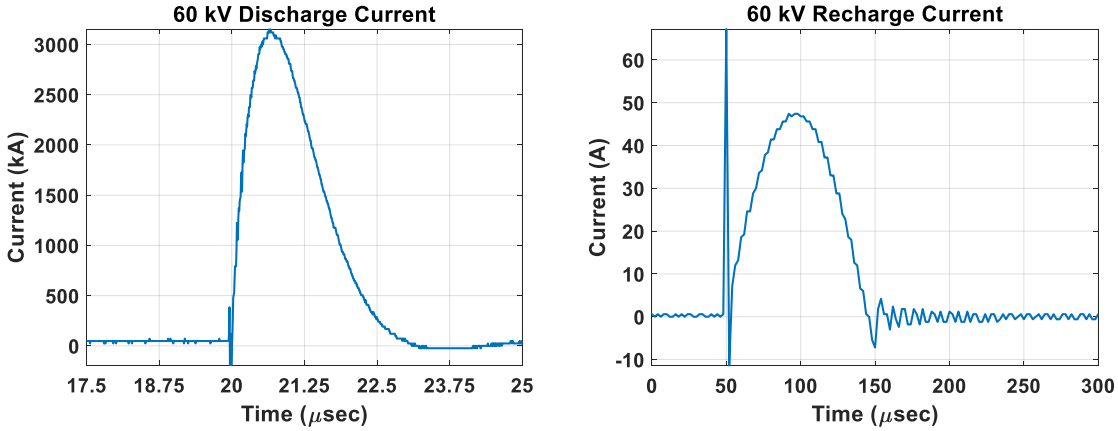

Figure 45: 60 kV discharge (Left) and recharge (right) current waveforms.

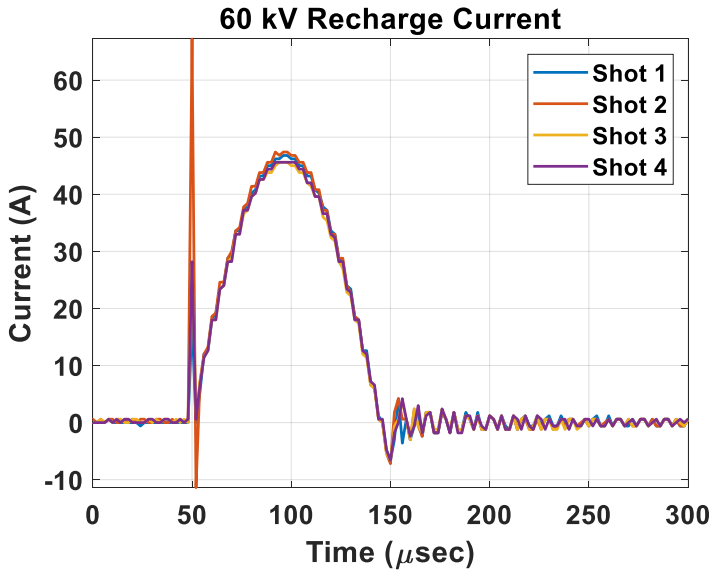

Figure 46: An overlaid comparison of the recharge voltage at 60 kV during four different shots.

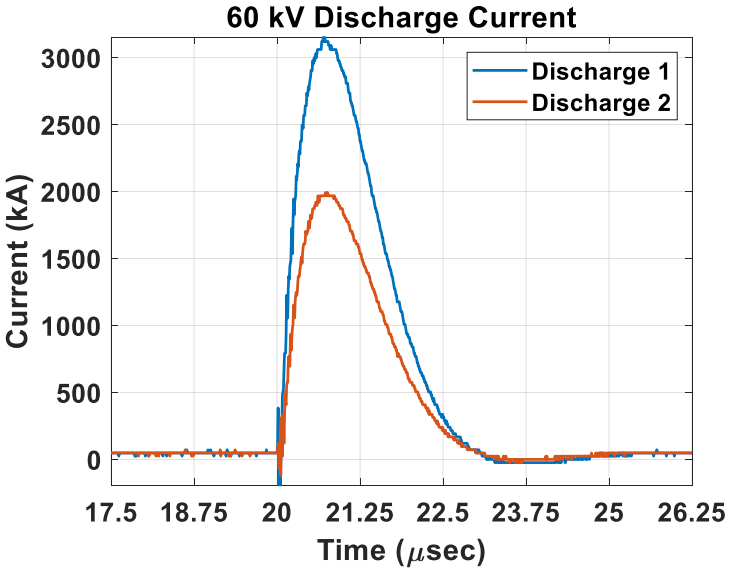

Figure 47: An overlaid comparison of Discharge 1 vs Discharge 2.

CHAPTER V

SUMMURY AND CONCLUSIONS

In the work presented here, a capacitive-inductive-capacitive (CLC) circuit testbed was proposed and implemented. The testbed was developed to characterize the performance of high-voltage, pulsed-power capacitors when subject to high rates of charge and discharge in well-controlled ambient conditions, with the focus on high rate recharge of the capacitor. So far, only experiments regarding the reliability of the testbed have been conducted, with a few preliminary results. The capacitors are of interest for use in a variety of compact, repetitive rate applications such Marx generator sources used to supply pulsed power to a few different loads.

As high rates of operation modes are increasingly becoming more of a focus for pulsed power systems, there is a need to understand how high voltage pulsed power capacitors perform, age, and fail in this kind of mode as well as various ambient conditions. There have many studies that have investigated how the capacitor performs in these kinds of modes, but many of the investigations did not cover rapid recharge, varied ambient conditions, and high peak current and voltage discharges. Now that the testbed is complete, it is available for future users to study capacitors of interest.

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