FUNCTIONALIZING SEMICONDUCTOR-CRYSTALLINE OXIDE HETEROSTRUCTURES FOR FUTURE APPLICATION IN ENERGY HARVESTING, SENSING, AND COMPUTING TECHNOLOGIES

By

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Abstract

Energy harvesting, sensing, and computing technologies utilizing conventional semiconductors have seen a plateau in their advancement for future applications. In order to address these issues, alternate materials are needed to improve present technologies. In my research, I proposed here that complex oxides can serve as potential candidate materials due to their properties.

Single crystalline $SrZrO_3$ thin film can be a potential candidate as dielectric material for Ge-based metal-oxide-semiconductor technologies. I present here a structural and electrical characterization of $SrZrO_3$ thin film grown epitaxially on Ge (001) substrate with oxide molecular beam epitaxy. X-ray photoemission spectroscopy has shown that $SrZrO_3$ thin film has a large conduction band and valence band offset with respect to Ge. Moreover, electrical characterization of the 4 nm thin film with capacitance-voltage and current-voltage have shown low leakage current densities and high dielectric constant.

The tunable charge transfer and built-in electric field have laid down groundwork for developing functional heterojunction for energy harvesting purposes. Charge transfer and built-in electric field were reported across heterostructures of epitaxial $SrNb_xTi_{1-x}O_{3-\delta}$ grown on Si (001). Transport measurement shows the formation of hole gas in Si. Hard x-ray photoelectron spectroscopy also shown asymmetries in core level spectra, which further confirm the built-in electric field across the heterojunction. The band bending due to built-in fields was spatially mapped out across the heterojunction with hard x-ray photoelectron spectroscopy.

The wet etching study of complex oxide thin films and newly developed recipe could be used for fabrication of crystalline oxide sensing microdevices for future applications. I report

here the study of wet etching of $BaTiO_3$ and $SrTiO_3$ films with HF Dip 10:1. The wet etching rate of $BaTiO_3$ and $SrTiO_3$ with different annealing conditions were determined using profilometer. The differences in etching rate for different annealing conditions are closely related to the bond density, crystallinity, and grain boundary of the films. A recipe was also developed to fabricate 156 nm $BaTiO_3$ microbridge. Diffraction pattern image has proven the microbridge still preserve its crystallinity after processing.

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Chapter 1 : Introduction

Conventional semiconductors have been the basis of energy harvesting, sensing, and computing technologies. For energy harvesting technologies, photovoltaic cells were commonly used to harvest solar energy. Photovoltaic cells generally consist of p-n junction, which is a heterojunction between a p-type and a n-type semiconductor. When a p-type semiconductor is placed in contact with a n-type semiconductor, there will be charge transfer across the interface that induces built-in electric fields. Photovoltaic cells utilize the built-in electric fields to direct photon generated electrons in order to create direct current. Moreover, semiconductor heterojunctions are also the building block of present device technologies. In the microelectronic technologies, Microelectromechanical Systems (MEMS) technology is widely employed in the sensing technologies, such as pressure sensor and resonator. Si based materials are the most used material for MEMS sensing devices due to their mechanical properties and the well-developed fabrication process for Si. Si is a very robust material that deforms elastically and low thermal expansion. [1] At last, one of the important components in computing technologies is the metal-oxide-semiconductor (MOS). MOS technology is utilized to construct integrated circuits, which are used in present computing devices. Si based oxide material and Si substrate are also used heavily in the MOS technologies.

However, as we move forward, energy harvesting, sensing, and computing technologies based on conventional semiconductors have reached a plateau in technology advancement. To address these issues in advancing energy harvesting, sensing, and computing technologies, I am going to explore the use of complex oxides as alternate materials for applications. Complex oxides have gained a lot of interest for their interesting material behaviors that are not found in conventional semiconductors. Some of the complex oxides' properties that could potentially be

utilized in energy harvesting, sensing, and computing technologies include semiconducting, ferroelectric, and dielectric behaviors.

Photoelectrocatalysis has gained tremendous amount of attentions for generating hydrogen fuel in energy harvesting technologies. Photoelectrochemical (PEC) cells were used for water splitting, where PEC cells use semiconductor materials to convert solar energy to produced hydrogen gas. Conventional semiconductors are ideal materials for PEC cells due to their small bandgaps in order to generate electron-hole pair to produce hydrogen gas, but they are not thermodynamically stable in aqueous condition. Instead of conventional semiconductors, some researchers have reported to use TiO_2 for PEC cells, but TiO_2 has a larger bandgap than conventional semiconductors that limits the light absorption. [2] Therefore, it is important to look for hybrid heterojunctions consist of complex oxides and semiconductors, in order to take advantages of both materials, namely, generate electron-hole pairs efficiently and thermodynamically stable in aqueous condition.

In the sensing technology, complex oxides can be introduced to the MEMS technology due to their electronic properties that are strongly coupled to mechanical properties. Those properties such as piezoelectricity, ferroelectricity, and metal-insulator transition can be tuned through material's strain and doping. Thus, complex oxides can be introduced to enhance present sensing technology.

As in MOS technology, Si is known to have lower electron and hole mobilities than Ge, which leads to the transition of Si technology to Ge technology. In order to switch to the Ge-based technology, a search for high dielectric constant gate material for Ge-based technology is needed. Hence, complex oxides can be explored to use as gate dielectric for Ge-based MOS devices.

The advancement in epitaxial growth of complex oxides on conventional semiconductors has provided a platform to functionalize complex oxide. The ideal epitaxial growth of complex oxides on semiconductors is to grow a full oxide layer without oxidizing the semiconductor substrate, due to the fact that the oxidized semiconductor is generally amorphous and will break the template for oxide epitaxy. The growth of epitaxial $SrTiO_3$ on silicon substrate without oxidize the Si was first founded by McKee et al. [3] This growth method is required to couple complex oxides to semiconductor electrically. Moreover, heterostructures that comprise of complex oxides and semiconductors could contain electronic properties from both materials that cannot be achieved by either of them alone.

The objective of my research is to explore new functionalities of complex oxides epitaxially grown on conventional semiconductors. In my dissertation, I will focus on studies of semiconducting, dielectric, and ferroelectric behaviors of complex oxides that are electrically coupled to semiconductors. In my first project, I have studied the dielectric behavior of $SrZrO_3$ thin film that was grown on Ge, which introduce $SrZrO_3$ as a potential gate dielectric material for Ge-based MOS devices. [4] I have also studied the charge transfer and built-in electric fields across the heterojunctions between Nb-doped $SrTiO_3$ and Si. The built-in fields across the complex oxide-semiconductor interface could be utilized for future energy harvesting application. [5] Lastly, I have determined the wet etching of $SrTiO_3$ and $BaTiO_3$ film and successfully developed a recipe to fabricate complex oxide MEMS device using conventional integrated circuit (IC) fabrication techniques. This recipe can enable a route to introduce complex oxide materials to the MEMS technology as well as for sensing technology.

1 Structural and electrical properties of single crystalline $SrZrO_3$ epitaxially grown on Ge (001)

- Z. H. Lim et. al. Journal of Applied Physics 122, 084102 (2017)

2 Charge Transfer and Built-in Electric Fields Between a Crystalline Oxide and Silicon

- Z. H. Lim et. al. Physical Review Letters 123, 026805 (2019)

3 Fabrication of $BaTiO_3$ microbridge with wet etching

- Z. H. Lim et. al. (manuscript in preparation)

1-1: Structural and electrical properties of single crystalline $SrZrO_3$ epitaxially grown on Ge (001)

Crystalline $SrZrO_3$ thin film could be a potential dielectric gate material for Ge-based MOS devices. In this project, we explore the structural and electrical properties of single crystalline $SrZrO_3$ that was grown epitaxially on Ge (001) substrate using oxide MBE. Photoemission spectroscopy shows that $SrZrO_3$ has a type-I band alignment with respect to Ge. The conduction and valence band offsets between $SrZrO_3$ and Ge are large enough to work as a dielectric gate material. Electrical characterization of the 4 nm film also reveals $SrZrO_3$ has dielectric constant of 23, and low leakage current.

1-2: Charge Transfer and Built-in Electric Fields Between a Crystalline Oxide and Silicon

The ability to tune charge transfer and built-in electric fields across oxide-semiconductor heterojunctions are useful for the development of energy harvester. In this project, we studied the charge transfer and built-in fields across $SrNb_xTi_{1-x}O_3$/ Si interface. Transport measurements of the solid solution show the formation of hole gas and built-in fields across the interface. Hard x-ray photoelectron spectroscopy analysis shows asymmetries in core level spectra due to the built-

in electric field. We also realized that by controlling the carrier concentration in $SrNb_xTi_{1-x}O_3$, we could tune the charge transfer and built-in fields across the oxide-semiconductor interface.

1-3: Fabrication of $BaTiO_3$ microbridge with wet etching

The wet etching and device fabrication of single crystalline complex oxides could lay down groundwork for functionalize complex oxide in MEMS. We report the wet etching of single crystal $SrTiO_3$ and $BaTiO_3$ films that were grown on undoped silicon substrate. The approximate etch rates were determined for films with different annealing conditions. The differences in etching rate for different annealing conditions are due to dangling bond densities in the film, crystallinity of the film, and the grain boundaries of the film. Epitaxial $BaTiO_3$ microbridge on Si (001) was fabricated utilizing conventional IC fabrication techniques. Diffraction pattern of the oxide microbridge shows that the film preserves its crystallinity after processing.

1-4: Statement of originality

The research in this dissertation was collaborative in nature, therefore I will summarize my role and the roles of others in the work in chapter 5, 6, and 7.

The growth of $SrZrO_3$ on Ge in chapter 5 was done by me and Kamyar Ahmadi-Majlan. C-V/I-V measurement and analysis were done by me. HAADF STEM image was taken by E. D. Grimley and J. M. LeBeau at North Carolina State University. XPS spectra was obtained and analyzed by Y. Du and S. A. Chambers at Pacific Northwest National Laboratory. The XRD and direct-space map of the heterostructure was obtained by M. Bowden at Pacific Northwest Laboratory (PNNL).

In chapter 6, the Nb-doped $SrTiO_3$ film grew on Si was done by me and Matthew Chrysler. Transport measurement was done by me and the LabView program that is used for transport measurement was written by Patrick Conlin and Ricky Hensley from UTA and updated by me. Transport measurement data was obtained and analyzed by me. HAADF STEM image was taken by A. N. Penn and J. M. LeBeau at the North Carolina State University. Hard x-ray photoelectron spectroscopy spectra were taken by N. F. Quackenbush, J. C. Woicik from National Institute of Standards and Technology, along with the help of J. M. Ablett from Synchrotron SOLEIL and T.-L. Lee from Diamond Light Source, Ltd. Conventional XPS spectra and all HAXPES/XPS related data analysis was done by P. V. Sushko and S. A. Chambers at PNNL. HAXPES measurement was done at Diamond Light Source, UK as well. ToF-SIMS measurements were performed at PPNL by Z. Zhu. Real space map measurements of the samples were performed at PNNL by M. Bowden. Poisson-Schrodinger solver code was developed by Dr. Ngai.

In chapter 7, $BaTiO_3$ and $SrTiO_3$ film was grown by me, Kamyar Ahmadi-Majlan, and Matthew Chrysler. Wet etching rate of materials was determined by Matthew Chrysler. XRD measurements were done by D. P. Kumah and his student at North Carolina State University. Diffraction pattern of microbridge was taken by J. M. LeBeau and his student at North Carolina State University. The photomask design and the fabrication recipe were developed by me, while the masks were made at University of Texas at Dallas.

Other than the research mention in this dissertation, I was also collaborating in two other projects. I have helped with the growth of $LaTiO_3/SrTiO_3$ film, and transport measurement along with data analysis mentioned in Kamyar Ahmadi-Majlan et. al. Applied Physics Letters, 112,

193104, (2018). In addition, I have help with the film growth of $SrZr_xTi_{1-x}O_3$ films mentioned in T. Chen et. al. Applied Physics Letters 113 (20), 201601 (2018).

Chapter 2 : Complex oxide

Complex oxides with a perovskite structure (ABO_3), as seen in figure [2-1] (a), exhibit a lot of interesting properties such as ferroelectricity, piezoelectricity, flexoelectricity, metal-insulator transition. [6] [7] Generally, rare-earth or alkaline-earth metals occupy the A-site, while the B-site cation of perovskite oxides is a 3d transition metal (Ti, Ni, Mn, etc.), which provides a large phase space for us to work with due to some of its properties that only transition metal oxides contain. [8] The perovskite oxide structure has the A-site ion siting at the eight corners of the cubic structure. Whereas the B-site transition metal (TM) is sitting at the center of the cube, and it is connected to six oxygens, which form an octahedral structure. Changing the A-site or B-site cation will lead to a different compound that exhibit different material properties. Figure [2-1] shows an example of a generic phase diagram of a material with substitution of A-site cation. When there is no substitution of A-site cation, the material will have “phase 1” behavior. As the substitution of the A-site cation concentration increase, the material will exhibit “phase 2” behavior as the substitution concentration reaches certain point. Therefore, as an example, we can tune the material’s behavior by switching out A-site cation.

The substitution of cation could affect the electronic structure of the material in two different ways, namely bandwidth control and filling control. [8] The bandwidth control can be explained with the oxide’s crystal structure. While the filling control is how electron relates to carrier density.

As one of the methods to control the electronic structure, bandwidth control can be understood by the distortion of the crystal structure. For a cubic perovskite structure where the angle between TM-oxygen-TM bond is 180^o, the overlap between the TM d-orbital and oxygen

p-orbital is maximum. The overlapping of d-orbital and p-orbital is called the hybridization, [9] which creates new continuous bands to allow electron to hop between two different titanium sites. However, if we start switching the A-site cation of a cubic perovskite structure with a larger size cation, the crystal structure will lose its symmetry and the bond angle between TM-oxygen-TM will be < 180°. Due to the structural distortion, the TM-oxygen-TM bond will rotate along the z-axis as seen in figure [2-2] (b). [10] With the bonding angle θ < 180°, the orbitals hybridization of the distorted structure decreased, which prevent the electron to hop between TM ions. The size of the A-site ion and B-site ion could be used to estimate the distortion of the cubic structure with Goldschmidt's tolerance factor. Goldschmidt's tolerance factor (t) can be calculated using $t = \frac{(r_A + r_O)}{\sqrt{2}(r_B + r_O)}$, where r_A is the radius of the A-site ion, r_B is the radius of the B-site ion, and r_O is the radius of oxygen. [11] For a cubic perovskite structure, the tolerance factor could range between 0.89 and 1.

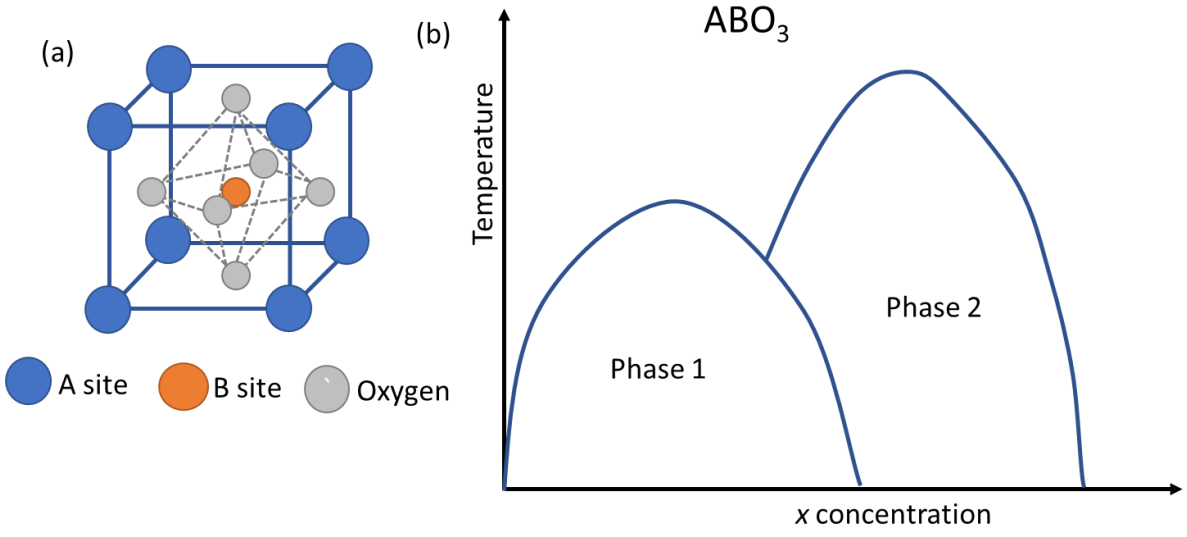


Figure 2-1:(a) Crystal structure of cubic perovskite structure. A-site cations sit at the structure's corner, while B-site cation sits at the center. B-site cation is also connected to 6 oxygens to form octahedral structure. (b) Generic phase diagram of a perovskite complex oxide (ABO_3)

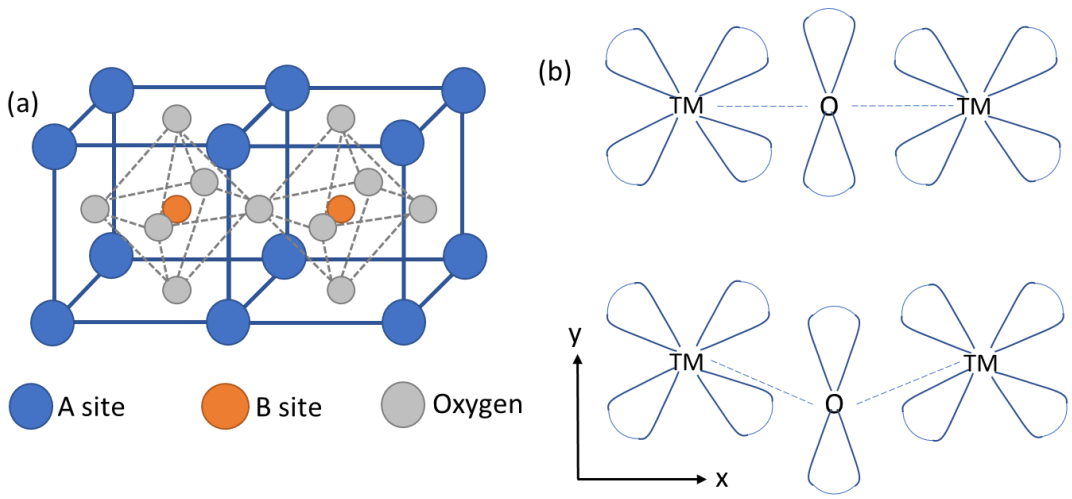


Figure 2-2: (a) Two perovskite structure unit cells that connect in line. (b) The bonding angle between Ti-O-Ti for cubic (top) and distorted structures (bottom). The octahedral of distorted structure will rotate in x-y direction, which causes bone angle to be < 180°.

Another method to affect the electronic structure is through filling control. For example, $SrTiO_3$ (STO) is a band insulator due to its large indirect band gap of 3.2 eV and there is no free electron in the structure. Sr has an electron configuration of [Kr] $5s^2$, which indicates that it has two electrons in the outer most 5s orbital. Sr tends to give up the two electrons from its outer most shell in order to stay in the stable state (Sr^{2+}). The same theory can be applied to Ti, which has electron configuration of [Ar] $3d^2$ $4s^2$. In order to stay in the most stable state (Ti^{4+}), Ti will give up 4 electrons from 3d and 4s orbitals. As for oxygen, which has 6 outer most shell electrons, will try to take in 2 electrons to stay in stable state (O^{2-}) with electron configuration [Ne]. So, the six free electrons coming from Sr and Ti are completely taken by the three oxygen. Therefore, there is no free electrons in STO structure. If we substitute Ti with another transition metal, such as Nb, this will make the $SrNbO_3$ (SNO)structure to exhibit metallic behavior due to the extra electron coming from Nb. Nb has electron configuration of [Kr] $4d^4$ $5s^1$ and will try to give up 5 electrons to stay in the stable state (Nb^{5+}), which means there is one extra free electron

than Ti^{4+}. In theory, $SrNbO_3$ has a cubic structure, which indicates all three t_{2g} states are degenerate. [12] So, the extra free electron from Nb can be placed in any of the t_{2g} states and make the structure to have metallic behavior. Figure [2-3] shows the d-orbital energy states for both $SrTiO_3$ and $SrNbO_3$, where the states are empty for $SrTiO_3$ and there is one electron occupies one of the lowest states in $SrNbO_3$. A solid solution, such as $SrNb_xTi_{1-x}O_3$, will have a mixture of energy states of both $SrTiO_3$ and $SrNbO_3$, where the t_{2g} states are partially filled by electron.

Figure 2-3: d-orbital energy states of STO (left) and SNO (right). STO energy states are empty since there is no free electron. Whereas one free electron from Nb will occupy in one of the t_{2g} degenerate states in SNO.

One of the reasons that transition metal oxides exhibits interesting properties is due to its splitting in d-shell orbitals. This splitting, as seen in figure [2-4], can be explained by the crystal field theory (CFT). [13] In general, there are five degenerate states in the d-shell orbitals, and they are $d_{z^2}, d_{x^2-y^2}, d_{xy}, d_{xz}$ and d_{yz}. The splitting of those degenerate states is due to the chemical environment of transition metal ions. Figure [2-5] shows that the transition metal ion electron orbitals of two of the degenerate states, $d_{z^2}, d_{x^2-y^2}$, are very close to the oxygen, which causes the energy to be slightly higher then d_{xy}, d_{xz} and d_{yz} states due to electron-electron

repulsion. The gap of the splitting is generally name as Δ_{oct} if it is a transition metal oxide that has octahedral structure. The higher energy states are called the "e_g" states, while the lower energy states are called the "t_{2g}" states. Moreover, according to Jahn-Teller theorem, for structure that is distorted from its original shape can make the t_{2g} and e_g orbitals split into different states. [13] [14] For a cubic structure that elongate along the z-axis to form a tetragonal structure, as seen in figure [2-6], which shows the schematic diagram of the distorted transition metal oxide structure. The bond lengths in the z-axis direction increase while the bond lengths in the x-axis and y-axis decreases in order to conserve the volume. The variation in bond lengths break the degeneracy in e_g orbitals and cause the d_{z^2} state has lower energy than $d_{x^2-y^2}$ energy state due to smaller electron-electron repulsion in z-axis direction. The same theory can apply to t_{2g} orbitals, that split them into d_{xy} state that has a slightly higher energy, and d_{xz}, d_{yz}, which have slightly lower energy as seen in figure [2-7].

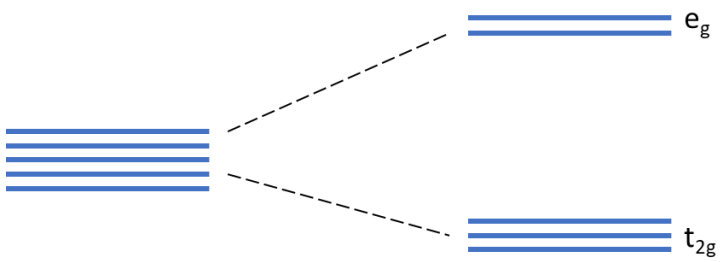


Figure 2-4: Schematic of crystal field splitting of d-orbital shell of a transition metal oxide, where e_g orbitals have higher energy and t_{2g} orbitals have lower energy

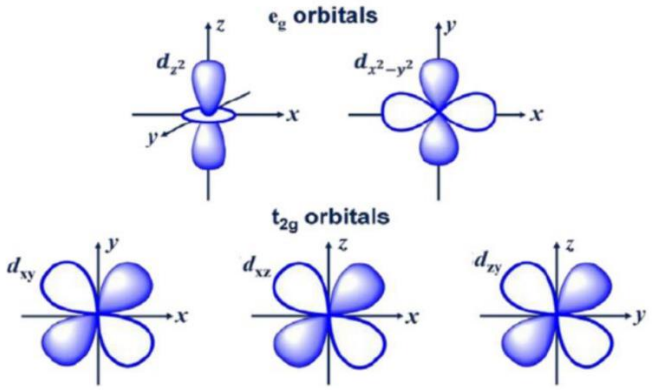


Figure 2-5: Diagram of d-orbital electron band of a transition metal. The electron orbitals of d_z^2 and $d_{x^2-y^2}$ is closer to the oxygens, which make them has a higher energy as compare to d_{xy}, d_{xz}, and d_{yz} orbitals. (taken from Biswas A., Kim K., and Jeong Y. H. "Metal–Insulator Transitions and Non-Fermi Liquid Behaviors in 5d Perovskite Iridates." Perovskite Materials. IntechOpen, 2016.)

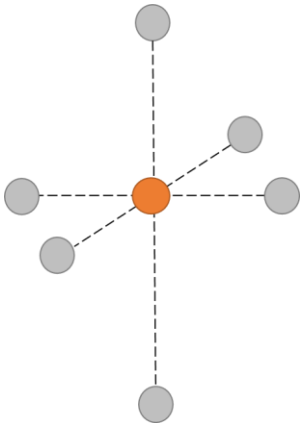


Figure 2-6: Schematic of a distorted Ti octahedral which is elongated along the z-direction. The bond lengths in the z-direction increase while the bond lengths in x- and y-directions decrease.

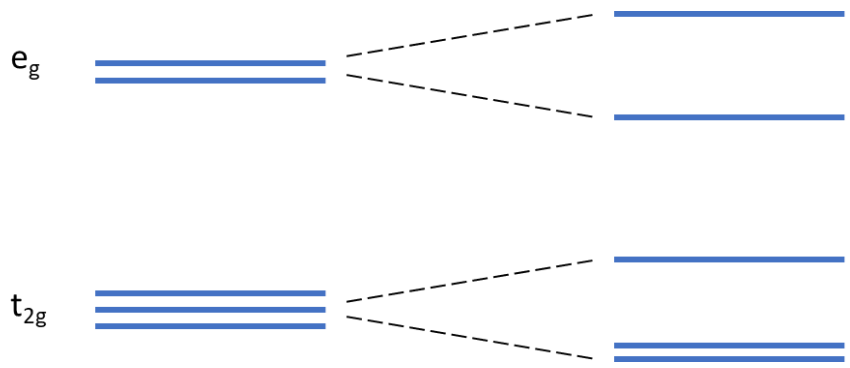


Figure 2-7: The splitting of d-orbital energy states due to Jahn-Teller effect. In e_g orbitals, the d_{z^2} state has lower energy than $d_{x^2-y^2}$ energy state due to smaller electron-electron repulsion. In t_{2g} orbitals, the d_{xy} state has a slightly higher energy than d_{xz} and d_{yz} states.

For a general transition metal oxide with free electrons, the occupation of electron in energy states will follow Pauli's exclusion principle and Hund's rule. Pauli's exclusion principle states that no two electrons with the same spin can occupied the same energy state and Hund's first rule states that to minimize the electron-electron repulsion interaction, electrons are more likely to occupy in different orbitals. [15] But it is worth noting that, Hund's first rule only hold for cases where Δ_{oct} is small, where the electron-electron repulsion energy in the same state is larger than Δ_{oct}. If Δ_{oct} is large as compare to electrostatic repulsion, then the electron could try to fill up the low energy t_{2g} states before filling in high energy states, and this is what we call the low-spin configuration. Figure [2-8] shows a schematic of the low-spin and high-spin configurations, and how electrons fill in the energy states in both cases.

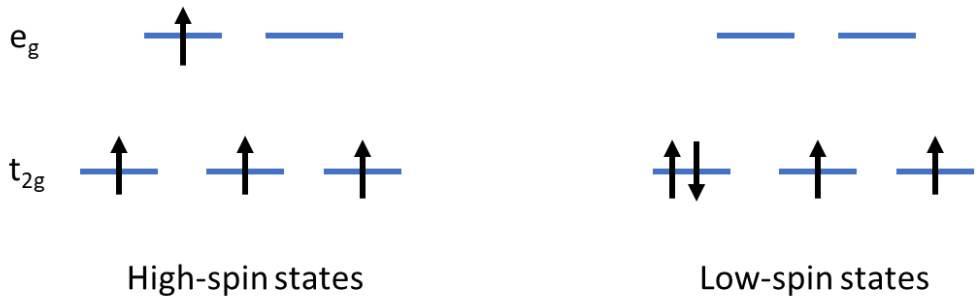


Figure 2-8: Schematic of difference between how electron occupied energy states for high-spin and low-spin configurations. The electrons will occupy different energy states since Δ_{oct} is small for high-spin states. While the electrons will occupy the low energy states before the high energy states since Δ_{oct} is large as compare to electrostatic repulsion.

In my research, I proposed the use of complex oxides for future application in energy harvesting, sensing, and computing technologies. I will focus on the semi-conducting, dielectric, and piezoelectric properties of complex oxides in order to address the issues I have mentioned in the previous chapter. I will also utilize the effect of switching out either the A-site or B-site cation to tune the complex oxides' behaviors for different project.

Chapter 3 : Oxide Molecular Beam Epitaxy

Molecular Beam Epitaxy (MBE) is a technique that is widely used for single crystal thin film deposition. MBE system typically consists of a few thermal effusion cells or e-beam evaporators that can heat up materials to their sublimation or melting temperature in order to evaporate ultra-high purity materials to deposit on the substrate. One of the advantages MBE has over some other thin film deposition technique is its atomic layer by atomic layer growth technique. [16] [17] MBE chamber is usually under ultra-high vacuum (UHV), so the growth process is under a very clean environment with no unwanted particles and gas molecules to contaminate the single crystal growth.

The MBE system in our lab was home built by Dr. Ngai and previous students, as seen in figure [3-1] (a). Our MBE system has a base pressure in the ~ 10^{-10} Torr. The system is also equipped with a load lock system for substrates exchange. Both the main chamber and load lock were pumped by two different cryogenic vacuum pumps. The cryopump uses compressed helium gas to cool down to around 10 K. As the cryopump cool down to around 10 K, most of the gases could be condensed on a cold surface and trapped on the surface. For some lighter gases such as helium and hydrogen, which have condensation temperature lower than 10 K, charcoal is used as an adsorbent to adsorb those lighter gases. There are 5 effusion cells and an e-beam evaporator installed in our system, where they are all covered by independent shutter that could use to control which material to deposit on to the substrate. Those 5 effusion cells contained 3 high temperature cells from Veeco and 2 low temperature cells from SVT and Veeco. High temperature cells can heat up to as high as 2000 ^{o}C, which are used to heat up materials like Lanthanum, Titanium etc. Our low temperature effusion cells are used to heat up Strontium, Manganese etc. E-beam evaporator is used for materials that have very high melting or

sublimation temperature, for example Nb and Zr. Our e-beam evaporator is from Thermionic Inc. In addition, our system also has a Residual Gas Analyzer (RGA) from MKS Instruments. It is a very useful tool to monitor molecules in our chamber, since it could detect any molecule's partial pressure as low as ~ 10^{-10} Torr regime in our system. A quartz crystal microbalance (QCM) from Inficon was also installed in our system for us to measure the flux of the materials. A quartz disc, which is a piezoelectric material, that is installed in the QCM will oscillate at resonant frequency. The oscillation frequency will change if there are materials deposit on top of it, and the change in frequency can be related directly to the mass of the deposited materials. So, by measuring the change in frequency, QCM can also determines the material deposition rate. Moreover, a substrate manipulator was utilized to hold the substrate. It can rotate the substrate during growth in order to increase the uniformity of the deposited thin film. A radio frequency (RF) plasma gun was also installed in the system to create oxygen ion for us to oxidize the substrate surface. The RF plasma gun will provide signal with enough energy to strip electron away from the oxygen molecule in order to create oxygen ion that is reactive to substrate surface. Lastly, our MBE was equipped with Reflected High Energy Electron Diffraction (RHEED) system from SVTA. The schematic drawing of the MBE system is shown in figure [3-1] (b).

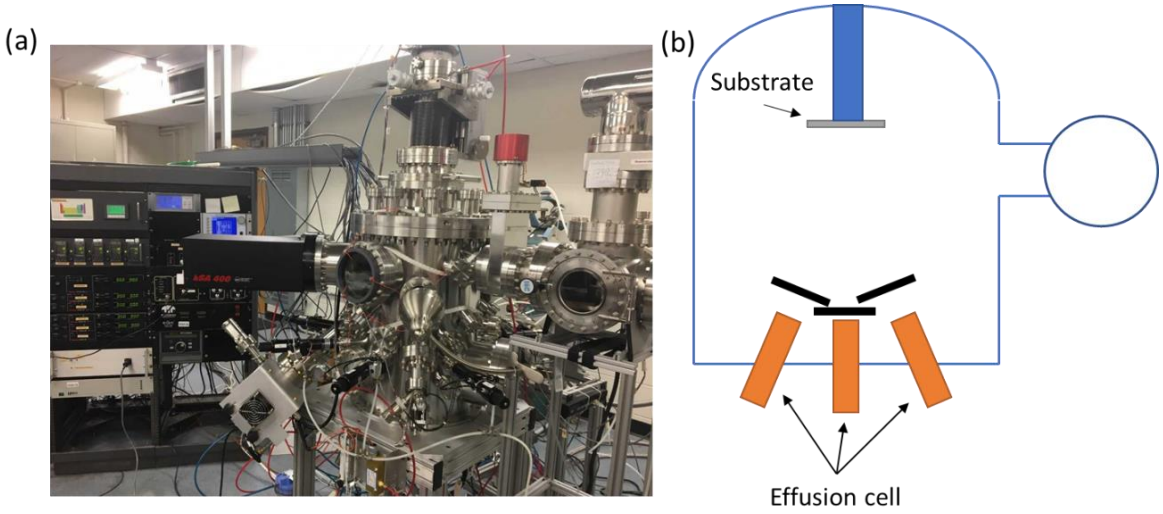


Figure 3-1: (a) Oxide MBE system in Dr. Ngai's lab. (b) Schematic of the oxide MBE system, where all effusion cells are covered with independent shutters.

The setup of RHEED consists of an electron gun and a photoluminescent detector screen. The gun was set up at a very small incident angle with respect to the substrate as seen in figure [3-2]. [18] As electron beam hits the surface, the electron will scatter from the thin film surface and forms constructive interference pattern on the detector screen if the films are crystalline. The incident electron wave has a wavevector *k*. Wavevector *k* is related to the wavelength of the electron wave, and the relationship can be written as $k = \frac{2\pi}{\lambda}$. Therefore, the magnitude of the electron wavevector depends on the energy of the electrons as well. For elastic scattering, the magnitude of the incident electron wavevector (k) will equal to the magnitude of diffracted electron wavevector (k'). The endpoint of the diffracted electron wavevector will land on a sphere with radius $|k|$, which the sphere is called the Ewald sphere. Since, RHEED is very surface sensitive, so diffraction pattern will only show the top layer of the film, which is like a 2-dimensional material. For a 2-dimensional material, the reciprocal lattice points of the material in the 3-dimensional space will no longer be point like. Since 2-dimentional material has no

thickness, so the reciprocal lattice in the z-direction is $\frac{2\pi}{0}$, which causes the reciprocal lattice to extend and become reciprocal rod. The RHEED pattern will form at where the reciprocal rods from the thin film surface intersect with the Ewald sphere as seen in figure [3-3]. The RHEED pattern intensity is also widely used to determine the roughness of the film and the number of layers of growth has been completed from the intensity oscillations. [19]

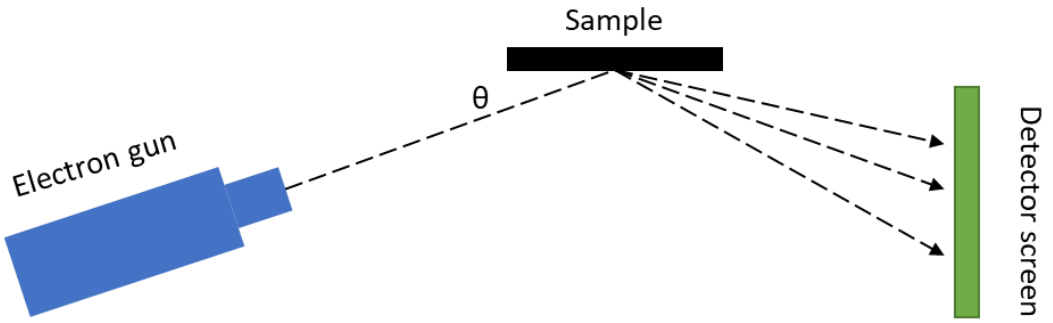


Figure 3-2: Schematic of RHEED setup, where the electron gun is set at a very small incident angle θ with respect to the substrate. The diffraction pattern of the material surface will show up on the detector screen.

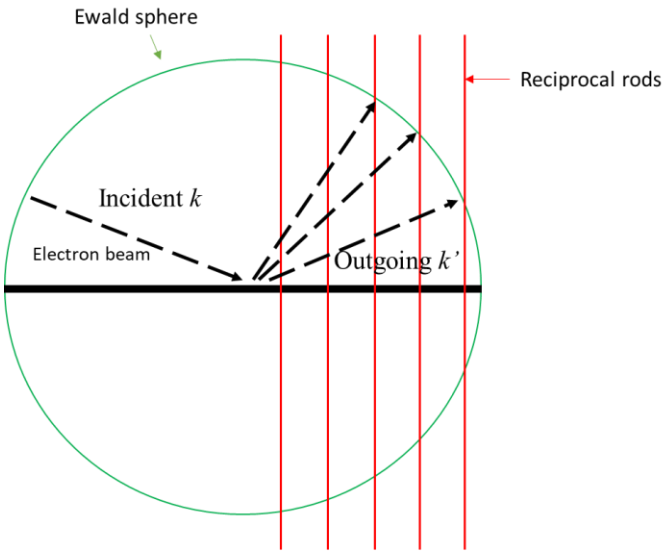


Figure 3-3: Schematic of the Ewald construction. The endpoint of the outgoing k' will land on Ewald sphere. RHEED spots will form at where the outgoing k' intersects with reciprocal rods.

RHEED can be used to confirm the crystallinity of the film during growth process. As the substrate rotates, the RHEED pattern on the detector screen will also change. Figure [3-5] (a), (b), and (c) show RHEED images taken along the [10], [11], and [21] directions respectively of a perovskite structure. The distance between the RHEED streaks is inversely proportional to the distance between sample lattice planes since RHEED pattern is in the reciprocal space. Figure [3-4] shows a schematic of different lattice planes of a cubic structure in real space. The distance between [21] lattice plane is the smallest, which explain the largest distance between the RHEED streaks along the [21] direction. Figure [3-5] (d), (e), and (f) also show RHEED images of film that are no longer 2-D, due to random dots (circle by red color) and splitting (circle by orange color) on the images. The random dots appear on the RHEED images can be understand as the beginning of 3-D island growth or the film starts turning into polycrystalline. Whereas the split in the streak is because of multi-level growth, i.e. the film is rough. Figure [3-6] is a schematic drawing of different type of RHEED images correlates to different type of growths. [18]

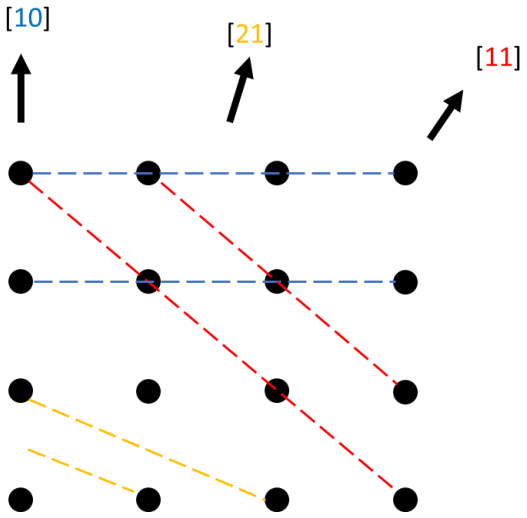


Figure 3-4: Different lattice planes of simple cubic structures. The directions of [10] (blue), [11] (red), and [21] (yellow) are pointed out by arrows.

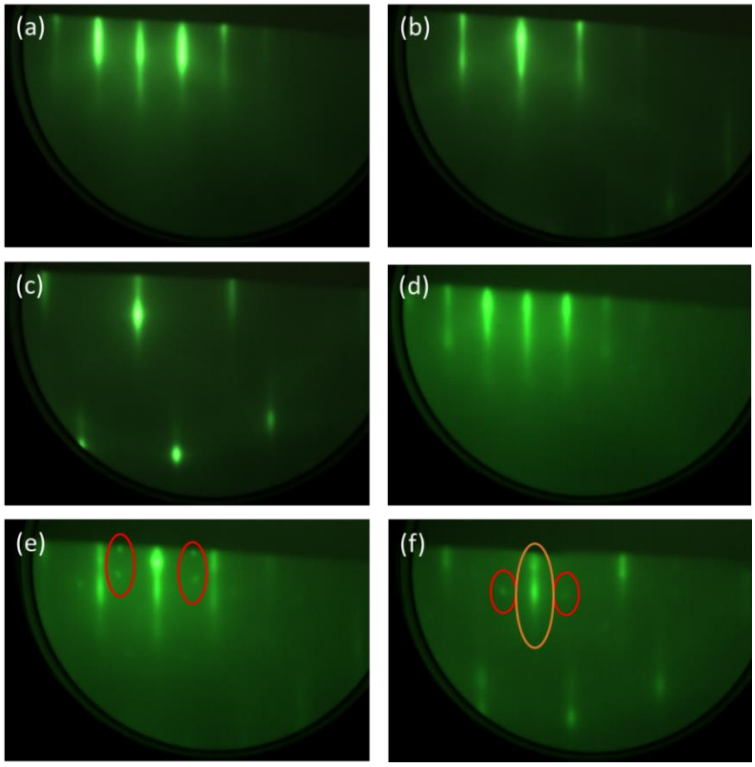


Figure 3-5: RHEED pattern of perovskite structure along the (a) [10], (b) [11], and (c) [21] direction. (c), (d), and (e) show the RHEED pattern of film with very rough surface along the [10], [11], [21] directions respectively. Random dots circle by red color indicates the beginning of 3-D island growth, while the streak splitting (circle by orange color) is due to rough surface.

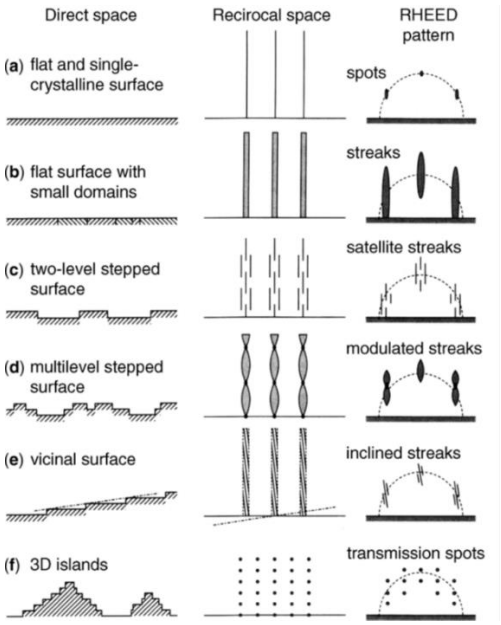


Figure 3-6: Different type of growths with their corresponding reciprocal space and RHEED pattern. [18]

Growth of STO on Si

In order to functionalize complex oxide and discover new device physics, it is necessary to be able to integrate complex oxide on silicon. The growth method of complex oxide $SrTiO_3$ (STO) thin film on Si was first developed by McKee et al. [3] With this approach, our group has always grown at least 2.5 unit cells (u.c.) of STO on Si substrate as a buffer layer or platform for any subsequent growth. Strontium desorption method was utilized to get a clean Si before the deposition of the first 0.5 monolayer (ML) of Sr. [20] This first 0.5 ML Sr on silicon is the most crucial part of the growth as it determines the base for all subsequence growth. In order to get the first 0.5 ML Sr on clean Si, a certain recipe was used as seen in figure [3-7]. The Si substrate was first exposed to oxygen plasma to remove any organic from the surface and get the surface oxidized. Then, two monolayers of Sr were deposited when the substrate was at 550 ^{o}C and the substrate was heated to 870 ^{o}C right after the deposition. Figure [3-7] (a) shows the RHEED image of the substrate at 870 ^{o}C, which contain a 2×1 due to the formation of dimers on the clean surface. The substrate was then cooled down to 660 ^{o}C, and the RHEED showed the formation of $2 \times 1 \rightarrow 3 \times 1$ as seen in figure [3-7] (c). This formation of 3×1 is coming from the residual Sr settle down to form a 1/6 ML on the surface as seen in figure [3-7] (d). When the substrate was cooled down to 660 ^{o}C, we deposited more Sr until the RHEED image showed a 2×1 reconstruction (figure [3-7] (e)), which indicates that we now have exactly 0.5 ML Sr on Si (figure [3-7] (f)). The reason of STO, which has a lattice constant of 3.905 Å, can be grown epitaxially on Si is because Si has a unit cell of 3.84 Å in length. So, STO will rotate 45^{o} when it is grown on Si as seen in figure [3-8] below. The small difference between STO lattice constant and Si unit cell length will induce compressive strain especially at the interface.

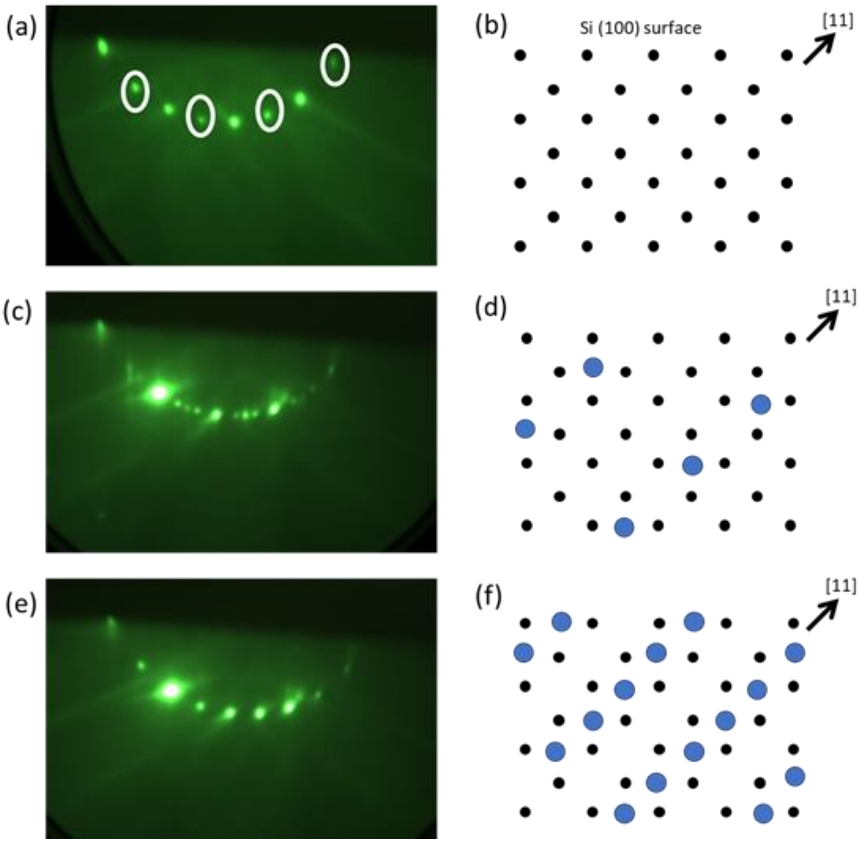


Figure 3-7: (a) and (b) are the RHEED pattern of clean Si surface and a schematic drawing of clean Si lattice. (c) and (d) are the RHEED pattern and how 1/6 monolayer Sr atoms sit on clean Si surface. (e) and (f) are the RHEED pattern and how 1/2 monolayer Sr atoms sit on Si surface.

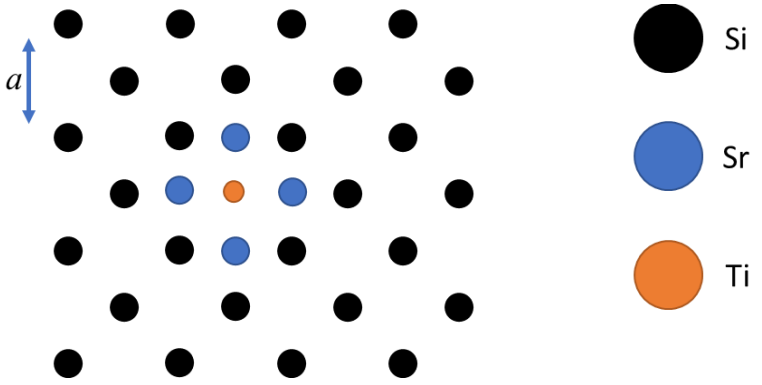


Figure 3-8: Schematic of how STO unit cell sits on Si unit cell. STO unit cell will rotate 45^{o} when it is grown on Si in order to compensate the large lattice constant mismatch between STO and Si.

Chapter 4 : Characterization technique

4-1: Capacitance-Voltage and Current-Voltage measurement

Capacitance-Voltage and Current-Voltage (C-V and I-V) are two methods to characterize semiconductor materials and devices electrically. They are widely used to determine the dielectric constant of metal-oxide-semiconductor capacitor (MOSCAP) structure. [21] [22] The technique is to measure the capacitance and leakage current of the dielectric materials while vary the voltage bias. The capacitance and the current data are then plotted out as a function of voltage bias.

In a MOSCAP, the total capacitance of the system is the sum of oxide layer capacitance and semiconductor depletion-layer capacitance. As seen in figure [4-1] (a), since the oxide capacitor is in series with the semiconductor depletion-layer capacitor, the total capacitance can be written as $\frac{1}{C_{tot}} = \frac{1}{C_{OX}} + \frac{1}{C_D}$, where C_{OX} is the oxide capacitance and C_D is the depletion-layer capacitance. [21] C_D is a variable capacitance that can be estimated using $C_D = \frac{\varepsilon_s}{W_D}$, where ε_s is the permittivity of semiconductor and W_D is the depletion width. In fact, the measured capacitance variation in C-V measurement is due to the variation of C_D. Figure [4-1] (b) showed a schematic plot of a C-V curve with high and low frequencies. If there is no depletion-layer capacitance, C-V measurement will show a straight horizontal line, since the oxide capacitance is generally independent from applied voltage.

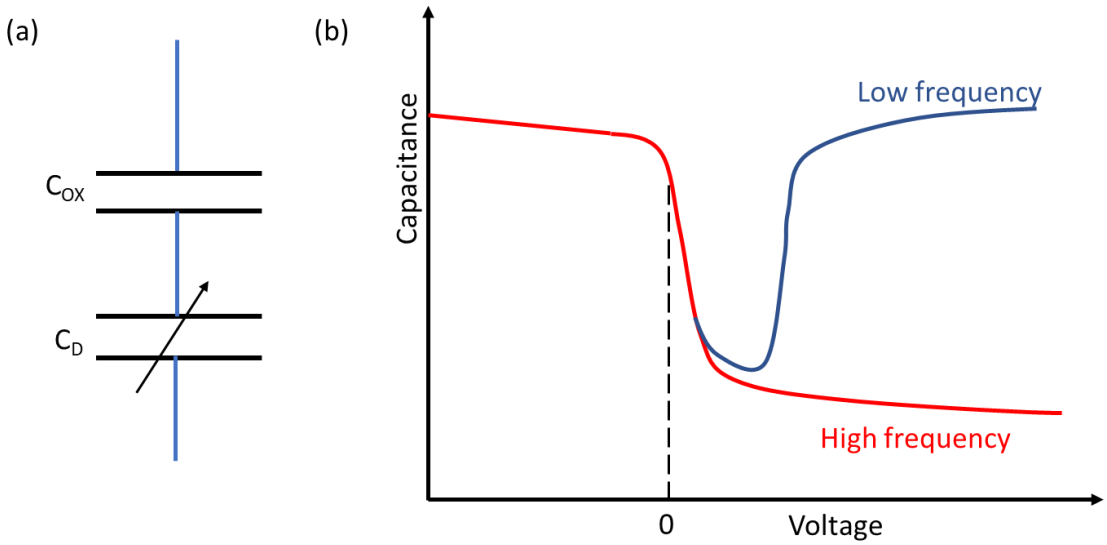


Figure 4-1: (a) The total capacitance in CMOS includes the capacitance of depletion layer in semiconductor and the capacitance of oxide layer, where the capacitor of depletion layer in semiconductor is in series with capacitor of oxide layer. (b) Schematic of C-V curve of high and low frequency. For low frequency C-V, the capacitance will increase due to inversion.

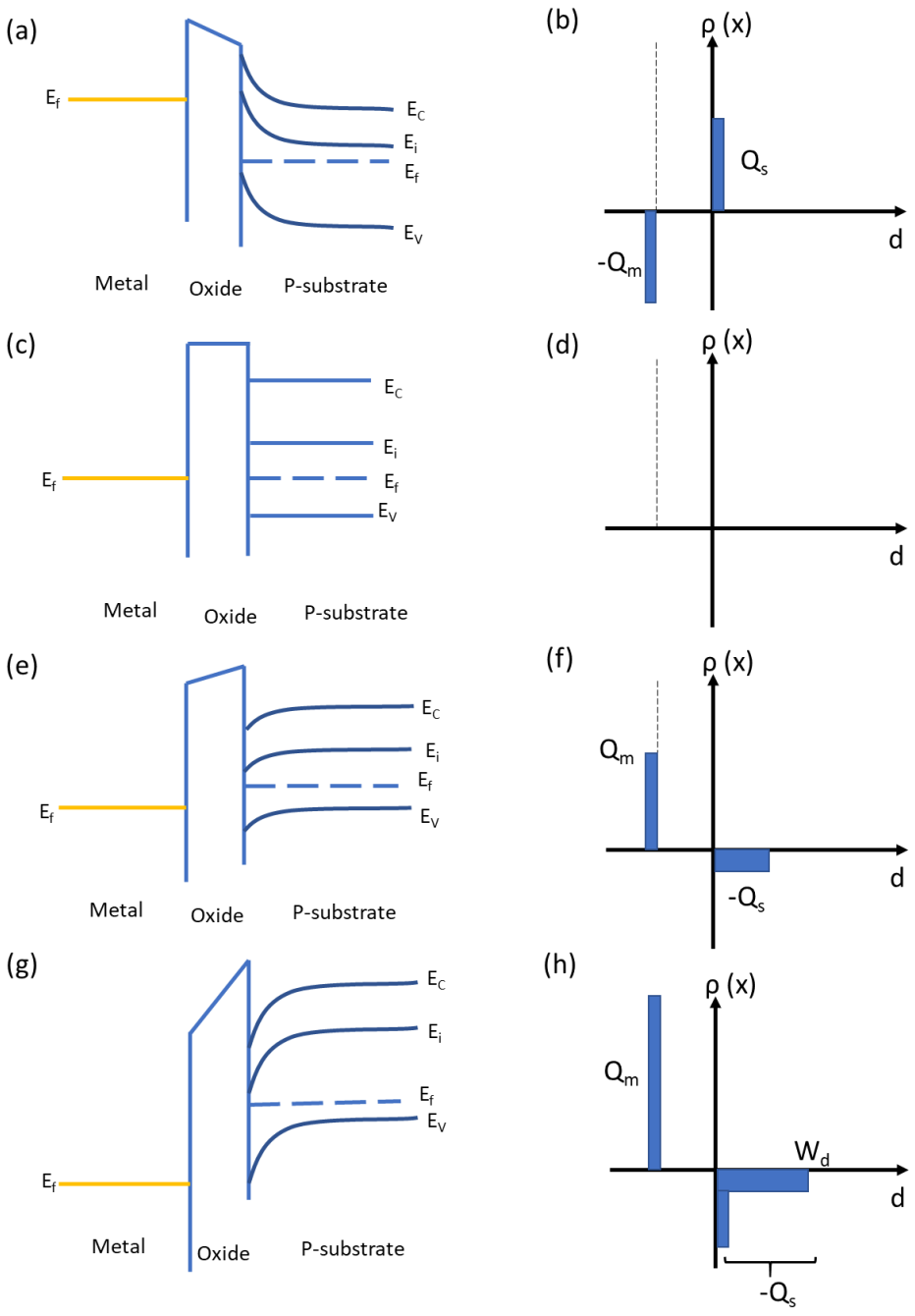


Figure 4-2: Band diagram of MOS heterostructure in (a) accumulation, (c) flat band, (e) depletion, and (g) inversion cases. Charge distribution diagram of MOS structure in (b) accumulation, (d) flat band, (f) depletion, and (h) inversion cases. In accumulation case, hole carriers in the semiconductor are attracted toward the oxide-semiconductor interface, and there is no depletion layer. In flat band case, there are no charges in the charge distribution diagram since there is no net difference in charge across the heterojunction. In depletion case, charges in the semiconductor will first fill in the depletion layer. As the supplied charges keep increasing, the charges in semiconductor fill up the whole depletion layer, and the extra charges will accumulate at the oxide-semiconductor interface, which causes the inversion.

For a perfect p-MOS, the electronic properties of the heterojunction can be explained by 4 cases, along with their band diagram and charge distribution diagram. When the biased voltage applied to the metal gate is less than 0 V, the hole carriers in the substrate will be attracted toward the oxide-semiconductor interface, where there is no depletion layer in semiconductor, and this is called the accumulation case. Figure [4-2] (a) shows the band diagram of a metal-oxide-semiconductor (MOS) heterostructure in accumulation case, while figure [4-2] (b) shows the charge distribution in accumulation case. [22] Due to the requirement of charge neutrality in the system, it is necessary to have Q_m, the charge per unit area on the metal, equal to Q_s, the charge per unit area in the semiconductor. In accumulation case, the measured capacitance is the total capacitance of the oxide layer. As the biased voltage increases, the conduction and valence band of the oxide and the semiconductor would be flat when the biased voltage applied to the metal gate reaches 0 V, which is called the flat band case. Figure [4-2] (c) and (d) show the band diagram and charge distribution of a MOS heterostructure in flat band case. Since there is no net difference in charge across the heterostructure in flat band case, so there are also no charges in the charge distribution diagram for flat band case. When the biased voltage applied to the metal gate keeps increases, the MOS heterostructure will get to the depletion case, where carriers occupy the acceptor states in the semiconductor, and then inversion case depends on the signal frequency. Figure [4-2] (e) and (f) show the band diagram and charge distribution of a MOS heterostructure in depletion case. When a positive voltage bias is applied to the metal, not only the charge density of the metal increases, the charges in the semiconductor will first fill in the depletion layer. As the voltage bias keeps increasing, the charges in the semiconductor will reach a maximum point in depth, at which conduction band approaches the Fermi energy, causing inversion to occur. This maximum point in depth is the depletion width W_d in the semiconductor.

The reason why inversion occurs at low frequency is because the recombination-generation rates of the minority carriers in the substrate can keep up with the variation frequency of the AC signal. [21] This allow the minority carriers exchange with the majority carriers in the substrate, which shows the increase in capacitance with increasing gate bias as compare to no increase in capacitance at high frequency measurement.

With the C-V measurement, we could also use it to study the interface-trapped charge (Q_{it}). The interface-trapped charge was seen exist at the oxide-semiconductor interface due to the interruption of the periodic lattice structure. [23] [24] One way to tell if there are any interface-trap states in the CMOS structure is by looking at the C-V data. If the C-V data shows hysteresis with sweeping gate voltage bias, then it is very likely that there are interface-trap states in the structure. There are a few different methods to calculate the interface-trap density, and the calculation detail of one of the ways we used (High-Low Frequency method) will be discussed in chapter 5. [25]

In a low frequency measurement mode, the interface-trap states that reside in the oxide layer close to the interface will be able to absorb charges. Therefore, a larger biased voltage is needed to achieve inversion, since the supplied charges will need to first fill up the interface-trap states before filling up the depletion layer, which causes the C-V curve to stretch out to higher bias voltage. As for the high frequency measurement mode, the interface-trap states are not fast enough to take in charge, therefore interface-trap states don't affect the C-V curve too much. In this regard, we could treat the interface-trap states as another capacitor in low frequency mode as seen in figure [4-3]. Figure [4-3] (a) shows that in low frequency mode, the capacitance from interface-trapped states, $C_{it,}$ is in parallel with capacitance from depletion layer, C_D, while in the high frequency mode, there is no C_{it}. Figure [4-4] also shows schematic drawing of the charge

distribution across the interface in low frequency mode. The charges will start by filling up the interface-trap states within the insulating oxide, as seen in figure [4-4] (a), before filling up the depletion layer within the semiconductor, as seen in figure [4-4] (b).

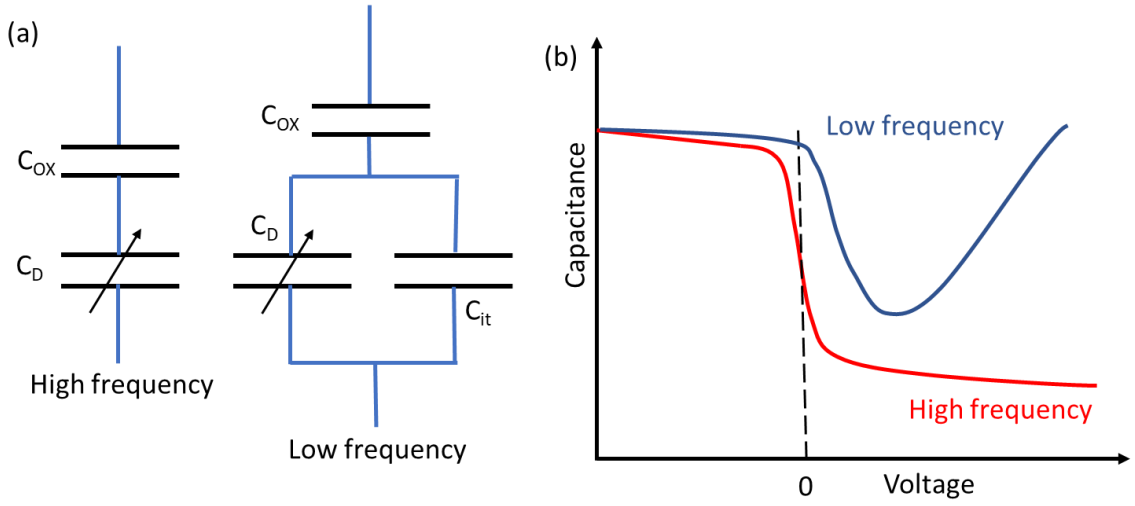


Figure 4-3: (a) Total capacitance of the MOS system for high and low frequency that include capacitance of interface-trap states. For low frequency measurement, the capacitor from interface-trap states is parallel to the capacitor from depletion layer. (b) The low frequency C-V curve will depart from high frequency C-V curve due to the effect from interface-trap states, which will cause the C-V curve to stretch out.

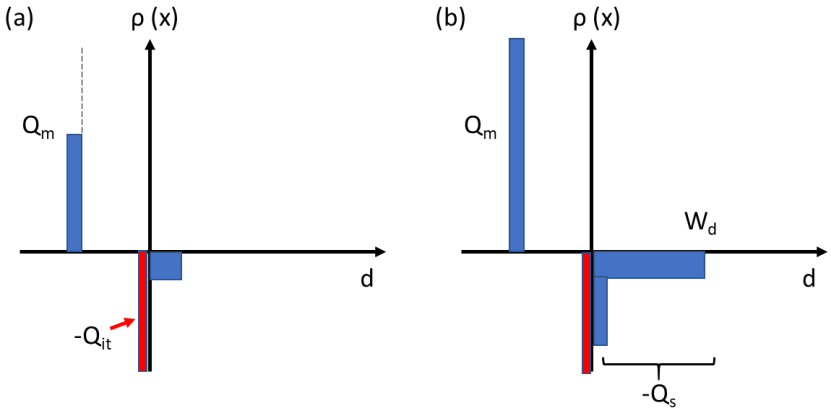


Figure 4-4: Charge distribution across heterojunction showing the charges will first fill up the interface-trap states before depletion layer.

Other than the C-V measurement, I-V measurement was used to determine the direct current through the device or semiconductor structures with an applied gate voltage bias, namely the leakage current. The leakage current is due to the conductance of the oxide layer under applied electric field. Leakage current is important in order to confirm if the device would work with the amount of voltage that supports the electronic circuit. There are a couple conductance mechanisms that could cause the leakage current, such as tunneling, thermionic emission, ionic conduction, etc. All the conductance mechanisms have certain voltage and temperature dependence, as seen in Sze et al. [21]

4-2: Van der Pauw method

Van der Pauw is a technique that is widely used to measure the resistivity and Hall coefficient in the sample because it could be used to measure samples with arbitrary shape as long as they are symmetric and have a surface area that is much larger than its thickness. [26] Four-point resistance measurement instead of two-point resistance measurement are usually used to obtain a more precise measurement because a four-point measurement was set up to eliminate the contribution from the lead and contact resistances. This is extremely important for taking a very precise measurement or very low resistance measurement. Moreover, four-point measurement is also used to determine the sheet resistance of thin film. In general, a four-point measurement is set up to have all four probes line up in a straight line, and the distance between each probe is arranged to be much larger than the thickness of the thin film. The van der Pauw method also uses the general four-point measurement technique, but the probes do not need to line up in a straight line. Instead, all four probes were set at the corner or the edges of the symmetrically shape sample as seen in figure [4-5]. [27] In figure [4-6], each contact is labeled with number 1 – 4, and this numbering system will be used for setting up the measurement.

Moreover, van der Pauw method has the advantage of determining the average resistivity of the sample, while the linear four-point measurement can only determine the resistivity in the sensing direction.

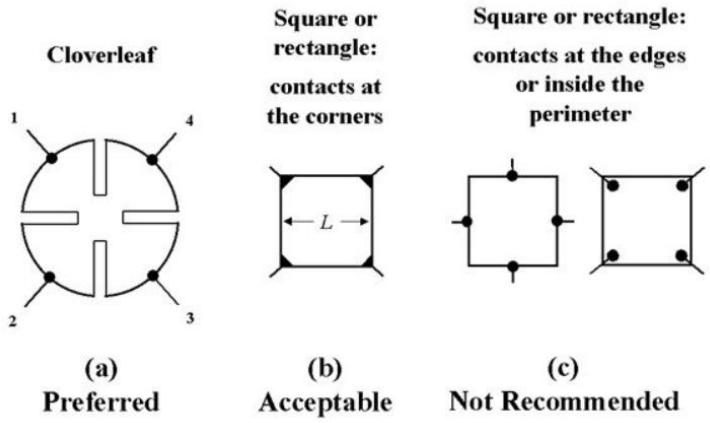


Figure 4-5: The preferred and acceptable way to make electrical contact on sample with 4 fold symmetries for van der Pauw measurement. [27]

In order to determine the resistivity and the sheet resistance of the sample, a series of resistance measurements were done with different combination of sensing directions. The measured resistance component can be written as $R_{12,43} = \frac{V_{43}}{I_{12}}$, where I_{12} is the dc current input into contact 1 and output through contact 2, and V_{43} is the voltage senses from contact 4 to contact 3. There will be 8 different combinations for the measured resistances, and they could be separate out into two groups with the average of them being R_A and R_B, as shown in equation [4.1] below.

$$R_A = \frac{\left(R_{21,34} + R_{12,43} + R_{43,12} + R_{34,21}\right)}{4} \; ; \; R_B = \frac{\left(R_{32,41} + R_{23,14} + R_{14,23} + R_{41,32}\right)}{4} \qquad [4.1]$$

$$exp\left(\frac{-\pi R_A}{R_s}\right) + exp\left(\frac{-\pi R_B}{R_s}\right) = 1 \quad [4.2]$$

From R_A and R_B, we could substitute them into equation [4.2], which is the van der Pauw equation. Then, van der Pauw equation can be solved numerically in order to obtain the sheet resistance. Once the sheet resistance was determined, we can also calculate the bulk resistivity of the material using $\rho = R_s d$, where d is the thickness of the thin film. In addition, we can also do the Hall measurement along with the obtained sheet resistance in order to determine the sheet carrier density and mobility of the carrier in the thin film.

Hall effect was first discovered in 1879, and it is an effective way to study the carrier in material. [28] It is widely used to determine the sheet carrier density and mobility in thin films using the Lorentz force. When a magnetic field is applied through a conductive material, the carriers in the material will experience a force and change their conducting path depending on their charge, as seen in figure [4-6] which is a schematic of Hall effect. Hall measurement can also be done using the van der Pauw variation, where the sample set up is almost the same as resistivity measurement other than the numbering system.

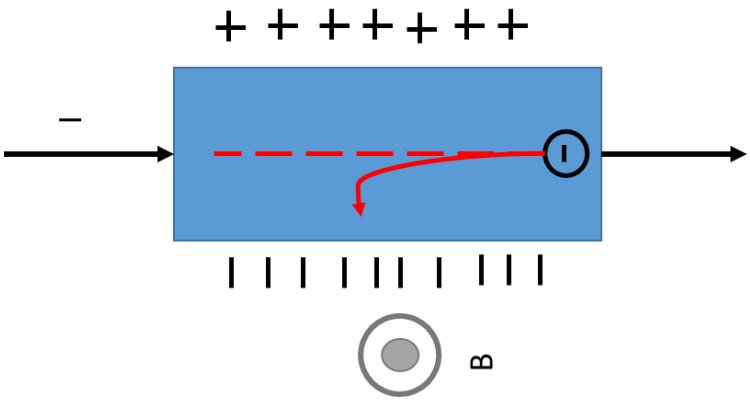


Figure 4-6: Schematic drawing of Hall effect. Magnetic field B is pointing out from the page. The electron will experience Lorentz force from the magnetic field and changes its path in the material as pointed out by the arrow. Electrons that are accumulated on one side of the material will create a potential difference in the material which is perpendicular to the current direction.

The new numbering system is shown in figure [4-7]. [27] For example, when the Hall voltage V_{24p} is measured, the current will input at contact 1 and output at contact 3, while the voltage was measured across contact 2 and 4. The "p" here indicates the magnetic field being positive. If the magnetic field is pointing in the +z direction, then the magnetic field is positive, and if it is pointing the other way around, it is negative. There are 8 different combinations of the measured Hall voltage and they could be arranged into 4 components, which are V_C, V_D, V_E, V_F. The detail on how to calculate the sheet carrier density and mobility from the Hall voltage will be shown in Chapter 6.

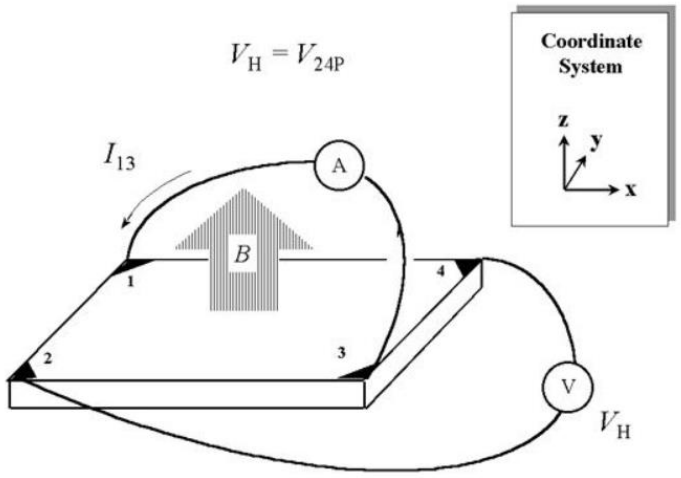


Figure 4-7: New numbering system for Hall measurement using van der Pauw method. The voltage sensing direction is perpendicular to the current direction. [27]

In the transport measurement setup, we made use of the Keithley 2400 and 2700. The Keithley 2400 is the source meter, which we use it as the current source for the measurement and use it for sensing voltage. The Keithley 2700 contains a multiplexer. During our measurement, we usually measure three samples at once every run and a multiplexer card is required to be used during measurement. The multiplexer card has the ability to turn on the required channel for

measurement, while keeping the other close. For example, the multiplexer will supply current through two different channels to the sample, while sensing the voltage from another two channels when we are taking measurement for one sample. Each sample will use four out of the twelve channels for taking measurement.

Chapter 5 : Structural and electrical properties of single crystalline $SrZrO_3$ epitaxially grown on Ge (001)

5-1: Introduction

Single crystalline complex oxide thin films have attracted attentions from researchers lately due to their interesting electronic, magnetic, and optical properties. Epitaxially grown complex oxide thin films on semiconductor substrates using Molecular Beam Epitaxy (MBE) has also open up pathway to discover the application of oxide-semiconductor structure, where akaline earth titanate $AeTiO_3$ (Ae = Ca, Sr, and Ba) is one of the most popular epitaxial platforms. [29] [30] [6] [31] For a lot of device applications, the complex oxides and the semiconductors need to be electrically coupled so that electrons can transfer from semiconductor to the oxide. In this regard, $AeTiO_3$ is the perfect candidates for this type of application due to its type-II band arrangement with respect to Ge, GaAs, and Si. [32] [33] [34] [35] In contrast, electrons transfer from semiconductor to oxide are not suitable for some other applications such as complementary metal oxide semiconductor (CMOS), which a type-I band offset is required for these applications. [36] In previous work, our group has showed that the band offset between the solid solution $SrZr_xTi_{1-x}O_3$ and Ge could be tuned continuously from type-II to type-I by controlling the Zr doping concentration, where this technique is called bandgap engineering. [37]

Conventional semiconductor-based CMOS is one of the most important devices in computing technology. Ge has gained some amount of interests recently for being one of the potential channel substrates for high performance and low power electronics, due to its higher bulk electron and hole mobilities as compare to Si. Especially for PMOS, which has high hole mobility at around 1900 $cm^2V^{-1}S^{-1}$ as compare to around 500 $cm^2V^{-1}S^{-1}$ in Si at room

temperature. [38] Due to the higher bulk electron and hole mobilities in Ge, industry has started to switch from Si-based technology to Ge-based technology. In this regard, a search for gate dielectric material for Ge-based CMOS devices is needed. In this chapter, I will present the structural and electrical characterization of $SrZrO_3$ (SZO) thin film grown on Ge substrate. I will also conclude that SZO could be a potential candidate for Ge based PMOS. I will show that SZO thin film is ideal for this purpose due to its large conduction and valence band offset, low leakage current, and the ability to modulate surface potential.

5-2: Film growth

Crystalline SZO thin films were grown on both n-type (As) and p-type (Ga) doped Ge wafer with the home built Molecular Beam Epitaxy (MBE) system in our lab. The custom built ultra-high vacuum chamber has a base chamber of $< 2 \times 10^{-10}$ Torr. The Ge wafer was first clean by chemical etching with diluted HCl and H_2O_2 before introduced into the growth chamber. [39] A 15% HCl and a 7% H_2O_2 were first made, then the Ge wafer was first dipped in 15% HCl for 20 seconds and then in 7% H_2O_2 for 30 seconds. This cleaning step was repeated for 3 times, and at the very last time, the wafer was dipped in diluted H_2O_2 for 1 minute instead of 30 seconds. After that, the wafer was rinsed in DI water and blow dried with ultra-pure O_2 gas. Once the Ge wafer was sent into the chamber, it was first heated up to 130 ^oC for 30 mins to dry off any remaining moisture and then was heated to 600 ^oC to thermally desorb GeO_x from the surface to get a clean surface. The Ge wafer was then cooled to ~ 400 ^oC and 0.5 monolayer of Sr was deposited. Another 1 monolayer of Sr was deposited in a background O_2 pressure of 3×10^{-7} Torr to form a base layer for additional growth. 2 monolayers of ZrO_2 and 1.5 monolayers of SrO were deposited at room temperature, and then the whole stack was heated up to 590 ^oC, with the film crystalized at around 510 ^oC. The subsequent SZO layers were grown at around 590 ^oC

with background oxygen pressure of 3×10^{-7} Torr at a growth rate of 1 unit-cell (u.c.) per minute. The Sr was thermally evaporated from an effusion cell while the Zr was evaporated with Thermionics electron-beam evaporator. Both of their fluxes were also calibrated using quartz crystal microbalance.

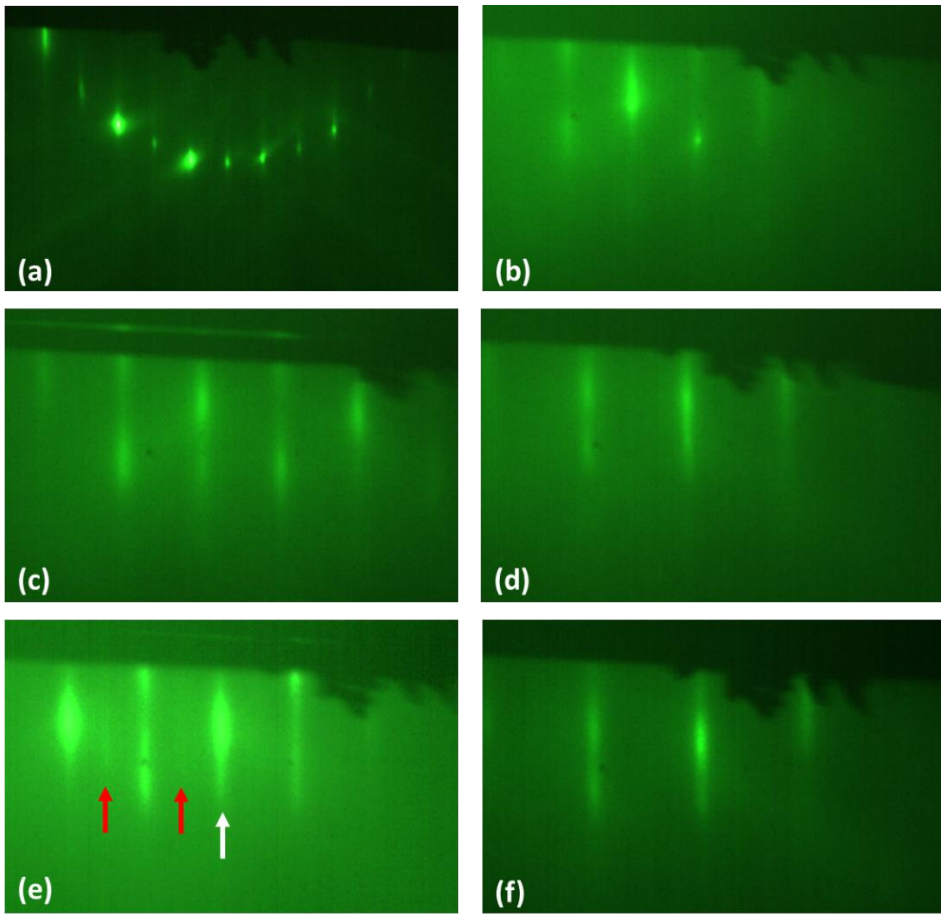


Figure 5-1: RHEED of SZO-Ge. (a) Clean Ge taken along the [11] directions. (b) With 2.5 unit-cells of SZO, taken along the [10] direction. (c) 10 u.c. of SZO on Ge taken along the [10] and (d) [11] directions. (e) 37 u.c. SZO on Ge taken along [10] and (f) [11] directions. 2 × 1 reconstruction was seen as the film thickness exceeds 22 u.c., and it is pointed out by red arrows in (e).

Reflection High Energy Electron Diffraction (RHEED) was utilized during the growth process to confirm the film's crystallinity, and the RHEED pattern is shown in figure [5-1]. Figure [5-1](a) shows a clean dimerized Ge surface, (b) shows 2 unit-cells SZO along the [10]

direction, while (c), (d), (e), (f) show the RHEED pattern of 10 and 22 u.c. SZO thin films along the [10] and [11] directions respectively. As seen in figure [5-1] (e), there was a 2×1 reconstruction when the film thickness exceeds 22 u.c. This reconstruction is consistent with a superstructure generally found in bulk SZO crystal. [40]

5-3: Electrical characterization

After growth, the wafer was broken into small pieces for different characterization purposes. The small sample pieces were first annealed at 400 ^{o}C for 5 minutes in flowing wet oxygen to minimize oxygen vacancies, which act as n-type dopants in the film. The samples were tested with different annealing time, and 5 minutes gave us the best result, while we also do not want to have a thick GeO_x layer at the interface. Then, 30 nm round shape nickel (Ni) contact pad in various area sizes were deposited through shadow mask using AJA e-beam evaporator in the cleanroom. After Ni deposition, the sample was characterized with micromanipulator probe station (Agilent technologies) for its electrical properties. Capacitance-voltage (C-V) and current–voltage (I-V) measurements were performed with the former at frequencies of 500 Hz to 1 MHz. The backside of the sample was mechanically scratched, and InGa eutectic was applied for counter electrode underneath the sample purpose. 10 μm radii tungsten probe was also used as probe connector. Figure [5-2] shows the schematic setup for electrical test. The 4 nm and 15 nm samples were also sent to Dr. Mark Bowden and Dr. Scott Chambers at Pacific Northwest National Laboratory (PNNL) for XRD and XPS measurements respectively. A 4 nm sample was also sent to Dr. LeBeau at North Carolina State University for scanning transmission electron microscopy (STEM) imaging. XRD measurements were done using a Panalytical Materials Research Diffractometer, while XPS measurements were performed using a Scienta Omicron R3000 energy analyzer with a monochromatic Al Kα X-ray source. Since all the films that were

being characterized were conductive enough to have no positive charge built up on the surface during measurement, so no charge compensation was used during the measurement. The XPS binding energy scale was calibrated with Au $4f_{7/2}$ peak from a polycrystalline Au foil, and Shirley background subtraction was used to fit all taken spectrum. A post-annealed 4 nm thick film was used for high resolution STEM imaging to determine how the post-annealing procedure affects the film interface. Conventional wedge polishing technique and argon ion milling were used to prepare the STEM sample. Probe-corrected FEI Titan G2 with 200 kV was used for high-angle annular dark-field (HAADF) STEM imaging. The detector itself has a 77 mrad as inner semi-angle, and 19.6 mrad for its probe convergence semi-angle. The images at each point of the sample were recorded with the RevSTEM method to prevent any drift related scan distortion. [41]

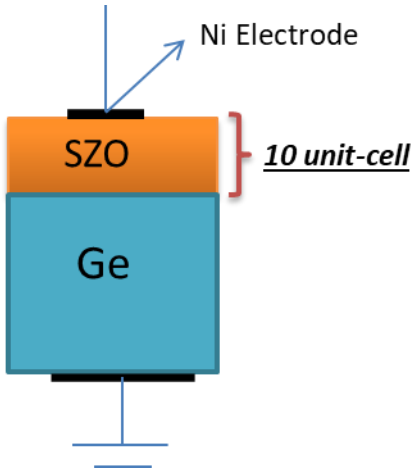


Figure 5-2: Schematic of the electrical set up for C-V and I-V measurements. Circular nickel electrode was deposited on the sample, while InGa eutectic was applied at the bottom of the substrate as counter electrode.

5-4: Results

The XRD measurements, as seen in figure [5-3], show the quantitative analysis of the 37 u.c. (15 nm) SZO film. Figure [5-3] (a) shows the survey scan of the 15 nm film while the inset shows the zoom in of SZO (002) peak. The finite thickness fringes of the rocking curve indicate that the film is about 15 nm thick and that the SZO-Ge interface and SZO surface are abrupt on the nanoscale. Figure [5-3] (b) shows the rocking curve of the film, which was measured with an analyzer crystal, has a full-width at half maximum (FWHM) of 0.63^{o} for the 15 nm thick film. The real space map of the film is shown in fig [5-3] (c). Both Ge (224) and SZO (103) peaks were measured at the same surface normal angle to obtain the real space map result. The lattice constant of SZO was multiplied by $\sqrt{2}$ to compare with the lattice constant of Ge since the perovskite SZO rotated 45^{o} with respect to the diamond cubic Ge substrate. As seen from the real space map, we can also conclude that the 15 nm SZO film was mostly relaxed since the d_{xy} of the measured SZO and Ge have a difference of roughly 0.2 Å. The calculated u.c. volume of our SZO film is about 68.8 $Å^3$, which is slightly smaller than bulk SZO u.c. volume that was reported by Wong et al. (69.1 $Å^3$). This slight difference is consistent with a small degree strain intact to the substrate, resulting in a 0.6% in-plane contraction and a 0.5% out-of-plane expansion of the lattice. [40]

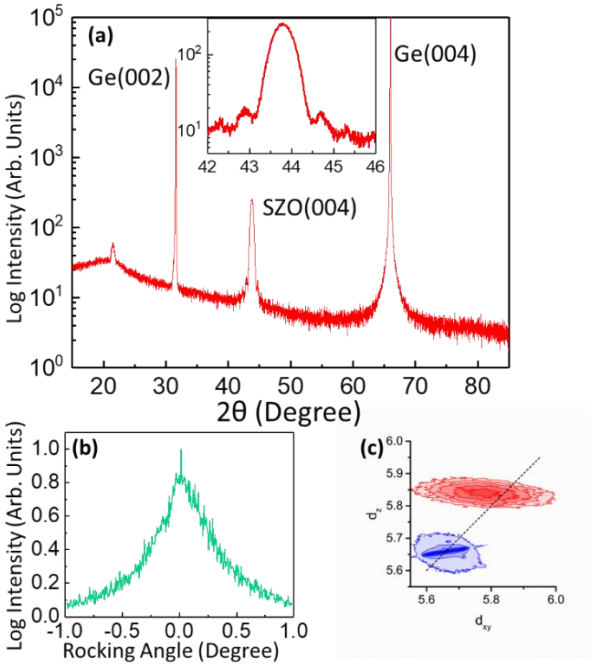


Figure 5-3: XRD survey scan of SZO-Ge heterojunction, where inset show the zoom in of SZO (002) peak. (b) Rocking curve of the SZO (002) peak shows a FWHM of ~0.63°. (c) Direct space map of the heterojunction. The SZO lattice constants were multiplied by $\sqrt{2}$ in order to compare with Ge lattice constants directly. Dashed line indicates where $d_{xy} = d_z$.

The band alignment of the SZO-Ge heterostructures can be calculated from the obtained XPS spectra. Figure [5-4] shows a schematic drawing of the band alignment with respect to the core level. From the figure, the valence band offset can be written as:

$$VB_{offset} = \left(E_{Ge3d5/2} - E_V\right)_{Ge} + \left(E_{Sr3p3/2} - E_{Ge3d5/2}\right)_{HJ} - \left(E_{Sr3p3/2} - E_V\right)_{SZO}$$

$\left(E_{Ge3d5/2} - E_V\right)_{Ge}$ is the difference between Ge core level binding energy and its valence band edge (VBE) of the Ge reference sample. $\left(E_{Sr3p3/2} - E_V\right)_{SZO}$ is the difference between SZO core level binding energy and its VBE of the SZO reference sample. $\left(E_{Sr3p3/2} - E_{Ge3d5/2}\right)_{HJ}$ is the difference between core level binding energy of Ge substrate and SZO thin film. Three samples

were measured with XPS, namely the clean Ge substrate, thick SZO film, and thin SZO film. Clean Ge substrate was used as a reference to obtain the Ge core level binding energy and its VBE, thick SZO film was used as a reference to obtain the SZO core level binding energy and its VBE, and thin SZO film was used to determine the difference between Ge and SZO core level binding energy.

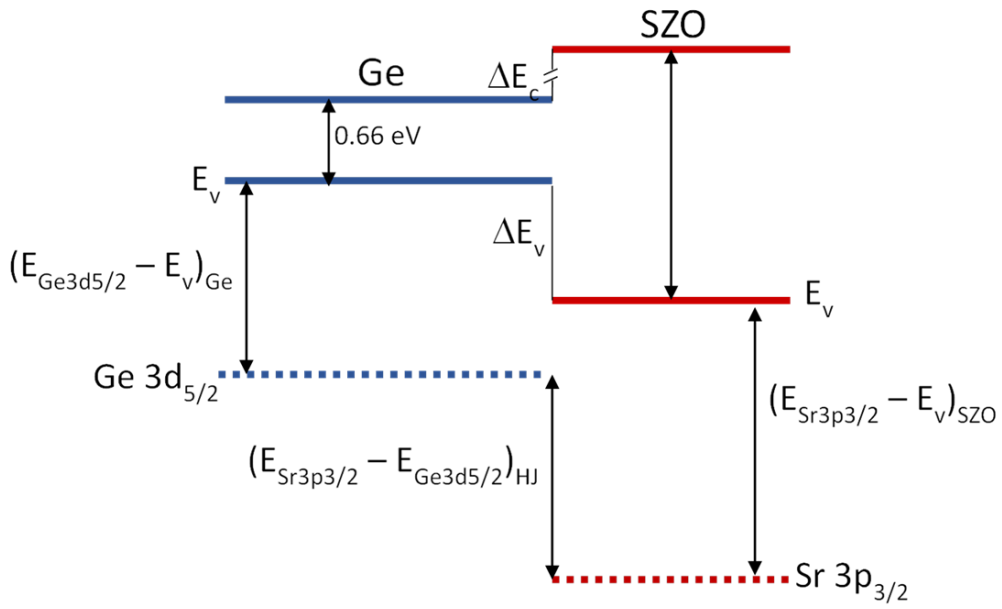


Figure 5-4: Schematic of the valence and core level band diagram of SZO-Ge heterostructure used to determine the valence and conduction band offsets between SZO thin film and Ge substrate.

Both the 15 nm and 4 nm SZO samples were used for XPS measurement in order to determine band alignment of SZO-Ge heterostructure. The valence band (VB) offset with respect to Ge was calculated from the spectra of both samples. [42] [37] Figure [5-5] shows the full XPS results and analysis. According to the calculation from Dr. Scott Chambers, by assuming a band gap of 5.6 eV for bulk SZO, [43] the Fermi level will be about 1.4 eV below the conduction band edge. Using the Sr $3d_{5/2}$ and Zr $3d_{5/2}$ core level binding energy, the differences between the core

binding energies and the valence band edge were calculated to be 130.25 eV and 178.53 eV respectively. From the analysis of 4 nm SZO film, we also concluded that the valence band offset between the SZO and Ge is about 3.66(7) eV, where the band gap of Ge is 0.66 eV. By using the band gap of bulk SZO mentioned above, a type-I band offset was confirmed for SZO film grown on Ge as seen in figure [5-6]. The difference between type-I and type-II band offset is shown in figure [5-7] as well. For type-I band offset, the conduction band of the film is higher than the conduction band of semiconductor, while the valence band of film is lower than the valence band of semiconductor.

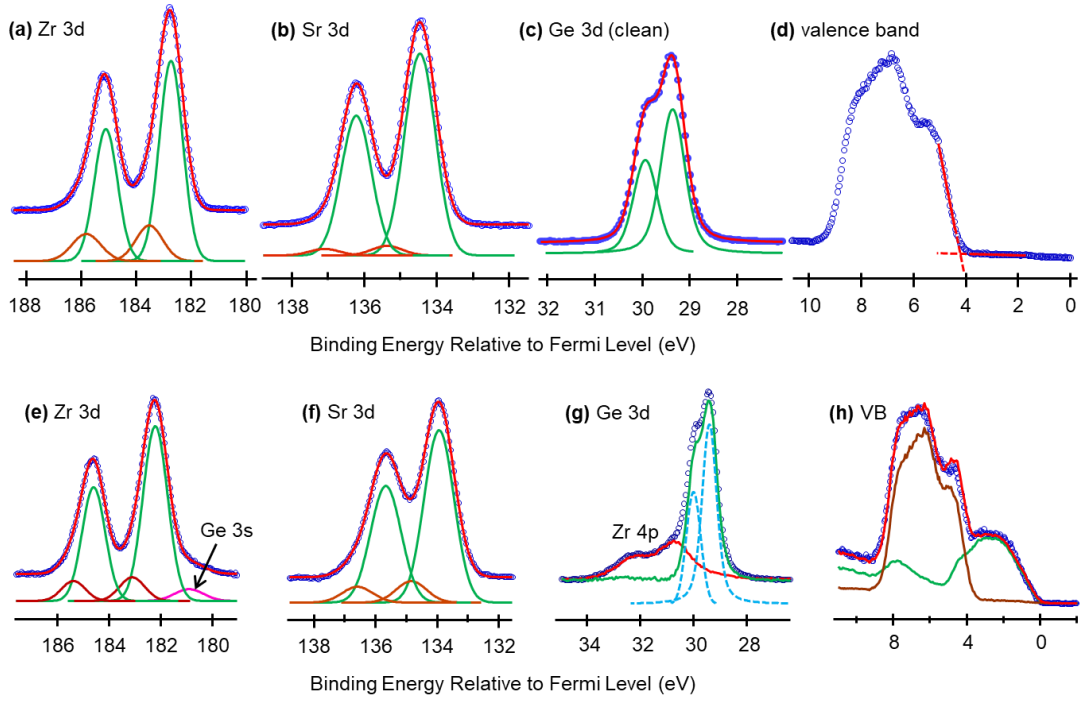


Figure 5-5: Full XPS result and analysis of SZO-Ge heterojunction. The lattice spin-orbit peaks are shown in green, while the brown shows the surface hydroxyl species. The red is the sum of all individual peaks. (a) and (b) are the core level spectra of Zr and Sr respectively obtained from 15 nm SZO film. (c) Ge core level spectrum obtained from clean Ge substrate. (d) Valence band edge of the thick SZO film was measured to be around 4 eV. (e), (f) and (g) are the core level spectra of Zr, Sr and Ge respectively measured from 4 nm SZO thin film. (h) Valence band edge of the 4 nm SZO thin film.

In contrast, the conduction band and valence band of oxide are lower than those of semiconductor for a type-II band offset. Having a type-I band offset for SZO-Ge heterostructure is required for SZO film to act as a gate dielectric on Ge for PMOS. Figure [5-8] shows the HAADF STEM image of our SZO-Ge interface, which confirmed the existence of a thin non-uniform GeO_x layer in between SZO thin film and Ge substrate from annealing. The SZO thin film is mosaic due to the Ge substrate steps and misfit at the interface. [44] Formation of Zintl phase was found at the interface and is shown in figure [5-8] pointed by white arrows. [45]

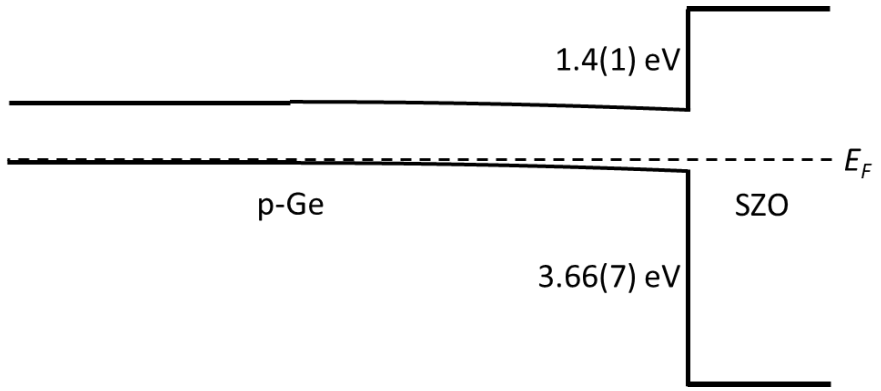


Figure 5-6: Band diagram showing the type-I band alignment between SZO and Ge substrate. The conduction band offset is 1.4 eV, and the valence band offset is 3.66 eV. Slight band bending was confirmed at the oxide-semiconductor interface.

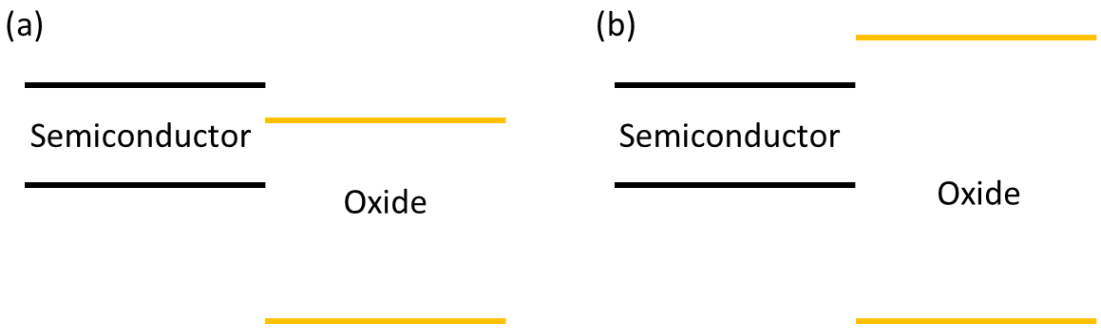


Figure 5-7: Schematic band alignment drawing of (a) type-II and (b) type-I band offset. The conduction and valence bands of oxide are lower than the conduction and valence bands of semiconductor for type-II band offset. Whereas for type-I band offset, the conduction band of oxide is higher than the conduction band of semiconductor, and the valence band of oxide is lower than the valence band of semiconductor.

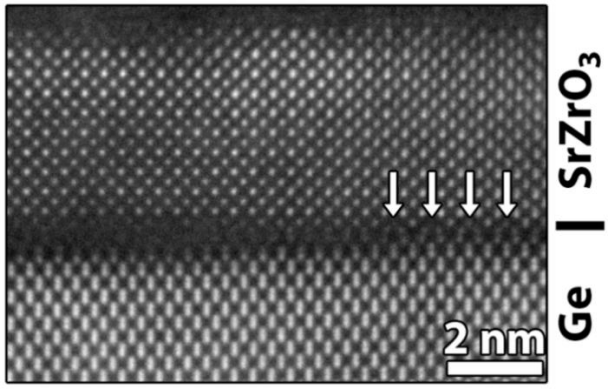


Figure 5-8: HAADF STEM image of the SZO-Ge interface. A non-uniform layer GeO_x layer can be seen on the left side after post-annealed. Zintl reconstruction indicated by white arrows.

The C-V and I-V measurements of the annealed 4nm film on n-type Ge wafer are shown in figure [5-9]. The inset of the figure shows that the leakage current densities are about 3×10^{-3} A cm^{-2} and 6×10^{-3} A cm^{-2} at -1V and +1V, respectively. The capacitance of the sample was also measured with respect to all frequencies within bias of +2 V and -1.5 V. The y-axis for both the C-V and I-V plots are normalized to area, i.e. they were plotted in capacitance or current divided by the area of the contact pad. From the C-V measurement result, accumulation case occurs at positive bias and either depletion or inversion case occurs at negative bias since the SZO film was grown on n-type Ge substrate. For 1 MHz down to 5 kHz data, all measurements started accumulation at positive bias and turned into depletion at negative bias, even though there was a small hump within bias from -0.5 V to -1 V. This anomaly peak-like structure is called weak inversion response, which is caused by thermally generated minority carriers in the film. [46] As for the 500 Hz data, an upturn was seen at the negative bias, which showed that SZO-Ge heterostructure could achieved a complete inversion at 500 Hz frequency. The figure [5-9] inset also shows the leakage current density of the SZO thin film. The leakage current density of SZO thin film is comparable to some of the popular gate dielectrics that are widely used, such as

Al_2O_3, ZrO_2, $LaAlO_3$, HfO_2, TiO_2, and $SrHfO_3$. [47] [48] [49] [50] [51] [52] [53] All C-V measurements were taken across different nickel contact pad sizes ranging from 5.725×10^{-4} cm^2 to 5.31×10^{-6} cm^2 as shown in table [5.1]. Figure [5-10] shows the measurements taken from across the sample with different electrode pad sizes at 1 MHz, where the results are generally consistent.

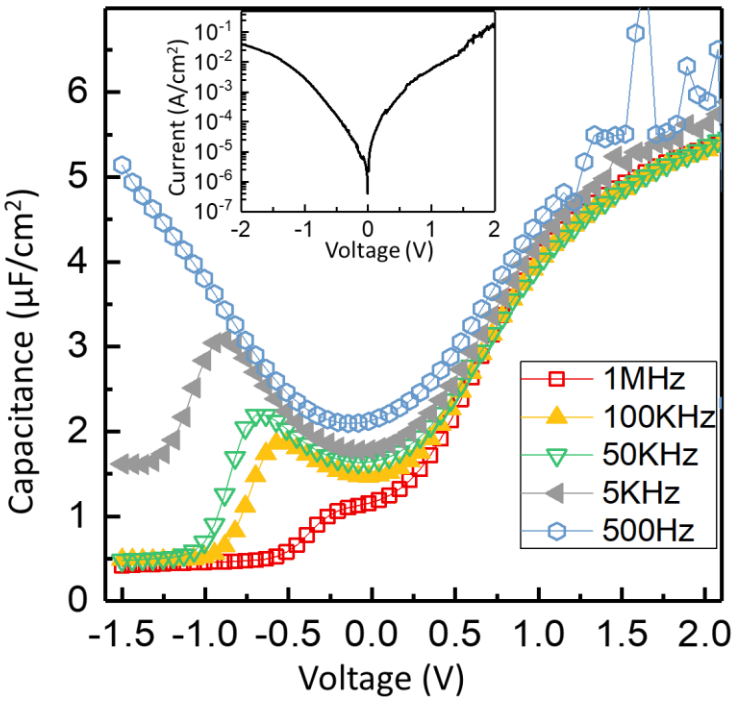


Figure 5-9: C-V measurement of SZO-Ge heterojunctions, where the bias voltage is applied to a nickel electrode on top of SZO. The inset showed the corresponding leakage current of that junction. Weak inversions appeared for all frequencies besides 500 Hz data.

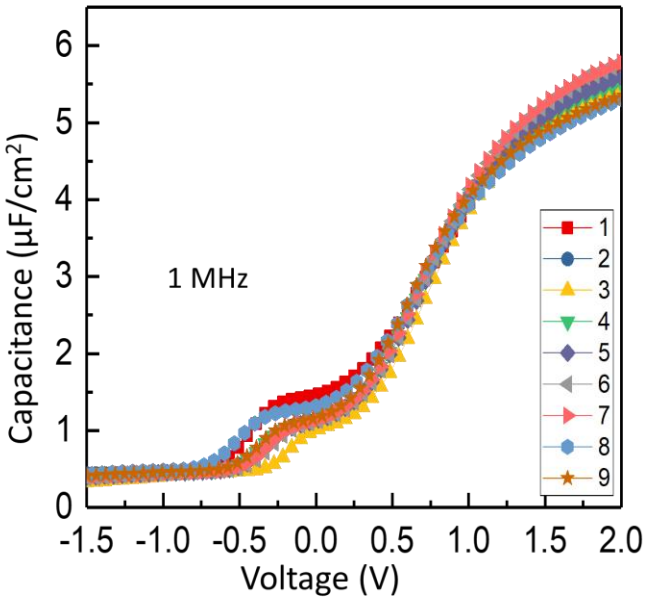


Figure 5-10: C-V measurement of 9 different junctions across a 5 × 5 mm post annealed sample. Results are generally consistent across the sample.

Figure [5-1l] shows more I-V measurements that were taken across a 5 × 5 mm postgrowth annealed 4 nm SZO sample in order to determine the effect of junction size. There are some variations in leakage current density with respect to junction size, but there is no clear trend to be observed. The leakage currents did not scale with junction size, which would suggest that the leakage currents are independent of grain boundaries. No hysteresis was found in our I-V measurement as we sweep the voltage bias, as seen in figure [5-12].

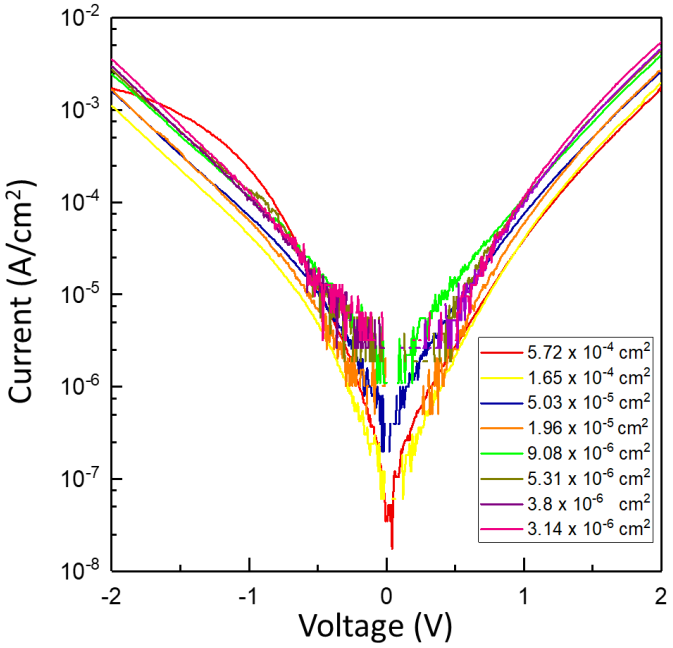


Figure 5-11: I-V measurements were taken from 8 different junctions located across a 5 × 5 mm post-annealed sample. These 8 junctions are varied in area size. Small variations can be found, but no clear trend was observed.

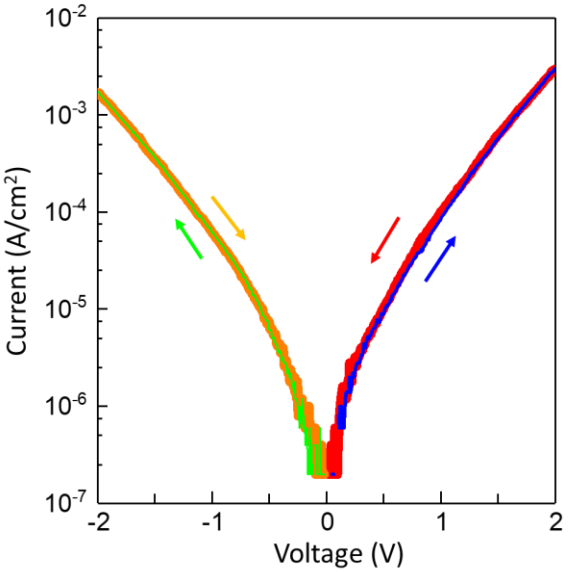


Figure 5-12: I-V measurement was taken with sweeping voltage bias, where the arrows indicate the sweeping direction. Minimal hysteresis was found.

Pad name	Pad size (cm^2)
A	5.725×10^{-4}
B	1.65×10^{-4}
C	5.03×10^{-5}
D	1.96×10^{-5}
E	9.08×10^{-6}
F	5.31×10^{-6}
G	3.8×10^{-6}
H	3.14×10^{-6}

Table [5.1]: Different pad names and their sizes on the shadow mask.

Dielectric constant and equivalent oxide thickness (EOT) of SZO thin film were calculated with C-V data. Equation [5.1] was used to calculate the dielectric constant, where *C* is the capacitance at accumulation case, *A* is the area of the contact pad, *d* is the thickness of the thin film, and ε_o is the dielectric of vacuum.

$$\kappa = \left(\frac{C}{A}\right)\frac{d}{\varepsilon_o} \quad [5.1]$$

$$EOT = d\left(\frac{\kappa_{SiO2}}{\kappa_{ox}}\right) \quad [5.2]$$

Equation [5.2] was used to calculate the EOT, where d is the thickness of the thin film, κ_{SiO2} is the dielectric constant of silicon dioxide, and κ_{ox} is the dielectric constant of SZO thin film. The calculated dielectric constant of SZO thin film is around 23, which is comparable to SiO_2 (3.9), HfO_2 (~ 20), and Zr doped STO film (29). [37] [54] EOT is an effective way to determine the efficiency of an unknown thin film as a gate dielectric with respect to SiO_2. It is known that SiO_2

has a better capacitive effect as the thickness decreases. But as the film thickness drops below 1 nm, the leakage current will be too high to function as a gate dielectric. So, other high-κ thin film could be use as gate dielectric. The 4 nm SZO thin film has a calculated EOT of about 0.7 nm, which means the 4 nm SZO thin film has the same capacitive effect of a 0.7 nm thick SiO_2 thin film.

Interface-trap states density was determined using the High-Low method, which is shown in equation [5.3]. [25] We believe these trap states are coming from the dangling bonds at the interface due to the relaxation of the film even at only 4 nm thin. The density of interface trap states was calculated using equation [5.3], where q is the electron charge in Coulomb, C_{LF} is the flat-band capacitance measured at low frequencies, C_{HF} is the flat-band capacitance measured at high frequencies, and C_{OX} is the maximum capacitance at accumulation states. The density of interface trap states of 4 nm SZO thin film is in the 10^{13} range. However, due to the small bandgap of Ge, it is very hard for us to make an accurate measurement of the density of interface trap states at room temperature. [55] At room temperature, the time constant for capture and emission processes of carriers through interface traps are much shorter for Ge due to its smaller bandgap, which causes the weak inversion to have contribution to the measured density of interface trap states at room temperature. We believe these interface trap states are due to the dangling bonds at the interface, the formation of GeO_x at the interface due to post annealing, and the growth using an e-beam evaporator.

$$D_{it} = \frac{1}{q}\left[\left(\frac{1}{C_{LF}} - \frac{1}{C_{OX}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{OX}}\right)^{-1}\right] \quad [5.3]$$

Schottky pinning parameter, S, is generally used to describe the pinning of metal on wide bandgap oxide. In the Bardeen limit, the metal is said to be pinned to the oxide, the metal Fermi

level will be fix regardless of the metal work function. The general equation of Schottky barrier height is shown in equation [5.4], where ϕ_n is the Schottky barrier height, Φ_m is the metal work function, Φ_s is the energy of the interface states in semiconductor, and χ_s is the electron affinity of the semiconductor. Therefore, in the Schottky limit, S = 1, the electron barrier height is related to work function of the metal. In contrast, when S = 0, it is the Bardeen limit, where the electron barrier height is pin to the energy of the semiconductor interface states with respect to the vacuum level. Schottky pinning parameter can be calculated using equation [5.5], [56] [57] where ε_∞ is the optical dielectric constant. A schematic diagram of the band alignment is shown in figure [5-13].

$$\phi_n = S(\Phi_m - \Phi_s) + \Phi_s - \chi_s \quad [5.4]$$

$$S = \frac{1}{1 + 0.1(\varepsilon_\infty - 1)^2} \quad [5.5]$$

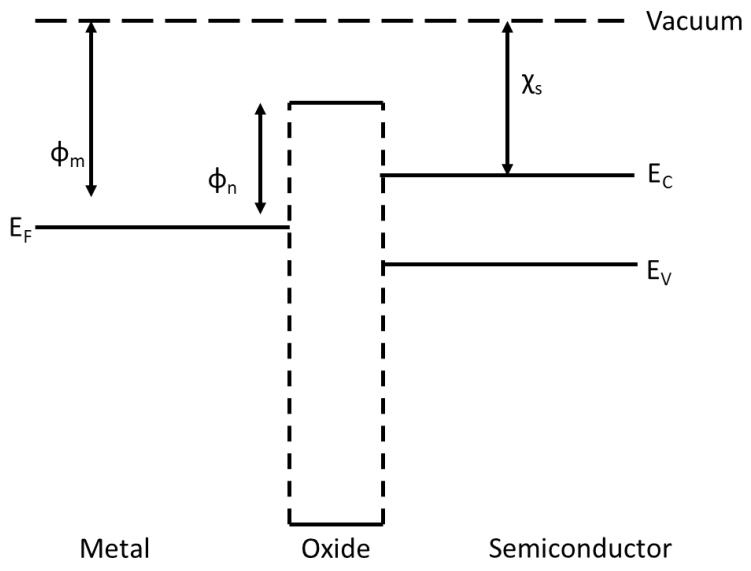


Figure 5-13: Schematic band diagram across MOS heterojunction.

Most of the *S* parameter of popular high-κ dielectric materials have been reported previously. It is reported that pinning parameter of SiO_2 is 0.86, which is close to the Schottky limit. Since SiO_2 is close to the Schottky limit, different metal work function will affect the electron barrier height ϕ_n, which in term will shift the flat band voltage. *S* value for STO was reported to be 0.28, which is close to the Bardeen limit. [58] It is also known that the barrier height of STO will not shift with different metal. [59] A flat band shift was seen for C-V measurements of SZO thin film with different metal electrodes, as seen in figure [5-14]. The flat band voltage shift between Ni and Cr electrodes can be written as $\Delta_{fb} = \phi_{Ni} - \phi_{Cr}$, where ϕ_{Ni} and ϕ_{Cr} are shown below. Since both Ni and Cr electrodes are deposited on the same film that was grown on the same substrate, so ϕ_s and χ_s are the same for both metals. Therefore, Δ_{fb} can be arranged into equation [5.6].

$$\phi_{Ni} = S(\Phi_{Ni} - \Phi_s) + \Phi_s - \chi_s \ ; \ \phi_{Cr} = S(\Phi_{Cr} - \Phi_s) + \Phi_s - \chi_s$$

$$\Delta_{fb} = \phi_{Ni} - \phi_{Cr} = S(\Phi_{Ni} - \Phi_{Cr}) \quad [5.6]$$

Figure [5-14] (a) shows the original C-V data taken with Ni and Cr electrodes, while figure [5-14] (b) shows the C-V data with Cr data normalized to Ni data. The difference in flat band voltage between Ni and Cr electrodes is measured to be 0.667 eV, while the difference in Ni and Cr work function, $\Phi_{Ni} - \Phi_{Cr}$, is 0.7 eV. From equation [5.6], the calculated *S* parameter value of SZO is around 0.95, which is higher than the *S* value of SiO_2. So, it is suggested that SZO is a gate dielectric that is toward the Schottky limit unlike STO. In theory, SZO has an optical dielectric constant of 4.7, and the calculated *S* value from equation [5.5] is 0.422, which is closer to the experimentally measured *S* value of ZrO_2, 0.52. [60] [61] It was also reported that different metal on ZrO_2 will shift its flat band voltage. [62] So, we hypothesize that SZO can have its flat

band voltage shifts due to different metal work function since its *S* parameter is very close to the Schottky limit. A more thorough investigation is needed in order to determine why the *S* value of SZO calculated from the experimental C-V data is more than two times larger than the one calculated from optical dielectric constant.

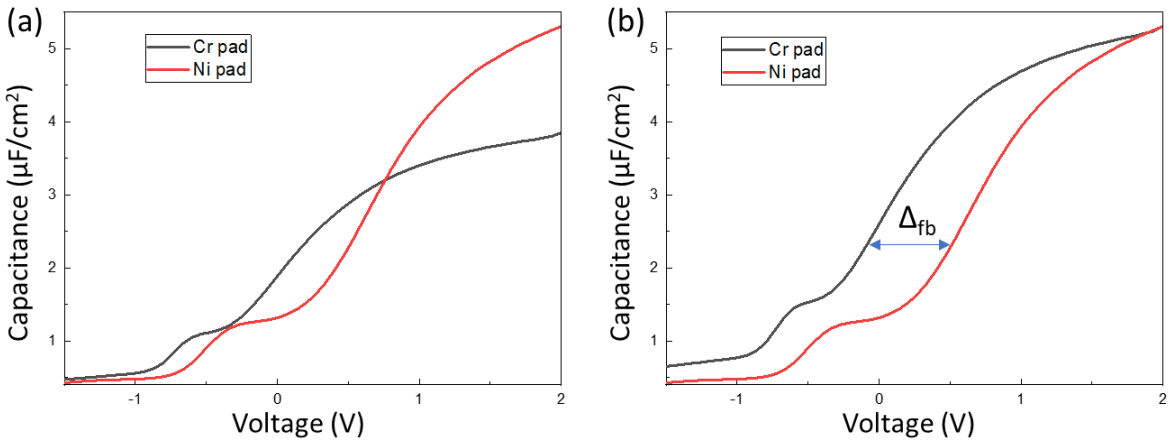


Figure 5-14: C-V measurement of SZO-Ge heterojunctions with nickel and chromium electrode. (a) Original C-V data taken with Ni and Cr electrodes. (b) C-V data where the Cr data was normalized to the Ni data.

5-4: Conclusion

In summary, epitaxial SZO thin films were successfully grown on n-type and p-type Ge substrate with oxide MBE, and the epitaxial SZO thin films were characterized both electrically and structurally. We also showed that SZO thin film exhibits some properties which is important for a PMOS devices, including large conduction and valence band offsets, and low leakage current. From our results, we can conclude that SZO could be a potential good dielectric gate material candidate for Ge-based MOS devices, because of its comparable dielectric constant and EOT with some other popular gate dielectric material such as HfO_2.

Chapter 6 : Charge Transfer and Built-in Electric Fields Between a Crystalline Oxide and Silicon

6-1: Introduction

p-n Junction, which consists of 2 types of semiconductor materials (p-type and n-type), make use of the charge transfer across the heterojunction and the built-in electric field to underpin the functionality of almost all semiconductor devices, such as transistors, diodes, solar cells, etc. [21] Other than p-n junction, there are other junction types that also make use of the charge transfer effect, for example n-n isotype and doped-intrinsic junctions, where the doped-intrinsic junction has led to the fundamental discovery of the fractional quantum Hall effect. [63]

Due to the advancements in epitaxial growth using MBE, we could now grow single crystalline complex oxides on semiconductors, which enable us to study the charge transfer phenomena across crystalline oxide and semiconductor heterojunctions. [3] The resulting atomically abrupt oxide-semiconductor interface enable continuity in the electric displacement, which is very important for charge transfer and built-in electric field. [64] [65] [66] [67] Complex oxides have some very interesting properties that conventional semiconductor does not have, such as propensity for degenerate doping, short electronic length scale, sizable band offsets, large temperature dependent dielectric constant, etc. Moreover, the assumptions of rigid band alignments and other semiclassical approximation are not applicable for oxide-semiconductor heterojunctions. This motivates the coupling between complex oxides and semiconductors, as it can gives rise to some novel electrical behaviors that semiconductor by itself cannot achieves. This type of hybrid heterojunction has potential in some applications such

as photochemical processes to nanophononics. [35] [33] [31] The objective of this project is to focus on the possible techniques to measure and study the built-in fields and band alignment.

In this project, we demonstrated charge transfer and built-in fields in a heterojunction comprised of Si and the solid solution $SrNb_xTi_{1-x}O_{3-\sigma}$ (SNTO). [68] $SrTiO_3$ (STO) by itself is a wide bandgap semiconductor, while $SrNbO_3$ (SNO) is a metal. So, by doping Nb into STO, we could control the effect of charge transfer and built-in fields by tuning the carrier densities. In this project, we demonstrated that built-in fields across the oxide-semiconductor interface can be induced to form a hole gas in the Si near room temperature. Hard x-ray photoelectron spectroscopy (HAXPES) was utilized to reveal pronounced asymmetric features in core-level spectra for both SNTO and Si. We showed that the analysis of the asymmetries enables built-in fields and band alignment to be spatially mapped out across the interface. The accomplishment on tunable charge transfer, built-in electric fields and its mapping using HAXPES lays down the groundwork for the development of functional oxide-semiconductor heterojunctions that are coupled through charge transfer. [69]

6-2: Experiment

Single crystal 12 nm and 20 nm $SrNb_xTi_{1-x}O_3/SrTiO_3$ was grown on undoped Si wafer for different Nb content including $x = 0$, $x = 0.08$, $x = 0.2$, and $x = 0.6$ with our home-built UHV MBE system. Si wafer was first cleaned with 225W oxygen plasma, and 2.5 unit-cells (u.c.) of STO was grown at room temperature and crystalized at 580 ^oC as a platform for the remaining film. Then, 5 u.c. of SNTO film was deposited 300 ^oC and was heated up to 580 ^oC to prevent any SiO_2 formation at the oxide-silicon interface. After that, the remaining 25 u.c. SNTO film was deposited at 580 ^oC. The background oxygen pressure during the growth process was control to 4×10^{-7} Torr. RHEED was also utilized during the growth to confirm the crystallinity of the

grown film. The wafer was then diced into a 4 × 4 mm square pieces for transport measurements.

Diced samples were taped to physical properties measurement system (PPMS) puck with Kapton tape for transport measurements. Kapton tape was chosen here due to its insulating properties and the ability to survive under high and extreme low temperature. An ultrasonic wedge wire bonder was utilized to connect the PPMS puck's electrode to the four corners of the sample with aluminum wire. Ohmic behavior was confirmed for aluminum wire that was wire bonded on oxide thin film by taking current vs. voltage (I-V) measurement. Another reason to check the I-V measurement was to determine the amount of current that we can apply for transport measurements. In order to obtain a strong signal and clean data, more than 35 μA of current was generally needed. But, if the applied current was too large, the wire or the sample might break down at very low temperature (< 10 K). A general rule of thumb to determine the amount of needed current is to first figure out the sheet resistance at room temperature, and then apply the amount of current that will produce a voltage signal of around 10-30 mV.

The transport measurements were done using the PPMS developed by Quantum Design Inc. Sheet resistance vs. temperature measurements were taken from 400 K to 4 K, while the Hall measurements were taken from 200 K to 400 K with temperature steps ranging from 3 K to 25 K. The measurement setup was the same mentioned in chapter 4, which consists a Keithley 2700 multiplexer, a Keithley 2400 source meter, the PPMS, and a LabView program that was originally written by two of the undergraduate students. The procedure of data collection was to heat up the sample to 400 K, then sheet resistance measurements were performed from 400 K down to 4 K. After that, the sample was warmed up to needed temperature and Hall measurements were performed with magnetic field from -9 T to 9 T.

The sheet resistance vs. temperature data from the LabView program can be used directly but the Hall measurements data needs to be normalized properly. The Hall resistance data was analyzed and fitted with the 2-carrier model using OriginLab software. The Hall signal data that was obtained from the LabView program are the Hall voltages V_{13}, V_{24}, V_{31}, and V_{42}, where the numbers are the assigned numbering system for van der Pauw technique as shown in chapter 4. Next, V_C, V_D, V_E, V_F was calculated using equations below, where the "P" and "N" indicate the voltage for positive field and negative field respectively:

$$V_c = V_{24P} - V_{24N}\,, V_D = V_{42P} - V_{42N}\,, V_E = V_{13P} - V_{13N}\,, V_F = V_{31P} - V_{31N}$$

From V_C, V_D, V_E, V_F, we can also calculate Hall resistance, carrier density and carrier mobility using equation [6.1], [6.2], and [6.3]. Note that the *B* here is the magnetic field in gauss, R_s is the sheet resistance at zero magnetic field, and *I* is the current in Ampere. The sign of n_s in equation [6.2] will indicate the dominate carrier type in conductivity. Both equation [6.2] and [6.3] are only applicable if one carrier is present. [27]

$$R_H = \frac{(V_C + V_D + V_E + V_F)}{8I} \quad [6.1]$$

$$n_s = \frac{8 \times 10^{-8} IB}{q(V_C + V_D + V_E + V_F)} \quad [6.2]$$

$$\mu = \frac{1}{q n_s R_s} \quad [6.3]$$

After transport measurement, the sample was also sent to our collaborators for scanning transmission electron microscope (STEM) imaging to confirm the abrupt interface and sent to United Kingdom for HAXPES measurements. The HAXPES measurements were done at the Diamond Light Source in the U.K. on the I09 Surface and Interface Structural Analysis beamline

at an X-ray energy of 5930 eV using a Si (111) double crystal monochromator followed by a Si (004) channel-cut high-resolution monochromator. The binding energy scale was calibrated with Au 4f core level, along with the Fermi edge of a gold foil. Angle-resolved measurement was also done with an X-ray incident angle at 30^{o}. A bulk $SrNb_{0.01}Ti_{0.99}O_3$ standard was mounted with the epitaxial sample for the HAXPES measurement using W wire, which made electrical contact between the front surface of the samples and the grounded sample holder as shown in figure [6-1]. Judging by the peak position of the bulk SNTO crystal, Si crystal, the SNTO/Si heterojunction, and the consistency of measured binding energy, we concluded that there was no charging effect during the measurement. Time-of-flight secondary ion mass spectroscopy (ToF-SIMS) measurements and XPS measurements were also performed at the Pacific Northwest National Lab (PNNL). A TOF.SIMS5 instrument was used for the SIMS measurements. Dual beam depth profiling strategy was utilized for the experiment, where a 1 keV Cs^+ beam (~45 nA) was used for sputtering, while another 25 keV Bi^{3+} beam (~0.57pA) was used as the analysis beam to collect SIMS depth profiling data. The Bi^{3+} beam was focused and only scan the center area of the Cs^+ crater. The XPS measurements were performed using a Scienta Omicron R3000 analyzer and a monochromatic AlKα X-ray source, which has an energy resolution of around 0.4 eV. Ag $3d_{5/2}$ core-level and a polycrystalline Ag foil were used to the system binding energy scale and the Fermi level respectively.

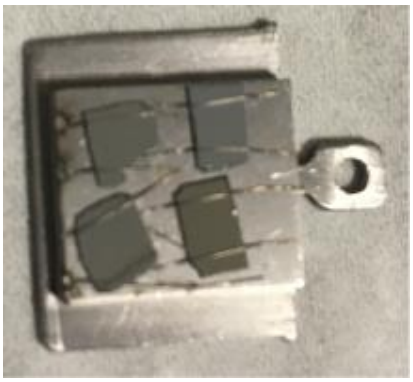


Figure 6-1: Sample set up for HAXPES measurement.

6-3: Results

The structural properties of the SNTO-Si heterojunction are shown in figure [6-2] and [6-4]. Figure [6-2] shows the dark field STEM image across the SNTO-Si interface, where the interface is atomically abrupt. The films are also relaxed with respect to Si from the direct space map image of the heterojunctions as seen in figure [6-3]. In figure [6-3], the red color indicates the SNTO film, while the blue is the Si. All SNTO lattice constants were multiplied by $\sqrt{2}$ in order to compare with Si lattice constant directly. All SNTO lattice constants in the x-y direction are larger than the Si lattice constant indicate the SNTO film is relaxed from the Si substrate.

The results of the sheet resistance and Hall measurements of the SNTO-Si heterojunctions with different Nb concentration are shown in figure [6-4]. As seen in figure [6-4] (a), the sheet resistance for $x = 0$ sample shows semiconducting behavior at low temperature. But, as the Nb concentration increase to $x = 0.6$, the sample also behaved like a metal at low temperature, which is what we expected to see as the electron carrier density increased. Around room temperature, there were anomalies (pointed out by arrows) in sheet resistances for $x = 0$, 0.08, and 0.2 samples. The sheet resistances decreased significantly close to room temperature,

and then increased again as the temperature increased. In order to study these anomalies, Hall measurements were performed for all samples around room temperature. Figure [6-4] (b) – (d) show the Hall resistance data for x = 0, 0.08, 0.2, where the sign of the Hall signal switch from negative to positive as the temperature increase across the anomaly. The crossover in sign of Hall signal indicates that the dominate carrier of the sample's conductivity ($\propto$ carrier density $\times$ carrier mobility) switches from electron into hole, even though the majority carrier in the heterojunctions is still electron. Non-linearities of the Hall signals also indicate that there was mixed conduction in the heterojunctions. As for the x = 0.6 heterojunction, no downturn in the sheet resistance, and no crossover in sign of its Hall signal is observed (figure [6-4] (e)).

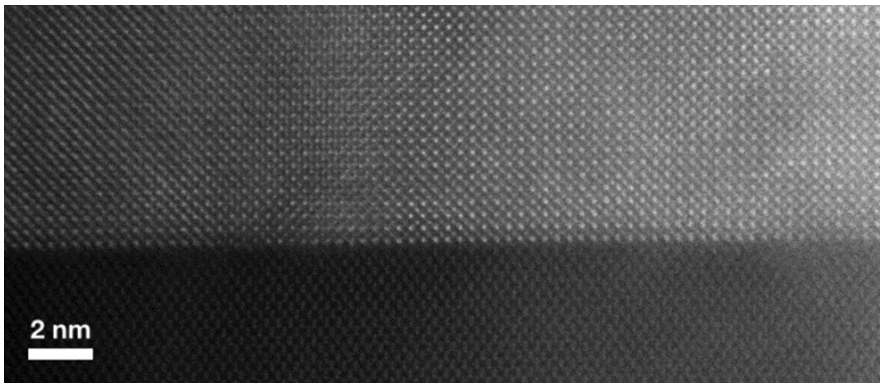


Figure 6-2: HAADF STEM image across the SNTO-Si interface. Interface is atomically abrupt.

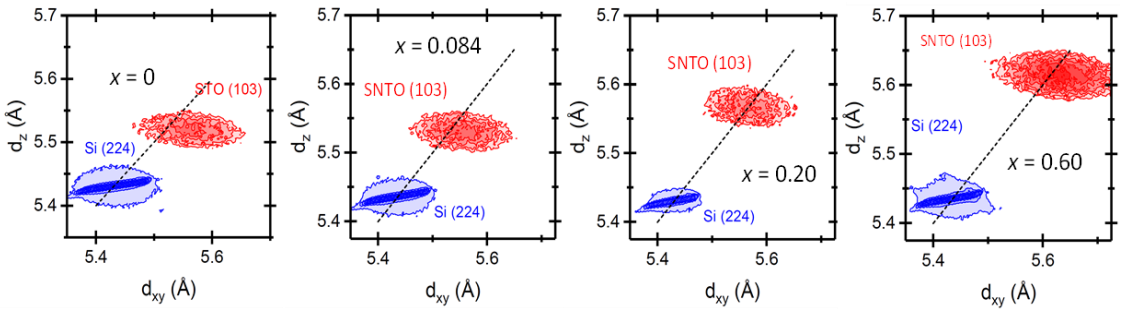


Figure 6-3: Direct space map image of SNTO-Si heterojunction with different Nb concentration. All oxide films are relaxed with respect to Si substrate.

Due to mix conduction in our heterojunctions, the conventional Hall model will not be able to fit the data. Instead, a 2-carrier model, as seen in equation [6.4], was used to analyze the Hall signals. [70] [71] This 2-carrier model was derived from the tensor of the conductivity equations as seen in equation [6.5] and [6.6], where n_i and μ_i are the sheet carrier density and mobility of the i_{th} channel, B is the magnetic field in gauss, and q is the charge of electron (1.6×10^{-19} C). Both 2-carrier and 3-carrier model were derived utilizing the conductivity tensors.

$$R_{xy} = \frac{B}{q}\frac{(\mu_1{}^2 n_1 + \mu_2{}^2 n_2) + (\mu_1\mu_2 B)^2(n_1 + n_2)}{(\mu_1 n_1 + \mu_2 n_2)^2 + (\mu_1\mu_2 B)^2(n_1 + n_2)^2} \quad [6.4]$$

$$\sigma_{xx}(B) = \sum_i^N \frac{q n_i \mu_i}{1 + \mu_i{}^2 B^2} \quad [6.5]$$

$$\sigma_{xy}(B) = \sum_i^N \frac{q n_i \mu_i{}^2 B}{1 + \mu_i{}^2 B^2} \quad [6.6]$$

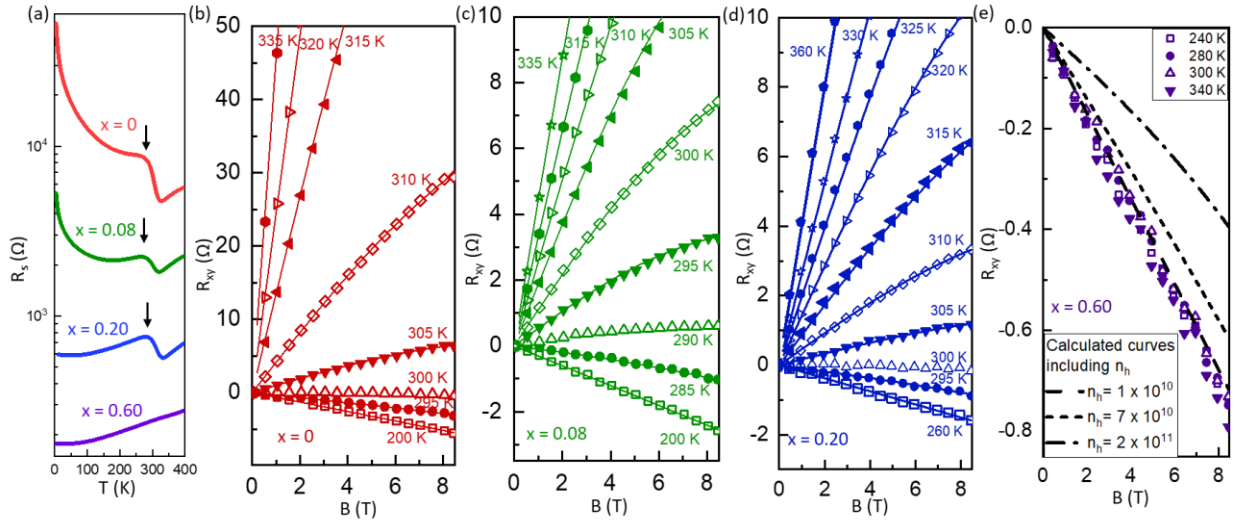


Figure 6-4: (a) Sheet resistance for different Nb concentration heterojunctions, where arrows point out the anomalies. (b), (c), (d), and (e) show the Hall resistance data for Nb concentration x = 0, 0.08, 0.2, 0.6 respectively. Crossover in Hall signals' sign were observed for x = 0, 0.08, and 0.6 samples.

In order to derive the 2-carrier model, N was first set to 2 for the conductivity tensors, and both conductivity tensors were substituted into R_{xy}. The expression as shown below was obtained from inverting the conductivity tensors:

$$R = \begin{pmatrix} R_{xx} & R_{xy} \\ R_{yx} & R_{yy} \end{pmatrix} = \begin{pmatrix} \sigma_{xx} & \sigma_{xy} \\ \sigma_{yx} & \sigma_{yy} \end{pmatrix}^{-1} = \frac{1}{{\sigma_{xx}}^2 + {\sigma_{xy}}^2} \begin{pmatrix} \sigma_{yy} & -\sigma_{xy} \\ -\sigma_{yx} & \sigma_{xx} \end{pmatrix}$$

In equation [6.4], the parameters were set to $n_1 = -n_e$, $n_2 = n_h$ and $\mu_1 = -\mu_e$, $\mu_2 = \mu_h$ for the sheet carrier densities and mobilities of the n- and p- type carriers in the SNTO and Si substrate respectively, in order to analyze the Hall signals with the 2-carrier model. The reason that n_1 and μ_1 being negative is simply because electron is negatively charged, and they move in the opposite direction as compare to hole under applied electric field.

In figure [6-4] (b) – (e), the curve lines are the fitted lines with the 2-carrier model, and we can see that they fit the data well. The hole carrier densities and mobilities were extracted with the 2-carrier model, and the results are shown in figure [6-5]. Since the 2-carrier model is a 4-parameters equation, which it can be fit to a range of values that are non-unique. So, a constraint was applied to the fitted value in order to obtain accurate results. The constraint that was used is that at B = 0 T, $R_s = R_{xx}(0) = \frac{1}{e(n_1\mu_1 + n_2\mu_2)}$. From figure [6-5], the obtained hole mobilities for concentration x = 0, 0.08, and 0.2 are close to 500 $cm^2V^{-1}s^{-1}$ at room temperature, which agree to what has been reported previously for Si substrate. The measured hole carrier densities are in the 10^{13} cm^{-2} ranges. Table [6-1] also shows the electron carrier densities and mobilities, where the values are close to what we have expected with the Nb doping level. Very little variation was found in n_e for the temperature range 200 K < T < 340 K, which is consistent with the n_e behavior for a x = 0 SNTO grown on a LSAT substrate.

x	n_e ($\times 10^{15}$ cm^{-2})	μ_e (cm^{2}V^{-1}s^{-1})
0	0.967 to 0.983	0.7 to 1.13
0.08	2.07 to 2.18	1.27 to 1.49
0.2	3.33 to 3.54	2.34 to 2.87
0.6	6.45 to 7.55	2.98 to 4.34

Table [6-1]: Electron carrier densities and mobilities for x = 0, 0.08, 0.2, and 0.6 sample measured from 200 K to 340 K.

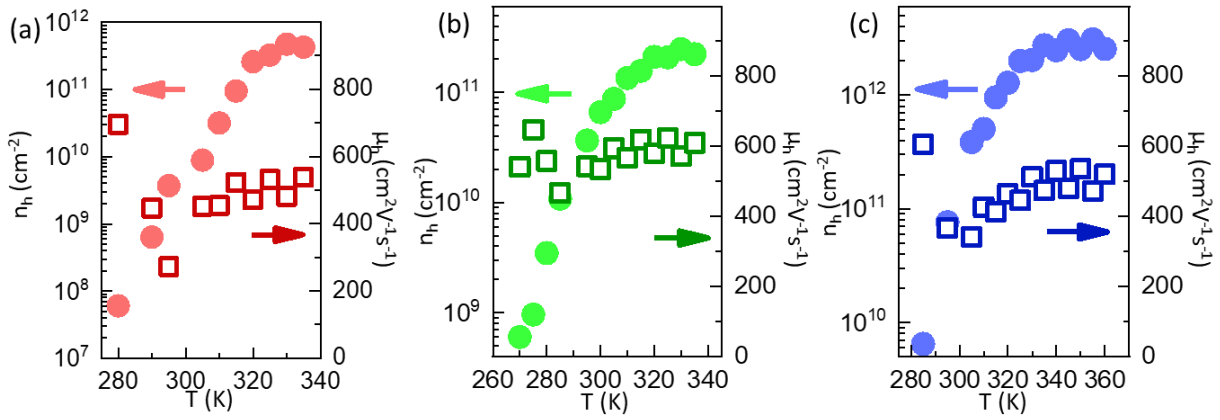


Figure 6-5: Hole carrier densities and mobilities for x = 0, 0.08, and 0.2 heterojunctions. All hole mobilities are around 500 cm^{2}V^{-1}s^{-1}, and the highest Hole carrier density is close to 3 × 10^{12} cm^{-2}.

In order to examine whether the bulk carrier has contribution to sample conductivity, a 3-carrier model (equation below) was also derived. In 3-carrier model, there are some slightly different parameter representations from the 2-carrier model, where $n_1 = -n_{e(\mathrm{SNTO})}$, $n_2 = n_{h(Si)}$, $n_3 = -n_{e(Si)}$, $\mu_1 = -\mu_{e(SNTO)}$, $\mu_2 = \mu_{h(Si)}$ and $\mu_3 = -\mu_{e(Si)}$. During the fit, fix parameter were used for $\mu_{e(Si)} \sim$ 1450 cm^{2}V^{-1}s^{-1} and $\mu_{h(Si)} \sim$ 500 cm^{2}V^{-1}s^{-1} as constraint for the fitting, and also to force two of the carriers in the bulk and the film to be electron, and the last carrier to be hole in the Si substrate.

$$R_{xy} = \frac{B}{q}\left[\frac{(n_1\mu_1{}^2 + n_2\mu_2{}^2 + n_3\mu_3{}^2) + (\mu_1\mu_2B)^2(n_1+n_2) + (\mu_1\mu_3B)^2(n_1+n_3) + (\mu_2\mu_3B)^2(n_2+n_3) + (\mu_1\mu_2\mu_3B^2)^2(n_1+n_2+n_3)}{(n_1\mu_1 + n_2\mu_2 + n_3\mu_3)^2 + (\mu_1\mu_2\mu_3B^2)^2(n_1+n_2+n_3)^2 + (\mu_1\mu_2B)^2(n_1+n_2)^2 + (\mu_1\mu_3B)^2(n_1+n_3)^2 + (\mu_2\mu_3B)^2(n_2+n_3)^2 + (\mu_1\mu_2\mu_3B^2)(2n_1n_2\mu_3 + 2n_2n_3\mu_1 + 2n_1n_3\mu_2)}\right]$$

The results of fitting the Hall signal with the 3-carrier model are shown in figure [6-6], where we concluded that the contributions from bulk carriers can be neglected. Figure [6-6] (a) and (b) show the Hall signal with various set electron densities fitted line for $x = 0$ at 260 K and 305 K respectively. At T = 260 K, for $n_{e(Si)}$ that are larger than 1×10^7 cm^{-2}, the fitted line will departs from the measured Hall data. As for T = 305 K, all $n_{e(Si)}$ that are larger than 1×10^8 cm^{-2} were not supported by out data. The obtained results set an upper bound for the bulk carrier densities, where these values were significantly smaller than the electron densities of the SNTO film and could be neglected. From these results, we have also concluded that 2-carrier model was sufficient for data analysis purpose.

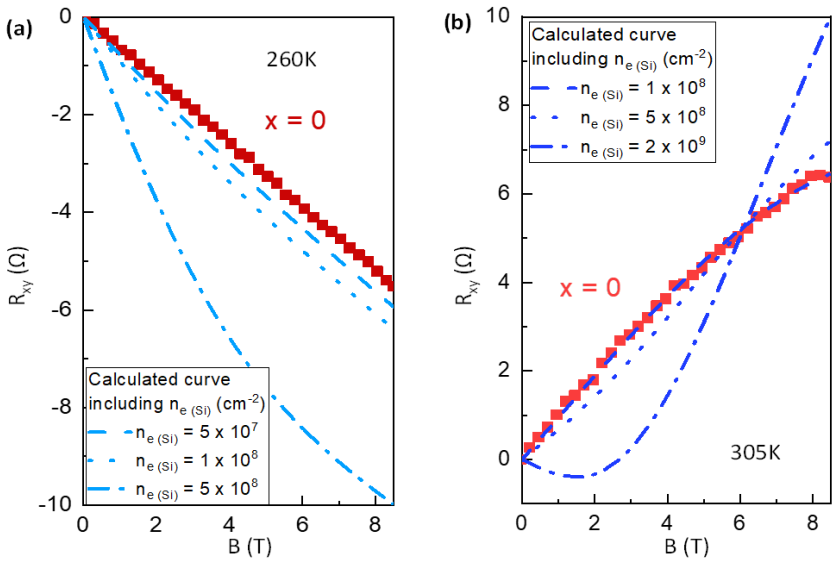


Figure 6-6: 3-carrier model fit for x = 0 heterojunction's Hall data taken at (a)260 K and (b)305 K. Plotted line is the model with contribution from the bulk. The fitted line will depart from the measured Hall signal as the bulk carrier density exceeds 1×10^7 cm^{-2} at 260 K and 1×10^8 cm^{-2} at 305 K.

In the next section, the HAXPES spectra were obtained by Dr. N. F. Quackenbush, Dr. J. M. Ablett, Dr. T.-L. Lee, and Dr. J. C. Woicik. Conventional XPS spectra and all HAXPES related analysis were done by Dr. P. V. Sushko and Dr. S. A. Chambers.

HAXPES has a high energy excitation (~ 6 keV), which enables us to obtain the electronic information across the oxide-semiconductor interface because the allowed probing depth is larger than the film thickness. [72] Figure [6-7] shows the core level spectra for $x = 0$ and 0.2 sample, along with the reference spectra for single crystal $SrNb_{0.01}Ti_{0.99}O_3$, and Si. The Ti 2p and Nb 3d spectra show in figure [6-7] (a) and (c) have multiple abnormal features, such as asymmetries of core level peak and multiple valences, pointed out by the arrows. Asymmetries of the core level peak were seen at the higher binding shoulder, and multiple Ti valences were seen at the lower binding energy shoulder. The abnormal features in Ti 2p and Nb 3d core level spectra were absent in the conventional XPS spectra (figure [6-8]). As for figure [6-7] (f), the asymmetry at the lower binding energy shoulder of Si 2p peak was reported to be Ti silicide. [73]However, STEM image doesn't show any Ti silicide.

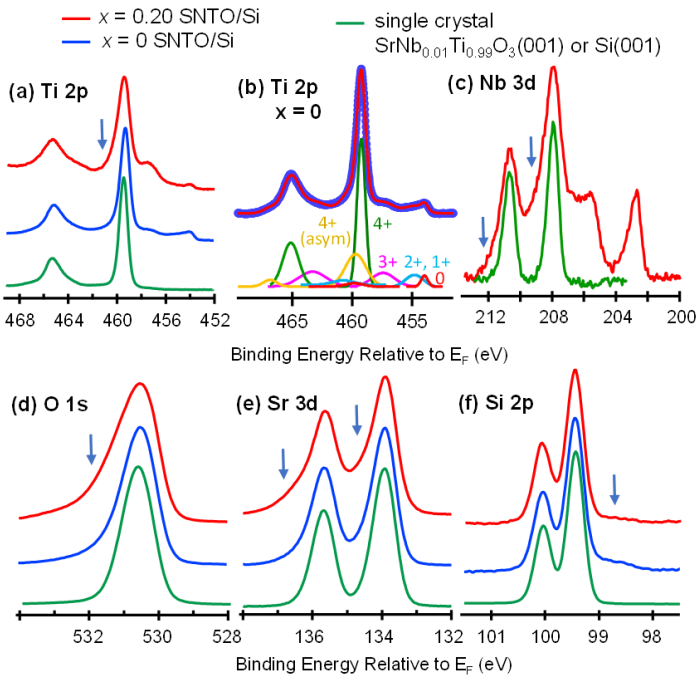


Figure 6-7: Core level spectra taken with HAXPES of x = 0 (red) and 0.2 (blue) heterojunctions along with bulk SNTO (green). Asymmetries of core level peak were seen in Ti 2p, Nb 3d, Sr 3d, and Si 2p spectra at higher binding energy shoulder, pointed out by arrows. Lower binding energy shoulders of Ti 2p were caused by multiple Ti valences.

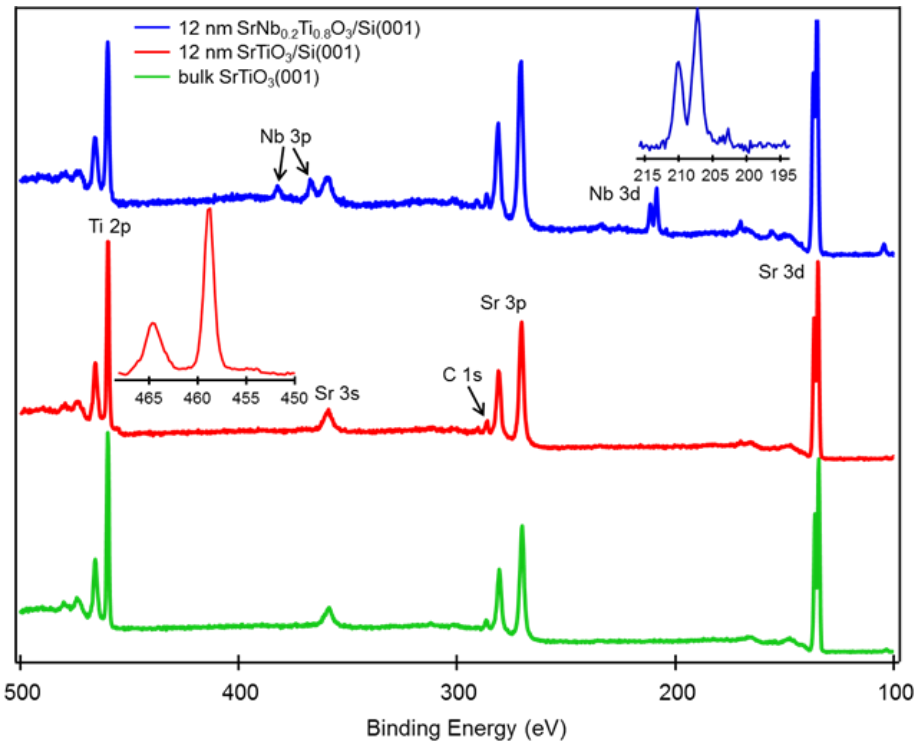


Figure 6-8: Spectra taken with conventional XPS for x = 0 (red) and 0.2 (blue) sample along with bulk STO (green). Insets are the zoom in of Ti 2p and Nb 3d core level peak, where no asymmetry of core level peak was found.

The core level peak asymmetries and multiple valences spectra features exhibit depth dependence indicating those features arise near the oxide-semiconductor interface. Conventional XPS was utilized to study the depth dependence of these asymmetries and multiple Ti valences, since the conventional XPS has a probe depth that is about 3 times smaller than HAXPES at 6 keV. The XPS spectra for 12 nm SNTO films with x = 0, and 0.2, along with the bulk STO (001) standard is shown in figure [6-8]. The insets show the zoom in Ti 2p and Nb 3d spectra for x = 0 and x = 0.2 heterojunctions respectively, where these insets are the only core level spectra that have slight deviation from the measured bulk STO spectrum. Both insets show low binding energy tail, which indicate of reduced valences. However, the intensities of the reduced species seen here are much lower than the one seen in HAXPES spectra. There is also no core level peak

asymmetry to be found in the conventional XPS spectra, which is seen in the HAXPES data. These results led us to believe that these reduced species are due to the screening of Ti^{4+} and Nb^{5+} from the itinerant electrons, which are reside deeper in the film due to the large built-in potential.

In addition to conventional XPS, angle-resolved HAXPES was also used to study the depth dependence asymmetries and multiple valences features seen in HAXPES spectra. In angle-resolved HAXPES, the effective probe depth decreases as the take-off angle for measurement decreases. Figure [6-9] shows the angle-resolved Ti $2p_{3/2}$ and Si 2p HAXPES spectra for $x = 0$ SNTO/Si heterojunction. As the electron take-off angle decreases, the peak of Ti $2p_{3/2}$ shifted to higher binding energy as a result of built-in fields. The high binding energy asymmetries in Ti $2p_{3/2}$ spectra, pointed out by the arrow to the left of Ti $2p_{3/2}$ peak, decreased when the probing depth move away from the interface, because the built-in fields are stronger at the interface. The Ti $2p_{3/2}$ low binding energy shoulder also decreased as the take-off angle decreased, indicates that the multiple Ti valences mainly reside deeper in the film. The Si 2p spectra also shows a reduction in low binding energy shoulder as the take-off angle increased. From the obtained results, we concluded that the core level peak asymmetries and multiple valences features are depth dependence and reside close to the oxide-semiconductor interface.

In order to confirm that the lower valences and the asymmetries of the most prominent peaks, as seen in the HAXPES spectra for the SNTO films grown on Si, are strictly due to the heterojunctions' properties, XPS measurements were also taken for SNTO film that are grown on LSAT substrate with $x = 0$ and 0.1 to compare with those grown on Si, and the results are shown in figure [6-10]. These films were grown in the exact same oxidation and temperature conditions as the films grown on Si substrate. As seen in the figure, there are no multiple valences or

asymmetries in Ti 2p and Nb 3d spectra for SNTO film grown on LSAT, [74] which confirm the independent heterojunction's properties grown on Si substrate.

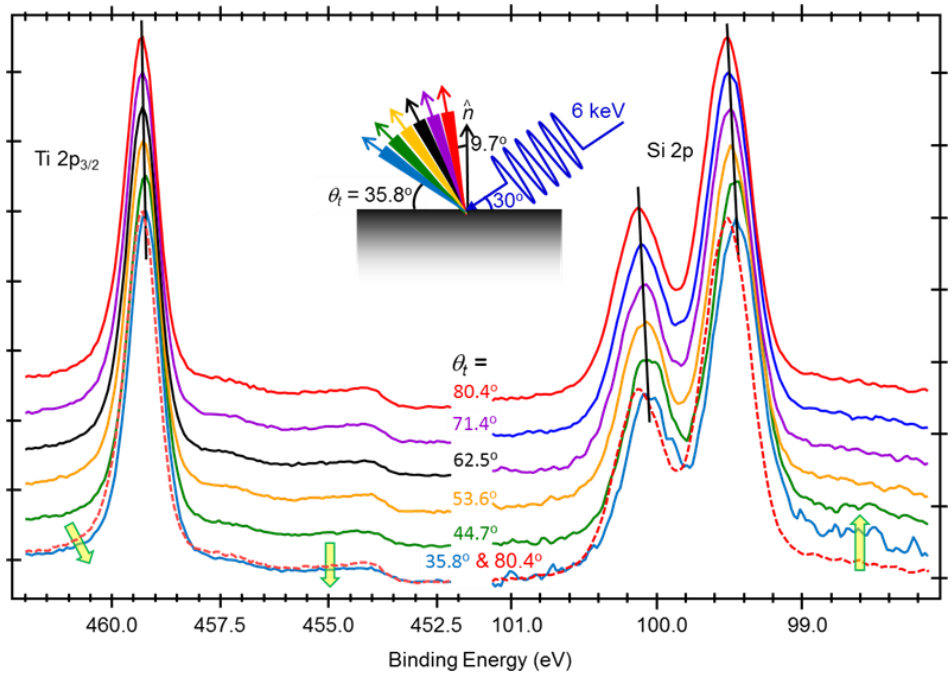


Figure 6-9: Angle-resolved Ti 2p3/2 and Si 2p HAXPES spectra for x = 0 SNTO/Si heterojunction. As the measurement take-off angle decreased, Ti core level peak asymmetries and lower valences features also decreased. Si lower binding energy shoulder features increased as the take-off angle decreased (closer to Si surface).

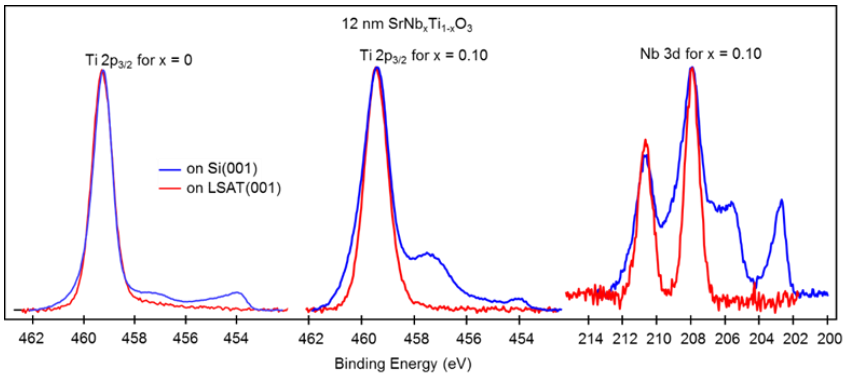


Figure 6-10: Core level spectra of 12 nm SNTO grown on Si and LSAT substrate for comparison. No lower valences and asymmetries were seen in SNTO grown on LSAT spectra, which indicates the abnormal features are due to oxide-semiconductor heterojunction's properties.

With the advantage of having large probe depth of HAXPES near normal emission, we show that the built-in fields caused the asymmetric and multiple valences features in the SNTO and Si Spectra, and that we could determine the spatial variations of these built-in fields from the HAXPES spectra. In order to analyze the spectra from the sample, Dr. S. A. Chambers and Dr. P. V. Sushko first modeled the Si 2p and Ti 2p spectra for $x = 0$ and $x = 0.2$ SNTO sample using sum of spectra taken from single crystal 1 % Nb-doped STO that are minimally affected by surface core-level shifts and band bending (figure [6-11]). The modeled Si 2p and Ti 2p reference spectra were assign to their corresponding peak in each layer within the probe depth. The intensities of the spectra were attenuated with respect to depth (z) with an inelastic damping factor, $\exp(\frac{-z}{\lambda sin\theta_t})$, where λ is the attenuation length, estimated to be around 7 nm for Si and 6 nm for STO. [72] Figure [6-12] shows a schematic of each individual layer of spectra, where the peaks shifted to a higher binding energy with built-in electric fields. Then, the heterojunction spectra were fitted to the sum of all layers of reference spectra.

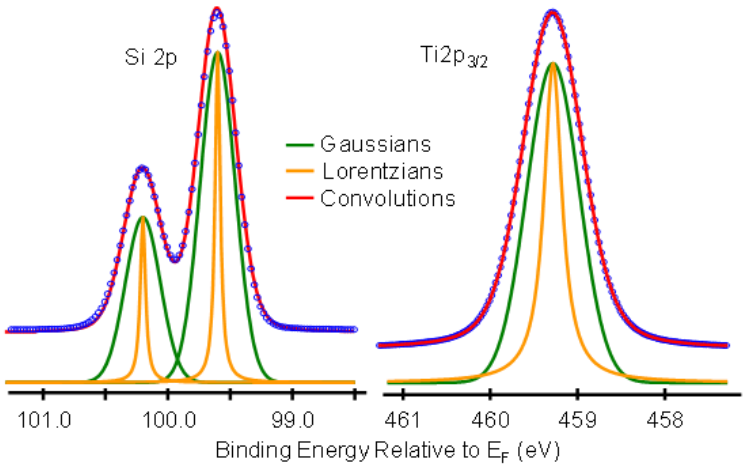


Figure 6-11: Reference Si 2p and Ti 2p3/2 spectra for clean Si substrate and 1% Nb doped STO bulk crystals. The fits to Voigt functions (red) were deconvoluted into Gaussians (green) and Lorentzians (yellow). These modeled spectra are minimally affected by band bending.

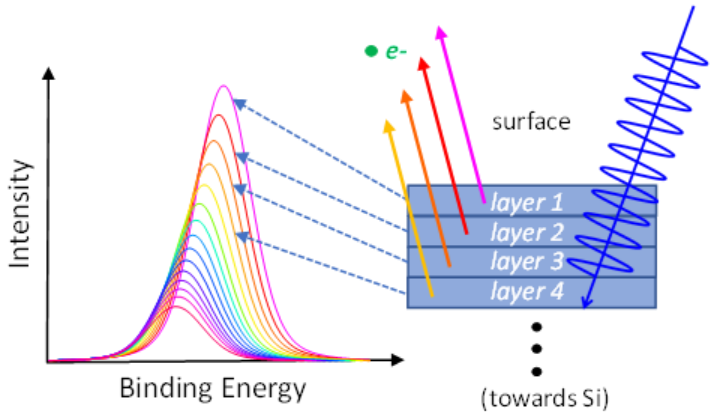


Figure 6-12: Schematic of depth dependence spectra shift for heterojunction contains built-in electric field across interface. The intensities of the spectra were attenuated according to their depth.

To fit the heterojunctions spectra, random binding energy was assigned to all layers. [72] These energies were sorted and reassigned to the layers to have the binding energy at their maximum intensity, $\varepsilon_{\max}(j)$, which is a function of depth. Then, a trial simulated heterojunction spectrum, $I_{\text{sim}}(\varepsilon)$, was created by summing over all spectra. In order to obtain the best fitted binding energy, a cost function as shown below (equation 6.7) will need to be minimize. The first term quantifies the goodness of the fit between the measured and simulated spectra, while the second term is to minimize the potential discontinuities between each layer.

$$\chi = \sqrt{\frac{1}{n}\sum_{i=1}^{n}\left[I_{\text{exp}}(\varepsilon_i) - I_{\text{sim}}(\varepsilon_i)\right]^2} + p\sum_{j=1}^{m}[\varepsilon_{\max}^{k}(j) - \varepsilon_{\max}^{k}(j+1)]^2 \quad [6.7]$$

The fitting from above fitted the asymmetric line shapes for both x = 0 and 0.2 heterojunction very well, as see in figure [6-13]. A total of 350 Si layers were included in the model, with only the first 220 layers have varied potential, because the contributions from deeper

layers are too small and can be neglected. Moreover, all 31 layers that contain Ti were included in the model. The right side of figure [6-13] (a) and (b) show the fit to the experimental heterojunction $x = 0$ and $x = 0.2$ spectra respectively. Whereas, the left side of the figures show the contour intensity plots of the layer-resolved spectra versus the distance from the interface.

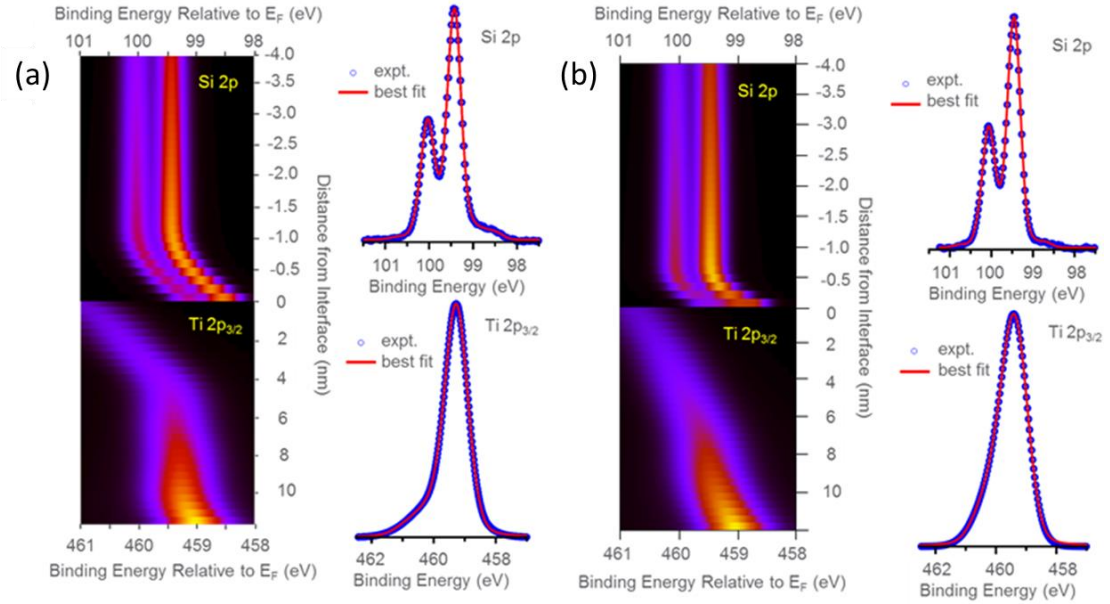


Figure 6-13: On the left side is the contour intensity plots of layer-resolved spectra for (a) x = 0 and (b) x = 0.2 heterojunctions. On the right is the sums of all spectra taken experimentally from both heterojunctions.

After fitting, a spatial map of the band bending across the $x = 0$ and $x = 0.2$ SNTO-Si heterojunctions was obtained using the Si 2p and Ti 2p spectra. Figure [6-14] shows the valence band spectra of the reference SNTO bulk crystal and Si. The valence band spectra allow us to determine the energy difference between the valence band maximum and the core-level energy. In order to map out the band bending, we can calculate the valence band edge relatives to the Fermi energy using $E_V(z) = E_{CL}(z) - (E_{CL} - E_V)_{ref}$, where $E_{CL}(z)$ is the depth dependence core-level binding energy and $(E_{CL}\text{-}E_V)_{ref}$ is the energy difference between the valence band

maximum and the core-level energy of the reference materials, i.e. the bulk single crystal STO or Si. The conduction band edge is just $E_V(z) - E_g$, where E_g is the band gap of the material. Figure [6-15] shows the band bending across the interface. The Si bands bend upward when approaching the interface, with the valence band maximum (VBM) very close to the Fermi energy level which accommodates the hole gas. Moreover, the bands on the SNTO side also bend upward as they move away from the interface.

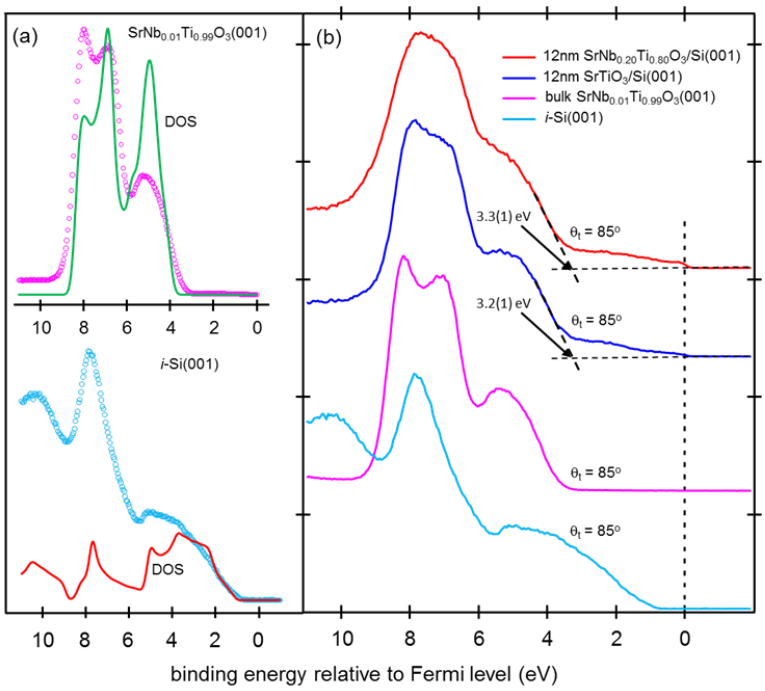


Figure 6-14: (a) HAXPES spectra of the i-Si(001) and SNTO bulk crystal valence bands, along with their Gaussian broadened theoretical densities of states. (b) Valence band spectra of SNTO bulk crystal, 12 nm heterojunctions and Si.

The formation of hole gas and built-in electric fields across the interface arise from the interplay of three phenomena, namely, n-type oxygen impurities in the surface of Si, type-III band alignment, and surface depletion in the SNTO. Heavy oxygen impurity (~ 10^{21} cm^{-3}) was found near the substrate surface even in a undoped Si substrate using time-of-flight secondary

ion mass spectroscopy (ToF-SIMS), as shown in figure [6-16]. The red color data indicates the oxygen densities in figure [6-16]. The oxygen impurities could diffuse to the surface during growth temperature and become n-type donors in the undoped substrate, [75] which makes the SNTO-Si heterojunction a n-n isotype junction.

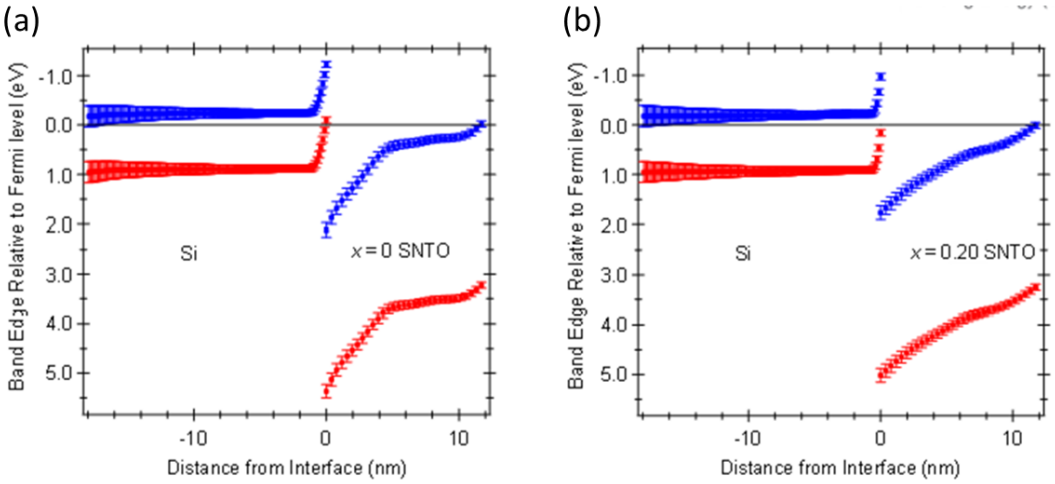


Figure 6-15: Band bending across the interface for (a) x = 0 and (b) x = 0.2 heterojunctions. The Si valence bands bend upward when approaching the interface, with VBM very close to the Fermi level, which accommodates the hole gas.

A type-III band alignment was also found in the SNTO-Si heterojunctions. The valence band offset (VBO) can be determined using the following equation,

$$\Delta E_V = \left(\Delta E_{Ti2p\frac{3}{2}-Si2p\frac{3}{2}}\right)_{int} + \left(E_{Si2p\frac{3}{2}} - E_V\right)_{Si} - \left(E_{Ti2p\frac{3}{2}} - E_V\right)_{SNTO}$$

Where $\left(\Delta E_{Ti2p\frac{3}{2}-Si2p\frac{3}{2}}\right)_{int}$ is the difference between the Ti 2p and Si 2p core-level binding energies at the interface, while the second and third term is the difference between core-level binding energy and the VBM for Si and Ti respectively. The corresponding value for

$\left(\Delta E_{Ti2p_{\frac{3}{2}}-Si2p_{\frac{3}{2}}}\right)_{int}$ is 362.66 eV, $\left(E_{Si2p_{\frac{3}{2}}}-E_V\right)_{Si}$ is 98.54 eV, and $\left(E_{Ti2p_{\frac{3}{2}}}-E_V\right)_{SNTO}$ is 455.74 eV. Whereas, the calculated VBO is 5.46 eV and 4.86 eV for x = 0 and x = 0.2 heterojunctions. By using $\Delta E_V - \Delta E_g$, we also calculated the conduction band offset to be 3.33 eV for x = 0 and 2.74 for x = 0.2. With this type-III band alignment setup, the electrons in the Si valence band were enabled to transfer to SNTO conduction band. [76]

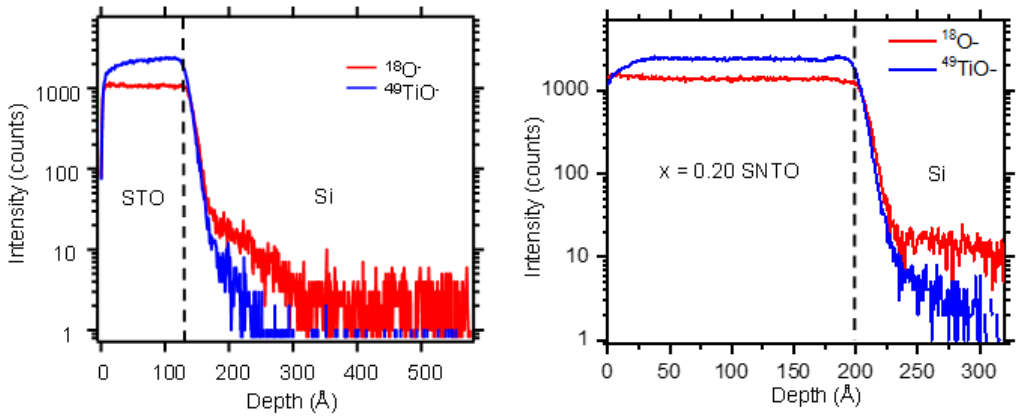


Figure 6-16: ToF-SIMS shows large amount of oxygen impurities at the heterojunctions interface. The red color data shows the number of oxygen impurities, where most of the impurities reside near the interface. Blue color data is the TiO^- signal, which shows the maximum knock-on effect since TiO^- has similar mass as Cs ions.

From the HAXPES spectra as seen in figure [6-15], we also noticed that the band also bend upward close to the SNTO surface, where this effect is consistent with surface depletion. [77] In order to confirm the field induced by surface depletion is coupled to the field associated with the hole gas, a 20 nm x = 0.2 SNTO sample that was grew with the same condition as the 12 nm sample, along with the 12 nm x = 0.6 SNTO sample were used for testing. If the fields induced by surface depletion is coupled to the fields associated with the hole gas, then a thicker sample or a higher concentration sample will weaken the coupling and cause a decrease in hole carrier density. The transport measurements of a thicker sample are shown in figure [6-17] and

confirm our hypothesis that the fields induced by surface depletion are indeed coupled to the fields induced by the hole gas. The hole carrier density n_h decreased by around 10 times with the film thickness increased by only 8 nm. No hole gas formation was found on the x = 0.6 Nb doped heterojunction, which has the highest carrier density further confirm the fields are coupled together.

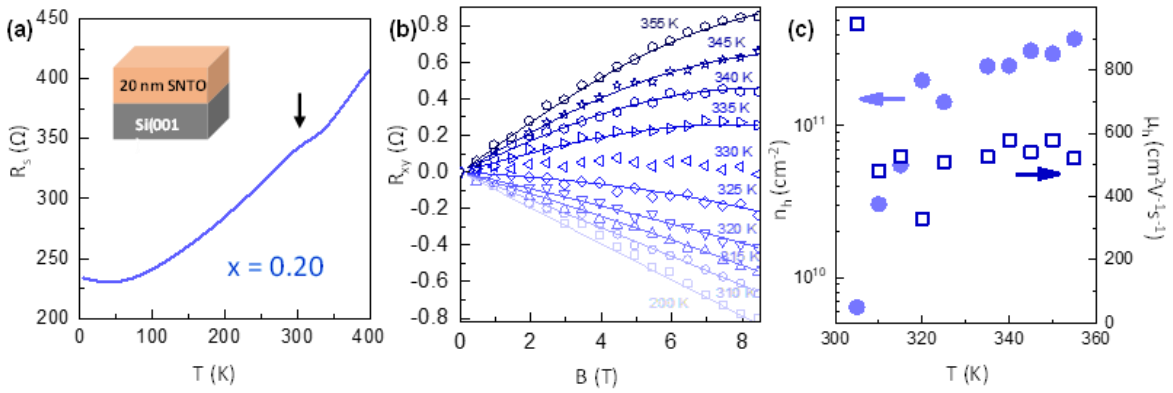


Figure 6-17: Transport measurement of 20 nm x = 0.2 heterojunction. (a) Sheet resistance of the 20 nm SNTO film shows a small anomaly at around room temperature. (b) Hall resistances still show cross over in sign. (c) Hole density is around 10 times smaller than those 12 nm films. Whereas the mobility is closed to 500 $cm^2V^{-1}s^{-1}$.

We suspect the increase of dielectric constant of SNTO as temperature decrease would enhance the screening of electron carriers, which will push the electron carriers in SNTO back into Si, therefore making the hole gas formation temperature dependent. [77] [78] Figure [6-18] shows the electron carrier density and mobilities for Nb concentration of 0.08 and 0.2 samples with respect to temperature. Both samples show decrease of carrier density and mobility as the temperature decrease, which indicates that some of the carriers begin to localize when the temperature decrease. A more thorough experiment is needed in order to investigate the dielectric constant of SNTO at low temperature.

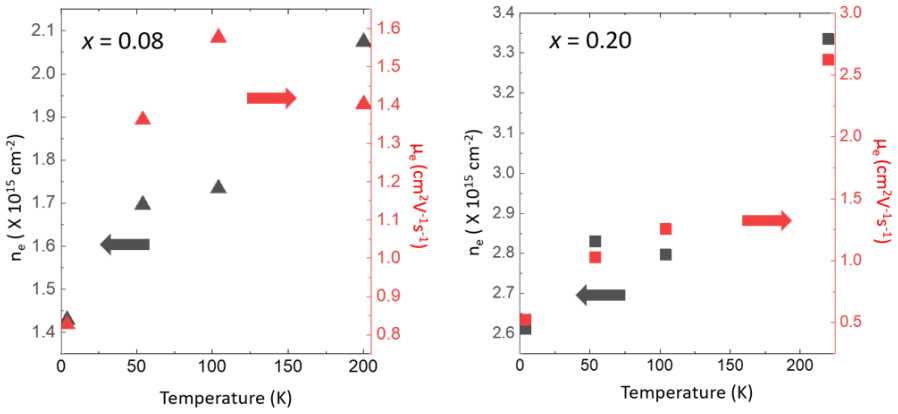


Figure 6-18: Temperature dependence electron densities and mobilities for x = 0.08 and 0.2 heterojunctions. The electron densities for both heterojunctions decreased as the temperature decreased, which indicates some of the carriers localized at low temperature.

6-4: Conclusion

In conclusion, we have demonstrated that by controlling the dopant level and carrier density in the hybrid heterojunctions, we were able to tune charge transfer and built-in electric fields across the interface. We were also able to map out the built-in fields layer by layer across the whole oxide-semiconductor heterojunctions interface using HAXPES. In addition, we have observed the interplay between band-offset, surface-depletion effect, and dielectric constant in our transport data that conclude the appearance of band bending in our heterojunctions. We also found out that the band alignment between STO and Si can be altered by introducing carriers into oxide film, which lead us to believes that we may be able to affect the work function by introduce oxygen vacancies or dopant carriers. [79]

Chapter 7 : Fabrication of $BaTiO_3$ microbridge with wet etching

7-1: Introduction

Microelectromechanical systems (MEMS) is the technology of creating microscopic devices or systems that generally consist of mechanical and electrical components. [80] A lot of the applications of MEMS can be characterized into two general classes, namely sensors and actuators. Typically, sensors are devices that detect surrounding information and convert the information into electrical signal, while actuators convert electrical signal into mechanical movement. In this regard, piezoelectric MEMS has gained a lot of research interest due to its usefulness in sensing and energy harvesting technologies. [81] [82] [83] [84] [85] Some of the applications of piezoelectric MEMS include surface acoustic wave (SAW) devices, resonators, and pressure sensors. [86] In addition, future piezoelectric MEMS applications include piezoelectric vibration energy harvesters (PVEHs), which are one of the important devices for Internet of Things technologies. [87] [88] [89]

Complex oxides exhibit unique properties that can be introduced to MEMS research, such as the piezoelectricity and ferroelectricity, which are perfect for piezoelectric MEMS devices. $PbZr_xTi_{1-x}O_3$ (PZT) was known for its strong piezoelectric properties, and groups have been using PZT to fabricate piezoelectric MEMS devices, such as accelerometers, force sensors, and membrane or cantilever structure devices. [90] [91] [92] [93] But, PZT is not an environmentally friendly material, which causes researchers to look for other materials that can replace PZT due to regulation of Pb usage. $BaTiO_3$ (BTO) is a complex oxide with perovskite structure that exhibit good piezoelectric property. [94] [95] [96] Groups have reported to use

BTO based material to fabricate MEMS devices. [97] Moreover, $LiNbO_3$ was also reported to use for fabrication of resonator. [86]

Free standing structure is one of the basic structures for piezoelectric MEMS devices in both industry and scientific research. Cantilever type devices were widely used for sensing application, energy harvesting device, and AFM tip. [80] Moreover, cantilever structures can also be used to study how strain can affect material properties. Previous studies have utilized cantilever structures to study the piezoresistive effect of $La_{1-x}Sr_xMnO_3$ (LSMO) thin film and the flexoelectric effect of $SrTiO_3$ (STO) film. [98] [99] As for bridge type devices, epitaxial $YBa_2Cu_3O_7$ (YBCO) bolometers and LSMO bolometers were reported previously. [100] [101]

In order to fabricate complex oxide devices, etching of complex oxides sample is needed. Etching is one of the fundamental methods on device patterning in fabrication process, and there are two main types of etching, namely, wet etching and dry etching. [102] Wet etching uses a chemical solution to etch material, which base on chemical reaction between the etchant and material. In contrast, dry etching uses either a combination of chemical and physical method to etch material, such as reactive ion etching and plasma etching, or purely physical method, such as ion milling. [102] Wet etching is generally used for larger device feature due to its simplicity and higher etching rate as compare to dry etching. In addition, dry etching can be much more complicated than wet etching since it is necessary to take different factors into account while creating a dry etching recipe, such as chamber pressure, RF power, and gases used in the process.

There are very few wet etching studies on BTO, while wet etching on other complex oxide, such as PZT, $SrTiO_3$ (STO), YBCO, and LSMO have been done before. Most of the wet etching on complex oxide focus on etching single crystal STO substrate to get a TiO_2 terminated surface in order to use it as oxide growth substrate. [103] [104] [105] The other studies reported

that YBCO and LSMO can be etched using HNO_3 and HCl respectively. [98] [97] There are also extensive studies on both wet and dry etching of PZT, since PZT itself was used in industry. [106] [107] [108] Dry etching method, such as ion milling, was mostly reported on etching BTO and $Ba_{1-x}Sr_xTiO_3$ (BST). [109] [110] [111]

In this chapter, I report a wet etching study on the effect of oxygen vacancies and dislocations to material etching rates. 156 nm BTO/STO stack and 200 nm STO films with different annealing conditions were etched with HF Dip 10:1, which is a mixture of 10 parts H_2O with 1 part of 49% hydrofluoric acid (HF). Etching rates were also determined by correspond etching depths to etching durations. Samples that were annealed have lower etching rate due to decrease in oxygen vacancies and sample dislocations.

The ability to wet etch BTO and STO films with HF Dip 10:1 has allowed us to fabricate complex oxide devices. A fabrication process recipe was developed utilizing some of the basic patterning, deposition and etching technique, such as silicon nitride deposition with sputtering and wet etching of BTO and STO film. 156 nm BTO/STO microbridges were fabricated successfully using the newly developed recipe. Optical microscope images and scanning electron microscope (SEM) images confirm the 156 nm oxide bridge is fully suspended.

One of the potential applications of a microbridge is to use as a new platform for scanning transmission microscope (STEM) imaging. A new STEM imaging platform that allowed a lateral electric field to be applied across the sample was designed. In combination with back side physical milling of Si substrate, the microbridge was designed to set on top on a thru hole. A 156 nm BTO/STO microbridge that was aligned on top of a thru hole was fabricated successfully with the new design, where the crystallinity of the microbridge was confirmed by STEM diffraction measurement.

7-2: Film growth

Two different samples were grown with oxide MBE system. 156 nm BTO/STO stack was used for both the etching rate experiment and device fabrication while 200 nm STO film was used for the etching rate experiment. An epitaxial 150 nm BTO and 6 nm STO stack was grown on undoped float zone double sided polish Si wafer with our home-built MBE system. Si wafer was first exposed to oxygen plasma to clean off any residual organics, and growth method developed by McKee et al. was used to obtain a Si wafer with 0.5ML of SrO as a template for subsequent layers. [3] 2.5 unit-cells (u.c.) of SrO and 2 u.c. of TiO_2 was deposited at room temperature and then heated up to 580 ^oC to form 2.5 u.c. of crystalline STO. Then, the remaining 13 monolayers of STO was deposited at substrate temperature 600 ^oC, and the remaining 150 nm BTO was deposited at substrate temperature 720 ^oC in a background oxygen pressure of 4×10^{-7} Torr. As for the 200 nm STO film, the first 5 nm of STO was deposited at 580 ^oC, and the remaining 195 nm STO was deposited at substrate temperature 650 ^oC. Reflecting High Energy Electron Diffraction (RHEED) was used in situ with the growth process to make sure the film is single crystalline during growth. Once the growth was done, both substrates were sent to cleanroom to be diced along the [100] direction (i.e. 45^o from the major flat). Devices were fabricated in UTA class 100 Cleanroom using the fabrication recipe listed at the end of chapter.

7-3: Photomask making

Two different masks were designed using AutoCAD, which contained either two out of the three device designs, namely, XRD bridge device, STEM bridge device, and cantilever device. A full view of a photomask is shown in figure [7-1]. All photomasks were made into both clear and dark field for pattern and lift off processes. Each of the device design also include

two to three different layers, which is shown in figure [7-3] (a), (b), (c). The three layers of mask are usually referring to 1st layer, 2nd layer and 3rd layer mask design respectively. 1st layer mask is the pattern use for the first lithography process which is the device HF etching layer. 2nd layer mask is for nickel lift off process, and 3rd layer mask is for silicon nitride lift off process. All three devices use very similar fabrication steps, as the recipe was designed specifically to work for all devices. The silicon nitride layer is to protect silicon under KOH etching, and nickel is used for electrical contact purpose. The photomask was made by the University of Texas at Dallas Cleanroom Research Laboratory.

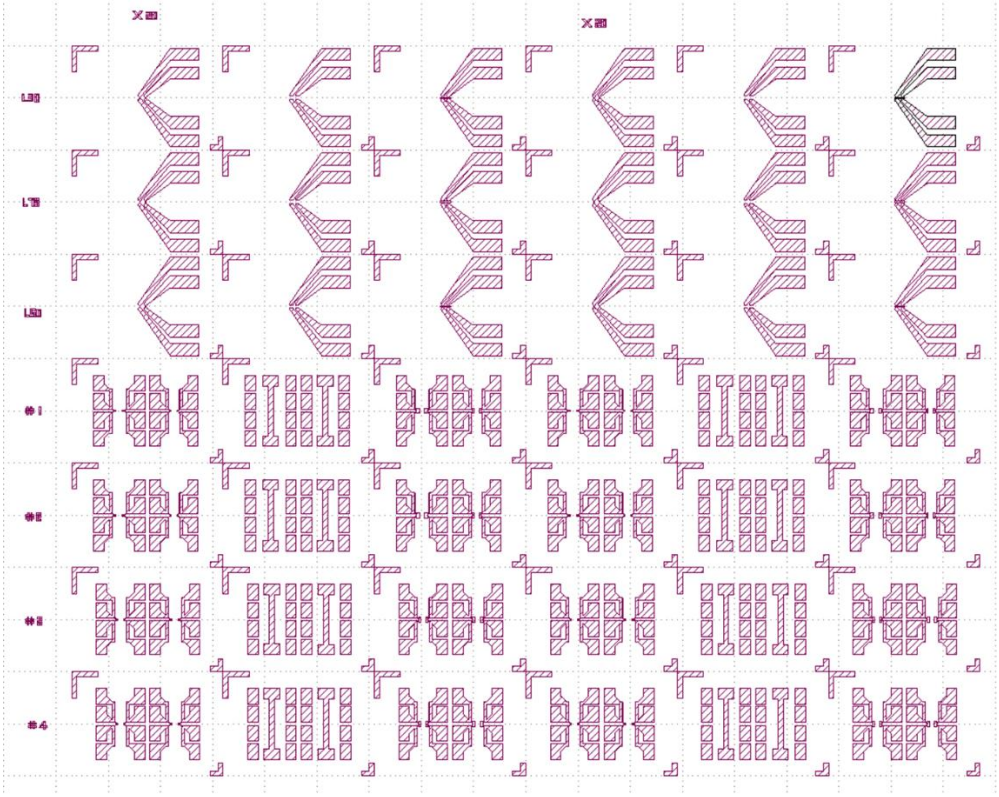


Figure 7-1: Full view of a photomask, which contain all three layers of the STEM bridge and cantilever design.

There are couple points that need to be considered while designing a photomask. It is particularly important to know that photoresist will clump up along the edge of the sample while spinning on photoresist for lithography. Since the mask was designed to work for small sample size (5.8 mm × 4 mm), so it is very important to keep at least 500 microns from the edge of the sample blank while designing a photomask. Next, it is also very important to make sure to include fiducial mark on the mask, as it serves the purpose to connect all layers of masks and make sure they stack up together nicely. As seen in figure [7-2], all devices were designed about 500 – 600 µm away from the edge of sample and they all have L-shape fiducial marks at two of the corners.

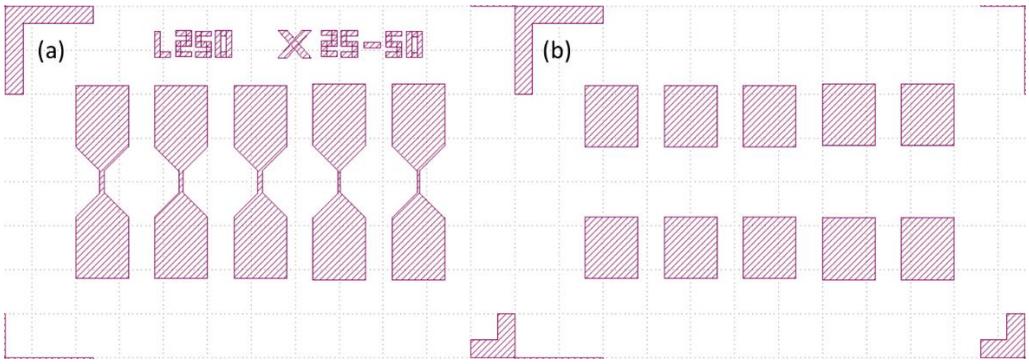


Figure 7-2: Design of microbridge for XRD measurement, where the devices are around 500 – 600 µm away from the edge to prevent photoresist clump up close to the devices.

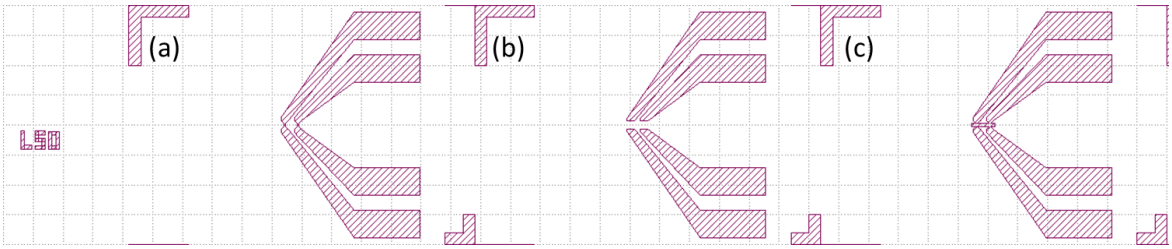


Figure 7-3: Design of microbridge for STEM measurement. (a) 1st layer of mask for HF oxide layer etching. (b) 2nd layer of mask for nickel lift off process. (c) 3rd layer of mask for silicon nitride lift off process.

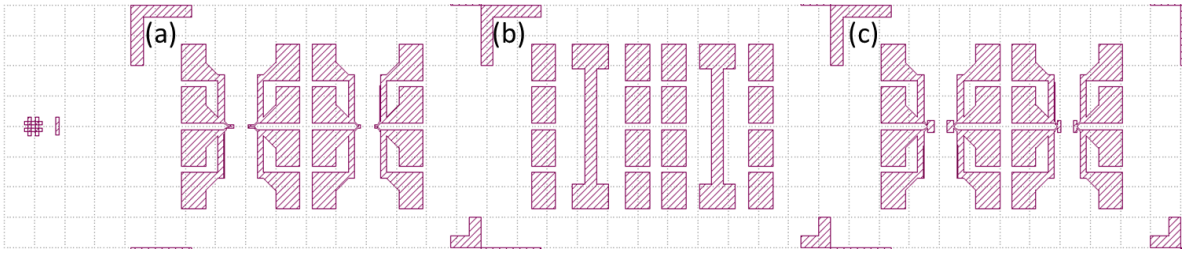


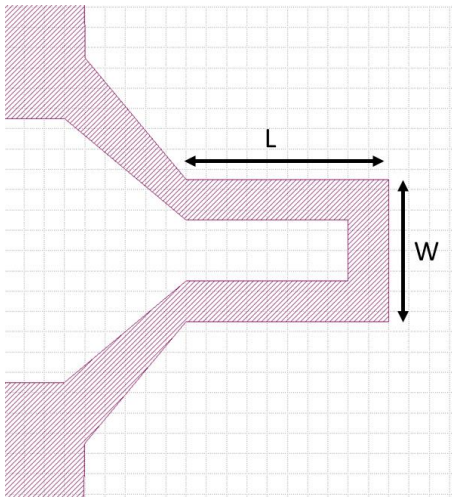
Figure 7-4: Design of cantilever device with (a), (b), and (c) are the 1st, 2nd, and 3rd layer of mask respectively. The #1 at the far left indicates this set of cantilever device has the dimension listed in the table below.

All three devices were designed with different dimensions, where the dimensions are indicated as below. Figure [7-2] shows the design of XRD bridge, with the length of the bridges are all 200 µm, while the bridge width "x" is either 25 or 50 µm. Figure [7-3] shows the design of STEM bridge device. This STEM bridge device was designed specifically for the STEM system used by Dr. James LeBeau group at Massachusetts Institute of Technology (MIT). The four contact pads on the right-hand side of the design was fix at that certain coordinates as they were designed to be connected toward the STEM system for lateral field measurement. The bridge width is set to be constant at 20 µm, while the bridge length ranges from 30 to 300 µm. As for the third device's design, which is shown in figure [7-4] is a prototype of a cantilever device. They are label with number 1, 2, 3, and 4 at the left-hand end of the mask for different dimensions. Each number set will have 4 cantilever devices with two different dimensions, and the dimensions are included in table [7.1]. Each of the device will have four contact pads for 4-point measurement, with a gate contact at the center. The device width is either 50 µm or 70 µm, and the device length range from 50 to 100 µm. The distance between the cantilever tip and the gate was set to 20 µm. The gate is designed for applying voltage bias in order to bend the cantilever, which means that the distance between the cantilever and the gate is crucial. The

distance must be large enough to satisfy the smallest resolution for mask making, lithography, and wet etching, as well as small enough to create the required force to bend the cantilever.

	Length (L)	Width (W)	Opening width	Opening length
1a	100	50	10	80
1b	40	50	10	20
2a	100	70	30	80
2b	40	70	30	20
3a	50	50	10	30
3b	75	50	10	55
4a	50	70	30	30
4b	75	70	30	55

Table [7.1]: Dimension of cantilever devices, where "a" indicates the device on the left and "b" indicates the device on the right. All dimensions show in the table are in μm. "L" is the length and "W" is the width of the cantilever. "Opening" is the center space part.



7-4: Photolithography

Photoresist was used to pattern device and as a wet etching mask due to its resistance against most acid. The difference between a positive and a negative resist is how they react when exposed to ultraviolet (UV) light. Positive resist will have its chemical structure changed after

exposed to UV light, and can be dissolved by resist developer. In contrast, negative resist will become insoluble after exposed to UV light, and the part that didn't expose to UV light can be removed using negative resist developer. [102] Schematic of the difference between positive and negative resist is shown in figure [7-5]. Positive resist S1813 was chosen for our process since positive resist generally has a better resolution as compare to negative resist. By going through spin on at 4000 RPM for one minute and a softbake at 115 ^{o}C for one minute, the resist thickness is about 1.3 µm. A softbake step is necessary as it dries off most of the solvent in the resist and prepares it for exposure. [112]

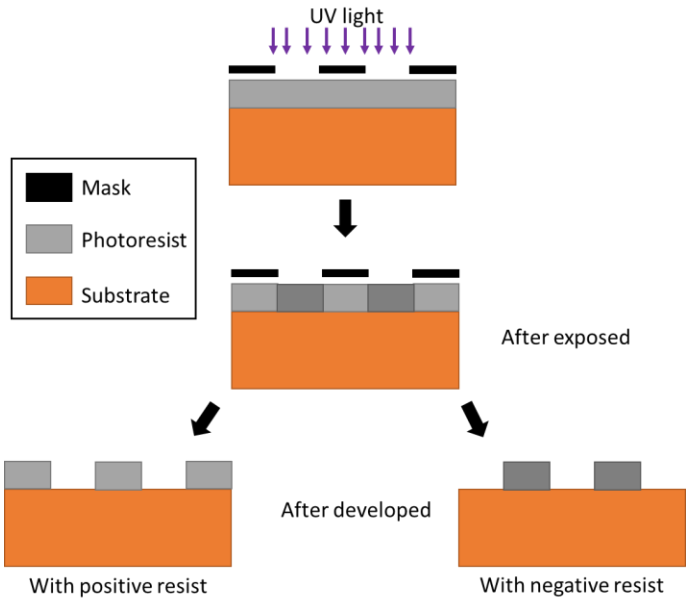


Figure 7-5: Difference between positive and negative photoresist after exposure. Positive resist will be able to dissolve by developer after exposed to UV light, while negative resist will strengthen after exposed to UV light.

The OAI backside aligner, which uses the I-line (365nm) UV light for exposure and has a power of 20 mW/cm^2, was used in the lithography process. UV exposure time will differ for different photoresist, and in general a thicker resist will require a longer exposure time. The OAI

backside aligner has a resolution of about 3 μm, which means that the smallest geometry of the designed device must be larger than 3 μm in order to obtain a well-defined geometry. In this recipe, the exposure time is set to 11 seconds, which is enough to expose the 1.3 μm thick photoresist. If the exposure time is longer than 11 seconds, the pattern features will show zig-zag type of edges instead of a straight one. While aligning the mask to the sample, both the corners of the sample piece need to align to the corner of fiducial marks to make sure the sample is not tilted with respect to the mask. The distance between fiducial mark was designed to be the same size as the sample, so if the sample's corners meet all the corner of the fiducial marks' corner, that means the sample was aligned correctly. Then, positive resist developer MF-319 was used to develop the resist. The total developing time ranges from 1 minute 30 seconds to 2 minutes. While developing the pattern, it is recommended to agitate or shake the sample every 15 seconds to slightly speed up the developing process. Developing for more than 2 minutes is not recommended as that will also damage the feature's geometry.

7-5: Silicon nitride and nickel deposition

Silicon nitride and nickel, respectively, protect the Si substrate and provides metal contacts. Both of them exhibit extremely low etching rates in a warm KOH bath. [113] Silicon nitride layer was deposited using AJA-Sputter system. The recipe that was set up in the system has deposition rate of about 1 nm/minute at the center of the substrate holder. Even though silicon nitride will not be etched by warm KOH in principle, but we have realized the nitride layer was mechanically peeled off after etching. We suspect that the peeling is due to adhesive problem from residual of HF etched. In order to increase the adhesion of nitride layer, the sample was bake at 100 ^{o}C for 1 minute after developed, and an additional pre-heat step, which heat up the substrate to 70 ^{o}C for 10 minutes, was added to the sputtering recipe. As for nickel layer, it

was deposited using AJA e-beam evaporator. There is a QCM installed inside the chamber, which was used to determine the deposited nickel thickness in real time.

7-6: Dimension characterization

There are two techniques that were used to measure the film thickness during the process, namely, profilometry and reflectometry. Reflectometer is used when a film was covered across the whole sample without any steps, while profilometer is used whenever there is a step or height difference that's more than 10 nm. The reflectometer has a detector to detect the reflected wave through the film and the substrate, which has different refractive index to determine the thickness of the film. As for the profilometer, it has a tip that is similar to an AFM tip that moves in one direction for ~500 μm in distance. Any step height differences that are larger than 10 nm on the sample will be detected. In principle, profilometer can also be used to determine the roughness of the film if the roughness is larger than 10 nm. This technique was also used to determine the wet etching rate of complex oxide thin films.

7-7: Wet etching

Two different wet etchings were introduced in the fabrication process, namely hydrofluoric acid (HF) etched of the oxide film and potassium hydroxide (KOH) silicon etching. HF Dip 10:1 was used to etch the BTO/STO film. The hydrophobic nature of clean Si was utilized to confirm the complex oxide films were etched completely. When the oxide films were etched completely, the sample can be rinsed with DI water, where water droplets will clump up and tend to stick to the un-etched film site. HF etching of the oxide film is considered isotropic, which means the etching rate should be the same for all directions.

KOH etching on silicon is anisotropic, since the etching rate is different for [100], [110], and [111] directions. [114] The different etching rate in [100] and [110] directions will create a 54.7^{o} slope as shown in figure [7-6], while the etching rate in [111] is very slow, and virtually non-existence. 30% KOH solution was prepared by weighing 69.4g of KOH pallets, and then add in DI water until the whole bath reached 200 ml. This 30% concentration was calculated by weigh, which means that the density of DI water was assumed to be 1 g/ml. The etching rate of silicon in 75 ^{o}C 30% KOH solution is about 1.1 microns/minute.

Figure 7-6: Anisotropic Si etch with KOH. The different etching rate in [100] and [110] directions will create a 54.7^{o} slope.

30% KOH solution was chosen since it is the balance point between etching roughness and etching rate. As seen in figure [7-7] (a), the Si etching rate gets higher as the solution concentration decrease. But it was also known that the etching surface of silicon will be roughen for solution concentration lower than 30%, which indicates that the optimum solution concentration is around 30%. [115] [116] [117] Figure [7-7] (b) shows the etching rate of KOH solution on SiO_2, where the etching rate on SiO_2 is much lower than for Si. In fact, a lot of bubbles will form when the silicon was being etched, while not a lot of bubbles were seen when SiO_2 was being etched. In order to prevent the sample from flipping over during the etching process, a plastic locking twizzer was utilized to clamp on one of the sample corners. When heating up the KOH solution with hot plate, a magnetic stir was used to ensure a uniform

temperature throughout the solution. Undoped silicon was used for thin film growth because any type of doped silicon wafers has a very low etch rate in KOH. Lastly, a list of common material and their etchant are shown below in table [7.2].

Material	Etchant
Silicon	HNA, warm KOH, SF_6 gas
Silicon dioxide	HF, BOE
Silicon nitride	Warm phosphoric acid

Table [7.2]: Common materials used in IC fabrication and their corresponding etchant.

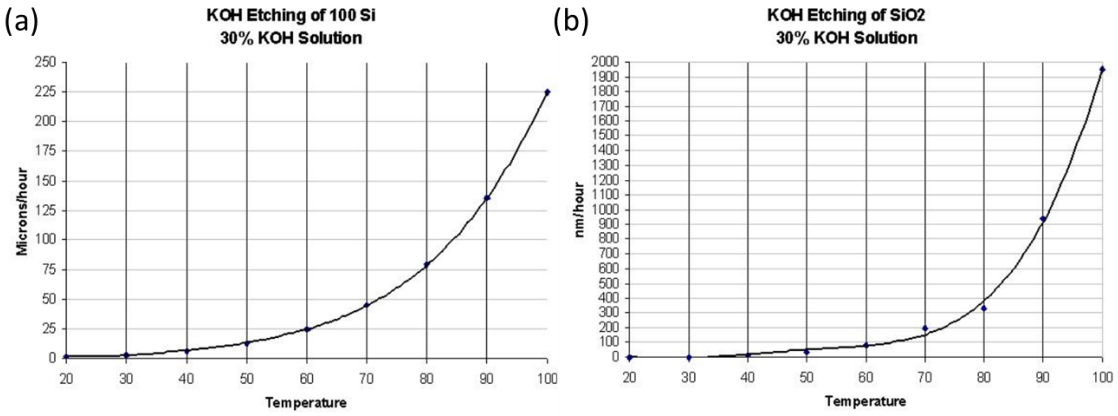


Figure 7-7: KOH etching rate on (a) Si (100) and (b) SiO_2. SiO_2 etching rate with 70 ^oC KOH is close to 300 times slower than Si. Etching rate also increase exponentially with respect to increase of temperature. (Taken from https://cleanroom.byu.edu/KOH)

7-8: Supercritical drying

Supercritical drying was designed to prevent suspended MEMS structures to break due to liquid stiction force. After wet etching, water droplets between the suspended microbridge and the substrate will create a stiction force when it is being dried, and the force is generally strong enough to pull down the suspended structures toward the substrate, causing breakage. So, instead

of blow dry or air dry the sample, supercritical drying was utilized to dry the sample after the structure was released. Supercritical dryer will first flush away water droplets with liquid CO_2. Then the chamber pressure and temperature were increased, which force liquid CO_2 to turn into gas phase directly from liquid without crossing the phase boundary. The schematic phase diagram of CO_2 is shown in figure [7-8].

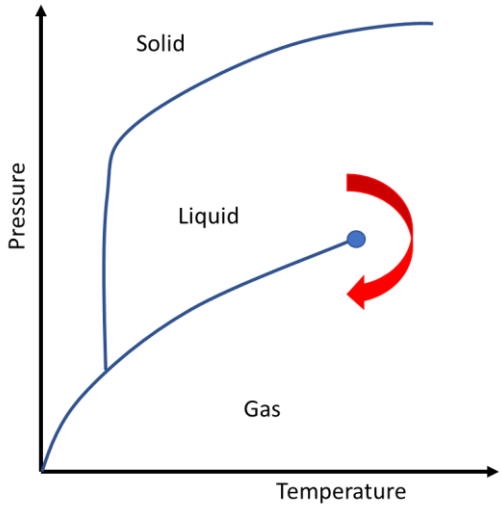


Figure 7-8: Phase diagram of CO_2. Liquid CO_2 was forced to turn into gas phase without crossing the phase boundary under high pressure and temperature (indicates by red arrow).

7-9: Etching and fabrication process

156 nm BTO/STO and 200 nm STO film were annealed at different conditions to study the effect of oxygen vacancies and film crystallinity on wet etching rate. Oxygen vacancies will be filled, and the crystallinity of film will be improved after annealed. The BTO/STO and STO wafer was first diced into 5.8 mm × 4 mm samples, where some of the samples undergo different annealing conditions, which include annealed at 900 ^{o}C in air for two hours and annealed at 450 ^{o}C with ultra-high purity wet oxygen supply for 45 minutes. Then, all samples

went through a 4-steps ultrasonic clean with DI water, Acetone, Methanol, and Isopropanol to get rid of any residual SrO and particles on sample surface. In order to determine wet etching on BTO/STO and STO films, conventional optical lithography process was used along with wet etching to create a step difference on the complex oxide samples, and the step height was measured with a profilometer. Photoresist was spun on and patterned with the procedure mentioned previously. All samples were then etched with HF Dip 10:1 for different durations, and the photoresist was washed away with ultrasonic in Acetone after HF etch. The height difference between the etched and unetched part was measured with a profilometer (KLA-P6), which has a $\pm$2 nm resolution. The pre-process as-grown sample and 900 ^{o}C annealed BTO/STO and STO samples were sent to Dr. Kumah at North Carolina State University for XRD measurements.

With the ability to wet etch complex oxide films with HF Dip 10:1, a recipe was developed to fabricate complex oxide microbridge device utilizing the wet etching technique. the flow diagram with all major parts of the fabrication recipe is shown below, and the recipe is included at the end of chapter. While all different major parts can be separate out and do not need to be continuous, it is still necessary to finish one whole part at once every time. The silicon nitride and the nickel deposition parts can be taken out for some devices, for example the device for XRD measurement do not need to have silicon nitride. A schematic diagram of the fabrication process is shown in figure [7-9]. Materials' selectivity with different etchant was carefully considered during the creation of the fabrication recipe. In addition, the whole process of making a microbridge device with this recipe takes about 15-20 hours.

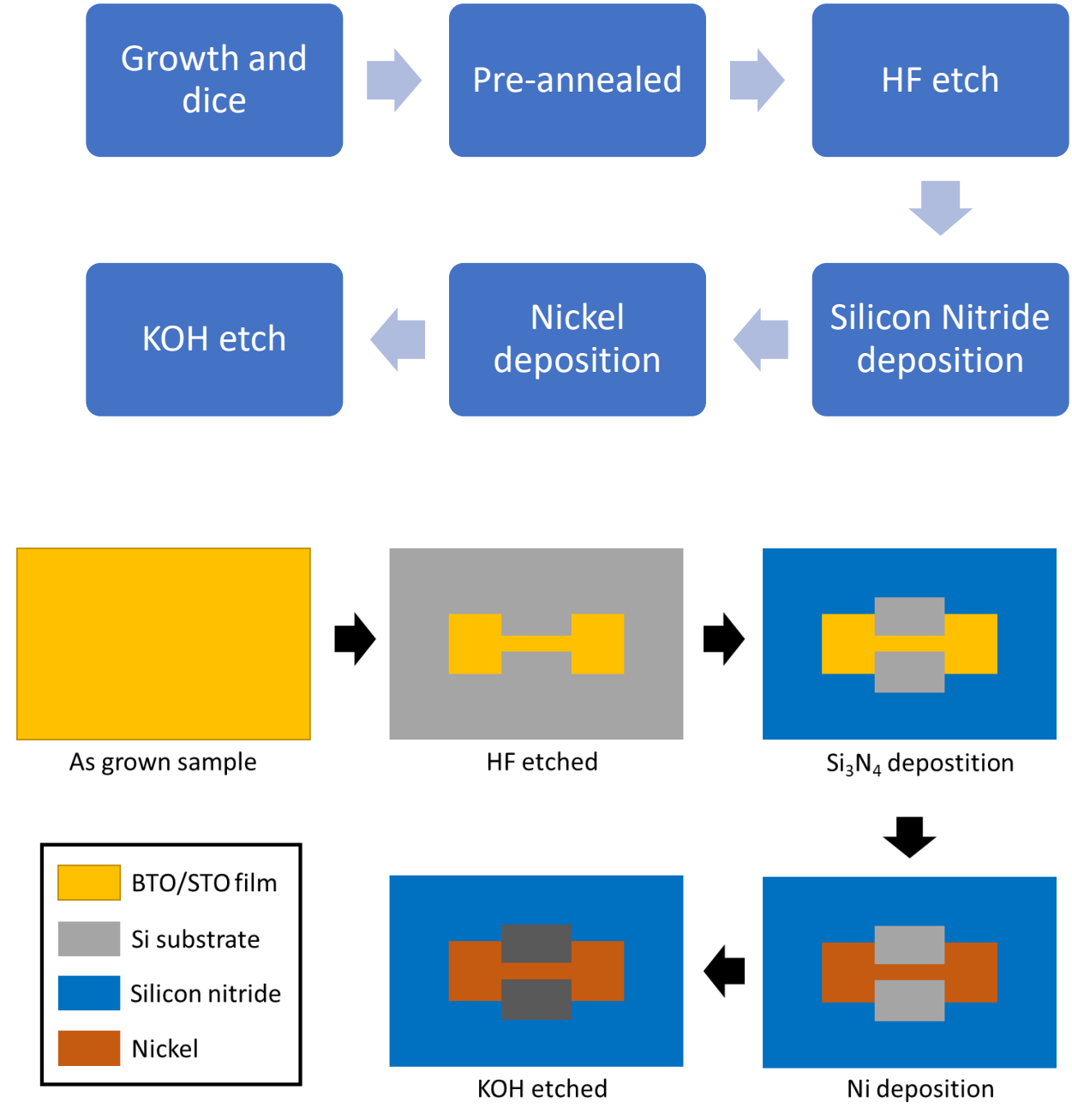


Figure 7-9: Schematic of the fabrication process for fabricating a complex oxide microbridge device.

The newly developed recipe was also used to fabricate a new STEM imaging platform that allows the application of lateral electric field in situ with imaging. In order to fabricate a

platform for STEM imaging, a thru hole underneath the microbridge is needed. The pre-annealed sample was sent to Allied Inc. to get the backside of the sample to physically mill out, as seen in figure [7-10]. Figure [7-10] (a) shows the bottom view, and (b) shows the cross section along the blue dash line in figure [7-10] (a). The milling depth will vary for different substrate, while the remaining thickness needs to be about 40 µm thick in order to hold up for processing.

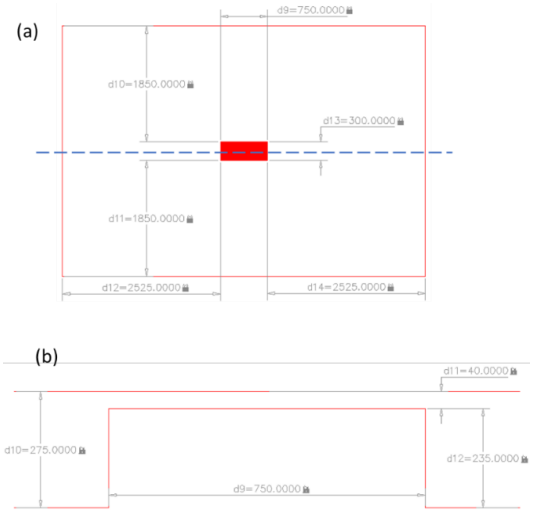


Figure 7-10: Substrate backside physical milling dimension. (a) bottom view, and (b) cross section view along the blue dash line. The dimension of the window is 300 µm × 750 µm, and the remaining thickness should be at least 40 µm.

7-10: Results

The structural properties of the 156 nm BTO/STO and 200 nm STO films were characterized with XRD. Figure [7-11] (a) shows the XRD survey scan of the annealed and as-grown BTO/STO and STO samples respectively, while their rocking curve measurements are shown in figure [7-11] (b) to (e). The BTO/STO rocking curve data shows a significant difference between annealed and un-annealed conditions. The full-width at half maximum (FWHM) of the annealed and as-grown BTO/STO sample are 0.421^{o} and 0.51^{o} respectively.

While the FWHM of the annealed and as-grown STO sample are 0.202^{o} and 0.197^{o} respectively. The results led us to believe that the crystallinity of the annealed BTO/STO film was significantly improved from the as-grown sample. However, there was not much difference between as grown and annealed STO film, even though we would think that the crystallinity should improve after annealed. The insets in figure [7-11] (a) show the RHEED of BTO/STO and STO film in the [10] direction.

The etching results of the BTO/STO and STO samples with different annealing conditions are shown in figure [7-12]. Figure [7-12] shows the plot of measured step height vs. etching duration, and the etching rate can be determined by the slope. Etching rate for BTO/STO and STO samples with different annealing conditions are also include in table [7.3] below. As-grown STO sample has the highest etching rate at around 357 nm/min among all STO samples, while O_2 annealed STO sample has etching rate of 24.24 nm/min and STO sample annealed at 900 ^{o}C has etching rate of 0.78nm/min. The BTO/STO sample that was annealed under oxygen rich environment has the highest etching rate of 390 nm/min, while the as-grown sample and sample that was annealed in air at 900 ^{o}C for two hours have etching rates of 250 nm/min and 155 nm/min respectively.

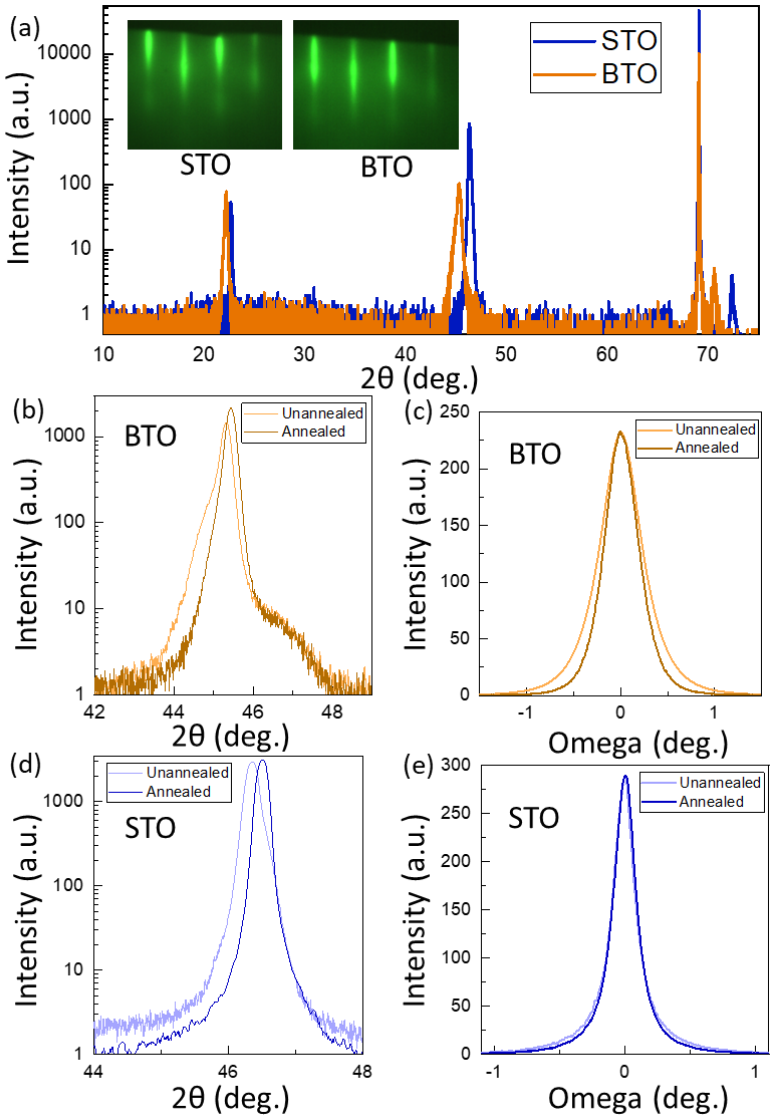


Figure 7-11: (a) Survey scan of un-annealed BTO/STO and STO samples, where inset shows the RHEED taken along [10] direction. (b) and (c) show the zoom in and rocking curve of annealed and un-annealed BTO/STO sample. The FWHM of BTO/STO sample rocking curves decreased from 0.51^o to 0.421^o after annealed. (d) and (e) show the zoom in and rocking curve of annealed and un-annealed STO sample. The FWHM of annealed and as-grown STO sample rocking curves are 0.202^o and 0.197^o respectively.

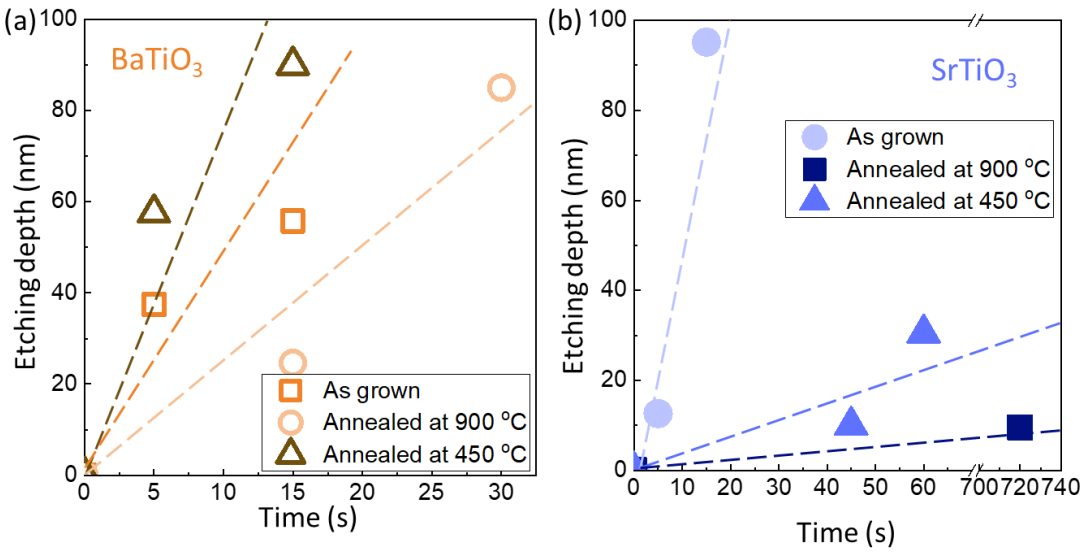


Figure 7-12: Etching rate of (a) BTO/STO and (b) STO samples with HF Dip 10:1.

Sample	Etching rate (nm/min)
As-grown BTO/STO	250
450 °C annealed BTO/STO	390
900 °C annealed BTO/STO	155
As-grown STO	357
450 °C annealed STO	24.24
900 °C annealed STO	0.78

Table [7.3]: Etching rate of different annealing condition thin film with HF Dip 10:1

The surface energy of a material, which is related to dangling bond density, is said to have effect on wet etching rate. According to the literature, the surface energy of a material can be determined by the surface dangling bond density. [118] In addition, the wet etching rate is directly proportional to the material's surface energy. [119] We believe that the different etching

rates between samples with different annealing conditions are due to the filling of oxygen vacancies. Oxygen vacancies in STO can create a bound state 0.7 eV below the conduction band edge to trap electron, and this trapped electron is considered as dangling bond in the sample. [120] [121] The oxygen vacancies in as-gown STO sample was filled by annealing and would reduce the dangling bond density in the sample, which explains the lowest etching rate for 900 ^{o}C annealed sample. Whereas as-grown STO sample has the largest amount of oxygen vacancies and leads to the highest etching rate.

The etching rate of the BTO/STO sample can be explained from the film dislocation and film crystallinity point of views. BTO/STO sample that was annealed at 900 ^{o}C for two hours has the lowest etching rate can be explained by the significant improvement of film crystallinity. We believe that as the film crystallinity improves, it is harder for etchant to break the bonding in the material which leads to a lower etching rate. The decreased in dislocations in annealed samples also have less dangling bond which leads to lower etching rate. As for BTO/STO sample that was annealed at 450 ^{o}C in oxygen rich environment, we suspect the sample has the most dislocation, which caused the sample to have the highest etching rate.

A few 156 nm thick BTO/STO microbridge devices with different pattern were fabricated with the fabrication process. Figure [7-13] (a) to (e) show the optical microscope pictures of the sample after each major part mentioned above. Figure [7-13] (a) shows the bridge device pattern of resist on BTO/STO sample. Figure [7-13] (b) shows image of the sample after HF etched, where the oxide film was patterned into the device shape. Next, figure [7-13] (c) shows that there was 200 nm silicon nitride deposited around the functional device as you can see that the color change from silver (silicon) to blue (silicon nitride), and the color of nitride followed the “silicon nitride on silicon” color code that was well established before. [122] Figure [7-13] (d) shows a

layer of 15 nm thick Ni pad, which is the shiny layer, deposited on the contact pad. Figure [7-13] (e) shows the final form of the working device, where the bridges were suspended completely.

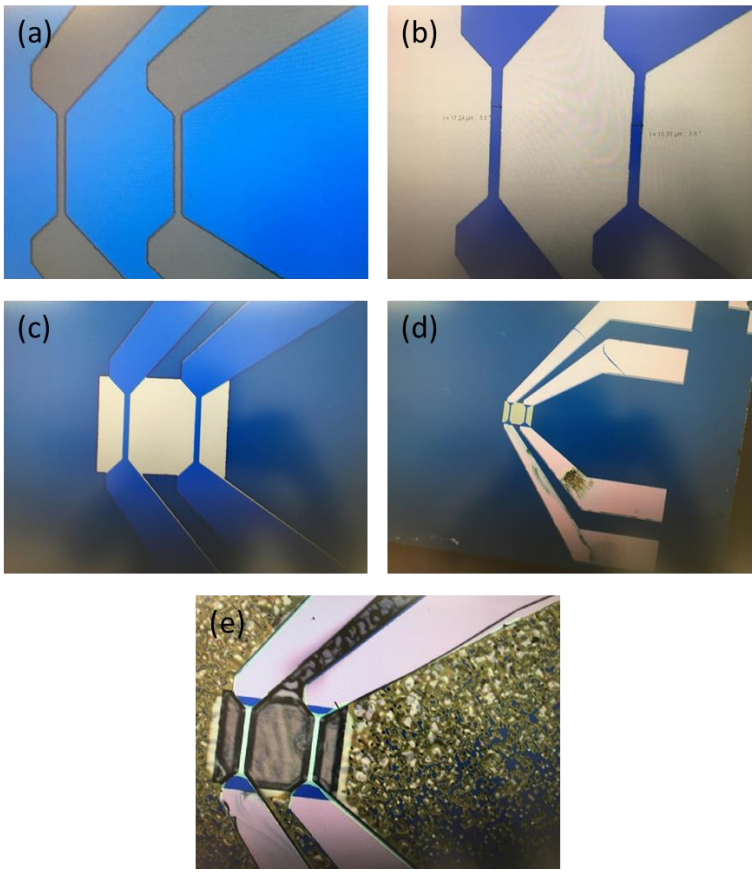


Figure 7-13: Optical image of the device after each major process. (a) Photoresist with the microbridge device pattern. (b) After HF etch, which the BTO/STO film was patterned into microbridge. (c) Si3N4 layer was deposited around a window for KOH etch. (d) 15 nm Ni was deposited as electrode. (e) After KOH etched, the bridge device was suspended.

Bridge devices with different pattern were fabricated with the 156 nm BTO/STO sample. Figure [7-14] (a) shows the optical image of the device, and figure [7-14] (b) to (d) show the SEM images of the devices. Figure [7-14] (b) to (d) also further confirm the bridges were fully suspended. In addition, figure [7-14] (c) and (d) show the edge of the bridges curved upward. We suspect the curving could be due to thermal strain from pre-annealed of the sample before processing.

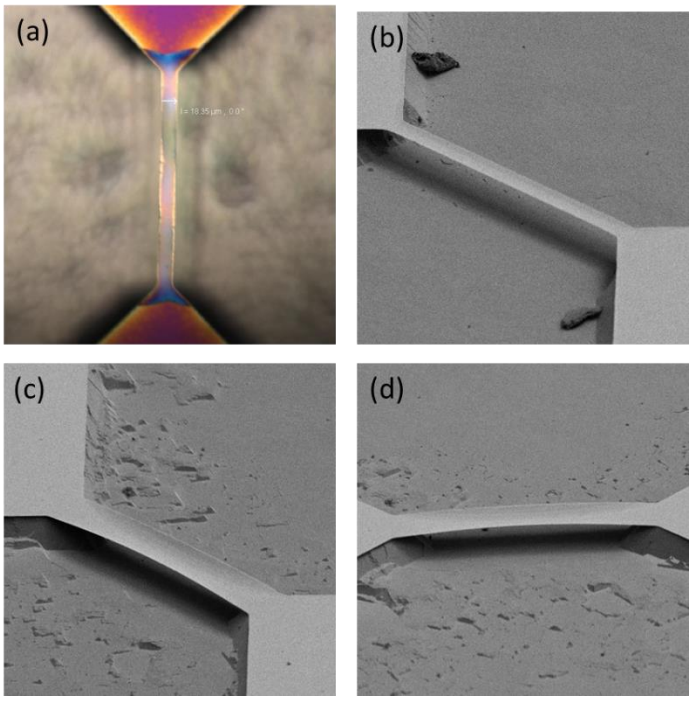


Figure 7-14: (a) Optical image of a BTO microbridge fabricated for XRD measurement. (b), (c) and (d) show the SEM images of the bridges on the same sample, which further confirm that our bridges were suspended. The edge of the bridges was curve as seen in (c) and (d).

Another bridge device as STEM imaging platform was fabricated on a sample that was back side milled by Allied Inc. and the images are shown in figure [7-15]. The part of the film that is on top of silicon appears to have darker blue color while the suspended part looks more transparent. In addition, a black window can be seen clearly underneath the bridge in figure [7-15] (a), which also confirm that the bridge device was suspended on top of a thru hole.

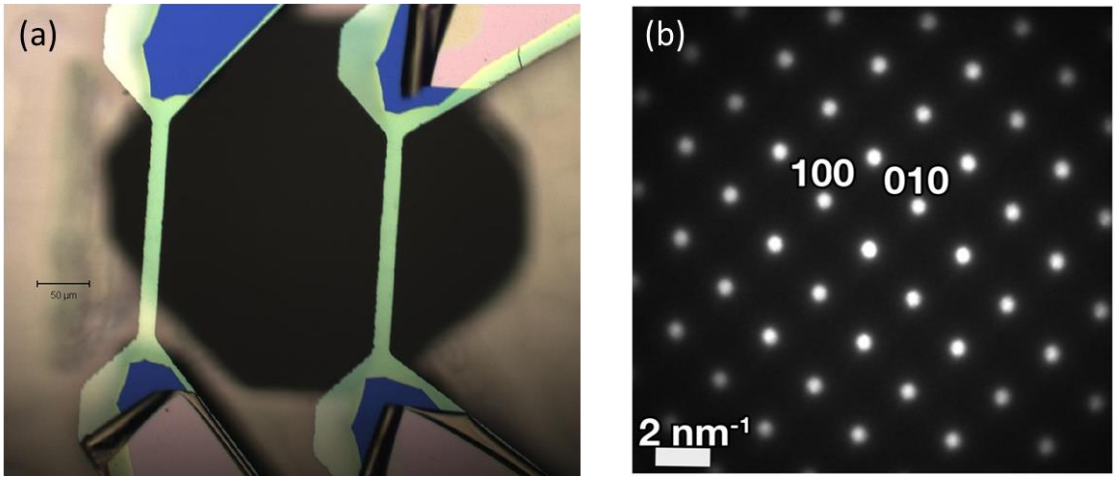


Figure 7-15: (a) Optical image of BTO microbridge on top of a thru hole. (b) Diffraction pattern of the microbridge shows crystallinity of the microbridge.

The successful device for STEM imaging was sent to Dr. LeBeau's group at North Carolina State University, which they have successfully taken diffraction pattern image of the crystal structure of the bridge as shown in figure [7-15] (b). From this figure, we could confirm that the bridge still maintains its single crystal quality after all processing steps, which is extremely important in order to create an epitaxial complex oxide device. However, due to the required pre-annealed in the sample preparation steps, the BTO/STO film is too rough to be able to do STEM measurement in the atomic level.

7-11: Discussion

In this experiment, there are still two problems that need to be resolved. First, to get a bridge device that has a smoother surface for atomic STEM imaging. Second, to prevent the Si_3N_4 and Ni to peel off from the sample during KOH etching.

In order to get a bridge device with a smoother surface, a different sample, such as STO, can be used to fabricate the device. The thickness of the film can be reduced to obtain a smoother film, and the sample can be pre-annealed at a slightly lower temperature.

A different annealing procedure can be utilized to prevent Si_3N_4 peels off from the sample during KOH etching. Sample can be annealed after the HF etch instead of before. Then, the Si_3N_4 will be deposited on SiO_2 layer that is formed from annealing, which is believed to have better adhesion. We also suspect that fluorine and hydrogen ion residuals from HF etch can affect the quality of Si_3N_4 layer, which annealing the sample after HF etch can get rid of the residuals. Instead of using Ni as the electrode, a softer metal, such as gold, can be used for electrode, which we believe gold electrode can stick to the sample better.

7-12: Conclusion

In conclusion, the experiment had demonstrated that HF Dip 10:1 can be used as acid etchant for BTO/STO and STO film. Our STO etching rate is comparable to other reported bulk STO etching rate at around 60 nm/min. [123] We have concluded that both complex oxide STO and BTO/STO with different annealing conditions can have different etching rates. We believe the difference in STO etching rate is due to the oxygen vacancies in the material, which correlate to sample's dangling bond densities and etching rate. Moreover, film crystallinity, and dislocations also play a vital role in etching BTO/STO due to the different bond strength and grain boundary dislocations.

Complex oxide microbridges with or without thru hole were also successfully fabricated with the newly developed recipe. This recipe includes the conventional photolithography, sputtering and wet etching technique. With this recipe and wet etching of complex oxides, we

could potentially introduce complex oxide materials to the MEMS technology. This can lead to a positive impact for future sensing technologies, taking advantages of the good piezoelectric properties of complex oxides. The crystallinity of the microbridge was confirmed with diffraction pattern taken by Dr. J. M. LeBeau. Nonetheless, some future work on getting a smoother surface bridge device is necessary as a new platform for STEM imaging in the atomic level. We believe that this developed process will lays down a new platform for STEM measurement, in which a lateral electric field can be applied across the sample.

Fabrication recipe

1. Dice wafer into 4 mm × 5.8 mm along the [100] direction, i.e. 45^{o} from the major flat.
2. 4-steps clean sample with ultrasonic sample in DI water for 15 minutes, then in Acetone, Methanol, and Isopropanol for 10 minutes each.
3. Pre-anneal sample at 900 ^{o}C for 2 hours. Take 4 hours to ramp up from room temperature to 900 ^{o}C and then stay at 900 ^{o}C for 2 hours. Once that is done, cool down automatically to room temperature. (annealing condition can be different for different film and thickness.)
4. 4-steps clean sample again with ultrasonic sample in DI water for 15 minutes, then in Acetone, Methanol, and Isopropanol for 10 minutes each.
5. The sample was then sent to Allied Inc. to mill a back-side window if needed.
6. 3-steps clean sample with ultrasonic sample in Acetone, Methanol, and Isopropanol for 10 minutes each. (This step is only needed if the sample was sent to Allied Inc.)
7. Mount sample on a piece of carrier wafer with a drop of photoresist and bake at 120 ^{o}C for 10 minutes.
8. Next, set the spinner recipe for spreading at 500 RPM for 5 seconds, then spinning at 4000 RPM for 60 seconds.

9. Do a pre-bake at 115 ^{o}C for 1 minute.
10. Expose sample with the correct mask pattern for 11 seconds.
11. Do a post exposure bake at 110 ^{o}C for 1 minute.
12. Next, develop the sample with MF-319 developer for 1 minutes 30 seconds to 2 minutes depending on the feature size.
13. Check the sample under optical microscope to make sure the feature size and pattern is good.
14. Etch sample with HF Dip 10:1 for around 2 minutes depending on the film thickness.
15. If the sample is etched completely, you should be able to see that the exposed Si becomes hydrophobic.
16. Wash away the photoresist and remove the sample from carrier wafer by doing 3-steps clean mentioned above.
17. Next, repeat all the photoresist patterning steps again for the Si_3N_4 deposition.
18. Follow step 7 to 13 for resist patterning. Use clear field mask #3 for exposure.
19. Bake sample at 100 ^{o}C for 1 minute, and then deposit 200 nm (240 minutes with pre-heat at 70 ^{o}C for 10 minutes) Si_3N_4 with AJA-sputter system.
20. Wash away the photoresist and remove the sample from carrier wafer by doing 3-steps clean.
21. Then, repeat all the photoresist patterning steps again for the Ni deposition.
22. Follow step 7 to 13 for resist patterning. Use dark field mask #2 for exposure.
23. Move the sample into AJA E-beam evaporator chamber and deposit 15 nm of Ni.
24. Soak the sample in Acetone for 15 minutes, then ultrasonic for 1 to 2 minutes to lift off excessive Ni and remove the sample from the carrier wafer, then rinse with IPA.
25. Next, prepare a 30% KOH by mixing 69.4g of KOH pallets into 200 mL solution.
26. Heat up hot plate to 203 ^{o}C and set the magnetic stir rotation to 120 RPM.

27. Set up the thermometer, beaker filled with KOH solution and etching basket.
28. Once the solution temperature measured to be about 75 ^{o}C, clamp the sample corner with locking twizzer. Put the sample into the Teflon etching basket in the KOH bath, and etch for 20 to 25 minutes depending on the bridge width or required etching depth. The sample needs to be positioned vertically.
29. When the KOH etching is done, remove the etched sample from KOH solution and put it in a shallow glass container that is filled with IPA. Then, check the sample under an optical microscope to make sure the bridge is fully suspended. (Skip this step if fabricating STEM imaging platform.)
30. After confirming the bridge survives, take the sample with IPA to supercritical dryer to dry the sample. Do not blow dry the sample as the stiction force between the substrate and bridge will break the bridge.

Chapter 8 : Conclusion

In this dissertation, I have addressed each of the issues mentioned in the introduction separately. Even though conventional semiconductor is widely employed in energy harvesting, sensing, and computing technologies, but the advancement in these technologies have reached a plateau due to some of the limitations of conventional semiconductors. Semiconductors use in photoelectrochemical (PEC) cell for energy harvesting will corrode since they are unstable in aqueous. Therefore, hybrid heterojunctions of complex oxides and semiconductors can be utilized in PEC cell due to their efficiency in generating electron-hole pairs and thermodynamically stable in aqueous condition. Complex oxides have their electrical properties strongly couple to mechanical properties, which can be introduced to the sensing industry. By taking advantages of complex oxides' interesting properties, such as piezoelectricity, ferroelectricity, and metal-insulator transition, complex oxides can potentially enhance present sensing technology. Moreover, in the metal-oxide-semiconductor (MOS) technology, Si has lower electron and hole mobilities as compare to Ge, which causes MOS technology to switch from Si-based to Ge-based. Complex oxides that have high dielectric constant can be employed as gate dielectrics for Ge-based MOS devices. In my research, I have shown how complex oxide can help advancing current energy harvesting, sensing, and computing technologies beyond the use of conventional semiconductor. The advancement in oxide MBE growth has allowed the complex oxide to couple electrically with semiconductor, which enable my research on functionalizing complex oxide for future technologies.

First, heterostructure of $SrZrO_3$ (SZO) grown epitaxially on Ge substrate was studied. The XPS measurement has shown a type I band alignment for SZO with respect to Ge. In addition, the conduction and valence band offset are large enough to use as dielectric material.

Electrical characterization with capacitance-voltage and current-voltage measurement on 4 nm SZO thin film has shown high dielectric constant and low leakage current. Therefore, SZO can be a potential candidate of gate dielectric material for Ge-based MOS technology.

In the next chapter, charge transfer and built-in electric fields between $SrNb_xTi_{1-x}O_3$/ Si heterojunctions were studied. Hole gas was found to exist at the heterojunctions interface utilizing transport measurement. Depth resolved hard x-ray photoelectron spectroscopy analysis has reveal that asymmetries and multiple valences in core level spectra are due to the presence of built-in electric fields across the interface. Charge transfer and built-in fields were able to tune via controlling carrier concentration in the heterojunctions. Thus, the ability to tune built-in electric fields across oxide-semiconductor heterojunctions can be useful for future energy harvesting technology.

At last, HF Dip 10:1 was found to be able to etch both $BaTiO_3$ and $SrTiO_3$ film. The etching rate was determined for film with different post-annealing conditions. The etching rates were found to be related to the oxygen vacancies, crystallinity and dislocations of the film. The wet etching of $BaTiO_3$ and $SrTiO_3$ has also enabled the development of fabrication recipe for complex oxide. A few 156 nm thick $BaTiO_3$ microbridges were fabricated utilizing conventional integrated circuit fabrication techniques and the newly developed recipe. Diffraction pattern of the oxide microbridge shows that the oxide microbridge preserves its crystallinity after processing. Therefore, the wet etching and fabrication of crystalline oxide devices will lay down groundwork for functionalize complex oxides in Microelectromechanical Systems. Moreover, this newly developed recipe was also utilized to fabricate a platform for STEM imaging in the atomic level, in which in plane electric fields can be applied across the sample.

In conclusion, my research has addressed the issues that were brought up in the introduction. Even though more future works are needed in order to utilize complex oxide for future applications, but it is hoped that the results of my research have laid down the groundwork in functionalizing crystalline complex oxides.

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