STUDY OF NEW TRANSISTOR ARCHITECTURE WITH ENERGY FILTERING

by

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THESIS

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ABSTRACT

STUDY OF NEW TRANSISTOR ARCHITECTURE WITH ENERGY FILTERING

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The thermodynamic limit of the subthreshold slope to 60mV/decade at 300K forces MOSFET devices to use high supply voltages (> 0.5V) and therefore dissipate a lot of energy. This physical limitation of transistors is a direct consequence of thermal excitation of electrons. This study investigates a new transistor architecture capable of suppressing thermally excited electrons using a quantum well as an energy filter. The energy filter consists of a 2nm SiO_2 tunneling barrier and a 2nm Quantum Well (QW) layer of Cr_2O_3 sandwiched between Ni electrodes and a channel of Si. Transistors having this QW energy filter have been fabricated using CMOS-compatible processes and materials. Their IV characteristics have been compared with control samples without tunneling barriers and QW layers to investigate suppression of thermally excited electrons. The three device configurations fabricated and studied include: sample with no tunneling barrier and no QW layer, sample with tunneling barrier only and sample with both tunneling barrier and QW layer. Gate modulation was observed in all three device configurations, demonstrating successful fabrication of transistors. These gate modulations, however, were observed only at large drain voltage (> 2V), indicating an efficient gate coupling was not established, which would obscure the energy filtering

effect that might have been present. A future study may focus on establishing an efficient gate coupling.

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Chapter 1: Introduction

1.1 Background

A critical component of electronic devices is the transistor. The past four decades have heralded tremendous improvement in the packing densities of transistors. This has been realized while keeping power consumption per unit area just about the same, following the scaling law[1-3]. However, at this point the scaling is no longer sustainable because further scaling of the supply voltage causes excessive power consumption per area.

The inability of further voltage scaling is because at 300K, the subthreshold slope of MOSFETs is fundamentally limited to 60mV/decade (Figure 1). Since subthreshold slope is fixed at room temperature, any reduction in supply voltage (V_{dd}), represented by shifting the red plot to the left, would lead to an increase in OFF-state current (Figure 1 – green plot).

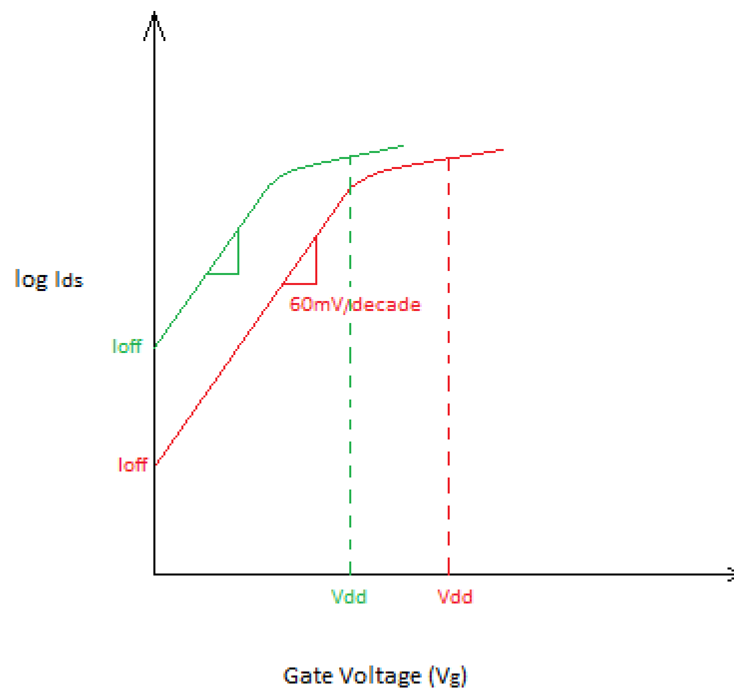

Figure 1: Subthreshold swing at 300K highlighting challenge with continuous scaling of supply voltage (Vdd)

Fundamentally, transistors are on-off switches made up of three primary components – source, drain and gate electrodes. An electron flow path is created as electrons flow from the source to the drain electrode. The gate electrode regulates this electron transfer. Under conditions of no gate bias, the conduction band of the silicon channel provides an energy barrier which prevents electron flow from the source to the drain electrode. However, at room temperature this blocking of electrons by the energy barrier is not perfect because electrons from the source experience thermal excitation and some of these electrons, having sufficient energy, overcome the energy barrier. This results in OFF-state leakage current. This OFF-state current leads to undesirable OFF-state power dissipation as shown in Figure 1.

Several approaches have been investigated to address this undesirable electron thermal excitation. One of the most widely studied architectures is the tunneling filed-effect transistor (TFET), which takes advantage of band-to-band tunneling to minimize Fermi-Dirac thermal excitation. TFETs generally consist of a p-type doped source electrode and an-type doped drain electrode. This architecture exploits band to band tunneling from the valence band of the p-type source to the conduction band of the n-type drain thereby limiting the contribution of Fermi-Dirac thermal excitation[4]. Various TFET architectures with different configurations have been investigated, including vertical structure[5-8], sidewall gating[9-12], planar structure[13-19] and nanowires[20-22]. Additionally, numerous material systems have also been studied, including, InAs-Si[23-26], InAs/GaSb-Si[27,28], AlGaSb-InAs[28,29] and 2D semiconductors (such as $MoTe_2$[30-32], WSe_2[33-35] and MoS_2[36-38]). Other TFET heterostructures investigated include stacked $WSe_2/SnSe_2$[35,39,40], p-channel GaN[41], junctionless $InAs/GaAs_{0.1}Sb_{0.9}$[42,43]. Typically, TFETs comprise of two or more semiconductors of varying band gaps, this makes it difficult to integrate them with Si-based

technology. In addition, TFETs tend to be ambipolar, thereby limiting their superiority in terms of carrier tuning or control[44,45]. Other transistor approaches to address Fermi-Dirac thermal excitation of electrons include impact-ionization[46-49] and dielectric gating of ferroelectrics[50-52].

Under normal operation and in accordance with the scaling rule, exponential reduction in transistor dimensions is accompanied by lowering of transistor supply voltage[1-3]. However, attempts at reducing transistor supply voltage (V_{dd}) without increasing OFF state current (I_{OFF}) would require a steeper subthreshold slope (lower subthreshold swing value), as represented in Figure 2. This is because the alternative approach shown in Figure 1 would lead to higher OFF-state current when supply voltage is lowered. But this has not been realized since the subthreshold slope is limited to 60mV/decade at 300K by thermally excited electrons[53-59]. Electrons experience excitation when transistors operate at room temperature in accordance with the Fermi-Dirac distribution. This is represented in Figure 3 as thermally excited electrons possessing sufficient energy overcome the energy barrier thereby generating OFF-state current when the device should be in a non-conductive state ($V_g < V_t$).

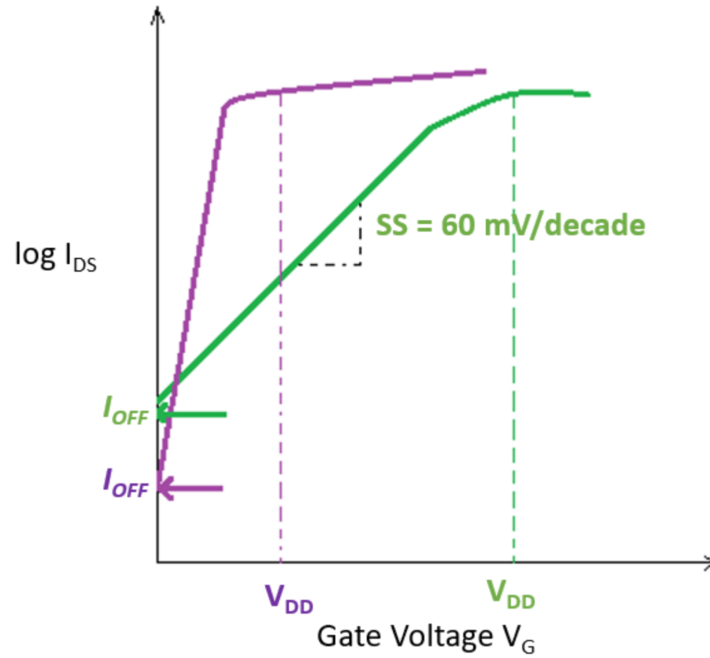

Figure 2: Subthreshold swing (green) limit at 300K. Lilac IV shows desired slope to reduce Vdd and Off-state current

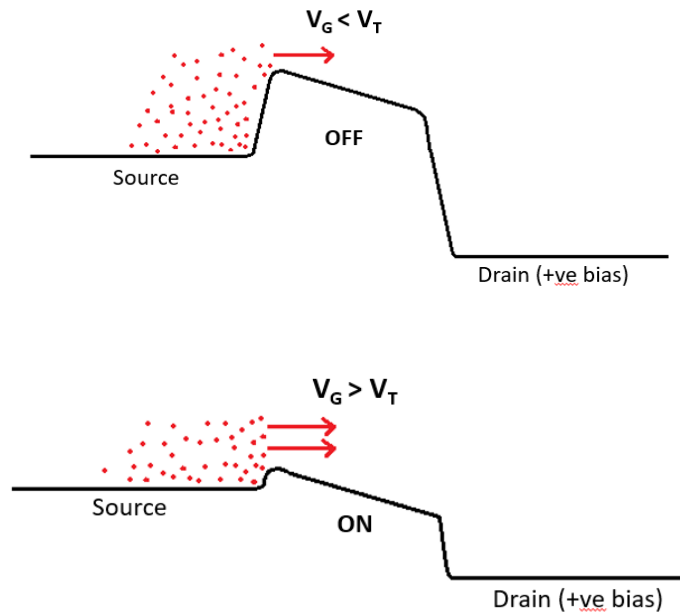

Figure 3: Conduction band energy diagrams for simplified MOSFET

1.2 Electron cooling mechanism

The inherent thermodynamic limitation of thermally excited electrons (at room temperature) leading to a gradual subthreshold slope and consequently a higher supply voltage in transistors is an issue that must be overcome in order to realize more efficient transistors[60-64].

It has been shown that it is possible to suppress thermally excited electrons without external cryogenic conditions or external cooling. This was done by using a discrete quantum state to filter thermally excited electrons, hence only cooled electrons contribute to transistor operation[65]. The device configuration is as shown in Figure 4. Source and drain electrodes are separated by an insulating layer of 2nm tunneling barrier SiO_2. A thin 2nm Cr_2O_3 layer serves as the quantum well energy filter while the quantum dot provides a pathway for electron transport. The quantum dot is situated accurately between the source and drain electrodes without having any direct contact with either electrodes: it is separated from the electrodes by both the tunneling barrier and the quantum well layer. Under operation at room temperature, thermally excited electrons assume energies higher than the fermi level of the source electrode[66,67]. With the quantum well structure tuned in such a way that the separation between its discrete energy levels exceeds 250 meV, ten times larger than the room temperature thermal energy of 25 meV[65]. Thermally excited electrons tunnel through the energy barrier and occupy the only available discrete energy level in the quantum well. With the very large spacing between quantum well energy levels (~250meV), electrons remain confined assuming an effective temperature of 0K since no nearby higher energy state exists in the quantum well. When the quantized energy level of the quantum dot aligns with the discrete energy level of the quantum well, electrons tunnel through the barrier to the quantum dot thereby

generating a source-drain current. This device configuration using a quantum dot and quantum well was earlier investigated by our group as a means to suppress thermally excited electrons[65].

This research builds on this underlying mechanism of electron transport while using a CMOS-compatible device architecture.

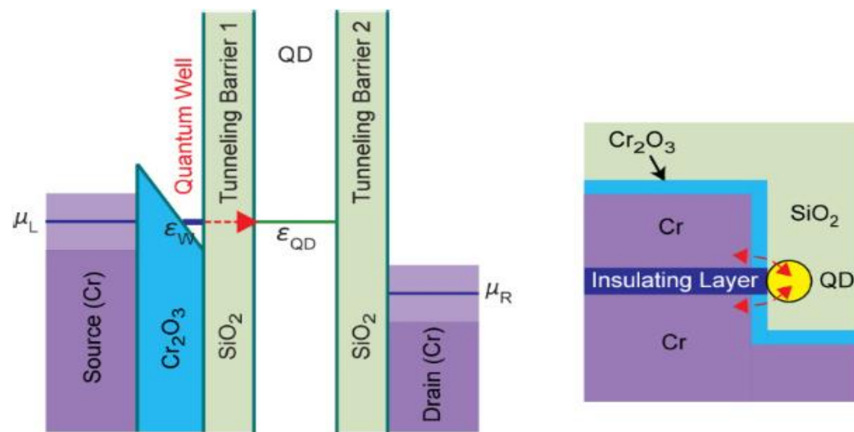

Figure 4: Double barrier Tunnel Junction structure and energy band diagram[65]

Chapter 2: Device Concept and Structure

The device architecture is shown in Figure 5. Fabrication was done on a p-type silicon wafer, with light n-type phosphorus doping. Doping was done to raise silicon fermi level close to the conduction band. The 2nm SiO_2 layer serves as the tunneling barrier which is necessary to help in the formation of the triangular quantum well of the 2nm Cr_2O_3 layer.

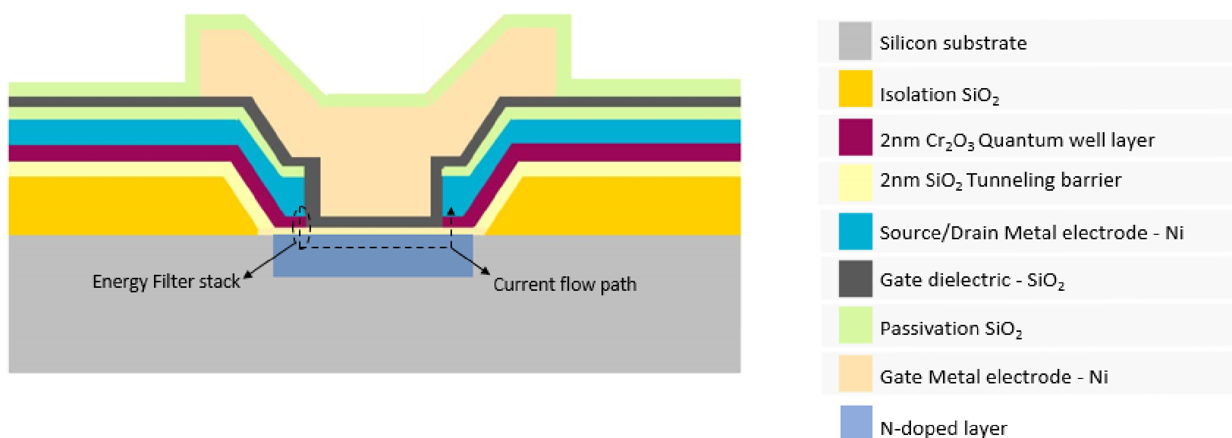

Figure 5: Cold Electron Transistor (CET) device schematic

The energy band diagrams in Figure 6 show the mechanism for electron transfer of the device. As thermally excited electrons overcome the energy barrier, they enter the quantum well structure and are forced to occupy the closest discrete energy level. This electron confinement means that no excitation path exists for these electrons, hence the effective temperature of the electrons is 0K. When no bias is applied to the device, the fermi level of the source electrode aligns with silicon fermi level. Application of a positive bias to the drain electrode lowers the drain fermi level such that it pulls the silicon energy bands downwards along with it. When a positive bias is simultaneously applied to the gate, the silicon energy bands are lowered even further. This leads

to a thinner energy barrier between the source and silicon conduction band. Hence, the energy filtered cold electrons can tunnel through to the silicon conduction band and further on to the drain electrode, producing source-drain current.

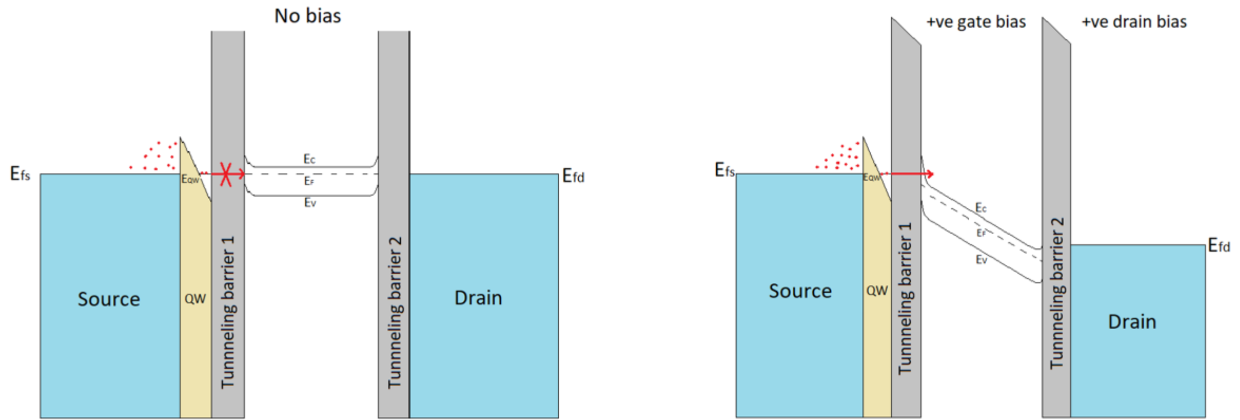

Figure 6: Energy band diagram illustrating CET principle of operation

Chapter 3: Experimental Procedure

3.1 Device Fabrication Overview

The fabrication process for barrier-free, double barrier tunnel junction and cold-electron double barrier tunnel junction devices are provided in this chapter.

A 4-inch silicon wafer serves as the substrate subsequently subjected to several processing steps of photolithography, thermal oxidation, physical vapor deposition (PVD), chemical vapor deposition (CVD), Reactive Ion Etching (RIE), wet chemical etching and several others prior to electrical characterization of final devices. This work is done in the class 100 cleanroom facility of the NanoFabrication Research Center at the University of Texas at Arlington. A detailed description of these processes is presented in this chapter.

3.2 Initial Mask Design Process Flow

3.2.1 Substrate Cleaning

Bare test grade n-type 4-inch wafers are stripped of native SiO_2 using HF (10:1) and cleaned of organic impurities with Piranha solution prior to deposition. HF (10:1) strip is carried out for 5 minutes, after which wafers are thoroughly rinsed under running deionized water and two baths of deionized water. Piranha solution is prepared using H_2SO_4 and H_2O_2 in a ratio 3:1 (60mL:20mL). Following 30 minutes of immersion in Piranha solution, the wafer is then thoroughly rinsed under running deionized water as well as in two baths of deionized water.

3.2.2 Isolation Oxide Growth – E-Beam SiO2 deposition

450nm SiO_2 was required for the device fabrication to serve as a protective pillar for the gate contact area. However, the initial deposition of the dielectric layer covers the entirety of the substrate. Subsequent processing steps were used to define the pillar dimensions as desired for the device geometry.

The deposition of this layer of silicon dioxide was done in an electron beam (e-beam) evaporator (CHA Inc.) by means of physical vapor deposition.

The samples were first placed in the deposition chamber. After vacuum conditions reached $< 1\times10^{-6}$ Torr, SIO_2 was deposited onto the silicon wafer at a rate of ˜ 1.0 Å/*s* and a deposition current of ˜ 3.8 *mA* for a total thickness of ˜ 450 *nm* by means of an electron beam. After the deposition is completed, the samples were unloaded from the deposition chamber and the thickness of the films were confirmed by taking measurements on the Gaertner Ellipsometer and the Ocean Optics Reflectometer.

3.2.3 First Photolithography and Development

The purpose of this first step of photolithography is to define the Si islands which would serve as the separation between source and drain contact pads for the array of devices.

Cleaned wafers were spin coated with negative photoresist NR9-1000PY on a Headway Rearch PWM32 Coater according to the following recipe:

500 rpm, 100 rpm/s, 5 s

3000 rpm, 1000 rpm/s, 60 s

0 rpm, 1000 rpm, 0.1 s

This was followed by pre-exposure bake on a Cole Palmer Hotplate at 150°C for 60 seconds. The sample was then loaded onto the substrate holder of the OAI Backside Aligner. The photomask was also loaded onto the mask plate of the Aligner. The substrate was then aligned with region of the photomask bearing the first mask lithography pattern by means of the x-y micrometer control knobs and the rotation micrometer control knob. Once this alignment was completed, the substrate

chuck current was set to 14 mA and then carefully raised by turning the chuck height dial clockwise until contact is established between the wafer substrate and the photomask. Contact was confirmed by observing the features on the photomask and the sample on the OAI Aligner LCD monitor screen. A 365 nm primary wavelength UV light generated by a mercury vapor lamp was then used for exposure. The exposure dose was 120 mJ/cm^2 . After exposure, the sample was unloaded and subjected to post exposure bake on a hot plate at 100°C for 60 seconds. Once baking is completed, the sample is allowed to cool down on a cool-down plate for about 30 seconds. Next, the sample is developed in a solution of RD6 photoresist developer for 10 seconds with gentle agitation of the developer bath. After development, the sample is rinsed with copious amounts of deionized water for a total duration of 10 mins. Fresh deionized water is used for the rinsing process after 2.5 minutes. Once rinsing is completed, the sample is blown dry with nitrogen.

3.2.4 Five Layer Hard Mask Metal Deposition and Lift-off

Given that first photolithography first defined a pattern of island trenches, this step deposits a hard metal mask across the entire sample. However, after lift-off, the hard metal mask would only persist in the island regions on the substrate.

Earlier device fabrication showed that having one hard mask metal layer resulted in pitting of the metal layer after hydrofluoric acid wet etch steps. Therefore, we resorted to using five alternating layers of chromium and gold as the hard mask.

The hard metal mask was deposited by physical vapor deposition using an electron beam evaporator (CHA Solution).

The samples were loaded into the deposition chamber on a substrate holder with the samples held in place by metal clamps. The substrate holder is set up in the tool such that the

samples face downwards while the source material is held in a crucible facing upwards. A deposition recipe as described below is created for the

process:

Layer 1 (Cr)

Deposition rate: 0.05 nm/s

Layer thickness: 5 nm

Layer 2 (Au)

Deposition rate: 0.05 nm/s

Layer thickness: 20 nm

Layer 3 (Cr)

Deposition rate: 0.05 nm/s

Layer thickness: 5 nm

Layer 4 (Au)

Deposition rate: 0.05 nm/s

Layer thickness: 20 nm

Layer 5 (Cr)

Deposition rate: 0.05 nm/s

Layer thickness: 5 nm

Once vacuum setpoints are reached the automatic process is started. At the conclusion of deposition, the samples and source material crucibles are unloaded from the deposition chamber. The samples are then stored for subsequent processing.

The lift-off process then follows as described below:

- Hold sample upside down with tweezer, immerse it in a solution of acetone and stay still for 60 seconds
- Transfer the sample, while still holding upside down, to a fresh beaker of acetone solution and shake vigorously for 120 seconds
- Transfer the sample into a fresh beaker of acetone solution, right side up
- Place the beaker of acetone solution in an ultrasonicator and sonicate for 15 minutes
- Take the sample out of the acetone solution and gently rinse with a squeeze bottle of isopropanol
- Place the sample in a beaker containing freshly prepared isopropanol solution
- Carry out isopropanol sonication of the sample for 15 minutes
- Gently blow the sample dry using nitrogen

3.2.5 Silicon Dioxide Dry etching

With the hard mask in place on the island region defined by the preceding steps, pillars of silicon dioxide capped with the hard mask are formed by dry etching. This is done using a Reactive Ion Etcher (Technics Macro RIE 8800). The
reactive ion etching was carried out in two steps. The first step was responsible for actual etching of silicon dioxide whereas the second step was aimed at getting rid of fluoride complexes and other derivative contaminants from the first etch
step. The recipe for this process was as follows:

Reactive Ion Etching Recipe (Technics Macro RIE 8800)

Step 1

Power: 600 W

Pressure: 160 mTorr

CF_4 : 30 sccm

O_2 : 3.6 sccm

Time: 215 s

Step 2

Power: 350 W

Pressure: 200 mTorr

O_2 : 11 sccm

Time: 270 s

At the conclusion of the etch process, the samples were unloaded from the etch chamber and the extent of dry etching was confirmed using a profilometer (KLA Tencor P6).

3.2.6 Silicon Dioxide Lateral Wet etching

Lateral etching of the silicon dioxide pillar was necessary to define the contact area for the source and drain contact terminals. Wet etching was done using hydrofluoric acid (50:1) for 55 seconds based on previously established etch rates from experiments carried out on dummy samples of the same silicon dioxide film.

3.2.7 Isolation Silicon Dioxide Deposition

With the laterally etched silicon dioxide pillar still in place, a thin film of silicon dioxide was deposited by physical vapor deposition. This film of dielectric was deposited to serve as an isolation layer for the source and drain of the devices. Deposition was carried out on an electron beam evaporator (CHA Inc.) according to the following deposition parameters:

Deposition temperature: Room temperature

Deposition rate: 0.06 nm/s

Chamber pressure: 3.4×10^{-6} Torr

Deposition current: 4.8 mA

Nominal deposition thickness: 30 nm

A control sample was loaded with actual samples for the deposition process. These control samples were measured after the deposition on the Gaertner
Ellipsometer; measured thickness was 33 nm.

3.2.8 Planarization Photoresist Coating

Planarization photoresist is a unique photoresist which is maintains its properties when exposed to high energy radiation (such as UV light). It can also serve as a sacrificial/protective layer for wet and dry etch processes.

It was desired that the hard mask as well as the ˜ 30 *nm* silicon dioxide on the hard mask be etched. So, the sample was coated with planarization photoresist (PC3-700) according to the following spin coating recipe on a Headway Rearch Coater:

Film Properties (Spin Coating)

Step 1:

Speed – 800 rpm

Ramp – 100 rpm/s Time – 80 s **Step 2:**

Speed – 0 rpm

Ramp – 100 rpm/s

Time – 0.1 s

Nominal thickness: 1500 – 1700 nm

After spin coating, post-coat bake was carried out on a Cole Palmer Hot Plate at 200°C for 120 seconds.

3.2.9 Planarization Photoresist Etchback

To expose the top of the silicon dioxide pillar, some of the planarization photoresist (PC3-700) had to be etched. Dry etching by reactive ion etching mechanism was preferred for this step. This etch was done on a Technics Macro RIE 8800 according to the following recipe:

Power: 350 W

Pressure: 200 mTorr

O_2 : 11 sccm

Time: 1050 s

Etching was done based on already established etch rate for this photoresist under this reactive ion etching conditions. These experiments are detailed later in this chapter.

Exposure of the top of the silicon dioxide/hard metal mask pillar was confirmed by measurements on a profilometer (KLA Tencor P6).

3.2.10 Silicon Dioxide and Hard Mask etching

The hard metal mask and ˜ 30 *nm* silicon dioxide were etched by wet etching. Beakers of hydrochloric acid (HCl), hydrofluoric acid (HF), chromium etchant and gold etchant were prepared. Etching was carried out on samples according to the following procedure with thorough rinsing in deionized water between each etch step:

HF (50:1) – 5 s

HCl – 5 s

Cr etchant – 10 s

Au etchant – 30 s

HCl – 5 s

Cr etchant – 10 s

Au etchant – 30 s

HCl – 5 s

Cr etchant – 10s

The final etch step was followed by thorough rinsing in deionized water and gently blow drying with nitrogen.

3.2.11 Planarization Photoresist Removal, Sample Cleaning and degassing

This step was aimed at completely taking off planarization photoresist from the surface of the sample. This cleaning step is also crucial to ensure that the surface of the sample is pristine to eliminate the risk of impurity-induced device failure.

First, beakers of acetone solution are prepared for the cleaning process and the sample is initially clean using a squeeze bottle of acetone. This is followed by placing the sample in the already prepared solution of acetone and subjecting the acetone solution containing the sample to

ultrasonication for 15 minutes. After acetone ultrasonication, the sample is carefully blown dry with nitrogen. Then the

sample is placed loaded onto a UV/Ozone cleaner for 15 minutes. Two more alternating cleaning cycles of acetone sonication and UV/Ozone cleaning follow this initial cycle. Next, the sample is rinsed with a squeeze bottle of isopropanol after which two cycles of isopropanol ultrasonication follow. Once isopropanol ultrasonication is complete. At the conclusion of the cleaning cycles, the sample is loaded onto AJA Sputter for degassing. The degassing process is essentially aimed at removing trapped solvents in the samples. The procedure for degassing is as presented below:

- Samples are held onto AJA Sputter substrate holder using metal clips
- Load lock chamber is vented to atmospheric pressure by opening the nitrogen vent valve
- Substrate holder is placed on transfer arm in load lock chamber
- Load lock chamber is closed
- Gate valve separating main chamber from load lock chamber is opened
- Transfer arm bearing substrate holder is moved from load lock chamber into the main chamber
- Tool spindle system is used to pick substrate holder off transfer arm spatula
- Spindle system now holding substrate holder is adjusted to the safe transfer height

- Transfer arm is retracted from main chamber to load lock chamber
- Gate valve separating load lock chamber from main chamber is closed
- Spindle rotation is turned on and rotation is set to 50 rotations per minute
- Substrate heater is turned on
- Heater temperature is increased from 15°C to 50°C
- Once at 50°C, substrate heater temperature is increased to 200°C in steps of 50°C
- The degassing process at 200°C lasts for 2 hours after which the substrate heater is turned off
- After one and a half hours, the chamber cools down to room temperature
- Spindle rotation is set to 0 rotations per minute and then turned off
- Spindle-substrate holder system is raised to safe transfer height
- Load lock-main chamber gate valve is opened
- Transfer arm is moved into main chamber from load lock chamber
- Substrate is lowered onto transfer arm spatula and unhinged
- Transfer arm bearing substrate holder is retracted from main chamber to the load lock chamber
- Gate valve is closed

- Load lock pump is turned off and nitrogen vent valve is opened
- Substrate holder is removed from load lock chamber
- Samples are unclamped from substrate holder

3.2.12 Second Mask (Source and Drain) Photolithography and Development

This alignment step defines the source and drain terminals of the devices. The process overlays the second pattern on the photomask with the previously defined pattern arising from the first photolithography process.

The samples were spin coated with a negative photoresist (NR9-1000PY) on a Headway Rearch PWM32 Coater with the following recipe:

Step 1

Speed – 500 rpm

Ramp – 100 rpm/s

Time – 5 s

Step 2

Speed – 3000 rpm

Ramp – 1000 rpm/s

Time – 60 s

Step 3

Speed – 0 rpm

Ramp – 1000 rpm/s

Time – 0.1 s

Spin coating was followed by pre-exposure bake on a Cole Palmer Hotplate at 150°C for 60 seconds. The sample was then loaded onto substrate holder of the OAI Backside Aligner. Then the photomask was loaded onto the mask plate and held in place by screws. Using the x-y micrometer control knobs, the substrate was aligned with the second mask pattern on the photomask (source-drain contact). Once the alignment is done, the substrate chuck current was set to 14 mA and a rotationary dial for controlling the substrate chuck movement is used to raise the substrate chuck until contact is established between the sample and the photomask. This is followed by UV exposure made possible by a mercury vapor lamp. The dose for the exposure was 120 mJ/cm^2 . Once exposure was completed, the photomask was unloaded from the mask plate and the sample was baked at 100°C for 60 seconds on a Cole Palmer Hotplate. After post-exposure bake, the sample can cool down on a cool-down plate before the next step. Development of the sample in a solution of RD6 photoresist developer follows. This process lasts for 10 seconds accompanied with gentle agitation of the developer solution throughout the process. At the conclusion of development, the sample is rinsed in several beakers of deionized water for a total duration of 10 minutes (the sample is transferred to a beaker of freshly prepared deionized water after every two and a half minutes). After deionized water rinsing, the sample is gently blown dry with nitrogen.

3.2.13 Tunneling Barrier Silicon Dioxide Deposition (Samples B and C)

For two samples in this processing batch, a tunneling barrier of silicon dioxide is deposited. Deposition is carried out by means of a sputtering mechanism on AJA Inc. Sputter tool in the cleanroom. This barrier defines the region through which electrons are expected to tunnel open biasing the devices once fabrication is complete.

The sputter deposition process is as carried out as described below:

- Samples are placed on a substrate holder and held in place by means of metal clips
- Sample surfaces are carefully blown with a nitrogen gun to get rid of any particles that may have settled on them
- Load lock chamber is vented to atmospheric pressure by means of a nitrogen purge
- Substrate holder is placed on transfer arm spatula in load lock chamber
- Load lock chamber is closed and pumped to a pressure of $< 2\times10^{-5}$ $mbar$
- Load lock gate valve is opened
- Transfer arm bearing the substrate holder is moved into the main deposition chamber
- Substrate holder is picked off transfer arm spatula by means of an adjustable z-height spindle rotational mechanism of the AJA Sputter deposition tool
- Spindle now holding substrate holder is adjusted to the safe transfer height
- Transfer arm is retracted from main deposition chamber to the load lock chamber
- Load lock gate valve is closed

- Spindle is adjusted to deposition height
- Spindle-substrate rotation is turned on and set to 50 rotations per minute
- Sputtering recipe is created as follows:

Nnaemeka_SiO2_G4_Spark

Power: 64W

Pressure: 35 mTorr

Ar: 30sccm, O2: 6 sccm

Coat time: 60 s (plasma ignition)

Temperature: RT

Nnaemeka_SiO2_G4_Dep_2nm

Power: 145 W

Pressure: 5 mTorr

Ar: 30 sccm, O2: 6 sccm

Temperature: RT

Pre-Sputter time: 120 s Deposition Time: 313 s

- Created recipe is started
- Matching network for sputtering is manually tuned to ensure reflected

power ranges from 0 – 1 W

- Sputter recipe proceeds to conclusion
- Spindle-substrate rotation is turned off
- Spindle Z position is adjusted to transfer height
- Load lock gate valve is opened
- Transfer arm is moved from load lock chamber to deposition chamber
- Substrate is lowered onto transfer arm spatula and unlatched from the spindle
- Transfer arm bearing substrate holder is retracted from main deposition chamber to the load lock chamber
- Load lock gate valve is closed
- Load lock pump is turned off
- Load lock nitrogen vent valve is opened to vent the load lock chamber to atmospheric pressure
- Load lock lid is taken off and substrate holder is taken out of the load lock chamber
- Sample is unclamped from substrate holder and stored in sample box

3.2.14 Chromium Oxide Deposition (Sample C)

This step involves the deposition of chromium oxide on one sample. This layer of chromium oxide is to provide the cold-electron filtering for this batch of devices.

The sputter deposition of chromium oxide is carried out on an AJA Sputter tool.

First, the sample is held onto a substrate holder by means of metal clips and fastened firmly by tightening the screws. With the sample firmly held in place, the sample surface is blown with nitrogen to remove any particles on it. At this point, the nitrogen purge valve is opened to vent the load lock chamber to atmospheric pressure. Once the load lock chamber is vented, the sample holder is placed on the transfer arm spatula with the sample. Also, two screws without clips are aligned with groves on the transfer arm spatula to serve as pivot screws for holding the sample holder in place once in the sputter deposition chamber. The load lock chamber is then closed with a lid and the load lock pump is turned on to allow pumping down of the load lock chamber to $< 2\times10^{-5}$ mbar. When this pressure tolerance is reached, the load lock gate valve is opened by turning a handle attached to the gate valve counterclockwise until the gate valve is completely open. As a safety precaution, the rotator spindle height of the AJA sputter tool is set to the transfer height before the next step. The transfer arm bearing the sample holder is now gently moved into the main sputter deposition chamber from the load lock chamber until it stops. This aligns the substrate holder directly below the rotator spindle which is designed to lock onto groves on the sample holder. The spindle height is lowered by adjusting the Z motion control knob until its forks slide into the groves of the substrate holder. The spindle is then rotated clockwise by turning the manual spindle rotation knob until it firmly holds onto the substrate holder. The wafer holder is now carefully raised to the safe transfer height by adjusting the manual Z motion control knob. The transfer arm in then retracted from the main chamber to the load lock chamber and the load lock gate valve is closed. Now, the substrate holder is adjusted to the deposition height (50 on the graduated column) by manually rotating the Z motion knob. The wafer rotation is then turned on and the control dial is set to 50 rotations per minute.

Before deposition starts, the main chamber must reach a pressure $< 2\times10^{-7}$ Torr.

The sputtering recipe Nnaemeka_Cr_2O_3 _G5_2nm is then created as follows:

Nnaemeka_Cr2O3_G5_Spark

Power: 64 W

Pressure: 35 mTorr

Ar: 30 sccm, O2: 6 sccm

Coat time: 60 s (plasma ignition)

Temperature: RT

Nnaemeka_Cr2O3_G5_Dep_2nm

Power: 145 W

Pressure: 5 mTorr

Ar: 30 sccm, O2: 6 sccm

Temperature: RT

Pre-Sputter time: 120 s

Deposition Time: 200 s

The recipe is now initiated. The preliminary steps of each step in the recipe require manual tuning of the matching networks for the RF plasma whereas the process times for each step

proceeds automatically. The manual tuning of the matching networks involves keeping the reflected power between 0 – 1W as the forward power is ramped up to the set points defined in the recipe. Once the reflected power is maintained at this level, the process proceeds automatically. When sputtering is complete, the substrate rotation dial is set to 0 rotations per minute and the rotation controller is turned off. The substrate holder height is adjusted to the safe transfer height by rotating the Z motion control knob. The load lock gate valve is opened by rotating the gate valve handle counterclockwise until the valve is fully open. The transfer arm is moved into the main chamber from the load lock chamber until it stops ie. positioned directly below the substrate holder. The substrate holder spindle is then lowered until it rests on the transfer arm spatula. The substrate spindle is then rotated so that it unlatches from the substrate holder. The substrate holder Z position is set to the safe transfer height and the transfer arm is moved from the main deposition chamber to the load lock chamber. The load lock gate valve is closed is then closed, and the load lock pump is turned off. This is followed by opening the nitrogen vent purge valve. Once the load lock chamber is vented to atmospheric pressure, the load lock lid is taken off and the substrate holder is taken out of the load lock chamber. The load lock lid is then placed back on the load lock chamber and the nitrogen purge valve is closed. The sample is now unclipped from the substrate holder and stored in a wafer box for further processing.

3.2.15 Source and Drain Contacts Metal Deposition (Samples A, B and C)

The goal of the preceding photolithography step was to define the regions where the source and drain contacts will be positioned on devices. This processing step caters to that by deposition of metal contacts for the source and drain openings created by the second photolithography step.

The deposition was done by means of a physical vapor deposition process using an electron beam evaporator (CHA Solution).

The procedure for the deposition is as follows:

- Samples are clipped onto substrate holder
- CHA Solution electron beam evaporator is vented
- Sample is loaded onto rotational substrate carrier in the tool
- Crucible containing chromium is placed in the appropriate pocket in the deposition chamber
- Deposition chamber is closed
- Deposition chamber is pumped to required vacuum setpoints for the deposition process
- Recipe for deposition is created as follows:
    - Deposition rate: 0.1 nm/s
    - Layer thickness: 100 nm
- Recipe for deposition is run
- Deposition chamber is vented to atmospheric pressure using nitrogen at the conclusion of the deposition process
- Substrate holder and target material crucible are unloaded from deposition chamber
- Samples are unclipped from substrate holder and stored in sample box

3.2.16 Lift-off, Photoresist Removal, Sample Cleaning and degassing

Excess metal deposited as well as photoresist from the previous process is to be removed during this step. The lift-off and sample cleaning process is carried out as described below:

- Samples are held upside down for 60 seconds in a solution of acetone
- Samples are agitated while still being held upside down in a freshly prepared solution of acetone for 120 seconds
- Samples are placed right side up in yet another freshly prepared solution of acetone
- Ultrasonication of the sample in acetone solution for 15 minutes follows
- Samples are blown dry with nitrogen
- Samples undergo UV/Ozone cleaning for 15 minutes
- Two additional alternating cycles of acetone sonication and UV/Ozone cleaning each lasting 15 minutes are carried out
- Two cycles of isopropanol sonication each lasting 15 minutes is carried out
- Samples are blown dry with nitrogen and stored in sample holder

The degassing step is carried out as follows:

- Metal clips are used to hold samples onto AJA Sputter substrate holder
- Load lock chamber is vented to atmospheric pressure by opening the

nitrogen vent valve

- Substrate holder is placed on transfer arm in load lock chamber
- Load lock chamber is closed
- Gate valve separating main and load lock chambers is opened
- Transfer arm with substrate holder in place is moved from load lock chamber into the main chamber
- Tool spindle system is used to pick substrate holder off transfer arm spatula
- Spindle system now holding substrate holder is adjusted to the safe transfer height
- Transfer arm is retracted from main chamber to load lock chamber
- Gate valve separating load lock chamber from main chamber is closed
- Spindle rotation is turned on and rotation is set to 50 rotations per minute
- Substrate heater is turned on
- Heater temperature is increased from 15°C to 50°C
- Once at 50°C, substrate heater temperature is increased to 200°C in steps of 50°C
- The degassing process at 200°C lasts for 2 hours after which the substrate heater is turned off
- After one and a half hours, the chamber cools down to room temperature
- Spindle rotation is set to 0 rotations per minute and then turned off

- Spindle-substrate holder system is raised to safe transfer height
- Load lock-main chamber gate valve is opened
- Transfer arm is moved into main chamber from load lock chamber
- Substrate is lowered onto transfer arm spatula and unhinged
- Transfer arm bearing substrate holder is retracted from main chamber to the load lock chamber
- Gate valve is closed
- Load lock pump is turned off and nitrogen vent valve is opened
- Substrate holder is removed from load lock chamber
- Samples are unclamped from substrate holder and stored in sample box

3.2.17 Passivation Silicon Dioxide Deposition

Silicon dioxide of thickness 50 nm is sputtered onto the samples to serve as a layer of passivation for all device features fabricated up to this point. Sputtering is carried out on AJA Sputter according to the following recipe based on earlier described processes for operating this tool:

Nnaemeka_SiO2_G4_Spark

Power: 64W

Pressure: 35 mTorr

Ar: 30sccm, O2: 6 sccm

Coat time: 60 s (plasma ignition)

Temperature: RT

Nnaemeka_SiO2_G4_Dep_50nm

Power: 145 W

Pressure: 5 mTorr

Ar: 30 sccm, O2: 6 sccm

Temperature: RT

Pre-Sputter time: 120 s

Deposition Time: 7837 s

3.2.18 Planarization Photoresist Coating

The sample was coated with planarization photoresist (PC3-700) according to the following spin coating recipe on a Headway Rearch Coater:

Film Properties (Spin Coating)

Step 1:

Speed – 800 rpm

Ramp – 100 rpm/s

Time – 80 s

Step 2:

Speed – 0 rpm

Ramp – 100 rpm/s

Time – 0.1 s

Nominal thickness: 1500 – 1700 nm

After spin coating, post-coat bake was done on a Cole Palmer Hot Plate at 200°C for 120 seconds.

3.2.19 Planarization Photoresist Etchback

This step is aimed at exposing the silicon dioxide pillar with 100 nm Cr (for Sample A), as well as 2 nm sputtered silicon dioxide (for Sample B) and 2 nm sputtered silicon dioxide in addition to 2 nm chromium oxide (for Sample C). The etching mechanism used to accomplish this is dry etching. This is carried out on a Technics Macro RIE 8800 tool with the following etch recipe:

Power: 350 W

Pressure: 200 mTorr

O_2 : 11 sccm

Time: 1095 s

This etching was made possible by already determined etch rate for PC3-700 planarization resist under these chamber conditions.

Once the etching was completed, KLA Tencor P6 Profilometer was used to confirm that the desired flats atop the silicon dioxide pillar has been exposed.

3.2.20 Chromium and Silicon Dioxide Etching

With the silicon dioxide pillar exposed, this processing step sought to etch the entire silicon dioxide pillar including the different layers on top the pillars for Samples B and C. Wet etching was used for this step and the following reagents were used: hydrochloric acid (HCl), hydrofluoric acid (HF), chromium etchant.

Etching was done for the samples as described below:

HF (50:1) – 40 s

HCl – 10 s

Cr etchant – 30 s

HF (50:1) – 300 s

The samples were rinsed with copious amounts of deionized water between each etch step. The samples were then blown dry with nitrogen at the conclusion of the wet etching sequence.

3.2.21 Planarization Photoresist Removal and Sample Cleaning and degassing

Planarization photoresist was removed during this step and the sample was thoroughly cleaned and degassed afterwards.

First, the samples were rinsed with a squeeze bottle of acetone. This was followed by acetone ultrasonication for 15 minutes. The samples were then UV/Ozone cleaned for 15 minutes. One more cycle of acetone ultrasonication and UV/Ozone cleaning followed, after which two isopropanol ultrasonication steps each lasting 15 minutes was done. The samples were then blown dry with nitrogen at the conclusion of the final isopropanol ultrasonication step.

The samples were then degassed in AJA Sputter according to the steps previously described.

3.2.22 Gate Silicon Dioxide Deposition

This step was incorporated to deposit the gate contact isolation oxide necessary for channel formation when devices are biased. The silicon dioxide used for this film was deposited by plasma-enhanced chemical vapor deposition on a TRION PECVD tool. The deposition was carried out after the deposition chamber was cleaned. The recipe for the deposition is as presented below:

TRION PECVD		
Step 1 (Passivation)	**Step 2 (Growth)**	**Step 3 (N_2 Purge)**
ICP Power: 0 W	ICP Power: 500 W	ICP Power: 0 W
Pressure: 1000 mTorr	Reflected Power Tolerance: 10 W	Pressure: 250 mTorr
N_2O: 179 sccm	Pressure: 1000 mTorr	N_2: 250 sccm
N_2: 250 sccm	N_2O: 179 sccm	Temperature: 380°C
SiH_4/Ar: 10 sccm	N_2: 250 sccm	Time: 180 s

Temperature: 250°C	SiH_4/Ar: 10 sccm	
Time: 1200 s	Temperature: 380°C	
	RF Stabilization Time: 10s	
	Time: 68 s	

Table 1: Gate Silicon Dioxide Deposition Recipe

3.2.23 Third Mask (Gate) Photolithography, Alignment and Development

To define the gate for the devices a third photolithography step was carried out. Samples were first coated with negative photoresist (NR9-1000PY) according to the following spin coating recipe:

Step 1

Speed – 500 rpm

Ramp – 100 rpm/s

Time – 5 s

Step 2

Speed – 3000 rpm

Ramp – 1000 rpm/s

Time – 60 s

Step 3

Speed – 0 rpm

Ramp – 1000 rpm/s

Time – 0.1 s

The photoresist coated samples were then annealed at 150°C for 60 seconds prior to alignment and UV exposure on the OAI Backside aligner. Alignment was done such that alignment marks on the photomask perfectly overlapped with alignment marks on the samples from the previous photolithography steps. The exposure dose for this step was 120 mJ/cm^2 . After exposure, the samples were baked at 100°C for 60 seconds. This was followed by development in RD6 photoresist developer once the sample had cooled down. Development lasted for a duration of 10 seconds while the developer solution containing the samples were gently agitated. After development, the samples were thoroughly rinsed in deionized water for 10 minutes with the deionized water being replaced after every 2.5 minutes. At the conclusion of deionized water rinsing, the samples were blown dry with nitrogen and stored in a sample holder.

3.2.24 Gate Contact Deposition

The gate terminal was deposited in this processing step by electron beam evaporation using CHA Solution E-Beam Evaporator. The sequence of steps for running the process are as earlier described and the process recipe for deposition of the gate metal are as shown below:

Target material: Chromium (Cr)

Nominal deposition thickness: 100 nm

Deposition rate: 0.1 nm/s

Deposition temperature: Room Temperature

3.2.25 Lift-off, Sample Cleaning and degassing

Surplus gate metal deposited as well as photoresist from the previous process is removed during this step. The lift-off and sample cleaning process are carried out as follows:

- Samples are held upside down for 60 seconds in a solution of acetone
- Samples are agitated while still being held upside down in a freshly prepared solution of acetone for 120 seconds
- Samples are placed right side up in yet another freshly prepared solution of acetone
- Ultrasonication of the sample in acetone solution for 15 minutes follows
- Samples are blown dry with nitrogen
- Samples undergo UV/Ozone cleaning for 15 minutes
- Two additional alternating cycles of acetone sonication and UV/Ozone cleaning each lasting 15 minutes are carried out
- Two cycles of isopropanol sonication each lasting 15 minutes is carried out
- Samples are blown dry with nitrogen and stored in sample holder

Sample cleaning is followed by degassing at 200°C for two hours on AJA Sputter according to the procedure earlier detailed.

3.2.26 Passivation Silicon Dioxide Deposition

The entirety of the samples is passivated with 50 nm of silicon dioxide in this step in preparation for creating vias for source, drain and gate contact terminals in subsequent processing steps.

Passivation silicon dioxide is deposited on AJA Sputter based on earlier described procedure for operating this tool according to the following recipe:

Nnaemeka_SiO2_G4_Spark

Power: 22 W

Pressure: 35 mTorr

Ar: 30sccm, O2: 6 sccm

Coat time: 60 s (plasma ignition)

Temperature: RT

Nnaemeka_SiO2_G4_Dep_50nm

Power: 142 W

Pressure: 5 mTorr

Ar: 30 sccm, O2: 6 sccm

Temperature: RT

Pre-Sputter time: 120 s

Deposition Time: 8707.8 s

After sputtering of 50 nm passivation silicon dioxide, the samples are stored in a wafer holder.

3.2.27 Fourth Mask (Via) Photolithography, Alignment and Development

This photolithography step defined cylindrical vias on top source, drain and gate metal contacts. Samples were first coated with negative photoresist (NR9-1000PY) according to the following spin coating recipe:

Step 1

Speed – 500 rpm

Ramp – 100 rpm/s

Time – 5 s

Step 2

Speed – 3000 rpm

Ramp – 1000 rpm/s

Time – 60 s

Step 3

Speed – 0 rpm

Ramp – 1000 rpm/s

Time – 0.1 s

Coated samples were then annealed at 150°C for 60 seconds prior to alignment and UV exposure on the OAI Backside aligner. Alignment was done to ensure perfect overlaying of photomask alignment marks for the fourth layer with alignment marks on the samples from the previous photolithography steps. The exposure dose for this step was 120 mJ/cm^2 . After exposure, samples were baked at 100°C for 60 seconds. This was followed by development in RD6 photoresist developer after the samples cooled down. Development in RD6 photoresist developer lasted for 10 seconds while the developer solution containing the samples were gently agitated. After development, the samples were thoroughly rinsed in deionized water for 10 minutes with the deionized water being replaced after every 2.5 minutes. At the conclusion of deionized water rinsing, the samples were blown dry with nitrogen and stored in a sample holder.

3.2.28 Silicon Dioxide etching and Argon Sputtering

With the vias defined by the preceding photolithography and development step, exposed passivation silicon dioxide was etched by reactive ion etching in the Technics Macro RIE 8800 according to the following recipe:

Step 1

Power: 600 W

Pressure: 160 mTorr

CF_4 : 30 sccm

O_2 : 3.6 sccm

Time: 200 s

Step 2

Power: 350 W

Pressure: 200 mTorr

O_2 : 11 sccm

Time: 45 s

This was followed by Argon sputtering to get rid of any photoresist residue or reactive ion etching byproducts which may have been present on the via contact surface. The recipe for the argon sputtering is as follows:

Power: 600 W

Pressure: 160 mTorr

Ar: 25 sccm

Time: 10 minutes

3.2.29 Chromium and Gold Contact Deposition

With the via surface cleaned, layers of chromium and gold were deposited by means of electron beam evaporation on AJA Electron Beam Evaporator according to previously described procedure for operating this tool with the following deposition parameters:

Layer 1 (Cr)

Deposition temperature: Room temperature

Deposition rate: 0.05 nm/s

Nominal deposition thickness: 5 nm

Deposition current: 2.8 mA

Layer 2 (Au)

Deposition temperature: Room temperature

Deposition rate: 0.05 nm/s

Nominal deposition thickness: 20 nm

Deposition current: 3.2 mA

At the conclusion of the deposition process, the samples were unloaded and stored in a wafer holder.

3.2.30 Photoresist Removal, Sample Cleaning and degassing

Removal of photoresist as well as metal deposited on photoresist is addressed by this processing step. The lift-off and sample cleaning process are carried out as follows:

- Samples are held upside down for 60 seconds in a solution of acetone
- Samples are agitated while still being held upside down in a freshly prepared solution of acetone for 120 seconds
- Samples are placed right side up in yet another freshly prepared solution of acetone
- Ultrasonication of the sample in acetone solution for 15 minutes follows
- Samples are blown dry with nitrogen
- Samples undergo UV/Ozone cleaning for 15 minutes
- Two additional alternating cycles of acetone sonication and UV/Ozone cleaning each lasting 15 minutes are carried out
- Two cycles of isopropanol sonication each lasting 15 minutes is carried out
- Samples are blown dry with nitrogen and stored in sample holder

After samples are cleaned, degassing is done at 200°C for two hours on AJA Sputter according to the procedure earlier described.

At this point, fabrication for this batch of devices is completed and electrical characterization is then carried out.

3.3 New Mask Design Process Flow

3.3.1 HF Strip and Piranha Cleaning

Bare test grade n-type 4-inch wafers are stripped of native SiO_2 using HF (10:1), this is done by immersing the wafer in 10:1 Hydrofluoric (HF) acid for 5 minutes. After HF immersion, the wafer is rinsed under running deionized water for about 2 minutes. This is then followed by thorough rinsing in 3 beakers of deionized water for 2 minutes.

To rid the wafer of organic impurities cleaning with Piranha solution is carried out. Piranha solution is prepared using H_2SO_4 and H_2O_2 in a ratio 3:1 (60mL:20mL). Piranha solution cleaning is done by immersing the wafer in the solution for 30 minutes after which thorough rinsing under both running deionized water and 3 beakers of deionized water is carried out. After rinsing, the wafer is thoroughly dried by blow-drying with N_2.

3.3.2 100nm SiO_2 Growth

SiO_2 was grown on the cleaned Si wafer by a process of dry thermal oxidation at 1100°C in an Oxidation Furnace (Tystar). The entire process for growing SiO_2 is defined on a recipe which is defined on the Tystar Oxidation Furnace computer. With the recipe made, the process is started. The first step involves ejection of the oxidation tube from the oxidation chamber. When the boat is out, the wafers are then placed in a wafer carrier and then placed centrally on the support rods of the furnace tube. The oxidation tube with the wafers loaded, is then gradually reinserted into the furnace in 15 minutes. After completely loading the wafers, the furnace is preheated to 700°C with ambient N_2, at a flow rate of 5000 sccm, for 30 minutes. Once 700°C is attained, the chamber temperature can stabilize at this set point (700°C) for 30 minutes. Once temperature tolerances are within compliance, the oxidation furnace temperature is ramped up to 1100°C in 1 hour still with ambient N_2 purge at a flow rate of 5000 sccm. A temperature stabilization step which lasts 30

minutes follows the ramp to 1100C. With the furnace temperature stable at 1100°C, growth of SiO_2 on the Si wafer begins with an O_2 flow of 3000 sccm; the growth takes 35 minutes. Once the growth is complete, an annealing step lasting 20 minutes follows; this step includes an ambient N_2 furnace purge at a flow rate of 5000 sccm. After the annealing step, the furnace temperature is ramped down to 700C. At this time, the wafers are then unloaded from the furnace. Once the wafers are taken out of the furnace, they can cool down prior to transferring them into wafer boxes. The thickness of SiO_2 grown is measured using the Gaertner Ellipsometer and Ocean Optics NC-UV-Vis Reflectometer.

3.3.3 First Photolithography and Development

The next step in the fabrication process involves defining an opening to allow direct contact between source and drain electrodes and the silicon substrate. To do this, the full 4-inch Si wafer is cleaved into four equal quadrants. This is important because the mask patterns are designed to match quadrants of a 4-inch Si wafer ie. first mask maps to quadrant 1, second mask maps to quadrant 2, third mask maps to quadrant 3 on photolithography mask.

Cleaving of wafers is done by making incisions along the circumference of the 4-inch wafer which align with boundaries of quadrants. A pair of tweezers are then used to gently pry either side of the incisions until cleavage occurs.

To reduce the risk of contamination from the wafer cleaving process, each quadrant is cleaned by ultrasonication in a bath of acetone for 15 minutes. After acetone ultrasonication, the wafer is then rinsed with a squeeze bottle of isopropanol. This is then followed by ultrasonication in a bath of isopropanol for 15 minutes. Following isopropanol ultrasonication, the wafer is blown dry with nitrogen.

In order to eliminate the risk of trapped solvents from the ultrasonication processes, the wafer is annealed on a Cole Palmer Hot Plate at 200°C for 20 minutes. Once the dehydration bake is complete, the wafer is coated with a negative photoresist (NR9-1000PY, Futurrex Inc.) according to the following spin coating recipe using a Headway Rearch PWM32 Coater:

500 rpm, 100 rpm/s, 5 s

3000 rpm, 1000 rpm/s, 60 s

0 rpm, 1000 rpm, 0.1 s

Negative resist spin coating is followed by pre-exposure bake to rid the coated photoresist of solvents. Pre-exposure bake is done on another Cole Palmer Hot Plate at 150°C for 60 seconds.

The desired patterning of the first mask is done by exposing negative photoresist to UV light. This process is carried out using an OAI Backside Aligner. The top right quadrant of the photolithography mask is aligned with the negative photoresist coated wafer. With the wafer aligned, the wafer is raised by means of a substrate chuck with current set to 14 mA. Once contact is established between the wafer and photolithography mask, a vacuum is formed to sustain contact between the wafer and the mask by activating vacuum contact mode on the OAI Aligner process setting. This first photolithography step requires an exposure dose of 120 mJ/cm2, which corresponds to an exposure time of 6 seconds. After UV exposure the wafer is unloaded and subjected to a post-exposure bake process immediately on a Cole Palmer Hot plate at 100°C for 60 seconds. After baking, the sample was developed in a photoresist developer (RD6, Futurrex Inc.) by immersion in the developer solution while agitating the beaker gently for a duration of 10 seconds. With development complete, the wafer is rinsed in several baths of deionized water for

10 minutes with the deionized water baths changed after every 2.5 minutes. Once deionized water rinsing is complete, the wafer is dried with nitrogen.

3.3.4 Reactive Ion Etching (SiO_2)

The next step in the fabrication process involves a reduction in the thickness of SiO_2 in the region exposed during the preceding photolithography step. This is done with the rest of the wafer protected by negative photoresist leaving only the trenches of "islands" left from the photolithography and development process. This dry etching process is favorable because etch selectivity between NR9-1000PY (negative photoresist) and SiO_2 is quite high during the SiO_2 etch process involving tetrafluoromethane (CF_4) and oxygen O_2 .

The reactive ion etching of SiO_2 is carried out in a Technics Macro-RIE 8800 tool. First off, the etch chamber is vented with a purge of N_2 . This is followed by the wafer being loaded onto the etch chamber platen; the wafer is centrally placed on the platen to facilitate uniform etching of SiO_2 . After wafer is loaded, the etch chamber is closed and pumped down to about 45 mTorr. The next step involves creating the etch recipe for the desired silicon dioxide etch process. It is desired that 80 nm of silicon dioxide is etched during this process to leave about 20 nm of SiO_2 remaining in the "island" region. The etch is run using the following recipe in two steps (the first step is the actual silicon dioxide etch while the second step is a descumming step to rid the wafer of fluoride complexes formed during the
silicon dioxide etch process) at a nominal etch rate of 0.8 nm/s:

Step 1

Power: 600 W

Pressure: 160 mT

CF_4 : 30 sccm

O_2 : 3.6 sccm

Time: 105 s

Step 2

Power: 350 W

Pressure: 200 mT

O_2 : 11 sccm

Time: 120 s

Once the reactive etching process is completed, the wafer is unloaded and stored in wafer storage box in preparation for the next fabrication step.

3.3.5 Lift-Off/Photoresist Removal

This processing step involves the removal of negative photoresist (NR9-1000PY) covering most of the sample in order to expose the underlying silicon dioxide. To do this, the wafer is first carefully rinsed with a squeeze bottle of acetone after which ultrasonication in a bath of acetone for 15 minutes is carried out. With acetone ultrasonication complete, the wafer is rinsed with a squeeze bottle of isopropanol. This is then followed by 15 minutes ultrasonication in isopropanol.

After isopropanol ultrasonication the sample is carefully blown dry with nitrogen and then stored in a wafer storage container for subsequent processing.

To confirm the degree of reactive ion etching of silicon dioxide in the previous step, the surface profile of the wafer features is scanned using a KLA Tencor P6 Profilometer. This is also important to help determine the starting silicon dioxide thickness in the regions neighboring the "island" defined during the first photolithography process (these surrounding regions will have source and drain contacts in subsequent processing steps).

The wafer is loaded centrally and carefully onto the KLA Tencor P6 Profilometer stage and a vacuum switched is turned on to hold the sample in place during the surface profiling process. The scan recipe is then selected for the profilometry process on the tool's software. The process of profiling the sample surface involves the use of a vibration-sensitive stylus capable of nanometer resolution vertical measurements. Several features on the sample are scanned (alignment and guide marks) and these measurements are recorded.

In addition to actual feature height measurements from the KLA Tencor P6 Profilometer, actual thicknesses of silicon dioxide remaining on the wafer are measured on the Gaertner Ellipsometer and the Ocean Optics Reflectometer. For measurements on both these tools, several readings are taken and recorded.

Thickness measurement on the Gaertner Ellipsometer involves warming up the tool laser for 15 minutes after which the sample is carefully loaded onto the wafer holding stage. With the wafer in place, the laser shutter is opened and the red laser for thickness measurement becomes visible on the region of interest of the sample. At this point, the wafer holding stage tilt and central alignment is resolved by means aligning two crosshairs corresponding with the stage tilt and x-y

alignment respectively through a viewport. The mechanism of tilt and axis alignment is completed by adjusting rotational knobs for each of these functions. Once the wafer is centrally, a silicon dioxide thickness measurement recipe is loaded (with a refractive index of 1.4571) and used to determine the SiO_2 thickness on the sample. This thickness measurement is recorded, the sample unloaded and stored in a wafer box for further processing.

For the Ocean Optics Reflectometer thickness measurement, a blank silicon wafer is first used to calibrate the equipment to establishment a base reflection profile. Then a thermally grown silicon dioxide recipe is loaded and used to measure the film thickness, which is then recorded. The wafer is now stored in a sample holder for subsequent processing.

3.3.6 HF (10:1) Etch (SiO_2)

At this point all silicon dioxide in the island region is completely etched to expose underlying silicon. This is important to establish a clear separation without any bridging material between the regions which source and drain contacts will be defined. Simultaneously, silicon dioxide in the surrounding regions is also etched until about 50 nm is remaining. This silicon dioxide thickness of 50 nm is crucial to allow for enough contrast during the next photolithography alignment step. We observed that, an SiO_2 thickness less than 50 nm made it almost impossible for second mask alignment to be done.

This hydrofluoric acid etch processing is done in two steps in order to monitor silicon dioxide etch rate for consistency with previously established etch rate data, as well as limit the possibility of over-etching; hence rendering the sample unsuitable for the next photolithography alignment process.

A beaker of hydrofluoric acid (10:1) is prepared and the sample is immersed in the solution for half the time required to leave 50 nm of silicon dioxide on majority of the sample surface. As

an illustration, if 80 nm of silicon dioxide was present on the sample, two hydrofluoric acid etch steps each lasting 47 seconds is carried out leaving 50 nm silicon dioxide at the end of the process (this calculation is based on an etch rate of 0.32 nm/s which we established from experiments).

After each etch step, KLA Tencor P6 Profilometer measurements, Gaertner Ellipsometer thickness measurements and Ocean Optics Profilometer thickness measurements are recorded to monitor how much silicon dioxide is etched and how much silicon dioxide is left. Then, the sample is stored in a wafer holder for further processing.

3.3.7 Tunneling Barrier Deposition (Samples B and C)

A tunneling barrier consisting of 1 nm silicon dioxide is sputter deposited using a sputtering tool: AJA Sputter. This process defines the barrier through which electrons are expected to tunnel when the device is biased. Two samples are processed in this way to provide a means of comparing bias responses based on the different structures present in devices.

Samples are held in place on a sample holder by means of metal clips. The surface of the samples is then blown with the nitrogen gun to rid the surface of particulate contaminants or impurities. Next, the load lock chamber of the sputtering chamber is vented with N_2 . This is followed by placing the sample holder with the samples facing downwards on a transfer arm in the load lock chamber. The placing of the sample holder in the load lock chamber is done in such a way that two horizontally aligned pivot screws fit snugly in groves which keep the sample holder stable on the load lock transfer arm. At this point, the load lock chamber is closed with a lid and the load lock pump is turned on. It is required that the load lock chamber attains a pressure $< 2\times10^{-5}$ mbar before proceeding to the next step. Once the desired load lock pressure is reached, the load lock manual gate valve is opened fully by turning the gate handle counterclockwise until is stops. With the load lock gate valve open, the wafer transfer arm is moved slowly into the main chamber until

it stops, this positions the wafer holder directly below the rotator spindle assembly of the AJA Sputter tool. At this point, the rotator spindle is lowered until it aligns with the lock-in groves of the sample holder. The spindle is then rotated to latch onto the sample holder. With the sample holder held firmly by the rotator spindle, the spindle is adjusted to the transfer height and the transfer arm is carefully retracted from the deposition chamber. Now the load lock manual gate valve is closed by turning the gate handle clockwise until it stops. Next, the rotator spindle with the sample holder held in place is adjusted to the deposition height. Once at the deposition height, the tool rotation for the spindle is set to 50 rotations per minute and this is confirmed by peering into the viewport. Before sputtering starts, the chamber pressure is confirmed to be $< 2\times10^{-7}$ Torr. Then the Nnaemeka_SiO_2 _G4_1nm sputtering recipe is created with "Spark" and "Deposition" steps. Also, the deposition time for the "Deposition" step is set to 157 seconds (based on the sputter deposition rate of 0.00637 nm/s).

Nnaemeka_SiO2_G4_Spark

Power: 64W

Pressure: 35mTorr

Ar: 30sccm, O2: 6sccm

Coat time: 60s (plasma ignition)

Temperature: RT

Nnaemeka_SiO2_G4_Dep_1nm

Power: 142W

Pressure: 5mTorr

Ar: 30sccm, O2: 6sccm

Temperature: RT

Pre-Sputter time: 120s

Deposition Time: 157s

The Nnaemeka_SiO_2 _G4_1nm sputter deposition recipe is now run. Although the sputter process is virtually automated on this tool, the matching network on the AJA Sputter needs to be tuned manually at the onset of both the "Spark" and "Deposition" steps. Tuning the matching network once the process starts involves keeping the reflected power between 0 – 1W for the sputtering process. Once the reflected power is within this tolerance (0 – 1W), the sputtering process carries on in an automated fashion until completion.

When the sputter deposition is done, the spindle rotation is reset to 0 rotations per minute and the sample holder height is adjusted to the transfer height. At this point, the load lock gate valve is opened by rotating the valve handle counterclockwise until it stops, and the transfer arm is carefully moved into the deposition chamber until it stops. The sample holder is then carefully lowered onto the transfer arm while aligning the pivot screws on the sample holder with the groves on the transfer arm spatula. The rotator spindle is then turned counterclockwise to unlatch the sample holder from the spindle, this then allows for the spindle to be raised to the transfer height. The transfer arm with the sample holder in place is then carefully retracted from the deposition chamber to the load lock chamber. This is followed by the closure of the load lock gate valve. The load lock pump is then turned off and the nitrogen purge valve for the load lock chamber is opened.

Once the load lock chamber is purged to atmospheric pressure, the sample holder is unloaded from the load lock chamber and the nitrogen purge valve is closed. The samples are then unclipped from the sample holder and stored in wafer boxes for further processing.

3.3.8 Second Mask Alignment and Development

This alignment step is required to define the source and drain terminals of the devices. It involves a process of photolithography which overlays the second mask pattern on the glass-chrome mask onto the previously defined pattern of the first photolithography process.

First, samples are annealed on a Cole Palmer Hot Plate at 200°C for 20 minutes.

After precoat annealing, the samples are spin coated with a negative photoresist (NR9-1000PY) using the following recipe on a Headway Rearch PWM32 Coater:

500 rpm, 100 rpm/s, 5 s

3000 rpm, 1000 rpm/s, 60 s

0 rpm, 1000 rpm, 0.1 s

At the conclusion of spin coating, the samples are annealed at 100°C for 60 seconds on another Cole Palmer Hot Plate; this is the pre-exposure baking step. While the spin coating is taking place, the UV lamp for the OAI Aligner (tool for photolithographic patterning) is warmed up for 15 minutes. Next, the Z-chuck electromotor is set to 14 mA. All three chuck alignment micrometers are then set to their respective center positions of 5 mm. The mask plate is then loosened and removed from the tool assembly by unscrewing four mounting thumbscrews and then sliding the mask plate off the aligner stage by means of two plate handles. The vacuum holding the dummy

mask in place is then turned off and our mask is now placed on the mask plate such that the chrome side of the mask faces upwards. The mask vacuum is now turned back on. The mask plate is then carefully placed back onto the aligner stage. Then the mask plate is held onto the aligner stage by fastening the mask plate thumbscrews. The photoresist-coated wafer is now placed on the chuck with the coated side facing up. The substrate vacuum is then turned on to hold the wafer in place. The chuck is then raised close enough to the mask to allow visibility of substrate alignment marks on the LCD monitor. This visualization on the LCD monitor is made possible by means of an objective/camera assembly. At this point, two alignment marks at two horizontal extremes of the substrate and mask are used to align the second mask pattern on the mask with the first mask alignment marks on the substrate. Once alignment is complete, full contact is established between the substrate and the mask. This is followed by turning on contact vacuum on the LCD control monitor. Doing this sustains the contact between the substrate and the mask. UV exposure then follows using a dose of 200 mJ/cm^2 . After exposure, the substrate chuck is lowered using the Z-height rotation dial to disengage contact between the substrate and mask, substrate vacuum is then turned off and the sample is unloaded from the Aligner. A post-exposure bake step is then carried out a Cole Palmer Hot Plate at a temperature of 100°C for 60 seconds.

After post-exposure bake, the sample is developed in a solution of RD6 Photoresist developer for 10 seconds while being agitated. Once development is complete, the wafer is rinsed in four baths of deionized water for 2.5 minutes each while gently agitating the baths. The next step entails gently drying the sample with a nitrogen blown gun. After nitrogen blow drying, the sample is stored for subsequent processing.

3.3.9 Chromium Oxide Deposition (Sample C)

This step involves the deposition of chromium oxide on one sample. This layer of chromium oxide is to provide the cold-electron filtering for this batch of devices. The mechanism of cold-electron filtering serves to limit the detrimental effects of thermally excited electrons to the operation of conventional transistors.

The sputter deposition of chromium oxide is carried out on an AJA Sputter tool in the Nanotechnology Research Center cleanroom.

To begin, the sample is held in place on a sample holder by means of metal clips and fastened firmly by tightening allen screws which hold the clips down. With the sample firmly held in place, the sample surface is then blown with nitrogen to rid it of any particles. At this point, the nitrogen purge valve is opened to vent the load lock chamber to atmospheric pressure. Once the load lock chamber is vented, the sample holder is placed on the transfer arm spatula with the sample facing downwards. Also, two allen screws without clips are aligned with groves on the transfer arm spatula to serve as pivot screws which would facilitate holding the sample holder in place once in the sputter deposition chamber. The load lock chamber is then closed with a lid and the load lock pump is turned on to allow pumping down of the load lock chamber to $< 2\times10^{-5}$ mbar. When this pressure tolerance is reached, the load lock gate valve is opened by turning a handle attached to the gate valve counterclockwise until the gate valve is completely open. As a safety precaution, the rotator spindle height of the AJA sputter tool is confirmed to be set to the transfer height before the next step. The transfer arm bearing the sample holder is now gently moved into the main sputter deposition chamber until it stops. This aligns the sample holder directly below the rotator spindle which is designed to lock onto groves on the sample holder. The spindle height is lowered by adjusting the Z motion control knob until its forks slide into the groves

of the substrate holder (4-inch sample holder height: 39 – 40 on the scaled column). At this point, the spindle is rotated clockwise by turning the manual spindle rotation knob until it firmly latches onto the substrate holder. The wafer holder is now slowly raised to the safe transfer height by adjusting the manual Z motion control knob. The transfer arm in then retracted from the main chamber to the load lock chamber and the load lock gate valve is closed. Now, the substrate holder is adjusted to the deposition height (50 on the graduated column) by manually rotating the Z motion knob. The wafer rotation is then turned on and the control dial is set to 50 rotations per minute.

Before deposition commences, the main chamber must attain a pressure < 2×10^{-7} Torr. Then the sputtering recipe Nnaemeka_Cr_2O_3_G5_1nm is created as follows:

Nnaemeka_Cr2O3_G5_Spark

Power: 64W

Pressure: 35mTorr

Ar: 30sccm, O2: 6sccm

Coat time: 60s (plasma ignition)

Temperature: RT

Nnaemeka_Cr2O3_G5_Dep_1nm

Power: 142W

Pressure: 5mTorr

Ar: 30sccm, O2: 6sccm

Temperature: RT

Pre-Sputter time: 120s

Deposition Time: 125s

The recipe is now initiated. The preliminary steps of each step in the recipe require manual tuning of the matching networks for the RF plasma whereas the process times for each step proceeds automatically. The manual tuning of the matching networks involves keeping the reflected power in the range 0 – 1W as the forward power is ramped up to the set points defined in the recipe. Once the reflected power is maintained at this level, the process proceeds automatically. When sputtering is complete, the substrate rotation dial is set to 0 rotations per minute and the rotation controller is turned off. Then the substrate holder height is adjusted to the safe transfer height by rotating the Z motion control knob. The load lock gate valve is then opened by rotating the gate valve handle counterclockwise until the valve is fully open. The transfer arm is then moved into the main chamber from the load lock chamber until it stops ie. positioned directly below the substrate holder. The substrate holder spindle is then lowered until it nestles on the transfer arm spatula with the pivot screws on the substrate holder well placed in the spatula groves. Then the substrate spindle is rotated so that it unlatches from the sample holder. The substrate holder Z position is then set to the safe transfer height and the transfer arm is retracted to the load lock chamber. At this point, the load lock gate valve is closed, and the load lock pump is turned off while the nitrogen vent purge valve is simultaneously opened. Once the load lock chamber is

vented to atmospheric pressure, the load lock unlidded and the substrate holder is taken out of the load lock chamber. The load lock lid is then placed back on and the nitrogen purge valve is closed. The sample is now unclipped from the substrate holder and stored in a wafer box for further processing.

3.3.10 Source and Drain Metal Contact Deposition (Samples A, B and C)

At this point, trenches exist in the regions of the sample where metal electrodes for source and drain contacts should be whereas negative photoresist (NR9-1000PY) covers the rest of the sample surface. This step involves the evaporation of electron beam-melted metal pellets onto the surface of the sample under vacuum conditions. Doing this results in the formation of source and drain metal electrodes.

CHA Solution Electron Beam Evaporator or AJA Electron Beam Evaporator were used for this process depending on which of the two tools were available.

CHA Solution Evaporator:

To begin with, the samples are fastened onto the substrate holder by means of screws and clips. Then the surfaces of the samples are blown with a nitrogen gun to get rid of particulate contaminants. Next, pellets of the metal electrode (Ni) are poured into a graphite crucible. The deposition chamber is then vented to atmospheric pressure by means of a nitrogen purge. At the conclusion of the vent step, the tool is put in “Standby” mode by clicking the touchscreen control monitor. Next, the CHA Solution evaporator door is unlocked by clicking on the “Lock” button on the touchscreen. The crucible containing the target material (Ni) is then placed in the appropriate pocket. The wafers are then loaded onto the planetary rotation substrate holder while

being held in place spring loaded clips. With the wafers loaded the tool door is closed. The process recipe is now programmed on the touchscreen as follows:

Thickness: 100 nm

Deposition rate: 1.0 Å/s

Temperature: Room temperature

The correctly made process number is then run; this is an automatic process which proceeds to completion without any interference. The evaporation is carried out under vacuum conditions Once the deposition is complete, the sample and crucible are unloaded and stored accordingly.

AJA Electron Beam Evaporator:

Operation of this tool is primarily manual. To begin with, the sample is held onto the substrate holder by means of metal clips clamped down by tightening thumbscrews. The load lock chamber is then vented by means of a nitrogen purge (ie. the nitrogen purge valve is opened manually). The load lock lid is then removed, and the substrate holder is placed face down on the transfer arm spatula. The load lock is closed, and the load lock pump is turned on to bring the load lock chamber to a pressure < 2×10^{-5} mbar. Before the next step the main chamber ion gauge sensor is checked to confirm that the main deposition chamber has a pressure < 2×10^{-7} Torr The load lock gate valve is then opened and the transfer arm is moved into the main deposition chamber. A lock-in spindle is then lowered by rotating a Z motion rotation knob. The substrate holder is now picked up by the spindle when the forks on the spindle latch into groves on the substrate holder. The spindle in now raised to the safe transfer height and the transfer arm is retracted form the main chamber to the load lock chamber. At this point, the load lock gate valve is closed. The spindle is then lowered to

the deposition height. This is followed by turning on the substrate rotation; the rotation dial is set to 50 rotations per minute for the deposition to ensure uniformity of the deposition process. The thickness monitor is now turned on and programmed to the appropriate film (Cr or Ni), acoustic impedance and Z-factor. The crucible source selector is also set to the correct target material (Cr or Ni). Next, the electron beam voltage supply is turned on and ramped up until the desired deposition rate is attained. This ramping up step is done with the thickness monitor and source material shutters open while the substrate shutter remains closed. When the deposition rate stabilizes at the desired value (1.0 Å/s), the thickness monitor shutter is opened while simultaneously resetting the measured thickness to 0 Å. Once the desired thickness of 100 nm is attained, the substrate shutter is closed, and the electron beam current is slowly ramped down to 0 mA. The electron beam voltage supply is now turned off, the substrate rotation is also turned off and the unloading process follows as shown below:

- Rotation spindle is raised to safe transfer height by adjusting Z motion control knob
- Load lock gate valve is opened by manually rotating gate handlebar counterclockwise
- The transfer arm is then moved from the load lock chamber into the main deposition chamber until it is positioned directly below the substrate holder
- The substrate holder is now lowered onto the transfer arm spatula
- The spindle forks are disengaged from the substrate holder

- The spindle system is now raised to the safe transfer height
- Transfer arm is retracted from main chamber to load lock chamber
- Load lock gate valve is closed
- Load lock pump is turned off
- Load lock nitrogen purge valve is opened
- Substrate holder is removed from load lock chamber at the completion of the venting to atmospheric pressure step
- Sample is unclipped from the substrate holder and transferred to wafer storage box.

3.3.11 Lift-off

The lift-off step is essentially aimed at getting rid of the protective photoresist and excess metal deposited during the previous step.

Firstly, three beakers of acetone solution and three beakers of isopropanol solution are prepared. The samples are held upside down in one beaker of acetone solution for 60 seconds while being held still. This allows flakes of the deposited metal to fall to the base of the beaker by means of gravity. With the sample still held upside down, agitation in another beaker of acetone solution for 60 seconds follows. This ensures that tiny flakes which may still be clinging onto the surface of the sample are taken off. The sample is then ultrasonicated in acetone solution for 15 minutes. After sonication, the sample is rinsed with a squeeze bottle of isopropanol before additional ultrasonication in a solution of isopropanol for 15 minutes. At the end of isopropanol ultrasonication, the sample is blown dry with nitrogen and stored in a sample holder.

3.3.12 PECVD Side wall and Gate Oxide Deposition

First a standard clean recipe is run on the PECVD tool for a duration of 3 minutes. Next, we run a conditioning recipe on the PECVD tool using a dummy sample. The dummy sample is placed in the load lock and the conditioning process proceeds automatically according to the following recipe:

Step1: Stabilization

Pressure: 1000mT

Temperature: 380C

Time: 1200s

Step 2: Deposition

ICP Power: 150W

Pressure: 1000mT

Temperature: 380C

Time: 250s

Step 3

Pressure: 250mT

Temperature: 360C

Time: 180s

The thickness of deposited SiO_2 is then measured using Ocean Optics Reflectometer and Gaertner Ellipsometer to determine the deposition rate. Based on thickness measured, deposition time is

calculated for 50nm SiO_2 for actual samples. Thickness of oxide is measured before and after deposition on actual samples. Deposition recipe for actual samples is as follows:

Step1: Stabilization

Pressure: 1000mT

Temperature: 380C

Time: 1200s

Step 2: Deposition

ICP Power: 150W

Pressure: 1000mT

Temperature: 380C

Time: 250s

Step 3

Pressure: 250mT

Temperature: 360C

Time: 180s

Thickness of deposited oxide is determined using ellipsometer and reflectometer. The next step is to etch back 45nm of silicon dioxide using Technics Macro RIE. Etch back is done in three steps leaving ~ 5nm silicon dioxide remaining. The final step in the gate oxide deposition process entails PECVD deposition of 5nm bringing the gate oxide thickness to ~ 10nm. Additionally, effective

sidewall thickness becomes ~ 55nm. At the conclusion of gate oxide deposition, we proceed to the next step of the fabrication process.

3.3.13 Third Mask (Gate) Photolithography, Alignment and Development

To define the gate for the devices a third photolithography step was carried out. Samples were first coated with negative photoresist (NR9-1000PY) according to the following spin coating recipe:

Step 1

Speed – 500 rpm

Ramp – 100 rpm/s

Time – 5 s

Step 2

Speed – 3000 rpm

Ramp – 1000 rpm/s

Time – 60 s

Step 3

Speed – 0 rpm

Ramp – 1000 rpm/s

Time – 0.1 s

The photoresist coated samples were then annealed at 150°C for 60 seconds prior to alignment and UV exposure on the OAI Backside aligner. Alignment was done such that alignment marks on the photomask perfectly overlapped with alignment marks on the samples from the previous photolithography steps. The exposure dose for this step was 120 mJ/cm^2 . After exposure, the samples were baked at 100°C for 60 seconds. This was followed by development in RD6 photoresist developer once the sample had cooled down. Development lasted for a duration of 10 seconds while the developer solution containing the samples were gently agitated. After development, the samples were thoroughly rinsed in deionized water for 10 minutes with the deionized water being replaced after every 2.5 minutes. At the conclusion of deionized water rinsing, the samples were blown dry with nitrogen and stored in a sample holder.

3.3.14 Gate Contact Deposition

The gate terminal was deposited in this processing step by electron beam evaporation using CHA Solution E-Beam Evaporator. The sequence of steps for running the process are as earlier described and the process recipe for deposition of the gate metal are as shown below:

Target material: Chromium (Ni)

Nominal deposition thickness: 100 nm

Deposition rate: 0.1 nm/s

Deposition temperature: Room Temperature

3.3.15 Lift-off, Sample Cleaning

Surplus gate metal deposited as well as photoresist from the previous process is removed during this step. The lift-off and sample cleaning process are carried out as follows:

- Samples are held upside down for 60 seconds in a solution of acetone
- Samples are agitated while still being held upside down in a freshly prepared solution of acetone for 120 seconds
- Samples are placed right side up in yet another freshly prepared solution of acetone
- Ultrasonication of the sample in acetone solution for 15 minutes follows
- Samples are blown dry with nitrogen
- Two cycles of isopropanol sonication each lasting 15 minutes is carried out
- Samples are blown dry with nitrogen and stored in sample holder

3.3.16 Passivation Silicon Dioxide Deposition

The entirety of the samples is passivated with 50 nm of silicon dioxide in this step in preparation for creating vias for source, drain and gate contact terminals in subsequent processing steps.

Passivation silicon dioxide is deposited on AJA Sputter based on earlier described procedure for operating this tool according to the following recipe:

Nnaemeka_SiO2_G4_Spark

Power: 22 W

Pressure: 35 mTorr

Ar: 30sccm, O2: 6 sccm

Coat time: 60 s (plasma ignition)

Temperature: RT

Nnaemeka_SiO2_G4_Dep_50nm

Power: 142 W

Pressure: 5 mTorr

Ar: 30 sccm, O2: 6 sccm

Temperature: RT

Pre-Sputter time: 120 s

Deposition Time: 8707.8 s

After sputtering of 50 nm passivation silicon dioxide, the samples are stored in a wafer holder.

3.3.17 Fourth Mask (Via) Photolithography, Alignment and Development

This photolithography step defined cylindrical vias on top source, drain and gate metal contacts. Samples were first coated with negative photoresist (NR9-1000PY) according to the following spin coating recipe:

Step 1

Speed – 500 rpm

Ramp – 100 rpm/s

Time – 5 s

Step 2

Speed – 3000 rpm

Ramp – 1000 rpm/s

Time – 60 s

Step 3

Speed – 0 rpm

Ramp – 1000 rpm/s

Time – 0.1 s

Coated samples were then annealed at 150°C for 60 seconds prior to alignment and UV exposure on the OAI Backside aligner. Alignment was done to ensure perfect overlaying of photomask alignment marks for the fourth layer with alignment marks on the samples from the previous photolithography steps. The exposure dose for this step was 120 mJ/cm^2 . After exposure, samples were baked at 100°C for 60 seconds. This was followed by development in RD6 photoresist developer after the samples cooled down. Development in RD6 photoresist developer lasted for 10 seconds while the developer solution containing the samples were gently agitated. After development, the samples were thoroughly rinsed in deionized water for 10 minutes with the deionized water being replaced after every 2.5 minutes. At the conclusion of deionized water rinsing, the samples were blown dry with nitrogen and stored in a sample holder.

3.3.18 Silicon Dioxide etching and Argon Sputtering

With the vias defined by the preceding photolithography and development step, exposed passivation silicon dioxide was etched by reactive ion etching in the Technics Macro RIE 8800 according to the following recipe:

Step 1

Power: 600 W

Pressure: 160 mTorr

CF_4: 30 sccm

O_2: 3.6 sccm

Time: 200 s

Step 2

Power: 350 W

Pressure: 200 mTorr

O_2: 11 sccm

Time: 45 s

This was followed by Argon sputtering to get rid of any photoresist residue or reactive ion etching byproducts which may have been present on the via contact surface. The recipe for the argon sputtering is as follows:

Power: 600 W

Pressure: 160 mTorr

Ar: 25 sccm

Time: 10 minutes

3.3.19 Lift-off, Sample Cleaning

Surplus gate metal deposited as well as photoresist from the previous process is removed during this step. The lift-off and sample cleaning process are carried out as follows:

- Samples are held upside down for 60 seconds in a solution of acetone
- Samples are agitated while still being held upside down in a freshly prepared solution of acetone for 120 seconds
- Samples are placed right side up in yet another freshly prepared solution of acetone
- Two cycles of ultrasonication of the sample in acetone solution for 15 minutes follows
- Samples are blown dry with nitrogen
- Two cycles of isopropanol sonication each lasting 15 minutes is carried out
- Samples are blown dry with nitrogen and stored in sample holder

At this point, fabrication of the devices is completed.

3.4 Electrical Characterization

The electrical characterization of fabricated devices was carried out at room temperature in the clean room using an Agilent 4155C Semiconductor Parameter Analyzer.

Electrical Characterization Measurement Procedure

- Clean probe tips with methanol and dab gently with lint-free cleanroom wipes
- Ensure that no static charge is built up on probe tips by biasing all probe tips to 0 V
- Establish contact with source and drain contact pads and run a 0 V bias to get rid of static charge
- Place two probe tips on source contact pad to measure conductivity
- Establish contact with source and drain pads, then bias the drain with a sweep from 0 – 2.5 V while holding the source contact at 0 V
- For devices with gate contacts:
    - Place gate probe tip on gate contact pad
    - Remove static charge by biasing gate probe tip to 0 V
    - Perform gate biasing in steps for 0 – 2 V or desired voltage bias condition while running a voltage sweep across source and drain terminals

Chapter 4: Results and Discussion

4.1 Overview

This section details the experiments carried out to establish etch rates for various films obtained from several deposition and growth tools as well as electrical data and analyses for fabricated devices. Difficulties encountered during fabrication and enhancements to thin film deposition, wet chemical etching as well as

reactive ion etching processes are also discussed in this chapter. Additionally, results from IV measurements of fabricated transistor devices are presented and discussed.

4.2 Fabrication Process Optimization

For successful execution of each fabrication step it was crucial to establish nominal etch rates and deposition rates for various tools, films and solutions required for the entire fabrication process.

4.2.1 Etch rate determination

Dry and wet etch rates were determined for Plasma Enhanced Chemical Vapor Deposition (PECVD), AJA and CHA Electron Beam Evaporators and AJA Sputter silicon dioxide films. Additionally, dry etch rates for NR9-1000PY negative photoresist in various reactive ion etch gas chemistries were determined.

4.2.1.1 Wet etching

AJA Electron Beam Evaporator SiO_2*:*

The hydrofluoric acid etch rate of a film of silicon dioxide deposited by electron

beam evaporation using AJA Electron Beam Evaporator was determined by

measuring the thickness of the film after four etch steps. These thicknesses were established based on refractive index measurements for the as-deposited film. Refractive index was obtained from measurements on Metricon 2010/M Prism Coupler. Additional thickness measurements were obtained from Gaertner Ellipsometer and Ocean Optics Reflectometer based on the film refractive index.

Film properties

Deposition temperature: 200°C

Deposition rate: 0.01 – 0.015 nm

Nominal deposition thickness: 1000 nm

	Metricon 2010/M Prism Coupler				
Time (s)	0	30	60	90	120
Thickness (nm)	1111.5	1057.9	996.7	932.0	859.5
Refractive Index	1.4652	1.4650	1.4661	1.4674	1.4682

Table 2: Metricon measurements AJA E-Beam SiO2

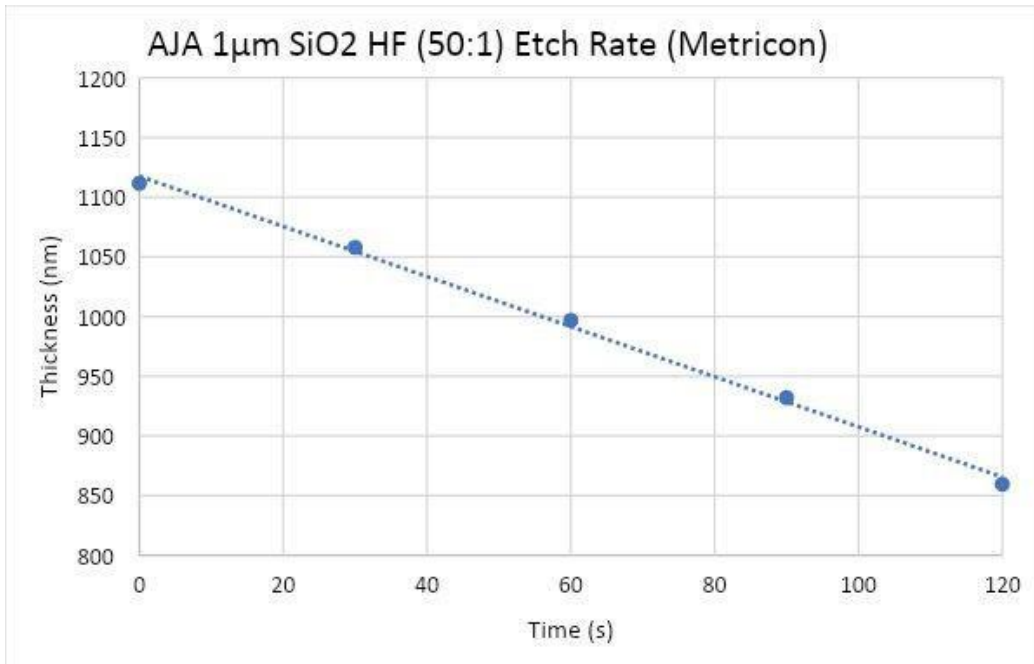

Figure 7: AJA E-Beam SiO2 HF (50:1) Etch Rate (Metricon)

Metricon measurements indicated an etch rate of 2.1 nm/s.

	Gaertner Ellipsometer				
Time (s)	0	30	60	90	120
Thickness (nm)	1148.7	1110.0	1038.6	992.7	926.4
Refractive Index	1.4652	1.4650	1.4661	1.4674	1.4682

Table 3: Ellipsometer measurements AJA E-Beam SiO2

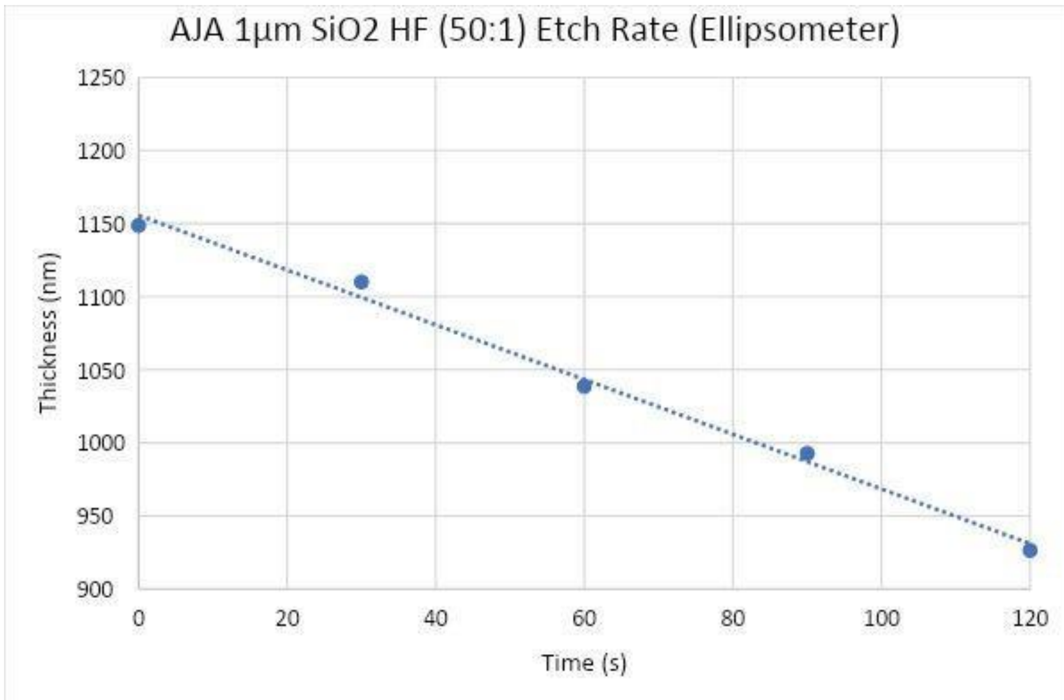

Figure 8: AJA E-Beam SiO2 HF (50:1) Etch Rate (Ellipsometer)

Gaertner Ellipsometer measurements indicated an etch rate of 1.9 nm/s.

	Ocean Optics Reflectometer				
Time (s)	0	30	60	90	120
Thickness (nm)	1145.7	1095.9	1035.3	997.3	926.7
Refractive Index	1.4668	1.4668	1.4668	1.4668	1.4668

Table 4: Reflectometer measurements AJA E-Beam SiO2

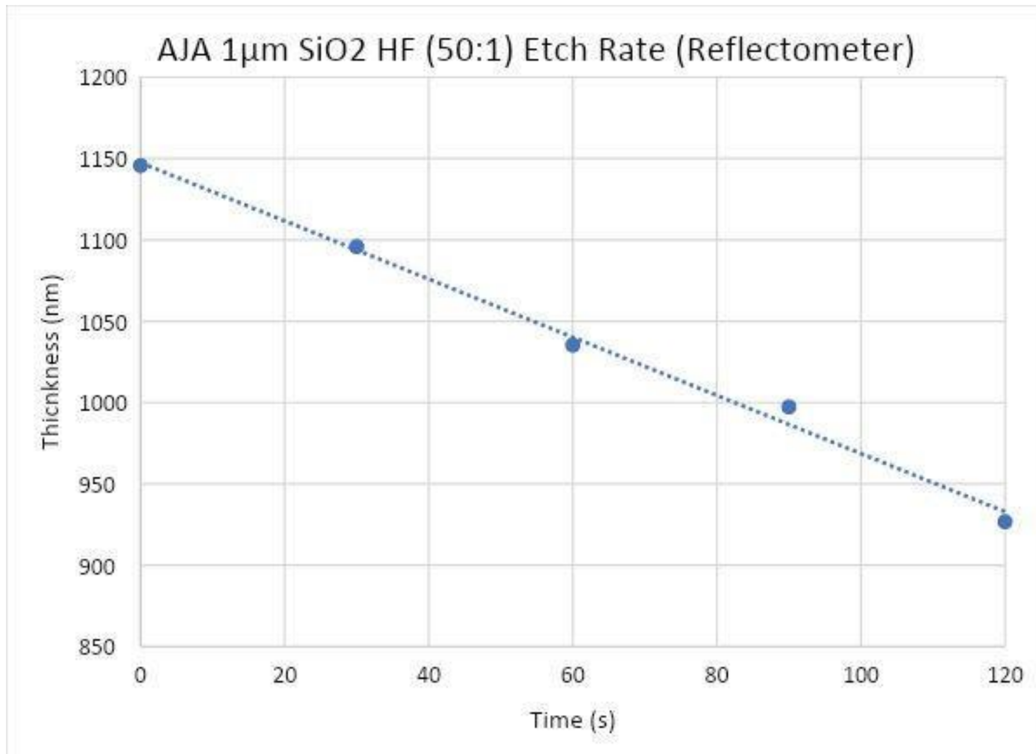

Figure 9: AJA E-Beam SiO2 HF (50:1) Etch Rate (Reflectometer)

Ocean Optics Reflectometer measurements indicated an etch rate of 1.8 nm/s.

AJA Sputter SiO_2:

A film of silicon dioxide was sputtered using AJA Sputter and the hydrofluoric acid etch rate was determined by measuring film thickness on two different metrology tools after four etch steps. Three spots on each film were measured after every etch step and the average of these measurements was used to obtain a

graphical description of the etch rate.

Film properties

Deposition temperature: Room Temperature

RF Power: 145 W

Nominal thickness: 80 nm

	Ocean Optics Reflectometer				
Time (s)	0	5	10	15	20
Thickness 1 (nm)	80.6	68.9	55.5	31.5	16.3
Thickness 2 (nm)	79.8	67.8	49.5	23.6	12.8
Thickness 3 (nm)	79.8	69.8	45.6	23.8	17.2
Average thickness (nm)	80.1	68.8	50.2	26.3	15.4

Table 5: Reflectometer measurements AJA Sputter SiO2

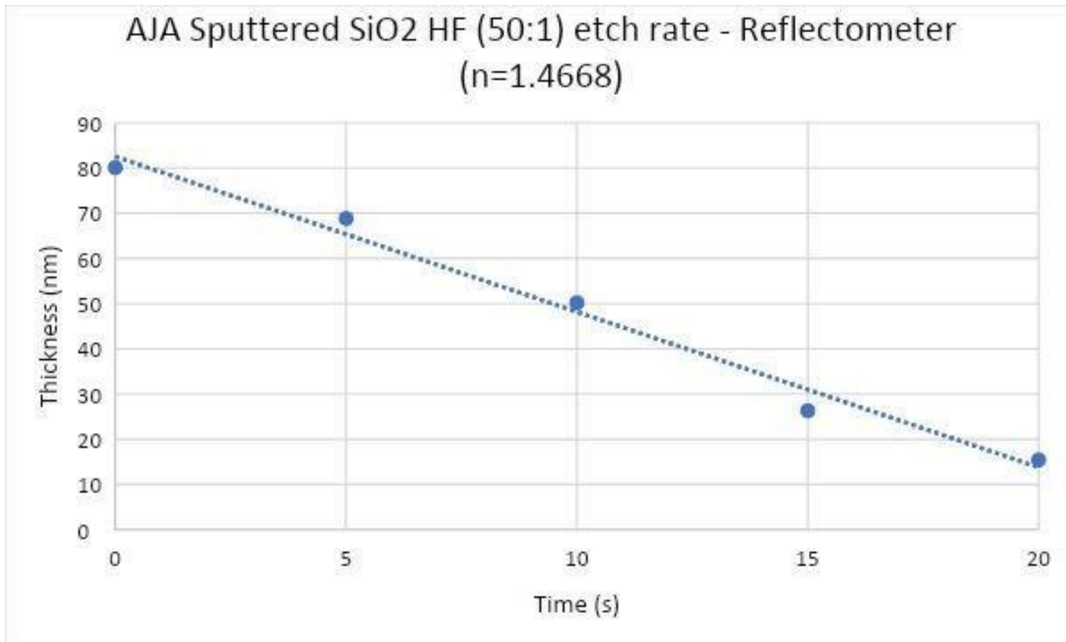

Figure 10: AJA Sputter SiO2 HF (50:1) Etch Rate (Reflectometer)

Ocean Optics Reflectometer measurements showed that the HF (50:1) etch rate for AJA Sputtered SiO_2 was 3.4 nm/s.

	Gaertner Ellipsometer				
Time (s)	0	5	10	15	20
Thickness 1 (nm)	76.9	64.2	59.5	31.3	19.1
Thickness 2 (nm)	77.2	65.7	58.9	35.1	14.9
Thickness 3 (nm)	77.1	63.9	61.9	49.6	15.1
Average thickness (nm)	77.1	64.6	60.1	38.7	16.4

Table 6: Ellipsometer measurements AJA Sputter SiO2

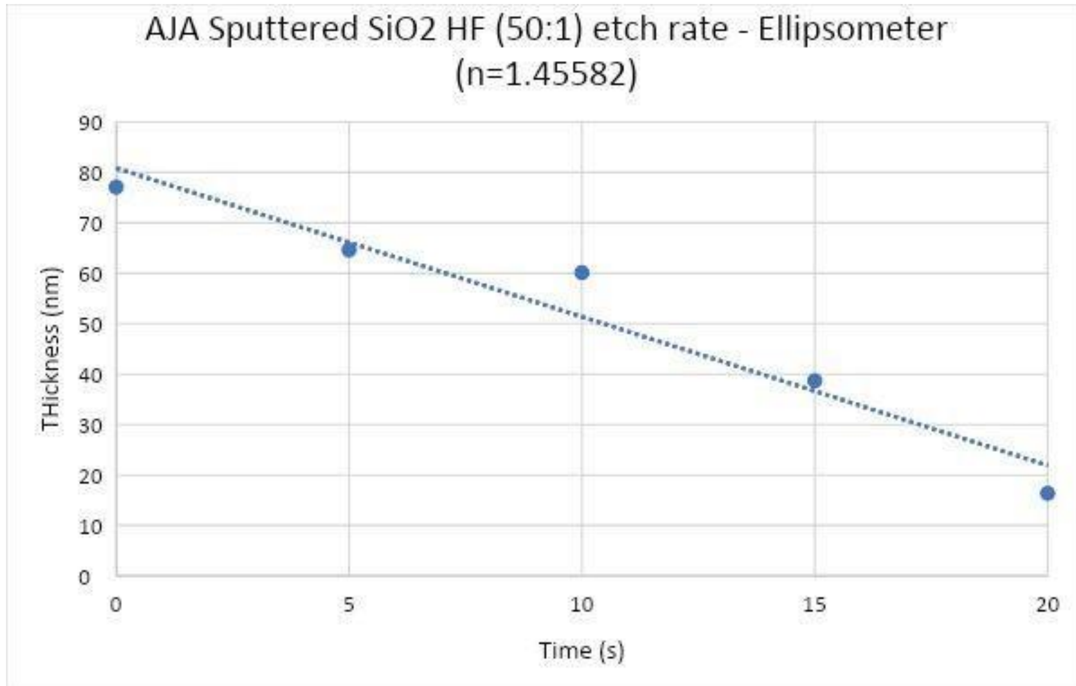

Figure 11: AJA Sputter SiO2 HF (50:1) Etch Rate (Ellipsometer)

Gaertner Ellipsometer measurements showed that the HF (50:1) etch rate for AJA Sputtered SiO_2 was 2.9 nm/s.

CHA Electron Beam Evaporator SiO_2:

A film of silicon dioxide was deposited by electron beam evaporation on CHA E-Beam Evaporator. The film was then etched with hydrofluoric acid (50:1) in four incremental steps of 30 seconds until a total etch time of 120 seconds was reached. The refractive index of the deposited film was determined using Metricon 2010/M Prism Coupler and this refractive index was used to establish film thicknesses on Gaertner Ellipsometer and Ocean Optics Reflectometer. These

thickness measurements were then plotted to obtain the etch rate for the film.

Film Properties

Deposition temperature: Room temperature

Deposition rate: 0.015 nm/s

Nominal deposition thickness: 1000 nm

	Metricon 2010/M Prism Coupler				
Time (s)	0	30	60	90	120
Thickness (nm)	1205.5	1113.5	1001.0	877.4	731.6
Refractive Index	1.4574	1.4571	1.4561	1.4546	1.4539

Table 7: Metricon measurements CHA E-Beam SiO2

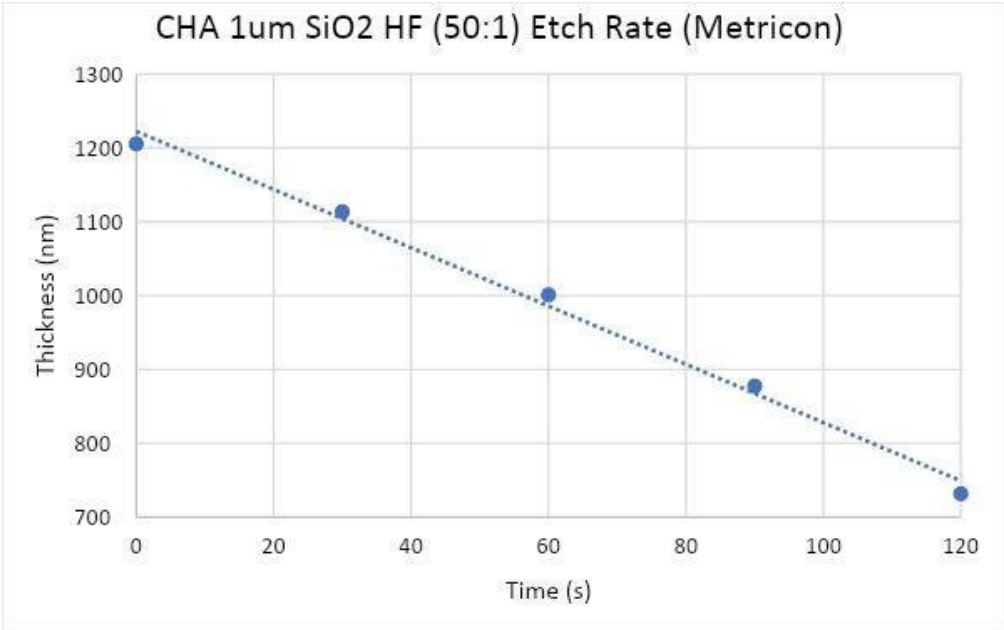

Figure 12: CHA E-Beam SiO2 HF (50:1) Etch Rate (Metricon)

Metricon thickness measurements gave an HF (50:1) etch rate of 3.9 nm/s.

	Gaertner Ellipsometer				
Time (s)	0	30	60	90	120
Thickness (nm)	1244.5	1186.1	1073.7	964.7	754.3
Refractive Index	1.4574	1.4571	1.4561	1.4546	1.4539

Table 8: Ellipsometer measurements CHA E-Beam SiO2

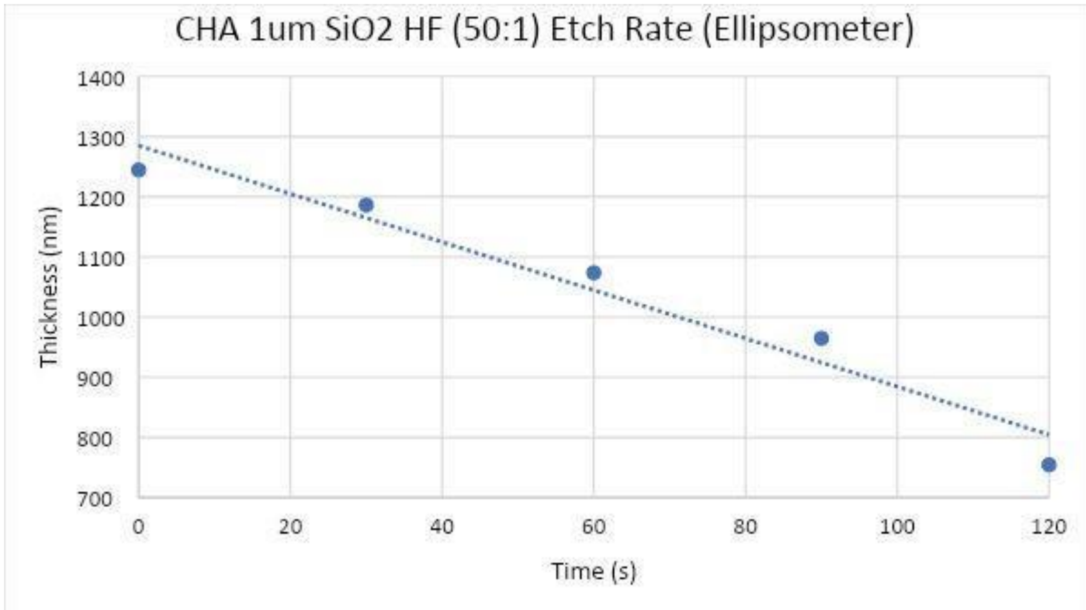

Figure 13: CHA E-Beam SiO2 HF (50:1) Etch Rate (Ellipsometer)

Gaertner Ellipsometer thickness measurements indicate an HF (50:1) etch rate of 4.0 nm/s.

	Ocean Optics Reflectometer				
Time (s)	0	30	60	90	120
Thickness (nm)	1254.5	1173.9	1104.2	708.4	733.8
Refractive Index	1.4668	1.4668	1.4668	1.4668	1.4668

Table 9: Reflectometer measurements CHA E-Beam SiO2

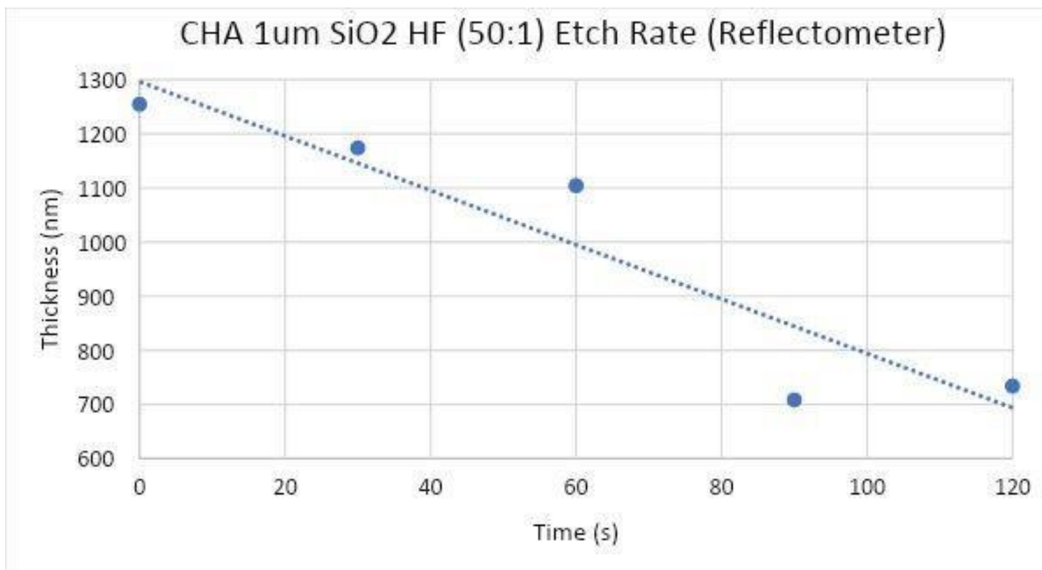

Figure 14: CHA E-Beam SiO2 HF (50:1) Etch Rate (Reflectometer)

Ocean Optics Reflectometer thickness measurements established an HF (50:1) etch rate of 5.0nm/s.

Plasma Enhanced Chemical Vapor Deposition (PECVD) SiO_2:

The hydrofluoric acid etch rate for a film of silicon dioxide grown using PECVD

process was determined by growing a film of nominal thickness 650 nm, establishing its refractive index using Metricon 2010/M Prism Coupler and subjecting the film to etching by immersion in a solution of hydrofluoric acid (50:1). Four incremental etch durations were used and the thickness of the film

was measured at five different spots on the wafer on an Ocean Optics Reflectometer and a Gaertner Ellipsometer. This etch experiment showed that PECVD silicon dioxide was etched at a significantly slower rate. So, these films were incorporated in fabrication steps requiring high quality silicon dioxide as well as device layers needed to be etched at very slow rates.

Film Properties/Recipe

TRION PECVD		
Step 1 (Passivation)	**Step 2 (Growth)**	**Step 3 (N_2 Purge)**
ICP Power: 0 W	ICP Power: 500 W	ICP Power: 0 W
Pressure: 1000 mTorr	Reflected Power Tolerance: 10 W	Pressure: 250 mTorr
N_2O: 179 sccm	Pressure: 1000 mTorr	N_2: 250 sccm
N_2: 250 sccm	N_2O: 179 sccm	Temperature: 380°C
SiH_4/Ar: 10 sccm	N_2: 250 sccm	Time: 180 s
Temperature: 250°C	SiH_4/Ar: 10 sccm	
Time: 1200 s	Temperature: 380°C	
	RF Stabilization Time: 10s	
	Time: 2700 s	

Table 10: PECVD SiO2 Film Deposition Recipe

Metricon Measurements		
	Refractive Index	**Thickness (nm)**
Measurement 1	1.4654	643.5
Measurement 2	1.4656	597.1
Measurement 3	1.4658	602.0
Average	*1.4656*	*614.2*
Standard deviation	*0.0002*	*25.5*

Table 11: PECVD SiO2 Refractive index and Film thickness measurements (Metricon)

Metricon 2010/M Prism Coupler established a refractive index of 1.4656 for PECVD SiO_2. This refractive index provided a basis for the recipes created on Gaertner Ellipsometer and Ocean Optics Reflectometer for subsequent measurements of this dielectric film.

Ellipsometer (n = 1.4656)					
Time (s)	0	60	300	610	1200
Thickness 1 (nm)	655.9	641.6	611.7	558.0	476.4

Thickness 2 (nm)	672.4	660.7	626.3	558.8	481.8
Thickness 3 (nm)	668.5	652.8	620.9	568.7	473.3
Thickness 4 (nm)	661.6	648.1	619.3	567.6	490.8
Thickness 5 (nm)	656.1	647.8	612.7	563.3	492.0
Average Thickness (nm)	662.9	650.2	618.2	563.3	482.9
Standard Deviation	7.4	7.1	6.1	4.9	8.3

Table 12: Ellipsometer measurements HF (50:1) etch of PECVD SiO2

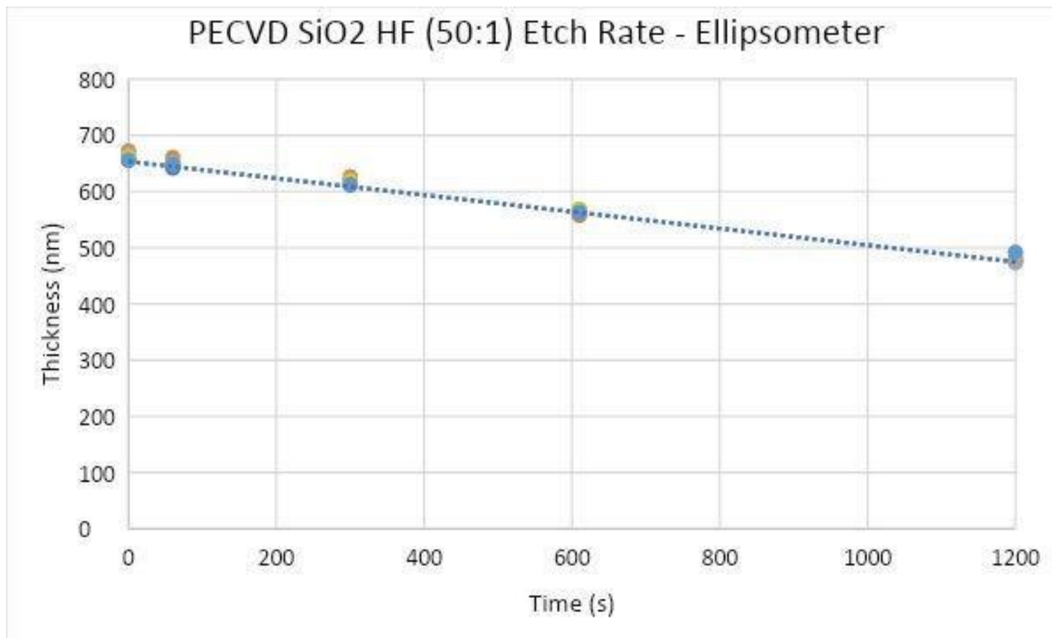

Figure 15: PECVD SiO2 HF (50:1) Etch Rate (Ellipsometer)

Gaertner Ellipsometer thickness measurements indicated an HF (50:1) etch rate of 0.15 nm/s.

Reflectometer (n = 1.4656)					
Time (s)	0	60	300	610	1200
Thickness 1 (nm)	665.4	651.6	614.2	564.1	477.5
Thickness 2 (nm)	666.8	659.9	614.3	565.1	477.6
Thickness 3 (nm)	664.8	658.5	615.0	565.3	481.5
Thickness 4 (nm)	679.3	661.5	626.7	575.0	485.6
Thickness 5 (nm)	676.2	650.6	626.0	573.2	478.2
Average Thickness (nm)	670.5	656.4	619.2	568.5	480.1
Standard Deviation	6.7	4.9	6.5	5.1	3.5

Table 13: Reflectometer measurements HF (50:1) etch of PECVD SiO2

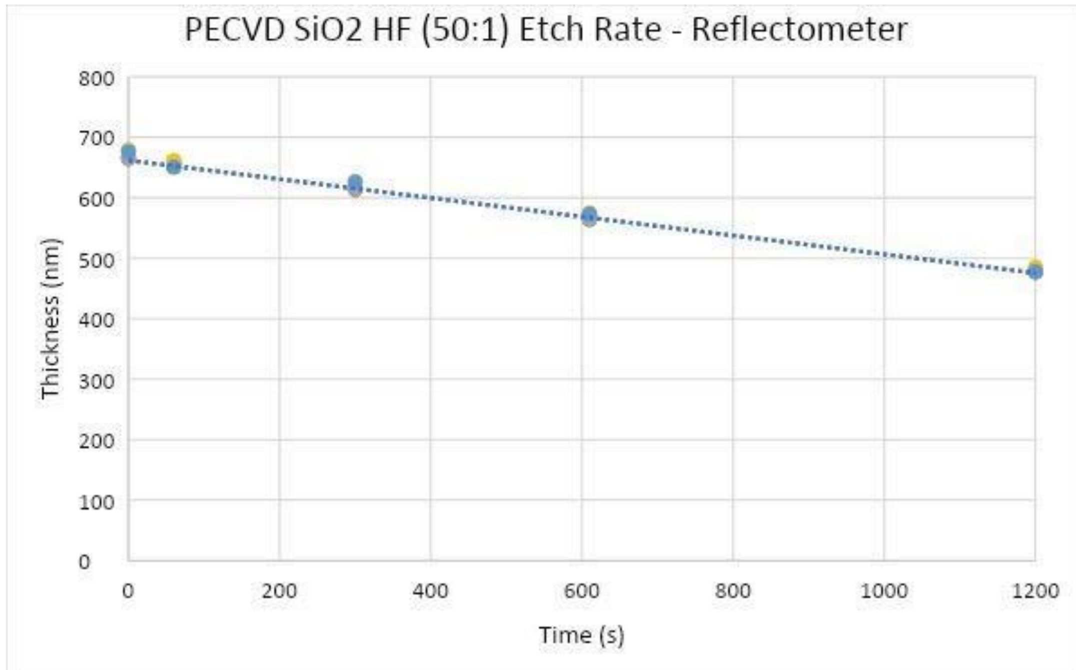

Figure 16: PECVD SiO2 HF (50:1) Etch Rate (Reflectometer)

Gaertner Ellipsometer thickness measurements indicated an HF (50:1) etch rate of

0.16 nm/s.

4.2.1.2 Reactive Ion etching

Given the isotropic nature of wet chemical etching, dry etching of dielectrics, in our case, silicon dioxide was preferred for various stages in the fabrication process since dry etching offered the possibility of more anisotropic (somewhat directional) etching. The dry etching mechanism employed for this was Reactive Ion Etching. This was carried out on a Technics Macro RIE 8800 tool in the Nanotechnology Research Center Cleanroom at the University of Texas at Arlington.

Reactive Ion Etching (RIE) was done on films of silicon dioxide obtained from electron beam evaporation (AJA E-Beam Evaporator) and Plasma-Enhanced Chemical Vapor Deposition (PECVD). Additionally, some RIE etch steps had to be carried out on substrates selectively protected with negative photoresist (NR9-1000PY) hence it was crucial to establish the rate at which the photoresist was being etched off even though it may not have been the target layer being etched. Also, etch experiments were carried out for Planarization Photoresist (PC3-700) for the initial mask process flow to prevent exposure of underlying device features during reactive ion etching steps.

AJA Electron Beam Evaporator SiO_2:

Film Properties

Deposition temperature: 200°C

Deposition rate: 0.01 – 0.015 nm

Nominal deposition thickness: 1000 nm

Reactive Ion Etching Recipe (Technics Macro RIE 8800)

Power: 600 W

Pressure: 160 mTorr

CF_4: 30 sccm

O_2: 3.6 sccm

	Metricon 2010/M Prism Coupler				
Time (s)	0	30	60	90	120
Thickness (nm)	1075.1	1021.6	955.9	923.2	893.5
Refractive Index	1.4654	1.4630	1.4641	1.4680	1.4632

Table 14: Metricon measurements AJA E-Beam SiO2

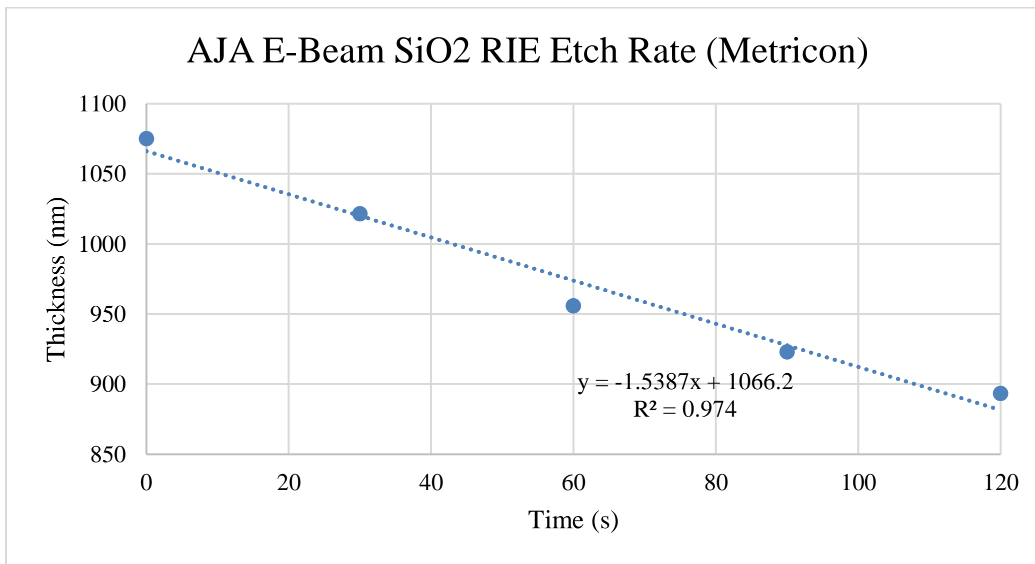

Figure 17: AJA E-Beam SiO2 RIE Etch Rate (Metricon)

Metricon measurements indicated a Reactive Ion Etch rate of 1.5 nm/s.

	Gaertner Ellipsometer				
Time (s)	0	30	60	90	120
Thickness (nm)	1155.5	1101.5	1065.6	982.9	939.1
Refractive Index	1.4654	1.4630	1.4641	1.4680	1.4632

Table 15: Ellipsometer measurements AJA E-Beam SiO2

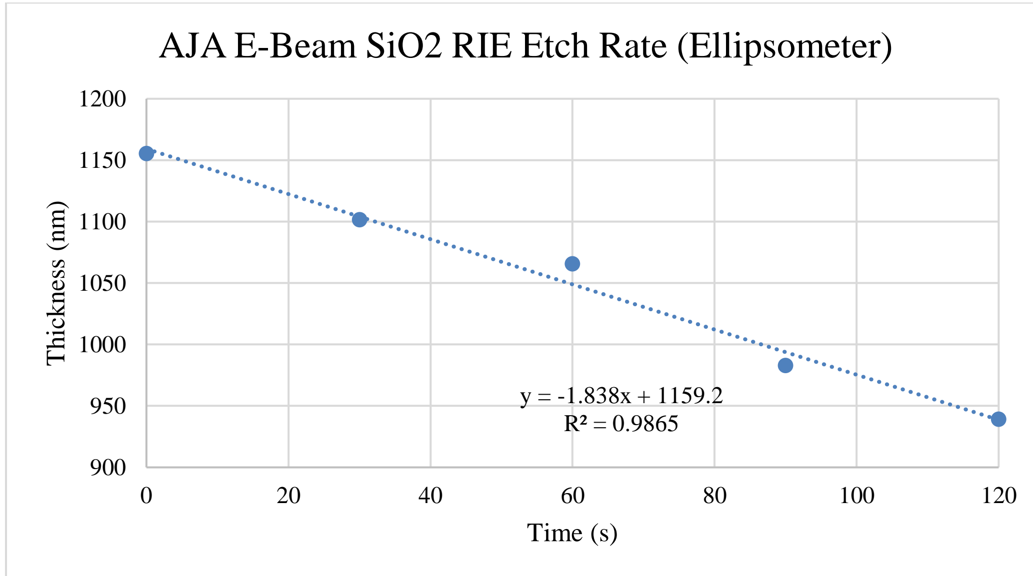

Figure 18: AJA E-Beam SiO2 RIE Etch Rate (Ellipsometer)

Ellipsometer measurements showed a Reactive Ion Etch rate of 1.8 nm/s for AJA E-Beam SiO_2

	Ocean Optics Reflectometer				
Time (s)	0	30	60	90	120
Thickness (nm)	1154.1	1087.1	1047.3	998.1	893.5
Refractive Index	1.4668	1.4668	1.4668	1.4668	1.4668

Table 16: Reflectometer measurements AJA E-Beam SiO2

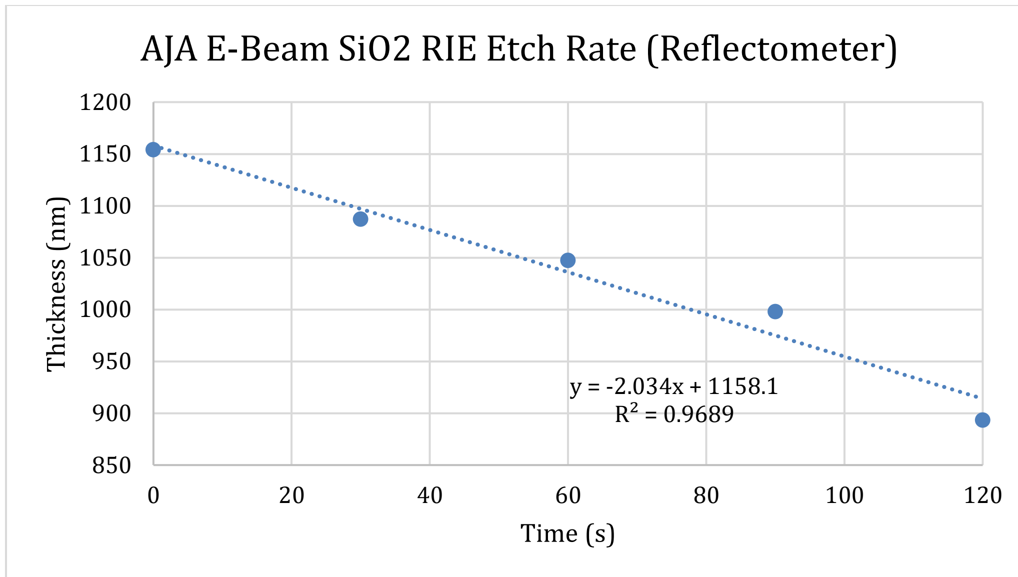

Figure 19: AJA E-Beam SiO2 RIE Etch Rate (Reflectometer)

Ocean Optics Reflectometer measurements indicated that the Reactive Ion Etch rate for AJA E-Beam SiO_2 was 2.0 nm/s.

Plasma Enhanced Chemical Vapor Deposition (PECVD) SiO_2:

The reactive ion etch rate of a film of silicon dioxide, with nominal thickness of 600 nm, grown using TRION PECVD was determined by obtaining the refractive index of the as-grown film on Metricon 2010/M Prism Coupler prior to etching the film in incremental steps. Refractive index measurements yielded only one reflection mode, as a result average from thicker PECVD silicon dioxide films was used. For each etch step, the silicon dioxide film was measured on two tools: Ocean Optics Reflectometer and Gaertner Ellipsometer.

Film Properties/Recipe

TRION PECVD		
Step 1 (Passivation)	**Step 2 (Growth)**	**Step 3 (N_2 Purge)**
ICP Power: 0 W	ICP Power: 500 W	ICP Power: 0 W
Pressure: 1000 mTorr	Reflected Power Tolerance: 10 W	Pressure: 250 mTorr
N_2O: 179 sccm	Pressure: 1000 mTorr	N_2: 250 sccm
N_2: 250 sccm	N_2O: 179 sccm	Temperature: 380°C
SiH_4/Ar: 10 sccm	N_2: 250 sccm	Time: 180 s
Temperature: 250°C	SiH_4/Ar: 10 sccm	
Time: 1200 s	Temperature: 380°C	
	RF Stabilization Time: 10s	
	Time: 2700 s	

Table 17: PECVD SiO2 Film Deposition Recipe

Metricon Measurements		
	Refractive Index	**Thickness (nm)**
Measurement 1	1.4656	588.5
Measurement 2	1.4656	594.2
Measurement 3	1.4656	591.4
Average	*1.4656*	*591.4*
Standard deviation	*0*	*2.9*

Table 18: PECVD SiO2 Refractive index and Film thickness measurements (Metricon)

Reactive Ion Etching Recipe (Technics Macro RIE 8800)

Power: 600 W

Pressure: 160 mTorr

CF_4 : 30 sccm

O_2 : 3.6 sccm

Ellipsometer (n = 1.4656)					
Time (s)	0	120	300	600	720
Thickness 1 (nm)	666.9	580.9	462.6	272.8	165.3
Thickness 2 (nm)	667.9	585.9	463.5	270.4	158.8
Thickness 3 (nm)	690.9	592.1	479.9	275.1	156.6
Thickness 4 (nm)	691.1	587.9	466.6	267.3	150.6
Thickness 5 (nm)	691.5	583.7	451.8	260.1	156.8
Average Thickness (nm)	681.7	586.1	464.9	269.2	157.6
Standard Deviation	13.0	4.2	10.1	5.8	5.3

Table 19: Ellipsometer measurements RIE etch of PECVD SiO2

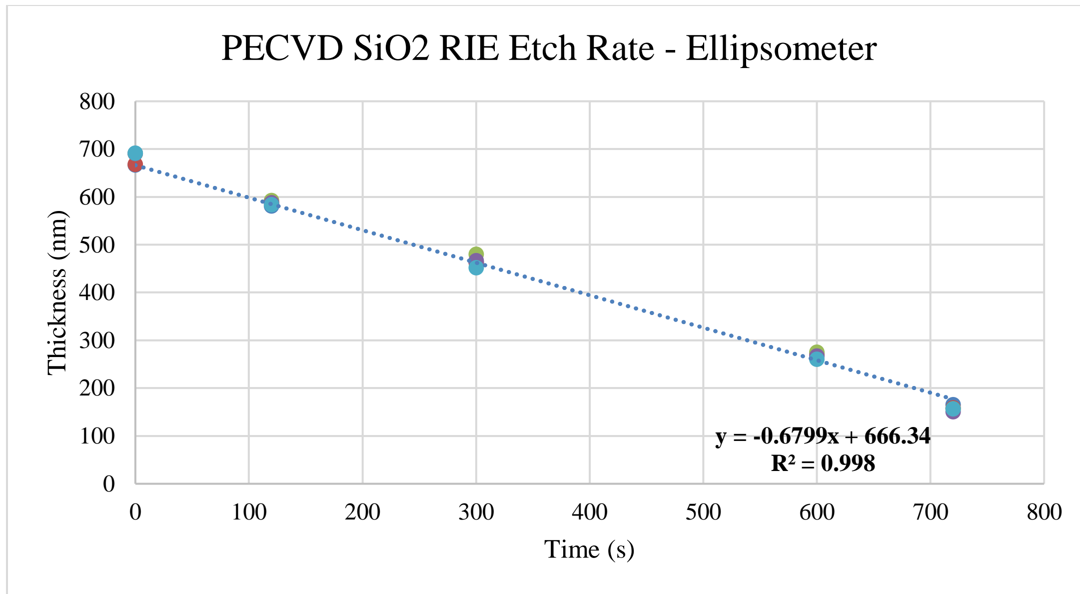

Figure 20: PECVD SiO2 RIE Etch Rate (Ellipsometer)

Gaertner Ellipsometer thickness measurements for PECVD silicon dioxide indicated an RIE etch rate of 0.68 nm/s.

Reflectometer (n = 1.4656)					
Time (s)	0	120	300	600	720
Thickness 1 (nm)	675.7	589.1	469.2	268.9	167.6
Thickness 2 (nm)	673.5	591.8	469.8	260.1	162.9
Thickness 3 (nm)	680.3	588.5	479.7	261.3	150.2
Thickness 4 (nm)	693.5	596.4	472.9	265.9	156.2
Thickness 5 (nm)	680.9	599.8	461.4	256.5	153.9
Average Thickness (nm)	680.8	593.1	470.6	262.5	158.2
Standard Deviation	7.8	4.9	6.6	4.9	7.0

Table 20: Reflectometer measurements RIE etch of PECVD SiO2

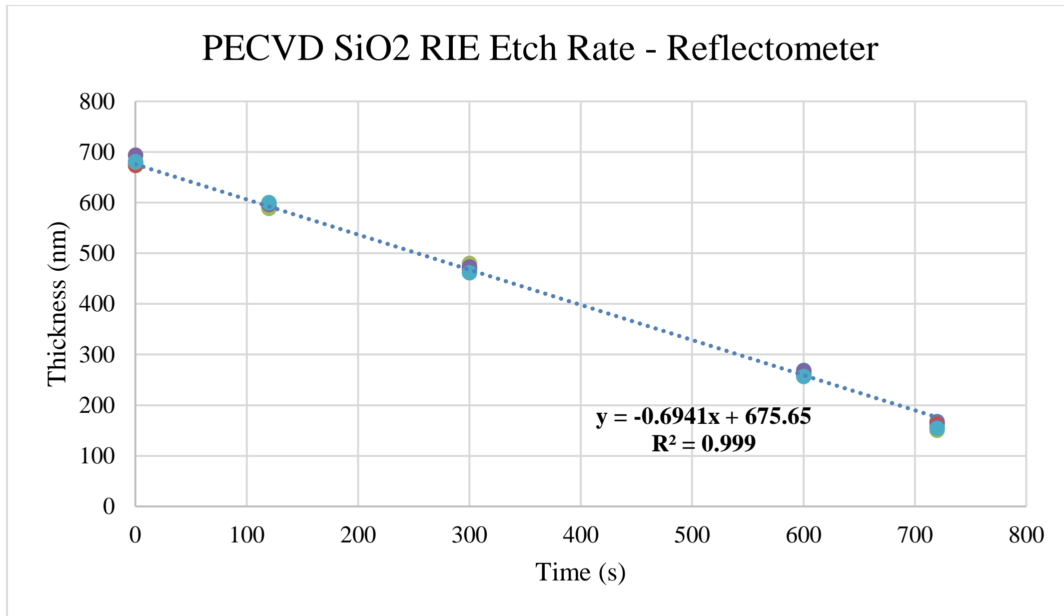

Figure 21: PECVD SiO2 RIE Etch Rate (Reflectometer)

Ocean Optics Reflectometer thickness measurements showed that the Reactive

Ion Etch rate for PECVD SiO_2 was 0.69 nm/s.

Planarization Photoresist PC3-700:

The fabrication process involves using planarization photoresist to protect devices contacts and regions when selectively etching silicon dioxide. Hence, it was important to determine the etch rate of this protective photoresist layer during the etch process to prevent over-etching and the unintended consequence of damaging underlying device features.

Film Properties (Spin Coating)

Step 1:

Speed – 800 rpm

Ramp – 100 rpm/s

Time – 80 s

Step 2:

Speed – 0 rpm

Ramp – 100 rpm/s

Time – 0.1 s

Nominal thickness: 1500nm

Reactive Ion Etching Recipe (Technics Macro RIE 8800)

Power: 350 W

Pressure: 200 mTorr

O_2: 11 sccm

Metricon Measurements				
Time (s)	0	100	300	600
Thickness 1 (nm)	1639.9	1472.2	1201.9	819.3
Thickness 2 (nm)	1597.1	1467.7	1180.0	807.0
Thickness 3 (nm)	1625.5	1513.2	1179.2	791.0
Average Thickness (nm)	1620.8	1484.4	1187.0	805.8

Table 21: Metricon measurements RIE etch for PC3-700 Planarization Photoresist

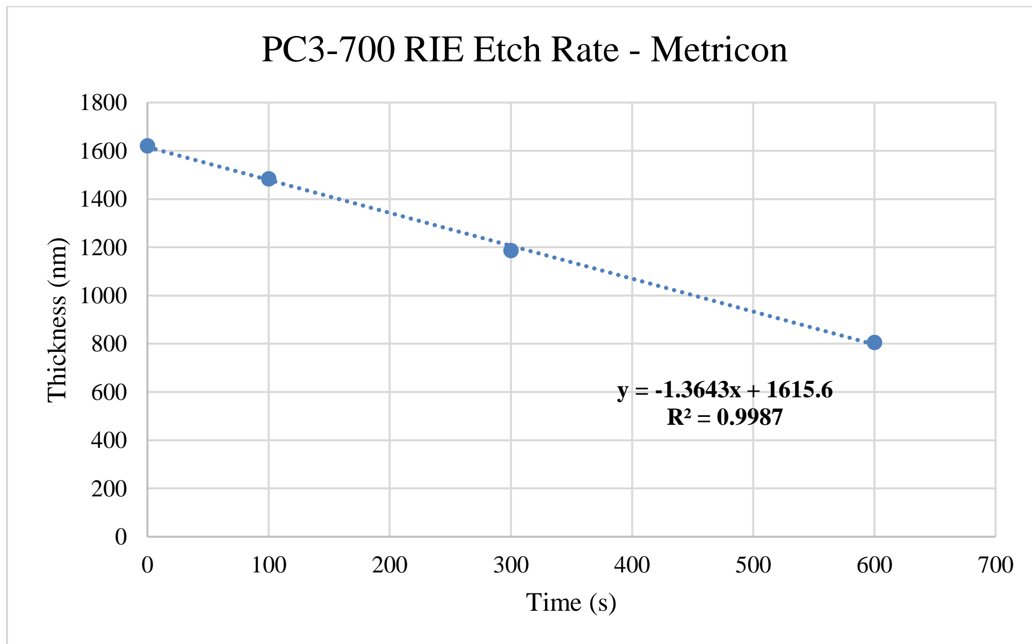

Figure 22: PC3-700 Planarization Photoresist RIE Etch Rate (Metricon)

Metricon thickness measurements showed that the Reactive Ion Etch rate for PC3-700 Planarization Photoresist was 1.36 nm/s.

Ellipsometer Measurements				
Time (s)	0	100	300	600
Thickness 1 (nm)	1690.6	1531.3	1219.8	815.7
Thickness 2 (nm)	1693.6	1532.9	1225.4	809.0
Thickness 3 (nm)	1686.9	1523.7	1216.1	799.0
Average Thickness (nm)	1690.4	1529.3	1220.4	807.9

Table 22: Ellipsometer measurements RIE etch for PC3-700 Planarization Photoresist

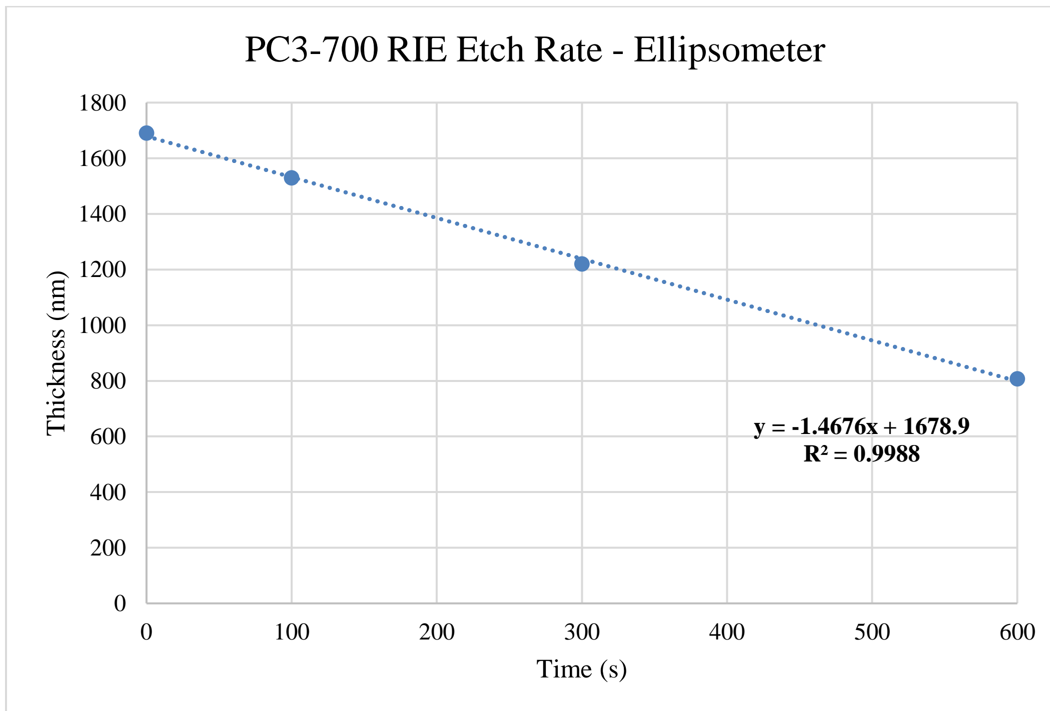

Figure 23: PC3-700 Planarization Photoresist RIE Etch Rate (Ellipsometer)

Ellipsometer thickness measurements resulted in a Reactive Ion Etch rate for PC3-700 Planarization Photoresist of 1.47 nm/s.

NR9-1000PY Negative Photoresist Argon Sputter Etch Rate:

Several reactive ion etching steps were carried out immediately after photolithography and development of samples. To monitor the etch margins safe for these processes, experiments were carried out to determine the etch rate of NR9-1000PY negative photoresist films. The thicknesses of the photoresist films were measured using Metricon 2010/M Prism Coupler and Gaertner Ellipsometer. These measurements provided information on etch rates so that etch times for the processing steps would not result in total erosion of the protective negative
photoresist films.

Film Properties **Spin Coating:**

Step 1:

Speed – 500 rpm

Ramp – 100 rpm/s Time – 5 s *Step 2:*

Speed – 3000 rpm

Ramp – 1000 rpm/s Time – 60 s *Step 3:*

Speed – 0 rpm

Ramp – 1000 rpm/s

Time – 0.1 s

Pre-Exposure Bake

Temperature: 150°C

Time: 60 s

OAI Aligner Exposure and Development

Vacuum Contact Mode

Substrate Chuck current: 14 mA

Measured UV Lamp Intensity: 17.7 mW/cm^2

Exposure Dose: 120 mJ/cm^2

Exposure time: 6.8 s

Post-Exposure Bake

Temperature: 100°C

Time: 60 s

Development

RD6 Developer: 10 s

Deionized water rinse: 600 s (water bath was changed every 150 s)

Nominal thickness: 1000 nm

Reactive Ion Etching Recipe (Technics Macro RIE 8800)

Power: 600 W

Pressure: 150 mTorr

Ar: 25 sccm

Metricon measurements			
Time (s)	0	300	600
Thickness 1 (nm)	1022.7	790.4	589.2
Thickness 2 (nm)	1025.5	774.2	581.5
Thickness 3 (nm)	1032.1	764.7	599.1
Average Thickness (nm)	1026.8	776.4	589.9

Table 23: Metricon measurements Argon RIE etch for NR9-1000PY Negative Photoresist

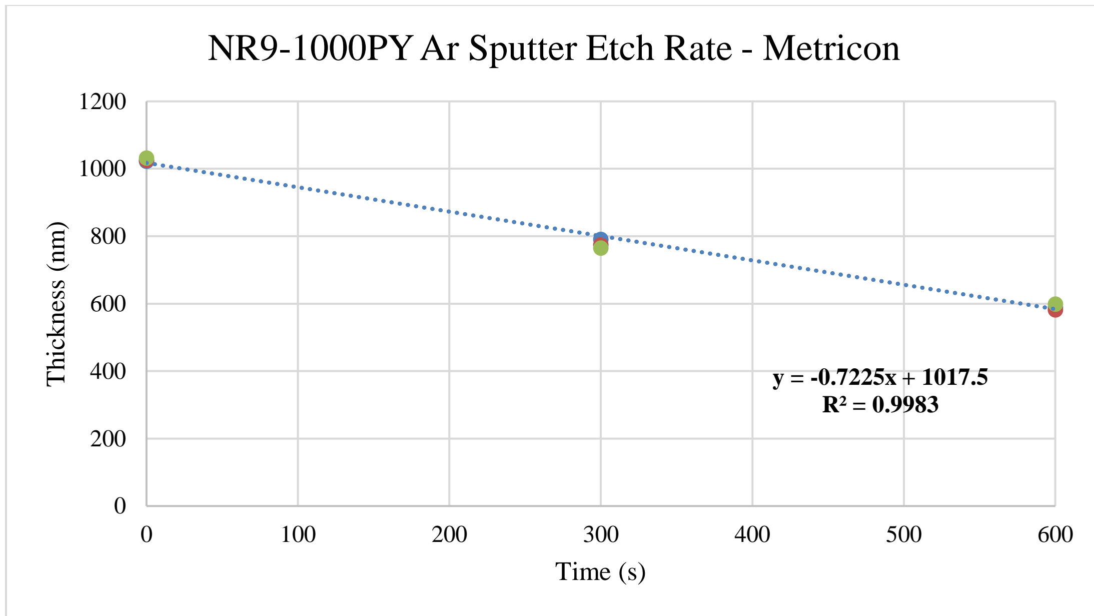

Figure 24: NR9-1000PY Negative Photoresist Argon RIE Etch Rate (Metricon)

Metricon thickness measurements indicated that the Argon Reactive Ion Etch rate for NR9-1000PY Negative Photoresist was 0.72 nm/s.

Ellipsometer measurements			
Time (s)	0	300	600
Thickness 1 (nm)	1060.37	822.4	604.2
Thickness 2 (nm)	1060.25	822.1	597.3
Thickness 3 (nm)	1047.3	808.6	597.6
Thickness 4 (nm)	1049.0	804.9	594.4
Thickness 5 (nm)	1058.9	805.1	596.2
Average Thickness (nm)	1055.2	812.6	597.9
Standard deviation	6.5	8.9	3.7

Table 24: Ellipsometer measurements Argon RIE etch for NR9-1000PY Negative Photoresist

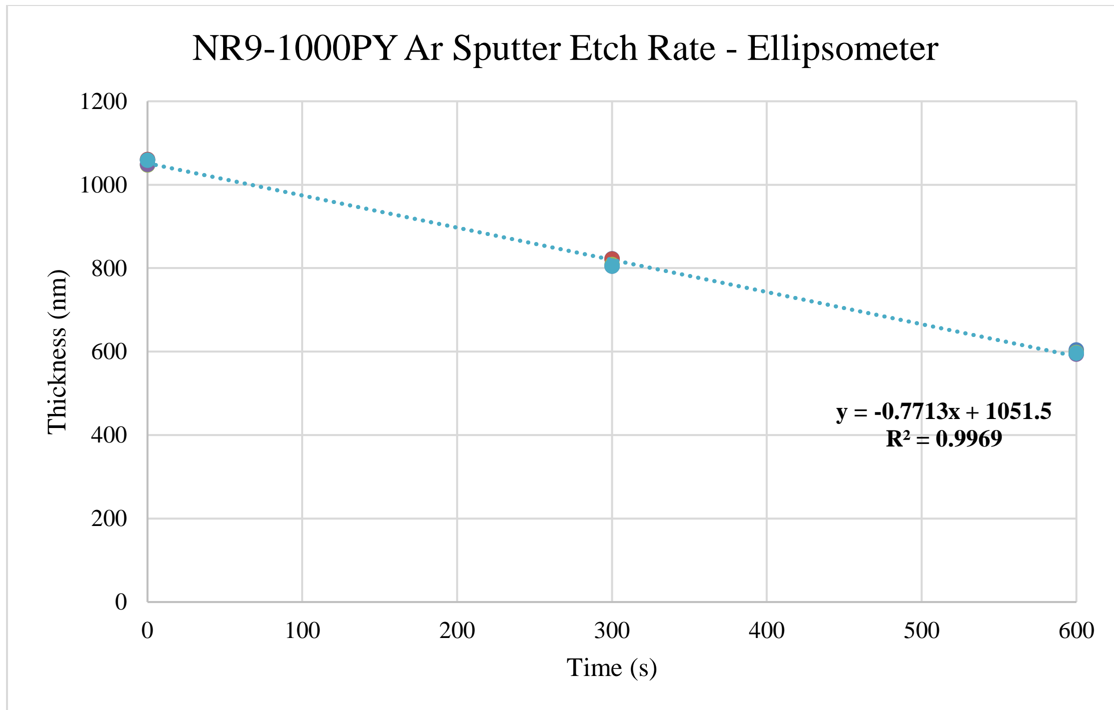

Figure 25: NR9-1000PY Negative Photoresist Argon RIE Etch Rate (Ellipsometer)

Ellipsometer thickness measurements indicated that the Reactive Ion Etch rate for NR9-1000PY Negative Photoresist was 0.77 nm/s.

NR9-1000PY Negative Photoresist Tetrafluoromethane-oxygen (CF_4/O_2) Etch Rate:

Reactive Ion Etching Recipe (Technics Macro RIE 8800)

Power: 600 W

Pressure: 150 mTorr

CF_4: 30 sccm

O_2: 3.6 sccm

Metricon measurements			
Time (s)	0	120	300
Thickness 1 (nm)	1010.1	798.1	531.4
Thickness 2 (nm)	1008.7	800.1	536.6
Thickness 3 (nm)	1008.0	801.1	534.6
Average Thickness (nm)	1008.9	799.8	534.2

Table 25: Metricon measurements CF4/O2 RIE etch for NR9-1000PY Negative Photoresist

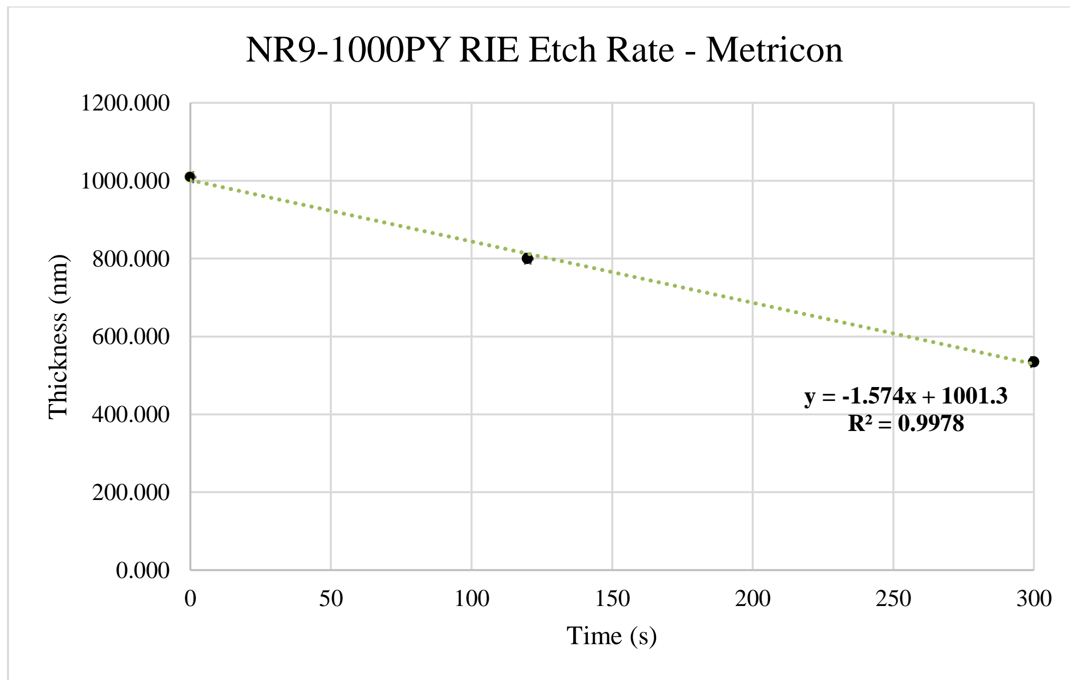

Figure 26: NR9-1000PY Negative Photoresist CF4/O2 RIE Etch Rate (Metricon)

Metricon thickness measurements indicated that the CF_4/O_2 Reactive Ion Etch rate for NR9-1000PY Negative Photoresist was 1.57 nm/s.

Ellipsometer measurements			
Time (s)	0	120	300
Thickness 1 (nm)	1064.7	842.4	587.5
Thickness 2 (nm)	1065.3	839.3	555.8
Thickness 3 (nm)	1062.4	836.5	568.6
Thickness 4 (nm)	1064.1	837.2	582.5
Thickness 5 (nm)	1063.9	838.9	573.6
Average Thickness (nm)	1064.1	838.8	573.6
Standard deviation	1.1	2.3	12.4

Table 26: Ellipsometer measurements CF4/O2 RIE etch for NR9-1000PY Negative Photoresist

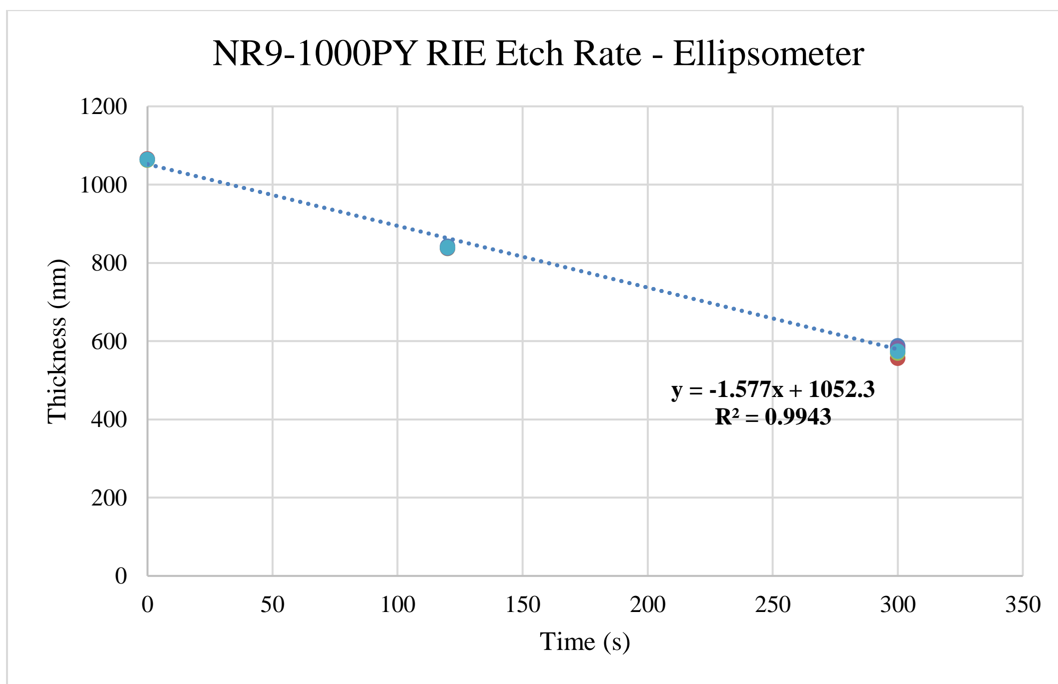

Figure 27: NR9-1000PY Negative Photoresist CF4/O2 RIE Etch Rate (Ellipsometer)

Ellipsometer thickness measurements indicated that the CF_4/O_2 Reactive Ion Etch rate for NR9-1000PY Negative Photoresist was 1.58 nm/s.

NR9-1000PY Negative Photoresist Oxygen (O_2) Plasma Etch Rate:

Reactive Ion Etching Recipe (Technics Macro RIE 8800)

Power: 600 W

Pressure: 150 mTorr

O_2: 11 sccm

Metricon measurements			
Time (s)	0	90	240
Thickness 1 (nm)	1014.3	892.2	689.9
Thickness 2 (nm)	1027.1	902.4	696.8
Thickness 3 (nm)	1035.0	899.9	684.5
Average Thickness (nm)	1025.5	898.2	690.4
Standard deviation	10.4	5.3	6.2

Table 27: Metricon measurements O2 Plasma RIE etch for NR9-1000PY Negative Photoresist

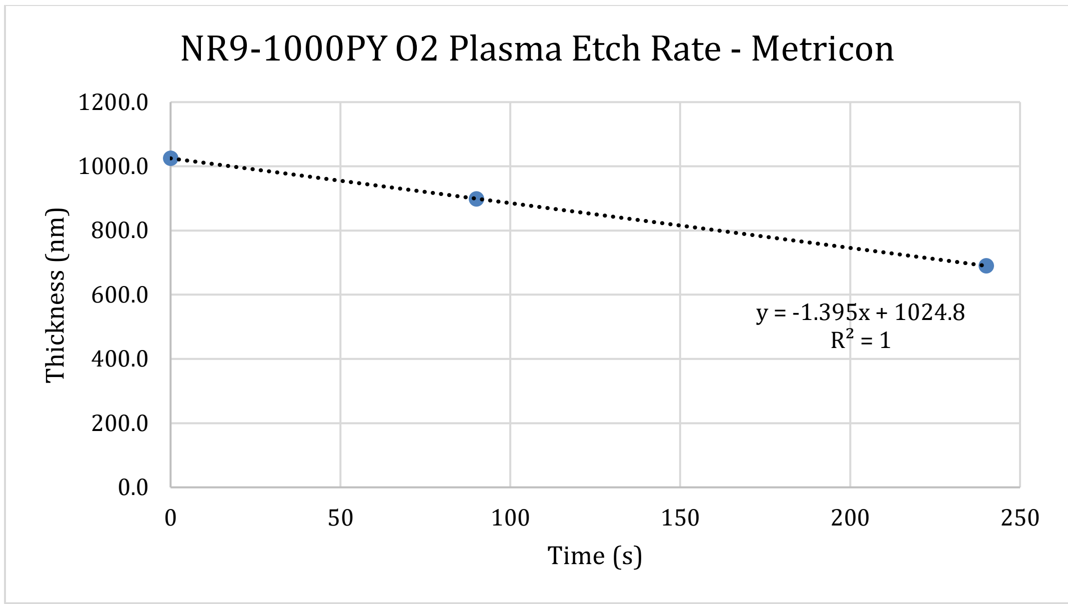

Figure 28: NR9-1000PY Negative Photoresist O2 Plasma RIE Etch Rate (Metricon)

Metricon 2010/M Prism Coupler thickness measurements showed that the O_2 Plasma Reactive Ion Etch rate for NR9-1000PY Negative Photoresist was 1.40nm/s.

Ellipsometer measurements			
Time (s)	0	90	240
Thickness 1 (nm)	1014.3	892.2	689.9
Thickness 2 (nm)	1027.1	902.4	696.8
Thickness 3 (nm)	1035.0	899.9	684.5
Average Thickness (nm)	1025.5	898.2	690.4
Standard deviation	10.4	5.3	6.2

Table 28: Ellipsometer measurements O2 Plasma RIE etch for NR9-1000PY Negative Photoresist

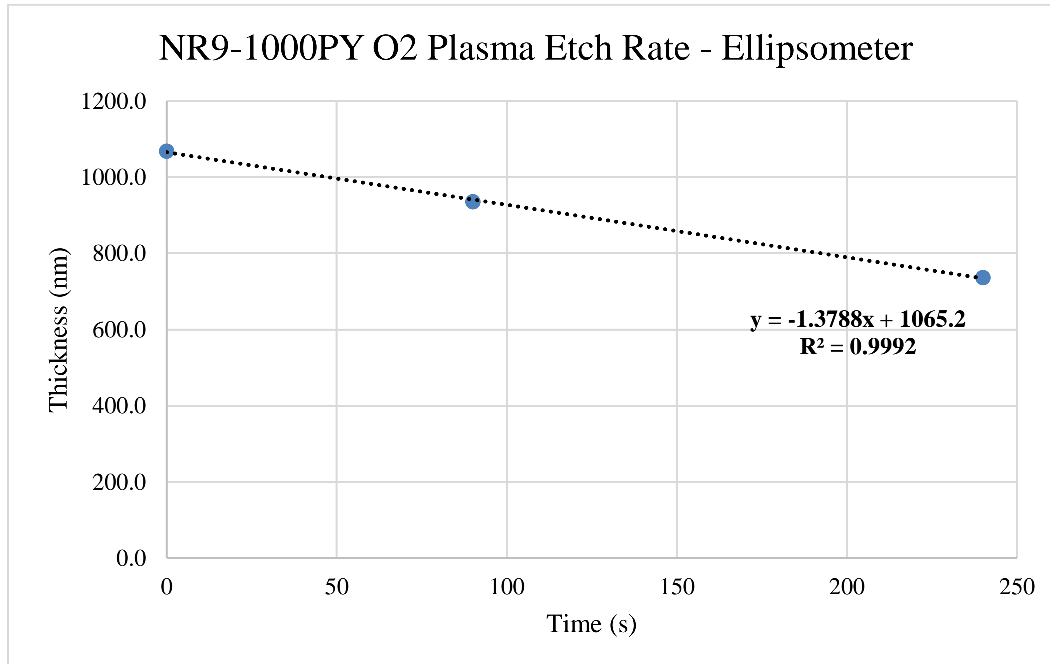

Figure 29: NR9-1000PY Negative Photoresist O2 Plasma RIE Etch Rate (Ellipsometer)

Gaertner Ellipsometer thickness measurements showed that the O_2 Plasma Reactive Ion Etch rate for NR9-1000PY Negative Photoresist was 1.38 nm/s.

4.3 Electrical Characterization

Once device fabrication is complete IV measurement for device was done. Electrical characterization was done with an Agilent 4155C Parameter Analyzer. The parameter analyzer system is connected to a probe station having 3 probes individually controlled by SMUs in the analyzer.

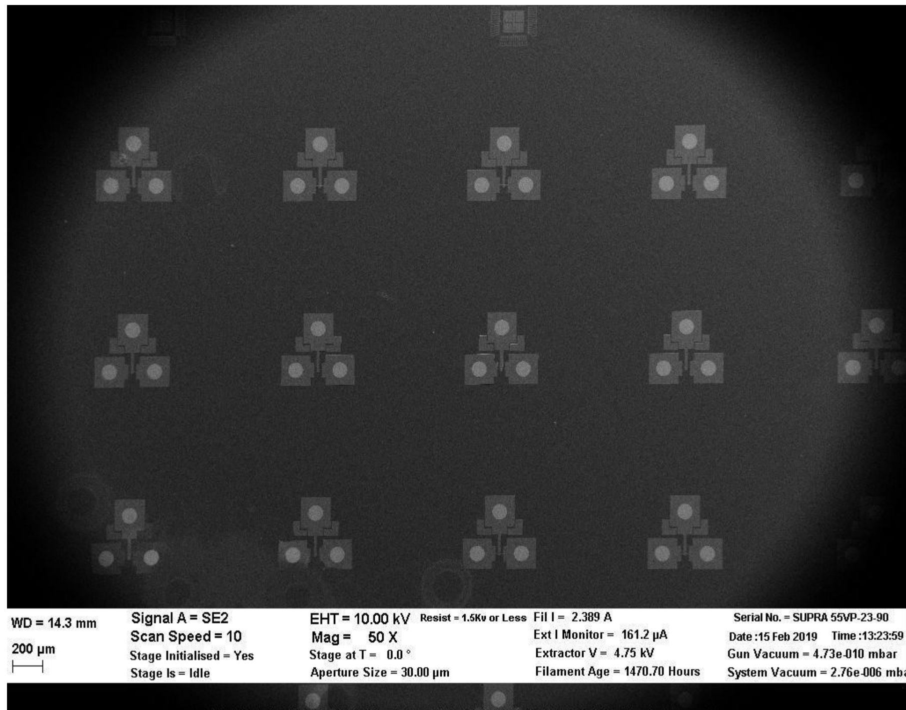

Figure 30: SEM image of Array of fully fabricated transistors

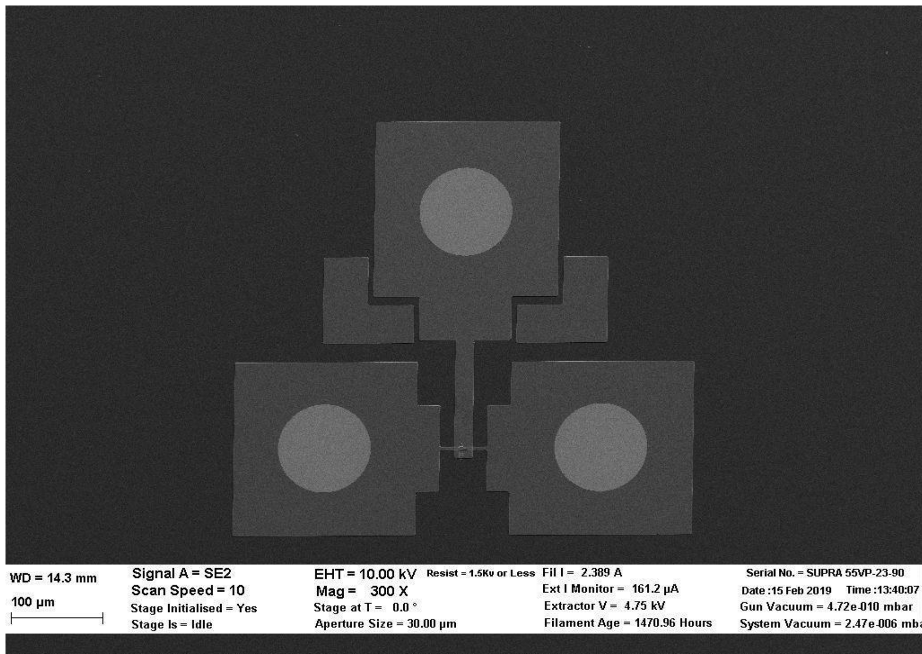

Figure 31: SEM image of Single Transistor Device: Courtesy Pushkar Gothe

Generally, each device is measured in three steps:

- Contact IV measurements for source, drain and gate contact pads
- Source-Drain IV measurement
- Gate modulation measurement (ie. source, drain and gate biasing)

Earlier measurements gave low contact IV data hinting at bad current flow from probe tips to contact pads. Several reactive ion etching recipes were explored to clean contact pads. We found that Ar sputter cleaning for 30s – 60s was sufficient to remove thin nickel oxide of few nanometers (1-3nm) that may have formed on the contact pads upon exposure to air.

For source-drain IV measurements, contact was established between probe tips and source and drain contact pads. The biasing was carried out such that, the source was held at a fixed voltage of 0V while the drain was swept from 0V to 2.5V or 0V to 5V. Sample A source-drain IV measurement exhibited transistor characteristic at 0V gate bias. In the case of sample B, the tunneling barrier ensured that only electrons having favorable energy could tunnel across the barrier and contribute to electronic transport. For sample C, the presence of an energy filter in addition to the tunneling barrier should lead to cooling of thermally excited electrons.

The array of devices fabricated is as shown in the figure below. We varied source and drain contact area as well as gate length in order to study their influence on source-drain current.

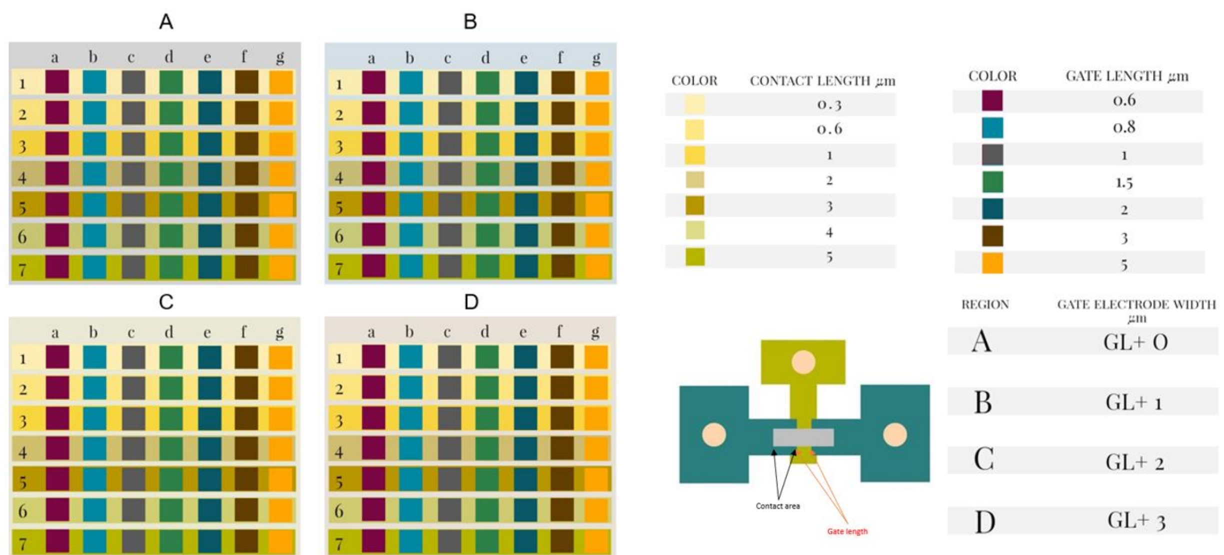

Figure 32: Photolithography mask layout showing variation in gate length and contact area

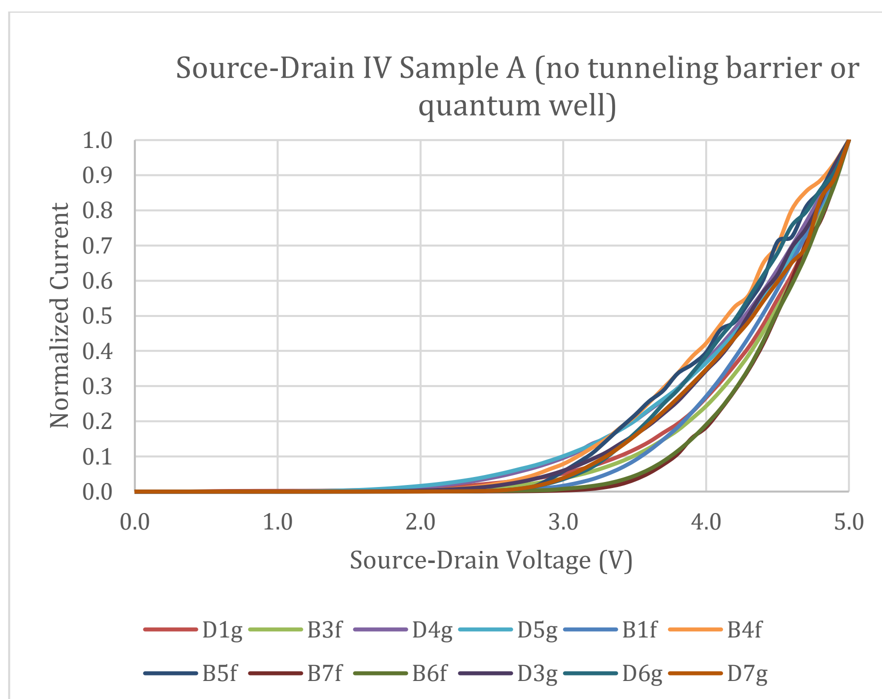

Figure 33: Normalized source-drain IV for sample with no tunneling barrier and no energy filter

The figure above shows normalized source-drain current for sample without energy barrier or energy filter. We normalized source-drain current to highlight the general trend for this sample's source-drain current measurement.

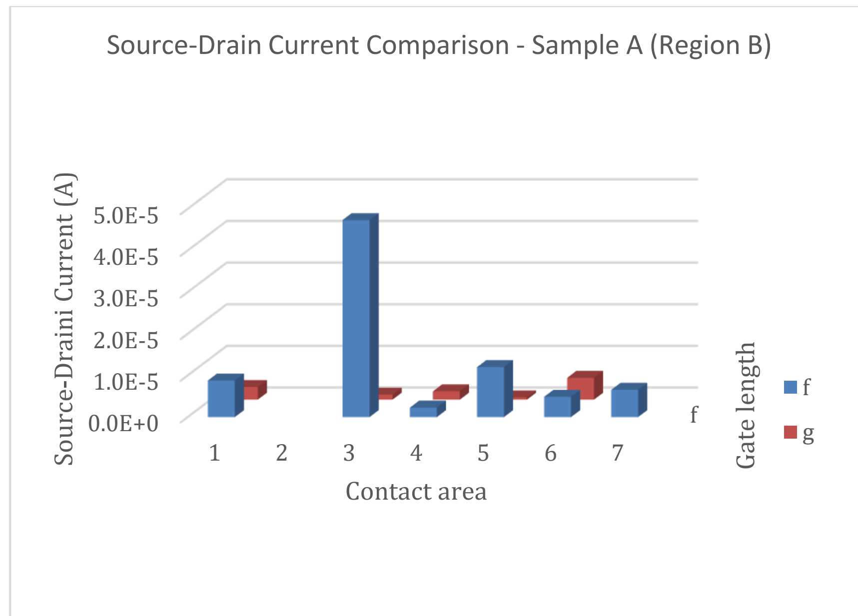

Figure 34: Source-drain current comparison for region B on sample with no tunneling barrier and no energy filter

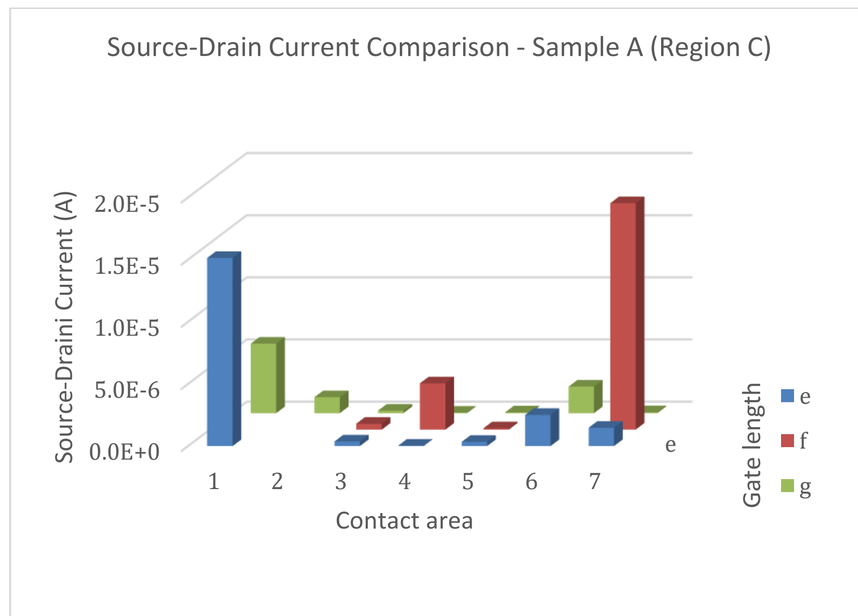

Figure 35: Source-drain current comparison for region C on sample with no tunneling barrier and no energy filter

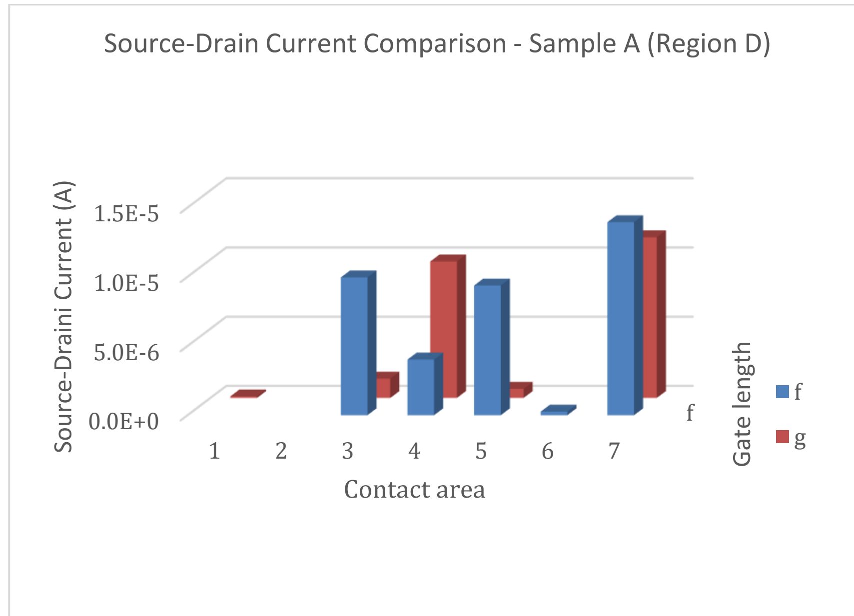

Figure 36: Source-drain current comparison for region D on sample with no tunneling barrier and no energy filter

The figures above compare absolute values of source-drain current with varying contact areas and gate lengths for samples having no tunneling barrier and no quantum well. We did not observe a reproducible correlation for source-drain currents with changing contact area or gate length.

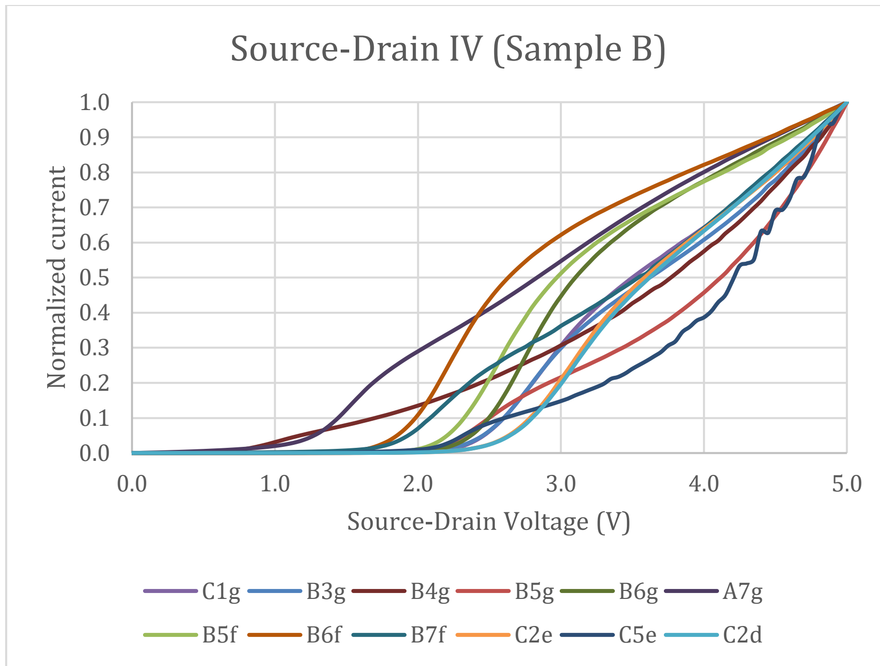

Figure 37: Normalized source-drain IV for sample with tunneling barrier and no energy filter

The figure above shows normalized source-drain current for sample with tunneling barrier but no energy filter. The plot shows an overall variation in source-drain currents with the only commonality being that all devices measured seemed to have some kink as the source-drain voltage increased.

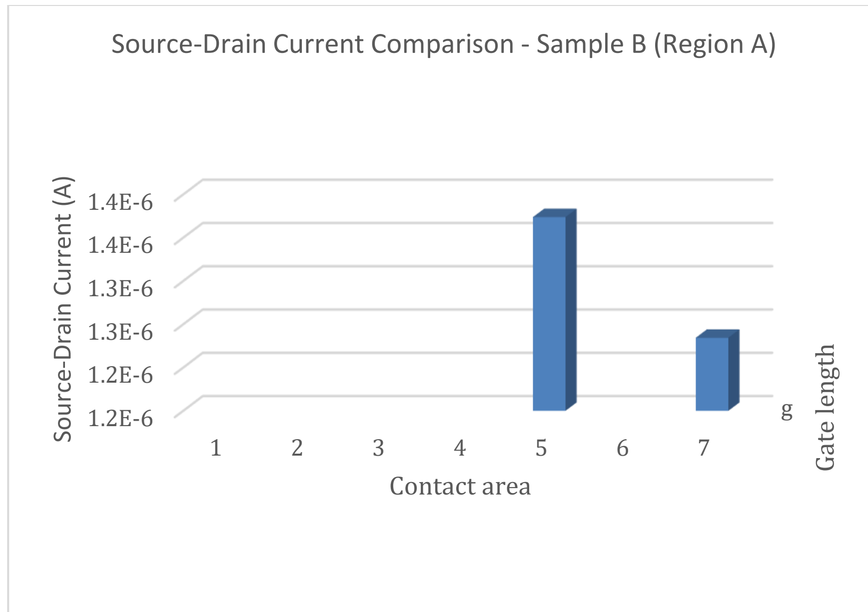

Figure 38: Source-drain current comparison for region A on sample with tunneling barrier and no energy filter

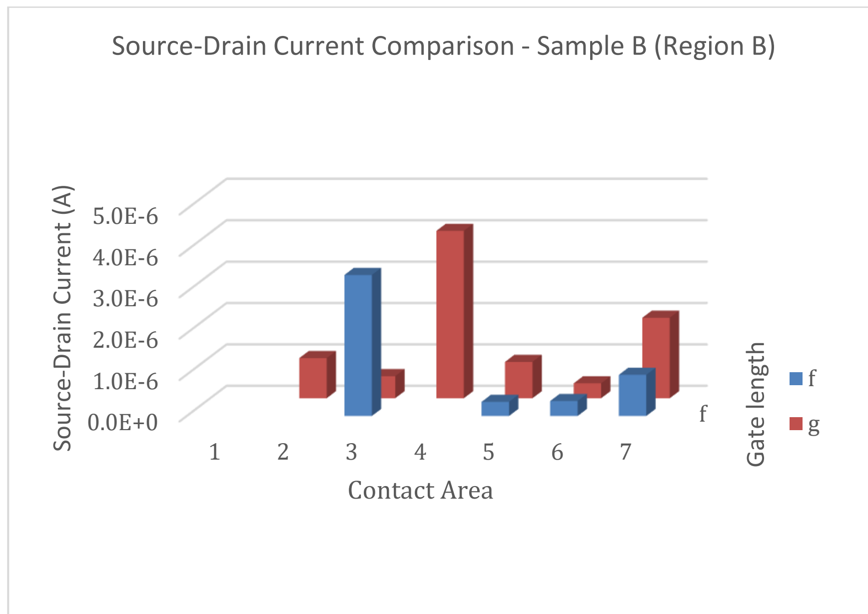

Figure 39: Source-drain current comparison for region B on sample with tunneling barrier and no energy filter

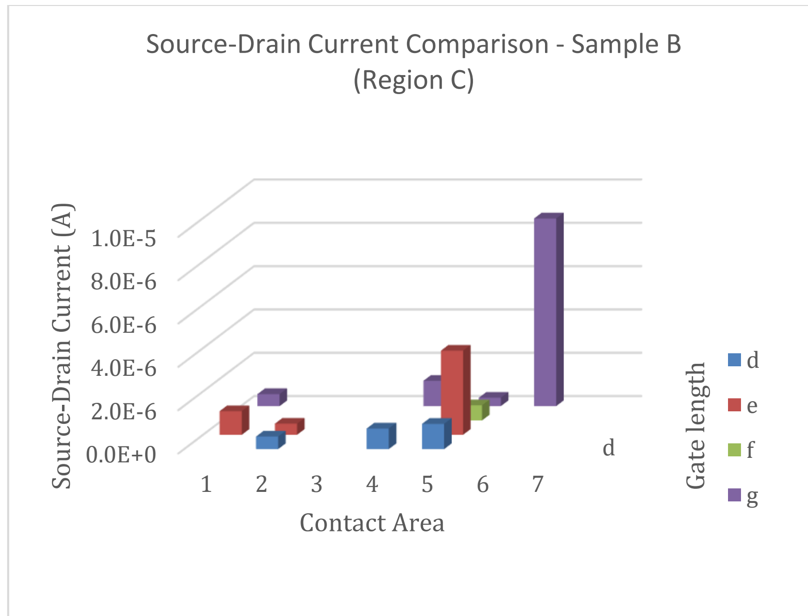

Figure 40: Source-drain current comparison for region C on sample with tunneling barrier and no energy filter

Comparison of source-drain current values with varying gate lengths and contact areas for the sample with tunneling barrier only, presented in figures above, failed to present a consistent correlation. This might have been due to a lack of source and drain electrode coupling.

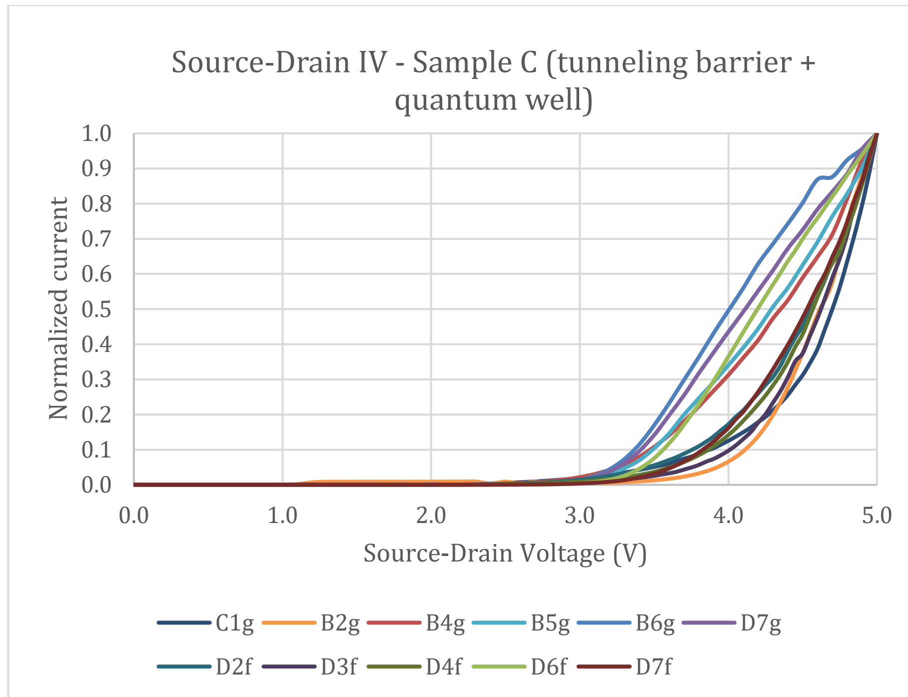

Figure 41: Normalized source-drain IV for sample with tunneling barrier and energy filter

When we normalized source-drain current for the sample with both tunneling barrier and quantum well energy filter, we observed that the onset of electron flow was delayed until about 3V - 3.5V source-drain IV. This implies that cooled electrons did not have sufficient energy to tunnel through to the conduction band of the silicon channel and further onto the drain electrode until the voltages were attained.

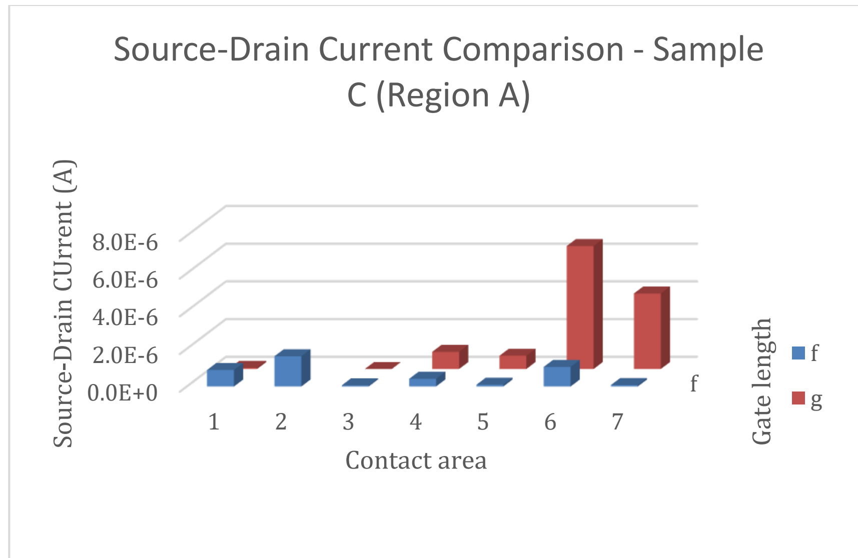

Figure 42: Source-drain current comparison for region A on sample with tunneling barrier and energy filter

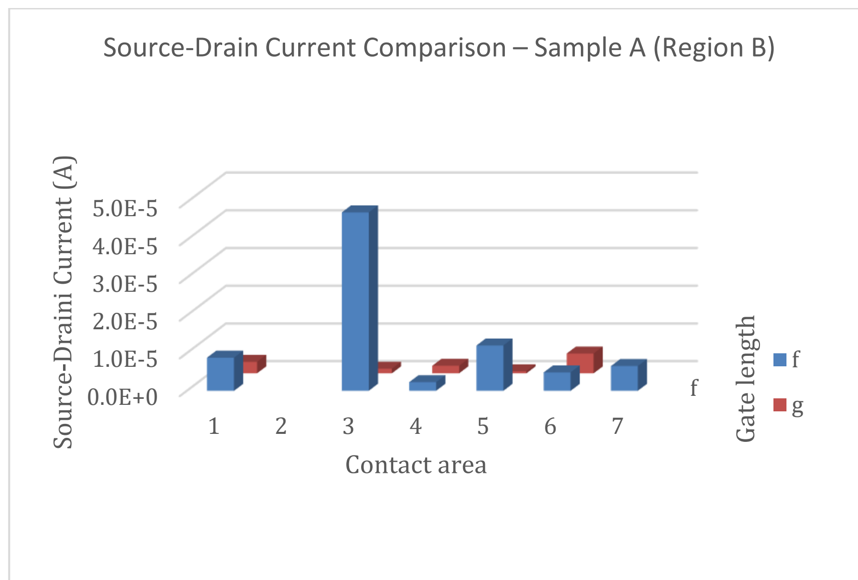

Figure 43: Source-drain current comparison for region B on sample with tunneling barrier and energy filter

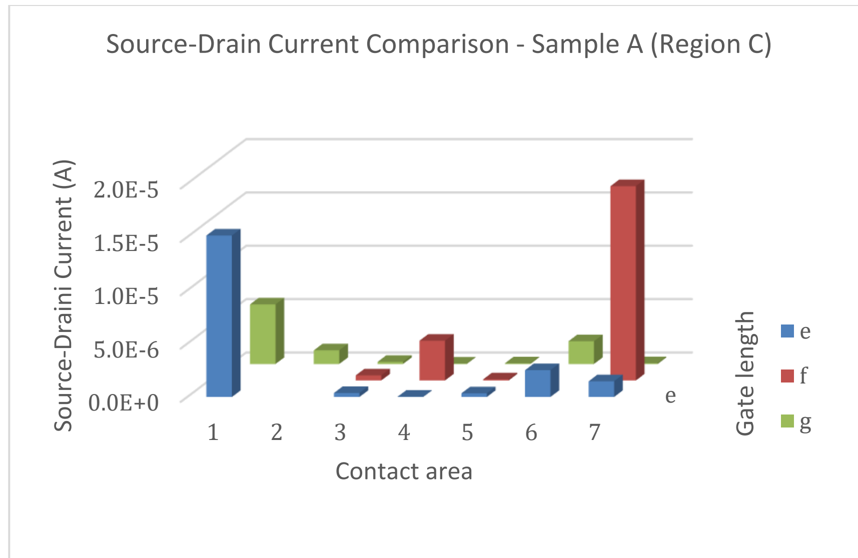

Figure 44: Source-drain current comparison for region C on sample with tunneling barrier and energy filter

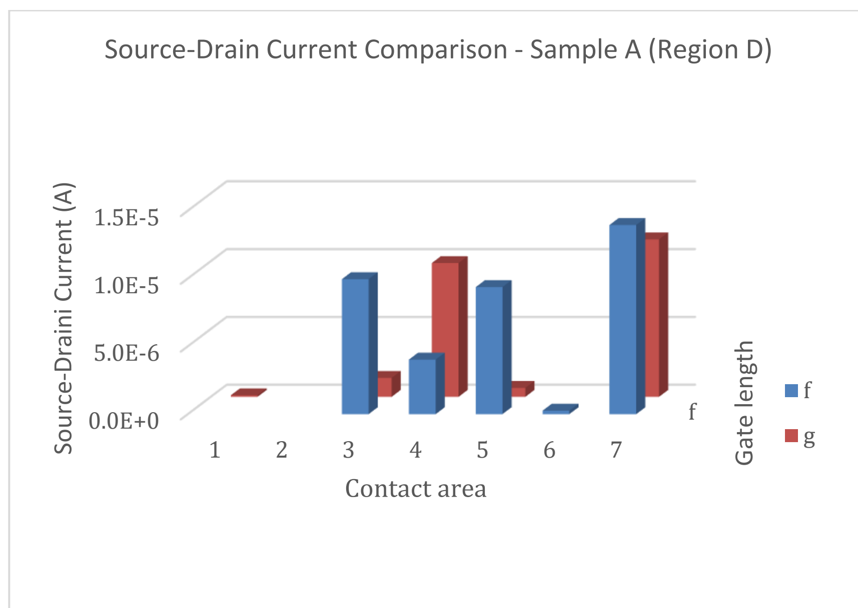

Figure 45: Source-drain current comparison for region C on sample with tunneling barrier and energy filter

Variation of contact area and gate length for the sample having both tunneling barrier and quantum well energy filter also did not present a consistent correlation with source-drain current.

This may be due to the absence of efficient source and drain electrode coupling with the silicon channel.

The third electrical measurement for devices was to observe gate modulation as gate bias is increased. A third probe tip is placed on the gate contact pad and gate bias is increased in a stepwise manner. This is done such that for each gate bias, the source-drain is swept from 0V to 5V. We start by varying the gate bias from 0V to 2V in 5 steps. If this initial measurement shows no gate electrode leakage, we proceed with larger gate bias variations.

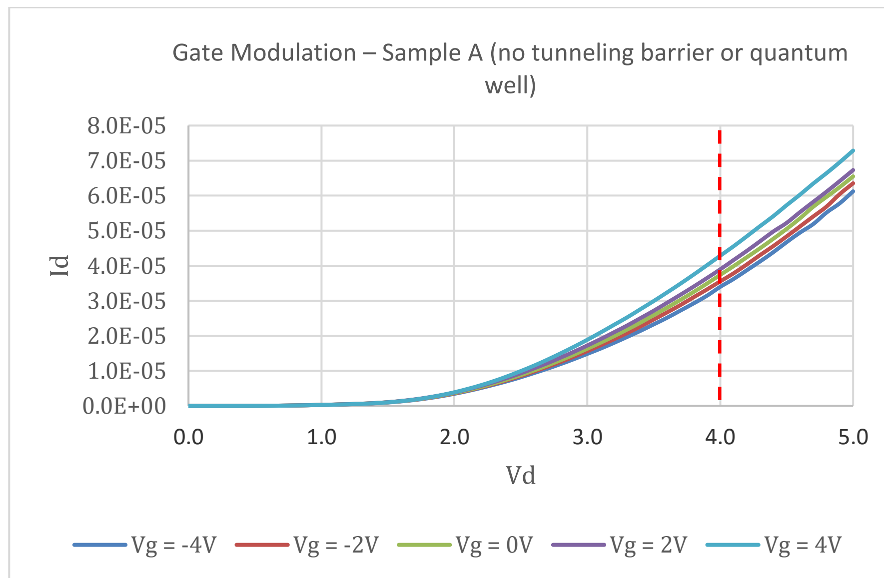

Figure 46: Drain current vs drain voltage with increasing gate bias for transistor device having no tunneling barrier and no energy filter

The figure above shows gate modulation for transistor device on sample A – without tunneling barrier and without energy filter. Here the applied gate bias was varied from -4V to 4V in steps of 2V. The IV characteristics observed can be explained using the energy band diagrams in Figure 47.

When no bias is applied, no path exists for electrons to flow due to the energy barrier of the silicon channel. Now, when we apply a positive drain bias, the fermi level of the drain electrode is lowered, and this pulls the energy bands of the silicon channel are also pulled downwards. When there is no gate bias applied, some thermal electrons can tunnel through since the conduction band energy barrier is thin enough. Application of a positive gate bias leads to lowering of the silicon semiconductor conduction than leading to an even thinner energy barrier. Hence even more electrons are able to tunnel through the energy barrier into the silicon conduction band and further on to the drain electrode. This leads to a gradual increase in the source-drain current.

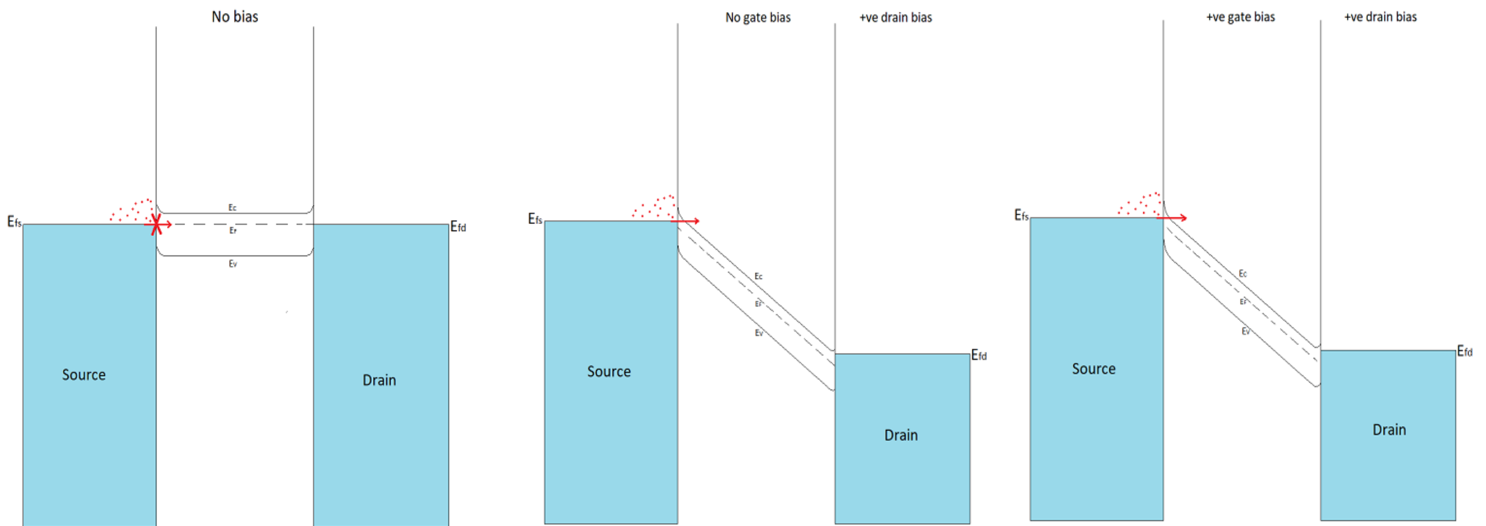

Figure 47: Energy band diagram showing electron transfer mechanism for different drain and gate biases of transistor device having no tunneling barrier and no energy filter

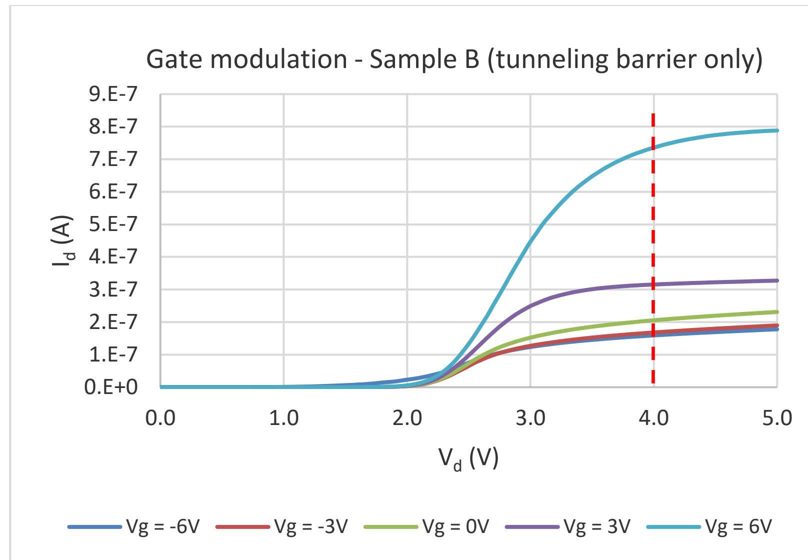

Figure 48: Drain current vs drain voltage with increasing gate bias for transistor device having tunneling barrier and no energy filter

The IV plot above shows gate modulation for sample B – with tunneling barrier but no quantum well energy filter. When no gate bias is applied and a positive bias is applied to the drain electrode, the fermi level of the drain electrode is lowered, and this drags the energy bands of the silicon channel downwards as well. This presents a situation where electrons can tunnel through the tunneling barrier as the conduction band-tunneling junction barrier is thin enough for electrons to go through. When a negative bias is applied to the gate and a positive bias is sustained on the drain electrode, the barrier to electron tunneling is still thin enough to allow electrons tunnel from the source electrode to the conduction band of the silicon channel. This is because, the negative gate bias is not large enough to compensate for the pulling down on the silicon energy bands. Further, when a positive gate bias is applied, the silicon energy bands are pulled downwards even more, thereby allowing more electrons to tunnel through.

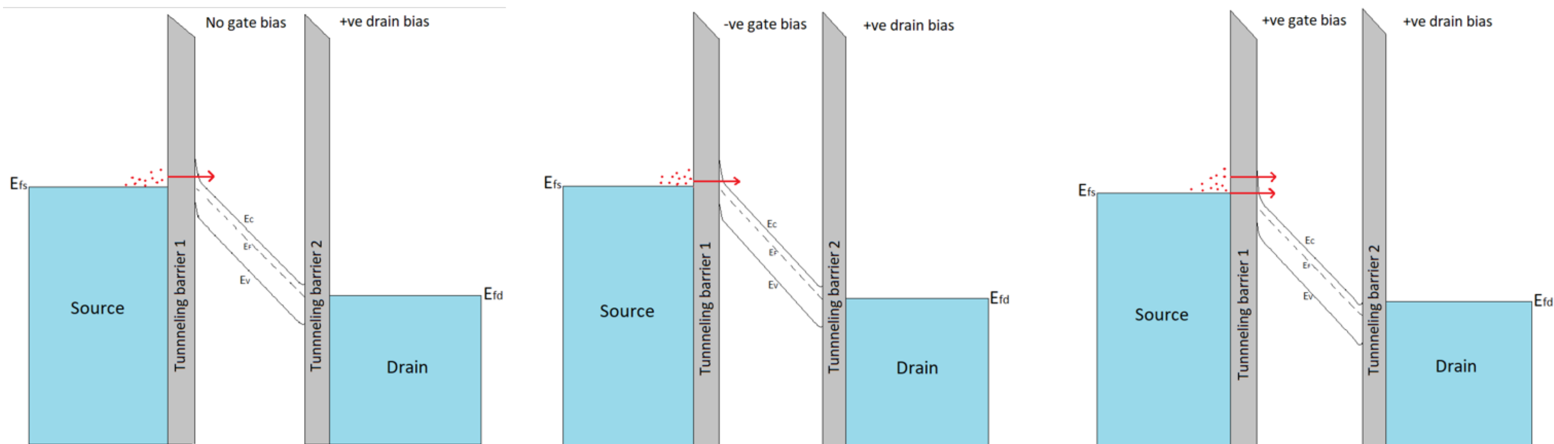

Figure 49: Energy band diagram showing electron transfer mechanism for different drain and gate biases of transistor device having tunneling barrier and no energy filter

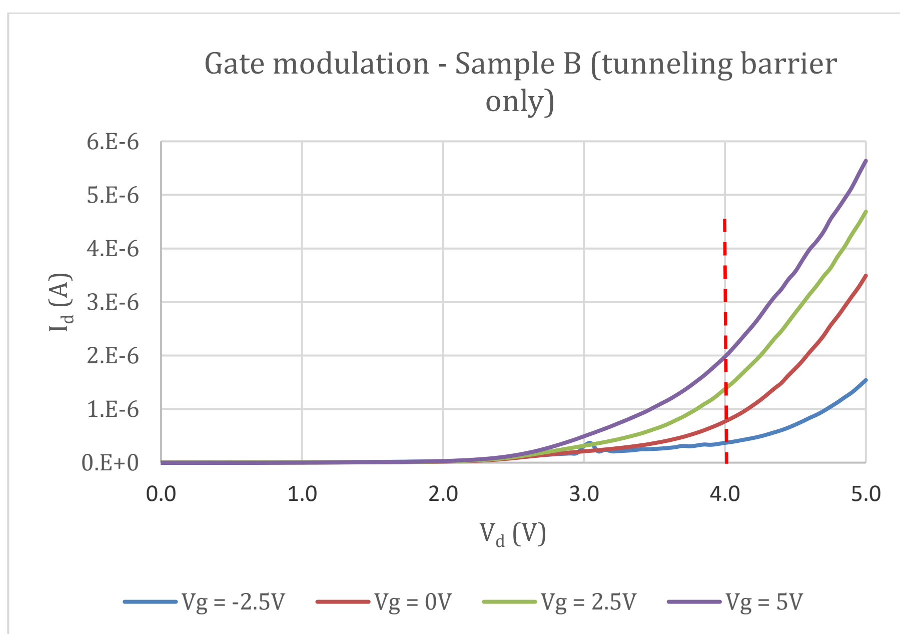

Figure 50: Drain current vs drain voltage with increasing gate bias for transistor device having tunneling barrier and no energy filter

For the device IV plot shown above, the sample has a tunneling barrier but no quantum well energy filter. The IV characteristics are explained using the band diagrams below. When no gate bias is applied and a positive bias is applied to the drain electrode, the fermi level of the drain

electrode is lowered, and this drags the energy bands of the silicon channel downwards as well. This presents a situation where electrons can tunnel through the tunneling barrier as the conduction band-tunneling junction barrier is thin enough for electrons to go through. When a negative bias is applied to the gate and a positive bias is sustained on the drain electrode, electrons do not tunnel through because there is a barrier to electron flow at the source electrode-silicon conduction band interface. We think this impediment to electron tunneling is because the device in question has both a smaller contact area and gate length compared with the earlier device which showed gate modulation. We believe that the comparatively smaller gate geometry may have contributed to better gate coupling. Further, when a positive gate bias is applied, the silicon energy bands are pulled downwards even more, thereby allowing more electrons to tunnel through.

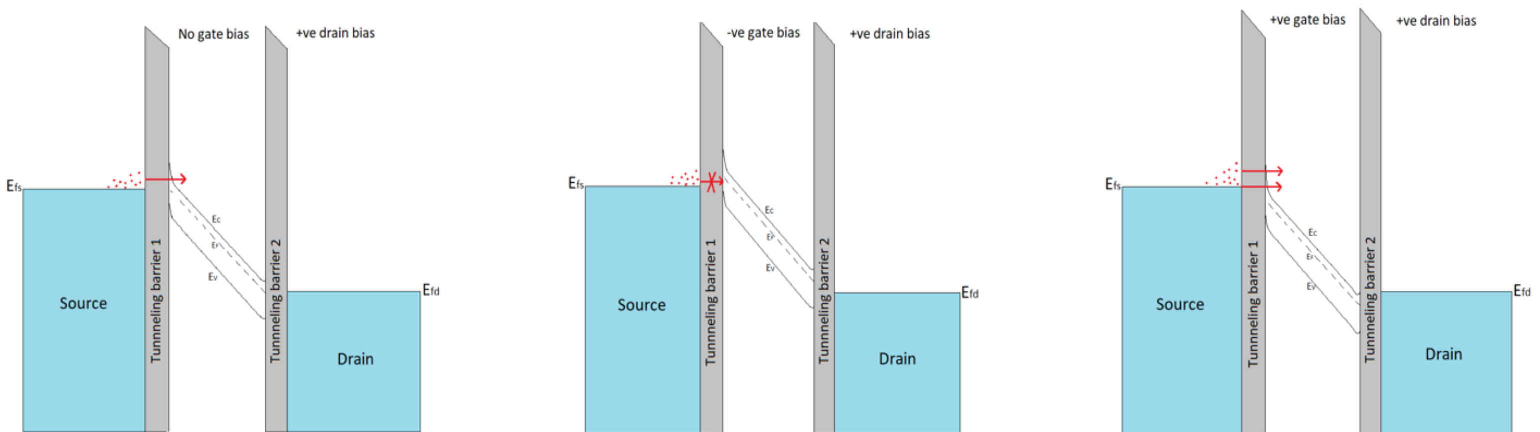

Figure 51: Energy band diagram showing electron transfer mechanism for different drain and gate biases of transistor device having tunneling barrier and no energy filter

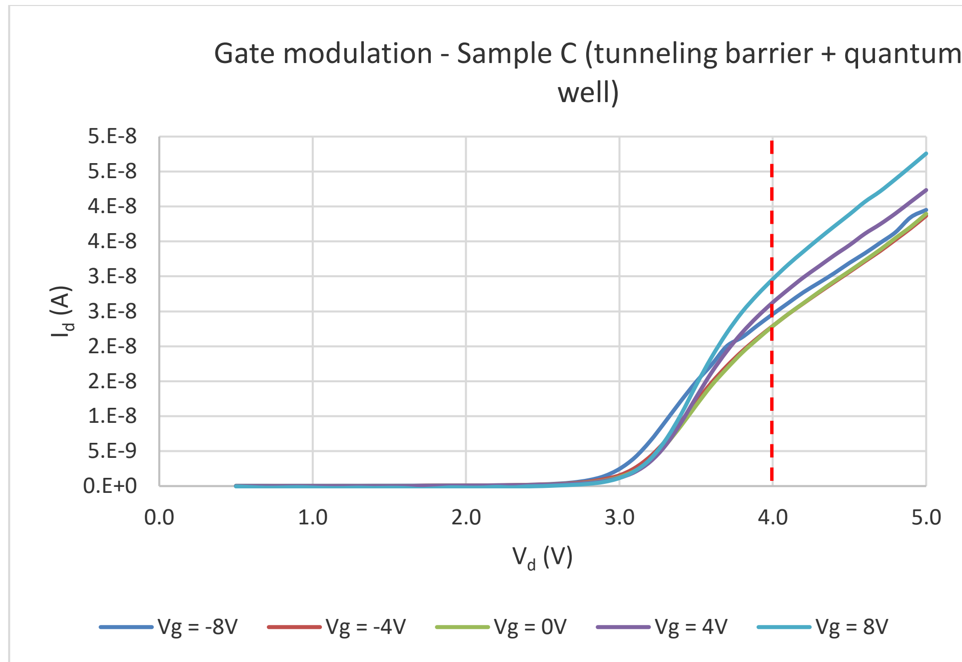

Figure 52: Drain current vs drain voltage with increasing gate bias for transistor device having tunneling barrier and energy filter

Gate modulation was also observed for sample C device (with tunneling barrier and energy filter layer). The IV gate modulation behavior is as shown above. The mechanism taking place for this device is depicted in the energy band diagrams below.

Application of a positive bias to the drain electrode lowers the fermi level of the electrode. When no gate bias is applied the lowered fermi level of the drain electrode drags the silicon energy bands downwards. This allows cooled thermally excited electrons in the quantum well layer energy filter occupying the closest discrete energy level of the quantum well to tunnel through to the silicon channel conduction band. This confined occupation of the quantum well fermi level is possible because a very large (~250meV) separation exists between discrete energy levels of the quantum well. When we apply a positive gate bias, the energy bands of silicon channel are lowered and this permits electrons in the discrete energy level of the quantum well to tunnel through even more. Application of negative bias to the gate, though it raises the silicon channel energy bands,

fails to totally compensate for the lowering effect of the positive bias applied to the drain. So, electrons are still able to tunnel through to the silicon conduction band and further on to the drain electrode thereby increasing source-drain current.

The observation of gate modulation at high drain voltages (> 3V) likely made it hard to verify energy filtering for this sample (tunneling barrier + quantum well energy filter). We think this was a consequence of inefficient gate coupling.

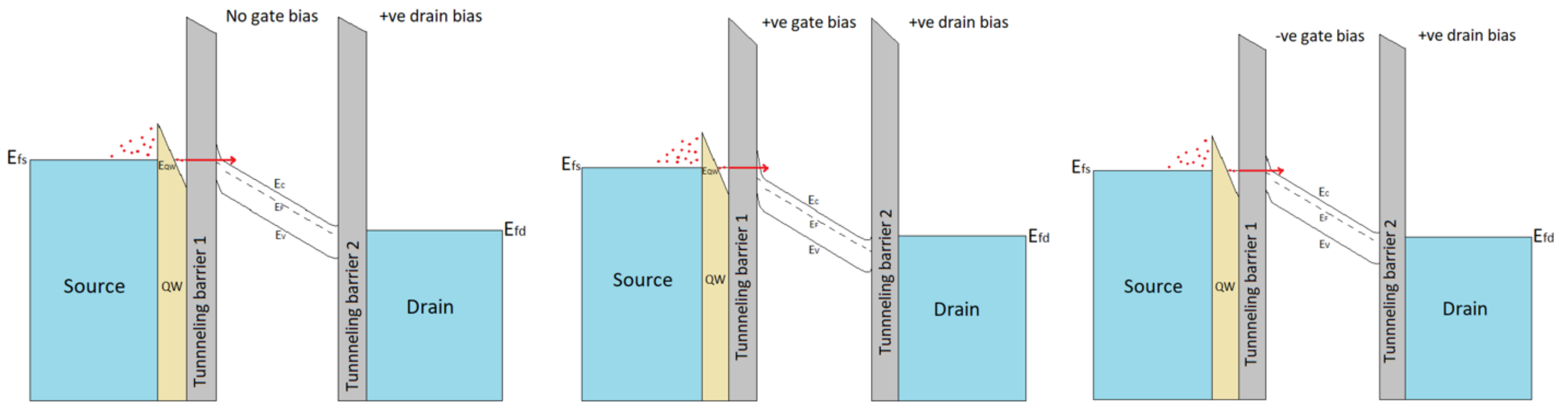

Figure 53: Energy band diagram showing electron transfer mechanism for different drain and gate biases of transistor device having tunneling barrier and energy filter

Chapter 5: Conclusion

A new device structure was designed for making cold electrons transistors. Fabrication processes were developed for implementing this new architecture. Fabrication procedure was optimized such that fabrication time was reduced from four weeks to one week. The energy filtering stack comprised of a 2nm SiO_2 tunneling barrier and a 2nm Cr_2O_3 quantum well (QW) layer between Ni source and drain electrodes and the silicon channel. Three different device types were fabricated to study the energy filtering effect: devices with no tunneling barrier and no QW energy filter, devices with tunneling barrier only and devices with both tunneling barrier and QW energy filter. Transistor IV characteristics was verified by gate modulation behavior of fabricated devices and gate modulation characteristics was observed at drain voltages > 2V. However, energy filtering effect was not able to be identified. This obscuring of possible energy filtering is a consequence of inefficient gate coupling, as evidenced by gate modulations only at large drain voltages.

The effect of gate geometry on current flow onset in fabricated devices was investigated. This was done by implementing an array of devices with varying gate lengths and varying source and drain electrode contact areas. However, device-to-device variation made it a challenge establishing a correlation.

Further work may focus on optimizing the device structure and geometry so that efficient gate coupling would yield energy filtering transistors.

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