Identification and Characterization of Gate Oxide Defects Responsible for Low Frequency Noise in MOSFETs

by

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Abstract

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The main objective of this work is to identify and characterize gate oxide defects that are present in submicron p-channel metal oxide semiconductor field effect transistors (pMOSFETs) and which are responsible for random telegraph signals (RTS). With the downscaling of MOSFETs, alternating capture and emission of channel carriers by defects residing at the oxide-semiconductor interface and bulk oxide have become a pronounced problem. Even though RTS has been used for several years as a tool to characterize the interface/bulk defects, RTS in pMOSFETs has been under-reported compared to that in nMOSFETs, resulting in less information on hole defects in pMOSFETs responsible for RTS. This work, using variable temperature RTS measurements on state-of-the-art pMOSFETs, provides an extensive study of the location of the active oxide defects and their energy in the oxide bandgap using a model based on first principles, and suggests a possible structure for the defects responsible for RTS.

There has been a significant knowledge gap in the field of the role of hot carrier stress for hole trapping in pMOSFETs that lead to RTS. In addition, the origin of trap activation and deactivation due to stress in pMOSFETs is not completely understood yet. Obtaining information about the trap generation and passivation mechanisms and the newly generated trap structure would need extensive amount of RTS data on several pMOSFETs at both pre-stress and post-stress conditions. This work presents variable temperature RTS data on unstressed and stressed submicron pMOSFETs. A structure of the defects responsible for RTS is proposed that can be generated or passivated as a result of stress.

At first room temperature RTS measurements were done on pMOSFETs of different gate areas biased at strong inversion and linear region of operation. The room temperature RTS data allowed extraction of trap position

from the Si-SiO_2 interface, trap energy level with respect to the SiO_2 valence band edge and the trap capture cross-section. The variable temperature RTS data, on the other hand, can be used to obtain information on the trap energy parameters such as capture activation energy, change in enthalpy and entropy in the system due to carrier emission, and the trap relaxation energy. Variable temperature RTS measurements were done on the pMOSFETs varying the temperature from 295 K down to 165 K. The trap energy parameters thus obtained were compared to the already published trap parameters reported by several researchers using other techniques. A possible trap structure was suggested.

Channel hot carrier (CHC) stress was applied to different sized pMOSFETs at room temperature for different durations. RTS measurements were performed following each stress step. Comparing the trap capture cross-sections and trap energy levels with respect to the SiO_2 valence band edge to the previously reported trap parameters, a structure of the stress-generated traps was suggested. Traps were observed to appear and disappear randomly after each stress interval. A possible explanation behind such phenomenon was proposed as well. To obtain more information about the stress-induced traps, variable temperature measurements were done on fresh and stressed pMOSFETs. The MOSFETs were stressed at room temperature, and a subsequent RTS measurement was performed at temperatures from 295 K down to 165 K. Comparison of the energy parameters of the stress-induced traps with the already characterized traps allowed us to make conclusions on the structure of those stress-induced traps.

Since 1/f noise is a major concern in short channel transistors, the traps responsible for 1/f noise in these devices need to be passivated as much as possible. This will help to quantify the maximum achievable limit of flicker noise in the downscaled devices, and hence find a technique for growth of gate oxide with minimal flicker noise. In this research, voltage and current noise power spectral densities of different sized nMOSFETs in three wafers with different oxide growth conditions have been measured, normalized, and compared. Correlations of the oxide growth steps with the measured flicker noise have been investigated.

The main novelty of this work lies in the facts that (i) it is the first time when such detailed analyses has been done on hole defects near the Si-SiO_2 interface that are responsible for RTS. A physical structure of the defects causing the switching events has been proposed. (ii) In addition to the process-induced defects, possible structures for stress-induced defects have also been discussed. (iii) Generation, activation and deactivation of traps with stress

are experimentally observed and explained. Finally, (iv) Trap volatility because of stress has been observed, and explained. Possible defect structures have been suggested, which provides further insight into the reliability issues in pMOSFETs in terms of noise and degradation.

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List of Symbols

C_{GC}	MOSFET gate to channel capacitance (Fcm^{-2})
$C_{GC_{inv}}$	MOSFET gate to channel capacitance in the inversion region (Fcm^{-2})
C_{ov}	MOSFET overlap capacitance (Fcm^{-2})
C_{ox}	MOSFET oxide capacitance (Fcm^{-2})
e	Total absolute error in fitted curve
E_C	Silicon conduction band edge (eV)
E_F	Fermi energy level (eV)
E_g	Silicon bandgap (eV)
E_{F_n}	Quasi Fermi energy level for electrons (eV)
E_{F_p}	Quasi Fermi energy level for holes (eV)
E_y	Electric field along the channel(Vcm^{-1})
E_R	Trap relaxation energy (eV)
E_T	Trap energy level (eV)
E_V	Silicon valence band edge (eV)
$E_{V_{ox}}$	Silicon dioxide valence band edge (eV)
f	Frequency (Hz)
f_t	Electron trap occupancy function
f_{th}	Hole trap occupancy function
F_m	Number of switching events within duration t_m
F_S	Sampling frequency of the oscilloscope (Hz)
g	Trap degeneracy factor
g_d	Donor degeneracy factor

g_D	MOSFET channel conductance, defined as $\partial I_{DS}/\partial V_{DS}$ (Ω^{-1})
g_m	MOSFET trans-conductance, defined as $\partial I_{DS}/\partial V_{GS}$ (Ω^{-1})
g_n	Generation rate of trapped oxide charges (s^{-1})
h	Planck's constant (J-s)
I	Current (A)
I_D	Drain current (A)
I_{DC}	Direct current (A)
I_{DS}	Drain-source current (A)
I_{sh}	Shot noise current (A)
$K_{1/f}$	Ratio of Hooge parameter to fluctuating number of carriers
k_B	Boltzmann's constant (JK^{-1})
L	MOSFET channel length (μm)
L_D	Debye length (μm)
M	Total number of bins
m_{ox}^*	Electron effective mass in the oxide (Kg)
m_p^*	Hole effective mass (Kg)
n_0	Inversion layer electron density per unit volume at equilibrium (cm^{-3})
$N_{0_{ox}}$	Number of trapped oxide charges at equilibrium
N_C	Effective density of states for electrons in the conduction band (cm^{-3})
N_D	Background donor doping concentration (cm^{-3})
N_D^+	Ionized doping concentration (cm^{-3})
n_i	Intrinsic carrier concentration (cm^{-3})
N_{inv}	Inversion layer electron density per unit area (cm^{-2})
N_{ox}	Number of trapped oxide charges
N_p	Total number of points in a signal in the oscilloscope

N_t	Density of occupied electron traps per unit area (cm^{-2})
N_V	Effective density of states for holes in the valence band (cm^{-3})
P_{inv}	Inversion layer hole density per unit area (cm^{-2})
P_t	Density of occupied hole traps per unit area (cm^{-2})
p	Inversion layer hole density per unit volume (cm^{-3})
p_0	Inversion layer hole density per unit volume at equilibrium (cm^{-3})
q	Electronic charge (C)
Q	Total charge in the inversion layer per unit area (Ccm^{-2})
Q_{ox}	Total charge in the oxide per unit area (Ccm^{-2})
Q_s	Total charge in the semiconductor (C)
r	Hole capture rate by trap per unit energy ($Hz\ eV^{-1}$)
r_n	Recombination rate of trapped oxide charges (s^{-1})
R	Resistance (Ω)
S_I	Current power spectral density ($A^2\ Hz^{-1}$)
$S_{I_{DS}}$	Power spectral density for drain-source current ($A^2\ Hz^{-1}$)
$S_{\Delta I_{DS}}$	Power spectral density for drain-source current fluctuations ($A^2\ Hz^{-1}$)
S_g	Power spectral density due to generation in trapped oxide charges (Hz^{-1})
S_N	Power spectral density of fluctuations in the number of carriers (Hz^{-1})
$S_{N_{ox}}$	Power spectral density of fluctuations in the number of trapped charge carriers in the oxide (Hz^{-1})
$S_{\Delta N_t}$	Power spectral density due to local filled traps (Hz^{-1})
$S_{Q_{ox}}$	Power spectral density due to all trapped oxide charges ($C^2\ Hz^{-1}$)
$S_{Q_{oxi}}$	Power spectral density due to a single trapped oxide charge ($C^2\ Hz^{-1}$)
S_r	Power spectral density due to recombination in trapped oxide

	charges (Hz^{-1})
S_V	Voltage power spectral density ($V^2\,Hz^{-1}$)
$S_{V_{DS}}$	Power spectral density for drain-source voltage ($V^2\,Hz^{-1}$)
$S_{V_{FB}}$	Power spectral density due to change in flat band voltage ($V^2\,Hz^{-1}$)
t	Inversion layer thickness (nm)
t_0	Inversion layer thickness at zero Kelvin temperature (nm)
t_m	Time duration for each bin (s)
T	Absolute temperature (K)
T_{ox}	Oxide thickness (nm)
T_t	Total time length of a signal in the oscilloscope (s)
V_C	Channel voltage (V)
V_D	Drain voltage (V)
V_{DS}	Drain to source voltage (V)
V_{DS_f}	Drain to source voltage in forward mode (V)
V_{DS_r}	Drain to source voltage in reverse mode (V)
V_{FB}	Flat band voltage (V)
V_{GS}	Gate to source voltage (V)
V_{OX}	Amount of bending in valence and conduction bands in SiO_2 (eV)
V_T	Threshold voltage (V)
$\overline{v}_{th}$	Average thermal velocity of channel carriers (cms^{-1})
W	MOSFET channel width (μm)
x	Direction into the substrate
x_T	Oxide trap location from Si/SiO_2 interface (nm)
y	Direction along the channel
y_T	Trap position along the channel measured from the source
z	Direction along the device width
α	Screened scattering coefficient (V-s)

α_m	Screened parameter relating change in bulk mobility with change in trapped oxide charges (V-s)
α_0	Fitting parameter in screened scattering coefficient model (V-s)
α_1	Fitting parameter in screened scattering coefficient model (V-s)
β	Current exponent in current noise PSD
ΔE_B	Trap capture activation energy (eV)
ΔE_{TV}	Trap energy level with respect to silicon valence band edge (eV)
Δf	Noise bandwidth (Hz)
Δg_n	Randomness in trapped oxide charge generation rate (s^{-1})
ΔH	Change in enthalpy (eV)
ΔN	Fluctuation in number of electrons that cause G-R noise
ΔN_{inv}	Number of local inversion layer electrons
ΔN_{ox}	Change in number of charges trapped in oxide
ΔN_t	Number of local filled electron traps
ΔP_{inv}	Number of local inversion layer holes
ΔP_t	Number of local filled traps
Δr_n	Randomness in trapped oxide charge recombination rate (s^{-1})
ΔS	Change in entropy (eV)
ΔV_{DS}	Fluctuation in drain to source voltage (V)
ΔV_T	Change in threshold voltage (V)
ε_0	Permittivity of free space (Fm^{-1})
ε_{Si}	Dielectric constant of silicon
ε_{SiO_2}	Dielectric constant of silicon dioxide
γ	Frequency exponent in flicker noise PSD
λ	Electron wave attenuation coefficient (cm^{-1})
μ	Effective channel carrier mobility ($cm^2 V^{-1}s^{-1}$)
μ_0	Effective channel carrier mobility at zero Kelvin temperature

	($cm^2V^{-1}s^{-1}$)
μ_{lat}	Carrier mobility due to lattice scattering ($cm^2 V^{-1}s^{-1}$)
μ_{imp}	Carrier mobility due to impurity scattering ($cm^2 V^{-1}s^{-1}$)
μ_{oth}	Channel carrier mobility due to other mechanisms ($cm^2 V^{-1}s^{-1}$)
μ_{ox}	Channel carrier mobility limited by gate oxide charge scattering ($cm^2 V^{-1}s^{-1}$)
φ_0	Difference between Si and SiO_2 band edges at the interface (eV)
σ	Trap capture cross-section (cm^2)
σ_0	Trap capture cross-section pre-factor (cm^2)
ψ	Potential at the channel at any point measured from the Si-SiO_2 interface (eV)
ψ_s	Surface potential at the Si-SiO_2 interface (eV)
$\overline{\tau}$	Average time constant for capture and emission of carriers by the trap (s)
$\overline{\tau}_0$	Average characteristic time constant (s)
$\overline{\tau}_1$	Average time constant for the lower RTS level (s)
$\overline{\tau}_2$	Average time constant for the upper RTS level (s)
$\overline{\tau}_c$	Average capture time constant for a trap (s)
$\overline{\tau}_e$	Average emission time constant for a trap (s)

Chapter 1 Introduction

1.1 Background and Research Motivation

For the last few decades, downscaling of electronic devices has been the primary reason behind the remarkable success of microelectronic industry. Placing millions of transistors in a single chip has allowed higher operating speed and lower power consumption at a cheaper price. Excellent properties of silicon and silicon dioxide have resulted in widespread use of MOSFETs in analog and digital applications. However, with the decrease in device dimensions, these small area devices have been suffering several reliability issues such as random telegraph signals (RTS), flicker noise, gate leakage current, and bias temperature instability (BTI). Oxide defects residing at the oxide-semiconductor interface or in the bulk oxide are responsible behind these mechanisms. In order to ensure reliable operation of the scaled devices, the physical structure and properties of these defects need to be investigated. This investigation would require extensive amount of experimental data and analyses using a trap diagnosis tool. RTS can be used as such a technique.

RTS was first reported by Kandiah *et al.* in a double-gated silicon JFET in 1978 [1], where they observed sudden peaks in the drain current at different gate and substrate bias, and temperatures. They attributed the drain current fluctuations to active Shockley-Read-Hall (SRH) centers in the Debye region, between the channel and fully depleted region. Later, in 1984, Ralls and coworkers observed discrete switching in the device resistances of MOSFETs with gate area of 0.1 μm × 0.1 μm at cryogenic temperatures [2]. They found capture and emission of electrons by oxide-semiconductor interface traps of various activation energies to be responsible behind this switching. They also found that although 1/f noise was observed in a large area device of area of 10 μm × 20 μm, no discrete switching was observed in that device. Discrete changes in the resistance was observed only in downscaled devices since with the decrease in device dimensions, very few traps will stay within the accessible range of the Fermi energy level to communicate with the channel electrons. Later, in 1988, Karwath and Schulz [3] used the deep level transient spectroscopy (DLTS) technique to study the interface traps in a small area MOSFET (1.2 μm × 1.5 μm). They pulsed the device in strong inversion to fill the traps, and then the pulse was applied in weak inversion region to make the filled traps empty. The consequent switching in the drain signal transient was observed (Fig. 1.1). This technique allowed them to access all traps with energy within the vicinity of the Fermi energy level.

However, analyses of these traps were very difficult, and hence very few information such as trap density, activation energy, and capture coefficient of these traps was possible to extract. Since then, RTS has been used as a trap diagnosis tool by numerous researchers [4], [5], [6], [7]. Increasing the drain voltage was found to decrease the average carrier capture time, while average emission time seemed to be independent of drain bias [4]. With the increase in lateral electric field, the channel electron temperature increases. At higher lateral electric fields, phonons emitted by the hot electrons contribute to increase the energy of the empty trap, thus decreasing the trap capture energy [4]. In addition, from the drain bias dependence of average capture and emission times in forward (where the drain and source voltages are applied to the actual drain and source terminals) and reverse (where drain and source terminals are interchanged) modes, effective trap location along the channel was estimated [4]. Trap capture cross-section, trap energy position in the silicon bandgap, and trap distance from the Si-SiO_2 interface were extracted using the gate bias dependence of the average time constants [5]. The average RTS capture and time constants have been found to be larger than the expected tunneling time constants, which indicated that carrier capture and emission process was not an elastic tunneling mechanism [6]. Screened Coulomb scattering theory was introduced and trap scattering coefficient was calculated [7]. Several RTS models have been reported that characterize the oxide defects [8], [9], [10]. Temperature dependence of traps with capture time of ~1s at room temperature was observed totally due to effects of intrinsic carrier density on carrier capture times [8]. Fluctuation in flat band voltage has been used to show that the variations in the normalized drain current RTS amplitudes with gate and drain bias are strongly correlated to the corresponding trans-conductance to drain current ratio [9], meaning that the number fluctuations of the channel electrons dominated over the fluctuations in the carrier mobility. Variable temperature RTS measurements have allowed extraction of important trap energy parameters such as capture activation energy, carrier emission energy, and trap relaxation energy [11], [12], [13]. RTS magnitude has been observed as a function of bias conditions, and device geometries, where in linear region, RTS magnitude has been found to be directly proportional to drain bias, independent of device width, and inversely proportional to the square of device length [14], [15]. Effects of discrete doping on RTS have also been investigated in detail, where inhomogeneous channel has been reported to increase the RTS magnitude [16], [17]. Effects of charge quantization on trap capture and emission times, screening coefficient, and effective channel electron mobility have been published as well [18]. In highly scaled devices, with high substrate doping and transverse electric field along the channel, the electron energy levels would split into discrete levels known as electric sub-bands (Fig. 1.2) [19], [20]. Therefore, while getting emitted

back to the channel, the captured carrier needs to gain additional amount of energy, which would change the carrier capture and emission times by the trap. The charge distribution along the substrate in the channel would peak at a

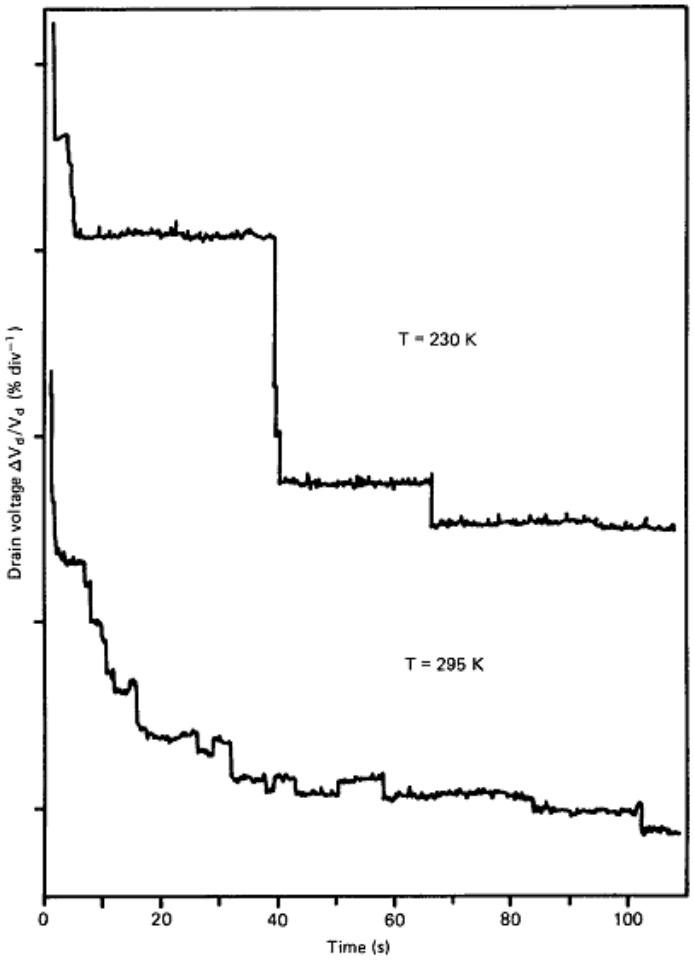


Fig 1.1 Switching observed in the drain signal transient in an nMOSFET of area (1.2 μm × 1.5 μm) at a gate voltage of 0.85 V, and drain current of 20 nA. The traps were filled using a gate voltage of 4.4 V for 5 min. Reprinted with permission from [3]

distance from the Si-SiO_2 interface (Fig. 1.2), which will affect the effective channel electron mobility and screening coefficient. These effects have been modeled in [18]. In addition to simple two-level RTS, observation of complex switching in the drain signals due to multiple active traps have also been reported [21], [22]. RTS has been responsible for read and write bit errors in SRAMs [23], variable retention times in DRAMs [24], read instability in RRAMs [25], and threshold voltage fluctuations in the program-and-erase cycles in flash memories [26], [27].

Not only the aforementioned reliability concerns, several nonlinearities also tend to show up in ultra-scaled MOSFETs such as channel length modulation, drain induced barrier lowering (DIBL), surface scattering, velocity saturation, impact ionization, and hot carrier effects [28]. All these nonlinear effects are responsible for degradation in device parameters in small area devices. DIBL increases the drain to source current in the sub-threshold region. Surface scattering reduces the channel carrier mobility. Velocity saturation decreases the device trans-conductance in the saturation region. Impact ionization creates additional electron-hole pairs leading to a current overrun. And hot carriers can enter the oxide, get trapped rising the oxide charge, thus increasing the device threshold voltage [28]. Moreover, the hot carriers can also create or activate passivated oxide defects that can cause additional RTS at the output. Hence, the hot carrier effects can significantly affect the reliable operation of small area MOSFETs. In order to suppress the hot carrier effects in device reliability, the physical mechanisms behind defect generation and passivation need to be understood. Once again that would need substantial amount of experimental RTS data analyses on stressed MOSFETs.

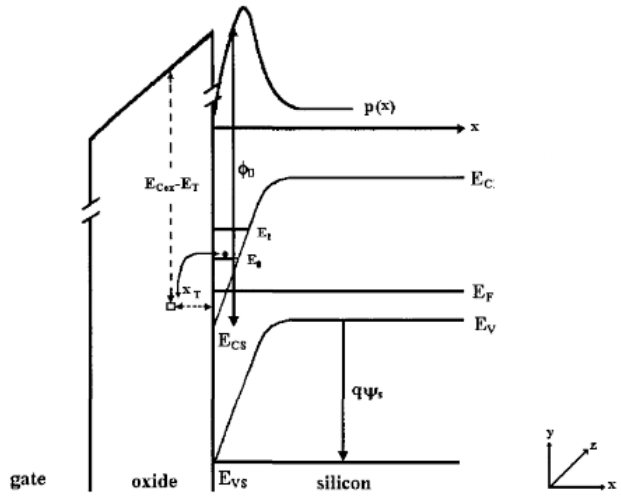


Fig. 1.2 Band diagram of an nMOSFET showing the quantized energy levels and charge distribution into the substrate. Reprinted with permission from [18]

Most of the IC manufacturing methodologies are developed on CMOS technologies, which would include both active electron and hole traps in the failure mechanisms. Even though RTS is being used as a non-destructive technique to characterize gate oxide traps for a few decades [29], RTS due to hole traps in pMOSFETs are severely under-reported compared to that due to electron traps in nMOSFETs. Most of the articles that reported RTS in pMOSFETs have limited their studies to the physical location, capture activation energy, and capture cross-section

of the responsible defects [30], [31], [32]. In 1991, Schulz and Karmann first reported RTS measurements on pMOSFETs at variable temperatures (90 K – 250 K), where they extracted the trap activation energies from the temperature dependence of hole capture and emission times [30]. They indicated Coulombic attractive center defects to be responsible for these RTS, and mentioned the mechanism to be a thermally activated one. Later, in 1993, Schofield and Borland reported RTS in pMOSFETs of area 1.25 μm × 1.25 μm varying the temperature between 77 K and 300 K [31]. They also observed hole capture and emission time to be dependent on temperature, and hence concluded the capture and emission process to be thermally activated. In 2000, they measured RTS in pMOSMETs of similar area at temperatures 4.2 K to 300 K [32]. They found the switching rate to be dependent on temperature only above 30 K, and to be independent of temperature below 10 K. From this observation, they reported the thermally activated mechanism to turn into a tunneling process below 10 K. However, neither groups studied the physical behavior of the responsible hole defects. Simoen and Clayes also did RTS measurements on pMOSFETs, where they observed the effects of substrate bias on hole capture and emission times [33], [34]. They reported the hole capture time of a Coulombic repulsive center to be significantly affected by the gate bias because of the exponential dependence of hole trap capture cross-section on the transverse field. However, the hole emission times were found to be unaffected by the gate voltage. In another article, the same group measured RTS as a function of gate and drain voltage to extract the trap characteristics such as trap position in the oxide from the Si-SiO_2 interface, and also along the channel [35]. Different trap characterization techniques have been reported to analyze the hole defects that are responsible for several MOSFET degradation mechanisms. Density functional theory (DFT) calculations have shown that E′ centers can trap and de-trap holes [36], [37]. DFT calculations have also suggested E_δ' and E_γ' centers to be the primary reason behind observing 1/f noise in pMOSFETs [38]. Time dependent defect spectroscopy (TDDS) measurements have shown that hydrogen related defects can cause stress-induced leakage current (SILC), and negative temperature bias instability (NBTI) [39], [40]. None of the reported hole defects have been linked with RTS so far. Therefore, there has been a significant lacking regarding the knowledge in physical behavior of hole traps in pMOSFETs that are responsible for RTS. This is the reason why this research primarily focuses on RTS in pMOSFETs i.e. hole defects in silicon dioxide.

Trap generation or deactivation concepts due to hot carrier stress have also been not studied in detail. Bollu *et al*. first applied electrical stress with high drain voltages on MOSFETs, and compared the switching in the device resistance at low temperatures for both damaged and undamaged FETs [41]. They observed that in case of the

undamaged devices, at low temperatures, due to close proximity of the Fermi energy level to the band edge, multiple traps became active at the same time, and the corresponding Lorentzian spectrum due to individual active defects superimposed on each other, whereas for the damaged FET, only discrete switching due to a single trap was present at all the measured temperatures. Other published reports on electrical stressing have confined their investigation to either capture and emission time constants, trap location both from the Si-SiO_2 interface and along the SiO_2 bandgap [42], [43], or modeling of RTS magnitude and channel degradation because of stressing [44], [45]. Application of electrical stressing has resulted in creation of new defects, which play a detrimental role in degrading the device parameters such as threshold voltage and trans-conductance [46], [47]. Ohata *et al.*[21] also observed electrical stress-induced RTS. However, they did not provide any analysis of the stress-induced RTS. Fang and coworkers [42] found a channel hot carrier (CHC) generated trap to reside closer to the oxide-semiconductor interface than the process-induced trap. The stress-induced trap had shorter time constants compared to the process-induced traps, and had a stronger influence on the surface mobility. Later, Kang *et al.*[43] also observed the effect of CHC on RTS in an nMOSFET. They found the trap to stay near the drain terminal along the channel and reported the trap position in the oxide from the oxide-semiconductor interface, and trap energy level with respect to the SiO_2 valence band edge. Simoen *et al.* worked on modeling the channel degradation observed due to application of CHC in pMOSFETs [48], [49]. They found the RTS magnitude to be increasing with the increase of stress time. However, they did not observe any stress-induced traps in their experiments. None of the published articles clearly explain how the defects are generated or activated upon stressing, and how the stress affects the RTS parameters. Therefore, the trap creation or passivation mechanisms are still very unclear to date. In addition, to minimize the effects of hot carriers on output noise, these defects need to be characterized in terms of position and capture cross-section, and their physical behavior needs to be studied thoroughly.

In this research, extensive RTS measurements were done on pMOSFETs of different areas ($\leq$ 1 μm^2) at different temperatures (165 K – 295 K) both in fresh and stressed conditions. Results of this study have been presented in the next chapters. Chapter 2 explains the RTS theories related to the hole traps in pMOSFETs. Chapter 3 includes the experimental setup used, and the measurement procedures followed in this study. Results and analyses of variable temperature RTS measurements in pMOSFETs are presented in Chapter 4. Hot carrier effects on RTS are discussed in Chapter 5. Chapter 6 includes measured flicker noise data and analyses on large area nMOSFETs (>1 μm^2) of different technologies.

1.2 Basic Mechanisms of Electrical Noise

Electrical noise can be termed as any random undesired fluctuation observed in a wanted signal [50]. Such disturbances in electrical signals can be categorized into two types: (i) Noise coming from external sources such as cross-talk between adjacent circuits, vibrations, interference from AC power lines and radio transmitters, and (ii) noise from internal sources, such as random fluctuations of different circuit components. The external noise can be eliminated employing certain methodologies such as proper shielding, designing layout, or using filters. The internal noise, however, can only be suppressed to a certain extent by appropriate designs such as developing equivalent circuit models for the observed noise, studying the physical behavior of the responsible defects for the noise mechanisms, or in case of analog and digital circuits, using differential amplifiers. Noise coming from inherent sources of the devices can be measured and analyzed to study different physical phenomena in electronic devices. Numerous researchers have been using inherent device noise as a technique to characterize the responsible defects. In this section, the discussion has been kept limited to only inherent electrical noise. Fundamental inherent electrical noise mechanisms include thermal noise, shot noise, generation-recombination (G-R) noise, random telegraph signals, and flicker noise.

1.2.1 Thermal Noise

Thermal noise (also known as Johnson noise, or Nyquist noise) originates due to random motion of charge carriers inside a material [51]. Thermal noise was first observed experimentally by J. B. Johnson of Bell Laboratories in 1927, and later analyzed theoretically by H. Nyquist in 1928 [52], [53]. In a conductor or resistor, whenever the temperature goes above 0 K, carrier motions get randomized. Even though the average current in a conductor over a long period of time is zero, the random carrier motions can result in flow of an instant current [50]. The power spectral density (PSD) of a resistor, R is uniform as a function of frequency, and is given by

$$S_I = \frac{4k_B T}{R} \Rightarrow S_V = 4k_B TR \tag{1.1}$$

where k_B is the Boltzmann constant = 1.38×10^{-23} JK^{-1}, and T is the absolute temperature.

1.2.2 Shot Noise

Shot noise is observed due to appearance of random charges flowing across a potential barrier. The current flown through a potential barrier over a specific period of time is determined by the number of charge carriers, each carrying a charge 1.6×10^{-19} C, which gives the amount of observed shot noise. Shot noise is a Poisson process, and was first observed by W. Schottky in a vacuum tube [50]. The shot noise rms value due to a current I_{DC} is given by

$$I_{sh} = \sqrt{2qI_{DC}\Delta f} \tag{1.2}$$

where q is the charge of an electron, and Δf is the noise bandwidth. The noise PSD can be written as

$$S_I = 2qI_{DC} \tag{1.3}$$

Shot noise is observed only if current is flown across a potential barrier such as vacuum tubes, p-n junctions, heterojunctions, and metal-semiconductor contacts.

1.2.3 Generation-Recombination (G-R) Noise

Electronic states that reside within the semiconductor bandgap, and are present because of various defects or impurities in the semiconductor and at its surfaces are known as traps. Generation-Recombination (G-R) Noise is attributed to the fluctuations in number of carriers available for carrier transport due to random capture and emission of these carriers by traps. The G-R noise PSD because of fluctuations in carrier number, ΔN is given by [54]

$$S_N(f) = \frac{4\Delta N^2 \bar{\tau}}{1+(2\pi f)^2 \bar{\tau}^2} \tag{1.4}$$

where f is frequency, and $\bar{\tau}$ is the average time constant associated with the transitions. G-R noise is only important if the trap energy level is within a few $k_B T$ of the Fermi energy level, so that the capture and emission of carriers take place at a similar rate. If the trap energy level is way above or below the Fermi energy level, then the trap will remain empty or filled with most of the time, and hence very few transitions will take place to generate noise.

1.2.4 Random Telegraph Signals (RTS)

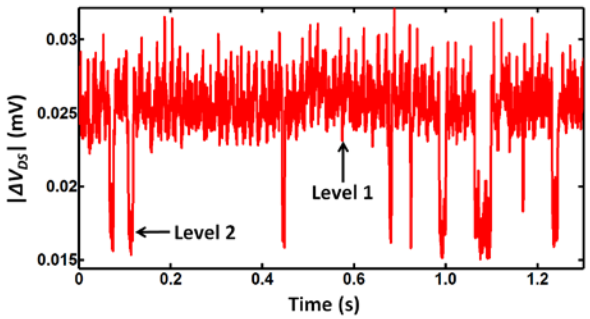


Fig. 1.3 A simple RTS with two levels originated due to a single active oxide trap.

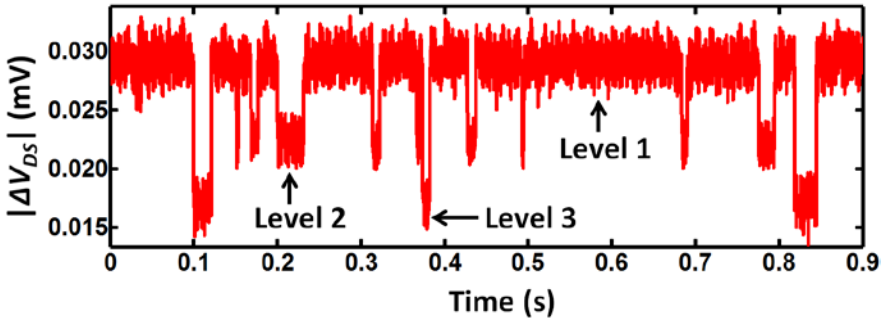


Fig. 1.4 A complex RTS with three levels. Three levels are observed because of two active traps. One trap causes the switching between levels 1 and 2. Switching between levels 1 and 3 takes place due to the other trap.

Random Telegraph Signals (RTS) is a special case of G-R noise, which results in multi-level switching in the device output signal (Fig. 1.3). Random capture and emission of single or multiple carriers by gate oxide defects residing at or near the oxide-semiconductor interface causes discrete switching in the device resistance. RTS can be simple (two levels) (Fig. 1.3), or complex (more than 2 levels) (Fig. 1.4). Trapping and de-trapping of a single active defect result in simple RTS, whereas finding the number of defects in a complex signal is quite complicated. A three-level RTS is usually observed because of two active traps [55] (Fig. 1.4). A four-level signal can be originated because of either two (Fig. 1.5) [56], or three traps (Fig. 1.6). RTS with more than 4 levels is almost impossible to analyze as it becomes very difficult to track the individual transitions. For a two-level signal, if the average time constants at the lower and higher level are $\overline{\tau}_1$ and $\overline{\tau}_2$ respectively, then for a fluctuation in current (ΔI), the noise PSD is given by [29]

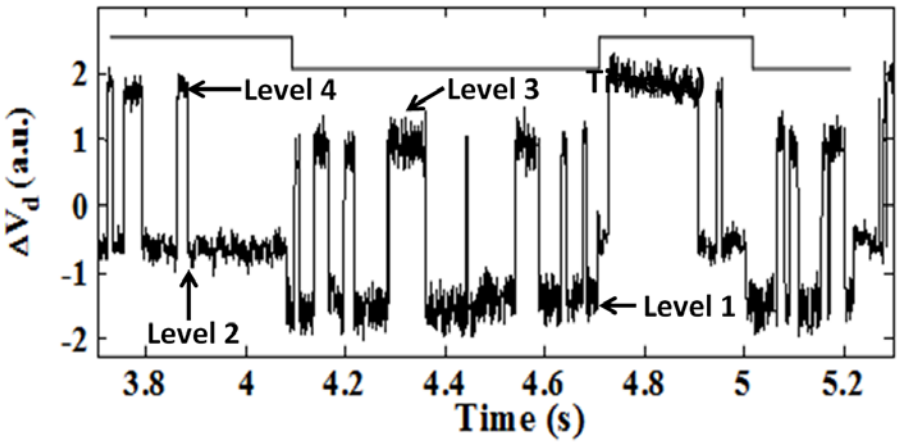


Fig. 1.5 A complex RTS with four levels. Switching because of a fast trap is modulated by switching due to another slow trap. Transitions between levels 1↔3 and 2↔4 take place because of the fast trap, whereas switching between levels 1↔2 and 3↔4 take place due to the slow trap. Such transitions are known as envelope transition [56].

$$S_I(f) = \frac{4(\Delta I)^2}{(\bar{\tau}_1 + \bar{\tau}_2)\left[(1/\bar{\tau}_1 + 1/\bar{\tau}_2)^2 + (2\pi f)^2\right]} \tag{1.5}$$

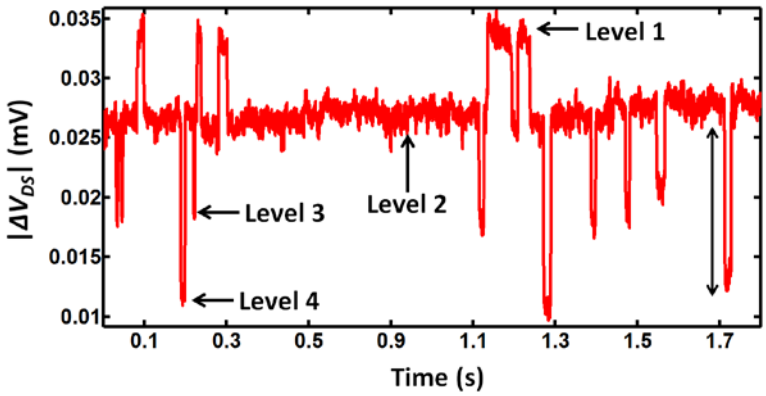


Fig. 1.6 A four-level RTS with three active traps. The first trap causes switching between levels 1 and 2. Transitions between levels 2 and 3 take place because of the second trap. The third trap originates transitions between levels 2 and 4.

The PSD of both RTS and G-R noise is of Lorentzian type (Fig. 1.7). G-R noise can be considered as addition of several RTS of similar time constants. RTS can be observed in time domain only for small number of active traps, and typically observed in small area devices (typically below 1 μm^2). For large number of active traps, Lorentzians due to individual traps with different trapping times get added, and the PSD takes the shape of that of flicker noise.

1.2.5 1/f Noise or Flicker Noise

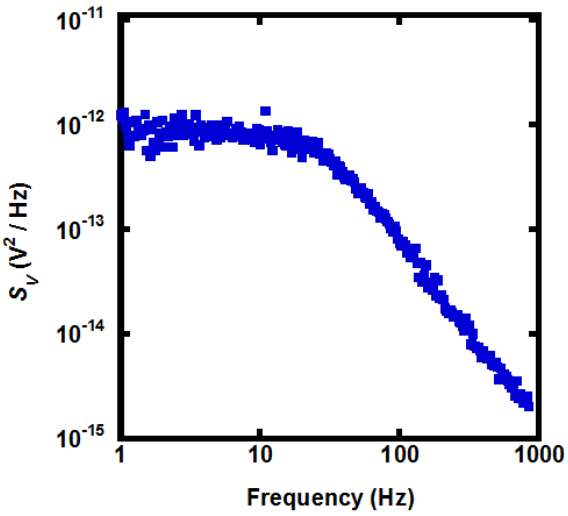


Fig. 1.7 Lorentzian shaped PSD of a simple RTS.

1/f noise or commonly known as flicker noise is observed in electronic devices due to processes that involve wide distribution of time constants such as random capture and emission of carriers, or fluctuations in number and mobility. The noise PSD is proportional to f^{γ} (Fig. 1.8), where γ, the frequency exponent varies between 0.7 and 1.3. The general form of the current PSD is given as

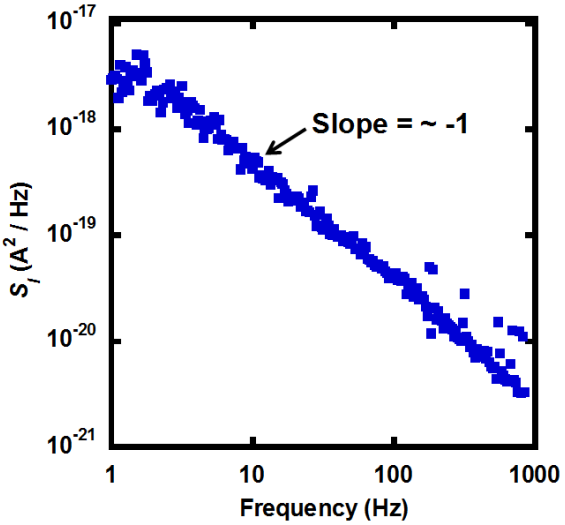


Fig. 1.8 Current PSD depicting flicker noise.

$$S_I = \frac{K_{1/f} I^{\beta}}{f^{\gamma}} \tag{1.6}$$

where $K_{1/f}$ is a constant, and β is the current exponent. Flicker noise is typically observed in the lower part of the frequency spectrum (10^{-5} to 10^{7} Hz) in several conductors and semiconductors [50], [54]. Two mechanisms work behind the current fluctuations: (i) Fluctuations in the number of carriers, or (ii) Fluctuations in carrier mobility.

In the last few decades, articles have been published regarding whether the fluctuations in the number or mobility dominate the flicker noise observed in MOSFETs. Initially the flicker noise was thought to be related to the quality of Si-SiO_2 interface. Hence, the interface trap density and the near interface oxide trap density were considered to be the primary factors behind observing flicker noise [57]. All models developed using this concept fall under number fluctuations theory. However, later, flicker noise observed in nMOSFETs showed excellent match with the number fluctuations theory [58], as well as the bulk mobility fluctuations theory [59], [60]. According to the bulk mobility fluctuations theory, the channel carrier mobility is limited by two mechanisms: lattice scattering, and impurity scattering [61]. The surface induced mobility fluctuations theory, on the other hand, takes into account the scattering between the induced charge carriers with the interfacial traps [62]. Later, it was discovered that upon trapping a channel carrier, fluctuations in the channel carrier number also resulted in a fluctuation in the carrier effective mobility via Coulomb interaction, which is known as correlated mobility fluctuations. Initially, flicker noise observed in the pMOSFETs did not show a good match with the number fluctuations theory [63], [64], [65], [66]. The correlated mobility fluctuation theory was introduced to correct the deviations observed in the number fluctuations model in pMOSFETs [50]. However, as the screening effect was not taken into consideration, that correction factor was reported to be too high to be physical [67]. The screening effect due to the channel carriers, and its effects on the effective channel carrier mobility were later taken into account in the Unified Noise and Mobility Fluctuations theory. The main theories used to explain flicker noise in MOSFETs are discussed in the following sub-sections.

1.2.5.1 Number Fluctuations Theory

Flicker noise due to fluctuation in the number of charge carriers in the MOSFET channel is related to active defects present close to the oxide-semiconductor interface. In 1957, McWorther presented a flicker noise model based on the quantum tunneling transitions taking place between the channel and the gate oxide defects [68]. Since the carrier capture and emission mechanism was considered as an equi-energy tunneling process, and the carrier capture probability by a trap decreases exponentially with the distance from the oxide-semiconductor interface [69], the tunneling time was considered as exponentially varying with distance from the interface. The trap density was taken as uniform with respect to distance and energy to obtain the distribution of time constants responsible for 1/f noise.

When an electron gets captured by an oxide defect, there will be a change in the oxide charge (δQ_{ox}), and the corresponding flat-band voltage, (δV_{FB}). These PSD of these two are related by [70]

$$S_{Q_{ox}} = S_{V_{FB}} C_{ox}^2 \tag{1.7}$$

where C_{ox} is the oxide capacitance per unit area. $S_{Q_{ox}}$ can be evaluated using the G-R noise theory. The general equation for the fluctuation in the number of trapped charges in the oxides with respect to time is given by [54]

$$\frac{dN_{ox}}{dt} = g_n\left(N_{ox}\right) - r_n\left(N_{ox}\right) + \Delta g_n\left(t\right) - \Delta r_n\left(t\right) \tag{1.8}$$

where N_{ox} is the number of trapped charges in the oxide, $g_n\left(N_{ox}\right)$ and $r_n\left(N_{ox}\right)$ are the generation and recombination rates respectively, both being functions of N_{ox}, $\Delta g_n\left(t\right)$ and $\Delta r_n\left(t\right)$ indicate the randomness in the generation and recombination rates. The number of trapped oxide charges can be expressed as $N_{ox} = N_{0_{ox}} + \Delta N_{ox}$, where $N_{0_{ox}}$ and ΔN_{ox} are the equilibrium number of trapped oxide charges and change in the number of trapped oxide charges respectively. At the equilibrium condition, $g_n\left(N_{0_{ox}}\right) = r_n\left(N_{0_{ox}}\right)$. The rate of fluctuation in the trapped oxide charges can be written as [54]

$$\frac{d\Delta N_{ox}}{dt} = \frac{\Delta N_{ox}}{\overline{\tau}} + \Delta g_n\left(t\right) - \Delta r_n\left(t\right) \tag{1.9}$$

Both $\Delta g\left(t\right)$ and $\Delta r\left(t\right)$ show shot noise. Therefore,

$$S_g(f) = S_r(f) = 2g_n\left(N_{0_{ox}}\right) = 2r_n\left(N_{0_{ox}}\right) \tag{1.10}$$

where S_g and S_r are PSDs of shot noise because of randomness in generation and recombination rates respectively. The total PSD of noise due to fluctuations in number of oxide trapped charges is calculated doing the Fourier analysis of Equation (1.9),

$$S_{N_{ox}}(f) = \frac{\overline{\tau}^2}{1+\omega^2\overline{\tau}^2}\left[S_g(f)+S_r(f)\right] = 4g_n\left(N_{0_{ox}}\right)\frac{\overline{\tau}^2}{1+\omega^2\overline{\tau}^2} \tag{1.11}$$

where $\omega = 2\pi f$ is the angular frequency. Again, $\int_0^\infty S_{N_{ox}}(f) = g_n\left(N_{0_{ox}}\right)\overline{\tau} = \overline{\Delta N_{ox}^2}$. Therefore, Equation (1.11) becomes,

$$S_{N_{ox}}(f) = 4\overline{\Delta N_{ox}^2}\frac{\overline{\tau}}{1+\omega^2\overline{\tau}^2} \tag{1.12}$$

Number of trapped oxide charges can be expressed in terms of oxide charge distribution as $Q_{ox} = qN_{ox}/WL$, where Q_{ox} is the oxide charge per unit area. PSDs due to change in oxide charge and change in number of trapped oxide charge are related as $S_{Q_{oxi}} = q^2 S_{N_{ox}}/W^2L^2$, where W and L are channel width and length respectively. Hence, PSD of the G-R noise generated due to a single active trap randomly capturing and emitting channel electrons are given as [50]

$$S_{Q_{oxi}} = \frac{4q^2\overline{\Delta N_{ox}^2}}{W^2L^2}\frac{\overline{\tau}}{1+\left(\omega\overline{\tau}\right)^2} \tag{1.13}$$

$\overline{\Delta N_{ox}}$ is calculated using Fermi-Dirac statistics

$$\overline{N_{ox}^2} = \left(1-f_t(E)\right)f_t(E)N_t \tag{1.14}$$

where $f_t(E)$ is the trap occupancy function. As the total number of traps is not known, the total PSD is found by integrating the individual PSDs with respect to space and energy [50]

$$S_{Q_{ox}} = \int_{E_v}^{E_c}\int_0^{T_{ox}}\int_0^L\int_0^W \frac{4q^2N_t(E,x,y,z)\left(1-f_t(E)\right)f_t(E)}{W^2L^2}\left(\frac{\overline{\tau}}{1+\left(\omega\overline{\tau}\right)^2}\right)dzdydxdE \tag{1.15}$$

where x, y, and z directions are considered as directions into the substrate, along the channel, and along the device width respectively, N_t is the trap density per unit volume per unit energy, T_{ox} is the oxide thickness, E_V and E_C are the silicon valence band and conduction band edges respectively. As mentioned before, in the McWorther model, the trap density is considered to be uniform with respect to space and energy. Therefore, $N_t(x, y, z, E) = N_t$. The product $(1 - f_t(E))\, f_t(E) = -k_B T\, df(E)/dE$ peaks near the Fermi energy level, and acts like a delta function. Hence,

$$S_{Q_{ox}} = \frac{4k_B T q^2}{WL} \int_0^{T_{ox}} N_t \left(\frac{\overline{\tau}}{1 + (\omega \overline{\tau})^2} \right) dx \tag{1.16}$$

The capture time constant for an electron to tunnel to a trap at a distance x from the oxide-semiconductor interface is given by [50]

$$\tau = \tau_0 e^{\lambda x} \tag{1.17}$$

where τ_0 is the characteristic time constant. The tunneling attenuation length (λ) can be found using the Wentzel-Kramers-Brillouin (WKB) theory [50]

$$\lambda = \left[4\pi \sqrt{2 q m_{ox}^* \varphi_0} / h \right] \tag{1.18}$$

where m_{ox}^* is the electron effective mass in the oxide, φ_0 is the difference between Si and SiO_2 conduction band edges at the interface, and h is Planck's constant.

If the oxide is thick enough, then the electron can never tunnel through to the gate-oxide interface. Instead, the tunneled electron keeps fluctuating between the trap and the channel conduction band. Therefore, the limit T_{ox} in (1.16) is replaced by ∞. Therefore, the final PSD becomes

$$S_{Q_{ox}} = \frac{4k_B T q^2 N_t}{\lambda WL f^{\gamma}} \tag{1.19}$$

γ depends on the trap distribution. If the trap density is higher near the oxide-channel interface than in the bulk oxide, then there are more high frequency traps than low frequency traps, leading to γ <1, and γ >1 is expected for the opposite case since there will be more low frequency traps than high frequency traps [50]. γ is taken as unity here since the trap distribution is assumed to be uniform with respect to depth. In terms of trans-conductance (g_m), the drain-source current PSD ($S_{I_{DS}}$) can be written as [70]

$$S_{I_{DS}}(f) = \frac{k_B T q^2 N_t}{\lambda W L f C_{ox}^2} g_m^2 \tag{1.20}$$

1.2.5.2 Mobility Fluctuations Theory

According to Hooge's empirical formula [71], the fluctuations in the drain to source current is observed mainly because of fluctuations in the bulk mobility. The current noise PSD is given by

$$S_I = \frac{\alpha_H I_{DC}^{\beta}}{N f^{\gamma}} = \frac{K_{1/f} I_{DC}^{\beta}}{f^{\gamma}} \tag{1.21}$$

where α_H is the Hooge parameter, which depends on the effective channel electron mobility (μ). In this model, effective channel electron mobility comprises of mobility limited by two physical mechanisms: (i) lattice scattering (μ_{lat}), and (ii) impurity scattering (μ_{imp}). Hooge did not include other mobility limiting mechanisms such as surface roughness, or remote Coulomb scattering because of trapped electrons. According to Mathiessen's Rule, channel electron mobility can be expressed as [71]

$$\frac{1}{\mu} = \frac{1}{\mu_{lat}} + \frac{1}{\mu_{imp}} \tag{1.22}$$

The Hooge parameter can be evaluated using

$$\alpha_H = \left(\frac{\mu}{\mu_{lat}} \right) \alpha_{lat} \tag{1.23}$$

where α_{lat} is the screening coefficient due to lattice scattering. The value of α_H is universally accepted as 2×10^{-3} [72]. However, researchers have found values of α_H one or several orders of magnitude less than 2×10^{-3}, and α_H was also found to be dependent on gate voltage and oxide thickness [73], [74]. While explaining the discrepancies in the values of α_H, Hooge and Vandamme suggested that phonon scattering is the only mechanism behind observing flicker noise, and the other scattering mechanisms reduce the value of α_H [61]. However, this explanation failed to always increase the observed α_H values to the expected value [74].

On the other hand, Ghibaudo *et al.* [70] considered fluctuations in both the number of channel carriers and the correlated effective mobility to be the reason behind observing the drain to source current fluctuations. According to MOSFET theory, change in the number of trapped charges can be represented by change in the MOSFET flat-band voltage. As both number and correlated mobility fluctuations are considered in this theory, the drain-source current fluctuations include fluctuations in both flat-band voltage and effective channel electron mobility is [70]

$$\delta I_{DS} = \frac{\delta I_{DS}}{\delta V_{FB}} \delta V_{FB} + \frac{\delta I_{DS}}{\delta \mu} \frac{\delta \mu}{\delta Q_{ox}} \delta Q_{ox} \tag{1.24}$$

Again,

$$\frac{\delta I_{DS}}{\delta V_{FB}} = -\frac{\delta I_{DS}}{\delta V_{GS}} = -g_m \tag{1.25}$$

In the linear region of operation,

$$\frac{\delta I_{DS}}{\delta \mu} = \frac{I_{DS}}{\mu} \tag{1.26}$$

Combining equations (1.24), (1.25), and (1.26),

$$\delta I_{DS} = -g_m \delta V_{FB} + \frac{I_{DS}}{\mu} \frac{\delta \mu}{\delta Q_{ox}} \delta Q_{ox} \tag{1.27}$$

The scattering coefficient is defined using an expression that reflects the variation in oxide charge with respect to carrier mobility [50]

$$\alpha_m = \frac{1}{\mu^2}\frac{\delta\mu}{\delta Q_{ox}} \tag{1.28}$$

Therefore,

$$\delta I_{DS} = -g_m \delta V_{FB} + \mu\alpha_m I_{DS}\delta Q_{ox} = -g_m \delta V_{FB} + \mu\alpha_m I_{DS}\delta V_{FB} C_{ox} \tag{1.29}$$

The PSD of the drain-source current noise can be expressed as

$$S_{I_{DS}} = S_{V_{FB}}\left(-g_m + \mu\alpha_m I_{DS} C_{ox}\right)^2 \tag{1.30}$$

Therefore, the plot of $\left(S_{I_{DS}}/I_{DS}^2\right)$ will follow the trend of $\left(g_m/I_{DS}\right)^2$ if the number fluctuation term dominates in the drain-source current noise.

1.2.5.3 Unified Number- Mobility Fluctuations Theory

When an inversion layer carrier gets trapped, it changes the number of channel carriers. According to the Unified Number and Mobility Fluctuations (UNMF) model, remote Coulomb scattering due to the charged trap (either at empty or filled state) affects the effective mobility of the channel carriers [72]. In the linear region of operation, the drain-source current in a MOSFET can be expressed as

$$I_{DS} = qW\mu N_{inv} E_y \tag{1.31}$$

where N_{inv} is the inversion layer electron concentration per unit area, and E_y is the applied electric field along the channel. For a small portion of the channel of width W and length Δy, the normalized change in drain-source current can be written as

$$\frac{\delta I_{DS}}{I_{DS}} = -\left(\frac{1}{\Delta N_{inv}}\delta\Delta N_{inv} \pm \frac{1}{\mu}\mu\right) \tag{1.32}$$

where ΔN_{inv} is the inversion layer electron number for that small portion of channel. In strong inversion, the number of inversion layer charge carriers becomes much larger than the number of depletion charge, gate charge, and oxide charges. Therefore, if the charge state of a single trap is changed because of capturing an electron, that charge is most likely to be the inversion charge, and that electron to be the inversion layer electron i.e. $\delta\Delta N_{inv} / \delta\Delta N_t = 1$, where ΔN_t is the number of filled traps. Moreover, $\Delta N_{inv} = W\Delta y N_{inv}$, and $\Delta N_t = W\Delta y N_t$. Equation (1.32) becomes

$$\frac{\delta I_{DS}}{I_{DS}} = -\left(\frac{1}{\Delta N_{inv}}\frac{\delta\Delta N_{inv}}{\delta\Delta N_t} \pm \frac{1}{\mu}\frac{\delta\mu}{\delta\Delta N_t}\right)\delta\Delta N_t \tag{1.33}$$

In this theory, the fluctuations in effective channel electron mobility are considered to be dominated by remote Coulomb scattering caused by captured electron. According to Mathiessen's Rule [72], the effective channel mobility is given by [75]

$$\frac{1}{\mu} = \frac{1}{\mu_{oth}} + \frac{1}{\mu_{ox}} = \frac{1}{\mu_{oth}} + \alpha N_t \tag{1.34}$$

where $\mu_{ox} = 1/\alpha N_t$ is the channel electron mobility limited by oxide charge scattering, and μ_{oth} is the channel electron mobility limited by other mechanism such as surface roughness, lattice scattering, and impurity scattering [76]. Fluctuations in the channel electron mobility due to fluctuation in the number of filled traps can be expressed as

$$\frac{\delta\mu}{\delta N_t} = -\frac{\alpha\mu_{oth}^2}{\left(1+\alpha N_t\mu_{oth}^2\right)} = -\alpha\mu^2 \tag{1.35}$$

Therefore,

$$\frac{\delta I_{DS}}{I_{DS}} = -\left(\frac{1}{W\Delta y N_{inv}} \pm \alpha\mu\frac{1}{W\Delta y}\right)\delta\Delta N_t \rightarrow -\left(\frac{1}{N_{inv}} \pm \alpha\mu\right)\frac{\delta\Delta N_t}{W\Delta y} \tag{1.36}$$

The corresponding noise PSD is given by

$$S_{\Delta I_{DS}} = \left[\frac{I_{DS}}{\Delta N_{inv}}\left(1 \pm \alpha\mu N_{inv}\right)\right]^2 S_{\Delta N_t} \tag{1.37}$$

$S_{\Delta N_t}$ can be found using the number fluctuations theory:

$$S_{\Delta N_t} = 4\int_{E_v}^{E_c}\int_0^W\int_0^{T_{ox}}\int_0^{\Delta y} \Delta N_t^2 \left(\frac{\overline{\tau}}{1+(\omega\overline{\tau})^2}\right) dxdydzdE \tag{1.38}$$

For a defect to get filled with an electron, not only an electron needs to stay at the trap energy level, but also the trap needs to be empty at the same time. Therefore, as discussed before, ΔN_t^2 can be expressed as $\Delta N_t^2 = f_t(E)\left(1-f_t(E)\right)N_t$. Therefore, Equation 1.33 becomes

$$S_{\Delta N_t} = 4\int_{E_v}^{E_c}\int_0^W\int_0^{T_{ox}} N_t(x,y,z,\mathrm{E})\left(1-f_t(E)\right) f_t(E)\Delta y\left(\frac{\overline{\tau}}{1+(\omega\overline{\tau})^2}\right) dxdzdE \tag{1.39}$$

$\left(1-f_t(E)\right) f_t(E) = -k_B T\, df_t(E)/dE$, which peaks near the Fermi energy level, and behaves like a delta function. As discussed before, uniform trap density is assumed here, i.e. $N_t(x,y,z,E) = N_t$. The tunneling capture time constant at a distance x from the Si-SiO_2 interface can be written as $\overline{\tau} = \overline{\tau}_0 e^{\lambda x}$. For thick oxides, the tunneling electron is never able to travel through the entire oxide layer, and that electron keeps moving back and forth from the trap to the conduction band. Hence, the limit T_{ox} can be replaced with ∞. Replacing ω with $2\pi f$, and evaluating the integral in (1.39),

$$S_{\Delta N_t} = \frac{k_B T W \Delta y N_t}{\lambda f} \tag{1.40}$$

The average PSD of I_{DS} because of fluctuation in I_{DS} due to fluctuation in number of carriers in a small portion of Δy along the channel is given as [77]

$$S_{I_{DS}} = \frac{1}{L^2}\int_0^L S_{\Delta I_{DS}} \Delta y dy \tag{1.41}$$

Therefore the drain to source current PSD becomes

$$S_{I_{DS}} = \frac{k_B T I_{DS}^2 N_t}{\lambda f W L}\left(\frac{1}{N_{inv}} \pm \alpha\mu\right)^2 \tag{1.42}$$

Here, '+' sign is used if the trap is a repulsive center (neutral when empty, negatively charged when full), and '-' sign is used if the trap is an attractive center (positively charged when empty, neutral when full). As a repulsive

center defect if negatively charged after capturing an electron, it affects the effective channel electron mobility via remote Coulomb scattering only at the filled state. Hence, a positive change in the fluctuation in the channel electron number causes a positive change in the effective channel electron mobility, resulting in a '+' sign. On the other hand, an attractive center trap is neutral when it is full. Therefore, there is no remote Coulomb scattering when the trap captures an electron. Hence, a positive change in the number fluctuations results in a negative change in the mobility fluctuations, leading to a '-' sign. These two trap types have been explained in detail in the later chapters.

In summary, the basic input electrical noise mechanisms and the relevant theories have been discussed briefly in this chapter. Careful analyses of these noise data can be used to investigate the responsible trap properties. This research confines its limit to low-frequency noise, or more specifically, random telegraph signals. The RTS parameters can provide important trap characteristics that can be used to study the structural behavior of oxide traps. This has been explained further in the following chapters.

Chapter 2 RTS in pMOSFETs

RTS is typically observed in small area devices (≤ 1 μm^2), while flicker noise is observed in devices with large gate areas (> 1 μm^2). Since the number of active defects is decreased in scaled devices, the probability of observing noise in the output signal due to a single active trap increases in small area devices. With the increase in device dimensions, more active traps with similar time constants start to show up, and hence the Lorentzians due to each active defect in the frequency spectrum fall onto one another, resulting in the 1/f noise spectrum. Hole capture and emission mechanism by oxide traps in pMOSFETs is similar to the trapping and de-trapping phenomena in nMOSFETs. However, in case of nMOSFETs, electron emission is due to the the release of a free electron from the trap to the conduction band, while for pMOSFETs, hole emission involves capture of a bonded electron from the valence band. This chapter discusses the theories, as well as RTS and trap characteristic parameters related to the capture and emission of channel holes by oxide defects. Extensive amount of RTS measurements as a function of temperature is required to extract the RTS and trap parameters. Some RTS and hole trap characteristics can be obtained from the measurements at a particular temperature such as average capture times ($\overline{\tau}_c$) and emission times ($\overline{\tau}_e$) , trap energy level with respect to oxide valence band edge ($E_T - E_{V_{ox}}$), trap position into the oxide from the Si-SiO_2 interface (x_T), trap position along the channel (y_T), RTS magnitude (ΔV_{DS}), screened scattering coefficient (α), and trap capture cross-section (σ). However, extraction of the trap energy parameters requires variable temperature RTS measurements. Such parameters include capture activation energy (ΔE_B), change in enthalpy (ΔH), change in entropy (ΔS), and relaxation energy (E_R).

2.1 RTS Theory

Random capture and emission of channel holes by defects at or near the Si-SiO_2 interface are known to be responsible for observing discrete switching in the drain signals of pMOSFETs [29]. RTS analyses provide a useful tool to extract the trapping characteristics of the defects. Some of those trap characteristic parameters are discussed in the following subsections.

2.1.1 Average Capture and Emission Times

Hole capture time is the time span when the trap remains empty, and the emission time indicates the time at which the trap remains filled with a hole [29]. The trap energy level in the SiO_2 bandgap affects the hole capture time, which depends exponentially on the trap energy level with respect to the Fermi energy level. The relation of the trap capture and emission times with the trap energy level comes from the basic Fermi-Dirac distribution. Let $E(n+1/n)$ indicate the defect energy level, where the defect hole occupancy changes from n electrons to $n+1$ electrons. The probability that the defect will be found at the state with $n+1$ holes can be expressed as [29]

$$f_{th} = 1 - f_t = 1 - \left\{ 1 + g \exp\left[\frac{E(n+1/n) - E_F}{k_B T} \right] \right\}^{-1} \tag{2.1}$$

where f_{th} is the trap hole occupancy function, f_t is the trap electron occupancy function, E_F is the Fermi energy level, and g is the trap degeneracy. If the trap at energy level $E(n+1/n)$ generates an RTS with average capture and emission times $\overline{\tau}_c$ and $\overline{\tau}_e$ respectively, then the probability that the defect will be filled with a hole is given by

$$f_{th} = 1 - f_t = 1 - \frac{\overline{\tau}_e}{\overline{\tau}_c + \overline{\tau}_e} = 1 - \left\{ 1 + g \exp\left[\frac{E(n+1/n) - E_F}{k_B T} \right] \right\}^{-1} \tag{2.2}$$

$$\frac{\overline{\tau}_c + \overline{\tau}_e}{\overline{\tau}_c} = \frac{\left\{ 1 + g \exp\left[\frac{E(n+1/n) - E_F}{k_B T} \right] \right\}}{g \exp\left[\frac{E(n+1/n) - E_F}{k_B T} \right]} \tag{2.3}$$

$$\frac{\overline{\tau}_e}{\overline{\tau}_c} = \frac{1}{g \exp\left[\frac{E(n+1/n) - E_F}{k_B T} \right]} \tag{2.4}$$

Denoting the trap energy level as E_T and taking the trap degeneracy factor as unity,

$$\frac{\overline{\tau}_c}{\overline{\tau}_e} = \exp\left[\frac{E_T - E_F}{k_B T} \right] \tag{2.5}$$

For a pMOSFET, with the increase of gate voltage magnitude, the hole occupancy, f_{th} increases. Hence, ($\overline{\tau}_c/\overline{\tau}_e$) decreases with the increase of gate voltage magnitude. This theory can be applied to find out whether the upper level or the lower level of an RTS voltage magnitude corresponds to τ_c [22]. This can be used further to determine the trap charge state before and after the hole capture. This has been explained in detail in Chapter 4, where RTS data analyses are reported.

2.1.2. Trap Energy Level With Respect to Oxide Valence Band Edge

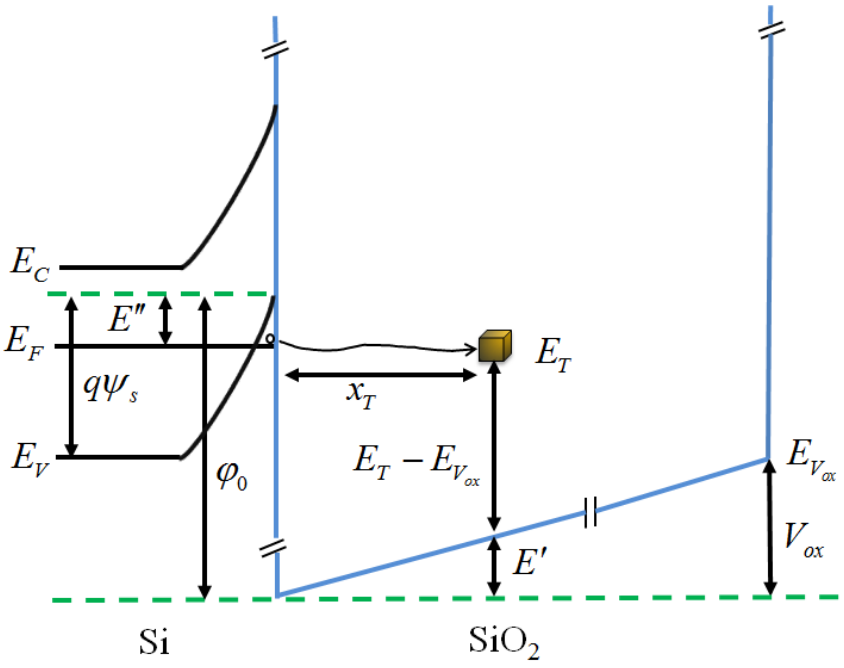


Fig. 2.1 A pMOSFET band diagram at the source terminal.

The band diagram of a typical pMOSFET at the source terminal, and the relevant symbols are shown in Fig. 2.1. According to Fig. 2.1,

$$\frac{E'}{x_T} = \frac{qV_{ox}}{T_{ox}} \tag{2.6}$$

$$E'' = q\psi_s - \left(E_F - E_V\right) \tag{2.7}$$

$$\phi_0 - E'' = E' + \left(E_T - E_{V_{ox}}\right) - \left(E_T - E_F\right) \tag{2.8}$$

where V_{ox} is the amount of band bending inside the oxide. Using the values of E' and E'',

$$E_T - E_F = \frac{qV_{ox}x_T}{T_{ox}} + \left(E_T - E_{V_{ox}}\right) - \phi_0 + E'' \tag{2.9}$$

$$E_T - E_F = \frac{qV_{ox}x_T}{T_{ox}} + \left(E_T - E_{V_{ox}}\right) - \phi_0 + q\psi_s - \left(E_F - E_V\right) \tag{2.10}$$

Now,

$$V_{ox} = V_{GS} - V_{FB} - \psi_s \tag{2.11}$$

where V_{GS} is the applied gate to source voltage. Therefore, combining Equations (2.5) and (2.10),

$$\ln\left(\frac{\overline{\tau}_c}{\overline{\tau}_e}\right) = -\frac{1}{k_B T}\left[\left(E_T - E_{V_{ox}}\right) - \left(E_F - E_V\right) - \phi_0 + q\psi_s + \frac{qx_T}{T_{ox}}\left(V_{GS} - V_{FB} - \psi_s\right)\right] \tag{2.12}$$

Equation 2.12 can be used to calculate $E_T - E_{V_{ox}}$.

2.1.3. Trap Position into the Oxide From the Si-SiO_2 Interface

x_T can be found differentiating equation 2.12 with respect to V_{GS}.

$$x_T = \frac{k_B T T_{ox}}{q}\frac{d\ln\left(\frac{\overline{\tau}_c}{\overline{\tau}_e}\right)}{dV_{GS}} \tag{2.13}$$

If a trap remains active for a high range of gate voltage, then the surface potential changes significantly over the gate voltage range. Therefore, to correctly extract x_T, this change in ψ_s needs to be incorporated while differentiating Equation 2.12 with respect to V_{GS}. Taking this change of ψ_s with respect to V_{GS} into account,

$$\frac{d\ln\left(\overline{\tau}_c/\overline{\tau}_e\right)}{dV_{GS}} = -\frac{1}{k_B T}\left[q\frac{d\psi_s}{dV_{GS}} + \frac{qx_T}{T_{ox}}\left(1 - \frac{d\psi_s}{dV_{GS}}\right)\right] \tag{2.14}$$

$$x_T = \frac{T_{ox}\left[\frac{kT}{q}\frac{d\ln\left(\overline{\tau}_c/\overline{\tau}_e\right)}{dV_{GS}} + \frac{d\psi_s}{dV_{GS}}\right]}{\frac{d\psi_s}{dV_{GS}} - 1} \tag{2.15}$$

2.1.4. Trap Position Along the Channel

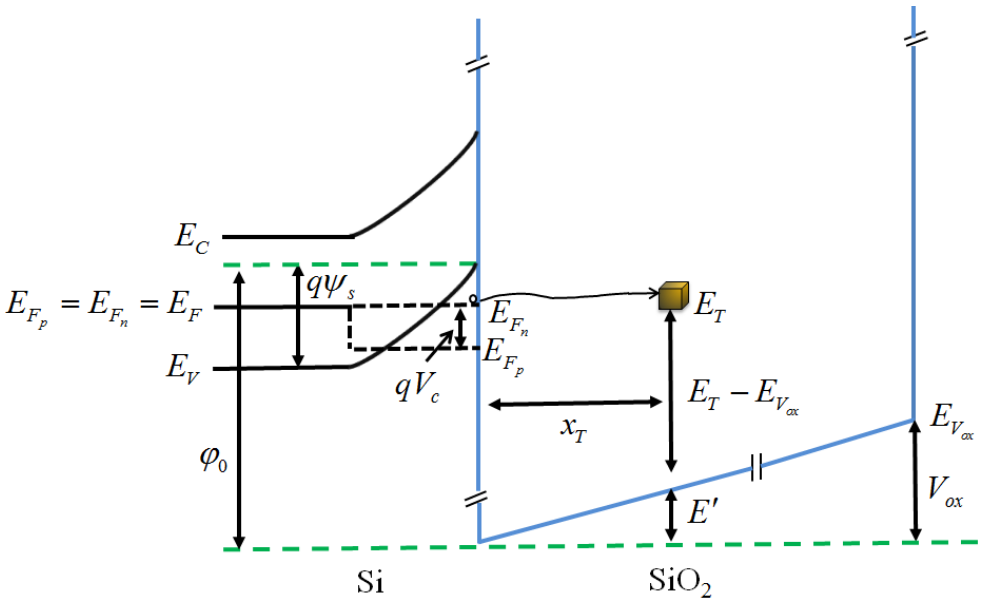


Fig. 2.2 pMOSFET band diagram at the point along the channel where the trap is located.

To extract the trap position along the channel, RTS measurements need to be taken at various drain voltages. If y is a point along the channel measured from the source, and V_C is the channel voltage at that point, then $V_C \approx yV_{DS}/L$ [78], where V_{DS} is the applied drain to source voltage. The band diagram for any point in the channel is shown in Fig. 2.2. The average hole capture and emission times will then be exponentially dependent on the trap energy level with respect to the quasi-Fermi energy level for holes. Therefore, in equation 2.12, E_F and ψ_s will be replaced by ($E_F + qV_C$) and ($\psi_s + V_C$) respectively [79]. Then Equation 2.12 becomes

$$\ln\left(\frac{\bar{\tau}_c}{\bar{\tau}_e}\right) = -\frac{1}{k_B T}\left[\left(E_V - E_F + qV_C\right) + \left(E_T - E_{V_{ox}}\right) - \phi_0 + q\left(\psi_s + V_C\right) + \frac{qx_T}{T_{ox}}\left(V_{GS} - V_{FB} - \psi_s - V_C\right)\right] \qquad (2.16)$$

V_C increases with the increase of V_{DS}, unless saturation mode is reached where the channel length starts to decrease. Therefore, ($\bar{\tau}_c/\bar{\tau}_e$) increases with the increase of V_{DS} in the linear region. Once the saturation mode arrives, ($\bar{\tau}_c/\bar{\tau}_e$) starts to decrease. Hence, ($\bar{\tau}_c/\bar{\tau}_e$) value reaches the maximum on the verge of saturation region. Since V_C depends on y, therefore, the drain voltage at which the maxima of ($\bar{\tau}_c/\bar{\tau}_e$) is observed depends on the

trap location along the channel. In the forward mode, where V_{DS} is applied between the actual drain and source terminals of the device, Equation 2.16 can be written as

$$\ln\left(\frac{\overline{\tau}_c}{\overline{\tau}_e}\right)_f = -\frac{1}{k_B T}\left[\left(E_V - E_F\right)+\left(E_T - E_{V_{ox}}\right)+qV_C-\phi_0+q\psi_s+qV_C+\frac{qx_T}{T_{ox}}\left(V_{GS}-V_{FB}-\psi_s\right)-\frac{qx_T}{T_{ox}}\frac{y}{L}V_{DS_f}\right] \quad (2.17)$$

where V_{DS_f} is the applied drain to source voltage in the forward mode of operation. In the reverse mode of operation, the drain and source terminals are switched. Hence, in the reverse mode of operation, $V_C \approx \left(1-\frac{y}{L}\right)V_{DS}$, and Equation 2.16 can be re-written as

$$\ln\left(\frac{\overline{\tau}_c}{\overline{\tau}_e}\right)_r = -\frac{1}{k_B T}\left[\left(E_V - E_F\right)+\left(E_T - E_{V_{ox}}\right)+qV_C-\phi_0+q\psi_s+qV_C+\frac{qx_T}{T_{ox}}\left(V_{GS}-V_{FB}+\psi_s\right)-\frac{qx_T}{T_{ox}}\left(1-\frac{y}{L}\right)V_{DS_r}\right] \quad (2.18)$$

where V_{DS_r} is the applied drain to source voltage in the reverse mode.

Therefore,

$$\ln\left(\frac{\overline{\tau}_c}{\overline{\tau}_e}\right)_f - \ln\left(\frac{\overline{\tau}_c}{\overline{\tau}_e}\right)_r = \frac{1}{k_B T}\left[q\frac{x_T}{T_{ox}}\frac{y}{L}V_{DS_f} - q\frac{x_T}{T_{ox}}\left(1-\frac{y}{L}\right)V_{DS_r}\right] \quad (2.19)$$

$$\frac{k_B T}{q}\ln\frac{\left(\frac{\overline{\tau}_c}{\overline{\tau}_e}\right)_f}{\left(\frac{\overline{\tau}_c}{\overline{\tau}_e}\right)_r} = \frac{x_T}{T_{ox}}\frac{y}{L}\left(V_{DS_f}+V_{DS_r}\right)-\frac{x_T}{T_{ox}}V_{DS_r} \quad (2.20)$$

Hence, the trap location along the channel can be expressed as

$$\frac{y_T}{L} = \frac{\left(\frac{T_{ox}k_B T}{x_T q}\right)\ln\frac{\left(\frac{\overline{\tau}_c}{\overline{\tau}_e}\right)_{f_{\max}}}{\left(\frac{\overline{\tau}_c}{\overline{\tau}_e}\right)_{r_{\max}}}+V_{DS_{r\max}}}{\left(V_{DS_{f\max}}+V_{DS_{r\max}}\right)} \quad (2.21)$$

2.1.5. RTS Magnitude and Screened Scattering Coefficient

When a channel hole gets trapped, both the number and effective mobility of the inversion layer holes get affected causing a switching in the device resistance. The drain to source current can be expressed as [29]

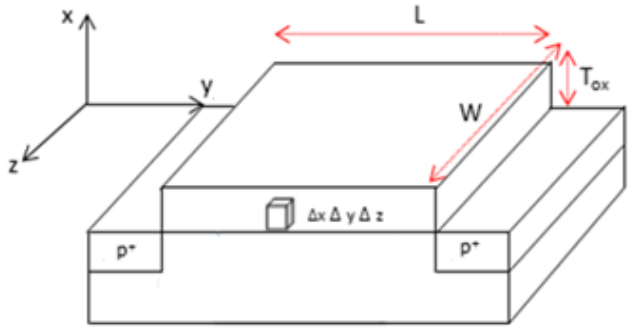


Fig. 2.3 Schematic of a pMOSFET.

$$I_{DS} = W \mu q P_{inv} E_y \tag{2.22}$$

where P_{inv} is the inversion layer hole concentration per unit area. Now, if a section of width W and length Δy in the channel is considered (Fig. 2.3), then for that small portion of the channel,

$$\Delta P_{inv} = P_{inv} W \Delta y \tag{2.23}$$

$$\Delta P_t = P_t W \Delta y \tag{2.24}$$

where ΔP_{inv} and ΔP_t are the number of channel holes and filled traps in the small element respectively. The effective channel hole mobility can be modeled as [75]

$$\frac{1}{\mu} = \frac{1}{\mu_{oth}} + \frac{1}{\mu_{ox}} = \frac{1}{\mu_{oth}} + \alpha P_t \tag{2.25}$$

The effective channel hole mobility is dominated by the screening effect as well as the trap location from the Si-SiO_2 interface [72]. Therefore, $\mu = 1/(\alpha P_t)$, and

$$\frac{\partial \mu}{\partial P_t} = -\frac{1}{\alpha P_t^2} \tag{2.26}$$

$$\partial \mu = -\alpha \mu^2 \partial P_t \tag{2.27}$$

Now,

$$\partial \Delta P_t = \partial P_t W \Delta y \tag{2.28}$$

Therefore,

$$\frac{\partial \mu}{\partial \Delta P_t} = -\left(\frac{\alpha \mu^2}{W \Delta y}\right) \tag{2.29}$$

From Equation 2.22,

$$\partial \Delta I_{DS} = WqE_y \left[\mu \frac{\partial \Delta P_{inv}}{\partial \Delta P_t} \pm \Delta P_{inv} \frac{\partial \mu}{\partial \Delta P_t} \right] \partial \Delta P_t \tag{2.30}$$

Therefore,

$$\frac{\partial \Delta I_{DS}}{I_{DS}} = \left[\frac{1}{\Delta P_{inv}} \frac{\partial \Delta P_{inv}}{\partial \Delta P_t} \pm \frac{1}{\mu} \frac{\partial \mu}{\partial \Delta P_t} \right] \partial \Delta P_t \tag{2.31}$$

Since increase in the number of filled trap decreases the number of channel holes and vice versa, the coupling coefficient between the fluctuations in channel holes to that in filled trap is negative, and in strong inversion, it is close to unity [76]. Hence, $\partial \Delta P_{inv} / \partial \Delta P_t \approx -1$. In addition, for trapping of single inversion layer hole, $\partial \Delta P_t = 1$. Therefore,

$$\frac{\partial \Delta I_{DS}}{I_{DS}} = \left[\frac{1}{P_{inv} W \Delta y}(-1) \pm \left(-\frac{\alpha \mu}{W \Delta y} \right) \right] \partial \Delta P_t \tag{2.32}$$

$$\frac{\partial \Delta I_{DS}}{I_{DS}} = \left[-\frac{1}{\Delta P_{inv}} \pm \alpha \mu \right] \frac{\partial \Delta P_t}{W \Delta y} \tag{2.33}$$

Again,

$$\partial \Delta I_{DS} = \partial I_{DS} \frac{L}{\Delta y} \tag{2.34}$$

Therefore,

$$\frac{\partial I_{DS}}{I_{DS}} = -\left(\frac{1}{\Delta P_{inv}} \pm \alpha \mu \right) \frac{1}{WL} \tag{2.35}$$

In strong inversion,

$$\frac{\Delta V_{DS}}{V_{DS}} \approx \frac{\Delta I_{DS}}{I_{DS}} = -\left(\frac{1}{P_{inv}} \pm \alpha\mu\right)\frac{1}{WL} \tag{2.36}$$

Here, the first term in the parenthesis is called number fluctuations, and the second term is known as mobility fluctuations. The sign between the two fluctuation terms depend on whether the trap is an attractive center, or a repulsive center. Repulsive center traps are neutral in empty state, and become positively charged in filled state. Therefore, the remote Coulomb scattering between the channel holes and the defect filled with a hole increases with the increase in number fluctuations. Hence, the positive sign is used for the repulsive center traps. On the other hand, attractive centers are negatively charged before capturing a hole, and become neutral after trapping a channel hole. Hence, the scattering between the channel holes and the filled defect decreases with the increase in fluctuations in channel holes. Therefore, these two fluctuation terms work in the opposite direction, resulting in a negative sign in Equation 2.36.

The screened scattering coefficient (α) can be calculated using Equation 2.36 once the RTS magnitude is extracted. α can be related with P_{inv} as $\alpha = \alpha_0 + \alpha_1 \ln(P_{inv})$, where α_0 and α_1 are fitting parameters [72]. Since the amount of screening will decrease with the increase of inversion layer hole numbers, therefore $\alpha_1 < 0$.

2.1.6. Trap Capture Cross-section

The hole capture rate for a defect residing at the oxide-semiconductor interface is given by [29]

$$\frac{1}{\overline{\tau}_c} = \int_{-\infty}^{E_V} r(E)dE \tag{2.37}$$

where $r(E)$ is the rate of transition per unit energy at energy E, and can be expressed as product of the particle flux and trap capture cross-section.

$$\frac{1}{\overline{\tau}_c} = \int_{-\infty}^{E_V} p(E)\overline{v}_{th}(E)\sigma(E)dE \tag{2.38}$$

where $p(E)$ is the hole concentration per unit volume per unit energy at energy E, and $\overline{v}_{th}(E)$ is the average thermal velocity of holes at energy E. A more simplified form of Equation 2.38 is used for calculation, where the hole concentration, mean thermal energy, and trap capture cross-section are considered uniform with respect to energy. Hence,

$$\frac{1}{\overline{\tau}_c} = p\overline{v}_{th}\sigma \tag{2.39}$$

Therefore, σ can be calculated using the extracted mean capture time of RTS.

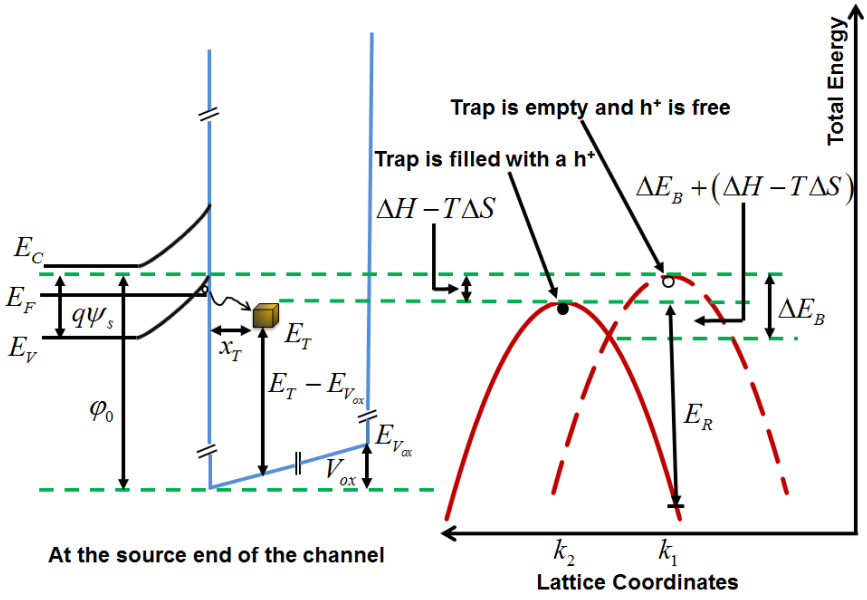


Fig 2.4 Configuration coordinate diagram of a pMOSFET with all trap energy parameters.

The hole capture and emission by oxide defects is a phonon assisted tunneling process [29]. Before trapping an inversion layer hole, the defect undergoes thermal vibrations. This thermal vibration is accompanied by vibrations from the surrounding lattice particles. This phenomenon helps the channel hole to get captured by the defect [11]. In order to get captured, the hole needs to cross a certain barrier, known as capture activation energy (ΔE_B). Upon getting trapped, the hole relaxes to the trap energy level, thereby emitting several phonons, which is related to the structural relaxation energy of the defect (E_R). To get released back to the valence band, the hole

trapped hole needs to obtain a certain amount of energy, known as emission energy. The excess energy from the hole capture and emission process is Gibbs free energy, which can be divided in to two parts: trap binding enthalpy (ΔH), and change in entropy (ΔS). This excess energy also gives the trap energy level with respect to the silicon valence band edge (ΔE_{TV}). The complete hole trapping and de-trapping process, along with the trap energy parameters are shown in Fig. 2.4.

2.1.7. Capture Activation Energy

Trap capture activation energy (ΔE_B) is an important trap energy parameter that can be used to study the structural behavior of the trap. Hole capture rate is largely affected by ΔE_B . In general, traps with higher ΔE_B show slower RTS than traps with lower ΔE_B values. ΔE_B can be related to the trap capture cross-section as [29]

$$\sigma = \sigma_0 e^{\left(-\Delta E_B / k_B T\right)} \tag{2.40}$$

where σ_0 is the trap capture cross-section pre-factor. It is obvious from Equation 2.40 that the Arrhenius plot of σ can be used to obtain both σ_0 , and ΔE_B .

2.1.8. Change in Enthalpy and Entropy

In the linear region of MOSFET operation, the drain to source current is given as [29]

$$I_{DS}(T) = p(T) q \mu(T) V_{DS} t(T) W/L \tag{2.41}$$

where t is the inversion layer thickness. The effective channel hole mobility and inversion layer thickness is dependent on temperature, and this dependence can be expressed as [29]

$$\mu(T) = \mu_0 T^{-3/2} \tag{2.42}$$

$$t(T) = t_0 T \tag{2.43}$$

where μ_0 and t_0 are the effective channel hole mobility and inversion layer thickness at zero Kelvin temperature. Combining Equations 2.41, 2.42, and 2.43,

$$p(T) = \frac{I_{DS}(T)T^{1/2}}{q\mu_0 V_{DS} t_0 (W/L)} \tag{2.44}$$

Mean thermal hole velocity can be expressed as

$$\overline{v}_{th} = \left(8k_B T/\pi m_p^*\right)^{1/2} \tag{2.45}$$

where m_p^* is the hole effective mass. Combining Equations 2.39, 2.40, 2.44, and 2.45,

$$\overline{\tau}_c = \frac{q\mu_0 V_{DS} t_0 (W/L)\exp(\Delta E_B/k_B T)}{\sigma_0 \left(8k_B T/\pi m_p^*\right)^{1/2} I_{DS}(T) T^{1/2}} \tag{2.46}$$

Again, for holes,

$$\frac{\overline{\tau}_e}{\overline{\tau}_c} = \frac{1}{g}\exp\left[-\frac{E_T - E_F}{k_B T}\right] \tag{2.47}$$

Therefore,

$$\overline{\tau}_c = \frac{\exp(\Delta E_B/k_B T)\exp(E_T - E_F/k_B T)}{g\sigma_0 \left(8k_B T/\pi m_p^*\right)^{1/2} p(T)} \tag{2.48}$$

The inversion layer hole density can be expressed as

$$p(T) = N_V\left[\frac{E_V - E_F}{k_B T}\right] \tag{2.49}$$

Hence,

$$\overline{\tau}_e = \frac{\exp\left[\left(\Delta E_B + \Delta E_{TV}/k_B T\right)\right]}{g\sigma_0 \left(8k_B T/\pi m_p^*\right)^{1/2} N_V} \tag{2.50}$$

$\Delta E_{TV} = E_T - E_V$ can be written in terms of trap binding enthalpy and change in entropy as $\Delta E_{TV} = \Delta H - T\Delta S$ [29].

Therefore, from Equation (2.50),

$$\overline{\tau}_e = \left(\frac{1}{g\sigma_0 \left(8k_B T/\pi m_p^*\right)^{1/2} N_V \exp(\Delta S/k_B T)}\right)\exp\left[\left(\Delta E_B + \Delta H/k_B T\right)\right] \tag{2.51}$$

Therefore, from the Arrhenius plot of $\overline{\tau}_e(T) N_V(T)\left[T/\left(m_p^*(T)\right)\right]^{1/2}$, ($\Delta E_B + \Delta H$), and ΔS can be extracted. ΔH can be easily calculated since ΔE_B is already known from the Arrhenius plot of σ. ΔH and ΔS provide

information about the internal energy and structural disorder of the system. Positive ΔH indicates an endothermic process i.e. hole emission is followed by heat absorption in the system, whereas negative ΔH means that the process is exothermic, and heat is evolved from the system following hole emission. Positive value of ΔS means that the system is more disordered when the hole is emitted back to the channel. Negative ΔS indicates less structural disorder in the system after hole emission.

2.1.9. Relaxation Energy

Another important trap identification energy parameter is relaxation energy (E_R). E_R can be expressed using the parabolic approximation of the $E-k$ diagram of the system (Fig. 2.4). According to Fig. 2.4, equating the two parabolas at $k_1 = 0$,

$$K^2 = \left(K - K_2\right)^2 + \left(\Delta H - T\Delta S\right) \tag{2.52}$$

If the two parabolas intersect each other at the point K_c , then,

$$K_c{}^2 = \left(K_c - K_2\right)^2 + \left(\Delta H - T\Delta S\right) \tag{2.53}$$

From the two curves, $E_{\mathrm{R}} = K_2^2, \Delta E_B = K_c^2$. Therefore,

$$K_c{}^2 = K_c{}^2 - 2K_cK_2 + K_2^2 + \left(\Delta H - T\Delta S\right) \tag{2.54}$$

$$4K_c^2K_2^2 = \left(E_R + \left(\Delta H - T\Delta S\right)\right)^2 \tag{2.55}$$

$$\Delta E_B = \frac{\left(E_R + \left(\Delta H - T\Delta S\right)\right)^2}{4E_R} \tag{2.56}$$

The temperature dependent trap energy parameters provide important information for identifying the physical structure of the defects responsible for RTS. In addition to the multi-phonon assisted tunneling mechanism explained in this chapter, quantum tunneling is also possible between the two states shown in Fig. 2.4 [80], [81]. However, to exhibit RTS, a trap needs to be very close to the silicon valence band edge. For those small values of ($E_T - E_V$), the tunneling process would be too fast to be observed in the time frame used for RTS [82]. This

supports the observation of Scofield *et al.* [32], where they found the tunneling mechanism to be responsible for hole capture and emission only below 10 K, when the trap carriers slow down by several orders of magnitude.

The RTS theories required for RTS data analyses have been discussed in this chapter. Application of these theories allows identification and analyses of the physical structure and behavior of the hole traps responsible for RTS in pMOSFETs. Detailed analyses of the actual defect species identified using the trap parameters such as ΔE_B, E_R, ($E_T - E_{V_{ox}}$) have been presented in the following chapters.

Chapter 3 Noise Measurement Procedure

In order to characterize the defects correctly, it is very important to have robust RTS data and distinct RTS levels in the measured signal. As noise and interference from both internal and external sources in the setup can corrupt the RTS data, it is very important to follow certain precautions while taking measurements to minimize those undesired effects. The 60 Hz frequency components from the power line will also overlap with the output signal if steps are not taken to eliminate that. It is also essential to protect the devices from electrostatic discharge (ESD). During taking the noise measurements, appropriate techniques were used to encounter the aforementioned issues.

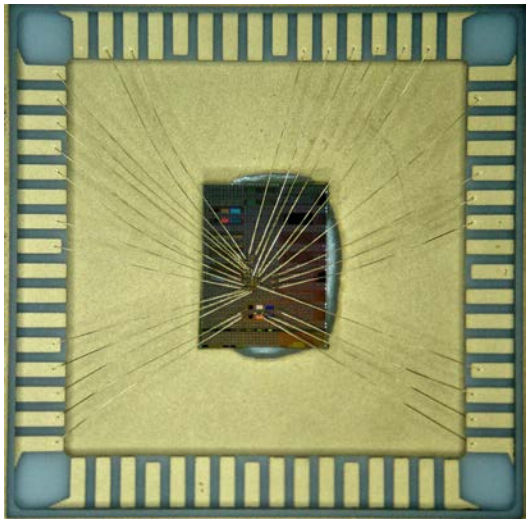


Fig. 3.1 Packaged chip where several devices are connected to the external leads.

At the wafer level, to isolate the device under test (DUT) from the external environment, a Micromanipulator 8600 series probe station was used. Once the functionality was verified and observation of RTS was confirmed in several devices, the wafer was diced into several dies and packaged to place it inside the cryostat (Fig. 3.1). Most of the experimental setup is placed inside a metallic shielded room (Fig. 3.2) to minimize the electromagnetic interference from the outside to the environment of the DUT in the cryostat. To protect the DUT from ESD, all the leads of that device were connected at the same potential when no experiment was going on. To bias the devices, a custom made, DC battery operated biasing circuitry was used (Fig. 3.3). While taking the measurements, static charges may flow into the terminals of the DUT and degrade the device. To prevent this, the device was always

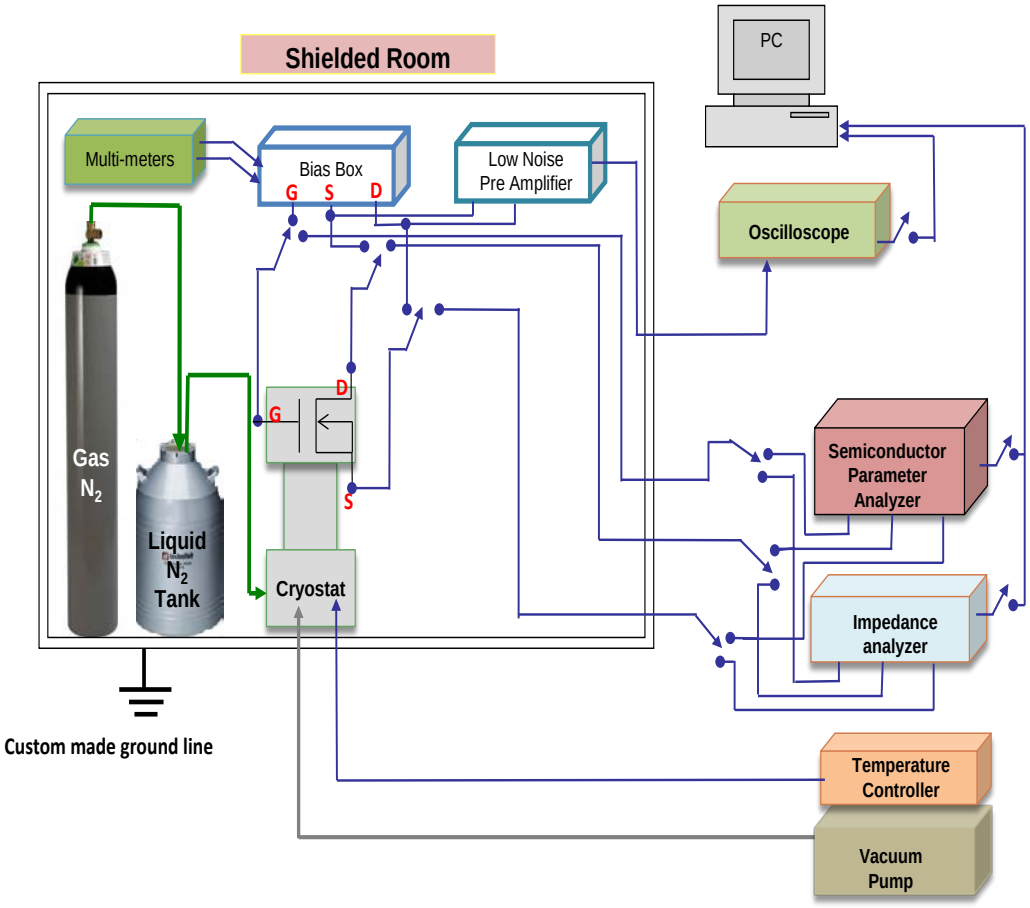


Fig. 3.2 RTS measurement setup.

handled using a static wrist strap. To eliminate the effect of the 60 Hz component originating from the power line, all DC operated equipment such as the biasing circuitry, preamplifier were placed inside the shielded room, while the AC operated equipment such as the semiconductor parameter analyzer (SPA), oscilloscope were placed outside the shielded room. The shielded room was kept completely closed during the noise measurements to minimize interferences from outside.

The variable temperature measurements were done with an open end flow system, where liquid nitrogen evaporation was used as the cooling method. The pressure at which the liquid nitrogen is released from the dewar had to be adjusted carefully for lowering the temperature accurately. To precisely control the temperature, a liquid nitrogen gas cylinder was kept inside the shielded room. A Matheson-Trigas dual stage general purpose pressure regulator regulated the pressure between the gas cylinder and the dewar at the dewar inlet. Liquid nitrogen was

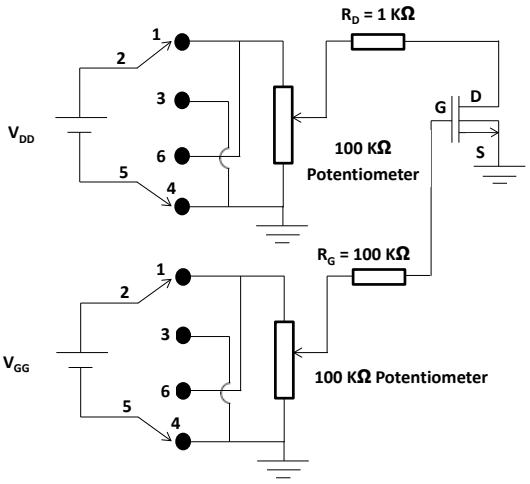


Fig. 3.3 Biasing circuitry used in the RTS measurement.

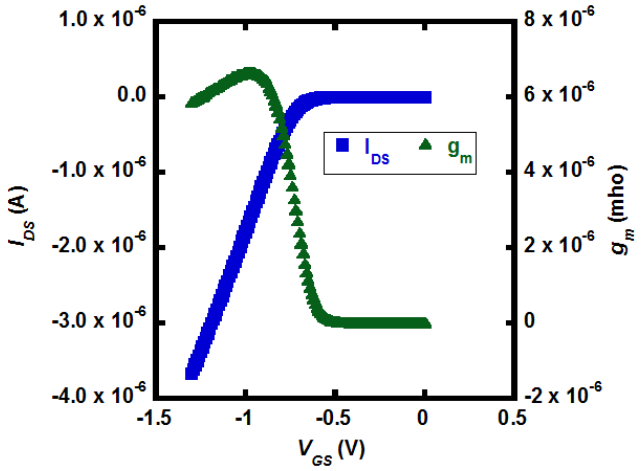


Fig. 3.4 Plot of drain-source current (I_{DS}) and transconductance (g_m) as a function of V_{GS} for a pMOSFET.

flown from a refillable liquid nitrogen dewar. Heat was applied using a wire wound resistive heater, which was located at the base of the stage where the DUT was placed. A Lakeshore 330 Autotuning Temperature Controller, which includes a PID controller, helped to obtain the desired temperature control. The proportional, integral, and differential constants were varied independently to make the temperature stable. The whole measurement consists of three steps: extraction of DC characteristics, extraction of C-V characteristics, and measurement of noise.

3.1 Extraction of DC Characteristics

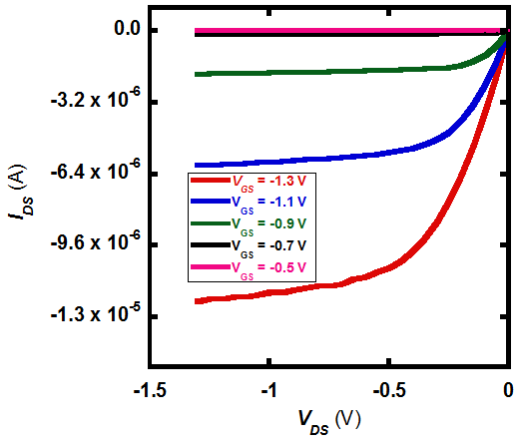


Fig. 3.5 Plot of I_{DS} as a function of V_{DS} at different V_{GS} for a pMOSFET.

DC parameters of the DUT such as drain current (I_D), trans-conductance (g_m), and channel conductance (g_D) were found with an Agilent 4156A SPA. Plot of I_{DS} and g_m as a function of both V_{GS} (Fig. 3.4) and V_{DS} (Fig. 3.5) were observed to verify the device functionality. The threshold voltage, V_T was determined from the x-axis intercept of the tangent drawn on $\sqrt{I_{DS}}$ at the point where $d\sqrt{I_{DS}}/dV_{GS}$ is minimum (Fig. 3.6). The aforementioned DC parameters were obtained following the same procedure at each temperature at which RTS was found.

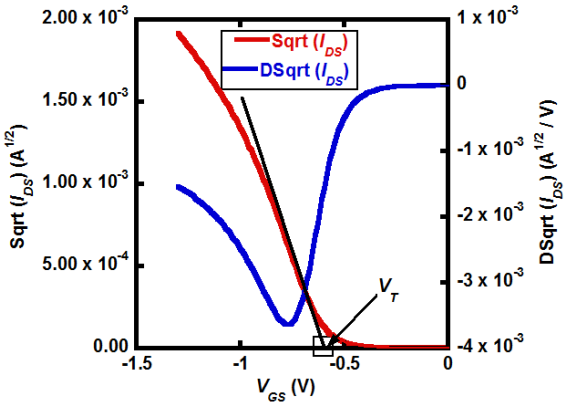


Fig. 3.6 Extraction of V_T in a pMOSFET. V_T is evaluated from the x-axis intercept of the tangent drawn on $(I_{DS})^{1/2}$ at the point where minimum of $d(I_{DS})^{1/2}/dV_{GS}$ occurs.

3.2 C-V Characteristics

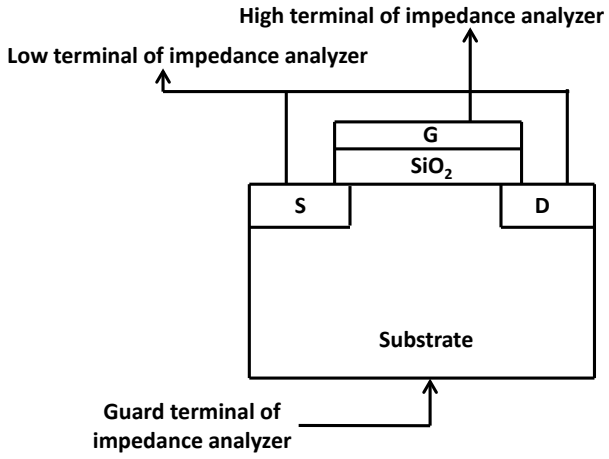


Fig. 3.7 Setup for extraction of C-V characteristics.

The C-V characteristics were plotted with the data obtained from an Agilent 4294A impedance analyzer. The C-V characteristic curve allowed calculating the oxide thickness. The gate to channel capacitance (C_{GC}) was measured by connecting the gate terminal to high end of the impedance analyzer, and drain and source to the low end of the impedance analyzer (Fig. 3.7). The total inversion layer charge (Q_{inv}) was obtained calculating the total area under the C-V curve. The inversion layer hole concentration was determined using [83]

$$P_{inv} = Q_{inv}\left(V_{GS}\right) = q\int_{0}^{V_{GS}} C_{GC}\left(V_{GS}\right)dV \tag{3.1}$$

The effective channel length (L_{eff}) was found through [83]

$$L_{eff} = L\left(1-\frac{C_{GC_{ov}}}{C_{GC_{inv}}}\right) \tag{3.2}$$

where $C_{GC_{ov}}$ and $C_{GC_{inv}}$ are gate to channel overlap capacitance, and gate to channel capacitance in the inversion region respectively. Finally, the oxide thickness (T_{ox}) was computed using $T_{ox} = \varepsilon_0\varepsilon_{SiO_2}/C_{ox}$, where C_{ox} is the

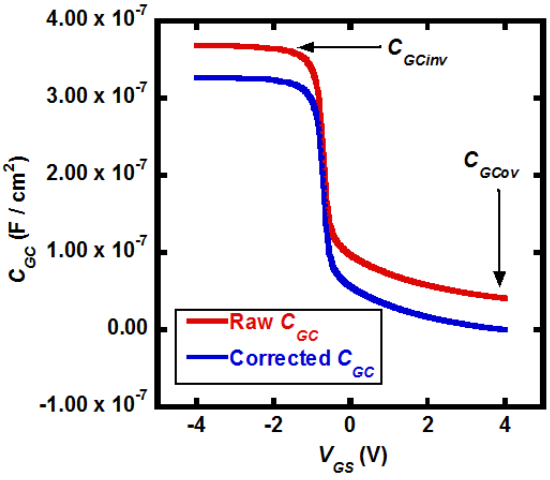


Fig. 3.8 C-V characteristics of a MOS capacitor.

corrected gate to channel capacitance obtained by subtracting the overlap capacitance from the raw gate to channel capacitance (Fig. 3.8), ε_0 is the permittivity of free space, and ε_{SiO_2} is the dielectric constant of silicon dioxide.

3.3 RTS Measurement Procedure

After verifying the DC characteristics and finding the C-V curve, RTS measurements were done at room temperature. After mounting the DUT in the cryostat, the effect of ESD was eliminated with the help of four metallic test clips so that all the leads had the same known voltage (Fig. 3.9). The leads were disconnected from the outer frame of the package with care so that the metallic clips connected to the leads do not come out. Then, the leads were connected to the cryostat connectors via four pin socket connectors (Fig. 3.10). The metallic test clips were taken out one by one with caution. All four terminals i.e. gate, source, drain and substrate were shorted together while connecting the test clips and disconnecting the device leads. Before applying bias to the device, the connections that shorted the four device terminals were taken out. The V_{GS} and V_{DS} were varied to find a suitable bias range in which an RTS was observed. Once the devices were biased, the output signal was amplified through an EG&G PAR113 low-noise preamplifier before feeding to an Agilent 54832B oscilloscope. The preamplifier was

operated in the AC coupling mode to suppress the DC components from the output signal. The source and substrate terminals were connected to the virtual ground of the biasing circuitry. However, grounding the substrate of the

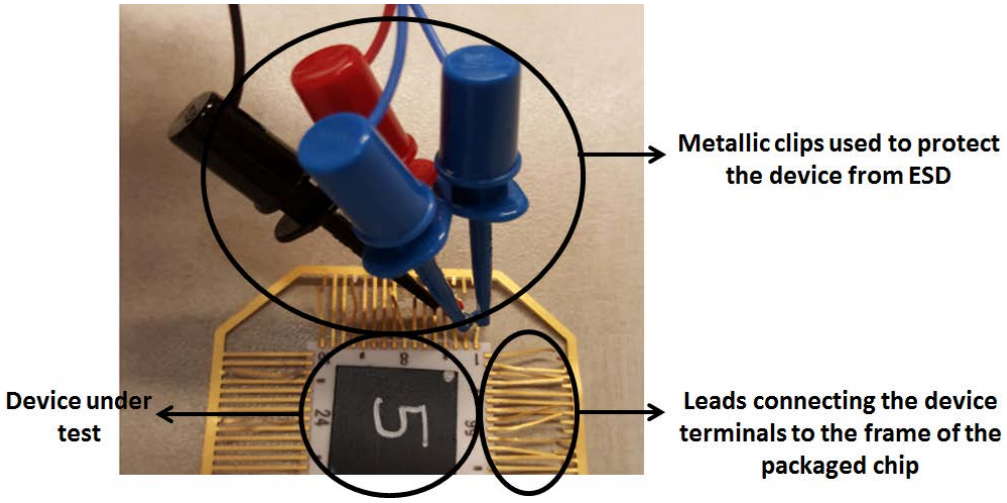


Fig. 3.9 Connection of metallic clips to the leads of the DUT in packaged die.

device to the virtual ground of the biasing box was not enough to quiet the extraneous noise which interfered with the RTS. The terminals needed to be connected to the actual ground, which was in turn connected outside the central system. Once an RTS was observed, measurements were taken at 8-10 bias points varying the V_{GS} and keeping the V_{DS} constant, all in the linear region of pMOSFET operation. The sampling frequency of the oscilloscope (F_S) is calculated using $F_S = N_p / T_t$, where N_p is the number of total points, and T_t is the length of the total time span of the signal. While recording the RTS traces, selection of the appropriate sampling frequency is essential. Lower sampling frequency will result in loss of observed switching events, while too many samples will add unnecessary points to the signal. The sampling frequency, as well as the time span was varied in such a way so that at least 500 switching events were present in each RTS trace. At low temperatures, the capture and emission processes slow down be several orders of magnitude because of lower carrier energy. Hence, it is very difficult to obtain 500 transitions between the RTS levels even in the maximum signal time span of the oscilloscope. In those cases, multiple traces for that bias point were recorded. These traces were then stitched together during the RTS analyses.

After finishing the room temperature RTS measurements, the temperature was dropped at different intervals. The cryostat pressure was kept below 65mTorr using a vacuum pump. The proportional, integral, and differential gains of the Lakeshore 330 temperature controller were fixed at 350, 50, and 0 respectively to have the optimal

temperature control [84]. After obtaining the desired vacuum level around 40 µm Hg, the liquid nitrogen and nitrogen gas cylinder nozzles were opened slowly to prevent liquid nitrogen overflow. The temperature controller display monitor was used to note down the temperature inside the cryostat. By trial and error, it was observed that for a pressure of nitrogen gas flow between 8 and 12 psi resulted in optimum cooling. Therefore, the nitrogen gas

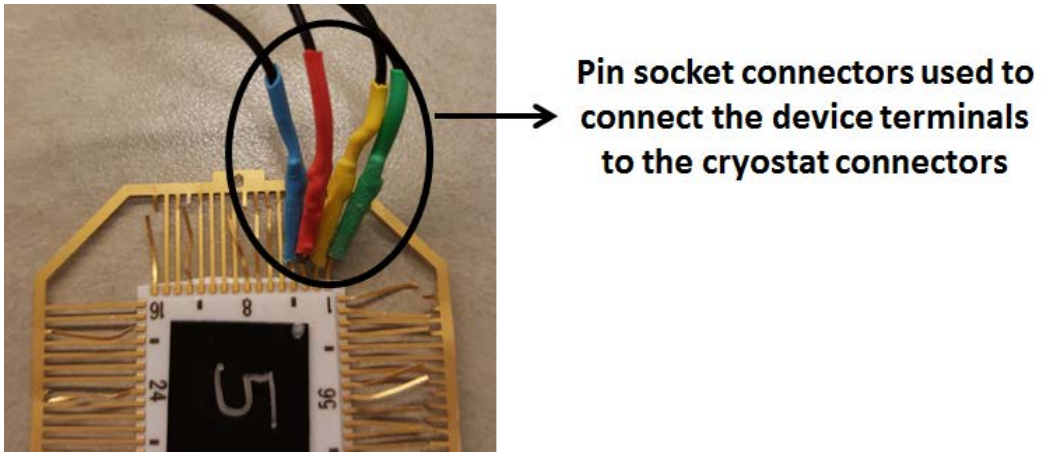


Fig. 3.10 Connection of pin socket connectors to the leads of the DUT in packaged die.

cylinder gauge pressure was set to between 8 and 12 psi. This pressure is very important for precise control of temperature. If less pressure is applied, the temperature will longer than usual to get fixed at the desired value. Application of too much pressure will result in the wastage of nitrogen gas.

3.4 Flicker Noise Measurements

The flicker noise measurements were taken at room temperature with the devices placed in the Micromanipulator 8600 series probe station. The flicker noise measurements were done with the same setup explained earlier. A HP 3562A dynamic signal analyzer, interfaced with a computer provided the flicker noise PSD. The PSD was obtained for three decades of frequency (Fig. 3.11). When there is no current flowing in a MOSFET, noise coming from the system background will be observed at the output, which includes noise coming from the preamplifier, 60 Hz power line, biasing circuitry, contact of the probe tips, and device thermal noise. PSD for background noise at each bias point was extracted, and was subtracted from the overall flicker noise during analyses

(Fig. 3.11). The AC power cord of the signal analyzer was grounded to the actual ground outside the system through a power outlet. This helped to reduce the effects of harmonics of the 60 Hz signal on the overall noise.

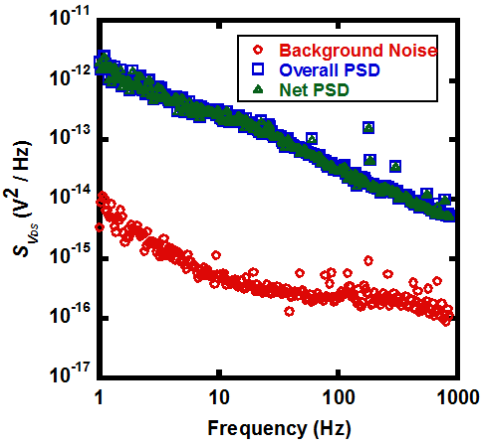


Fig. 3.11 Measured background noise, overall PSD and the subtracted net PSD of an nMOSFET.

3.5 Stress Procedure

To analyze the effects of hot carriers on RTS and trap characteristics, the devices were stressed using the Agilent 4156A SPA. RTS measurements were done at variable temperatures. However, the devices were stressed

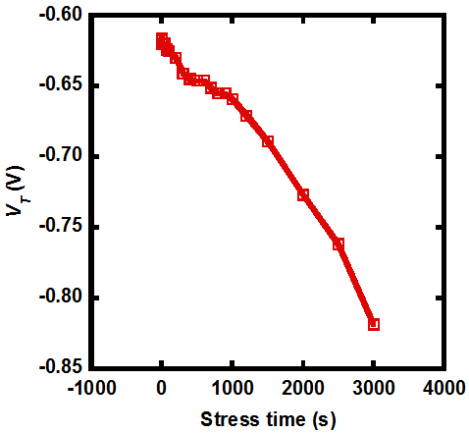


Fig. 3.12 Threshold voltage degradation with stress time for a pMOSFET.

only at room temperature so that the carriers have sufficient energy to degrade the DC characteristics. After completing the variable temperature RTS measurements at a particular stress interval, the device temperature was allowed to come up to the room temperature before any further stressing was done. After each stressing interval, the

aforementioned DC characteristic parameters were recorded. Stress was applied at different intervals until around 30% degradation on the threshold voltage (V_T) was observed (Fig. 3.12).

This Chapter describes all the necessary techniques followed during RTS and flicker noise measurements. The accuracy of the noise analyses covered in the next Chapters highly depends on the minimization of outside interferences in the recorded noise data. The setups and measurement procedures described in this Chapter certainly ensure to obtain noise data with negligible overlap with outside disturbances.

Chapter 4 RTS Results and Analyses

RTS is observed because of alternate capture and emission of channel carriers by defects residing near the Si-SiO_2 interface and in SiO_2. RTS can be used as a technique to characterize the gate oxide defects. However, in order to extract the defect characteristics, it is essential to correctly analyze the measured RTS data. First step is to find out if the responsible trap is an attractive center (negatively charged when empty, neutral when full), or a repulsive center (neutral when empty, positively charged when full). Consequentially, careful analyses need to be carried out to determine whether the upper level or the lower level of the RTS corresponds to the capture time. For RTS with more than two levels, extraction of time constants for each RTS level is also very important. This chapter focuses on the RTS data obtained from measurements at variable temperatures, and their analyses.

4.1 Device Specifications and Measurement Conditions

RTS measurements at variable temperatures were taken on 15 pMOSFETs in total from room temperature down to 165 K, all in linear region of operation. Representative results of 4 devices are presented here. The devices

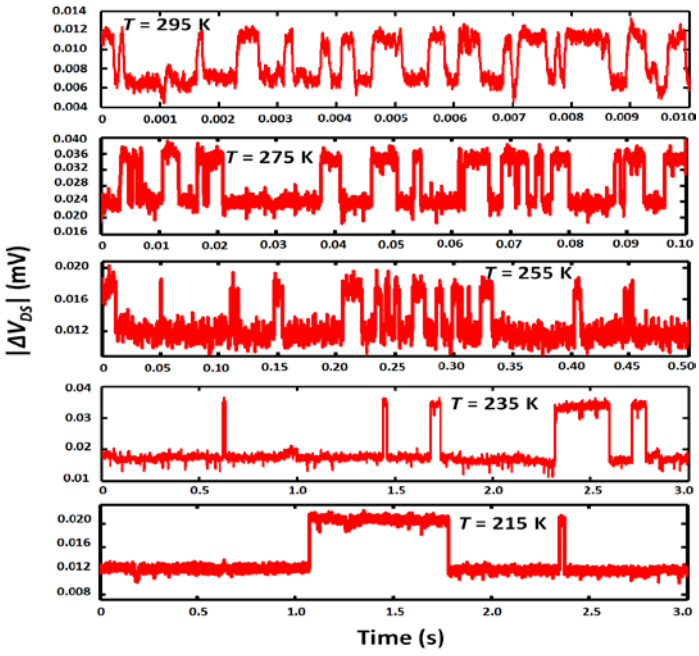


Fig. 4.1 Sample RTS observed in PMOS50 at different temperatures. V_{GS}= -1.5 V, V_{DS}= -0.4 V.

are named as PMOS500 ($W \times L$ = 1 µm × 0.5 µm), PMOS550 ($W \times L$ = 1 µm × 0.55 µm), PMOS600 ($W \times L$ = 1 µm × 0.6 µm), and PMOS700 ($W \times L$ = 1 µm × 0.7 µm). For the device PMOS700, the measurement conditions were T = 245–295 K, V_{GS} = -1.8 to -2.3 V, and V_{DS} = -0.5 V. For PMOS550, RTS was observed at T = 215-295 K, V_{GS} = -1.5 to -2.3 V, and V_{DS} = -0.4 V. For PMOS600, the bias and temperature conditions were T = 215-295 K, V_{GS} = -1.65 to -1.9 V, and V_{DS} = -0.5 V. For PMOS500, the RTS was present at T = 175-265 K, V_{GS} = -2.15 to -2.5 V, and V_{DS} = -0.5 V. A sample two-level RTS recorded in the device PMOS550 at different temperatures are shown in Fig. 4.1. Similar two-level RTS was found in all four devices in the measured temperature and bias ranges mentioned above. Observation of two-level RTS indicates that a single trap is responsible for RTS in each device. All devices were 5 V rated. The oxide thickness of the devices was measured to be 12.1 nm.

4.2 Average Capture and Emission Times

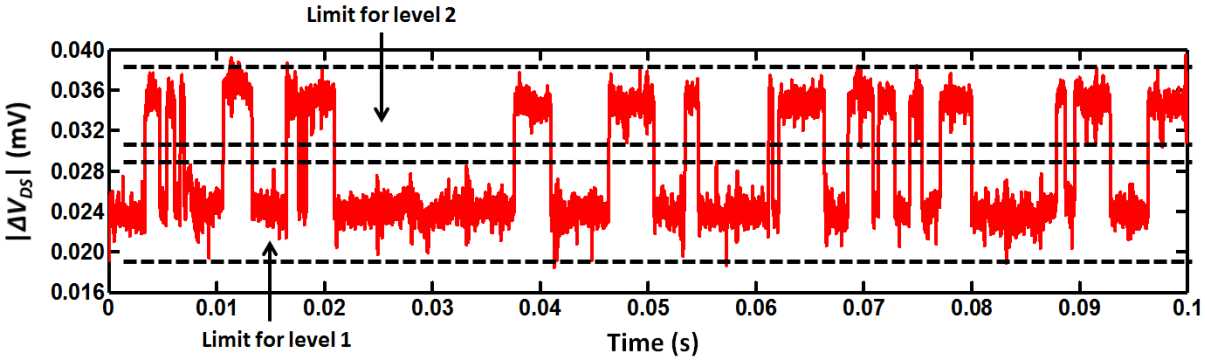


Fig. 4.2 Defining limits for each RTS level.

RTS analyses started with defining a high and low limit for each of the RTS levels (Fig. 4.2). A MATLAB code was developed to compute the time spent at each RTS level for each switching event. The probability to switch from one RTS level to another follows Poisson's statistics, and the time spent at each RTS level follows an exponential distribution (Fig. 4.3) [56], [85]. The average time spent at each level was calculated using $\bar{\tau} = \sum_{m=1}^{M} t_m |F_m| \Big/ \sum_{m=1}^{M} |F_m|$, where t_m is the time duration for each bin m, M is the total number of bins, and F_m is the number of switching events within the duration t_m. The behavior of the average capture time as a function of V_{GS}

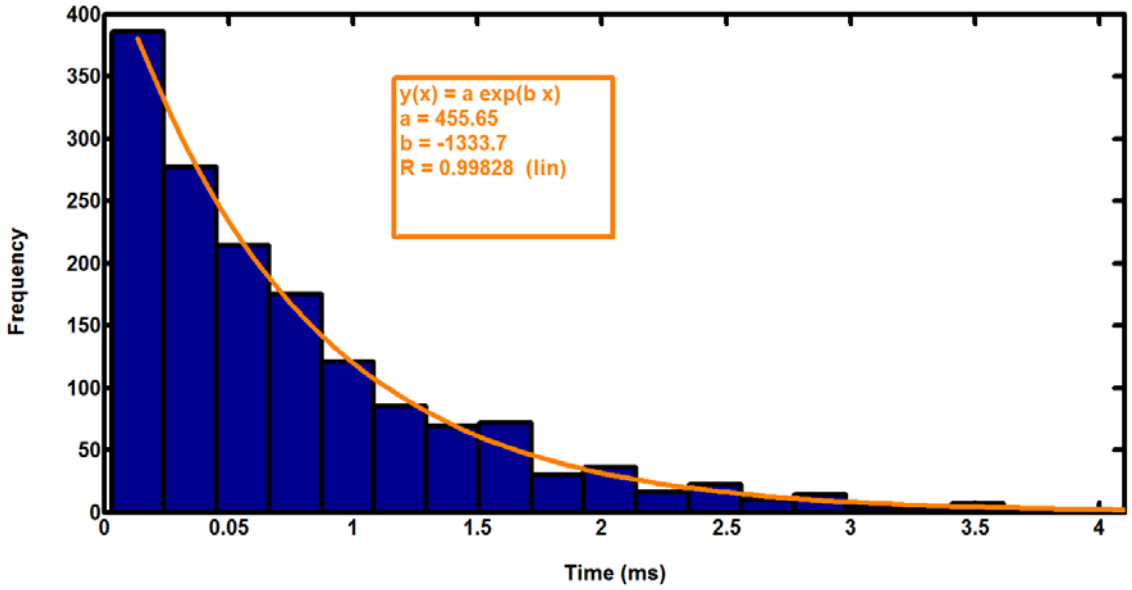


Fig. 4.3 Distribution of time spent at the higher level for PMOS550. V_{GS} = -1.5 V, V_{DS} = -0.4 V, T = 295 K.

can be used to find out whether the trap is an attractive center or a repulsive center. For a pMOSFET, $\overline{\tau}_c/\overline{\tau}_e = f_t/(1-f_t) = (1-f_{th})/f_{th}$. Equations 2.40 and 2.50 are re-written here for convenience:

$$\overline{\tau}_c = \frac{e^{(\Delta E_B/k_BT)}}{\sigma_0 p \overline{v}_{th}} \tag{4.1}$$

$$\overline{\tau}_e = \frac{\exp\left[\left(\Delta E_B + \Delta E_{TV}/k_BT\right)\right]}{g\sigma_0\left(8k_BT/\pi m_p^*\right)^{1/2} N_V} \tag{4.2}$$

With the increase in gate voltage magnitude, in addition to the increase in inversion layer hole number, the trap hole occupancy also increases. The increase in inversion layer hole concentration decreases the average hole capture time ($\overline{\tau}_c$) (Eq. 4.1). Depending on the trap energy level with respect to the silicon valence band edge, the average emission time might increase or decrease with the increase of gate voltage magnitude. Fig. 4.4 shows the band diagram of a pMOSFET. With the increase in gate voltage magnitude, the amount of bending in the oxide valence band (V_{OX}) increases. The increase in V_{ox} shifts the trap energy level with respect to the silicon valence band edge as well (Fig. 4.4). Hence, depending on the trap energy level with respect to the silicon valence band edge, the

average emission time ($\bar{\tau}_e$) might increase, decrease, or remain the same with the increase in $|V_{GS}|$. Even if $\bar{\tau}_e$ experiences a decrease with the increase in $|V_{GS}|$, the decrease in $\bar{\tau}_e$ is less than the decrease in $\bar{\tau}_c$ because of the denominator in Eq. 4.2. Therefore, $\bar{\tau}_c/\bar{\tau}_e$ will decrease with the increase in $|V_{GS}|$. During analyses, the pattern of average time spent at each RTS level is observed as a function of V_{GS} .If the average time spent at the lower level

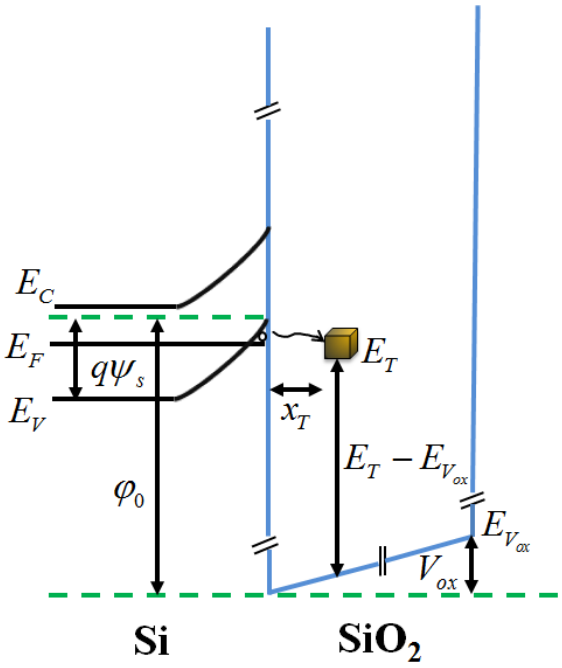
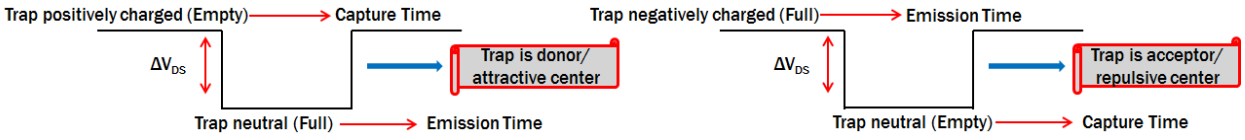


Fig. 4.4. Band diagram of a pMOSFET. With the increase in gate voltage magnitude, V_{OX} increases. Since trap energy level is measured with respect to the oxide valence band edge, the trap energy level will also move. Therefore, the trap energy level with respect to the silicon valence band edge will change, reflecting a change in the average emission time constant.

For electron traps:



For hole traps:

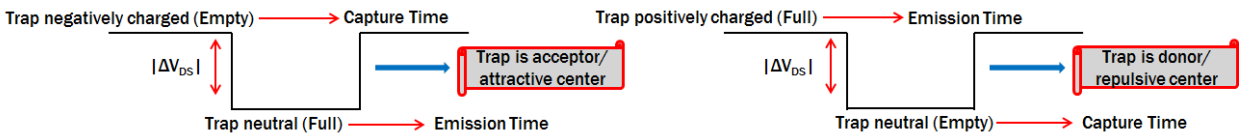


Fig. 4.5 Summary of identification of trap types. An attractive center is a termed as a 'donor' for electron traps in nMOSFETs, while an attractive center in pMOSFETs is termed as an 'acceptor'. The terms 'attractive' and 'repulsive' have been used in this work to avoid any confusion.

decreases with the increase in V_{GS} magnitude, then the bottom level corresponds to capture time constant, $\overline{\tau}_c$. If the average time constant for the upper level shows a decrease when the magnitude in V_{GS} increases, then the average time spent at the upper level is $\overline{\tau}_c$.

When a trap is charged, the channel holes will experience remote Coulomb scattering because of the positively charged channel holes, and the charged trap. This remote Coulomb scattering between the channel holes and the charged trap will increase the channel resistance. The pMOSFETs used in the experiments were biased with

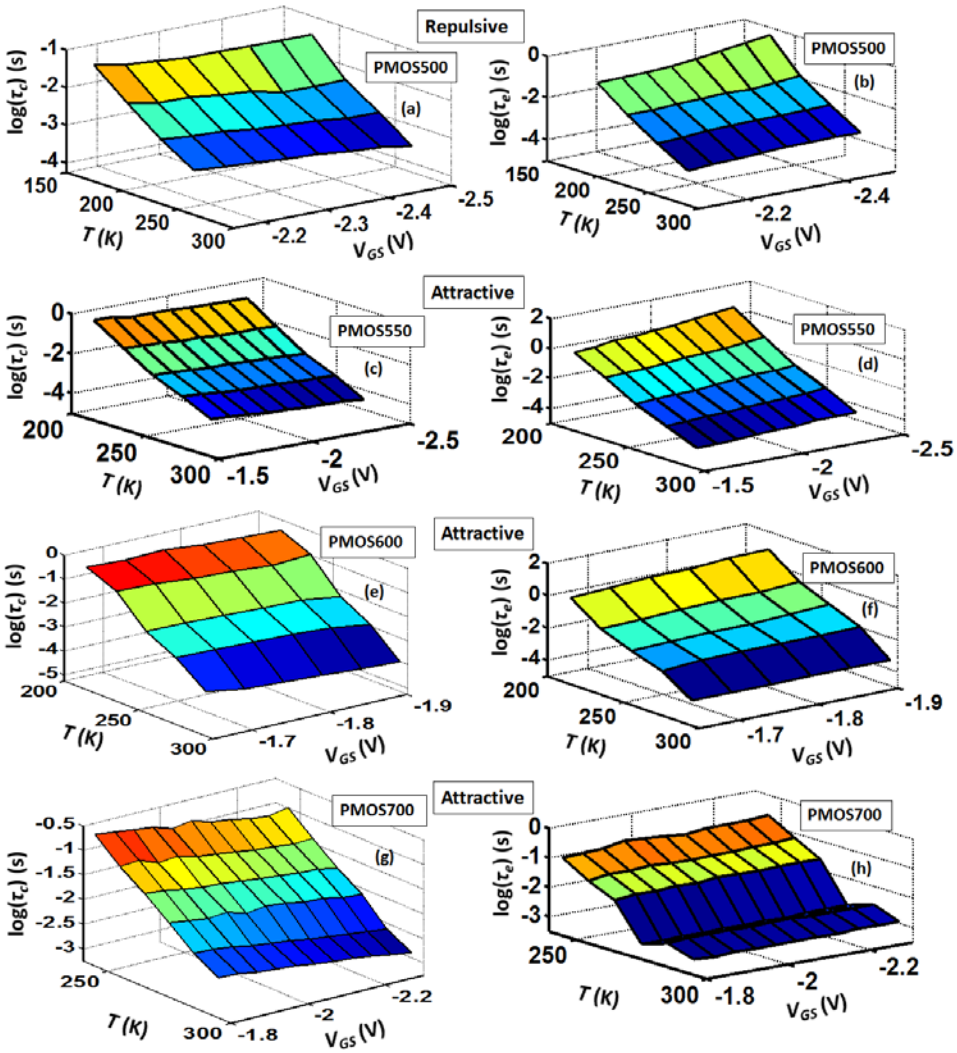


Fig. 4.6 Experimentally measured average hole capture and emission times as a function of V_{GS} and T. For PMOS500, PMOS600 and PMOS700, V_{DS} = -0.5 V. For PMOS550, V_{DS} = -0.4 V.

a constant current source. Hence, a charge trap will result in an increase in the V_{DS} magnitude. An attractive center hole trap is negatively charged when empty, while a repulsive center trap is positively charged when it captures a hole. Therefore, if the lower level of an RTS in absolute value is found to be indicating $\overline{\tau}_c$, then the trap responsible is empty when it is not charged i.e. the trap is a repulsive center. If $\overline{\tau}_c$ corresponds to the upper level of an RTS in absolute value, then the trap is charged when it is empty, which makes the trap an attractive center. Commonly, the trap types are mentioned as 'donors' and 'acceptors' [85]. However, the terms 'donors' and 'acceptors' are defined in terms of charge states related to the capture and emission of electrons. Using similar terms in case of hole traps might make the definitions of the trap types complicated and confusing. Therefore, to avoid any confusion, 'attractive centers' and 'repulsive centers' have been used in this work to indicate the charge states of the traps prior and after hole capture. Definition of both trap types in case of both electron and hole traps have been summarized in Fig. 4.5. For the devices PMOS550, PMOS600, and PMOS700, the upper level of the RTS correspond to $\overline{\tau}_c$, and for PMOS500, the bottom level correspond to $\overline{\tau}_c$. Hence, PMOS500 is a repulsive center, whereas PMOS550, PMOS600, and PMOS700 are attractive center traps. It is important to note that the observation of attractive and repulsive center traps in the MOSFETs is totally random. If another device of same dimensions is taken, either of the two types of traps can be observed. Comments about the trap type cannot be made before taking the RTS measurements. However, the distribution of the traps can be statistically quantified using RTSSIM [85]. The plots of experimentally measured $\overline{\tau}_c$ and $\overline{\tau}_e$ are shown in Fig. 4.6 as a function of V_{GS} and temperature for all four devices.

To extract the trap characteristic parameters, the following parameters are used [86]:

Average thermal velocity of inversion layer holes, $\overline{v}_{th}(T) = \sqrt{\frac{8k_B T}{\pi m_p^*}}$.

Electron effective mass, $m_n^*(T) = m_0(1.053 + 0.00012T)$, where m_0 is mass of an electron.

Hole effective mass, $m_p^*(T) = m_0(0.6135 + 0.00269T - 3x10^{-6}T^2)$.

Silicon bandgap, $E_g(T) = 1.166 - \frac{4.730x10^{-4}T^2}{(T + 636)}$.

Effective density states of electrons in the conduction band, $N_C(T) = 2\left(\frac{2\pi m_n^* k_B T}{h^2}\right)^{3/2}$.

Effective density states of holes in the valence band, $N_V(T) = 2\left(\frac{2\pi m_p^* k_B T}{h^2}\right)^{3/2}$.

Intrinsic carrier concentration at equilibrium, $n_i(T) = \sqrt{N_C N_V}\, e^{-E_g/(2k_B T)}$.

Hole concentration per unit volume, p is calculated using $p(T) = p_0(T)e^{-(q\Psi_s/k_B T)}$ [86], [82], where p_0 is the equilibrium hole concentration. Here,

$$p_0 = \frac{n_i^2(T)}{n_0(T)} \approx \frac{n_i^2(T)}{N_D(T)} \approx \frac{n_i^2(T)}{N_D^+(T)} \tag{4.3}$$

where n_0 is the equilibrium electron concentration, N_D and N_D^+ are the background donor doping concentration, and ionized doping concentration respectively. However, at low temperatures, some of the carriers freeze out. Therefore, at low temperatures, we cannot assume the background donor doping concentration to be equal to the electron concentration i.e. $n_0 = N_D^+ \neq N_D$. The equilibrium electron concentration can be expressed as [86] $n_0(T) = N_C(T)e^{(E_F - E_C)/k_B T}$. The ionized donor concentration is related to the background donor doping concentration by

$$N_D^+(T) = n_0(T) = \frac{N_D}{1 + g_d e^{(E_F - E_D)/k_B T}} \tag{4.4}$$

where E_D and g_d are the donor energy level and donor degeneracy factors respectively. Equation (4.4) can be modified as

$$n_0(T) = \frac{N_D}{1 + g_d e^{(E_F - E_C)/k_B T} e^{(E_C - E_D)/k_B T}} = \frac{N_D}{1 + \left(\frac{g_d}{N_C(T)}\right) e^{(E_C - E_D)/k_B T} n_0(T)} \tag{4.5}$$

$$\left(\frac{g_d}{N_C}\right) e^{(E_C - E_D)/k_B T} n_0^2 + n_0 - N_D = 0 \tag{4.6}$$

Solving Equation (4.6) n_0 can be written as

$$n_0(T) = \frac{-1 \pm \sqrt{1 + 4\left[\left(\frac{g_d}{N_C(T)}\right)e^{(E_C - E_D)/k_BT}\right]N_D}}{2\left[\left(\frac{g_d}{N_C(T)}\right)e^{(E_C - E_D)/k_BT}\right]} \tag{4.7}$$

The surface potential (ψ_s) also needs to be calculated for analyzing the trap parameters. ψ_s is calculated via the Poisson's equation. From the charge neutrality equation, Poisson's equation can be expressed as [86]

$$\frac{\delta^2\psi(x)}{\delta x^2} = \frac{\delta}{\delta x}\left(\frac{\delta\psi(x)}{\delta x}\right) = \frac{-q}{\varepsilon_{si}}\left[p_0\left(e^{q\psi(x)/k_BT} - 1\right) - n_0\left(e^{-q\psi(x)/k_BT} - 1\right)\right] \tag{4.8}$$

where $\psi(x)$ is the potential at the channel measured at a point x from the Si-SiO_2 interface. The total charge in the semiconductor (Q_S) is computed by integrating Equation (4.8) from the bulk towards the interface. Q_S is calculated as

$$Q_S = \sqrt{2k_BTn_0\varepsilon_{Si}}\left\{\left(e^{-q\psi_s/k_BT} + \frac{q\psi_s}{k_BT} - 1\right) + \left(\frac{n_i}{n_0}\right)^2\left(e^{q\psi_s/k_BT} - \frac{q\psi_s}{k_BT} - 1\right)\right\}^{1/2} \tag{4.9}$$

Finally, ψ_s is calculated using the measured P_{inv} through the C-V characteristics, and by solving Equation (4.9).

$$P_{inv} = \left\{\frac{\sqrt{2}\varepsilon_{Si}k_BT}{q^2L_D(T)}\sqrt{\left(u + e^{-u} - 1\right) + \left(\frac{n_i}{n_0}\right)^2\left(e^u - u - 1\right)}\right\} - n_0\sqrt{\frac{2\varepsilon_{Si}\psi_s}{qn_0}} \tag{4.10}$$

where $u = q\psi_s/k_BT$, and $L_D(T) = \sqrt{\left(\varepsilon_{Si}k_BT/q^2n_0\right)}$ is the Debye length.

4.3 Trap Location From the Si-SiO_2 Interface

The trap distance from the Si-SiO_2 interface (x_T) was extracted through [82]

$$x_T = \frac{T_{ox}\left[\frac{kT}{q}\frac{d\ln\left(\bar{\tau}_c/\bar{\tau}_e\right)}{dV_{GS}} + \frac{d\psi_s}{dV_{GS}}\right]}{\frac{d\psi_s}{dV_{GS}} - 1} \tag{4.11}$$

As mentioned in Chapter 3, T_{ox} was calculated from the C-V characteristics via $T_{ox} = \varepsilon_0\varepsilon_{SiO_2}/C_{ox}$. x_T is shown in Fig. 4.7 for all four devices at different temperatures. The trap locations of the four devices varied from 0.39 nm to 1.4 nm. According to R. Salh [87], the Si-O bond length in the SiO_2 network varies between 0.154 nm and 0.169

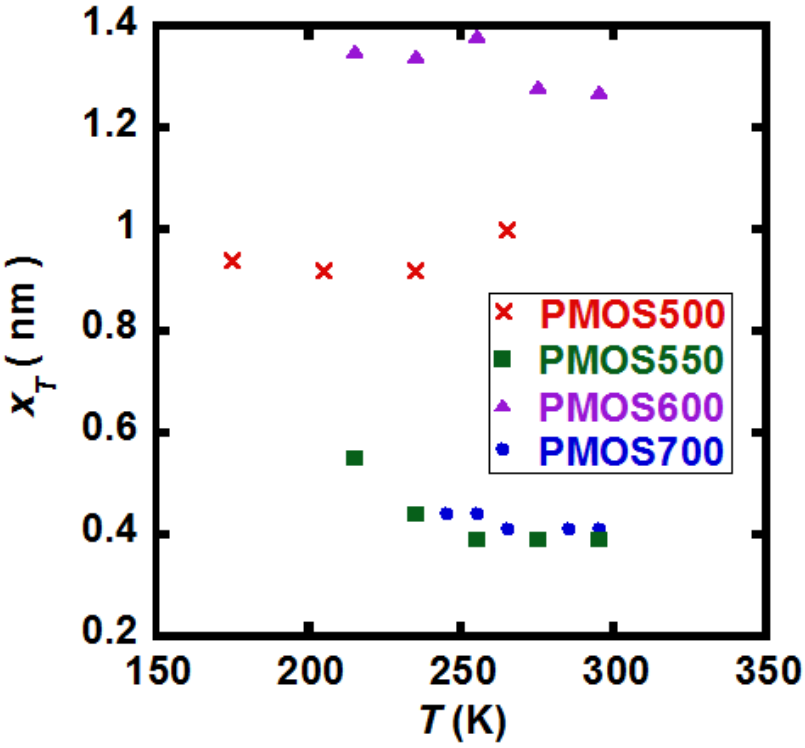


Fig. 4.7 Trap location of the traps across all the measured temperatures. As expected, the trap location does not show a significant variation with respect to temperature. The physical location does not indicate the type of trap.

nm. This indicates that the traps responsible for RTS in the devices are not Pb centers (a trivalent Si center at the Si-SiO_2 interface) [88]. Both attractive center and repulsive center defects were found to be residing at similar locations from the Si-SiO_2 interface. Hence, the physical location was not an indicator of the trap types. No correlation was found between the time constants of the traps and their location from the Si-SiO_2 interface. This is consistent with

the observations reported by Nagumo *et al*. [89]. This supports the fact that the random capture and emission of the channel holes by the gate oxide defects is indeed phonon-assisted tunneling, and not elastic tunneling.

4.4 Trap Position Along the SiO_2 Bandgap

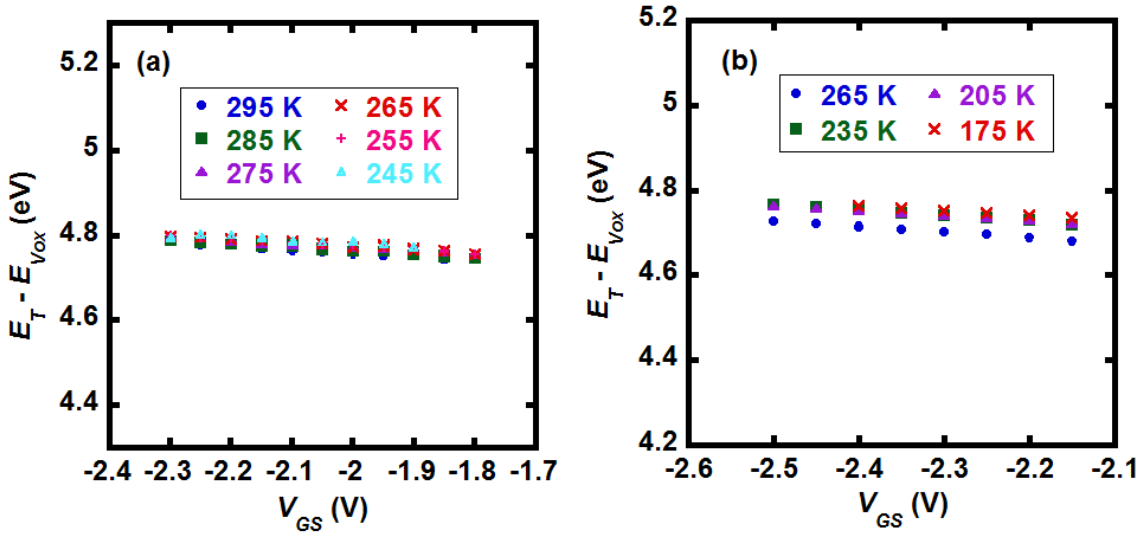


Fig. 4.8 Trap energy level with respect to the SiO_2valence band edge: (a) For PMOS700, (b) PMOS500. Both the attractive and repulsive center traps are located around the same energy level along the SiO_2 bandgap. Hence, trap energy level does not indicate the trap type either.

The trap energy level with respect to the SiO_2 valence band edge was found from the following expression.

$$\ln\left(\frac{\bar{\tau}_c}{\bar{\tau}_e}\right) = -\frac{1}{k_B T}\left[\left(E_T - E_{V_{ox}}\right) - \left(E_F - E_V\right) - \phi_0 + q\psi_s + \frac{qx_T}{T_{ox}}\left(V_{GS} - V_{FB} - \psi_s\right)\right] \tag{4.12}$$

$E_T - E_{V_{ox}}$ for all the traps are shown in Fig. 4.8. The values of $E_T - E_{V_{ox}}$ vary from 4.68-4.78 eV. This indicates that the traps are located just below the silicon valence band edge. Hence, the traps were easily accessible by the channel holes since the Fermi level is close to E_V at these bias points.

4.5 RTS Magnitude

Each of the RTS levels corresponded to a Gaussian distribution in the histogram (Fig. 4.9). The RTS magnitude was extracted from the difference between the peaks of the Gaussian distributions. When a channel hole

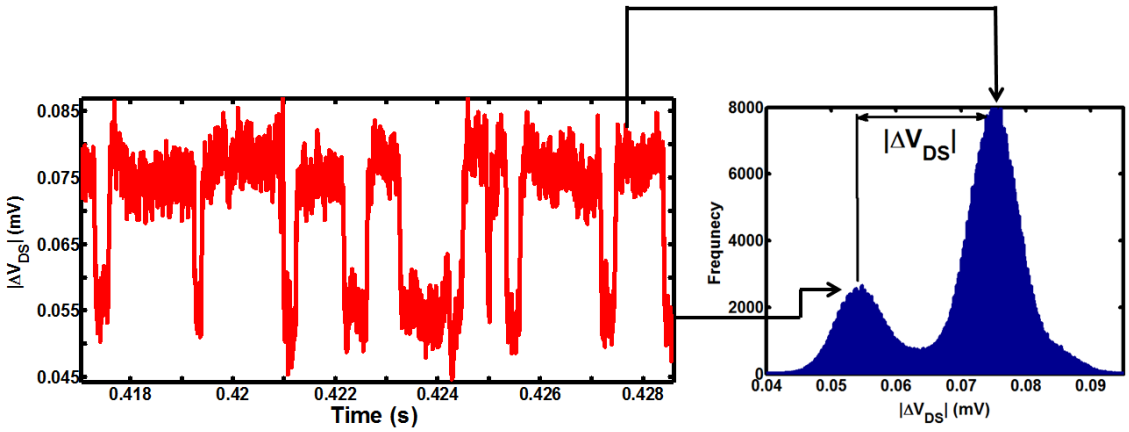


Fig. 4.9 Extraction of RTS magnitude for PMOS550. V_{GS}= -1.5 V, V_{DS}= -0.4 V, T= 295 K.

gets captured by a trap, number of the channel hole fluctuates. According to the unified number and mobility fluctuations theory (UNMF) [72], in addition to the change in the channel hole number fluctuations, the charged trap also causes fluctuations in the effective mobility of the channel hole via remote Coulomb scattering. In strong inversion, the normalized fluctuation in drain voltage can be written as [72]

$$\frac{\Delta V_{DS}}{V_{DS}} = -\left(\frac{1}{P_{inv}} \pm \alpha\mu\right)\frac{1}{WL} \tag{4.13}$$

As explained in Chapter 2, the sign between the fluctuation terms in the parenthesis depends on the trap charge states before and after hole capture: '-' sign is used in case of attractive center traps, and '+' sign is used for repulsive center traps. Therefore, everything else being equal, a repulsive center trap will result in higher RTS magnitude than an attractive center. This is evident from Fig. 4.10, where PMOS500, being a repulsive center exhibits around one order of higher RTS magnitude than the attractive center traps.

The number and mobility fluctuation terms in Eq. (4.13) were calculated from the measured RTS magnitude. P_{inv} was extracted by integrating the measured C-V characteristics [85]. $1/P_{inv}$ was computed using the

extracted P_{inv}. The mobility fluctuations were calculated by subtracting the number fluctuations from the normalized RTS magnitude. Since the devices are almost identical in size, therefore, the hole number fluctuations of all the traps were similar. On the other hand, PMOS500 showed roughly one order of magnitude higher mobility fluctuations than the other traps since a positively charged trap causes more scattering than a negatively charged trap (Fig. 4.10).

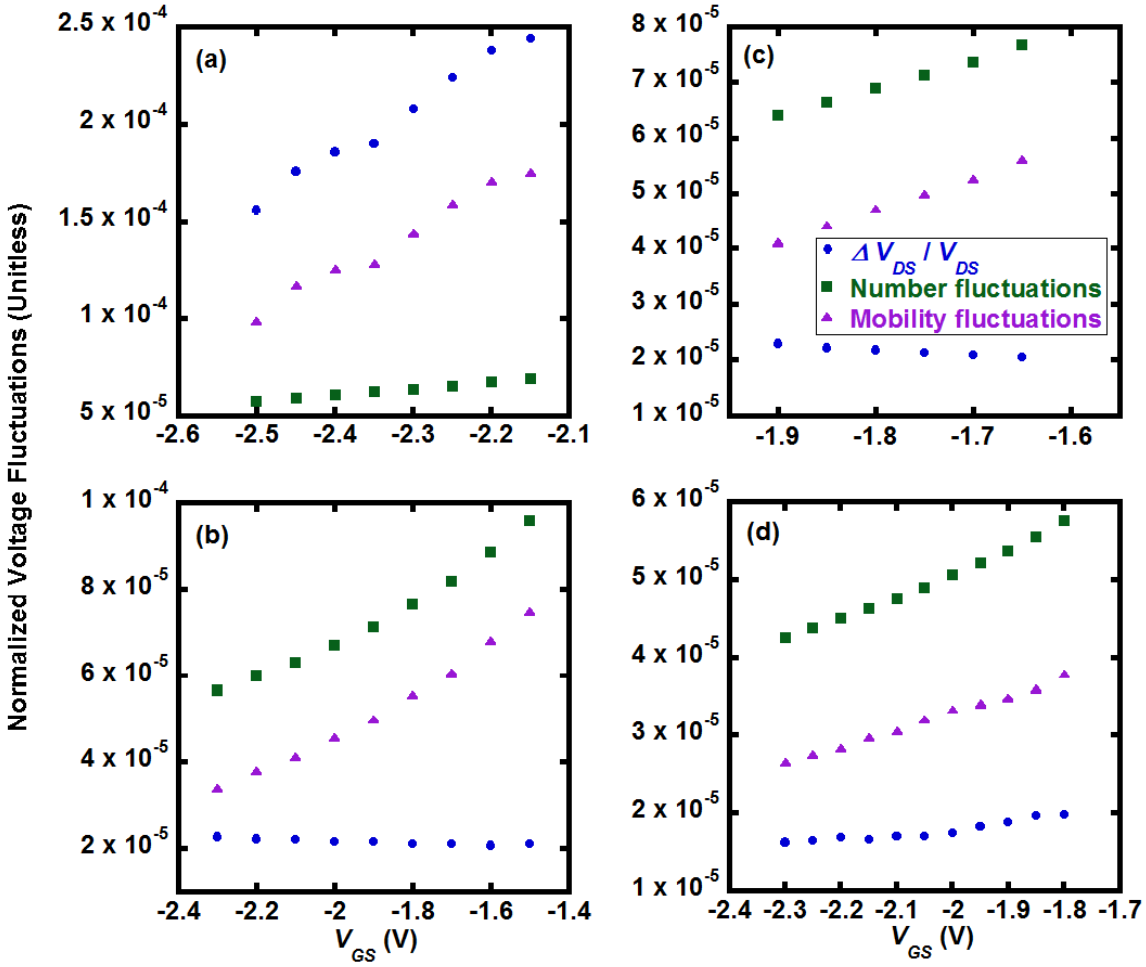


Fig. 4.10 RTS magnitude normalized to drain voltage, number fluctuations, and mobility fluctuations for (a) PMOS500 at V_{DS}= -0.5 V, T= 265 K, (b) PMOS550 at V_{DS}= -0.4 V, T=295 K (c) PMOS600 at V_{DS}= -0.5 V, T= 295 K and (d) PMOS700 at V_{DS}= -0.5 V, T= 295 K. Since PMOS500 is a repulsive center, therefore, the number and mobility fluctuations get added, while the two fluctuations terms get subtracted for the other traps. As a result, PMOS500 shows roughly one order of higher RTS magnitude than the other traps.

4.6 Screened Scattering Coefficient

Screened scattering coefficient (α) was found from the mobility fluctuations term extracted through Equation 4.13. μ was calculated using $\mu = g_D L/WqP_{inv}$. The calculated α values at different V_{GS} and temperatures

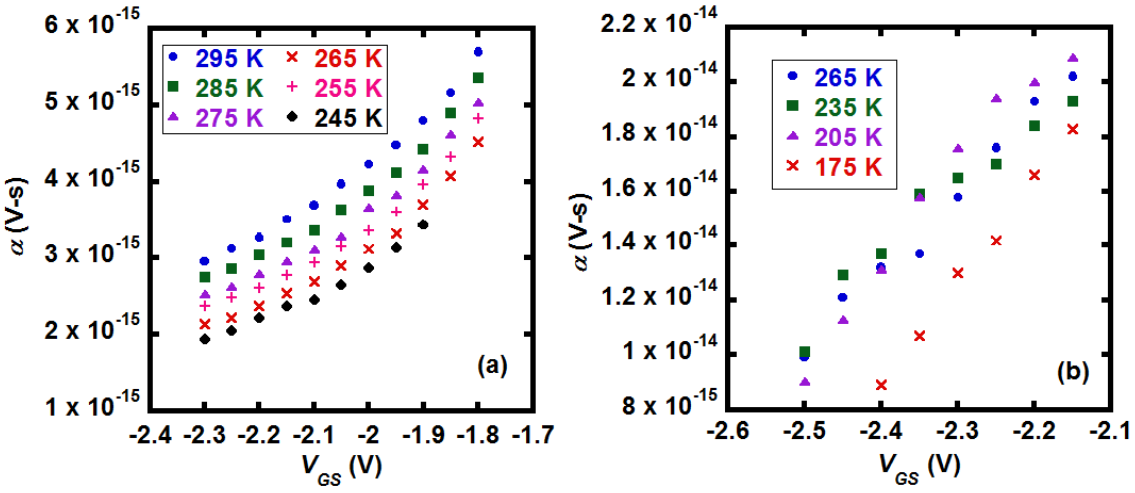


Fig. 4.11 Screened scattering coefficient across all the measured V_{GS} and temperatures: (a) For PMOS700 at V_{DS}= -0.5 V, (b) PMOS500 at V_{DS}= -0.5 V. Since PMOS500 is a repulsive center and PMOS700 is an attractive center, therefore α values of PMOS500 are around one order of magnitude higher than PMOS700 as a positive charged trap causes more hole scattering than a negatively charged defect.

are shown in Fig. 4.11. With the increase of V_{GS} , channel hole concentration increases. This reduces the amount of screening and hence α is decreased. With the increase in temperature, μ is decreased due to increased phonon scattering. However, the mobility fluctuation decreased with the increase of temperature. Therefore, α showed a slight decrease with the increase in temperature.

4.7 Capture Cross-section

Capture cross-section of the traps were calculated through the Shockley-Read-Hall statistics [29]:

$$\sigma = \frac{1}{p\bar{v}_{th}\bar{\tau}_c} \tag{4.14}$$

Capture cross-sections of PMOS500 and PMOS550 are shown in Fig. 4.12. The values of σ varied from 10^{-27} – 10^{-23} cm^2, which were within the similar range of the capture cross-section values, previously reported using RTS [90]. However, the aforementioned σ values disagreed with some other published trap capture cross-section values

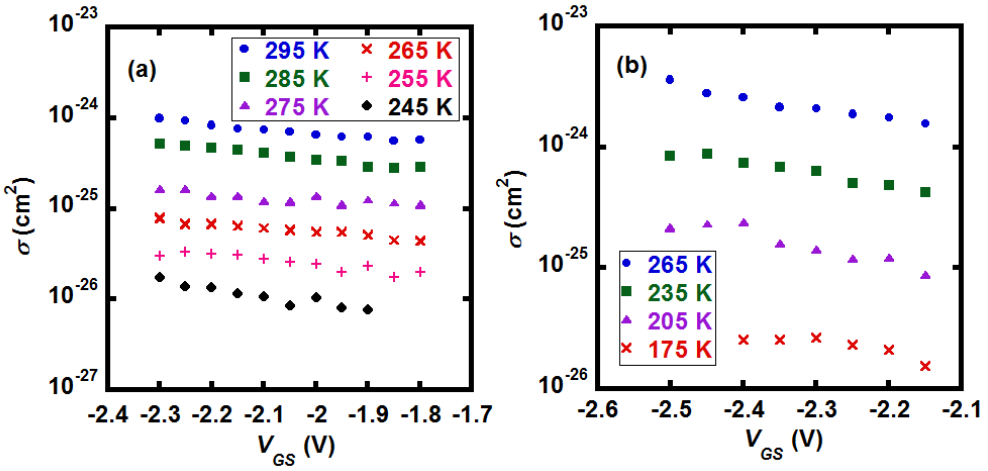


Fig. 4.12 Capture cross-sections across all the measured V_{GS} and temperatures: (a) For PMOS700 at V_{DS}= -0.5 V, (b) PMOS500 at V_{DS}= -0.5 V. With the decrease in temperature, the hole motion slowed down, resulting in a decrease in capture cross-sections.

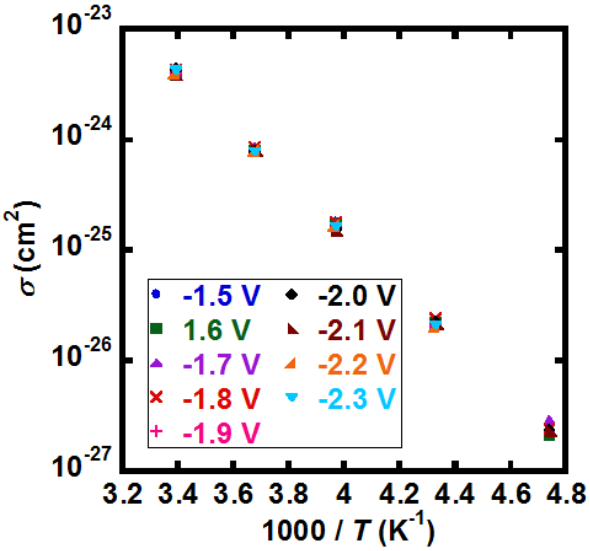


Fig. 4.13 Arrhenius plot of σ for PMOS550 at different gate voltages at V_{DS}= -0.4 V. Slope of this plot gives the trap capture activation energy (ΔE_B).

extracted through charge pumping measurements [91], [92], [93]. This was partially because of the slower time constants, and partially due to the limitations of the formulation used by Kirton and Uren [29]. In addition, Equation 4.14 assumes the trap to be surrounded by uniform layer of channel carriers, and not a distance away from them as a trap would be from the channel carriers. However, the carrier distribution is not uniform along the channel. Moreover, position of the peak of the carrier concentration in silicon changes with gate voltage. Therefore, Equation 4.14 is only an approximation [94]. Furthermore, the vibration frequencies of the two charge carrier states are assumed to be same (i.e. same curvature for both parabolas in Fig. 2.4). This is also incorrect and would need some corrections to be made in the expressions used to calculate the capture cross-sections [95], [96]. However, that topic is beyond the scope of this work.

4.8 Capture Activation Energy

As mentioned in Chapter 2, trap capture activation energy (ΔE_B) is related to the capture cross-section as [29]:

$$\sigma = \sigma_0 e^{\left(-\Delta E_B / k_B T\right)} \tag{4.15}$$

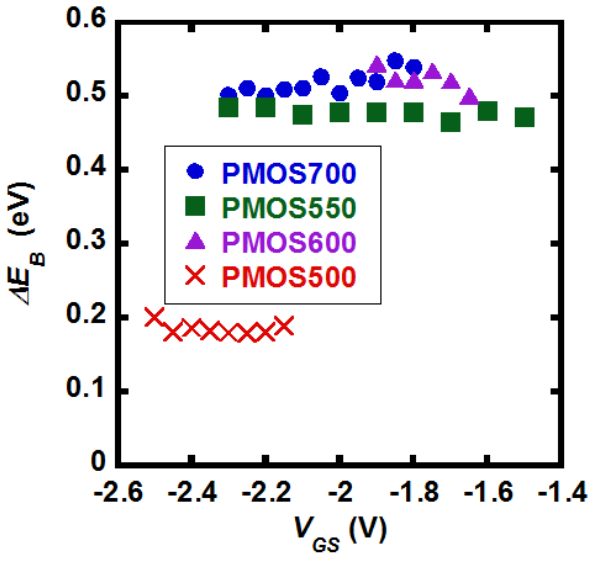


Fig. 4.14 Capture activation energy of all the traps. For PMOS500, PMOS600 and PMOS700, V_{DS}= -0.5 V. For PMOS550, V_{DS}= -0.4 V. Switching due to PMOS500 was faster than the other traps because of its lower ΔE_B.

ΔE_B and capture cross-section pre-factor (σ_0) were found through the Arrhenius plot of σ (Fig. 4.13). ΔE_B values of PMOS550, PMOS600, and PMOS700 (attractive centers) were found to be ~0.5 eV, whereas the ΔE_B values of PMOS500 (repulsive center) was ~0.2 eV (Fig. 4.14). This higher ΔE_B value of the attractive centers was the primary reason behind the higher time constants for the attractive center defects [13]. The narrow V_{GS} range in the RTS experiments has kept the change in ΔE_B negligible (Fig. 4.14) [12], [29]. Since the average capture time is exponentially dependent on ΔE_B, even a slight change in ΔE_B causes a significant change in $\bar{\tau}_c$.

4.9 Change in Enthalpy and Entropy

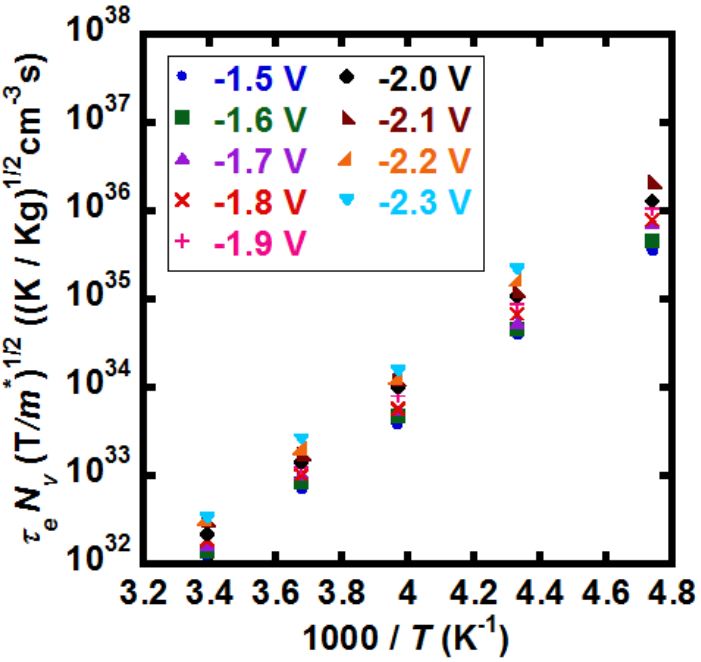


Fig. 4.15 Arrhenius plot of normalized average emission time constant for PMOS550 at different gate voltages at V_{DS}= -0.4 V. Slope of this plot gives the change in enthalpy (ΔH). The y-axis intercept can be used to extract the change in entropy (ΔS).

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Arrhenius plot of $\bar{\tau}_e N_V \left(T/m_p^*\right)^{1/2}$ was used to find $\left(\Delta E_B + \Delta H\right)$ and $\Delta S/k_B$ (Fig. 4.15). ΔH was calculated by subtracting ΔE_B from the obtained $\left(\Delta E_B + \Delta H\right)$ values. ΔH values of the traps are shown in Fig. 4.16(a). Positive values of ΔH indicate that the hole emission is an endothermic process, whereas negative ΔH

infer an exothermic process. ΔS values (Fig. 4.16(b)) indicated the amount of disorder in the system. Negative ΔS values suggested more disorder in the local environment around the defect in lattice after capturing a hole, whereas positive ΔS values meant that the system was more disordered after emitting the hole back to the channel. Negative ΔH means that heat is transferred to the lattice when the captured hole is emitted back to the channel. The

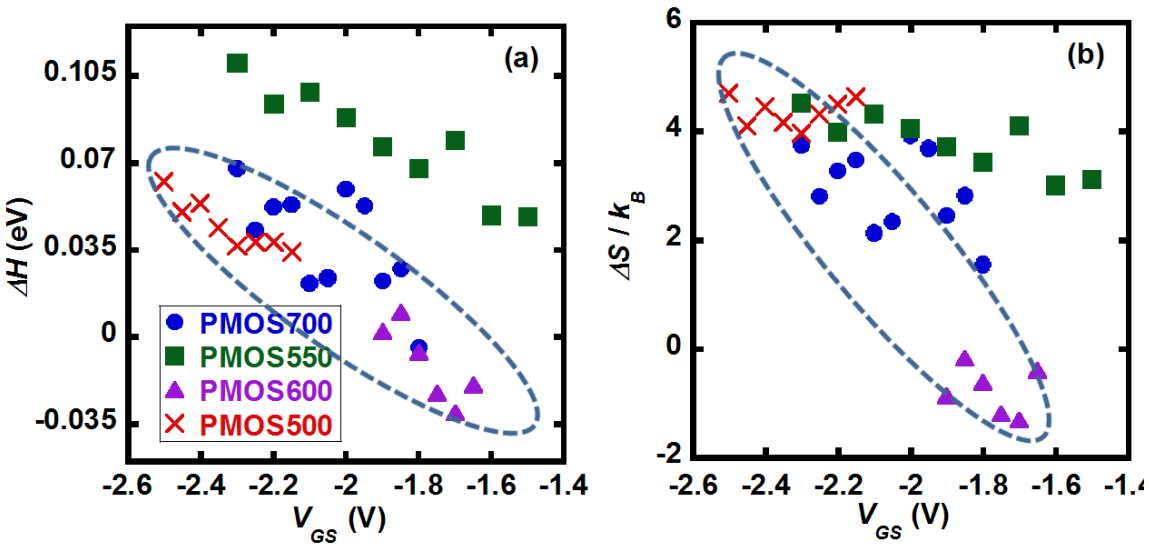

Fig. 4.16 (a) Change in enthalpy, and (b) change in entropy for all traps. For PMOS500, PMOS600 and PMOS700, V_{DS}= -0.5 V. For PMOS550, V_{DS}= -0.4 V.

transferred heat might increase the binding force between the neighboring atoms, leading to less entropy when the trap is empty of a hole. The $(\Delta H - T\Delta S)$ values of the traps varied from -53.6 meV up to 8.14 meV across the measured V_{GS} and temperature range. This observation confirmed that the traps were located near the silicon valence band edge at the Si-SiO_2 interface [82].

4.10 Relaxation Energy

Another important parameter to identify the defect structures is relaxation energy (E_R), which gives information about structural relaxation of the defects due to phonon exchange during capture and emission of the channel holes. When a carrier gets trapped, it relaxes to the trap energy level by emitting several phonons, and this

determines the value of the relaxation energy. E_R was calculated through the obtained ΔE_B, ΔH and ΔS values solving:

$$\Delta E_B = \frac{\left(E_R + \left(\Delta H - T\Delta S\right)\right)^2}{4E_R} \tag{4.16}$$

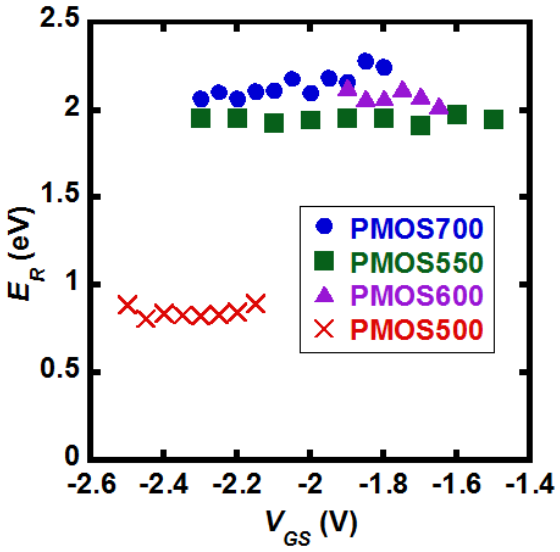

Fig. 4.17 Relaxation energy of all the traps. For PMOS500, V_{DS}= -0.5 V, T= 265 K, for PMOS600 and PMOS700, V_{DS}= -0.5 V, T= 295 K, for PMOS550, V_{DS}= -0.4 V, T= 295 K.

As shown in Fig. 4.17, E_R of PMOS500 (repulsive) was ~0.8 eV, whereas the other traps showed a relaxation energy of ~2.0 eV (attractive). Comparing to the other traps, smaller ΔE_B values resulted in smaller E_R values for PMOS500. However, it is still not clear why the ΔE_B and E_R were observed to be much lower than the other traps.

4.11 Trap Species

To identify the defect structures responsible for RTS, the experimentally found ΔE_B, E_R and $E_T - E_{V_{ox}}$ values were compared to the already published defect parameters. A list of parameters of all the studied defects is shown in Table 4.1. $E_T - E_{V_{ox}}$ values of our traps varied between 4.6 and 4.8 eV across all measured gate voltages and temperatures. This eliminates certain types of E′ center defects from possible defect candidates such as two-fold

coordinated silicon neutral vacancy centers (II-Si), and a pair of under-coordinated oxygen atom and over-coordinated silicon atom (III-O/V-Si) since both of these defects are close to either $E_{V_{ox}}$ or $E_{C_{ox}}$ [37]. $E_T - E_{V_{ox}}$ values of hydrogen defects and hydroxyl E′ center defects matched with the $E_T - E_{V_{ox}}$ values of our traps [38], [39], [97], [98], [99]. However, the ΔE_B and E_R values of the hydrogen defects and the hydroxyl E′ centers are reported to be higher than that of the defects presented in this Chapter [38], [39], [97], [98], [99]. This ruled out both the hydrogen related defects and the hydroxyl E′ centers from the possible candidates.

According to the density functional theory calculations using generalized gradient approximation (DFT-GGA), a certain type of E′ center, a pair of three-coordinated silicon defects (D-III-Si) exhibits a relaxation energy of ~1 – 2 eV upon capturing a hole from the channel [37]. This defect lies deep in the SiO_2 bandgap, with energy levels around 4.8 – 5.6 eV from the SiO_2 $E_{V_{ox}}$. Since both E_R and $E_T - E_{V_{ox}}$ of the D-III-Si defect match with those of the attractive center defects observed through RTS, therefore D-III-Si defect is thought to be the attractive center defect responsible for RTS. One silicon atom in the D-III-Si defect has a doubly occupied sp^3 orbital. Upon capturing a hole, one of the paired electrons is neutralized, and hence the structure behaves like an attractive center defect defined earlier. After trapping a hole, the O-Si-O bond angle increases from ~103^0 to ~107^0 (Fig. 4.18(a)) [37].

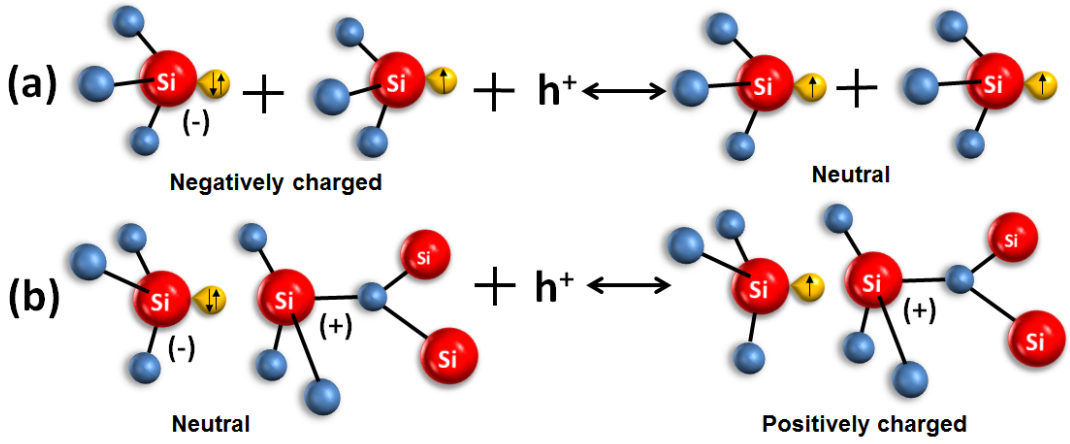

Fig. 4.18 (a) Pair of dissociated three-fold coordinated silicon atoms (D-III-SI) acting as a Coulombic attractive center, (b) Puckered/back-projected E_γ' center (III-O/III-Si) acting as a repulsive center. The solid lines and arrows indicate Si-O bonds and dangling electrons respectively. The bond angles and lengths are not drawn to scale.

$$\equiv Si^{\bullet} + \equiv Si:^{-} + h^{+} \leftrightarrow \equiv Si^{\bullet} + \equiv Si^{\bullet} \quad (4.17)$$

where $\equiv$ indicates three silicon-oxygen bonds, $^{\bullet}$ means a single unpaired electron, and : represents paired electrons in a single sp^3 orbital. These defect centers are negatively charged when empty, and get neutralized after trapping a

Table 4.1- Summary of the energy parameters of all the studied defects.

Trap species	Trap Type	Capture activation energy (ΔE_B) (eV)	Relaxation energy (E_R) (eV)	$E_T - E_{V_{ox}}$ (eV)	$E_T - E_V$ (eV)
Aforementioned attractive centers	-/0	0.47-0.55	1.91-2.28	4.69-4.81	-0.04 - +0.02
D-III-Si	-/0		0.5-2.3 [37]	4.8-5.6 [37]	
H bridge defect	-/0		2.5 [38], 1.71 [99]	4-6.5 [38], 3.8-5.2 [97]	
III-Si/V-Si	-/0		1.7-2.1 [37]	5.0-5.6 [37]	
III-O/V-Si	-/0		~1.7 [37]	5.1-6.3 [37]	
NOV	-/0		0.5-1 [37]	~7.1 [37]	
II-Si	-/0		~1.2 [37]	~6.9 [37]	
Aforementioned repulsive center	0/+	0.18-0.20	0.81-0.89	4.68 – 4.73	-0.07 - -0.04
III-O/III-Si	0/+		0.5-1.8 [37]	3.9-5.3 [37]	~0 [97]*
H bridge defect	0/+	0.1-1.0 [39]	1.5-2.0 [39]**, 2.0-2.5 [38], 2.22 [99]	4-6.5 [38], 4.3-4.9 [97]	-1.0 - +0.5 [39], [98]
Hydroxyl E' center	0/+	0.2-1.0 [39], ~ 0.4 [98]	~2.0 [39]***		-1 - +1 [39], [98]
$E_{\delta}^{'}$ center	0/+			2.9-3.1 [97]	
NOV	0/+	1.5 – 2.5 [39]	~1.0 [37], ~ 3.0 [39]	1.6-2.4 [37]	-1.3 – -3.7 [98], [39]
III-Si/V-Si	0/+		~1.0 [37]	2.1-2.9 [37]	
III-O/V-Si	0/+		0.7-1.1 [37]	2.2-2.5 [37]	

Green highlights: agreement with the attractive trapping centers reported our manuscript.

Yellow highlights: agreement with the repulsive center reported in our manuscript.

Gray highlights: disagreement with the values reported in our manuscript.

*Referred as the "puckered configuration of $E_{\gamma}^{'}$" in [97]. ** Calculated from Fig. 13 of [39].

*** Calculated from Fig. 16 of [39].

hole, which is similar to the charge states observed in an attractive center.

On the other hand, the repulsive center, PMOS500 was considered to be another type of E′ center, a pair of under-coordinated Si atom and over-coordinated oxygen atom (III-O/III-Si) [37] (also known as puckered/back-projected oxygen vacancy center [97], [100]). According to the DFT-GGA calculations [37], energy level of the III-O/III-Si defect varies from 3.8 eV to 5.2 eV from the oxide valence band. Upon capturing a hole, the defect structure undergoes a relaxation of ~0.8 – 1.5 eV. Both these parameters match with the $E_T - E_{V_{ox}}$ and E_R of the repulsive center, PMOS500. After trapping a hole from the silicon valence band, one of the dangling bond electron is neutralized, increasing the average O-Si-O bond angle to ~108-109^0 from ~103^0 (Fig. 4.18(b)) [37]. This defect is neutral when empty of a hole, and becomes positively charged when filled with a hole. Hence, the charge states of this defect before and after hole trapping also match with those of a typical repulsive center defect.

$$^{+}\equiv O + \equiv Si:^{-} + h^{+} \leftrightarrow {}^{+}\equiv O + \equiv Si^{\bullet} \tag{4.18}$$

Since the D-III-Si and the III-O/III-Si defects are the closest to the silicon valence band edge [37], therefore these two defects are predicted to be the most dominant defects during hole capture in pMOSFETs. This prediction matches with the results observed through RTS experiments.

A major concern was the bandgap calculated through DFT calculations. The SiO_2 bandgap was found to be ~6 eV using DFT calculations [37], whereas the actual SiO_2 is ~9.1 eV. Therefore, a correction in the band edges as well as the defect energy levels were needed while finding the $E_T - E_{V_{ox}}$ using the DFT calculations. According to Lany and Zunger [101], while correcting the energy levels for deep SiO_2 bandgap defects, correcting only the $E_{V_{ox}}$ and $E_{C_{ox}}$ keeping E_T constant would be sufficient. Therefore, keeping the defect levels (Fig. 2 in [37]) fixed [102], the G_0W_0 scheme in hybrid DFT calculations were used in correcting the band edges [103]. After correcting the band edges, $E_T - E_{V_{ox}}$ of the defects reported in [37] was found to be ~4.8 eV, which matched with that of the defects observed in RTS experiments.

The traps reported in this Chapter differ from the results reported by Grasser *et al* [39], [40], [98], where they used time dependent defect spectroscopy (TDDS) experiments to characterize the oxide defects, and predicted hydrogen defects and hydroxyl E′ centers to be responsible for RTS. RTS probes into switching traps that lead to

noise in drain signal, whereas TDDS characterizes the oxide traps that causes gate oxide leakage and threshold degradation. Therefore, these two techniques analyze two different types of traps. The fact that the TDDS experiments are done at elevated temperatures (~125^0C) [98] also supports this. RTS can detect traps within a narrow energy window, but is capable of differentiating the attractive center traps from the repulsive centers. TDDS, on the other hand, is able to detect traps of a much broader energy window, but it cannot be utilized to identify the attractive or repulsive center defects.

E′ centers have been reported to be amphoteric in nature, capable of capturing both electrons and holes [82]. It is therefore not surprising to find E′ centers to be responsible for RTS in nMOSFETs [12], [13], [85], as well as pMOSFETs [82]. It is also interesting to observe that the capture cross-sections, capture activation energies, change in enthalpy and entropy and relaxation energies of repulsive center defects in pMOSFETs are within the similar range of values as the repulsive center traps in nMOSFETs [12], [13]. Therefore, the repulsive center defect structure, the puckered/back-projected E_{γ}' center (also called $E_{\gamma 4}'$ center in [38], [100]) is capable of capturing an electron from the silicon conduction band and releasing it to the valence band. Cobden *et al.* [94] also reported similar findings in their RTS analyses. However, they did not comment about the defect type in their article. Their results also agree with Nicklaw *et al.* [100] and Anderson *et al.* [37], who calculated the defect energy levels using DFT. These findings point towards the III-O/III-Si defects to be responsible for RTS in both nMOSFETs and pMOSFETs.

Another interesting point to notice is that in case of both attractive and repulsive center defects, only one under-coordinates silicon atom ($\equiv Si^{\bullet}$) takes part in switching charge states and undergoes structural changes. The counterparts in both the defect pairs take no part in switching the defect charge state. This can be the reason behind the ΔH and ΔS values falling under the same trend line as a function of V_{GS} (Figs. 4.16 (a)-(b)). However, the PMOS550 showed RTS at a lower V_{DS} than the other traps, and exhibiter higher ΔH and ΔS than the other traps. A possible explanation behind this is that the trap might be located near the drain side along the channel since the emission activation energy depends on the position of the quasi-Fermi energy with respect to the trap energy level. Therefore, higher energy would require for PMOS550 to emit the capture hole back to the channel, which would reflect in higher values of ΔH and ΔS.

In summary, variable temperature RTS measurements were done on 15 different sized pMOSFETs, among which four devices have been presented in this chapter. Two different types of E′ centers were found to be responsible for RTS in these devices: a pair of dissociated three-coordinated Si defects (D-III-Si) as attractive centers, and a puckered/ back-projected oxygen vacancy center as repulsive center. This is one of the very few works that suggest a defect structure responsible for RTS in pMOSFETs.

Chapter 5 Effects of Channel Hot Carrier Stress on RTS

Hot carrier effects have been a major concern in short channel devices in recent times. Channel holes with excess energy in a pMOSFET can damage the oxide-semiconductor interface and hence alter the device parameters such as threshold voltage and transconductance. To investigate in detail the mechanisms behind hot carrier-induced damage to the device parameters, application of hot carrier stress on MOS devices has been a matter of interest for the last several years. In addition to degrading the device parameters, some hot holes might gain enough energy to cross the barriers between the valence bands of oxide and semiconductor [86]. Hence, those highly energetic holes can tunnel to the oxide, damage the oxide lattice, and create additional defects in the lattice [86]. Those newly created defects can capture channel holes during MOSFET operation, and cause additional RTS at the output signal. In Chapter 4, characterization of process-induced oxide defects was presented using variable temperature RTS measurements, and a possible structure of the responsible defect was proposed. However, no information on the above mentioned stress-induced traps was obtained in that work. To clearly understand the mechanism behind the creation of stress-induced traps that might be responsible for RTS, extensive amount of stress and RTS measurements need to be done followed by careful analyses of the obtained noise data. This Chapter discusses the bias conditions and cumulative times of stress applied on the MOSFETs under test. RTS measurements after each stress, and detailed analyses of the obtained RTS data are also included. Finally, the trap generation mechanism and the stress-induced defect structure have been suggested.

5.1 Stress Conditions, Device Specifications and Measurement Conditions

Determination of the appropriate stress condition was the first step in the experiments. Among all types of electrical stress conditions, channel hot carrier (CHC) stress is known to cause the maximum degradation in device parameters [104]. The condition for worst degradation in CHC are (i) $V_G = V_D/2$ for devices with channel length <0.25 μm [105], [106], and (ii) $V_G = V_D$ for devices with channel length >0.25 μm [107], [108], [109], [110], where V_G and V_D are applied gate and drain voltage, respectively. The pMOSFET device lengths varied from 0.5 to 1 μm. Even though stressing at $V_G = V_D/2$ would result in worst degradation in the device characteristics, interface degradation would dominate over the bulk oxide degradation in such stress [110]. The bulk oxide degradation

mechanism dominates over the interface degradation when a device is stressed at $V_G = V_D$ [110]. All measured pMOSFETs are 5 V rated devices. Therefore, while stressing the devices, a voltage higher than 5 V had to be applied across the gate and drain terminals. To find out the optimum stress bias condition, the devices were stressed at V_G = V_D = -6 V, and V_G = V_D = -7 V for different durations. The device threshold voltage and transconductance degradation were monitored right after each stress step. Stressing at V_G = V_D = -7 V resulted in very fast degradation in the device threshold voltage, whereas applying V_G = V_D = -6 V as stress condition caused very slow degradation in the device threshold voltage. Therefore, an intermediate stress condition, V_G = V_D = -6.5 V was chosen as the

Table 5.1- RTS levels and traps active at different stressing times.

Cumulative stress time (sec)	Number of levels in RTS	Traps active
0, 5, 10, 40, 70, 100	3	A, B
200	2, 3	A, C
300	2	A
400	2, 3	A, C
500	3	A, B
600	2	A
700	3	A, B
800	2, 3, 4	A, B, D
900, 1000, 1200	2, 3	A, C, D
1500	3	A, B
2000	2, 3	E, F
2500	2	G, H
3000	No RTS	N/A

Table 5.2– Sample of measured MOSFET parameters at different stressing times.

Cumulative stress time (sec)	Threshold voltage (V)	Mobility Degradation*	Gate leakage current* (A)
0	-0.616	N/A	-1.73×10^{-7}
5	-0.617	0.52%	-2.69×10^{-7}
10	-0.620	0.43%	-2.28×10^{-7}
40	-0.620	1.74%	-2.27×10^{-7}
70	-0.624	2.44%	-2.22×10^{-7}
100	-0.625	2.68%	-2.25×10^{-7}
200	-0.630	4.40%	-2.12×10^{-7}
300	-0.641	5.68%	-2.05×10^{-7}
400	-0.645	7.15%	-2.05×10^{-7}
500	-0.646	8.28%	-2.05×10^{-7}
600	-0.646	9.90%	-2.44×10^{-7}
700	-0.651	9.54%	-2.09×10^{-7}
800	-0.655	10.53%	-2.20×10^{-7}
900	-0.655	11.80%	-2.11×10^{-7}
1000	-0.659	12.72%	-2.00×10^{-7}
1200	-0.671	14.00%	-2.03×10^{-7}
1500	-0.689	16.59%	-2.07×10^{-7}
2000	-0.727	18.39%	-2.09×10^{-7}
2500	-0.762	22.25%	-2.38×10^{-7}

* V_{GS} = -2.3 V, V_{DS} = -0.4 V

stress voltage.

In order to investigate the process-induced traps, RTS measurements were taken on different µm-sized pMOSFETs at room temperature. Upon finishing the RTS measurements on the MOSFETs in pre-stress condition, CHC was applied using V_{GS} = V_{DS} = -6.5 V for different durations to probe the stress-induced traps (Table 5.1). RTS experiments were done right after each stress step to minimize the effects of carrier relaxation. Measurements were

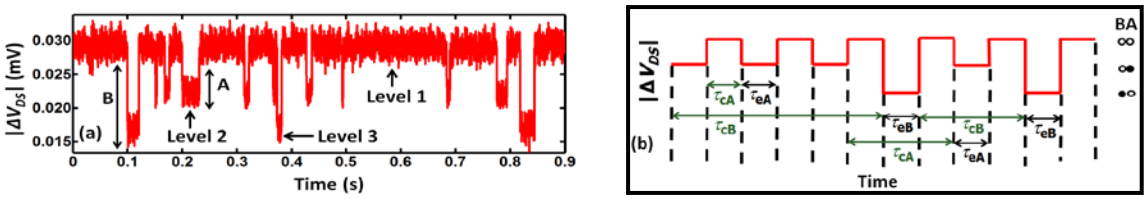

Fig 5.1 (a)– Sample RTS observed at V_{GS} = -2.4 V, V_{DS} = -0.4 V before applying any stress when traps A and B are active. Switching between levels 1↔2 was observed because of trap A, while trap B caused the switching between levels 1↔3; (b) Calculation of capture and emission times. Since both traps A and B are attractive centre traps, the upper level of the RTS magnitude corresponds to the capture time, and time spent at the bottom level is the emission time. Green arrows are used to show capture times, whereas black arrows are used to indicate emission times. The two circles at the right denote the states of traps B and A at different RTS levels. Empty circle indicates an empty hole trap (filled with an electron), while a filled circle indicates that the trap is filled with a hole (empty of an electron).

taken on eight pMOSFETs in total, among which representative results of one pMOSFET of $W \times L$ = 1 × 0.7 µm^2 are presented in this Chapter. For RTS experiments, V_{GS} was varied from -1.6 V to -3.6 V. While taking the RTS data due to a particular trap, V_{DS} was kept constant. Different traps became active at different V_{GS} ranges, as well as at different V_{DS} values. V_{DS} had to be varied between -0.2 V and -0.6 V to capture RTS due to all active traps. The C-V measurements were taken on a MOS capacitor of $W \times L$ = 90 × 100 µm^2 using the procedure described in Chapter 3. As mentioned in Chapter 3, the C-V data were used to calculate P_{inv} and T_{ox}. The DC characteristics were verified, and the threshold voltage and transconductance were found using the SPA. The MOSFETs were stressed using the SPA. Cumulative stress of 3000 seconds was applied using the aforementioned conditions with step size of 5 seconds to 500 seconds (Table 5.1). The sampling frequency and the total time span of the recorded RTS signal were adjusted to record at least 500 transitions between different RTS levels.

5.2 Results

Before application of any stress, a 3-level RTS was observed (Fig. 5.1(a)). A 3-level RTS can be attributed to two different traps [55]. The two pre-stress traps are named as A and B. After 200 seconds of stress, trap B

disappears and a new trap C was observed that resulted in another 3-level RTS (Fig. 5.2(a)). Later, traps B and C were found to be volatile in nature, appearing and disappearing with subsequent stress. A simple 2-level RTS (Fig. 5.3) was observed after 300 and 600 seconds of stress, where only trap A was active (Table 5.1). Upon 800 seconds of stress, a new trap D was observed (Fig. 5.4), which was later found to interact with the pre-stress traps A and B, and result in a 4-level RTS (Fig. 5.5(a)). After 2000 seconds of stress, traps A, B and C disappeared, and two new traps, E and F were observed (Figs. 5.6 and 5.7). Traps E and F disappeared after further stress. Two other traps, G and H appeared after 2500 seconds of stress (Figs. 5.8 and 5.9), which got deactivated after 3000 seconds of stress. The summary of the observed traps at each stress step is shown in Table 5.1. Each trap was differentiated from the

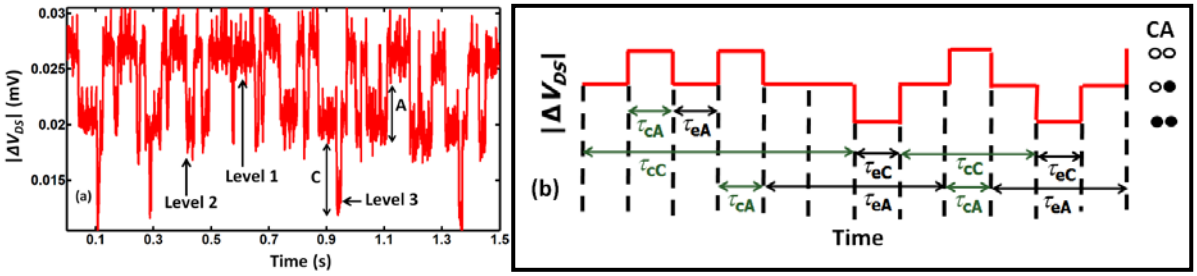

Fig 5.2 (a)- RTS observed at V_{GS} = -2.9 V, V_{DS} = -0.4 V, 200 seconds of stressing. A third level appeared in the signal which was observed due to trap C. Similar traces were observed after 400, 900, 1000 and 1200 seconds of stressing; (b)- Calcuration of capture and emission times for A and C. Unlike Fig. 1, no transitions between 1↔3 take place. Rather the transitions to level 3 occur from level 2. This also indicates that C is filled with a hole only if A is filled with a hole. Level 2 corresponds to emission time of A and capture time of C.

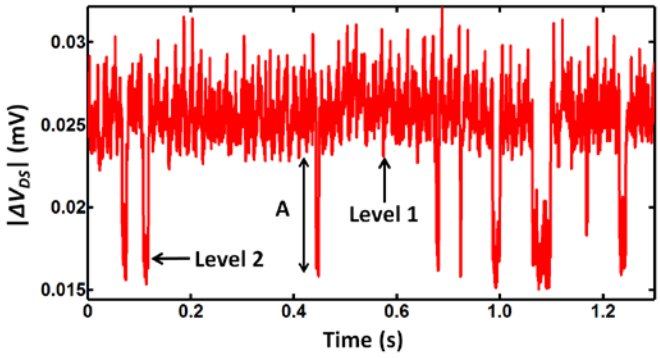

Fig 5.3 Sample RTS observed at V_{GS} = -2.3 V, V_{DS} = -0.4 V after 200 seconds of stressing when only trap A is active. Similar two-level RTS was observed at other bias and stress conditions when only trap A was active. The time spent at level 1 is the capture time, while level 2 corresponds to the emission time.

other traps by its active gate voltage ranges, average time constants, and RTS magnitude. Using the procedure explained in Chapter 4, the rate of change of time constant ratio with respect to gate voltage was used to find out if a trap is an attractive or a repulsive center. Depending on the number of active traps and number of bias points, RTS measurements duration after each step of stress varied from an hour to three and a half hours. During RTS

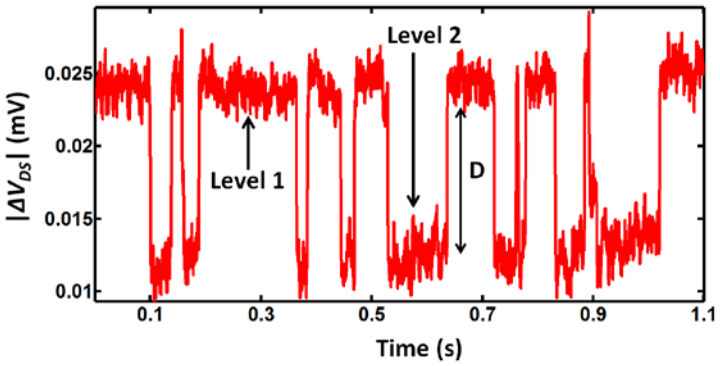

Fig 5.4 Sample RTS observed at V_{GS} = -1.6 V, V_{DS} = -0.6 V after 800 seconds of stressing when only trap D is active. Similar two-level RTS was observed at low gate voltages after 900 seconds of stressing.

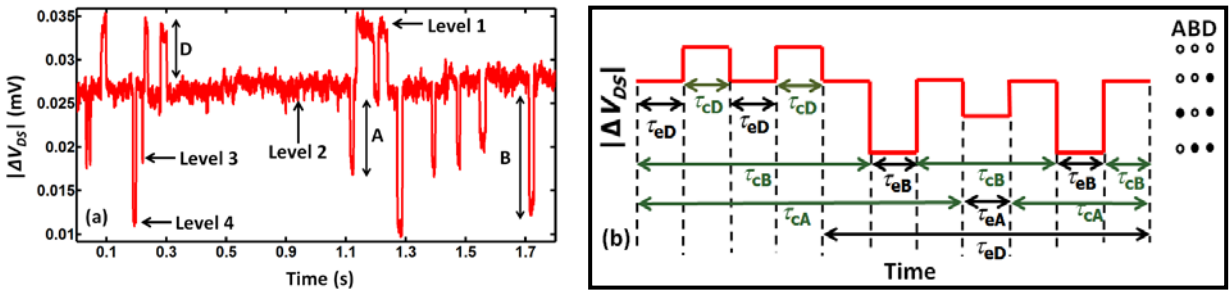

Fig 5.5 (a)- RTS observed at V_{GS} = -2.3 V, V_{DS} = -0.6 V after 800 seconds of stressing. In addition to trap D, traps A and B are also active resulting in a 4-level complex RTS. (b)- Calculation of capture and emission times. Since all three traps A, B, and D are attractive centers, upper level of the RTS magnitude due to a particular trap corresponds to the capture time, and bottom level corresponds to the emission time of the respective trap. States of each trap are shown at the right side.

measurements, only the permanent effects of stress were observed. During the RTS experiments at a particular stress time, the RTS recorded before that stress interval was not observed at any point. After 2500 seconds of stress, the device threshold voltage, hole mobility and gate leakage current varied by 23.7%, 35.8% and 37.6% respectively (Table 5.2). It is important to note that the traps mentioned above are the ones electrically active and close to the Fermi energy level and hence accessible to us with the oscilloscope sampling rate and measurement time spans.

5.3 Average Capture and Emission Times

Multiple traps might become active at the same time while taking the RTS measurements, resulting in complex RTS. MATLAB codes were written to calculate the average time spent at each RTS level using the same procedure described in Chapter 4. Since the switching probabilities follow Poisson's statistics, the time constants at each RTS level followed exponential distribution [56], [85]. For a particular trap, with the increase in gate voltage magnitude, the ratio of average capture to emission time decreases [82]. The pattern of each particular RTS level as

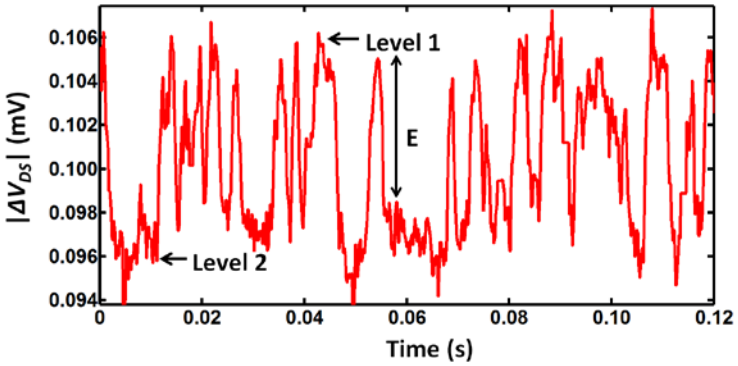

Fig 5.6 Sample RTS observed at V_{GS} = -2.1 V, V_{DS} = -0.2 V when only trap E is active.

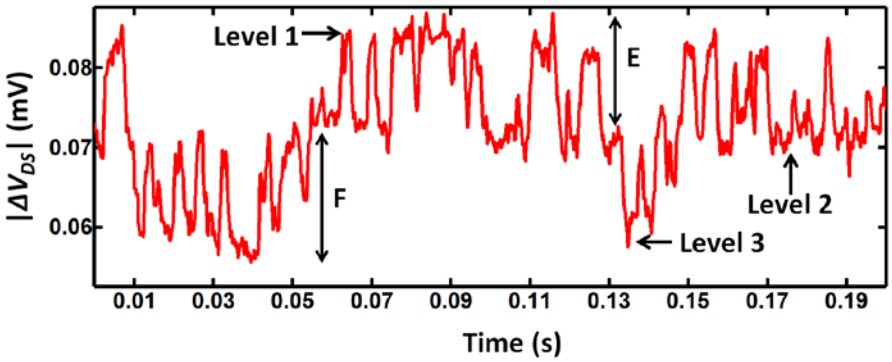

Fig 5.7 RTS at V_{GS} = -2.3 V, V_{DS} = -0.3 V when an additional level was observed because of trap F. Both the traps were observed at 2000 seconds of stressing. The capture and emission times were extracted using the same method as shown in Fig 5.2 (b).

a function of V_{GS} was observed to find out if a particular level corresponds to $\overline{\tau}_c$ or $\overline{\tau}_e$ for a particular trap. The upper level of $|\Delta V_{DS}|$ corresponded to $\overline{\tau}_e$ for trap H, and $\overline{\tau}_c$ for the other traps. Hence, traps A to G were found to be Coulombic attractive center traps, whereas trap H was found to be a repulsive center trap.

Extraction of $\overline{\tau}_c$ and $\overline{\tau}_e$ for a simple 2-level RTS is straight forward and explained in Chapter 4. However, calculation of $\overline{\tau}_c$ or $\overline{\tau}_e$ for a complex RTS is complicated and needs special attention. A sample RTS trace is shown in Fig. 5.1(a) where traps A and B are active. All transitions in the RTS in Fig. 5.1(a) take place from level 1. This indicates that the occupancy of traps A and B do not depend on each other. As both A and B are attractive centers, level 1 corresponds to $\overline{\tau}_c$ for both A and B, level 2 indicates $\overline{\tau}_e$ for A, and $\overline{\tau}_c$ for B, and level 3 belong to $\overline{\tau}_c$ for A and, $\overline{\tau}_e$ for B (Fig. 5.1(b)). After 200 seconds of stress when traps A and C are active, the switching events take place between levels 1↔2 and 2↔3 (Fig. 5.2(a)). Therefore, the occupancy of trap C is dependent on the occupancy of trap A. Using similar analysis procedure as explained in Chapter 4, average time spent at level 1 can be found as $\overline{\tau}_c$ for trap A, and mean time spent at level 3 is $\overline{\tau}_e$ for trap C (Fig. 5.2(b)). At level 2, trap A is filled with a hole and

trap C is empty of a hole. Hence, $\bar{\tau}_e$ for trap A is constituted by consecutive levels 2 and 3, whereas $\bar{\tau}_c$ for trap C is made up of levels 1 and 2 (Fig. 5.2(b)).

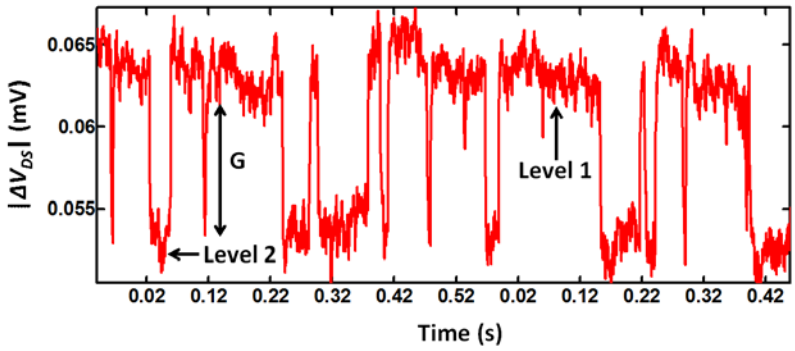

Fig 5.8 RTS recorded at V_{GS} = -1.7 V, V_{DS} = -0.2 V when only trap G is active.

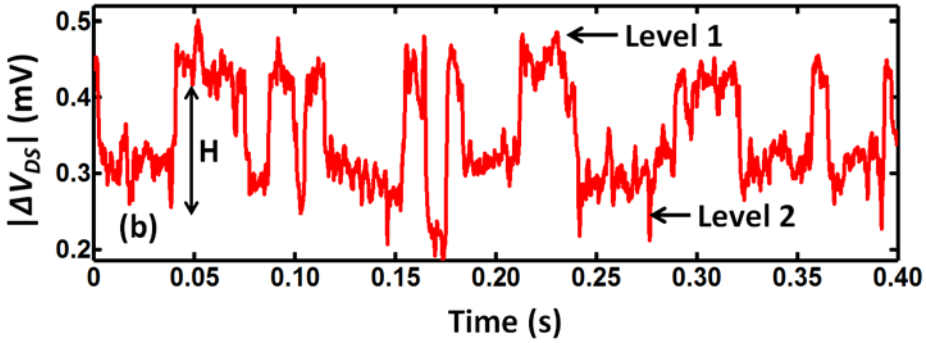

Fig 5.9 RTS at V_{GS} = -2.1 V, V_{DS} = -0.6 V, where only trap H is active. Both the traces were obtained after 2500 seconds of stressing. Trap H is a repulsive center. Therefore, unlike the other traps, for H level 1 corresponds to emission time, while level 2 corresponds to capture time.

After 800 seconds of stress, at lower gate voltages, a 2-level RTS was recorded, due to a new trap D (Fig. 5.4). Therefore, at higher gate voltages, when RTS because of traps A and B was added to the already present RTS, it was possible to identify 3 traps: A, B and D from the resultant 4-level RTS (Fig. 5.5(a)). Therefore, in Fig. 5.5(b), level 1 indicates $\bar{\tau}_c$ for traps A, B and D, level 2 belongs to $\bar{\tau}_c$ for A and B, and $\bar{\tau}_e$ for D, level 3 corresponds to $\bar{\tau}_c$ for B, and $\bar{\tau}_e$ for A and D, and finally, the time spent at level 4 is $\bar{\tau}_c$ for A, and $\bar{\tau}_e$ for B and D. In Figs. 5.1(b), 5.2(b) and 5.5(b), occupancies of the traps are shown. In addition, identification of $\bar{\tau}_c$ and $\bar{\tau}_e$ for each of the traps are included as well. As shown in Fig. 5.10, $\bar{\tau}_c$ or $\bar{\tau}_e$ of the traps did not show any dependence on stress time.

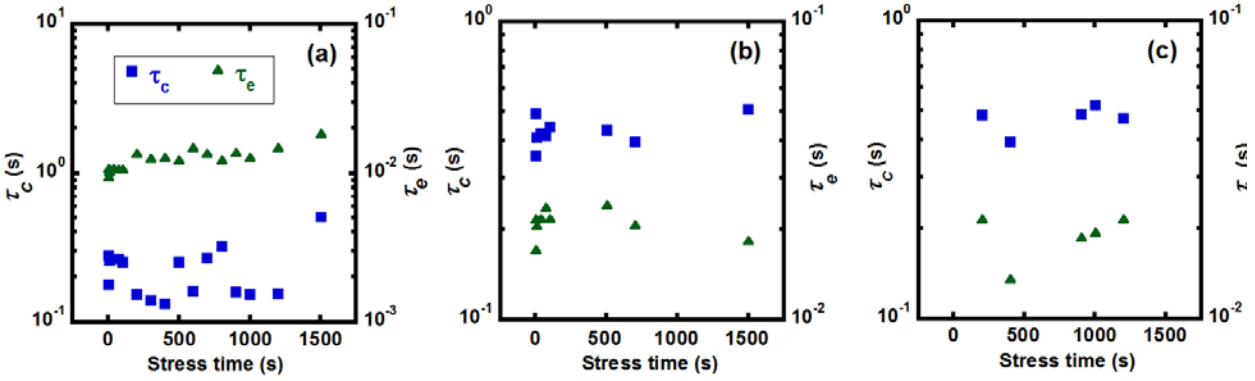

Fig 5.10. Plot of average capture and emission times with respect to stress time for (a) Trap A, (b) Trap B, and (c) Trap C. For traps A and B, V_{GS} = -2.4 V, V_{DS} = -0.4 V. For trap C, V_{GS} = -2.7 V, V_{DS} = -0.4 V. Capture and emission time constants did not show any particular dependence on stressing time for any of the traps.

5.4 RTS Amplitude

RTS amplitude for each trap was calculated from the difference in the Gaussian peaks in the amplitude histograms of the corresponding RTS levels [13]. RTS magnitude of trap H is around one order of magnitude higher than the other traps (Fig. 5.11 (a)-(h)). This is another indication that trap H is a repulsive center defect, while the other traps are attractive centers [82]. As explained in Chapter 4, normalized RTS magnitude is the resultant of two voltage fluctuation components: number fluctuations, and mobility fluctuations. Number fluctuations were calculated using P_{inv} obtained from the C-V data. After each stressing, for a particular trap, the applied V_{GS} range was kept the same to ensure a similar inversion layer. However, V_T may be shifted after each stressing. Hence, after a stressing interval, the inversion layer hole concentration at a particular V_{GS} may not be the same as the pre-stress condition. To solve this issue, while calculating P_{inv} at a particular stress, change in the threshold voltage (ΔV_T) at that stress was taken into account, and P_{inv} was calculated at the corresponding $V_{GS} - |\Delta V_T|$. At a given channel inversion condition, the contributions of the channel carrier number fluctuations should be the same no matter what the trap is. Since trap H is a repulsive center, the '+' sign is used between the two voltage fluctuation components in the UNMF model, whereas the '-' sign is used for the other traps. This addition of the two fluctuation components results in higher RTS amplitude in repulsive centers. This explains roughly one order of magnitude higher RTS

amplitude for H compared to others (Fig. 5.11). However, as a function of stress time, none of the traps show any particular behavior (Fig. 5.12).

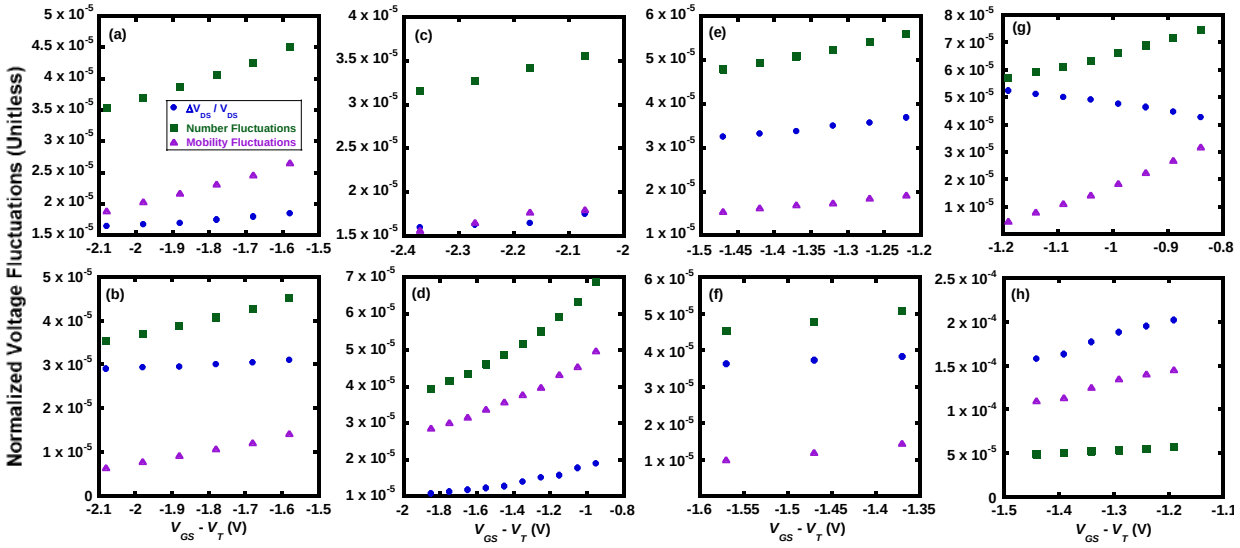

Fig 5.11 Drain voltage RTS fluctuations normalized to drain voltage, charge carrier number fluctuations, and mobility fluctuations for (a)- trap A at V_{DS} = -0.4 V, 0 sec stress; (b)- trap B at V_{DS} = -0.4 V, 0 sec stress; (c) trap C at V_{DS} = -0.4 V, 200 sec stress; (d)- trap D at V_{DS} = -0.6 V, 800 sec stress; (e)- trap E at V_{DS} = -0.2 V, 2000 sec stress; (f)- trap F at V_{DS} = -0.3 V, 2000 sec stress; (g)- trap G at V_{DS} = -0.2 V, 2500 sec stress; (h)- trap H at V_{DS} = -0.6 V, 2500 sec stress. H is a repulsive centre trap while the other 7 traps are attractive centres, which justifies the larger RTS magnitude due to trap H than that of the other traps. Repulsive centres also result in higher mobility fluctuations.

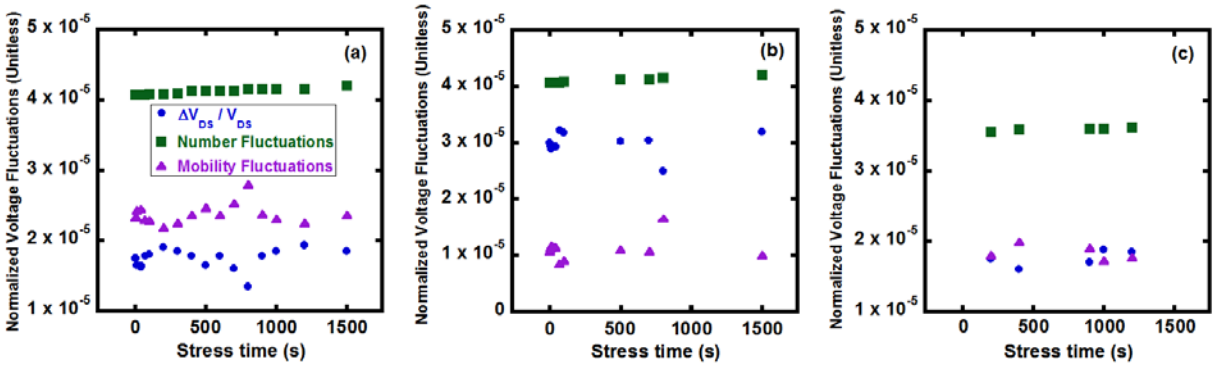

Fig 5.12. Plot of normalized RTS magnitude, number and mobility fluctuations as a function of stress interval for (a) Trap A, (b) Trap B, and (c) Trap C. For traps A and B, V_{GS} = -2.4 V, V_{DS} = -0.4 V. For trap C, V_{GS} = -2.7 V, V_{DS} = -0.4 V.

5.5 Trap Location From the Si-SiO_2 Interface

The trap distances from the Si-SiO_2 were from the $(\overline{\tau}_c/\overline{\tau}_e)$ ratio using the expression derived in Chapter 2. x_T of all the traps varied from 0.60 – 1.65 nm. As mentioned in Chapter 4, the Si-O bond length varies from 0.154-

0.169 nm [87] (Fig. 5.13(a)). Hence, the traps are located deeper than one SiO_2 tetrahedral structure from the Si-SiO_2 interface. Therefore, like the traps reported in Chapter 4, these traps are not Pb centers either. Comparing to the

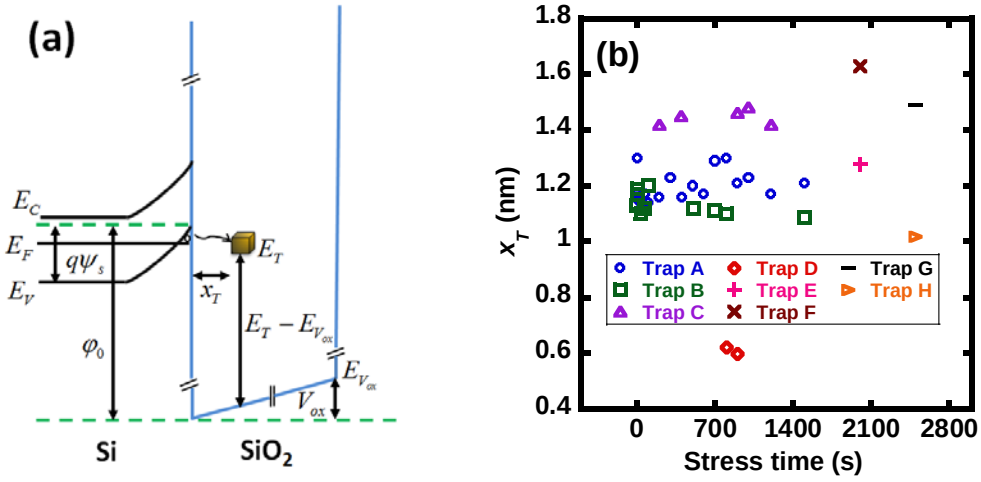

Fig 5.13 (a)– Band diagram of a pMOS at the source end of the channel; (b)-plot of trap distance from the Si/SiO_2 interface with respect to stress time. x_T and E_T - E_{Vox} values indicate that the traps are oxide traps that reside just below the silicon valence band edge.

process-induced traps, the stress-induced traps were found to be located both in the bulk SiO_2 and closer to the Si-SiO_2 interface. The random position of the stress-induced traps in the oxide can be attributed to the injection of hot carriers into the bulk oxide [110].

5.6 Trap Capture Cross-sections and Energy Level With Respect to Oxide Valence Band Edge

Trap capture cross-sections and $E_T - E_{V_{ox}}$ for traps A, B and C are shown in Fig 5.14 as a function of gate voltages at different stress times. $E_T - E_{V_{ox}}$ of all the traps varied from 4.6 eV to 4.78 eV, indicating that both the

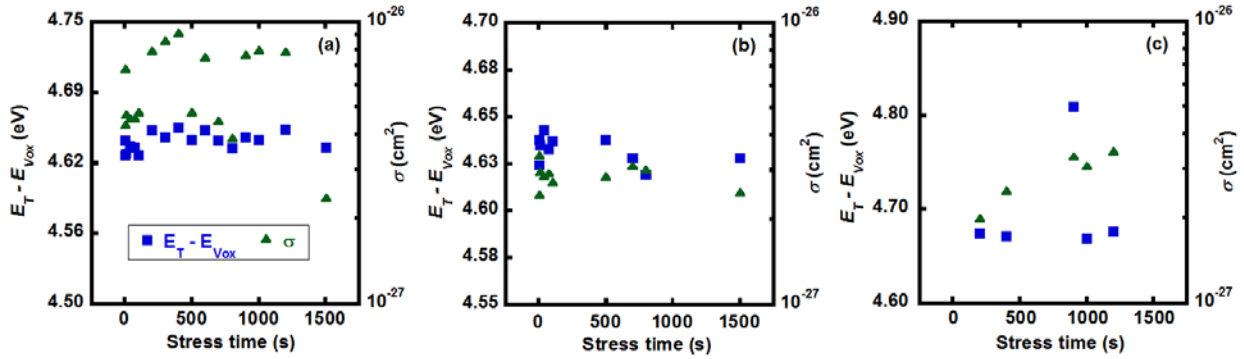

Fig 5.14. Plot of trap energy levels with respect to oxide valence band edge and capture cross-sections as a function of stress time for (a) Trap A, (b) Trap B, and (c) Trap C. For traps A and B, V_{GS} = -2.4 V, V_{DS} = -0.4 V. For trap C, V_{GS} = -2.7 V, V_{DS} = -0.4 V.

process-induced and stress-induced traps are located just below the valence band edge of silicon (Fig. 5.13(b)). Hence, the traps can readily capture channel holes at the active gate biases. σ and $E_T - E_{V_{ox}}$ for all traps are summarized at Table 5.3. The fact that $\bar{\tau}_c$ and $\bar{\tau}_c$ did not exhibit any particular trend as a function of stress time is

Table 5.3- Trap capture cross-sections and energy levels.

Trap	Capture cross-section (σ) (cm^2)	$E_T - E_{V_{ox}}$ (eV)
A (0 sec stress)	$4.92 – 7.92 \times 10^{-27}$	4.61 – 4.68
B (0 sec stress)	$2.61 – 5.88 \times 10^{-27}$	4.61 – 4.68
C (200 sec stress)	$4.83 – 6.35 \times 10^{-27}$	4.67 – 4.71
D (800 sec stress)	$3.42 – 6.37 \times 10^{-26}$	4.74 – 4.85
E (2000 sec stress)	$2.12 – 4.58 \times 10^{-25}$	4.66 – 4.71
F (2000 sec stress)	$5.98 – 18.3 \times 10^{-27}$	4.58 – 4.63
G (2500 sec stress)	$7.11 – 8.19 \times 10^{-26}$	4.64 – 4.67
H (2500 sec stress)	$5.65 – 5.81 \times 10^{-26}$	4.72 – 4.74

reflected in the invariability of σ and $E_T - E_{V_{ox}}$ (Fig. 5.14). For a particular trap, as similar values of σ and $E_T - E_{V_{ox}}$ were observed at each stress time, it is clear that the application of stress did not change the existing trap characteristics. Rather it affected only the creation, passivation, and reactivation of the traps. The σ and $E_T - E_{V_{ox}}$ values for all the process-induced as well as stress-induced traps were in the similar range as those of the traps listed in Chapter 4. This is the primary reason behind considering the attractive center traps earlier in this Chapter (both process-induced and stress-induced) as a pair of D-III-Si defects, and the repulsive center as puckered/back-projected oxygen vacancy defect.

5.7 Trap Creation, Trap Activation and Deactivation

Application of the large vertical electrical field during CHC is believed to be the reason behind the creation of E′ centers in the aforementioned device. The application of an electric field introduces lattice distortion that leads to charge polarization [111]. Because of the polarization, each SiO_2 molecule experiences a net local electric field that is much larger than the applied electric field. At the earlier mentioned stressed condition, the induced electric field reduces the activation energy of the Si-Si bond in an oxygen vacancy from 1.15 eV to 0.77 eV (Fig. 5.15) [111]. This lower activation energy indicates that the Si-Si bond breakdown process can take place at room temperature upon stressing. In addition, the broken structure shown in Fig. 5.19 resembles to the structures of the D-

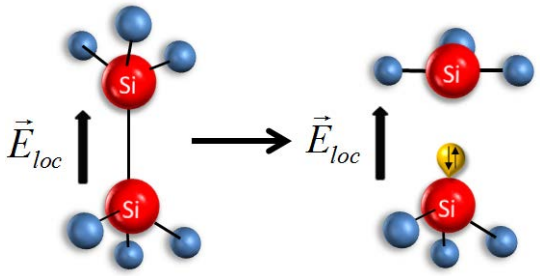

Fig 5.15 E′ center creation mechanism: Local electric field acting on a neutral oxygen vacancy. The strained Si-Si bond collapses into a planar sp^2 configuration. The remaining structure with two electrons in the sp^3 orbital can act as a hole trap.

III-Si and puckered/back-projected oxygen vacancy defect published by our group before [82]. The similarity of the broken structure, together with the match in the σ and $E_T - E_{V_{ox}}$ values suggest that the creation of E′ centers might be one of the reasons behind observing the stress-induced RTS. Self-heating (SH) of the channel carriers might, however, contribute to the generation of oxide defects as well. Self-heating of the channel carriers might become quite high during application of high gate and drain voltages. This self-heating might cause additional degradation in

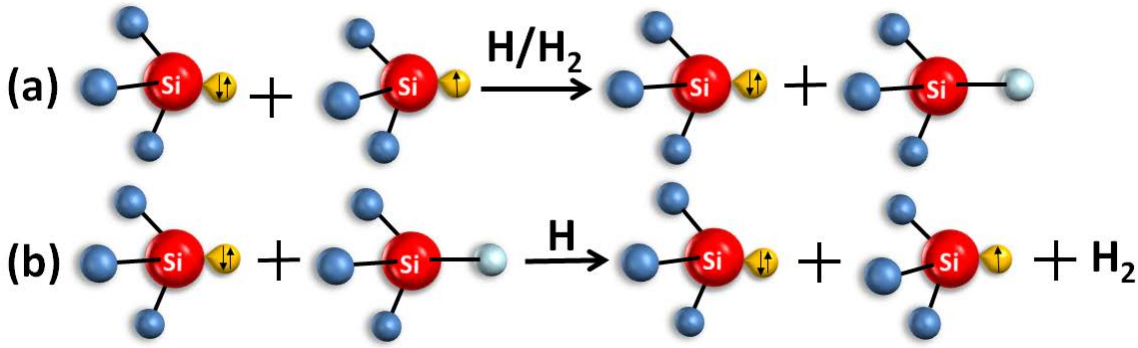

Fig 5.16 Trap deactivation and reactivation phenomena: (a)- Hydrogen passivation of the D-III-Si defect centre, resulting in a Si-H bond; (b)- passivated structure releases the hydrogen by reacting with another hydrogen atom, thus restoring its original structure.

the device threshold voltage and transconductance via trapping in interfacial and bulk oxide traps [112], [113]. Stressing at such high drain voltage causes damage primarily due to bulk oxide trap generation [114]. These SH-induced bulk oxide traps might get activated during MOSFET operation and cause additional RTS. Moreover, the SH mechanism can result in additional bias temperature instability (BTI) degradation and lead to errors in hot carrier injection (HCI) and time dependent dielectric breakdown (TDDB) lifetime predictions [115]. However, it was not possible to separate the effects of self-heating on degradation of the device characteristics and oxide trap generation.

Reaction of hydrogen atom released from the Si-SiO_2 interface due to channel hot carriers with E′ centers is proposed to be the reason behind volatility of traps B and C. The barrier for the hydrogen atom with an E′ center is ~0.4 eV [116], [117], whereas the reaction barrier for releasing the hydrogen by reacting with another hydrogen atom is <0.5 eV [118]. Hence, it is possible for both the reactions to readily take place at room temperature.

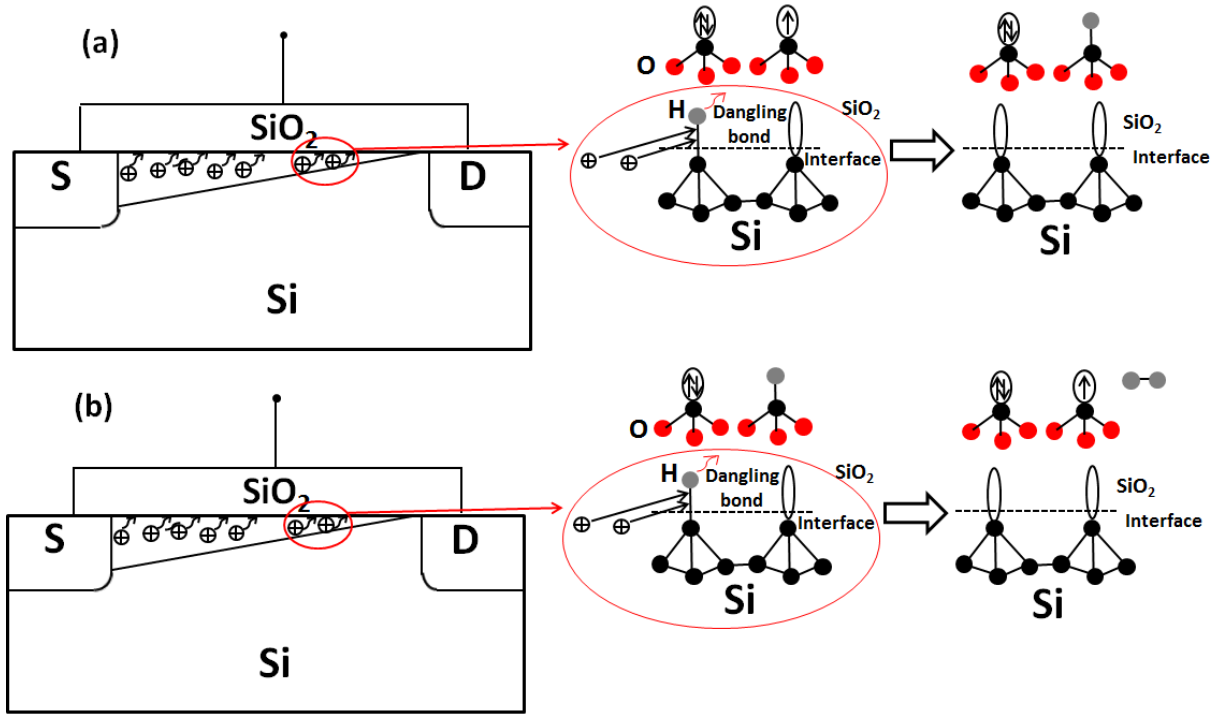

Fig 5.17 The proposed mechanism for trap volatility: (a)-Channel hot holes release a hydrogen atom from the Si-SiO_2 interface dissociating a Si-H bond. The released hydrogen atom drifts within the oxide to react with a pair of D-III Si defect. The reaction deactivates the defect; (b)-Upon further stressing, channel hot holes release another hydrogen atom from the Si-SiO_2 interface that drifts through the oxide towards the gate and reacts with the passivated D-III Si defect. The defect gets reactivated releasing a H_2 molecule. Black circles represent silicon atoms, red circles indicate oxygen atoms. Hydrogen atom is presented using grey circles, and dangling bonds are indicated using blank ovals. Ovals with bidirectional arrows indicate paired electrons while ovals with a single arrow represent single unpaired electrons.

Hydrogen atoms are already known for passivating and de-passivating interface defects [119]. The small barrier energies for the aforementioned reactions are indications that the capture and release of hydrogen atoms with E′ centers with subsequent stress might be the reason behind the volatility of the trapping centers B and C. The defects get passivated when they react with a hydrogen atom, and become reactivated again by releasing H_2 upon reacting with another stress-released hydrogen atom (Figs. 5.16(a)-(b)). The reactivation of an already passivated trap can obviously be another reason behind observing the stress-induced RTS.

$$Si^{\bullet} + H \rightarrow Si - H \quad (5.1)$$

$$Si - H + H \rightarrow Si^{\bullet} + H_2 \quad (5.2)$$

where "˙" represents a single unpaired electron, and Si-H indicates a single bond between silicon and hydrogen.

The primary concern remains about the source of the reactant hydrogen atoms. Presence of large amount of hydrogen in bound form has been reported before [120], [121]. Hydrogen can remain bound to the oxide-semiconductor interface, or get trapped by the defects residing in the oxide [122]. When the channel hot carriers are introduced, they cause impact damage to the Si-SiO_2 interface, and generate new interface traps releasing hydrogen atoms [123], [124]. The released hydrogen atoms drift towards the gate where they react with the oxide defects. The whole mechanism is presented in Fig. 5.17. The H/H_2 reaction/diffusion (R-D) model for interface traps depicts that the interface trap-released hydrogen atoms diffuse out from the Si-SiO_2 interface [125]. However, in our case, the applied negative bias drifts the hydrogen atoms towards the gate [126]. It is important to note that the R-D mechanism has been used to explain only the motion of the released hydrogen atoms in the oxide and their interactions with the E′ centers, not to represent the generation of oxide defects. In addition, application of high electric field and reaction of stress-released hydrogen atoms with the oxide defects are suggested only as the trap

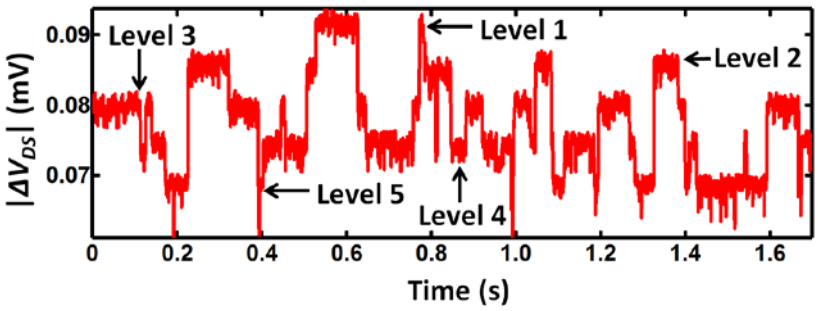

Fig. 5.18 A 5-level RTS observed at V_{GS} = -3.4 V, V_{DS} = -0.4 V after 5 seconds of stressing. Transitions between different levels in this signal are totally random, making it impossible to analyze.

generation, trap activation and passivation mechanism, not the phenomena responsible for RTS. The RTS theory has already been explained in Chapter 2.

Even though possible theories behind finding stress-generated RTS and trap volatility have been provided here, some other observations in this work are still beyond explanation. In addition to the RTS traces shown at the beginning of this Chapter, some more complex RTS were also recorded (Fig. 5.18). This might happen due to activation of more oxide traps, or metastability of the already existing defects. Such complex RTS is impossible to analyze and hence the reason behind such multi-level switching is still unknown. In addition, upon 200 seconds of stress, at higher gate voltages, the occupancy of a stress-induced trap was found to be dependent on that of a

process-induced trap. Trap C remained empty until trap A captures a hole (Fig. 5.2(b)). This means that trap C can release the bonded electron to the silicon valence band only if trap A releases its trapped electron back to the valence band. The physical reasons behind such finding are yet to be understood.

5.8 Variable Temperature RTS Measurements

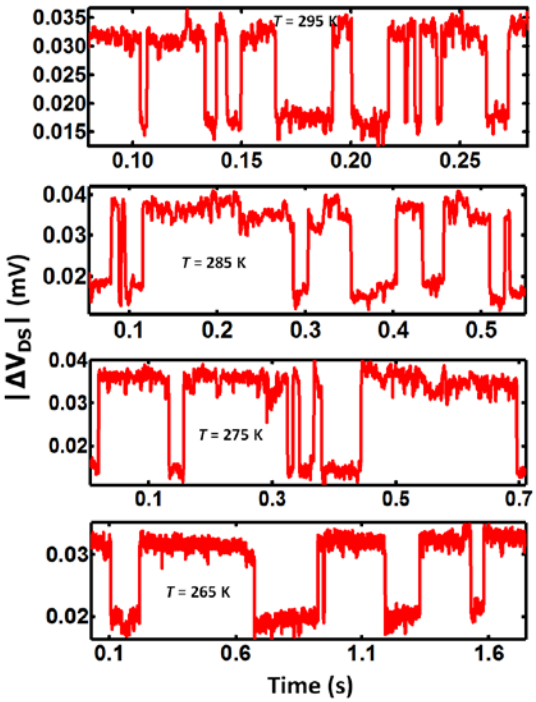

Fig. 5.19 Two-level RTS observed due to P41 at V_{GS} = -2.0 V, V_{DS} = -0.5 V. Similar two-level RTS was observed due to the other traps.

To investigate the trap energy parameters and the trap structures further, variable temperature RTS measurements were done in both fresh and stressed pMOSFETs. Using the same techniques and setup described in Chapter 3, RTS experiments were taken at different temperatures (255 K – 295 K). Stress was applied using the same bias conditions mentioned earlier in this Chapter at suitable intervals. Stress was applied only at room temperature to ensure that the carriers have sufficient energy to degrade the device characteristics. Variable temperature RTS measurements were taken as soon as the stress for a particular interval was finished. Measurements were done on 10 devices in total, among which 4 devices are reported in this Section: (i) SP41 with $W \times L = (1 \times 1)$ μm^2, in which a process induced trap P41 was observed, which disappeared after 50 seconds of stress, and two stress-induced traps, $S41_{50A}$ and $S41_{50B}$ were found to be active at two different bias ranges. The stress-induced traps

became inactive after further stress. (ii) SP221 of $W \times L = (1 \times 0.5)$ µm^2, in which a process-induced trap, P221 was present, which disappeared after stress, and no other trap was active upon stress. (iii) SP222 with $W \times L = (1 \times 0.5)$ µm^2, in which existence of a process-induced trap, P222 was found, which disappeared after stress. After 200

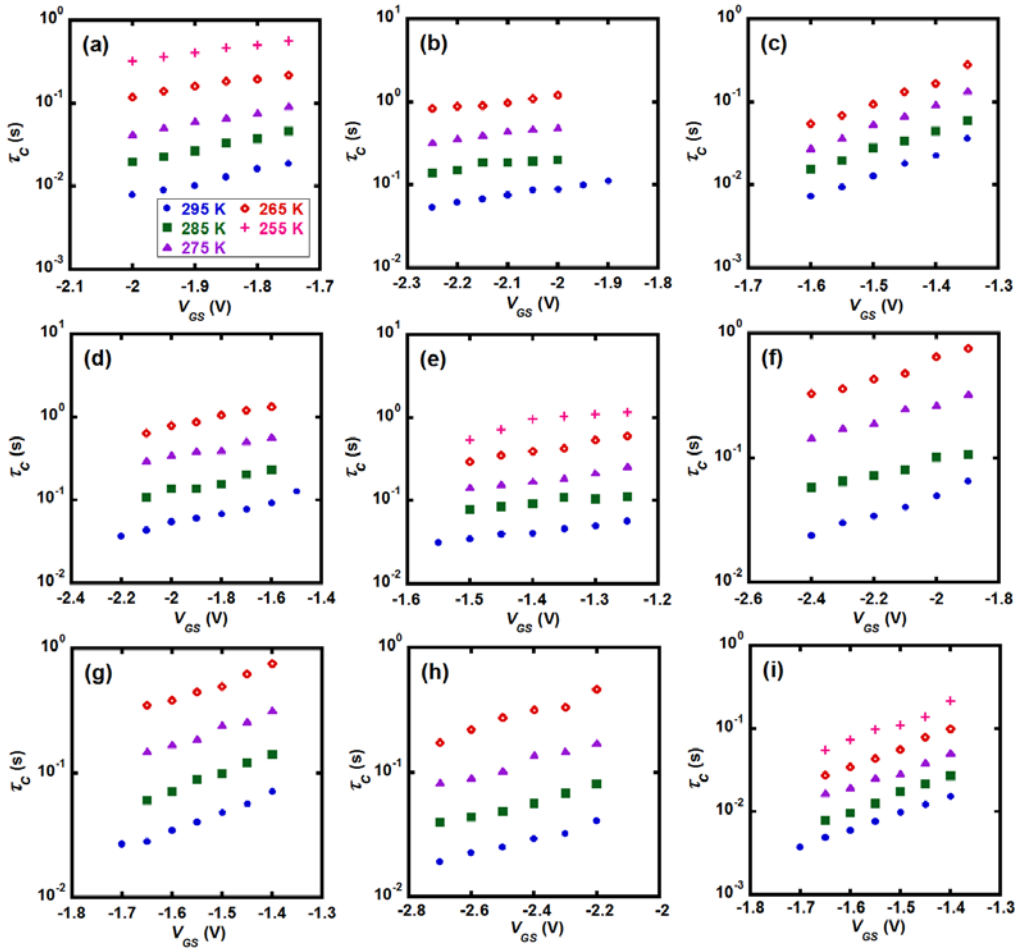

Fig 5.20 Average capture time constants as a function of V_{GS} at different temperatures for (a)- trap P221 at V_{DS} = -0.5 V, (b)- trap P222 at V_{DS} = -0.05 V, (c) trap $S222_{200}$ at V_{DS} = -0.15 V, (d)- trap P41 at V_{DS} = -0.5 V, (e)- trap $P41_{50A}$ at V_{DS} = -0.1 V, (f)- trap $P41_{50B}$ at V_{DS} = -0.3 V, (g)- trap P61 at V_{DS} = -0.1 V, (h)- trap $S61_{50}$ at V_{DS} = -0.2 V, (i)- trap $S61_{100}$ at V_{DS} = -0.1V. The mean capture times corresponded to the upper level of the RTS magnitude for all the traps, which means that all the traps were attractive centers.

Table 5.4– Threshold voltage of each device after different stress intervals at room temperature.

Cumulative stress time (sec)	SP221	SP222	SP41	SP61
0	-0.587	-0.517	-0.624	-0.602
50	-0.604	-0.570	-0.624	-0.602
100	-0.608	-0.594	-0.640	-0.609
200	-0.638	-0.717	-0.651	-0.612
500	-0.765		-0.681	-0.629
1000			-0.772	-0.743

seconds of stress, a stress-induced trap $S222_{200}$ was observed, and that trap was not present anymore after application of stress, and (iv) SP61 of $W \times L = (1 \times 0.7)$ μm^2, in which a process-induced trap, P61 was observed, which got deactivated after stress. Two stress-induced traps, $S61_{50}$, and $S61_{100}$ were observed after 50 and 100 seconds of stress, respectively. Trap $S61_{50}$ was absent when further stress was applied on the 50 seconds stressed-

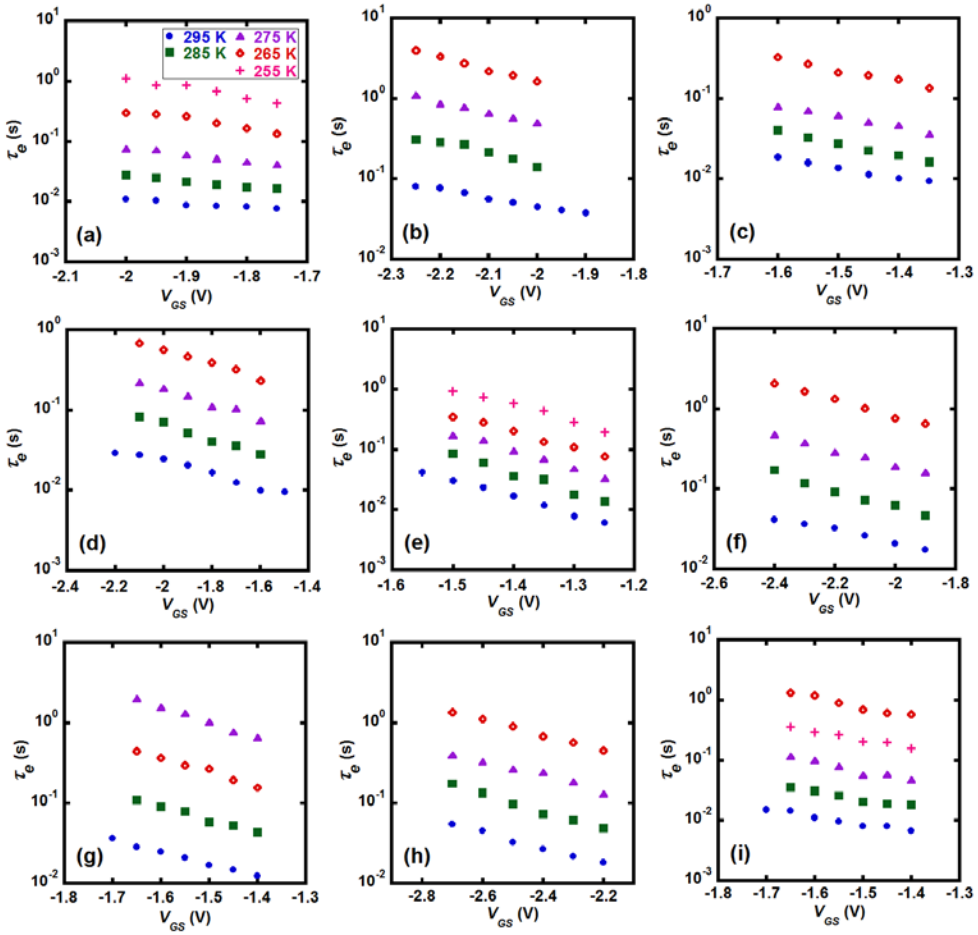

Fig 5.21 Average emission time constants as a function of V_{GS} at different temperatures for (a)- trap P221 at V_{DS} = -0.5 V, (b)- trap P222 at V_{DS} = -0.05 V, (c) trap $S222_{200}$ at V_{DS} = -0.15 V, (d)- trap P41 at V_{DS} = -0.5 V, (e)- trap $P41_{50A}$ at V_{DS} = -0.1 V, (f)- trap $P41_{50B}$ at V_{DS} = -0.3 V, (g)- trap P61 at V_{DS} = -0.1 V, (h)- trap $S61_{50}$ at V_{DS} = -0.2 V, (i)- trap $S61_{100}$ at V_{DS} = -0.1V. The mean emission times were found to be the average time spent at the lower level of the RTS magnitude for all the traps, meaning that all the traps were attractive centers.

device, and trap $S61_{100}$ was not active any more when the 100 seconds stressed-device was further stressed. Therefore, nine traps were found to be responsible in total: four process-induced and five stress-induced, each showing a simple 2-level RTS (Fig. 5.19). The first letters in the names of the traps denote whether the trap is process-induced or stress-induced. The first letter is followed by the device name. Finally, the number in the subscript in the trap names are the particular stress time in seconds at which the corresponding trap became active.

The threshold voltage degradation for each of the aforementioned four devices with stress times are shown in Table 5.4. Depending on the active range of a particular trap, V_{GS} was varied from -1.25 V to -2.7 V, range of V_{DS} was between -0.05 V and -0.5 V, and the temperature was varied between 255 K and 295 K decreasing 10 K at a time.

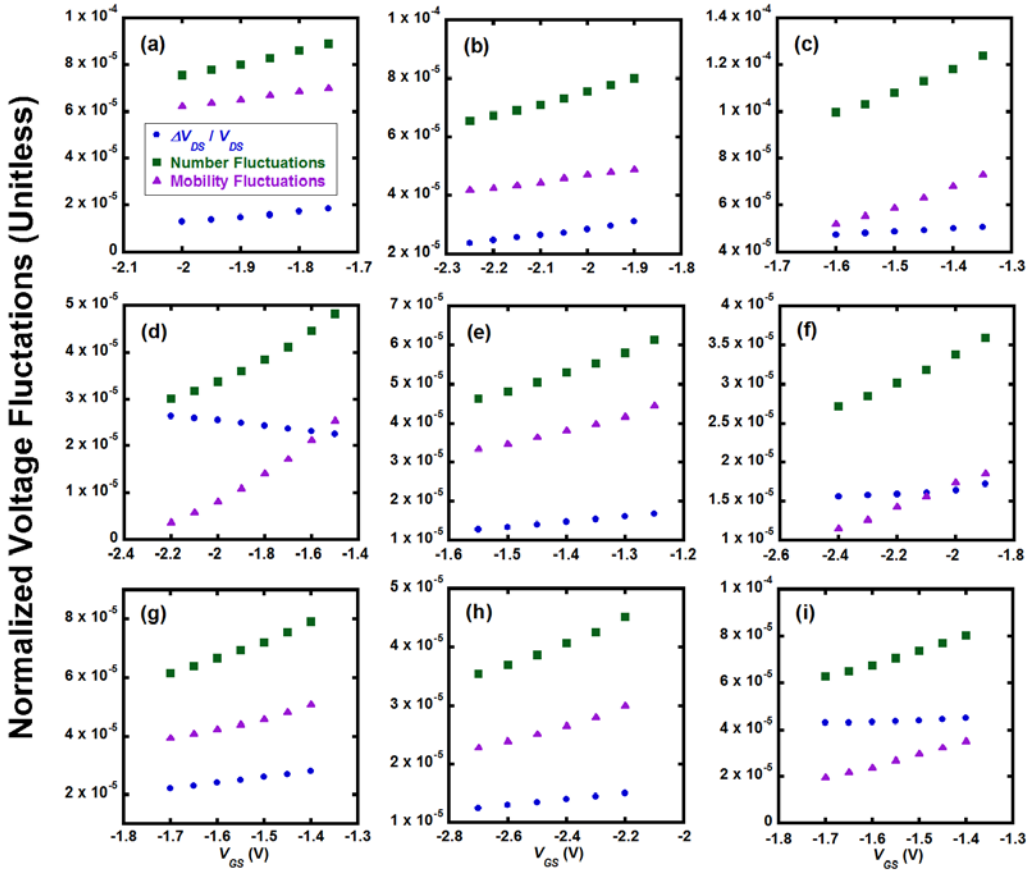

Fig 5.22 Normalized RTS magnitude, number fluctuations, and mobility fluctuations as a function of V_{GS} at room temperature for (a)- trap P221 at V_{DS} = -0.5 V, (b)- trap P222 at V_{DS} = -0.05 V, (c) trap $S222_{200}$ at V_{DS} = -0.15 V, (d)- trap P41 at V_{DS} = -0.5 V, (e)- trap $P41_{50A}$ at V_{DS} = -0.1 V, (f)- trap $P41_{50B}$ at V_{DS} = -0.3 V, (g)- trap P61 at V_{DS} = -0.1 V, (h)- trap $S61_{50}$ at V_{DS} = -0.2 V, (i)- trap $S61_{100}$ at V_{DS} = -0.1V. The RTS magnitudes of the traps were found to be in the similar range of values as the previously reported attractive center traps.

The fact that the all the process-induced and stress-induced traps disappear upon application of further stress indicates that stressing the devices does not alter the trap parameters. Rather stress affects only trap generation and deactivation. This supports the finding reported earlier in this Chapter. The average capture and emission time of each RTS traces (Fig. 5.20-5.21) is calculated using the same procedure described in Chapter 4. From the pattern of average time constants of higher and lower levels of RTS, all nine traps were found to be attractive centers. RTS magnitude and the normalized voltage fluctuations (Fig. 5.22) also match with those of the attractive centers reported earlier in this Chapter, and also in Chapter 4. x_T of the traps varied from 0.6 – 2.1 nm (Fig. 5.23). Hence,

just like the already reported traps, the aforementioned nine traps are not Pb centers.

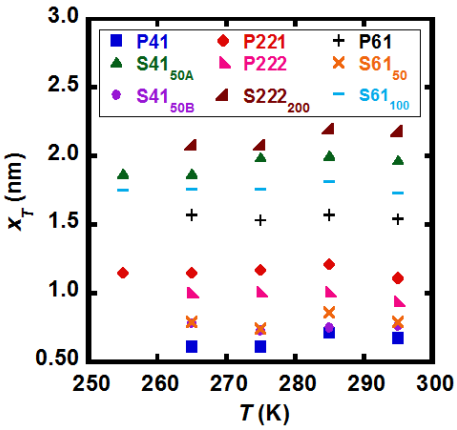

Fig. 5.23 Trap locations of all nine traps across all the measured temperatures.

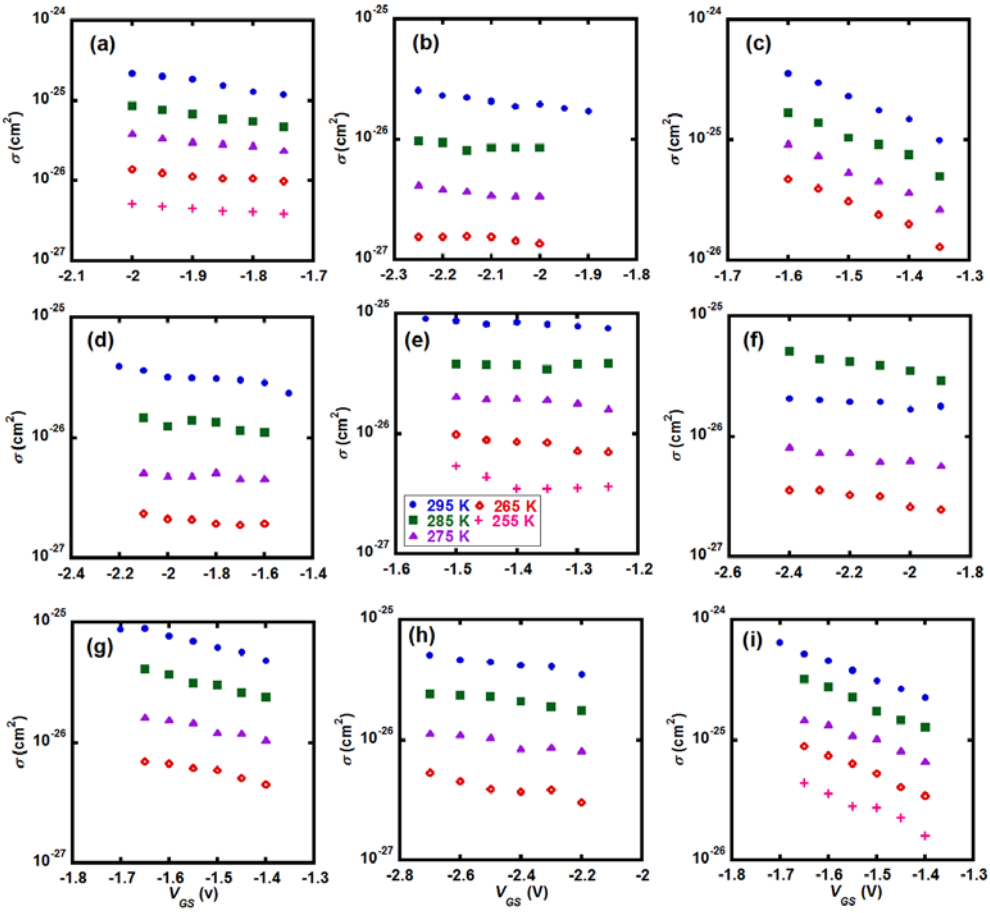

Fig. 5.24 Trap capture cross-sections as a function of V_{GS} at different temperatures for (a)- trap P221 at V_{DS} = -0.5 V, (b)- trap P222 at V_{DS} = -0.05 V, (c) trap $S222_{200}$ at V_{DS} = -0.15 V, (d)- trap P41 at V_{DS} = -0.5 V, (e)- trap $P41_{50A}$ at V_{DS} = -0.1 V, (f)- trap $P41_{50B}$ at V_{DS} = -0.3 V, (g)- trap P61 at V_{DS} = -0.1 V, (h)- trap $S61_{50}$ at V_{DS} = -0.2 V, (i)- trap $S61_{100}$ at V_{DS} = -0.1V.

Table 5.5- $E_T - E_{Vox}$ for all traps at room temperature. Similar values of $E_T - E_{Vox}$ were found at other temperatures.

Trap	$E_T - E_{Vox}$ (eV)
P221	4.68 – 4.72
P222	4.70 – 4.74
$S222_{200}$	4.56 – 4.63
P41	4.68 – 4.75
$S41_{50A}$	4.56 – 4.63
$S41_{50B}$	4.71 – 4.77
P61	4.61 – 4.67
$P61_{50}$	4.73 – 4.78
$P61_{100}$	4.62 – 4.68

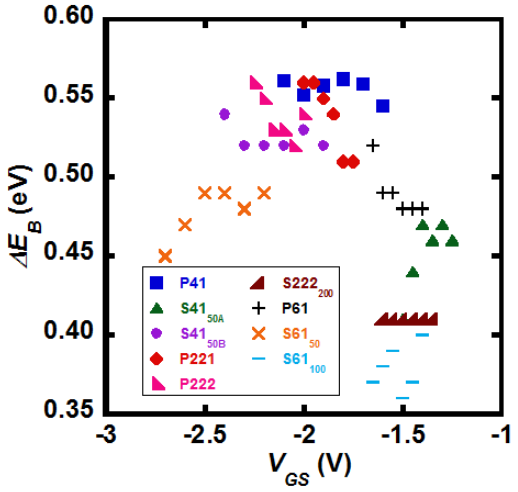

Fig. 5.25 Trap capture activation energies.

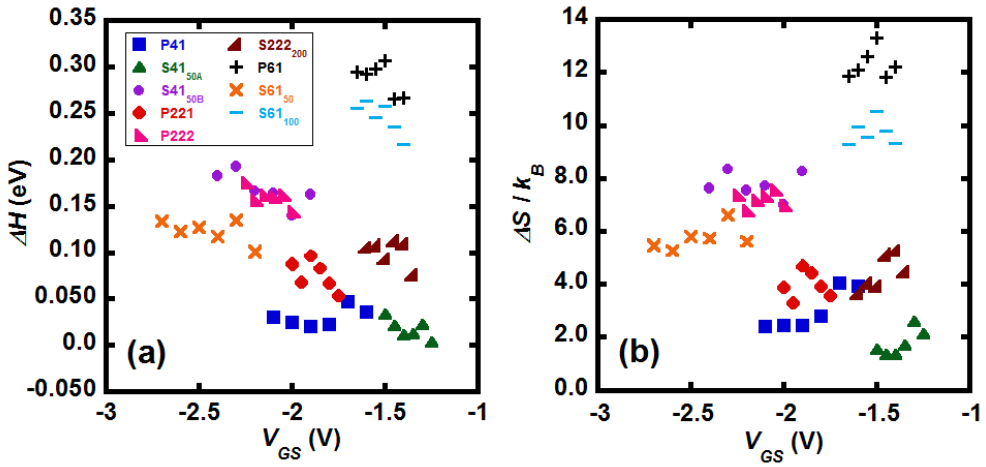

Fig. 5.26 (a) Change in enthalpy and (b) Normalized change in entropy of all traps.

σ (Fig. 5.24) and $E_T - E_{V_{ox}}$ (Table 5.5) values were in similar ranges as the other attractive center traps in Chapters 4 and 5. $E_T - E_{V_{ox}}$ values varied from 4.56 eV to 4.78 eV, once again indicating that the traps are located just below

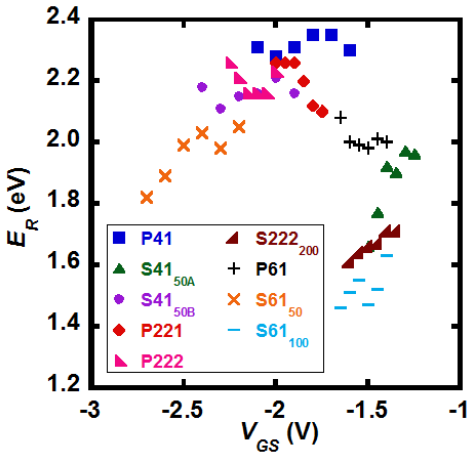

Fig. 5.27 Trap relaxation energies as a function of gate voltage at room temperature. Similar relaxation energies were obtained at other temperatures. The relaxation energies are within the similar range of the already reported attractive center traps.

the silicon valence band edge.

The values of ΔE_B, ΔH, ΔS and E_R for all the traps are shown in Figs. 5.25, 5.26(a), 5.26(b) and 5.27 respectively. σ, E_R, and $E_T - E_{V_{ox}}$ values of the traps are within similar ranges as the D-III Si defect pair, shown in Table 4.1. This confirms our conclusion made earlier in this Chapter that both process-induced and stress-induced attractive center traps are in fact D-III-Si defects. This also supports the trap generation mechanism explained in Fig. 5.15.

In summary, impact of introducing channel hot carriers on creation or passivation of traps responsible for RTS in pMOSFETs has been explored in detail, and presented in this Chapter. Applied stress was found to activate and deactivate traps, but not alter their RTS characteristics. The capture cross-section, σ and $E_T - E_{V_{ox}}$ values for the traps obtained from room temperature RTS experiments were in similar ranges as the σ and $E_T - E_{V_{ox}}$ for the traps reported in Chapter 4. Therefore, the process-induced and stress-induced attractive center traps were suggested to be a pair of D-III-Si defects, and the repulsive center was proposed to be a puckered/back-projected oxygen vacancy center defect. Application of high vertical field is thought to be the primary reason behind creating stress-

induced defects. Movement of stress-released hydrogen atoms within the SiO_2 and their reactions with the newly generated and already passivated E′ center defect are most likely the mechanism behind observing volatile traps upon stress. Later, variable temperature RTS measurements were carried out. From the trap characteristic parameters, the process-induced and stress-induced attractive center defects were found to be D-III-Si defects, which supports the conclusions made from the room temperature RTS measurements. The observations and theory behind such remarks that are presented in this Chapter can bring new insight into the effects of stress on RTS in pMOSFETs as RTS in pMOSFETs have been severely underreported compared to nMOSFETs.

Chapter 6 Flicker Noise Measurements and Analyses

Flicker noise or 1/f noise is one of the major sources of noise in MOSFETs. Flicker noise is observed due to the interaction of a large number of traps with distributed trapping time constants situated at the Si-SiO_2 interface or in the oxide with the channel carriers. In frequency domain, the power spectral density (PSD) of a RTS trace is given by a Lorentzian spectrum [29]. When a large number of traps with different trapping time constants become active at the same time, each of the active traps corresponds to a Lorentzian of a specific corner frequency. The individual Lorentzians get added and the final shape looks like a 1/f noise spectrum – a straight line with a downward slope of ~1 (Fig. 6.1) [127]. Therefore, RTS measurements are typically taken on small area devices (<1 μm^2), whereas the flicker noise experiments are done on large area devices (>1 μm^2). The effects of different gate

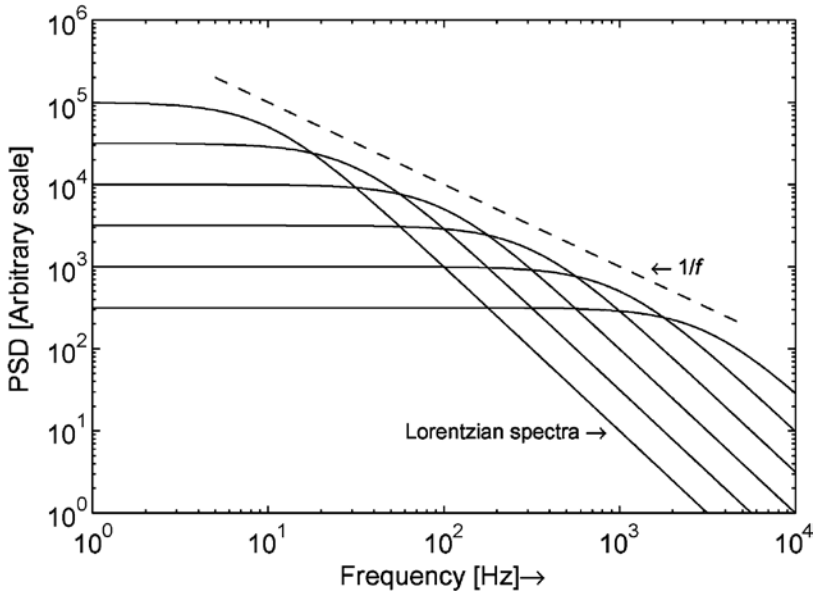

Fig. 6.1 Individual Lorentians with different corener frequencies are added to result in 1/f noise spectrum. Reprinted with permission from [127].

oxide processing techniques on oxide defects leading to low-frequency noise in MOSFETs need to be quantified. The contributions to low frequency noise by all types of oxygen vacancies such as Pb centers and E′ centers need to be reduced as much as possible, and a realistically achievable limit of flicker noise need to be determined. The main goal of this study was to investigate the effects of different gate oxide processing techniques on oxide defects that act as electron traps and are responsible for RTS or 1/f noise.

In this work, flicker noise measurements were performed on different sized nMOSFETs of three different wafers that were fabricated using different processing techniques by Texas Instruments. The voltage PSDs of nMOSFETs from the three wafers were normalized with respect to W, L, and T_{ox} to achieve meaningful comparison. The process steps used in fabricating the wafers were related to the amount of flicker noise observed. Finally, the number and mobility fluctuations observed on the three wafers were compared to find out the dominant noise mechanisms.

6.1 Device Specifications, Measurement Conditions

An HP 3562A Dynamic Signal Analyzer was used to obtain the flicker noise spectra of nMOS devices of different sizes from three different technologies, referred as X2388, X2550, and X2396. The gate dielectric of all three wafers is SiO_2. The nominal oxide thickness of X2388, X2550, and X2396 are 8.7 nm, 12.1 nm, and 12.7 nm, respectively. The channel widths of the measured devices varied from 0.5 µm to 20 µm, and the channel lengths varied from 1 µm to 10 µm. Verification of the device functionality, DC characteristics extraction, biasing the devices, and C-V characteristics extraction were done following the same procedure described in Chapter 3. Once flicker noise spectrum was observed in the dynamic signal analyzer, measurements were taken for $V_{GS} - V_T$ = 0.25 V to 2.25 V with a step size of 0.25 V, keeping the drain voltage fixed at 0.2 V. For each bias point, the voltage noise spectrum was observed for 3 decades of frequency, from 1 Hz to 1000 Hz. The drain current at each bias point was measured using a multimeter, and the conductance (g_D) was found using $g_D = I_{DS}/V_{DS}$. Flicker noise PSDs in MOSFETs of the three wafers with similar dimensions were compared together. Based on the dimensions, the MOSFETs were divided into seven different categories where similar devices with similar gate area were kept in the same category:

(i) MOSFETs with $W \times L$ = 1×10 µm^2 and 1×5 µm^2 from the wafer X2388, $W \times L$ = 1×10 µm^2 from X2550, 1×20 and 1×4 µm^2 from X2396.

(ii) MOSFETs with $W \times L$ = 5×0.7 µm^2 from X2388, $W \times L$ = 5×0.7 µm^2 from X2550, and 6×0.6 µm^2 from X2396.

(iii) MOSFETs with $W \times L$ = 5×1 µm^2 from X2388, and $W \times L$ = 5×1 µm^2 from X2550.

(iv) MOSFETs with $W \times L$ = 10×1 μm^2 from X2388, $W \times L$ = 10×1 μm^2 from X2550.

(v) MOSFETs with $W \times L$ = 5×10 μm^2 from the X2388, $W \times L$ = 5×10 μm^2 from X2550, and 6×20 μm^2 from X2396.

(vi) MOSFETs with $W \times L$ = 10×10 μm^2 from the X2388, $W \times L$ = 10×10 μm^2 from X2550, and 4×20 μm^2 from X2396.

(vii) MOSFETs with all other dimensions from the three wafers.

6.2 Analysis Procedure

At each gate voltage, the background noise (obtained at V_{DS} = 0 V) was subtracted from the measured 1/f noise (Fig. 6.2(a)). A straight line was fitted on each log-log voltage noise PSD plot to as high frequency as possible. The value of γ, the frequency component of 1/f$^{\gamma}$ spectral shape was obtained from that fitting (Fig. 6.2 (a)). For the small length devices, there were some bias points at which either RTS was observed, or the flicker noise magnitude could not be distinguished from the background noise by more than one order of magnitude. Those noise data were excluded from the analysis. For comparing the noise magnitude of different devices, the curve-fitted 10 Hz noise magnitude was used.

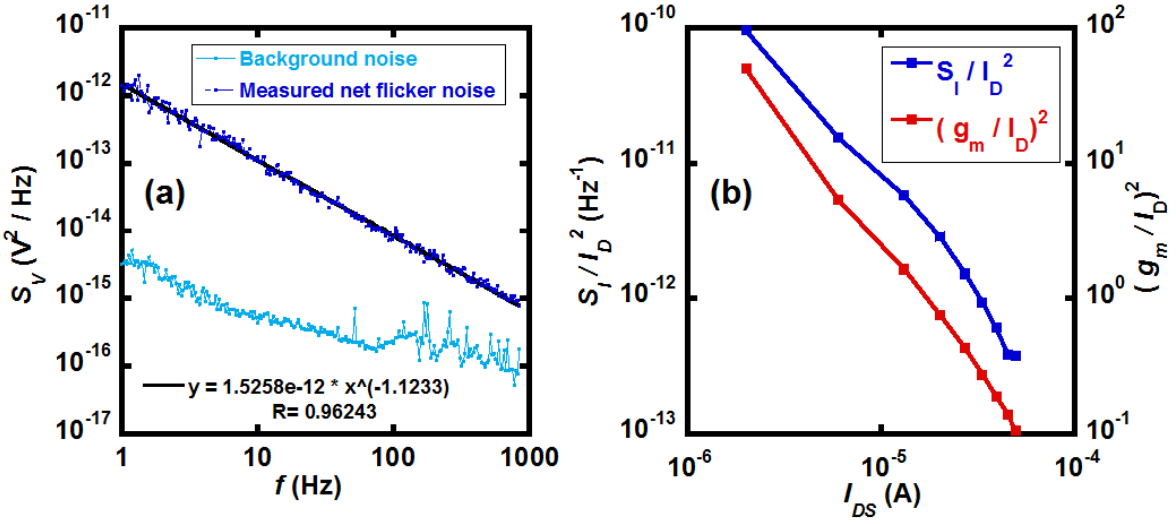

Fig. 6.2. (a) Background, net measured, and curve fitted flicker noise spectrum (b) Current noise PSD and $(g_m/I_D)^2$ for a MOSFET of $W \times L$ = 1 × 1 μm^2 from X2388.

The drain current noise magnitude was calculated using $S_{I_{DS}} = g_D^2 S_{V_{DS}}$, where $S_{V_{DS}}$ is the drain-source voltage noise PSD. The transconductance was extracted through

$$g_m = \frac{\delta I_{DS}}{\delta V_{GS}} = \mu C_{ox} \frac{W}{L} V_{DS} \tag{6.1}$$

For all MOSFETs, the normalized current noise spectrum showed the similar trend as $\left(g_m / I_D\right)^2$ as a function of I_{DS}, which indicates that the flicker noise observed in these devices follow the number fluctuation theory (Fig. 6.2 (b)) [50]. Normalization of the noise spectra was done according to the number fluctuation theory to achieve a meaningful comparison of the three different wafers [50].

$$\frac{S_{I_{DS}}(f) WL}{I_{DS}^2 T_{ox}^2} = \frac{k_B T q^2 N_t(E_F)}{\lambda f \varepsilon_{ox}^2} \frac{g_m^2}{I_{DS}^2} \tag{6.2}$$

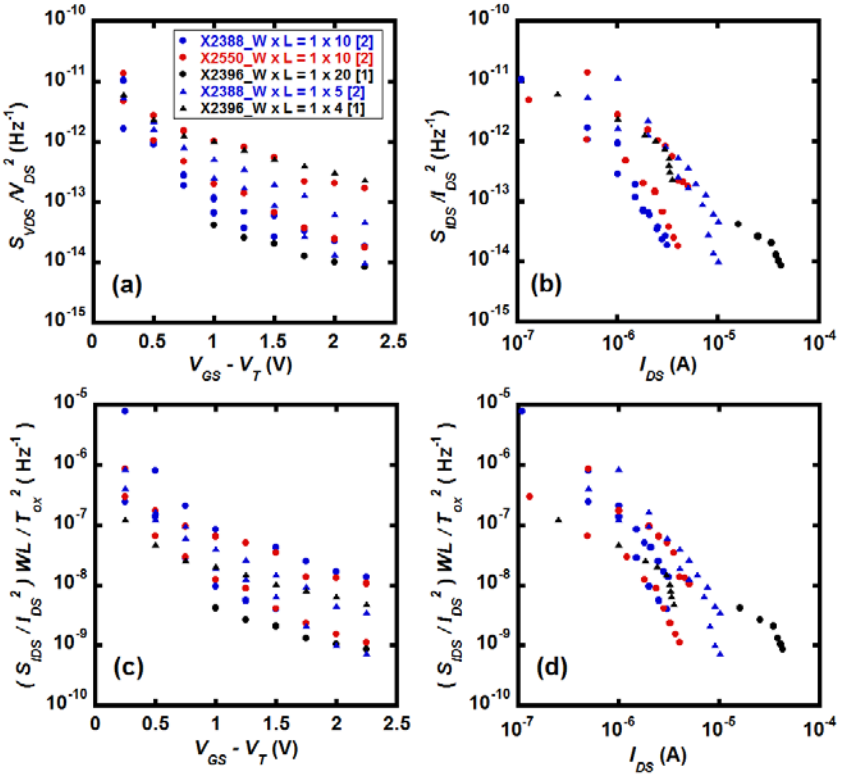

Fig. 6.3 Comparison of (a) voltage noise magnitude, (b) current noise magnitude, (c) and (d) normalized current noise magnitude for the MOSFETs of $W \times L$ = 1 × 10 μm^2 and 1 × 5 μm^2 from the wafer X2388, $W \times L$ = 1 × 10 μm^2 from X2550, 1 × 20 and 1 × 4 μm^2 from X2396. The numbers in the brackets denote the number of MOSFETs measured for that particular dimension.

6.3 Results

Normalized voltage and current noise magnitude for all the categories of the MOSFETs are shown in Figs. 6.3-6.9.

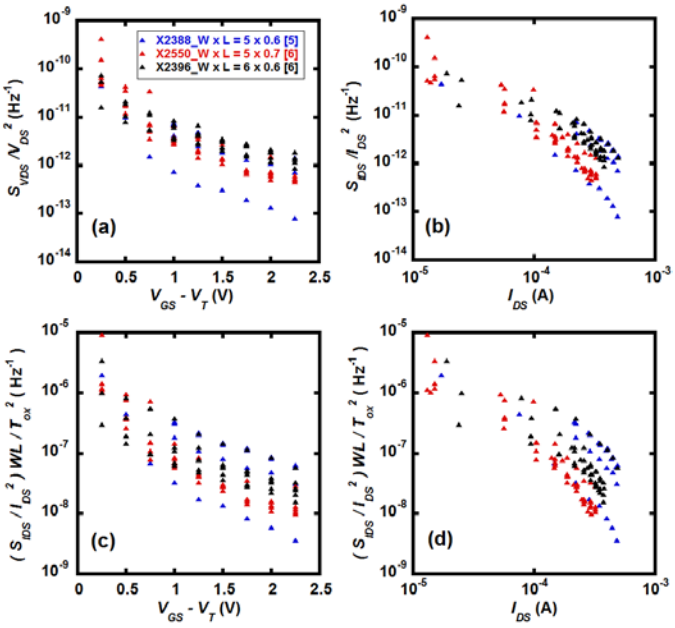

Fig .6.4 Comparison of (a) voltage noise magnitude, (b) current noise magnitude, (c) and (d) normalized current noise magnitude for the MOSFETs of $W \times L = 5 \times 0.6$ µm^2 from X2388, $W \times L = 5 \times 0.7$ µm^2 from X2550, and 6×0.6 µm^2 from X2396. The numbers in the brackets denote the number of MOSFETs measured for that particular dimension.

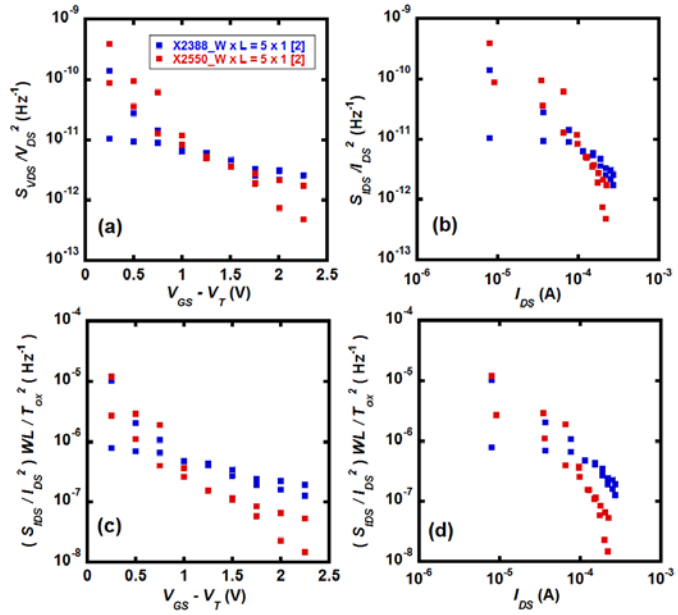

Fig. 6.5 Comparison of (a) voltage noise magnitude, (b) current noise magnitude, (c) and (d) normalized current noise magnitude for the MOSFETs of $W \times L = 5 \times 1$ µm^2 from X2388, and $W \times L = 5 \times 1$ µm^2 from X2550. The numbers in the brackets denote the number of MOSFETs measured for that particular dimension.

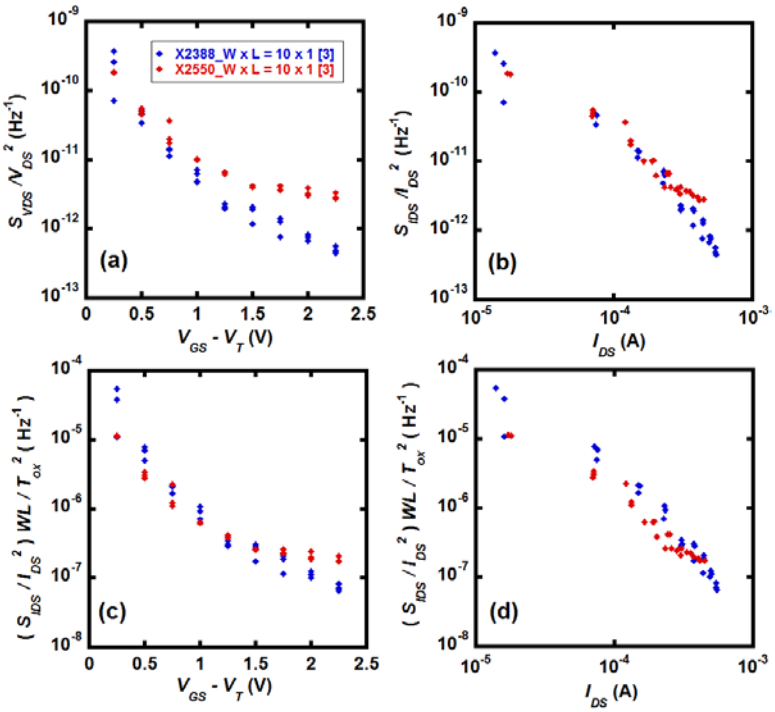

Fig. 6.6 Comparison of (a) voltage noise magnitude, (b) current noise magnitude, (c) and (d) normalized current noise magnitude for the MOSFETs of $W \times L = 10 \times 1$ μm^2 from X2388, and $W \times L = 10 \times 1$ μm^2 from X2550. The numbers in the brackets denote the number of MOSFETs measured for that particular dimension.

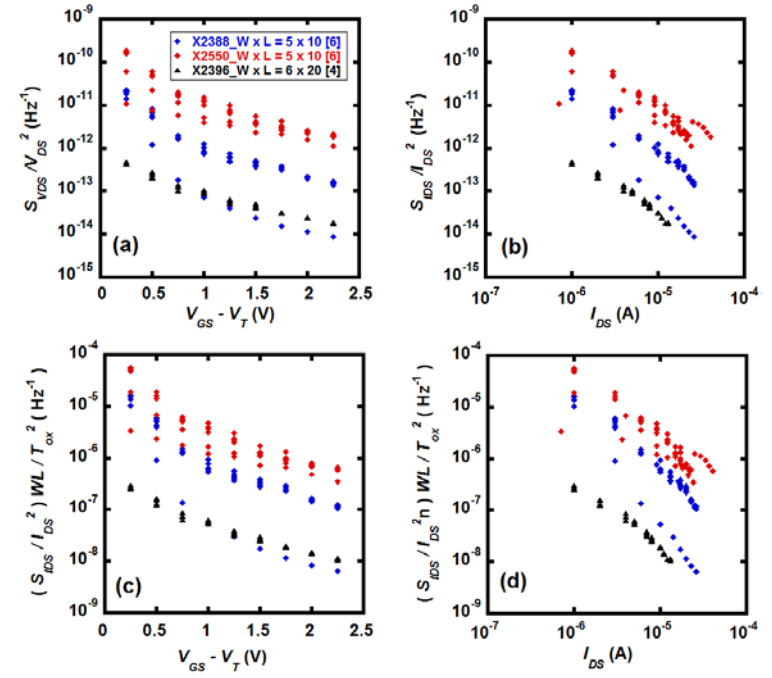

Fig. 6.7 Comparison of (a) voltage noise magnitude, (b) current noise magnitude, (c) and (d) normalized current noise magnitude for the MOSFETs of $W \times L = 5 \times 10$ μm^2 from X2388, $W \times L = 5 \times 10$ μm^2 from X2550, and 6×20 μm^2 from X2396. The numbers in the brackets denote the number of MOSFETs measured for that particular dimension.

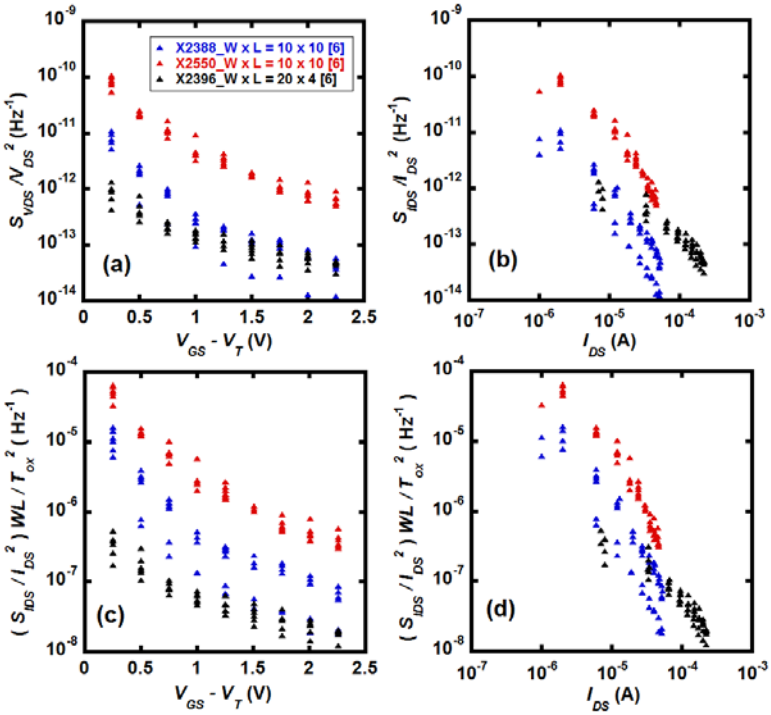

Fig. 6.8 Comparison of (a) voltage noise magnitude, (b) current noise magnitude, (c) and (d) normalized current noise magnitude for the MOSFETs of $W \times L = 10 \times 10$ μm^2 from X2388, $W \times L = 10 \times 10$ μm^2 from X2550, and 4×20 μm^2 from X2396. The numbers in the brackets denote the number of MOSFETs measured for that particular dimension.

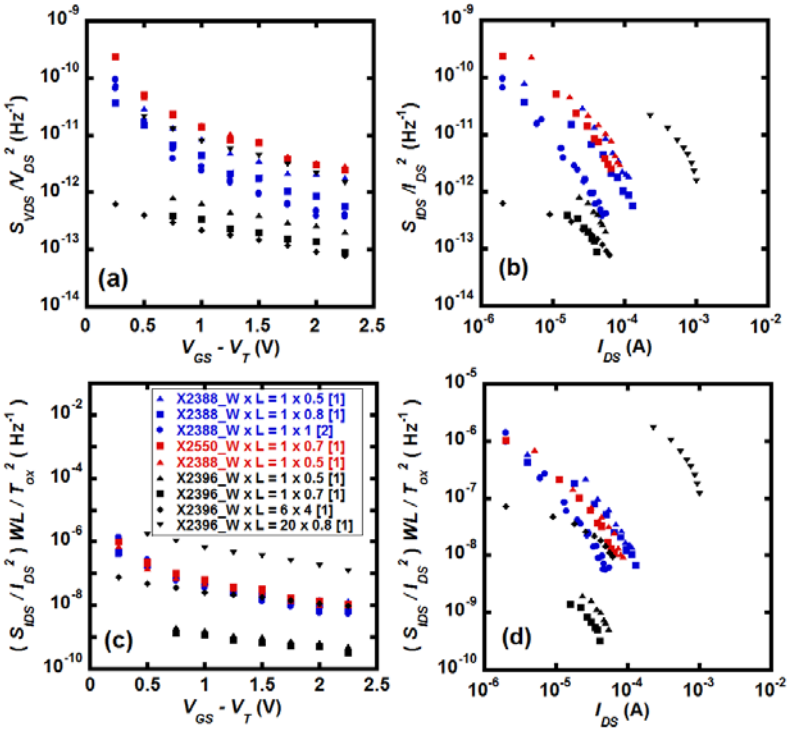

Fig. 6.9 Comparison of (a) voltage noise magnitude, (b) current noise magnitude, (c) and (d) normalized current noise magnitude for the MOSFETs which don't fall into the first six categories. The numbers in the brackets denote the number of MOSFETs measured for that particular dimension.

Figures 6.3-6.9 show that MOSFETs falling in categories (i), (ii), (iii), (iv) and (vii) (smaller gate area comparing to the other two categories) do not provide trustable noise data to compare the gate oxide process variations. Only the large area MOSFETs (>10 μm^2) in categories (v) and (vi) provide a consistent pattern of flicker noise PSDs of the three wafers. MOSFETs in wafer X2396 showed the lowest amount of noise, whereas MOSFETs in X2388 and X2550 showed intermediate and highest amount of 1/f noise, respectively. These observations also justify the fact that with the decrease in gate area, the variability in the measured 1/f noise increases [24]. The data obtained from MOSFETs of categories (v) and (vi) were studied thoroughly, and were be used for further research works.

6.4 Relation of Process Techniques with the Amount of Observed Flicker Noise

The three wafers were fabricated using three different process techniques. Differences in the fabrication steps such as doping concentrations, dose of dopants, annealing temperature led to the difference in the obtained 1/f noise in the wafers. Rapid increase of oxygen vacancy has been reported if greater than 875^0C is used as an annealing temperature [128]. The annealing temperature for X2388, X2550 and X2396 were 850^0C, 900^0C, and 850^0C, respectively. Therefore X2550 is expected to show higher 1/f noise than the other two wafers, which matches with the results of our experiments.

Fluorine implantation has been used in the wafers X2550 and X2396. Fluorine is capable of creating Si-F bond with the oxygen vacancies located at or near the Si-SiO_2 interface [129]. Hence the silicon dangling bonds presented at the interface or bulk oxide get passivated and less 1/f noise is observed [130]. Higher dose of fluorine implantation in X2396 would allow diffusion of more fluorine atoms through the oxide layer towards the Si-SiO_2 interface [131]. Therefore, X2396 was predicted to show less amount flicker noise than the other two wafers. The results in our experiments matched with this prediction.

Wafers X2550 and X2396 were sintered with H_2 for 30 minutes. The hydrogen species are capable of diffusing through the oxide and create Si-H bonds, thus passivating the silicon dangling bonds at or near the Si-SiO_2 interface [129]. Hence, X2550 and X2396 are expected to show less 1/f noise than X2388, which did not match with our observations. However, even though the effects of individual process steps have been discussed here, the

correlated effects of the steps are still unknown. Therefore, it is difficult to relate the amount of 1/f noise to the fabrication techniques.

6.5 Fitting the Observed Flicker Noise to the UNMF Model

As discussed in Chapter 1, according to the UNMF noise model, the drain-to-source current noise PSD can be expressed as [50]

$$S_{I_{DS}} = \frac{k_B T I_{DS}^2 N_t}{\lambda f WL}\left(\frac{1}{N_{inv}} \pm \alpha\mu\right)^2 \tag{6.3}$$

The observed flicker noise PSDs were curve-fitted to the UNMF noise theory to extract the trap density and screened scattering coefficient. The first and second terms in the parenthesis in (6.3) is known as number fluctuations and mobility fluctuations, respectively. The '+' sign is used for repulsive center traps, whereas the '-' sign is used for attractive center traps. Since only repulsive center traps were observed in the nMOSFETs [85], the '+' sign was used to fit the flicker noise data to the UNMF noise model. The screened scattering coefficient, α can be expressed as $\alpha = \alpha_0 + \alpha_1 \ln\left(N_{inv}\right)$, where $\alpha_1 < 0$ [72]. To fit the noise PSD curves to the UNMF noise model, the absolute error minimization technique was used. The absolute error values at the bias points were added together and differentiated with respect to α_0 and α_1 to find the optimum α_0 and α_1. The total absolute error value can be expressed as

$$e = \sum_{i=1}^{n}\left| S_{IDS_i} - c\left[\begin{array}{l} \dfrac{1}{N_{inv_i}^2} - 2\alpha_0\dfrac{1}{N_{inv_i}}\mu_i - 2\alpha_1\dfrac{1}{N_{inv_i}}\ln\left(N_{inv_i}\right)\mu_i - \alpha_0^2\mu_i^2 \\ -2\alpha_0\alpha_1\ln\left(N_{inv_i}\right)\mu_i^2 - \alpha_1^2\left\{\ln\left(N_{inv_i}\right)\right\}^2\mu_i^2 \end{array}\right] N_t I_{DS_i}^2 \right| \tag{6.4}$$

where $c = k_B T / \lambda f WL$. Differentiating 6.4 with respect to α_0 and equating to zero,

$$\alpha_0 \sum \mu^2 I_{DS}^2 + \alpha_1 \sum\left\{\ln\left(N_{inv}\right)\mu^2 I_{DS}^2\right\} = -\sum \frac{1}{N_{inv}}\mu I_{DS}^2 \tag{6.5}$$

Similarly, differentiating 6.4 with respect to α_1 and equating to zero,

$$\alpha_0 \sum \ln\left(N_{inv}\right)\mu^2 I_{DS}^2 + \alpha_1 \sum\left\{\ln\left(N_{inv}\right)^2 \mu^2 I_{DS}^2\right\} = -\sum\left\{\ln\left(N_{inv}\right)\right\}\mu I_{DS}^2 \tag{6.6}$$

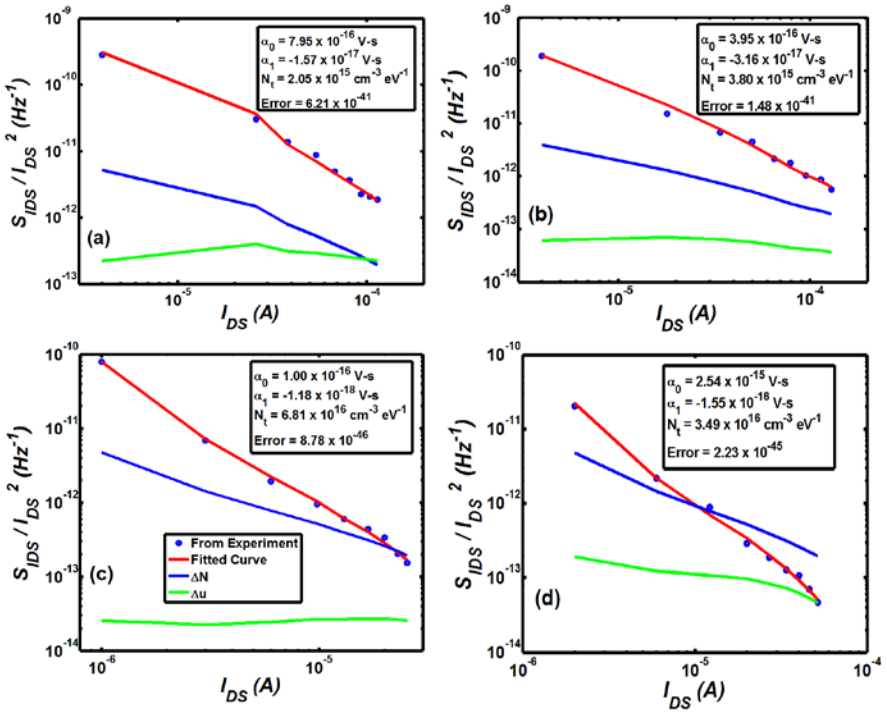

Fig. 6.10 The experimentally measured current PSD, fitted curve, number and mobility fluctuations for X2338 MOSFETs with (a) $W \times L$ = 1 × 0.5, (b) $W \times L$ = 1 × 0.8, (c) $W \times L$ = 5 × 10, and (d) $W \times L$ = 10 × 10.

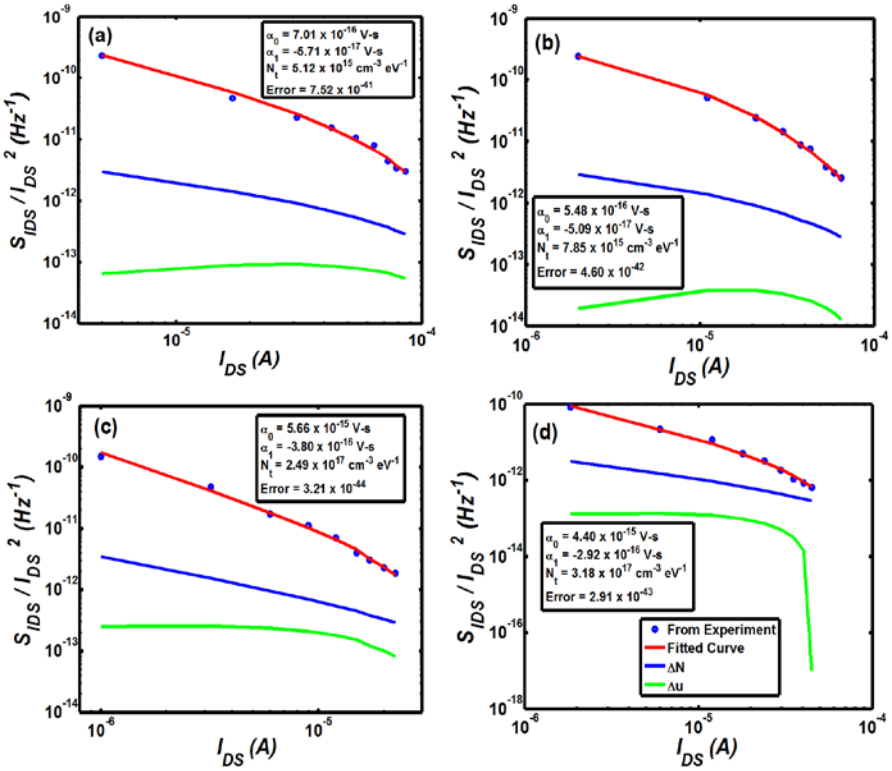

Fig. 6.11 The experimentally measured current PSD, fitted curve, number and mobility fluctuations for X2550 MOSFETs with (a) $W \times L$ = 1 × 0.5, (b) $W \times L$ = 1 × 0.7, (c) $W \times L$ = 5 × 10, and (d) $W \times L$ = 10 × 10.

Solving 6.5 and 6.6, the optimum α_0 and α_1 were found. For all the measured flicker noises, the number fluctuation at the 1st bias point dominated the mobility fluctuation by at least two orders of magnitudes. Therefore, at the first bias point, the mobility fluctuation term was neglected, and the value of N_t was calculated from that.

$$S_{I_{DS}} = c\frac{1}{N_{inv}^2}N_t I_{DS}^2 \Rightarrow N_t = \frac{S_{I_{DS}} N_{inv}^2}{cI_{DS}^2} \tag{6.7}$$

The obtained values of α_0, α_1, and N_t are listed in Table 6.1 for all categories of devices in all three wafers. The measured, curve-fitted normalized current noise PSD, number fluctuations and mobility fluctuations components for different sized devices of the three wafers are shown in Figs. 6.10-6.12.

Since MOSFETs with large gate area (>10 μm^2) showed less variability, their data exhibited a better fit. For the large gate area MOSFETs, it is clear from Figures 6.10-6.12 that the number fluctuation term dominates over the mobility fluctuations for all three wafers. The normalized number, and mobility fluctuations terms for the large area MSOFETs have been compared in Figs. 6.13 and 6.14, respectively. The normalized number fluctuations

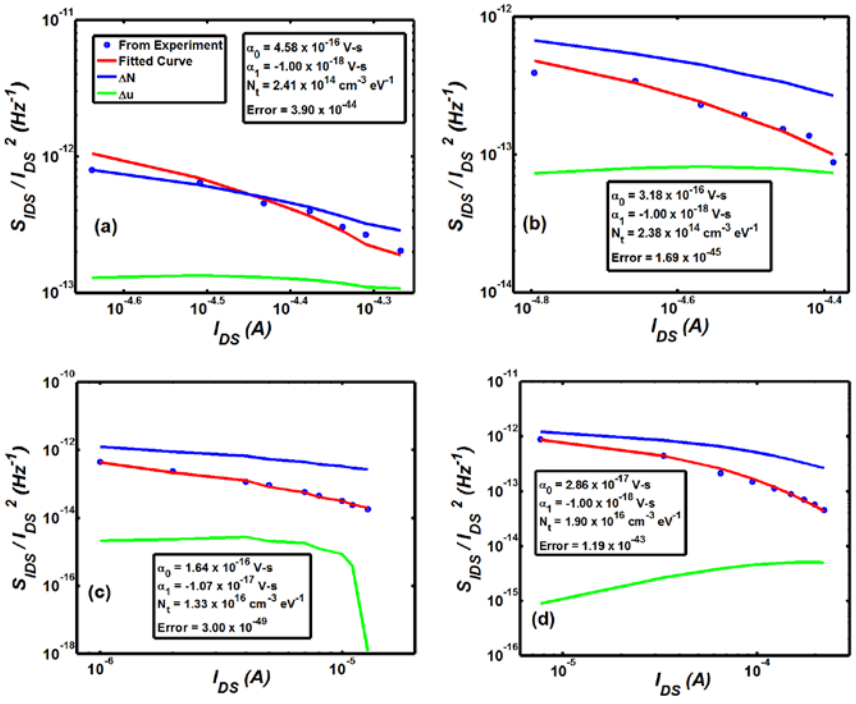

Fig. 6.12 The experimentally measured current PSD, fitted curve, number and mobility fluctuations for X2396 MOSFETs with (a) $W \times L$ = 1 × 0.5, (b) $W \times L$ = 1 × 0.7, (c) $W \times L$ = 6 × 20, and (d) $W \times L$ = 20 × 4.

exhibited by MOSFETs with W × L= 20 × 4 for X2396 are comparable with the other two wafers at some of the bias points. For all other cases, the fluctuation terms of X2396 are significantly lower than X2388 and X2396.

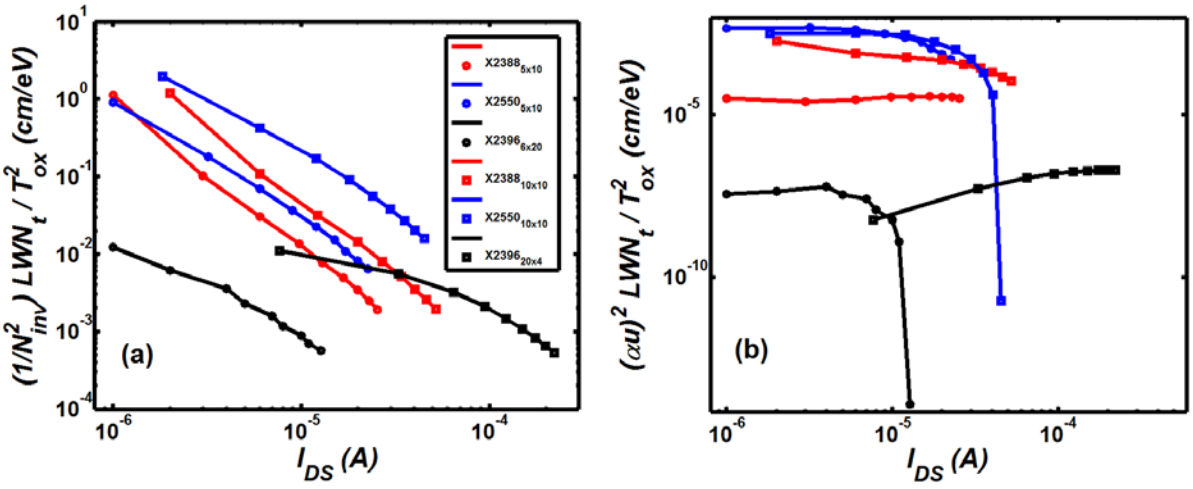

Fig. 6.13 Normalized (a) number fluctuations and (b) mobility fluctuations as function of I_{DS} exhibited by MOSFETs with $W \times L = 5 \times 10$ and 10×10 of X2388 and X2550, and $W \times L = 20 \times 4$ and 6×20 for X2396.

Table 6.1– Optimum values of α_0, α_1 and N_t obtained from curve fitting

Wafer	Dimension ($W \times L$)	N_t ($cm^{-3}ev^{-1}$)	α_0 (V-s)	α_1 (V-s)	error
X2388	5 × 10	6.81×10^{16}	1.00×10^{-16}	-1.18×10^{-18}	8.78×10^{-46}
	10 × 10	3.49×10^{16}	2.54×10^{-15}	-1.55×10^{-16}	2.23×10^{-45}
	1 × 0.5	2.05×10^{15}	7.95×10^{-16}	-1.57×10^{-17}	6.21×10^{-41}
	1 × 0.8	3.80×10^{15}	3.95×10^{-16}	-3.16×10^{-17}	1.48×10^{-41}
X2550	5 × 10	2.49×10^{17}	5.66×10^{-15}	-3.80×10^{-16}	3.21×10^{-44}
	10 × 10	3.18×10^{17}	4.40×10^{-15}	-2.92×10^{-16}	2.91×10^{-43}
	1 × 0.5	5.12×10^{15}	7.01×10^{-16}	-5.71×10^{-17}	7.52×10^{-41}
	1 × 0.7	7.85×10^{15}	5.48×10^{-16}	-5.09×10^{-17}	4.60×10^{-42}
X2396	6 × 20	1.33×10^{16}	1.64×10^{-16}	-1.07×10^{-17}	3.00×10^{-49}
	20 × 4	1.90×10^{16}	2.86×10^{-17}	-1.00×10^{-18}	1.19×10^{-43}
	1 × 0.5	2.41×10^{14}	4.58×10^{-16}	-1.00×10^{-18}	3.90×10^{-44}
	1 × 0.7	2.38×10^{14}	3.18×10^{-16}	-1.00×10^{-18}	1.69×10^{-45}

In summary, flicker noise measurements were taken on nMOSFETs of three different technologies. The noise PSDs of differently sized MOSFETs were compared. Only devices with a gate area >10 μm^2 exhibited consistent and comparable noise data. Wafer X2550 showed the maximum 1/f noise, while X2396 was the wafer with the lowest amount of noise. Individual correlations of the noise data with some of the fabrication steps were investigated. The experimentally obtained noise data curves were fit to the UNMF noise model to extract the trap density and screened scattering coefficients. The number fluctuation term dominated over the fluctuations in

mobility in most of the cases. The normalized number and mobility fluctuation terms obtained from three wafers were also compared. In most of the cases, both the normalized number and mobility fluctuation terms of X2388 and X2550 dominated over those from X2396.

Chapter 7 Conclusion

This research concentrates on measuring and analyzing RTS in pMOSFETs to study the associated hole defects located at or near the Si-SiO_2 interface. RTS experiments were done at room temperature as well as lower temperatures down to 165 K. The variable temperature RTS data allowed extraction of trap characteristic parameters such as capture activation energy, change in enthalpy and entropy and relaxation energy. The calculated trap energy parameters were compared to the already published trap parameters found using other techniques. This helped to investigate the physical structures and behaviors of the responsible defects. From the pattern of the average time spent at RTS upper and lower levels as a function of gate bias, traps were identified to be attractive or repulsive centers. Both Coulombic attractive and repulsive center defects were found to cause the switching in the MOSFET drain voltage. The attractive center traps were identified as a pair of dissociated three-coordinated silicon atoms (commonly known as D-III-Si), and the repulsive center trap showed similar trap parameters to a pair of under coordinated silicon and over coordinated oxygen atom (III-O/III-Si, also known as puckered/back-projected oxygen vacancy defect). Mostly nMOSFETs are used in the modern analog and high-speed circuits because of higher drive current and electron mobility. This might be one of the reasons for which hole defects responsible for RTS in pMOSFETs have not gained much attention compared to the electron defects in nMOSFETs. However, pMOSFETs are also a major part in digital CMOS applications where low power consumption is one of the primary performance criteria. Most of the research works concentrating on hole defects limited their study to the physical location of the trap from the oxide-semiconductor interface, and along the channel. This is the first work to investigate the hole trap characteristics in such detail, and to suggest physical structures for the traps that might lead to RTS.

To study the hot carrier effects on RTS and trap parameters as well as MOSFET DC parameters such as threshold voltage and transconductance, channel hot carrier stress was applied to several submicron pMOSFETs. RTS measurements were taken on unstressed and stressed MOSFETs to observe the impact of hot carriers. Both pre-stress and post-stress RTS were observed in the experiments. Capture cross-sections and trap energy level with respect to the SiO_2 valence band edge were found to be within similar ranges as the process-induced traps observed before. Therefore, the pre-stress as well as post-stress defects responsible for RTS were thought to have the same physical structure as the previously observed traps: the attractive center being a pair of D-III-Si defects, and the repulsive center being the puckered/back-projected oxygen vacancy defect. Breakage of Si-Si bond in a neutral

oxygen vacancy due to high vertical electric field is suggested to be the reason behind the creation of stress-induced traps. Two attractive center traps were observed to be appearing and disappearing randomly with stress. Movement of channel hot carrier stress-released hydrogen atoms within SiO_2 and their reactions with oxide defects have been proposed as the mechanism behind the volatile nature of the traps. Hydrogen atoms remain in bound form at the Si-SiO_2 interface or with the defects residing in the oxide. After applying stress, the channel hot carriers strike at the Si-SiO_2 interface releasing hydrogen atoms. The released hydrogen can drift through oxide towards the gate where it can react with an oxide trap to passivate the defect. Upon further stress, another hydrogen atom may get released from the Si-SiO_2 interface and react with the already passivated defect. As a result the defect restores its original structure releasing a hydrogen molecule. The barrier energies of the reactions are in the range of 0.4-0.5 eV, which implies that these reactions can easily take place at room temperature.

In order to find out more properties of the stress-induced traps, variable temperature RTS measurements were taken. The capture cross-sections, trap energy levels with respect to the SiO_2 valence band edge, capture activation energies and relaxation energies of the stress-induced traps were found to be within the similar ranges as the process-induced traps observed before. This observation ensured that application of stress only affected the trap generation, passivation or reactivation phenomena, not the trap characteristic parameters. This is the first work that explains the creation of stress-induced E′ centers in pMOSFETs that are responsible for RTS. This research is also the first work that reports the observation of volatile RTS due to both process-induced and stress-induced traps, and presents a possible mechanism behind the trap volatility.

Flicker noise PSDs on nMOSFETs of three wafers with different gate oxide growth conditions have been compared. The voltage noise PSDs were normalized with respect to channel length, width and oxide thickness before comparison. As a function of drain-to-source current, the normalized current PSD of all MOSFETs showed a similar trend as $(g_m/I_{DS})^2$. This behavior indicated that the 1/f noise in the MOSFETs followed the number fluctuations theory. Correlations of the observed flicker noise with the individual gate oxide growth conditions were studied. The normalized current PSDs with respect to the drain-to-source current were curve-fitted to the Unified Number and Mobility Fluctuations noise theory to extract the trap density and the screened scattering coefficient. This research might be very useful for developing optimum gate oxide growth conditions for passivating the oxide defects that might lead to RTS and flicker noise.

Although this research provides detailed analyses on hole traps responsible for RTS in pMOSFETs and explains the trap creation, deactivation and reactivation mechanism due to stress, some other aspects of hole trapping and de-trapping mechanism are still unknown. Hence, opportunities for further research works related to this topic are available. This work concentrated characterization of hole defects only in SiO_2. Similar analysis procedures can be used to investigate the properties of hole defects present in different high-k dielectrics such as HfO_2 and ZrO_2. Effects of channel hot carrier stress were investigated in terms of trap generation and passivation/reactivation and change in trap characteristic parameters. However, fixed charges and interface states will also be created due to stress. These charge states will cause additional scattering altering the amount of screening caused by the channel holes. Hence, the screened scattering coefficient will be affected due to stress. These effects have not been considered while characterizing the oxide defects in this research. The modeling of the screened scattering coefficient with stress conditions and intervals might be another area with potential research opportunities that needs special attention.

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