Study of Electromigration failure mechanism in micro solder joint

By

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Dissertation

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Abstract

The miniaturizing trend for advanced electronic devices has motivated the microelectronic industries to pursue device integration and packaging technology based on the micro-bump solder joint. This type of the joint enables devices with far higher interconnect density and miniaturized form factors which are ideal for mobile applications. The focus of this research is to conduct comprehensive investigation on the electromigration (EM) reliability of micro solder joint. For that purpose, a series of EM tests on micro solder joints under direct current (DC) load was conducted with variation in the contributing factors to EM failure, including solder joint arrangement (change of interfacial layer addition), Cu pillar geometry (elliptical vs. cylindrical), EM test temperature, and current density. For this research, a customized EM test system with an oil-bath was developed to enable effective joule heat dissipation and maintenance of temperature uniformity and stability for the duration of EM testing. Our studies on EM failure kinetics and microstructural mechanism have produced a few important findings: 1) failure rate does not follow a single activation energy model, and it is far more sensitive to test temperature than the predicted by a conventional model. This is determined to be resulted by a limited amount of the solder material that is under two competing processes during EM test, a formation of intermetallic compound (IMC) and EM damage by voiding. The failure mode changes by change of dominant process among these two. Our extensive failure analysis on EM tested samples at different temperatures revealed that EM void damage due to EM of Sn is the dominant factor for the samples tested at low range of EM testing. On the other hand, IMC formation rate is the process that controls the failure kinetics of the joints tested at high temperature range of EM testing. 2) It is found that failure can happen even if the solder joint fully converted to IMC even though IMC joints are immune against EM damage. The results showed that failure location shifted to the interface of Cu interconnect and IMC joint. Unbalanced interdiffusion of Cu and Sn through IMC joint is the source of discontinuity formation, also known as the Kirkendall effect. 3) The investigation of micro solder joints isolated from Cu pillar by a Ni interfacial layer showed that the EM failure can be suppressed by the back-stress effect. Very thin thickness of micro solder joint along with low aspect ratio (thickness to length) makes the back-stress effect to be sufficient to prevent EM damage. The back-stress effect is found to be very sensitive to test temperature, and

the back-stress effect diminishes at high temperature as it is outcompeted by EM rate of Sn. 4) Our study on fine pitched solder joint with cylindrical joint geometry leads to a finding of a unique failure mechanism caused by a formation of extended solid solution. The EM testing at extremely high current density causes interdiffusion of Cu and Sn to continue even after full conversion of the solder joint to the IMC. In this case, we observed that grain boundaries in Cu interconnects are the main routes of interdiffusion and responsible for the unique failure mechanism. Finally, our findings suggest the complexity of failure mechanism in this type of solder joint compared to conventional solder joints like BGA (ball grid array) or flip-chip joints. Small amount of solder material along with low aspect ratio of the joint makes the failure kinetics and mechanism to be very sensitive to test temperature and joint geometry. Our findings also suggest that failure mechanism of micro solder joint under EM cannot be understood by considering a single metallurgical process but demands considerations on various contributing factors.

Dedication

To my lovely wife for her unconditional support, endless love, limitless understanding, and encouragement for the completion of this stage of my life. Also, to my mother and soul of my brother and father who had great impacts and inspirations on my life.

Acknowledgments

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Chapter 1: Research Description

1-1- Proposed Research and Objectives

This research aims to investigate the mechanism of electromigration (EM) failure in solder based interconnects. The study was conducted on a solder joint with an extremely thin thickness of solder, that is called micro solder joint, with an aim of better understanding the EM failure mechanism in micro solder joint and also to determine effect of various contributing factors including joint geometry, interfacial layer addition, and EM test conditions.

Specific objectives of this study are 1) a better understanding of the mechanism and kinetics of EM failure under varying load conditions, 2) comparing EM lifetime of different solder geometry and interfacial addition, and 3) identifying new failure mechanisms, if any, that may be hidden in EM under DC condition. For that purpose, the experiments were designed to conduct a series of comparative EM tests on representative solder interconnects under direct current (DC) load in accelerated EM test conditions, with variation in the contributing factors to EM failure. The following parameters that may have contribution to EM failure, both intrinsic and extrinsic, were considered in the design of experiment: Solder joint geometry by changing Cu pillar geometry (elliptical vs. cylindrical), addition of interfacial layer to the solder joint and its arrangement at the interfaces of the solder joint, and EM test conditions such as temperature and current density. The data and understanding resulting from this project will provide key answers to the contributing factors that may change EM failure mechanism in this particular solder joint i.e., micro solder joint. Moreover, the kinetics study of failure can yield a model that provides enhanced predictability of device reliability. This kinetics model and understanding of the failure mechanism will be greatly helpful for engineers to conduct EM reliability assessments with greater confidence.

1-2- Research summary

As mentioned above, sets of experiments were designed and performed to explore systematically failure kinetics and mechanism in the micro solder joint. The first considered aspect is the measurement of MTTF of the sample tested under accelerated (EM) condition. MTTF data can be used for constructing a failure kinetics model. Based on Black's kinetics model[1], MTTF

defined as $MTTF \approx j^{-n} \exp\left(\frac{E}{kT}\right)$ which j is the current density, n is the current density exponent, E is the thermal activation energy, T is the temperature and k is the Boltzmann constant. To calculate the thermal activation energy (E) and current density exponent (n), different testing temperature and current density were selected for performing EM tests. At the constant current density, EM tests were conducted at different temperatures to calculate the thermal activation energy (E), $MTTF \sim \exp\left(\frac{E}{kT}\right)$. Also, different current densities applied to the samples at a constant temperature to calculate the current density exponent (n), $MTTF \sim j^{-n}$. The EM test conditions used in this study, temperatures and current densities, are listed and explained in the experimental method chapter. Understanding microstructural change and identifying failure mode of the solder joint under EM test is another purpose of this research. To this end, the failure of micro solder joints was tracked during experiments utilizing in situ joint's electrical resistance measurement, and also extensive failure analysis was performed on the EM tested samples with an aim of understanding the failure mode and microstructure change.

Chapter 2: Literature Review

2-1- What is Electromigration?

Generally, atomic migration can be caused by various forces in solid state phase. The types of migration include (1) chemical diffusion due to concentration gradients that is called chemical diffusion, (2) atomic migration caused by temperature gradients that is called thermomigration, (3) atomic migration caused by mechanical stress that is called stress migration, and (4) atomic migration caused by an electrical field that is called electromigration (EM)[2]. The subject of this research is the EM and failure caused by it.

Atoms in n the conductor are subjected to two forces. The first force is an electrostatic force field that directs the atoms to the direction of electric field. This force can safely be ignored in most cases because the positive metal ions are shielded to some extent by the negative electrons in the conductor. The second force is electron wind force (F_{wind}) which is generated by the momentum transfer between conduction electrons and metal ions in the crystal lattice. Indeed, the primary cause of EM is this electron wind force in the direction of the current flow, which its name has analogy as a breeze or wind blowing through the leaves of a tree [2]. Figure 2-1 shows two forces exposed to a metal ion due to current flowing in the conductor.

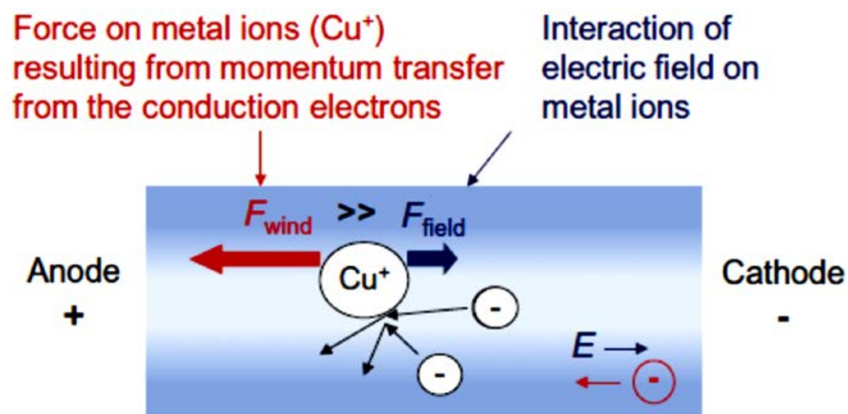


Figure 2-1. Two forces impose on metal ions (Cu) in the conductor. EM happens in the direction where the result of the dominant force is, figure is taken from reference c.

The resulting force in the direction of the electron wind transmits kinetics energy to the metal ions. When this transmitted energy exceeds a given trigger, which is called activation energy Ea,

diffusion starts and make atoms to move in direction of electron flow. This directional diffusion transports material in the direction of the electron motion that is from the cathode (-) to the anode (+)[2].

According to the free electron model of conductivity of metals, where the lattice is perfect, the conduction electrons are unconstrained and free to move in the metal. The only exception that limits the movement of the electrons is the process of scattering due to their interactions with phonon vibration. This scattering is responsible for the non-zero electrical resistance and consequently heat generation which is called Joule heating. Nevertheless, in low electric current density, the amount of scattering or the momentum exchange between the electrons and atoms is not sufficient to displace atoms, resulting in no influence on atomic diffusion. However, when the current density is high, above 10^4 A/cm^2 for most metals scattering by electrons enhances atomic displacement in the direction of electron flow. This atomic displacement under the influence of electric field (mainly a high-density electric current) is called EM. When a diffusing atom stays at the activated state, which is out of its equilibrium position, it possesses a very large scattering cross-section (Figure 2-2).

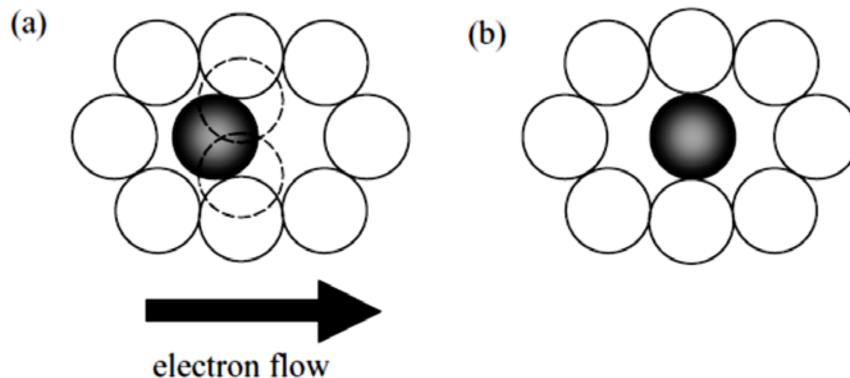


Figure 2-2. Schematic diagram of EM of a diffusing atom (a) before, and (b) at the activated state, where it possesses a very large scattering cross-section, figure is taken from reference [3].

EM will not occur in an ordinary household extension cord that conducts electricity because the electric current density in the cord is low, about 10^2 A/cm^2, and also the temperature is not high enough for atomic diffusion in copper[3].

The mass transport due to EM is the result of a combination of thermal and electrical effects

on diffusing atoms. For example, when a conducting line is kept at a very low temperature (e.g., liquid nitrogen temperature), EM cannot occur because atomic mobility is not enough to activate diffusion of atoms, even though there is a sufficient level of driving force for migration. High current density and elevated temperature are the essential factors for active EM, but EM damage rate like voiding is determined by the flux divergence. Also, if there is no flux divergence throughout the conductor, equilibrium will be everywhere, and EM-induced damage such as voiding and extrusion cannot happen because of the prevailing equilibrium in the entire of a conductor. Regarding this fact, if we have continuous atomic or vacancy flux in the interconnect, the cathode can supply vacancies and the anode can accept them continuously. In other words, mass flux divergence is necessary to have EM damage in an interconnect, and uniform fluxes of atoms and vacancies throughout a conductor will not cause EM damage[3].

Generally, if one could assume homogeneous material transport the entire of wiring, there would be no change throughout the interconnect. Meaning that the same amount of replenished material would be removed throughout the interconnect. Practically, numerous required features in an IC chip causes inhomogeneities through its wiring. As a result, the atomic flux will be inhomogeneous through the chip wiring. Some of the features which resulting inhomogeneities in chip designs are[2]:

- ends of interconnects,
- changes in the direction of interconnects,
- change of layers,
- change of interconnect cross-sections that lead to varying current densities,
- damages created in manufacturing or varying temperature distributions, and/or
- mechanical tension gradients
- The interface of different materials such as solder joints and wire bonds

Mass depletion or accumulation in the vicinity of such inhomogeneities can happen due to divergences in the diffusional flow. Such depletions and accumulations will gradually lead to the formation of voids (can create open circuit damage) or hillocks that can cause short circuit damage to the interconnect. Figure 2-3 shows typical EM induced damage in the interconnects. Whiskering is another consequence of EM and appears as the spontaneous growth of tiny, filiform hairs from a metallic surface (see Figure 2-3 right). Whiskers formation can cause short circuits and arc in

electronic circuits[2].

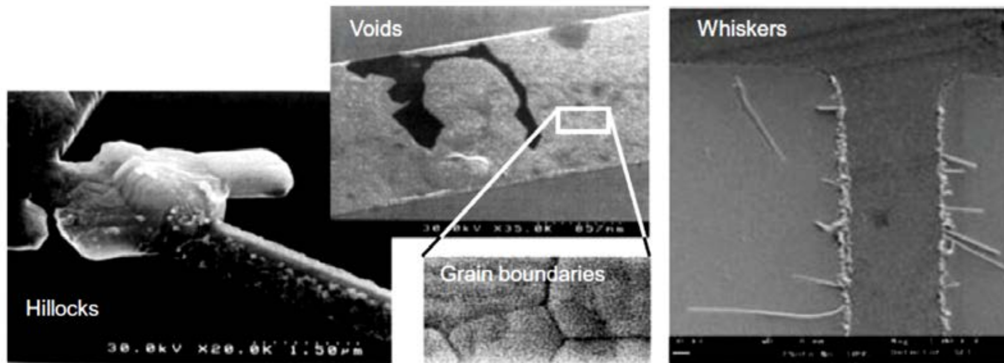


Figure 2-3. Hillock and void formations in wires due to EM; Whisker growth on a conductor is shown on the right, figure is taken from reference [2].

Based on theoretical stipulation proposed by Huntington and Grone, the electrical force acting on a diffusing atom (ion) is taken to be [1]:

$$F_{EM} = Z^{*}eE = (Z^{*}_{el} + Z^{*}_{wd})\, eE$$

where e is the charge of an electron and E is the electric field (E = ρj, where ρ is the resistivity and j is the current density) and Z^{*} is the effective charge number of EM. Z^{*}_{el} can be regarded as the nominal valence of the diffusing ion in the metal when the dynamic screening effect is ignored, and it is responsible for the field effect and $Z^{*}_{el}eE$ is called the direct force. Z^{*}_{wd} is an assumed effective charge number representing the momentum exchange effect between electrons and the diffusing ion, and $Z^{*}_{wd}eE$ is called the electron wind force. For a good conductor, effective charge number is generally found to be of the order of 10, so the electron wind force is much greater than the direct force for EM in metals. Hence, EM-induced atomic flux is in the same direction as electrons flow[3]. There are two atomic fluxes in the metals under EM enhanced diffusion. Atomic flux due to chemical diffusion (J_i^{Chem}) and ccurrent induced atomic flux (J_i^{EM}), which the following equations describe these atomic fluxes[4]:

$$J_i^{Chem} = -D_i \frac{\partial C_i}{\partial x}$$

$$J_i^{EM} = C_i \frac{D_i}{kT} Z_i^{*} e \rho_i j$$

where D_i is diffusivity coefficient of atom i, C is chemical concentration and T is absolute

temperature. These atomic fluxes cause the atom movement in direction of electrons flow. The schematic of this atom migration is depicted in Figure 2-4.

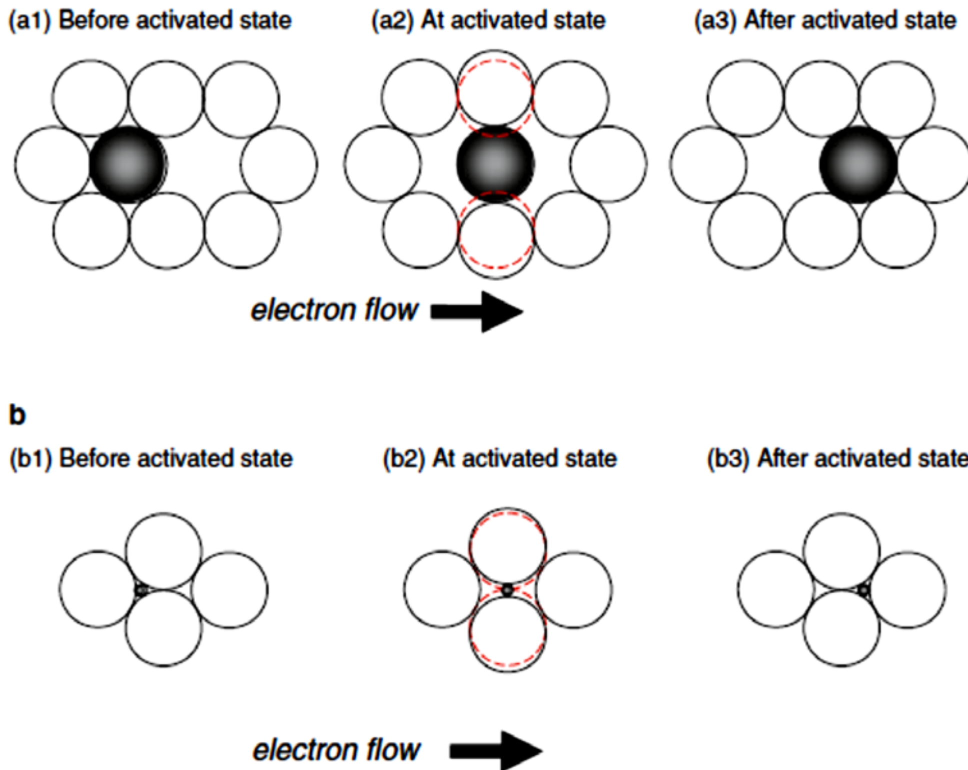


Figure 2-4. Schematic diagram of EM for atoms diffuse by (a) vacancy mechanism, and (b) interstitial mechanism, figure is taken from reference [5].

In summary, EM involves both atomic and electron fluxes due to combination of high current density and heat. EM occurs in the conductor when subjected to high density current at elevated temperatures, but formation of EM-induced damage requires the presence of flux divergence in the interconnect[3].

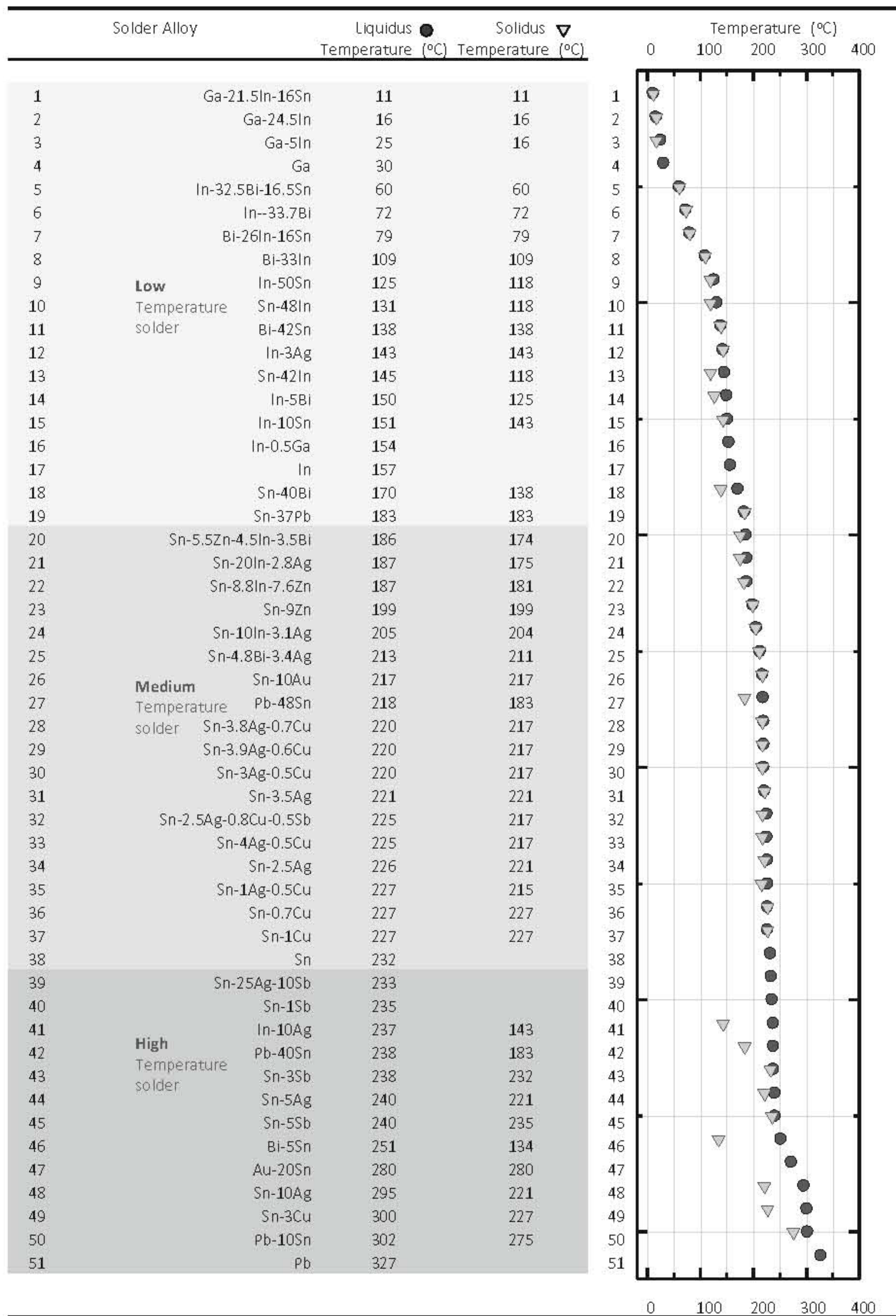
2-2- Solder joint alloys

Having a stable system in the context of electronic devices involves the stability of layer structure that components bonded together. Strong bonding between the two material sets can have different consequences: it may be stable, or it may cause a shift from one weak link to another

weak interface. Several types of interconnections exist in electronic systems including the electronic plug-in cord, pin connectors, solder joints connecting the printed circuit board (PCB) and modules, solder joints connecting modules to a component, wire bond interconnects, or solder bumps (on a flip-chip joint) from the component substrate to the Si die, and microbumps that connecting a Si die to another stacked Si die. Functionality and configuration within electronic systems for each type of interconnection can be different[6]. Solder is one of the most popular interconnection methods that has been used to join copper pipes for house plumbing and to join copper wires/pads in every electrical product. Solder joints are ubiquitous and the essential process in solder joining is the chemical reaction between copper and tin. This reaction forms intermetallic compounds that cause a strong metallic bonding. Copper–tin (Cu-Sn) metallurgical binary system is as important as the iron-carbon (Fe-C) binary system and historic bronze (Cu-Sn alloy) age suggested because of its vast impact on human civilization. Typical solder alloy used to join copper parts is lead (Pb) and tin; however, due to environmental concern of lead toxicity, the Pb-free solder in plumbing is already common, and Pb-free solders are being introduced into electronic and electrical products[3].

Currently, Sn-based solder alloys have replaced Pb-bearing solders in most applications in the whole electronics industry since 2006. Regarding this, replacing the Pb with Sn was not sufficient for solder joints and it required alloy elements such as Cu and Ag to meet requirements [6]–[16]. Nearly all the eutectic Pb-free solders are Sn-based and the eutectic alloys consisting of Sn and noble metals such as Au, Ag, and Cu. Also, other alloying elements to Sn such as Bi, In, Zn, Sb, and Ge have been considered. Table 2-1 listed the binary Pb-free solder systems with their eutectic points that compared with Sn-Pb eutectic. According to this table, there is a large temperature range between the eutectic temperatures of Sn-Zn (198.5^{o}C) and Sn-Bi (139°C), for which no known Pb-free solder system exists. The closest melting point to that of eutectic Sn-Pb among all the eutectic Pb-free solders is the eutectic Sn-Zn that has received much attention in Japan, especially. Zinc (Zn) can be a good candidate for the eutectic alloy with Sn because it is cheap and readily available, but it quickly forms a stable oxide[6].

Table 2-1. Selected solder alloy compositions and liquidus/solidus temperature, table is taken from reference [6].



	Category	Solder Alloy	Liquidus Temperature (°C) ●	Solidus Temperature (°C) ▽
1		Ga-21.5In-16Sn	11	11
2		Ga-24.5In	16	16
3		Ga-5In	25	16
4		Ga	30	
5		In-32.5Bi-16.5Sn	60	60
6		In--33.7Bi	72	72
7		Bi-26In-16Sn	79	79
8		Bi-33In	109	109
9	Low Temperature solder	In-50Sn	125	118
10		Sn-48In	131	118
11		Bi-42Sn	138	138
12		In-3Ag	143	143
13		Sn-42In	145	118
14		In-5Bi	150	125
15		In-10Sn	151	143
16		In-0.5Ga	154	
17		In	157	
18		Sn-40Bi	170	138
19		Sn-37Pb	183	183
20		Sn-5.5Zn-4.5In-3.5Bi	186	174
21		Sn-20In-2.8Ag	187	175
22		Sn-8.8In-7.6Zn	187	181
23		Sn-9Zn	199	199
24		Sn-10In-3.1Ag	205	204
25		Sn-4.8Bi-3.4Ag	213	211
26	Medium Temperature solder	Sn-10Au	217	217
27		Pb-48Sn	218	183
28		Sn-3.8Ag-0.7Cu	220	217
29		Sn-3.9Ag-0.6Cu	220	217
30		Sn-3Ag-0.5Cu	220	217
31		Sn-3.5Ag	221	221
32		Sn-2.5Ag-0.8Cu-0.5Sb	225	217
33		Sn-4Ag-0.5Cu	225	217
34		Sn-2.5Ag	226	221
35		Sn-1Ag-0.5Cu	227	215
36		Sn-0.7Cu	227	227
37		Sn-1Cu	227	227
38		Sn	232	
39		Sn-25Ag-10Sb	233	
40		Sn-1Sb	235	
41		In-10Ag	237	143
42	High Temperature solder	Pb-40Sn	238	183
43		Sn-3Sb	238	232
44		Sn-5Ag	240	221
45		Sn-5Sb	240	235
46		Bi-5Sn	251	134
47		Au-20Sn	280	280
48		Sn-10Ag	295	221
49		Sn-3Cu	300	227
50		Pb-10Sn	302	275
51		Pb	327	

Such stable oxide shows very poor wetting behavior, resulting in excessive drossing during wave soldering. Hence, a forming gas ambient is required to shield the molten alloy during soldering. In terms of wetting properties, Bismuth (Bi) containing alloys show very good behavior. However, the availability of Bi is a practical issue because the primary source of Bi is a by-product in Pb refining. Then, by restricting the use of Pb, much less Bi will be available. The United Nations Environment Program has identified antimony (Sb) as a harmful element. Germanium (Ge) is used only as a minor alloying element of multicomponent solders due to its reactivity. Indium (In) is too scarce and too expensive to be considered for broad applications, besides it forms oxides very easily[6].

When the surface and interfacial energies are considered, unlike Sn-Pb, which has low wetting energy, the surface energies of these Pb-free solders are higher than eutectic Sn-Pb. This leads to their wetting angle on Cu to be usually larger, about 35 to 40°. The microstructure of eutectic Sn-Pb has no IMC but for Pb-free eutectic solders, they are a mixture of Sn and IMCs because of the alloys typically containing Ag and/or Cu. Metallic Sn has anisotropic mechanical and electrical properties due to its body-centered tetragonal lattice structure. As a result, the mechanical and electrical properties of these Pb-free eutectic solders is found to be anisotropic. Thus, the dispersion of the IMC may lead to the formation of inhomogeneous microstructures, particularly in the case of Ag_3Sn that may grow in preferred crystallographic directions of Sn. On the cross-sectional image of a eutectic Sn-Ag-Cu solder joint which is prepared by deep etching, a plate-like Ag_3Sn can be seen as illustrated in Figure 2-6. Formation of such Ag_3Sn plate-like in a high-stress area, such as the corner of a solder bump, can be the cracks initiation place and can propagate along the interface between the Ag_3Sn and solder. The interface crack propagation leads to fracture failure as observed in Figure 2-6. If the Ag concentration in the solder is less than 3%, the formation of such large plate-like IMC can be avoided[3].

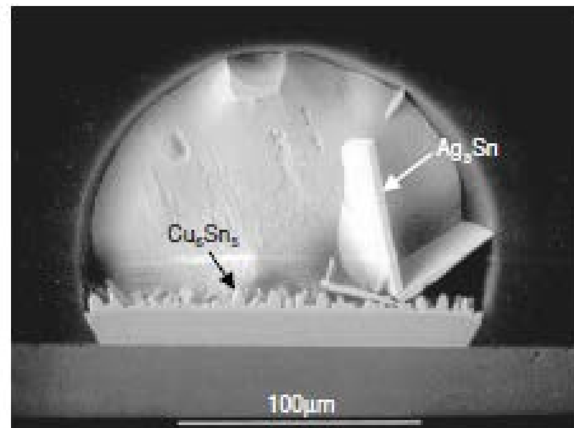


Figure 2-5. SEM image of Ag3Sn platelet in Sn-Ag-Cu solder joint, figure is taken from reference [3].

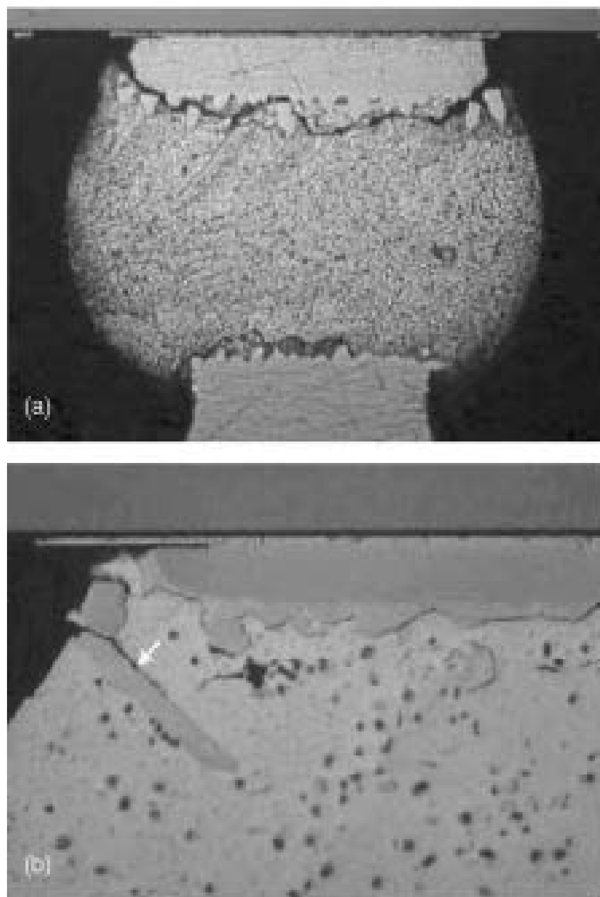


Figure 2-6. SEM image of crack at the corner of Sn-Ag-Cu solder joint, figure is taken from reference [3].

Among the Pb-free solders, the most promising Pb-free solders that can replace the eutectic Sn-Pb are the eutectic Sn-Ag-Cu (SAC), eutectic Sn-Ag, and eutectic Sn-Cu. These Sn-based solders have a very high concentration of Sn, e.g., the eutectic Sn-Cu has 99.3 wt% Sn and the eutectic Sn-Ag-Cu has about 95 to 96 wt% of Sn. Hence, the solder reaction between the Pb-free and Cu is mostly the Cu-Sn reaction[3].

There are a number of SAC alloy compositions in current use, and many more have been developed in the past. While SAC solder is quickly becoming popular in electronic packaging, the technology is rapidly changing to new directions. One of the main thrusts behind such change is the further scaling of existing packaging structures, such as flip-chip and BGA (Ball Grid Array), while another is the emergence of 3D packaging where the use of exceptionally miniaturized solder interconnects is essential. As the solder amount is small compared to joining substrates in such cases, better control of the IMC growth is necessary. For example, the joint with fully converted to IMC is the result of excessive reaction with Cu in microbumps, and it can make the joint to be prone to failure by shock or fatigue. In order to resolve such concern, the SAC alloy systems with microalloying have been developed. SAC alloys containing a minute amount of Ni, Co, Mn, or Ge are now developed as ball materials for BGA applications while microalloying with Pd and Fe are also under investigation[8], [17]–[25]. The beneficial effects of microalloying are becoming well demonstrated, but the links between microstructure and reliability are not fully understood. Further, microalloying may not provide enough protection against reliability issues stemming from excessive IMC growth. When solder alloy without increasing the brittleness is required, one approach can be alloys contain higher Cu to reduce reactivity with Cu itself. In the case of 3D packaging technology, need for new SAC alloys may be related to the process itself where lower amount of the solder alloys is needed to join interconnects. Trapping cavities is one of critical and common defects in the solder joint where a small volume of solder reacts with a large joint surface. Since flux is the source of cavity formation, it can be prevented by the use of fluxless soldering or a flux that does not produce cavities. But, it will inevitably require different SAC solder alloys because existing alloys' compatibility with a fluxless process or new fluxes needs to improve[6], [26]. The efforts to develop new alloy systems thus are progressing. Some of these efforts are also motivated to tune the mechanical strength (to lower it in many cases) of SAC alloys and their reliability [6].

On top of all concerns, the lack of suitable alloys for high-temperature applications is one of the most serious challenges to removing the Pb–Sn alloy system from the solder materials. For instance, many of the electronics used for automobile applications are required to withstand at operating temperatures near 150 °C[27]. For such applications, solder alloys with melting temperatures close to 300 °C or higher are essential. Previously, 95Pb–5Sn alloy, which has a reasonably high melting temperature as well as mechanical and chemical stability, was used. There are no suitable replacement Pb-free solder alloys of 95Pb-5Sn. Sn–Au eutectic solder is qualified for such application, but it is impractical because of its excessive cost [28]. Alloys currently are considered and being developed for high temperature applications include Sn–Sb and high Ag–Sn, but their properties are still not comparable to 95Pb–5Sn [29]. Therefore, solder alloy development for the high temperature application is one area that needs many developments[6].

2-3- Electromigration in the solder joints

There have been concerns on the reliability of solder joint among the microelectronic packaging industries for a long time. An example of such concern can be found from the low cycle fatigue of tin-lead (Sn-Pb) solder joints in flip-chip technology. The fatigue failure occurs by the cyclic thermal stress between a Si chip and its substrate. At present, the risk of fatigue failure is reduced by the application of underfill material (epoxy) between the chip and its substrate. Replacing Sn-Pb solders with Pb-free solders has resulted in new reliability issues, mostly due to Pb-free alloys having a very high concentration of Sn. With high concentration of Sn, the solder becomes too reactive with Cu, resulting in excessive growth Cu-Sn IMCs and thus making the joint to be prone to mechanical failure by fatigue and shock. It also increases the susceptibility of solder joint to EM induced failures. It is especially concerned in consumer electronics where demand for devices with greater functionality and performance has intensified. Such devices make the solder joint to carry higher current density. A typical solder joint has two interfaces, Cu UBM (under bump metal) /solder and Cu/interconnect, and these interfaces are the locations where failures tend to occur. As previously mentioned, the metallic bonding of the solder joint with interconnect requires the formation of IMCs at the interfaces, and then the interfacial IMCs will

greatly affect the properties and reliability of the joint. EM failure occurs typically at the cathode interfaces[3]. Since flux divergence is a necessary condition for the development of EM failure, the triple points of grain boundaries and/or interfaces between dissimilar materials are the most common failure locations in electronic packaging. As is shown schematically in Figure 2-7, a solder is with two interfaces. one at the cathode and one at the anode, and they become the common failure sites. Under EM, the vacancies accumulate at cathode interface due to Sn atoms migrating toward the anode. This makes voids to form at the cathode interface. The interfaces become the dominant failure site because they are place of the maximum flux divergence[3].

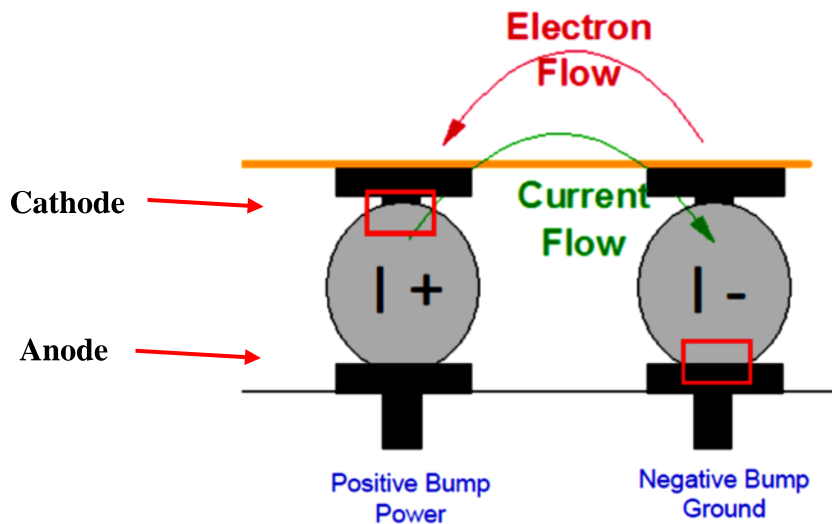


Figure 2-7. Schematic of solder joint under current flowing, figure is taken from reference [30].

It is known that Sn is more prone to EM. In case of Al or Cu interconnects, EM failure is known to occur at current densities execeeding10^5 to 10^6 A/cm^2. In case of solder joint, it can fail at 10^3 to 10^4 A/cm^2, which is far lower than those for Al or Cu. This exceptional susceptibility of Sn to EM failure is rooted to the fact that the diffusivity of Sn is far higher than Al or Cu. The melting temperature of Sn is ~310°C and therefore the bulk diffusion occurs even at room temperatures. This is why EM in solder joints can be a serious reliability concern[3].

In understanding EM failure in solder joint, it is important to consider the effect of the joint geometry. Unlike in Al or Cu thin film interconnects, the EM failure in solder joint is affected greatly by the current crowding. The current crowding occurs because an electric current takes the

conduction path with the lowest resistance. Electrons become concentrated at the entrance of the solder bump as current direction abruptly changes at the corner. This leads to higher current density in the solder bump near the entrance point. It can be as high as one order of magnitude higher than the average current density in the middle of the bump. The entrance of the solder joint is the most probable place where EM failure initiates because of the current crowding in addition to significant level of flux divergence. Figure 2-8 depicts the cross-section of a solder joint with pancake-type void formation at the cathode interface. As the initial void forms at the entrance of electrons in the joint interface, the point of current crowing will be displaced to the front of the void as void growth proceeds. Therefore, there will be little change in the electric resistance of the solder bump by the initial void formation. This resistance change raises gradually by growth of the void along the cathode interface as long as the current can pass through the solder bump. Finally, an abrupt change occurs only when the void has extended across the entire joint or when the contact becomes an open circuit[3]. On the other hand, atoms at the anode side react with the interconnect, e.g. Cu, and consumed by the slowly growing IMC.

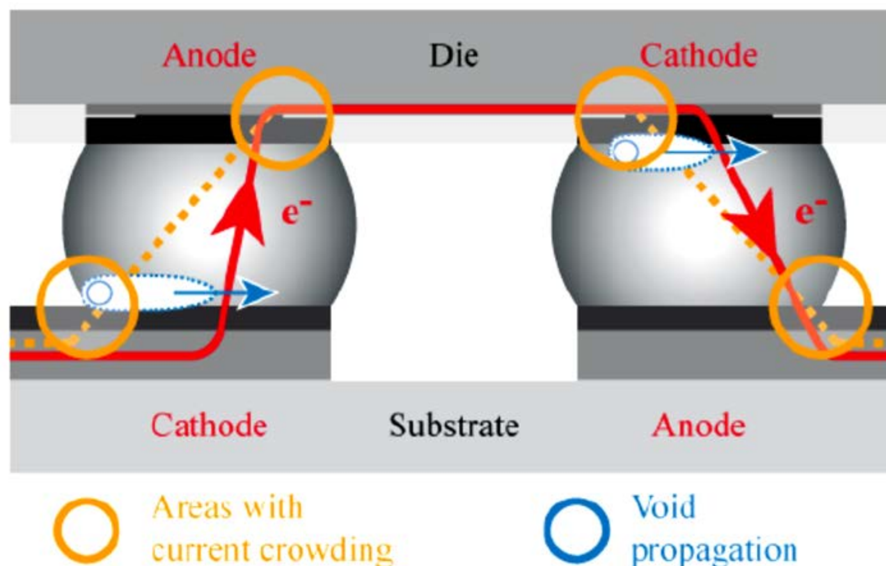


Figure 2-8. In areas with localized increase of current density (current crowding) void initiation and propagation occurs at the cathode side during EM testing, figure is taken from reference [31].

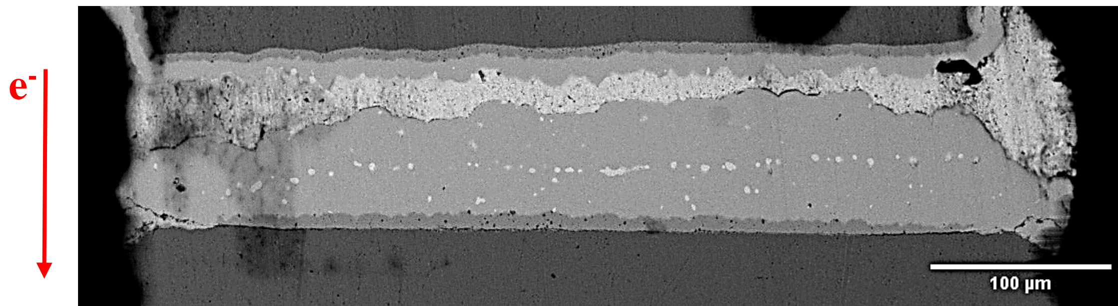


Figure 2-9. SEM cross-sectional image of the EM tested solder joint that shows deposition of IMC at the anode side of the joint.

The growth of EM-induced void can be accelerated by a sequence demonstrated in Figure 2-10. Here, an initial EM causes the void formation that reduces the cross-sectional area for electron conduction. The decrease in the cross-sectional area then makes the local current density to be higher. This also results in local temperature to increase with increase in the Joule heat. Both higher current density and temperature makes EM to be intensified and leads to acceleration of the void growth[2].

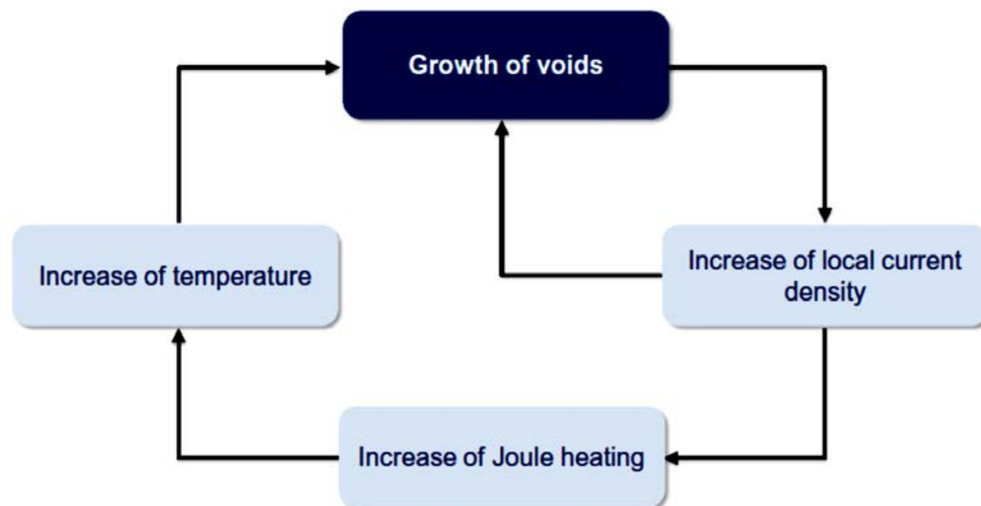


Figure 2-10. Acceleration of the growth of voids by positive feedback loop, figure is taken from reference [2].

2-4- Mean-Time-to-Failure of Flip Chip Solder Joints

The lifetime of a device in the electronic industry is predicted by using the mean time to failure (MTTF) calculation. In 1969, Black provided the following equation to analyze failure in Al interconnects caused by EM[1]:

$$MTTF \approx j^{-n} \exp\left(\frac{E}{kT}\right)$$

The derivation of the equation was based on an estimate of the rate of mass transport resulting in the formation of a void across an Al interconnect. In essence, overall mass transport flux(J) induced by EM is proportional to the current density and diffusivity according to the following formula:

$$J \approx j^{n} \exp\left(\frac{-E}{kT}\right)$$

Note that Black's equation takes a form of reverse relationship of the MTTF with J, i.e., MTTF $\approx \frac{1}{J}$.The most interesting feature of the Black's equation is the dependence of MTTF on the square power of current density, i.e., n =2 which is seen in various EM studies conducted on Al interconnects. However, subsequent studies have been reported controversial results, ranging from 1 to numbers higher than 2. The exponent is especially large when EM failure occurs with considerable amount of Joule heating. The controversy indicates that careful analysis should be conducted when Black's equation is applied to the EM failure analysis of the solder joints. When EM reliability is studied, accelerated tests is necessary, which involves testing at high temperatures and current. High temperature tests are needed to determine the activation energy. The temperature range must be selected carefully so that the diffusion mechanism is the same as the reliability condition under consideration. In the case of a solder joint, EM failure proceeds by a nucleation and growth of void along the interface as is shown in Figure 2-8. The time required to reach failure is not only controlled by the growth of a void across the contact interface. In fact, the incubation time of void nucleation has a greater contribution to the time of the failure, and it takes most of the total time to failure. The portion of the time which takes propagation of the void across the entire contact is smaller than void nucleation time[3].

The effect of current crowding on failure is crucial and should be included in the analysis of MTTF. Current crowding makes the entrance corner of the solder joint to be with higher current

density. Combined with higher local temperature raise due to Joule heating the increase in EM by current crowding leads to the corner to be subjected to intensified EM. Moreover, IMC formation both at the cathode and the anode interfaces can affects failure rate when IMC formation has a sizable fraction of the solder joint. This is not considered in Black's original model of MTTF, and Black's equation needs to be modified to correctly predict solder joint lifetime [3]. It has been reported that Black's equation can be modified to include the effect of current crowding and joule heating[32]:

$$MTTF \approx (cj)^{-n} \exp\left(\frac{E}{k(T + \Delta T)}\right)$$

where c is due to current crowding and has a magnitude of 10 and ΔT is due to joule heating. Both parameters c and ΔT will reduce the MTTF from Black's equation, i.e., make the solder joint fail much faster. Since excessive heat can be generated under higher current density, ΔT depends strongly on j. In other words, the modified equation leads to kinetics model that is much more sensitive to the change of current density than Black's equation. Generally, the design of solder joint and interconnect affects the value of ΔT, because of them affecting heat dissipation[3]. Ideally EM testing needs to be conducted at condition where the amount of Joule heating should be low, and it can be achieved by proper heat dissipation strategy during accelerated EM failure test. The approach used in this research to dissipate the excessive Joule heating via cooling media as is discussed in the following chapter.

2-5- Microbump joints

According to Moore's law, the number of transistors in a dense integrated circuit double about every two years[33]. One of reasons behind such miniaturizing is to enable devices with advanced functionalities and operation speed. The distance between the components needs to be reduced in order to increase the operation speed. Shorter distance is desired not only for application specific integrated circuit (ASIC) chip but also for central processor unit (CPU) as well as other devices assembled in the same system. Microelectronic industries make chips' distances short using TSV (through silicon via) that connects vertically stacked Si chips through via holes. In TSV, vias are made in Si chips and fill them with conductive metal like Cu. TSV technology has

enabled a new form of package and interconnect, which connects one Si die to another one using an even more miniaturized solder joint that is called microbumps[6]. An example of microbump used for connecting chips by through silicon via (TSV) technology is shown in Figure 2-11.

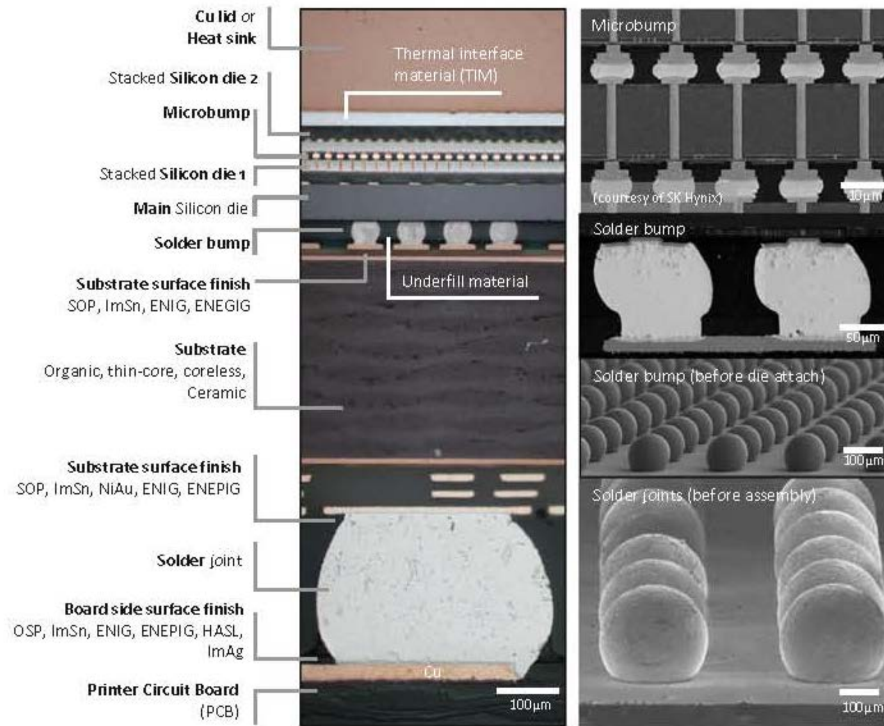


Figure 2-11. Flip-chip connected package with Silicon die stack-up with through silicon via (TSV) and microbump connection, figure is taken from reference [6].

The need for advanced packaging technology like microbump has intensified with a growing demand for portable electronic devices in recent years, such as smartphones and tablet computers where devices with high-volume capacity, high speed, low power consumption, and large-scale integration (LSI) are essential. In order to deal with such demands, smaller and thinner semiconductor packages are required. Recently, the 3D semiconductor packages such as Package on Package (PoP), capable of stacking different IC packages such as memory and logic have developed[34]. The evolution of semiconductor packaging technology is depicted in Figure 2-12.

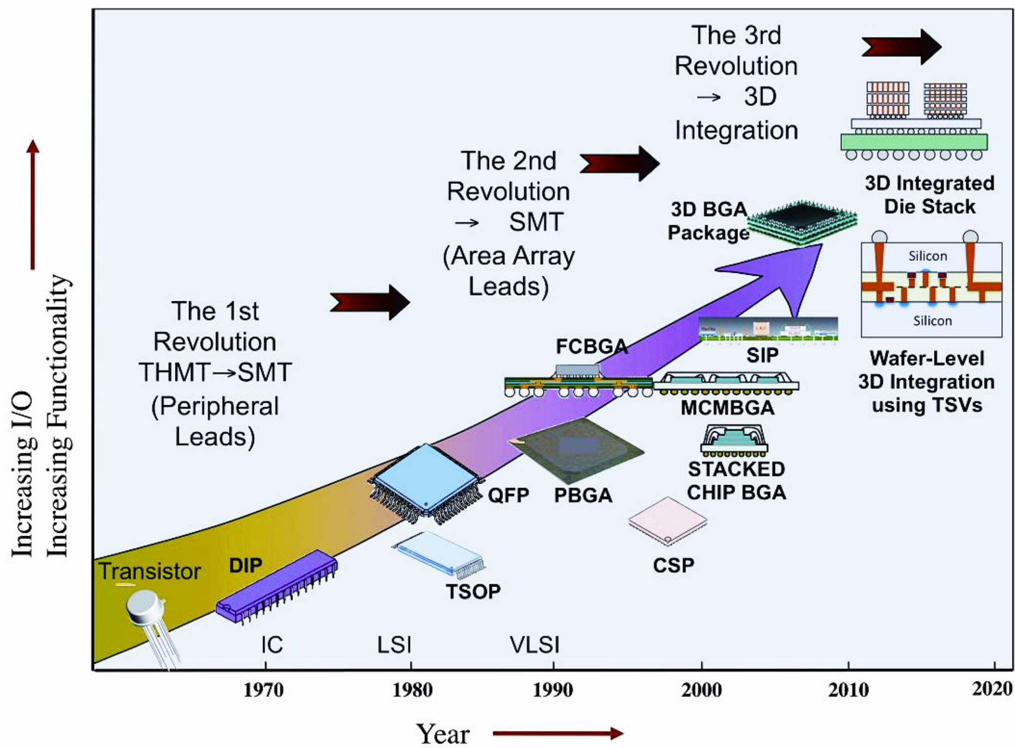


Figure 2-12. Packaging evolution by increasing functionality, figure is taken from reference [35].

The microbump is basically a modified form of the flip chip bump structure. The conventional flip chip solder bump (or C4 bump, following the original IBM-designed, "control collapsed chip connection") is susceptible to current crowding at the entry of electric current to the solder bump. As mentioned before, the current crowding results in the formation of micro-voids which gradually grow at the interface between the solder bump and the UBM layer until a failure happens. A simple approach to deal with the current crowding challenge is to reduce the bump height and the UBM area in the line of the C4 solder bump[36], [37]. An alternative approach is the Cu pillar joints, illustrated in Figure 2-13, which is becoming popular in recent years[38]. In this process, bulk of the solder is replaced by an electroplated Cu pillar, which is deposited directly over the UBM. The main advantage of the Cu pillar joint is that the high local current density region is always within Cu rather than solder material[39]. The higher melting point of Cu compared to the solder material is the reason for having much higher EM-resistance. The higher melting point means higher activation energy is required for atom migration. Also, the current distribution will be uniform before the electrons enter the solder joint so that EM becomes less of

an issue in this type of joint. Further, a tighter pitch is achievable in this technology since the molten solder has a less tendency to touch the molten solder from neighboring joints[37].

While the benefit of microbump is clear, it makes the contact area of solder to be reduced. Smaller contact area makes the current density to increase along with the danger of EM induced failures. Increasing the thickness of the UBM is a very promising way of fighting against the threat of EM failure as it reduces the current crowding. A 3D microbump has a flip-chip structure but the Cu UBM is replaced by a Cu pillar. Implementation of the Cu pillar has advantages: the high electrical conductivity of Cu and the high volume of the Cu pillar enable the fast spread of the electric current through the Cu pillar to avoid the current crowing at the UBM/solder interface. In a Cu pillar structure, the thickness of the solder layer is usually kept as small as possible to be within ~10–30 μm[36].

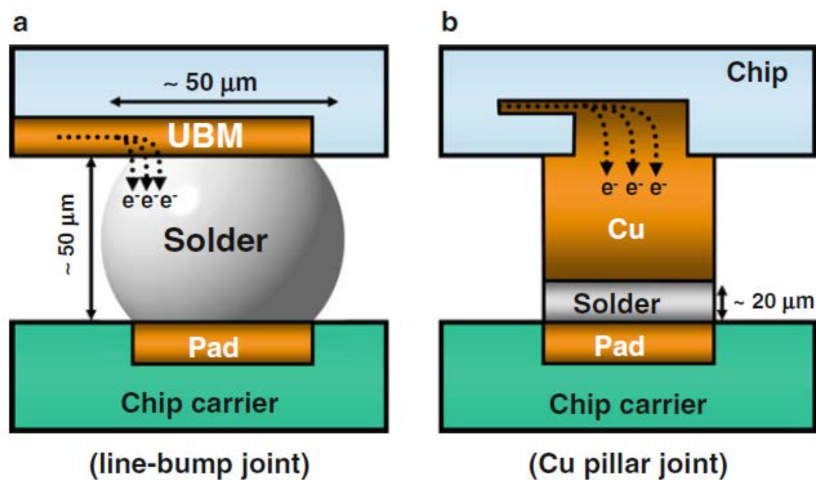


Figure 2-13. (a) Schematic drawing of a flip-chip solder joint. (b) Schematic drawing of a Cu pillar bump, figure is taken from reference [37].

The purpose of using micro solder joints is to increase the I/O (Input/Output) density and thus to enable higher performance. It has been under extensive development and used in some of the advanced packaging technologies like 3D packaging. On the other hand, since the amount of solder material in the micro solder joint is very limited, a diffusion barrier layer such as Ni or NiP is required to prevent the full conversion of solder. Otherwise, the joint is filled with the brittle IMC after chip joining preprocess, making the joint to be prone to mechanical fracture. The reaction of the Ni layer with the solder material forms Ni_3Sn_4 intermetallic compound as well but

IMC formation rate is lower than Cu-Sn interaction [40], [41].

2-6- Importance of EM in micro solder joints

As described above, the process of EM in the interconnect of an integrated circuit (IC) is a major reliability concern for IC designers. EM occurs when there is a high density of current in the interconnect. The current density (j) defines as the quotient of the flowing current (I) and the cross-sectional area (A) of the conductor:

$$j = \frac{I}{A}$$

Therefore, current density will increase when we have either the increase of current (I) in the numerator or interconnect geometry parameters such as the cross-sectional area (which will decrease A in the denominator). These two parameters, i.e. I and A are clearly critical in the context of EM. Scaling of ICs size reduces the cross-sectional areas of the metallic interconnects, but the required currents cannot be reduced to the same extent even by reducing the supply voltages and gate capacitances. Then EM concerns arise due to increased current density. This unequal change in the contact area and current is plotted in Figure 2-14[2].

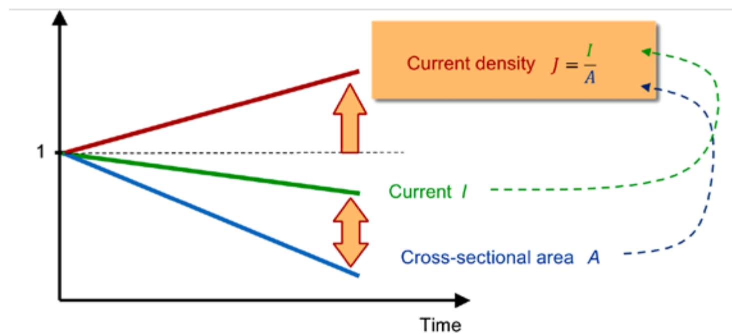


Figure 2-14. Projected current densities due to decreasing interconnect cross-sections and only slightly falling currents, figure is taken from reference [2], [42].

As is presented in the previous section, the microelectronics industry is currently transitioning from traditional flip-chip technology to 3D (or 2.5D) integrated circuits (ICs) to meet the demands for higher packaging density, better performance, and smaller form factors. In 3D

ICs, micro bumps connect through Si vias (TSV) to joint several Si chips together. The redistribution layer (RDL) is used in the TSV chip for connecting TSV with micro bumps (Figure 2-15) [43], [44].

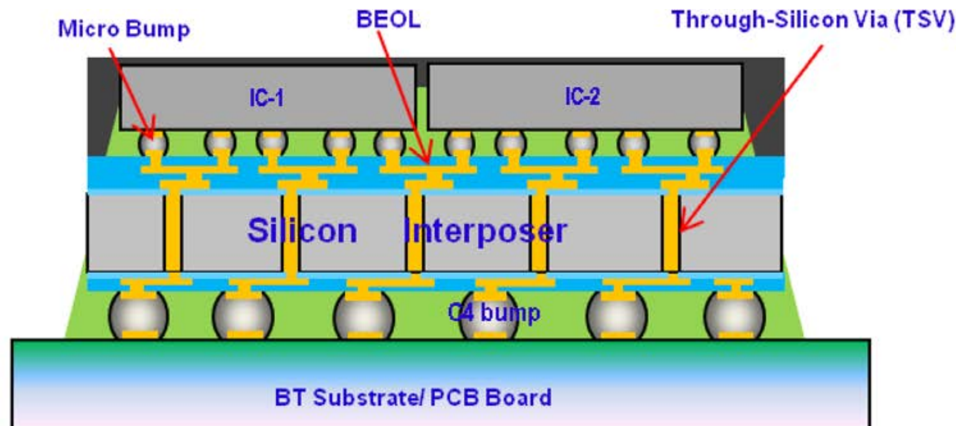


Figure 2-15. Schematic of IC integration in 3D packaging, figure is taken from reference [43].

The micro bumps usually have a diameter of about 10–20 µm, which is almost one order of magnitude smaller than flip-chip first level interconnect (FLI). The joule heating in micro bumps will increase dramatically while the same power demand creates much more current density. It will be much higher when all the Si chips are stacked together. Reliability concerns in 3D ICs arise due to EM in micro bumps, TSV, and RDL[45]. If the level of Joule heating is very high, it may also induce a large thermal gradient and local high temperature which eventually induces thermomigration failure, circuit burn or even melting of the solder joints [46]–[48]. Common EM failure mode is the failures at IMC/solder interface due to flux divergence induced by Sn self-diffusion [46], [47]. On the other hand, the dissolution of UBM on the cathode side can also accelerate and cause failures due to the depletion of UBM. It has been reported that Sn grain orientations have a great impact on the Cu dissolution rate [49], [50]. As mentioned before, main EM failure mode in solder joints is void formation that involves void nucleation and its propagation. The place that voids start to nucleate is near the entrance of electrons. The momentum exchange between electron wind and metal ions causes to moving away of the predominant diffusion species and increases number of vacancies. Further atoms migration results in high density of atomic scale vacancies that eventually link together and form void. In Sn-based Pb-free

solders, the predominant diffusion specie is the Sn atom and the EM failure occurs between the IMC and the solder on cathode side. In essence, flux divergence exists at the Sn/IMC interface on substrate side causes the void nucleation and propagation along that interface which lead to EM failure in the joint. Many factors can involve the EM failure of solder joints inducing Sn self-diffusion, solder alloying, IMC formation, current crowding, metallization dissolution, and solder joint height. All these factors are applicable to micro bumps in 3D packaging as well[45]. Some of EM failure of micro solder joints caused by of these factors are illustrated in Figure 2-16.

The solder joint under EM condition has a very dynamic nature under electron wind force and high temperature. Metallization and Sn will keep reacting to form IMCs from both cathode and anode. This reaction will either coarsen the existing IMC particles in the solder matrix or increase the thickness of the IMC on the anode side. The metallization is typically Cu or Ni and IMC formation due to its reaction with Sn causes volume shrinkage. This shrinkage will generate Sn vacancies during the reaction. Then, the probability of solder voids nucleation and growth at IMC/solder interface on the cathode side, where Sn atoms flux divergence happens. With respect to this fact, IMC formation and the instability of the solder system can reduce the EM capability[45].

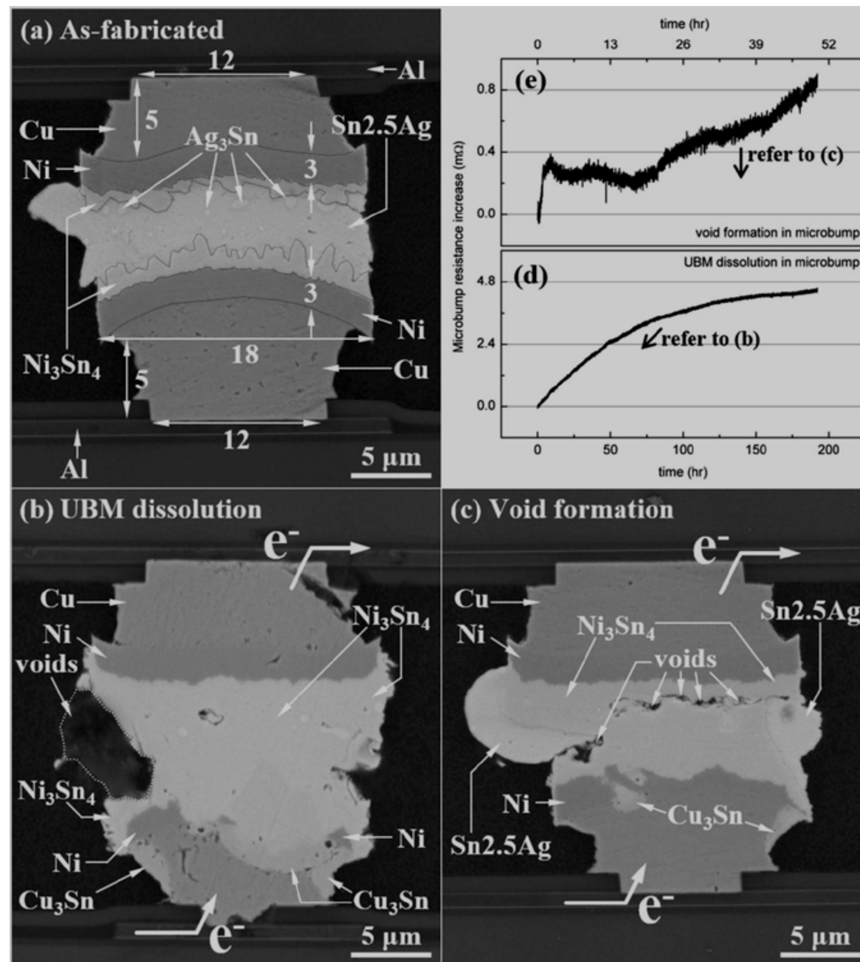


Figure 2-16. (a) The SEM image of the as-fabricated 18 μm microbump; The SEM image showing (b) the UBM dissolution and (c) the void formation induced by EM after 9.2×10^4 A/cm^2 at 150 °C for 192.3 and 50.0 h, respectively; The resistance increases due to (d) the UBM dissolution in (b), and (e) the void formation in (c), figure is taken from reference [51].

In the case of smaller 3D packaging micro bumps, the IMC reaction can impact EM failure even more dramatically because the Sn volume is very limited and easy to be exhausted. On the other hand, the IMC formation can have an advantage when the thick IMC on the anode side can reduce the effective Sn-based solder height and delay or eliminate the EM damage due to Sn flux divergence. During current stressing, full consumption of Sn will make thicker anode side IMC and thinner cathode side IMC to merge. However, when cathode and anode IMC merges together, a gap can form because the IMC reaction accompanies volume shrinkage. Since IMC on the anode side is thicker, the gap can be formed close to the cathode side when more Sn are exhausted. It has

been reported that when Cu to Sn volume ratio is larger than 0.52, the solder joint will convert fully to Cu_6Sn_5. In other words, as long as the Cu height is taller than half of the solder height, the solder joint fully converted to IMC before it fails by complete Cu dissolution. It is reported that Cu_6Sn_5 is more susceptible to EM than Cu_3Sn, by the fact that Cu_6Sn_5 has lower solidus temperature and higher resistivity than Cu_3Sn. Despite the very high intrinsic EM resistance of full IMC bump, in some cases it can fail at Cu_3Sn/Cu interface, as reported in Cu/Sn-Ag/Cu micro bumps[45].

As mentioned above, the EM failure mechanism can be different in the micro solder joint. One obvious reason is related to the fact that the joint contains a limited amount of the solder so that it can be quickly converted to Cu-Sn intermetallic compounds (IMC) prior to EM developing sizable damage [48]. In a typical Pb-free solder joint, usually, Sn and Cu are two active atomic species that constituting the total EM flux and since it contains Sn in excess of 95 wt.%, Sn EM flux is regarded as the main source of voids. Cu is continuously replenished from the cathode end of the joint and also low solubility of Cu in Sn solder makes Cu EM flux to be small, so the contribution of Cu EM on void volume should be negligibly small. However, Cu can play a significant role in EM failure mechanism of the micro solder joint because an accelerated growth of Cu-Sn IMC can interfere with the void growth. Where Sn solder layer is very thin, the growth of Cu-Sn IMC on both sides of solder joints can reach and merge together before the formation of EM voids in Sn solder. As we know, the full IMC joint is immortal against EM void by owing the fact that IMC requires much more activation energy for atoms migration. Consideration of Sn EM flux and fast IMC formation due to the low amount of solder material suggests that EM failure mechanism in the micro solder joint can be substantially different from what is known from the conventional solder joint. In the case of micro solder joint, EM failure mechanism involves two kinetically competing processes, which are the rate of voiding by Sn EM and IMC growth by Cu EM[52], [53].

Chapter 3: Experimental Methods

3-1- Sample structure

The samples used in this research are structurally a flip-chip on a lead frame (LF) with Pb-free Sn-Ag-Cu (SAC) solder alloys. As mentioned in the research summary chapter, there are two main groups of samples with different geometry. The geometry of the first group of samples is presented in Figure 3-1. As depicted in 3D schematic, solder alloy is placed between a Cu pillar and a lead frame (LF). It can be seen that the joint geometry is elliptical shape with a design of current flowing from lead frame to the solder joint and exit from support joints.

In order to confine the EM load to the target joint, we placed a number of supporting joints near the EM pillar and used them to provide distributed current paths to the joint under EM testing. This arrangement was used to make the test current to flow from the LF to Cu-pillar, meaning that EM is directed from the pillar to the LF direction. In addition, there were bumps that were not subjected to the EM, which served as reference bumps to compare microstructure of EM tested and thermally stressed solder joint.

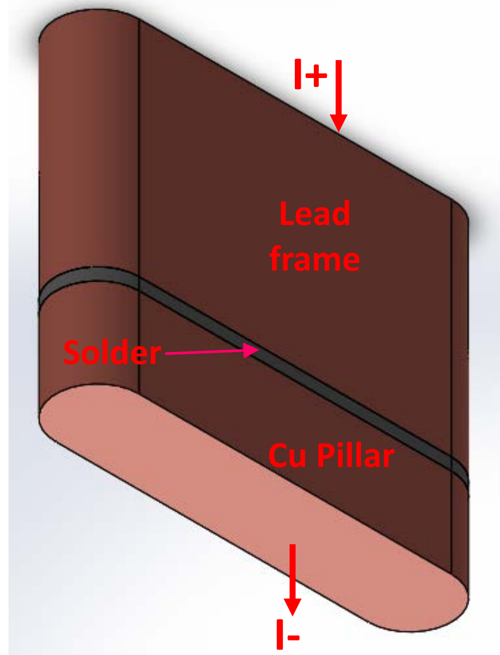


Figure 3-1. 3D schematic of first group of samples used in this research.

In samples with elliptical geometry, there are different arrangements of interfacial layer

(Ni) at the solder/interconnect, and they are the joint without Ni layer, Ni layer added to the interface of the solder and lead frame, Ni layer added at both interface of solder with lead frame and Cu pillar . The essential configuration of these joints are presented in Figure 3-2 (a), (b), and (c) respectively.

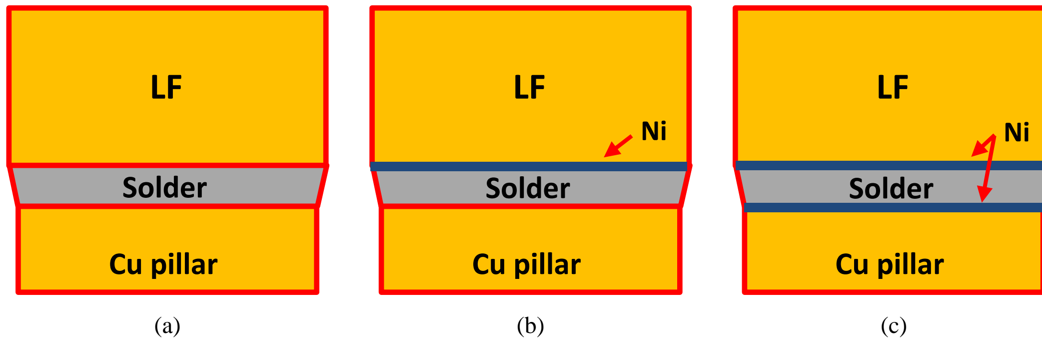


Figure 3-2. Cross-sectional schematic of elliptical shape samples (a) without Ni layer, (b) Ni layer added at LF side, (c) Ni layer added to both LF and Cu pillar side.

As presented in Figure 3-2, where the schematic representations of the joint cross section are illustrated, the Cu-pillar is patterned on top of Si wafer and mated to the LF using electroplated lead-free SAC alloys. The dimension of the Cu pillar is approximately 300µm in length, 110µm in width, and 65µm in height. The mating electrode of the bump is the Cu-LF coated with Pd as the pre-plated layer (Pd pre-plated LF). The solder joint is formed by subjecting the assembly to a standard reflow condition. As mentioned above, different arrangements with and without Ni interfacial layer prepared for this study. While the joint arranged of the bare Cu pillar and Ni coated lead frame was the focus of our study, we also prepared the samples with Cu pillar having ~3µm Ni finish to study the impact of the diffusion barrier on the EM mechanism. The distance between the top of the Cu-pillar and bottom of the LF before reflowing is approximately 20-30µm, but due to the formation of IMC phases at both the pillar and the LF interface, the actual solder layer thickness after the reflow is reduced to ~15-25 µm for both the assembly with the Ni coated and the bare Cu pillar. Figure 3-3 through Figure 3-5 show cross-sectional SEM images of elliptical shape samples with different interfacial layer arrangements. As we can see, there is a limited amount of solder joint between the IMC layers in all types of joint arrangement. Microstructure images at higher magnification that are illustrated in Figure 3-6 through Figure 3-8 show more detail of the solder joint.

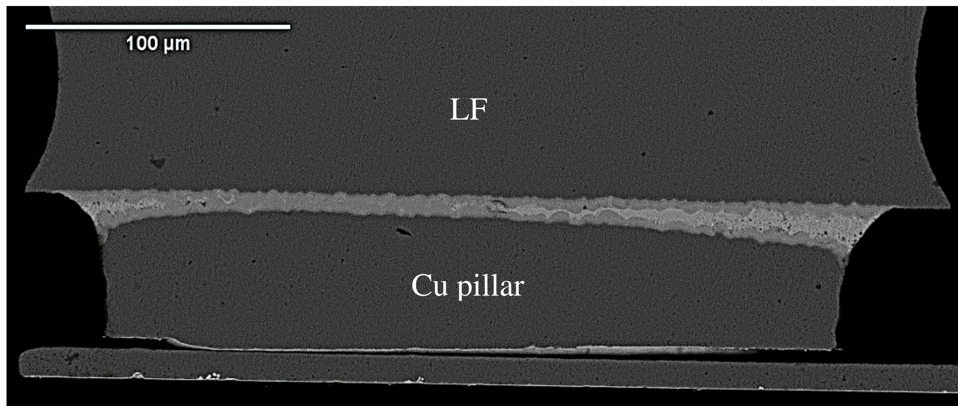


Figure 3-3. Cross-sectional SEM image of elliptical shape samples without Ni interfacial layer.

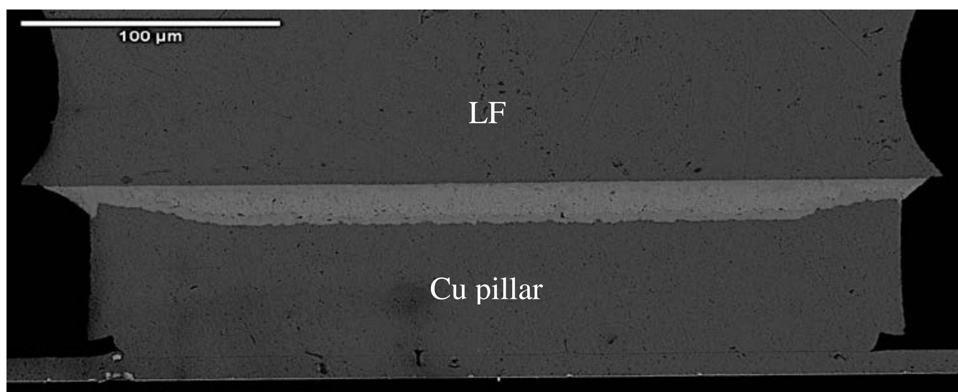


Figure 3-4. Cross-sectional SEM image of elliptical shape samples, Ni layer added at LF side.

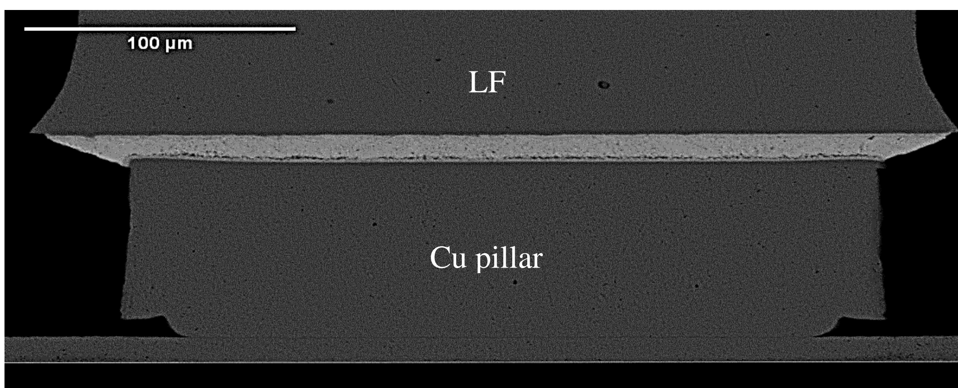


Figure 3-5. Cross-sectional SEM image of elliptical shape samples, Ni layer added to both LF and Cu pillar side.

The cross-sectional SEM views of the different arrangements show that the growth of the IMC phase on both interfaces, Cu pillar/solder, and solder/LF, causes the thickness of the solder layer to be substantially reduced especially in the samples that no Ni layer was added to the solder interfaces.

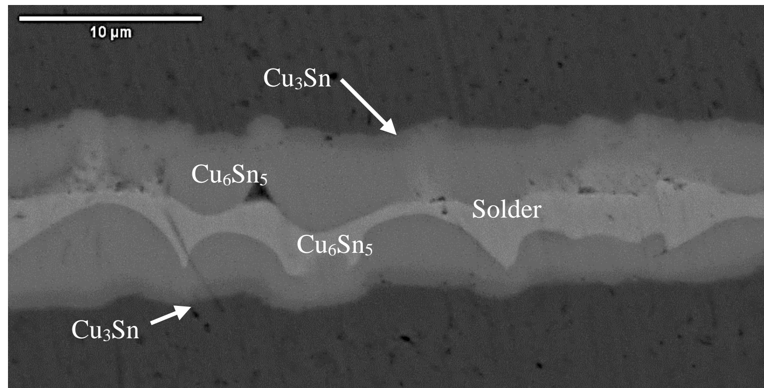


Figure 3-6. Cross-sectional SEM image of elliptical shape samples without Ni interfacial layer.

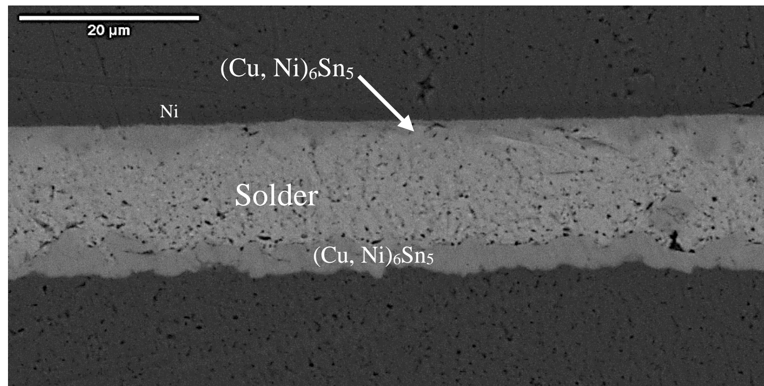


Figure 3-7. Cross-sectional SEM image of elliptical shape samples, Ni layer added at LF side.

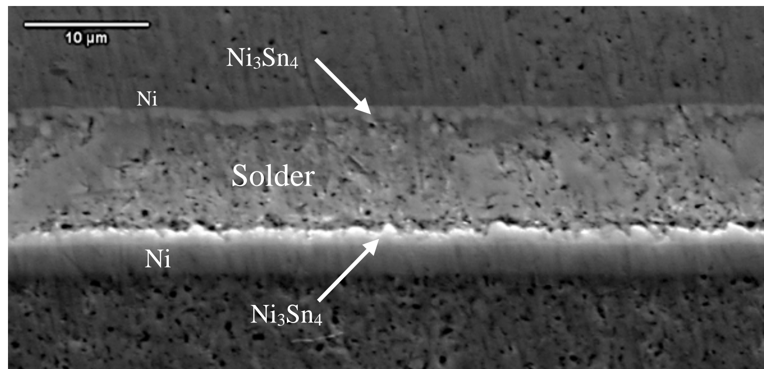


Figure 3-8. Cross-sectional SEM image of elliptical shape samples, Ni layer added to both LF and Cu pillar side.

The chemical composition of IMC phases was determined by the use of EDS (energy dispersive spectroscopy) analysis. This analysis determines the IMC phases formed due to the interaction of solder at interfaces during the reflow. The IMC phase found in the sample without Ni layer is determined to be Cu_6Sn_5 at both the pillar and the LF interface with a thin layer of Cu_3Sn on the Cu_6Sn_5. Figure 3-6 shows the scallop shape IMC formed at the interfaces of solder joint with Cu interconnects. In addition, most of the solder material converted to IMC due to extended interaction of solder with Cu at both interfaces during the reflow process. In the case of the sample with Ni layer at one side (Figure 3-7), $(Ni,Cu)_6Sn_5$ phase is found to form at both interfaces even though Ni layer is not present at the interface of Cu pillar and the solder. The reason that Ni presents at both solder interfaces is because that the diffusion of the Ni through the molten Sn during reflow forms Ni contained IMC at the time of solidification[6]. Ni_3Sn_4 phase formed at both LF and Cu pillar interfaces in the samples with Ni layer at both interfaces (Figure 3-8). The addition of Ni at both sides of the solder limited interaction of the solder and Cu interconnect, then the formed IMC composed of Ni and Sn intermetallic that is Ni_3Sn_4.

As per this research outline (Figure 1-1), there are samples with another geometry that have called cylindrical Cu pillar. 3D schematic of this type of sample is illustrated in Figure 3-9. The geometry of this sample type is designed to have a smaller Cu pillar length (about 1/3 of elliptical shape) and consequently, solder size has been shrunk to the size of Cu pillar. Other components of the sample's structure such as lead frame and Cu trace thickness are the same as first group of the samples (elliptical Cu pillar shape). Reducing the size of the Cu pillar will produce high current

density at lower level of current flowing since the contact area diminished around 1/3 compared to the previous sample structure.

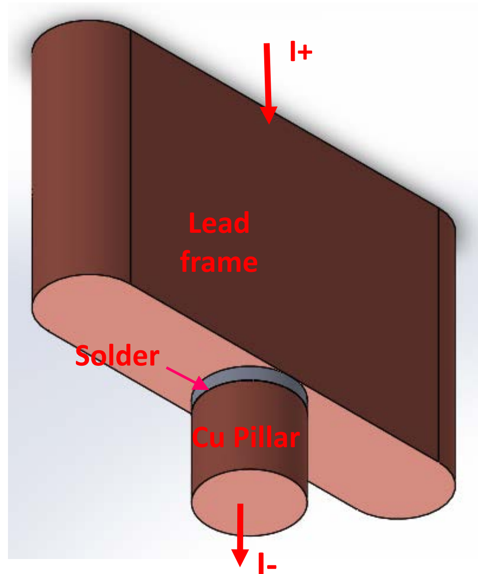


Figure 3-9. 3D schematic of samples with cylindrical shape Cu pillar.

The cross-sectional schematic and SEM microstructure of the cylindrical shape sample is shown in Figure 3-10. As illustrated in this figure, a very limited amount of the solder material is situated between the lead frame and Cu pillar. Since there is no Ni layer at interfaces of the solder, interaction of Sn and Cu created Cu_6Sn_5 after the reflowing process. Also, a thin layer of Cu_3Sn is formed between Cu_6Sn_5 and Cu interconnects that is not distinguishable in the given magnification of the microstructure.

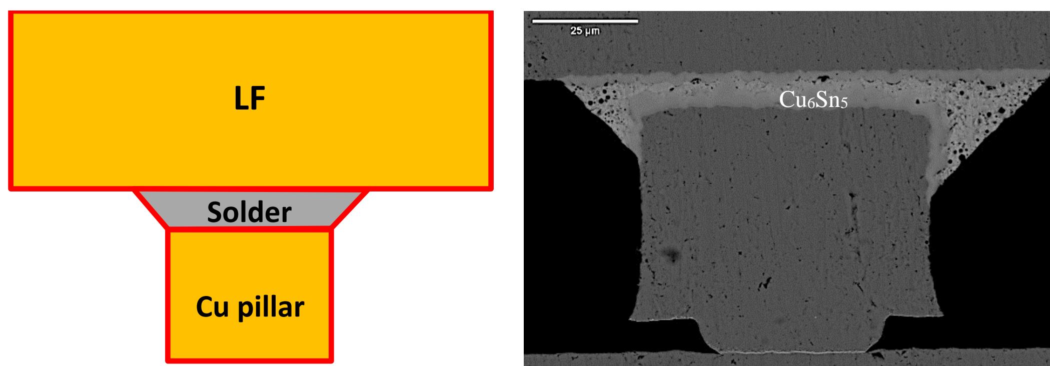
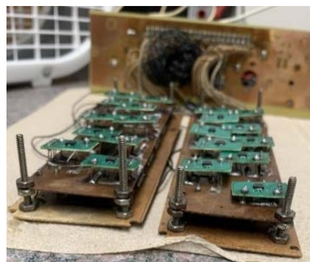


Figure 3-10. Cross-sectional view of samples with cylindrical shape Cu pillar.

3-2- Electromigration test set up and design of experiments

In order to induce EM failure in the micro solder joint, we needed to apply exceptionally high current density into the solder joint. Practically, applying high current has limitations due to high excessive heat generation. The high amount of heat generation due to Joule heating can affect EM failure mechanism and impose test artifacts like further thermal stress on the joint. Then, we must manipulate this generated heat to remove that kind of test artifact. In this respect, we developed for this research a customized EM test system with an oil bath to enable effective JH dissipation and maintenance of temperature uniformity and stability for the duration of EM testing. The temperature of the joint during the test was monitored using the on-chip temperature sensor, and the temperature of the ambient was adjusted to bring the joint temperature to the target temperature. With the help of circulating oil, we were able to limit the temperature difference between the sample and oil to under 10ºC even with a current density exceeding 36 kA/cm^2. The oil-bath system was placed into an oven to elevate the temperature of the Bath. Also, for each test leg 20 samples were assembled on the testing board. The test board was designed to flow constant current into the samples and measure the voltage of the micro solder joint and temperature sensor (RTD) during EM test for every single sample. The oil-bath and assembled samples on the test boards are shown in Figure 3-11. Also, Figure 3-12 shows complete features of the oil-bath system with voltage and temperature sense connections.



Assembled samples on the test boards

Oil-bath

Testing board inserted to the oil-bath

Figure 3-11. Assembled samples on test boards and oil-bath system for EM test.

Figure 3-12. Oil-bath system with all connections.

Before running EM test, joule heating measurement was done based on the temperature constant resistance (TCR) method for each test condition to calculate generated heat due to applying high current density. The resistance is directly related to the temperature as,

$$R = R_0\big(1 + \alpha(T_D - T_0)\big)$$

where T_0 is the reference temperature (0ºC), R_0 is the resistance at T_0, α is the temperature coefficient of resistance (TCR) and T_D is the average temperature of the test structure[54].

Temperature raise due to JH is generally given by $\Delta T \propto RI^n; n > 2$.

The procedure for JH calibration was performed as per the following steps:

1. Gain low level of constant current from the power supply (like 0.3 A) to apply the samples. This level of current was sufficiently low to produce negligible JH.
2. Measure resistance of the joints at room temperature (can be excluded from TCR measurement because room temperature can vary).
3. Increase oven temperature incrementally and measure the resistance to get at least 5 points (the final temperature should be around 10ºC lower than the target test temperature).
4. Plot R vs T and fit data using linear fit. R(T)=R(0)+ST; R(0)=R at T=0 ºC.
5. Determine TCR by $\alpha = \frac{S}{R_0}$
6. Project resistance at target temperature by using $R(T_t)=R(0)+ST_t$.
7. Increase current to the target testing current, measure the resistance and adjust the oven

temperate to closely match the measured R to the projected R without JH.

8. Calculate the sample temperature using $\Delta T = [R(T_m) - R(T_t)]/S$

The linear relationship of R vs T is plotted in Figure 3-13, also the JH level increased due to applying current is marked in the plot.

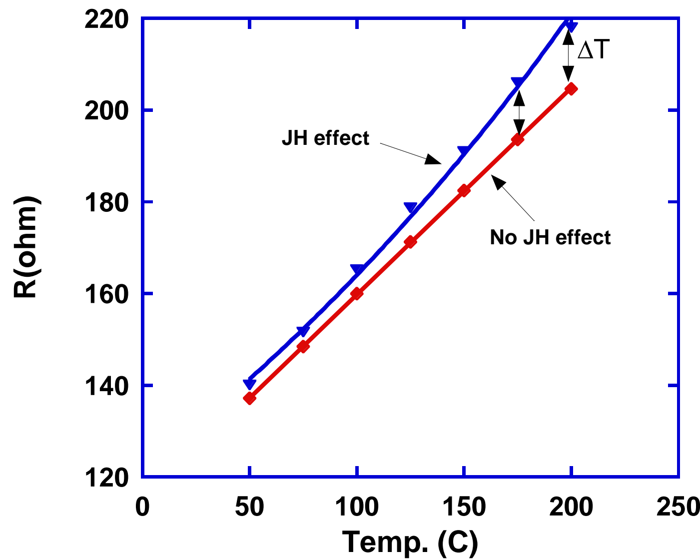


Figure 3-13. Linear relationship between R and T and JH level(ΔT) due to applying current.

As mentioned in the previous chapter, based on Black's equation ($MTTF \approx j^{-n} \exp\left(\frac{E}{kT}\right)$), to calculate the thermal activation energy (E) different temperatures are used at constant current density. In addition, to calculate the current density exponent (n) different current densities are applied to the samples at a constant temperature. Figure 3-14 explains how test conditions are selected to calculate thermal activation energy and current density exponent by variation of EM test temperature and current density.

Slope= activation energy (E)

MTTF

0.5 1 1.5 2 2.5 3 3.5

$1/T(K^{-1})$

(a)

Slope= current density exponent (n)

MTTF

Current density(J)

(b)

Figure 3-14. The method used to calculate EM failure (a) thermal activation energy, (b) current density exponent.

Table 3-1 presents the bath temperature used to conduct EM testing of given samples at the target temperature based on joule heating measurement for elliptical shape samples.

Table 3-1. EM test conditions based on joule heating measurement for elliptical shape samples.

Sample	Current, A	Current density, kA/cm^2	EM T, °C	Bath T, °C	δT, °C
Ni layer added at LF side	11	36	144	136.5	7.5
	11	36	152	144	8
	11	36	160	152	8
	11	36	170	161.5	8.5
	12	40	152	142	10
	12	40	170	160	10
Ni layer added to both LF and Cu pillar side	11	36	160	151	9
	11	36	170	160	10
without Ni layer	11	36	170	162.5	7.5

In situ measurement of solder joint voltage for each sample was performing during EM test by means of data acquisition equipped with a voltmeter. The voltage values were sending to the computer and they were recording by using the National Instruments LabVIEW program. The

program was designed to capture the joint voltage and convert it to resistance. The overall scheme of the EM test procedure, which shows different parts of the experiment set-up, is depicted in Figure 3-15.

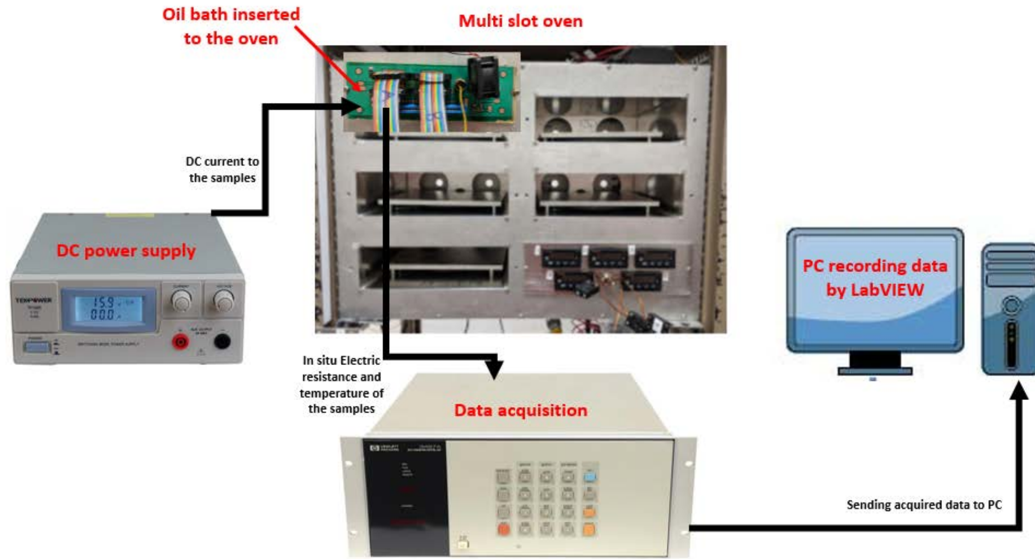


Figure 3-15. EM test set up used in this research.

After failing the samples or elapsed time of testing, samples were pulled out from the oil-bath and failure analysis was done for investigating microstructure changes. For failure analysis of samples that contains Ni-Sn intermetallic, the Cross-section of samples after the test was prepared by employing ion cross-section polishing to omit mechanical polishing artifacts. Cross-sections of solder joints were prepared, and microstructure changes were studied employing SEM/EDS. Besides, in some cases, EBSD was performed to identify the orientation of the grains and phases.

The second stage of this research is the study of EM failure on the samples with cylindrical geometry. In order to be able to compare EM failure kinetics in both sample structures, which are elliptical and cylindrical geometry, the amount of current density was selected in the same range to have a reliability evaluation in the same stressing test matrix.

In this respect, 3A is the equal current amount that transfers the current density of 36 kA/cm^2 to the solder joint in the joint with cylindrical shape Cu pillar. Moreover, the result for the

samples that no Ni interfacial layer added to solder interfaces showed that quick conversion of the joint to the IMC makes it immortal against EM failure. Since we are studying EM failure in the solder joint, the design of the experiment should be on the purpose to induce EM failure. Then, a higher test current in addition to 3A is considered to create failure in the joint. Joule heating measurement at different test currents helped us to determine its level. This calculation suggested the currents that would not incorporate test artifacts such as high thermal stress. Based on that, the currents that generate heat lower than 10°C were selected for EM test. Experiments are designed at different test currents and temperatures for calculation of failure kinetics parameters like thermal activation energy and current density exponent according to Black's equation, which explained the previous chapter. Table 3-2 shows the EM test condition by considering the joule heating level and design of the experiment. The same test procedure was employed to run EM test and after failing the samples, statistical and failure analysis were done for each test leg. Collecting data of all experiments allows us to determine failure kinetics parameters and failure mode in the solder joint with fine pitch Cu pillar geometry.

Table 3-2. Table 1. EM test currents and temperatures used for testing samples with cylindrical geometry.

Sample	Current, A	Current density, kA/cm^2	EM T, ^{o}C	Bath T, ^{o}C	δT, ^{o}C
Cylindrical Cu pillar	3	36	152	146	6
	4.2	51	142	144	7
	4.2	51	152	152	8
	5.5	67	142	161.5	9.5
	5.5	67	152	142	10

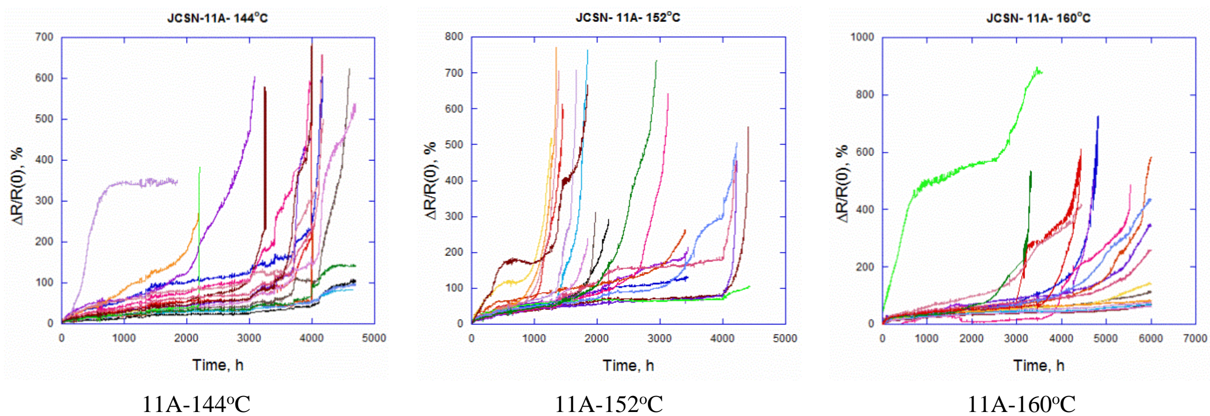
At the end, this comprehensive study will give us an idea to understand the EM failure mechanism in the micro solder joints. By doing these efforts and compare the results with conventional flip chip solder joint, we can distinguish similarity and discrepancy of EM failure in both types of solder joint.

Chapter 4: Results and discussion

4-1- Failure Kinetics in Joint with elliptical joint geometry

4-1-1- **Samples with Ni layer at solder/LF interface**

As mentioned in experimental detail, samples with Ni layer added to LF side are the main type of elliptical shape samples to derive failure kinetics parameters. The resistance changes of samples during the EM test were monitored and once the resistance change showed a substantial increase, more than 300 percent (runaway increase), the current flow through that sample bypassed. However, the actual failure criterion is lower than runaway increase, and typical resistance increase to be considered failed joint is 20% in operational condition[55]–[57]. The graphs of resistance changes of samples tested at different test conditions are shown in Figure 4-1. As we can see in these graphs, samples are failed in various testing times. The time to failure (TTF) is defined to be the time that resistance change reaches more than 300 percent increase, which is illustrated as a runaway rise in graphs.



11A-144ºC 11A-152ºC 11A-160ºC

Figure 4-1. Resistance changes of EM tested samples (elliptical geometry) at different test temperatures with 36 kA/cm^2.

A cumulative probability refers to the probability that the value of a random variable falls within a specified range. Frequently, cumulative probabilities refer to the probability that a random variable is less than or equal to a specified value. It has been reported that the cumulative distribution function of failure (CDF) for a group of single interconnects can be fitted by a

normal/lognormal distribution[54]. The values of cumulative probability based on different TTF were calculated by the following formula,

$$Cumulitive\ probility = \frac{i - 0.3}{N_{total} + 0.4}$$

where i is the rank of the sample after all the samples were sorted by TTF and N_{totoal} is the total number of the samples. If the relationship of cumulative probability versus TTF falls to a linear trend, it indicates that failure events are normally distributed. As we can see in Figure 4-2, TTF versus cumulative probability falls to a linear trend. Meaning that TTF statistics fits very well to a normal distribution with the shape factor (slope of linear fit) reasonably uniform across the samples failed at different temperatures. The TTF shown in these plots is collected by fitting the TTF of 17~20 samples to cumulative probability for each testing condition.

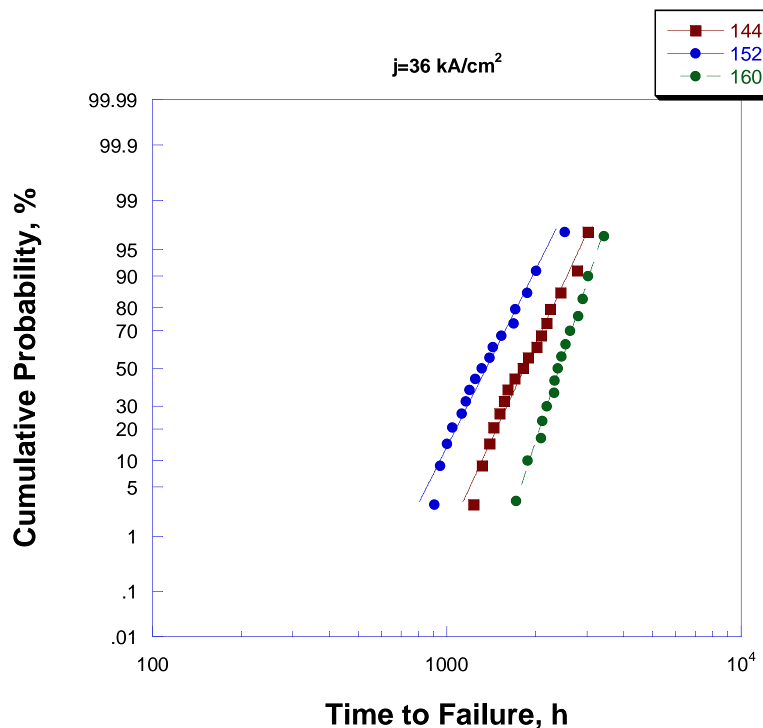


Figure 4-2. TTF of samples tested under 36 kA/cm^2 at three different temperatures as a function of normal cumulative probability.

Mean time to failure (MTTF) analysis is the popular method that electronic industry uses

to predict the lifetime of a device. Basically, the MTTF is the time when half of the samples are failed. Meaning that, if we draw a line from 50% cumulative probability toward the linear trend, the time that crosses the line is the MTTF. Figure 4-3 Shows how to find MTTF from a graph of cumulative probability vs TTF.

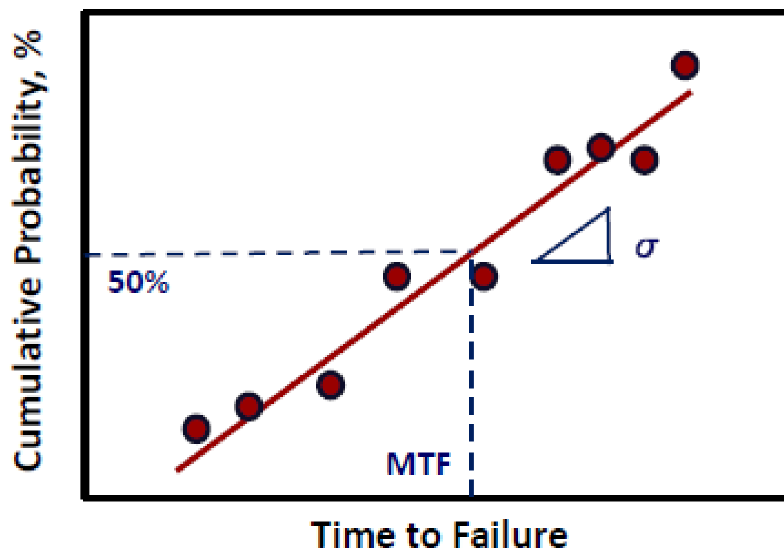


Figure 4-3. Determining the mean TTF from cumulative probability vs TTF graph.

MTTF of each test leg was calculated from cumulative probability vs TTF graph and Figure 4-4 shows the variation of MTTF as a function of testing temperature for the samples EM tested under current density of 36 kA/cm^2. Despite the previous studies that have been reported a linear change of MTTF with temperature, which implies single thermal activation energy kinetics, note the fact that the MTTF in Figure 4-4 does not follow a single activation energy relationship with temperature. The data seems to suggest that some sort of abnormal process is involved in the failure kinetics at 152°C, where the direction of the linear relationship is changed. It is almost tempting to attribute this behavior to the error in setting the test temperature because JH induced temperature change is often difficult to accurately compensate. However, as indicated in Table 3-1, the temperature was well regulated and cannot be a source of the abnormality. We believe that it is rooted more in the physical mechanism that is the EM failure kinetics being governed by two competing processes. EM void formation due to Sn migration prior to its conversion to IMC is dominant at the lower range temperature range where MTTF decreases by raising test temperature.

On the other hand, full conversion of solder to IMC that makes solder immortal against EM is the dominant process at higher test temperature and this dominant process is changed kinetics of MTTF with temperature. This phenomenon will be discussed more in the following section where failure analysis microstructures can better explain this change of dominant process.

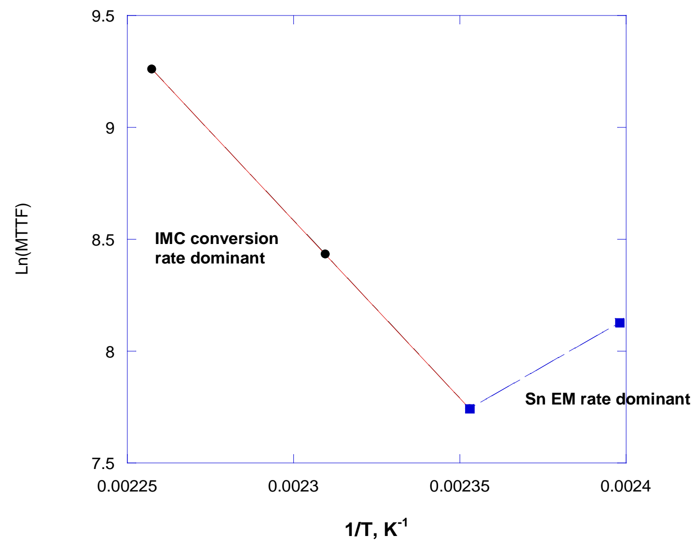
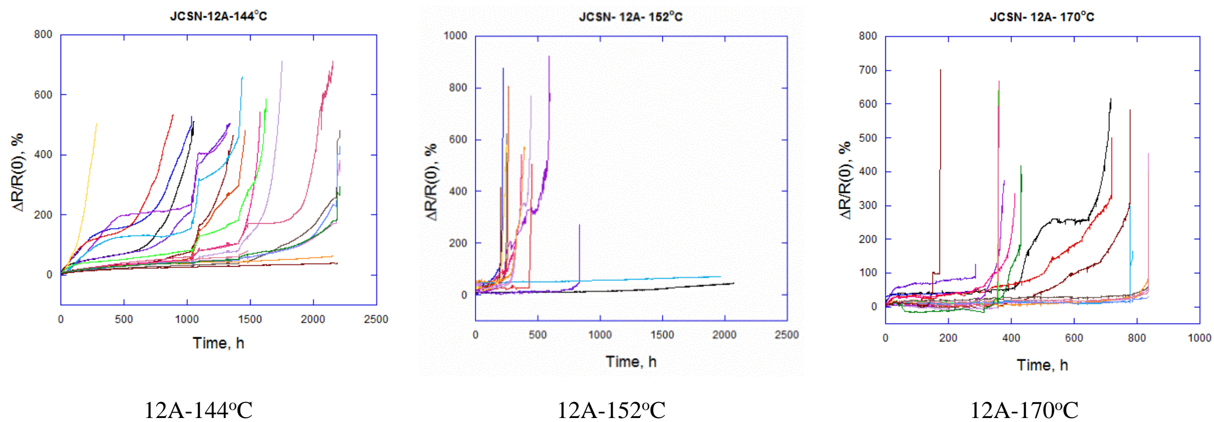


Figure 4-4. The MTTF of EM failure as a function of test temperature for samples tested under 36 kA/cm^2.

Curve fit calculation shows that activation energy between 144ºC to 152ºC is about 0.73 eV and between 152ºC to 170ºC is -1.37 eV as well. Since the sign of activation energy changed, definitely we cannot use single activation energy for the MTTF equation to predict the lifetime of this particular micro solder joint under current density of 36 kA/cm^2. Then, the thermal activation must be reported for a specific temperature range that the thermal activation energy is calculated.

For the samples tested at 12A (40 kA/cm^2), the resistance change graphs are shown in Figure 4-5. EM test under 12A (40 kA/cm^2) performed at 144ºC, 152ºC and 170ºC. As we can see in resistance change graphs, runaway resistance change is considered as a failure criterion similar to the samples tested at lower current density.



12A-144ºC 12A-152ºC 12A-170ºC

Figure 4-5. Resistance changes of EM tested samples (elliptical geometry) at different test temperatures with 40 kA/cm^2.

Based on the resistance change graphs, failure times were extracted and cumulative probability versus TTF is plotted in Figure 4-6. This graph shows that cumulative probability fits linear with TTF although for the samples tested at 170ºC some points deviate from linearity. MTTF was derived from normal distribution plots for each testing temperature. Figure 4-7 is plotted MTTF versus temperature between 144ºC and 170ºC for the samples tested with 12A (40 kA/cm^2) current load. As we can see in this graph, the failure kinetics does not follow single activation energy similar to the sample tested under 11A (40 kA/cm^2) current load. According to Figure 4-8, MTTF is reduced by increasing test temperature from 144ºC to 152ºC meaning that elevated temperature can accelerate EM damage rate and cause a shorter TTF. However, increasing testing time from 152ºC to 170ºC shows the increase of MTTF by increasing test temperature. As described above, the conversion rate of solder to IMC is higher than EM damage in the solder joint at high temperature test conditions. As a result, EM test at higher temperature does not necessarily show shorter failure time unlike the previous studies have been reported for conventional solder joints. This unique behavior is due to the limited amount of solder material in the micro solder joint that converts to IMC before substantial EM damage inside of the joint. The general expectation is that once the solder converts to IMC it will be immortal against EM damage such as EM-induced voids. However, as we can see in the resistance change graphs, the samples are failed even after full conversion of the solder joint to IMC. The failure analysis on the failed samples, even after full conversion to the IMC, will give us a better understanding of failure mode

in the following section.

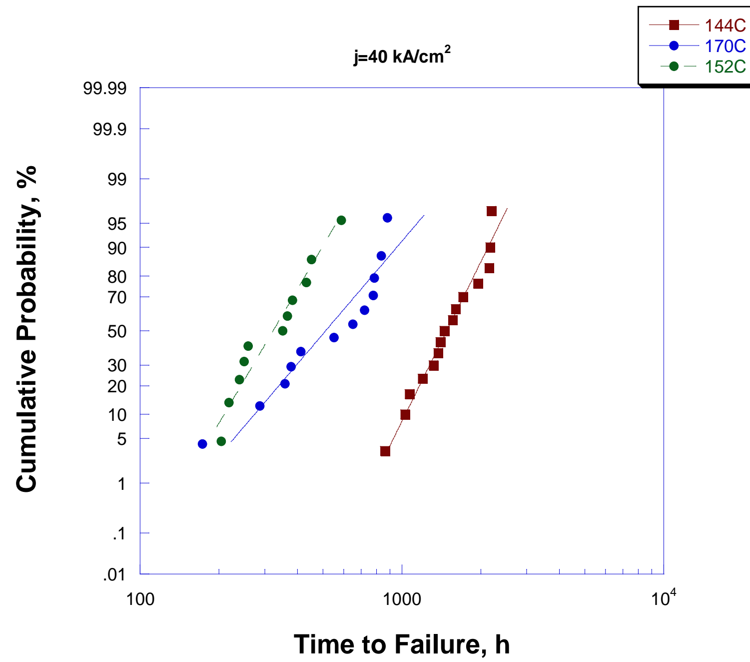


Figure 4-6. TTF of samples tested under 40 kA/cm^2 at two different temperatures as a function of normal cumulative probability.

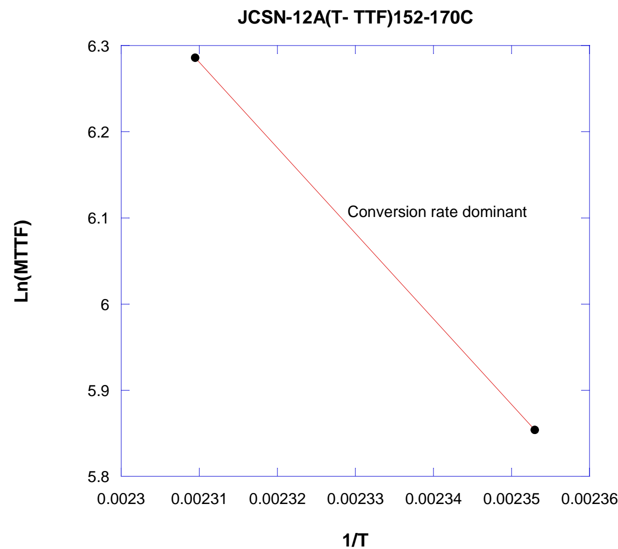


Figure 4-7. The MTTF of EM failure as a function of test temperature for samples tested under 40 kA/cm^2.

Another coefficient we need to adapt Black's equation to our experiment's failure kinetics is the current density exponent. Variation of MTTF with current density is plotted in Figure 4-8. This graph is useful to calculate the current density exponent of Black's equation. In a constant temperature, the current density exponent was calculated, and it is about 0.5 for 144ºC and 152ºC respectively. We can see that increasing current density reduces failure time of samples in both 144ºC and 152ºC EM test temperature. It is in accordance with black's equation prediction that higher current density accelerates TTF. Although the value of calculated current density exponent for micro solder joint is lower than the value reported for conventional flip-chip solder joint[58]–[62], the trend of its change is in accordance with previous reports for conventional solder joint. In other words, we can anticipate that increasing current density will facilitate failure in the micro solder joints.

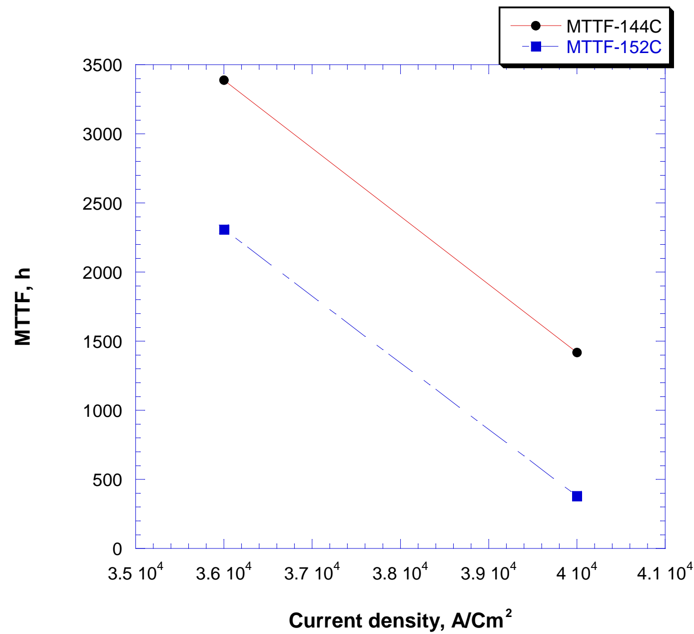


Figure 4-8. MTTF versus current density at 144°C and 152°C EM test condition.

4-1-2- **Samples with Ni layer at both solder interfaces**

According to the design of experiments, there were two test legs to investigate the effect of Ni layer addition on the failure mechanism. Figure 4-9 shows examples of electrical resistance change of joints tested at 160 and 170°C under 36 kA/cm^2 as a function of time for the samples with Ni layer at both interfaces of the solder joint and lead frame and Cu pillar. It is seen that samples tested at both temperatures show a similarity in resistance change until the point of the physical failure that is defined by an exponential increase in resistance. As evident in the plot, samples at both test temperatures show a first stage of resistance change characterized by a rapid 20-40% increase within the first ~200hrs. In the second stage, the rate of resistance increase is excessively low. This second stage is short-lived for the samples tested at 170°C because of runaway increase, which is a failure indication, but it is found to last to the limit of our testing time, 3000 hours, for samples tested at 160°C.

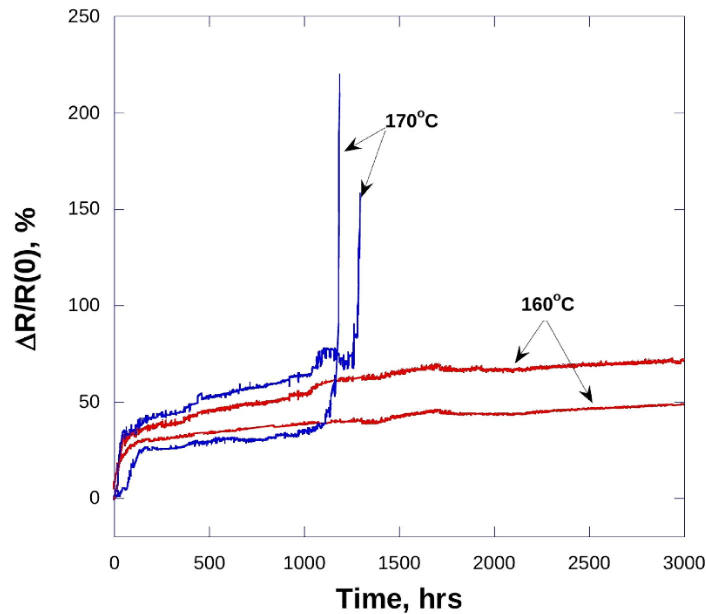


Figure 4-9. Resistance change percent during EM test (under 36 kA/cm^2) for the samples with Ni layer at both interface of the solder joint and lead frame and Cu pillar (elliptical geometry).

At first glance, the failure kinetics shown in Figure 4-9 may appear normal because based on Black's equation the EM failure rate is known to change exponentially with the temperature at a given current density and the absence of the failure at 160°C may simply be the result of a slower failure rate. Even if all samples are assumed to fail at 3000 hours, at the end of our testing time, the activation energy exceeds 2.5eV, which is far greater than any reported value for EM failure in Sn-based solder joints. More typical values for activation energy have been reported about 0.6-1.5eV[60], [62]–[65]. So, it seems there is a factor that delayed the failure of the micro solder joint in this particular joint arrangement. Our analysis of the failure rate, microstructural characterization, and also results from testing at few other conditions reveals that the delay in failure is not the result of slower kinetics at the lower temperature. In fact, it is related to the fundamental change in the EM mechanism in the micro solder joint. Analysis of the microstructure in the following section will provide more information about the delaying effect.

4-1-3- **Samples without Ni layer at solder interfaces**

One test leg of samples without interfacial layer was tested at 170ºC under 11 A (36 kA/cm^2) current load. The resistance changes graph versus the EM testing time is plotted in Figure 4-10. This graph shows that the resistance of the samples reached a certain level and no considerable change happened after that level. The constant level of resistance change, which is also called resistance saturation stage[66], [67], can be associated with the fact that full of the solder is converted to IMC. As the microstructure of reflowed sample before EM test is shown in Figure 3-6, a very thin layer of solder material remained in the middle of Cu-Sn IMC. As a result, it can be expected that remained solder material, converts quickly to IMC during EM test. Then, a fully converted solder to IMC can stay with negligible resistance change without showing any failure due to EM damage. Then, this constant level of resistance change was expected due to the fast reaction of Cu and Sn that forms the IMC joint.

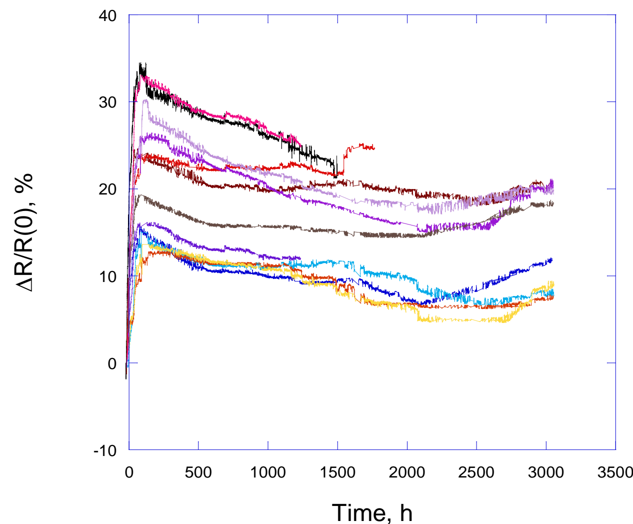


Figure 4-10. Resistance change percent during EM test (under 36 kA/cm^2) for the samples without Ni interfacial layer pillar (elliptical geometry).

4-2- Failure analysis of EM tested elliptical joint

4-2-1- Samples with Ni layer at solder/LF interface

To better understand the failure mechanism in the micro solder joints, especially the ones responsible for unique and unusual failure behaviors shown in Figure 4-4, a large number of failed samples tested at various conditions were subjected to microscopic characterization. This effort enabled us to find consistent features that are in support of the failure mechanisms proposed in our study. The cross-section microstructure of some representative samples, which were tested under 36 kA/cm^2 at 144ºC, 152ºC, 160ºC, and 170ºC, are shown in Figure 4-11 through Figure 4-14.

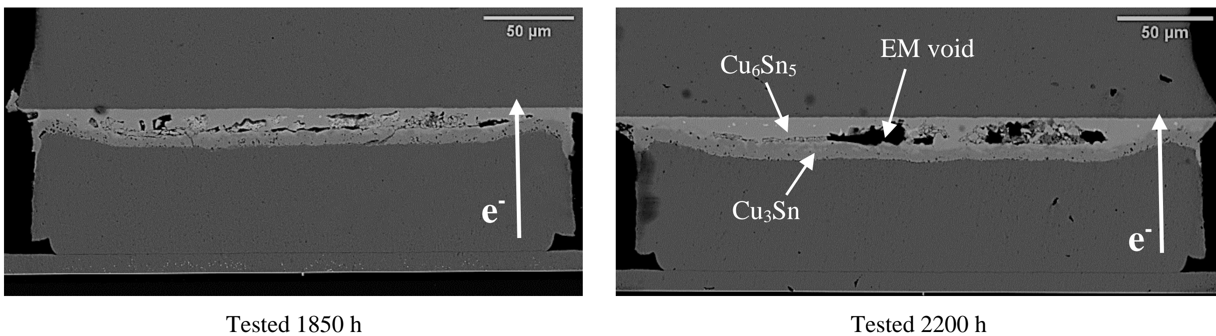


Figure 4-11. Cross-sectional SEM micrographs of samples (elliptical geometry) after EM testing under 36 kA/cm^2 at 144ºC.

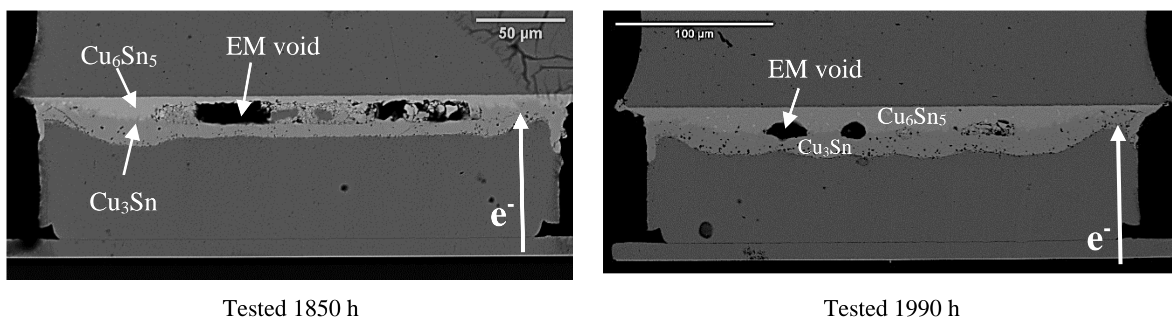


Figure 4-12. Cross-sectional SEM micrographs of samples (elliptical geometry) after EM testing under 36 kA/cm^2 at 152ºC.

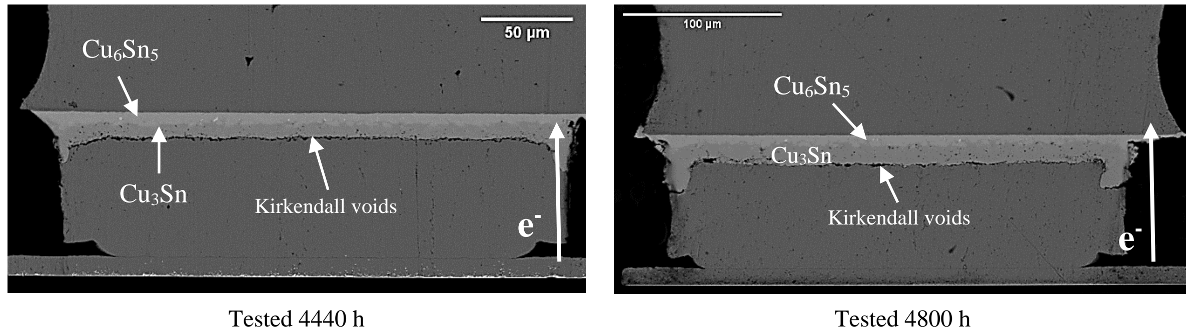


Figure 4-13. Cross-sectional SEM micrographs of samples (elliptical geometry) after EM testing under 36 kA/cm^2 at 160°C.

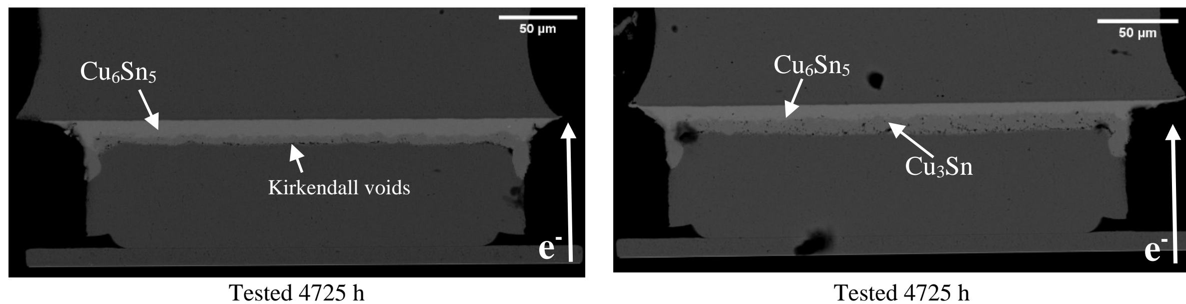


Figure 4-14. Cross-sectional SEM micrographs of samples (elliptical geometry) after EM testing under 36 kA/cm^2 at 170°C.

According to these microstructure images, the samples tested at a lower temperature like 144°C and 152°C show EM void inside of micro solder joint, but cross-sectional SEM image of samples tested at a higher temperature like 160°C and 170°C showed full conversion of solder material into IMC without substantial EM void inside of micro solder joint. It needs to mention that the failure has not happened yet for the samples tested at 170°C as Figure 4-14 illustrated microstructures of solder joints after EM test. In the case of samples tested at lower test temperature, it can be seen that the majority of voids trapped inside of the joint are formed at the original interface between Cu pillar and Sn solder. This occurs because EM force directed from Cu pillar (cathode) to LF (anode) direction causes Sn to migrate toward LF side producing counter-flux of vacancy to accumulate at Sn/Cu pillar interface. As it is noted, the failure type with more trapped voids in the joint is more prevalent at a lower temperature, which is consistent with the

failure mechanism we propose for the unusual temperature dependence of EM failure kinetics in Figure 4-4. At higher test temperature, resistance change graphs showed runaway failure, but the damage is not happened inside of solder joint due to EM void. Figure 4-13 shows that a discontinuity line between the solder joint, which is fully converted to IMC, and the interface of Cu pillar and solder is the location of failure. Since the failure location is not occurred inside of the solder joint, further microstructure investigations required to be done. In order to probe this failure mode, cross-sections of the solder joint were prepared at different locations for capturing scanning electron microscope (SEM) images. The locations that each cross-section was prepared are depicted in Figure 4-15.

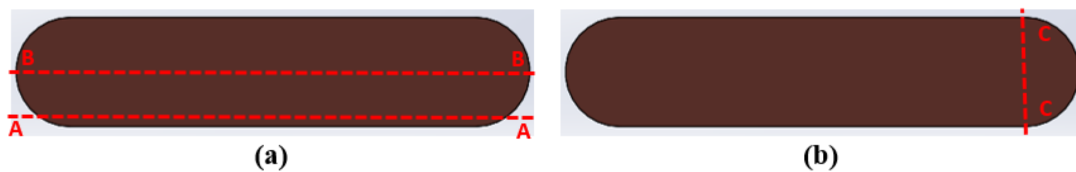


Figure 4-15. Top view of the micro solder joint (elliptical geometry) that showing the locations cross-sectional cut prepared.

Figure 4-16 shows the cross-sectional image of the micro solder joint, which is prepared from the AA location in Figure 4-15(a). As is illustrated, the deep growth of the IMC toward the Cu pillar is occurred. Since there is a Ni diffusion barrier layer at the lead frame interface, the direction of IMC growth is limited toward the Cu pillar side only [36]. In addition, EDS analysis is revealed the IMC consists of two phases, which are Cu_6Sn_5 and Cu_3Sn, while the majority of the extended phase toward the Cu pillar is Cu_3Sn. Initially, we thought that this amount of IMC growth happened entirely within the volume of the solder joint, and the consumption of the Cu pillar by the vast growth of the IMC is the main reason for the joint failure. However, by further grinding and reaching to the middle of the joint, i.e., BB location in Figure 4-15 (a), the thickness of the IMC toward the Cu pillar decreased as it is shown in Figure 4-17. As we can see in this image, the Cu_3Sn is not grown as extensive as happened at the surface of the joint. In fact, the difference between these two cross-sectional microstructures suggests that the extensive growth of the IMC at the surface occurred because of enhanced surface interdiffusion of Sn and Cu. In general, we know that the diffusion rate at the surface is higher than that of the grain boundary and the lattice diffusion (i.e. $D_{surface} > D_{gb} > D_{lattice}$)[68]. The downward scaling of solder joints, such as

the micro solder joint, facilitates the short circuit diffusion such as surface diffusion, and this diffusion path has a significant role in the diffusion process. Furthermore, as we can see in Figure 4-16 some scattered voids within the surface-grown Cu_3Sn phase. The formation of these voids is attributed to an unequal interdiffusion of Cu and Sn, and they have been named Kirkendall voids in previous studies[4], [69]–[76]. Basically, an insufficient lattice shift, leading to the super-saturation of excess vacancies in the diffusion couple, causes Kirkendall void formation[76]. In the present case, unbalanced surface interdiffusion of Cu and Sn through Cu_3Sn has occurred, and scattered voids are related to this unbalanced interdiffusion. If these voids become linked together, they can create separation at the interface, which is occurred in the middle of the solder joint (see Figure 4-17). Also, the Kirkendall voids within the IMC can greatly deteriorate the mechanical properties of solder joints.

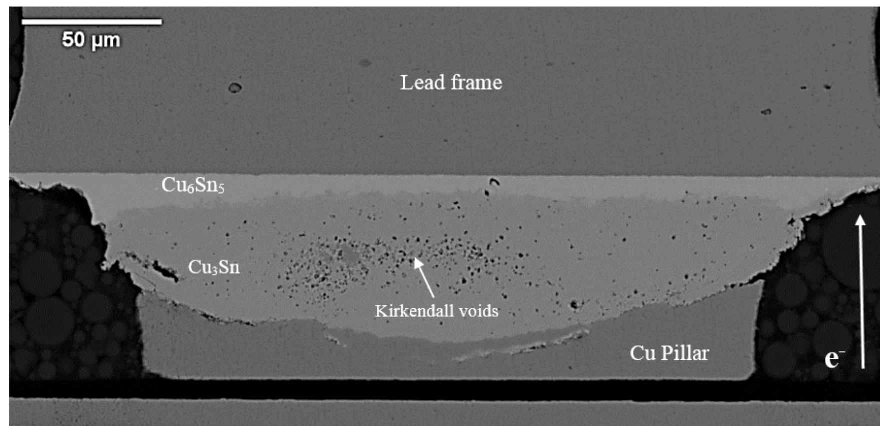


Figure 4-16. SEM image of the cross-section prepared at AA location of sample (elliptical geometry), which is shown in Figure 4-15(a), after EM test under 36 kA/cm^2 at 160°C .

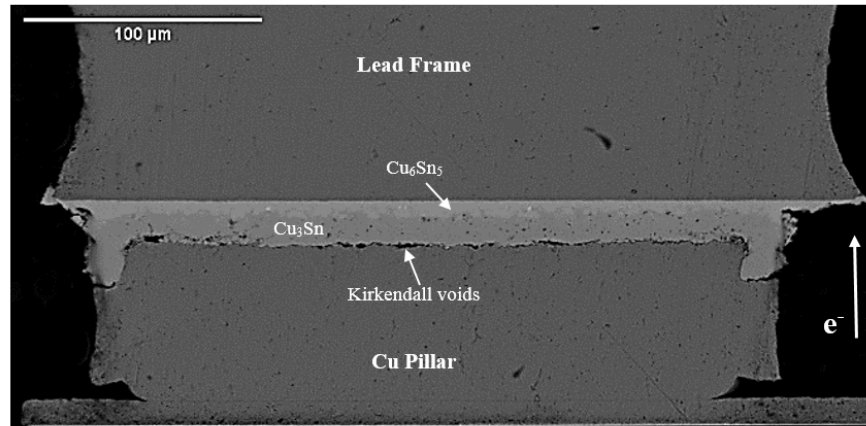


Figure 4-17. Figure 1. SEM image of the cross-section prepared at BB location of sample (elliptical geometry), which is shown in Figure 4-15(a), after EM test under 36 kA/cm^2 at 160°C.

As mentioned above, a discontinuity along the interface of the Cu pillar/ Cu_3Sn formed due to the linking of Kirkendall voids, and the resulting gap separated the Cu pillar from the IMC. In fact, unbalanced interdiffusion of species in the matrix of Cu_3Sn is the source of flux divergence. Kirkendall voids form when the diffusivities of counter diffusing elements are different[77]. In our case, the extensive growth of Cu_3Sn due to surface diffusion created a more available IMC matrix for the interdiffusion of atoms. The diffusivities of Cu and Sn are unequal in Cu_3Sn that led to void formation inside of Cu_3Sn because the diffusivity of Cu is higher than Sn in Cu_3Sn, according to previous studies[78]–[83]. General observations of micro-sized solder joints showed that Cu_6Sn_5 and Cu_3Sn IMCs form sequentially, and Kirkendall voids will likely form in the Cu_3Sn layer or at the interface between Cu_3Sn and Cu[79], [84]–[86]. These Kirkendall voids have not been observed in the Cu_6Sn_5 intermetallic compound because the interdiffusion of both Cu and Sn in the Cu_6Sn_5 is very limited[48]. The values of Table 4-1 indicate that diffusion of Cu is faster than Sn in Cu_3Sn, while of similar speed in Cu_6Sn_5.

Essentially, the difference in diffusion coefficients of Cu, D_{cu}, and Sn, D_{Sn}, in the Cu_3Sn will cause a vacancy flux in the matrix i.e., Cu_3Sn. The vacancy flux in Cu_3Sn, J_v,Cu_3Sn, is given by [82],

$$J_{v,Cu3Sn} = -(J_{Cu,Cu3Sn} - J_{Sn,Cu3Sn}) = (D_{Cu,Cu3Sn} - D_{Sn,Cu3Sn})\frac{\partial C_{Cu,Cu3Sn}}{\partial x}$$

Table 4-1. Intrinsic diffusion coefficients of elements in different phases[83].

Phase	Element	D(m^2/s), 170 ºC	reference
Cu	Cu	$1.07*10^{-29}$, $3.46*10^{-29}$	[78]
	Sn	$3.98*10^{-26}$	[79]
Sn	Cu	$1.06*10^{-9}$ (//c), $3.04*10^{-11}$ (⊥c)	[80]
	Sn	$1.81*10^{-16}$(//c), $4.43*10^{-16}$ (⊥c)	[78]
Ni	Ni	$8.95*10^{-38}$, $1.61*10^{-37}$	[78]
Sn	Ni	$1.47*10^{-8}$(//c), $7.73*10^{-11}$ (⊥c)	[81]
Cu_3Sn	Cu	$5.12*10^{-16}$	[82]
	Sn	$1.46*10^{-16}$	[82]
Cu_6Sn_5	Cu	$9.42*10^{-16}$	[82]
	Sn	$9.44*10^{-16}$	[82]
Ni_3Sn_4	Ni	$1.36*10^{-17}$	[82]
	Sn	$6.81*10^{-18}$	[82]
//c parallel to c-axis; ⊥c perpendicular to c-axis			

During high temperature current stressing of a Cu/Sn/Ni/Cu microbump, the solder material first converts to the Cu_6Sn_5 due to the interaction of Cu and Sn, then the Cu_6Sn_5 will convert to Cu_3Sn at the expense of more Cu diffusing toward to the joint. In other words, Cu can diffuse through the IMC and react with Sn, and at the same time, Sn can diffuse through the IMC and react with Cu. Since Cu diffusion is several times faster than Sn diffusion through the Cu_3Sn[87], a vacancy flux forms towards the Cu during the reaction[45]. When the number of Kirkendall voids increases and they accumulate near the interface of Cu_3Sn/Cu pillar, they will merge and create a separation between the solder joint and Cu pillar that eventually results the failure. This failure mode, which occurred at a high temperature EM test, is enhanced by EM but the mechanism is completely different from conventional EM voiding damage. Some previous studies [36], observed the Kirkendall void formation in solder joints under the annealed test condition (i.e., without current stressing), but the difference is that EM accelerates interdiffusion of Cu and Sn and Kirkendall void formation will occur faster. EM is enhanced the growth of IMC specifically Cu_3Sn due to short circuit diffusion i.e., surface diffusion and it makes a reasonable condition for unbalanced diffusion of species within the IMC. As a result, in the case of samples tested under EM test conditions, this type of failure due to interface separation can occur earlier than samples under only thermal annealing conditions.

Figure 4-18 shows the cross-section view that is prepared in the perpendicular direction of the solder joint's length i.e. CC location in Figure 4-15(b). As we can see, this image confirms that the surface diffusion occurred at both sides of the joint, but IMC growth in the middle of the joint

is not the same extend of growth at the surface of the solder joint. Besides, the accumulation of Kirkendall voids at the interface of the Cu pillar and Cu_3Sn is clearly visible. Extensive characterization of the failed joint led to the conclusion that the failure kinetics contains two-stage: at the first stage the micro solder joint is converted to IMC, and subsequent consumption of the Cu pillar by the growth of IMC results in Kirkendall void formation. In fact, surface diffusion of Cu and Sn enhanced the rate of IMC formation prior to void formation inside of the solder joint.
The graph that shows the resistance changes versus the time of EM testing (Figure 4-1) is in agreement with the two-step failure mechanism. The initial conversion of the solder material to the Cu_6Sn_5 caused electrical resistance of the joint to increase. Subsequently, we do not see a considerable change in resistance until a runaway rise occurred. This second resistance increase, where the change in resistance rapidly increases, is associated with the coalescence of Kirkendall voids and the thereafter formation of a discontinuity at the interface of Cu pillar/Cu_3Sn. Since this discontinuity created a gap at the interface like an open circuit failure, it can be responsible for the resistance rise at the second stage of resistance change.

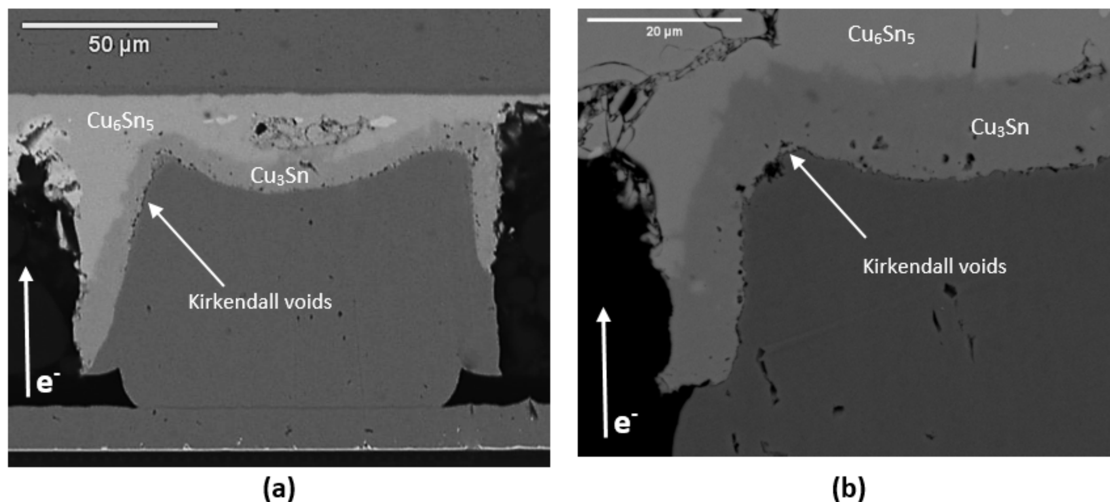


Figure 4-18. SEM image of the cross-section prepared at CC location, which is shown in Figure 4-15(b), after EM test under 36 kA/cm^2 at 160ºC.

For the samples tested at higher testing current (12 A equal to 40 kA/cm^2), failure analysis was performed, and cross-section images of the samples are shown in Figure 4-19 through Figure 4-21. As Figure 4-19 illustrates, EM voiding damage caused solder joint failure for the samples

tested at a low range of test temperature similar to the samples tested at this range of temperature with lower current density (36 kA/cm^2). In fact, EM of Sn before conversion to IMC leads to void formation inside of micro solder joint. On the other hand, in the case of samples EM tested at higher temperatures, the growth of IMC toward Cu pillar is taken place more extensively for the samples EM tested at this test current load. The failure occurred while IMC penetrated deep into the Cu pillar and IMC reached the Cu metallization trace underneath of Silicon. The unsymmetrical feature of IMC growth might be because of current crowding that causes IMC growth more in the region poses more electron flow density. This current crowding effect facilitated more EM induced atomic flux that accelerated IMC formation. The right side of cross-section image in Figure 4-20 and Figure 4-21 is the place electrons enter into the solder joint and generally, electrons choose the shortest path to flow through a conductor. In other words, this region carries the highest current density due to higher current load to the solder joint. As showed in Figure 4-7, 152°C is the temperature that failure kinetics changes the direction of linear trend due to change of dominant factor that governs failure mechanism. The comparison of microstructures of samples tested at 152°C shows both failure mechanism, EM voiding in the joint and exaggerated IMC growth, have occurred (see Figure 4-20). The observations of this test temperature revealed that samples failed at a shorter testing time has an indication of EM void inside of the solder joint. On the other hand, the cross-sectional microstructure of samples failed at longer time shows deep IMC growth as a root cause of failure due to current crowding.

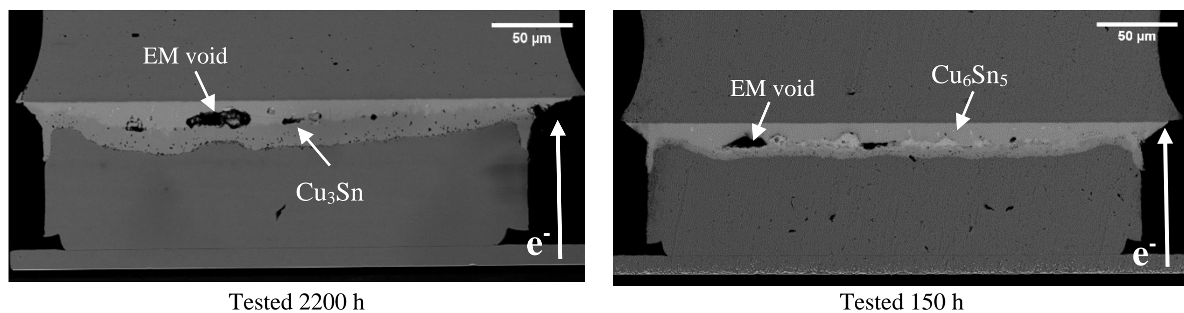


Figure 4-19. Cross-sectional SEM micrographs of samples (elliptical geometry) after EM testing under 40 kA/cm^2 at 144°C.

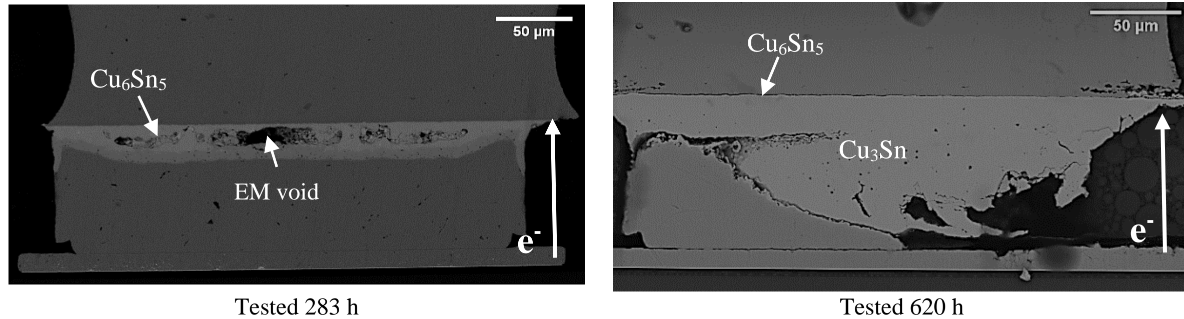


Figure 4-20. Cross-sectional SEM micrographs of samples (elliptical geometry) after EM testing under 40 kA/cm^2 at 152ºC.

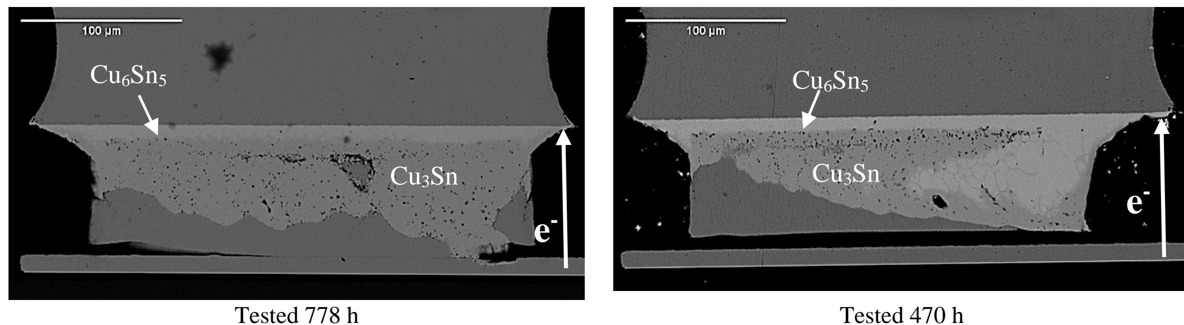


Figure 4-21. Cross-sectional SEM micrographs of samples (elliptical geometry) after EM test under 40 kA/cm^2 at 170ºC.

As mentioned above, the growth of Cu_3Sn accompanies by Kirkendall void formation due to unequal interdiffusion of Cu and Sn. Since higher current density results in the current crowding in the Cu pillar, the local joule heating effect around voids inside of Cu_3Sn contributes to the growth of IMC due to local higher temperature. In fact, unlike the samples tested at 11 A (36 kA/cm^2), which failure happens due to merge of Kirkendall voids at the IMC/pillar interface, the samples tested at 12 A (40 kA/cm^2) exhibit the failure mode by deep growth of IMC toward Cu pillar. The Kirkendall voids exist in both microstructure of samples tested at 11 A and 12 A, but its distribution inside of the IMC provides different failure modes. At 11A EM test load, Kirkendall voids can gradually align at the interface and create joint separation, but in the case of 12A EM test condition, the possible mechanism is that local joule heating at the voids area enhances Sn interdiffusion that led to more IMC growth toward Cu pillar. This accelerated IMC growth can be

a reasonable clue to explain why failure took place earlier in samples tested at higher current density.

As a summary of the unusual EM failure kinetics of the samples EM tested, we observed two modes of failure mechanism. The first is the kinetics of voiding by EM in the solder joint that is responsible for inducing critical damage, while the second is the rate of IMC growth in the joint. The factors affecting the kinetics of these two processes are not necessarily the same and scale differently with temperature. Specifically, the voiding kinetics is governed by the EM diffusivity of Sn atoms in Sn matrix $(Z^*D)_{Sn}$, while the IMC growth rate is governed more by either chemical diffusivity or EM diffusivity of Cu in Sn $(Z^*D)_{Cu}$. We believe that activation energy for voiding, $(Z^*D)_{Sn}$, is lower than the one for IMC conversion of Sn, $(Z^*D)_{Cu}$, at lower temperature and the conversion rate is dominant at higher temperatures. The EM failure then occurs less readily than what is predicted from the failure rate at low temperatures (where voiding rate is more dominant). This seems to explain the data in Figure 4-4 and the microstructural failure mechanism detailed above. It is important to note that the effect of failure governed by two competing processes would not be noticeable in the case of the conventional solder joint because excessively large dimensions of solder cause the effect of IMC formation to have negligible influences and failure to proceed without the competition. Moreover, our results showed that the variation of current density follows the similar behavior that is observed in previous EM failure kinetics studies. Meaning that the increase of current density will cause faster failure time in both cases of conventional solder joints and micro solder joints.

4-2-2- **Samples with Ni layer at both solder interfaces**

The clear difference in the joint microstructure characterized after EM testing at 160 and 170^oC can be seen from SEM micrographs shown in Figure 4-22. In samples tested at 170^oC, the joint microstructure contains well developed voids across the entire interface of the joint. The rest of the joint is mostly converted to Ni_3Sn_4 IMC. Except for a few exceptionally extended voids, the majority of voids in the joints are narrow and located along the cathode side of the joint. Since voids form by the collection of vacancies that flow opposite to the direction of EM, the voids forming at the cathode end implies that the failure is indeed induced by EM of Sn. Additional

evidence for Sn EM being responsible for voiding can be seen from the cross-sectional SEM micrograph in Figure 4-23. Note the presence of the remnant Sn phase located right next to the downstream side of the larger voids. Because the void open-circuits the Ni-EM path, the Sn phase survives and remains in the joint as scattered islands. On the other hand, no such voiding activity is seen in samples tested at 160ºC. While void does occur at the outer edges of the joint, no void is found in the inner area of the joint. The 160°C joint is found to be fully converted to Ni_3Sn_4 IMC without the remnant Sn phase seen in 170°C samples. Analysis of the microstructure suggests that the 160°C samples reach a condition of "immortality" due to full conversion of the joint to Ni_3Sn_4 IMC in which EM is practically inactive [88], [89].

Microstructural analysis of the EM tested samples is consistent with resistance data shown in Figure 4-9. The process of void nucleation and growth continues without impedance in the case of samples tested at 170ºC to the point of runaway failure that is characterized by an exponential growth of void due to increase in local current density and temperature. On the other hand, the failure process is interrupted by the full conversion of the joint to Ni_3Sn_4 IMC for the testing at 160ºC. This is well evidenced in the resistance data shown in Figure 4-9 where the resistance of samples tested at 160ºC shows a slow and small increase after the initial rise. According to the microstructural inspection, the initial rise in resistance corresponds to the early void formation caused by Sn-EM and seen mostly at the outer edge of the joint. The steady state increase in the resistance after the first rise is attributable to the continued conversion of Sn to Ni_3Sn_4 IMC. The small amount of resistance increase occurs with IMC growth because Ni_3Sn_4 has higher electrical resistivity than Sn and Ni; the electrical resistivities of Ni_3Sn_4, Sn, and Ni are known to be 28.8, 14.0, and 6.8 μΩ-cm, respectively[90].

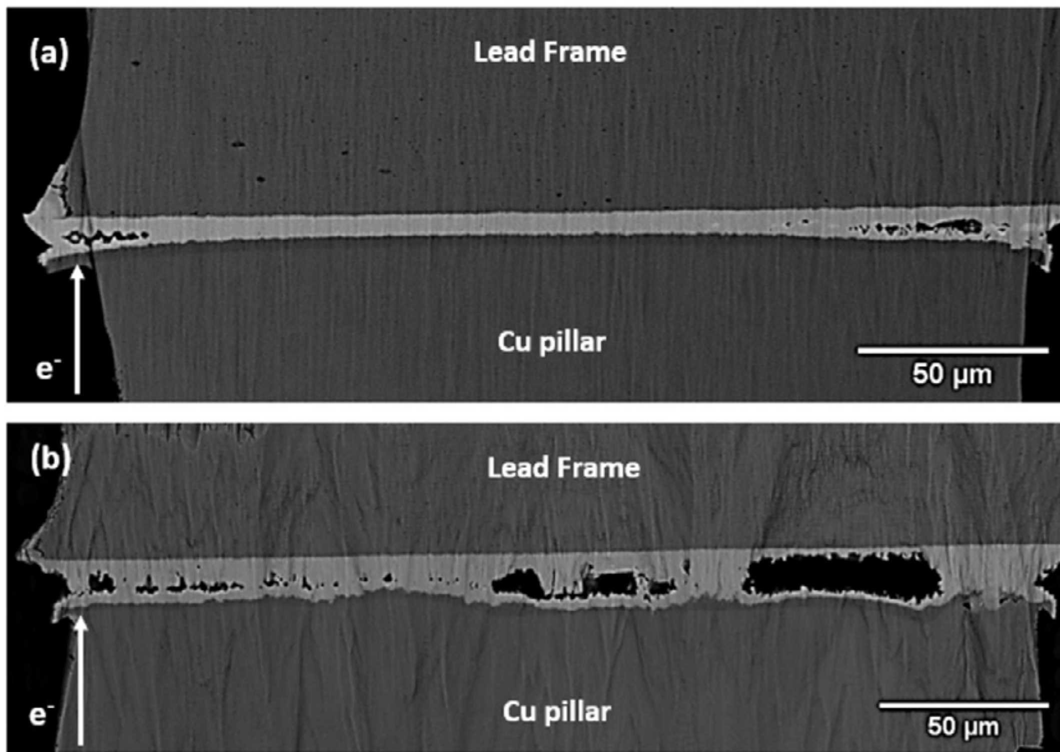


Figure 4-22. SEM micrographs showing the cross-sectional microstructure of samples tested at 160°C (a) and 170°C (b).

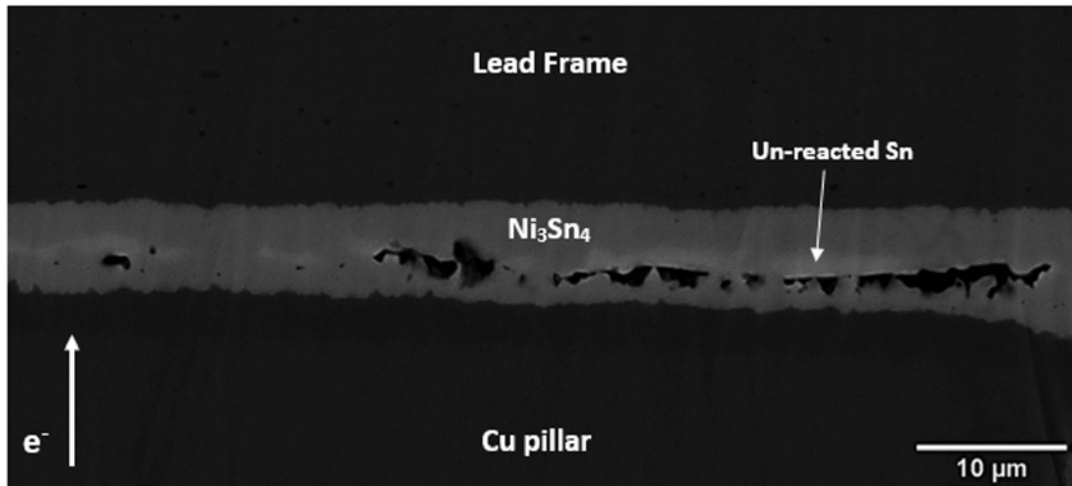


Figure 4-23. A SEM micrograph showing the cross-sectional microstructure of samples tested at 170°C. Note the presence of unreacted Sn phase in the joint.

It is not possible to explain both the EM induced microstructures in Figure 4-22 by a simple consideration of the kinetics competition between voiding and IMC growth. This mechanism may be consistent with the microstructural analysis of samples tested at 170°C, but not those tested at 160°C. One may argue that the IMC asymmetry in the samples tested at 170°C may be a result of the growth driven by Ni diffusion from the anode after the cessation of Ni-EM. However, time-lapse microstructure inspection of the samples tested at 170ºC present consistent evidence that the growth of IMC from the anode that results in the asymmetric pattern of IMC growth shown in Figure 4-22(b) and Figure 4-23 is the result of EM assisted Ni_3Sn_4 IMC growth. If EM assisted fast growth of Ni_3Sn_4 suppressed voiding at 160°C, then the joint should show the same IMC phase grown from anode to cathode. However, high resolution microstructural characterization reveals that such mechanism does not account for the IMC growth behaviors seen in our study. The anomalous evidence is presented in Figure 4-24, a cross-sectional SEM micrograph, and an EDS scan of Ni distribution across the joint. The microstructure of a sample tested for ~348hrs, Figure 4-24, clearly shows the symmetric growth of IMC. The same IMC growth pattern is found in a sample subjected to the same temperature for similar duration of time without current, as shown in Figure 4-24. The Sn phase remaining in the joint represents the growth front of the IMC phase at the time of test termination. Note that the growth of Ni_3Sn_4 does not show any sign of EM-induced bias in its growth direction. The growth seems to be of almost equal rate at both anode and cathode. The symmetric growth of IMC is supported by the EDS analysis shown in Figure 4-24 (b) that measures Ni content across the joint for three cases of EM testing times, 0, 348, and 1500 hours.

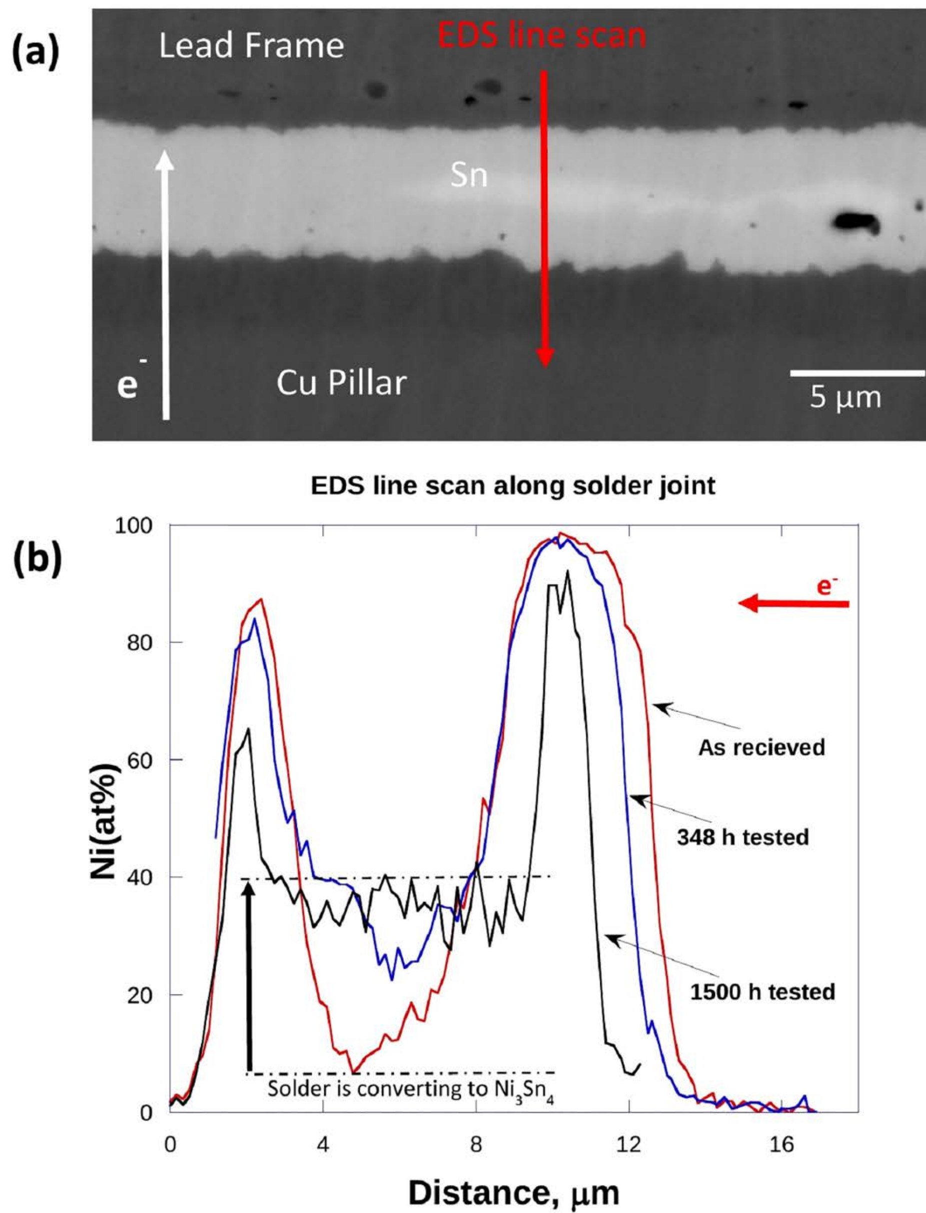


Figure 4-24. (a) SEM micrograph showing the cross-sectional microstructure of a sample after testing under 36 kA/cm^2 at 160°C for 348 hours (b) and the Ni distribution across the joint.

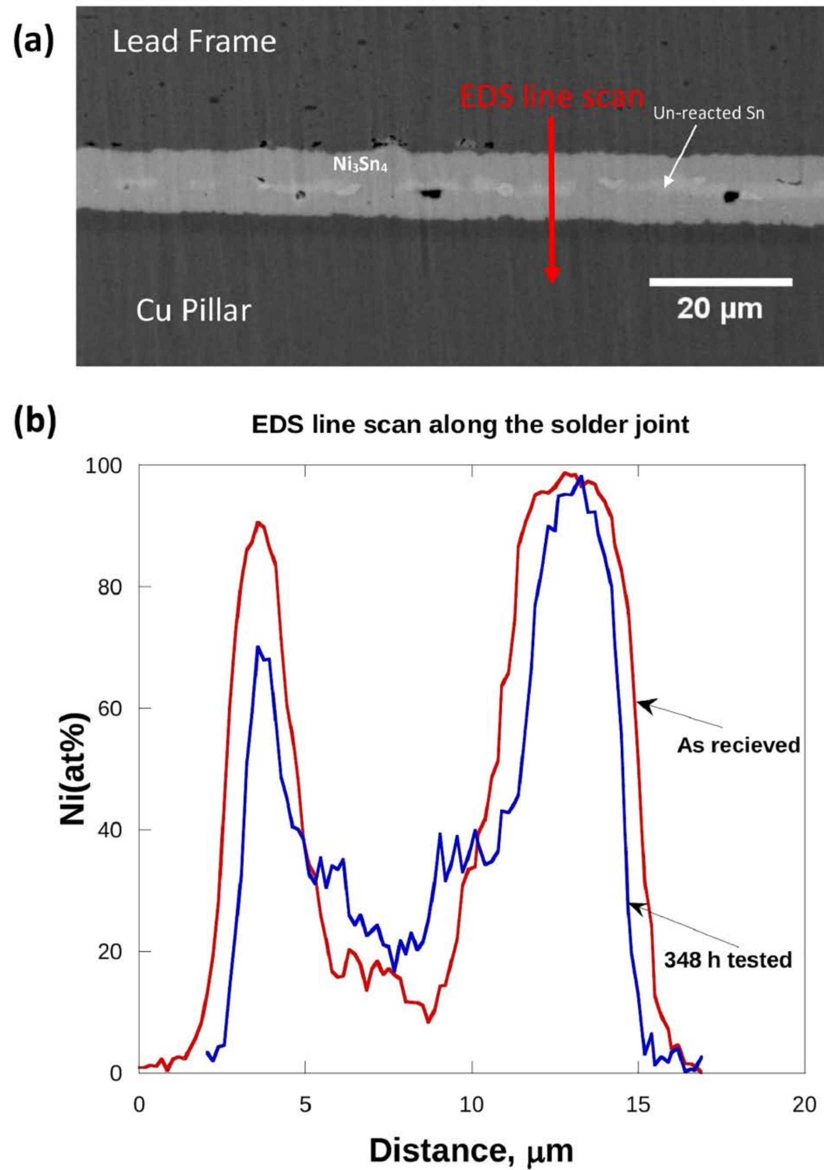


Figure 4-25. (a) SEM micrograph showing the cross-sectional microstructure of a joint after thermal aging at 160°C for 348 hours (b) and the Ni distribution across the joint.

A schematic representation of two different Ni_3Sn_4 IMC growth mechanisms is presented in Figure 4-26 as a summary of our observations. In samples tested at 170°C, the growth mechanism follows Figure 4-26 (a), meaning that IMC at the anode side preferentially grows. This is a classic case of an EM-driven IMC growth and is due to the EM of elemental Ni in the solder

matrix toward the anode. The existing IMC phase at the cathode dissolves to replenish the loss of Ni in the matrix while the IMC at the anode grows with the arrival of excess Ni. The second IMC growth pattern seen in our study follows the mechanism shown in Figure 4-26 (b) where no such biased growth occurs.

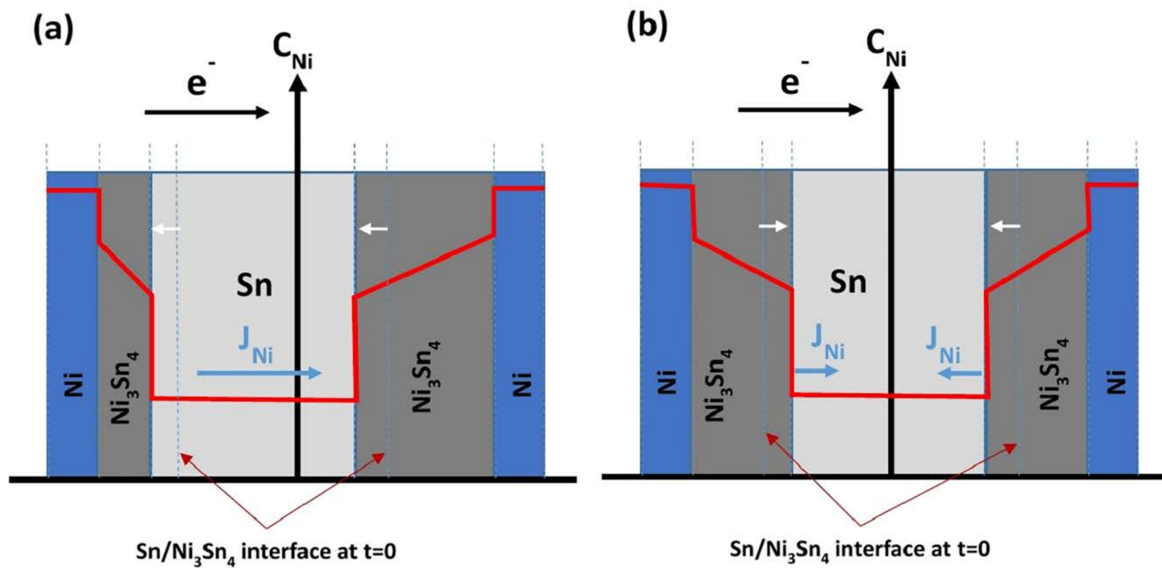


Figure 4-26. A schematic representation of two Ni_3Sn_4 IMC growth behaviors seen in this study.

As shown in the schematic mechanism, such growth is possible only when there is no EM force acting on IMC growth, meaning that the growth is directed only by the force of chemical diffusion. A chemical diffusion only mechanism seems improbable under our exceptionally high level of current density, and so the explanation for the microstructure is not possible without considering additional factors known to affect EM. The only possible way for EM to have a negligible impact on IMC growth in spite of samples subjected to high density current is when EM occurs under the influence of the back-diffusion forces created by a stress-gradient[45], [60], [67], [91]. According to the established theory, the total atomic flux in a system under EM force is determined by two competing forces, EM and stress driven backflow[3], [92]:

$$J = \frac{CD}{kT}\left(Z^{*}e\rho j - \frac{\Omega d\sigma}{dx}\right) \qquad (1)$$

where ρ, Ω, and σ denote the resistivity of host element, atomic volume, and hydrostatic pressure, respectively, while others have their usual meanings. When the EM force is completely

counterbalanced by the back-stress, the atomic flux vanishes, leading to the well-known critical "Blech length" condition of

$$(JL)_c = \frac{\Omega\Delta\sigma}{Z^* e\rho} \quad (2)$$

where L represents the thickness of the solder joint. When the system meets the condition of eq.(2), EM will no longer impact the microstructural development of the joint. The Blech length effect, however, arises only by EM of solvent, Sn in our situation, not by the solute. Yet, if the backflow effect is responsible for the absence of biased IMC growth at 160ºC, it must be that the back-stress force developed by Sn EM is acting to reduce the EM diffusivity of the Ni solute to nothing, $(Z^*D)_{Ni}\sim 0$. Figure 4-27 shows counter acting forces in a thin micro solder joint. It should be noted that the Blech effect only could overcome the EM flux where the buildup of stress gradient is sustainable to result in steady back flow flux.

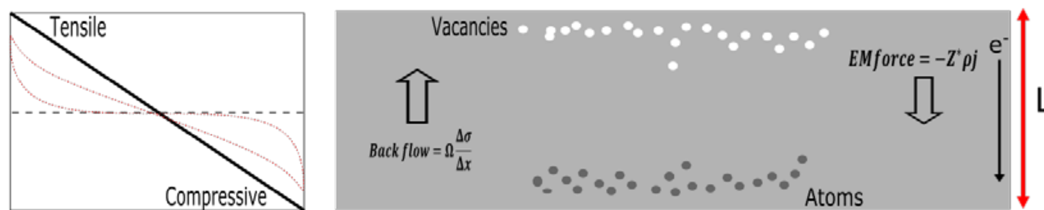


Figure 4-27. Schematic presentation of counteracting forces in a thin solder joint.

The existence of the Blech's length effect is well proven in the study of EM in thin metallic films, but such effect has not been proposed for solder joints except for a study by Hsu et. al[55], where the back-stress effect is assumed to exist from the observation of excessive time required for EM failure of micro joint when tested at current density below 15 kA/cm^2. We believe that back-stress effect does exist in low aspect ratio (thickness to length) solder joint when the joint is subjected to EM with mechanical constraints. One of the key parameters in eq.(2) affecting the back-stress is the level of hydrostatic stress. The hydrostatic stress is limited by the yield strength of the material, and SAC solder is an alloy with low yield strength, a few tens of MPa at elevated temperatures. In addition to the low yield strength, the geometric configuration of common solder joints does not allow the sustained existence of the stress. The low aspect ratio (thickness/length) of the solder joint permits the release of stress by the process of dislocation glide or creep, making the stress effect too small to observe. On the other hand, the solder joint used in our study, which

has a low aspect ratio, may provide the ideal condition of sustaining the hydrostatic stress beyond the yield strength and thus allowing the development of the back-stress sufficient to suppress the EM force both for Ni and Sn. This may also explain why voids are found to form at the outer edges of the joint, where the solder is thicker and close to the edge surface where stress relaxation by dislocation glide is active.

It may be simply thanks to the very low aspect ratio joint geometry in our study being unusually sensitive to the back-stress in the microstructural evolution. In fact, our estimation of the critical EM condition based on eq.(2) supports this possibility. For the solder thickness L~10μm, the critical current density, J_c, is estimated to be close to 40 and 34 kA/cm^2 at 160 and 170°C, respectively, when the known yield strength of the bulk SAC solder alloy at each temperature is used[93]. It is interesting to note that our test current density, 36 kA/cm^2, is lower than the critical density for 160°C but is close to the one for 170°C. This result suggests that the back-stress would provide complete protection against EM at 160°C while the protection may be partial at 170°C. The estimate seems to correlate reasonably well with the failure data, at least to the extent to suggest the back-stress as an important factor to consider in the failure analysis of the micro solder joint. The remaining question for future study is the mechanism by which hydrostatic stress is relaxed at 170°C despite the geometric constraint that hinders plastic deformation by dislocation glide. Stress relaxation by other processes such as creep is highly probable and deserves serious consideration. While the existence of the back-stress effect and the resulting suppression of Sn EM is reasonably well demonstrated in our study, its impact on Ni EM is not well understood and demands additional studies with careful analysis. In fact, understanding the mechanism of Ni-EM in Sn-based alloys is of growing interest due to its potential as an alloying element to enhance EM resistance of solder joints. Past studies on this subject present the generally agreed upon the result that the EM rate of Ni is higher than that of Sn in the solder matrix. Our observations, however, suggest that it is not always the case. The solder joint microstructures developed by EM at 160°C shown in Figure 4-22 through Figure 4-24 clearly suggest that EM diffusivity of Ni can be vanishingly small, $(Z^*D)_{Ni} \sim 0$, evidenced by the growth of Ni_3Sn_4 IMC without noticeable bias in the growth direction. On the other hand, the time-lapse tracking of IMC growth in samples tested at 170°C shows that the EM diffusivity of Ni is sufficient to produce exaggerated growth of IMC at the anode side. These two seemingly contradicting behaviors of Ni-EM may be the result of

varying magnitude of the back-stress developed in the Sn matrix with temperature. In the case of 160ºC EM, the driving force for Ni-EM, namely by Z_{Ni}*ej, is counterbalanced by the back-stress, so that $(Z^*D)_{Ni}$~0. Note that $(Z^*D)_{Ni}$~0 is a result of Z_{Ni}*~0 and that D_{Ni} is maintained at a reasonably high level. This allows IMC to grow fast but only by the process of chemical diffusion. The reduced back-stress due to Sn EM at 170ºC leads to just a partial countering of EM force, making $(Z^*D)_{Ni}$ be non-zero, resulting in biased IMC growth. The finding of Ni EM influenced by the back-stress in Sn solder is not so surprising because Ni atom would be subjected to the same stress gradient via elastic interaction with Sn. What is surprising is the indications that the back-stress may impart a greater impact on Ni than Sn. This seems to be the case because, with no sign of asymmetric IMC growth that would signify Ni EM at 160°C, Ni EM appears to be almost completely absent from the start.

An equally interesting and potentially important result from the study of Ni_3Sn_4 IMC growth is the finding suggesting the absence of anisotropy in EM diffusivity of Ni. It is reported that Ni diffusivity along the [001] axis of Sn grain is orders of magnitude higher than the other axes due to interstitial diffusion. The anisotropy in diffusivity is expected to lead to highly accelerated EM diffusivity and growth of Ni_3Sn_4 phase in Sn grains where the EM direction is aligned with [001] axis. Nonetheless, microstructural characterization of samples tested both at 160 and 170ºC does not reveal any indication of Ni EM anisotropy affecting Ni_3Sn_4 IMC growth. As is shown in Figure 4-22 through Figure 4-25, Ni_3Sn_4 IMC is found to grow at a more or less uniform rate across the whole joint. Even though the Sn grain orientation found using EBSD (electron back-scattered diffraction) clearly suggests the existence of [001] grains as shown in Figure 4-28, there are no particular segments of the joint with features suggesting faster growth IMC. The absence of the anticipated anisotropy effect in our samples may suggest that the enhanced EM of Ni along [001] axis occurs when the solder is relatively free of stress. Under compressive stress, the open space along [001] axis of Sn may deform sufficiently to shut down the interstitial path. In this regard, it is important to note that the solder in our study is likely to be placed under a certain level of compressive stress during EM testing because of the joule heat induced expansion of solder against surrounding constraint.

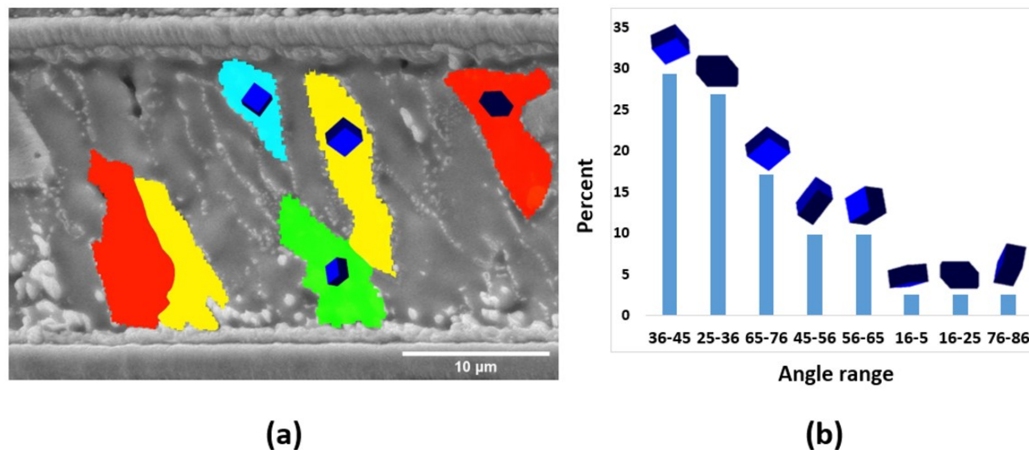


Figure 4-28. An image showing the EBSD orientation map of solder at as-received condition (a) and (b) a plot of displaying statistical distribution of angle between c-axis of Sn and EM direction.

4-2-3- **Samples without Ni layer at solder interfaces**

The last group of samples that EM tested are the solder joints without interfacial diffusion barrier (Ni) layer. A cross-section image of sample EM tested at 170ºC with 36 kA/cm^2 is shown in Figure 4-29. This cross-section image shows that the solder joint is fully converted to IMC. Although there is EM induced void inside of the solder joint, in the region that the solder is thicker, the damage is not substantial to induce joint failure. As shown in resistance change graphs (Figure 4-10), the constant level of the resistance changes after the initial increase is associated with the fact that IMC is immortal against more EM damage. Hence, cross-section image of tested samples verifies that full conversion of the solder joint to IMC makes the joint immune against EM. Since the solder thickness is very low and the joint does not have Ni interfacial layer, a sizable fraction of the solder already converted to IMC after reflowing and remained solder transformed quickly to IMC during EM test. Basically, Ni–Sn reaction rate is much slower than that of Cu–Sn[94]. For example, a Ni interfacial layer in the Cu-Sn system may act as a diffusion barrier where no further Cu_3Sn formation can occur[95], [96]. Therefore, since in this group of the samples there is not Ni interfacial layer, IMC conversion occurred faster than other groups of samples with Ni layer. As mentioned before, the interaction of the solder joint with the Cu pillar and lead frame is the reason that the solder joint is mostly converted to IMC. This interaction continues during EM test and Cu

and Sn can diffuse together even if the solder joint is fully converted to IMC. The continuation of Cu and Sn interdiffusion is caused that initial formed IMC (Cu_6Sn_5), which has a higher content of Sn, converted to Cu_3Sn that is Cu rich phase. In fact, Cu_6Sn_5 is the source of Sn for interdiffusion toward Cu at the pillar and lead frame side. In addition, there is a discontinuity at the interface of the joint with the lead frame. This discontinuity is the separation created by Kirkendall void due to the growth of Cu_3Sn toward the lead frame, but the rate of gap creation is quite slow because both interfaces of the solder joint can have Cu, Sn interaction without any diffusion barrier.

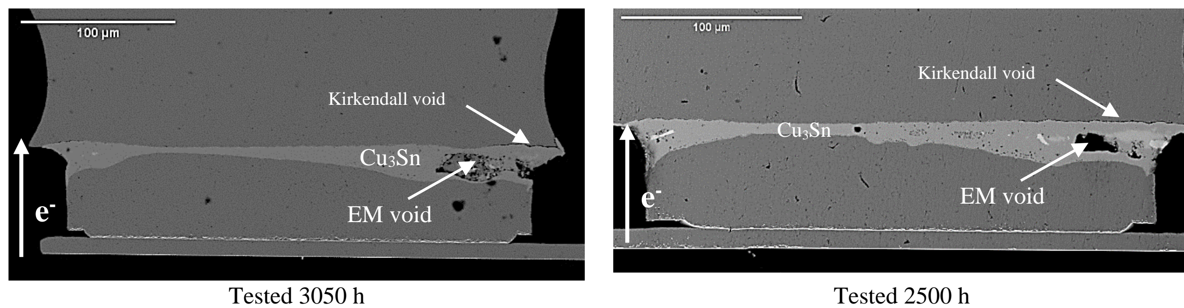


Figure 4-29. Cross-section SEM image of the sample (elliptical geometry) EM tested at 170°C.

4-3- Tracking electric resistance change (Cylindrical joint geometry)

The resistance changes of samples with cylindrical shape solder joint are plotted in Figure 4-30 for the samples tested at 3A and 4.2A (this amount of current produce a current density equal to 36 and 51 kA/cm^2 respectively).

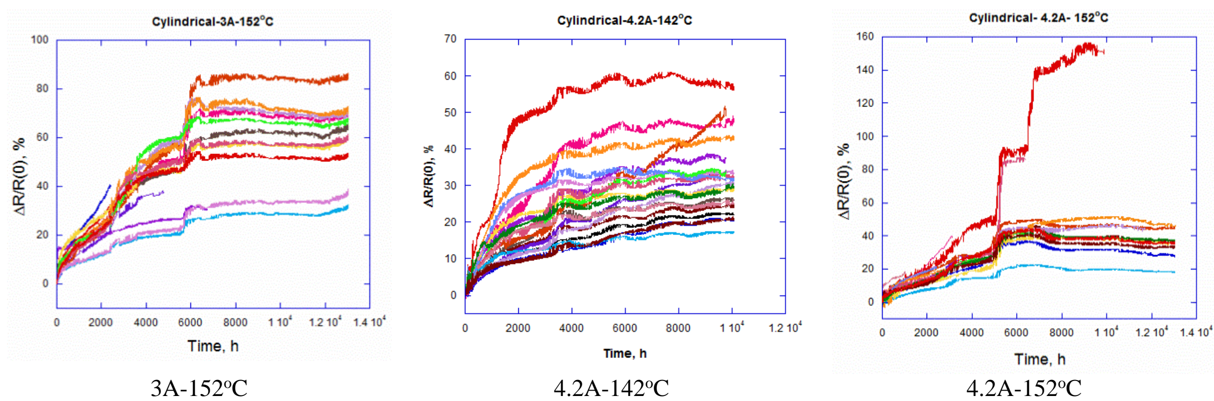


Figure 4-30. Resistance change of EM tested samples (cylindrical geometry) at different current loads.

As it was expected, based on the results for the same joint arrangement and current density of elliptical joint geometry, samples did not show failure, and the joint resistance remained at a constant value after the initial rise. This resistance change trend remains constant even for the sample tested under 4.2A (51 kA/cm^2 current density). Although there are few outlier samples that showing high resistance change, most of the samples did not show failure at this test condition. The condition of experiments was designed to characterize the factors contributing to the EM failure kinetics of the joint, most notably the activation energy and current density exponent, but as graphs of Figure 4-30 suggest the failure have not occurred even after 14000 hours of EM testing time. Then, we could not calculate the MTTF of each test leg for implementing to failure kinetics model. Unlike the elliptical shape samples, Since it is required to have at least two MTTF values for calculating parameters of the failure kinetics model, we were not able to calculate the constants of the kinetics equation to anticipate failure time because most of the test legs of cylindrical shape joints did not fail. However, microstructural studies of EM tested samples may give some insights in terms of microstructure changes and IMC formation.

The last test leg of cylindrical joint geometry was carried out under an exceptionally high amount of current density which was 67 kA/cm^2 (5.5A). Figure 4-31 shows the resistance changes graph of samples tested at this level of current load. In this test condition, the initial resistance rise occurred quickly, and we do see a runaway increase after the constant level stage. Apparently, this observation is an indication of failure in the joint, but we need to do failure analysis to investigate the failure mechanism.

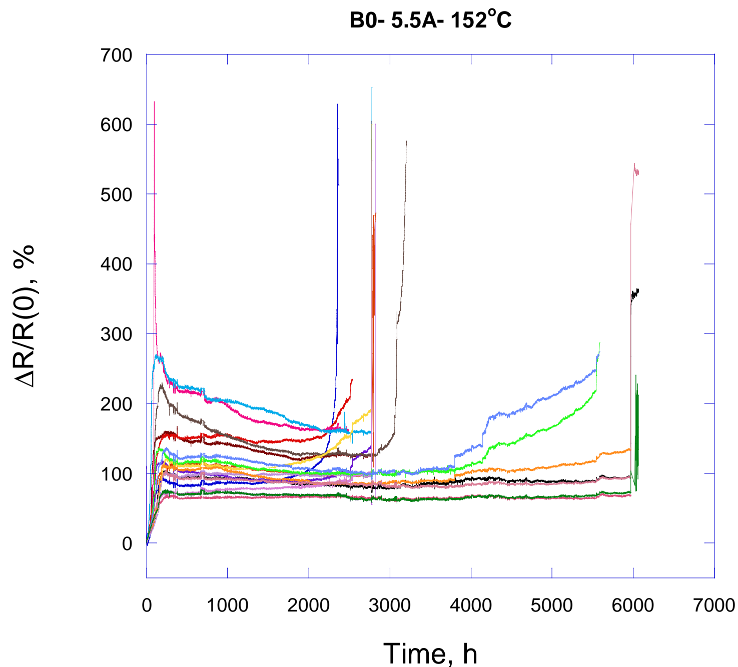


Figure 4-31. Resistance changes of cylindrical shape samples EM tested at 5.5A and 152°C.

4-4- Failure analysis of EM tested samples (Cylindrical joint geometry)

In the case of samples tested at 3 A and 4.2 A, there was not any considerable resistance change other than a slight increase due to the IMC formation. As illustrated in Figure 4-32, the solder joint is completely converted to the intermetallic compounds (IMC). The sequential IMC formation clearly is shown in Figure 4-32 where the microstructure of the sample after an elapsed time of the EM test shows the microstructural evolution of the solder joint. These results are expected according to the sequence of IMC formation, wherein Cu_6Sn_5 forms first and then converts to Cu_3Sn by further interaction of Cu-Sn due to chemical diffusion and EM atomic flux. While the entirety of the joint is converted to Cu_3Sn phase, there was not any sign of failure in terms of microstructural change and electrical resistance, meaning that a full IMC joint is immortal against EM damage at this level of current density i.e., 36 kA/cm^2. Furthermore, the Kirkendall

voids within the Cu_3Sn have not aligned at the interface to create a discontinuity. In fact, since the joint arrangement does not have a Ni diffusion barrier at the interfaces, the interaction of Cu and Sn is not limited to the Cu pillar face, unlike the samples with a Ni layer at the LF end, which showed failure due to the alignment of Kirkendall voids at the interface. We can see some partial void alignment occurred at the LF/joint interface, but it happened after an extended period of testing time i.e., 13000 h. That said, it is fair to state that the joint with this geometry (cylindrical) and arrangement is persistent against this level of EM load (36 kA/cm^2). Moreover, in all current stressing test conditions, we can clearly observe that conversion of Cu_6Sn_5 to Cu_3Sn eventually caused the extension of the joint thickness due to the growth of the IMC. The overall thickness of the fully Cu_3Sn joint is higher than the thickness of Cu_6Sn_5 and solder joint due to further interaction of Sn with Cu taking place at both ends of the Cu pillar and LF.

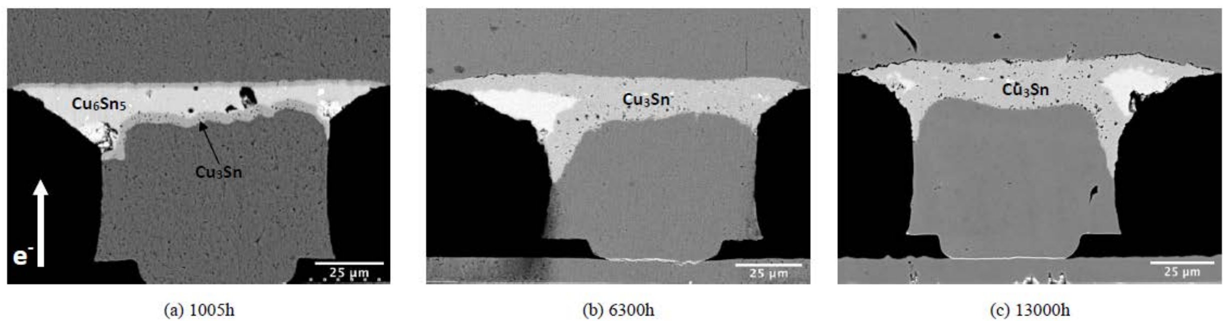


Figure 4-32. Cross-sectional view of EM tested samples under 36 kA/cm^2 at 152°C.

On the other hand, the failure analysis of the sample that is EM tested at 5.5A shows an interesting microstructure when a runaway increase occurred in the resistance changes plot. We can see in Figure 4-33 that the IMC phase has developed into the Cu pillar, and eventually delamination occurred at the place where the Cu pillar is connected to a Cu trace. Besides the formation of voids inside of the solder joint, the region shows an extension of an IMC phase into the Cu pillar, a unique phenomenon caused by an extreme level of current stressing.

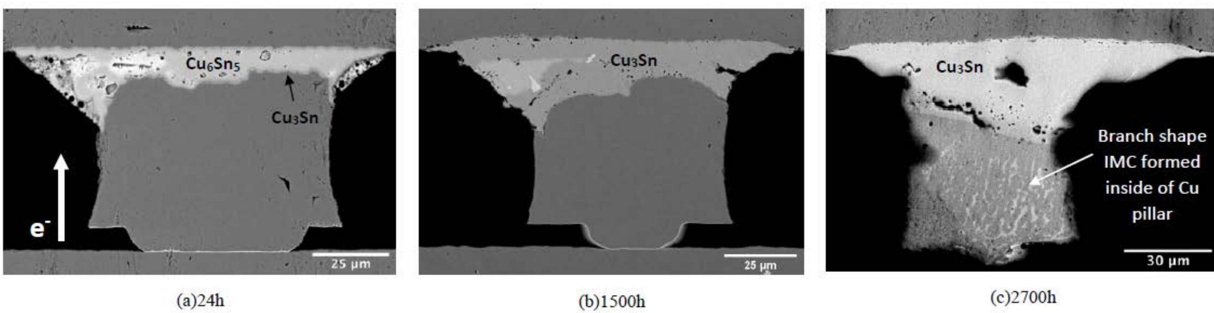


Figure 4-33. Cross-sectional view of EM tested samples under 67 kA/cm^2 at 152ºC.

As we can see in Figure 4-33, there is branch shaped phase that is formed inside of the Cu pillar. The branch shape of the IMC through the Cu pillar can be a sign that considerable interdiffusion occurred at the grain boundaries (GB) of Cu inside of the pillar. Multiple methods were employed to characterize the formed phases and identify the diffusion mechanism which is responsible for this extent of IMC formation. The first attempt was to identify the regions in the Cu pillar that endured a high amount of interdiffusion. In this order, the sample was etched by a diluted Nitric acid solution to reveal the highly stressed areas. As is shown in Figure 4-34, the regions that are highly attacked by the etchant correspond to the locations where the branch-shaped IMCs are formed. The boundaries of the Cu grains appear to be the paths along which the IMC are formed. In Figure 4-35, the micrograph of the Cu pillar grains, which is revealed by low angled ion etching, clearly confirms that the locations that the IMC formed are at the grain boundaries of the Cu pillar.

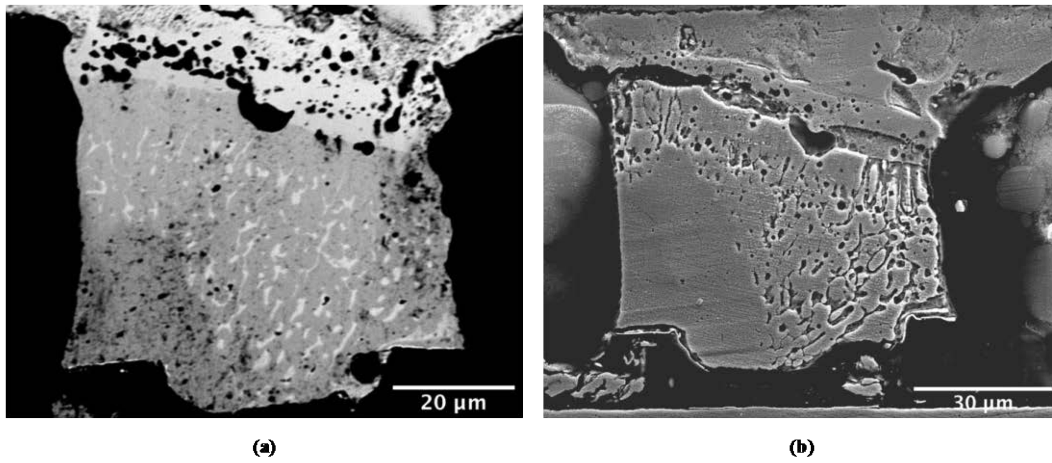


Figure 4-34. Cross-sectional view of EM tested samples under 67 kA/cm^2 (a) compositional mode image before etching (b) topographical mode image after etching.

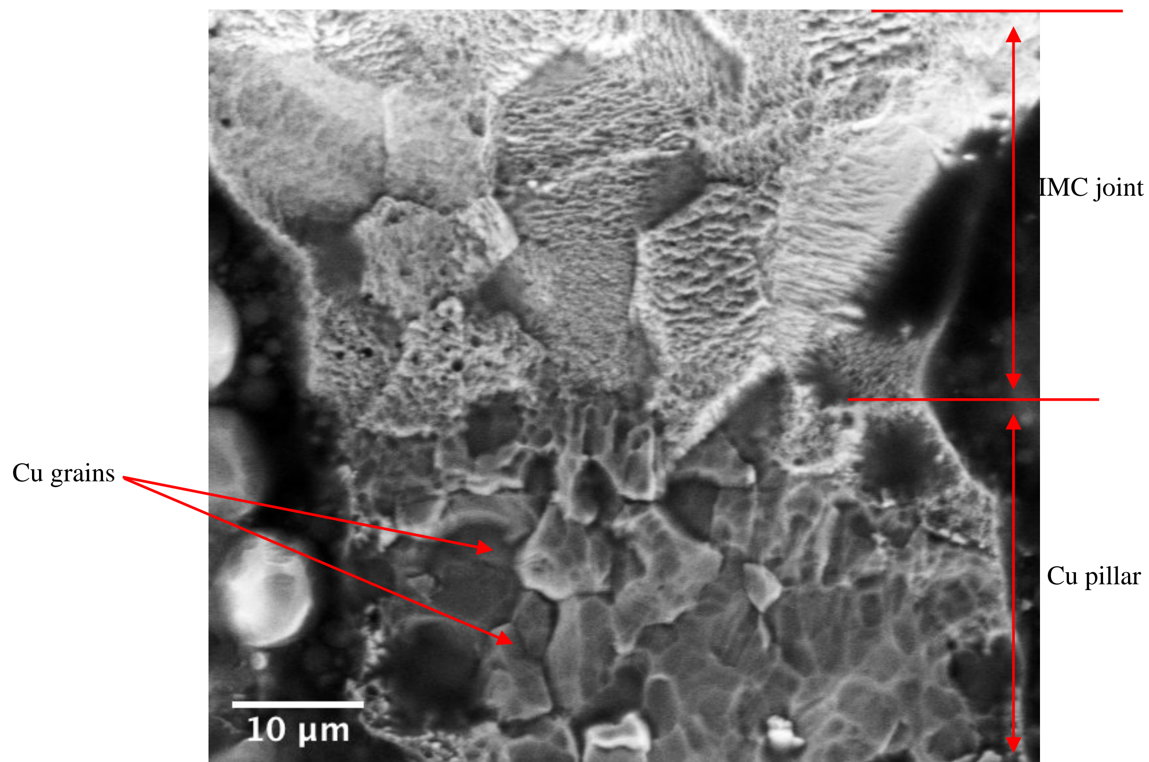
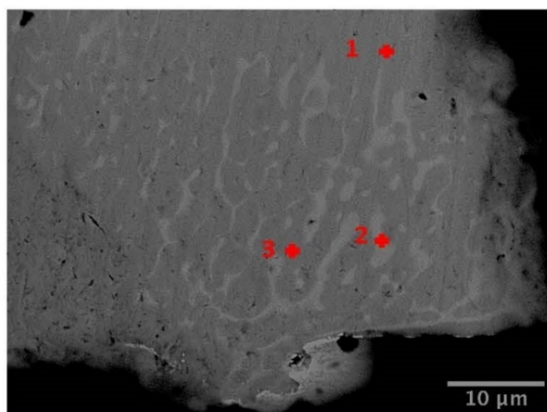


Figure 4-35. Cross-sectional image of the joint after ion etching which is showing grains of Cu pillar and IMC converted solder joint.

As a second method of analysis, the chemical analysis by EDS was done to characterize the IMC phase that extends into the Cu pillar. The locations where point EDS was performed are shown in Figure 4-36 along with their elemental compositions. As the detail of Figure 4-36 shows, the composition of the branch-shaped phase is close to Cu_3Sn phase, and the analysis inside of the affected grains is showing a presence of Sn in the Cu grains. It is very likely that a solid solution of Sn in Cu is formed although the equilibrium binary phase diagram of Cu-Sn suggests that Sn is almost immiscible in Cu at the lower temperatures.



Point	Cu(wt%)	Sn(wt%)
1 (Solid solution)	83.73	16.27
2 (Cu_3Sn)	66.44	33.56
3 (Solid solution)	91.48	8.52

Figure 4-36. EDS analysis of different points in regions where Cu-Sn interdiffusion occurred.

Since EDS analysis may have some limitations in quantifying the composition, another characterization method may be necessary to verify that the formed phases at the grain boundaries are Cu_3Sn. For this purpose, an EBSD analysis was performed to identify the crystal structure of the phases. The finding obtained by an EBSD point analysis suggests that the crystal structure of the branched IMC phase is similar to the crystal structure of Cu_3Sn. As a comparison of point EBSD analysis's is presented in Figure 4-37, the Kikuchi pattern obtained from the joint, which is Cu_3Sn. This pattern is similar to the pattern with the same crystal structure taken from the IMC formed in the grain boundaries of the Cu pillar. Thus, we can conclude that the EBDS point

analysis verifies the EDS analysis and it is clear evidence that Cu_3Sn formed in grain boundaries of Cu.

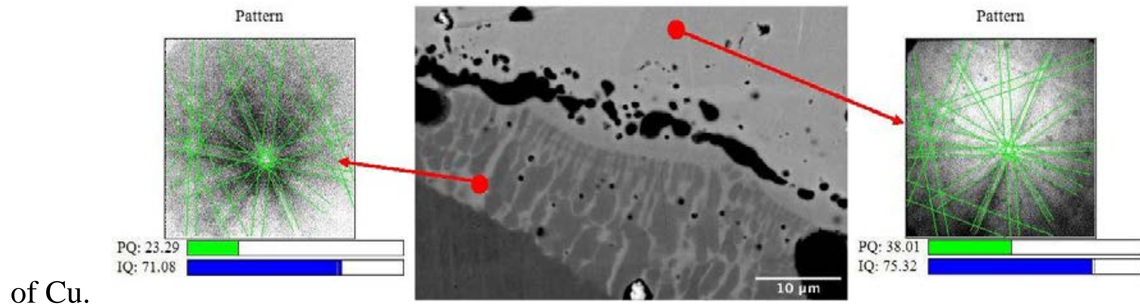


Figure 4-37. Cross-sectional SEM image of EM tested sample with point EBSD analysis done on the Cu3Sn and the IMC formed in the grain boundary.

Moreover, the cross-sectional microstructure of samples tested for a longer time shows that the branch-shaped IMCs are dissolved, and a uniform layer appeared in the affected zone within the Cu pillar. As is illustrated in Figure 4-38, there is an intermediate layer between the solder joint and the Cu pillar that is distinguished by a contrast in color. The branch shaped Cu_3Sn, which was formed before, does not exist in this microstructure and it is replaced with a uniform layer instead. The EDS line scan was conducted to show the Cu and Sn concentration profile from the joint toward the Cu pillar. The profiles are embedded on the cross-sectional microstructure to have a better presentation of the compositional change. As the concentration profile shows, there is a gradual composition profile of Sn after the Cu_3Sn IMC joint. It means the affected area is not pure Cu, and a small amount of Sn is dissolved through the intermediate layer. Since Cu is diluted by Sn in that region and the concentration of elements is not in the range of Cu-Sn IMC formation, it seems an extended solid solution of Sn in Cu is formed.

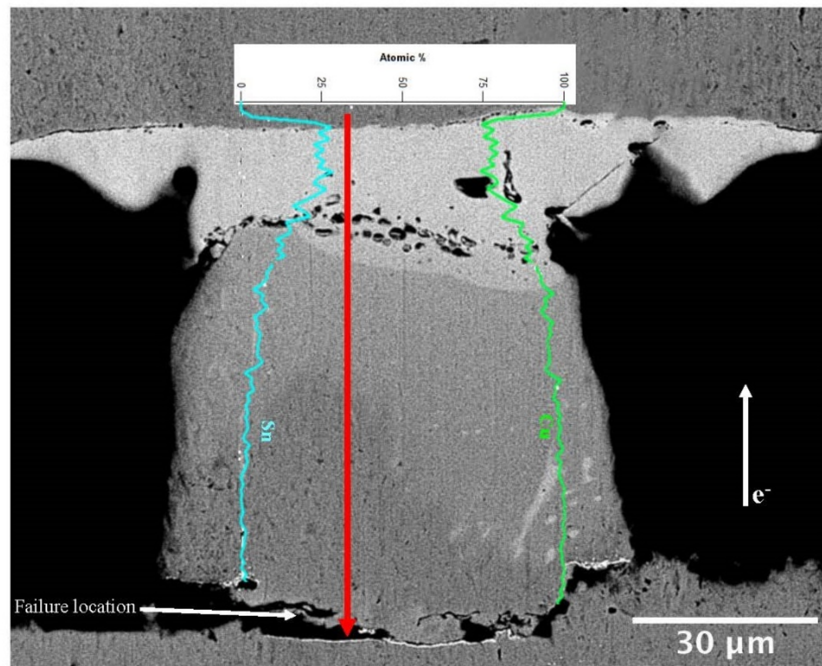


Figure 4-38. Cross-sectional SEM image of EM tested sample with EDS line scan taken along the solder joint to Cu pillar.

Another EBSD analysis was performed to identify the crystal structure of the intermediate layer. Figure 4-39 shows the intermediate layer formed between the joint and Cu pillar along with EBSD map analysis. As we can see in this picture, the affected layer has FCC crystal structure, which is similar to the crystal structure of pure Cu. Then, it is direct evidence that the analyzed layer is a Cu matrix that contains Sn. In other words, a solid solution of Sn in the Cu matrix is formed during a prolonged EM test under exceptional high current density.

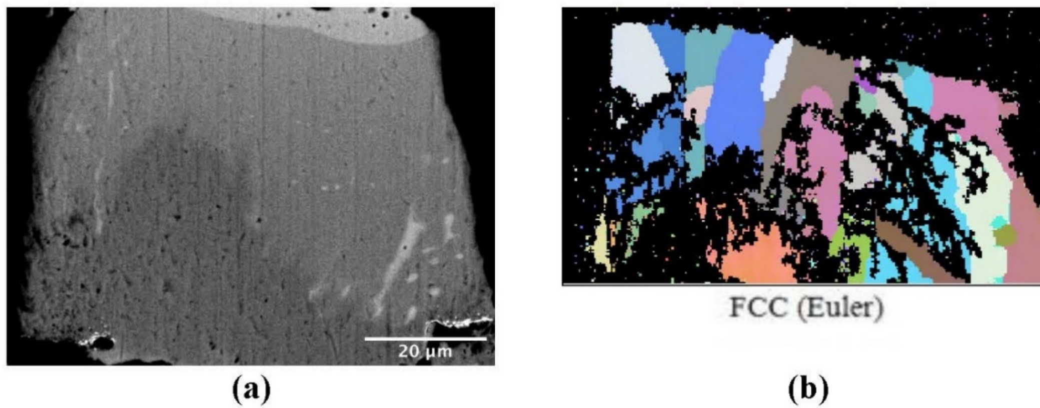


Figure 4-39. (a) Cross-sectional SEM image of EM tested sample, (b) EBSD map taken from (a) area.

The microstructure evolution of samples tested under current density of 36 kA/cm^2 suggests that IMC conversion is taken place sequentially based on the equilibrium phase diagram until the joint fully converts to Cu_3Sn. In this case, no microstructure changes after conversion of the solder joint to Cu_3Sn is observed. However, in the case of samples under current density of 67 kA/cm^2, results are revealed that interdiffusion of Cu and Sn is not stopped even after full conversion of the joint to Cu_3Sn. The most important, and interesting, finding we see in this test leg is the IMC growth through Cu's grain boundaries which is induced by exceptional high current density. A possible mechanism based on our observations is that a high amount of current stressing pushes Cu atoms to take the place of Sn atoms from IMC phase, and in turn, Sn atoms move toward Cu grains. Most previous studies, aging or current stressing investigation, reported and considered the growth of Cu-Sn IMC's up to the formation of Cu_3Sn. Presumably, the interaction of Cu-Sn will be stopped because Cu and Sn are immiscible at low temperatures according to the binary phase diagram[72], [89], [96]–[99]. Essentially, in aging condition at 152ºC without current flow, Sn cannot diffuse through GB's from Cu_3Sn phase, because there is a large thermodynamic barrier for releasing Sn from Cu_3Sn and diffuse into Cu side. So, our results suggest that this barrier may has been overcome by applying exceptional current stressing conditions. The question is that how it has happened? Which mechanism is responsible to fulfil the driving force required for Sn and Cu interdiffusion in this case? One clear evidence our results imply is the grain boundaries of Cu grains where the formation of Cu_3Sn occurred in GBs as Figure 4-36 and Figure 4-37 are illustrated. Basically, a grain boundary is a place that ordered arrangement of atoms ends and

dislocations and broken bond atoms exist at the regions where two or more grains reach together. The grain boundary is a classic fast diffusion path rather than bulk diffusion, but in a Cu-Sn system, this fast diffusion route is not enough to induce the driving force of interdiffusion in a thermal or even moderate thermal/current stressing condition. Wu et. al. [100] has reported the formation of a solid solution of tin in copper by using mechanical alloying which induced a high density of dislocations at grain boundaries. In addition, there are a few studies[101], [102] which have reported the formation of an extended solid solution under current-stressing conditions. The main reason that may justify the solid solution formation is associated with a high density of dislocations at the solvent grain boundaries due to EM. Therefore, the EM force causes more disturbance in the grain boundaries, which leads to the reduction of the driving force for the Cu-Sn interaction. Our observation evidently demonstrates these diffusion routes through the boundaries. Moreover, the continuation of the EM load that causes the branch-shaped microstructure to change to a uniform intermediate layer between Cu and IMC joint, which is shown in Figure 4-38 and Figure 4-39. As our characterization efforts are revealed, this intermediate region is a solid solution of Sn in Cu. In fact, the continuation of current stressing caused the dissolution of the IMC phase formed at the grain boundaries and their diffusion into the Cu grains. This suggests that the source of Sn which diffuses into the Cu grains is Cu_3Sn formed at GB. The mechanism that involves IMC formation at grain boundaries and the solid solution formation as well, in an immiscible system during EM test, can be attributed to several aspects. The stress field of dense dislocations has been proposed as a responsible mechanism for the formation of the solid solution[103]. In addition, the large grain boundary area which poses stored enthalpy could serve as a driving force for alloying[104], [105]. The very high density of dislocations produced by electron wind force at grain boundaries induces stress on the solute atoms. Highly stressed regions will extend by the continuation of testing time. Therefore, the combination of effective factors will produce a driving force to overcome the thermodynamic barrier (3.12 $kJ \cdot mol^{-1}$[100]) for the formation of a solid solution comprised of Cu(Sn).

Chapter 5: Summary

5-1- Results summary

The experiments were carried out in this research produced different failure mechanisms discussed in previous chapter. The change of joint resistance and failure analysis microstructure enabled us to understand failure mode at different test conditions. As a summary of various experiments results, the following implications are presented:

1) In the case of samples with Ni layer at the solder/LF interface, two failure modes are involved in the EM failure mechanism of the micro solder joint. We saw that the MTTF does not follow a single activation energy. As Figure 5-1 showed, there is a turning point in the direction of MTTF change with temperature despite what was expected based on Black's equation. It is discussed that two competing processes involved in the reliability of micro solder joints are the source of the failure mode change. It is shown that there are two main failure modes in samples which are tested under 11A (36 kA/cm^2). EM test results obtained from experiments at lower testing temperatures such as 144°C and 152°C suggest that the rate of EM in Sn is higher than the rate of Sn conversion to IMC. In contrast, the IMC conversion rate is dominant for the samples tested under higher temperatures like 160°C and 170°. Figure 5-2 depicts a schematic of different failure modes for the samples which are EM tested under 11A (36 kA/cm^2). Based on the microstructure of the failed samples, EM voiding inside of the micro solder joint is the characteristic of failure mode in the case when Sn EM rate is dominant. On the other hand, when the IMC conversion rate is dominant, the microstructure showed that the solder joint is fully converted to the IMC without substantial EM voids inside of the solder joint. In this case, a separation between the Cu pillar and grown IMC due to the Kirkendall void alignment at the interface is responsible for the joint failure. A Kirkendall void is the nature of interdiffusion of Sn and Cu. Electron wind force intensifies interaction of Sn and Cu that lead to extensive Kirkendall void formation. These voids eventually merge and create a separation that cuts current flowing at the interface.

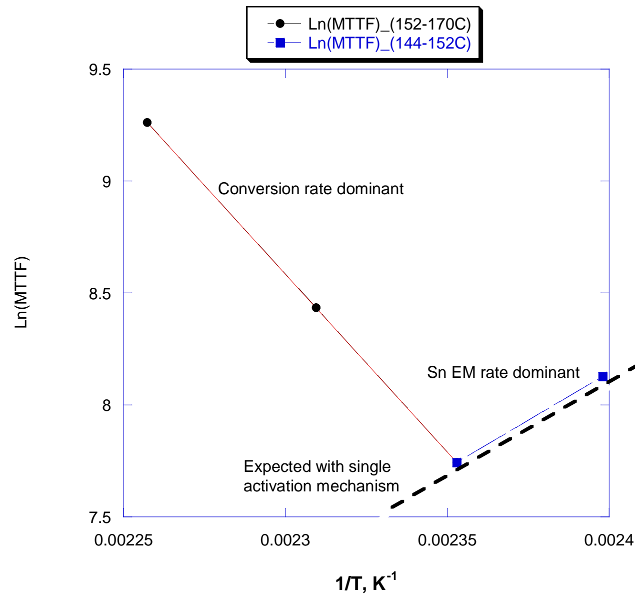
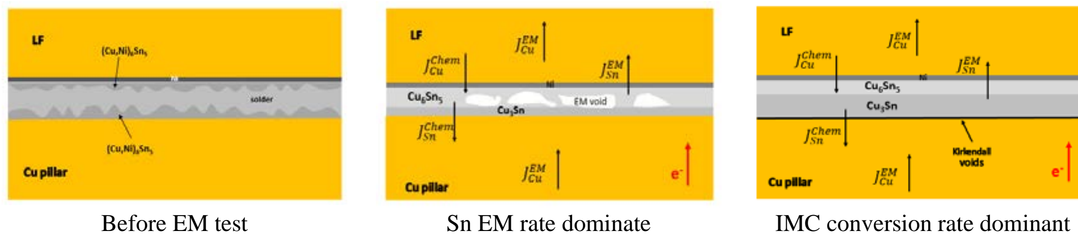


Figure 5-1. Variation of MTTF versus temperature for the samples with Ni layer at solder/LF interface under 36 kA/cm^2 EM test.

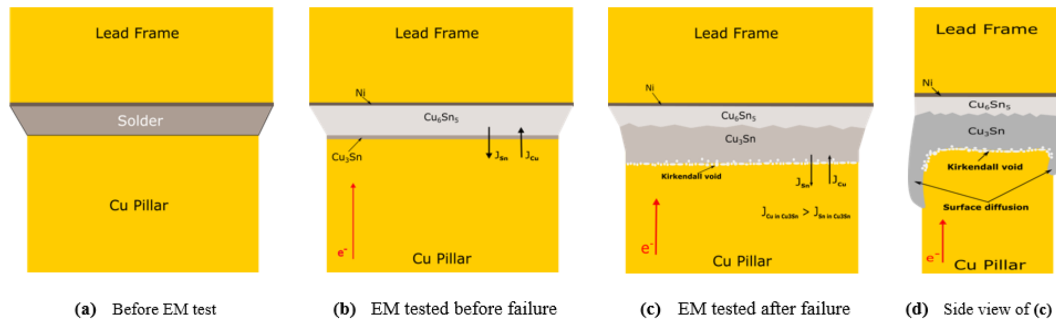


Before EM test | Sn EM rate dominate | IMC conversion rate dominant

Figure 5-2. Schematic of different failure modes for the samples (elliptical geometry) with Ni layer at solder/LF interface under 36 kA/cm^2 EM test.

2) EM facilitated the interaction of Cu and Sn interdiffusion during the test at a higher temperature and the failure mechanism is associated with two stages. In the first stage, the reaction of Sn and Cu converts the solder to the IMC. This conversion is extensive at the surface of the solder joint because of the surface diffusion mechanism. In the second stage, an unbalanced interdiffusion of Cu and Sn through the formed IMC resulted in formation of Kirkendall voids, which are ultimately responsible for the failure. Since the location of the failure shifted to the interface of the solder joint and Cu pillar, and since this type of

failure is induced by the flux divergence, the EM enhanced growth of the IMC is very sensitive to the geometry and arrangement of the solder joint to eliminate or reduce short circuit diffusion paths that the failure mechanism. The schematics that depict the evolution of the micro solder joint during the EM test is represented in Figure 5-3.



(a) Before EM test **(b)** EM tested before failure **(c)** EM tested after failure **(d)** Side view of **(c)**

Figure 5-3. Schematic representation of micro solder joint (elliptical geometry) evolution during EM test at high temperature.

3) The results of EM test at higher current load, i.e., 12A (40 kA/cm^2), showed similar results in terms of kinetics of the failure. Meaning that at a lower test temperature, EM of Sn prior to conversion to the IMC is the mechanism that caused the void formation inside of the solder joint. At higher test temperatures, the IMC conversion rate is dominant process, but the current crowding in the joint caused extensive IMC growth toward the Cu pillar. The change of MTTF versus test temperature under a current density of 40 kA/ cm^2 is plotted in Figure 5-4. The microstructure of the failed samples under a 12A testing load showed that deep growth of Cu-Sn toward Cu pillar. Figure 5-4 schematically illustrates that the deep growth of Cu_3Sn into the Cu pillar occurred in regions where current crowding accelerates the growth of the IMC.

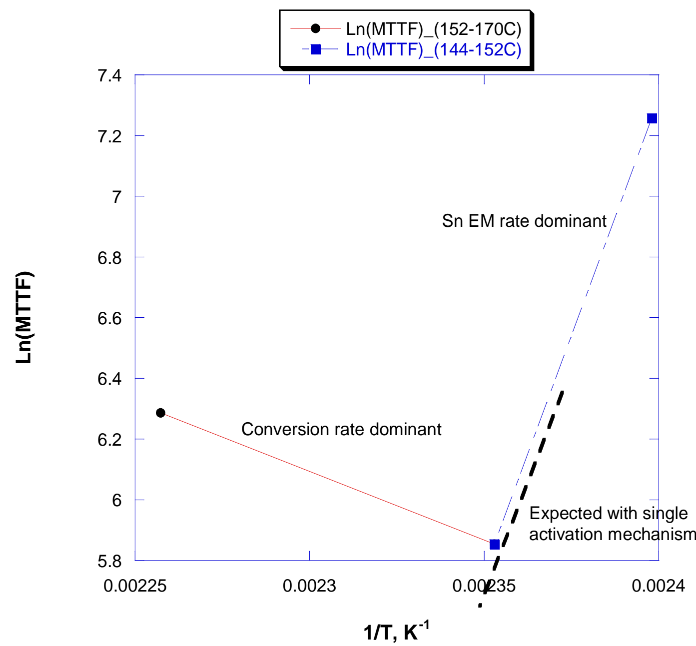


Figure 5-4. Variation of MTTF versus temperature for the samples with Ni layer at solder/LF interface under 40kA/ cm^2 EM test.

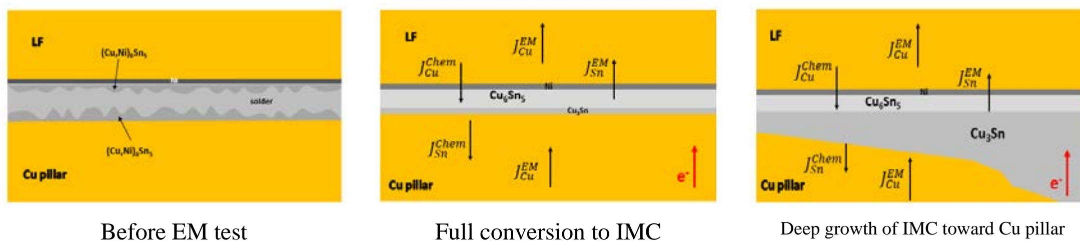


Figure 5-5. Schematic of failure mode for the samples (elliptical geometry) with Ni layer at solder/LF interface under 40 kA/ cm^2 EM test.

4) In the case of samples with a Ni interfacial layer at both interfaces of the solder joint, the results from samples tested at 160°C presented that the solder joint is immune against EM damage, whereas samples which were tested at 170°C resulted in failure. This result suggests that in this group of samples, the back-stress due to the low profile thickness of the solder joint counteracts the EM damage inside of the solder joint. On the other hand,

higher test temperature, i.e., 170 ºC, resulted in EM failure in the solder joint because the back-stress gradient is decreased due to higher temperature and the rate of EM damage is dominant. Figure 5-6 shows the change of microstructure of the solder joint during the EM test when the EM force is not impeded by the back-stress and EM-induced voids formed inside of the solder joint.

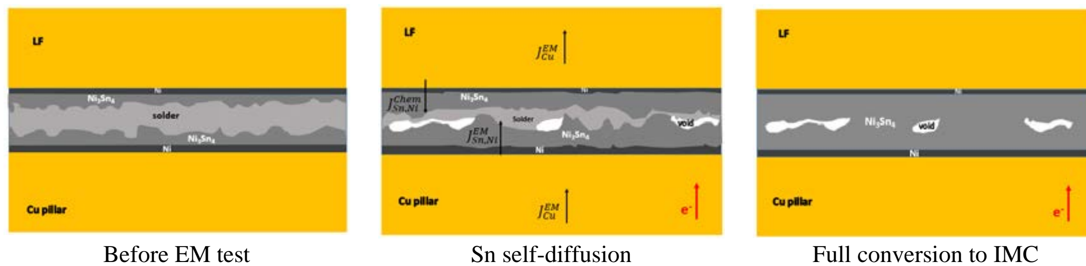


Figure 5-6. Schematic of failure mode for the samples with Ni layer at both solder interface under36 kA/cm^2 EM test.

In fact, it is first found that the EM failure by void growth is in kinetics competition with the IMC growth rate, meaning that the joint achieves the condition of EM failure immunity when IMC growth outcompetes the voiding to fully convert the joint to Ni_3Sn_4 IMC phase. It is, however, our conclusion that the solder joint cannot attain such a condition where the joint conversion to IMC proceeds faster than the voiding even in micro solder joints without assistance from the back-stress effect. It is shown that the joint tested at 160ºC in our study is subjected to the back-stress effect to the extent that the EM force for both Ni and Sn ceases to exist. This stops the voiding while the IMC growth continues by diffusion processes, enabling the attainment of a full IMC conversion prior to EM-induced voiding. Reduction in the back-stress effect, as occurs in the joint tested at 170ºC, causes the joint to fail by EM voiding because Sn-EM can proceed faster than the IMC conversion. In addition to the low aspect ratio (thickness to length) joint structure favoring back-stress generation, the isolation of the Sn-EM flux enabled by Ni_3Sn_4 IMC at both interfaces is responsible for the unique results seen in our study.

5) The elliptical shaped solder joint samples lacking a diffusion barrier layer at the interfaces did not show EM failure. The failure analysis results offered the fact that this type of solder

joint is immortal against EM damage since it has a very thin layer of solder after reflowing, and an unlimited interaction with Cu at both interfaces quickly converts the solder joint to IMC. As we know, the intermetallics are persistent against EM damage. Thus, no EM failure is occurred in the testing of this group of samples. The schematic of the microstructural evolution of this group of samples during the EM test is presented in Figure 5-7.

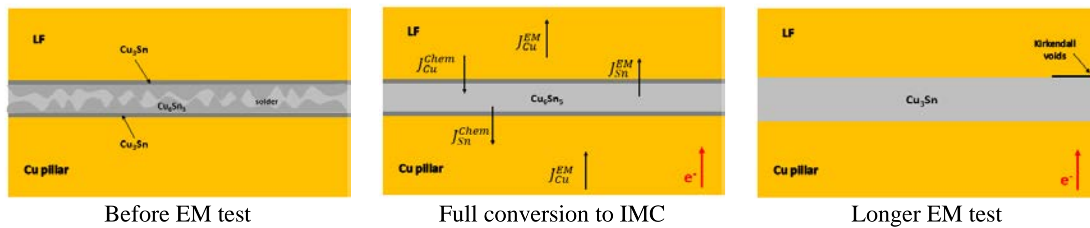


Figure 5-7. Schematic of failure mode for the samples without Ni layer at solder interfaces under 36 kA/cm^2 EM test.

6) The samples with a cylindrical joint geometry tested at 36 kA/cm^2 did not show failure due to full IMC conversion of the solder joint. Therefore, the attempt to find a kinetics model to anticipate the failure time was not achievable because the failure data at different temperatures and current densities were not sufficient to calculate the parameters of the failure kinetics. However, the results of the cylindrical samples which were tested at a higher current density, 67 kA/cm^2, showed a unique failure mode due to the extended solid solution of Sn in Cu. The experimental observations revealed clear evidence of the Cu-Sn interdiffusion even after a full conversion of the solder material to the IMC. In fact, interdiffusion through the grain boundaries of the Cu grains is facilitated by electron wind force. Further studies revealed that IMCs formed at the grain boundaries are dissolved into the Cu grains by the replenishing of Sn within the Cu matrix at a prolonged period of time during the EM test. Therefore, an extended solid solution of the Sn in Cu is established despite the equilibrium phase stability. By comparing the evidence observed in this study and the affecting factors involved in the formation of the solid solution, we can speculate a mechanism that may describe the unusual results of this study. First, the polycrystalline fine grain Cu pillar processed by electroplating consists of a large number of grain

boundaries that increase the surface to volume ratio of grains. These available grain boundaries inherently are fast diffusion routes. Then, an exceptionally high current density induces more dislocated atoms, especially ones with weak bonding. Additional dislocations produced by the electron wind force increase the density of dislocations at the grain boundaries. As mentioned in the previous chapter, the level of stress reaches a level where the driving force is supplied for the interdiffusion of Cu and Sn within the grain boundaries. Since migrated Cu atoms at the interface with the Cu-Sn IMC produces a high local concentration gradient of Cu at the GB regions. Sn atoms then start to diffuse through Cu_3Sn toward the grain boundaries. The substitution of Cu and Sn atoms gradually formed Cu_3Sn at those boundaries. In the next step, the width of the grain boundaries gradually extends and there will be an atomic flux of Sn into the Cu grains. This step is depicted schematically in Figure 5-8. Eventually, all the IMC formed at the grain boundaries dissociate and the released Sn diffuses into the Cu grains. Therefore, a layer of the solid solution of Sn in Cu will form. All steps of microstructural changes are illustrated schematically in Figure 5-9. The results of this mode of failure are imperative in the identification of the effects of extreme current density on Cu-Sn system rather than the previously known phase formation based on equilibrium thermodynamic of phase stability.

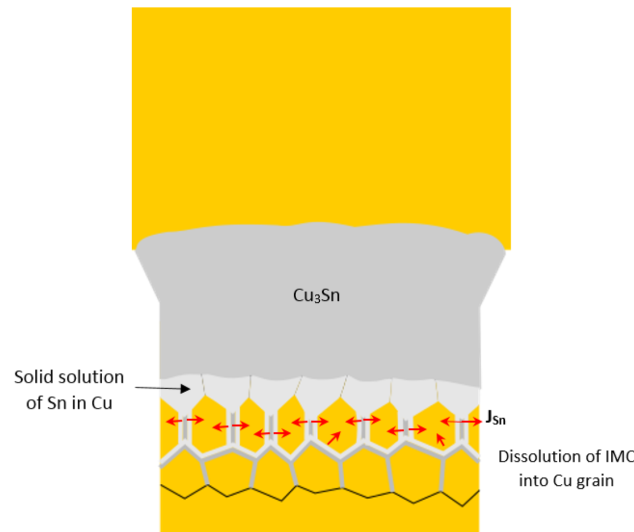


Figure 5-8. Suggested mechanism that depicting solid solution formation in Cu grains in cylindrical joint geometry.

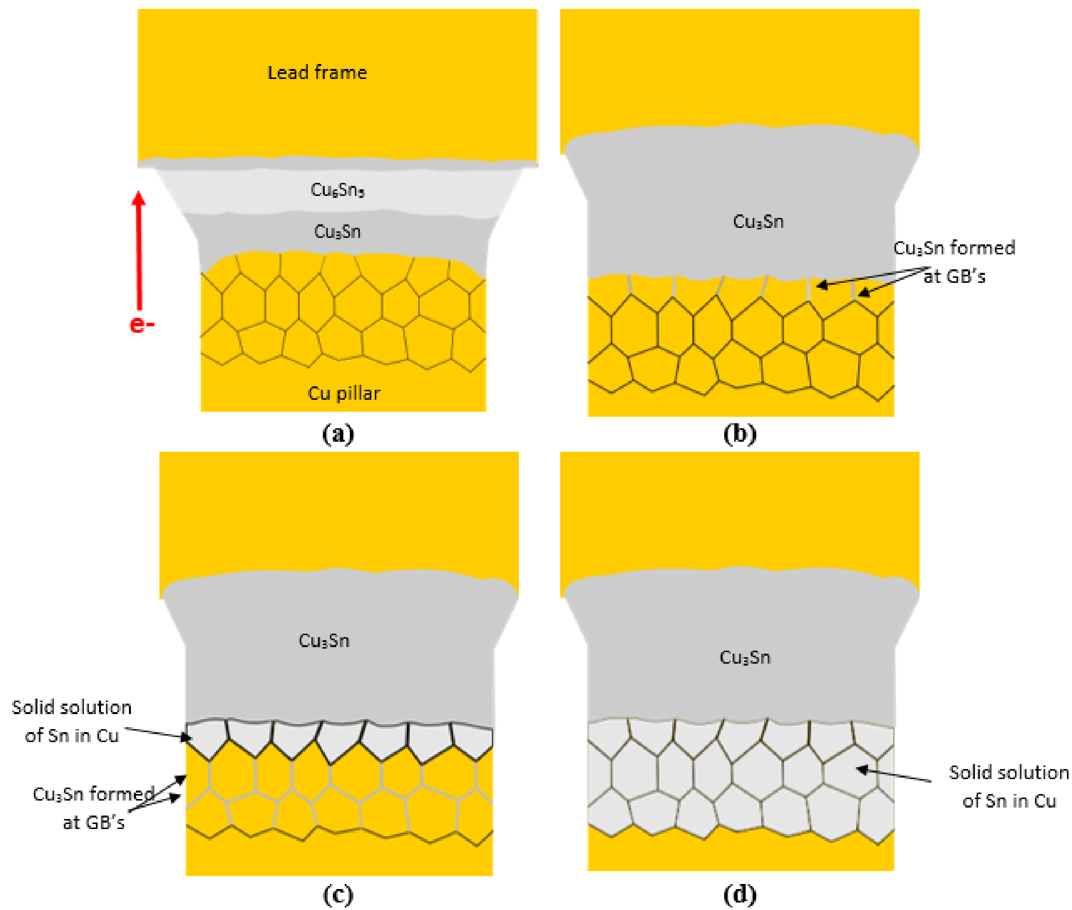


Figure 5-9. Microstructure evolution of IMC joint in cylindrical joint geometry(a) Cu_6Sn_5 is converting to Cu_3Sn, (b) Cu_3Sn formed at GB near the interface, (c) solid solution formed at Cu grains near the interface, (d) solid solution proceeded in more Cu grains.

5-2- Conclusion

The focus of this research is to investigate the EM reliability of micro solder joints. Several experiments were performed to better understand the mechanism involved in the EM failure. The first implication that our finding offers is the complexity of the failure mechanism in this type of solder joint compared to conventional solder joints like BGA or flip chip joints. Essentially, a low amount of solder material along with a low aspect ratio (thickness to length) of the joint revealed results which suggest that the failure kinetics and mechanism are very sensitive to test temperature and current density. Secondly, to our surprise, it is found that failure can happen even if the solder

joint has fully converted to the IMC which was assumed immune against EM damage. Our observation clearly demonstrates that the back-stress effect can impede EM damage in the micro solder joint where the joint is confined between the Ni layers. Also, our study on EM failure of a fine pitched solder joint (cylindrical geometry) is resulted to find a unique failure mechanism due to the extended solid solution formation. Finally, conclusions of the results in this research give notable clues to consider factors impacting the EM reliability of micro solder joints.

Chapter 6: References

[1] J. R. Black, "Metallization failures in integrated circuits." doi: 10.1002/nav.3800080206.

[2] J. Lienig and M. Thiele, *Fundamentals of Electromigration- Aware Integrated Circuit Design*. Springer, 2018.

[3] K. Tu, *Solder Joint Technology*. Springer, 2007.

[4] B. Chao *et al.*, "Electromigration enhanced intermetallic growth and void formation in Pb-free solder joints," *Phys, J Appl*, vol. 084909, no. October, 2006, doi: 10.1063/1.2359135.

[5] H. M. Tong, Y. S. Lai, and C. P. Wong, *Advanced flip chip packaging*. Springer, 2013.

[6] T. K. Lee, T. R. Bieler, C. U. Kim, and H. Ma, *Fundamentals of lead-free solder interconnect technology: From microstructures to reliability*. Springer, 2015.

[7] M. Abtew and G. Selvaduray, "Lead-free Solders in Microelectronics," *Mater. Sci. Eng. R Reports*, vol. 27, no. 5, pp. 95–141, 2000, doi: https://doi.org/10.1016/S0927-796X(00)00010-3.

[8] H. X. Xie, L. Jiang, and N. Chawla, "Effect of cerium addition on wetting, undercooling, and mechanical properties of Sn-3.9Ag-0.7Cu Pb-free solder alloys," *J. Mater. Sci. Mater. Electron.*, vol. 24, no. 9, pp. 3456–3466, 2013, doi: 10.1007/s10854-013-1270-7.

[9] P. T. Vianco and D. R. Frear, "Issues in the replacement of lead-bearing solders," *JOM*, vol. 45, no. 7, pp. 14–19, 1993, doi: 10.1007/BF03222374.

[10] K. J. Puttlitz and K. A. Stalter, *Handbook of lead-free solder technology for microelectronic assemblies*. CRC Press, 2004.

[11] J. H. Lau, C. P. Wong, N.-C. Lee, and S.-W. R. Lee, *Electronics Manufacturing: With Lead-Free, Halogen-Free, and Conductive-Adhesive Materials*. New York: McGraw-Hill Education, 2003.

[12] Y. Kariya and M. Otsuka, "Effect of bismuth on the isothermal fatigue properties of Sn-3.5mass%Ag solder alloy," *J. Electron. Mater.*, vol. 27, no. 7, pp. 866–870, 1998, doi: 10.1007/s11664-998-0111-6.

[13] I. E. Anderson, "Development of Sn-Ag-Cu and Sn-Ag-Cu-X alloys for Pb-free electronic solder applications BT - Lead-Free Electronic Solders: A Special Issue of the Journal of Materials Science: Materials in Electronics," K. N. Subramanian, Ed. Boston, MA: Springer US, 2007, pp. 55–76.

[14] T. Laurila, J. Hurtig, V. Vuorinen, and J. K. Kivilahti, "Effect of Ag, Fe, Au and Ni on the growth kinetics of Sn–Cu intermetallic compound layers," *Microelectron. Reliab.*, vol. 49, no. 3, pp. 242–247, 2009, doi: https://doi.org/10.1016/j.microrel.2008.08.007.

[15] K. S. Kim, S. H. Huh, and K. Suganuma, “Effects of fourth alloying additive on microstructures and tensile properties of Sn–Ag–Cu alloy and joints with Cu,” *Microelectron. Reliab.*, vol. 43, no. 2, pp. 259–267, 2003, doi: https://doi.org/10.1016/S0026-2714(02)00239-1.

[16] J.-Y. Park, R. Kabade, C.-U. Kim, T. Carper, S. Dunford, and V. Puligandla, “Influence of Au addition on the phase equilibria of near-eutectic Sn-3.8Ag-0.7Cu Pb-free solder alloy,” *J. Electron. Mater.*, vol. 32, no. 12, pp. 1474–1482, 2003, doi: 10.1007/s11664-003-0117-z.

[17] C.-M. Chuang and K.-L. Lin, “Effect of microelements addition on the interfacial reaction between Sn-Ag-Cu solders and the Cu substrate,” *J. Electron. Mater.*, vol. 32, no. 12, pp. 1426–1431, 2003, doi: 10.1007/s11664-003-0111-5.

[18] D. H. Kim, M. G. Cho, S.-K. Seo, and H. M. Lee, “Effects of Co Addition on Bulk Properties of Sn-3.5Ag Solder and Interfacial Reactions with Ni-P UBM,” *J. Electron. Mater.*, vol. 38, no. 1, pp. 39–45, 2009, doi: 10.1007/s11664-008-0529-x.

[19] Y. Kariya and M. Otsuka, “Mechanical fatigue characteristics of Sn-3.5Ag-X (X=Bi, Cu, Zn and In) solder alloys,” *J. Electron. Mater.*, vol. 27, no. 11, pp. 1229–1235, 1998, doi: 10.1007/s11664-998-0074-7.

[20] T. Laurila *et al.*, “Evolution of microstructure and failure mechanism of lead-free solder interconnections in power cycling and thermal shock tests,” *Microelectron. Reliab.*, vol. 47, no. 7, pp. 1135–1144, 2007, doi: https://doi.org/10.1016/j.microrel.2006.07.095.

[21] T. Lee, W. Xie, and K. Liu, “Impact of isothermal aging on Sn-Ag-Cu solder interconnect board level high G mechanical shock performance,” in *2011 IEEE 61st Electronic Components and Technology Conference (ECTC)*, 2011, pp. 547–552, doi: 10.1109/ECTC.2011.5898565.

[22] J. Karppinen, J. Li, J. Pakarinen, T. T. Mattila, and M. Paulasto-Kröckel, “Shock impact reliability characterization of a handheld product in accelerated tests and use environment,” *Microelectron. Reliab.*, vol. 52, no. 1, pp. 190–198, 2012, doi: https://doi.org/10.1016/j.microrel.2011.09.001.

[23] C. M. L. Wu, D. Q. Yu, C. M. T. Law, and L. Wang, “Properties of lead-free solder alloys with rare earth element additions,” *Mater. Sci. Eng. R Reports*, vol. 44, no. 1, pp. 1–44, 2004, doi: https://doi.org/10.1016/j.mser.2004.01.001.

[24] C. M. L. Wu, M. L. Huang, J. K. L. Lai, and Y. C. Chan, “Developing a lead-free solder alloy Sn-Bi-Ag-Cu by mechanical alloying,” *J. Electron. Mater.*, vol. 29, no. 8, pp. 1015–1020, 2000, doi: 10.1007/s11664-000-0166-5.

[25] C. E. Ho, W. Gierlotka, and S. W. Lin, “Strong effect of Pd concentration on the soldering reaction between Ni and Sn–Pd alloys,” *J. Mater. Res.*, vol. 25, no. 11, pp. 2078–2081, 2010, doi: DOI: 10.1557/jmr.2010.0268.

[26] R. W. Chuang, D. Kim, J. Park, and C. C. Lee, "A fluxless process of producing tin-rich gold-tin joints in air," *IEEE Trans. Components Packag. Technol.*, vol. 27, no. 1, pp. 177–181, 2004, doi: 10.1109/TCAPT.2004.825757.

[27] D. Shangguan and A. Achari, "Evaluation of lead-free eutectic Sn-Ag solder for automotive electronics packaging applications," in *Proceedings of 16th IEEE/CPMT International Electronic Manufacturing Technology Symposium*, 1994, pp. 25–37 vol.1, doi: 10.1109/IEMT.1994.404695.

[28] S. Anhock, H. Oppermann, C. Kallmayer, R. Aschenbrenner, L. Thomas, and H. Reichl, "Investigations of Au-Sn alloys on different end-metallizations for high temperature applications [solders]," in *Twenty Second IEEE/CPMT International Electronics Manufacturing Technology Symposium. IEMT-Europe 1998. Electronics Manufacturing and Development for Automotives (Cat. No.98CH36204)*, 1998, pp. 156–165, doi: 10.1109/IEMTE.1998.723081.

[29] K. Suganuma, S.-J. Kim, and K.-S. Kim, "High-temperature lead-free solders: Properties and possibilities," *JOM*, vol. 61, no. 1, pp. 64–71, 2009, doi: 10.1007/s11837-009-0013-y.

[30] T. Wassick, "Electromigration Overview for Pb – Free Solder Systems : A Power IC Perspective," 2012.

[31] S. Härter, R. Dohle, A. Reinhardt, J. Goßler, and J. Franke, "Reliability study of lead-free flip-chips with solder bumps down to 30 μm diameter," *Proc. - Electron. Components Technol. Conf.*, no. June, pp. 583–589, 2012, doi: 10.1109/ECTC.2012.6248889.

[32] W. J. Choi, E. C. C. Yeh, and K. N. Tu, "Mean-time-to-failure study of flip chip solder joints on Cu/Ni(V)/Al thin-film under-bump-metallization," *J. Appl. Phys.*, vol. 94, no. 9, pp. 5665–5671, 2003, doi: 10.1063/1.1616993.

[33] B. G. E. Moore, "Cramming more components onto integrated circuits," *Electronics,* vol. 38, no. 8, 1965.

[34] Y. Nakamura and S. Katogi, "Technology Trends and Future History of Semiconductor Packaging Substrate Material," 2013.

[35] J. Gotro, "Polymers in Electronic Packaging: Introduction to Flip Chip Packaging," *Polymer Innovation Blog*, 2018. https://polymerinnovationblog.com/polymers-electronic-packaging-introduction-flip-chip-packaging/.

[36] K.-L. Lin, "Fundamentals of Solder Alloys in 3D Packaging," in *3D Microelectronic Packaging*, vol. 57, no. 1, 2017, pp. 86–96.

[37] H. M. Tong, Y. Lai, and C. P. Wong, Eds., *Advanced Flip Chip Packaging*. Springer, 2013.

[38] J. W. Nah *et al.*, "Electromigration in flip chip solder joints having a thick Cu column bump and a shallow solder interconnect," *J. Appl. Phys.*, vol. 100, no. 12, 2006, doi:

10.1063/1.2402475.

[39] K. N. Tu, "Recent advances on electromigration in very-large-scale-integration of interconnects," *J. Appl. Phys.*, vol. 94, no. 9, pp. 5451–5473, 2003, doi: 10.1063/1.1611263.

[40] H. Zhang, E. Perfecto, V. L. Calero-ddelc, and F. Pompeo, "An Effective Method for Full Solder Intermetallic Compound Formation and Kirkendall Void Control in Sn-base Solder Micro-joints," in *2015 Electronic Components & Technology Conference*, 2015, pp. 1695–1700.

[41] W. H. Chen, C. F. Yu, H. C. Cheng, Y. M. Tsai, and S. T. Lu, "IMC growth reaction and its effects on solder joint thermal cycling reliability of 3D chip stacking packaging," *Microelectron. Reliab.*, vol. 53, no. 1, pp. 30–40, 2013, doi: 10.1016/j.microrel.2012.06.146.

[42] I. S. Devised *et al.*, "I NTERNATIONAL T ECHNOLOGY R OADMAP FOR S EMICONDUCTORS 2 . 0," 2015.

[43] X. Zhang *et al.*, "Heterogeneous 2.5D integration on through silicon interposer," *Appl. Phys. Rev.*, vol. 2, no. 2, 2015, doi: 10.1063/1.4921463.

[44] S. Q. Gu, "Material innovation opportunities for 3D integrated circuits from a wireless application point of view," *MRS Bull.*, vol. 40, no. 3, pp. 233–241, 2015, doi: 10.1557/mrs.2015.9.

[45] P. Liu, "Fundamentals of Electromigration in Interconnects of 3D Packaging," in *3D Microelectronic Packaging*, vol. 57, no. 1, Y. Li and D. Goyal, Eds. 2017, pp. 223–244.

[46] K. N. Tu and T. Tian, "Metallurgical challenges in microelectronic 3D IC packaging technology for future consumer electronic products," *Sci. China Technol. Sci.*, vol. 56, no. 7, pp. 1740–1748, 2013, doi: 10.1007/s11431-013-5261-y.

[47] K. N. Chen and K. N. Tu, "Materials challenges in three-dimensional integrated circuits," *MRS Bull.*, vol. 40, no. 3, pp. 219–222, 2015, doi: 10.1557/mrs.2015.8.

[48] K. N. Tu, H. Y. Hsiao, and C. Chen, "Transition from flip chip solder joint to 3D IC microbump: Its effect on microstructure anisotropy," *Microelectron. Reliab.*, vol. 53, no. 1, pp. 2–6, 2013, doi: 10.1016/j.microrel.2012.07.029.

[49] M. Lu, D. Y. Shih, P. Lauro, C. Goldsmith, and D. W. Henderson, "Effect of Sn grain orientation on electromigration degradation mechanism in high Sn-based Pb-free solders," *Appl. Phys. Lett.*, vol. 92, no. 21, 2008, doi: 10.1063/1.2936996.

[50] Y. Wang *et al.*, "Effects of Sn grain structure on the electromigration of Sn-Ag solder joints," *J. Mater. Res.*, vol. 27, no. 8, pp. 1131–1141, 2012, doi: 10.1557/jmr.2012.10.

[51] Y. W. Chang *et al.*, "A new failure mechanism of electromigration by surface diffusion

of Sn on Ni and Cu metallization in microbumps," *Sci. Rep.*, vol. 8, no. 1, pp. 1–10, 2018, doi: 10.1038/s41598-018-23809-1.

[52] M. Y. Kim, L. S. Chen, S. H. Chae, and C. U. Kim, "Mechanism of void formation in Cu post solder joint under electromigration," in *IEEE 64th Electronic Components and Technology Conference*, 2015, pp. 135–141, doi: 10.1109/ECTC.2015.7159582.

[53] H. Madanipour *et al.*, "Effect of Intermetallic Compound Growth on Electromigration Failure Mechanism in Low-profile Solder Joints," in *IEEE 69th Electronic Components and Technology Conference*, 2019, pp. 1316–23, doi: https://doi.org/10.1109/ECTC.2019.00204.

[54] M. Ding, "Investigation of Electromigration Reliability of Solder Joint in Flip-Chip Packages," The University of Texas at Austin, 2007.

[55] H. Hsu, T. Y. Lin, and F. Y. Ouyang, "Evaluation of electromigration behaviors of Pb-free microbumps in three-dimensional integrated circuit packaging," *J. Electron. Mater.*, vol. 43, no. 1, pp. 236–246, 2014, doi: 10.1007/s11664-013-2840-4.

[56] M. Lu, T. Wassick, G. Advocate, and B. Backes, "Electromigration and thermal migration in Pb-free interconnects," *Proc. - Electron. Components Technol. Conf.*, vol. 2015-July, pp. 2036–2039, 2015, doi: 10.1109/ECTC.2015.7159882.

[57] C. V. Thompson and J. R. Lloyd, "Electromigration and IC Interconnects," *MRS Bull.*, vol. 18, no. 12, pp. 19–25, 1993, doi: 10.1557/S088376940003904X.

[58] Y. J. Park, K. D. Lee, and W. R. Hunter, "A variable current exponent model for electromigration lifetime relaxation in short Cu interconnects," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 2–5, 2006, doi: 10.1109/IEDM.2006.346966.

[59] A. S. Budiman *et al.*, "Electromigration-induced plastic deformation in Cu interconnects: Effects on current density exponent, n, and implications for em reliability assessment," *J. Electron. Mater.*, vol. 39, no. 11, pp. 2483–2488, 2010, doi: 10.1007/s11664-010-1356-4.

[60] M. Lu, D. Y. Shih, C. Goldsmith, and T. Wassick, "Comparison of electromigration behaviors of SnAg and SnCu solders," in *IEEE 47th Annual International Reliability Physics Symposium*, 2009, pp. 149–154, doi: 10.1109/IRPS.2009.5173241.

[61] B. Ebersberger, R. Bauer, and L. Alexa, "Reliability of lead-free SnAg solder bumps: Influence of electromigration and temperature," *55th Electron. Components Technol. Conf. Vols 1 2, 2005 Proc.*, no. condition C, pp. 1407–1415, 2005, doi: 10.1109/ECTC.2005.1441970.

[62] J. H. Lee *et al.*, "Joule heating effect on the electromigration lifetimes and failure mechanisms of Sn-3.5Ag solder bump," *Proc. - Electron. Components Technol. Conf.*, pp. 1436–1441, 2007, doi: 10.1109/ECTC.2007.373984.

[63] A. Roy and C. M. Tan, "Very high current density package level electromigration test for copper interconnects," *J. Appl. Phys.*, vol. 103, no. 9, 2008, doi: 10.1063/1.2917065.

[64] D. Goyal, P. Liu, and A. Overson, "A Comparison Study of Cu Dissolution Mechanism and Kinetics in Solder Joints under Electromigration and Extended Reflow," *Proc. - Electron. Components Technol. Conf.*, vol. 2018-May, pp. 440–447, 2018, doi: 10.1109/ECTC.2018.00072.

[65] H. C. Ma *et al.*, "Reliability and failure mechanism of copper pillar joints under current stressing," *J. Mater. Sci. Mater. Electron.*, vol. 26, no. 10, pp. 7690–7697, 2015, doi: 10.1007/s10854-015-3410-8.

[66] R. G. Filippi *et al.*, "The effect of current density, stripe length, stripe width, and temperature on resistance saturation during electromigration testing," *J. Appl. Phys.*, vol. 91, no. 9, pp. 5787–5795, 2002, doi: 10.1063/1.1459616.

[67] M. Lu, D. Y. Shih, P. Lauro, and C. Goldsmith, "Blech effect in Pb-free flip chip solder joint," *Appl. Phys. Lett.*, vol. 94, no. 1, pp. 0–3, 2009, doi: 10.1063/1.3067863.

[68] D. A. Porter and K. E. Easterling, *Phase Transformations in Metals and Alloys*, 3rd ed. CRC Press, 2009.

[69] C. Y. Liu *et al.*, "Electromigration-induced Kirkendall voids at the Cu Cu 3 Sn interface in flip-chip Cu Sn Cu joints Electromigration-induced Kirkendall voids at the Cu / Cu 3 Sn interface in flip-chip Cu / Sn / Cu joints," *J. Appl. Phys. Lett.*, vol. 112114, no. 2007, pp. 2005–2008, 2010, doi: 10.1063/1.2714100.

[70] K. Zeng, R. Stierman, T. C. Chiu, D. Edwards, K. Ano, and K. N. Tu, "Kirkendall void formation in eutectic SnPb solder joints on bare Cu and its effect on joint reliability," *J. Appl. Phys.*, vol. 97, no. 2, 2005, doi: 10.1063/1.1839637.

[71] K. H. Kuo, C. Mao, K. Wang, J. Lee, F. L. Chien, and R. Lee, "The impact and performance of electromigration on fine pitch Cu pillar with different bump structure for flip chip packaging," *Proc. - Electron. Components Technol. Conf.*, vol. 2015-July, no. 153, pp. 626–631, 2015, doi: 10.1109/ECTC.2015.7159657.

[72] S. H. Kim and J. Yu, "Secondary IMC formation induced by Kirkendall voiding in Cu / Sn – 3 . 5Ag solder joints," 2010, doi: 10.1557/JMR.2010.0232.

[73] J. Y. Kim, J. Yu, and S. H. Kim, "Effects of sulfide-forming element additions on the Kirkendall void formation and drop impact reliability of Cu / Sn – 3 . 5Ag solder joints," *Acta Mater.*, vol. 57, no. 17, pp. 5001–5012, 2009, doi: 10.1016/j.actamat.2009.06.060.

[74] Y. Wang *et al.*, "Effect of intermetallic formation on electromigration reliability of TSV-microbump joints in 3D interconnect," *Proc. - Electron. Components Technol. Conf.*, no. May, pp. 319–325, 2012, doi: 10.1109/ECTC.2012.6248849.

[75] Y. Jung and J. Yu, "Electromigration induced Kirkendall void growth in Sn-3 . 5Ag / Cu

solder joints," vol. 083708, 2014, doi: 10.1063/1.4867115.

[76] Y. Liu, Y. Chu, and K. N. Tu, "Scaling effect of interfacial reaction on intermetallic compound formation in Sn / Cu pillar down to 1 m m diameter," *Acta Mater.*, vol. 117, pp. 146–152, 2016, doi: 10.1016/j.actamat.2016.07.004.

[77] E. Kirkendall, L. Thomassen, and U. Clair, "Rates of Diffusion of Copper and Zinc in Alpha Brass," *Am. Inst. Min. Metall. Eng.*, vol. 967, no. Technical publication, 1938.

[78] E. A. Brandes, Ed., *Smithells metals reference book, sixth edition*. London: Butterworth Publishers, 1983.

[79] K. Hoshino, Y. Iijima, and K. ichi Hirano, "INTERDIFFUSION AND KIRKENDALL EFFECT IN Cu-Sn ALLOYS.," *Transactions of the Japan Institute of Metals*, vol. 21, no. 10. pp. 674–682, 1980, doi: 10.2320/matertrans1960.21.674.

[80] B. F. Dyson, T. R. Anthony, and D. Turnbull, "Interstitial diffusion of copper in tin," *J. Appl. Phys.*, vol. 38, no. 8, p. 3408, 1967, doi: 10.1063/1.1710127.

[81] D. C. Yeh and H. B. Huntington, "Extreme Fast-Diffusion System: Nickel in Single-Crystal Tin," *Phys. Rev. Lett.*, vol. 53, no. 15, pp. 1469–1472, 1984, doi: 10.1103/PhysRevLett.53.1469.

[82] Y. Wang, S. H. Chae, J. Im, and P. S. Ho, "Kinetic study of intermetallic growth and its reliability implications in Pb-free Sn-based microbumps in 3D integration," *Proc. - Electron. Components Technol. Conf.*, pp. 1953–1958, 2013, doi: 10.1109/ECTC.2013.6575845.

[83] Y. Li and D. Goyal, Eds., *3D Microelectronic Packaging.*, vol. 57, no. 1. The Springer Series in Advanced Microelectronics, 2017.

[84] J. Park, S. Kim, M. Jeong, and Y. Park, "Effect of Cu – Sn intermetallic compound reactions on the Kirkendall void growth characteristics in Cu / Sn / Cu microbumps Effect of Cu – Sn intermetallic compound reactions on the Kirkendall void growth characteristics in Cu / Sn / Cu microbumps," *Jpn. J. Appl. Phys.*, vol. 06, pp. 2–6, 2014.

[85] L. Yin and P. Borgesen, "On the root cause of Kirkendall voiding in Cu 3 Sn," *J. Mater. Res.*, pp. 455–466, 2011, doi: 10.1557/jmr.2010.47.

[86] M. O, G. Vakanas, N. Moelans, M. Kajihara, and W. Zhang, "Formation of compounds and Kirkendall vacancy in the Cu-Sn system," *Microelectron. Eng.*, vol. 120, pp. 133–137, 2014, doi: 10.1016/j.mee.2013.09.009.

[87] S. Kumar, C. A. Handwerker, and M. A. Dayananda, "Intrinsic and Interdiffusion in Cu-Sn System," *J. Phase Equilibria Diffus.*, no. 32, pp. 309–319, 2011, doi: 10.1007/s11669-011-9907-9.

[88] C. C. Wei, C. F. Chen, P. C. Liu, and C. Chen, "Electromigration in Sn-Cu intermetallic

compounds," *J. Appl. Phys.*, vol. 105, no. 2, pp. 3–8, 2009, doi: 10.1063/1.3072662.

[89] W. G. Moffatt, G. E. C. Research, and D. C. T. M. Operation, *The Handbook of Binary Phase Diagrams*, no. v. 4. General Electric Company, Corporate Research and Development, Technology Marketing Operation, 1981.

[90] Y. . Huang, C. . Chen, B. . Lee, H. . Chen, C. . Wang, and A. T. Wu, "In Situ Electromigration in Cu-Sn and Ni-Sn Critical Solder Length for Three-Dimensional Integrated Circuits," *J. Electron. Mater.*, vol. 45, no. 12, pp. 6163–6171, 2016, doi: 10.1007/s11664-016-4874-x.

[91] J. Ni, A. Maniatty, Y. Liu, J. Hao, and M. Ring, "Electromigration Induced Stress in Lead-Free Solder Joints," in *IEEE 66th Electronic Components and Technology Conference*, 2016, pp. 538–543, doi: 10.1109/ECTC.2016.371.

[92] I. A. Blech, "Electromigration in thin aluminum films on titanium nitride," *J. Appl. Phys.*, vol. 47, no. 4, pp. 1203–1208, 1976, doi: 10.1063/1.322842.

[93] D. R. Smith, T. A. Siewert, S. Liu, and J. C. Madeni, "Database for Solder Properties with Emphasis on New Lead-free Solders," *National Institute of Standards and Technology & Colorado School of Mines*, 2002. https://www.nist.gov/publications/database-solder-properties-emphasis-new-lead-free-solders.

[94] Y. Liu, Y. Chen, S. Gu, D. Kim, and K. N. Tu, "Fracture reliability concern of (Au , Ni) Sn 4 phase in 3D integrated circuit microbumps using Ni / Au surface fi nishing," *Scr. Mater.*, vol. 119, pp. 9–12, 2016, doi: 10.1016/j.scriptamat.2016.02.025.

[95] Z. Zhao, S. Yanga, A. Hua, and M. Ua, "Influence of solder layer thickness on the interfacial reaction in Ni / Sn / Cu system," in *16th International Conference on Electronic Packaging Technology*, 2015, pp. 447–449, doi: https://doi.org/10.1109/ICEPT.2015.7236623.

[96] S. Annuar, R. Mahmoodian, M. Hamdi, and K. N. Tu, "Intermetallic compounds in 3D integrated circuits technology: a brief review," *Sci. Technol. Adv. Mater.*, vol. 18, no. 1, pp. 693–703, 2017, doi: 10.1080/14686996.2017.1364975.

[97] N. Saunders and A. . Miodownlk, "The Cu-Sn (Copper-Tin) System," *Bull. Alloy Phase Diagrams*, vol. 11, no. 3, pp. 278–287, 1990.

[98] K. N. Tu and R. D. Thompson, "Kinetics of interfacial reaction in bimetallic CuSn thin films," *Acta Metall.*, vol. 30, no. 5, pp. 947–952, 1982, doi: 10.1016/0001-6160(82)90201-2.

[99] A. Zribi, A. Clark, L. Zavalij, P. Borgesen, and E. J. Cotts, "The growth of intermetallic compounds at Sn-Ag-Cu solder/Cu and Sn-Ag-Cu solder/Ni interfaces and the associated evolution of the solder microstructure," *J. Electron. Mater.*, vol. 30, no. 9, pp. 1157–1164, 2001, doi: 10.1007/s11664-001-0144-6.

[100] Z. F. Wu, J. Wu, L. Zhang, C. Liu, and R. Wu, “Solid solubility extension of copper-tin immiscible system during mechanical alloying,” *Mat.-wiss. u. Werkstofftech*, vol. 49, pp. 54–60, 2018, doi: 10.1002/mawe.201700125.

[101] C. L. Liang and K. L. Lin, “Non-equilibrium supersaturation behavior in a Cu/Sn/Cu interconnect induced by room temperature electromigration,” *J. Alloys Compd.*, vol. 789, pp. 336–344, 2019, doi: 10.1016/j.jallcom.2019.03.055.

[102] Y. T. Chiu, C. H. Liu, K. L. Lin, and Y. S. Lai, “Supersaturation induced by current stressing,” *Scr. Mater.*, vol. 65, no. 7, pp. 615–617, 2011, doi: 10.1016/j.scriptamat.2011.06.041.

[103] J. Eckert *et al.*, “Mechanically driven alloying and grain size changes in nanocrystalline Fe Cu powders MechanicaHy driven alloying Fe-Cu powders and grain size changes,” *J. Appl. Phys.*, vol. 2794, no. 73, pp. 2794–2802, 1993, doi: 10.1063/1.353055.

[104] J. Y. Huang, Y. K. Wu, and H. Q. Ye, “Allotropic transformation of cobalt induced by ball milling,” *Acta Mater.*, vol. 44, no. 3, pp. 1201–1209, 1996, doi: 10.1016/1359-6454(95)00234-0.

[105] A. Benghalem and D. G. Morris, “Structural evolution during intense ball milling of copper-niobium mixtures,” *Scr. Metall. Mater.*, vol. 27, no. 6, pp. 739–744, 1992, doi: 10.1016/0956-716X(92)90498-4.