

RELIABILITY ENHANCEMENT OF HETEROGENEOUS 3D
INTEGRATED CIRCUIT AND CHARACTERIZATION OF
THERMAL INTERFACE MATERIAL

by

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DISSERTATION

Submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy at
The University of Texas at Arlington
August 2020

Arlington, Texas

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Acknowledgements

I would like to express my gratitude to Professor Dereje Agonafer for constantly motivating and encouraging me, his invaluable advice during my doctoral studies, and providing me an opportunity to work at Electronic, MEMS & Nanoelectronics Systems Packaging Center (EMNSPC). It has been a wonderful experience working with him in the research projects and learn from the conference visits. I would also like to thank him for serving as the committee chairman.

I am grateful to Dr. Abdolhossein Haji-Sheikh, Dr. Miguel Amaya, Dr. Md Rassel Raihan, Dr. Zeynep Çelik-Butler and Dr. Fahad Mirza for serving on my committee, providing me valuable inputs, and giving numerous learning opportunities.

I would like to thank all the students at EMNSPC for their support. Thanks to all the staffs for supporting me throughout my academic career the University of Texas at Arlington. Specially thanks to Lanie Gordon, Wendy Ryan, Flora Pinegar, Ayesha Fatima, Kathy Priester, and Mike Baker for assisting me during my studies at the University of Texas at Arlington. You all have been wonderful.

I am thankful to all my Professors who have been helping and encouraging me through my academic career. I also would like to mention my friends for supporting and inspiring me.

Finally, I would like to acknowledge the financial, academic, and technical support of the University of Texas at Arlington.

July 30, 2020

Dedication

To my mother who inspired me in every aspect of my life.

To my father who inspired me to become an engineer and taught me how to be a good person.

I would like to dedicate to my grandparents who inspired me to become successful specially my maternal grandparents for their hard work towards my career.

I would like to dedicate to my beloved wife for being with me throughout the journey.

I would like to dedicate to my siblings specially to my younger brother for supporting me.

I would like to dedicate to my cousins for all the joyous moments and being good influence.

I would like to extend my profound appreciation to Professor Dereje Agonafer for his mentorship and advice.

I would not be here without any of you.

Abstract

RELIABILITY ENHANCEMENT OF HETEROGENEOUS 3D INTEGRATED CIRCUIT AND CHARACTERIZATION OF THERMAL INTERFACE MATERIAL

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The University of Texas at Arlington, 2020

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Electronic products require high functional integration in small footprints with lower cost. At the same time, it is required to maintain effective communication between the IC's and the electronic systems. Various challenges are arising due to these factors such as signal processing time, heat dissipation, structural integrity, chip package interaction which need to be dealt effectively during electronic packaging. 3D stacking of the processors and the components accomplishes these goals and in high computing application it reduces the delay. Through-silicon via (TSV) is the heart of 3D integration, and the stacking of chips is emerging now as a powerful tool to converge the demands of integrated circuit (IC) packages. In 3D TSV dies are stacked on top of another so heat trapped in a small region which is difficult to dissipate that may cause failures in electronic devices. Since the TSV's go through dies, and dies have transistors, the transistors cannot be placed in a thermally stressed area. It is challenging to dissipate heat from the dies which are stacked. Due to the heat, thermal stresses developed at the interfaces of different materials, which causes structural integrity issues like cracking and warpage. According to coefficient of thermal expansion (CTE) values different materials try to expand and compress differently. Also, the interface of Si/SiO₂ is brittle and hence crack can form in Cu core and in

dielectric layer of TSV. In this study, structural integrity during die attachment process of a 2-die 3D TSV package is studied. Finite element methods have been used to examine the thermo-mechanical stresses and fracture parameters of the structure of 3D TSV package. The Stress intensity factor is analyzed thereby highlighting the prevalent modes of cracking in TSV. Stress intensity factor arising in the TSV and J-Integral with respect to design changes are studied at different crack positions on TSV.

Electronic devices generally produce heat during normal operation. Heat dissipation of the semiconductor packages has become one of the limiting factors in miniaturization. Thermal interface material plays a significant role in the electronic devices for transferring heat since it enhances the heat transfer rate between contact surfaces. It is one of the essential materials used in electronic packages. When two solid surfaces are attached, there can be microvoids between the surfaces. These voids are generally filled by air, which increases the thermal resistance. Without good thermal contact, heat-dissipating devices cannot dissipate heat efficiently. For good thermal contact, thermal interface materials are needed. Characterization of the properties of thermal interface materials has gained importance since it plays a critical role in heat dissipation and life cycle of the electronic packages. Thermal interface materials are made of different compounds. Silicone is one of the compounds which is widely used in thermal gap filler materials. Also, there are thermal interface materials that do not contain silicone. In this study, silicone and silicone-free thermal interface materials are studied. Properties such as complex modulus, coefficient of thermal expansion, dielectric properties are studied, and the effect of silicon content is investigated. The effect of thermal aging on the properties of silicone based and silicone free thermal interface materials are also analyzed in this study.

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Chapter 1

Introduction

The need for higher computing power is increasing rapidly. With the increasing demand, it has become indispensable to make efficient devices with cheaper cost. At the beginning, with the invention of integrated circuit is 1959, higher computing power was achieved primarily through density scaling and commensurate performance enhancement of transistors because of continuously scaling down the device dimensions in a harmonious manner. It has resulted in a steady doubling of device density from one technology node to another [1]. As the demand for electronic devices increased, devices needed to be more efficient but the space requirement for the device has shrunk over time. So multiple dies need to be stacked in a small space. Through-silicon via (TSV) enable us to stack multiple dies in a very small space. Stacking multiple dies in a small space has different mechanical and thermal issue. In this work thermal management of the Through-silicon via has been studied for 3D stacked devices.

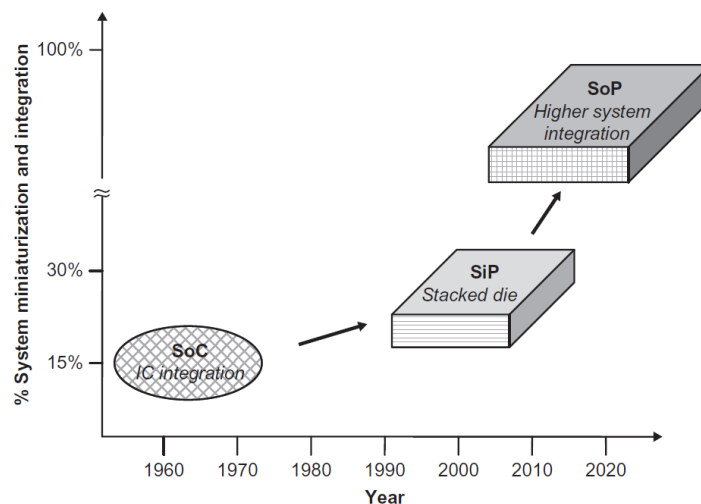


Fig. 1.1: Miniaturization and integration trends of ICs in 1960s to systems in the 2020s. IC, integrated circuit; SiP, system-in package; SoC, system-on-chip; SoP, system-on-package [2].

As shown in Fig. 1.2, the miniaturization trend in transistors continued to follow Moore’s law reducing to 32 and 22 nm sizes and reaching beyond complementary metal-oxide semiconductor devices. At the same time, a second trend of More than Moore is the functional diversification of components increases in a package including IC chips, passives, MEMS, sensors, and biochips. A third trend is system integration and packaging innovations. This will be benefited from the other two trends, smaller transistors, and more diverse devices.

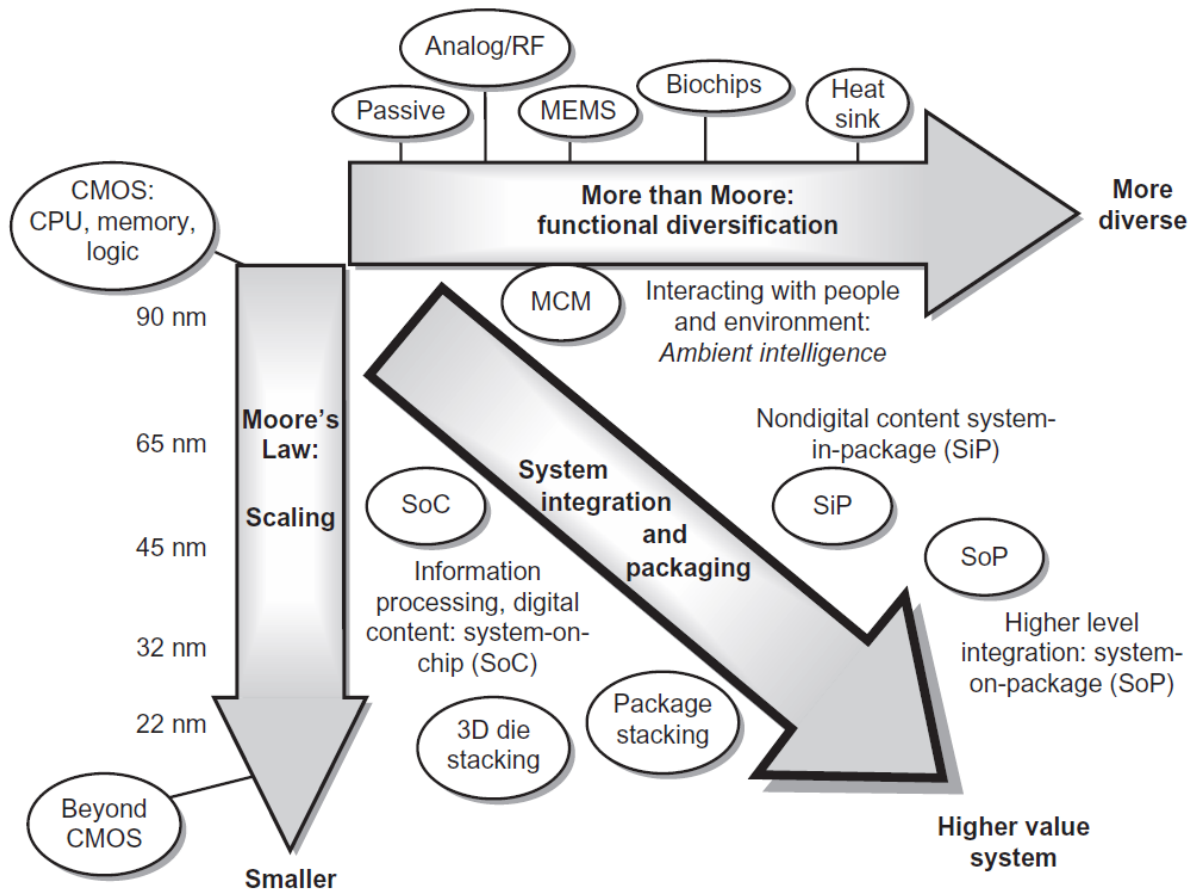


Fig. 1.2: Moore’s law, “More than Moore” approaches combined with system integration for development of high-value systems. CMOS, complementary metal-oxide semiconductor; CPU, central processing unit; MCM, multichip module; MEMS, microelectromechanical systems; RF, radio frequency [2].

1.1 SoC, SiP and 3D Integration

Systems-on-chip (SoCs) contain an incredible amount of functionality in a single silicon die. The SoCs generally include a processor, digital logic, memory, and analog components, along with embedded software. But traditional single-die SoCs have disadvantages. One of the disadvantages is all components are placed on the same die at the same process node, at the same time analog and RF design at advanced process nodes is extremely challenging. One of the other challenges for single-die SoCs is mixed-signal integration and verification which is placing digital and analog circuitry in close proximity can cause many problems. Possibly the biggest concern with SoC design today is the rising development costs [3].

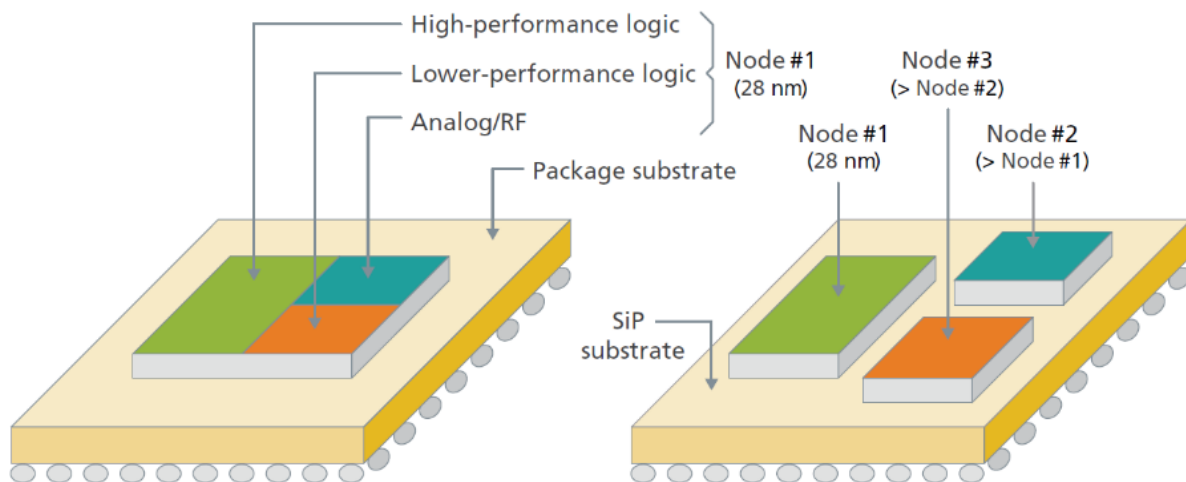


Fig. 1.3: System-on-Chip (SoC) compared to System-in Package (SiP) [3].

An alternative to single-die SoCs is to place multiple silicon die into a single package. It will be possible to use a 90nm process for analog/RF circuitry, and a 28nm process for digital logic as shown in Fig. 1.3. System-in-package (SiP) and multi-chip module (MCM) have been used to refer to multi-die packaging technologies. In this technology multiple dies are mounted on a common substrate that is used to connect them together [3].

Three-dimensional (3D) integration offers numerous electrical advantages like shorter interconnection distances between different dies in the stack, reduced signal delay, reduced interconnect power and design flexibilities [4]. The dies in the package shown in Fig. 1.4 is a three-dimensional (3D) package, connected peripherally with wires, this type of package is called wirebonded package. Dies stacked in package shown in Fig. 1.5 are interconnected with through-silicon vias (TSVs). Using TSVs multiple dies are stacked and dies can be interconnected through dies. It enables us to achieve high functionality, high performance, low power requirements, high bandwidth, and small form factor [4]. With higher functionalities 3D TSV packages brings new sets of challenges.

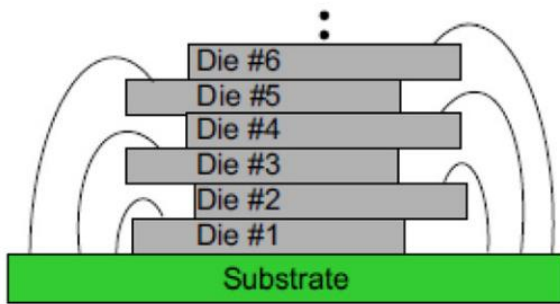


Fig. 1.4: Die stacked 3D wire bonded package [4]

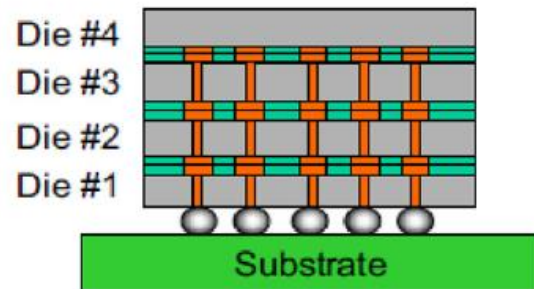


Fig. 1.5: Die stacked 3d TSV packages [4]

In 3D integrated circuit vertical electrical interconnection within each chip are provided using TSVs. The TSVs are made in each thinned chip by drilling holes using either laser ablation or deep reactive ion etching (DRIE) [4]. After that, the sides of the holes are coated with an insulator, followed by a thin conductor onto which the via metal is electrodeposited. Electrical interconnection between adjacent chips in the stack can be achieved by conventional C4 bump or low-profile solder or thermocompression bonds to reduce the inter-chip spacing [5]. TSVs can be fabricated at pitches of tens of microns so interconnect densities can be achieved that are more

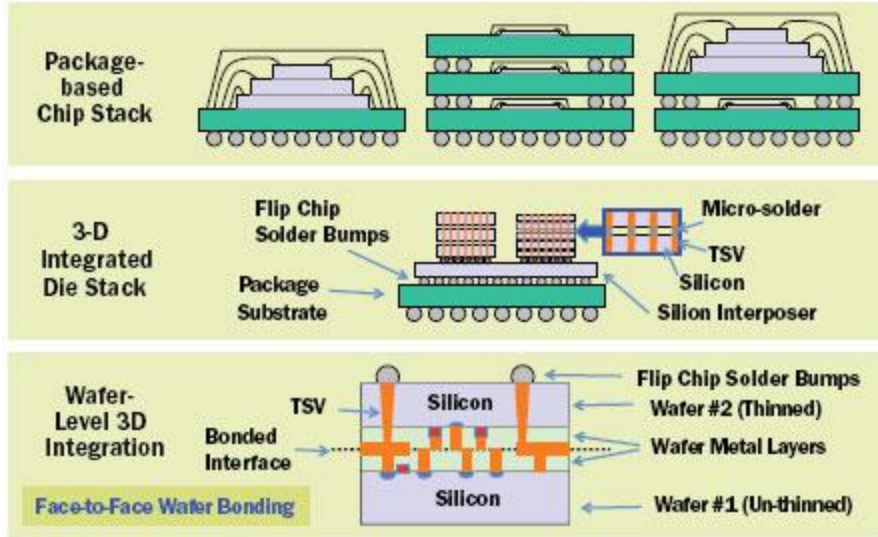


Fig. 1.6: Major types of 3D packages along with specific examples [6]

than three orders of magnitude higher than of the package-based stacking technology. This technology can accommodate stacks with larger numbers of dies within a smaller form factor and with better signal integrity than is possible with wire-bonded stacked dies [6]. Different types of packages using this technology are shown in Fig. 1.6.

1.2 Application of Thermal Interface Materials

With the advent of 5G technology the importance of 3D integration is even more important. Consumer electronic products such as digital cameras, cellphones etc. requires high fictional integration in small footprints with lower cost. Due to miniaturization coupled with the requirement of high density, performance and, more features per square centimeter of Printed Circuit Board so engineers have been forced to think differently. 3D stacking of the processors and the components accomplishes the goals and in high computing application it reduces the delay [7].

Electronic packages are made with different materials. The material properties of the packages needs to fit the requirements of the packages. It is not possible to achieve desirable

outcome from a device without using a material that functions properly for that work. Thermal interface material plays a significant role in the electronic devices. It is one of the most important materials that is used in an electronic package. The electronic devices need to dissipate a lot of heat especially while it is operating in its maximum capacity or close to it. Materials of high thermal conductivity are necessary for efficient heat transfer for the purposes purpose of heating or cooling. In electronic industry one of the most critical need is material of higher thermal conductivity for the thermal interface materials [8]. Heat dissipating devices such heat spreader or heat sink is attached on die to remove the heat. The contact between the die and the heat removing device contains micro-voids which increases significant thermal resistant.

Thermal interface material is used to reduce the thermal resistance between the die and the heat removing component. There are various commercially available TIMs but these are not limited to Greases, Elastomeric pad and phase change materials rather TIMs can be fabricated by dispersing high conductivity particles such as metals (silver, copper) or ceramics (Aluminum Oxide, Zinc Oxide or Boron Nitride) within organic phase such as silicone grease. The aim is to have a material with similar mechanical properties as organic phase but a higher effective thermal conductivity [9]. The characterization “Beginning of Life” performance of TIMs is not sufficient since performance can degrade with usage [10]. Most of the thermal interface material that is available contains silicone. There are thermal Interface materials that do not contain silicone. The properties of silicone free thermal interface material are not as prevalent as silicone based thermal interface material. In this work the effect of temperature will be analyzed for silicone based and silicone free thermal interface material.

Chapter 2

Literature Review

2.1 Heterogeneous Integration

Heterogeneous integration uses packaging technology to integrate dissimilar chips, photonic devices, or components with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem. System-in-package (SiP) is very similar to heterogeneous integration, except heterogeneous integration is for finer pitches, more inputs/outputs, higher density, and higher performance [11]. 3D ICs with through-silicon vias (TSVs) meet the demand of increasing density, higher bandwidths, and lower power [12].

There are different ways researchers classified different Heterogeneous packaging systems. In general, it can be classified as heterogeneous integrations on organic substrates, heterogeneous integrations on silicon substrates (with TSV-interposers), heterogeneous integrations on silicon substrates (with TSV-less interposers such as bridges), heterogeneous integrations on fan-out RDL (redistribution-layer) substrates, and heterogeneous integrations on ceramic substrates. In next few years there will be more implementations of a higher level of heterogeneous integrations on these various substrates, whether it is for performance, form factor, power consumption, signal integrity, or cost [11].

2.1.1 Through-silicon via (TSV)

Through-silicon via (TSV) is a vertical electrical connection passing through a silicon die. These are copper vias with diameters that may range from 1 to 30 microns. A 3D IC using TSVs involves two or more dies connected together using TSVs. Three-dimensional (3D) silicon

integration of active devices with TSVs, thinned silicon, and silicon-to-silicon fine-pitch interconnections offers many product benefits. Advantages of these emerging 3D silicon integration technologies can include the following: power efficiency, performance enhancements, significant product miniaturization, cost reduction, and modular design for improved time to market [13]. It offers compelling power, performance, and form factor advantages in many application. It may curb the escalating costs of SoC development. It is possible to stack multiple dies from different process nodes. It is not necessary to move all system components, including analog and RF, to a single process node.

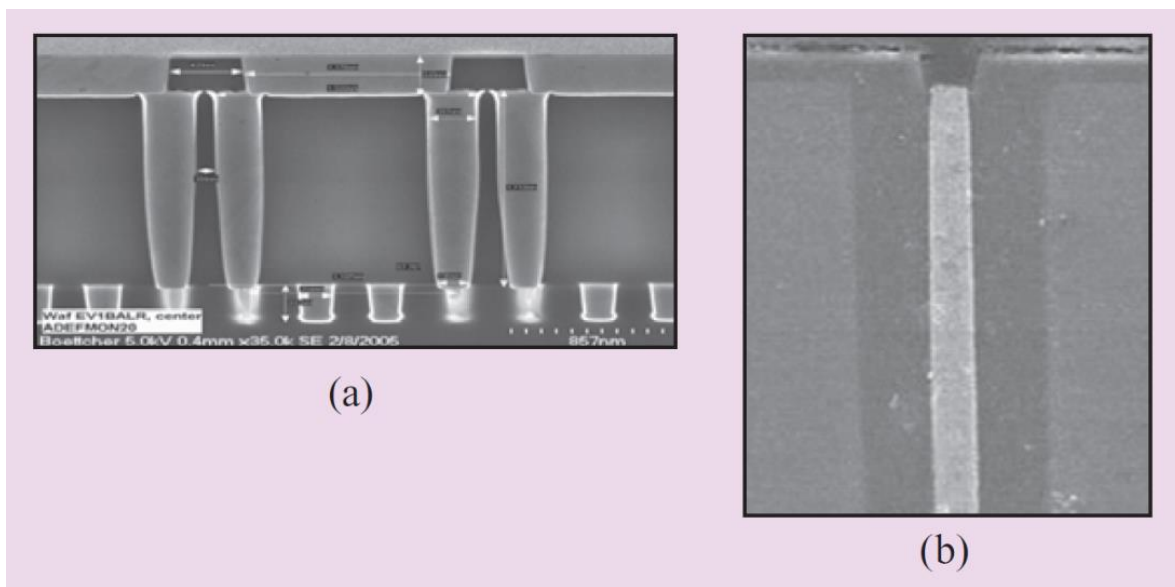


Fig. 2.1: Examples of TSV cross-sections: (a) 0.14- μm -diameter TSV; (b) 2- μm -diameter TSV [13]

2.1.2 Heterogeneous 3D Stacking and 3D Integrated Circuit

3D stacking technology enables the integration of different technologies onto a single chip and provides performance benefits by decreasing communication latency. At the same time, stacking resources vertically makes it harder to remove the generated heat, leading to elevated on-chip temperatures. The downside of the high on-chip temperature is a limiting factor on the

performance and reliability of the process or and incurs higher cooling costs. To get the true potential of 3D-stacked dies, accurate thermal modeling, design-stage thermal analysis, and development of efficient runtime management strategies are essential [1] . Heat is a major problem in electronic packages and specially in 3D packages, removing heat from the system is a big challenge. The heat trapped in between the stacked die is difficult to remove and many causes of failure. Thermal stress can be developed due to CTE mismatch in different materials such as silicon, copper if heat cannot be removed efficiently [14][15][16] [17]. Following are some of the key stacking approaches.

2.1.2.1 Die to Die (D2D) 3DIC Structure

In this approach electronic components are built on multiple dies, which are then aligned and bonded. Die to die bonding stacks known good quality dies together. It ensures manufacturing yield is controlled at a sufficiently high level before attachment. TSV cost is high and it requires a long lead time to make Heterogeneous stacking. But it is easy able to realize the wide band and low power consumption compare than Fan-our WLP process.

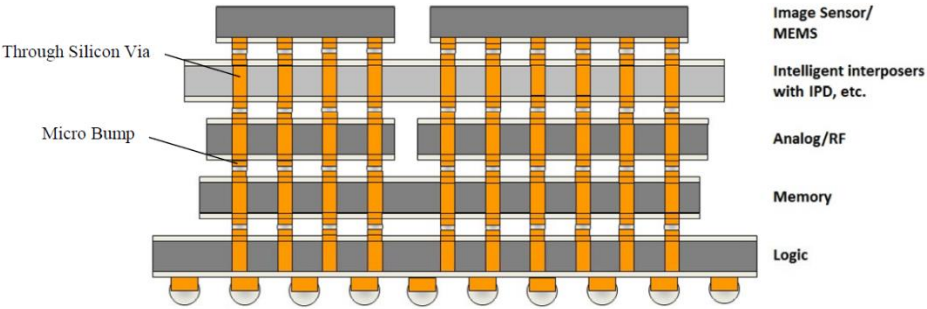


Fig. 2.2: Heterogeneous 3D IC using D2D process [18]

2.1.2.2 Die to Wafer (D2W) 3DIC Structure

In this approach electronic components are built on two semiconductor wafers. Same as the wafer-on-wafer method, thinning and TSV creation are performed either before or after bonding and additional die may be added to the stacks before dicing.

2.1.2.3 Wafer to wafer (W2W) 3DIC Structure

In this process electronic components are built on two or more semiconductor wafers, which are then aligned, bonded, and dices into 3D ICs. A W2W 3DIC structure is shown in Fig.4.

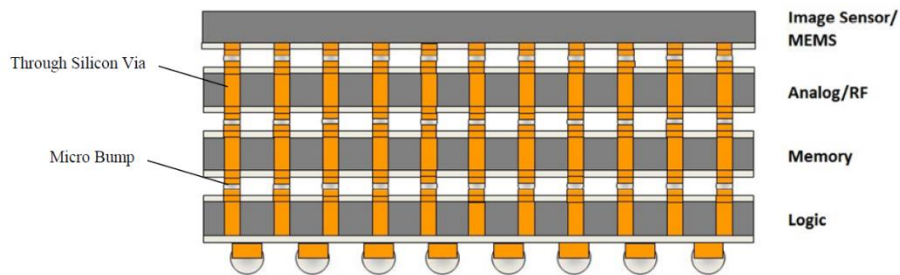


Fig. 2.3: Heterogeneous 3D IC using W2W process [18]

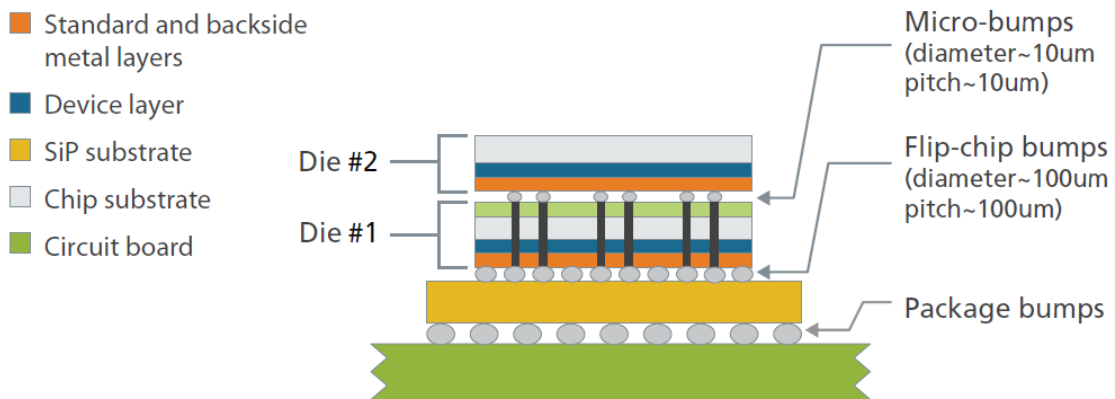


Fig. 2.4: A simple 3D IC using TSVs [3]

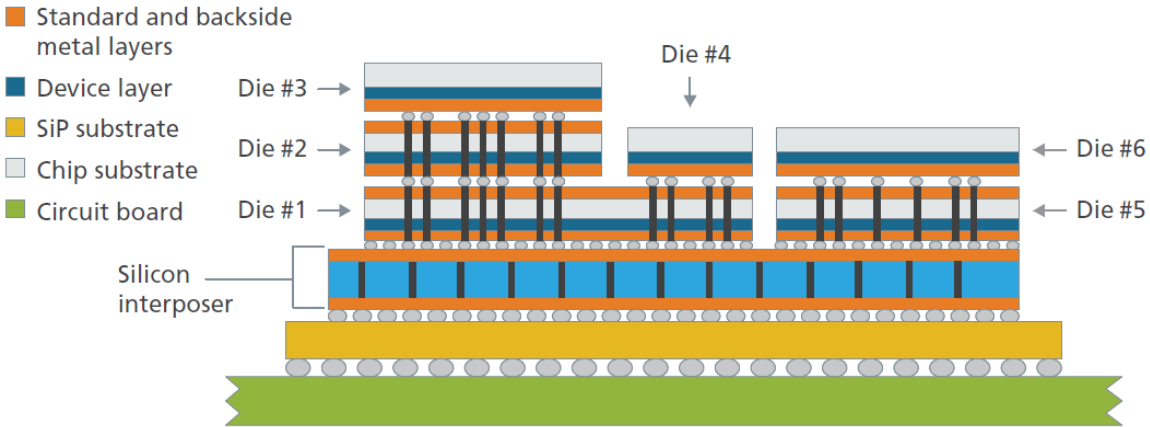


Fig. 2.5: More complex 3D IC using TSVs and 6 die [3]

3D stacking provides better performance at the same time it decreases communication latency. Stacking resources vertically makes it harder to remove the generated heat, leading to elevated temperature at the bottom of the stack as the heat from the bottom chip will have to go through the other chip. During reflow process the package cools down from high temperature. The expanded Cu can press the surrounding Si substrate and degrade the performance of those transistors near the TSV. One of the major concerns associated with TSV is the reliability issue of the TSV based devices due to the CTE mismatch between silicon and copper.

2.2 Thermal Interface Material

Heat dissipation is one of the central issue due to the increasing demands for microprocessors. Efficient heat dissipation of electronic devices maintaining reliability is a major issue in electronic industries. Researchers are investigating different cooling strategies [19] [20] [21]. Prasher et al. studied contact resistance of curable polymer gel thermal interface materials that have different mechanical properties due to difference in the rheology of the polymers. They proposed a semi-analytical model for the contact resistance of cured gel TIMs. This model shows that contact resistance of cured gel TIMs depends on the roughness of the substrate, thermal

conductivity of the TIM, applied pressure, and the shear modulus of the TIMs. Grease pump-out problem due to temperature cycling was systematically studied [22]. Yu et al. studied two kinds of silicone grease containing graphene nanoparticles or reduced graphene oxide were prepared and investigated thermophysical properties [23]. Sun et al. investigated novel nanocomposite thermal interface material (Nano-TIM) consisting of a silver coated polyimide network and the indium matrix. Nano-TIM is used for heat dissipation in integrated circuits and electronic packaging. In this study shear strength of the Nano-TIM was investigated with DAGE-4000PSY shear tester [24]. In power electronics package, a grease layer forms the interface between the direct bond copper (DBC) layer or a baseplate and the heat sink. This grease layer has the highest thermal resistance of any layer in the package. Narumanchi et al. describes the progress in characterizing the thermal performance of some conventional and novel thermal interface materials. They acquired, modified, and improved an apparatus based on the ASTM D5470 test method and measured the thermal resistance of various conventional greases. They also measured the performance of phase-change materials and thermoplastics through the ASTM steady-state and the transient laser flash approaches, and compared the two methodologies [25].

Goel et al. studies the importance of considering TIM degradation in mobile applications. They studied various TIM characterization approaches prevalent in industry and found that there is also wide disparity in testing methodologies used across industry to evaluate its performance maps with usage. Also suggested a set of characterization techniques for better TIM evaluation [10].

Developing new thermal interface materials (TIMs) is a key activity to meet package thermal performance requirements for future generations of microprocessors. Deppisch et al. studied the failure mechanisms and reliability performance of indium solder TIM as a function of

integrated heat spreader metallization thickness, TIM bond line thickness, and die size. Also studied the steps taken to improve its temperature cycle performance. They performed different analysis using thermal resistance measurements, scanning-electron microscopy, scanning-acoustic microscopy, and transmission- electron microscopy to characterize the solder TIM thermal performance, interfacial microstructure, and failure mechanisms [26].

Liu et al. in their work classified existing thermal interface materials and analyzed their advantages and disadvantages. They also reviewed state-of-the-art research with an emphasis on those materials based on various carbon allotropes, such as graphite, carbon nanotubes (CNTs) and fibers. Other kinds of fillers with high thermal conductivity, such as silicon carbide, boron nitride, aluminum nitride, aluminum oxide, silver and other metals, have also been extensively studied [27]. Misrak et al. characterized the material properties of thermally conductive gap fillers and studied the change in properties due to thermal aging [28]. Ahsan et al. used experimental techniques to evaluated thermo-physical properties such as heat capacity, thermal conductivity and diffusivity of metallic powder [29]. Chen et al. introduced functionalized carbon nanotubes (CNTs) into silicone grease to accompany the subsistent metallic oxide particles. The goal was enhancing the thermal contact conductance of the composite grease as thermal interface materials (TIMs). They found that the thermal impedance of the silicone grease could be further decreased by 35% with the addition of 2 wt.% carboxylated CNTs [30]. Zhang et al. fabricated a novel composite by rolling graphene sheets into vertically aligned graphene film (VAGF) then penetrating liquid polydimethylsiloxane (PDMS) into it. The thermal conductivity of the VAGF/PDMS composite is up to $614.85 \text{ Wm}^{-1} \text{ K}^{-1}$, an improvement per wt% of as high as 3329% compared to pure PDMS. The enhancement occurred due to the vertical alignment of graphene films with high in-plane thermal conductivity, thus form a rapid and effective heat-transfer path

[31]. Liu et al. investigated the phase change behavior of organic and inorganic phase change materials, such as paraffin wax, microcrystalline wax, $\text{Na}_2\text{SO}_4 \cdot 10\text{H}_2\text{O}$ and $\text{CaCl}_2 \cdot 6\text{H}_2\text{O}$ by differential scanning calorimetry. They also determined the melting and solidification temperatures, supercooling, heat of fusion and thermal cycling stability of these materials, with and without additives. [32].

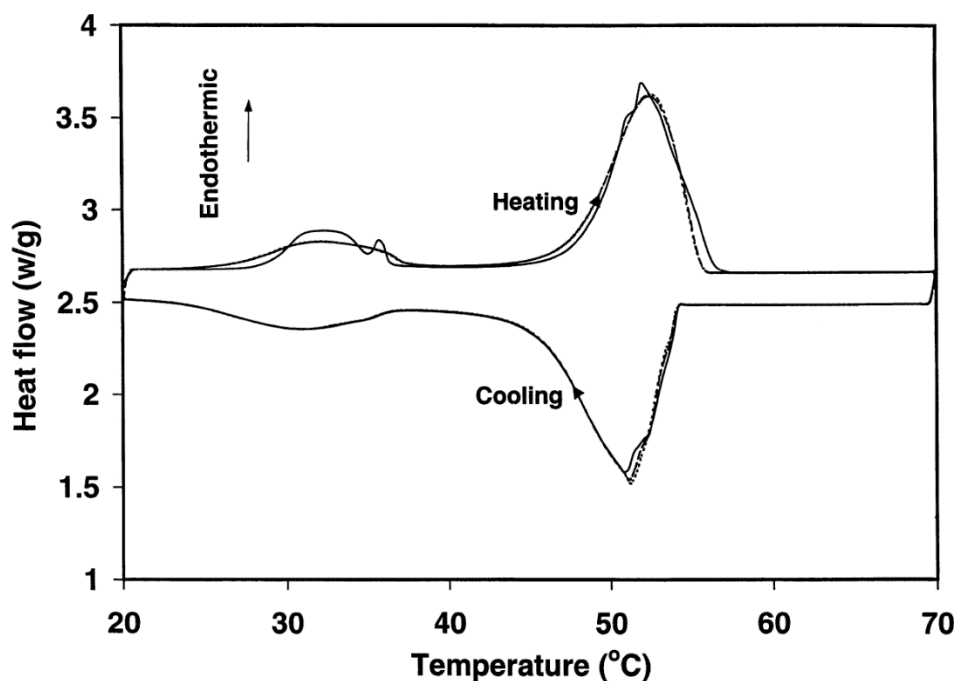


Fig. 2.6: DSC curves of paraffin wax: (-) first cycle; (- -) second cycle; (. .) third cycle [32]

Yu et al. investigated the thermophysical properties of silicone grease containing graphene nanoplatelets or reduced graphene oxide. They found that when the volume fraction was 1%, the reduced graphene oxide was the most effective additive for enhancing the heat transfer properties of silicone, and graphene nanoplatelet was slightly inferior to the former. And when the concentration was enhanced, the viscosity of silicone grease containing reduced graphene oxide became very large because of its rich pore structure [23].

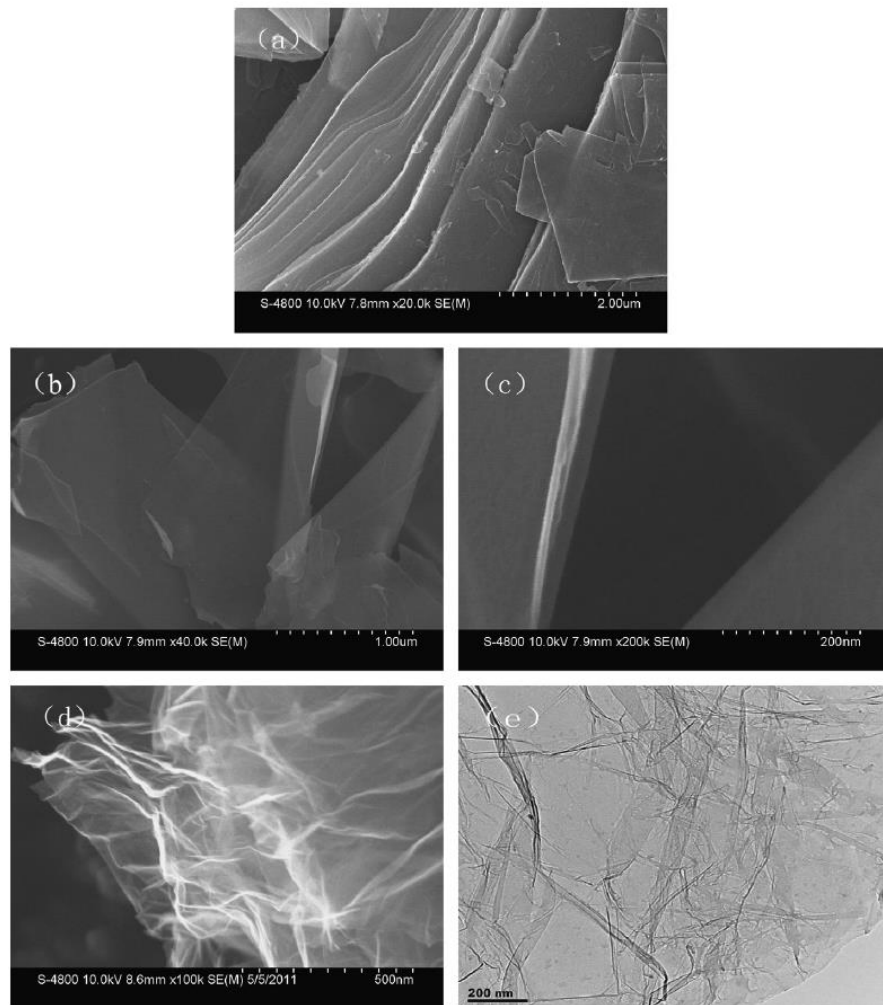


Fig. 2.7: The typical scanning SEM and TEM images of graphite, GNP and RGO. (a) graphite, SEM; (b)GNP, SEM; (c) GNP, TEM; (d) RGO, SEM; (e) RGO, TEM [23]

Chapter 3

Reliability Enhancement of Heterogeneous 3D Integrated Circuit

3.1 Heterogeneous 3D Integrated circuit

Reliability is a major issue in electronic packages. The enhancement of reliability can help an electronic package to perform more efficiently. One of the main interests 3D integration is to reduce global interconnect lengths, to increase circuit functionality and to enable new 3D circuit architectures [33]. In heterogeneous 3D Integrated Circuit reliability and thermal management is even more important. Since multiple dies are attached in a heterogenous integrated 3D IC. So, reliability of the package is critical for optimum performance of the device.

3.2 Challenges in 3D TSV package

3D integrated circuit became more efficient when TSVs are used. There are challenges associated with this technology. Some of the challenges were addressed during packaging development are temporary Bonding and Debonding with Large C4 Solder Bumps, Handling Large, Thin Die for Mass Reflow and Warpage Control for Top Die Attach with Micropillars Backside RDL Processing and Underfill Resin Bleed [34]. Previously 3D integrated circuits were developed using wire bonds which creates RC delay, power loss issues, and only utilizes peripheral I/Os, with reduced functionality. Numerous functionalities and more input and output, less RC delay can be achieved by TSV. 3D IC offers the advantages of design flexibility, high bandwidth, smaller footprint, efficient utilization of chip real estate (CRE), etc., with Through-silicon via technology posing more scope with its shorter die-to-die interconnects, low RC delay and parasitic resistance [35].

3.3 Limitations of TSV Technology

Tremendous research effort has been devoted to the development and improvement of various TSV fabrication process steps. However, relatively less work has addressed the TSV reliability issues. In literature numerous studies on the effect of board thickness on the thermo-mechanical reliability of Wire Bond Chip package, BGA and WLCSP packages are prevalent [36] [37] [38] [39] [40]. Studies are performed on board level solder joint reliability assessment of Megtron and FR-4 boards under different conditions such as power cycling and thermal cycling [41] [42]. Limited studies on TSV have focused on the analysis of thermo-mechanical failure mechanism, and most of these studies have approached this problem empirically. The heat trapped in between the stacked die is difficult to remove and cause many failures. The dies are made of silicone. Due to the unique feature of TSV and the high mismatch in the coefficient of thermal expansion between silicon substrate, metal core, material and dielectric layer, large stress may develop, and these stresses may lead to various reliability issues [35] [43]. Materials with different CTE values try to expand and compress differently. One of the techniques to minimize the issue is to evaluate the critical areas across the length of the TSV and determine the modes of cracking prevalent along the TSVs using fracture mechanics.

3.4 Fracture Mechanics

Fracture mechanics presumes the presence of a crack. Stress state in the region of the crack may be one of plane strain or plain stress. Linear-elastic fracture-mechanics (LEFM) theory becomes applicable in this case since the zone of yielding around the crack is small compared to the dimensions of the part. This theory assumes that the bulk of material behaves according to Hook's law [44].

3.5 Modes of Crack Displacement

Depending on the orientation of the loading versus the crack, the applied loads may tend to pull the crack open in tension, shear crack in-plane, or shear (tear) it out-of-plane as shown in Fig. 3.1.

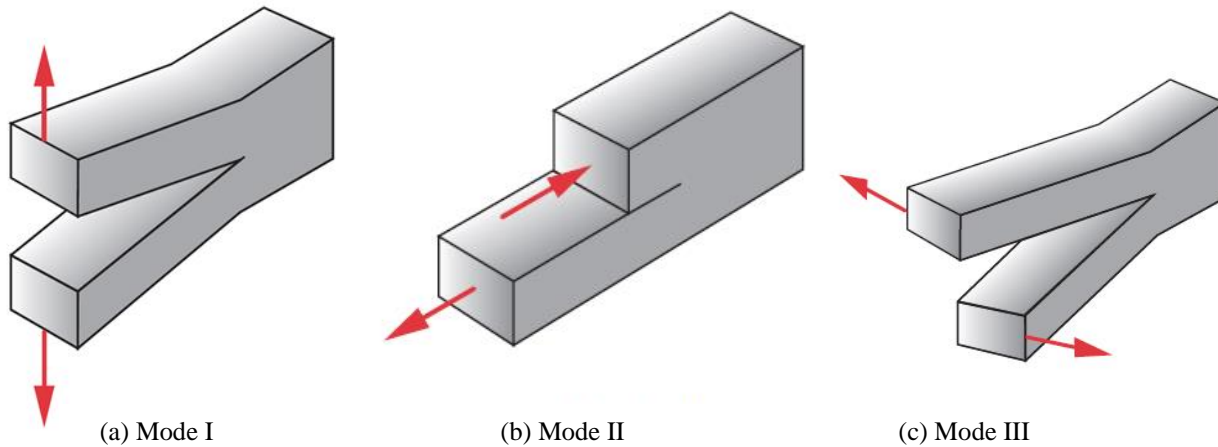


Fig. 3.1: Three Modes of Crack Displacement [44]

3.6 Stress intensity factor

The Fig. 3.2 shows a plate of width $2b$ under tension with a through crack of width $2a$ in the center. The crack is assumed to be sharp at its ends, and b is much larger than a . The crack's cross section is in the xy plane. Polar coordinate system $r-\theta$ is also set up in the xy plane with its origin at the crack tip as shown in Fig. 3.2 (b). From the theory of linear elasticity, for $b \gg a$, the stresses around the crack tip, expressed as a function of the polar coordinates and higher-order terms of small value omitted [44].

$$\sigma_x = \frac{K}{\sqrt{2\pi r}} \cos \frac{\theta}{2} \left[1 - \sin \frac{\theta}{2} \sin \frac{3\theta}{2} \right] + \dots$$

$$\sigma_y = \frac{K}{\sqrt{2\pi r}} \cos \frac{\theta}{2} \left[1 + \sin \frac{\theta}{2} \sin \frac{3\theta}{2} \right] + \dots$$

$$\tau_{xy} = \frac{K}{\sqrt{2\pi r}} \sin \frac{\theta}{2} \cos \frac{\theta}{2} \cos \frac{3\theta}{2} + \dots$$

$\sigma_z = 0$; for plane stress.

Or $\sigma_z = \nu(\sigma_x + \sigma_y)$; $\tau_{yz} = \tau_{zx} = 0$; for plane strain

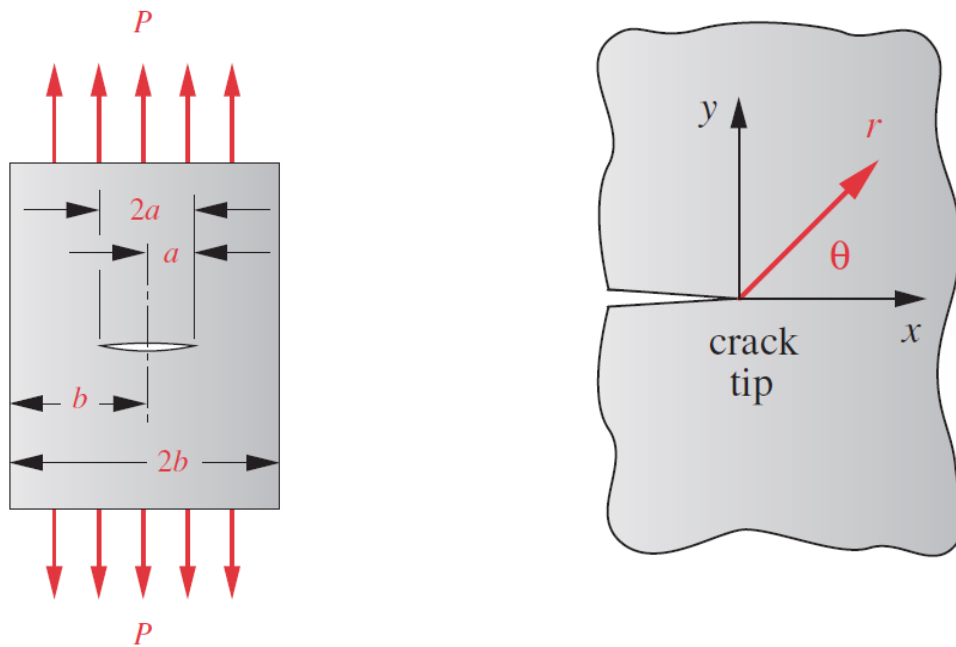


Fig. 3.2: A Through-Crack in a Plate in Tension [44].

3.7 J-Integral

Rice et al. proposed that the method of energy release rate can be extended to nonlinear materials, where the energy release rate is being expressed as a path-independent line integral

called J integral. It is one of the techniques to evaluate the strain energy release rate (work energy per unit fracture surface area) in a material [45].

$$W = W(x, y) = W(\boldsymbol{\varepsilon}) = \int_0^{\boldsymbol{\varepsilon}} \boldsymbol{\sigma}_{ij} d\boldsymbol{\varepsilon}_{ij}$$

Where, $\boldsymbol{\varepsilon} = [\boldsymbol{\varepsilon}_{ij}]$ infinitesimal strain tensor.

Thus, the integral J is defined by

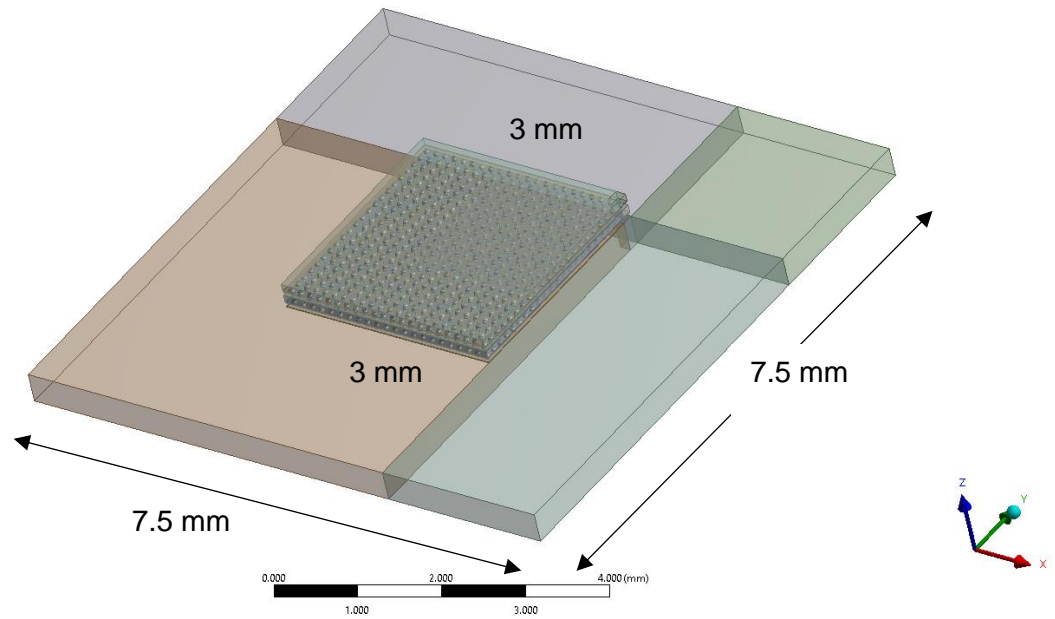
$$J = \int_{\Gamma} \left(W dy - T \cdot \frac{\partial u}{\partial x} ds \right)$$

where, Γ is a curve surrounding the notch tip, the integral being evaluated in a counterclockwise sense starting from the lower flat notch surface and continuing along the path Γ to the upper left surface. Here, T is the traction vector defined according to the outward normal along Γ , $T_i = \sigma_{ij}n_j$, ds is an element of arc length along Γ , and u is the displacement vector [45].

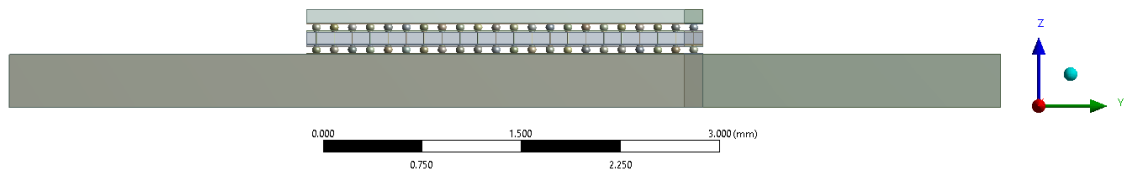
3.8 Description of the model

3.8.1 Array model

The array model shown in Fig. 3.1 is comprised of two die 3D flip chip package. Dies are connected by TSVs. Complete model of the package shown below. ANSYS DesignModeler is used for building the geometric model. One of the most challenging parts of the research will be building the geometric CAD model of the structure.

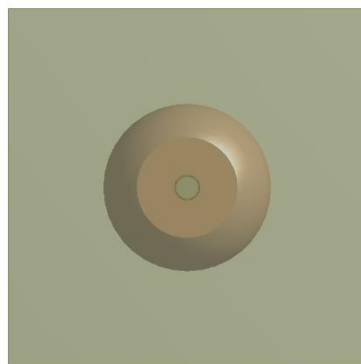


(a)



(b)

Fig. 3.3: 3D TSV Array Model (a) Isometric view (b) Front view



Cu core diameter 0.009 mm

SiO₂ thickness 0.0005 mm

Fig. 3.4: Top view on the unitcell

3.8.2 Compact model

A compact model of the array model is used to perform the analysis. Mirza et al. developed a novel approach of using compact model to simulate the fractures, as the size of the full array model is large with TSVs (~8000 TSVs and μ -bumps) and micro bumps [46] [47]. Using the compact model reasonable computational time can be maintained. The simulation is performed in three steps. At first the global model on the compact scale is formulated and solved. Then the results from the solution are used to generate boundary conditions for the sub model 1. The sub model 1 is part of the critical region having detailed features. These boundary conditions are then applied on the sub model 2 which is part of the sub model 1. The boundary conditions are shown in Fig. 3.6.

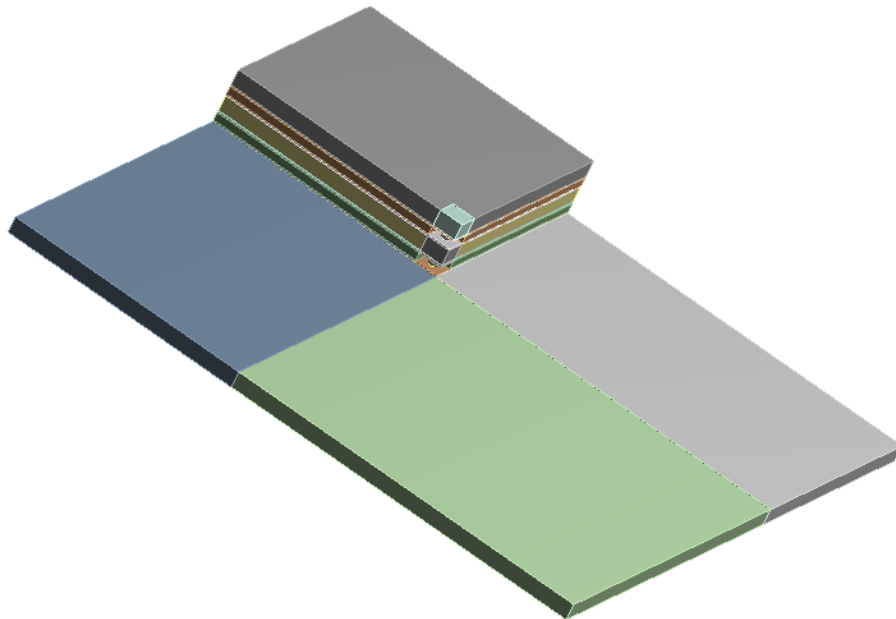


Fig. 3.5: Compact Model

A: Case1-0.01 mm
Fixed Support
Time: 350. s
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- A Frictionless Support
- B Frictionless Support 2
- C Fixed Support

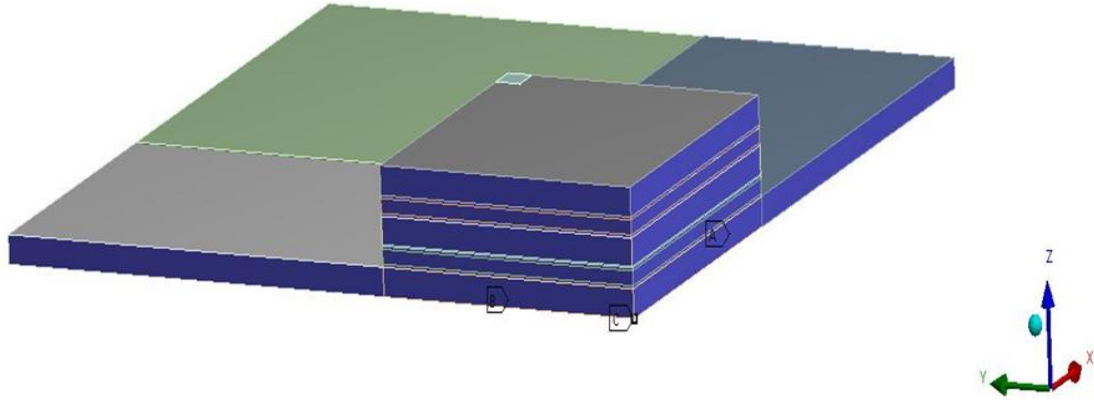


Fig. 3.6: Boundary Conditions

Symmetry Region 2
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- A Symmetry Region
- B Symmetry Region 2

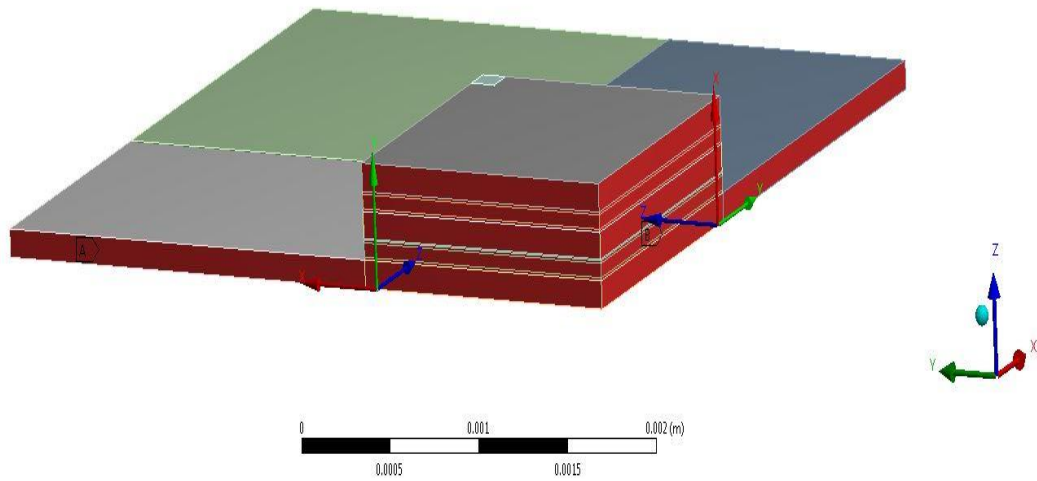


Fig. 3.7: Symmetry Regions

3.8.3 Model Description and Analysis Process

Design Modeler is used to build the full array model and the quarter symmetry of the array model and compact model. ANSYS 2019 is used to develop the fractures on Cu surface and dielectric layer. Quarter symmetry TSV package is used to simulate under reflow condition for analyzing various stresses developed within the TSV. Sub-modeling technique is used to analyze the fracture parameter of copper core and the dielectric layer of the TSV. The cracks are modeled at a different position on TSV. The behavior of stress intensity factor and J-integral is studied varying the thickness of the top die. In this study, nine cracks were modeled along the TSV at same direction. Anand's viscoplastic material property considering plastic deformations has been modeled. To describe the inelastic behavior of lead-free solder, Anand's viscoplastic constitutive law is used. Anand's viscoplastic model has total nine material constants A , Q , ξ , m , n , h , a , s , \hat{s} that are used throughout the solder strain-rate and temperature sensitivity [16] [14] [48]. The Anand constants for the effective block in provided in Table 3.3.

Table 3.1: Materials Properties used for Si, SiO₂ and Cu [14]

Material	Young's Modulus (GPa)	Poisson's Ration	Coefficient of Thermal Expansion (CTE) (ppm/°C)
Silicon	169	0.26	2.3
SiO ₂	75	0.17	0.5
Copper	117	0.3	16.7

Table 3.2: Anand Constant for SAC 305 [14]

No.	Anand's Constant	Value	Units
1	s_0	1.3	MPa
2	Q/R	9000	1/K
3	A	500	sec ⁻¹
4	ξ	7.1	Dimensionless
5	m	0.3	Dimensionless
6	H_0	5900	MPa
7	\hat{s}	39.5	MPa
8	n	0.03	Dimensionless
9	a	1.5	Dimensionless

Table 3.3: Anand's Constant for effective block in the compact model [46]

No.	Anand's Constant	Value	Units
1	s_0	0.15	MPa
2	Q/R	9000	1/K
3	A	500	sec ⁻¹
4	ξ	7.1	Dimensionless
5	m	0.3	Dimensionless
6	H_0	5900	MPa
7	\hat{s}	3	MPa
8	n	0.03	Dimensionless
9	a	1.5	Dimensionless

3.8.4 Reflow condition

Reflow is a process refer to the temperature above which a solid mass of solder alloy is certain to melt. It is a common method of attaching microelectronic components to the printed circuit board (PCB) after that the whole assembly is subjected to controlled heat. Solder paste is used to attach the electronic components. In this study, crack is modeled along the TSV and reflow thermal load is applied to the 3D package for assembly. In reflow condition, the thermal load applied is 200°C, at 300 second the reflow temperature is brought down to room temperature at 25°C and then it remains at room temperature till 350 second. Fig. 3.8 shows the reflow profile.

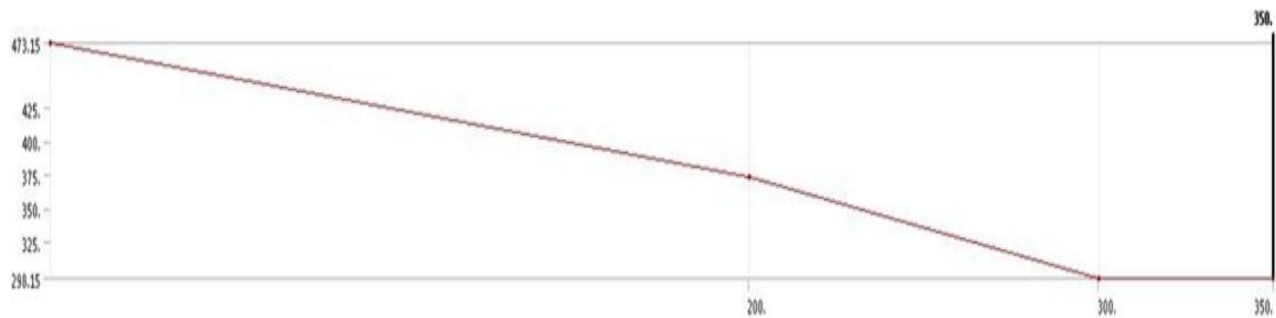


Fig. 3.8: Reflow profile

3.8.5 Meshing and Crack Modeling

Here crack propagation is inserted at different positions along the cylindrical dielectric layer and Cu core of TSV. This is the vulnerable region where more chances of crack to grow due to the developed thermal stress because of CTE mismatch between Cu and SiO₂. Modeling of horizontal and vertical crack for the TSV package is done by using ANSYS 2019. For semi-elliptical cracks tetrahedron mesh profile is used on the exterior surface of TSV. The cracks have been modeled in the sub model 2 which is one of the symmetrical parts of sub model 1. Then sub model 2 was again subjected to the same reflow condition with importing cut boundary constraints from the sub model 1. Equal space have been taken for simulating the cracks along the length of

TSV. The plot for the relation between stress intensity factor (SIF) and crack location have been shown in this study. Also, J-integral is shown in the results for crack locations. To avoid radial crack, K should be less than K_c , i.e. $K < K_c$ where K_c is fracture toughness of silicon [35].

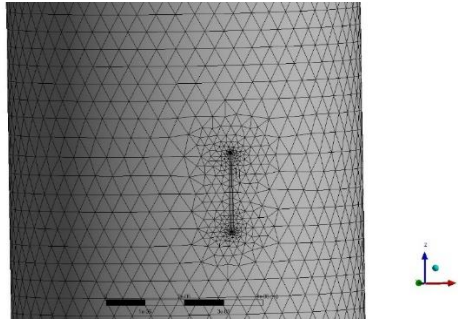


Fig. 3.9: Vertical Crack on Cu surface

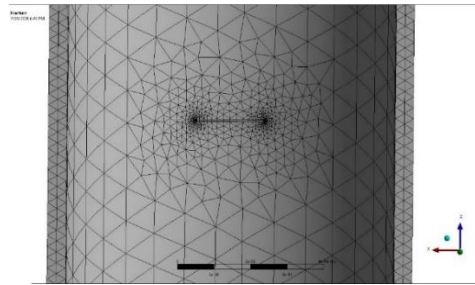


Fig. 3.10: Horizontal Crack on SiO₂

3.8.5.1 Mesh Sensitivity Analysis

Mesh sensitivity analysis has been performed in TSV sub model. The model with 20152 mesh elements has been chosen. Table 3.4 shows the mesh sensitivity analysis performed on the TSV sub model.

Table 3.4: Mesh Sensitivity Analysis

No. of Elements	No of Nodes	Equivalent Stress (Pa)
20152	42976	4.7265E+08
22119	48144	4.7300E+08
89557	190674	4.7300E+08

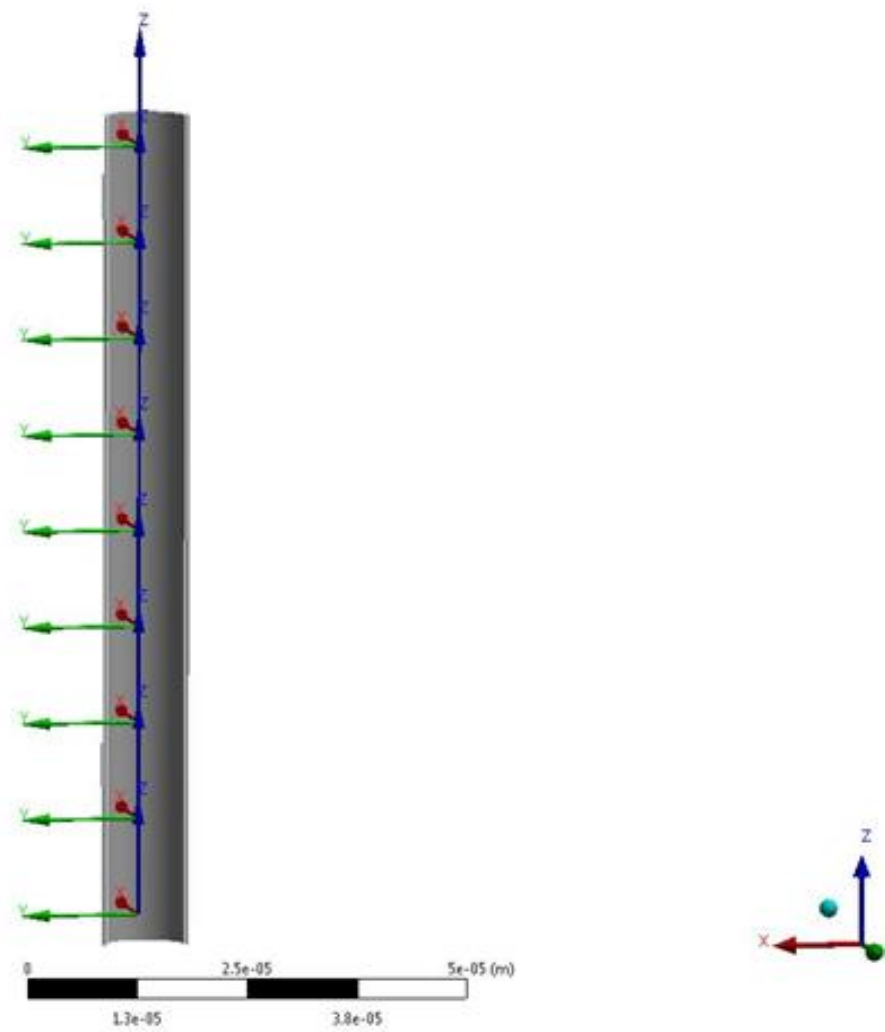


Fig. 3.11: Generation of coordinates for cracks

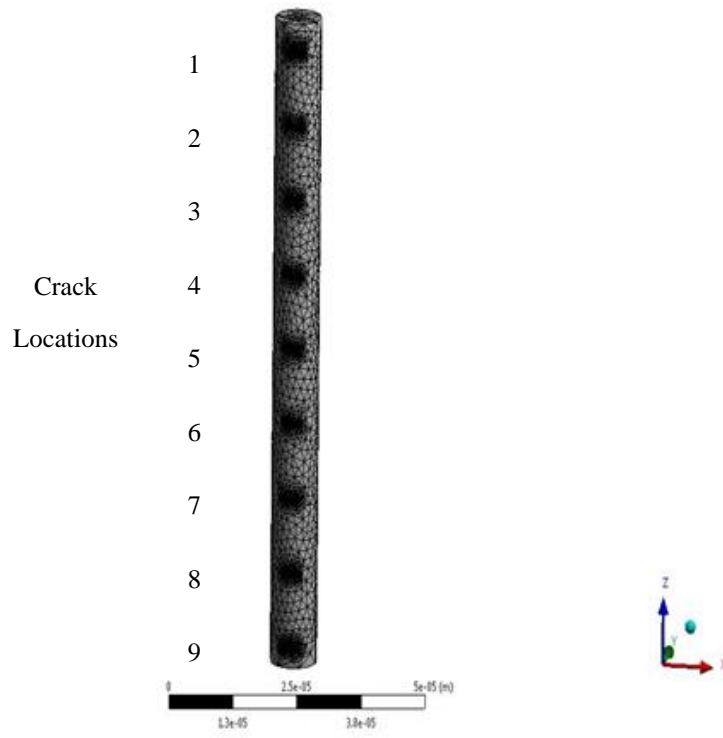


Fig. 3.12: Crack locations of Cu surface

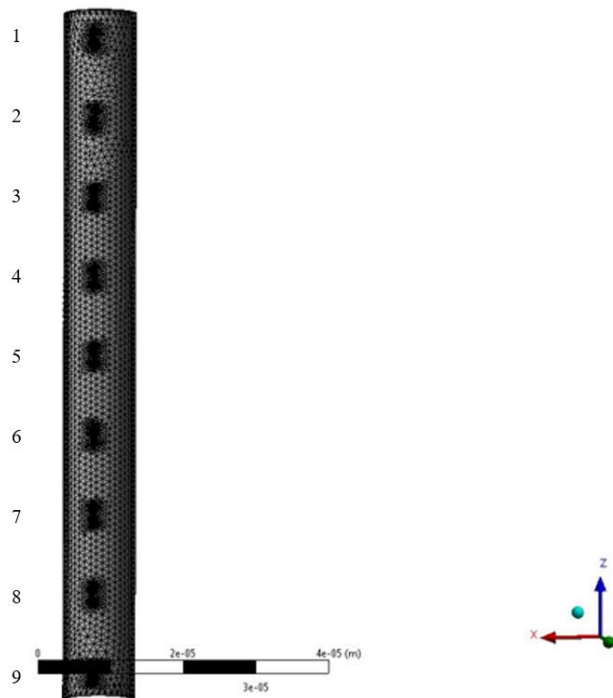


Fig. 3.13: Crack locations on dielectric layers

3.9 Results and Discussion

The goal of this study is the study the effect of die thickness on the reliability of the through-silicon vias (TSVs). The top die thickness is varied from 0.1 mm to 0.3 mm, and horizontal and vertical cracks are modeled in nine locations on the SiO₂ surface and Cu surface of TSV. Stress Intensity Factor and J-Integral are determined on the SiO₂ and Copper surfaces.

The results show that the maximum equivalent stress of the global compact model with the changes of top die thickness. Equivalent stresses (Von-Mises) obtained after simulating under reflow condition.

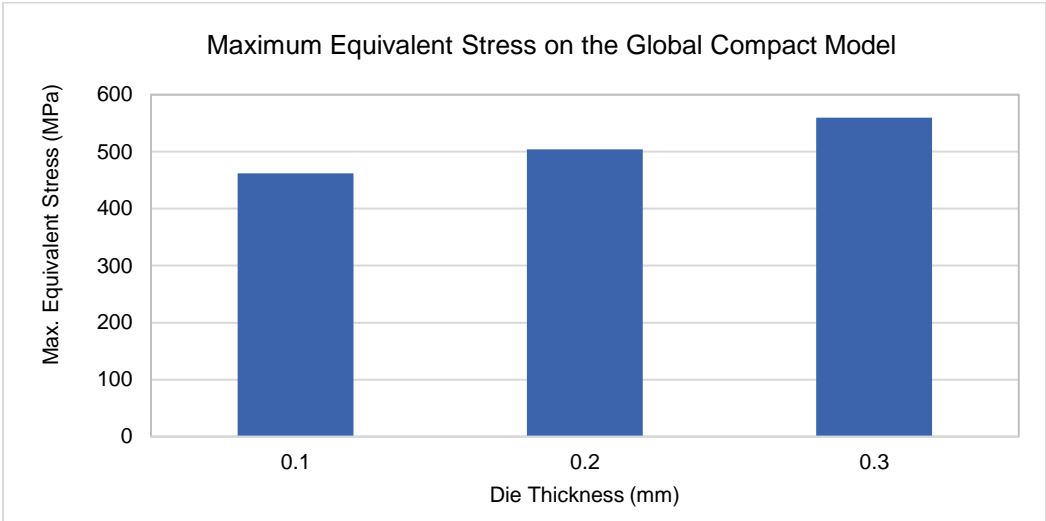


Fig. 3.14: Max. Equivalent Stress on the Global Model

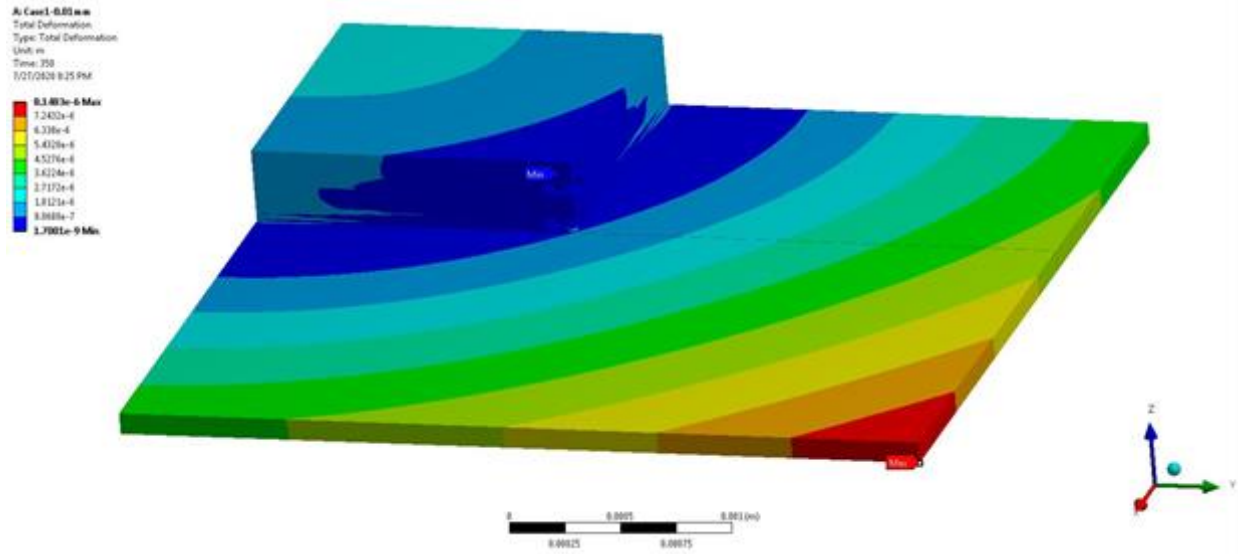


Fig. 3.15: Equivalent Stress on the quarter symmetry of the compact model

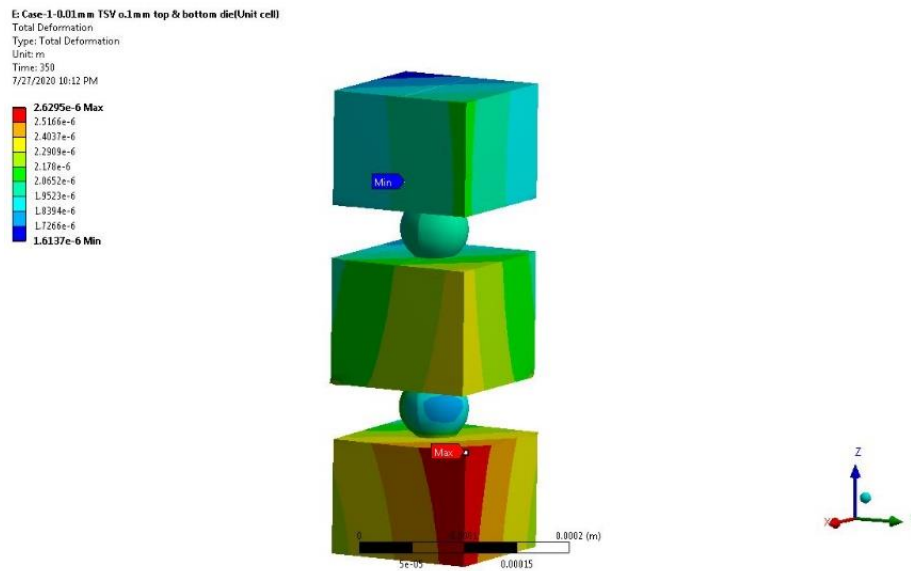


Fig. 3.16: Equivalent stress on Sub model 1

E: Case-1-0.01 mm TSV o.1mm top & bottom die(Unit cell)
 Equivalent Stress 2
 Type: Equivalent (von-Mises) Stress
 Unit: Pa
 Time: 350
 7/27/2020 10:14 PM

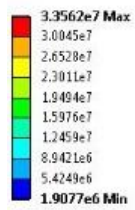


Fig. 3.17: Equivalent stress on Sub model 2

3.9.1 Stress Intensity Factor (SIF) on SiO₂ Layers and Cu Surface

3.9.1.1 SIF on SiO₂ Layers

Stress intensity factor (SIF) at different crack locations are determined for the horizontal crack. From Fig. 3.10 it seems that for the horizontal crack, SIF is stable at the middle part of the TSV for all different die thicknesses. At the bottom SIF is higher for die thickness 0.1 mm and at the top side SIF is higher for die thickness 0.3 mm. From Fig. 3.11 similar SIF pattern is found at the middle section is for the vertical cracks. For die thickness 0.3 mm, SIF is higher than two die thickness combinations.

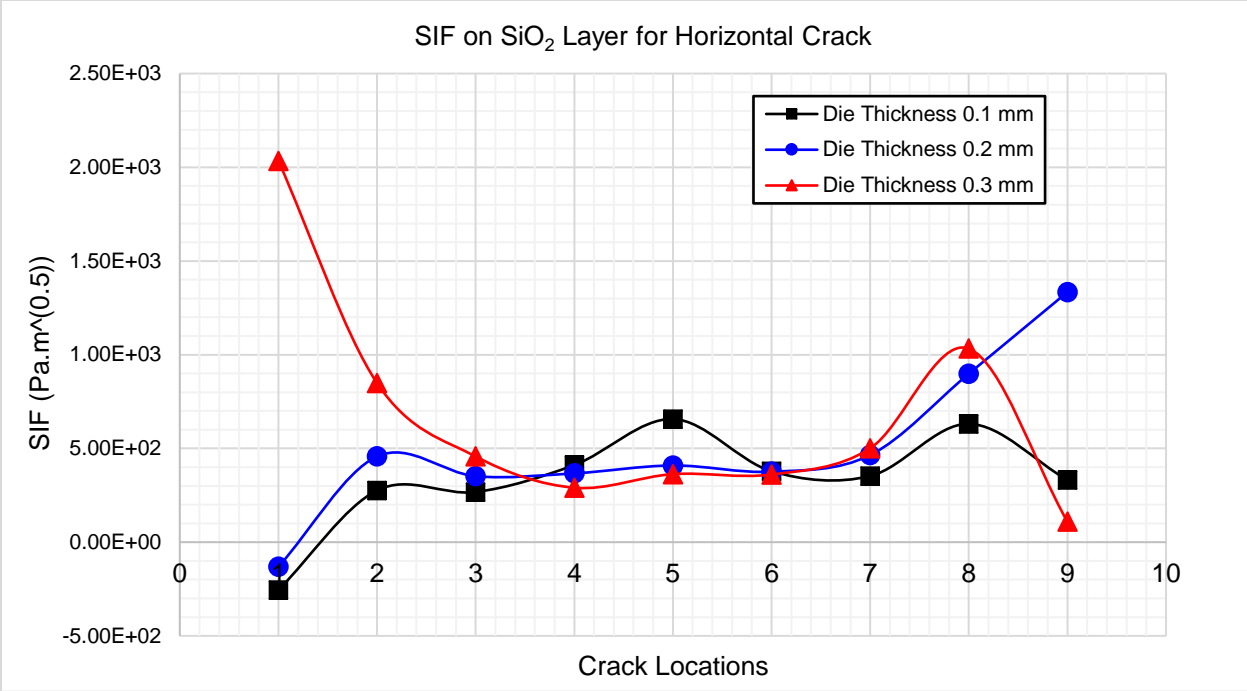


Fig. 3.18: SIF on SiO₂ Layer for Horizontal Crack

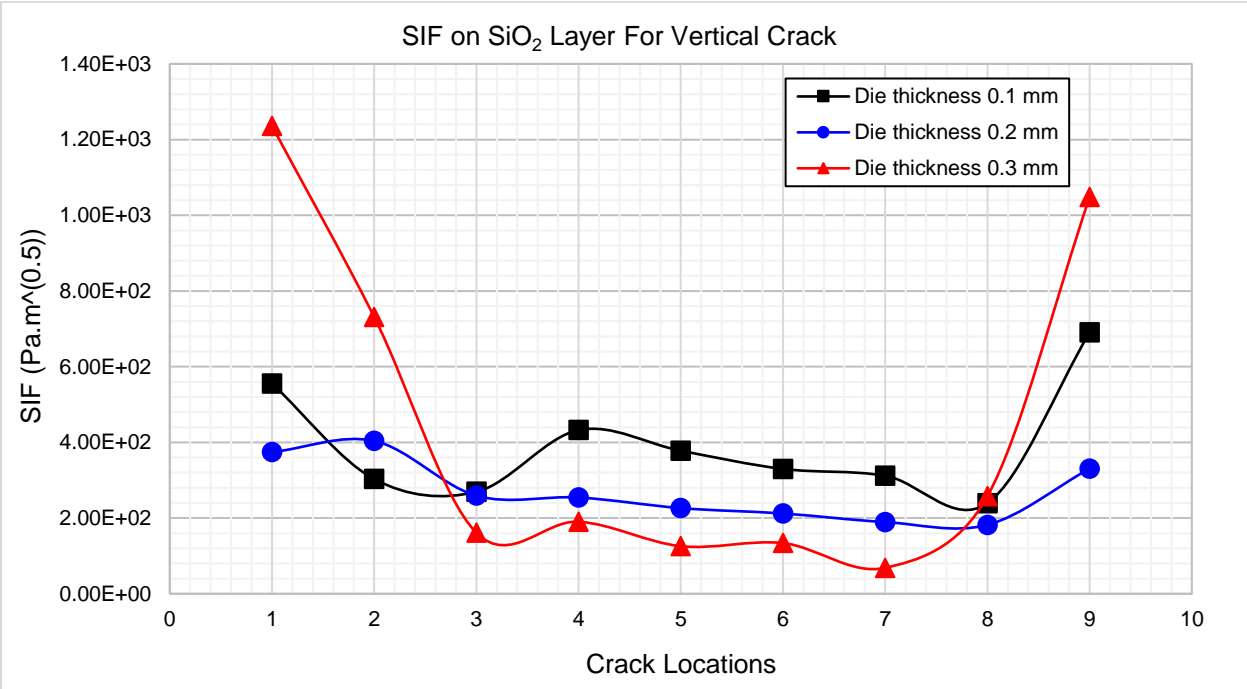


Fig. 3.19: SIF on SiO₂ Layer for Vertical Crack

3.9.1.2 SIF on Cu Surface

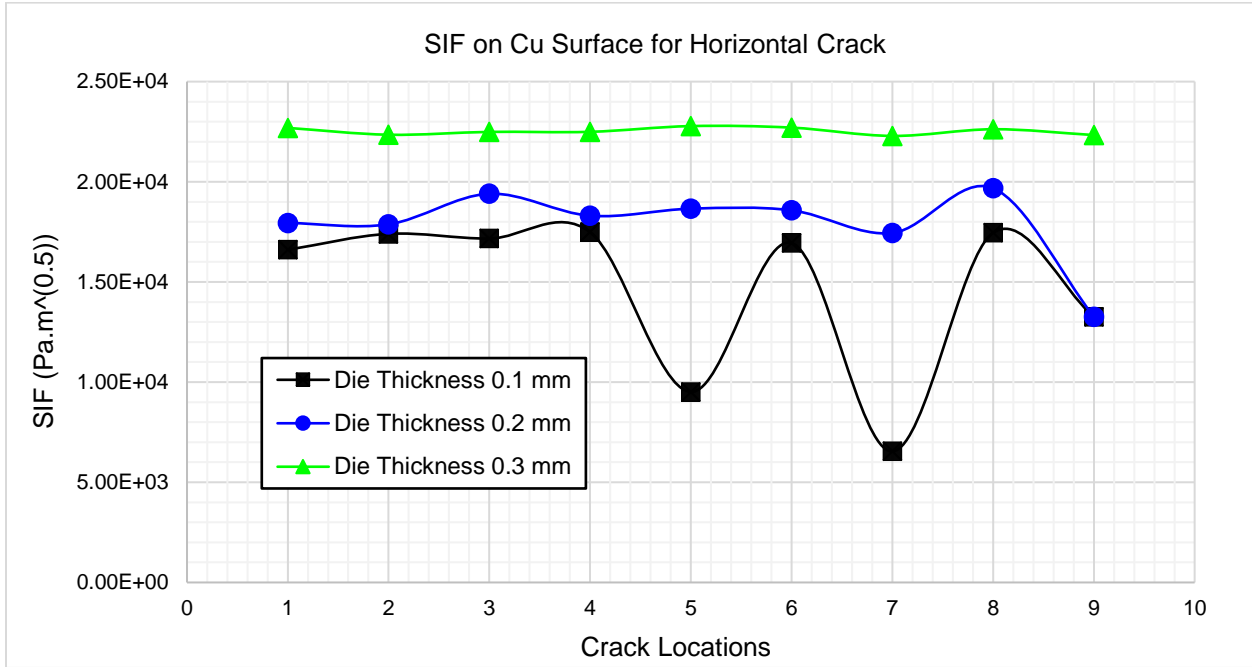


Fig. 3.20: SIF on Cu Surface for Horizontal Crack

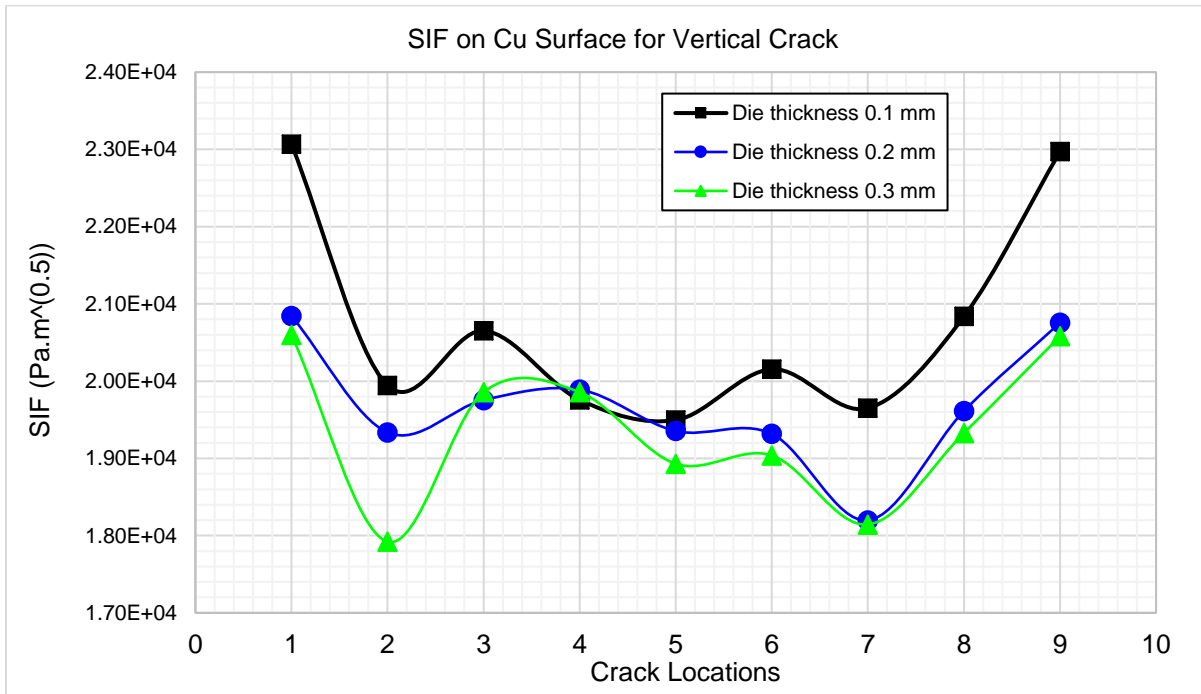


Fig. 3.21: SIF on Cu Surface for Vertical Crack

3.9.2 J-Integral on SiO₂ and Cu Surface

Changing the top die thickness from 0.1 mm to 0.3mm the value of J-integral is shown in the plots above for different crack positions. From the observation of these plots above, J-integral have a relationship with the of die thickness. When the thickness of die is increasing from 0.1 mm to 0.3 mm the value of J-integral is decreasing in all the cases for both SiO₂ layer and for Cu surface, which signifies constancy in crack driving force. J-integral is the crack driving energy and it is taking care of all the SIF. When the die thickness is increased, the developed J-integral is decreasing. When the developed J-integral reaches at a critical value, crack will propagate.

3.9.2.1 J-Integral on SiO₂

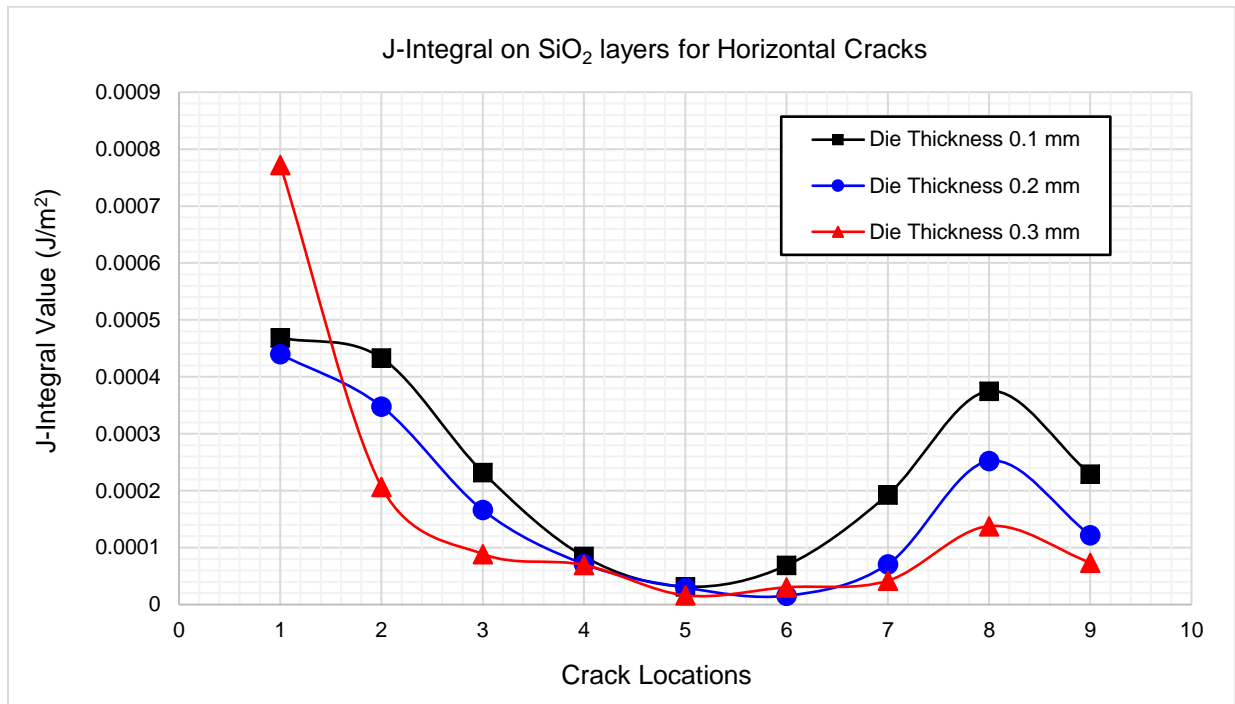


Fig. 3.22: J-Integral on SiO₂ layers for Horizontal Cracks

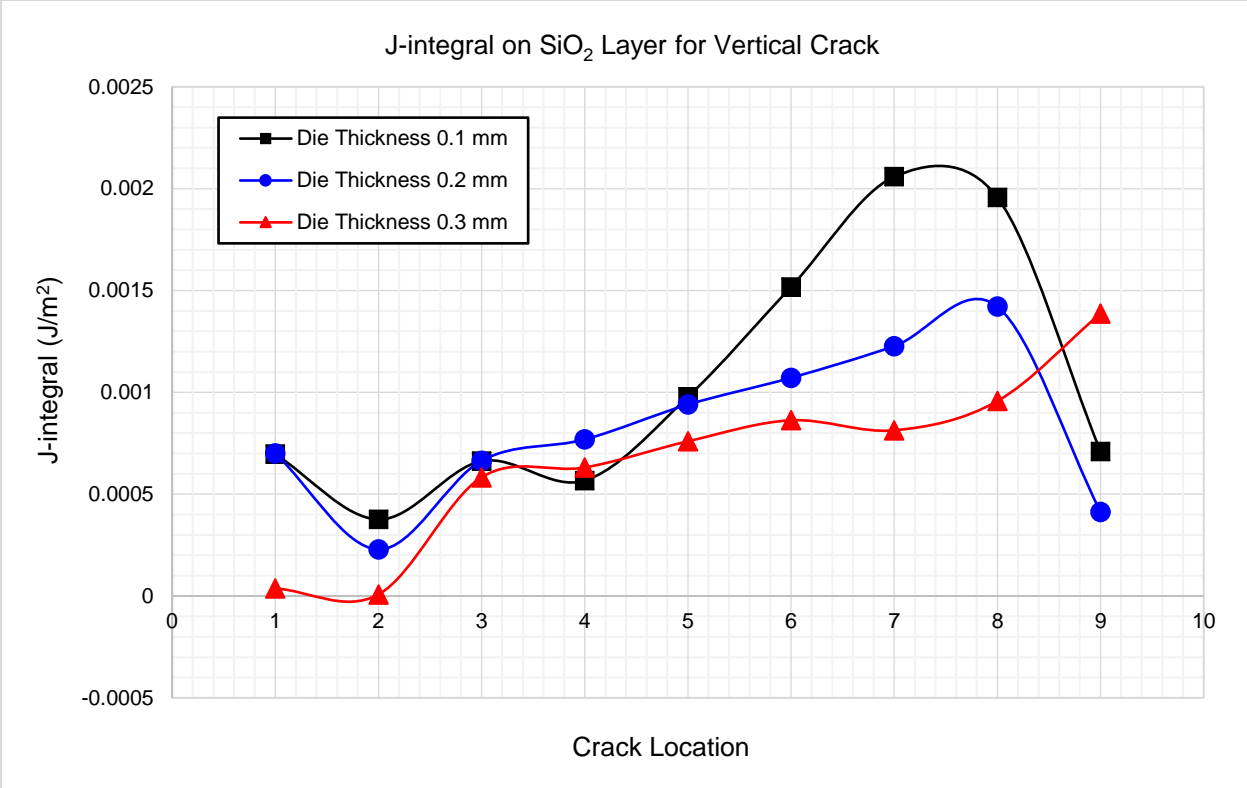


Fig. 3.23: J-integral value on SiO₂ Layer for vertical crack

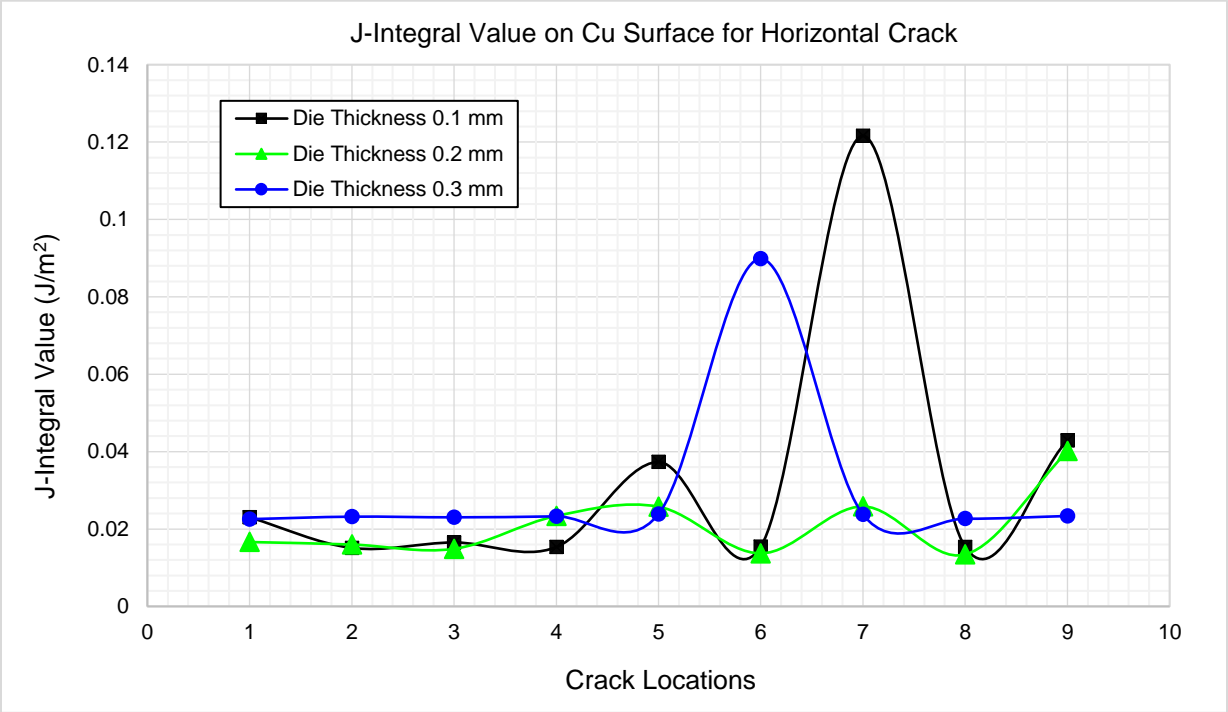


Fig. 3.24: J-Integral Value on Cu Surface for horizontal crack

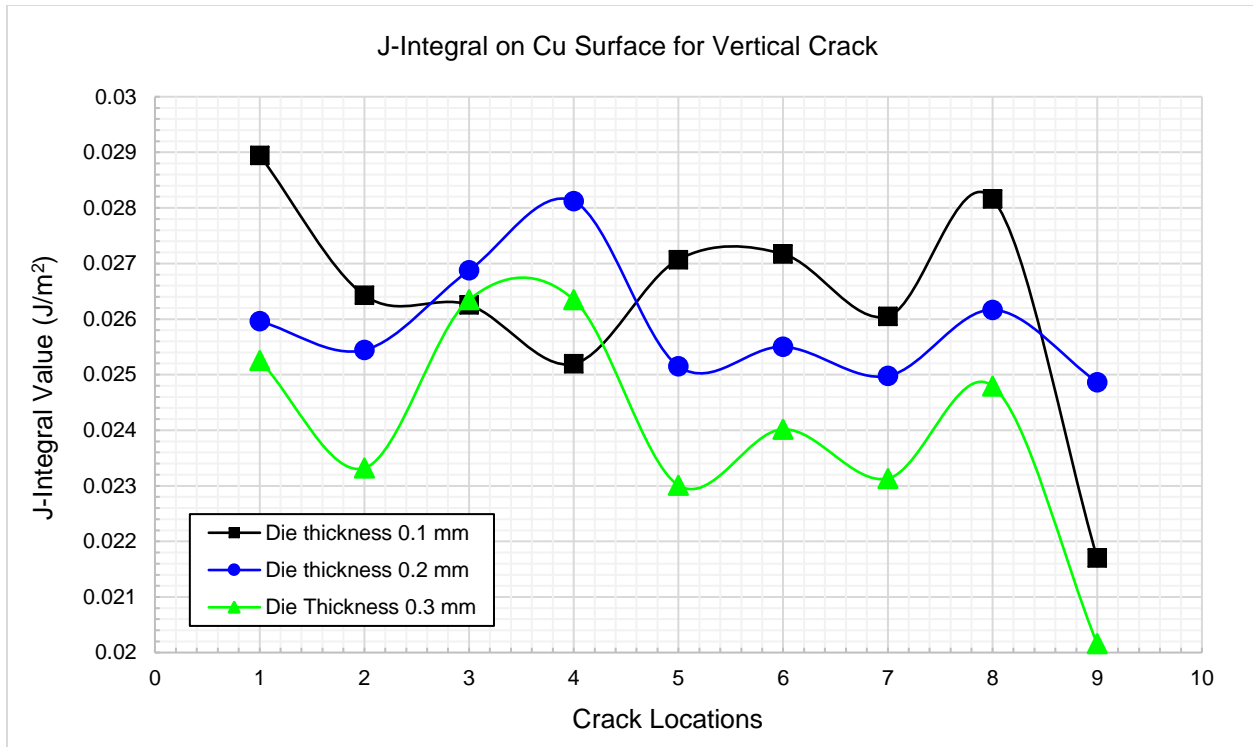


Fig. 3.25: J-Integral on Cu Surface for Vertical Crack

The Stress intensity factor and J-Integral at the crack locations as shown above. From the SIF and J-Integral results it can be predicted that the top and bottom part of TSV is more susceptible to fracture than the middle region of TSV. From the pattern of the results it can be predicted that the middle area of TSV is susceptible to Mode 1 fracture as the value of SIF is lower and stable in the middle region of the TSV [35]. From the results it can also be predicted that the top and bottom portions of the TSVs are more susceptible to Mode 2, Mode 3 fracture since the value of SIF is higher in those regions. For designing reliable heterogeneous 3D IC these factors need to be taken into consideration.

Chapter 4

Characterization of Thermal Interface Materials

Thermal Interface Material (TIM) plays an important role in the performance of an electronic device. Conduction heat transfer is involved in the use of a heat sink to dissipate heat from an electronic package, the heating of a hot plate, the operation of heat exchanger and so on. Attaining effective heat transfer by conduction requires materials of high thermal conductivity. It also requires a good thermal contact between the two surfaces across which heat transfer occurs [8]. TIMs are chosen mostly based on utilizing the advantage of one or more of the three parameters, namely, higher bulk thermal conductivity, lower bond line thickness (BLT) and lower contact resistance. There are other important parameters such as pressure dependence, cost, re-workability, operational life, shelf life, susceptibility to non-uniformity in dynamic pressure loading, and ease of use have also plays a major role in the selection and development of TIMs [10]. TIM is used to minimize the thermal contact resistance between the central processor unit (CPU) and the heat sink [49]. As the power density of microelectronic devices continues to escalate and it is expected to exceed 100 W/cm^2 [50][51][52] thermal management is becoming more and more challenging. One of the major thermal management issues in electronics cooling involves reducing the thermal resistance between the microprocessor chip and its accompanying heat sink by use of thermal interface material (TIM). TIM is used to transfer the heat effectively from the silicon die to the sink while incurring as small a temperature drop as is possible [50]. It is widely used to minimize the contact thermal resistance between heat generating electronic components and a variety of cooling systems such as heat sinks and heat pipes [53]. The Fig. 4.1 presents a TIM and temperature distribution. The joints are comprised of three individual thermal resistance in series.

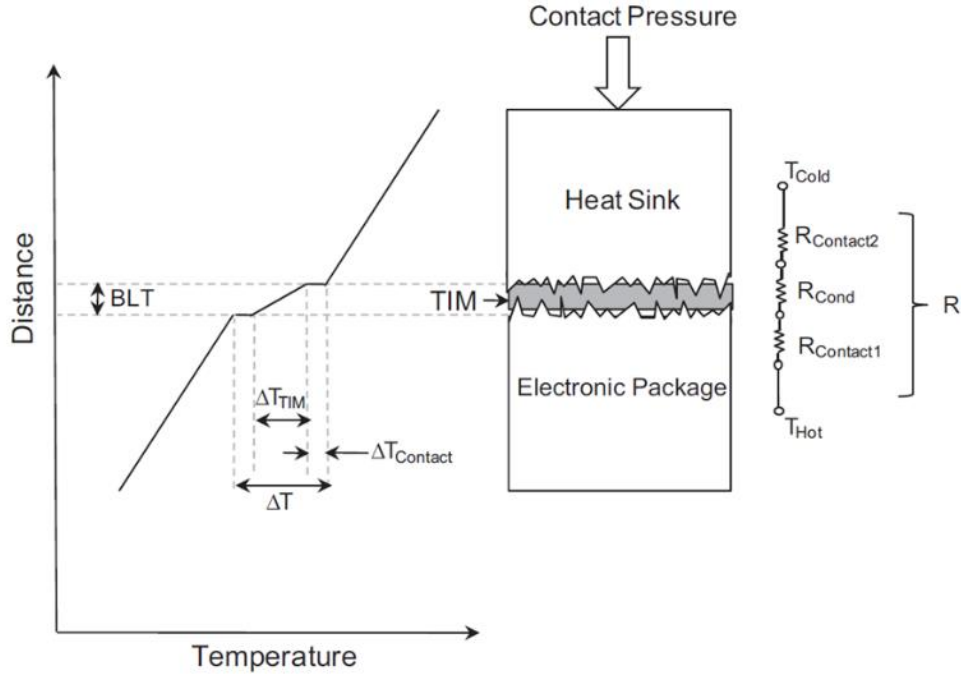


Fig. 4.1: Schematic representing a real TIM and associated temperature distribution [9].

The effective thermal resistance is given by,

$$R = R_{\text{Contact1}} + R_{\text{Cond}} + R_{\text{Contact2}}$$

where,

R_{Contact1} = the contact resistance between TIM and the lower surface

$R_{\text{Cond}} = \text{BLT}/k_{\text{TIM}}$ is the bulk resistance of the TIM layer

R_{Contact2} = the contact resistance between TIM and the upper surface

Characterization of the properties of thermal interface materials has gained importance since it plays a critical role in the thermal dissipation and the life cycle of the of the electronic packages. Heat dissipation of the semiconductor packages has become one of the limiting factors in miniaturization. The thermal budget consists of three parts the heat transfer to the outside world to be improved by better heat sinks, higher air velocities and liquid cooling, the thermal resistance of the package itself, and the interface resistance that is defined as the sum of the thermal resistance of the interface material plus both contact resistances [54]. The transfer of heat by conduction is

involved in the use of a heat sink to dissipate heat from an electronic package. Materials of high thermal conductivity requires for effective transfer of heat by conduction. It also requires a good thermal contact between the two surfaces (for example, the surface of a heat sink and the surface of a printed circuit board) across which heat transfer occurs. The use of expensive thermally conducting materials for the components is a waste without good thermal contact. The attainment of a good thermal contact requires thermal interface material (TIM) [55]. Different characterization techniques can be used to characterize the properties of materials [56]. The characterization techniques used in this study are discussed in the following sections.

In the context of electronics applications, TIMs can be arbitrarily categorized as polymer-based TIMs, solders, metallic foils, sintered metallic TIMs and carbon nano-tubes [53][49]. Moisture is very important factor, affecting the modulus, strength, and damping properties of polymers [57]. It can have a major impact on the dielectric properties of the thermal interface materials.

4.1 Properties for Thermal Interface Materials

The properties of thermal interface materials are very important for optimum performance of electronic devices. Some of the properties are discussed in the following section.

4.1.1 Complex Modulus

A material is sinusoidally deformed, and the resulting stress is recorded to characterize the viscoelastic behavior of the material. In the case of an ideal elastic material, the stress and strain are in phase, and the phase shift $\delta = 0$ and in the case of an ideal viscous material, the stress and strain are 90° out of phase [58]. Dynamic (commonly sinusoidal) perturbations are used to study the viscoelastic behavior of a material. The material is subjected to an oscillatory strain with frequency ω . From the Fig., we can write the following expressions for strain and stress:

$$\epsilon = \epsilon_0 \sin \omega t$$

$$\sigma = \sigma_0 \sin(\omega t + \delta)$$

in the above equation for stress, δ is the phase angle or phase lag between the stress and strain.

From these expressions, the tensile storage modulus E' and the tensile loss modulus (E''), and complex modulus are the following,

$$E' = \left(\frac{\sigma_0}{\epsilon_0}\right) \cos \delta$$

$$E'' = \left(\frac{\sigma_0}{\epsilon_0}\right) \sin \delta$$

Now using complex variables [58],

$$\epsilon = \epsilon_0 \exp i (\omega t)$$

$$\sigma = \sigma_0 \exp i (\omega t + \delta)$$

$$E = E' + E''$$

In normal operating condition the temperature of the electronic device increases and decrease depending the operating condition. The change of temperature has impact on the thermal interface materials (TIMs). Effect of thermal aging on the TIMs will be discussed in this study.

4.1.2 Coefficient of thermal expansion

Dimension of a body changes with the change in temperature. In general, if the temperature increases, the body will expand, whereas if the temperature decreases, it will contract. For homogeneous and isotropic material, the algebraic change in the length of the member [59]

$$\delta_T = \alpha \Delta T L$$

Here,

α = a property of the material, referred to as the linear coefficient of thermal expansion

ΔT = the algebraic change in temperature of the member

L = the original length of the member

δ_T = the algebraic change in the length of the member

For electronic devices coefficient of thermal expansion (CTE) is very important. CTE mismatch, the difference in elastic modulus in different materials can affect the device performance and may result in failure of the device.

4.1.3 Dielectric Properties

Dielectric properties are very important properties of thermal interface material. Low dielectric materials possess myriad of electrical, thermal chemical, and mechanical properties that are just as crucial as the name that classifies them. The applications of low dielectric constant materials are dictated by these other properties, and the choice of low dielectric material may have a tremendous effect on a device's performance. The Dielectric constant is ratio of the permittivity of a substance to that of free space. Material containing polar components, for instance, polar chemical bonds which are presented as electric dipoles has higher dielectric constant, in which the electrical dipoles align under as external electric field. This align of dipoles adds to the electric field. As a result, a capacitor with a dielectric medium of higher k will hold more electric charge at the same applied voltage or, in other words, its capacitance will be higher. The dipole formation is a result of electronic polarization, distortion polarization, or orientation polarization in an alternating electric field. These phenomena have characteristic dependencies on the frequency of the alternating electric field, giving rise to a change in the real and imaginary part of the dielectric constant between the microwave, ultraviolet, and optical frequency range [60].

Dielectric materials must meet material property requirements for successful integration into the interconnect structures. These requirements are based on electrical properties, thermal stability, thermomechanical and thermal stress properties, and chemical stability [60].

The important electrical properties can be outlined as

- Low dielectric constant,
- Low dielectric loss and leakage current, and
- High breakdown voltage.

4.2 Type for Thermal Interface Materials

There different type of thermal interface materials is available in the industry. Following are some of the different types of thermal interface materials:

1. Thermal grease
2. Thermal Gel
3. Phase change material (PCM)
4. Liquid metal alloy (LMA)
5. Soft Metal Alloy (SMA)
6. Solder
7. Thermal Gap filler
8. Thermal Gap filler pad

Some of the different types of thermal interface materials are discussed in the following section.

4.2.1.1 Thermal Grease

Thermal greases are generally used to attach heat sinks to CPUs in personal computers. These are designed to flow into the surface imperfections, minimizing the interface resistance. It is prepared by emulsions of ceramic or metal particles in an organic or silicon fluid. The emulsion particles increase the thermal capacity and provide body to minimize flow out of the interface. The contact layer of thermal greases must be very thin since the bulk thermal conductivities of the

greases are very low (1-4 W/m°C) [61]. With high temperatures or extensive thermal cycling, the thermal greases have suffered from drying out or voiding from pumping out of the interface.

4.2.1.2 Gels

Gels are cured to form cross-linked polymer chains which provides lateral stability to minimize the problem associated with liquid TIM materials. These are reusable, they generally have a slightly lower thermal conductivity than thermal grease [61].

4.2.1.3 Thermal Gap Filler

Thermal gap fillers are used to fill air gaps between different components such as metal enclosures and chasses, PC boards and heat sinks. It is better for application where large gap tolerances are present due to steps, rough surfaces, and high stack-up. These gap filler materials allow the designer to be less concerned with components proximity to heat sinks or heat spreaders [62].

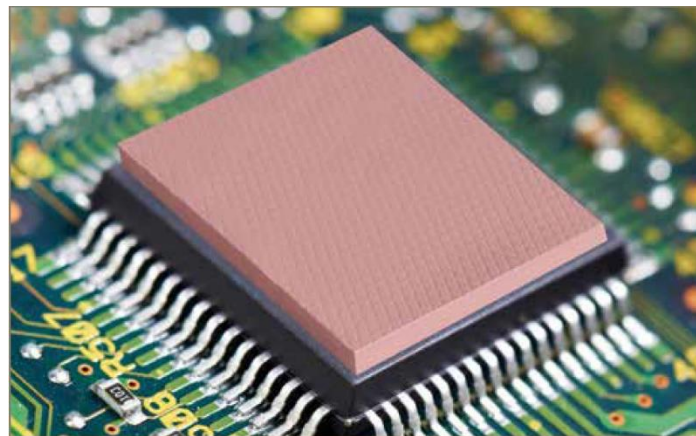


Fig. 4.2: Thermally Conductive Gap Filler Pads [63]



Fig. 4.3: Thermally Conductive Attachment Tapes [63]

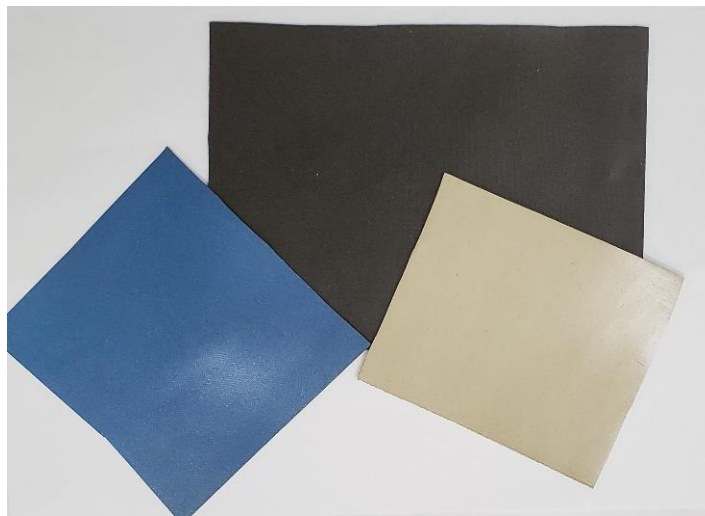


Fig. 4.4: Thermally Conductive Gap Filler Pads

4.3 Experimental Techniques

The experimental techniques and equipment used for this study will be described in this chapter. The systems used for measuring the thermal, mechanical, and dielectric properties will be explained in the following sections.

4.3.1 Dynamic Mechanical Analysis

Dynamic Mechanical Analysis method is used to measure the mechanical properties of the sample by measuring the stress or strain that is generated for the stress or strain applied in varying

degrees (vibration) over time to the sample. If dynamic mechanical analysis is thought of as a method of thermal analysis, it can be interpreted as a measurement technique of the relationship between temperature and the mechanical properties of a sample related to vibration load (or strain) [64]. The schematic of the dynamics mechanical analyzer is shown in Fig. 4.5.

By using different attachments, loss modulus (E''), storage modulus (E'), and loss tangent ($\text{Tan}\delta$) can be measured. The relationship between these properties and complex modulus (E^*), whose magnitude is comparable to Young's modulus, is given by Eqs. (1) and (2). Relation of modulus values to loss tangent is given by Eq. (3) [28].

$$E^* = E' + iE'' \quad (1)$$

$$|E^*| = \sqrt{E'^2 + E''^2} \quad (2)$$

$$\text{Tan}\delta = \frac{E''}{E'} \quad (3)$$

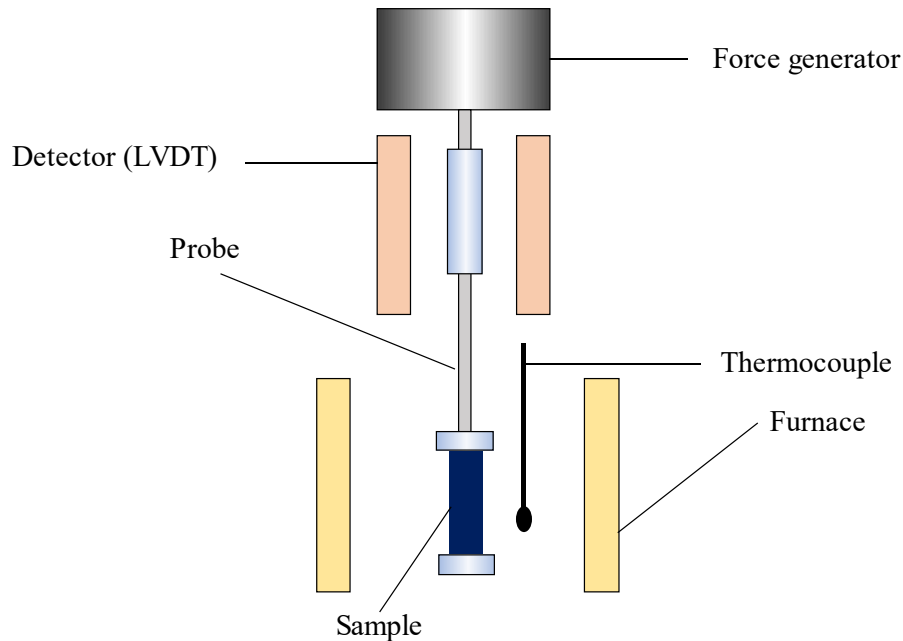


Fig. 4.5: Schematic of Dynamic Mechanical Analyzer (Tension mode) [65]

4.3.2 Thermomechanical Analyzer

Thermomechanical Analyzer is used to measure the coefficient of thermal expansion (CTE) and glass transition temperature of the thermal interface material.

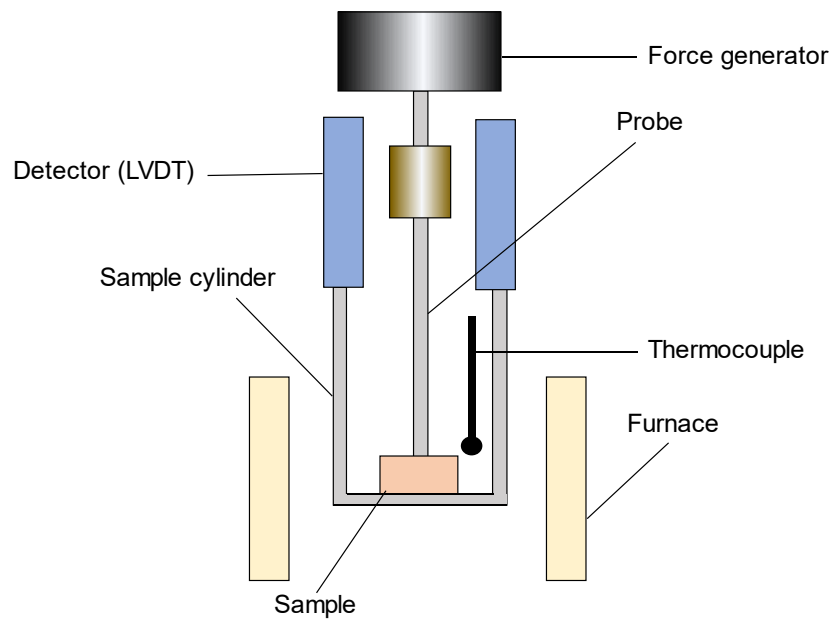


Fig. 4.6: Schematic of Thermomechanical Analyzer (TMA) [65]

4.3.2.1 Advance Features of TMA

Air Cooling Feature

The air-cooling feature reduces the temperature of the furnace to the desired level using compressed air when measurement is completed.

Protect Feature

This feature prevents damage to the furnace caused by temperature limit input errors or system malfunctions. Damage to the furnace is caused by runaway temperatures due to instrument

malfunctions or sample fusion from incorrect maximum temperatures being entered in the temperature program [65].

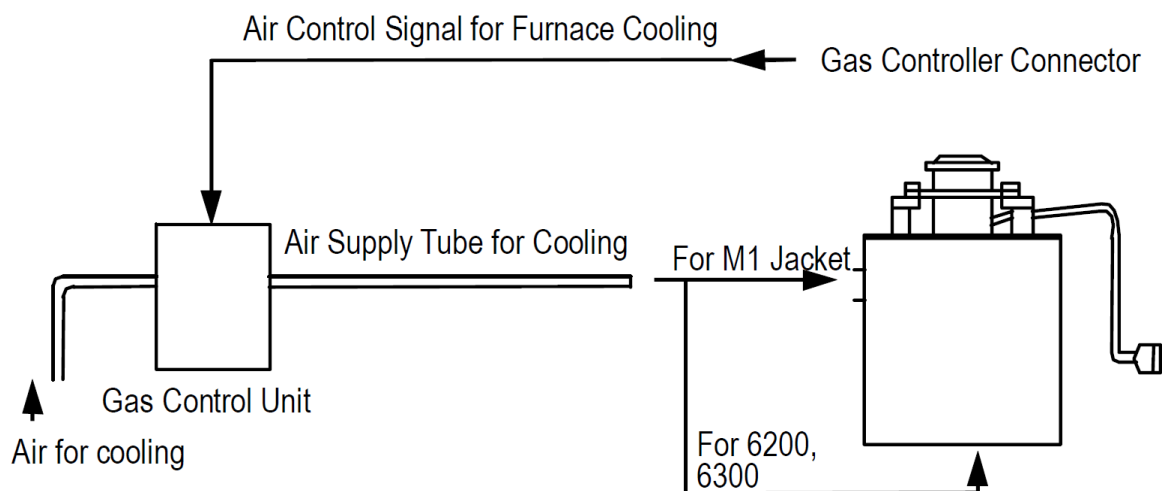


Fig. 4.7: Schematic of TMA air cooling feature [65]

Temperature Pre-calibration Feature

The temperature pre-calibration feature keeps the difference between the program temperature and sample temperature at a minimum during measurement. It studies the relationship between both temperatures and corrects and controls the program temperature based on this relationship.

Auto Step Temperature Control Feature

This feature improves the reaction of the temperature dispersion by changing the speed of the temperature increase in response to the reaction speed of the DTMA signal [65].

4.3.3 Differential Scanning Calorimetry (DSC)

Calorimetry is one of the primary techniques for measuring the thermal properties of materials to establish a connection between temperature and specific physical properties of substances [66]. Differential scanning calorimetry measures the difference in the amount of heat

required for increasing temperature of the sample and reference as a function of temperature. It can also measure the amount of heat absorbed or released during these transitions. The thermal properties of the polymer and the decomposition behavior are studied using differential scanning calorimetry. It also detect the transitions of melts, glass transitions, phase changes, and curing [67]. In a heat flux DSC system, the sample and reference are heated at the same rate from a single heating source. Temperature difference between the pans is recorded and converted to a power difference. This power difference gives the difference in heat flow [66].

$$\Delta P = \frac{\Delta Q}{dt}$$

Heat is be supplied to raise the temperature of a material. The amount of energy required to heat one gram of the material one degree Celsius is specific heat capacity of a material. Specific heat capacity (C_p) is characteristic thermodynamic property of a material. Using DSC, the heat flow in a sample is measured. It is a measure of how the material stores additional energy at the molecular level when it is heated. For instance, if the molecules in the material can only vibrate, as in a crystal, then heat flow is low; if they can also rotate and translate, then the heat flow becomes higher. When a material is heated through the glass transition region, the molecules gain mobility, the material softens, and heat flow increases [68]. Thus, heat flow indicates changes in structure. In an ideal DSC, the empty pan baseline would be a straight line at zero milliwatts. If a sample were heated in this ideal DSC then the displacement from the zero line would be given by [69] [70].

$$dQ/dt = C_p * \beta * W$$

where,

dQ/dt is heat flow,

β is heating rate and

W is the sample specimen mass.

In this study, thermal gap filler material is used for the study. Thermal Gap Fillers are used to fill air gaps between components or PC boards and heat sinks, it is important to study the thermal properties of this material. In general, gap filler materials are viscoelastic in nature. These materials have rubber like properties, and they are called elastomer. Elastomers are special polymers that have both high viscosity and elasticity. The glass transition temperature of elastomer is well below the room temperature and they can be envisaged as one large molecule of macroscopic size [71]. DMA is used to confirm its viscoelastic nature. There is a certain temperature called the glass transition temperature (T_g) at which polymeric material shows state changes. While the polymer is cooled below this temperature, it becomes hard and brittle, like glass and above this temperature they behave like rubber [72]. So, it is obvious that elastomer should behave like rubber at room temperature as the glass transition temperature is very low for elastomer. Intermolecular forces between the polymer chains are weak and crosslinks completely suppress irreversible flow but the chains are very flexible at temperatures above the glass transition, and a small force leads to a large deformation [73] [74]. So, elastomers have a low Young's modulus and very high elongation at break when compared with other polymers.

When the temperature drops, elastomers become harder and less flexible and when the temperature reaches the glass transition temperature, they lose their rubber-like properties entirely. At even lower temperatures they may crack. Generally, changes in elastomer properties due to low temperature are physical, and fully reversible unless the elastomeric part is exposed to large

tensions which can cause damage below the brittle or glass transition temperature. The opposite is true when an elastomer is exposed to high temperatures, that is to temperatures near or above the service temperature limit. At these temperatures, elastomers often undergo irreversible chemical changes. For instance, the polymer backbone may undergo chain scission, or the polymer molecules may crosslink, causing the elastomeric part to become either softer or more rigid, which, in turn, reduces their resistance to compression set [71] [75].

4.3.3.1 Differential Scanning Calorimeter (DSC)

Differential Scanning calorimeter (DSC) will be used to measure the heat capacity of the thermal interface materials. For this study model DSC 25 will used. DSC is a thermodynamical tool for direct assessment of the heat energy uptake, which occurs in a sample within a regulated increase or decrease in temperature. In this process calorimetry is particularly applied to monitor the changes of phase transitions [76] [77].



Fig. 4.8: Differential Scanning Calorimetry Setup.

4.3.4 FTIR

Fourier transform infrared (FTIR) spectroscopy has been the dominant technique used for measuring the infrared (IR) absorption and emission spectra of most materials, with substantial advantages in signal-to-noise ratio, resolution, speed, and detection limits. One of the major advantages of the FTIR technique over other spectroscopic method is that practically all compounds show characteristic absorption/emission in the IR spectral region and based on this property it can be analyzed both quantitatively and qualitatively [78]. For this experiment Thermo Nicolet 6700 FTIR Spectrometer is used to evaluate the chemical compounds properties in the samples.



Fig. 4.9: Thermo Nicolet 6700 FTIR Spectrometer [79]

4.3.5 Broadband Dielectric Spectroscopy (bBDS)

Broadband Dielectric Spectroscopy (bBDS) is the study of the interaction of electromagnetic waves with matter. Determining the dielectric properties of a material it has become a very prominent tool. Morphological homogeneity, the interactions of structural and electrical properties between the particles, and the shape as well as the orientation of the combining phases are several different factors that can change the dielectric spectra of a heterogeneous

material. Dielectric properties of a heterogeneous material are generally calculated in the frequency range of 10^{-6} Hz to 10^{12} Hz.

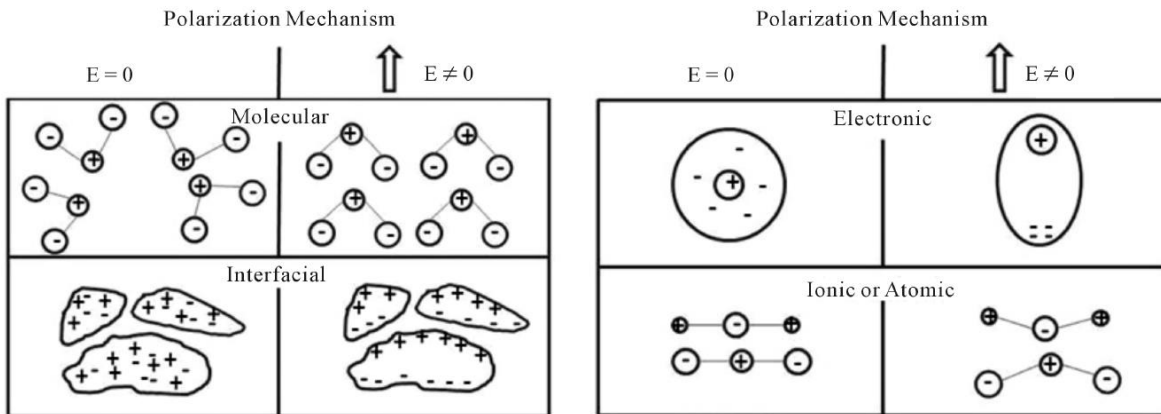


Fig. 4.10: Dielectric responses of material constituents at broad band frequency ranges and different polarization mechanism [80]

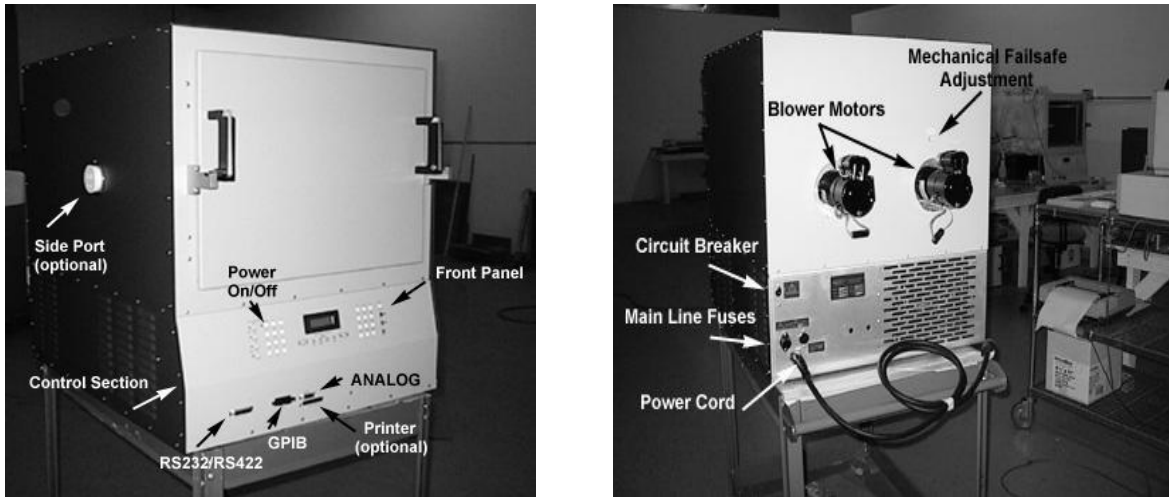
The interaction between matter and electromagnetic waves are characterized in detail using Maxwell's equations. The material system is made of various polarization mechanisms such as ionic (molecular), dipolar (orientational), interfacial (Maxwell–Wagner–Sillars), electronic polarization and hopping charge polarization [80].

4.4 Temperature and Humidity Test Chambers

4.4.1 Temperature Test Chamber

The temperature test chamber that will be used for this study is model EC127. Samples placed inside the chamber area subjects to either cooled or heated air which circulates from the intake in rear of the test chamber area, vertically downwards back into the test chamber area, across the roof of the test chamber and inside the baffle. Inside test chamber area baffle, resistance heaters heat the circulating air and the refrigeration systems evaporator cools the air. The controller in the Model EC127 automatically maintains the desired temperature and rate of change of temperature in the chamber test area. The controller of this chamber uses Proportional, Integral

and Derivative (PID) control techniques. If needed it is possible to tailor, the characteristics of the PID algorithms independently for both heat and cool [81].



(a)

(b)

Fig. 4.11: (a) EC 127 front view, (b) EC 127 rare view [81]

4.4.2 Thermotron Environmental Chamber

The environmental chamber in Fig. 6 will be used for the preparation of the prepare the thermal aged samples. The temperature range of this environmental chamber is -70°C to 180°C . It has temperature control of $\pm 0.3^{\circ}\text{C}$ ($\pm 0.5^{\circ}\text{F}$). The standard deviation from mean is measured at -25°C (-13°F) or 100°C (212°F). Climatic Chamber performance is based upon laboratory ambient conditions of 23.9°C and may vary slightly. Environmental Chambers with listed water requirements can be built with remote air-cooled condensers. This equipment is not designed to process hazardous materials [63].



Fig. 4.12: Thermotron Environmental Chamber

4.5 Sample Preparation

Commercial silicone based and silicone free based thermal interface materials are tested to determine the mechanical, thermal, and dielectric properties of the thermal gap filler materials.

4.5.1 Sample Preparation Method

Thermal gap filler samples are prepared using the Steel plates. Spacers are placed in between the plates. Pressure is inserted using clamps. Using the manufacturer specification, the materials are prepared. The schematic shows how force is applied on the samples to get the required dimension of the sample.

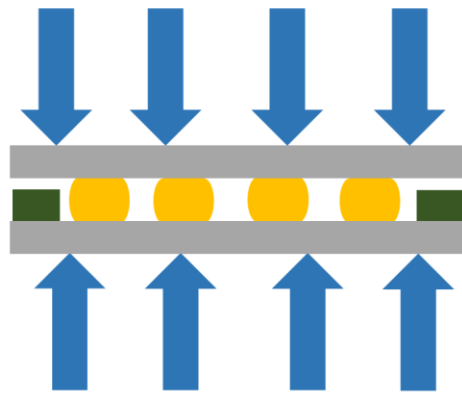


Fig. 4.13: Schematic diagram of TIM sample preparation

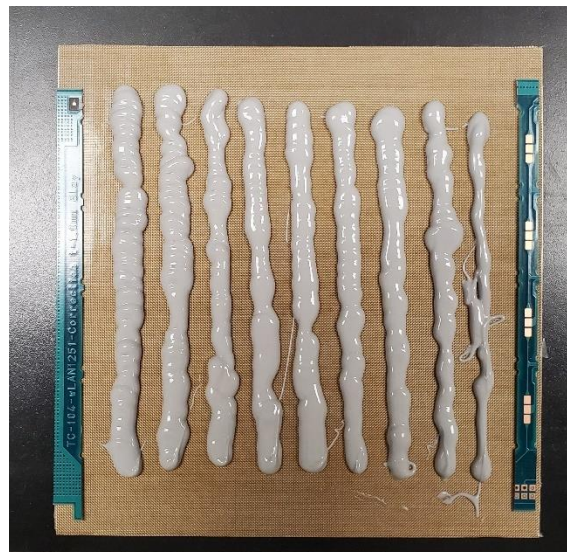


Fig. 4.14: TIM A Dispensed on the Steel Plate on top of Teflon sheet and spacers on the sides

4.5.2 Cured Sample

Using the manufacturer specification, the materials are cured. The Fig. 4.15 below shows cured silicone free sample.

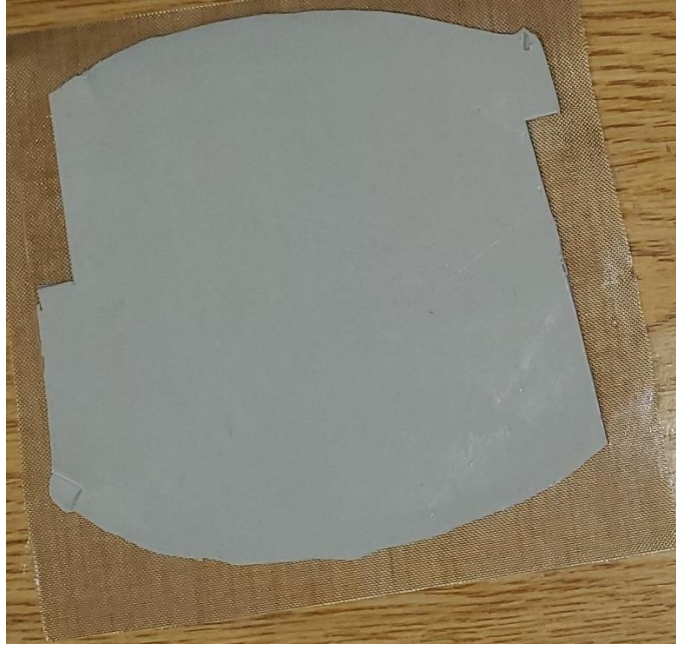


Fig. 4.15: Cured Silicon based sample



Fig. 4.16: Cured silicone free TIM sample

4.5.3 Thermal Aging

The thermal storage life of the thermal interface material is measured using following JESD22-A103E standard. The conditions for the high temperature storage life is mentioned in Table 4.1. Considering the automotive electronics, condition A has been chosen. One set of samples are maintained at Condition A for 2000 hours.

Table 4.1: High temperature storage conditions [82].

Condition A: +125 (-0/+10) °C
Condition B: +150 (-0/+10) °C
Condition C: +175 (-0/+10) °C
Condition D: +200 (-0/+10) °C
Condition E: +250 (-0/+10) °C
Condition F: +300 (-0/+10) °C

Another set of samples for both TIM A and TIM B are maintained at 85°C for 300 hours and results are analyzed for both types of thermal interface materials.

4.6 Experimental Results and Discussions

In this study, material characterization will be performed for two different types of thermal interface materials, these are silicone based and silicone free thermal interface material. these are silicone based and silicone free thermal gap filler maters. Silicone based TIMs are named as TIM A and silicone free TIMs are named as TIM B.

TIM A – Silicone based TIM

TIM B – Silicone free TIM

Silicone based thermal interface materials are used in industries for some time. Silicone free thermal interface materials are not as prevalent as silicone based thermal interface materials.

In many applications such as optical, medical, and sensor devices certain requirements preventing manufacturer from using silicone-based products [83]. Temperature Test Chamber is used for performing the thermal aging of the TIMs. The Fig. 4.16 shows the thermal gap filler materials inside the thermal chamber.



Fig. 4.17: TIM samples inside the thermal chamber.

This study focuses on the effect of temperature on silicone based and silicone free thermal interface materials at different thermal aging duration. Properties of thermal interface materials are required to know to select the right thermal interface material for a device. Mechanical properties such storage modulus, loss modulus, coefficient of thermal expansion is measured. Dynamic mechanical behavior of thermal interface materials is measured with dynamic mechanical analysis. The storage and loss modulus are measured for silicone based and silicone free thermal interface material using dynamic mechanical analyzer.

Change in relative length with the change of temperature is measured using Thermomechanical Analyzer for silicone based and silicone free thermal interface materials. Thermal, dielectric, and chemical compound properties of the thermal interface materials (TIMs)

are measured using differential scanning calorimetry and dielectric properties of the thermal interface materials will be measured using broadband dielectric spectroscopy.

4.6.1 Complex Modulus

4.6.1.1 Complex Modulus of TIM A

Complex modulus for TIM A is measured before and after thermal aging at 125°C. From Fig. 4.17 it is found that the complex modulus of TIM A is higher when it is thermally aged at 125°C. For the TIM A thermal aged samples complex modulus started to decrease after about 48°C with increasing temperature.

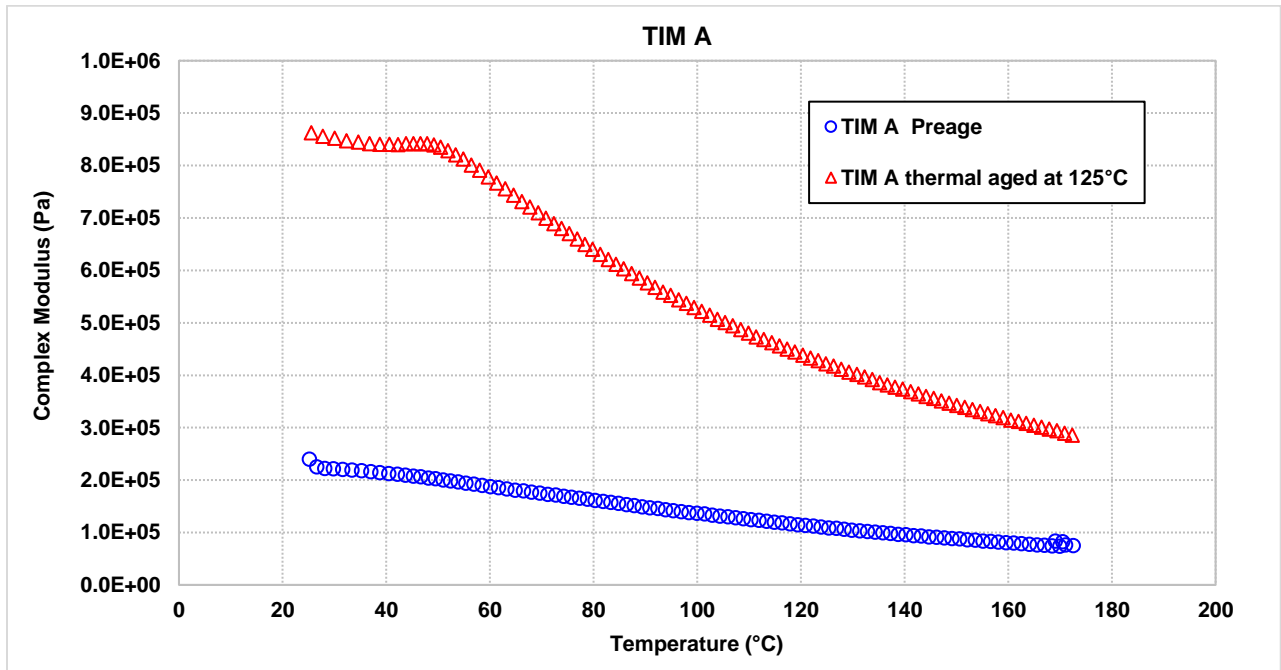


Fig. 4.18: Complex Modulus of TIM A

4.6.1.2 Complex Modulus of TIM B

For TIM B complex modulus is measured before and after thermal aging. Fig. 4.18 shows the Complex Modulus for TIM B before aging, Fig. 4.19 shows the Complex Modulus of TIM B after thermal aging at 125°C, and Fig. 4.19 shows the Complex Modulus of TIM B after thermal

aging at 85°C. The Complex Modulus of TIM B before aging is lower than the thermal aged TIM B, with increase of temperature the Complex Modulus of TIM B increases. From Fig. 4.19 it is found that the complex modulus of TIM B is much higher when it is thermally aged at 125°C. TIM B becomes hard when it is thermal aged at 125°C. When TIM B is aged at 85°C, the Complex Modulus is higher than the preage TIM B but lower than TIM B thermal aged at 125°C.

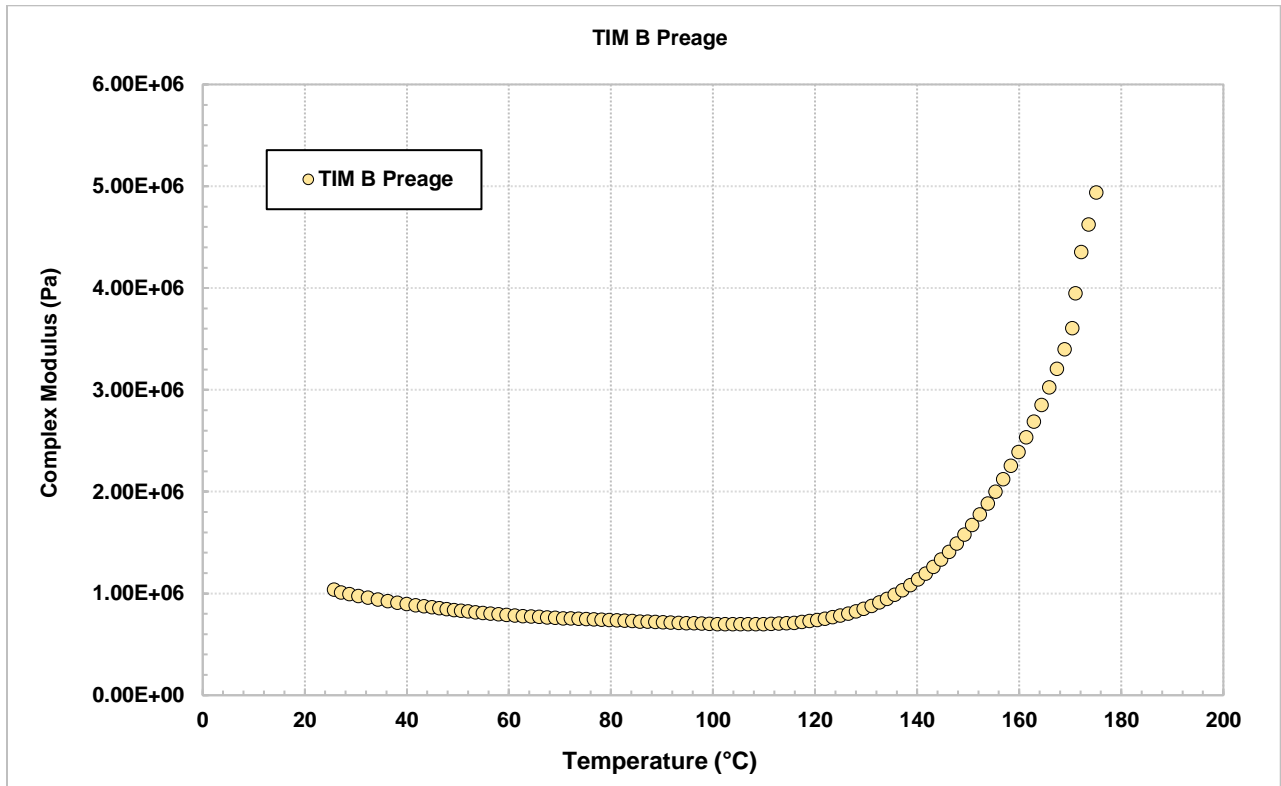


Fig. 4.19: Complex Modulus of TIM B Preage

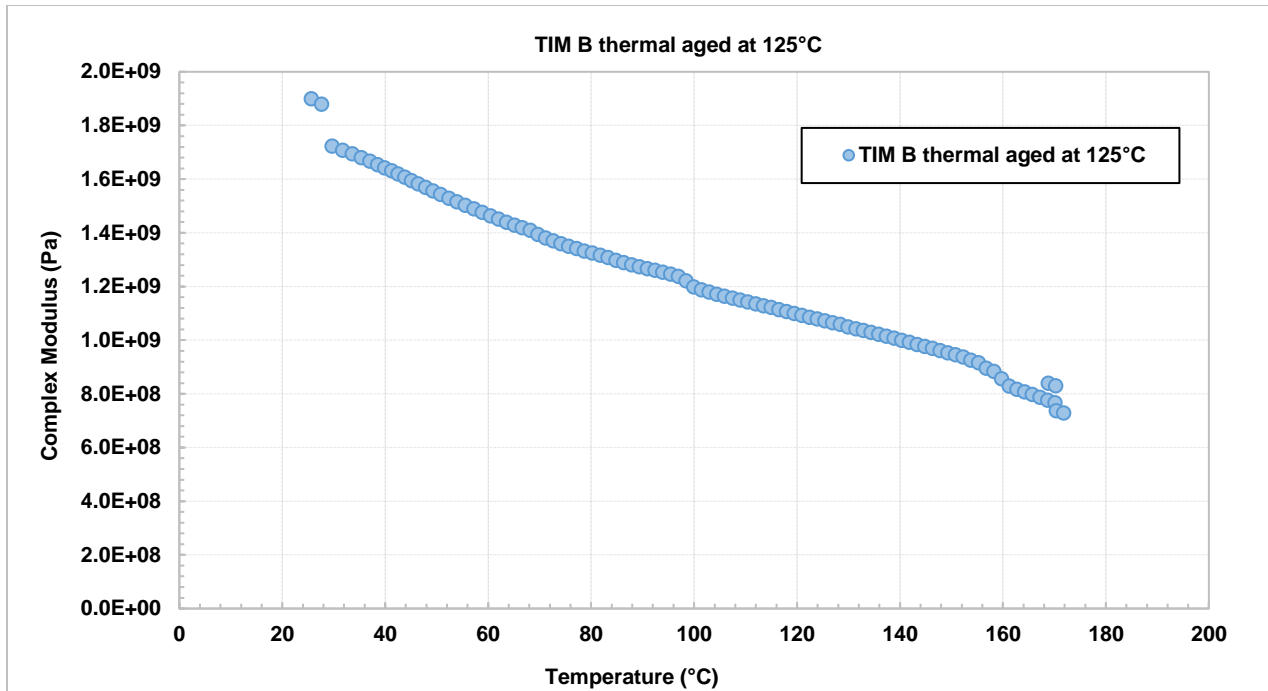


Fig. 4.20: Complex Modulus of TIM B Thermal Aged at 125°C

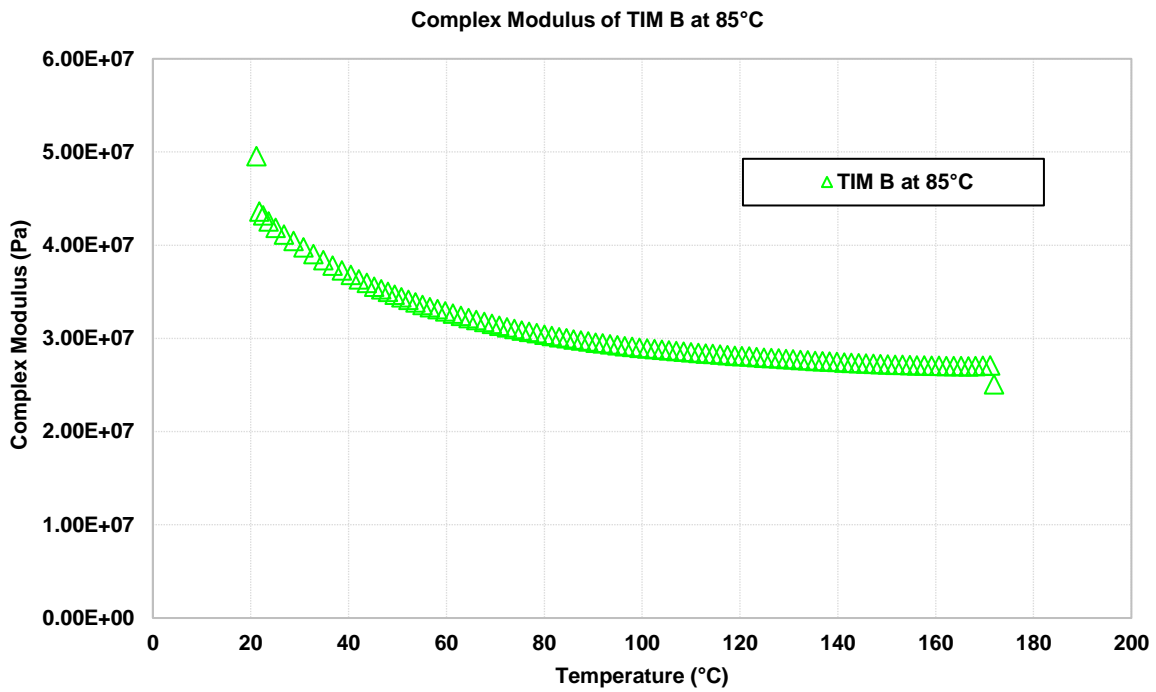


Fig. 4.21: Complex Modulus of TIM B Thermal Aged at 85°C.

4.6.2 Coefficient of Thermal Expansion

In this study change in relative length is measured with the change of temperature. For TIM A change in relative length with temperature is higher for preage samples and it is lower for TIM A thermal aged at 85° and lowest for TIM A thermal aged at 125°.

4.6.2.1 Change in Relative Length with Temperature for TIM A

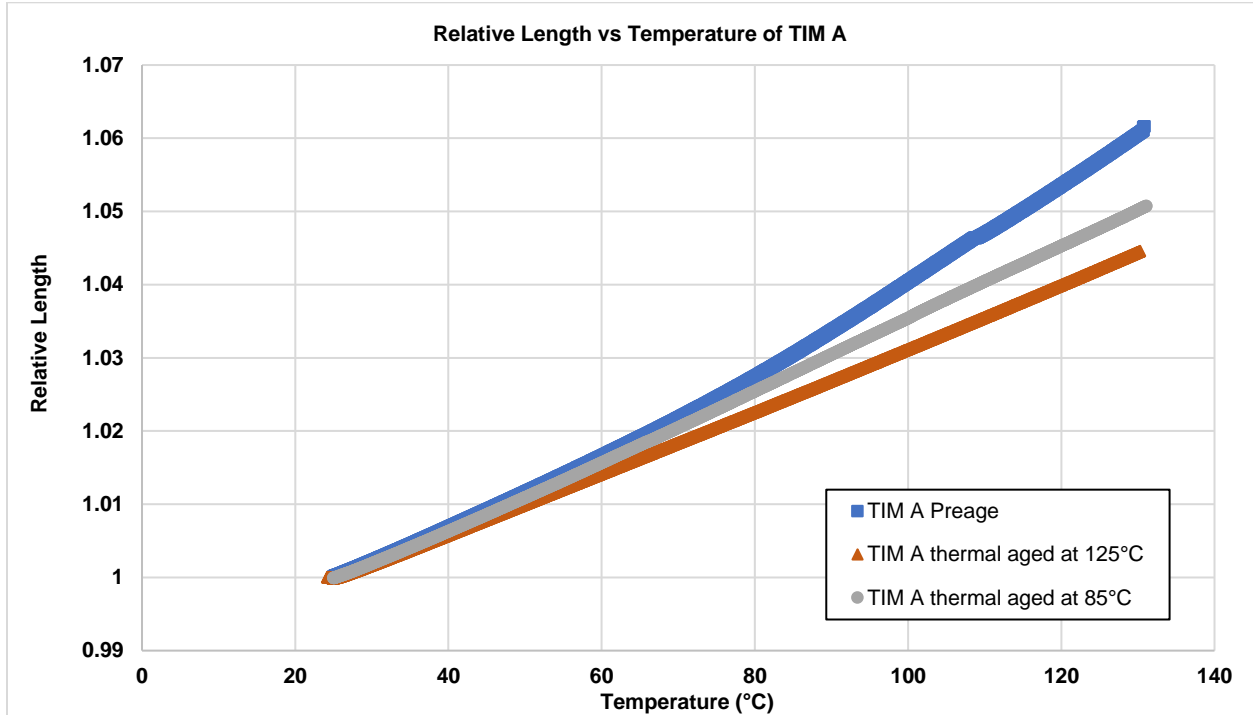


Fig. 4.22: Change in Relative Length with temperature for TIM A.

4.6.2.2 Change in Relative Length with Temperature for TIM B

Relative length is measured with the change of temperature for TIM B. In the case of TIM B change in relative length with temperature for preage and thermal aged at 125°C samples are very close. On the other hand the change in relative length with temperature for thermal aged at 85°C samples higher than preage or 125°C samples.

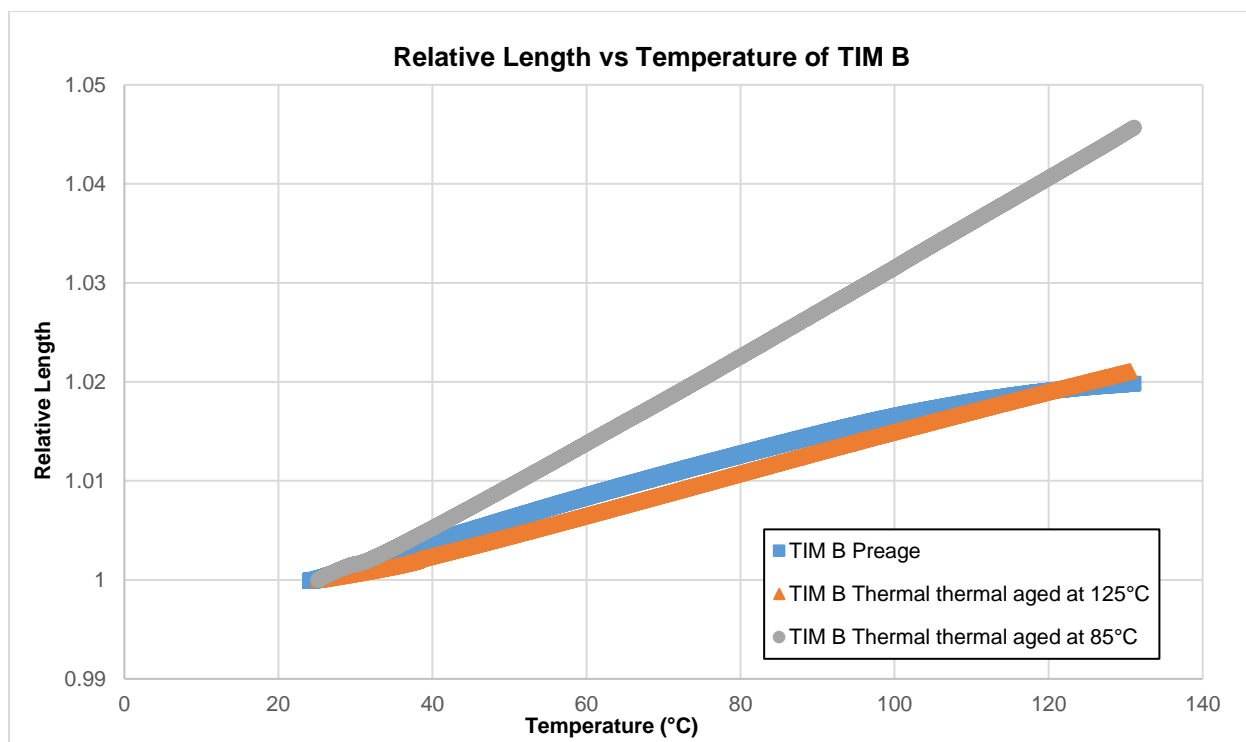


Fig. 4.23: Change in Relative Length with temperature for TIM B

4.6.3 Thermal Properties

In this study, two types of gap filler material TIM A and TIM B are used. Discovery DSC 25 is used to analyze the thermal properties. Tzero Aluminum pan is used and a ramp from 40°C temperature to 450°C at a heating rate of 5, 10, and 15 °C/min to investigate changes of thermal properties occurred in this temperature range.

4.6.3.1 Thermal Properties of TIM A

At 220°C, TIM A showed sudden drop of heat flow. There is a certain transition occurred at this temperature. From DSC curve it is assumed the rubber like mixture undergoes decomposition at this temperature. The DSC curve showed heat flows into the sample because of some endothermic process such as melting, evaporation, decomposition etc. During the decomposition, reaction occurred inside the material that causes a visible exothermic peak in the

DSC curve. There is a good possibility that oxidation occurred, and the polymer molecules may crosslink.

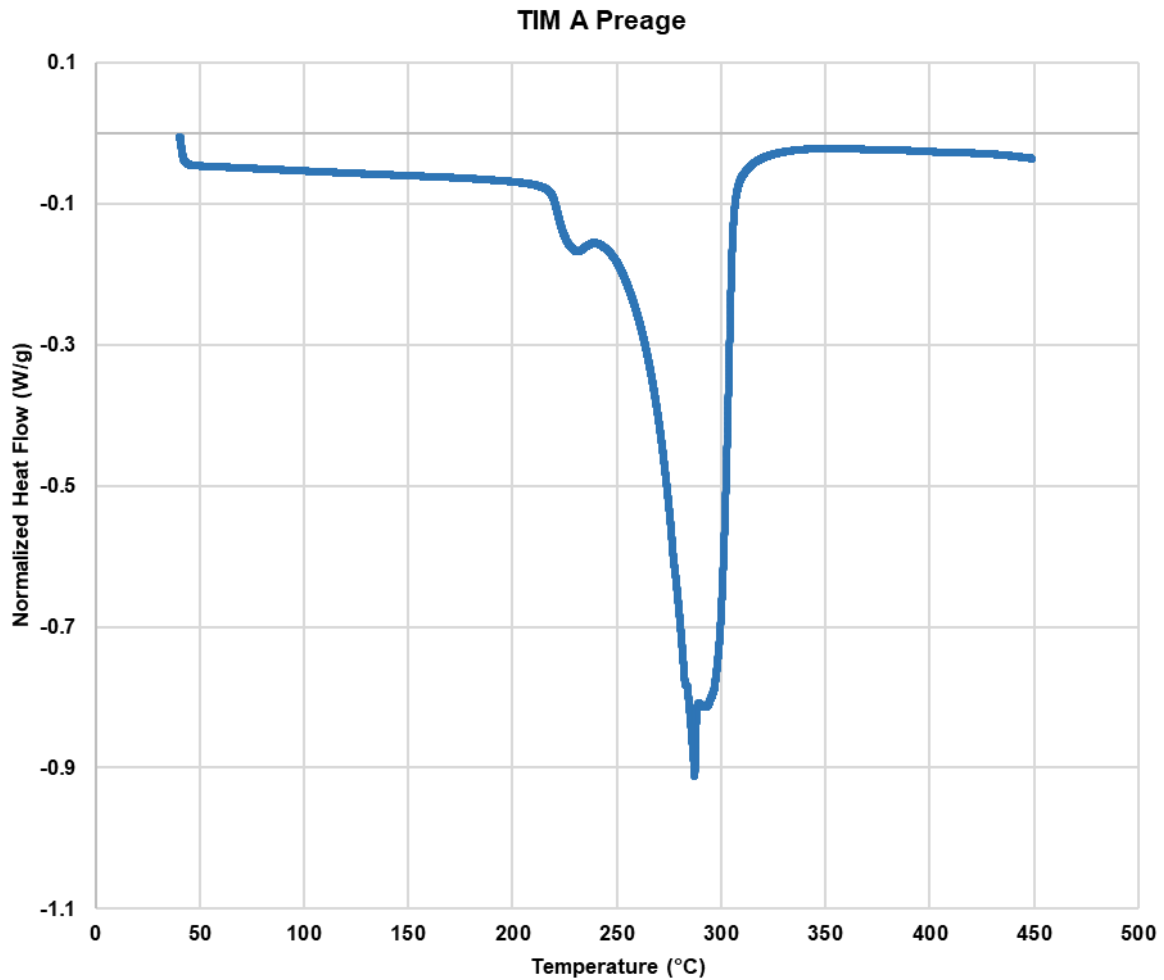


Fig. 4.24: Normalized Heat Flow vs Temperature for TIM A Preage samples

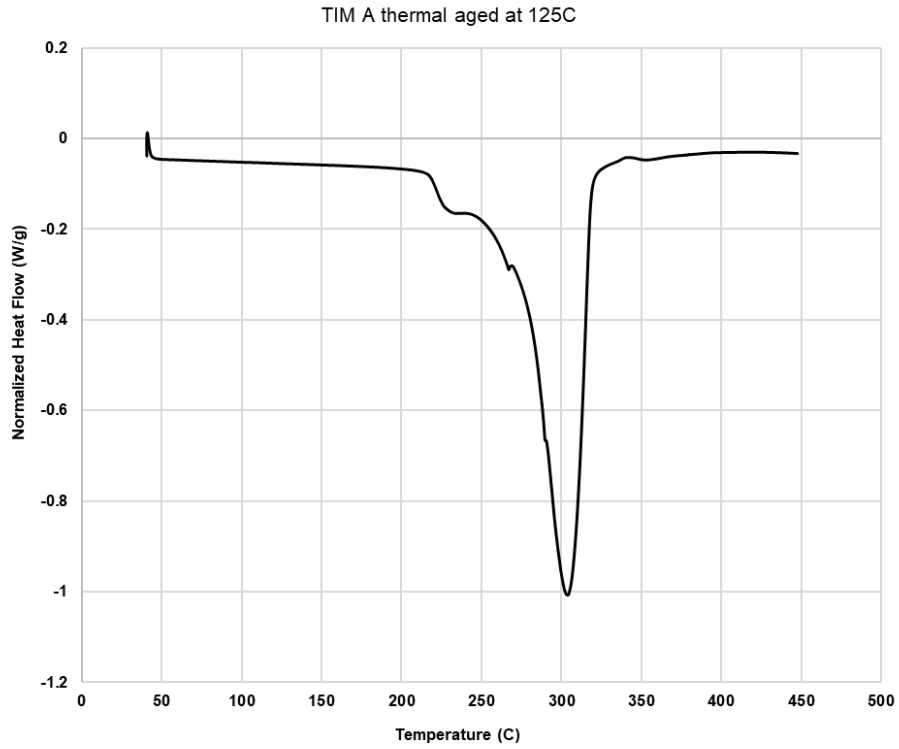


Fig. 4.25: Normalized Heat Flow vs Temperature TIM A thermal aged at 125°C

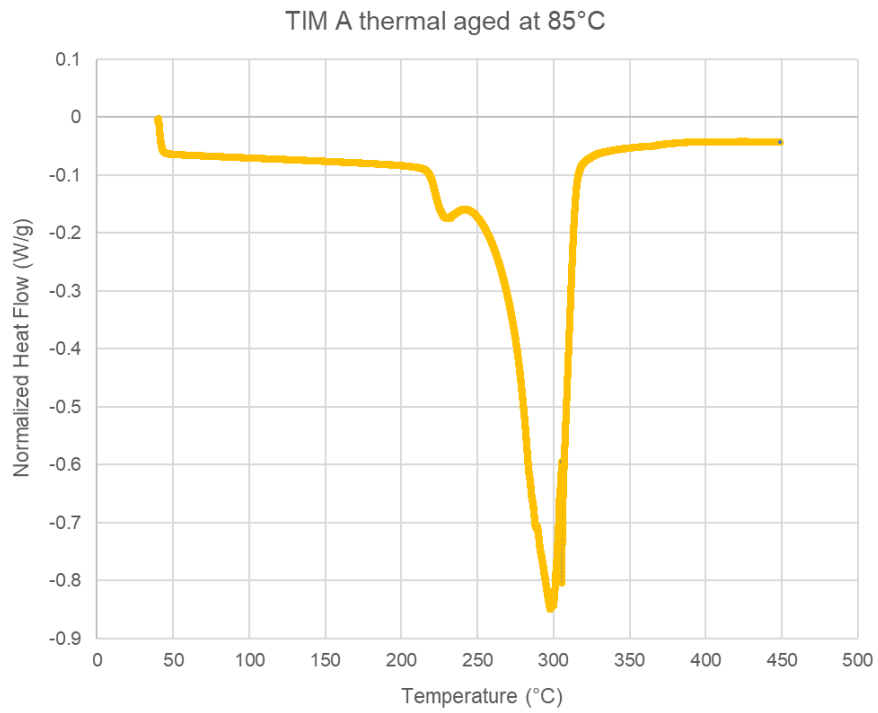


Fig. 4.26: Normalized Heat Flow vs Temperature thermal aged at 85°C

The crosslinking will cause the elastomeric part to become hard. That is why during thermal aging, TIM B became hard and showed brittle like behavior. Hardening is common since free radicals are produced when rubber is exposed to heat and oxygen, in this process, new crosslinks form. Under certain conditions cross-linkers and accelerators confined in the elastomer can decrease the thermal stability because they easily undergo thermal decomposition at higher temperature producing radicals that can accelerate thermo-oxidative degradation of the network [84].

On the other hand, same DSC experiments were performed for thermally aged TIM B material with same condition. We found that thermal ageing does not change the decomposition temperature, but it is observed clear reduction in reaction heat. From this observation in thermally aged material, polymer chain is almost cross linked and there is less energy left for further reaction. Most of the elastomers will undergo significant changes over time when exposed to heat, light, or oxygen. These changes can have huge effect on the life and properties of the elastomers can only be prevented or slowed down by the addition of UV stabilizers, antiozonants, and antioxidants [85][86].

Depending on the microstructure of the diene elastomer, oxidative degradation will either cause hardening or softening. For instance, polybutadiene usually undergoes oxidative hardening whereas polyisoprene softens when exposed to oxygen and heat [87]. On the other hand polymers with pendent bulky side groups will undergo strain softening since radical recombination reactions are less likely to occur because of steric hindrance. Alternatively, these polymers degrade by chain scission caused by disproportionation and hydrogen abstraction. And for this reason, preaged TIM A shows softening during heating. From DSC curve, we found thermal degradation occurred at 225°C. The preage material showed reaction heat at 245° Celsius that can be explained by thermal

oxidation with subsequent chain scission. On the contrary, it is assumed that thermally aged TIM A showed less reaction heat in DSC curve and polymer scission already occurred during thermal aging. To surely validate our findings, we used FTIR to understand chemical compound changes in material with thermal aging.

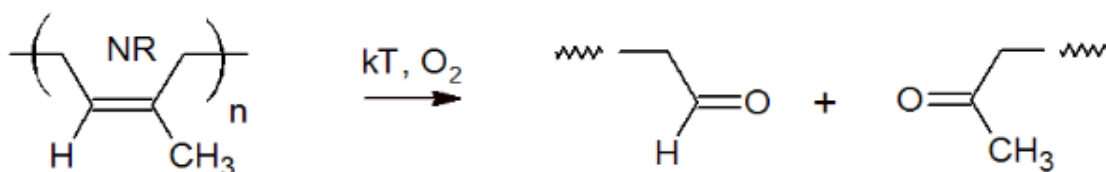


Fig. 4.27: Oxidative Softening - Chain Scission [87]

If we compare the heat flow direction, it is very clear from the curve that TIM A sample shows endothermic heat flow that means it absorbs energy with respect to empty reference pan. However, TIM B showed exothermic heat flow that means it dissipates heat.

From the DSC curve we found that around 220°C this material showed a sudden drop in heat flow. DSC curve showed that heat flowed into the sample as a result of some endothermic process such as melting, decomposition, evaporation occurred in the sample.

As the temperature increases the material undergoes chemical changes. For example, the polymer backbone may have undergone a chain scission. That's why after thermal aging there is no change in elastic behavior. It is found from the DSC curve that there is oxidation occurred in the sample during thermal aging.

4.6.3.2 Thermal Properties of TIM B

Around 215°C there is a sudden drop in temperature. From the DSC curve we are assuming some oxidation also occurred and polymer molecule undergone crosslinking. The crosslinking will cause the elastomeric part to become hard. That is why during thermal aging, TIM B became hard and showed brittle like behavior. Hardening is more common because free radicals produced when this material is exposed to heat and oxygen, and thus from new crosslinks.

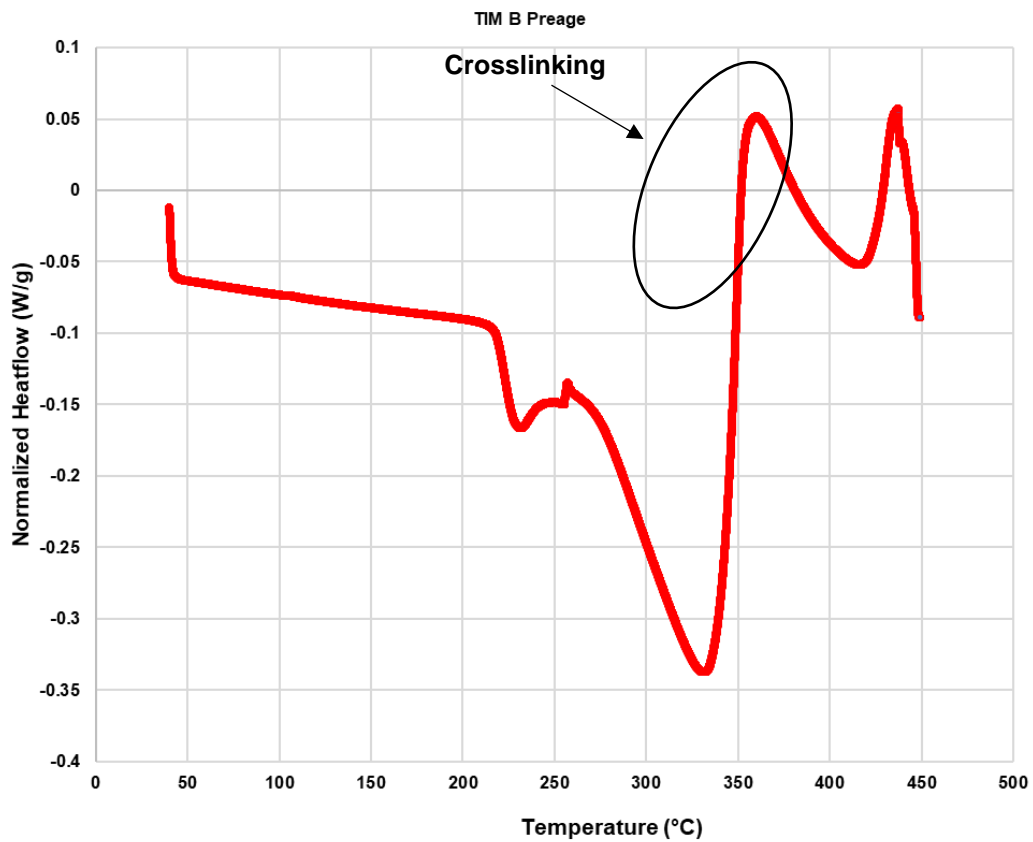


Fig. 4.28: Normalized Heat Flow vs Temperature TIM B preage samples

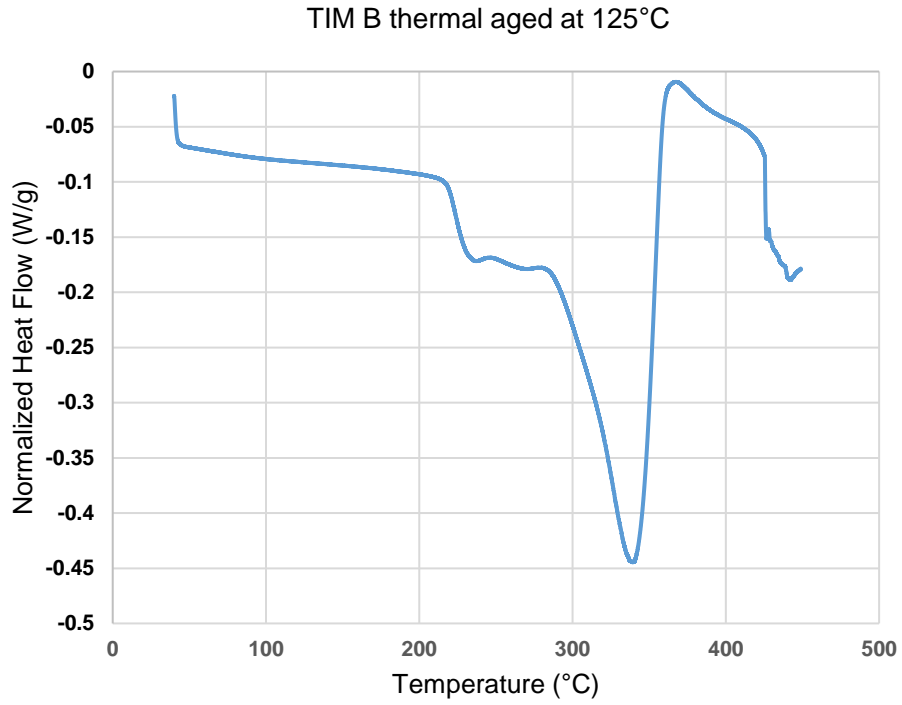


Fig. 4.29: Normalized Heat Flow vs Temperature TIM B thermal aged at 125°C

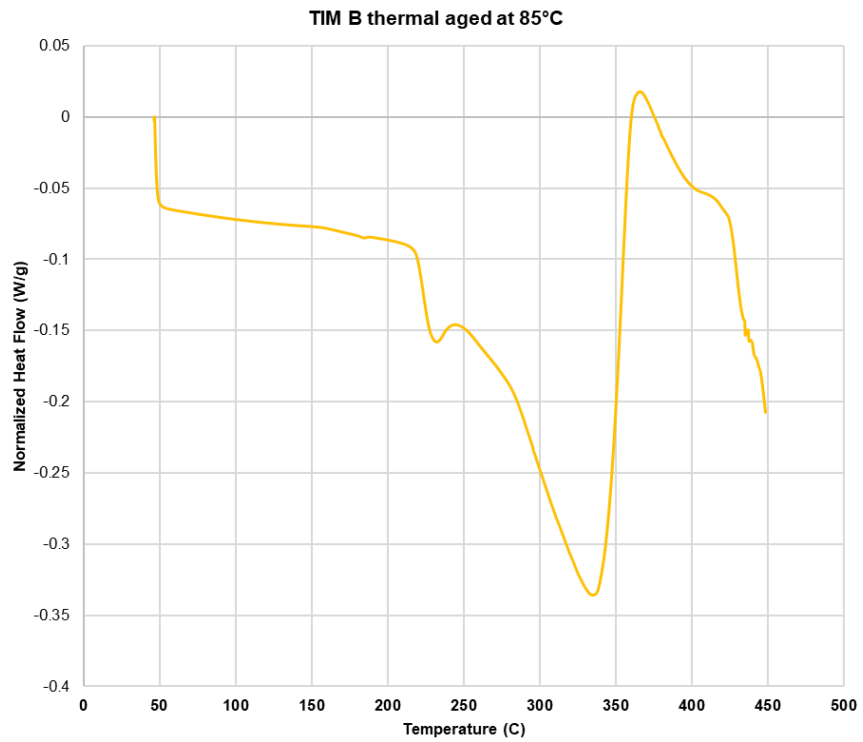


Fig. 4.30: Normalized Heat Flow vs Temperature TIM B thermal aged at 85°C

4.6.4 Chemical Compound Properties Measurement using FTIR

For this experiment we used NICOLET 6700 FTIR to evaluate the chemical compounds in the samples. For every sample 32 scans were collected. The spectra were collected for wavelength of 4000cm^{-1} to 600 cm^{-1} .

4.6.4.1 Chemical Compound Properties Measurement using FTIR for TIM A

TIM A preage material showed intense peak at 1258 cm^{-1} wavelength which indicates the presence of silicon organic compounds with a methyl group. Methyl groups attached to a silicon atom give rise to a characteristic sharp symmetrical deformation absorption around 1260 cm^{-1} [88]. The asymmetrical deformation is weaker and occurs around 1400 cm^{-1} . As the material is thermally aged, it is found that a certain decrease in the intensity at this wavelength which indicates polymer chain scissions occurred during thermal aging. Moreover, the peak at 2962cm^{-1} wavelength is analyzed, it shows CH_3 and CH_2 bond decreases with thermal aging. This is a clear indication of polymer chain scission. The thermally aged material showed a small peak at 1515 cm^{-1} wavelength from which it can be assumed that there was oxidation during thermal aging. The peak at 1515 cm^{-1} wavelength represents 3,4-dihydroxy-3-cyclobutene-1,2-dione functional group [89]. TIM A preage sample also showed peak at 3520 cm^{-1} and 3438 cm^{-1} wavelength which defines -OH bond (Carboxylic acid) and -OH stretching vibration. In thermally aged sample, the intensity decreased which indicates that -OH bond was broken at elevated temperature and free oxygen caused thermal oxidation.

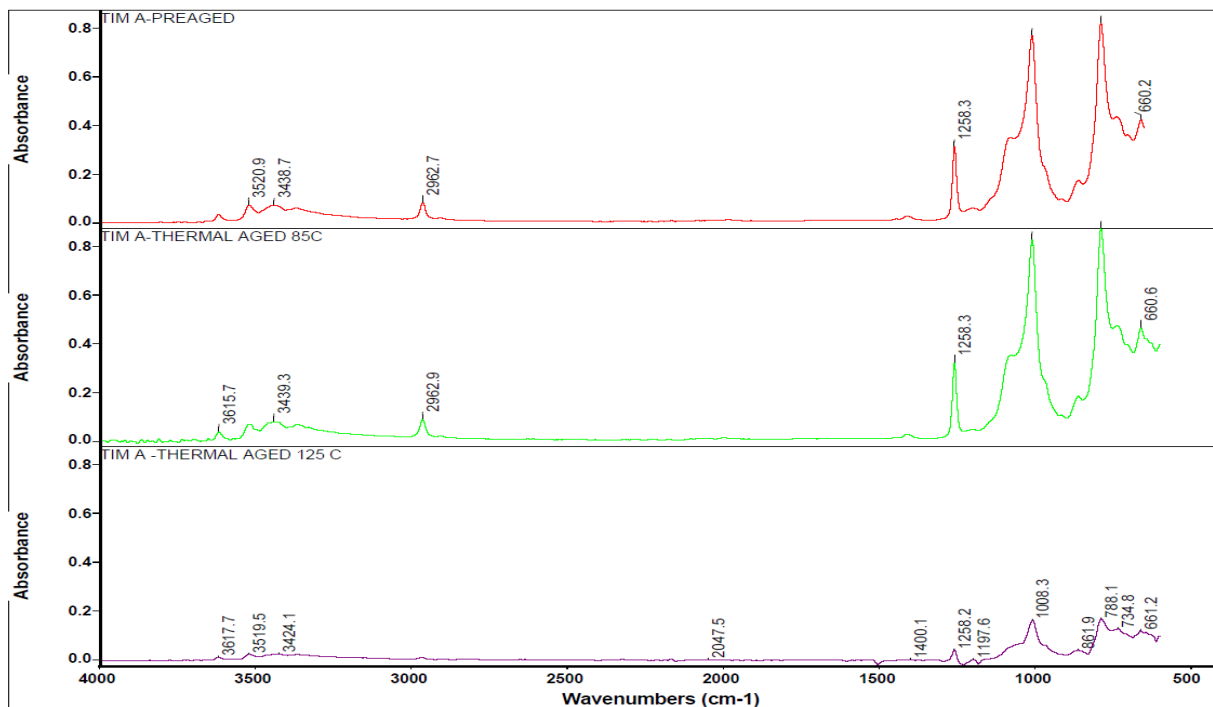


Fig. 4.31: FTIR Spectra for TIM A

4.6.4.2 Chemical Compound Properties Measurement using FTIR for TIM B

FTIR analysis is performed for preaged TIM B and thermally aged TIM B, it is found that CH₃ and CH₂ bond increases with thermal aging at 2921 cm⁻¹ wavelength which indicates with thermal aging polymer chain crosslink. The FTIR also shows the presence of -OH and C=O functional group at the wavenumber 3452 cm⁻¹ and 1710 cm⁻¹, respectively. C=O stretching vibration generally occurred at 1711 cm⁻¹wavelength [90].

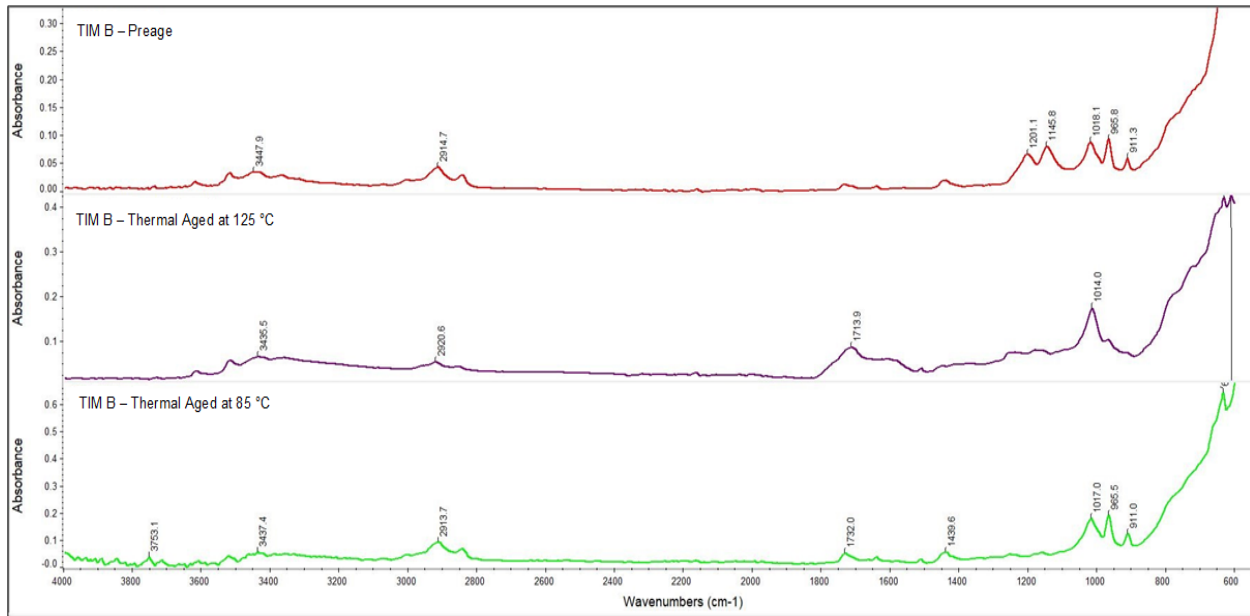


Fig. 4.32: FTIR Spectra for TIM B.

So, there was a good possibility that the sample went through thermal oxidation during thermal aging and assumed during thermal aging C=O bonds degraded, and more hydrogen bond formed. From the FTIR data we see that there is no peak at 1258 cm^{-1} , so it indicates that it is silicon free TIM. At peak 965 cm^{-1} , for preaged material there is a presence carbon-carbon double bond. With the thermal aging we found that the density of carbon-carbon double bond decreases. From the literature it is known that as the carbon-carbon double bond decreases more crosslinking occurs and found that oxidation occurred which cause the presence of Carbonyl functional group in the thermally aged material. From FTIR result it is confirmed the TIM A is silicone-based material, however, TIM B is silicone free elastomer.

4.6.5 Dielectric Properties

The dielectric properties of the thermal interface materials are measurement by Broadband Dielectric Spectroscopy (bBDS). From bBDS the dielectric properties, such as the Dielectric

relaxation (DRS) value were calculated from real permittivity value at different frequency [91].

For the measurement 1-volt AC current fluctuates in between 10^{-1} to 10^6 Hz.

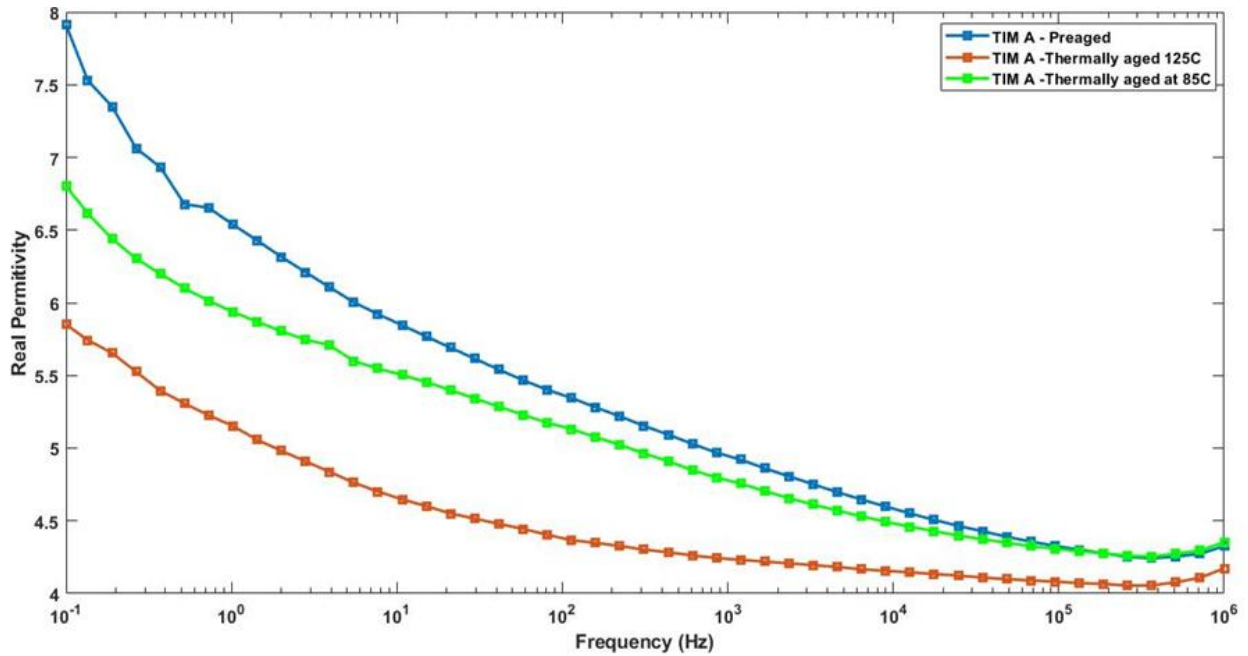


Fig. 4.33: Real Permittivity of TIM A.

The complex permittivity has real and imaginary parts. Here the real part expresses the ability of a material to polarize in response to an applied field. Greater the polarization developed by a material in an applied field of given strength, the greater the dielectric constant. The imaginary part is associated with dielectric loss. When AC electric field is applied, the electric field direction is altered with a certain frequency. The molecules inside the material also change its dipole direction with altering AC electric field. This is called orientational polarization. This phenomenon only occurs when the frequency range of AC current fluctuates in between 10^{-1} to 10^6 Hz [60].

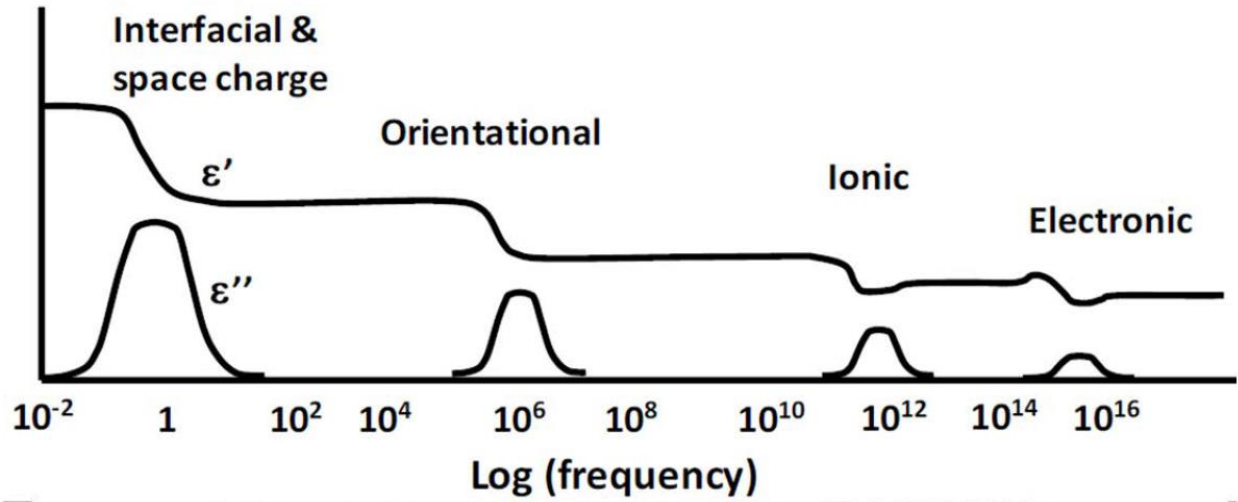


Fig. 4.34: Dielectric response of material constituents at broad band frequency ranges [80]

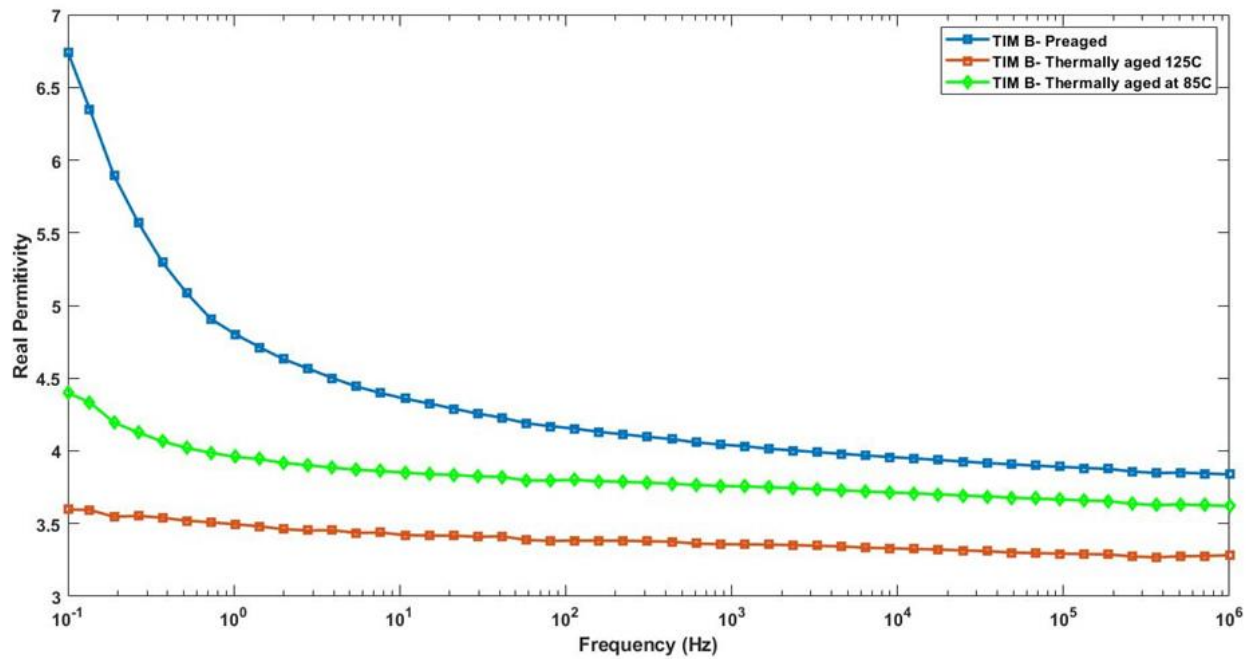


Fig. 4.35: Real Permittivity of TIM B

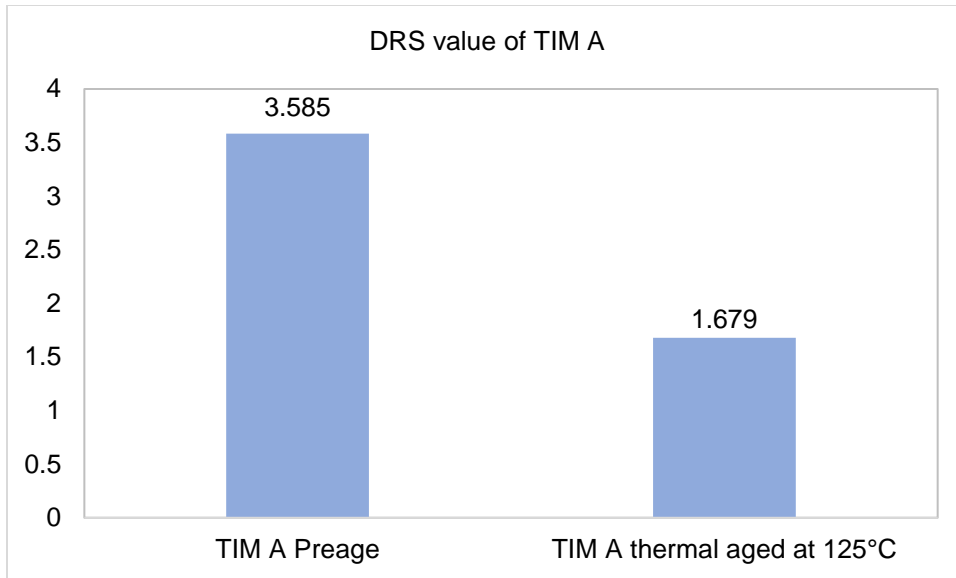


Fig. 4.36: DRS value of TIM A

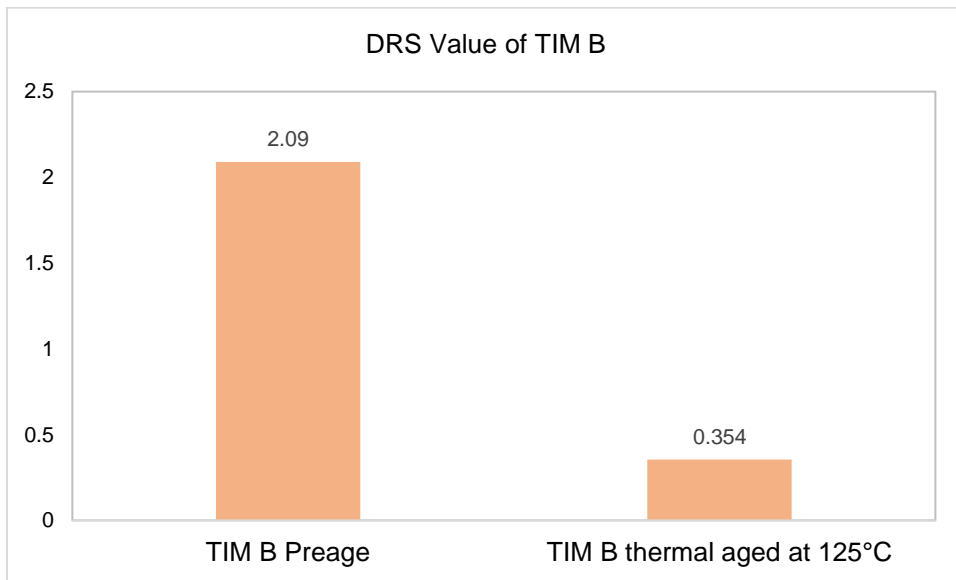


Fig. 4.37: DRS value of TIM B

For both type of sample DRS value decreased with thermal aging. That means electrical conductivity decreases with the thermal aging and less polarization occurs inside the material. For TIM B thermally aged sample, polymer crosslinking degrades the dielectric property. The polymer chain does not get polarized easily due to crosslinking or bulky group in chain.

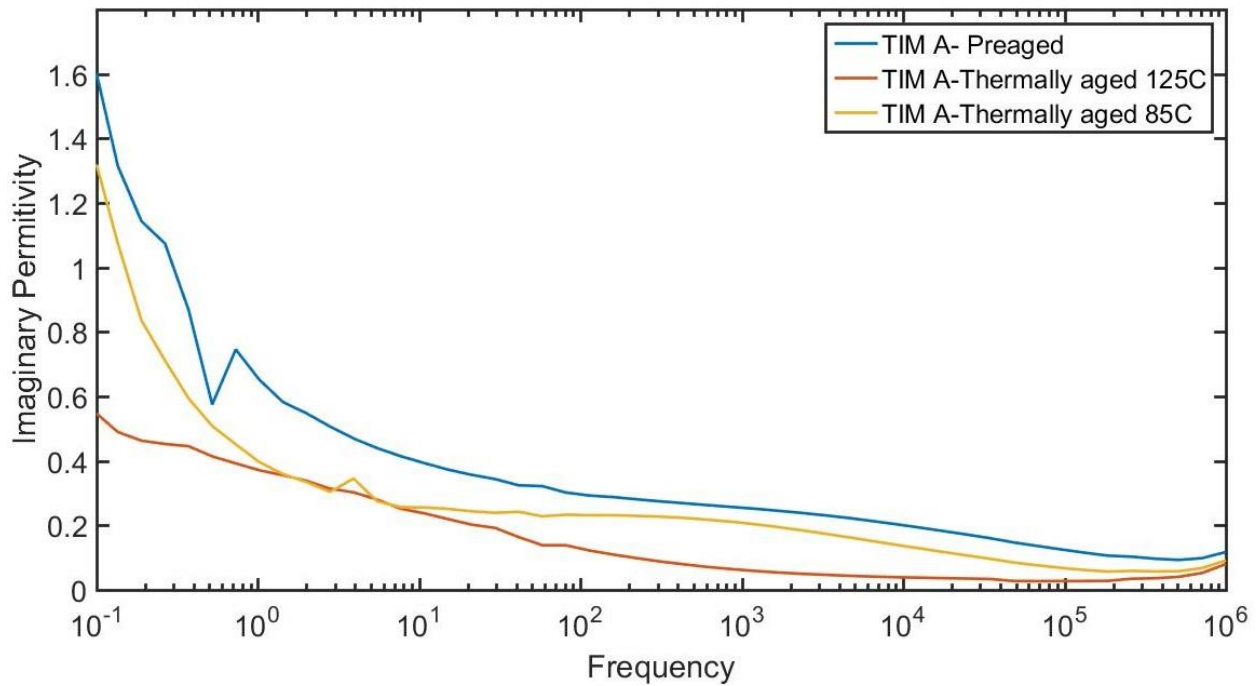


Fig. 4.38: Imaginary Permittivity of TIM A

TIM A also showed decreasing dielectric properties with thermal aging. From FTIR data it was observed that polymer chain breaks and oxidation occurred during thermal aging. The signals at 1079-1088 cm^{-1} are attributed to asymmetric vibrations of (Si-O-Si); the signals at 952-953 cm^{-1} are attributed to asymmetric vibrations of (Si-OH) [92]. With thermal aging the Si-O-Si bond density reduces that may cause decrease in dielectric properties. Besides, during oxidation, the cross-linking unzips and it swells, takes on moisture and softens [93]. The signals at 3435-3456 cm^{-1} are attributed to the stretching modes of adsorbed water molecules. From FTIR data we found -OH bond density decreases with aging that also may also increase the resistivity of the material. With increasing electric field frequency, the change of dipole direction inside material also increased. However, the atoms inside the material have inertia that cause a reluctance to move with changing electric field. So, the molecules work against the electric field at higher frequency and causes a loss which is known as dielectric loss.

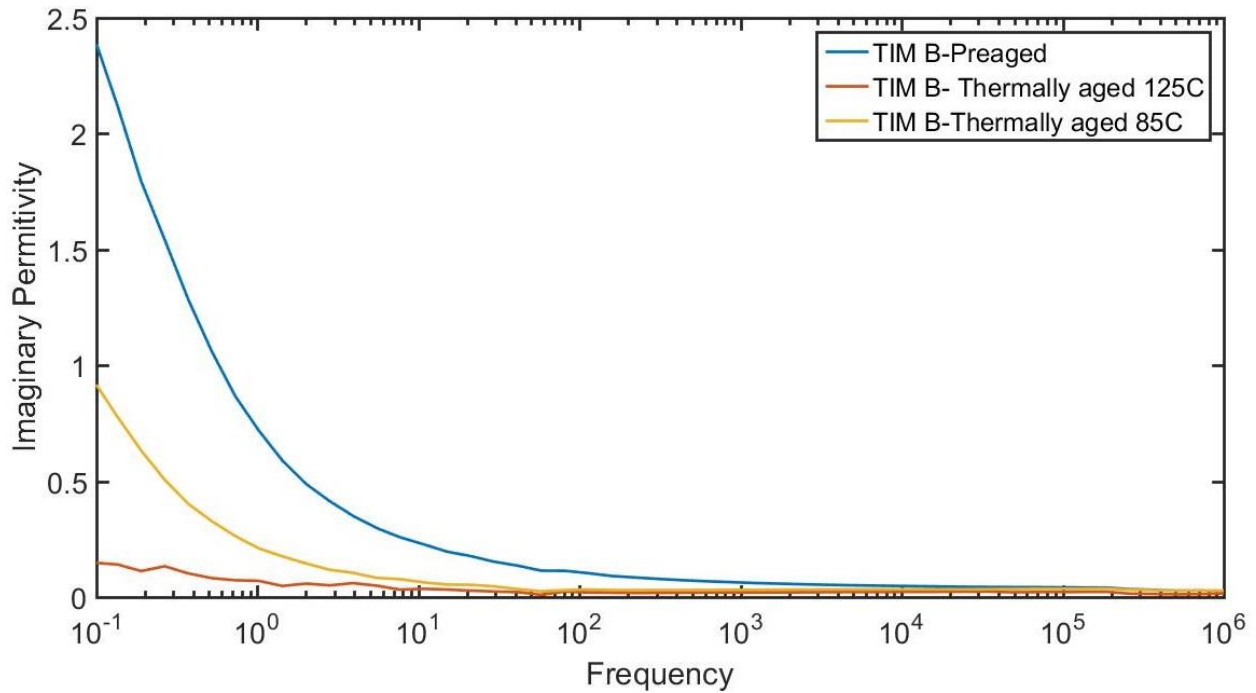


Fig. 4.39: Imaginary Permittivity of TIM B

Moreover, the imaginary permittivity also decreases for both TIM A and TIM B samples with thermal aging. The imaginary part indicates the dielectric loss of the material. As the polarization decreases in sample, the dielectric loss should also be decreased.

Chapter 5

Future Work

The back end of line (BEOL) is the second portion of IC fabrication, where the individual devices get interconnected with wiring on the wafer, the metallization layer. The total mechanical stress σ_{total} in a brittle film without plasticity deposited on a Si-substrate consists of two components, the thermal stress σ_{thermal} and the intrinsic stress $\sigma_{\text{intrinsic}}$ [94]. The stress developed on the SiO₂ layer due to effect of Intrinsic stress can be analyzed in SiO₂. APDL code for applying intrinsic stress on different layers has already been developed and applied on small scale model and it can be incorporated on a global model. Experimental analysis can be performed for 3D IC packages to find out solutions for different thermal and reliability issues. To deal with the thermal issue in 3D IC packages, artificial intelligence can be used.

Effect of temperature and humidity can be studied on different types of thermal interface materials. Using computational tools, the effect of the properties of the thermal interface materials on electronic package can be studied. The degradation of the thermal interface materials can be studied in the in-situ condition in the electronic packages. Also test vehicle can be developed to study the life cycle of thermal interface materials under different operating conditions.

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Biography

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