INVESTIGATION OF THE CHANNEL HOT CARRIER (CHC) STRESSING EFFECTS AND IDENTIFICATION OF THE STRESS-INDUCED OXIDE TRAPS LEADING TO RTS IN PMOSFETS

by

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Abstract

Investigation of the Channel Hot Carrier (CHC) Stressing Effects and Identification of the Stress-Induced Oxide Traps Leading to RTS in pMOSFETs

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Electrical stressing mechanisms are responsible for the generation of stress-induced gate SiO_2 defects, in addition to the presence of process-induced oxide traps, in MOSFETs. Random telegraph signal (RTS) can be utilized as a tool to characterize these defects. Channel hot carrier (CHC) stressing is reported to result in the worst degradation in pMOSFETs. However, the effects of CHC on RTS for pMOSFETs are under-reported. The main objective of this work is to investigate the impact of the CHC stressing on pMOSFETs by analyzing RTS. For this reason, the effects of CHC stressing on different RTS parameters are examined. Additionally, responsible defect sites are identified.

At first, CHC stressing is conducted for up to 2000 seconds with variable time intervals of 5 seconds to 200 seconds under room temperature. Then, different RTS parameters are inspected to study the impact of CHC stressing. The investigated RTS parameters are average carrier capture and emission times by the trap, trap position, trap energy level with respect to the oxide valence band edge, capture cross-section, RTS amplitude, and screened scattering coefficients. CHC stressing does not impact the position of the trap and the trap energy level with respect to the oxide valence band edge. The decrease of relaxation energy is considered to be responsible for the change in average capture time and capture cross-section with stressing for the stress-induced traps. However, further investigations are required which would focus on variable temperature measurements. The generated fixed positive oxide charges result in additional charge screening on the traps with stressing. Therefore, the Coulomb screened scattering coefficient decreases. As a result, the amount of mobility fluctuations is lowered, and we observe an increase in RTS amplitude with stressing. The novelty of this work lies in the fact that the two-dimensional mobility fluctuations model is implemented for the very first time to theoretically determine the screened scattering coefficients under CHC stressing in pMOSFETs. Later, these theoretically determined screened scattering coefficients are compared with the measured ones.

Moreover, detailed studies of the thermal activation process and structural relaxation energies are required to identify the defect centers under CHC stressing. Therefore, performing the variable temperature RTS

measurements is necessary. To fully characterize the defects, variable temperature RTS measurements are conducted from room temperature down to 215 K. CHC stressing is performed for up to 1200 seconds. Additional RTS trap parameters such as capture activation energy, emission activation energy, relaxation energy, change in enthalpy, and change in entropy are determined. Faster capture times are exhibited by the stress-induced traps, which result from the larger trap capture cross-sections. A pronounced difference is observed in the change of entropy among the process- and stress-induced traps upon hole emission from the defect site to the Si valence band. This points to the possibility of a different structural defect being responsible behind the stress-induced traps than the native ones. Two different types of defects, D-III Si and hydrogen bridge are identified as the trapping center in SiO_2 for the pMOSFETs under CHC stressing.

Like RTS, flicker (1/f) noise has also been a prominent source of noise in MOSFETs. Our goal is to find ways to passivate the traps and thereby minimize the amount of 1/f noise. 1/f noise PSD measurements are carried on nMOSFETs from three different wafers. Then the current noise PSD data are normalized with respect to the channel width, length, and oxide layer thickness. Later, 1/f noise PSD data are curve fitted to the unified numbers and mobility fluctuations (UNMF) model to determine the trap density and the screened scattering coefficients. The normalized 1/f noise data are correlated with the fabrication steps across the wafers. By incorporating necessary changes in the fabrication steps, 1/f noise can be minimized.

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List of Symbols

b	Variation parameter used in Stern-Howard wavefunction (cm^{-1})
c	Screening parameter of hole (m^{-1})
C_{GC}	Gate-channel capacitance (F/cm^2)
$C_{GC_{cor}}$	Corrected gate-channel capacitance (F/cm^2)
$C_{GC_{inv}}$	Gate-channel capacitance in the inversion region (F/cm^2)
$C_{GC_{OV}}$	Gate-channel overlap capacitance in the accumulation region (F/cm^2)
c_{hh}	Screening parameter of heavy hole (m^{-1})
c_{lh}	Screening parameter of light hole (m^{-1})
C_{OX}	Oxide charge capacitance (F/cm^2)
d_v	Valley degeneracy factor
E	Energy of an electronic level (eV)
E_C	Si conduction band edge (eV)
E_D	Donor energy level (eV)
E_F	Fermi energy level (eV)
E_g	Bandgap of Si (eV)
E_p	Energy where $Eg(E)_{2D} f_p(E)$ peaks (eV)
E_R	Relaxation energy (eV)
E_S	Energy level of state S (eV)
E_T	Trap energy level (eV)
$E_T - E_{V_{OX}}$	Trap energy level with respect to the oxide valence band edge (eV)
E_V	Si valence band edge (eV)
$E_{V_{OX}}$	Oxide valence band edge (eV)
E_{VS}	Valence band maximum in Si (eV)
E_y	Electric field along the channel (V/cm)
E_0	First allowed quantized energy level of Si valence band (eV)
E'	Oxide valence band bending along the trap position (eV)

E''	Difference of the energy level between Fermi energy level and Si valence band at the Si-SiO_2 interface (eV)
f	Frequency (Hz)
f_e	Probability of a defect site being filled with an electron
f_h	Probability of a defect site being filled with a hole
F_n	Total number of switching events in one bin
$f_p(E)$	Fermi-Dirac hole distribution function
F_s	Surface electric field (V/m)
$f_T(E)$	Fermi-Dirac probability distribution function for electron
g	Trap degeneracy factor
$g(E)_{2D}$	Two-dimensional density of states (cm^{-2})
g_d	MOSFET channel output conductance (A/V)
g_{do}	Degeneracy factor of donor
$g_e\left(N_{0_{OX}}\right)$	Generation rate of the oxide charges in the equilibrium condition (s^{-1})
$g_e(N_{OX})$	Generation rate of the oxide charges (s^{-1})
g_m	MOSFET channel transconductance (Ω^{-1})
h	Planck's constant (Js)
I	Current (A)
I_{DS}	Drain-source current (A)
k	Lattice co-ordinate ($ev^{1/2}kg^{-1/2}rad^{-1}s$)
k_B	Boltzmann's constant (JK^{-1})
k_c	Lattice co-ordinate at the intersection of two energy curves (defect site filled with a hole and empty of a hole) ($ev^{1/2}kg^{-1/2}rad^{-1}s$)
k_1	Lattice co-ordinate when the trap is empty of a hole ($ev^{1/2}kg^{-1/2}rad^{-1}s$)
k_2	Lattice co-ordinate when the trap is filled with a hole ($ev^{1/2}kg^{-1/2}rad^{-1}s$)
$K_{1/f}$	Constant used in the Hooge's flicker noise model
L	Channel length of the device (cm)
L_D	Debye length (nm)
L_{eff}	Effective channel length of the device (cm)

m^*	Conductivity effective mass of hole (kg)
m_d^*	Density of state effective mass of hole (kg)
m_{dhh}^*	Density of state effective mass of heavy hole (kg)
m_{dlh}^*	Density of state effective mass of light hole (kg)
m_{hh}^*	Conductivity effective mass of heavy hole (kg)
m_{lh}^*	Conductivity effective mass of light hole (kg)
m_n^*	Effective electron mass (kg)
m_p^*	Effective hole mass (kg)
m_z^*	Quantized effective mass of hole in z direction (kg)
n	Number of bins
N	Number of the particles in a state
N_C	Effective density of states of electrons in the conduction band (cm^{-3})
N_D	Background donor doping concentration (cm^{-3})
n_i	Intrinsic carrier concentration at equilibrium (cm^{-3})
N_{inv}	Inversion layer channel electron density of a nMOSFET (cm^{-2})
N_{OX}	Total number of trapped oxide charges
$N_{0_{OX}}$	Number of trapped oxide charges in equilibrium condition
N_t	Trap density in a nMOSFET per unit area (cm^{-2})
N_T	Volume density of the traps per unit energy in the nMOSFET (cm^{-3}eV^{-1})
$N_T\left(E,x,y,z\right)$	Distributions of the traps in the gate dielectric of the nMOSFET (cm^{-3}eV^{-1})
N_V	Effective density of states of holes in the valence band (cm^{-3})
n_0	Equilibrium electron concentration (cm^{-3})
N_D^+	Ionized donor doping concentration (cm^{-3})
p	Inversion layer hole density per unit volume in a pMOSFET (cm^{-3})
P	Probability of finding the system in a particular state
P_{inv}	Inversion layer hole density in the pMOSFET (cm^{-2})
P_{invhh}	Inversion layer heavy hole density of the pMOSFET (cm^{-2})
P_{invlh}	Inversion layer light hole density of the pMOSFET (cm^{-2})

P_t	Trap density in a pMOSFET (cm^{-2})
$p_v(z)$	Modified valence band hole distribution due to two-dimensional modeling (cm^{-1})
p_{2D}	Hole density for the two-dimensional case (cm^{-2})
p_0	Equilibrium hole concentration (cm^{-3})
q	Electronic charge (C)
Q_D	Total depletion layer charge in MOSFET (Ccm^{-2})
Q_f	Fixed positive oxide charge per unit area (Ccm^{-2})
Q_{inv}	Total inversion layer charges per unit area in the MOSFET (Ccm^{-2})
Q_{OX}	Oxide charges per unit area in the MOSFET (Ccm^{-2})
R	Resistance of the conducting channel (Ω)
$r(E)$	The rate of transition per unit energy at energy E (s^{-1}eV^{-1})
$r_e(N_{OX})$	Recombination rate of the oxide charges(s^{-1})
$r_e(N_{0_{OX}})$	Recombination rate of the oxide charges in the equilibrium condition (s^{-1})
S_{g_e}	Fourier transform of the randomness in the generation rate of the oxide charges (Hz)
S_I	Current noise power spectral density (PSD) (A^2/Hz)
$S_{I_{DS}}$	Power spectral density (PSD) due to the drain-source current noise (A^2/Hz)
S_N	Power spectral density (PSD) of the generation-recombination noise due to carrier number fluctuations (Hz^{-1})
$S_{N_{OX}}$	Power spectral density (PSD) due to the fluctuation in the number of oxide charges (Hz^{-1})
$S_{Q_{OX}}$	Power spectral density due to fluctuation in the amount of oxide charges (C^2/Hz)
S_{r_e}	Fourier transform due to the randomness in the recombination rate of the oxide charges (Hz)
S_V	Voltage noise power spectral density (PSD) of the thermal noise (V^2/Hz)
$S_{V_{DS}}$	Drain-source voltage noise power spectral density (PSD) of the noise (V^2/Hz)
$S_{V_{FB}}$	Voltage noise power spectral density (PSD) due to the flat-band voltage (V^2/Hz)
$S_{\Delta I_{DS}}$	Power spectral density (PSD) due to the drain-source current fluctuations (A^2/Hz)
$S_{\Delta N_t}$	Power spectral density due to the fluctuation in the number of occupied traps in a small WΔy area of a nMOSFET (Hz^{-1})

t	Time (s)
T	Temperature (K)
t_n	Time span of each bin (s)
T_{OX}	Oxide layer thickness (cm)
t_s	Stressing time (s)
U_{empty}	Energy of the defect site when it is empty of a hole (eV)
U_{full}	Energy of the defect site when it is full with a hole (eV)
V_{DS}	Drain-source voltage (V)
V_{FB}	Flat-band voltage (V)
V_{GS}	Gate-source voltage (V)
V_{OX}	Band bending inside the oxide (V)
V_{TH}	Threshold voltage (V)
W	Channel width of the device (cm)
x	Coordinate axis along the channel width (μm)
y	Coordinate axis along the channel length (μm)
z	Coordinate axis along the oxide depth from the Si-SiO_2 interface (nm)
Z_G	The grand partition function
z_T	Trap position into the oxide from the Si-SiO_2 interface (nm)
α	Coulomb screened scattering coefficient (Vs)
α_{gh}	Ghibaudo's screened scattering parameter (Vs/C)
α_H	Hooge's parameter
α_m	Screened scattering coefficient from RTS measurements (Vs)
α_t	Screened scattering coefficient from the theoretical two-dimensional modeling (Vs)
α_{thh}	Screened scattering coefficient from the theoretical two-dimensional modeling for heavy hole (Vs)
α_{tlh}	Screened scattering coefficient from the theoretical two-dimensional modeling for light hole (Vs)
α_0	Fitting parameter of the screened scattering coefficient from the UNMF model (Vs)
α_1	Fitting parameter of the screened scattering coefficient from the UNMF model (negative in magnitude) (Vs)

β	Current exponent in the current noise PSD of the 1/f noise
γ	Frequency exponent in the current noise PSD of the 1/f noise
$\delta\Delta N_{inv}$	Fluctuations in the number of inversion layer electrons in the small area $W\Delta y$ of a nMOSFET
$\delta\Delta N_{t}$	Fluctuations in the number of traps in the small area $W\Delta y$ of a nMOSFET
ΔE_{B}	Capture activation energy (eV)
ΔE_{TV}	Trap energy level with respect to Si valence band edge (eV)
ΔE_{0}	Energy difference between the valence band maximum and the first allowed quantized energy state of hole (eV)
ΔE_{0hh}	Energy difference between the valence band maximum and the first allowed quantized energy state of heavy hole (eV)
ΔE_{0lh}	Energy difference between the valence band maximum and the first allowed quantized energy state of light hole (eV)
ΔG	Gibbs free energy (eV)
$\Delta g_{e}(t)$	Randomness in the generation rate of the oxide charges (s^{-1})
ΔH	Change in enthalpy (eV)
ΔI	Difference between the upper and lower levels of current in a random telegraph signal (RTS) (A)
δI_{DS}	Fluctuations in the drain-source current in a small area (A)
ΔI_{DS}	Drain-source current fluctuations (A)
ΔN	Fluctuation in the number of carriers due to trapping/detrapping event
$\overline{\Delta N^{2}}$	Mean square value of the fluctuation in the number of carriers
ΔN_{inv}	Number of inversion layer electrons in the small WΔy area of a nMOSFET
ΔN_{OX}	Excess number of oxide charges from equilibrium
$\overline{\Delta N_{OX}^{2}}$	Mean square value of the excess number of oxide charges from equilibrium
δN_{t}	Trap density fluctuations in the nMOSFET (cm^{-2})
ΔN_{t}	Number of traps in the small WΔy area of a nMOSFET
ΔP_{inv}	Total number of inversion layer holes in a small area $W\Delta y$
ΔP_{t}	Total number of traps in a small area $W\Delta y$ of a pMOSFET
$\partial\Delta P_{inv}$	Fluctuations in the total number of inversion layer holes in a pMOSFET

$\partial\Delta P_t$	Fluctuations in the total number of traps in a small area $W\Delta y$ in a pMOSFET
δQ_{OX}	Fluctuations in the oxide charge density (Ccm^{-2})
$\Delta r_e(t)$	Randomness in the recombination rate of the oxide charges (s^{-1})
ΔS	Contribution from the change of entropy in Gibbs free energy (eVK^{-1})
$\Delta S/k_B$	Change in entropy
ΔV_{DS}	Drain-source voltage fluctuations (V)
$\lvert\Delta V_{DS}\rvert$	RTS amplitude (V)
δV_{FB}	Fluctuations in the flat-band voltage (V)
δV_{GS}	Fluctuations in the gate-source voltage (V)
Δy	Small channel length (cm)
$\delta\mu$	Effective channel carrier mobility fluctuations (cm^2/Vs)
ε_{av}	Average dielectric constant of Si and SiO_2
ε_0	Permittivity of the free space (F/cm)
ε_{Si}	Dielectric constant of Si
ε_{SiO_2}	Dielectric constant of SiO_2
$\zeta(z)$	Stern-Howard wavefunction ($cm^{-1/2}$)
κ	Plane wave wave-vector (m^{-1})
κ_{hh}	Plane wave wave-vector of heavy hole (m^{-1})
κ_{lh}	Plane wave wave-vector of light hole (m^{-1})
κ'	Final plane wave state wave vector (m^{-1})
λ	Electron wave attenuation coefficient (cm^{-1})
μ	Effective channel carrier mobility in a MOSFET (cm^2/Vs)
μ_{imp}	Mobility due to impurity scattering (cm^2/Vs)
μ_{lat}	Mobility due to lattice scattering (cm^2/Vs)
μ_{oth}	Mobility except oxide charge scattering (cm^2/Vs)
μ_{OX}	Mobility limited by oxide charge scattering(cm^2/Vs)
μ_t	Mobility limited by oxide charge scattering in a two-dimensional mobility fluctuations model (cm^2/Vs)
σ	Trap capture cross-section (cm^2)

σ_0	Capture cross-section pre-factor (cm^2)
$\overline{\tau}$	Time constant of the transition of a signal between two levels (s)
$\overline{\tau}_c$	Average capture time(s)
$\overline{\tau}_e$	Average emission time (s)
$\overline{\tau}_h$	Time constant of the higher level of a current signal RTS (s)
$\overline{\tau}_l$	Time constant of the lower level of a current signal RTS (s)
$\overline{\tau}_0$	Characteristic time constant (s)
$\overline{v}_{th}$	Average thermal velocity of holes (cms^{-1})
ϕ	Half of the angle between initial and final plane wave states
ϕ_B	Height of the tunneling barrier seen by the carriers at the Si-SiO_2 interface (eV)
φ_0	Energy difference between the valence band edges of Si and SiO_2 at the Si-SiO_2 interface (eV)
χ	Degeneracy of a particular state
ψ_s	Surface potential (eV)
ω	Lattice vibration frequency (rad/s)
$\hbar$	Reduced Planck's constant (Js)

Chapter 1: Introduction

1.1 Background and Motivations Behind the Research Work

Downscaling the transistor dimensions over the last few decades following Moore's law has paved the way for rapid development in the CMOS technology. Miniaturization of the transistor size has led to higher operating speed, less amount of dissipated power, and cheaper manufacturing cost. It has inspired advancements in the information and data communication fields. However, since the device dimensions have become smaller, reliability issues have also been a concern from the circuit design perspective. Downsizing of the devices has introduced different types of noise like burst noise, random telegraph signal noise, and flicker noise. The presence of these unwelcoming noise components in the desired signal causes degradation of the device performance. To ensure higher reliability and to maintain proper operation of the device, minimizing the impact of noise is of great concern. Identifying the responsible defect centers for the noise component as well as the detailed examination of the defect properties can help us to ensure reliable operation of the device.

The very first appearance of the discrete switching behavior of the current through the semiconductor came from the detection of the burst noise. Burst noise was prominent in the reverse-biased Ge, Si junctions and tunnel diodes [1], [2]. This type of noise was supposed to originate from the surface effects, tunneling, and the random thermal fluctuation mechanisms [1], [2]. The distribution density functions for the pulse lengths of this noise followed an exponential law [2]. Burst noise was investigated in the forward-biased Si diodes and transistors under the active operating region as well as being incorporated in the equivalent circuits of the diode and transistor [3], [4]. This noise resulted from the current modulation through a defect when there was a charge state change of a generation-recombination site, positioned close to the defect center [4]. The time constants of the burst noise were also computed for the generation-recombination site [4].

However, the very first confirmation of the single carrier switching activities showing random telegraph signal (RTS) came from the work of Kandiah *et al*., by conducting an experiment on electronic devices [5]. They implied that the Shockley-Read-Hall centers present in the Debye region (between the channel and fully depleted region) of the double gate four-terminal Si JFET were responsible for the low-frequency noise. Kandiah *et al*. later demonstrated that the charging/discharging of a single trap in the Debye region generated RTS [6]. On the electron emission from the defect site to the channel, the channel resistance was lowered and drain-source current increased [6]. Later, Ralls *et al.* investigated RTS for a comparatively smaller dimension device (0.1 μm^2) in cryogenic temperatures [7]. They reported the exponential dependence of the time constants on temperature and voltage as well as calculating the corresponding

activation energies of the trap. The change of resistance was found to be consistent with the transfer of the channel carrier into the defect site. They implemented the mark space ratio to determine the trap position. Lattice distortion replaced quantum tunneling as the carrier capture mechanism in their work. Howard *et al*. later obtained a similar kind of result [8] to Ralls *et al.* [7], showing the temperature and bias voltage dependence of the capture and emission time constants for the traps. In addition, Howard *et al.* commented on the charge state of the defect site after an electron capture for the very first time [8]. After the capture of an electron, neutral or positively charged defect site became negatively charged or neutral, respectively, in that work [8]. Welland and Koch traced data related to RTS by utilizing the scanning tunneling microscope (STM) and found that this was consistent with the creation of the localized surface states [9]. The trapping of the carrier in the defect site led to the perturbation of the tunneling current in the vicinity of the site. With the increase of the gate voltage, time spent in the high current level decreased while time spent in the low current level was almost unaffected as reported by Uren *et al*. [10], [11], [12]. While capturing an electron, the negative electrostatic potential from the trapped charge increased the channel resistance, which led to the reduced capture time with biasing [12]. The capture and emission activities are believed to be taking place via a multi-phonon process. Later, in the works by Schulz *et al*., the multi phonon process was replaced by the utilization of the thermionic emission model while discussing the Coulomb repulsive centers [13]. They reported on the first observation of the individual attractive centers in pMOSFETs [14]. Shi *et al*. studied the impact of emission and capture of a trapped carrier on electron mobility [15]. They determined the trap's location along the channel from the difference between the forward and reverse bias mode and held discussions on the effect of electron heating on the capture cross-section of the trap and amplitude of the RTS.

Capture and emission activities by the individual defect sites were studied in detail by Kirton *et al*. [12]. They not only determined the capture and emission times but also the trap position from the interface, along with various RTS parameters, such as capture cross-section pre-factor, capture activation energy, relaxation energy, and change in enthalpy/ entropy. Multi-level switching in the output were observed for the nMOSFETs due to the presence of multiple traps at the same time. A four-level RTS resulting from three separate traps was reported by Amarasinghe *et al*. [16]. Influence from one of the traps over another one was observed to result in an energy level shift. For the trap positioned nearest to the interface, the computed screened scattering coefficient was the most sensitive to the gate voltage change. Later, traps placed deeper into the Si dioxide were studied in a separate work [17]. The effect of the Coulomb blockade was minimal due to the screening of the mobile charge carriers while operating the device in the strong inversion region, contrary to the weak inversion region. The two-dimensional mobility fluctuations model helps to understand the underlying physical mechanisms behind the screened Coulomb scattering between the inversion layer charge carriers and the trapped charge [18]. As the device size down-scaled, the channel

doping concentration was increased to prevent the punch-through effect and premature turn-on of the devices [19]. In high-doping density devices of small-scale dimensions, carrier motion is quantized to the perpendicular direction of the Si-SiO_2 interface [20], [21], [22]. Subsequently, electric sub-bands are present in the respective channel carrier energy bands for n- and pMOSFETs [21], [22]. As a result, two-dimensional quantum mechanical treatments were carried out for the small-scale devices in contrast to the classical three-dimensional treatments. Two-dimensional mobility fluctuations model was successfully implemented to calculate the mobility limited by the oxide charge scattering for nMOSFETs [22]. Screened Coulomb scattering coefficients were calculated from this model for both the interface and oxide traps in nMOSFETs [21], [22].

Recently, RTS has been a major source of concern for device reliability issues, especially for memory devices. The presence of RTS is an obstacle for performing read and write operations correctly in memory devices [23], [24]. In the dynamic random-access memory (DRAM) devices, the presence of multi-valued and metastable leakage currents has been reported to cause a failure in retaining the data for a specific hold time [25], [26]. The observation of the variable retention time ultimately led Yaney and Restle *et al*. to study RTS, which indicated the presence of a single defect in the depletion region. Resistance random access memory (RRAM) is gaining popularity nowadays because of the low cost of fabrication, fast read/write operation, low power consumption, and low threshold voltage [27]. However, in the path of development for RRAM, the presence of RTS in the RRAM current has caused reliability issues and affected memory stability [28]. Furthermore, RTS also provides information about the localized source of defects inside the active material. A significant amount of drain current fluctuation was observed during the read operation for the deeply scaled non-volatile memory devices [29]. Later, phase change memory devices were also studied to understand the impact of RTS [30].

Over the last few decades, the rapid downscaling of the device dimension has caused the reduction of the insulating oxide layer thickness, while the supply voltage has remained constant. As a result, there has been an increase in the vertical electric field in the oxide. Similarly, channel length scaling leads to a higher electric field in the channel. This increased channel electric field is responsible for the hot carrier effects in MOSFETs. During the hot carrier stressing, the carriers in the channel obtain higher kinetic energy to cause damages on the Si-SiO_2 interface and inside the SiO_2. To identify the defect sites responsible for the damages by hot carrier stressing, studying RTS is of significant importance. Most of the publications have dealt with the effect of the hot carrier stressing on nMOSFETs [31], [32], [33]. There are different types of hot carrier stressing mechanisms such as the drain avalanche hot carrier (DAHC), channel hot carrier (CHC), and negative bias temperature instability (NBTI) stress. During DAHC stressing, the drain terminal of the MOSFET is biased at twice the voltage of the gate terminal. Both terminal voltages are above the

rated operating voltage of the device. While implementing NBTI, the PMOSFET is stressed at a high temperature range (80-150 degree C) and high negative voltage in the gate [34]. During CHC stressing, the gate and drain terminal of the MOSFET are biased at equal voltages above the rated operating condition. Due to the hot carrier stressing, degradation in several dc parameters such as drain current, gate current, threshold voltage, subthreshold slope, etc. has been observed [35], [36].

Comparing various stressing mechanisms, CHC stressing causes the worst degradation in pMOSFETs [37], [38], [39]. The smaller impact ionization rate of the carriers, as well as the higher Si-SiO_2 barrier, lead to lower amounts of degradation in pMOSFET than its nMOSFET counterpart [38]. Although being under-reported, to ensure reliable operation of the pMOSFETs, much broader analyses are required to identify the responsible defect centers by examining the RTS parameters under CHC stressing. In the literature, a pioneering publication discussed the effect of DAHC stressing on nMOSFETs by analyzing the RTS data to determine trap position from the Si-SiO_2 interface and position of the trap energy level with respect to the conduction band edge of SiO_2 [40]. Fang *et al*. reported smaller time constants and closer trap position to the Si-SiO_2 interface while comparing the stress-induced traps with the process-induced traps [40]. A similar conclusion was rendered about the position of the trap under DAHC stressing from the works of Kang *et al*.; they also mentioned a lower value for the difference between the energy level of the trap to the edge of the conduction band for the process-induced ones [41]. The effect of DAHC stressing on the RTS amplitude has been scrutinized in the works of Simoen *et al*. for the process-induced traps [42], [43], [44]. Variation of the oxide and interface layer capacitance has been tied to the change of RTS amplitude for the MOSFETs in their notable work. However, additional publications are lacking information to determine whether the RTS amplitude would also be affected in similar ways for the stress-induced ones. Overall, CHC stressing needs to be explored in greater detail alongside the DAHC mechanism.

In most of the cases, not enough importance is given to identify the responsible defect center under the influence of different degradation mechanisms. The RTS parameters such as capture activation energy, relaxation energy, and trap energy level are helpful to gather information about the identification of the defect centers. Detailed investigations have been performed for the nMOSFETs [45], [46] alongside pMOSFETs [47] to identify the responsible defect centers under fresh conditions (no stressing mechanism taken into consideration). E'_δ and E'_γ centers have been reported to be the major candidates for the defects in the pMOSFETs without any type of impact due to stressing [48], [49], [50], [51]. These E'_δ and E'_γ centers were also viewed to be responsible behind flicker (1/f) noise in pMOSFETs [52]. One type of E' center (D-III Si) has also been identified to work as a defect center for the pMOSFETs [53], [54]. Furthermore, there have been some reports about the Hydrogen-related defects acting as a contender in the case of the stress-induced leakage currents (SILC) and NBTI [55], [56]. However, there is still a significant

knowledge gap due to the lack of examination of the CHC effects from the detailed study of the RTS trap parameters. The defect centers responsible behind the process and stress-induced traps need to be identified.

In this research work, RTS measurements were performed to study the effect of the CHC stressing on different RTS parameters at the room temperature for the pMOSFETs. The variable temperature measurements were also carried out to identify responsible defect centers. In the next chapters, we will proceed with these matters in detail. Chapter 2 includes the experimental setup required to take the RTS/ flicker noise measurements at/or below the room temperature. The definitions of different RTS parameters are explained in chapter 3. In chapter 4, discussions are carried out to study the effect of the CHC stressing on the room temperature RTS parameters. Chapter 5 includes elaborate discussions of the CHC effect on the variable temperature RTS parameters (such as activation energies, change in enthalpy/entropy) and the identification of the defect centers are undertaken. Chapter 6 covers a detailed study of the flicker noise data taken on available wafers from nMOSFETs of different technologies.

1.2 Different Types of Electrical Noise

Noise is defined as an unwanted perturbation in the desired signal from a device. It represents the fluctuation of current and voltage in phase and magnitude from their average values. That random fluctuation integrated over a long time period results in no change from the average for stationary noise sources. There are two types of noise sources. External noise sources comprise noise from crosstalk between nearby circuits, interference from AC power lines, and electromagnetic signals. On the other hand, there are different types of internal noise including thermal noise, generation-recombination noise, random telegraph signal noise, and flicker noise. Defects positioned inside the bulk semiconductor oxide or at the oxide-semiconductor interface are responsible for the internal noise in the MOSFETs. Although it is impossible to eliminate the internal noise, its effect can be minimized by identifying and studying the physical properties of the defects as well as making necessary improvements in the fabrication process of the device.

1.2.1 Thermal Noise

Thermal noise originates from the random motion of charge carriers due to the impact of temperature above zero Kelvin. Velocity/mobility of the carriers are affected by the resulting scattering events. Within a little time window, there could be more carriers flowing in a certain direction than in the other directions, resulting in a small amount of current in that direction [57]. However, the average current recorded over a

long time period is zero. Thermal noise is sometimes also referred to as Johnson noise or Nyquist noise as it was discovered by J. B. Johnson in the year 1927 and was later theoretically explained by H. Nyquist [58], [59]. The voltage noise power spectral density (PSD) of the thermal noise is [60],

$$S_V = 4k_B TR \tag{1.1}$$

Here, k_B is Boltzmann's constant, T is temperature in Kelvin, and R is the resistance of the conducting channel.

Thermal noise exists in every resistive circuit to set the lowest limit of the electrical noise without any application of the biasing voltage. Emphasis must be given to eliminate the unnecessary resistance parts to minimize the impact of thermal noise.

1.2.2 Generation-Recombination Noise

Inside the semiconductor, there are different types of transition mechanisms present for the carriers. There are generation and recombination of the electron-hole pairs, and the trapping of carriers in the defect sites. There are electronic states present in the forbidden bandgap of the semiconductor known as traps. These trap centers can either capture or emit the carriers, which results in a fluctuation of the number of carriers known as generation-recombination noise. The PSD of the generation-recombination (g-r) noise due to carrier number fluctuation is [61],

$$S_N(f) = 4\overline{\Delta N^2} \frac{\overline{\tau}}{1+(2\pi f)^2 \overline{\tau}^2} \tag{1.2}$$

Here, ΔN is the fluctuation in the number of carriers due to trapping/ detrapping, $\overline{\tau}$ is the time constant of the transitions, and f is the frequency.

1.2.3 Random Telegraph Signal (RTS) Noise

RTS noise is a special case of g-r noise that occurs when the number of involved traps is small. Discrete switching of the current or voltage due to random capture and emission of the carriers from the channel to the defect site results in RTS. RTS is generally observed in small area devices (< 1 μm^2). However, the presence of the parasitic current at the periphery of the gate can also result in RTS in larger area devices [57]. Two-level RTS comes from the trapping/detrapping of the carriers in a single defect site. A sample two-level RTS signal is shown in Fig. 1.1.

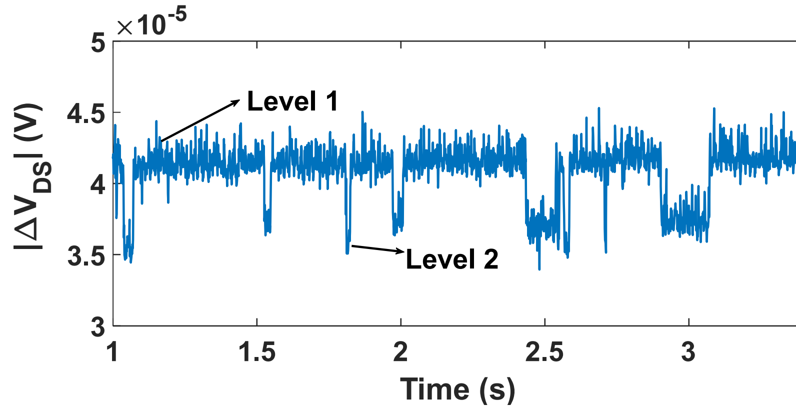


Fig. 1. 1 Two level RTS signal. The transition between level 1 and 2 indicates the presence of a single trap.

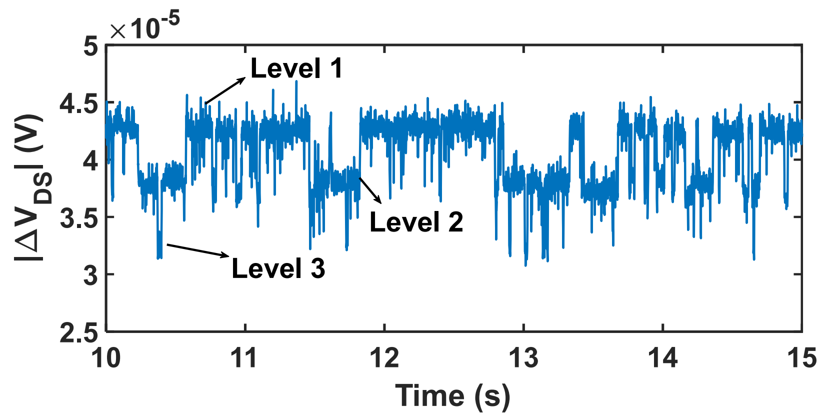


Fig. 1. 2 Three level RTS signal. The transition from level 1 to 2 indicates the presence of one trap. The transition from level 2 to 3 indicates the presence of another trap at the same time span of the recorded data.

Multi-level RTS can also be observed due to the presence of multiple traps. The three-level RTS signal is shown in Fig. 1.2. The transition from level 1 to 2 occurs due to the capture and emission of the carriers in one of the defect sites. On the other hand, the transition from level 2 to 3 occurs due to the presence of an additional trap site.

Envelope transition is a multilevel RTS signal due to the presence of two separate (fast and slow) traps. There are two types of envelope transitions. In the first type of envelope transition, switching between levels (1-3 and 2-4) are due to the presence of the same trap (Fig. 1.3) [62]. As a result, either the amplitude difference between level 1 and level 3 or level 2 and level 4 denotes the RTS amplitude of the first trap. Switching activities between level 1 and 3 are denoted as the 'lower envelope' whereas, the transitions between level 2 and 4 are denoted as the 'upper envelope'. The presence of the second trap causes modulation between the upper and lower envelopes. The average of the maxima of level 1 and 3 is

determined. Similarly, the average of the maxima of level 2 and 4 is determined. The RTS amplitude of the second trap is computed by subtracting these averages.

In the second type of envelope transition, switching between the consecutive levels (1-2 and 3-4) are due to the presence of the same trap (Fig. 1.4) [62]. As a result, either the amplitude difference between level 1 and 2 or level 3 and 4 denotes the RTS amplitude of the first trap. The RTS amplitude of the second trap is computed by subtracting the averages of the maxima between level 1 and 2, and level 3 and 4.

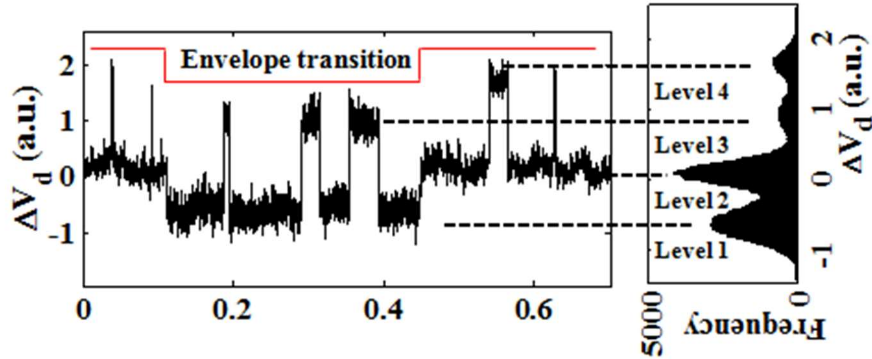


Fig. 1. 3 The presence of envelope transition in a multi-level RTS signal [62].

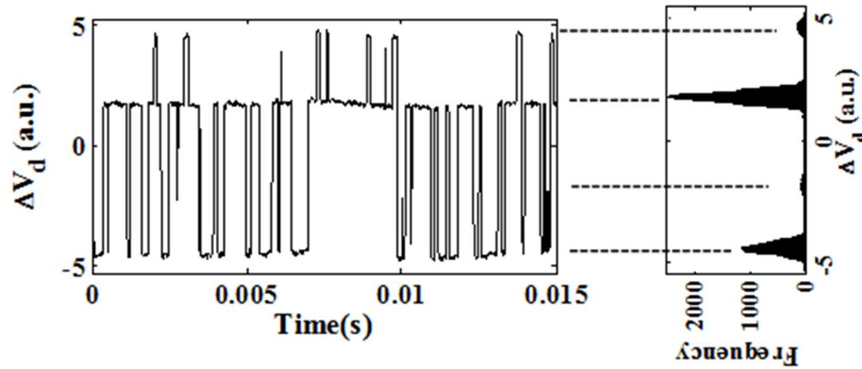


Fig. 1. 4 The presence of envelope transition in a multi-level RTS signal [62].

The current noise power spectral density of RTS is [63],

$$S_I(f) = \frac{4(\Delta I)^2}{(\overline{\tau}_l + \overline{\tau}_h)\left[(1/\overline{\tau}_l + 1/\overline{\tau}_h)^2 + (2\pi f)^2\right]} \tag{1.3}$$

Here, ΔI is the amount of fluctuation in a two level RTS signal, whereas $\overline{\tau}_l$ and $\overline{\tau}_h$ are the average time constants of the lower and upper level, respectively. The PSD of the RTS signal is in Lorentzian form (Fig. 1.5).

1.2.4 Flicker Noise

Flicker (1/f) noise originates from the fluctuation in the number and mobility of the carriers when the entire process involves a large number of traps. 1/f noise PSD is observed in the low-frequency part of the spectrum. When there are isolated traps with different time constants, their individual Lorentzian PSD's can add up to result in the 1/f noise spectrum. The current noise PSD of the 1/f noise is:

$$S_I = \frac{K_{1/f} I^{\beta}}{f^{\gamma}} \tag{1.4}$$

Here, $K_{1/f}$ is constant, β is a current exponent which equals 2 , and γ is known as frequency exponent in the range of 0.7-1.4. A sample voltage noise PSD of 1/f noise is shown in Fig. 1.6.

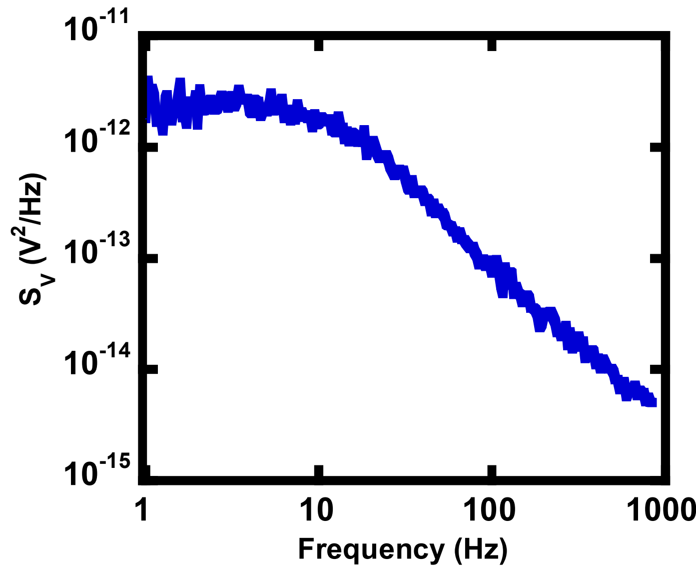


Fig. 1. 5 The voltage noise PSD of a two-level RTS signal.

While studying the 1/f noise mechanism in MOSFETs, there have been debates about whether the fluctuation in the number of carriers in the channel or the change of the carrier mobility can produce a better explanation behind the experimentally obtained 1/f noise data. In the early days, there was the number fluctuations model proposed by McWhorter [64]. This model was quite successful in explaining the experimentally obtained 1/f noise PSD data for the nMOSFETs [65], [66]. However, the lack of correlation between the data and theoretical modeling in the case of pMOSFETs paved the way for the adaptation of the Hooge's mobility fluctuations model [67]. Although this mobility fluctuations model was successfully applied in numerous cases [68], [69], [70], it was subjected to severe criticism. There was a lack of physical reasoning in choosing the value of one of the controlling parameters in this mobility fluctuations model. As

a result, researchers like Ghibaudo tried to include both the number and mobility fluctuations simultaneously while working to develop a universal model for both n- and pMOSFETs [71]. C. Hu *et al*. successfully developed the unified number mobility fluctuations theory considering the impact of both the

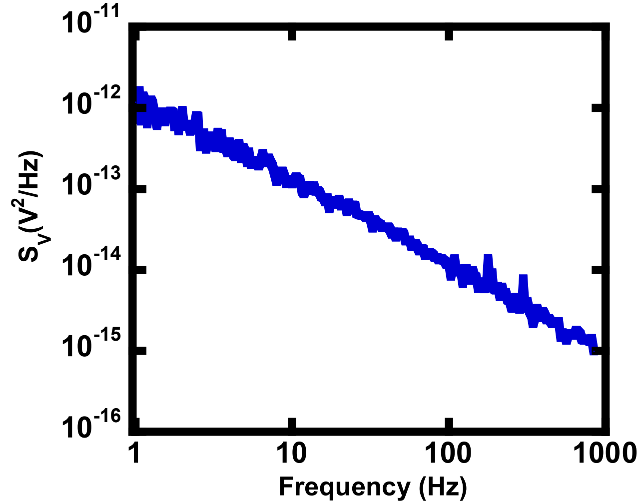


Fig. 1. 6 The voltage noise PSD of a flicker (1/f) noise. The slope in this case is very close to 1, which is agreeing to be within the range of 0.7-1.4.

number and mobility of the channel carriers [72]. That model has been successfully implemented later in many research works regarding both n- and pMOSFETs [45], [47], [73]. In the next section, the development of these models will be discussed.

1.2.4.1 Number Fluctuations Model

Number fluctuations model was proposed by A. McWhorter in 1957. It has provided an explanation for the experimental 1/f noise data by considering the fluctuation in the number of carriers in the channel. The carriers from the channel communicate with the gate oxide trap sites through the quantum tunneling mechanism. Based on the quantum mechanical tunneling concept, the carrier from the channel takes a longer time to be trapped in a defect site further away from the Si-SiO_2 interface, whereas on the contrary, it takes comparatively a small amount of time for the carrier to be trapped on or very near to the interface. Density of the trap is considered to be uniform in both energy and distance from the interface in order to produce the distribution in time constants of the 1/f noise.

The change in the number of oxide traps, resulting from the fluctuation in the number of carriers with time is [74],

$$\frac{dN_{OX}}{dt} = g_e(N_{OX}) - r_e(N_{OX}) + \Delta g_e(t) - \Delta r_e(t) \tag{1.5}$$

Here, N_{OX} is the number of trapped oxide charges, $g_e(N_{OX})$ is the generation rate of the traps, $r_e(N_{OX})$ is the recombination rate of the traps, $\Delta g_e(t)$ is the fluctuation in the generation rate, and $\Delta r_e(t)$ is the fluctuation in the recombination rate.

The number of trapped oxide charges is represented as, $N_{OX} = N_{0_{OX}} + \Delta N_{OX}$, where $N_{0_{OX}}$ is the equilibrium number of trapped oxide charges and ΔN_{OX} is the excess number of oxide charges from the equilibrium. Neglecting the higher order terms in ΔN_{OX} produces the equilibrium condition $g_e(N_{0_{OX}}) = r_e(N_{0_{OX}})$. Here, $g_e(N_{0_{OX}})$ and $r_e(N_{0_{OX}})$ are the generation and recombination rate of the oxide charges under the equilibrium condition, respectively. Then using the Langevin equation [74],

$$\frac{d\Delta N_{OX}}{dt} = \frac{\Delta N_{OX}}{\overline{\tau}} + \Delta g_e(t) - \Delta r_e(t) \tag{1.6}$$

Here, $\frac{1}{\overline{\tau}} = \left(\frac{dr_e}{dN_{OX}} - \frac{dg_e}{dN_{OX}}\right)\Big|_{N_{0_{OX}}}$; $\overline{\tau}$ is the time constant.

Performing the Fourier transform of Eqn. 1.6 gives,

$$S_{N_{OX}}(f) = \frac{\overline{\tau}^2}{1+(2\pi f)^2\,\overline{\tau}^2}\left[S_{g_e}(f) + S_{r_e}(f)\right] \tag{1.7}$$

The generation and recombination processes are random and independent of each other [75]. Shot noise is generated when the carriers cross a potential barrier independently and randomly [57]. As a result, both $\Delta g_e(t)$ and $\Delta r_e(t)$ show shot noise [74], [76]. Their shot noise PSD are represented as [74],

$$S_{g_e}(f) = S_{r_e}(f) = 2g_e(N_{0_{OX}}) = 2r_e(N_{0_{OX}}) \tag{1.8}$$

Now using Eqn.1.8 in Eqn. 1.7,

$$S_{N_{OX}}(f) = 4g_e(N_{0_{OX}})\frac{\overline{\tau}^2}{1+(2\pi f)^2\,\overline{\tau}^2} \tag{1.9}$$

The mean square value of ΔN_{OX} can be determined as [74],

$$\overline{\Delta N_{OX}^2} = \int_0^\infty S_{N_{OX}}(f)df = 4g_e\left(N_{0_{OX}}\right)\int_0^\infty \frac{1}{\left(1/\overline{\tau^2}\right)+\left(2\pi f\right)^2}df = g_e\left(N_{0_{OX}}\right)\overline{\tau} \tag{1.10}$$

Using Eqn. 1.10, Eqn. 1.9 can be rewritten as [57],

$$S_{N_{OX}}(f) = 4\overline{\Delta N_{OX}^2}\frac{\overline{\tau}}{1+\left(2\pi f\right)^2\overline{\tau^2}} \tag{1.11}$$

The oxide charge per unit area is, $Q_{OX} = \left(qN_{OX}/WL\right)$. Here, q is the elementary charge, W is the channel width, and L is the channel length of the MOSFET.

Then the PSD due to the change in the amount of oxide charges can be written as,

$$S_{Q_{OX}}(f) = \frac{4q^2\overline{\Delta N_{OX}^2}}{W^2L^2}\frac{\overline{\tau}}{1+\left(2\pi f\right)^2\overline{\tau^2}} \tag{1.12}$$

As the trap site is occupied with a carrier, the mean square value of ΔN_{OX} is calculated for the trap at energy E. The Fermi-Dirac distribution function $f_T(E)$ is utilized as [57],

$$\overline{\Delta N_{OX}^2} = f_T(E)\left[1-f_T(E)\right] \tag{1.13}$$

Substituting Eqn. 1.13 into Eqn. 1.12 and then assuming a density of traps $N_T(E,x,y,z)$, the total PSD due to change in the amount of the trapped oxide charges is [57],

$$S_{Q_{OX}} = \int_{E_V}^{E_C}\int_0^{T_{OX}}\int_0^L\int_0^W \frac{4q^2}{W^2L^2}f_T(E)\left[1-f_T(E)\right]N_T(E,x,y,z)\frac{\overline{\tau}}{1+\omega^2\overline{\tau^2}}dxdydzdE \tag{1.14}$$

where, E_C is the conduction band edge in Si, E_V is the valence band edge in Si, and T_{OX} is the SiO_2 layer thickness.

Since uniform trap density has been assumed, $N_T(E,x,y,z) = N_T$. Using $f_T(E)\left[1-f_T(E)\right] = -k_BT\, df_T(E)/dE$ [57], Eqn. 1.14 becomes,

$$S_{Q_{OX}} = \frac{4q^2}{WL}\int_{E_V}^{E_C}\int_0^{T_{OX}} N_T\left(-k_BT\right)\frac{df_T(E)}{dE}\frac{\overline{\tau}}{1+\left(2\pi f\right)^2\overline{\tau^2}}dxdE = \frac{4k_BTq^2N_T}{WL}\int_0^{T_{OX}}\frac{\overline{\tau}}{1+\left(2\pi f\right)^2\overline{\tau^2}}dx \tag{1.15}$$

McWhorter has assumed the transfer of the carrier between the channel and the oxide defect site as a quantum mechanical tunneling process. The tunneling time constant can be represented as function of the distance x into the oxide as [57],

$$\overline{\tau} = \overline{\tau_0} e^{\lambda x} \tag{1.16}$$

Here, $\overline{\tau}_0$ is the characteristic time constant and λ is electron wave attenuation coefficient. λ is determined by using the Wentzel-Kramers-Brilloin (WKB) theory as [77],

$$\lambda = \left[\frac{4\pi}{h} \sqrt{2m^* \phi_B} \right] \tag{1.17}$$

where, m^* is the effective mass of the carrier, h is Planck's constant, and ϕ_B is the height of the tunneling barrier, seen by the carriers at the Si-SiO_2 interface.

Now using Eqn. 1.16 into Eqn. 1.15; and then performing the integration,

$$S_{Q_{OX}} = \frac{k_B T q^2 N_T}{WL\lambda f} \tag{1.18}$$

The PSD of the oxide charge is also represented alternatively as (replacing f with f^γ) [57],

$$S_{Q_{OX}} = \frac{k_B T q^2 N_T}{WL\lambda f^\gamma} \tag{1.19}$$

The frequency component γ is equal to 1 for uniform trap density (as shown in Eqn. 1.18). If the trap density N_T is higher in magnitude and closer to the Si-SiO_2 interface than further away, then $\gamma < 1$. Similarly, for the opposite case of distribution for N_T makes $\gamma > 1$.

MOSFET channel transconductance is, $g_m = \frac{\delta I_{DS}}{\delta V_{GS}} = -\frac{\delta I_{DS}}{\delta V_{FB}}$, where, δI_{DS} is the drain-source current fluctuation, δV_{GS} is the gate-source voltage fluctuation, and δV_{FB} is the fluctuation in flat-band voltage of the MOSFET. We can write down the PSD relation among these parameters as, $S_{I_{DS}} = g_m^2 S_{V_{FB}}$. It is known that, in the linear region of operation, the relation between the oxide charge density Q_{OX} and the oxide capacitance C_{OX} is, $Q_{OX} = C_{OX} V_{GS}$. Then, $\delta Q_{OX} = C_{OX} \delta V_{GS} = -C_{OX} \delta V_{FB}$; here, δQ_{OX} is the oxide charge fluctuation in the MOSFET. Then the PSD due to the change of the oxide charge is expressed as,

$$S_{Q_{OX}} = C_{OX}^2 S_{V_{FB}} \tag{1.20}$$

where, $S_{V_{FB}}$ is the PSD due to the fluctuation of flat-band voltage in the MOSFET. Using Eqn. 1.20 in the previously derived relation $S_{I_{DS}} = g_m^2 S_{V_{FB}}$, we obtain,

$$S_{I_{DS}} = g_m^2 \frac{S_{Q_{OX}}}{C_{OX}^2} \tag{1.21}$$

Then using Eqn. 1.18 in Eqn. 1.21 [71],

$$S_{I_{DS}} = \frac{k_B T q^2 N_T}{\lambda f W L} \frac{g_m^2}{C_{OX}^2} \tag{1.22}$$

1.2.4.2 Mobility Fluctuations Model

Hooge's empirical formula asserts that the drain current noise PSD is generated by the fluctuation of the mobility of the channel carriers. Hooge's theory is expressed as [57],

$$\frac{S_{I_{DS}}}{I_{DS}^2} = \frac{q\alpha_H}{fWLQ_{inv}} \tag{1.23}$$

where, α_H is the Hooge's parameter, I_{DS} is the drain-source current, and Q_{inv} is the inversion layer charge per unit area in the MOSFET. Hooge's parameter is evaluated as [57],

$$\alpha_H = \sum_j \left(\mu/\mu_j\right)^2 \alpha_j \tag{1.24}$$

Here, μ is the effective mobility of the channel carriers, μ_j is the mobility limited by either lattice or impurity scattering, and α_j is the screening parameter of lattice or impurity scattering.

Although Hooge's parameter is supposed to be a constant in the theory, its range of value is affected by the thickness of the insulating oxide layer [78] as well as the bias voltage dependence of different scattering mechanisms. Typically, the range of α_H is between 10^{-3} and 10^{-6} [57]. For buried channel Si pMOSFETs, values of 10^{-7} is observed for α_H [79], whereas for JFETs the value of α_H is of the order of 10^{-8} [80], [81]. Effective channel mobility depends on mobility limited by lattice scattering and impurity scattering. Mobility limited by oxide charge scattering or surface roughness scattering is not taken into consideration. According to Matthiessen's rule,

$$\frac{1}{\mu} = \frac{1}{\mu_{lat}} + \frac{1}{\mu_{imp}} \tag{1.25}$$

where, μ_{lat} and μ_{imp} are the mobility limited by lattice scattering and impurity scattering, respectively.

1.2.4.3 Correlated Mobility Fluctuations Model

In addition, with the carrier number fluctuations, a more detailed approach was considered by Ghibaudo to include the fluctuations of the scattering rate leading to the effective mobility fluctuations [71]. As a result, the drain current fluctuation is expressed as [71],

$$\delta I_{DS} = \frac{\delta I_{DS}}{\delta V_{FB}} \delta V_{FB} \Big|_{\mu = constant} \pm \frac{\delta \mu}{\delta Q_{OX}} \delta Q_{OX} \Big|_{V_{FB} = constant} \tag{1.26}$$

Here, $\delta\mu$ is the fluctuation in the effective mobility of the channel carriers. Using the definition of the channel transconductance,

$$\frac{\delta I_{DS}}{\delta V_{FB}} = -\frac{\delta I_{DS}}{\delta V_{GS}} = -g_m \tag{1.27}$$

In the linear region of operation for the MOSFET,

$$\frac{\delta I_{DS}}{\delta \mu} = \frac{I_{DS}}{\mu} \tag{1.28}$$

Now, using Eqn. 1.27 and Eqn. 1.28 in Eqn. 1.26,

$$\delta I_{DS} = -g_m \delta V_{FB} \pm \frac{I_{DS}}{\mu} \frac{\delta \mu}{\delta Q_{OX}} \delta Q_{OX} \tag{1.29}$$

From Matthiessen's rule,

$$\frac{1}{\mu} = \alpha_{gh} Q_{OX} + \frac{1}{\mu_{oth}} \tag{1.30}$$

Here, μ_{oth} is the mobility limited by lattice scattering, impurity scattering and surface roughness scattering, and α_{gh} is the screened scattering parameter used by Ghibaudo and its unit is (Vs/C) [71].

By differentiating both sides of Eqn. 1.30 with respect to Q_{OX} ,

$$\frac{\delta}{\delta Q_{OX}}\left(\frac{1}{\mu}\right)=\alpha_{gh} \Rightarrow -\frac{1}{\mu^2}\frac{\delta\mu}{\delta Q_{OX}}=\alpha_{gh} \tag{1.31}$$

Substituting Eqn. 1.31 into Eqn. 1.29,

$$\delta I_{DS}=-g_m\delta V_{FB} \mp I_{DS}\alpha_{gh}\mu\delta Q_{OX}=-g_m\delta V_{FB} \pm I_{DS}\alpha_{gh}\mu C_{OX}\delta V_{FB} \tag{1.32}$$

The PSD of the drain-source current noise is expressed as,

$$S_{I_{DS}}=S_{V_{FB}}\left(-g_m \pm I_{DS}\alpha_{gh}\mu C_{OX}\right)^2 \tag{1.33}$$

1.2.4.4 Unified Number and Mobility Fluctuations Model

Unified number and mobility fluctuations (UNMF) model incorporates not only the number fluctuations but also the correlated surface mobility fluctuations mechanism. Coulomb scattering effect of the channel carriers, being trapped inside the defect sites is considered while computing the correlated mobility fluctuations. In the linear region of operation in a nMOSFET, the drain-source current is given as [72],

$$I_{DS}=W\mu qN_{inv}E_y \tag{1.34}$$

where, N_{inv} is the inversion layer electron density in the channel per unit area of the nMOSFET and E_y is the applied electric field along the channel.

Correlated fluctuation in the carrier number and surface mobility has been induced by fluctuation in the occupancy of the oxide trap. The fractional change of drain current in the small area of the channel of width W and length Δy is expressed as [72],

$$\frac{\delta I_{DS}}{I_{DS}}=-\left(\frac{1}{\Delta N_{inv}}\delta\Delta N_{inv} \pm \frac{\delta\mu}{\mu}\right) \tag{1.35}$$

where, ΔN_{inv} is the number of inversion layer electrons in the small area $W\Delta y$ of the nMOSFET and $\delta\Delta N_{inv}$ is the fluctuation in ΔN_{inv}.

The addition or subtraction sign between the terms in right hand side of Eqn. 1.35 depends on whether the trap is an attractive or a repulsive center. For the nMOSFETs, in case of the trap being an attractive center, the positively charged defect center becomes neutral after capturing an electron. Channel resistance from the number and mobility fluctuations acts in a reverse way and the sign becomes negative between

these counterparts. On the contrary, if the trap is a repulsive center, neutral defect center becomes negatively charged after capturing an electron. A positive sign is incorporated in that case in Eqn. 1.35.

The number of inversion layer electrons in the small area of $W\Delta y$ is, $\Delta N_{inv} = W\Delta y N_{inv}$ and the total number of occupied traps in that area is, $\Delta N_t = W\Delta y N_t$; here, N_t is the trap density per unit area.

During capture, the inversion layer electron from the channel gets trapped inside the defect site of SiO_2. As the decrease of one inversion layer electron means that one trap is now occupied with that electron; we can write, $\delta\Delta N_{inv} / \delta\Delta N_t = 1$. Taking all these things into consideration, Eqn. 1.35 becomes,

$$\frac{\delta I_{DS}}{I_{DS}} = -\left(\frac{1}{\Delta N_{inv}} \frac{\delta\Delta N_{inv}}{\delta\Delta N_t} \pm \frac{1}{\mu} \frac{\delta\mu}{\delta\Delta N_t} \right) \delta\Delta N_t = -\left(\frac{1}{N_{inv} W\Delta y} \pm \frac{1}{\mu} \frac{1}{W\Delta y} \frac{\delta\mu}{\delta N_t} \right) \delta\Delta N_t \tag{1.36}$$

Here, $\delta\Delta N_t$ is the fluctuation of the number of traps in the small area $W\Delta y$.

Following Matthiessen's rule, the effective channel mobility is expressed as,

$$\frac{1}{\mu} = \frac{1}{\mu_{OX}} + \frac{1}{\mu_{oth}} = \alpha N_t + \frac{1}{\mu_{oth}} \tag{1.37}$$

Here, α is the screened scattering coefficient, μ_{OX} is the mobility component limited by the oxide charge scattering, and μ_{oth} is the mobility component limited by other scattering mechanisms, namely lattice scattering, impurity scattering and surface roughness scattering. μ_{OX} has been replaced with $1/\alpha N_t$. Making further simplifications, Eqn. 1.37 becomes,

$$\mu = \frac{\mu_{oth}}{1 + \alpha N_t \mu_{oth}} \tag{1.38}$$

Differentiating both sides of Eqn. 1.38 with respect to N_t leads to,

$$\frac{\delta\mu}{\delta N_t} = \frac{-\mu_{oth}\alpha\mu_{oth}}{\left(1 + \alpha N_t \mu_{oth}\right)^2} = \frac{-\alpha\mu_{oth}^2}{\left(1 + \alpha N_t \mu_{oth}\right)^2} = -\alpha\mu^2 \tag{1.39}$$

Replacing Eqn. 1.36 with Eqn. 1.39,

$$\frac{\delta I_{DS}}{I_{DS}} = -\left(\frac{1}{N_{inv}} \pm \alpha\mu \right) \frac{\delta\Delta N_t}{W\Delta y} \tag{1.40}$$

Further simplification of Eqn. 1.40 leads to,

$$\frac{\delta I_{DS}}{I_{DS}} = -\left(\frac{1 \pm \alpha\mu N_{inv}}{N_{inv}}\right)\frac{\delta \Delta N_t}{W\Delta y} = -\left(\frac{1 \pm \alpha\mu N_{inv}}{\Delta N_{inv}}\right)\delta \Delta N_t \tag{1.41}$$

The corresponding PSD of the fractional drain current is,

$$S_{\Delta I_{DS}} = \left[\frac{I_{DS}}{\Delta N_{inv}}\left(1 \pm \alpha\mu N_{inv}\right)\right]^2 S_{\Delta N_t} \tag{1.42}$$

where, $S_{\Delta N_t}$ is the PSD due to the fluctuation in the number of the occupied traps in the $W\Delta y$ area of the nMOSFET. Now from the previously derived number fluctuations theory, PSD of the number fluctuation in trap density is,

$$S_{\Delta N_t}\left(f\right) = 4\overline{\Delta N_t^2}\frac{\bar{\tau}}{1+\left(2\pi f\right)^2\overline{\tau^2}} \tag{1.43}$$

where, $\overline{\Delta N_t^2} = f_T\left(E\right)\left[1 - f_T\left(E\right)\right]$; is the mean square value for the fluctuation in the number of traps. For a carrier to get trapped inside the defect site from the channel, both the carrier and the trap must be in the same trap energy level. In addition, when the carrier is going to be trapped inside the defect site, the site must have to be empty of any carrier before that. Now, to calculate the total PSD of the trap density (as shown in the derivation of the number fluctuation model) from Eqn. 1.43,

$$S_{\Delta N_t} = 4\int_{E_V}^{E_C}\int_0^{T_{OX}}\int_0^{\Delta y}\int_0^{W}\overline{\Delta N_t^2}\frac{\bar{\tau}}{1+\left(2\pi f\right)^2\overline{\tau^2}}N_T\left(E,x,y,z\right)dxdydzdE \tag{1.44}$$

$$S_{\Delta N_t} = 4\int_{E_V}^{E_C}\int_0^{T_{OX}}\int_0^{\Delta y}\int_0^{W} f_T\left(E\right)\left[1 - f_T\left(E\right)\right]N_T\left(E,x,y,z\right)\frac{\bar{\tau}}{1+\left(2\pi f\right)^2\overline{\tau^2}}dxdydzdE \tag{1.45}$$

As the trap density is considered to be uniform over the gate area and the product $f_T\left(E\right)\left(1 - f_T\left(E\right)\right)$ is sharply peaked around the quasi Fermi level; then in the similar way (as done before in the number fluctuations model section), $S_{\Delta N_t}$ is,

$$S_{\Delta N_t} = \frac{k_B T W \Delta y N_T}{f\lambda} \tag{1.46}$$

Then the PSD of the drain-source current can be calculated as [82],

$$S_{I_{DS}} = \frac{1}{L^2}\int_0^L S_{\Delta I_{DS}} \Delta y dy \tag{1.47}$$

Applying Eqn. 1.46 into Eqn. 1.42,

$$S_{\Delta I_{DS}} = \left[\frac{I_{DS}}{\Delta N_{inv}}\left(1 \pm \alpha\mu N_{inv}\right)\right]^2 \frac{k_B T W \Delta y N_T}{f\lambda} = \left[I_{DS}\left(\frac{1}{N_{inv}} \pm \alpha\mu\right)\right]^2 \frac{k_B T N_T}{\left(W\Delta y\right) f\lambda} \tag{1.48}$$

Then replacing in Eqn. 1.48 into Eqn. 1.47,

$$S_{I_{DS}} = \frac{1}{L^2}\int_0^L \left[I_{DS}\left(\frac{1}{N_{inv}} \pm \alpha\mu\right)\right]^2 \frac{k_B T N_T}{W f\lambda} dy \tag{1.49}$$

Performing the integration in the right-hand side of Eqn. 1.49 leads to,

$$S_{I_{DS}} = \frac{k_B T I_{DS}^2 N_T}{W L f\lambda}\left(\frac{1}{N_{inv}} \pm \alpha\mu\right)^2 \tag{1.50}$$

In this chapter, literature review is carried out to summarize the research works in the field of device noise and reliability. Different types of noise are studied, and the development of 1/f noise models are discussed. In the subsequent chapters, the experimental setup to obtain RTS data will be shown and careful analysis of the acquired RTS data will be carried out.

Chapter 2: Noise Measurement Procedures and Setup

Recorded random telegraph signal (RTS) data are utilized to identify the defect centers and gather information about their properties. However, reliable identification of the defect center is possible only if the observed RTS data points from the oscilloscope are accurate. In this case, the entire noise measurement process is needed to be set up to eliminate any possibility of interference from the undesired internal/external noise sources. The functionality of the device is also required to be checked in different phases of the measurement to ensure that the device is still functioning properly. As these small-size MOSFETs are very sensitive to electrostatic discharge (ESD), precautions are necessary to prevent its harmful effect. Details about the noise measurement procedure are discussed in this chapter. The experimental setup utilized for the noise measurements is also shown.

There are three major steps in the noise measurement experiments, applicable for both RTS and flicker noise. These are (1) extraction of the DC parameters, (2) examination of the C-V characteristics, and (3) acquisition of the RTS/ flicker noise data. A detailed discussion is provided in the next section.

2.1 DC Measurements

The Agilent 4156A Semiconductor Parameter Analyzer (SPA) was used to verify the functionality of the MOSFET by extracting DC parameters such as drain-source current I_{DS}, channel output conductance g_d, and trans-conductance g_m. Current-voltage characteristic plots (I_{DS}, g_m vs. gate-source voltage V_{GS} and I_{DS} vs. drain-source voltage V_{DS}), attained from the SPA are presented in Figs. 2.1 and 2.2.

One of the important device parameters, threshold voltage V_{TH}, was determined from $\sqrt{I_{DS}}$ and $d\sqrt{I_{DS}}/dV_{GS}$. A tangent was drawn on the plot of $\sqrt{I_{DS}}$ at the point where $d\sqrt{I_{DS}}/dV_{GS}$ is minimum. The intercept of the tangent with V_{GS} is denoted as V_{TH} for the device in Fig. 2.3.

Similarly, g_d, another important parameter which was directly obtained from the SPA, while recording the I_{DS} vs. V_{DS} plot, was later utilized to calculate the effective channel carrier mobility μ of the MOSFET.

2.2 C-V Measurements

C-V measurements were carried out by using an Agilent 4294A Impedance Analyzer. The main goal was to determine the inversion layer charge densities present at different V_{GS} values and compute the SiO_2 layer thickness. The calculated inversion layer charge densities also helped to find out the effective channel carrier mobility μ for the device at different V_{GS} values. C-V measurement setup is shown in Fig. 2.4. The high terminal of the impedance analyzer was connected to the gate; the low terminal was connected to both the drain and source; and the guard terminal was connected to the substrate of the MOSFET.

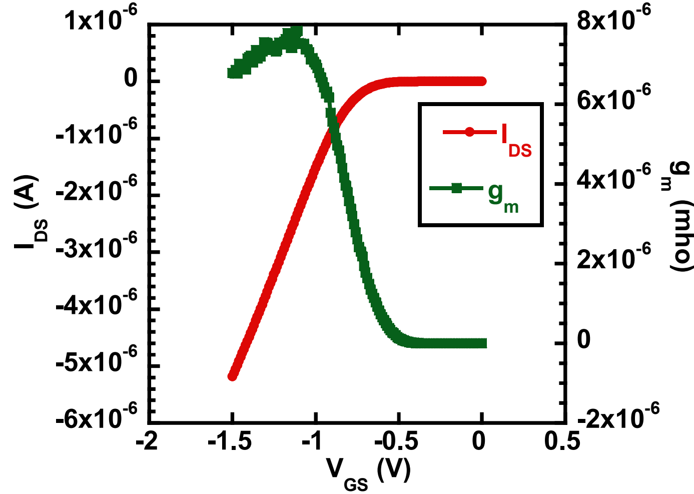


Fig. 2. 1 Drain source current I_{DS} and channel transconductance g_m as a function of gate-source voltage V_{GS} for a pMOSFET.

During the measurement steps, the gate-channel capacitance C_{GC} was recorded as a function of V_{GS} (Fig. 2.5). From the raw C_{GC} data for a range of V_{GS}, gate-channel capacitance in the inversion region $C_{GC_{inv}}$ and gate-channel overlap capacitance in the accumulation region $C_{GC_{OV}}$ were determined. C_{GC} was corrected as $\left(C_{GC_{cor}}\right)$ by subtracting the overlap capacitance of the accumulation region $C_{GC_{OV}}$ from the raw C_{GC} data. The total inversion layer charge Q_{inv} was calculated from the area under the $\left(C_{GC_{cor}} - V_{GS}\right)$ plot. Then the inversion layer hole concentration was determined as [83],

$$P_{inv} = \frac{Q_{inv}\left(V_{GS}\right)}{q} = \frac{\int_{0}^{V_{GS}} C_{GC_{cor}}\left(V_{GS}\right) dV}{q} \tag{2.1}$$

Here, q is the electronic charge. The effective channel length was calculated as [83],

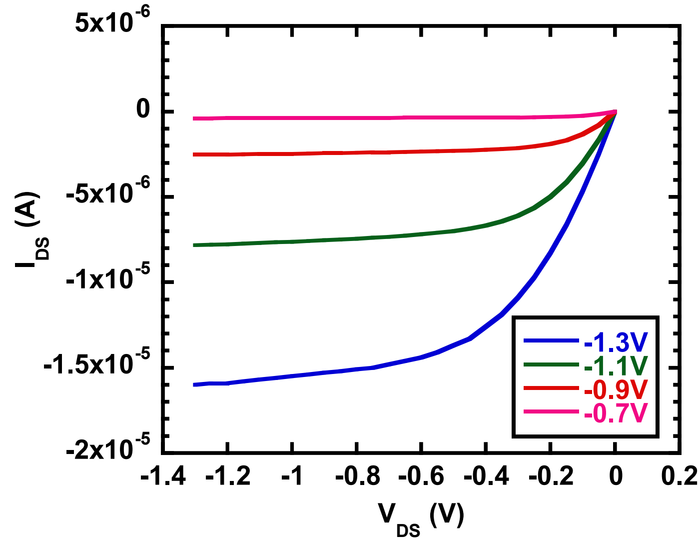


Fig. 2. 2 Drain source current I_{DS} as a function of drain-source voltage V_{DS} for different V_{GS} values of a pMOSFET.

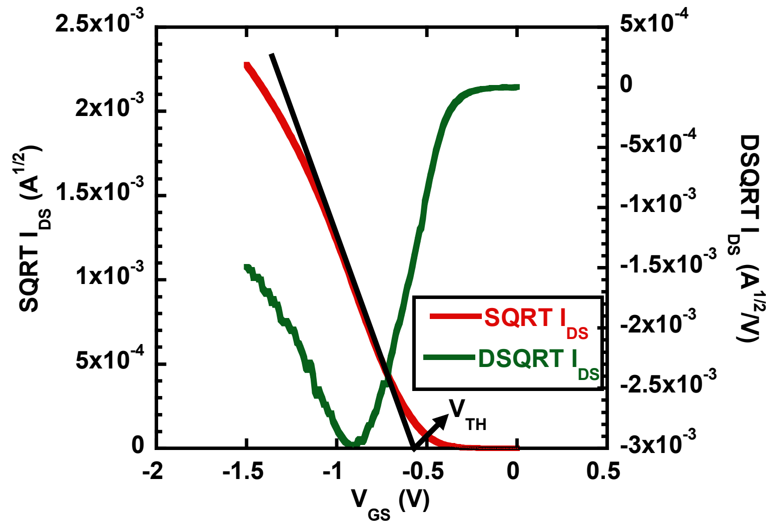


Fig. 2. 3 Extraction of threshold voltage V_{TH} in a pMOSFET. The intersect of the drawn black line on V_{GS} denotes V_{TH}.

$$L_{eff} = L\left(1 - \frac{C_{GC_{OV}}}{C_{GC_{inv}}}\right) \tag{2.2}$$

Here, L is the channel length of the pMOSFET.

C-V data were later utilized to calculate the oxide thickness of the pMOSFET as,

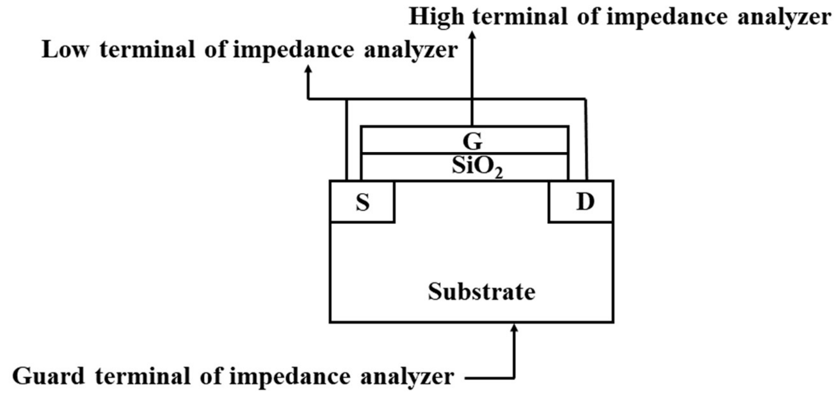


Fig. 2. 4 C-V measurement setup.

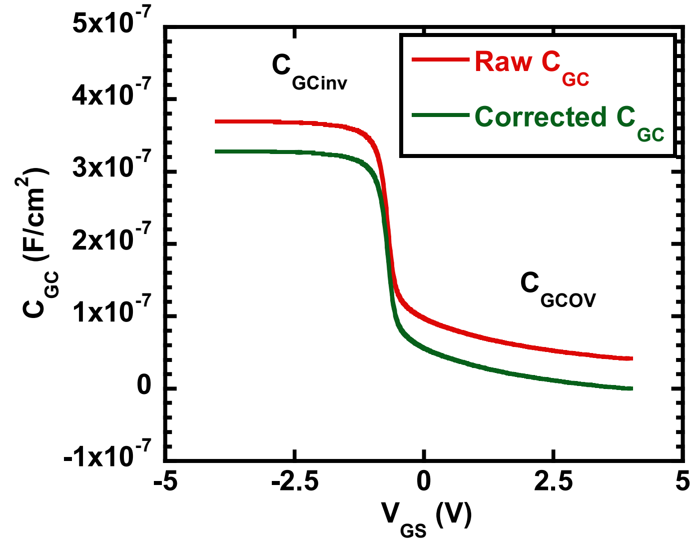


Fig. 2. 5 C-V characteristic plot of a MOS capacitor.

$$T_{OX} = \frac{\varepsilon_0 \varepsilon_{SiO_2}}{C_{OX}} \tag{2.3}$$

where, ε_0 is the free space permittivity, ε_{SiO_2} is the dielectric constant of SiO_2, and C_{OX} is the capacitance of the oxide layer.

2.3 Setup for Flicker (1/f) Noise Measurements and Procedures

The setup for the flicker (1/f) noise measurements is shown in Fig. 2.6. Flicker (1/f) noise power spectral density (PSD) data were recorded by utilizing an HP 3562A Dynamic Signal Analyzer. The device was placed inside the Micromanipulator 8600 probe station.

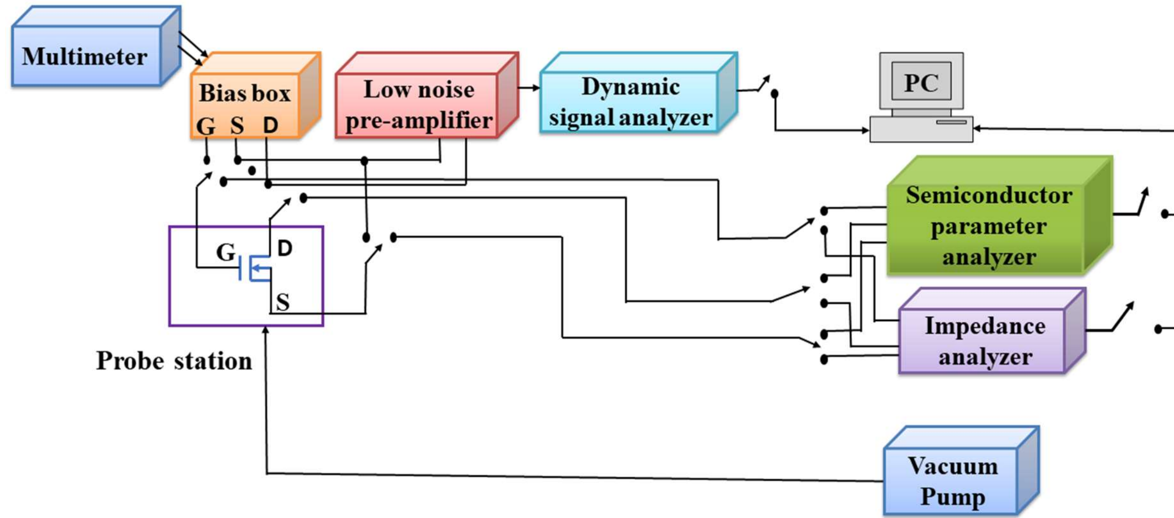


Fig. 2. 6 Flicker (1/f) noise measurement setup.

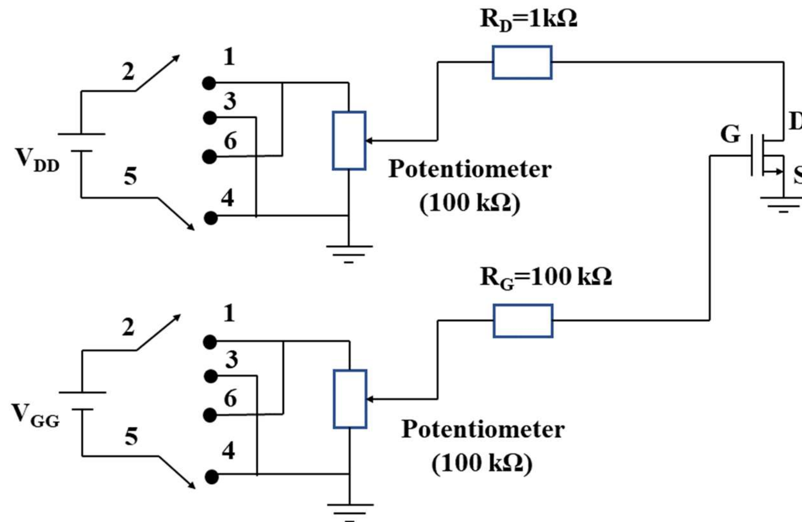


Fig. 2. 7 Biasing circuitry of the DC battery used in both RTS and 1/f noise measurements.

In the beginning, the functionality of the MOSFET was tested using the SPA. After obtaining the I-V characteristic plots, the threshold voltage V_{TH} was determined. A home-made battery-operated DC bias box

was used in this experiment to provide drain-source and gate-source bias voltages for proper operation of the MOSFET device in the linear region. The internal circuit diagram of the DC bias box is shown in Fig. 2.7. Two sets of 13.6 Volt batteries were used for current biasing the gate-source and drain-source terminals of the MOSFET. The voltage divider concept was utilized with a 100 kΩ potentiometer in this case. Miniature SPDT 7203 toggle switches were used to apply the battery voltages across the potentiometer. To prevent the flow of gate leakage current and premature turn-on of the MOSFET, a 100 kΩ resistance was used in the gate terminal. To current bias the MOSFET, a 1 kΩ drain resistance was used in the drain terminal. The biasing signal was amplified with a low noise preamplifier (model 113, EG&G). Then the amplified output signal was fed to the dynamic signal analyzer (HP 3562A). The dynamic signal analyzer was used to plot voltage noise PSD as a function of frequency f .

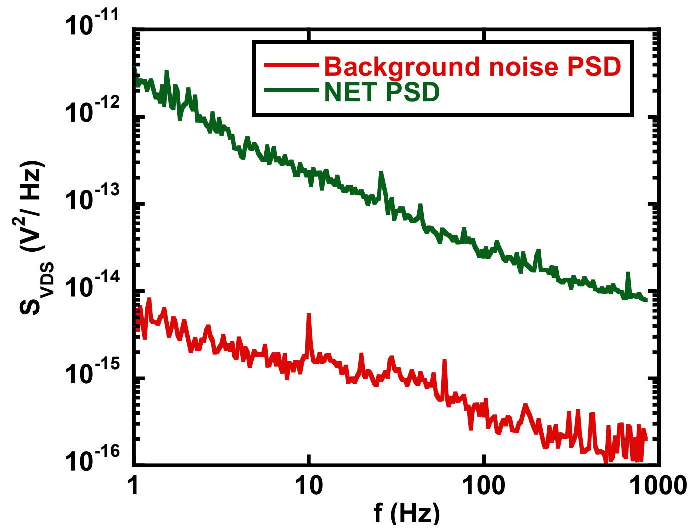


Fig. 2. 8 Background noise and net power spectral density (PSD) of a nMOSFET.

After making all the necessary connections for the measurement setup (Fig. 2.6), the background noise power spectral density (PSD) was obtained as a function of frequency from 1 Hz to 1 kHz. When recording the background noise PSD in the dynamic signal analyzer, V_{DS} was kept at zero volts for various V_{GS} values. Background noise consists of noise from the 60 Hz power line, biasing circuitry, pre-amplifier, contact point of the probe tips, and thermal noise. After determining the background noise PSD, V_{DS} of the device was changed to 200 mV, and the device was operated in the linear region for various V_{GS} values. The raw voltage noise PSD data were then obtained from the dynamic signal analyzer. The net voltage noise PSD was calculated by subtracting the background noise PSD from the raw voltage noise PSD (Fig. 2.8). A customized computer program based on a noise measurement algorithm was stored on the PC. The algorithm contains commands to plot the PSD data as a function of frequency in a log-log scale. That

algorithm also contains other information i.e., the start and end value for the frequency range, number of decades the frequency spans, how many averages of PSD data are going to be performed, and which channel of the dynamic signal analyzer is going to be active showing the output trace. All the data obtained from the dynamic signal analyzer were also saved on that PC. For a better estimation of the noise data, averages of 30 sets of data were recorded in the dynamic signal analyzer (for both background noise PSD and voltage noise PSD). To have more data points in the lower range of frequency, the logarithmic resolution criteria was chosen instead of the linear resolution.

2.4 RTS Noise Measurements Under Channel Hot Carrier (CHC) Stressing

RTS measurements were carried out for the pMOSFETs under two different experimental setups. In the first experimental setup, RTS data were recorded only at room temperature for different stressing times under CHC. pMOSFET was placed inside the micromanipulator probe station in that case. For the second experimental setup, the device was placed in a cryostat inside the shielded room as variable temperature measurements were taken for different stressing times. In this second case, room temperature measurements were also taken inside the shielded room. In this section, we discuss only the variable temperature experimental measurement procedures and setup.

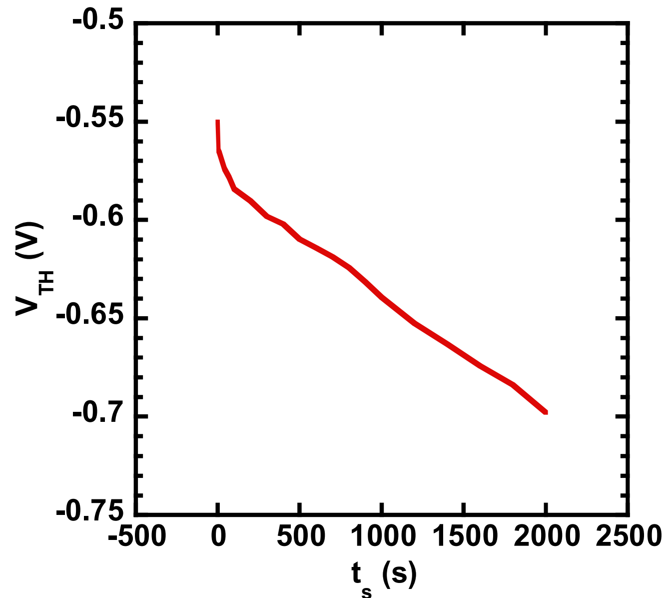


Fig. 2. 9 Degradation of threshold voltage V_{TH} as a function of stressing time t_s for a pMOSFET.

In the beginning, the device was placed in the cryostat inside the shielded room and examined for its functionality by using the SPA. Different DC parameters like threshold voltage V_{TH}, channel conductance

g_d, and $I-V$ characteristics were recorded. A detailed description about the acquisition of these DC parameters can be found in section 2.1. Once the device functionality was verified, we started to take the RTS measurements. A DC power source operated by battery was employed to bias the device in the linear region by adjusting the gate-source voltage V_{GS} and drain-source voltage V_{DS}. A low noise pre-amplifier was utilized, and an oscilloscope was used to record the amplified output signal. The device was scanned for a variable range of V_{GS} from -1 to -4 V at a fixed V_{DS} of -0.2 V to check for RTS, and the frequency of sampling and total time period were chosen to ensure at least 800 transitional switching events in the recorded RTS data [46], [47]. After taking the room temperature measurements, a cryogenic system was utilized to perform variable temperature measurements of the device RTS down to 215 K. Details about the cryogenic system and its setup are discussed in the next section. Once the variable-temperature measurement was completed on the fresh device, the device was stressed at $V_{GS} = V_{DS} = -6\ V$ using the SPA back in the room temperature. Again, the device functionality was verified, and the DC parameters were recorded. RTS data were first recorded at room temperature and afterward at variable temperatures. Stressing was performed for up to 1200 seconds with variable time intervals of 100 to 300 seconds. The recorded RTS data led to the determination of various RTS trap parameters to identify the responsible defect center for all the traps. The recorded V_{TH} values from the SPA for one of the devices as a function of stressing time t_s is shown in Fig. 2.9.

2.5 Experimental Setup for RTS Measurements Under Variable Temperatures

Performing the variable temperature measurements are necessary to calculate the RTS parameters responsible for the identification of the defect centers. The setup for the variable temperature RTS measurements is shown in Fig. 2.10.

The device was placed in a cryostat inside a metallic shielded room to lower the electromagnetic interference from the instruments, which were present outside the shielded room. All the DC-operated equipment were placed inside the shielded room. AC line power driven equipment were present outside the shielded room to prevent electromagnetic disturbances. A known voltage was always maintained on the leads of the device to protect it from electrostatic discharge (ESD). To minimize the heat exchange by convection between the device and the surroundings, the cryostat was evacuated using a rotary pump. The vacuum pump was used to keep the cryostat pressure below 65 mTorr.

To perform the variable temperature measurements, an open-end flow system using liquid N_2 evaporation was utilized. A refillable buffer Dewar was used inside the shielded room instead of the liquid N_2 tank to

minimize the noise. The accuracy and stability of the temperature control mechanism depended largely on the pressure of the liquid N_2 inside the Dewar. For this reason, a high pressure N_2 gas cylinder was used. A pressure regulator was placed between the gas cylinder and the Dewar to maintain the required pressure level, which precisely controlled the temperature. The pressure of the N_2 gas flow was kept between 8 and 12 psi for an optimum level of control over temperature [46].

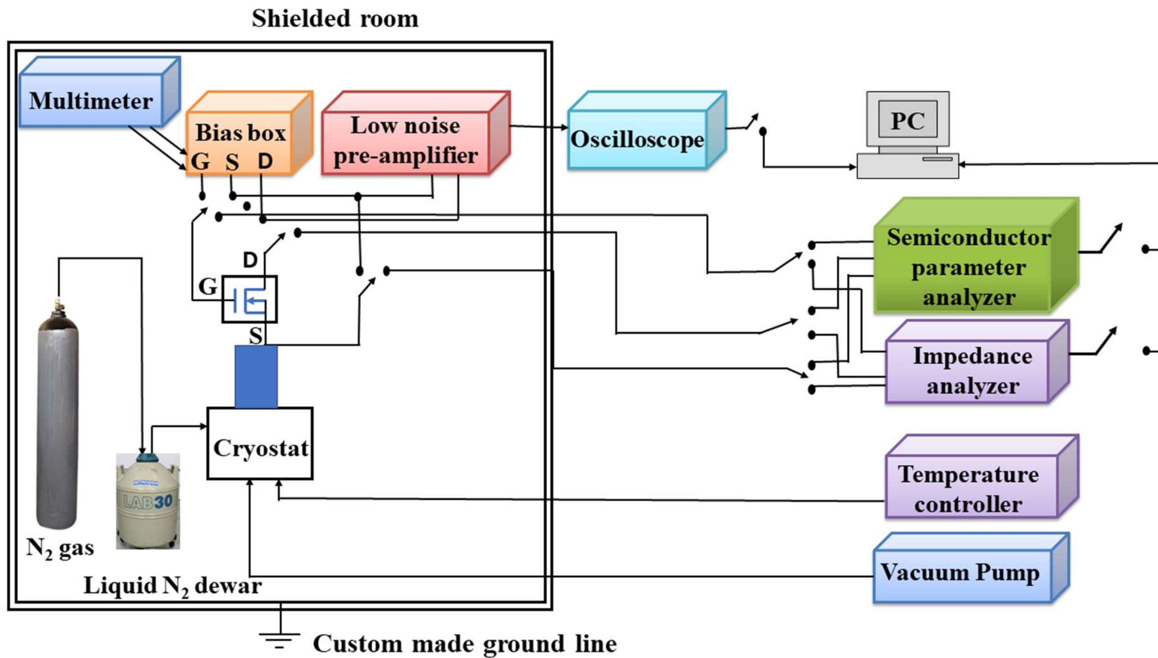


Fig. 2. 10 RTS noise measurement setup under variable temperature.

A PID controller was utilized to set the temperature of the system. PID parameters were independently set through the control panel. A Lakeshore 330 Autotuning temperature controller was used for this purpose. The proportional, integral, and differential gains of the controller were fixed at 350, 50, and 0, respectively [84].

In this chapter, the measurement techniques and the setup for obtaining reliable RTS and flicker (1/f) noise data are discussed. These steps were maintained for the entire duration of the experiment, from the testing of device functionality to the procurement of data at the end.

Chapter 3: RTS Trap Parameters in pMOSFET

The trapping/ detrapping of the channel carrier into the defect site results in a random telegraph signal (RTS). These defect sites are located inside SiO_2 or at the Si-SiO_2 interface of a MOSFET. The presence of RTS is generally observed in small area MOSFETs $\left(\le 1\mu m^2\right)$. A two-level RTS denotes only one active trap, whereas the presence of multi-level RTS represents multiple active traps within the time window of the measurement. Analyzing the RTS is a vital part of obtaining information about the identity of the defect as well as understanding its different physical properties. There are several trap parameters obtained from room temperature RTS experiments: carrier average capture time $\left(\overline{\tau}_c\right)$, carrier average emission time $\left(\overline{\tau}_e\right)$, RTS amplitude $\left(\Delta V_{DS}\right)$, trap position $\left(z_T\right)$, capture cross-section $\left(\sigma\right)$, screened scattering coefficient $\left(\alpha\right)$, and the trap energy level with respect to the oxide valence band edge $\left(E_T - E_{V_{OX}}\right)$. However, the identification of the defect is not possible by determining only these parameters. Variable temperature RTS measurements are required to determine some other trap parameters necessary for the identification of the defect. These parameters are capture cross-section pre-factor $\left(\sigma_0\right)$, capture activation energy $\left(\Delta E_B\right)$, change in enthalpy $\left(\Delta H\right)$, change in entropy $\left(\Delta S/k_B\right)$, and relaxation energy $\left(E_R\right)$.

In this chapter, the theory and definition of these RTS trap parameters (both from the room temperature and variable temperature RTS experiments) are discussed for pMOSFETs.

3.1 Average Capture and Emission Times

Capture time denotes the amount of time that the defect site is empty, that is, from the time emission occurs to the time of carrier capture from the channel. On the other hand, emission time is defined as the time span when the trap site is filled with the carrier. It is the amount of time that the charge carrier remains trapped in the defect site before being emitted to the channel. In this section, the relation between the average capture and emission time with the trap energy level is discussed.

When the electron or hole gets captured in the defect site, the carrier occupancy changes. The grand partition function of a system is utilized to define the occupancy of the defect site with the carriers. It is expressed as [12], [85],

$$Z_G = \sum_{ASN} e^{-(E_S - NE_F)/k_B T} \tag{3.1}$$

Here, ASN stands for summation over S number of states and N number of particles. E_S is the energy level of the state S, E_F is the Fermi energy level, k_B is the Boltzmann's constant, and T is the temperature.

The probability of finding the system in a state of N_1 number of particles at E_1 energy is [12],

$$P(N_1, E_1) = \frac{\chi e^{-(E_1 - N_1 E_F)/k_B T}}{Z_G} \tag{3.2}$$

where, χ is the degeneracy of that particular state (N_1, E_1). Now, considering a defect system of two separate charge states, n and $(n+1)$, the grand partition function of the whole system is represented as [12],

$$Z_G = \chi(n) e^{nE_F/k_B T} + \chi(n+1) e^{-\{E(n+1/n) - (n+1)E_F/k_B T\}} \tag{3.3}$$

Here, $\chi(n)$ is the degeneracy of the n- electron state, $\chi(n+1)$ is the degeneracy of the $(n+1)$ electron state, and $E(n+1/n)$ is the energy difference between the $(n+1)$ and n states. In the n-electron state, the energy of the system is considered zero.

The probability of the defect site being filled with an electron is [12],

$$P(n+1) = f_e = \frac{\chi(n+1) e^{-\{E(n+1/n) - (n+1)E_F/k_B T\}}}{\chi(n) e^{nE_F/k_B T} + \chi(n+1) e^{-\{E(n+1/n) - (n+1)E_F/k_B T\}}} = \left[1 + \frac{\chi(n)}{\chi(n+1)} e^{E(n+1/n) - E_F/k_B T}\right]^{-1} \tag{3.4}$$

After introducing the trap degeneracy factor $g = \chi(n)/\chi(n+1)$, Eqn. 3.4 can be rewritten as,

$$f_e = \left[1 + g e^{E(n+1/n) - E_F/k_B T}\right]^{-1} \tag{3.5}$$

The probability of the defect site being filled with a hole is $f_h = 1 - f_e$. After replacing the trap energy level $E(n+1/n)$ as E_T, f_h can be expressed as,

$$f_h = 1 - \left[\frac{1}{1 + g e^{E_T - E_F/k_B T}}\right] \tag{3.6}$$

For the RTS of average capture time $\bar{\tau}_c$ and average emission time $\bar{\tau}_e$, the ratio of these two parameters can be expressed as a function of the probability of the trap site being filled with a hole (f_h) as [47],

$$\frac{\overline{\tau}_c}{\overline{\tau}_e} = \frac{1 - f_h}{f_h} \tag{3.7}$$

Substituting for f_h from Eqn. 3.6 into Eqn. 3.7,

$$\frac{\overline{\tau}_c}{\overline{\tau}_e} = ge^{-(E_T - E_F)/k_B T} \tag{3.8}$$

With the increase of the gate-source voltage magnitude V_{GS}, the hole occupancy function f_h increases. This leads to the decrease of $\left(\overline{\tau}_c / \overline{\tau}_e\right)$ with the increase in the magnitude of V_{GS}. Therefore, the upper and lower levels of a two-level RTS can be detected as either $\overline{\tau}_c$ or $\overline{\tau}_e$.

3.2 Energy Level and Position of The Trap

Position of the trap z_T denotes the defect site location measured from the Si-SiO_2 interface into SiO_2. The energy level of the trap E_T is represented with respect to the valence band edge of SiO_2. Fig. 3.1 is used to determine these parameters. In Fig. 3.1, band diagram of the pMOSFET is shown with respect to its source terminal. From Fig. 3.1,

$$\frac{E'}{z_T} = \frac{qV_{OX}}{T_{OX}} \tag{3.9}$$

$$E'' = q\psi_s - \left(E_F - E_V\right) \tag{3.10}$$

$$\varphi_0 - E'' = E' + \left(E_T - E_{V_{OX}}\right) + \left(E_F - E_T\right) \tag{3.11}$$

Here, q is the electronic charge, V_{OX} is the band bending inside the oxide, T_{OX} is the oxide layer thickness, ψ_s is the surface potential, E_V is the Si valence band, φ_0 is the energy difference between the valence band edges of Si and SiO_2 at the Si-SiO_2 interface, and $E_{V_{OX}}$ is the oxide valence band edge (Fig. 3.1). Rearranging Eqn. 3.11,

$$E_T - E_F = E' + \left(E_T - E_{V_{OX}}\right) - \varphi_0 + E'' \tag{3.12}$$

Replacing E' and E'' terms from Eqns. 3.9 and 3.10, respectively into Eqn. 3.12,

$$E_T - E_F = \frac{qV_{OX} z_T}{T_{OX}} + \left(E_T - E_{V_{OX}}\right) - \varphi_0 + q\psi_s - \left(E_F - E_V\right) \tag{3.13}$$

The band bending inside the oxide is,

$$V_{OX} = V_{GS} - V_{FB} - \psi_s \tag{3.14}$$

where, V_{FB} is the flat band voltage. Using Eqns. 3.8 ($g = 1$ is used for the trap degeneracy factor) and 3.14 in Eqn. 3.13,

$$-k_B T \ln\left(\frac{\overline{\tau}_c}{\overline{\tau}_e}\right) = \frac{q\left(V_{GS} - V_{FB} - \psi_s\right) z_T}{T_{OX}} + \left(E_T - E_{V_{OX}}\right) - \varphi_0 + q\psi_s - \left(E_F - E_V\right) \tag{3.15}$$

$$\Rightarrow \ln\left(\frac{\overline{\tau}_c}{\overline{\tau}_e}\right) = -\frac{1}{k_B T}\left[\left(E_T - E_{V_{OX}}\right) - \left(E_F - E_V\right) - \varphi_0 + q\psi_s + \frac{qz_T}{T_{OX}}\left(V_{GS} - V_{FB} - \psi_s\right)\right] \tag{3.16}$$

The position of the trap with respect to the oxide valence band edge $\left(E_T - E_{V_{OX}}\right)$ can be computed from Eqn. 3.16, once all the other parameters are known.

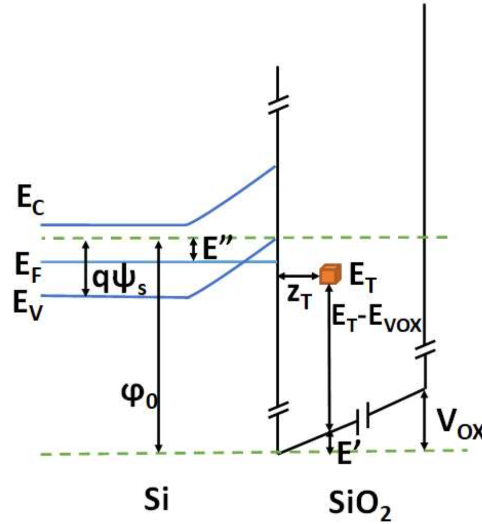


Fig. 3. 1 Energy band diagram of a pMOSFET at the source end of the channel.

The trap position z_T can be determined by differentiating both sides of Eqn. 3.16 with respect to V_{GS}. In some of the earlier works, ψ_s was considered constant with respect to V_{GS} in this differentiation [16], [17]. However, in pMOSFETs, with the increase of the magnitude of V_{GS}, conduction and valence band bend

more in the direction of higher electronic energy, resulting in an increase in ψ_s magnitude (Fig. 3.1). Consequently, z_T is computed by differentiating both sides of Eqn. 3.16 with V_{GS} as,

$$\frac{d}{dV_{GS}}\left(\ln\frac{\overline{\tau}_c}{\overline{\tau}_e}\right)=-\frac{1}{k_BT}\left[\frac{qz_T}{T_{OX}}\left(1-\frac{d\psi_s}{dV_{GS}}\right)+q\frac{d\psi_s}{dV_{GS}}\right] \tag{3.17}$$

$$\Rightarrow\frac{qz_T}{T_{OX}}\left(1-\frac{d\psi_s}{dV_{GS}}\right)=-k_BT\frac{d}{dV_{GS}}\left(\ln\frac{\overline{\tau}_c}{\overline{\tau}_e}\right)-q\frac{d\psi_s}{dV_{GS}} \tag{3.18}$$

The trap position z_T is represented as,

$$z_T=\frac{T_{OX}\left[\frac{d\psi_s}{dV_{GS}}+\frac{k_BT}{q}\frac{d}{dV_{GS}}\ln\left(\frac{\overline{\tau}_c}{\overline{\tau}_e}\right)\right]}{\left(\frac{d\psi_s}{dV_{GS}}-1\right)} \tag{3.19}$$

3.3 RTS Amplitude and Screened Scattering Coefficient

RTS amplitude ΔV_{DS} is the fluctuation of the drain-source voltage V_{DS} with respect to time and it is represented as the difference between two consecutive levels in the RTS. The capture of a carrier from the channel into the defect site inside SiO_2 causes number and mobility fluctuations of the channel carriers. In this section, a mathematical relationship of the RTS amplitude with these fluctuations is established for a pMOSFET.

In the linear region of a pMOSFET, drain-source current is,

$$I_{DS}=W\mu qP_{inv}E_y \tag{3.20}$$

Here, W is the channel width of the device, μ is the effective mobility of the channel carriers, P_{inv} is the inversion layer hole density of the pMOSFET per unit area, and E_y is the applied electric field along the channel.

Whenever a hole gets trapped in the defect center, there is a fluctuation in the number and mobility of holes in the channel. From Eqn. 3.20,

$$\frac{\partial I_{DS}}{I_{DS}}=\left[\frac{1}{\Delta P_{inv}}\frac{\partial\Delta P_{inv}}{\partial\Delta P_t}\pm\frac{1}{\mu}\frac{\partial\mu}{\partial\Delta P_t}\right]\partial\Delta P_t \tag{3.21}$$

where, ΔP_{inv} is the number of inversion layer holes in a small area of $W\Delta y$, ΔP_t is the total number of occupied traps in that $W\Delta y$ area. They are represented as,

$$\Delta P_{inv} = P_{inv} W \Delta y \tag{3.22}$$

$$\Delta P_t = P_t W \Delta y \tag{3.23}$$

P_t is the trap density per unit area of a pMOSFET. According to Matthiessen's rule, the effective channel carrier mobility can be represented as [57],

$$\frac{1}{\mu} = \frac{1}{\mu_{oth}} + \frac{1}{\mu_{OX}} = \frac{1}{\mu_{oth}} + \alpha P_t \tag{3.24}$$

where, μ_{OX} is the mobility due to oxide charge scattering, μ_{oth} is the mobility component limited by other scattering mechanisms (lattice scattering, impurity scattering, and surface roughness scattering), and α is the screened scattering coefficient. Now, Eqn. 3.24 is simplified as,

$$\mu = \frac{\mu_{oth}}{1 + \alpha \mu_{oth} P_t} \tag{3.25}$$

Differentiating both sides of Eqn. 3.25 with respect to P_t,

$$\frac{\partial \mu}{\partial P_t} = -\frac{\alpha \mu_{oth}^2}{\left(1 + \alpha \mu_{oth} P_t\right)^2} = -\alpha \mu^2 \tag{3.26}$$

Replacing Eqn. 3.23 in Eqn. 3.26,

$$\frac{\partial \mu}{\partial \Delta P_t} = \frac{1}{W \Delta y}\left(\frac{\partial \mu}{\partial P_t}\right) = \frac{-\alpha \mu^2}{W \Delta y} \tag{3.27}$$

As the inversion layer hole gets trapped inside the defect site and the decrease of one inversion layer hole from the channel causes the increase of one trapped hole inside SiO_2, we can write $\delta \Delta P_{inv} / \delta \Delta P_t = 1$. Taking this relationship between $\delta \Delta P_{inv}$ and $\delta \Delta P_t$ into consideration and using Eqn. 3.27, Eqn. 3.21 becomes,

$$\frac{\partial I_{DS}}{I_{DS}} = \left[\frac{-1}{P_{inv} W \Delta y} \pm \frac{1}{\mu}\left(\frac{-\alpha \mu^2}{W \Delta y}\right)\right] \partial \Delta P_t = -\left[\frac{1}{P_{inv}} \pm \alpha \mu\right] \frac{\partial \Delta P_t}{W \Delta y} \tag{3.28}$$

The drain-source current fluctuation for the entire channel length L of the device can be represented as,

$$\Delta I_{DS} L = \partial I_{DS} \Delta y \tag{3.29}$$

where, ΔI_{DS} is the fluctuation in the drain source current. For trapping a single inversion layer hole in the defect site ($\partial\Delta P_t = 1$), Eqn. 3.28 becomes,

$$\frac{\Delta V_{DS}}{V_{DS}} \approx \frac{\Delta I_{DS}}{I_{DS}} = -\left[\frac{1}{P_{inv}} \pm \alpha\mu\right]\frac{1}{WL} \tag{3.30}$$

Here, V_{DS} is the drain-source voltage and ΔV_{DS} is the fluctuation in the drain-source voltage (also known as RTS amplitude) of a pMOSFET.

Number and mobility fluctuations are represented by the right-hand side terms of Eqn. 3.30, respectively. The addition or subtraction sign between them depends on whether the trap is an attractive or a repulsive center [47]. In case of the trap being an attractive center, the negatively charged defect center becomes neutral after capturing a hole. Channel resistance from the number and mobility fluctuations acts in reverse order and the sign becomes negative between these counterparts. On the contrary, if the trap is a repulsive center, a positive sign is incorporated in Eqn. 3.30.

3.4 Trap Capture Cross-section

Capture cross-section is an area around the defect site within which it can capture a carrier. The capture rate of a hole in the defect site inside SiO_2 or at the Si-SiO_2 interface is [12],

$$\frac{1}{\overline{\tau}_c} = \int_{-\infty}^{E_V} r(E)dE \tag{3.31}$$

Here, $r(E)$ is the rate of transition per unit energy at energy E .

The rate of transition per unit energy $r(E)$ is expressed as the multiplication of the inversion layer hole concentration per unit volume $p(E)$, average thermal velocity of holes $\overline{v}_{th}(E)$, and capture cross-section $\sigma(E)$ at E . Therefore,

$$\frac{1}{\overline{\tau}_c} = \int_{-\infty}^{E_V} p(E)\overline{v}_{th}(E)\sigma(E)dE \tag{3.32}$$

The hole concentration, average thermal velocity, and capture cross-section are considered uniform with respect to E . Therefore, Eqn. 3.32 can be simplified as,

$$\frac{1}{\overline{\tau}_c} = p\overline{v}_{th}\sigma \tag{3.33}$$

The trap capture cross-section σ is calculated by utilizing Eqn. 3.33. $\overline{\tau}_c$ is determined by analyzing the RTS, whereas $\overline{v}_{th} = \left(8k_B T/\pi m_p^*\right)^{1/2}$ [12], where m_p^* is the effective mass of hole. However, the hole concentration p needs to be determined. The hole concentration p is calculated from [86],

$$p(T) = p_0(T)e^{-q\psi_s/k_B T} \tag{3.34}$$

where, p_0 is the equilibrium hole concentration. It is determined from,

$$p_0(T) = \frac{n_i^2(T)}{n_0} \approx \frac{n_i^2(T)}{N_D(T)} \approx \frac{n_i^2(T)}{N_D^+(T)} \tag{3.35}$$

where, n_i is the intrinsic electron concentration, n_0 is the equilibrium electron concentration, N_D is the background donor doping concentration, and N_D^+ is the ionized donor doping concentration.

The intrinsic electron concentration is represented as,

$$n_i(T) = \sqrt{N_C(T)N_V(T)}e^{-E_g(T)/2k_B T} \tag{3.36}$$

where, N_C is the effective density of states of electrons in the conduction band, N_V is the effective density of holes in the valence band, and E_g is the bandgap of Si. These parameters are calculated from,

$$N_C(T) = 2\left(\frac{2\pi m_n^* k_B T}{h^2}\right)^{3/2} \tag{3.37}$$

$$N_V(T) = 2\left(\frac{2\pi m_p^* k_B T}{h^2}\right)^{3/2} \tag{3.38}$$

$$E_g(T) = 1.166 - \frac{4.73\times10^{-4}T^2}{(T+636)} \tag{3.39}$$

Here, m_n^* is the effective mass of electron and h is Planck's constant.

At low temperatures, due to carrier freeze out, background donor doping concentration cannot be considered to be equal to the equilibrium electron concentration $\left[n_0 = N_D^+ \neq N_D\right]$. The equilibrium concentration of electron is represented as [86],

$$n_0(T) = N_C(T)e^{E_F - E_C/k_B T} \tag{3.40}$$

Here, E_C is the conduction band of Si. The ionized donor doping concentration is represented as,

$$N_D^+(T) = n_0(T) = \frac{N_D}{1 + g_{do}e^{E_F - E_D/k_B T}} \tag{3.41}$$

Here, g_{do} is the donor degeneracy factor and E_D is the donor energy level. Eqn. 3.41 can be rewritten as,

$$n_0(T) = \frac{N_D}{1 + \left(\frac{g_{do}}{N_C(T)}\right)e^{E_C - E_D/k_B T} n_0(T)} \tag{3.42}$$

After solving Eqn. 3.42, n_0 is expressed as,

$$n_0(T) = \frac{-1 \pm \sqrt{1 + 4\left[\left(\frac{g_{do}}{N_C(T)}\right)e^{E_C - E_D/k_B T}\right]N_D}}{2\left[\left(\frac{g_{do}}{N_C(T)}\right)e^{E_C - E_D/k_B T}\right]} \tag{3.43}$$

Here in Eqn. 3.43, plus sign is always used before the square root term on the right-hand side. The minus sign is omitted as it would result in a negative n_0 value.

Determining the surface potential ψ_s is essential to calculate the hole concentration p in Eqn. 3.34. ψ_s also plays a major role to determine the energy level of the trap with respect to the oxide valence band edge and the position of the trap from the Si-SiO_2 interface (section 3.2). ψ_s is calculated from,

$$P_{inv} = \left\{\frac{\sqrt{2}\varepsilon_0\varepsilon_{Si}k_B T}{q^2 L_D(T)}\sqrt{\left(u + e^{-u} - 1\right) + \left(\frac{n_i}{n_0}\right)^2\left(e^u - u - 1\right)}\right\} - n_0\sqrt{\frac{2\varepsilon_0\varepsilon_{Si}\psi_s}{qn_0}} \tag{3.44}$$

Here, ε_0 is the permittivity of the free space, ε_{Si} is the dielectric constant of Si, $u = q\psi_s/k_B T$, and $L_D(T) = \sqrt{\varepsilon_0\varepsilon_{Si}k_B T/q^2 n_0}$ is known as Debye length. P_{inv} is obtained experimentally from the C-V measurements.

3.5 Capture Activation Energy and Capture Cross-section Pre-factor

In Fig. 3.2, a configuration co-ordinate diagram of a pMOSFET is shown. The carrier trapping and detrapping from the channel to the defect sites inside SiO_2 is a multi-phonon assisted tunneling process [10], [11], [12]. A hole from the valence band needs to overcome an energy barrier to get captured in the defect site inside SiO_2. The required amount of energy for the hole to cross this barrier is defined as the capture activation energy ΔE_B. Once the hole is trapped in the defect site, it emits several phonons to get back to the trap energy level. This amount of emitted phonon energy needed for structural relaxation is known as E_R. The energy required by the hole to get back to the valence band from the defect site is the emission activation energy. The difference of energy between the capture and emission is known as Gibbs free energy ΔG. It is expressed as $\Delta G = \Delta H - T\Delta S$, where ΔH is the change in enthalpy and ΔS is related with the change in entropy.

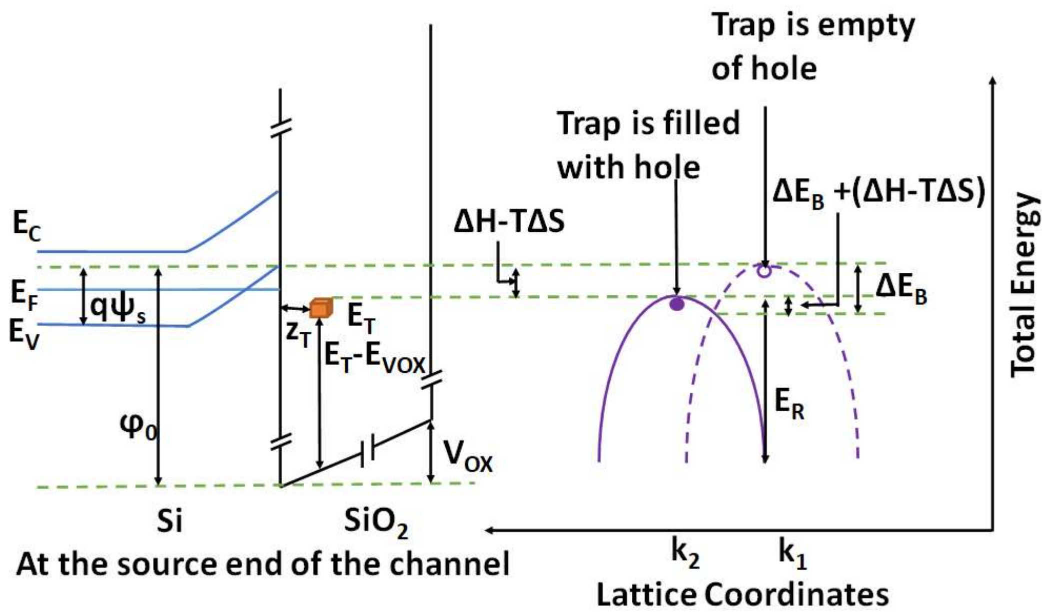


Fig. 3. 2 Configuration co-ordinate diagram of a pMOSFET.

There is a relation between capture cross-section σ and capture activation energy ΔE_B expressed as [12],

$$\sigma = \sigma_0 e^{-\Delta E_B / k_B T} \tag{3.45}$$

Here, σ_0 is the capture cross-section pre-factor. From the Arrhenius plot of σ, both σ_0 and ΔE_B can be calculated.

Without performing the variable temperature RTS measurements, determination of σ_0 and ΔE_B is not possible.

3.6 Emission Activation Energy

The energy required for the trapped hole to get back to the valence band from the defect site is known as the emission activation energy. It is shown as $\left[\Delta E_B + \left(\Delta H - T\Delta S\right)\right]$ in Fig. 3.2. In this section, mathematical derivations are carried out to determine the emission activation energy. From Eqn. 3.8,

$$\overline{\tau}_e = \frac{\overline{\tau}_c}{g} e^{E_T - E_F / k_B T} \tag{3.46}$$

Using Eqn. 3.45, the average capture time $\overline{\tau}_c$ is expressed as,

$$\overline{\tau}_c = \frac{1}{\sigma \overline{v}_{th} p(T)} = \frac{e^{\Delta E_B / k_B T}}{\sigma_0 \overline{v}_{th} p(T)} \tag{3.47}$$

Mean thermal velocity is represented as [12],

$$\overline{v}_{th} = \left(\frac{8 k_B T}{\pi m_p^*} \right)^{1/2} \tag{3.48}$$

The inversion layer hole density is,

$$p(T) = N_V(T) e^{E_V - E_F / k_B T} \tag{3.49}$$

Using Eqns. 3.47 and 3.48 in Eqn. 3.46,

$$\overline{\tau}_e = \frac{e^{\Delta E_B / k_B T} e^{E_T - E_F / k_B T}}{g \sigma_o \left(\frac{8 k_B T}{\pi m_p^*} \right)^{1/2} p(T)} \tag{3.50}$$

Substituting Eqn. 3.49 in Eqn. 3.50,

$$\overline{\tau}_e = \frac{e^{\Delta E_B / k_B T} e^{E_T - E_F / k_B T} e^{E_F - E_V / k_B T}}{g \sigma_o \left(\frac{8 k_B T}{\pi m_p^*} \right)^{1/2} N_V} \tag{3.51}$$

Defining trap energy level with respect to the Si valence band edge $\Delta E_{TV} = E_T - E_V$ in Eqn. 3.51,

$$\overline{\tau}_e = \frac{e^{\Delta E_B + \Delta E_{TV}/k_B T}}{g\sigma_o \left(\frac{8k_B T}{\pi m_p^*}\right)^{1/2} N_V} \tag{3.52}$$

The ΔE_{TV} term is expressed as the resultant of the change in enthalpy ΔH and change in entropy $\Delta S/k_B$, $\Delta E_{TV} = \Delta H - T\Delta S$. In a pMOSFET, change in entropy $\Delta S/k_B$ occurs upon hole emission from the oxide trap to the channel. When a hole is emitted from the defect site to the Si channel (an electron capture from the Si valence band), structural relaxation occurs around the defect. This structural relaxation involves the displacements of the lattice atoms in the vicinity of the defect site [87]. As a result, there is a change in the amount of disorder of the local environment around the defect. $\Delta S/k_B$ is an indicator of that disorder in the system.

Replacing the ΔE_{TV} term in Eqn. 3.52,

$$\overline{\tau}_e = \frac{e^{\Delta E_B + \Delta H/k_B T}}{g\sigma_o \left(\frac{8k_B T}{\pi m_p^*}\right)^{1/2} N_V e^{\Delta S/k_B}} \tag{3.53}$$

From the Arrhenius plot of $\tau_e(T) N_V(T) \left[T/m_p^*(T)\right]^{1/2}$, change in enthalpy ΔH and change in entropy $\Delta S/k_B$ can be calculated.

Positive ΔH indicates the process is endothermic, whereas negative ΔH represents an exothermic process. During the endothermic process, after the emission of the hole from the defect site to the valence band, heat is absorbed in the system. However, for the exothermic process, heat is evolved from the system after the emission of the hole from the defect. Positive ΔS means that the system is more disordered when the hole is emitted from the defect site to the valence band. On the other hand, negative ΔS represents less disorder for the system after the emission of the hole back to the channel.

3.7 Relaxation Energy

Once the hole is trapped in the defect site, it emits several phonons to get back to the trap energy level. This amount of energy is the relaxation energy E_R of the trap (Fig. 3.2).

In Fig. 3.2, there are two parabolas represented by solid and dashed lines separately. The parabola with a dashed line represents the energy U_{empty} for the system as a function of the lattice co-ordinate when the trap is empty of a hole. On the other hand, the solid parabola indicates the energy U_{full} for the system when the defect is full of a hole. These energy terms in these two different trap states are represented as,

$$U_{empty} = \frac{1}{2} M\omega^2 \left(k - k_1\right)^2 = A\left(k - k_1\right)^2 \tag{3.54}$$

$$U_{full} = \frac{1}{2} M\omega^2 \left(k - k_2\right)^2 + \Delta G = A\left(k - k_2\right)^2 + \Delta G \tag{3.55}$$

Here, Gibbs free energy is $\Delta G = \Delta H - T\Delta S$, M is the mass of the defect site, ω is the lattice vibration frequency, k is the lattice co-ordinate, k_1 is the corresponding lattice co-ordinate value when the defect site is empty of hole ($k_1 = 0$) and k_2 is the corresponding lattice co-ordinate when the defect site is full with a hole.

From the Fig 3.2, $E_R = Ak_2^2$, $\Delta E_B = Ak_c^2$, where k_c is the corresponding lattice co-ordinate point of the intersection of the two plots. In the intersecting point k_c,

$$U_{empty} = U_{full} \Rightarrow Ak_c^2 = A\left(k_c - k_2\right)^2 + \Delta G \tag{3.56}$$

Simplifying it further,

$$Ak_2^2 - 2Ak_c k_2 + \Delta G = 0 \tag{3.57}$$

Using E_R and ΔE_B in Eqn. 3.57,

$$\left(E_R + \Delta G\right)^2 = 4A^2 k_2^2 k_c^2 \Rightarrow \left(E_R + \Delta G\right)^2 = 4E_R \Delta E_B \tag{3.58}$$

$$\Delta E_B = \frac{\left(E_R + \left(\Delta H - T\Delta S\right)\right)^2}{4E_R} \tag{3.59}$$

Once ΔE_B, ΔH, and $\Delta S/k_B$ are determined from the Arrhenius plots, E_R can be easily computed by utilizing Eqn. 3.59.

In this chapter, the basic definitions and theoretical aspects of the RTS trap parameters have been discussed. Both the room and variable temperature RTS trap parameters have been studied. In the next chapters, these parameters will be utilized to explain different physical properties of the trap and to identify the responsible defect center for the RTS in the pMOSFETs.

Chapter 4: Channel Hot Carrier (CHC) Stressing Effect on Room Temperature RTS Parameters

Among the main MOSFET stressing mechanisms, such as drain avalanche hot carrier (DAHC) stress, channel hot carrier (CHC) stress, and negative bias temperature instability (NBTI) stress, CHC stressing is singled out as resulting in the worst degradation of different DC parameters (channel transconductance, drain source current, and threshold voltage) [34], [37], [38], [39]. Even though it is the worst degradation mechanism, the effect of CHC stressing on random telegraph signals (RTS) has not been given enough attention in pMOSFETs. Degradation of pMOSFETs is much less than nMOSFETs due to the smaller impact ionization rate of the charge carriers as well as the higher Si-SiO_2 energy barrier for holes compared to electrons [38]. Therefore, the effect of CHC on RTS for pMOSFETs has been under-reported. However, investigations on different degradation mechanisms and their effect on RTS are still needed for successful operation of these devices.

In this chapter, the effect of CHC stressing on different RTS trap parameters namely screened scattering coefficient which controls the amount of charge carrier mobility fluctuations due to remote Coulomb scattering by the trap, RTS fluctuation amplitude, average capture time, and capture cross-section will be discussed. The generation of positive fixed oxide charge with stressing has an influence on the screened Coulomb scattering of the channel carriers and consequently their mobility, in addition to the commonly accepted self-screening of the channel carriers. Here, theoretical two-dimensional modeling of the screened Coulomb scattering coefficient for pMOSFETs is carried out and applied, for the very first time, to the case of CHC stressing and RTS. Previously, this model was used only for nMOSFETs under no stressing condition.

Results of this work have been reported in IEEE Transactions on Device and Materials Reliability [88].

4.1 RTS Measurements and Device Specifications

pMOSFETs of smaller dimensions (<1 μm^2) [12] were used for taking RTS measurements under CHC stressing. The pMOSFETs were provided by Texas Instruments. Fourteen devices were tested and RTS was observed among eight devices, indicating the presence of the process-induced traps that are accessible at room temperature and in the linear region of operation. These eight devices were later examined for the presence of stress-induced traps after variable stressing time intervals. In total, RTS data from eleven process-induced and four stress-induced traps were analyzed. As a representative, results from one of the pMOSFETs with a width of W= 0.6 μm and length of L= 0.6 μm are reported here. The gate dielectric was SiO_2 grown to the nominal thickness of 8.7 nm, using dry oxidation followed by N_2 annealing. This

pMOSFET exhibited three process and three stress-induced traps, which allowed us to compare and contrast the properties of these different traps on the same device.

At the beginning of each RTS measurement process, DC characterization was done to extract threshold voltage V_{TH} and current-voltage (I-V) characteristics for the fresh device and after each subsequent stressing. Channel conductance g_d was measured using the Semiconductor Parameter Analyzer (SPA) with reference to the gate to source voltage V_{GS}. The device was scanned by varying V_{GS} at a fixed drain to source voltage V_{DS} to detect any RTS. The MOSFET was placed inside a probe station. A battery-operated DC bias box was used to bias the pMOSFET in the linear region of operation. The drain and source output terminals were fed into a low noise pre-amplifier in differential mode. The low noise pre-amplifier had a gain range of 10-10000 and its output was connected to the oscilloscope. The utilization of the low noise pre-amplifier helped us to measure the low level of voltage fluctuations during RTS measurements on the oscilloscope by amplifying the original signal with the gain. The experimental setup and procedures to conduct RTS measurements were already discussed in chapter 2. The details about the RTS measurement setup can also be found in [46], [47], [62]. After taking the RTS measurements, the pMOSFET was stressed at a higher magnitude of V_{GS} and V_{DS} compared to the rated maximum operating voltage of -5 V. After stressing, the MOSFET was scanned again to detect any switching events in the drain voltage. Stressing was done cumulatively up to 2000 seconds with variable time intervals of 5 seconds to 200 seconds. Here, the reported device was stressed at $V_{GS} = V_{DS} =$ -6 V. During RTS measurements, the range of V_{GS} was from -1 to -4 V and V_{DS} was kept at -0.2 V. All measurements were taken at room temperature and in the linear region of operation following the standard measurement procedures [46], [47], [62]. The frequency of sampling and the RTS data time span were chosen in such a way that there were at least 800 switching events for each type of transition. Two-level and three-level RTS were analyzed to study different trap parameters such as capture time, emission time, trap position, capture cross-section, and RTS amplitude. C-V measurements were carried out with a Precision Impedance Analyzer to quantify the amount of inversion layer charge carrier per unit area Q_{inv} and the oxide layer thickness T_{OX} [45], [89].

4.2 Trap Position and Energy Level

Sample RTS traces for different traps are shown in Figs. 4.1, 4.2, and 4.3. RTS levels for individual traps and their range of presence in different stressing time intervals are summarized in Table 4.1. Trap position z_T and energy level with respect to the SiO_2 valence band edge $\left(E_T - E_{V_{OX}}\right)$ are averaged over all stressing time instances. $\left(E_T - E_{V_{OX}}\right)$ is calculated from [47],

$$\ln\left(\frac{\overline{\tau}_c}{\overline{\tau}_e}\right) = -\frac{1}{k_B T}\left[\left(E_T - E_{V_{OX}}\right) - \left(E_F - E_V\right) - \varphi_0 + q\psi_s + q\frac{z_T}{T_{OX}}\left(V_{GS} - V_{FB} - \psi_s\right)\right] \tag{4.1}$$

Here, $\overline{\tau}_c$ is average capture time, $\overline{\tau}_e$ is average emission time, k_B is Boltzmann's constant, T is temperature, E_F is the Fermi energy in Si, E_V is the Si valence band edge, φ_0 is the energy difference between Si and SiO_2 valence band edges at the Si-SiO_2 interface, q is the electronic charge, ψ_s is surface potential, and V_{FB} is the flat-band voltage.

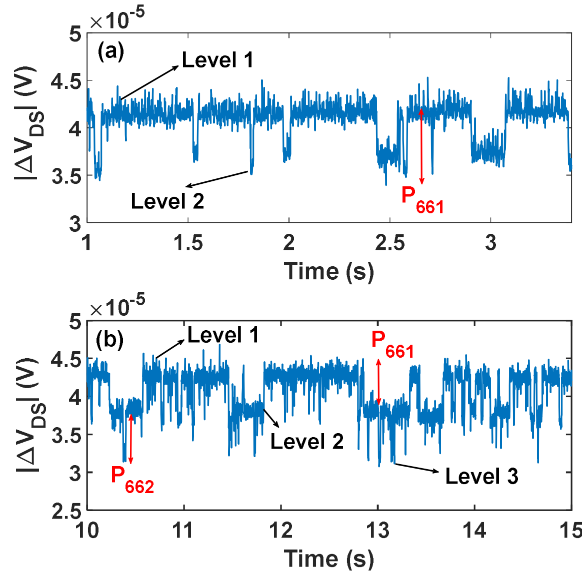


Fig. 4. 1 (a) Two level RTS signal observed on the fresh device at V_{GS} = -1.0 V due to the first process-induced trap P_{661}. (b) Three level RTS signal observed in the fresh device at V_{GS} = -1.1 V. Transition from level 1 to 2 denotes presence of the process-induced trap P_{661} and transition from level 2 to 3 denotes presence of the second process-induced trap P_{662}.

Trap position z_T is calculated by differentiating both sides of Eqn. 4.1 with respect to V_{GS}. Then the trap position z_T is represented as [47], [73]:

$$z_T = \frac{T_{OX}\left[\frac{d\psi_s}{dV_{GS}} + \frac{k_B T}{q}\frac{d}{dV_{GS}}\ln\left(\frac{\overline{\tau}_c}{\overline{\tau}_e}\right)\right]}{\left(\frac{d\psi_s}{dV_{GS}} - 1\right)} \tag{4.2}$$

Neither the trap location nor energy showed any change with stressing.

In Table 4.1, P denotes a process-induced trap and S represents a stress-induced trap. The subscript below the symbol is the width, length of the device, and the specific number given to the trap. Although P_{663} shows RTS after 5 seconds of stressing, still we consider it as a process-induced trap. The Si-O bond length in the

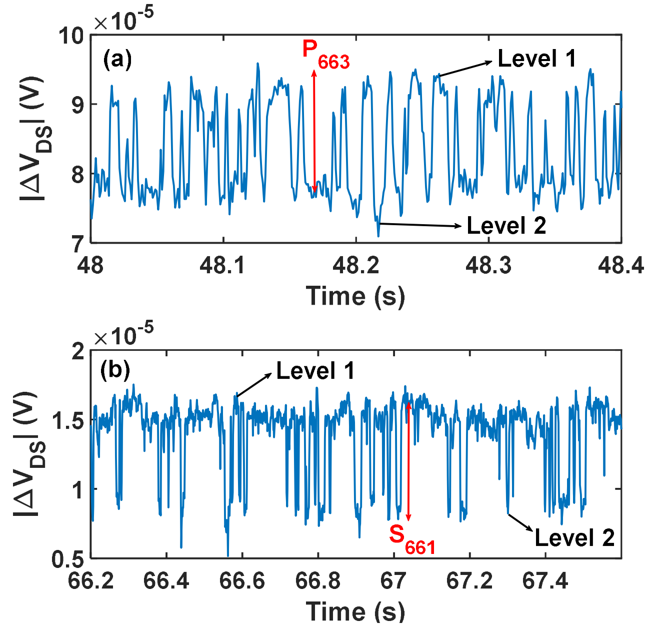


Fig. 4. 2 (a) Two level RTS signal observed after 40 s of stressing at V_{GS} = -1.7 V due to the process-induced trap P_{663}. (b) Two level RTS signal observed after 70 s of stressing at V_{GS} = -2.6 V denotes trap S_{661}.

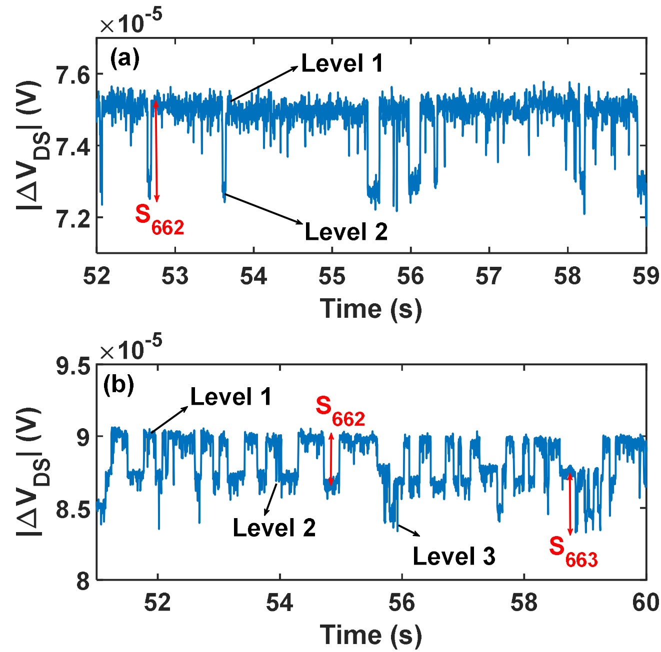


Fig. 4. 3 (a) Two level RTS signal observed after 700 s of stressing at V_{GS} = -3.5 V due to the stress-induced trap S_{662}. (b) Three level RTS signal observed after 800 s of stressing at V_{GS} = -3.65 V. Transition from level 1 to 2 denotes presence of the stress-induced trap S_{662} and transition from level 2 to 3 denotes presence of the other stress-induced trap S_{663}.

SiO_2 network is 0.154-0.169 nm [90], whereas the nearest trap reported here is at 1.27 nm to Si-SiO_2 interface. Therefore, none of the traps can be considered as a Pb center [91]. $\left(E_T - E_{V_{OX}}\right)$ values obtained for the traps point to the fact that trap energy level E_T has to be within a few $k_B T$ of E_F so that communication becomes viable between the defect site and channel carrier [46]. V_{TH} is found to be increasing in magnitude with stressing time t_s . After 2000 seconds of stressing, a 26.9% increase has been observed in V_{TH} from the fresh condition.

Table 4. 1: Trap summary

Trap	RTS Levels	Stress time t_s (s)*	z_T (nm)	$\left(E_T - E_{V_{OX}}\right)$ (eV)**
P_{661}	2/3	0-400	1.93±.032	4.538±.018
P_{662}	2/3	0-300	2.45±.027	4.471±.006
P_{663}	2	5-500	4.28±.046	4.284±.027
S_{661}	2	40-2000	1.27±.037	4.751±.005
S_{662}	2/3	600-1400	3.57±.041	4.434±.017
S_{663}	2/3	700-1200	4.38±.031	4.337±.009

*No RTS was observed for P_{662} at 40 seconds of stressing, whereas for P_{663}, no RTS was observed at 10 and 70 seconds. **For P_{661}, P_{662}, P_{663}, S_{661}, S_{662}, and S_{663}, trap energy level is evaluated at V_{GS} = -1.3, -1.5, -1.7, -2.5, -3.6, and -3.7 V, respectively. V_{DS} = -0.2 V.

4.3 Effect of Stressing on Trap Stability

Switching between RTS levels occurs due to capture and emission of holes from the channel by the gate oxide defect sites. This entire process is governed by Poisson's statistics. The amount of time the trap is present in different charge states shows an exponential distribution. The average time in each RTS state can be expressed as, $\bar{\tau} = \sum_{n=1}^{N} t_n \left|F_n\right| \Big/ \sum_{n=1}^{N} \left|F_n\right|$ [47]. Here, n denotes the number of bins, t_n is the time span of each bin, and F_n is the total number of switching events in one bin.

Average capture time $\bar{\tau}_c$ and emission time $\bar{\tau}_e$ are plotted in Fig. 4.4 for P_{661} and P_{662} as a function of V_{GS} before stressing. Figures 4.5 and 4.6 depict $\bar{\tau}_c$ and $\bar{\tau}_e$ versus the stressing time t_s . Average capture time $\bar{\tau}_c$ can be expressed as, $\bar{\tau}_c = 1/p\sigma\bar{v}_{th}$ [47], where p is the inversion layer hole density per unit volume, σ is the capture cross-section, and $\bar{v}_{th}$ is the average hole velocity in the channel. Due to negative V_{TH} shift with t_s , the magnitude of ψ_s reduces and leads to lower p values with increasing stressing time. However, this lowering of p alone cannot explain the behavior of observed $\bar{\tau}_c$ for the traps, especially S_{662} and S_{663}. The impact of σ is significant in explaining $\bar{\tau}_c$ change with t_s observed for S_{662} and S_{663}

(Fig. 4.5). The capture times show a decrease with stressing in stress-induced traps while no such dependence is observed for the process-induced ones. This matter is discussed further in the next subsection while studying the effect of stressing on capture cross-section in detail. It is to be noted that trap position z_T is not affected significantly with change of t_s for any of the traps (Fig. 4.7). This is to be expected, since the trapping center, i.e., the defect, does not move with stress. In addition, it is quite possible for traps with different z_T to have similar emission times, like S_{662} and S_{663} do, (Figs. 4.6 and 4.7), since $\overline{\tau}_e$ depends not only on the position of the trap but also on the trap capture cross-section σ and the trap energy E_T. This is defined by the modified Shockley-Read-Hall statistics [12],

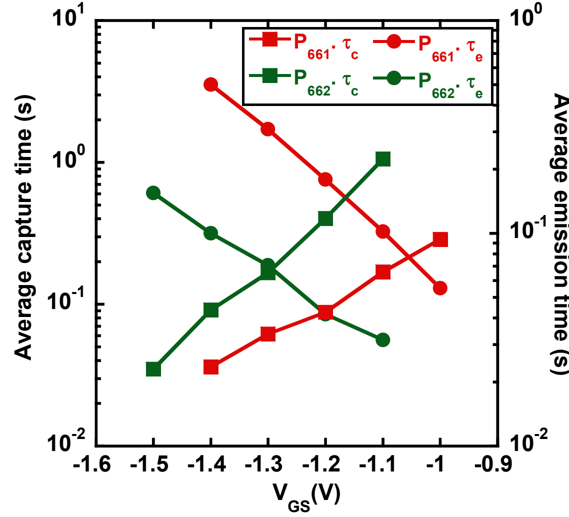


Fig. 4. 4 Average capture time $\overline{\tau}_c$ and emission time $\overline{\tau}_e$ as a function of gate to source voltage for two of the process-induced traps P_{661} and P_{662} present in the fresh device.

$$\overline{\tau}_e = \frac{1}{g\sigma p\overline{v}_{th}} e^{(E_T - E_F)/k_B T} \tag{4.3}$$

where p is the inversion layer hole density per unit volume, $\overline{v}_{th}$ is the average hole velocity of the channel, trap degeneracy $g = 1$, E_T is the trap energy level, and E_F is the hole Fermi level.

4.4 Effect of Stressing on Trap Capture Cross-section

Capture cross-section σ of the trap is related to the capture activation energy and temperature as, $\sigma = \sigma_0 e^{-\Delta E_B / k_B T}$ [12]. It represents the area around the trap within which the trap can capture a hole. Here,

σ_0 is the capture cross-section pre-factor and ΔE_B is capture activation energy. We have calculated the capture cross section σ from the measured $\overline{\tau}_c$ using [12],

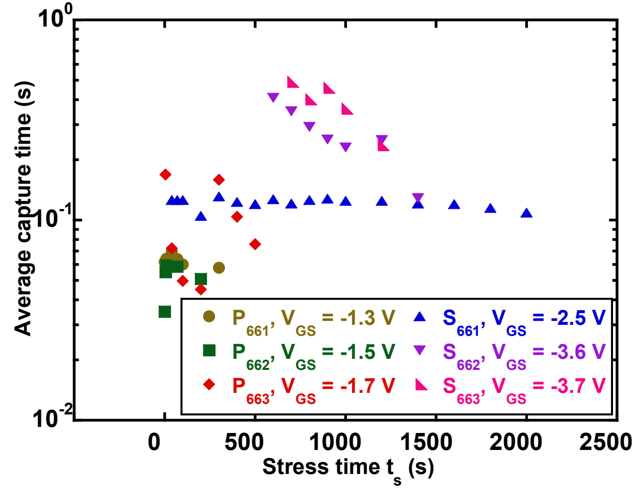


Fig. 4. 5 Average capture time $\overline{\tau}_c$ as function of stress time t_s for all the traps. $\overline{\tau}_c$ is observed to be decreasing with stressing for two of the stress-induced traps S_{662} and S_{663}.

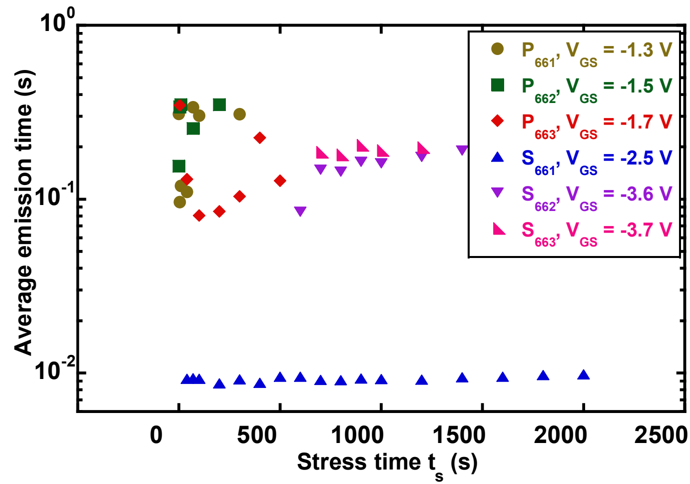


Fig. 4. 6 Average emission time $\overline{\tau}_e$ as a function of stress time t_s for all the traps. It is not changing significantly with stressing for the traps.

$$\sigma = \frac{1}{\bar{\tau}_c p \bar{v}_{th}} \tag{4.4}$$

Here, $p = p_0 e^{-q\psi_s/k_B T}$ [86], where p_0 is the equilibrium hole concentration. Average hole velocity can be computed from $\bar{v}_{th} = \left(8k_B T/\pi m_p^*\right)^{1/2}$ [12], where m_p^* is the effective mass of the hole. In Fig. 4.8, σ is shown as function of t_s at a fixed V_{GS} for the process and stress-induced traps.

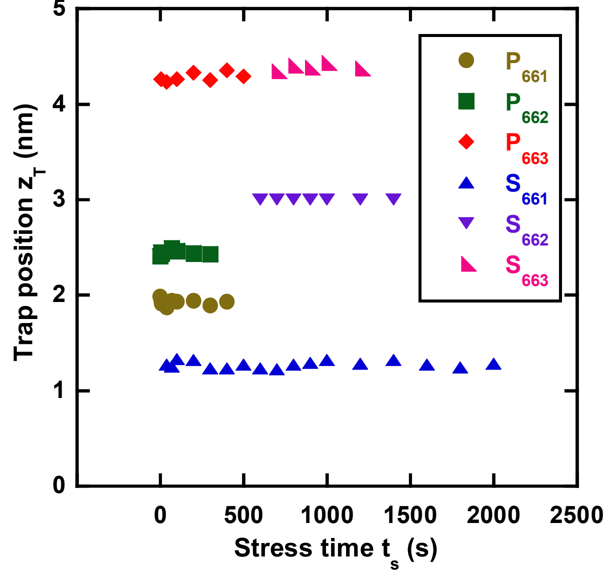


Fig. 4. 7 Position of the traps from the Si-SiO$_2$ interface as function of stress time t_s. Stressing does not affect the trap positions significantly. No distinction between the process and stress-induced traps are observed while comparing their positions from the Si-SiO$_2$ interface.

The capture cross-section increases with stressing time for the stress-induced traps (Fig. 4.8), while no such dependence is observed for the process-induced ones. As expressed in Eqn. 4.4, capture time is inversely proportional to the capture cross-section, which is the area around the trap within which the trap can capture a hole. The capture cross-section can be expressed in terms of the capture cross-section pre-factor σ_0 and is an exponential function of the barrier energy, ΔE_B, that the hole faces for being captured by the trap: $\sigma = \sigma_0 e^{-\Delta E_B/k_B T}$ [12]. The capture cross-section pre-factor σ_0 is inversely proportional to the relaxation energy E_R [92]. When a hole gets trapped in a defect site, it emits several phonons to get to the trap energy level E_T, and the emitted phonon energy corresponds to E_R, the relaxation energy of the defect and the surrounding atomic configuration that make up the trapping site [46], [47]. The decrease of $\bar{\tau}_c$, and the corresponding increase of σ with t_s imply that the structural relaxation the trapping site experiences

upon hole capture is diminished with stress. Variable temperature RTS measurements discussed in the next chapter shed light into this phenomenon.

4.5 Effect of Stressing on Screened Scattering Coefficients

Screened scattering coefficient α_m for the traps is calculated from the RTS measurements using [47],

$$\left|\frac{\Delta V_{DS}}{V_{DS}}\right| = \frac{1}{WL}\left(\frac{1}{P_{inv}} \pm \alpha_m \mu\right) \tag{4.5}$$

Here, μ is the effective mobility of the hole in the channel, P_{inv} is the inversion layer charge density per unit area obtained in C-V measurements, W is the channel width, L is the channel length, and ΔV_{DS} is the RTS amplitude.

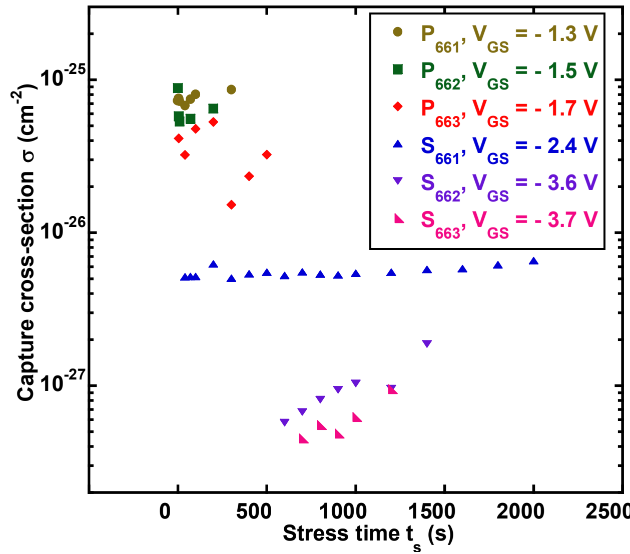


Fig. 4. 8 Capture cross section σ with respect to stress time t_s for all the traps. Its increase is observed with stressing specifically for S_{662} and S_{663}.

Number and mobility fluctuations are represented by the right-hand side terms of Eqn. 4.5. The addition or subtraction sign between these fluctuation components depends on whether the trap is a repulsive or an attractive center, respectively [47]. All the traps presented in the reported device here were found to be attractive centers. Experimentally found and theoretically calculated screened scattering coefficients α_m and α_t are represented in Fig. 4.9 as a function of P_{inv} for all the traps at different stressing times. Increasing inversion carrier density leads to more charge screening between the trapped charge and the channel carriers, leading to reduced α_m.

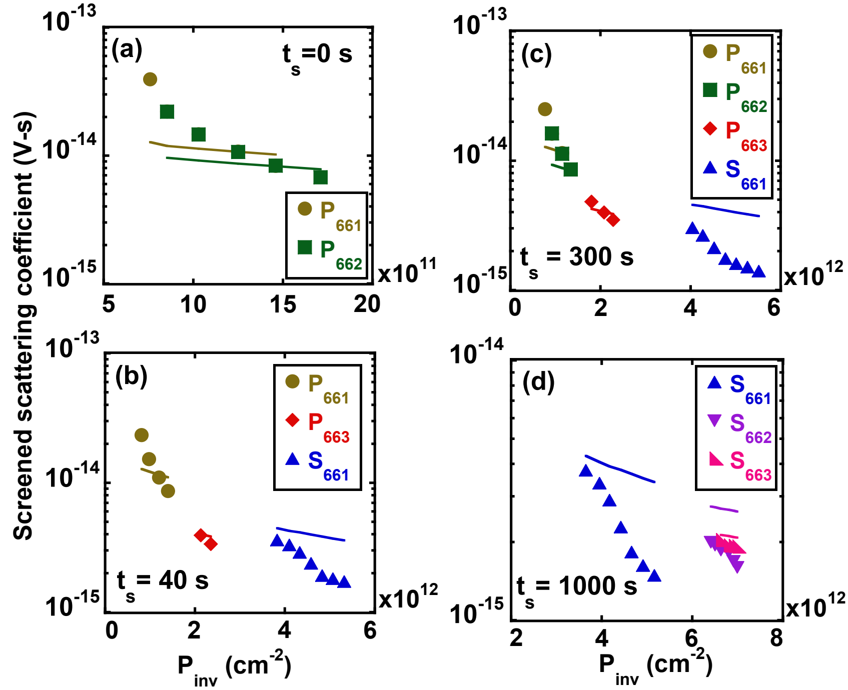


Fig. 4. 9 Screened scattering coefficient from our measurements α_m and from our theoretical modelling α_t with respect to inversion layer charge density P_{inv} for different traps at different stressing times (a) 0 s, (b) 40 s, (c) 300 s, and (d) 1000 s. Symbols and solid lines with the same color correspond to α_m (measured) and α_t (theoretical) for the same trap, respectively.

In Fig. 4.10, α_m and α_t are plotted for the process-induced and stress-induced traps as a function of t_s. The shift in V_{TH} with t_s indicates the generation of an increased amount of fixed positive oxide charge Q_f [34], [39], [93]. Fixed positive oxide charges Q_f are in near proximity to the Si-SiO_2 interface [94], [95], [96]. These additional Q_f charges with more CHC stressing lead to a higher amount of screening on the traps alongside P_{inv}. For the process-induced traps, there is a negligible reduction of α_m with stressing [Fig. 4.10(a)]. On the contrary, α_m decreases specifically with t_s for the stress-induced traps S_{662} and S_{663} [Fig. 4.10(b)].

4.5.1 Modeling Quantization Effects on Screened Scattering Coefficients

As the device size is downscaled, the channel doping concentration is increased to prevent the punch-through effect and premature turn on of the devices [19]. In high doping density devices with dimensions scaled down, carrier motion is quantized in the perpendicular direction to the Si-SiO_2 interface [20], [21],

[22]. Therefore, the two-dimensional quantum mechanical treatments are carried out for the small-scale devices in contrast to the classical three-dimensional treatments. The two-dimensional mobility fluctuations model was successfully implemented to calculate the mobility limited by the oxide charge scattering for nMOSFETs [22]. Screened Coulomb scattering coefficients have been calculated from this model for both the interface and oxide traps in nMOSFETs [21], [22].

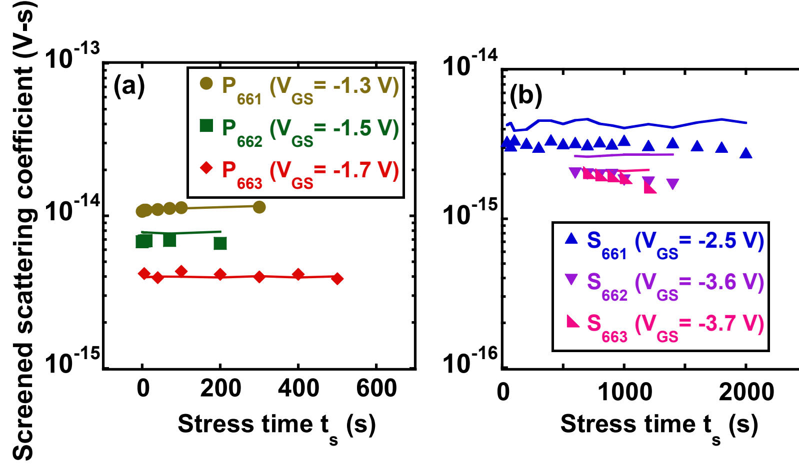


Fig. 4. 10 Screened scattering coefficient from measurements and theoretical modelling with respect to stressing time t_s for (a) process-induced; (b) stress-induced traps. Symbols: α_m (measured) , solid lines: α_t (theoretical).

Two-dimensional quantum mechanical treatment is carried out here for investigating the screened Coulomb scattering. Two important effects of quantization on pMOSFETs are (a) valence band splitting and (b) modified valence band carrier distribution $p_v(z)$ [22].

The inversion layer electric field of the pMOSFET creates a quantum potential well. As the width of the well is smaller than the channel carrier wavelength, the valence band is quantized into discrete electric sub-bands. In this case, the hole is thought to be present at the first quantized energy level sub-band, below the valence band maximum at Γ point. The hole density for the two-dimensional case is, $p_{2D} = \int g(E)_{2D} f_p(E) dE$. Here, $g(E)_{2D}$ is the two-dimensional density of states and $f_p(E)$ is the Fermi-Dirac hole distribution function. The number of holes per unit area in a two-dimensional system is,

$$p_{2D} = \left(\frac{m_d^* k_B T}{\pi \hbar^2} \right) \left\{ \ln \left(1 + e^{(E_0 - E_F)/k_B T} \right) \right\} \tag{4.6}$$

Here, m_d^* is the density of states effective mass of hole, $\hbar$ is the reduced Planck's constant, and E_0 is the first allowed quantized energy level of the Si valence band.

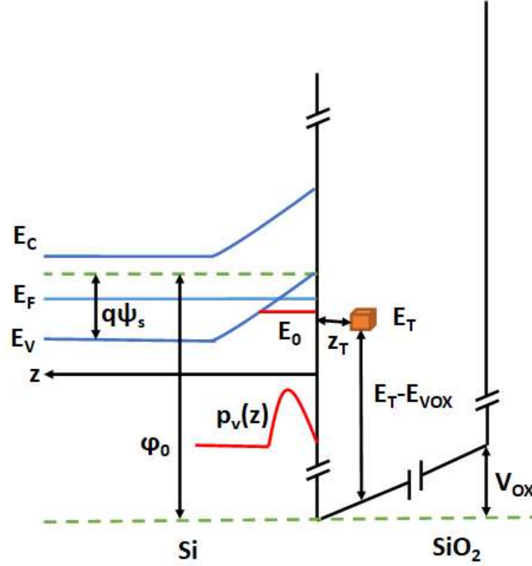


Fig. 4. 11 Band diagram of the pMOSFET at the source end of the channel.

In the classical two-dimensional case of the carrier distribution, density of the carrier is considered to be the highest at the Si-SiO_2 interface [19], [20]. However, in the quantum mechanical two-dimensional case, the charge centroid is shifted towards the bulk (Fig. 4.11) [21], [22]. Taking the modified valence band charge carrier distribution $p_v(z)$ per unit length along the perpendicular direction to the Si-SiO_2 interface (z direction), the inversion layer charge density per unit area can be expressed as, $P_{inv} = \int p_{2D} p_v(z) dz$ [21], [22]. The charge carrier distribution $p_v(z)$ (Fig. 4.11) for the quantum mechanical two-dimensional case is determined from the Stern-Howard wave-function $\zeta(z)$. Under the assumption that the lowest energy sub-band has all the carriers, the Stern-Howard wave-function is represented by a trial function $\zeta(z) = \left(b^{3/2}/\sqrt{2}\right) z e^{-bz/2}$ [19], [97], [98], [99]. Here, b is known as the variation parameter. The total energy in the quantized sub-band level E_0 is the summation of the expectation values of the hole kinetic energy, hole potential energy resulting from interaction with inversion and depletion region holes, and image potential [98]. All these energy components are functions of b [98]. As a result, following the maximization of E_0 (the first allowed quantized energy level) , the variation parameter b is expressed as [19], [22], [98],

$$b = \left\{ \frac{12qm_z^*}{\hbar^2 \varepsilon_{Si} \varepsilon_0} \left[Q_D + (11/32) Q_{inv} \right] \right\}^{1/3} \tag{4.7}$$

Here, m_z^* is the hole quantized effective mass in z direction, ε_{Si} is the dielectric constant of Si, ε_0 is the permittivity of free space, Q_D is the total depletion layer charge, and Q_{inv} is the total inversion layer charge. Stern-Howard wave-function is used to compute the location of the charge centroid to be $3/b$ away from the Si-SiO$_2$ interface [21], [22]. The integration of the probability function is carried out as [22],

$$\int_0^{\bar{z}} p_v(z)dz = \frac{b^3}{2}\int_0^{\bar{z}} z^2 e^{-bz} dz = 0.58 \tag{4.8}$$

Then, using Eqn. 4.6 and 4.8, the inversion layer charge carrier density for the two-dimensional quantum mechanical case can be expressed as,

$$P_{inv} = \left(\frac{m_d^* k_B T}{\pi \hbar^2}\right)\left\{\ln\left(1+e^{(E_{VS}-\Delta E_0 - E_F)/k_B T}\right)\right\} \times 0.58 \tag{4.9}$$

Here, $\Delta E_0 = E_{VS} - E_0$ is the energy difference between the valence band maximum and the first allowed quantized level for holes. P_{inv} can be expressed for the heavy hole and light hole cases individually as,

$$P_{invhh} = \left(\frac{m_{dhh}^* k_B T}{\pi \hbar^2}\right)\left\{\ln\left(1+e^{(E_{VS}-\Delta E_{0hh} - E_F)/k_B T}\right)\right\} \times 0.58 \tag{4.10}$$

$$P_{invlh} = \left(\frac{m_{dlh}^* k_B T}{\pi \hbar^2}\right)\left\{\ln\left(1+e^{(E_{VS}-\Delta E_{0lh} - E_F)/k_B T}\right)\right\} \times 0.58 \tag{4.11}$$

Here, m_{dhh}^* is the density of states effective mass of heavy hole, m_{dlh}^* is the density of states effective mass of light hole, ΔE_{0hh} and ΔE_{0lh} are the first allowed quantized energy levels for the heavy and light hole bands, respectively, with respect to the valence band maximum E_{VS}. P_{invhh} and P_{invlh} are calculated using the occupation factor plot as a function of the surface electric field F_s [100], defined as, $F_s = (Q_D + Q_{inv})/\varepsilon_{Si}\varepsilon_0$ [100]. Once the shift of the energy level for the heavy hole case ΔE_{0hh} and light hole case ΔE_{0lh} is calculated from Eqn. 4.10 and 4.11, the value for the wave-vector of the plane wave κ for the carriers can be computed by taking the parabolic approximation of the energy bands for heavy and light holes as,

$$\Delta E_{0hh} = \frac{\hbar^2 \kappa_{hh}^2}{2m_{dhh}^*} \quad and \quad \Delta E_{0lh} = \frac{\hbar^2 \kappa_{lh}^2}{2m_{dlh}^*} \tag{4.12}$$

In our theoretical modeling, ΔE_0 values are not calculated using the conventional triangular potential well approximation [19], [21]. The triangular potential well approximation does not work well for the strong inversion region [99], [101], and the surface electric field used in calculating the sub-band energy level

needs to be replaced by an effective electric field [102]. A weighting coefficient needs to be properly chosen to make the triangular approximation work [102]. Therefore, as mentioned above, we determined ΔE_{0hh} and ΔE_{0lh} values from Eqns. 4.10 and 4.11. In the next subsection, these calculated wave-vectors κ_{hh} and κ_{lh} (for heavy and light holes, respectively) from Eqn. 4.12 lead to the determination of α_t for the heavy and light holes.

4.5.2 Two-dimensional Mobility Fluctuations Model for pMOSFET

The two-dimensional mobility fluctuations model provides an understanding for the underlying physical mechanisms behind the screened Coulomb scattering between the inversion layer charge carriers and the trapped charge [18]. Mobility limited by the oxide charge scattering can be represented by the two-dimensional mobility fluctuation model as [21], [22],

$$\mu_t^{-1} = \frac{m^* q^3}{8\hbar\pi\varepsilon_{av}^2 E_p} \int_0^{\pi/2} \frac{\sin^2\phi}{\left(\sin\phi + \left(c/2\kappa\right)\right)^2} e^{-4\kappa z_T \sin\phi} d\phi P_t \tag{4.13}$$

Here, m^* is the conductivity effective mass of hole, ε_{av} is the average dielectric constant of Si and SiO_2, κ is the magnitude of the plane wave state, 2ϕ is the angle between initial plane wave state κ and final plane wave state κ', P_t is the number of oxide traps per unit area, and c is a parameter representing screening effects by the inversion layer holes. E_p is the energy where $Eg\left(E\right)_{2D} f_p\left(E\right)$ peaks. Screening parameter c is represented as [18], [22], [103],

$$c = \frac{2q^2 m^* d_v}{4\hbar^2 \pi\varepsilon_{Si}} \left(1 - e^{-\pi\hbar^2 P_{inv}/k_B T m^* d_v}\right) \tag{4.14}$$

Here, d_v is the valley degeneracy factor of hole. The screened scattering coefficient for the heavy holes and light holes can be expressed separately according to Eqn. 4.13 as,

$$\alpha_{thh} = \frac{m_{hh}^* q^3}{8\hbar\pi\varepsilon_{av}^2 E_p} \int_0^{\pi/2} \frac{\sin^2\phi}{\left(\sin\phi + \left(c_{hh}/2\kappa_{hh}\right)\right)^2} e^{-4\kappa_{hh} z_T \sin\phi} d\phi \tag{4.15}$$

$$\alpha_{tlh} = \frac{m_{lh}^* q^3}{8\hbar\pi\varepsilon_{av}^2 E_p} \int_0^{\pi/2} \frac{\sin^2\phi}{\left(\sin\phi + \left(c_{lh}/2\kappa_{lh}\right)\right)^2} e^{-4\kappa_{lh} z_T \sin\phi} d\phi \tag{4.16}$$

Here, m_{hh}^* and m_{lh}^* are the conductivity effective mass of heavy and light holes, respectively. κ_{hh} and κ_{lh} can be calculated from Eqn. 4.12. The screening parameters for these two cases are computed from,

$$c_{hh} = \frac{2q^2 m_{hh}^* d_v}{4\hbar^2 \pi \varepsilon_{Si}} \left(1 - e^{-\pi\hbar^2 P_{invhh} / k_B T m_{hh}^* d_v}\right) \tag{4.17}$$

$$c_{lh} = \frac{2q^2 m_{lh}^* d_v}{4\hbar^2 \pi \varepsilon_{Si}} \left(1 - e^{-\pi\hbar^2 P_{invlh} / k_B T m_{lh}^* d_v}\right) \tag{4.18}$$

Finally, the total theoretical Coulomb screened scattering coefficient is calculated adding Eqn. 4.15 and 4.16,

$$\alpha_t = \alpha_{thh} + \alpha_{tlh} \tag{4.19}$$

It should be noted that, according to Eqn. 4.15 and 4.16, both α_{thh} and α_{tlh} have an exponential dependence on z_T, which is extracted from the measured RTS data and therefore comes with experimental fluctuations with respect to stressing time. These fluctuations are amplified in the exponential form, and lead to a wavy line in the computed α_t with respect to t_s in Fig. 4.10 (b).

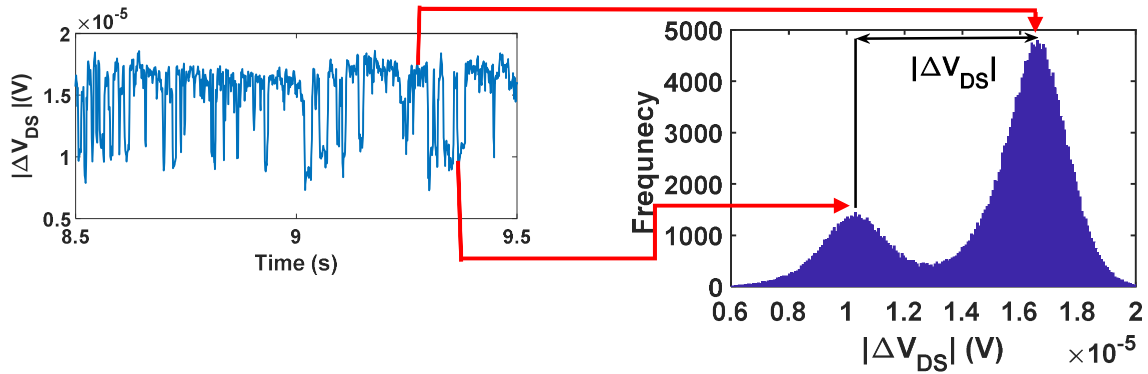


Fig. 4. 12 Determination of RTS amplitude $|\Delta V_{DS}|$ from the Gaussian peaks of a two level RTS. Here, the two level RTS corresponds to a stress-induced trap S_{661}, recorded at V_{GS} = -2.7 V after 200 s of stressing.

In the two-dimensional theoretical modeling, screening is taken to be only dependent on P_{inv} and z_T. The effect of the generated fixed positive oxide charge Q_f with t_s is not considered. However, the V_{TH} shift with t_s confirms the generation of Q_f [34], [39], [93]. Although Q_f is in close proximity to the Si-SiO$_2$ interface [94], [95], [96], the exact position of Q_f cannot be determined from our RTS measurements. Q_f is not considered in the theoretical modeling since the quantification of the exact amount and position of Q_f is not possible from the RTS measurements. However, the increased amount of Q_f with t_s can be considered as the determining factor behind the differences between α_m and α_t.

4.6 Effect of Stressing on RTS Amplitude

Difference of the Gaussian peaks of the amplitude histogram from RTS data defines the experimentally obtained RTS amplitude [45], [47], [89]. Gaussian distributions corresponding to the upper and lower levels of a two level RTS are shown here in Fig. 4.12. The difference between the Gaussian peaks of these levels is expressed as RTS amplitude $|\Delta V_{DS}|$. In Fig. 4.13(a) and 4.13(b), RTS amplitude is represented separately

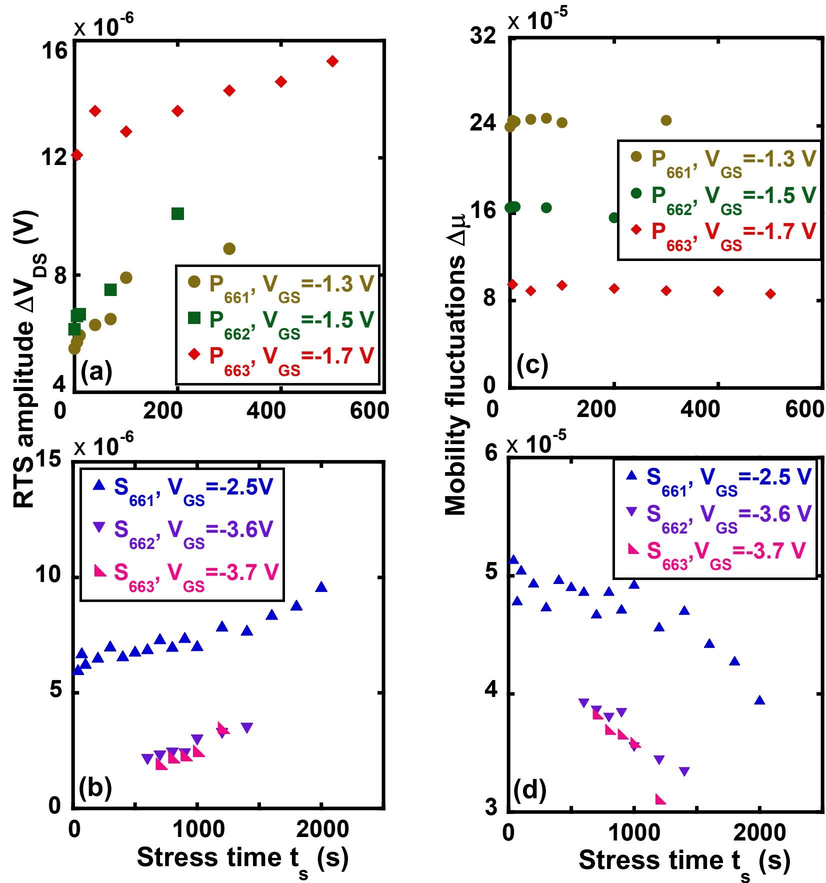


Fig. 4. 13 RTS amplitude ΔV_{DS} with respect to stress time t_s for (a) process-induced; (b) stress-induced traps. Mobility fluctuations $\Delta\mu$ with respect to stress time t_s for (c) process-induced; (d) stress-induced traps.

for the process-induced and stress-induced traps as a function of t_s. It is observed that the RTS amplitude is increasing with t_s for all the process-induced and stress-induced traps. With the increment of t_s, the generation of more positive fixed oxide charges leads to V_{TH} shift (increase of V_{TH} magnitude with t_s). Consequently, P_{inv} reduces and results in a higher number fluctuations with t_s at a fixed V_{GS}. On the other hand, mobility fluctuations decreases with t_s due to the decrease of α_m [Fig. 4.13(c) and 4.13(d)]. The

relative change of mobility fluctuations compared to number fluctuations leads to increasing RTS amplitude with t_s .

In this chapter, the effect of CHC stressing on different RTS trap parameters have been discussed. The two-dimensional mobility fluctuations model is successfully implemented for pMOSFETs in the case of CHC stressing and RTS. The positive fixed oxide charge generated due to stressing plays a consequential role in additional screening of the channel carriers from scattering by the oxide traps and therefore leads to lower mobility fluctuations. This in turn increases the overall RTS amplitude with stressing time for the case of hole-attractive trapping centers in SiO_2. The negative threshold voltage shift due to fixed oxide charge generation also leads to the reduction of the trap relaxation energy, which increases the trap capture cross-section by increasing the cross-section pre-factor. As the trap capture cross-section is impacted due to stress, this factor leads to the decrease of the average capture time for the defects. The identification of the defect centers responsible to act as the process-induced and stress-induced traps is not possible without some additional evaluation of the RTS trap parameters in the variable temperature measurements. In the next chapter, variable temperature RTS measurements are discussed to identify the defect centers under CHC stressing.

Chapter 5: Identification of Channel Hot-Carrier Stress-Induced Oxide Traps in pMOSFETs

Besides the presence of oxide defects in pristine MOSFETs, different types of electrical stressing mechanisms have been reported to generate additional SiO_2 defects [104], [105], [106]. Identification of these defects is necessary as they are responsible for the degradation of different DC parameters in a MOSFET. Random telegraph signals (RTS) involve multi-phonon assisted tunneling of the channel carriers into the defect sites present at the Si- oxide interface or inside the gate oxide in MOSFETs [17], [107]. Therefore, RTS measurements and analyses can be implemented to probe into these process- and stress-induced oxide defects for identification through experimental quantification of the carrier capture and emission activation energies, structural relaxation in the oxide network due to trapping/ detrapping, and entropy change as well as the energy level and position of the trap in the oxide.

In the previous chapter, the effect of channel hot carrier (CHC) stressing was studied on different trap parameters, i.e., capture time, capture cross-section, RTS amplitude and screened scattering coefficients in pMOSFETs. However, the physical reasons behind the structural relaxation and its impact on capture time and capture cross-section could not be explained without evaluating thermal activation processes related to capture and emission of carriers by the traps. Variable temperature RTS measurements are required for this purpose, and for identification of the CHC-stress-created oxide hole defect centers in pMOSFETs.

In this chapter, emphasis is given to study the impact of CHC stressing on the process- and stress-induced traps by examining the temperature-dependent RTS parameters. Hole capture and emission activation energies are measured and analyzed, corresponding to the emission and capture of a valence band (VB) electron, respectively, by the oxide trap. Change in the system entropy, as well as the energy associated with structural relaxation around the defect upon hole emission (electron capture from VB) are quantified, resulting in identification of the stress-induced traps with energies in the proximity of the silicon VB edge. Physical reasons behind the differences in these parameters between the process- and stress-induced traps are explored.

Results of this work have been reported in IEEE Transactions on Electron Devices [108].

5.1 RTS Measurement Technique

During a typical measurement cycle, at first DC I-V characteristics were recorded with a semiconductor parameter analyzer (SPA) at room temperature, from which threshold voltage V_{TH} and channel conductance

g_d were extracted. Subsequently, RTS measurements were performed inside a room shielded to protect the pMOSFET from external interference [62]. A DC power source operated by a battery stack was employed to bias the device in the linear region by adjusting the gate-source voltage V_{GS} and drain-source voltage V_{DS}. RTS switching ΔV_{DS} was recorded in the time domain with an oscilloscope connected to the pMOSFET's drain and source terminals through a low-noise preamplifier.

The devices were scanned for RTS in V_{GS} from -1 to -4 V at a fixed V_{DS} of -0.2 V. The sampling frequency and total time span of the recorded RTS data in the oscilloscope were chosen to ensure at least 800 transitional switching events between two consecutive levels [46], [47], [62]. A precision impedance analyzer was used to obtain C-V data and compute T_{OX}, the gate SiO_2 layer thickness and P_{inv}, Si inversion layer charge density per unit area [45], [89].

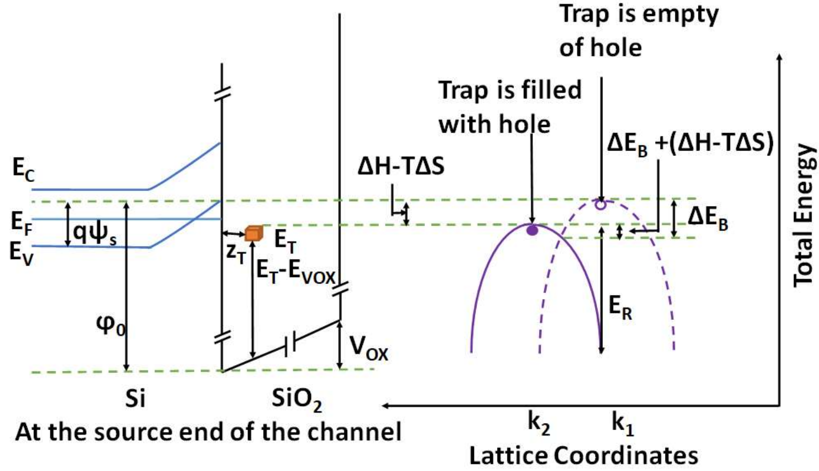


Fig. 5. 1 Configuration co-ordinate and energy band diagram of the pMOSFET.

All equipment operated by DC were protected inside the shielded room from outside interference, whereas AC-operated ones like the impedance analyzer, oscilloscope, semiconductor parameter analyzer (SPA), and temperature controller were placed outside. A passive, continuous-flow liquid nitrogen cryogenic system placed inside the shielded room allowed the precise control of the device temperature, down to 78 K. Detailed information on the measurement set-up can be found in chapter 2. I-V, C-V, and RTS measurements were repeated down to 215 K, where the RTS switching became too slow to obtain a statistically meaningful number of transitions.

Once the variable-temperature measurements were completed on the fresh device, the pMOSFET was allowed to warm up to room temperature. The stressing was done at $V_{GS} = V_{DS} = -6\,V$. Again, I-V, C-V, and RTS were recorded at room and cryogenic temperatures. Variable time intervals of 100 to 300 seconds were chosen to perform CHC stressing on the devices up to 1200 seconds.

In total, seven pMOSFETs were studied. As a representative for all, here we report on the results from four devices of the same channel width and length with a gate area less than 0.3 μm^2. It was experimentally observed that one process- and one stress-induced trap is present in each of the four pMOSFETs, allowing us to compare the defect properties under CHC.

5.2 RTS Analyses Procedures and Results

Capture and emission of the channel carriers by SiO_2 defects are governed by a multi-phonon assisted tunneling process [12]. The energy band and configuration co-ordinate diagram are represented in Fig. 5.1 for a pMOSFET. Here, E_V and E_C are the valence and conduction band edge of Si, respectively. E_F is the Si Fermi energy level, ψ_s is the surface potential, φ_0 is the energy level difference between the Si and SiO_2 valence band edges at the interface, z_T is the position of the trap inside SiO_2 from the Si-SiO_2 interface, E_T is the trap energy level, and $E_{V_{OX}}$ is the SiO_2 VB edge. The channel hole overcomes an energy barrier ΔE_B to get captured by the trap with a phonon interaction energy corresponding to the generalized lattice coordinate change from k_1 to k_2 (Fig. 5.1). The difference in energy between the capture and emission process is defined as Gibbs free energy $\Delta H - T\Delta S$, comprised of the enthalpy change, ΔH and the entropy change, ΔS. The associated structural relaxation of the oxide lattice caused by hole trapping, as described by the generalized lattice coordinate change from k_1 to k_2, is represented by the relaxation energy E_R [12], [46], [47]. Trap position z_T, trap energy level with respect to the SiO_2 VB edge $\left(E_T - E_{V_{OX}}\right)$ as well as the aforementioned energy parameters are summarized in Table 5.1.

Table 5. 1: Extracted trap properties

Trap	Temperature (K)	Stress time t_s (s)	z_T (nm)	$E_T - E_{V_{OX}}$ (eV)	ΔE_B (eV)	ΔH (eV)	$\Delta S/k_B$	E_R (eV)
P_{61}	255-295	0-300	0.86±0.01	4.67	0.35-0.43	0.13-0.27	6.68-12.4	1.47-1.80
S_{61}	235-295	300-1200	0.41±0.02	4.76	0.51-0.58	0.02-0.07	3.39-5.18	2.18-2.43
P_{62}	275-295	0-100	1.64±0.02	4.62	0.49-0.54	0.17-0.22	10.03-11.74	2.08-2.31
S_{62}	215-295	300-800	1.43±0.03	4.63	0.26-0.30	0.05-0.11	3.42-5.26	1.01-1.26
P_{63}	255-295	0-300	0.66±0.02	4.67	0.42-0.50	0.10-0.17	6.99-10.11	1.84-2.13
S_{63}	225-295	500-1200	0.85±0.03	4.76	0.25-0.32	0.08-0.17	1.39-5.94	0.89-1.16
P_{64}	250-295	0-300	0.69±0.01	4.67	0.46-0.53	0.07-0.16	6.14-10.35	2.03-2.24
S_{64}	250-295	500-1000	1.07±0.02	4.70	0.39-0.49	0.05-0.15	2.28-4.51	1.45-1.95

The first subscript denotes the width of the device and the second identifies the pMOSFET. *For P_{61}, S_{61}, P_{62}, S_{62}, P_{63}, S_{63}, P_{64} and S_{64}, trap energy level is evaluated at V_{GS} = -1.7, -3, -3, -1.7, -2, -1.5, -2 and -1.5 V, respectively. Here, V_{DS} =-0.2 V.

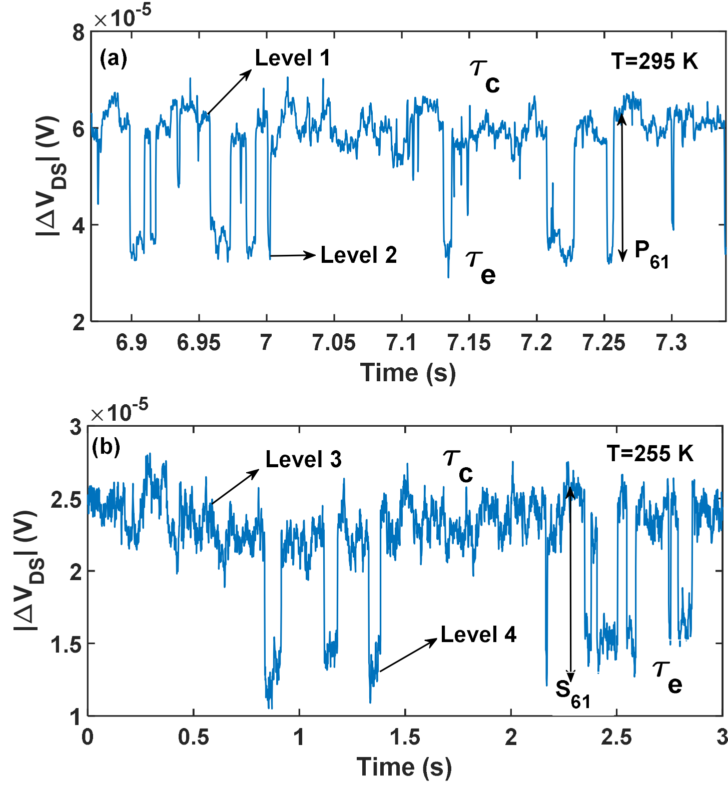


Fig. 5. 2 Two level RTS observed in pMOS1. (a) Transition from level 1 to 2 represents the process-induced trap P_{61} at V_{GS} = -1.65 V under fresh condition at T =295 K, (b) transition from level 3 to 4 denotes the presence of the stress-induced trap S_{61} at V_{GS} = -2.7 V after 300 seconds of stressing at T =255 K.

Recorded sample RTS traces are shown in Figs. 5.2 and 5.3. The average time spent at each level was computed through the statistical analysis described in [47]. Since the ratio of the average capture time $\overline{\tau}_c$ to average emission time $\overline{\tau}_e$ is, $\overline{\tau}_c/\overline{\tau}_e = (1-f_h)/f_h$, where f_h is the hole occupancy function for the trap, the capture to emission time ratio should decrease with increasing $|V_{GS}|$ [47]. Based on the V_{GS} dependence of the $\overline{\tau}_c/\overline{\tau}_e$ ratio, the higher level was identified as the capture time, while lower level was the emission time. Thus, all measured traps were attractive (acceptor-type), indicated by the high state corresponding to the trap being negatively charged when empty of a hole (full of an electron) and low state being the trap getting neutralized by capturing a hole (equivalent to emitting an electron to the Si VB). A detailed explanation of this identification method is provided in [47], and not repeated here.

5.2.1 Trap Position and Energy Level

Once the mean capture and emission times are computed for each bias condition, temperature and stressing interval, the trap position z_T is found by differentiating Eqn. 5.1 with respect to V_{GS}, using the $\overline{\tau}_c$ and $\overline{\tau}_e$ data [47], [73],

$$\ln\left(\frac{\overline{\tau}_c}{\overline{\tau}_e}\right) = -\frac{1}{k_B T}\left[\begin{array}{l}\left(E_T - E_{V_{OX}}\right) - \left(E_F - E_V\right) - \varphi_0 \\ +q\psi_s + q\dfrac{z_T}{T_{OX}}\left(V_{GS} - V_{FB} - \psi_s\right)\end{array}\right] \tag{5.1}$$

Here, k_B is the Boltzmann constant, T is the temperature, q is the elementary charge, and V_{FB} is the flat-band voltage. ψ_s is calculated by utilizing the Poisson's equation [46]. Results are summarized in Table 5.1 and plotted in Fig. 5.4 for the process (P)- and stress (S)-induced traps observed in four different

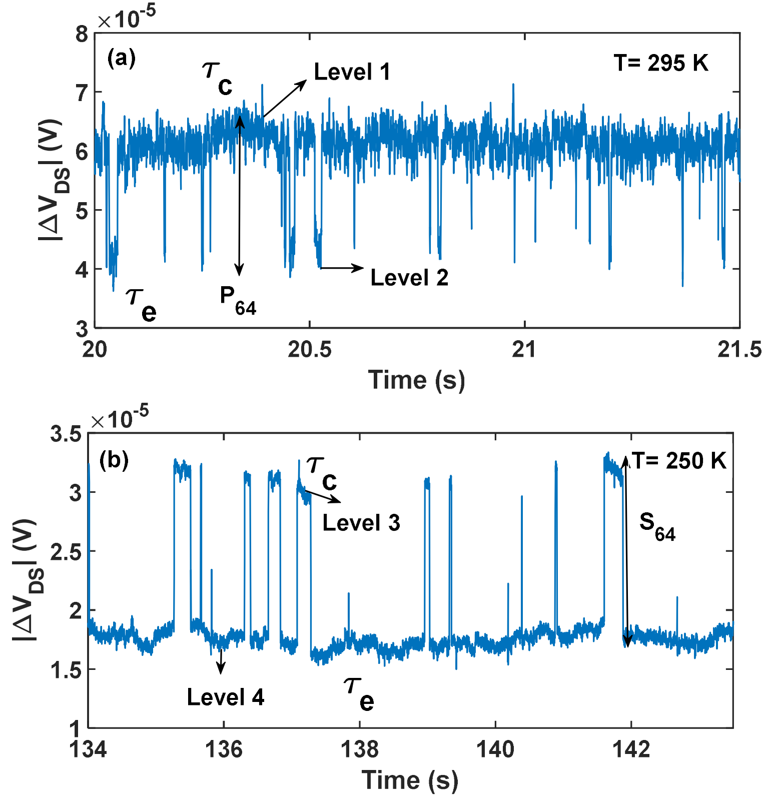


Fig. 5. 3 Two level RTS observed in pMOS4. (a) Transition from level 1 to 2 represents the process-induced trap P_{64} at V_{GS} = -1.9 V under fresh condition at T =295 K, (b) transition from level 3 to 4 denotes presence of the stress-induced trap S_{64} at V_{GS} = -1.5 V after 500 seconds of stressing at T =250 K.

pMOSFETs. Circle symbols indicate the process- and triangle symbols are used for the stress-induced traps for all figures. The position of the traps eliminates any possibility of a Pb center (dangling Si bond at the Si-SiO_2 interface) [90], [91]. In some of the earlier works, it was observed that the stress-induced traps are

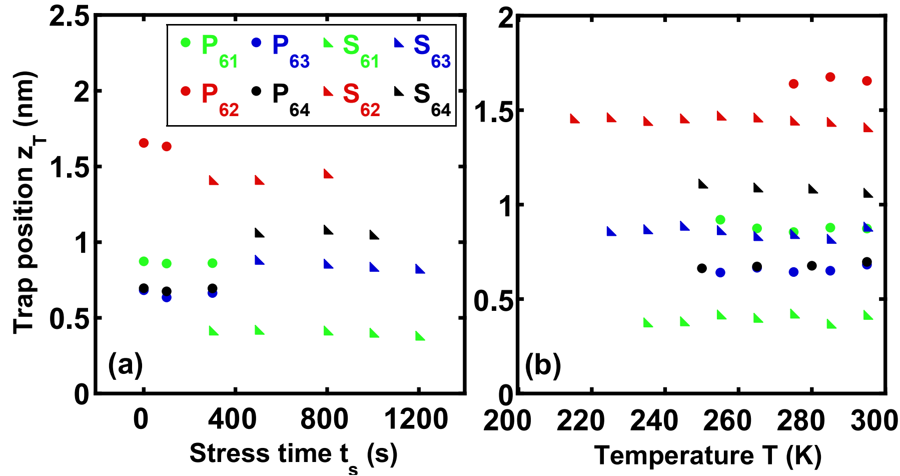


Fig. 5. 4 Trap position z_T as a function of the (a) stressing time t_s at T = 295 K, (b) temperature T for the process-induced traps (t_s = 0 s) and t_s = 300 s, 300 s, 500 s and 500 s for S_{61}, S_{62}, S_{63} and S_{64}, respectively. Circle symbols indicate the process-, whereas triangle symbols are for the stress-induced traps. The same convention is used for all the subsequent figures.

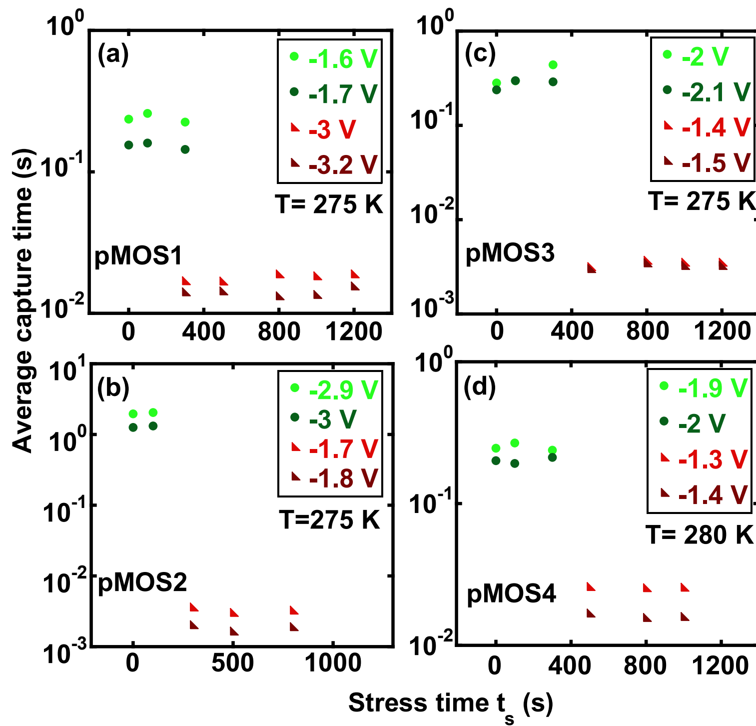


Fig. 5. 5 Average capture time $\overline{\tau}_c$ as a function of stressing time t_s for the representative V_{GS} values. Stress-induced traps are faster than their process-induced counterparts.

positioned closer to the Si-SiO_2 interface than the process-induced ones [40], [41]. However, here, no such correlation between the trap position and its origin exists (Table 5.1).

Once z_T is known, again utilizing Eqn. 5.1, and the measured capture and emission times, $\left(E_T - E_{V_{OX}}\right)$ are extracted. The values of 4.6-4.8 eV shown in Table 5.1 indicate that the trap energies are slightly below the Si valence band edge, facilitating the capture/emission of holes from the VB to the defect site inside SiO_2 by a multi-phonon assisted tunneling process.

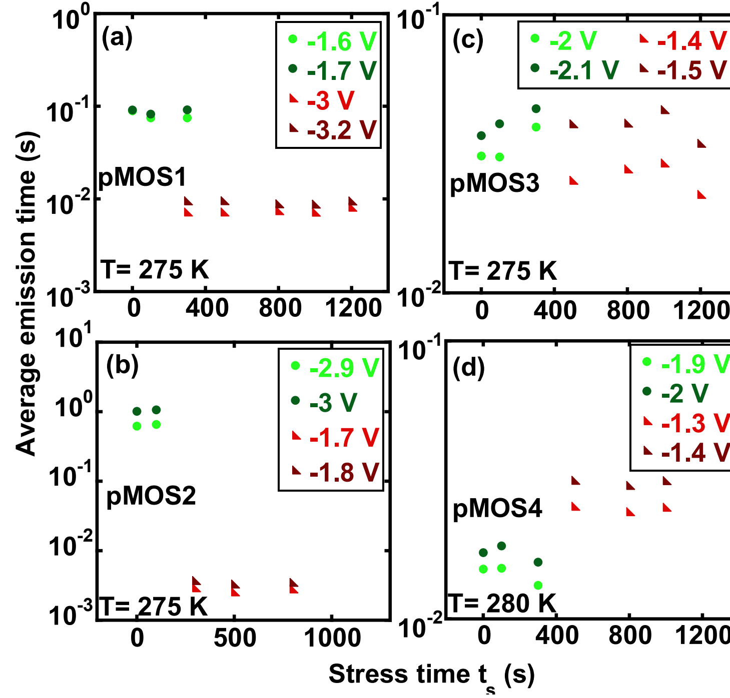


Fig. 5. 6 Average emission time $\overline{\tau}_e$ for representative V_{GS} values as a function of stressing time t_s.

As expected, stressing was not found to change the position or the energy of the trap. It should be noted that process-induced traps for pMOSFETs 3 and 4 have similar locations and trap energies. Although location is random, trap energy is one of the identifiers for the defect [46], [47].

5.2.2 Trap Time Constants and Capture Cross-Section

By examining $\overline{\tau}_c$ as a function of CHC stressing time t_s, it is observed that the stress-induced traps are faster than their process-induced counterparts in each device (Fig. 5.5). However, as the mean switching times and z_T are clearly not correlated with each other, elastic tunneling does not play a significant role. When compared to our previous work [88], the stress-induced traps here are two orders of magnitude faster in capturing holes ($\overline{\tau}_c \sim 10^{-3}$ s - 10^{-2} s) than the previously reported ones ($\overline{\tau}_c \sim 10^{-1}$ s - 10^{0} s), but only one order of magnitude faster in emitting them ($\overline{\tau}_e \sim 10^{-3}$ s - 10^{-2} s here compared to $\overline{\tau}_e \sim 10^{-1}$ s in [88]). This is shown in Fig. 5.6. At cryogenic temperatures, the switching slows down. Therefore, at low temperatures,

we cannot see the activity of the traps that were relatively slow to start with at T=295 K, since the number of RTS transitions becomes too small for a meaningful statistical analysis. Therefore, we are limited to relatively fast traps at room temperature to start with.

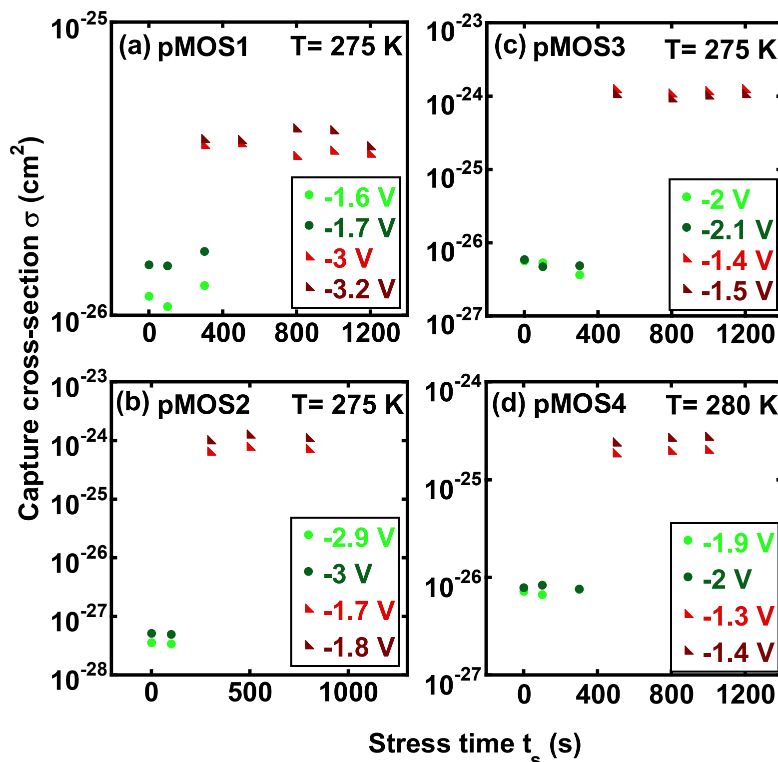


Fig. 5. 7 Capture cross-section σ reported as a function of stressing time t_s for representative V_{GS} values.

Faster capture times exhibited by the stress-induced traps are due to the larger trap capture cross-section σ, which denotes the area around the trap within which it can capture a hole. It is computed as, $\sigma = 1/\overline{\tau}_c p\overline{v}_{th}$ [12], where p is the inversion layer hole density per unit volume and $\overline{v}_{th}$ is the average hole velocity. Higher σ values are observed for the stress-induced traps than the process-induced ones as depicted in Fig. 5.7. Comparing these values of $\sigma \approx 10^{-24}$ cm^2 - 10^{-25} cm^2 with $\sigma \approx 10^{-27}$ cm^2 - 10^{-28} cm^2 reported for T=295 K only in [88] for the stress-induced traps, we believe the difference is due to the accessibility of the traps with our measurements. For its activity to be measurable by our technique, the probed trap has to be within $\sim \pm 3k_B T$ of the Fermi energy level. RTS method is unable to detect switching activities outside the range of $\overline{\tau}_c/\overline{\tau}_e = 0.1\text{-}10$ [47]. In addition, as we decrease the temperature, the energy range of accessible traps gets narrower. These limitations may be the reasons to have a different range of

σ for the stress-induced traps in the current and our previous works. It should be noted that none of these parameters ($\overline{\tau}_c$, $\overline{\tau}_e$ and σ) show any significant change in behavior with t_s.

5.2.3 Effect of Stressing on RTS Amplitudes

As mentioned earlier, all traps were hole-attractive, where the trap is negatively charged when empty of a hole (filled with an electron), and becomes neutral after it captures a hole from the valence band (loses

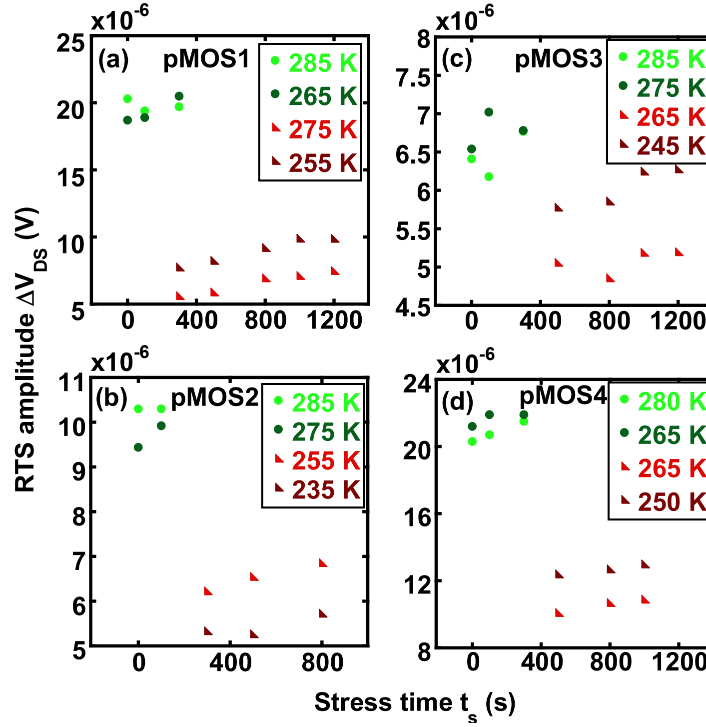


Fig. 5. 8 RTS amplitude ΔV_{DS} as a function of stressing time t_s for different temperatures T for (a) V_{GS}=-1.6 V (P61), V_{GS}=-3 V (S61), (b) V_{GS}=-3 V (P62), V_{GS}=-1.7 V (S62), (c) V_{GS}=-2.1 V (P63), V_{GS}=-1.35 V (S63) and (d) V_{GS}=-1.9 V (P64), V_{GS}=-1.4 V (S64).

the electron to a vacant Si-Si bond in the channel). According to the Unified Numbers and Mobility Fluctuations Model [72], the normalized drain voltage RTS fluctuation amplitude can be expressed as [47],

$$\left|\frac{\Delta V_{DS}}{V_{DS}}\right| = \frac{1}{WL}\left(\frac{1}{P_{inv}} - \alpha\mu\right) \tag{5.2}$$

where, α is the Coulomb screened scattering coefficient, W is the channel width, and L is the channel length. The effective hole mobility μ in Si is calculated from the measured g_d and P_{inv} as, $\mu = g_d L / WqP_{inv}$

[46]. The 1st term inside the parenthesis in Eqn. 5.2 corresponds to fluctuations in the number of holes due to trapping while the 2nd term is the mobility fluctuations due to remote Coulomb scattering from the charged trap. RTS amplitudes for the process and stress-induced traps are plotted in Fig. 5.8 for different devices as a function of t_s . It is observed that the RTS amplitude is increasing with t_s for the traps, which

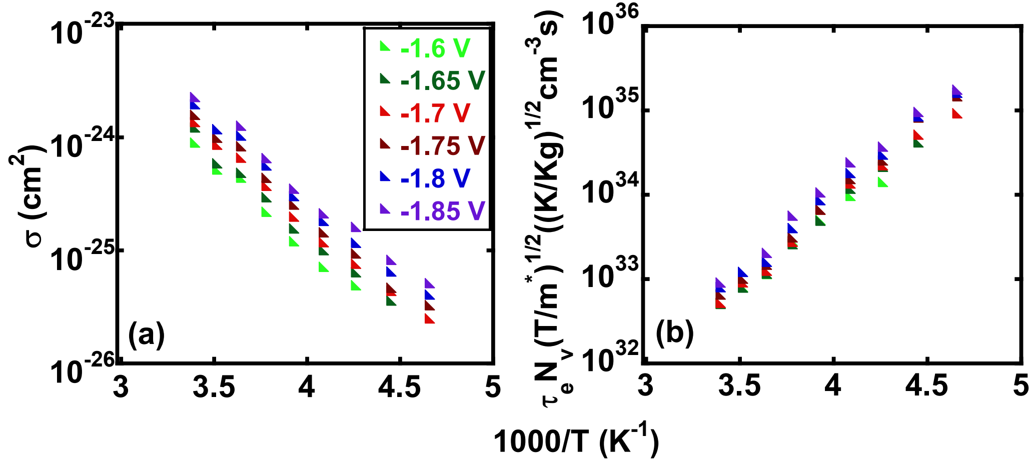


Fig. 5. 9 Arrhenius plot of S63 for different V_{GS} values at t_s = 300 s for the (a) capture cross-section σ, from which capture activation energy ΔE_B is computed. (b) The normalized mean emission time, from which change in enthalpy ΔH and change in entropy $\Delta S/k_B$ are determined.

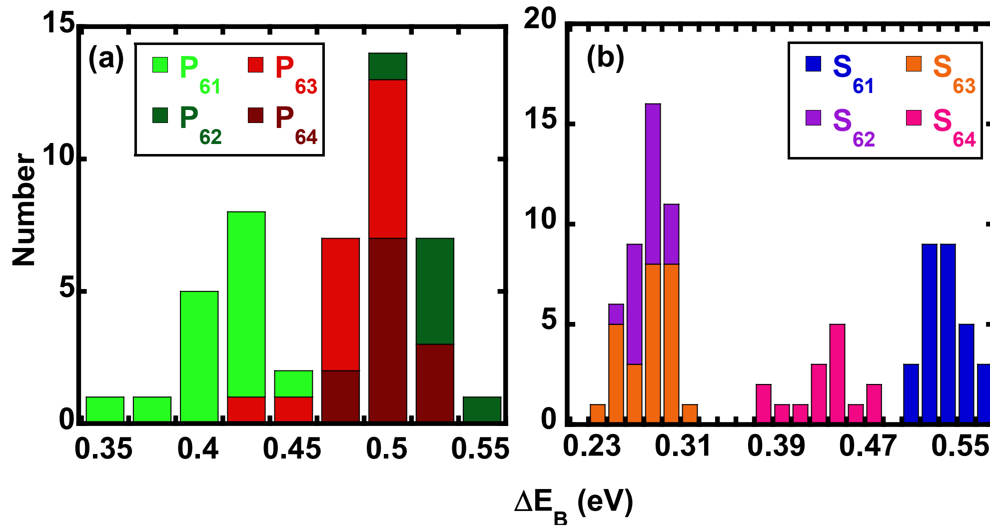


Fig. 5. 10 Distribution of the capture activation energy ΔE_B for all the stressing time instances for the (a) process-induced, (b) stress-induced traps of all the reported devices.

is consistent with our previous work regarding CHC stressing effect for room temperature [88]. Higher number fluctuations (1st term in Eqn. 5.2) result from the negative threshold voltage V_{TH} shift due to the

generation of the fixed positive oxide charge. However, the mobility fluctuations (2nd term in Eqn. 5.2) are decreasing due to the decrease of the screened scattering coefficient α [88]. As a result, the total RTS amplitude increases with t_s .

5.2.4 Activation Energies of Traps from RTS Data

Carrying out variable temperature measurements allowed us to obtain additional trap energies, such as capture activation energy ΔE_B , relaxation energy E_R , change in enthalpy ΔH , and change in entropy $\Delta S/k_B$. A summary of these has been presented in Table 5.1 as a range for all stressing times.

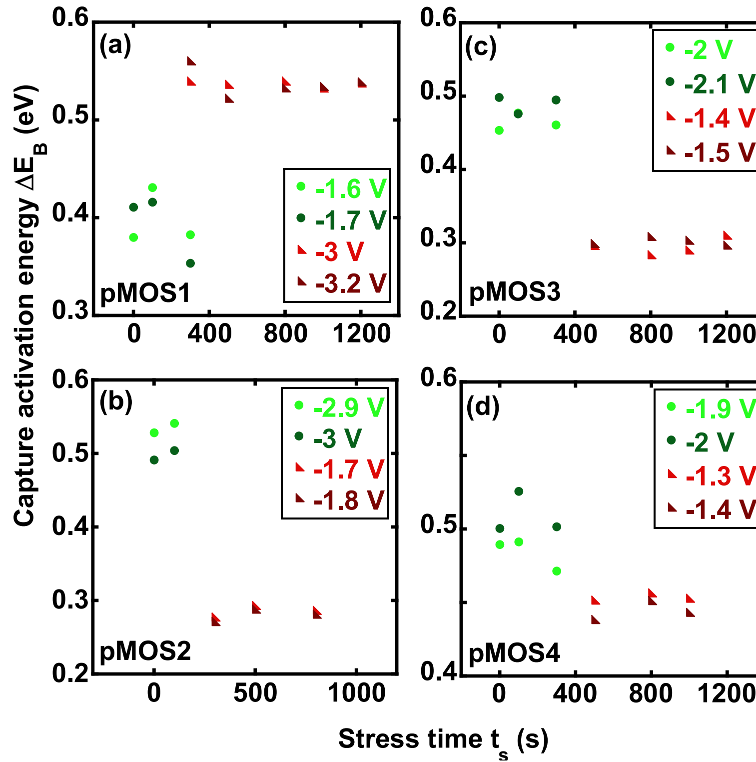


Fig. 5. 11 Capture activation energy ΔE_B as a function of stressing time t_s for representative V_{GS} values.

From the Arrhenius plot of σ, capture cross-section pre-factor σ_0 and ΔE_B are extracted [Fig. 5.9 (a)]. In Fig. 5.10, the distributions of ΔE_B for the process-induced and stress-induced traps are shown separately. Apart from pMOS1, in all other cases, the process-induced traps have higher ΔE_B values than their stress-induced counterparts (Fig. 5.11). This phenomenon leads to having faster stress-induced traps, as there is an exponential relation between $\overline{\tau}_c$ and ΔE_B . In pMOS1, it seems that σ_0 is also playing a strong role in

the determination of $\bar{\tau}_c$ alongside ΔE_B. Previously, $\Delta E_B \approx$ 0.1 eV and $\Delta E_B \approx 0.29$ eV - 0.40 eV were reported for the process- and stress-induced traps, respectively, under DC stressing in nMOSFETs [46].

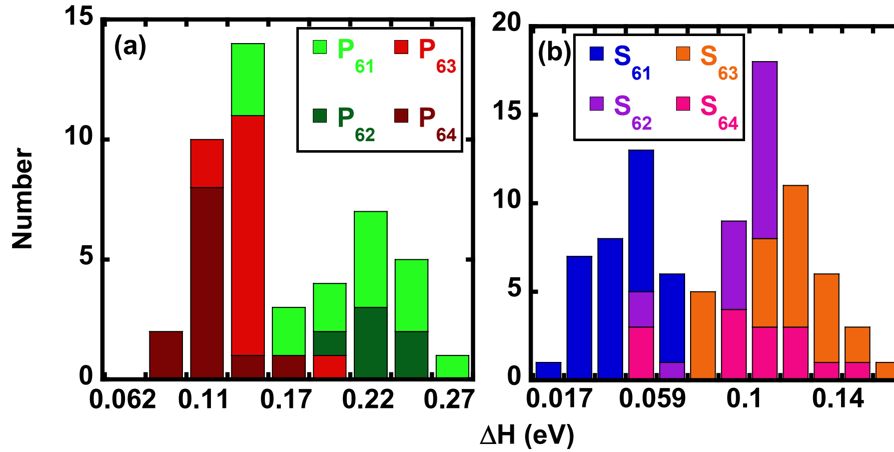


Fig. 5. 12 Distribution of the change in enthalpy ΔH under stressing time instances for the (a) process-induced, (b) stress-induced traps.

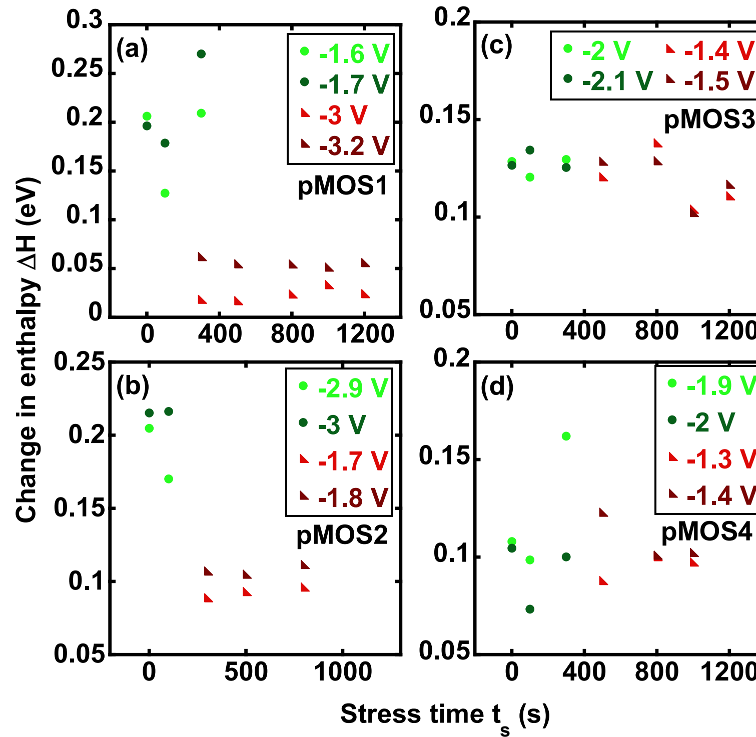


Fig. 5. 13 Change in enthalpy ΔH as a function of stressing time t_s for the representative V_{GS} values.

The Arrhenius plot of $\overline{\tau}_e N_v \left(T/m^*\right)^{1/2}$ from Fig. 5.9 (b) is used to calculate $\left(\Delta E_B + \Delta H\right)$ and $\Delta S/k_B$ [47],

$$\overline{\tau}_e = \frac{1}{g\left(8k_B T/\pi m^*\right)^{1/2} N_v \sigma_0 e^{\Delta S/k_B}} e^{\left[(\Delta E_B + \Delta H)/k_B T\right]} \quad (5.3)$$

Here, $g = 1$ is the degeneracy factor of trap, k_B is Boltzmann's constant, T is temperature, m^* is the effective hole mass, and N_v is the effective density of states of the hole. As ΔE_B is already computed from the Arrhenius plot of σ, ΔH can be easily determined by utilizing Eqn. 5.3.

In Fig. 5.12, the distributions of ΔH for the process-induced and stress-induced traps are shown separately. There are overlaps observed among the range of ΔH values between the process-induced and stress-induced traps. ΔH is plotted as a function of stressing time t_s for the devices in Fig. 5.13. Positive ΔH values infer an endothermic process for all the traps reported.

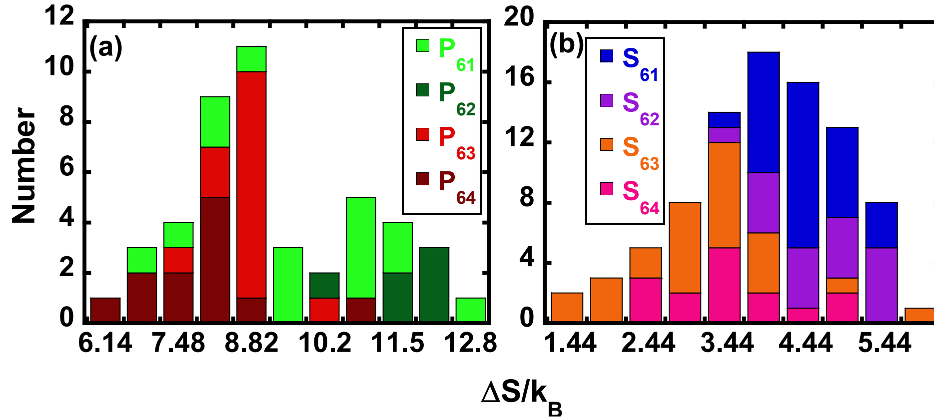


Fig. 5. 14 Distribution of the change in entropy $\Delta S/k_B$ under all the stressing time instances for the (a) process-induced, (b) stress-induced traps. Emission of a hole from the trap, corresponding to capture of a bonded electron from the silicon channel results in a larger increase in the system entropy for process-induced traps.

Perhaps the most pronounced difference between stress- and process-induced traps is the entropy change ΔS upon hole emission (Fig. 5.14). Lower $\Delta S/k_B$ values are observed for all stress-induced traps, compared to their process-induced counterparts (Fig. 5.15).

The relaxation energy E_R can be determined through [47],

$$E_R = \left[\sqrt{\Delta E_B} + \sqrt{\left\{\Delta E_B - \left(\Delta H - T\Delta S\right)\right\}}\right]^2 \quad (5.4)$$

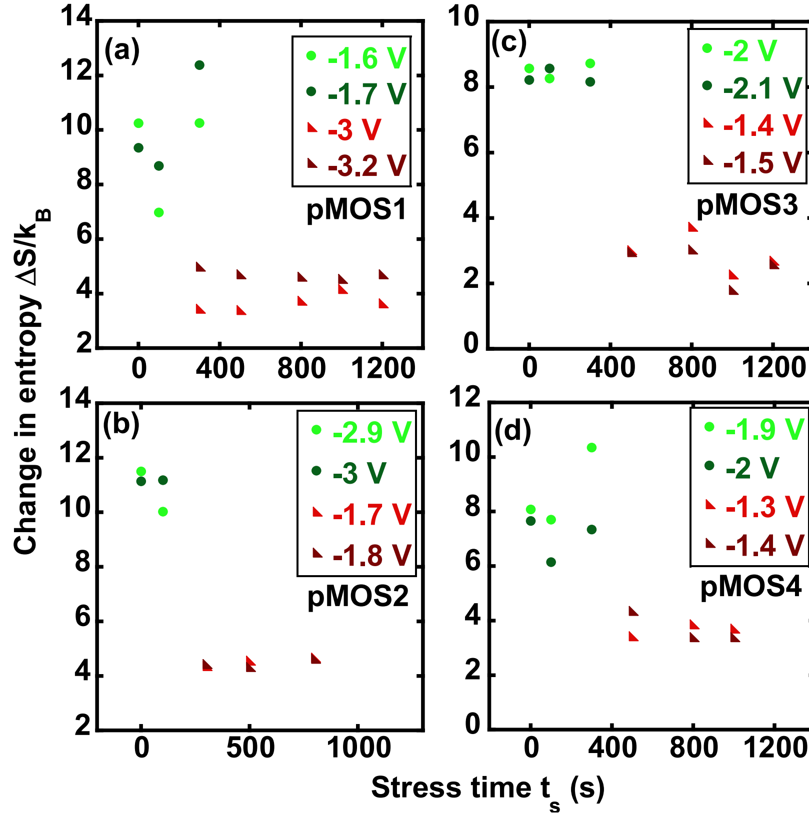


Fig. 5. 15 Change in entropy $\Delta S/k_B$ for representative V_{GS} values as a function of stressing time t_s.

which corresponds to the amount of phonon energy exchange and structural relaxation during the trapping / detrapping process. In Fig. 5.16, the distribution of E_R for the process-induced and stress-induced traps are shown separately. E_R is plotted as a function of t_s for each pMOSFET in Fig. 5.17. Two stress-induced traps, S_{62} and S_{63} [Fig. 5.17 (b, c)] stand out from the others with $E_R \approx 1\,eV$, for which possible reasons will be discussed later.

5.3 Identification of the Defect Centers

The relaxation energy E_R and $\left(E_T - E_{V_{OX}}\right)$ are identifiers of the defect centers responsible for hole trapping in pMOSFETs. Deep hole trap energy levels of $E_T - E_{V_{OX}} \approx 4.8\,eV$ can take several candidates out of consideration, such as neutral oxygen vacancy, a pair of under-coordinated Si and over-coordinated Si atoms, a pair of under-coordinated O and over-coordinated Si atoms, and II-Si since these represent shallow trap energy levels close to the SiO_2 conduction band edge [53].

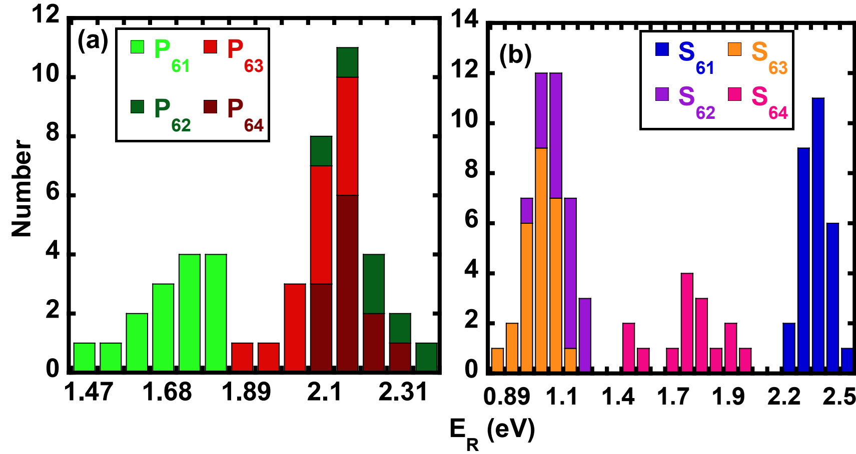


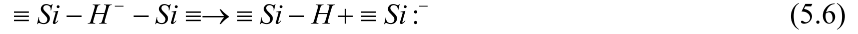
Fig. 5. 16 Distribution of relaxation energy E_R under stressing time instances for the (a) process-induced, (b) stress-induced traps.

D-III Si, on the other hand, is a strong candidate. Its $E_T - E_{V_{OX}} \approx 4.8 - 5.6eV$ matches our calculated value together with E_R of $\sim 0.6 - 2.3eV$ [47], [49]. D-III Si is a defect pair, having a single electron in the sp^3 orbital in one part and paired electrons in the sp^3 orbital in the other part. This defect center is negatively charged. After capturing a hole, it is neutralized and two Si dangling bonds are created, each having one unpaired electron in the sp^3 orbital as [47],

$$\equiv Si^{\bullet} + \equiv Si:^{-} + h^{+} \leftrightarrow \equiv Si^{\bullet} + \equiv Si^{\bullet} \tag{5.5}$$

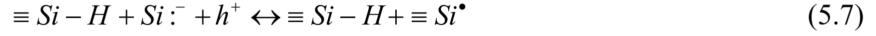
Here, $\equiv$ indicates the bond between Si and three adjacent oxygen atoms, $\bullet$ is the single unpaired electron, and : is the paired electrons in the sp^3 orbital. In this case, the negatively charged defect center becomes neutral afterward representing attractive centers. After the capture of a hole, the average O-Si-O bond angle in the Si dangling bonds changes from ~103° to 107°, indicating the strengthening of the sp^3 hybridization [54].

For some of the defects observed here, hydrogen bridge defect is also a possible candidate, having a higher amount of relaxation E_R in the range of ~1.7-3 eV [52], [109], [110]. Its trap energy level also satisfies our calculations [50], [52]. Hydrogen bridge defect occurs when the hydrogen atom gets in between the oxygen vacancy in SiO_2. It is a complex defect structure containing the presence of hydrogen atom in oxygen vacancy [109]. This defect is believed to be present from the processing stage as trapping of hydrogen is very common in oxygen vacancies because of its abundance in even the driest oxides [55]. Hydrogen bridge defect can be represented as positioned in the middle of a Si-Si bond as, $\equiv Si - H^{-} - Si \equiv$. In detail, this structure can be expressed alternatively in the negatively charged state as,



$$\equiv Si - H^{-} - Si \equiv \rightarrow \equiv Si - H + \equiv Si:^{-} \quad (5.6)$$

After capturing a hole, the negatively charged hydrogen bridge defect center becomes neutral as,



$$\equiv Si - H + Si:^{-} + h^{+} \leftrightarrow \equiv Si - H + \equiv Si^{\bullet} \quad (5.7)$$

In a neutral state, the hydrogen bridge defect is comprised of two parts; one part representing Si-H bond and the other part is a dangling Si bond with a single electron [109].

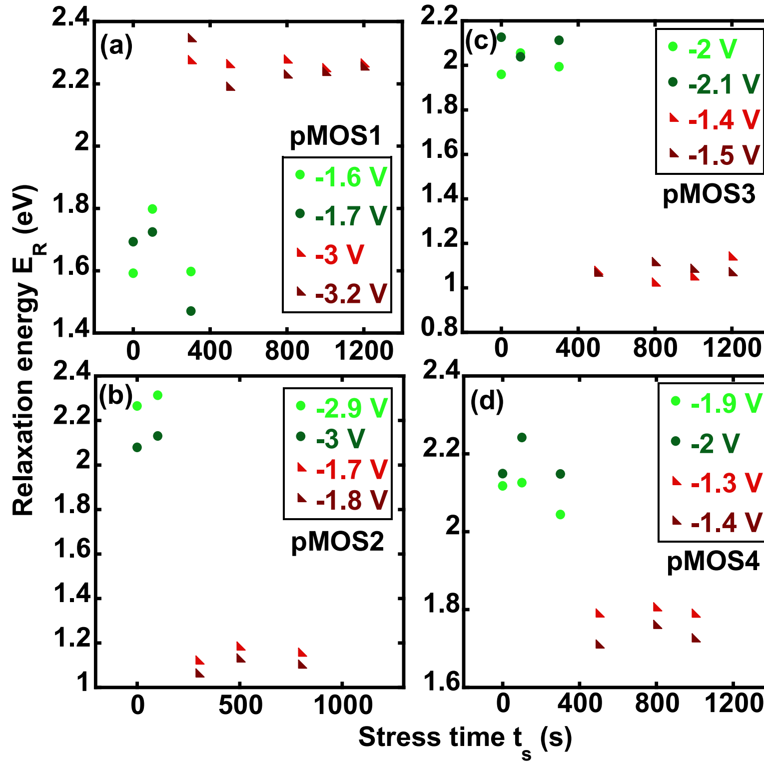


Fig. 5. 17 Calculated relaxation energy E_R as a function of stressing time t_s for representative V_{GS} values. The structural relaxation the defect undergoes when it emits a hole, i.e., captures an electron from the valence band, for the stress-induced defects in pMOS2 and pMOS3 is clearly much less than the other traps.

Based on the abovementioned discussion, by comparing our calculated $\left(E_T - E_{V_{ox}}\right)$ (Table 5.1) and E_R values (Table 5.1 and Fig. 5.17), a list of possible candidates for the defect centers in all the devices is summarized in Table 5.2. Because of the fact that the calculated $\left(E_T - E_{V_{ox}}\right)$ and E_R values satisfy both D-III Si and hydrogen bridge defect centers, it is hard to assign one particular defect center. However, for two of the stress-induced traps, S_{62} and S_{63}, the lower E_R value [Fig. 5.17 (b, c)] is more unique than others and satisfies the condition of only D-III Si being responsible for the defect site.

Table 5. 2 : Defect Candidates

pMOSFET	Trap type	
	Process-induced	Stress-induced
1	D-III Si/ H-bridge	D-III Si/ H-bridge
2	D-III Si/ H-bridge	D-III Si
3	D-III Si/ H-bridge	D-III Si
4	D-III Si/ H-bridge	D-III Si/ H-bridge

Previously, by only computing $\left(E_T - E_{V_{OX}}\right) \approx$ 4.58 eV – 4.85 eV, D-III Si was speculated to be the attractive defect center, whereas puckered / back- projected oxygen vacancy (a pair of III- Si and III- O defects) was thought to act as the repulsive defect center for the pMOSFETs under CHC stressing at room temperature [73]. Hydrogen was found to be responsible for activation / deactivation of the traps [73].

For nMOSFETs, on the other hand, E_R ~ 0.44 eV - 0.46 eV and E_R ~ 1.20 eV - 1.29 eV were reported for the process- and stress-induced traps, respectively [46]. Trap energy level with respect to the conduction band edge $\left(E_{C_{OX}} - E_T\right) \approx$ 2.78 eV -3.31 eV, alongside the mentioned E_R values led to the identification of the repulsive defect sites as unrelaxed neutral oxygen deficiency centers (V_0 ODC II) for nMOSFETs [46]. Clearly, different types of defect centers are created with stressing in pMOS and nMOS. They also interact differently with the channel free electrons and the electrons in the Si bonds.

In this chapter, discussions have been carried out to study the effects of CHC stressing by analyzing different capture and emission activation energy parameters for pMOSFETs. There is a pronounced difference in the change of entropy, as the stress-induced traps show a lower change in entropy than its process-induced counterparts when the hole is emitted back into the channel from the defect site. Disassociated III-Si and hydrogen bridge defects are identified to be responsible for hole trapping. Two of the stress-induced traps show considerably lower structural relaxation and act uniquely as a D-III Si defect.

Chapter 6: Analyses of Flicker Noise in nMOSFETs

It is known that flicker (1/f) noise increases with decreasing device dimensions. Therefore, MOSFET downscaling has highlighted its prominence as well as its unpredictability due to high variation from device to device. The power spectral density (PSD) of the 1/f noise is obtained by adding up the power spectral densities from different RTS (random telegraph signals) with different corner frequencies [10]. The PSD of the RTS is known as Lorentzian. The RTS spectra that add up to the 1/f noise in the frequency domain have an exponential distribution of time constants in the time domain representing the trapping/ detrapping of the channel carriers to the defect sites at the Si-SiO_2 interface or inside SiO_2 [11]. In Fig. 6.1, PSD of the 1/f noise is represented as a function of frequency f , showing the addition of the Lorentzian spectra [111].

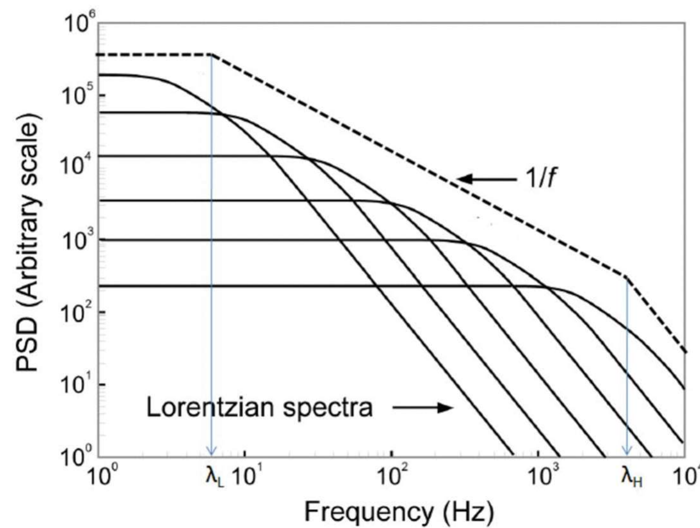


Fig. 6. 1 1/f noise power spectral density (PSD) as a function of frequency f . Lorentzians from RTSs with different corner frequencies added up to produce the 1/f noise PSD. λ_L and λ_H are the corner frequencies of the slowest and fastest traps, respectively [111]. (Reprinted with permission. Copyright © 2015, IEEE)

There has been a long debate on whether the number or mobility fluctuations of the channel carriers is responsible as the origin of 1/f noise. Number fluctuations model of 1/f noise was proposed by A. L. McWhorter in 1957 [64]. This model successfully explained the experimentally obtained 1/f noise PSD data for the nMOSFETs [65], [66]. However, McWhorter's number fluctuations model did not take the multi-phonon assisted tunneling process into account, which is widely considered nowadays as the mechanism for capture/ emission of the channel carriers into the defect sites in MOSFETs. Moreover, the Coulomb scattering effect of the channel carriers, being trapped inside the defect sites was also completely ignored in McWhorter's model. In 1969, F. N. Hooge proposed a new 1/f noise model, based on the mobility fluctuations of the channel carriers [67]. There was, however, a lack of physical reasoning to choose the

value of one of the controlling parameters in this mobility fluctuations model. As a result, researchers like Ghibaudo and Chenming Hu tried to include both the number and mobility fluctuations while working to develop a universal model for both the n- and pMOSFETs. Ghibaudo *et al.* presented the correlated mobility fluctuations model [71], whereas C. Hu *et al.* successfully developed the unified number and mobility fluctuations theory considering the impact of both the number and mobility of the channel carriers [72].

In this chapter, flicker (1/f) noise data from three different wafers of three different nMOSFET technologies are examined. The dominant noise mechanism between the number and mobility fluctuations is determined by analyzing the experimental 1/f noise data. As the wafers were fabricated in different technologies, normalization of the 1/f noise is performed with respect to the oxide layer thickness T_{OX}, oxide capacitance C_{OX}, channel width W, and channel length L to achieve a meaningful comparison of the noise levels among them. Subsequently, these 1/f noise data are related to the different fabrication process parameters to explain the distinctions among the observed noise levels.

6.1 Specification of the nMOSFET Devices and Measurement Steps

Different dimensions of nMOSFETs were examined to measure 1/f noise on wafers x2388, x2550, and x2396, named as such by Texas Instruments. For some of the smaller device dimensions, Lorentzian PSD was observed which denotes the presence of RTS as the primary noise component. However, in most of the cases in larger gate area devices, 1/f noise PSD was observed. In Table 6.1, the dimensions of the devices from different wafers are listed for which 1/f noise was observed. The number of devices used for 1/f noise measurements under each dimension is also shown.

Table 6. 1: Device information from the three different wafers for 1/f noise measurements

Wafer x2388		Wafer x2550		Wafer x2396	
W × L (μm²)	Number of devices	W × L (μm²)	Number of devices	W × L (μm²)	Number of devices
1×0.5	1	1×0.5	1	1×0.5	1
1×0.8	1	1×0.7	1	1×0.7	1
1×1	1	1×1	1	1×4	1
1×5	2	1×10	2	1×20	1
1×10	2	5×0.7	6	6×0.6	6
5×0.6	5	5×1	2	6×4	1
5×1	2	5×10	6	6×20	4
5×10	6	10×1	3	20×0.8	1
10×1	3	10×10	6	20×4	6
10×10	6				

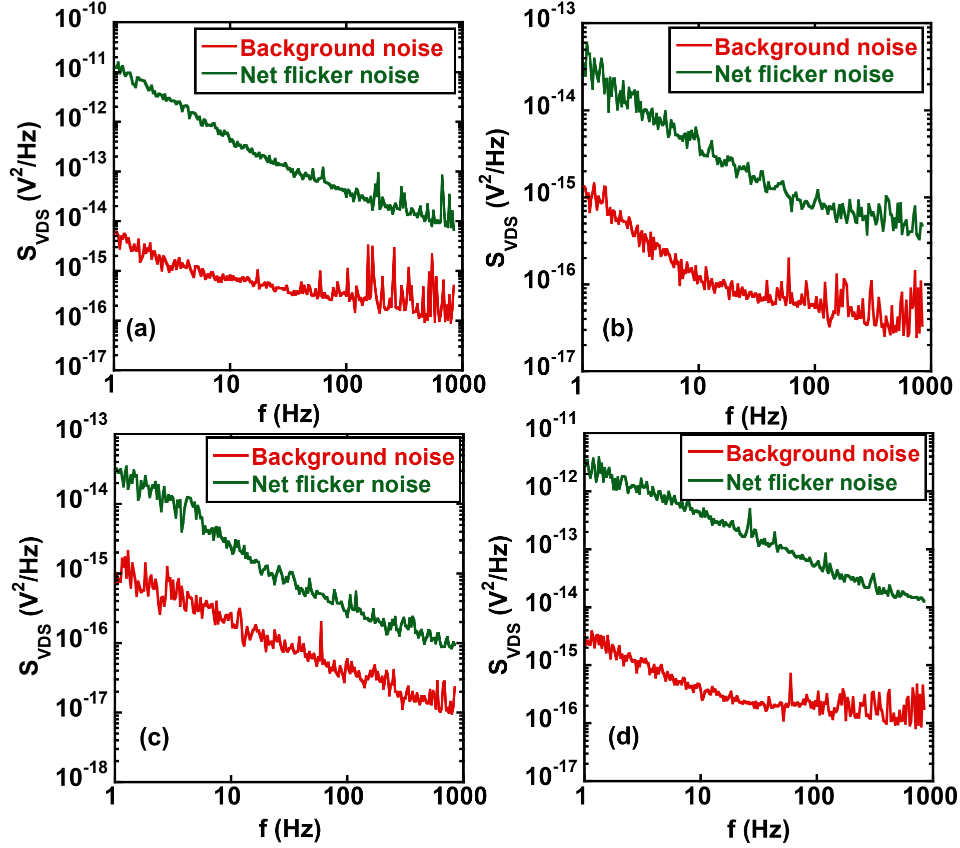


Fig. 6. 2 Background noise and flicker (1/f) noise PSD as function of frequency f for (a) $W \times L$ =10×1 μm² from x2388, (b) $W \times L$ =10×10 μm² from x2388, (c) $W \times L$ =20×4 μm² from x2396, and (d) $W \times L$ =5×10 μm² from x2550.

For all the nMOSFETs, 0.2 V was applied at the drain terminal and gate-source overdrive voltage $(V_{GS} - V_{TH})$ was incremented by 0.25 V from 0.25 V to 2.25 V. At the very beginning, Semiconductor Parameter Analyzer (SPA) measurements were carried out to check the functionality of the device, and then the 1/f noise measurements were taken. The range of frequency f for the experiments was from 1 to 1000 Hz. The first step of the measurement process was to record the background noise PSD. Background noise was measured at each gate-source overdrive bias point by keeping the drain voltage at zero volts, that is, drain and source are shorted. Background noise depends on the device thermal noise, system noise, contact noise, noise from the biasing circuitry, noise from the pre-amplifier, and noise from the 60 Hz component of the power line. After completely measuring the background noise PSD at each of the gate-source overdrive bias points, voltage noise PSD was measured at each of these bias points again by applying 0.2 V drain voltage. Net voltage noise PSD was calculated at each bias point by subtracting the background

noise from the drain voltage noise PSD. Details about the measurement techniques and setup were previously discussed in detail in chapter 2.

Some of the voltage noise PSDs as a function of frequency are plotted in Fig. 6.2. Net voltage noise PSD and background noise PSD are represented in the same plot. Net PSD of the 1/f noise data is curve fitted up to 100 Hz to calculate the frequency exponent γ . From the 1/f noise measurements, the frequency exponent γ is found to be between 0.7 and 1.4, which makes it a typical 1/f noise.

6.2 Mathematical Analysis of the 1/f Noise Data

Normalization of the 1/f noise is performed based on the number fluctuation theory as [57],

$$\frac{S_{I_{DS}}}{I_{DS}^2} = \frac{q^2 k_B T}{\lambda f W L C_{ox}^2 \left(V_{GS} - V_{TH}\right)^2} N_T \tag{6.1}$$

Here, $S_{I_{DS}}$ is the drain-source current noise PSD, I_{DS} is the drain-source current, q is the electronic charge, k_B is the Boltzmann constant, T is temperature in K, λ is the tunneling attenuation coefficient, and N_T is the volume density of the oxide traps per unit energy in the nMOSFET.

$S_{I_{DS}}$ is calculated from $S_{I_{DS}} = g_d^2 S_{V_{DS}}$, where g_d is the channel output conductance measured by SPA, and $S_{V_{DS}}$ is the drain-source voltage noise PSD obtained from the 1/f noise measurements. Transconductance of the device in the linear region is defined as,

$$g_m = \frac{\delta I_{DS}}{\delta V_{GS}} = \mu C_{ox} \frac{W}{L} V_{DS} \tag{6.2}$$

where, μ is the effective mobility of the channel carriers. Eqn. 6.1 can be alternatively rewritten by considering the channel transconductance g_m in the linear region $\left[g_m = I_{DS} / \left(V_{GS} - V_{TH}\right)\right]$ as [57],

$$\frac{S_{I_{DS}}}{I_{DS}^2} = \frac{k_B T q^2 N_T}{\lambda f W L C_{OX}^2} \frac{g_m^2}{I_{DS}^2} \tag{6.3}$$

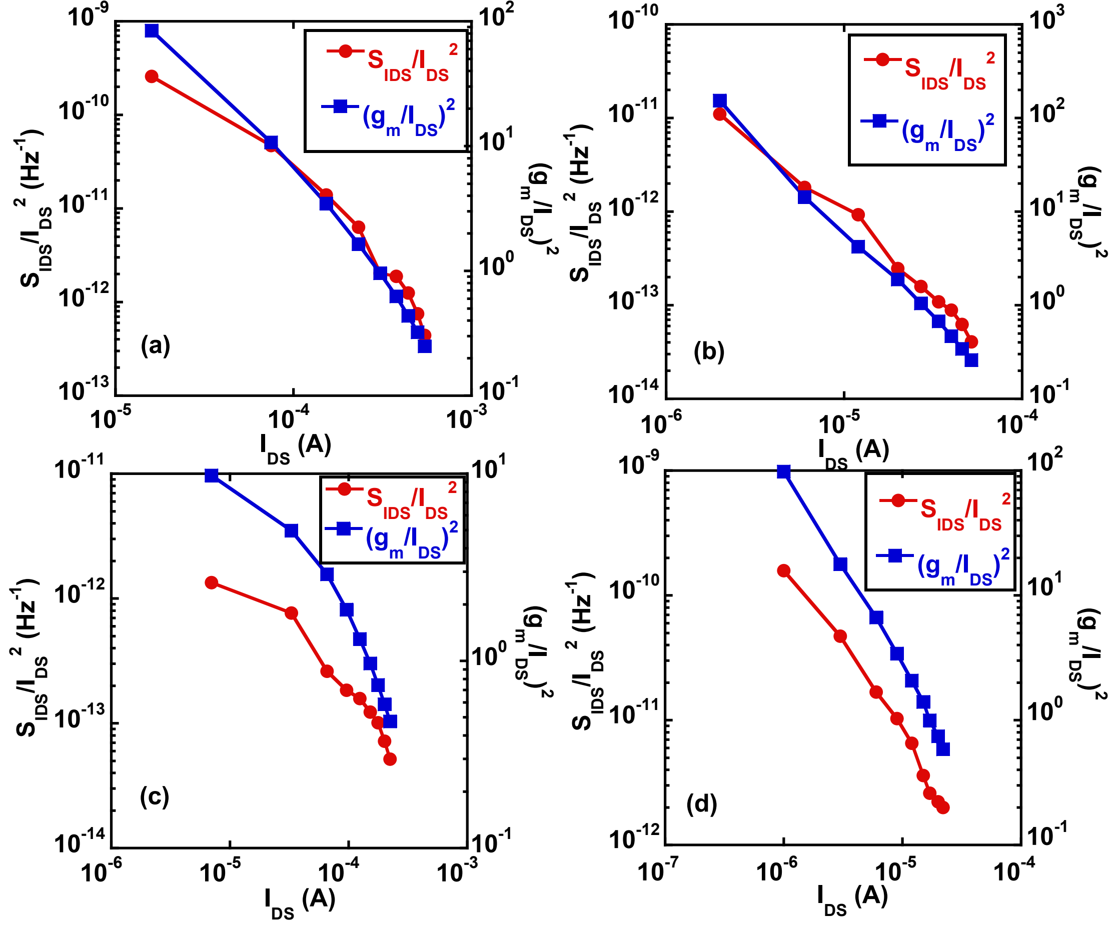


Fig. 6. 3 Current noise PSD and $\left(g_m/I_{DS}\right)^2$ as function of I_{DS} for (a) $W\times L$ =10×1 μm^2 from x2388, (b) $W\times L$ =10×10 μm^2 from x2388, (c) $W\times L$ =20×4 μm^2 from x2396, (d) $W\times L$ =5×10 μm^2 from x2550.

From Eqn. 6.3, it is observed that the normalized current noise PSD would follow the pattern of $\left(g_m/I_{DS}\right)^2$ if the number fluctuation acts as the dominant flicker noise mechanism in our measurements. In Fig. 6.3, x2388 (10×1) μm^2, x2388 (10×10) μm^2, x2396 (20×4) μm^2, and x2550 (5×10) μm^2 devices have their current noise PSD normalized. They show good correlated fitting with the number fluctuation model as they are following the $\left(g_m/I_{DS}\right)^2$ pattern. Hence, it can be inferred that number fluctuation mechanism is playing a dominant role in our 1/f noise measurement experiments for these 3 different kinds of wafers.

For a meaningful comparison of different MOSFETs, normalization of the current noise PSD is performed with respect to W, L, and T_{OX} as [57],

$$\frac{S_{I_{DS}}WL}{I_{DS}^2 T_{OX}^2} = \frac{k_B T q^2 N_T}{\lambda f \varepsilon_0^2 \varepsilon_{OX}^2} \frac{g_m^2}{I_{DS}^2} \tag{6.4}$$

where, ε_0 is the permittivity of the free space, and ε_{OX} is the dielectric constant of SiO_2.

6.3 Normalization of the Flicker (1/f) Noise Data

In this section, normalized current noise PSDs are compared among similar width devices from the wafers. The aim is to determine which wafer is showing the highest comparative noise level among them and to find out the physical reasons behind.

In Figs. (6.4-6.7, 6.10), it is clear that for the smaller dimension MOSFETs, it is not possible to compare the noise levels due to high variability from device to device. Transistor variability can be divided into spatial and temporal variability. Spatial variability consists of two types: variability within the die and variability from die to die, whereas temporal variability considers aging and transients [112]. All the elements of the chip are equally affected from the die to die variations. Asymmetries of chamber gas flow, thermal gradients, imperfections in equipment operation, and process flow are the main reasons behind the die to die variations. On the other hand, variability within the die causes electrical characteristics of the transistors i.e., threshold voltage V_{TH} to fluctuate non-uniformly across a chip. Variability within the die can be categorized into symmetric and random components. Random dopant fluctuation is the variation in the crystalline Si structure due to nonuniformity of dopant atoms in the channel because of their irregular distributions. However, for the larger dimension devices, obtained data patterns are consistent across the number of devices of a particular dimension [Fig. 6.8, 6.9]. MOSFETs from the x2396 wafer show the lowest amount of noise, whereas x2550 shows the highest level of 1/f noise. MOSFETs from x2388 have showed an intermediate level of noise. For the larger device dimensions, 1/f noise results in a small amount of inter device variation. Only one or two traps are present in today's deeply scaled devices, and this lesser number of traps causes significant inter-device variation [113]. The variability effect on different sizes of devices is shown in Fig. 6.11.

The larger dimension MOSFETs from these three different wafers are studied further in the later sub-sections.

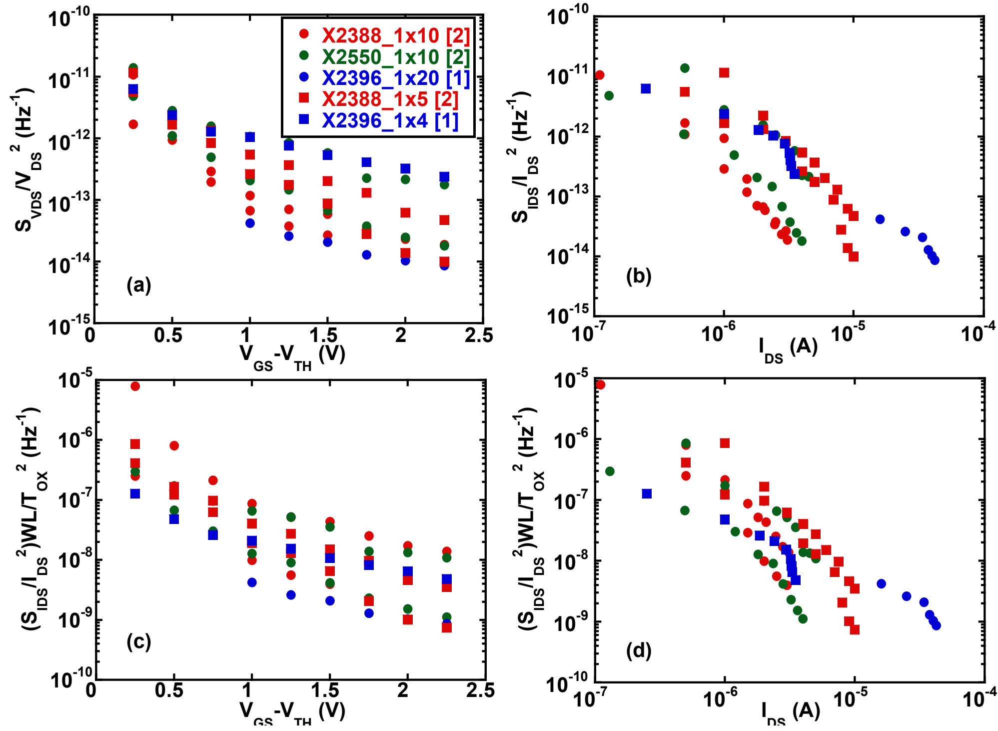


Fig. 6. 4 Comparing (a) voltage noise PSD, (b) current noise PSD, (c) & (d) normalized current noise PSD from $W \times L$ =1×10, 1×5 μm^2 of x2388, $W \times L$ =1×10 μm^2 of x2550, and $W \times L$ =1×20, 1×4 μm^2 of x2396. The number inside the bracket stands for the numbers of nMOSFETs used for that device dimension.

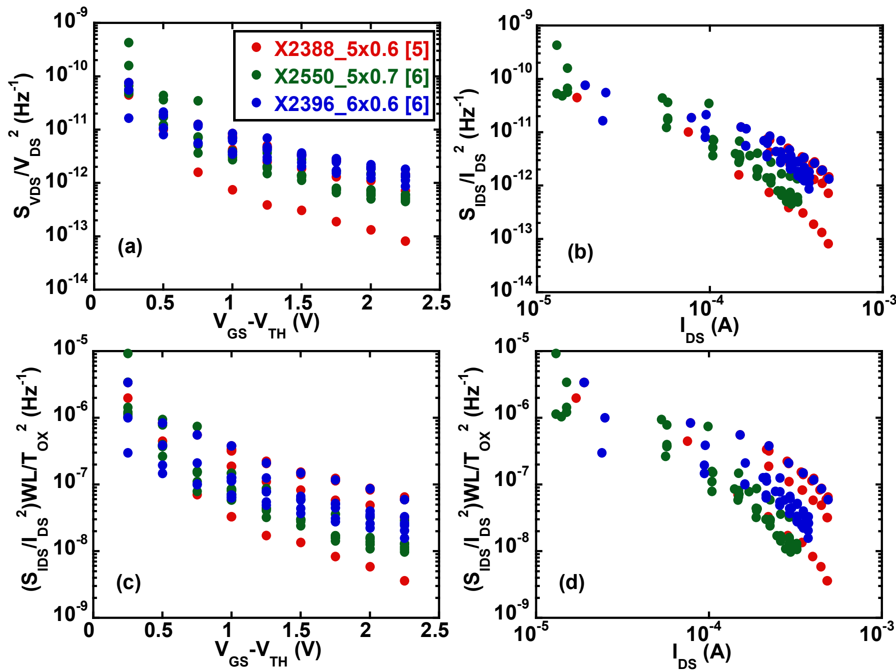


Fig. 6. 5 Comparing (a) voltage noise PSD, (b) current noise PSD, (c) & (d) normalized current noise PSD from $W \times L$ =5×0.6 μm^2 of x2388, $W \times L$ =5×0.7 μm^2 of x2550, and $W \times L$ =6×0.6 μm^2 of x2396.

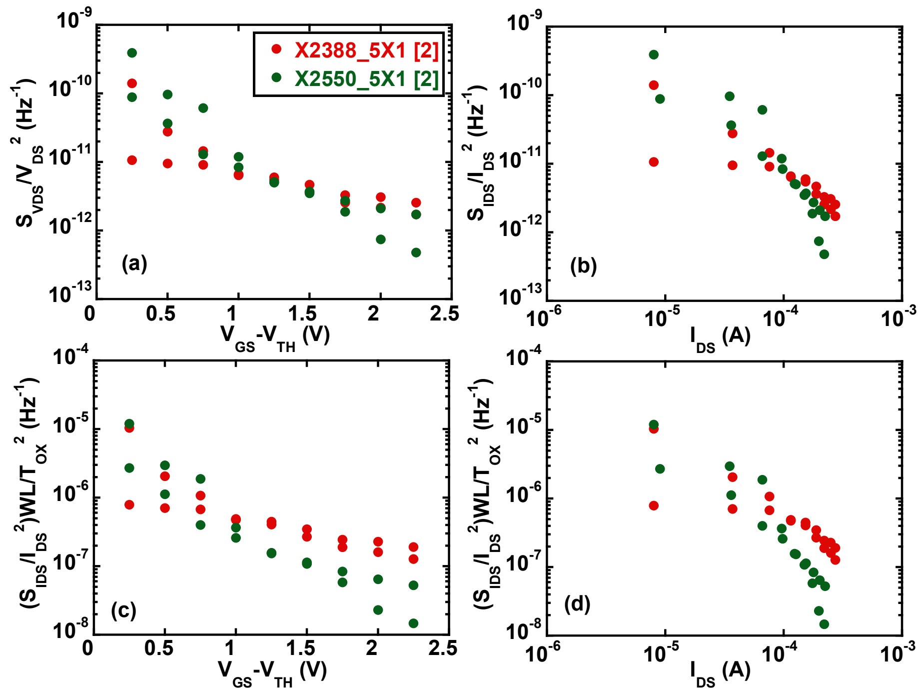


Fig. 6. 6 Comparing (a) voltage noise PSD, (b) current noise PSD, (c) & (d) normalized current noise PSD from $W \times L = 5{\times}1\ \mu m^2$ of x2388 and $W \times L = 5{\times}1\ \mu m^2$ of x2550.

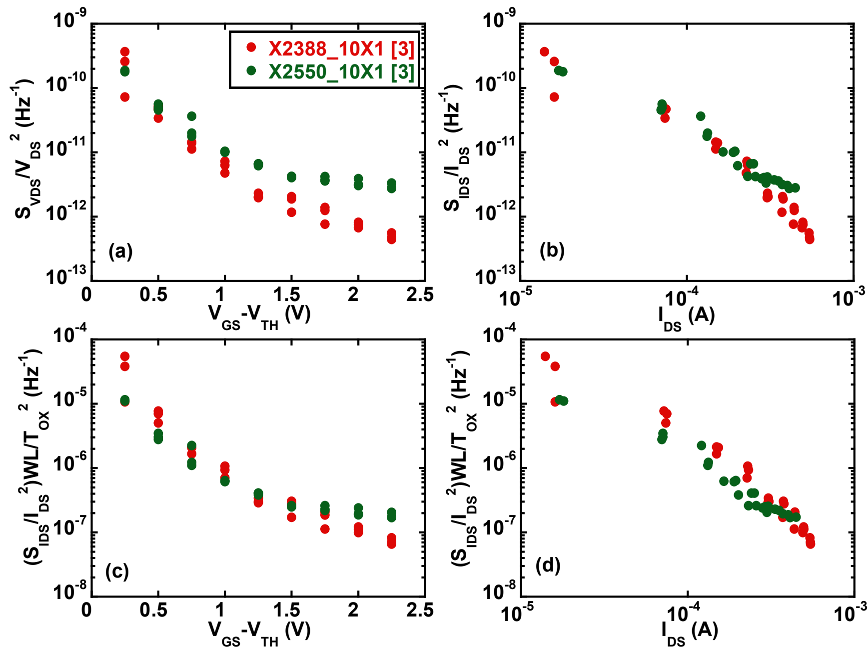


Fig. 6. 7 Comparing (a) voltage noise PSD, (b) current noise PSD, (c) & (d) normalized current noise PSD from $W \times L = 10{\times}1\ \mu m^2$ of x2388 and $W \times L = 10{\times}1\ \mu m^2$ of x2550.

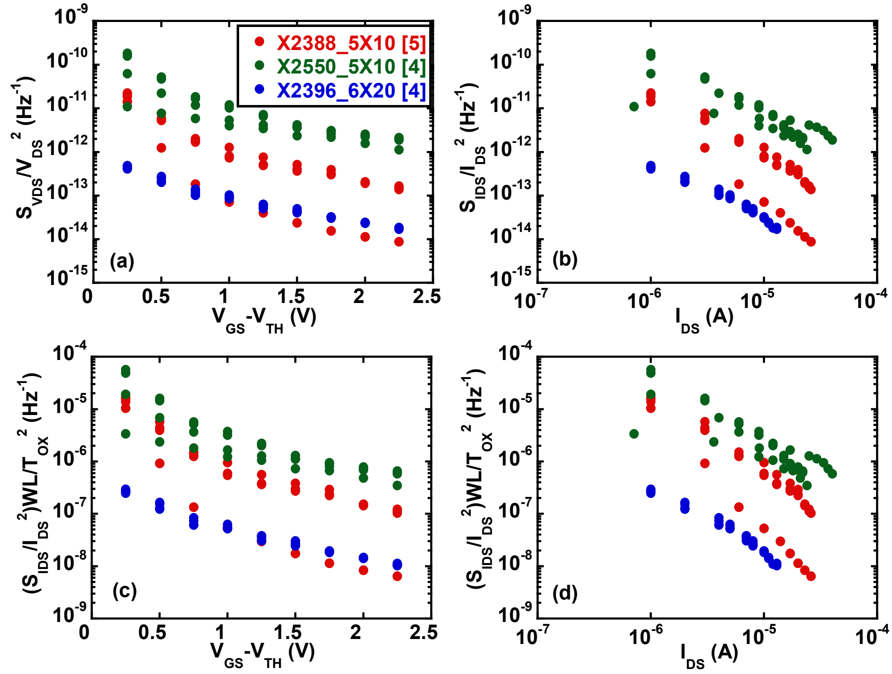


Fig. 6. 8 Comparing (a) voltage noise PSD, (b) current noise PSD, (c) & (d) normalized current noise PSD from $W \times L$ =5×10 μm² of x2388, $W \times L$ =5×10 μm² of x2550, and $W \times L$ =6×20 μm² of x2396.

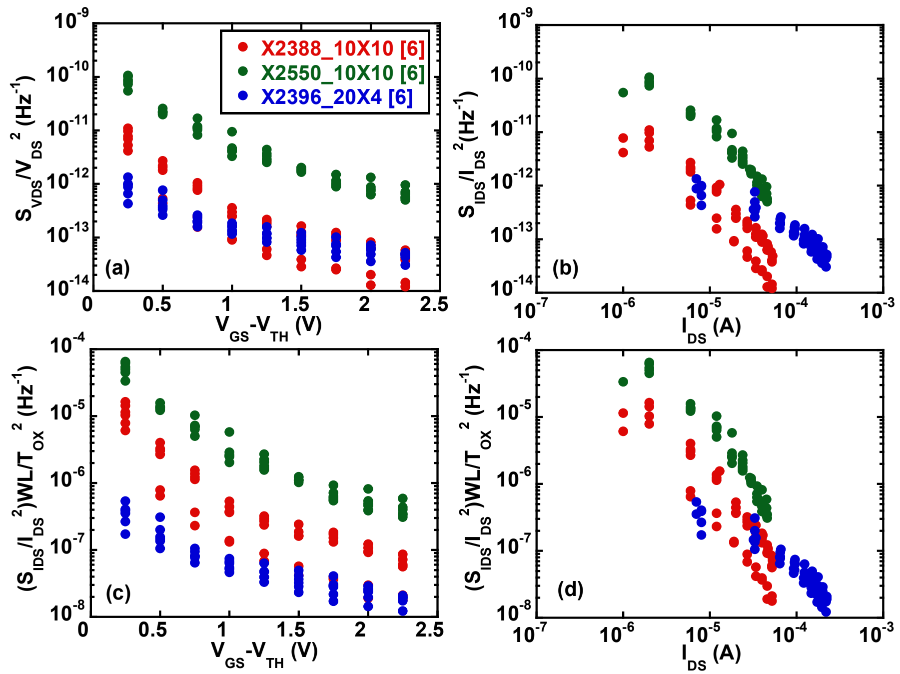


Fig. 6. 9 Comparing (a) voltage noise PSD, (b) current noise PSD, (c) & (d) normalized current noise PSD from $W \times L$ =10×10 μm² of x2388, $W \times L$ =10×10 μm² of x2550, and $W \times L$ =20×4 μm² of x2396.

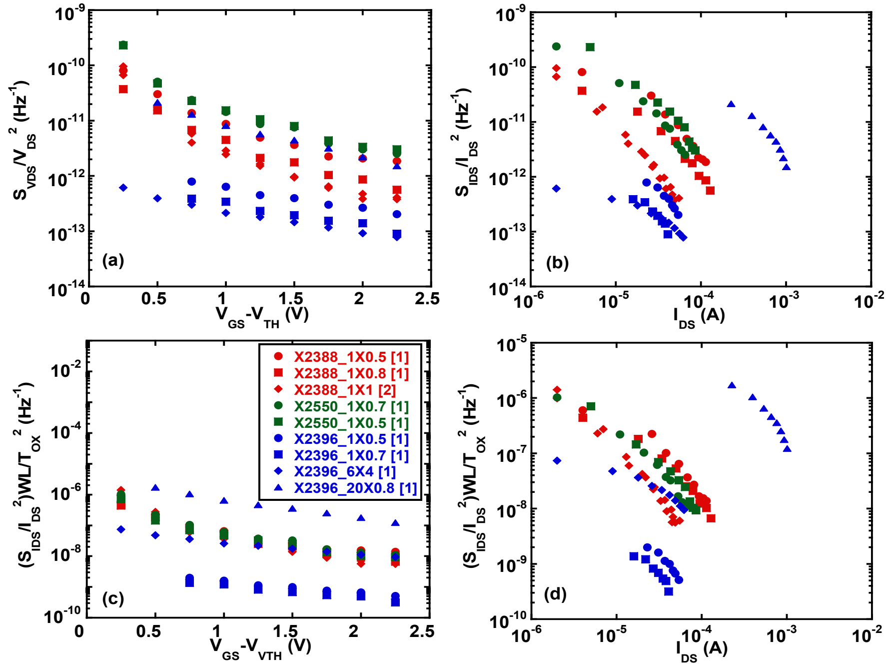


Fig. 6. 10 Comparing (a) voltage noise PSD, (b) current noise PSD, (c) & (d) normalized current noise PSD from $W \times L$ =1×0.5 μm^2 , $W \times L$ =1×0.8 μm^2 and $W \times L$ =1×1 μm^2 of x2388, $W \times L$ =1×0.5 μm^2 and $W \times L$ =1×0.7 μm^2 of x2550, and $W \times L$ =1×0.5 μm^2, $W \times L$ =1×0.7 μm^2, $W \times L$ =6×4 μm^2, and $W \times L$ =20×0.8 μm^2 of x2396.

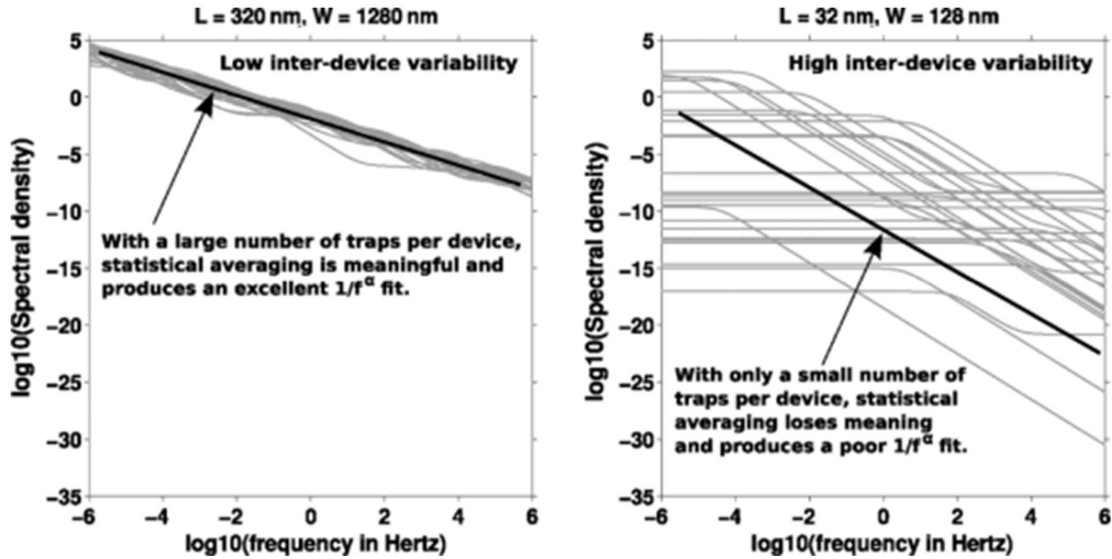


Fig. 6. 11 Comparison of variability in devices with different sizes [113]. (Reprinted with permission. Copyright © 2013, IEEE)

6.4 Correlation of the Process Parameters with 1/f Noise across Different Wafers

Different MOSFET fabrication steps were followed across these three wafer lots. Differences in the doping conditions, doses, and uses of different materials in the gate oxide layer led to the different amounts of normalized 1/f noise among the wafers. In our measurements, we have used x2550, x2388 and x2396 wafers from Texas Instruments Inc., and it has been observed that x2550 shows the highest amount of normalized 1/f noise, while the x2396 shows the lowest amount of normalized 1/f noise for larger device dimensions. In this section, process conditions of the wafers will be correlated to the experimentally obtained normalized 1/f noise data from our experiments.

At the poly gate annealing stage, annealing temperatures of 900°, 800°, and 900° C were used for wafer x2550, x2388, and x2396, respectively. Temperatures in the range of 800° to 875° C have a very negligible impact on the generation of oxide charge [114]. However, for annealing temperatures greater than 875° C, a sharp increase in the generated oxide charges occurs [114]. The increase in the amount of oxide charge leads to the creation of an increased number of oxygen vacancies. Annealing temperatures for x2550 and x2396 were 900° C. Therefore, there would be a higher amount of oxide charges in x2550 and x2396 than in the x2388 wafer, leading to a larger amount of normalized 1/f noise than x2388 due to its higher annealing temperature.

Fluorine (F) was used for implantation in wafer x2550, and boron fluoride (BF) was used for implantation in wafer x2396. Incorporation of F helps to reduce the amount of 1/f noise in the devices [115], [116]. F removes hydrogen from the Si-SiO_2 system by reacting with it and thus deactivates the interface and oxide trap sites [117]. Due to F implantation, the dangling bonds at the Si-SiO_2 interface are passivated, and the number of interface traps decreases [115]. In wafer x2396, deeper penetration of F is possible inside SiO_2 than x2550 wafer due to the higher energy of the implants [116]. As a result, more F can reach to the Si-SiO_2 interface for x2396 than x2550, leading x2396 wafer to have the lowest amount of 1/f noise. However, there was no implantation profile given for x2388. If only the effect of the gate poly implant is taken into account, then wafer x2388 may have the highest normalized 1/f noise.

Both x2550 and x2396 wafers were sintered at 435° C for 30 minutes using H_2. In that case, these wafers would show lower 1/f noise than x2388.

Although the impact of some of the known process parameters are discussed here separately on the normalized 1/f noise, the correlations among these parameters are unknown for explaining the comparative level of normalized 1/f noise in these 3 wafers. As a result, it is difficult to relate these process parameters comprehensively to the amount of the observed normalized 1/f noise.

6.5 Extraction of Trap Density and Screened Scattering Coefficient Parameters Based on the Unified Noise Model

Trap density and the amount of screened scattering coefficients are investigated in this section from the experimental 1/f noise data. According to the Unified Number and Mobility Fluctuations (UNMF) model for the 1/f noise, the drain-source current noise PSD is represented as [72],

$$S_{I_{DS}} = \frac{k_B T I_{DS}^2 N_T}{\lambda f W L} \left(\frac{1}{N_{inv}} \pm \alpha \mu \right)^2 \tag{6.5}$$

Here, N_{inv} is the inversion layer charge density of the nMOSFET, and α is the screened scattering coefficient. The first term inside the parenthesis of the Eqn. 6.5 is the number fluctuations, and the second term is the mobility fluctuations, respectively. The plus sign stands for the repulsive trap centers, whereas the minus sign stands for the attractive trap centers. In our work in this case, repulsive trap centers are mostly observed in nMOSFETs, so the plus sign will be the predominant symbol [46]. The screened scattering coefficient α is represented as [72],

$$\alpha = \alpha_0 + \alpha_1 \ln\left(N_{inv}\right) \tag{6.6}$$

where, α_0 and α_1 are the fitting parameters, and $\alpha_1 < 0$ [72].

To calculate the amount of volumetric trap density N_T and the screened scattering parameters α_0 and α_1, current noise PSD of different dimensions of devices from these three wafers are curve-fitted to the UNMF model. Levenberg-Marquardt algorithm is utilized as the numerical technique by implementing the lsqcurvefit function in MATLAB. Levenberg-Marquardt algorithm is the most widely used optimization algorithm for solving non-linear least square problems [118]. This is a combination of two numerical algorithms: the gradient descent method and the Gauss-Newton method. The main idea behind implementing the Levenberg-Marquardt algorithm is that it is more robust and faster to converge to the solution than the other algorithms [119]. In Fig. 6.12-6.14, the normalized current noise PSD is curve fitted with the UNMF model for different MOSFETs. Number and mobility fluctuations are also shown in the same plot alongside with the normalized current noise PSD and the curve fit for a particular dimension of device. In Table 6.2, volumetric trap density N_T, remote coulomb scattering coefficients α_0, and α_1 are listed alongside the associated error between our 1/f noise PSD and the curve fitted PSD.

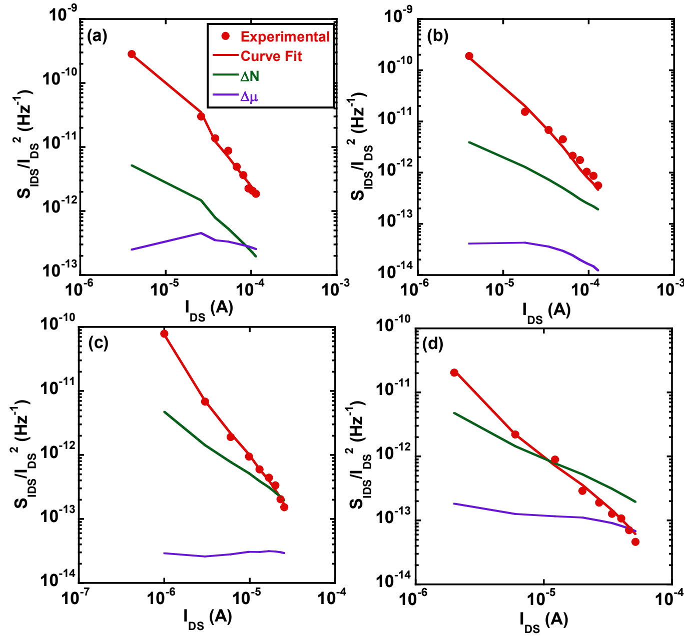


Fig. 6. 12 Normalized 1/f current noise PSD data from the experiments, Curve fitted 1/f noise PSD data, number, and mobility fluctuations in x2388 nMOSFETs from (a) W×L=(1×0.5) μm^2, (b) W×L=(1×0.8) μm^2, (c) W×L=(5×10) μm^2, and (d) W×L=(10×10) μm^2.

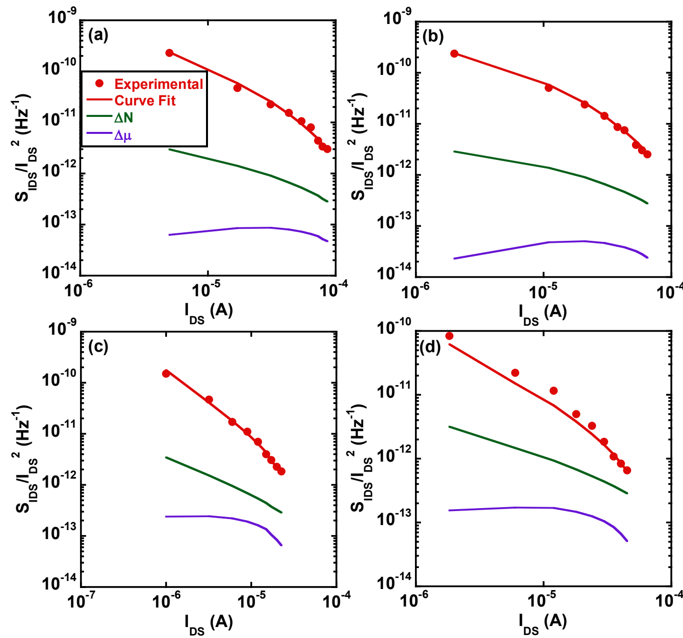


Fig. 6. 13 Normalized 1/f current noise PSD data from the experiments, Curve fitted 1/f noise PSD data, number, and mobility fluctuations in x2550 nMOSFETs from (a) W×L=(1×0.5) μm^2, (b) W×L=(1×0.7) μm^2, (c) W×L=(5×10) μm^2, and (d) W×L=(10×10) μm^2.

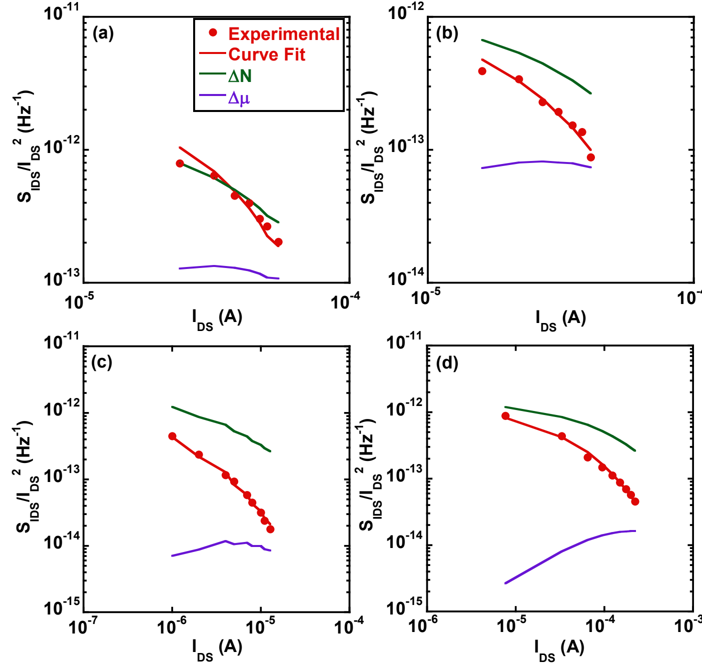


Fig. 6. 14 Normalized 1/f current noise PSD data from the experiments, Curve fitted 1/f noise PSD data, number, and mobility fluctuations in x2396 nMOSFETs from (a) W×L=(1×0.5) μm^2, (b) W×L=(1×0.7) μm^2, (c) W×L=(6×20) μm^2, and (d) W×L=(20×4) μm^2.

Table 6. 2 : Obtained values of N_T, α_0, and α_1 for different wafers from numerical techniques of curve fitting. Bracket beside (W×L) denotes numbers of devices used for averaging current noise PSD from our measurements.

Wafer	$(W \times L)$ μm^2	N_T (cm^{-3}ev^{-1})	α_0 (V-s)	α_1 (V-s)	error
x2388	5×10 [4]	6.61×10^{16}	1.12×10^{-16}	-1.14×10^{-18}	8.51×10^{-46}
	10×10 [6]	3.5×10^{16}	2.13×10^{-15}	-1.24×10^{-16}	4.19×10^{-45}
	1×0.5 [1]	1.85×10^{15}	8.5×10^{-16}	-1.15×10^{-17}	6.34×10^{-41}
	1×0.8 [1]	3.51×10^{15}	3.18×10^{-16}	-2.8×10^{-17}	4.62×10^{-41}
x2550	5×10 [4]	2.55×10^{17}	5.62×10^{-15}	-3.8×10^{-16}	3.94×10^{-44}
	10×10 [6]	3.18×10^{17}	4.83×10^{-15}	-3.0×10^{-16}	8.14×10^{-42}
	1×0.5 [1]	5.12×10^{15}	7.42×10^{-16}	-6.32×10^{-17}	8.10×10^{-41}
	1×0.7 [1]	7.85×10^{15}	5.86×10^{-16}	-5.17×10^{-17}	7.32×10^{-42}
x2396	6×20 [4]	1.33×10^{16}	3.31×10^{-16}	-2×10^{-17}	4.92×10^{-49}
	20×4 [6]	1.8×10^{16}	5.94×10^{-17}	-1×10^{-18}	7.52×10^{-44}
	1×0.5 [1]	2.41×10^{14}	4.58×10^{-16}	-1×10^{-18}	3.90×10^{-44}
	1×0.7 [1]	2.38×10^{14}	3.2×10^{-16}	-1×10^{-18}	1.69×10^{-45}

6.6 Comparison between the Normalized Number and Mobility Fluctuations for the Large Dimension Devices

In this section, comparisons are made for the normalized number and mobility fluctuations among the wafers. The number and mobility fluctuations are normalized with respect to W, L, and T_{OX}. The oxide layer thickness for the wafers x2388, x2550, and x2396 are 8.7 nm, 12.1 nm, and 12.7 nm, respectively. The normalized number and mobility fluctuations are plotted in Fig. 6.15 for the devices with larger dimensions as a function of I_{DS}. N_T values from Table 6.2 contribute to the normalized number and mobility fluctuations. The parameter, α, determined using Eqn. 6.6 (the fitting parameters, α_0 and α_1 are from Table 6.2), is used for the calculation of the normalized mobility fluctuations.

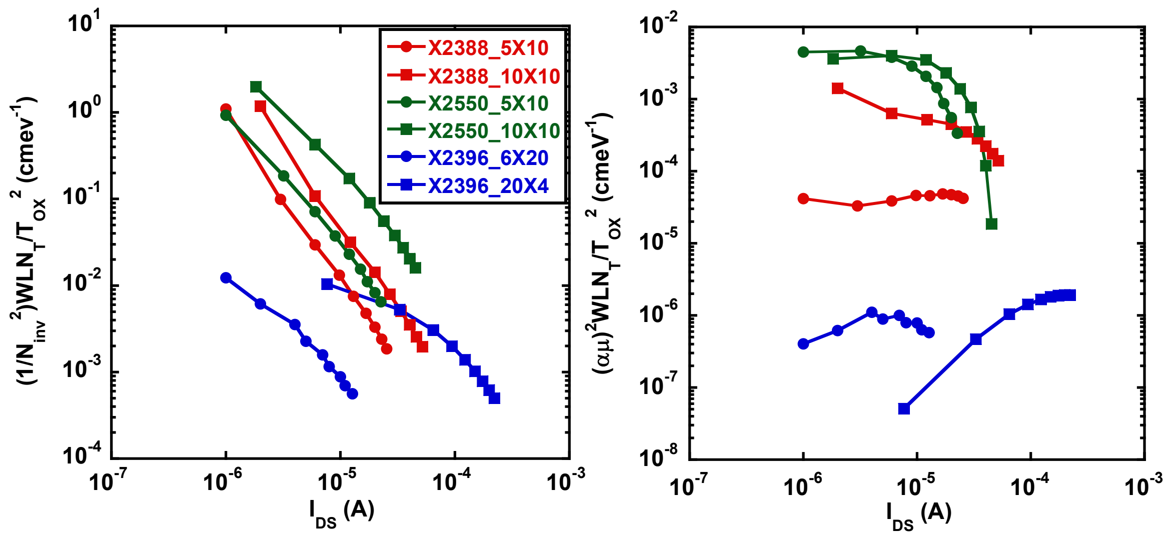


Fig. 6. 15 Comparison of normalized (a) number and (b) mobility fluctuations as a function of I_{DS} for different dimensions of devices across the wafers. The dimensions of the wafers are: x2388, x2550 (W×L= 5 µm×10 µm, 10 µm×10 µm), and x2396 (W×L= 6 µm×20 µm, 20 µm×4 µm).

From Fig. 6.15 (a), it is observed that the nMOSFETs from wafer x2396_6×20 represent a relatively lower amount of normalized number fluctuations than the other two wafers. The trap density N_T of x2396_6×20 is significantly lower than N_T from x2550 and x2388 (Table 6.2). In addition, the $1/N_{inv}^2$ value is also lower for x2396_6×20 than the other two wafers. These two factors, comparatively lower N_T and $1/N_{inv}^2$ leading to the observation of the lowest normalized number fluctuations for x2396_6×20. On the other hand, nMOSFETs from wafer x2550 show a slightly higher normalized number fluctuations than their

x2388 counterparts with the same area. The comparatively higher N_T of the nMOSFETs from x2550 is the reason behind this (Table 6.2).

In Fig. 6.15 (b), nMOSFETs from x2396 clearly exhibit the lowest amount of normalized mobility fluctuations, while nMOSFETs from x2550 represent the highest amount of normalized mobility fluctuations. The calculated α (utilizing Table 6.2 and Eqn. 6.5), corresponding to the Coulomb screened scattering, is the dominant contributing factor behind the different amounts of normalized mobility fluctuations observed in these wafers. MOSFETs from x2396 have the lowest α, while MOSFETs from x2550 have the highest α. Besides the impact of α, trap density N_T also plays an important role here behind the differences in the normalized mobility fluctuation levels since $N_{T_{2550}} > N_{T_{2388}} > N_{T_{2396}}$.

In this chapter, experimentally obtained 1/f noise data from the nMOSFETs of different wafers are studied. Number fluctuations act as the dominant 1/f noise mechanism among the wafers. The 1/f noise data are normalized with respect to the channel width, length, and oxide layer thickness, and compared among the larger dimension devices across the wafers. Poly gate annealing at 900° C, boron fluoride (BF) implantation, and sintering using H_2 lead to the lowest normalized 1/f noise in x2396. On the other hand, using fluorine (F) instead of the BF implantation leads to the highest normalized 1/f noise in x2550. Although for x2388 we have no information about the implantation profile and sintering technique, the normalized 1/f noise is intermediate instead of being the highest among the wafers. Poly gate annealing at 800° C may play a dominant role behind that intermediate noise level for x2388. Trap density and fitting parameters of the screened scattering coefficients are determined from the normalized 1/f noise data by implementing the Levenberg-Marquardt algorithm-based curve fitting technique. Comparatively lower trap density and higher inversion layer charge density led to the lowest normalized number fluctuations for x2396_6×20. On the other hand, the lowest screened scattering coefficients and the trap density among the wafers contribute to the lowest amount of normalized mobility fluctuations in x2396.

Chapter 7: Conclusions

Random telegraph signals (RTS) result from multi-phonon assisted tunneling of the channel carriers into the defect sites present on the Si-SiO_2 interface or inside SiO_2 of a MOSFET. Analyzing RTS has been important not only to study the process-induced defects but also to examine the stress-generated oxide defects in the MOSFETs, which are created during operation. Typically, accelerated operation conditions are mimicked by electrically stressing the devices for much shorter periods of time. Channel hot carrier (CHC) stressing has resulted in the worst degradation in MOSFETs. Although being reported as the most degrading mechanism, there was not as much interest in investigating the impact of CHC in pMOSFETs compared to nMOSFETs due to the smaller impact ionization rate of the charge carrier as well as the higher Si-SiO_2 energy barrier for holes compared to electrons.

We investigated the effect of CHC stressing on the process-induced and stress-induced traps by analyzing RTS. Experiments were conducted at room temperature for stressing times up to 2000 seconds. Then the CHC stressing effect was studied on different RTS parameters such as screened scattering coefficient, RTS amplitude, capture time, and capture cross-section. The negative shift of the threshold voltage with stressing indicated the generation of an increased amount of fixed positive oxide charges. Generally, there is charge screening between the trapped charge and the channel carriers. Furthermore, the newly generated fixed positive oxide charges contributed to additional charge screening on the traps. Therefore, the Coulomb screened scattering coefficient decreased with stressing. This reduction of the screened scattering coefficient with CHC stressing led to lower mobility fluctuations. As a result, RTS amplitude increased with stressing for the hole-attractive trapping centers in SiO_2. Contrary to the classical three-dimensional treatments, two-dimensional quantum mechanical treatments were carried out here for the small-scale devices because of the quantized carrier motion in a perpendicular direction to the Si-SiO_2 interface. The two-dimensional mobility fluctuations model was implemented successfully for the very first time in the case of CHC stressing for pMOSFETs to calculate the screened Coulomb scattering coefficient theoretically. The comparison between the theoretically and experimentally obtained screened scattering coefficients pointed towards the impact of the newly generated fixed oxide charges. The reported trap capture cross-section increased with stressing time for the stress-induced traps, most likely resulting from the reduction of the trap relaxation energy. The behavior of the capture cross-section led to the decrease of the average capture time for the stress-induced defects with stressing. However, the trap relaxation energy could not be determined by conducting experiments only at room temperature. Moreover, it was also not possible to identify the responsible defect sites in SiO_2 from the room temperature experiments.

To remedy these shortcomings, CHC stressing effects were investigated under the variable temperature experimental setup to identify the defect sites as well as to examine additional RTS parameters. CHC stressing was conducted on pMOSFETs from room temperature down to 215 K, up to 1200 seconds. In all four examined pMOSFETs, faster stress-induced traps were reported than their process-induced counterparts. Larger trap capture cross-sections of the stress-induced traps were responsible for this behavior. Additional trap parameters such as capture activation energy, emission activation energy, change in enthalpy, and entropy were quantified from the variable temperature RTS measurements. A pronounced difference was reported in the change in entropy $\left(\Delta S/k_B\right)$ between the process- and stress-induced traps. Lower $\Delta S/k_B$ values were reported for the stress-induced traps, compared to the process-induced ones. This difference in $\Delta S/k_B$ value implied the possibility of a different type of structural defect to be responsible for the stress-induced traps than the process-induced ones. The parameters, namely structural relaxation energy and the trap energy level with respect to the oxide valence band edge, helped to identify the defects. The disassociated III-Si and Hydrogen bridge defects were recognized as the hole trapping centers in SiO_2.

Alongside RTS, flicker (1/f) noise has been one of the prominent noise sources in MOSFETs. The presence of multiple traps in MOSFET results in a 1/f noise power spectral density (PSD); we find this by adding up Lorentzian waveforms from different RTSs with different corner frequencies. Here 1/f noise PSDs were calculated at different gate-source overdrive voltages in nMOSFETs from three technologies. It was evident from the experiments that 1/f noise followed the number fluctuation theory, as the current noise PSD followed the $\left(g_m/I_{DS}\right)^2$ pattern in the nMOSFETs. Later, the PSDs were normalized with respect to the channel length, width, and oxide thickness in different wafers. Discussions were carried out to correlate the normalized 1/f noise PSD with the fabrication steps of the wafers. Later, these normalized 1/f noise PSD data were curve fitted to the unified flicker noise model to extract the trap densities and screened scattering coefficients across the wafers. These experimentally obtained trap densities and screened scattering coefficients were incorporated to compare the normalized number and mobility fluctuations among the wafers. The outcomes from the correlation between the experimental 1/f noise data and the fabrication steps proved useful in improving the gate oxide growth conditions and passivate the defects responsible for 1/f noise in the MOSFETs.

To sum up, process- and stress-induced traps were investigated here in detail to understand the impact of CHC stressing in pMOSFETs. For this reason, the trap properties were studied by analyzing the RTS parameters. The novelty of our work here lies in the fact that we incorporated the two-dimensional mobility fluctuations model of the screened Coulomb scattering coefficient for pMOSFETs for the very first time in

the case of CHC stressing. The two-dimensional mobility fluctuations model was utilized to calculate the theoretical screened Coulomb scattering coefficients and compare them with the experimentally determined screened Coulomb scattering coefficients. Moreover, through variable temperature RTS measurements, process- and stress-induced defect centers were identified as disassociated III-Si and Hydrogen bridge in SiO_2 of the pMOSFETs under CHC stressing. However, there are several other electrical stressing mechanisms, such as drain avalanche hot carrier (DAHC) and negative bias temperature instability (NBTI) stress. The impact of these mechanisms in pMOSFETs can also be investigated in the future by similarly analyzing the RTS parameters. The responsible defect sites can also be identified in that regard. Besides, RTS analyses can be conducted to investigate defects in some high-k dielectric materials, i.e., HfO_2, ZrO_2 instead of SiO_2 gate oxide in MOSFETs.

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