STUDY OF SAC SOLDER INTERCONNECT PARAMETERS IN MICROELECTRONIC PACKAGING AND THEIR EFFECTS ON ELECTROMIGRATION FAILURE MECHANISMS

by

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DISSERTATION

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DEDICATION

To my family, with the hope that I have made them proud.

To my husband, for patiently supporting me and loving me unconditionally throughout my ambitious endeavors.

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ABSTRACT

Study of SAC Solder Interconnect Parameters in Microelectronic Semiconductor Packaging and their Effects on Electromigration Failure Mechanisms

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As the shrinkage of electronic devices becomes more appealing, so do their high capacity and efficiency. This demand for ever-shrinking sizes of electronic devices follows the trend predicted by Moore's Law. To achieve smaller devices, reduced sizes of solder joints, Cu traces, Cu pads, and other components in packages are implemented with tighter tolerances for geometries and layouts. With each incremental change in dimension or material, new reliability challenges emerge. Electromigration (EM), the directional diffusion of atoms with the flow of electrons, has been an inevitable reliability concern for microelectronic device packaging. It is one common failure mechanism in wafer-level chip scale packages (WCSP). EM is heavily influenced by the presence of current crowding, resistance, and subsequent Joule heating (JH). As the current flows through an integrated circuit (IC), the electrons flow in the opposite direction, causing a mass diffusion of metal atoms from the cathode end of a solder joint to the anode end of a solder joint either by dissolution at the interface or by migration within the bulk. As this directional EM diffusion occurs, vacancies in the conductive material lattice begin to form. In classical EM failure, these voids propagate until they reach across the entire solder cathode interface, and EM failure finally occurs by open circuit.

Failure by EM is especially exacerbated by the demand for ever-decreasing device sizes and increased efficiency and power carrying capabilities. Appealing to these demands requires smaller IC vias and increased densities of current paths, leading to larger current densities as high current flows through thin IC components. There are a number of methods employed by industry to mitigate the effects of EM, including the implementation of an under-bump metallization (UBM) layer, solder shape and size, and diffusion barriers. A UBM is essentially a layer of Cu that is situated between the Cu trace on the silicon chip substrate and the solder joint mounted onto the printed circuit board (PCB), through which current is routed to the solder joint, to the UBM and the redistribution layer (RDL), and finally, to the chip. Another mitigation effort is the implementation of a polyimide (PI) layer situated between the RDL and the UBM with limited sized openings to control the current crowding at the UBM/SAC interface. The following studies aim to understand the effects of such design modifications' effects and in-use conditions on theoretical mechanisms behind the EM failure in device ICs, paying close attention to current crowding, JH, and localized stress on the cathode end of the device under test (DUT) solder bump, where EM voiding occurs.

The research presented in this dissertation is intended to explore the fundamental reasoning behind EM experimental results reported by Yi Ram Kim et. al. [1-3] through the finite element method (FEM) with four key objectives: 1) Identify the fundamentals supporting whether a certain current flow configuration may be more favorable over another in early or later failure; 2) Determine the fundamentals supporting the hypothesis that there is an optimal UBM thickness that can extend the lifetime of a DUT in an IC; 3) Determine the fundamental mechanisms behind how the duty factor (DF) of direct current (DC) "on time" may accelerate or decelerate the failure rate in DUTs incorporated in WCSPs; 4) Investigate how the alteration of a PI opening impacts the

current crowding and stress in the DUTs incorporated in WCSPs. This dissertation presents key findings in our studies, especially those which lead to a better understanding of metallurgical and structural mechanisms affecting EM failures. Compressive stress has been found to benefit the WCSP interconnect reliability against EM mechanisms as it blocks the void growth across the interface between a SAC solder joint and a UBM. However, those have been determined to be limited by the current crowding and JH. Interconnect designs and parameters were further investigated through FEM to identify those which best benefit WCSPs against EM failure, such as UBM thickness and controlled PI openings. Supporting for ideal current conditions such as symmetry DC, asymmetry DC, and pulsed-DC under low and high-frequencies was also furnished. Future work, including an investigation of plasticity effects under non-DC conditions and comparing different solder joint geometrical parameters, are also suggested in this dissertation.

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CHAPTER 1: INTRODUCTION

1.1 Background and Significance

One of the most significant challenges presenting in microelectronic packaging is the reliability of interconnect technology. Even more challenging is the design for smaller, thinner electronic devices, driving the demand for smaller microelectronic components. Various structural designs such as materials, integrated circuit (IC) component size and shape, and ratios of materials to mitigate coefficient of thermal expansion (CTE, α) mismatch are implemented in order to appeal to the demand for efficient current distribution through the chip package [1, 4]. Many challenges arise when trying to obtain optimal package designs within the confines of budgets and available technology, such as thermomigration (TM), chemical migration, electrochemical migration (ECM), and, more relevant to the research presented in this dissertation, electromigration (EM). TM is the transport of material, resulted by a temperature gradient within a solid. Chemical migration is the transport of material, resulted by a chemical gradient within a solid. ECM is the ion transport of electrically conductive material between adjacent metal conductors, forming dendrites. EM is the transportation of metal ions from the cathode (-) end to the anode (+) end within the electrically conductive solid as electrons collide with the metal ions, resulting in voids caused by displaced material. EM is affected by current density and temperature. EM in interconnects and packages is also significantly affected by current crowding and JH. EM may be aided or obstructed by the amount of compressive stress generated by the CTE mismatch with JH. EM failure rates may also be impacted by microstructural characteristics such as grain orientation and diffusivity of an atom of one material through the lattice structure of another material. The significance of these phenomena is that the reliability of packages depends on their resistance

against the aforementioned failure mechanisms. This research has been done in partnership with industry liaisons and has contributed to an enhanced understanding of EM failure mechanisms and how particular package designs and materials selection may benefit reliability of packages and their internal components.

1.2 Research Motivation and Scope

The primary objective of this research is to gain a greater understanding of the EM failure mechanisms which occur when a current load is flowing through a solder joint in a wafer-level chip scale package (WCSP). The finite element method (FEM) is the key method which will be implemented to understand the fundamental mechanism driving the EM failure in solder joints used in WCSPs. FEM techniques are useful in capturing the physics occurring within electronic packages, including WCSPs, which cannot be identified by traditional failure analysis methods such as microstructural characterization using a scanning electron microscope (SEM), energy dispersive x-ray (EDX), or electron back-scatter electron diffraction (EBSD).

Consumers are attracted to thinner electronic devices with greater capabilities and efficiency. This device shrinkage trend follows Moore's Law, developed by Gordon Moore. It has an empirical relationship between the device shrinkage and the increased transistor density in an IC to meet consumer demands over time. According to Moore's Law, the number of transistors in a densely-packed IC doubles approximately every two years. The law is based on an observation, but it also projects predictions into the future. This relationship is presented in a semi-log plot of transistor counts for microprocessors over time as new products are released onto the market. As this trend progresses, the cost to develop each new device increases and industry is met with a number of other physical challenges. The price tag can be a limiting factor to production and

innovation, which can have economic consequences. To challenge the increase in costs, new materials are explored. Despite these efforts, some experts, including Moore, speculate that the model is becoming obsolete as physical limitations are expected to occur. Forecasters expect that Moore's Law will be phased out by 2025. To meet this challenge head-on, industry is exploring new chip and package architectures, quantum computing, and AI machine learning. A drawback to Moore's model, and similar empirical models, is that they cannot perfectly predict the lifetime of solder bumps as there are many underlying physical failure mechanisms which occur in solder joints. Reliability test data presented in this sort of model provides a statistical estimate of a

Figure 1 Moore's Law presented in an exponential growth of the number of transistors per square inch on an integrated circuit (IC) [6].

lifetime for packages but does not tell the story of the mechanism of failure [5].

As industries work to fulfill the growing demand in device shrinkage with higher transistor density and higher efficiency, smaller components with smaller IC geometries and a reduction in metallic material are utilized, carrying a higher current density load, sometimes exceeding 10 kA/cm^2 to meet the increase in power demand. Thus, solder joints are something of a weak point

among electronic package components. The resulting current crowding is the driving force behind EM, where the directional flow of electrons (electron wind) travels in the opposite direction of the current flow. For EM to commence, this electron wind has a greater force than the electrostatic force. In WCSPs, there is a polarity effect such that the electron wind forces the directional flow of metal atoms from the cathode (-) end of the DUT solder joint to the anode (+) end of the DUT solder joint. These electrons collide with the conductive atoms, driving them through the SnAgCu (SAC) solder joint lattice. As these atoms are forced to move toward the anode end of the solder joint, vacancies are formed in the SAC lattice on the cathode end of the solder joint, once there are not enough metal atoms left to fill the vacancies [7, 8]. At this point, the vacancies in the SAC lattice can lead to a localized tensile stress within the lattice. That combined with the loss of material allows a void to nucleate at the cathode end. Over time, the void propagates along the SAC/substrate interface, commonly resulting in failure by open circuit. The electronics industry has challenged this failure mechanism through a number of technologies, one primary focus in this study being the implementation of a Cu UBM layer between the substrate and the SAC solder joint, prolonging the EM lifetime. In cases where the UBM is too thin, the Cu is consumed quicker than in cases where the UBM is thicker; however, there is a limit to the benefit that a thicker UBM may add to the longevity of the solder joint, the effects of which are studied in this proposed research. Another mitigation technique studied in this research is the use of a polyimide (PI) layer between the UBM and redistribution layer (RDL) with a controlled opening diameter through which current may pass to control the current crowding location and stress at the DUT/UBM interface, the typical EM failure site in WCSP solder interconnects.

Without the presence of PI layer and openings, the current flows through the DUT solder joint, it typically consolidates at the top corner of the solder joint, where the current exits the joint.

Consolidated current density is also referred to as current crowding. Depending on the current flow configuration, the current crowding may vary. With current crowding comes JH. When a device experiences JH, the materials used in the devices all expand with the change in temperature, which can be gauged from the coefficient of thermal expansion (CTE). Mismatches in CTE among package components is a primary contributor among failure mechanisms and thus premature failure in electronic packages, as the difference in expansion rate between materials which share an interface causes stress generation. CTE mismatch is the driving force behind catastrophic failures such as delamination, and fatigue crack formation and propagation. Additionally, the level of stress generated by the CTE mismatch may also play a role in either slowing EM failure kinetics or enhancing them by stress-induced voiding. This, in turn impacts the mean-time-to-failure (MTTF) model, which is used to predict the EM reliability of a microelectronic package.

The problem statement is thus how various WCSP parameters and conditions impact the current crowding, JH, and stress development and how these fundamental thermal-structural-electrical phenomena affect EM reliability of the weakest links of package components: solder joints. The research hereby presented in this dissertation has been inspired by the intriguing findings obtained by Yi Ram Kim et. al. and the outcomes are aimed at gaining a fundamental understanding behind EM failure kinetics and mechanisms observed during comprehensive EM experiments [1-3]. The four key objectives are as follows:

1) Identify the fundamentals supporting whether a certain current flow configuration may be more favorable over another in early or later EM failure ranks;

2) Determine the fundamentals supporting the hypothesis that there is an optimal UBM thickness that can extend the EM lifetime of a DUT in an IC;

3) Determine the fundamental mechanisms behind how the duty factor (DF) of direct current (DC) "on time" may accelerate or decelerate the EM failure kinetics in DUTs incorporated in WCSPs;

4) Investigate how the alteration of a PI opening impacts the current crowding and stress in the DUTs incorporated in WCSPs.

Simply put, the objectives of this research are to establish a baseline in gaining an understanding of the fundamental impacts of these variables on the EM reliability through FEM, to relate these understandings to EM experimental results, and to give meaningful insight in package design advancements. There are limitations to the capabilities of FEM in these applications, so the overall aim is to understand the behavior of the DUTs rather than producing exact values and plots. Each of these aims are related as they are intended to gain understanding of EM reliability of WCSPs with various design parameters (UBM thickness and PI opening) used to improve their reliability and under different testing conditions (current flow configuration and constant vs pulsed-DC). The significance of this research is its potential future applicability to package design evolution in industry. The general approach, theoretical procedures and methods, discussion, and conclusion will be presented for each one of the project scopes.

CHAPTER 2: LITERATURE REVIEW

This chapter focuses on the package of interest for the scope of this research, typical EM failure mechanisms, typical mechanical failure observations in microelectronic packages, microstructural effects on EM and mechanical failure phenomena, and mitigation efforts deployed by industry to meet these challenges. Also discussed is the background of the FEM approach used to understand the stress and EM mechanisms occurring in solder interconnects during EM testing.

2.1 Wafer-level Chip Scale Package and Power-Wafer-level Chip Scale Package Technology

Wafer-Level Chip Scale Package (WCSP or WLCSP) technology is the packaging of an integrated circuit (IC) at the wafer level. This goes against traditional package technologies, which assemble individual package units after dicing them from a wafer. It is essentially comprised of a flip-chip assembly of a chip package with a Si chip imbedded in an epoxy of some sort, the bottom of which has exposed conductive metal (usually Cu) substrates or a redistribution layer (RDL) which route current through the chip. The metal substrates are bonded to a printed circuit board

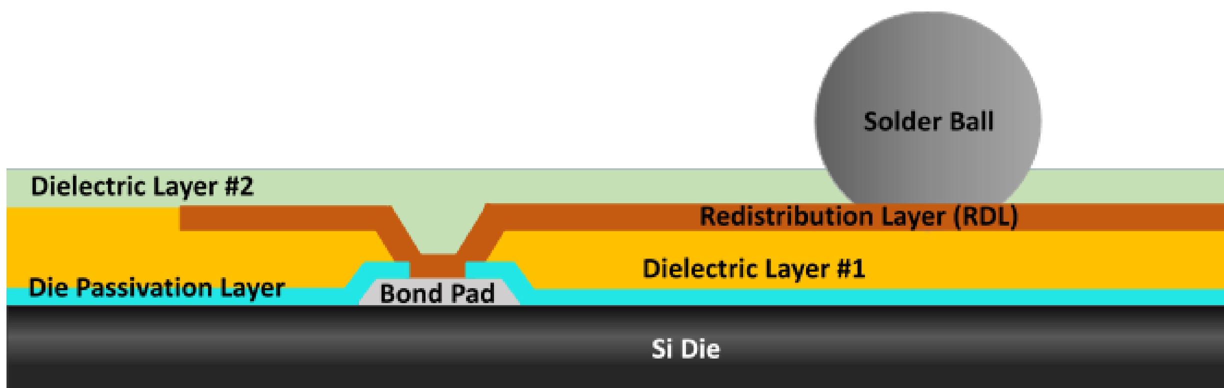

Figure 2 Cross-sectional layout of a WCSP, typically consisting of a Si die, die passivation layer, dielectric layers, redistribution layer, and solder ball.

(PCB) using a ball grid array (BGA) pattern of solder bumps. **Figure 2** illustrates a schematic of the WCSP with the layers on the Si die side. In some cases, an underfill layer surrounds the solder bumps and is sandwiched between the Si chip package and the PCB as a means to reduce the effects of CTE mismatch and to provide additional structural support. The chip scale package (CSP) is defined as a package that is less than 1.2x the size of the chip itself, and more recently, it's actually a 1:1 ratio between the chip size and the package size. Reducing the size of the package allows many advantages, including a small footprint of the package, lower parasitics (especially at high frequency use conditions), and an increase in inputs/outputs per unit area than the BGA packaging typically allows.

WCSPs have been advantageous for testing purposes, as well as accelerated manufacturing purposes. They allow for the integration of the wafer fabrication, packaging, test, and burn in at the wafer-level to streamline the manufacturing process and get the product to market and into consumer devices faster. One of the most popular applications of WCSPs are smart phones, inside which multiple WCSPs are integrated. The functions of WCSPs include sensing, power management, and wireless capabilities. As the demand for smaller, thinner devices with higher efficiency and power capabilities persists, the size in these WCSPs shrink and they are subjected to higher current densities during in-use conditions which introduces a number of reliability concerns for extreme in-use conditions.

2.2 Electromigration Failure in Wafer-Level Chip Scale Packages

Sn-Pb solder materials, particularly eutectic 63Sn-37Pb, has historically been favorable in the electronics industry. Eutectic Pb-containing solders were very attractive for their low cost, low melting temperatures, high ductility, wettability, and compatibility on various substrate surfaces and devices, and considerably decent reliability [9]. In 1986, Congress amended the Safe Drinking Water Act. This amendment prohibited the use of lead in pipes but more importantly for the electronic industry, solder joints and solder flux [10]. Not to mention, a further push to unleaded solder originated from the European directive in 2002 and UK regulation in 2006. To fulfill the limitations of this legislation, the electronics industry commonly utilizes different concentrations of Sn, Ag, and Cu in SAC solder joints. There has not yet been a perfect solder alloy that replicates the reliability and material properties of lead-based solder alloys; however, there are a number of

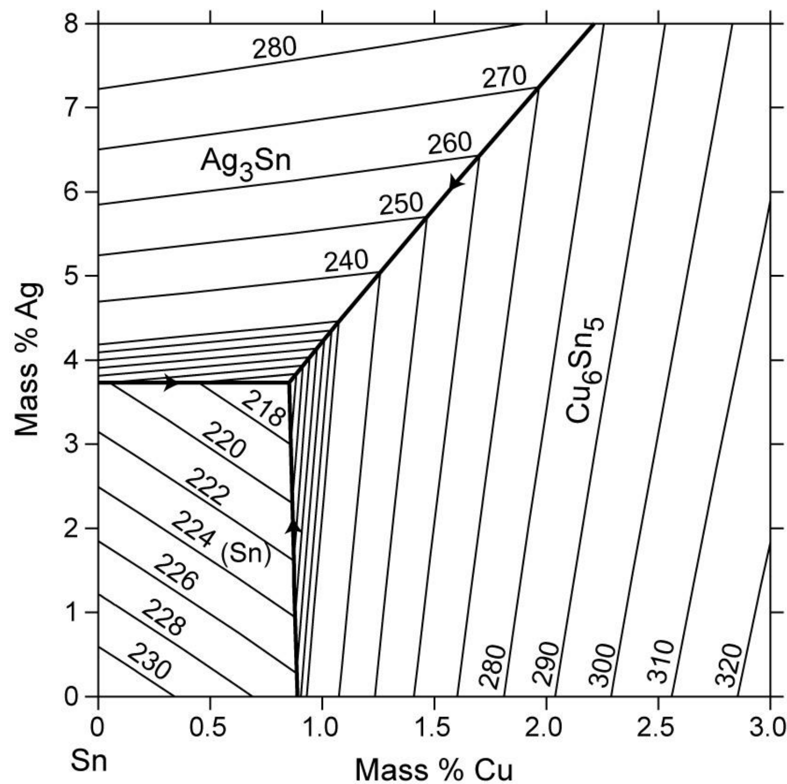

Figure 3 Sn-Ag-Cu ternary phase diagram [11].

substitution materials that have been applied in industry. **Figure 3** is a ternary Ag-Cu-Sn system by which various SAC solder alloy compositions are selected. Typically, the Pb-free solder materials would be Sn-enriched. The solder material studied in this research is Sn3.8Ag0.7Cu. The implementation of a new kind of material, such as SAC rather than Pb-Sn solder materials, introduces new complications, one of which is EM.

As discussed previously, EM is the directional transport of metal atoms in a conductor from one end of the conductor, the cathode (-), to another, the anode (+), due to current flow. It is a common reliability concern for IC used in microelectronic packaging. Simply put, as current flows from the anode end of the solder joint to the cathode end of the solder joint, electrons flow in the opposite direction: from the cathode end of the solder joint to the anode end of the solder joint.

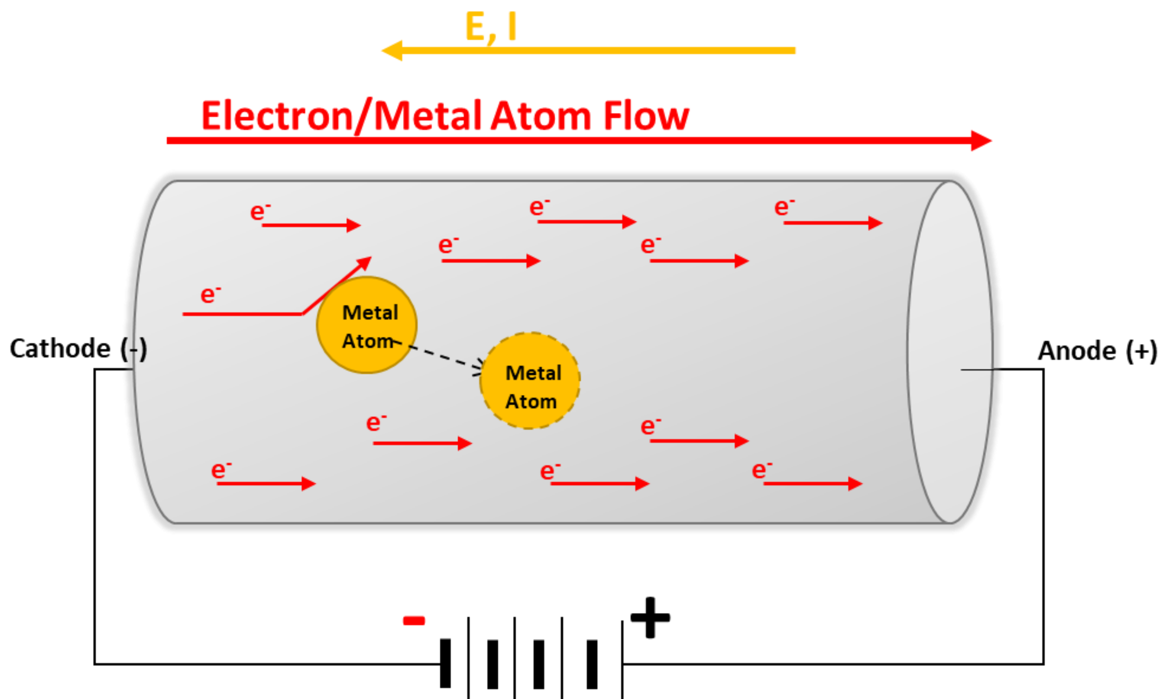

Figure 4 Illustration of electrons transferring momentum to the metal atom, driving the electromigration of the metal atoms from the cathode end to the anode end of the conductive solid.

Mechanisms of EM can also be explained by two counteracting forces: 1) activated and positively charged metal ions are forced toward the cathode by the electric field, accounting for the electrostatic force or Coulomb force, and 2) negatively charged electrons move toward the anode and transmit an impulse to the metal ions, accounting for the electron wind force. In the lattice structure of the metal IC, a flux of ions flows parallel to the electron wind. With current densities high enough, the electron wind force may exceed the activation energy (E_a), and EM follows. The mass flow that occurs takes place along interfaces, at grain boundaries and surfaces, and by volume diffusion. Grain boundary and interfacial diffusion are the dominating transport mechanisms under operating thermal conditions. **Figure 4** illustrates the electron collision with an atom which diffuses through the alloy. The momentum transfer from the electrons flowing through the IC forces these metal atoms to migrate. As this occurs, atom depletion occurs at the cathode end and atom accumulation occurs at the anode end.

The classical mechanisms of EM in DC conditions are void nucleation and void propagation. The electron flux drives the flow of the Cu atoms by dissolution at the interface between the SAC solder joint and the Cu UBM or by migration in the bulk until vacancies form in inhomogeneous regions, also known as the EM flux divergence region. **Eq. 1** below defines the EM flux, J, which is caused by an electron wind force induced by electric current.

$$J = Nz^{*}e\rho j\frac{D}{kT} \qquad \textbf{[Eq. 1]}$$

Where N is the atomic concentration, Z* is the effective valency of the diffusing species, *e* is the electron charge, *j* is the current density, ρ is the electrical resistivity, T is the absolute temperature, and k is the Boltzmann's constant. The equation is derived from Fick's law of diffusion to account for the diffusivity times the driving force.

Cu diffuses preferentially in regions of high current crowding and JH, where the local EM flux divergence is highest. Voids may originate at the grain boundaries, caused by vacancies due to the atomic depletion induced by EM. EM drives vacancy diffusion, thus leading to vacancy accumulation on the cathode end of the interconnect and vacancy depletion on the anode end of the interconnect. Vacancy saturation, which occurs once a critical concentration of vacancies is reached, leads to the nucleation of a void. The rate at which a void may nucleate depends on many factors such as the SAC alloying elements and concentrations, the solder joint size and shape, whether or not there is a presence of a diffusion barrier (such as a Ni plating on the cathode end of the solder joint), the rate of the interface reaction leading to the growth of the intermetallic compound (IMC), and the degree of JH [7, 8 12, 13].

Void nucleation relies on the competition between the vacancy flux and the atomic flux in the presence of an electrical field. Conductive material such as Cu migrates through the SAC solder interconnect by way of vacancy exchange. Expanding on **Eq. 1**, we reveal the atomic flux and the vacancy flux, which oppose one another under an electrical field, in **Eq. 2** below, where J_v, J_a, C_v, C_a, D_v, D_a, E, kT, Z^*, e, and a represent the vacancy flux, atomic flux, vacancy concentration, atomic concentration, vacancy diffusivity, atomic diffusivity, activation energy, thermal energy, effective charge, and the elementary charge, respectively.

$$J_v = C_v \frac{e|Z^*|D_a}{kT} E = -C_a \frac{e|Z^*|D_a}{kT} E = -J_a \qquad \textbf{[Eq. 2]}$$

The void nucleation acts as a catalyst for failure. Once a void nucleates, the rate at which it propagates depends on mechanical factors such as stress at the void tip. Simultaneously, the remaining material at the interface becomes more vulnerable as it is subjected to a higher amount of current density. As the void grows, the conduction area decreases, leading to higher resistance, higher current density at the void front, and localized JH. Once the void length reaches a critical length, runaway failure is observed in the tested samples, as the percent change in resistance approaches infinity. This void propagation progresses across the entire joint on the cathode end, situated at the interface between the SAC solder joint and the Cu UBM, resulting in an open-circuit failure. **Figure 5** illustrates the void nucleation and propagation at the interface between the Cu UBM and the SAC solder bump, as electrons flow from the cathode end of a solder bump to the anode end of a solder bump.

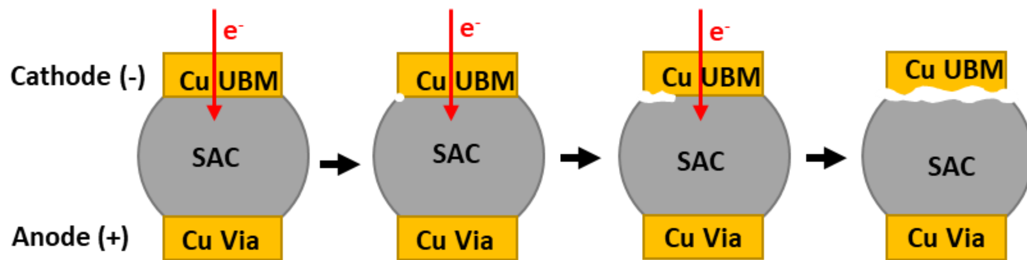

Figure 5 Illustration of void nucleation and propagation at the interface between the Cu UBM and the SAC solder bump.

For decades, scientists have expended efforts to define EM mechanisms and the reliability of devices against EM failure. There are a number of mechanisms behind EM failure kinetics and reliability, many of which remain a mystery. The most well-known method of estimating EM kinetics is Black's model, developed by James R. Black. Black developed a semi-empirical equation in the late 1960's to predict the reliability of solder material against EM. The mean time to failure (*MTTF*) is proportional to the constant based upon the cross-sectional area of the

interconnect (A), the activation energy (E_a), Boltzmann's constant (k_B), temperature (T), the current density (j), and the current density exponent (n), as defined by **Eq. 3.**

$$MTTF = \frac{A}{j^n} \exp\left(\frac{E_a}{k_B T}\right) \qquad \textbf{[Eq. 3]}$$

E_a and n are determined experimentally, so this equation is valid only to specific testing conditions and packages [14]. Black's model is commonly modified to apply to various package types, depending on interconnect size, material, and geometry. With even the smallest changes in IC size, geometry, or material, this reliability model changes. It may also be modified to apply to certain use conditions. It is necessary to understand the fundamental mechanisms behind EM failure to accurately predict a device's reliability.

Because a separate test must be conducted under at least three conditions for each adjustment to package components in order to obtain useful information that will allow each variable to be determined, the process for predicting and improving the reliability of microelectronic packaging is costly in terms of time, manpower, resources, and money. By identifying relationships and key mechanisms which drive the EM failure, one can reasonably narrow down testing parameters in order to reach an optimal design within certain cost and technology limitations. The purpose of this study is to identify mechanisms which either contribute to failure or prolong failure in WCSPs. The primary method of gaining insight in the failure mechanisms which affect EM failure kinetics is through FEM. Results obtained through FEM analysis may be related to EM experimental results to identify a physical pattern in which the EM failure kinetics are impacted. Identifying these key mechanisms may provide a fundamental understanding of the EM failure mechanisms, and how to influence package components to obtain optimal designs within modern constraints.

2.2.1 Current Stressing and Mechanical Mechanisms in Electromigration

One of the most concerning aspects impacting the reliability of microelectronic packaging is the stressed caused by CTE mismatch between materials which are bonded to one another. Each material has a different CTE. When two different materials are bonded together, one material which shares a contact with another may expand farther, resulting in tensile stress on one material and compressive stress on the other while the material with a smaller CTE restricts the material with a greater CTE. The effects of the CTE mismatch are impacted by the ratio of the material present. The impacts of the CTE mismatch will be discussed further in detail in the following section; however, for a brief understanding, **Figure 6** fulfills an illustration purpose.

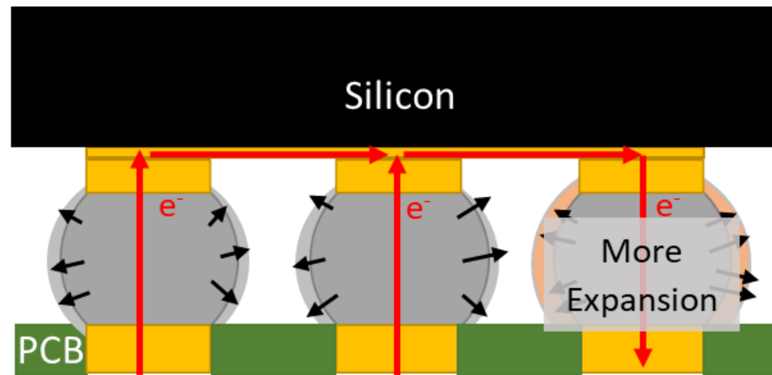

Figure 6 Illustration of the DUT expansion and how it compares to the support bump.

Material	Coefficient of Thermal Expansion
Copper (Cu)	~17.0 ppm/°C
SAC (SnAgCu) Solder Alloy	~24.0 ppm/°C

Table 1 Summary of Coefficient of Thermal Expansion of Cu and SAC.

Figure 6 illustrates the expansion of the DUT, as the surrounding bumps do not expand at the same rate. The DUT shares a contact with the Cu via and the Cu UBM. **Table 1** lists the coefficient of thermal expansions for Cu and the SAC solder alloy, which are bonded together in the electronic package. The smaller CTEs in more rigid materials like Si and PCB also impact the stress of the more ductile Cu and Sn. With the difference in CTE expansion, a significant amount of shear stress is expected to develop on the DUT. Meanwhile, a significant amount of compressive stress is expected to develop in the DUT due to the difference in JH among solder joints. Since the surrounding support bumps do not expand at the same rate, they are under tension since the DUT is expanding more than they are. The support bumps act as a constraint, as they hold the package together while the DUT expands, further compounding the stress developing on the DUT.

Stress generation, especially shear stress, can sometimes be problematic for mechanical reliability of semiconductor packages because it can cause delamination of the solder joint from the substrate, delamination of a potential PI layer or encapsulation from the Si die, cratering in the Si die, and so forth. When it comes to reliability of semiconductor packaging against EM failure, however, compressive stress may be beneficial as it concentrates on the void front as EM commences, blocking the void growth. There are, however, limitations to this benefit, which will be discussed in coming sections.

2.2.2 Intermetallic Compound Growth Observed in Electromigration

As we know from their differing activation energies, Cu diffuses quicker through the Sn lattice of the solder joint, whose phase β-Sn is body centered tetragonal (BCT), than Sn does. The diffusion rate is accelerated in areas of high current crowding and JH. JH, associated with the current crowding in different regions of the solder joint, plays an important role in EM failure kinetics. JH can be correlated to the current and the resistance of a material. The higher the resistance, the higher the JH. Similarly, the higher the current level, the higher the current crowding. **Eq. 4** demonstrates the proportional relationship between the power of thermal energy (P), the current (I), and the resistance (R) within the conductive material.

$$P \, \alpha \, I^2 R \qquad \textbf{[Eq. 4]}$$

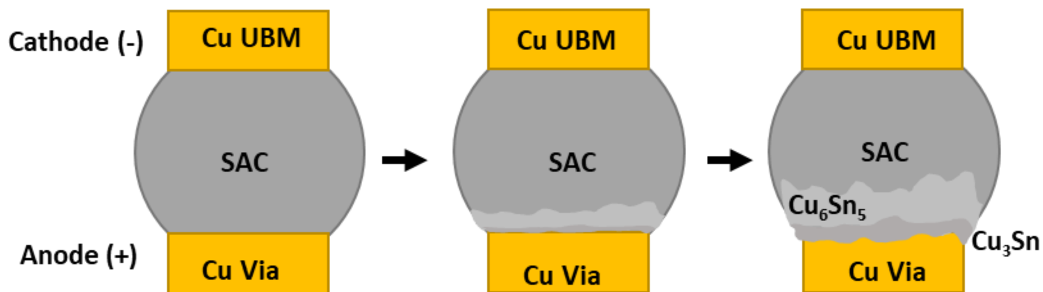

Figure 7 Illustration of IMC formation and growth at the anode end of the solder joint the Cu concentration increasing until the Cu3Sn IMC is formed near the Cu pad/lead frame interface.

In WCSPs, SAC solder ICs are assembled between a Cu UBM substrate and a Cu pad/lead frame. IMCs form at the anode end of the solder joint. The IMC progresses from Cu_6Sn_5 and evolves to Cu_3Sn as Cu continues to diffuse, leading to a higher concentration of Cu towards the Cu pad/lead frame. **Figure 7** illustrates the development of the IMCs at the anode end of the WCSP BGA solder joint. The complex reactions between the reactants at the Cu UBM/SAC solder joint interface are fundamental phenomena between the liquid and solid metals and alloys. As the

IMC layer grows, the stability of the SAC IC is compromised [15], and Cu material is removed and relocated from the cathode end to the anode end of the solder joint. Having such a variation in accumulation and depletion of the Cu concentrations within the solder joint results in hillocks, whiskers, and voiding on the anode end. Meanwhile on the cathode end, EM voids form due to the depletion of Cu. During solid-state aging, the IMC phases form via heterogeneous nucleation and growth, at the Cu pad/SAC solder interface. In micro solder joints, Kirkendall voids commonly emerge in the interface between the Cu substrate and the Cu_3Sn IMC [15-18]; however, that is not commonly observed in WCSP BGA solder joints.

2.2.3 Microstructural Effects Accelerating Electromigration

EM failure in Pb-free solder joints has proven to be a major reliability concern. As the demand for efficient thinner devices becomes more and more apparent, semiconductor packages and IC also shrink. With smaller devices, these high power and compact devices are subjected to high current crowding, JH, resulting in failure by EM. Industry has taken many initiatives to curb the reliability concerns pertaining to EM, such as implementing a UBM layer with an optimal thickness, utilizing diffusion barriers such as a Ni plating between the UBM and the SAC solder bump, and utilizing different types of SAC alloys, where additives such as Bi are considered. However beneficial these approaches have been, they still have their limitations and EM is still a reliability concern, albeit a semi-mitigated concern. What’s more is variables like solder alloys, solder joint geometries, and UBM thicknesses do not explain anomalies like sudden, early failures, or prolonged failures by up to two orders of magnitude. Another hypothesis is that the microstructure at the EM failure site may play a role in EM failure kinetics. This must be considered when examining FEM data and experimental data, as it may serve as an explanation for random failures which do not show much of a pattern, regardless of mitigation techniques.

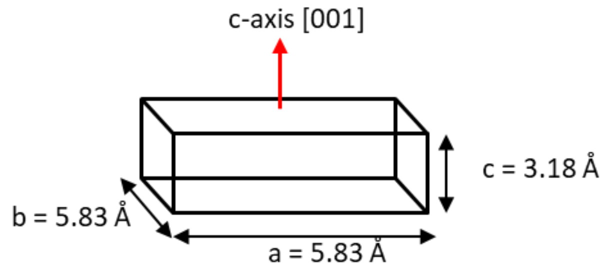

Figure 8 Body-centered-tetragonal (BCT) crystal structure.

In the case of Cu-EM mitigated voiding in the Sn solder joint, the general EM failure mechanism has been determined to depend on the nucleation and propagation of voids along the solder joint/UBM interface, followed by the complete consumption of the Cu supplied by the UBM. It is therefore agreed that anomalous variations failure kinetics likely depend on another factor such as the aberrantly high EM diffusivity (Z*D) of the atomic species at the joint/UBM interface, typically Cu and Sn. If the failure mechanism can be agreed that the microstructure or Sn grain orientation may have an impact on the rate at which the EM diffusive materials can travel through the lattice at the interface. One such prediction is that if there is the presence of a Sn orientation of [001] at the interface, which is aligned with the direction of the EM, then the diffusivity of the EM species will be exceptionally high, explaining the accelerated EM failure kinetics. This is possible because β-Sn in the solder joint has a BCT crystal structure with anisotropic properties, as illustrated in **Figure 8**. The BCT structure has lattice constants a=b= 5.83 Å and c=3.18 Å. The c-axis has a larger diffusion path, requiring a lower activation energy compared to the a and b axes, resulting in up to 500X faster diffusion rate. The alignment of the c-axis, or [001] grain orientation, with the EM directionality accelerates the EM failure kinetics [7, 8 19, 20, 21-25].

2.3 Mitigation Designs to Prolong Electromigration Failure

Industry has embraced many methods of mitigating EM failure and shear stress on the solder joints. One well-known approach in solder bump flip-chip applications is the implementation of an a UBM layer. Essentially, a Si die has Cu traces, or RDL, which route current through the solder bumps and the Si chip. Adding a layer of Cu between the Cu trace and the solder bump adds its own benefits, including: 1) providing an added Cu supply to fill vacancies in the solder bump caused by EM; 2) providing a solderable metal layer so that the adhesion strength of the solder bump is sufficient; 3) to minimize the stress on the Si die – too thick of a UBM may result in cratering in the Si; 4) to dampen the stress on the solder joint. Most important for addressing the EM effects is the added Cu supply that the UBM provides to fill vacancies which are formed by EM forcing material from the Cu/SAC solder joint interface on the cathode end to the anode end of the solder bump. This additional supply of Cu assists in the prolonging of a device's reliability against EM failure.

A UBM which is too thin is consumed quicker than what is desired, the void forming earlier than it would in samples with greater UBM thicknesses and propagating along the UBM/SAC interface. A UBM which is too thick may slow the nucleation of the void, but the exact mechanism which may increase the void propagation rate is unknown. This is where the FEM may be

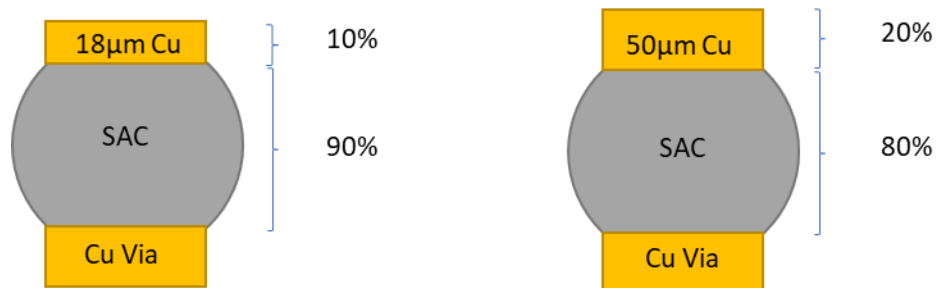

Figure 9 Illustration of aspect ratios of UBM:SAC, where the 18µm Cu UBM to SAC solder joint ratio is approximately 1:9 and the 50 µm Cu UBM to SAC solder joint ratio is approximately 2:8.

beneficial to better understand how the current crowding, JH, and stress development may play a role in reliability.

Adjusting the ratio of the UBM will dampen the effects of the stress, while also appealing to EM longevity. **Figure 9** illustrates the aspect ratios of the UBM:SAC solder joints, where the 18μm UBM to SAC solder joint ratio is approximately 1:9. Meanwhile the 50 μm UBM:SAC solder joint ratio is approximately 2:8. Experimental results suggest that the 50 μm UBM dampens the stress development on the solder joint compared to the 18μm UBM (interchangeably described as 18C), as the 18 μm UBM samples have a longer MTTF than 50 μm UBM samples under EM testing. Understanding the stress which develops at the interface between the UBM may be key to determining an optimal thickness of the UBM to increase the lifespan of a solder bump against the effects of EM.

2.4 Fatigue Behavior Among Various BGAs without Underfill

Fatigue occurs with cyclic stress which exceed the yield stress of a material. Solder interconnects subjected to thermal fatigue undergo cyclic stress induced by cyclic temperatures. The typical microstructural feature among materials which experienced failure by fatigue is the formation and propagation of a crack.

Package type and size have been found to influence the fatigue life among interconnects. **Figure 10** illustrates the relationship between fatigue lifetime and package type. Packages with relatively larger die sizes (60% of the package size or greater) fail earlier than those where the die size is smaller (50% or less of the entire package). WCSPs have actually shown to be least reliable against fatigue failure, which will come into play in the pulsed-DC model [26]. Adding to the die size, the CTE mismatch among all of the package materials is theoretically substantial

enough to generate a considerable amount of shear stress. Thus, warpage and plastic deformation are expected to factor into fatigue life cycles among packages subjected to fluctuating temperature and stress by pulsed-DC.

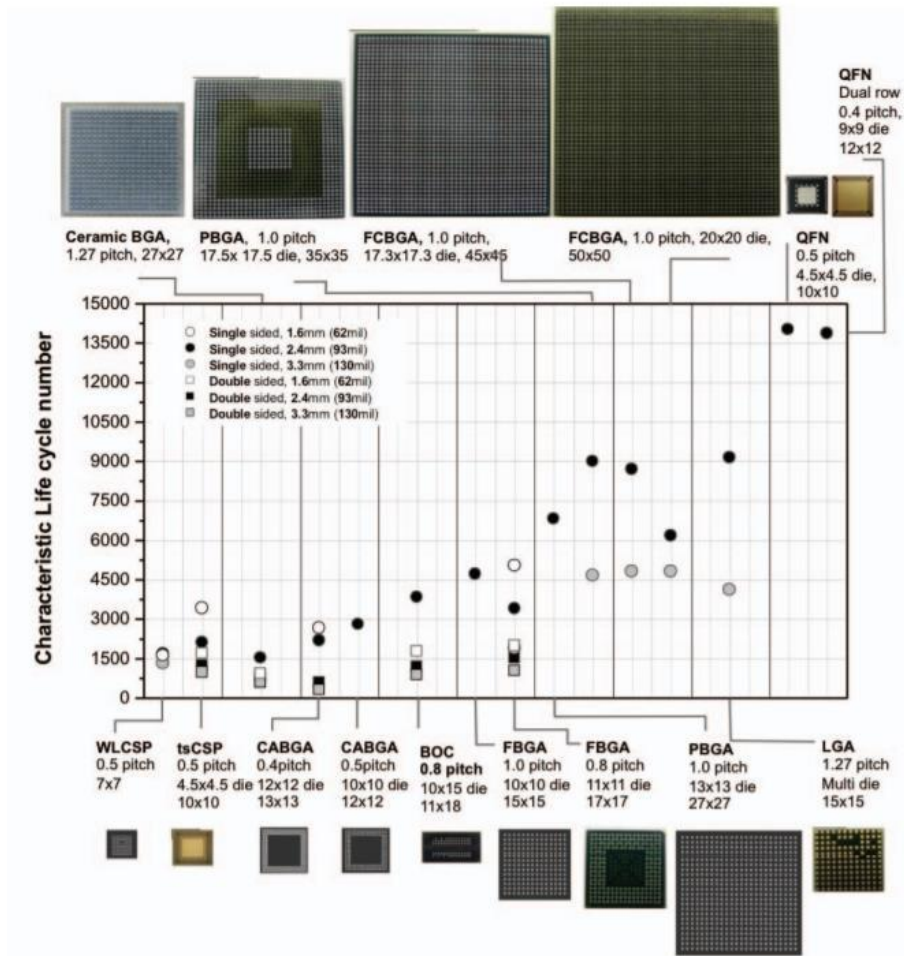

Figure 10 Characteristics of thermal life cycle number among varying package types [26].

2.5 Finite Element Method and Applications to Semiconductor Package Interconnects

FEM is a technique used for numerical analysis to obtain reasonably approximate solutions to an engineering problem. The research presented in this dissertation is completed using built-in equations in two different FEM packages: ANSYS and ABAQUS. FEM results will be interpreted

quantitatively and related to EM experimental results qualitatively. However, it is worth understanding how these two software packages solve complex problems, so we will divulge in them.

FEM works on the basis that a solution region may be modeled in an analytical manner by replacing it with an assembly of discrete elements within the model. This assembly of elements is generated through a meshing function in the FEM package. A schematic example of a 3-node

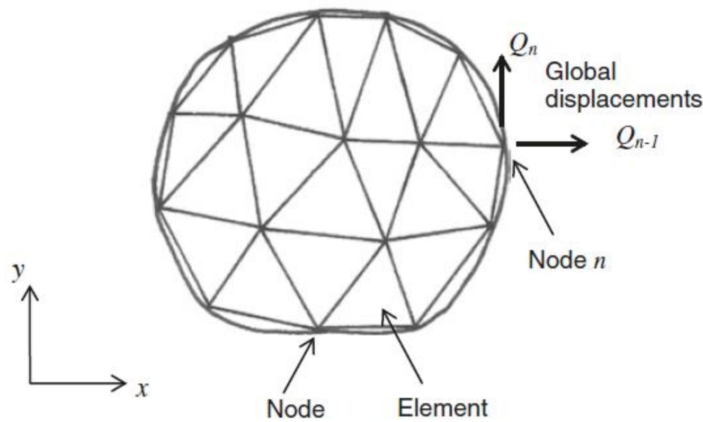

Figure 11 Discretization of a solution domain into an assembly of 3-node triangular finite elements along with a linear elastic material response. [5].

triangular element along a linear elastic material response and a linear elastic material response can be seen in **Figure 11**. Elements are not limited to triangular-shaped elements, in fact many may be tetrahedral, hexagonal, or a combination of all three in the form of a free mesh. But, for simplicity in understanding, we will focus on the triangular 3-node element as it is the simplest element.

Within each element, the outputs of importance vary depending on the problem type. For example, outputs of displacement and temperature would be calculated in the elements. These

outputs are governed by differential equations which are relevant to the engineering problem based upon the boundary condition inputs and the outputs selected.

FE equations used for elements which undergo a displacement are expressed in a matrix form given by **Eq. 5** where $[k]$, $\{q\}$, and $\{f\}$ are the stiffness matrix, the vector which consists of nodal displacement values, and the vector with corresponding elemental nodal forces, respectively. Derivations of the FE equations based on **Eq. 5** starts by assuming the presence of a displacement field within an element. Coordinates are also considered as well as displacement variables. The x and y axes indicated in **Figure 12** are denoted as *u* and *v*, respectively.

$$[k]\{q\} = \{f\} \qquad \textbf{[Eq. 5]}$$

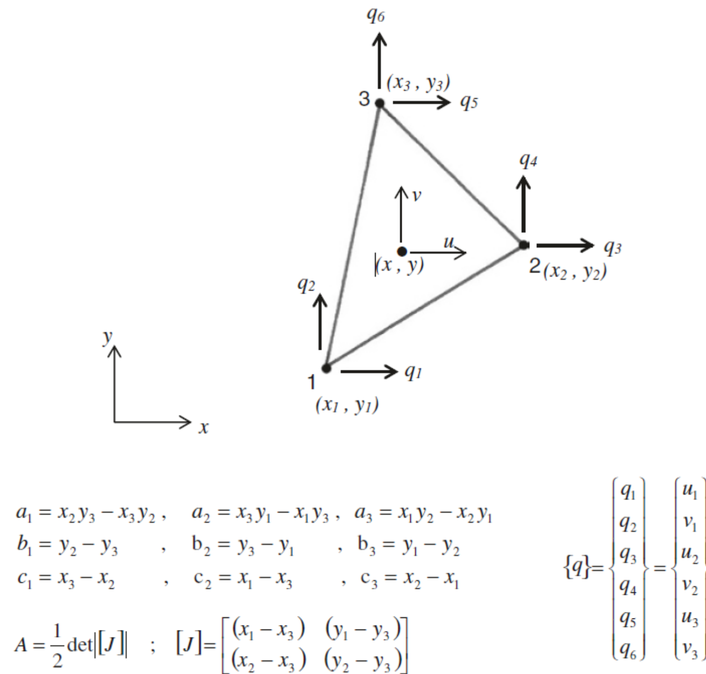

Figure 12 A 3-nodal triangular element with element nodal displacements. An element nodal connectivity is defined to provide the connection between local and global numbers of each element in the mesh [5].

Displacements within the elements vary according to the interpolation or shape functions, denoted as N_i, where $i = 1, 2, 3$ using the 3-node element assembly presented above. Along the x-axis, the displacement can be given by the matrix described in **Eq. 6**.

$$[u] = \begin{bmatrix} N_1 & 0 & N_2 & 0 & N_3 & 0 \\ 0 & N_1 & 0 & N_2 & 0 & N_3 \end{bmatrix} \begin{Bmatrix} q_1 \\ q_2 \\ q_3 \\ q_4 \\ q_5 \\ q_6 \end{Bmatrix} \qquad \textbf{[Eq. 6]}$$

The shape function, as denoted by N_i, can be represented using Cartesian coordinates of the elemental nodes, given by **Eq. 7**, where indices i, Δ, a_i, b_i, *and* c_i are the node numbers for the element, the area of the element, and functions of nodal coordinates of the element. The 3-node triangular element with nodal displacements is presented in **Figure 12**.

$$N_i = \frac{1}{2\Delta}(a_i + b_i + c_i) \qquad where\ i = 1, 2, 3 \qquad \textbf{[Eq. 7]}$$

N_1, N_2, and N_3 are alternative forms of the shape functions which can be prescribed using local coordinates, ξ and η, which both vary so that they are $0 \leq (\xi, \eta) \geq 1$. The shape functions must satisfy the condition where $N_1 + N_2 + N_3 = 1$. Each shape function assumes a value of unity at their respective nodes so that they would vary linearly to zero at the other two nodes to which they are not assigned. **Figure 13** illustrates representative shape functions in local coordinate systems for 3-node elements.

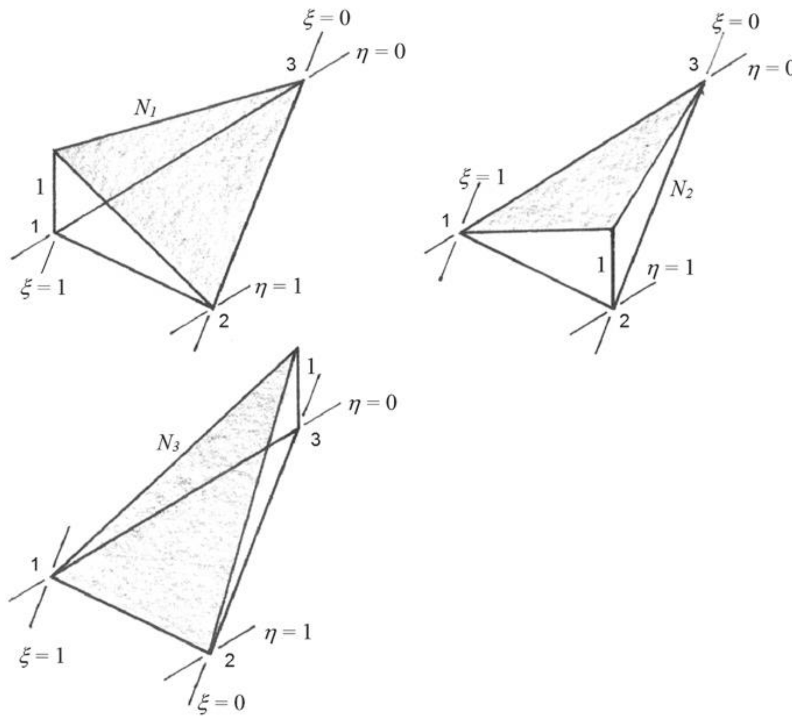

Figure 13 Representative shape functions in local or generalized coordinate systems for 3-node elements [**5**].

The strain-displacement relationship based upon small strain theory is presented in **Eq. 8**. Three independent strain components are included in the strain vector and that is because only three is necessary for solving the plane elasticity problem for the 3-node elements.

$$\{\varepsilon\} = \begin{Bmatrix} \varepsilon_x \\ \varepsilon_y \\ \gamma_{xy} \end{Bmatrix} = \begin{Bmatrix} \frac{\partial u}{\partial x} \\ \frac{\partial v}{\partial y} \\ \frac{\partial u}{\partial x} + \frac{\partial v}{\partial y} \end{Bmatrix} = \begin{bmatrix} \frac{\partial N_1}{\partial x} & 0 & \frac{\partial N_2}{\partial x} & 0 & \frac{\partial N_3}{\partial x} & 0 \\ 0 & \frac{\partial N_1}{\partial x} & 0 & \frac{\partial N_2}{\partial x} & 0 & \frac{\partial N_3}{\partial x} \\ \frac{\partial N_1}{\partial x} & \frac{\partial N_1}{\partial x} & \frac{\partial N_2}{\partial x} & \frac{\partial N_2}{\partial x} & \frac{\partial N_3}{\partial x} & \frac{\partial N_3}{\partial x} \end{bmatrix} \begin{Bmatrix} u_1 \\ v_1 \\ u_2 \\ v_2 \\ u_3 \\ v_3 \end{Bmatrix} \quad \textbf{[Eq. 8]}$$

Finally, **Eq. 9** is developed based on the partial differentiation of **Eq. 7**.

$$\frac{\partial N_i}{\partial x} = \frac{b_i}{2\Delta}; \ \frac{\partial N_i}{\partial y} = \frac{c_i}{2\Delta}; i = 1, 2, 3 \quad \textbf{[Eq. 9]}$$

The strain-displacement relationship can finally be defined in terms of nodal coordinates, as presented in **Eq. 10**.

$$\begin{Bmatrix} \varepsilon_x \\ \varepsilon_y \\ \gamma_{xy} \end{Bmatrix} = \begin{bmatrix} (y2 - y3) & 0 & (y3 - y1) & 0 & (y1 - y2) & 0 \\ 0 & (x3 - x2) & 0 & (x1 - x3) & 0 & (x2 - x1) \\ (x3 - x2) & (y2 - y3) & (x1 - x3) & (y3 - y1) & (x2 - x1) & (y1 - y2) \end{bmatrix} \begin{Bmatrix} u_1 \\ v_1 \\ u_2 \\ v_2 \\ u_3 \\ v_3 \end{Bmatrix}$$

[Eq. 10]

A simplified version of this final equation is given in **Eq. 11**, where [B] contains the nodal coordinate values of the element, leading to a constant strain field within the element. The element is known as a constant strain-triangular (CST) element.

$$\{\varepsilon\} = [B]\{q\} \quad \textbf{[Eq. 11]}$$

Linear elasticity outputs in metallic materials are obtained in the program by using the Constitutive equations given by Hook’s Law, defined by **Eq. 12**, which uses Cartesian stress and strain components. This is simplified to **Eq. 13**.

$$
\begin{Bmatrix} \sigma_x \\ \sigma_y \\ \sigma_z \\ \tau_{xy} \\ \tau_{xz} \\ \tau_{yz} \end{Bmatrix} = \frac{E}{(1+v)(1-2v)} \begin{bmatrix} 1-v & v & v & 0 & 0 & 0 \\ v & 1-v & v & 0 & 0 & 0 \\ v & v & 1-v & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1-2v}{2} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1-2v}{2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1-2v}{2} \end{bmatrix} \begin{Bmatrix} \varepsilon_x \\ \varepsilon_y \\ \varepsilon_z \\ \gamma_{xy} \\ \gamma_{xz} \\ \gamma_{yz} \end{Bmatrix} \qquad \textbf{[Eq. 12]}
$$

$$
\{\sigma\} = [C]\{\varepsilon\} \qquad \textbf{[Eq. 13]}
$$

Where σ_x, σ_y, σ_z are normal stress, τ_{xy}, τ_{xz}, τ_{yz} are shear stress components, ε_x, ε_y, ε_z are normal strain, and γ_{xy}, γ_{xz}, γ_{yz} are shear strain. *E* and *v* are the elastic modulus and Poisson's ratio, respectively. [C] in the matrix is the elasticity matrix. Static equilibrium would require that all shear stresses are equivalent to one another.

Elastic behavior in metallic materials is defined by Hooke's Law in the elastic region of the stress vs strain diagram. **Figure 14** below is a representative stress-strain diagram for a typical Sn-Ag-Cu solder alloy, with a particular highlight in the elastic range to describe the elastic

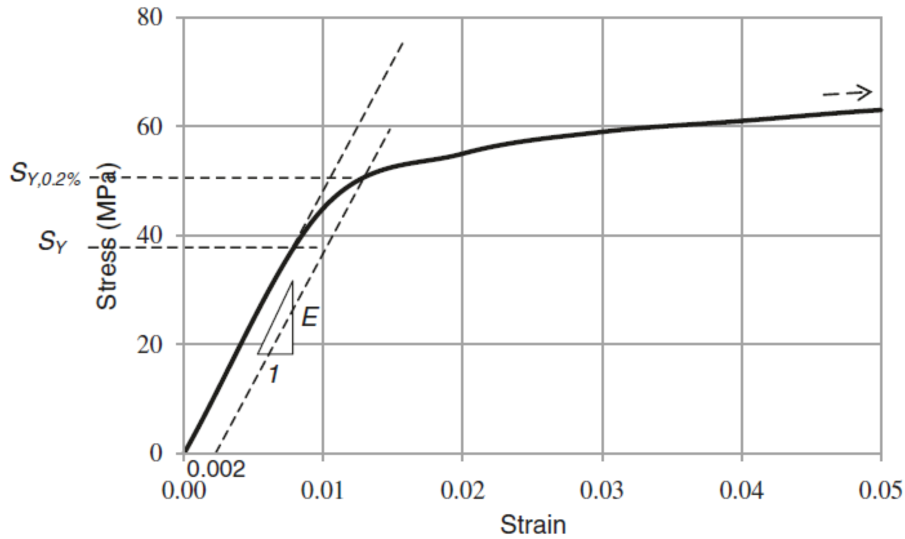

Figure 14 Stress-strain diagram of a typical Sn-Ag-Cu solder alloy with an emphasis on the elastic behavior [5].

behavior. The stress-strain curve follows a linear trend until the yield stress is achieved and then plasticity follows. Due to the complications of plastic modeling, a primary focus throughout this study will be on the elastic response of solder material, with intuitive plastic response thereby interpreted. The yield stress, denoted by S_Y can easily be extrapolated from the curve, which is commonly used as a material input for FE simulation as it is the point where stress-strain first deviates from linearity. During FEM, the solder alloy is also assumed to be homogeneous and isotropic when inputting the mechanical and material properties as the model is set up.

Stress and strain rates are complex, so 3D Cartesian stress and strain components are implemented to describe the internal stress of the material. This leads to the use of the generalized Hooke's Law, which relates the stresses to the strains at each material point under elastic conditions.

In this research, the material response to current and thermal loads are quantified in terms of displacement, stress, and strain responding at every point or node in the material. Mechanical behavior has commonly been described in a stress-strain curve, where the elastic region is in the linear portion of the diagram, which was presented in **Figure 14**. Mechanical properties such as E (Young's Modulus) and S_Y (Yield Stress) are obtained from this type of diagram. Temperature, of course plays a role in the mechanical response in materials. For example, fluctuating temperature may lead to strain hardening, thus increasing the potential for fatigue failure. As another example, long-term exposure of a metallic material to high temperature could lead to creep deformation.

FEM is useful in gaining a better understanding of the behavior of electronic packaging because it is a tool which may be used to recreate physically occurring phenomena observed in a package when subjected to various types of loads. More specifically, the material behaviors are an

area of interest when conducing an FEM study on a device. Microelectronic packages can be studied under many different conditions with a variety of variables. The traditional method of determining a package's reliability is by subjecting a batch of samples to a physical test of some sort, such as thermal cycling, accelerated EM testing, shear testing, creep testing. As previously discussed, the studies which inspired this research were accelerated EM testing under two areas of interest: 1) constant current and temperature and 2) pulsed-DC current and constant temperature. These types of studies gained valuable insight on package behaviors, which can be useful in-tandem with FEM; however, eventually, FEM may prove to be a cost-effective resource for estimating EM reliability trends. FEM may also be useful in narrowing a testing matrix to save both time and money.

FEM is commonly used in industry as part of a "Design-for-Reliability" approach. Employing such technology could lead to a shortened product development time while also increasing a product's reliability. However, the challenge in meeting this goal is to develop a valid study with known accuracy based upon predetermined limits. The FEM work done in this research is to establish a baseline in identifying a relationship between the EM reliability and a general material response trend produced during EM testing among various testing conditions and design parameters.

CHAPTER 3 : FINITE ELEMENT METHOD PRELIMINARY DATA AND SETUP EXPLORATION

This chapter will present the initial steps in verifying the finite element method (FEM) model used in the studies. A number of software packages, including ANSYS, COMSOL, and ABAQUS, were considered for modelling the EM stress effects in WCSPs. ANSYS was the most economic choice because a student license was available to students by the university. COMSOL was another option for the same reason and because collaboration with a research lab with a research license was an option. ABAQUS was a less economic option, but with a wider range of capabilities in transient thermal-electrical-structural studies with a variety of output options. The next sections will describe the steps necessary to identify the best modeling methods to obtain accurate outputs that sufficiently demonstrate physics within the model.

3.1 FEM Study Approach Background

FEM has increasingly become popular to gain understanding of stress development in a part under high current and high thermal loads. This is particularly useful in predicting the performance trend of a package depending on its integrated circuit geometry and materials. Two programs in this research were taken into consideration to run FEM simulations: ANSYS AIM and ABAQUS Standard/Explicit CAE. Each have their own benefits: ANSYS AIM offers a simplistic user interface; however, its structural-thermal-electrical function is limited such that it is unsuitable for transient studies. Meanwhile, ABAQUS offers a more complex user interface, while offering transient and steady-state thermal-electrical-structural studies and meshing capabilities. ABAQUS' fully coupled thermal-electrical-structural analysis is useful in obtaining steady-state and transient thermal solutions, while the electrical potential remains static throughout

the study. This function couples temperature, electrical potential, and displacement fields to allow for output fields such as thermal, electrical potential, stress, strain, and plastic deformation, among other desirable outputs.

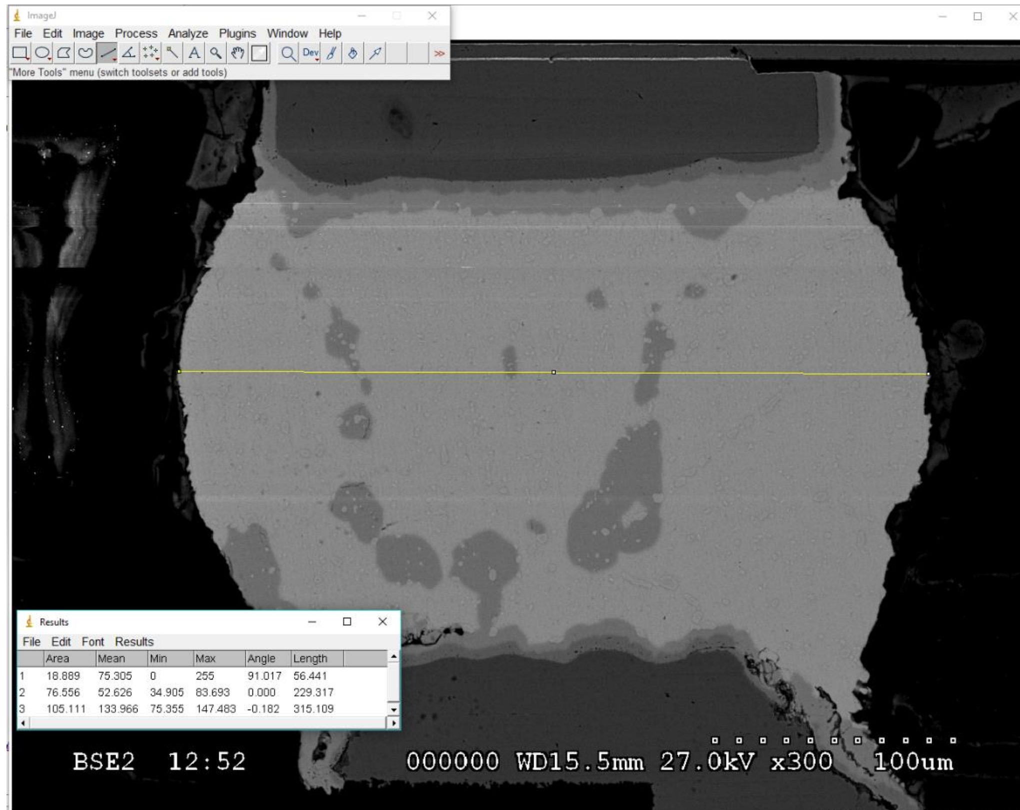

Figure 15 ImageJ approximation for the DUT interfacial area and diameter.

FEM is conducted on a CAD model using wafer-level chip scale package (WCSP) design parameters, which incorporates a 5x5 ball grid array (BGA). ImageJ, an open source measurement program, was used to determine the geometry of the solder bumps and the interfaces shared between the SAC solder joint and the Cu pad and UBM. **Figure 15** depicts the ImageJ approximation based upon an SEM image taken in backscattered electron (BSE) mode of the DUT. To begin, a calibration of the measurement was completed by using the scale at the bottom right corner of the BSE image. Next, a line was taken across the entire solder bump, averaging 300 µm

in diameter. Another line was taken across the interface between the Cu UBM and the solder bump, which averaged 230 µm in length. A third line was taken across solder bump from top to bottom at the contacts between the SAC solder bump and the UBM, which averaged 230 µm tall. Finally, for this particular UBM thickness, a line was taken measuring the top to the bottom of the UBM, which averaged 50 µm, which is correct, as the solder bump in this BSE image is of the DUT in a WCSP with a 50 µm UBM incorporated in the package.

Figure 16 is a schematic of a full-scale model of the WCSP BGA, which is designed using SolidWorks in one whole part with small subsections for each component such as the Cu via, SAC solder joint, PCB and Cu under bump metallization layer. For simplification, the full model was

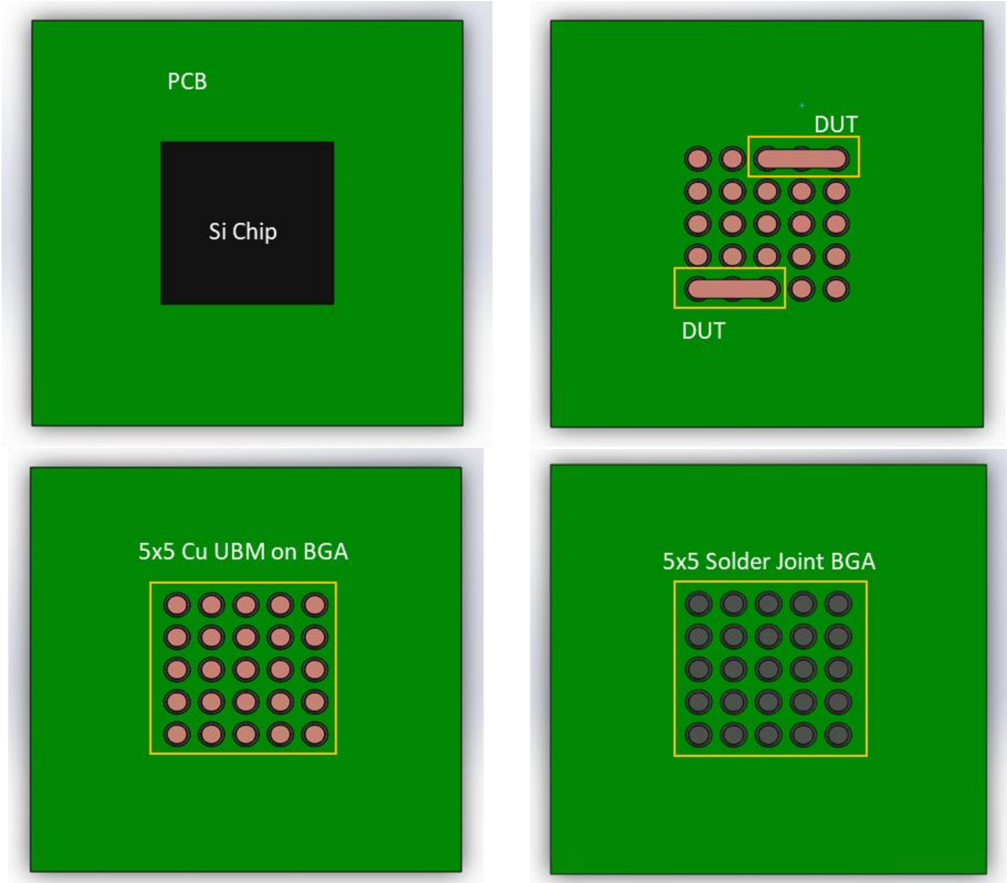

Figure 16 SolidWorks full-scale CAD model of the WCSP BGA

reduced to a sub-model, which is equivalent to 1/5th of the full 5x5 BGA. After modeling with SolidWorks, the model is exported to a STEP file, which is compatible with most FEM software packages, including ANSYS and ABAQUS. The general process which is followed for each study is outlined in the workflow chart in **Figure 17**.

Essentially, the STEP file is imported into ANSYS or ABAQUS CAE in a Standard/Explicit Model. Materials are generated and properties are defined. Then each part (Cu vias, Cu UBMs, Cu plate, Si chip, solder balls) is assigned a section which represents each material present in the package. Once the assembly is developed, the meshing is completed. Since the degrees of freedom (DOF) in this model are primarily voltage/current and temperature, with a fixed surface on the bottom of the PCB, we know that the model needs to be a coupled thermal-electrical-structural study to give the desired outputs: stress, strain, temperature, and current

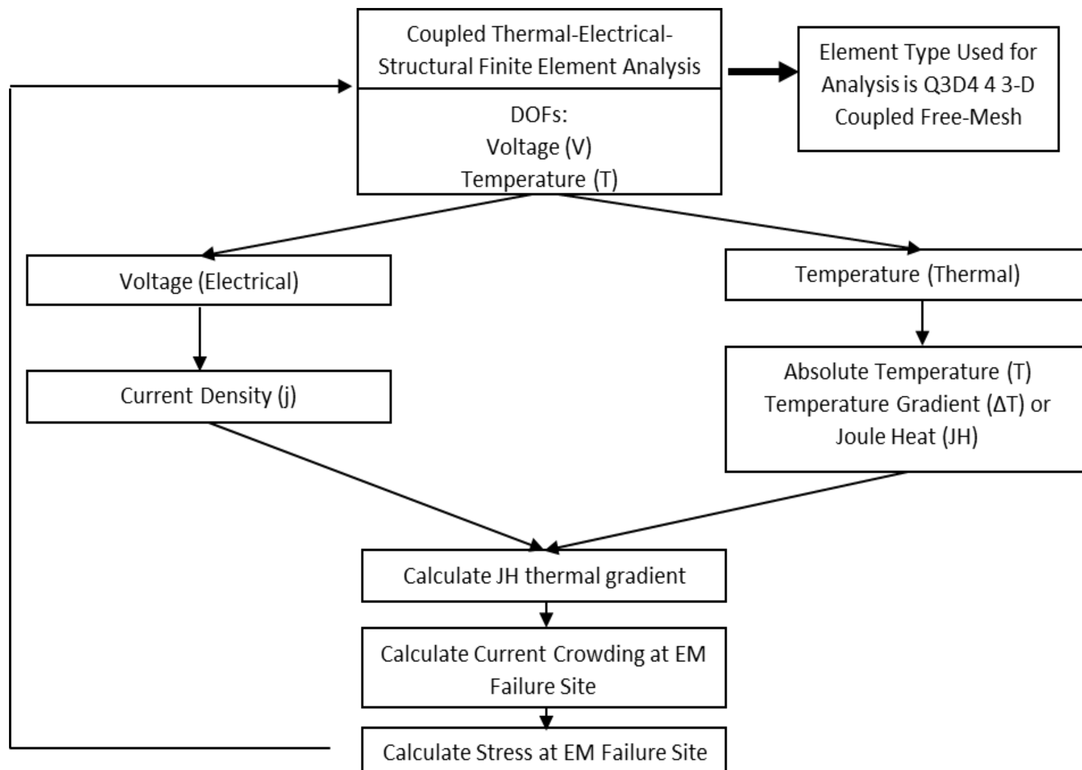

Figure 17 Outline of entire FEM study and post-processing analysis workflow. This process is repeated for current configuration, UBM thickness, induced voids, PI opening, and Pulse-DC studies.

crowding. The exact process which is followed is explained more in depth in the coming sections and chapters with respect to each aim.

3.1 Theoretical Calculations of the UBM Thickness Effect on Stress

Prior to committing to simulations, calculations were necessary for sanity check purposes. Assuming we know how much the SAC solder joint, and the Cu are expected to expand, we can calculate the stress and strain by measuring the lengths.

$$L_T^0 = L_{Cu}^0 + L_{Sn}^0 \qquad \textbf{[Eq. 13]}$$

$$\Delta L = [(L_{Cu}^0 * \alpha_{Cu}) + (L_{Sn}^0 * \alpha_{Sn})]\Delta T \qquad \textbf{[Eq. 14]}$$

Where the CTE of the UBM and the solder joint, α_{UBM} is represented by α_{Cu} and $\alpha_{Solder\ Joint}$ is represented by α_{Sn}. α_{Cu} is assumed to be 1.77E-5 °C^{-1} and α_{Sn} is assumed to be 2.40E-5 °C^{-1}. The predicted strain is therefore calculated using the below equation

$$\mathcal{E} = \frac{\Delta L}{L_0} \qquad \textbf{[Eq. 15]}$$

By using the strain obtained by **Eq. 7**, the compressive stress can be calculated using **Eq. 16**, where the elastic modulus, E, for the solder SAC387 material is assumed to be 47 GPa.

$$\sigma_c = E * \mathcal{E} \qquad \textbf{[Eq. 16]}$$

Of course, the above method requires us to know the amount by which the solder and Cu material that share contacts expand by. It's especially complicated when you have one solder joint expanding farther than others since it carries a higher amount of current than surrounding bumps. For simplification, one can also calculate the stress purely using the change in temperature (ΔT),

Young's Modulus (E) of a given material, and the CTE of that material (α) as presented by **Eq. 17.**

$$\sigma = E * \alpha * \Delta T \qquad \textbf{[Eq. 17]}$$

Where σ is the stress calculated, E is Young's Modulus of a given material, α is the coefficient of thermal expansion of a given material, and ΔT is the change in temperature. Using **Eq. 17**, and substituting the variable properties, we can estimate that for 10°C in JH, the stress accounting for just Sn expansion is revealed by the below calculation.

$$\sigma = E * \alpha * \Delta T$$

$$\sigma = [(47E + 10)Pa * (2.4E - 5) * 10℃] * (1E - 6)$$

$$\sigma = 11.75\ MPa$$

Neglecting the stress in other materials, one can conclude that a realistic value of theoretical stress generated in the solder joint should be around 11.75 MPa, above the yield stress of 11.35 MPa at 160°C. This assumes a JH value of 10 degrees, which is the case in the full model; however, the sub model which has a lower mass might experience higher JH and generate more stress. Assuming a JH value of 15 degrees, a realistic expectation of the theoretical stress generated through FEM should be around 17.63 MPa. This value will be certainly impacted by the ratio of materials present, so it is merely useful as a gauge to compare if the values obtained through FEM are remotely realistic.

Another important metric to be wary of is the current density. Theoretically, current crowding in a symmetrical current flow configuration would be greatest at either corner of the

DUT, which should be around 9.63 kA/cm^2 on either corner. An asymmetrical current flow configuration the current should be the greatest at one corner of the DUT, which should be about twice that of the symmetrical current flow, at least 18 kA/cm^2.

These calculations and estimates are useful starting points to determine whether or not our model is capturing the physics accurately. If the model is not capturing the physics accurately, modifications in the boundary conditions may resolve the issue.

3.2 Developing the FEM Model

All models to be investigated are modeled in SolidWorks and then exported as a STEP file to be imported into the simulation software. The two major contenders of software packages considered for the purpose of FEM modeling the stress effect in EM-tested WCSPs will be discussed further in the next sections.

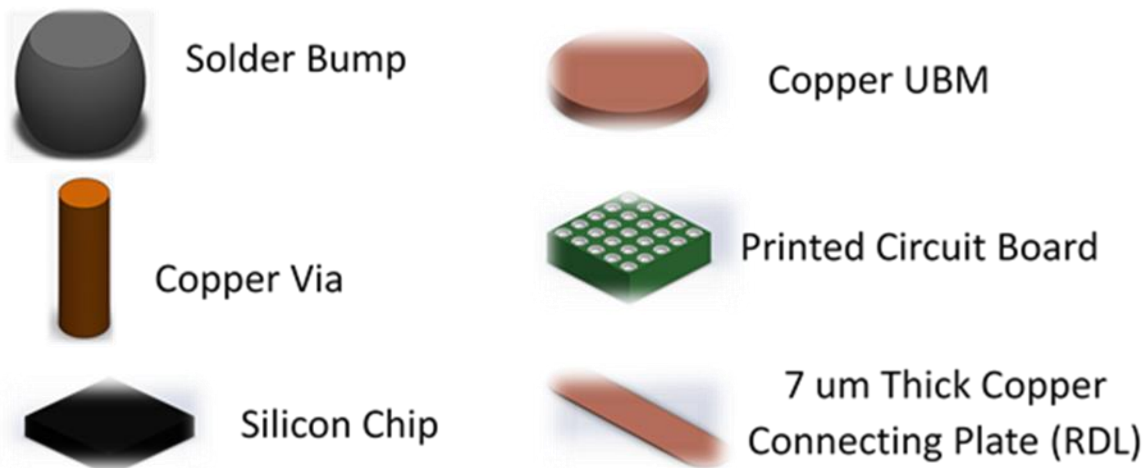

Figure 18 WCSP package individual parts which are assembled in a SolidWorks assembly file, then exported to a STEP file.

The WCSP sample is a simple 5x5 BGA, with a pitch of 0.4 mm, and solder bumps which have a diameter of 0.230 mm bonded between a Cu via (in the PCB) and a 0.018 mm, 0.035 mm,

and 0.05 mm UBM (on the Si chip substrate). **Figure 18** depicts each of the individual WCSP parts which were developed in their own individual SolidWorks part files, then brought into a

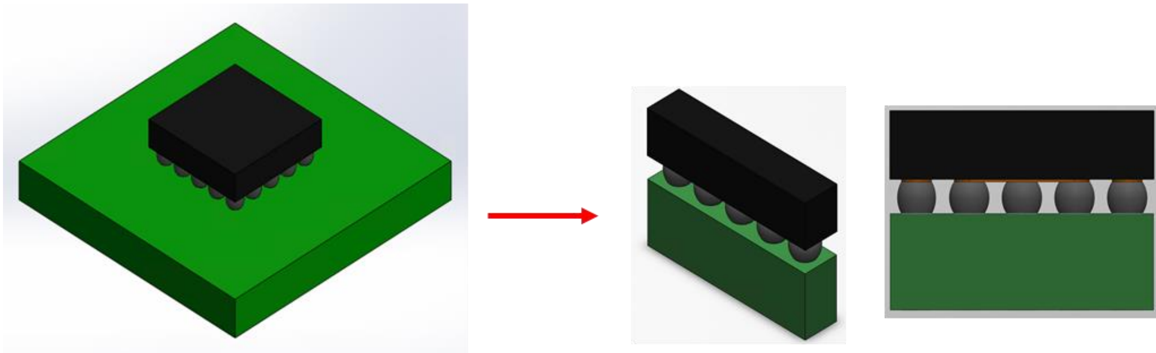

Figure 19 SolidWorks full 5x5 BGA WCSP model reduced to the 5x1 submodel, which is exported in a STEP file and imported into ABAQUS.

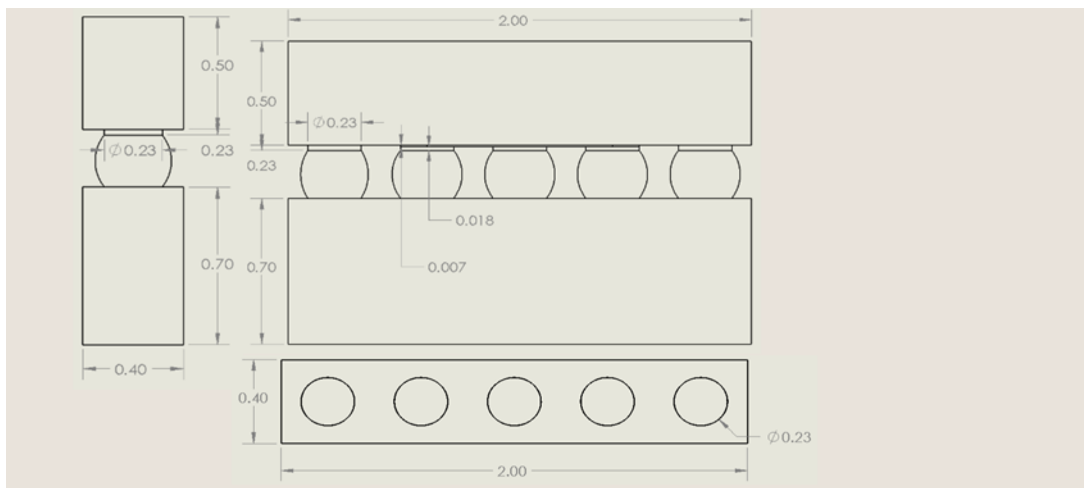

Figure 20 SolidWorks model of a 5x1 BGA submodel with dimensions, mm.

SolidWorks assembly file. In the assembly file, the package parts were assembled by mating the surfaces to one another and assigning concentric conditions as appropriate. The assembly of the model then exported as a STEP file, which is a compatible file type for most FEM software packages.

Figure 19 illustrates the full-model of the 5x5 BGA WCSP designed in SolidWorks. This model is reduced to a 1x5 BGA submodel for simplicity and to achieve a very fine mesh size for

improved result output accuracy. Reducing to a submodel also saves computational costs and time, as well. The design follows the above computer aided design (CAD) layout produced using SolidWorks in **Figure 20** and as defined in **Table 2**. Initially, the submodel was assumed to include a 3x1 BGA of solder bumps sandwiched between a Si die and a PCB, as only three solder bumps, on RDL, and thus three UBMs and Cu vias are included in the testing circuit. However, upon studying with this model in ABAQUS, it became clear that there are limitations with the modeling capabilities. The shear and tensile stress in the outer two bumps in a 3x1 submodel overwhelm the model so much that the device under test (DUT) does not exhibit any compressive stress. So, a 5x1 submodel was proposed where the three inner solder bumps are used for the purpose of obtaining a trend, and the two outer bumps are used for constraint purposes.

Table 2. Dimensions of Geometry

Part	Thickness (mm)	Length (mm)	Width (mm)	Other Details
Si Die	0.5	2.0	0.4	Pitch = 0.4 mm
Cu UBM	0.018, 0.035, 0.050	0.23	0.23	
Cu Via	0.7	0.23	0.23	
Solder Ball (Sn3.8Ag0.7Cu)	0.3	0.23	0.23	
FR4 PCB	0.7	2.0	0.4	
Cu RDL	0.007	1.03	0.23	

Table 2 Dimensions of WCSP Geometry

After modeling in SolidWorks, the model is exported in a STEP file, which is compatible with ABAQUS, and then imported into ABAQUS Standard/Explicit CAE model. Each material is defined using the below table properties, and then each subsection is defined using the material

assignments defined in **Table 3**.

Table 3. Material Properties							
Material	Thermal Conductivity, k ($\frac{W}{m^oC}$)	Density, ρ ($\frac{kg}{m^3}$)	Isotropic Elastic Modulus, E (Pa)	Isotropic Poisson's Ratio, ν	Isotropic Electrical Conductivity, σ ($\frac{S}{m}$)	Coefficient of Thermal Expansion (CTE), α, (C^{-1}) [(ppm/°C)*E -5]	Specific Heat c_p ($\frac{J}{kg^oC}$)
Si Die	124	2330	1.65E+11	0.22	1E-12	2.6E-6	702
Cu UBM and Vias	400	8978	1.2E+11	0.38	5.8E+7	1.77E-5	385
Solder Ball (Sn3.8Ag 0.7Cu)	57	7500	4.7E+10	0.4	8.25E+6	2.4E-5	218
FR4 PCB	0.294	1900	2.2E+10	0.15	0.004	1.8E-5	1369
Polyimide	0.12	1420	2.5E+9	0.34	1.167E-14	2.0E-5	1093

Table 3 Material properties of WCSP model components.

After material properties are defined, sections are assigned according to each component in the WCSP assembly. A total of 18 sections are assigned in each submodel. Following that, boundary conditions, such as convection, ambient temperature, air coefficient, current/voltage input, grounds, and coordinate constants or fixed constraints are assigned. The development of these methodologies is discussed further in the next section.

3.3 Exploring ANSYS Finite Element Method Software Capabilities

Initially, ANSYS Workbench or ANSYS AIM were considered for FEM simulations because the university subscribes to student seats of the programs. As ANSYS Workbench was not intuitive for thermal-mechanical-structural studies, ANSYS AIM became the initial software of choice.

Simulations using ANSYS began by first creating the model in SolidWorks. One can opt to use Claim Space, a CAD function of ANSYS; however, since SolidWorks presented with more familiarity, the software was selected for CAD modeling purposes. Each individual part of the package, including the solder bumps, the Cu UBMs, Cu vias, PCB, Cu RDL, and Si die were developed and then brought into an assembly file to assemble the submodel. A 5x1 submodel is described here because that is what was ultimately decided upon after attempting to run a full model simulation on ANSYS and failing due to the number of elements exceeding the license allowance. The SolidWorks submodel was then exported into a STEP file, which was then imported into ANSYS. SolidWorks can be exported to IGES, which is also compatible with ANSYS, but the author elected to use STEP files for simulation purposes since many other software programs, including COMSOL and ABAQUS, are compatible with imported STEP files, as well.

Importing an assembled submodel, assigning material properties, and assigning boundary conditions were intuitive and the model gave warnings before running whether something imperative was missing. Additionally, meshing in ANSYS was an automatic function, and the user need only concern themselves with assigning a mesh size or fineness that would allow the

program to solve the simulation in a timely fashion while also producing a sufficient number of data points and acceptable accuracy.

Each boundary condition was defined, including a fixed constraint on the bottom of the PCB and bottoms of the Cu vias to allow the package to remain in place while the model will naturally expand feely upward, with the only added constraints being the support bumps which do not expand as far as the DUT solder bump. These constraint bumps due to the difference in solder bump expansion contribute to the compressive stress development as the current flows through the model. The mismatch in the CTEs for the materials which share contacts would

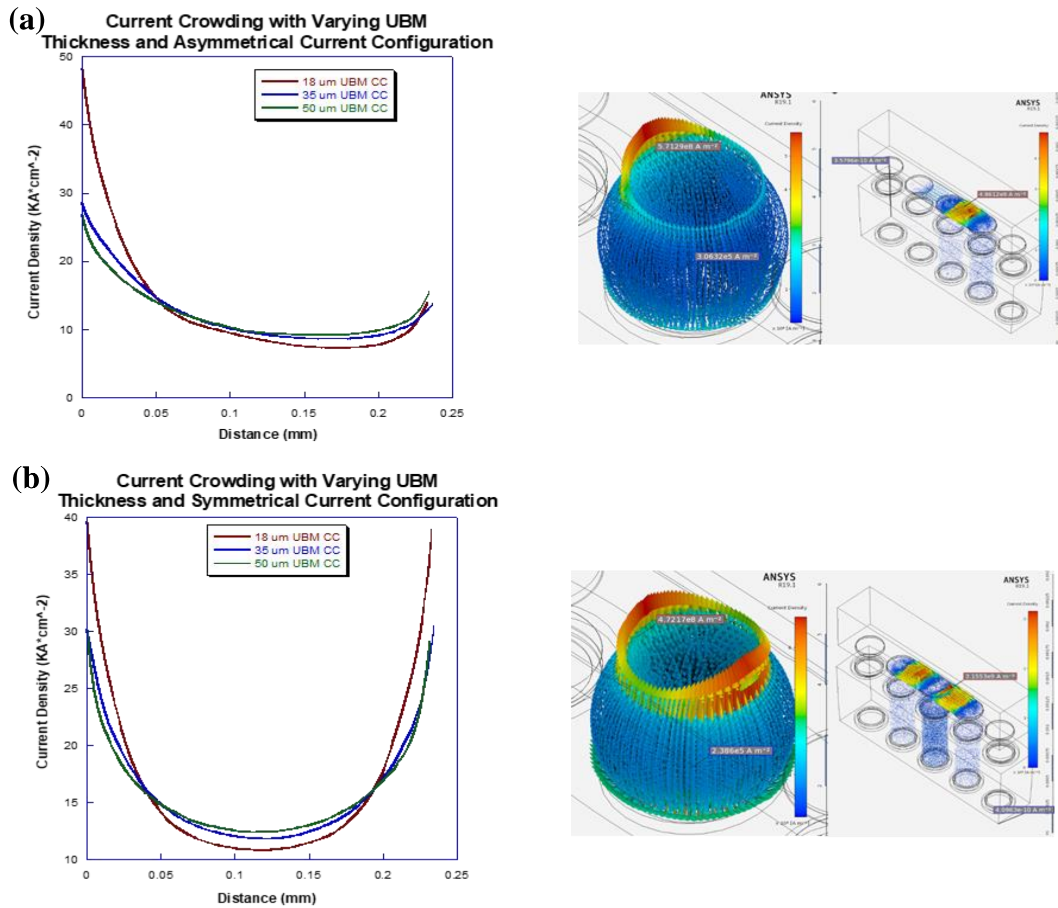

Figure 21 Current crowding computational results using ANSYS for **(a)** asymmetrical current flow configuration and **(b)** symmetrical current flow configuration.

contribute to the shear stress development as the current flows through the model, generating JH. The computation time per simulation was approximately 2-3 hours, which was relatively reasonable. A path was drawn across the DUT/UBM interface during post processing and the data along that line was exported to an excel file, which was then analyzed and plotted using KaleidaGraph.

ANSYS appeared to yield current density values which are higher than predicted the maximum on the corners being over 40 kA/cm^2, which may be explained by a singularity effect, which could be resolved with meshing refinement. While this value is excessive, the simulation

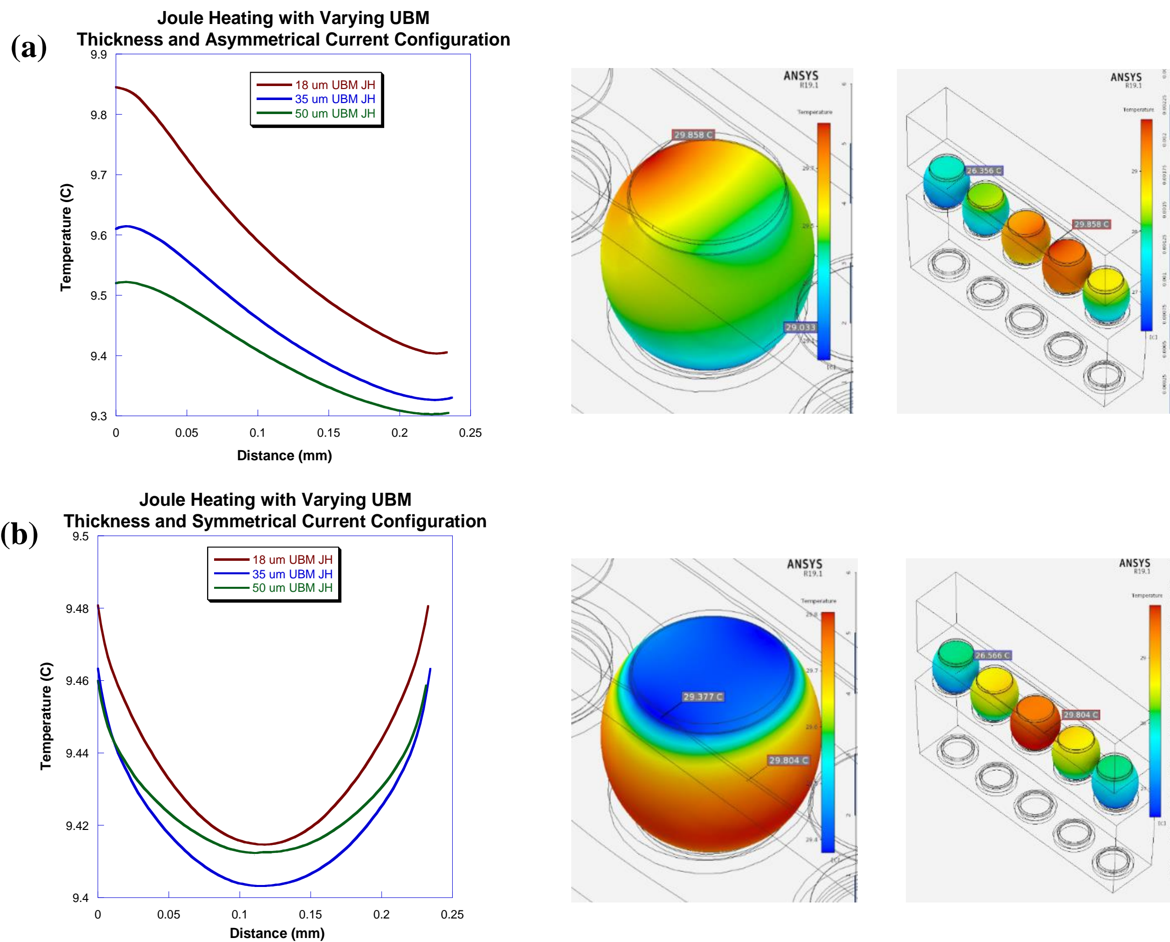

Figure 22 Joule heat computational results using ANSYS for **(a)** asymmetrical current flow configuration and **(b)** symmetrical current flow configuration.

did exhibit had respectable trends, nonetheless, as observed in **Figure 21**. Observing the current density along the interface in **Figure 21,** the 18μm UBM WCSP model has the highest amount of current crowding, followed by 35 μm, and finally 50 μm. This follows our predictions that the thicker the UBM, the more distributed the current density across the interface is – that is also apparent when looking at the center of the solder bump/UBM interface, where the 50 μm WCSP model has a higher amount of current density and thus a better distribution of current density.

Meanwhile, with an air convection of 1 $Wm^{-2}°C^{-1}$ applied, JH trends were also respectable, as can be observed in **Figure 22**. However, these results were obtained using conditions without forced air convection, which is what samples are tested under. Forced air convection typically lies between 5 and 500 $W/(m^2K)$, so while this trend is respectable, it is not realistic of the physics occurring within the WCSP model under EM testing conditions.

The stress trends comparing the UBM thickness of models subjected to symmetrical and asymmetrical current flow configurations and their void formation can be observed in **Figure 23**

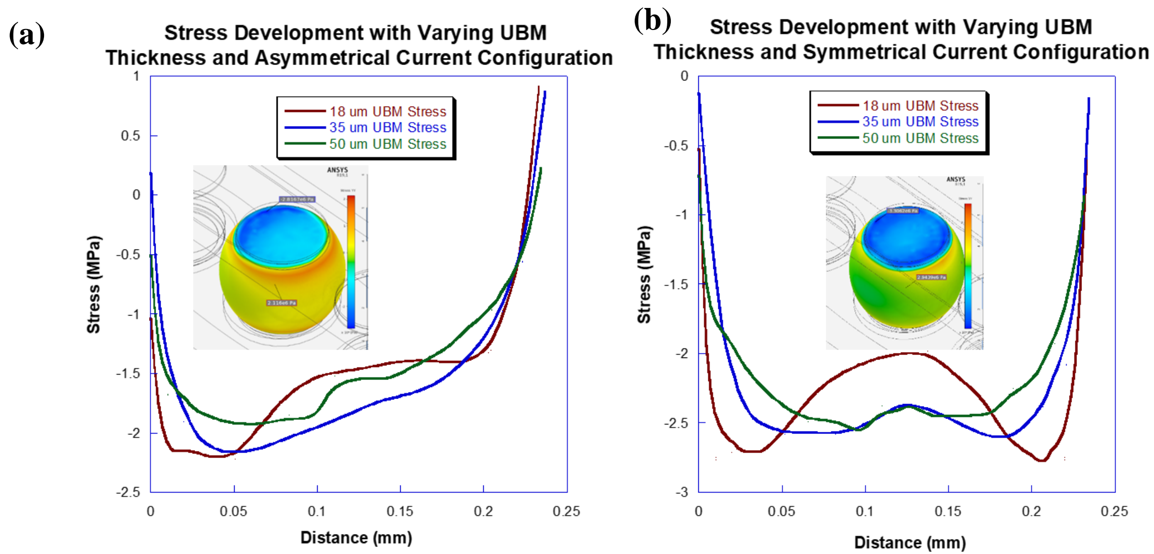

Figure 23 Stress computational results using ANSYS for **(a)** asymmetrical current flow configuration and **(b)** symmetrical current flow configuration.

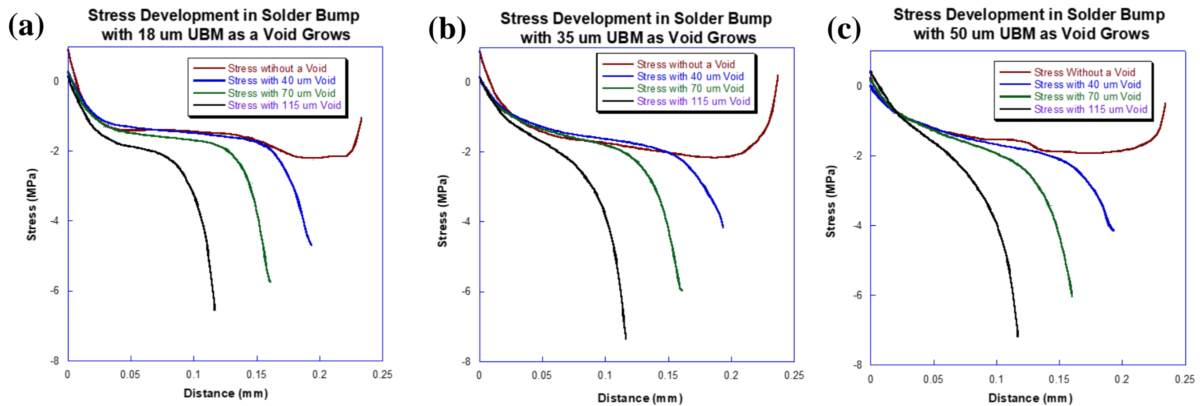

Figure 24 Stress with void growth computational results using ANSYS for WCSP models with **(a)** 18 μm UBM, **(b)** 35 μm UBM, and **(c)** 50 μm UBM subjected to asymmetrical current flow configurations.

and **Figure 24**, respectively. The compressive stress generated was notably higher in WCSP models with thinner UBMs (18 μm) than with those with thicker UBMs (50 μm). The WCSP models with 35 μm UBMs provided the best balance between Cu supply, current density distribution, and stress, as its stress was comparable with that of 18μm, but had better current density distribution. This could explain the performability of the 35 μm UBMs under EM testing – they had a longer MTTF than both 18μm and 50 μm UBM WCSP samples did. Also supporting our hypotheses of the compressive stress blocking the void growth, and EM runaway failure occurring once the solder bump void reaches a critical length. As a void propagates across the solder bump DUT/UBM interface, the current density, JH, and compressive stress compound at the void front for all three models; however, the 35 μm UBM revealed a greater magnitude of stress at the void front for the largest void, supporting the exceptional reliability of the 35 μm UBM WCSPs compared to the other two models.

ANSYS is a powerful simulation tool; however, it became quickly realized that ANSYS has limitations in producing realistic stress values with the coupled thermal-electrical-structural

studies. The key takeaway from ANSYS attempts is that it reveals respectable trends; however, it does not properly capture the physics so the values reported are not anywhere near what may be considered accurate or realistic – recall the estimated stress calculated in 3.1. It is apparent that ANSYS calculates the stress to be too low, the largest magnitude of stress being 2.5 MPa without voids and 8 MPa with voids. Current crowding also appeared to be too high, which may be owed to a singularity effect at the edge of the solder bump. This singularity effect may be problematic and could have been eliminated by refining the mesh; however, the stress trends and lack of transient capabilities were already reasons to abandon the use of ANSYS as a software for solving these complex thermal-electrical-structural problems. Credit, however, is owed to the trends which were obtained, as they supported experimental predictions. The compressive stress magnitude was notably higher in WCSP models with thinner UBMs. As a void propagates, the current density, JH, and compressive stress compound at the void front.

Additionally, it was imperative to observe the behavior of the model under pulsed-direct current (pulsed-DC) boundary conditions, a study which requires transient capabilities, and the student version of ANSYS was suitable only for steady-state studies. This limitation made it impossible to observe solder behavior under transient DC and pulsed-DC conditions. That said, ABAQUS became a primary interest moving forward.

3.4 Exploring ABAQUS Finite Element Method Software Capabilities

ABAQUS is an excellent tool for modeling fully coupled thermal-electrical-structural analyses, and it has both steady-state and transient capabilities. One of the complications added by switching from a steady-state study to a transient study is determining the number and size of time increments. When defining the transient analysis in ABAQUS, time increments can be selected

automatically based on a maximum allowable nodal temperature change indicated by the user. There is a relationship between the minimum usable time increment and the element size in the case of second-order elements. That relationship is defined by **Eq. 18**, where Δt is the time increment, ρ is the density, *c* is the specific heat, *k* is the thermal conductivity, and Δl is a typical element dimension, like the length of a side of an element.

$$\Delta t > \frac{\rho c}{6k} \Delta l^2 \quad \textbf{[Eq. 18]}$$

When a time increment is smaller than Δl in a mesh of second-order elements, spurious oscillations can be seen in the solution. This is particularly true with boundaries that have rapid temperature changes. The oscillations are non-physical and may cause issues with obtaining accurate solutions. First-order elements do not have these same issues because the heat capacity terms become lumped together; however, the problem of locally inaccurate solutions for small time increments may still remain. When small time increments are required for solving the solution, a finer mesh would be necessary in local regions which show rapid temperature changes. While there is no upper limit on the time increment size, nonlinearities in the problem may lead to complications in achieving convergence in the model.

Additionally, complicated is the determination of how JH is generated in the model. Earlier, the power of thermal energy was discussed in terms of JH. ABAQUS/CAE actually depends on the user specification of the amount of thermal energy generated due to the electrical current, presented by Joule's law, as presented in **Eq. 19**.

$$P_{ec} = J * E = \frac{\partial \varphi}{\partial x} * \sigma^E * \frac{\partial \varphi}{\partial x} \quad \textbf{[Eq. 19]}$$

Joule's law describes the rate of electrical energy, denoted by P_{ec}, which is dissipated by the current flowing through a given conductor. The amount of thermal energy released as internal heat in the body is denoted by $\eta_v P_{ec}$, where η_v is an energy conversion factor, which can be specified in the material definition. All electrical energy in the model is assumed to convert into heat with the conversion factor assumed to be equal to 1.0 unless the Joule heat fraction is otherwise specified.

ABAQUS' coupled thermal-electrical-structural elements are useful in solving the type of problem examined in this study as it simultaneously requires solutions with temperature, electrical potential, and displacement. The first-order coupled thermal-electrical-structural elements offered by ABAQUS calculate the thermal expansion by using a constant temperature over the element. The second-order coupled thermal-electrical-structural elements offered by ABAQUS use a lower-order interpolation for temperature than for displacement, which means that parabolic variation of displacements and a linear variation of temperature are used. These are used to gain a compatible variation of thermal and mechanical strain, allowing the outputs of stress and strain obtained in the solution. Second-order elements may give the desired outputs, but the added complication adds to the difficulty in gaining a fully converged solution.

Implementing ABAQUS is easier said than done. An initial challenge in implementing ABAQUS was meshing as this function does not share the same traits as that in ANSYS. A submodel, which consisted of rectangular features of every section of the model was relatively simple to establish a structured mesh compatible with thermal-electrical-structural simulations and results were obtained relatively quickly, within a few hours. Initial attempts at ABAQUS indicated that a SolidWorks assembly exported as a STEP file was not suitable for easy ABAQUS simulations. This became apparent when running simulations and discovering that the current

would run through the Cu via but would not continue to flow through the Sn joint or the rest of the circuit. After importing the assembly, the user would need to essentially assign contacts so that the program would recognize that the conductive materials share a surface and can allow the current to continue flowing. This effort can be avoided by simply creating one part with several solid bodies, or sections, taking care not to merge any of the solid bodies when extruding them in SolidWorks. These sections are easily identifiable. Once troubleshooting through these steps, ABAQUS yielded results that gave more promise in terms of capturing the physics than ANSYS did.

A preliminary study was done on a square model, which was imported via a STEP file, which was exported form a SolidWorks model. Each section and its material properties were defined according to **Table 2** and **Table 3**, respectively. Convection surfaces, CONVEC1 through CONVEC7-2 are defined. Sets are also assigned, which are tagged when setting up the boundary conditions. Three sets for the X, Y, and Z constants were defined and assigned to the bottom surfaces of the model (Cu vias and PCB bottom). Next, the voltage ground and input sets were defined and also defined and assigned to the bottom of the Cu vias connected to the circuit, so that current enters through the bottom of one Cu via and exits the circuit through the next. The sink temperature was set to 25°C and the air coefficient on all exposed surfaces was set to 1. A structured Hexagonal thermal-electrical-structural linear mesh was assigned with element sizes 5E-5, and then generated.

Next, two steps were defined. The first step, labeled “Initial” is steady-state, which is useful for establishing the X, Y, and Z constant boundary conditions, which limit the model from rotating or sliding in any direction. These were assigned to the bottom faces of the PCB, and Cu vias of the model. The predefined ambient temperature is also defined in the first step, which was set to 25°C

for this step. The second step, labeled “Step 1” is transient, which means it is time-dependent and is useful for solving problems which lack linearity solutions. “Step 1” was set to calculate for 10,000 seconds. The initial step was set to 0.01, the minimum step size was set to 0.001, and the maximum step size was set to 100. The maximum temperature change allowed per increment was set to 2 degrees.

Output requests were selected. In ABAQUS, two types of outputs are involved: History Output Requests and Field Output Requests. History Output Request selected was energy, and outputs every 1 increment, n, was selected. The Field Output Requests selected include energy,

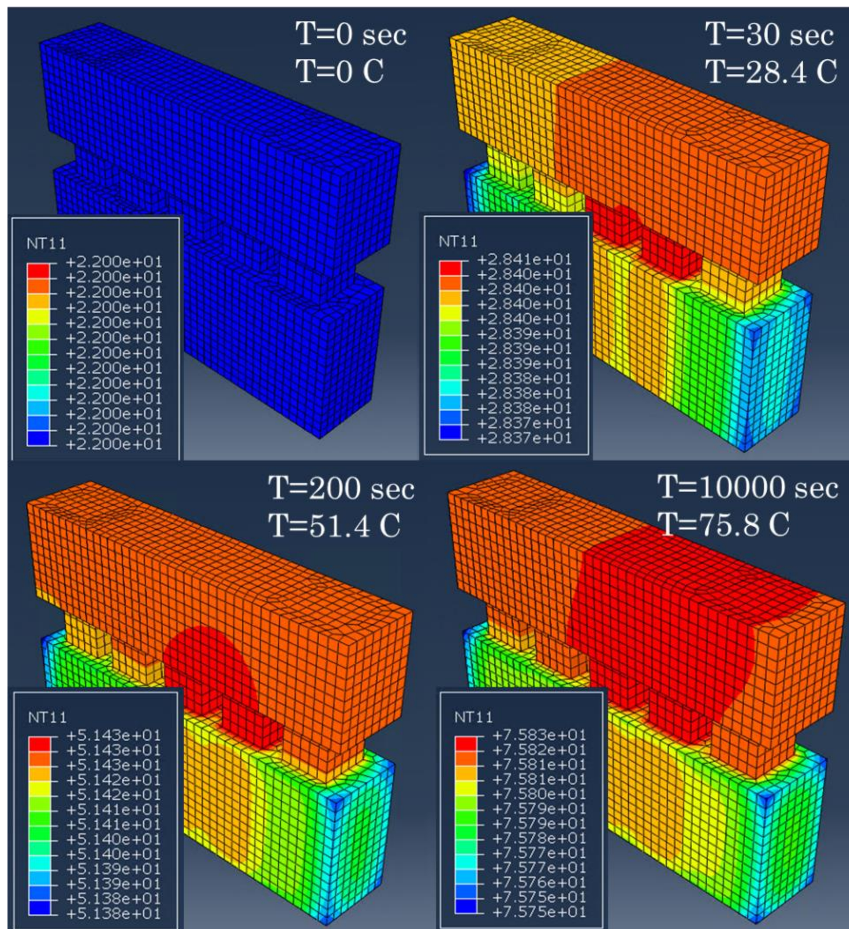

Figure 25 Temperature in crude square WCSP model with 0.01 V input.

contacts and forces, elastic stress, elastic strain, temperature (nodal and integrational), and current density. The data for the Field Output Requests was collected every 2 increments, n.

Once all boundary conditions, material properties, and mesh are all generated and assigned, a job is created. The job was set to save the data in a documents folder. The number of processors was set to 4. The job was then submitted and allowed to run, which took approximately three hours per simulation. Below are some preliminary results obtained using the square WCSP submodel. **Figure 25, Figure 26, and Figure 27** show the current crowding magnitude, JH, and shear stress generated in the square model using a voltage boundary condition of 0.01 V, respectively. The

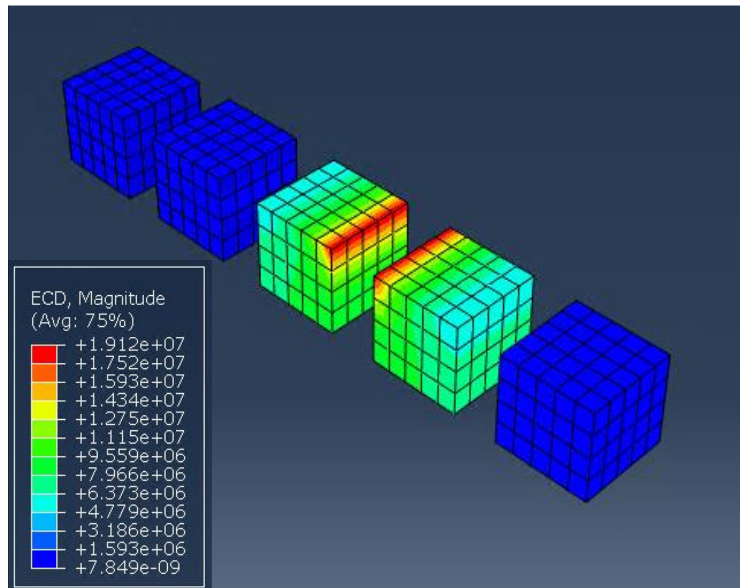

Figure 26 Current density magnitude in crude square WCSP model with 0.01 V input.

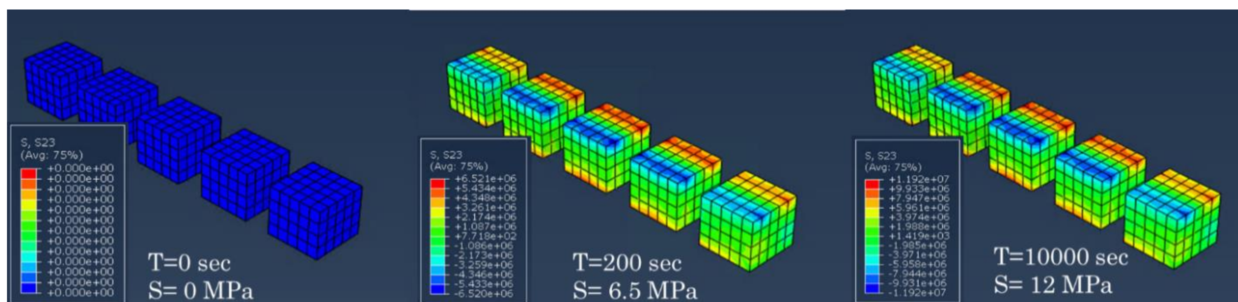

Figure 27 Shear stress (y-z) in crude square WCSP model with 0.01 V input.

model generated shear stress values of 12 MPa, which is respectable considering the preliminary stress values calculated prior to running simulations was approximately 12 MPa. Already, this is a significant improvement from thermal-electrical-structural solutions obtained by ANSYS.

Developing a structured mesh for the model with round solder joints, UBMs, and vias is not as simple to accomplish as with a square submodel and requires a number of partitions. This is necessary due to the spherical nature of the solder bumps and also due to the lack of symmetry within the model. Even with a considerable amount of partitions on the model, a number of bad elements were generated. Bad elements are problematic because they can impact the feasibility that the model might yield a solution. A potential method in solving this would be implementing an outrageously refined mesh; however, that would considerably add to the computation time.

To solve this issue a tetrahedral free-mesh was utilized. The coupled thermal-electrical-structural element type used for analysis is Q3D4 4 3-D Coupled Free-Mesh, with a global mesh size of 2E-5 and curvature control of 0.1. This will result in a number of elements and nodes, which will depend on the size of the model. For instance, for the 18C model with the 18μm-thick UBM, the meshed model's number of nodes and elements are 124,660 and 679,926, respectively. For larger models with thicker UBMs, the number of elements and nodes will be greater. The mesh type was selected such that it is compatible with thermal-electrical-structural analysis. A free mesh structure was chosen rather than a structured mesh for a number of reasons, one being the complexity of the model once a void is introduced. Since the submodel already was non-symmetrical, multiple partitions needed to be made, especially on the solder joint, Cu vias, Cu UBMs, PCB where the Cu vias are located, and the Cu RDL, which are all non-square, while sharing the space with square objects. With the given constraints, the shared surfaces and edges, and the predicted additional complexities which are expected with voids included in the model, a

tetrahedral free mesh form was chosen over a tetrahedral structured or hexahedral sweep for simplicity in achieving an effective mesh. A structured mesh is comprised of a uniform pattern of elements, which may be beneficial in terms of computational memory. A tetrahedral unstructured

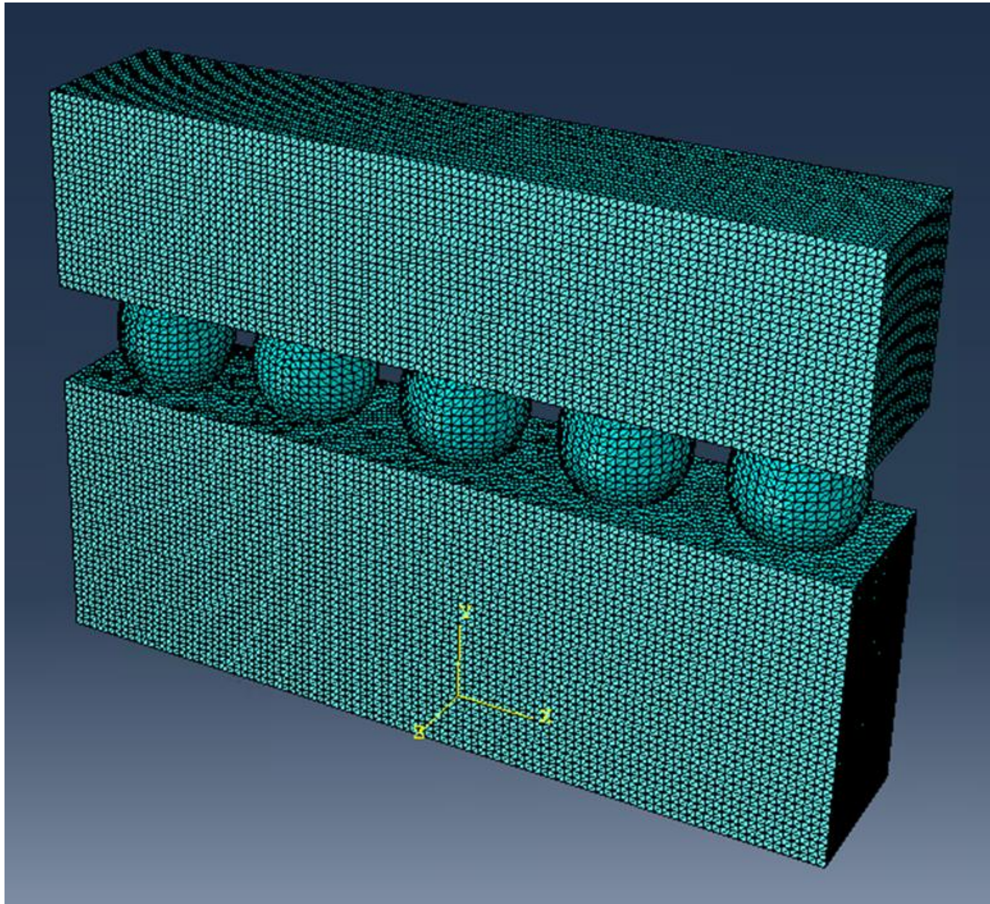

Figure 28 Q3D4 3-D Coupled Free-Mesh of the WCSP submodel, which is has a global mesh size of 2E-5 and a controlled curvature of 0.1.

or free mesh is comprised of a non-uniform pattern of and combines structured and non-structured meshes to achieve convergences on the model. These non-uniform patterns are especially useful in complicated geometries within various regions of the model, where a structured model would require a large number of partitions to resolve bad elements which cannot be meshed otherwise. The unstructured mesh generates structured mesh in simple geometries and would allow for local refinements of the grid in these more complex geometries.

The size of the mesh is relatively fine compared the default settings in the program. The finer the mesh, the better precision and accuracy in data, as well as an increase in data points when measuring across a number of nodes along an interface; however, a coarser mesh would require a shorter solve time while giving rough data that is less precise or accurate. Thus, a balance was struck by identifying an acceptable threshold for the mesh size. On average, for UBM thickness and current flow configuration models, the solve time was approximately three hours. As the model became more complex, such as added voids and Pulse-DC, that solve time would be extended, sometimes by up to a week. **Figure 28** illustrates the mesh of the WCSP submodel examined in this study and the following two studies. Take particular note of the x, y, and z coordinates in the origin included in the model. Default orientations in ABAQUS assumed the y axis to be in the direction of what is actually typically assumed as the z axis. All analysis takes this into account and the model is allowed to expand freely in the y direction.

While training, the boundary conditions of voltage were assumed in place of a current input. Voltages are calculated according to the resistance of the circuit for each current flow configuration. Temperatures are set, accounting for JH development with the current flow, such that the final temperature is 165°C. Convections are set to maintain the final temperature of 165°C with the air coefficient of 1.

With the assumption of a voltage input, the voltage input needs to be calculated to determine the voltage boundary conditions. The voltage boundary conditions are calculated by taking the current flow configuration and UBM thicknesses into account. The circuit has a combination between parallel and series circuitry. As the UBM increases, the overall resistance within the circuit increases. Additionally, depending upon the current flow configuration, the resistance will also differ between symmetry and asymmetry. A schematic of the circuitry is outlined in **Figure 29**, where the current paths are identified, as well as each resistance source.

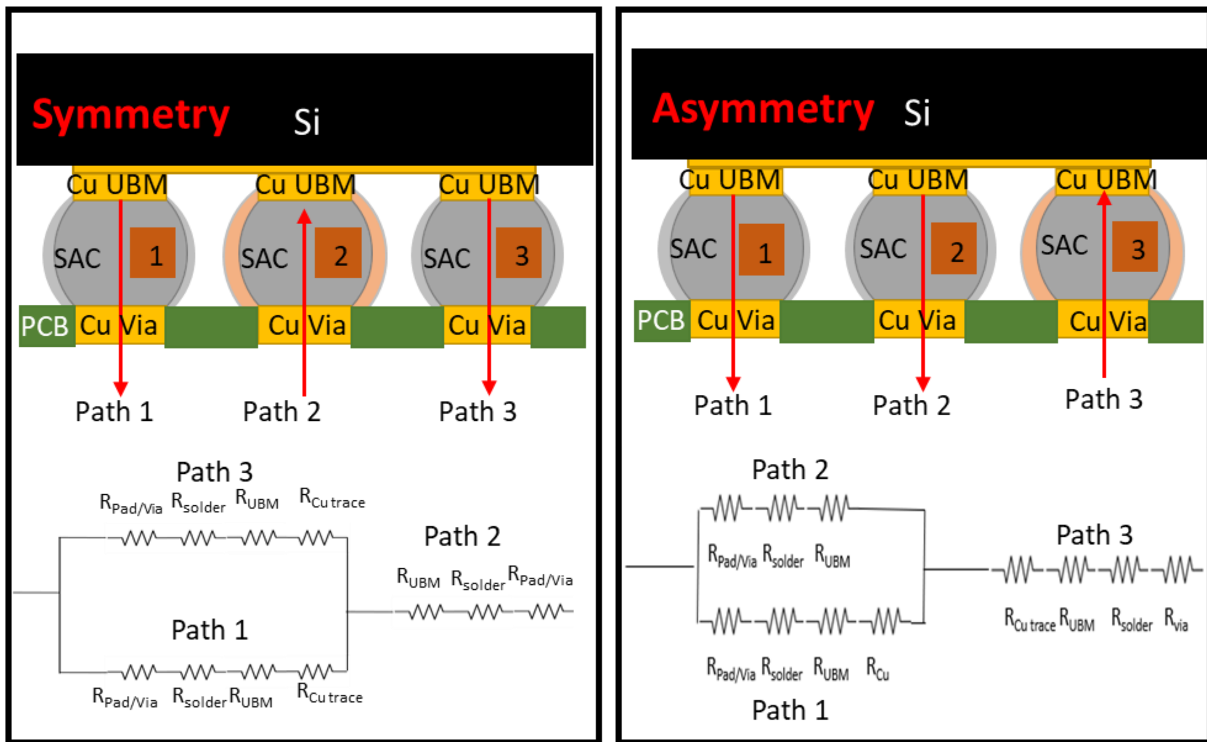

Figure 29 Schematic of current routed through WCSP circuitry for calculating the resistance and voltage boundary conditions along the circuit for each current flow configuration.

First, the resistance of each section of the WCSP model is calculated, including the Cu pad/via, solder, Cu trace, and the Cu UBM. This is done using **Eq. 20** and **Eq. 21** for square traces and round traces, respectively.

$$R = \rho * \frac{L}{T*W}[1 + \alpha(T - T_0)] \qquad \textbf{[Eq. 20]}$$

$$R = \rho * \frac{L}{\pi * (\frac{d}{2})^2} [1 + \alpha(T - T_0)] \qquad \textbf{[Eq. 21]}$$

As mentioned previously, the circuits for symmetry and asymmetry current flow configurations are comprised of a combination of series and parallel circuits. That in mind, **Eq. 22** and **Eq. 23** are used to determine the total resistance of the series paths and the resistance of the parallel circuit, respectively.

$$R_t = R_1 + R_2 + R_3 ... + R_n \qquad \textbf{[Eq. 22]}$$

$$\frac{1}{R_t} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} ... + \frac{1}{R_n} \qquad \textbf{[Eq. 23]}$$

In accordance with **Figure 29**, the resistances are calculated for each current flow configuration as follows. For the symmetrical current flow configuration, Path 3 and Path 1 are each individually calculated in series, and then calculated in parallel to one another. That final value from the parallel calculation is calculated in series with Path 2. For the symmetrical current flow configuration, Path 2 and Path 1 are each individually calculated in series, and then calculated in parallel with one another. The value from Path 1 and Path 2 in parallel is calculated in series with Path 3. The differences in the numbers of resistors in the circuit, in accordance with parallel or series, results in differing resistance values from circuits with symmetrical and asymmetrical current flow configurations.

Using Ohm's Law in **Eq. 24**, the voltages which are applied to each WCSP model are calculated with respect to their individual total resistances of their circuits, according to the current flow configurations. I is current (A), R is resistance (Ω), and V is voltage (V).

$$V = IR \qquad \textbf{[Eq. 24]}$$

Table 4. Voltage Boundary Conditions	**Voltage (4 A)**	**Resistance (Ω)**
18C Symmetry	0.031479764	0.007869941
18C Asymmetry	0.058810119	0.01470253
35C Symmetry	0.031522198	0.00788055
35C Asymmetry	0.058863204	0.014715801
50C Symmetry	0.03155964	0.00788991
50C Asymmetry	0.058910027	0.014727507

Table 4 Calculated Voltage Boundary Conditions

The voltage boundary conditions and resistance values for each circuit in the WCSP FEM models are highlighted in **Table 4.** The voltage boundary conditions applied with respect to the most common current application during EM testing, 4 A. With the known resistance values and the known current input value, V could be isolated and identified.

Sets are identified and assigned to surfaces of specified sections of the model: “POTEN-GROUND,” “POTENTIAL,” “XCONST,” “YCONST,” “ZCONST,” which are assigned 0 V for ground, voltage potential, displacement/rotation constant in the X direction, displacement/rotation constant in the Y direction, and displacement/rotation constant in the Z direction, respectively. **Figure 30** illustrates the set assignments for each of the sets.

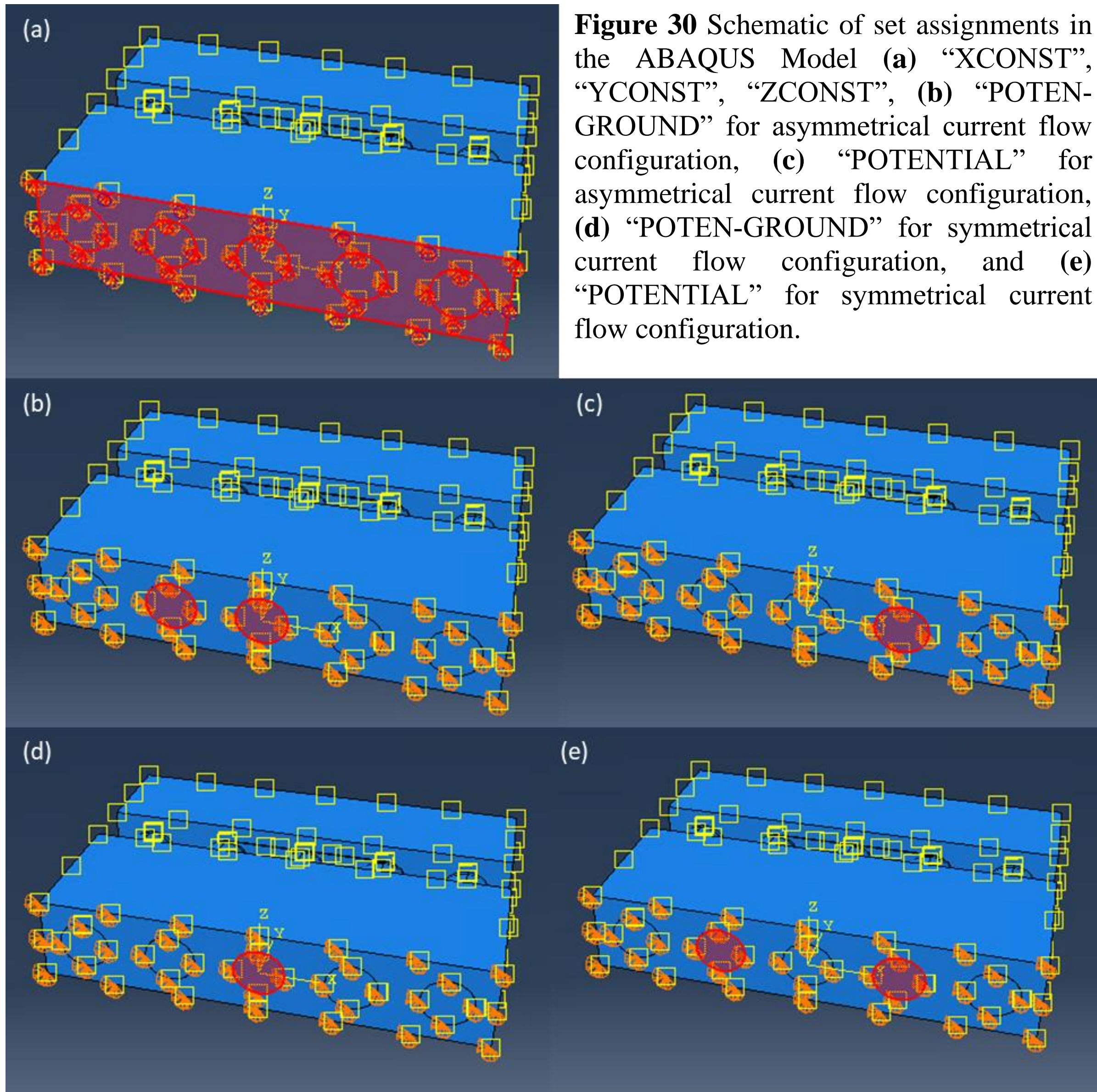

Figure 30 Schematic of set assignments in the ABAQUS Model **(a)** "XCONST", "YCONST", "ZCONST", **(b)** "POTEN-GROUND" for asymmetrical current flow configuration, **(c)** "POTENTIAL" for asymmetrical current flow configuration, **(d)** "POTEN-GROUND" for symmetrical current flow configuration, and **(e)** "POTENTIAL" for symmetrical current flow configuration.

Transient FEM studies are to be carried out for each UBM thickness and current flow configuration. The initial step defined the X, Y, and Z constants and the ambient temperature. The ambient temperature is set so that the final temperature, after current begins running, is 165℃. This takes some trial and error to get a good approximation for the total FEM experiment. The second step expanded upon the initial step boundary conditions and incorporated a convection boundary condition on all exposed surfaces with an air coefficient of 1. The second step is a

transient study over the span of 10,000 seconds, with a total of 1,000,000,000 iterations. The initial, minimum, and maximum increment sizes are 0.001, 0.0001, and 100, respectively. The maximum temperature by which the model can change per increment is 2°C. Looking at **Figure 30**, the voltage input corresponds to the “POTENTIAL” sets in both symmetry and asymmetry current flow configurations. **Table 4** outlines the voltage values applied based upon the current flow configuration and the UBM thickness. This information is applicable to the current flow configuration study, the UBM thickness study, and the void growth study.

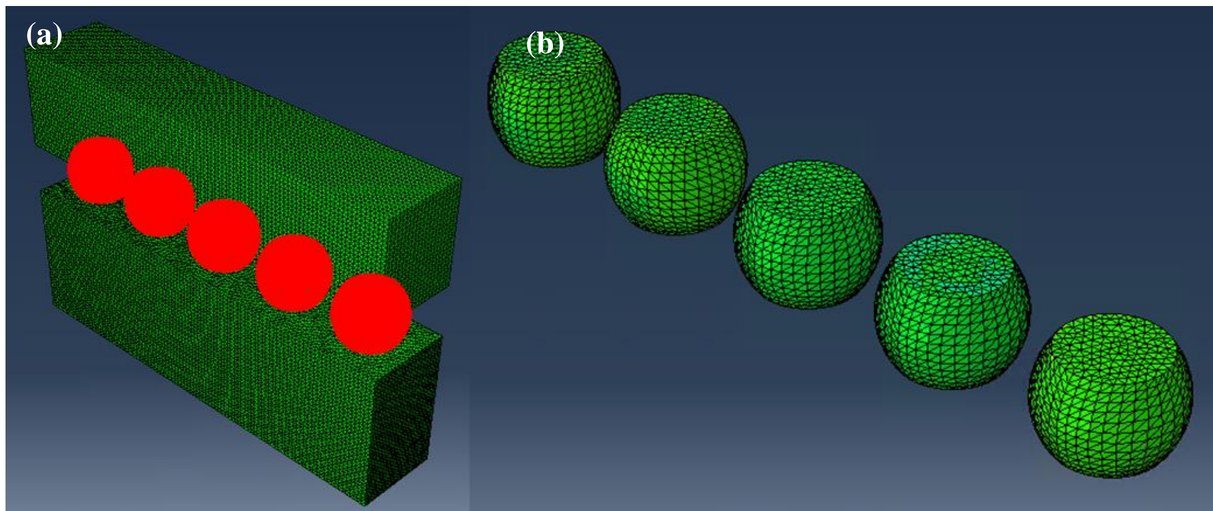

Figure 31 Isolating solder joints, the focus of the study. **(a)** shows the solder joints highlighted in the submodel before being replaced in **(b)**.

Once all boundary conditions are set, meshes are completed, and materials are defined, a job is created and submitted for the solver to complete. Once the solver is complete, post-processing is necessary to obtain important data, particularly for the stress in the Y direction, temperature to obtain the JH generation data, and current crowding data.

In the results tab, the solder joints are selected and isolated for post-processing examination, as demonstrated in **Figure 31**, which shows the stress results of the asymmetrical current flow configuration model in the results viewport of ABAQUS. Notice the color variances

in the DUT, the solder joint second from the right. In this image, the stress in the Y direction is considered. However, judging the stress by the naked eye will not yield satisfactory precision of the results.

To obtain a more precise estimate of the stress and temperature development over time, a graph obtained by creating XY data from the field output in the output database (ODB). Over time, current crowding will remain constant once it is on, so that will be measured along a path across the interface between the DUT and the UBM rather than at a node or integration point over time. To obtain the time data for stress, an integration point is selected, and the stress development over time is calculated. The final stress will be the maximum stress, as it plateaus at this point.

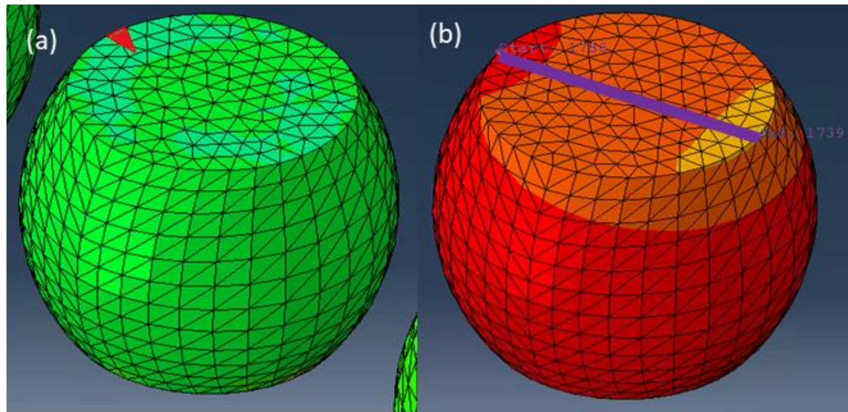

Figure 32 (a) integration point selected for stress, current crowding, and temperature. **(b)** path across interface for stress, current crowding, and temperature.

The integration point, or element, is selected based upon where the highest amount of current crowding, stress, and JH is likely going to be, according to the viewport, as can be seen in **Figure 32 (a)**. To obtain better data for stress, the integration point where the highest level of stress is located is chosen. The integration point selected for exporting stress, current crowding, and temperature over time. A program may be written to simplify this step; however, because it may require judgement from the user to identify the maximum integration point where stress,

temperature, and current density are at a maximum, it may be more beneficial to do so this process manually, especially in the case of symmetry because the maximum value may not consistently be on the same side of the DUT or on the same element. To gain an understanding of the localized JH, stress, and current crowding on the DUT, a path is created along the X-axis on the cathode end of the DUT**. Figure 32 (b)** illustrates the line created across the interface between the solder bump and the Cu UBM, is done by selecting a node on either rend of the DUT at the DUT/UBM interface.

To export the data so it may be processed and analyzed using an excel sheet and KaleidaGraph, one would simply edit the data, and copy and paste the data to the appropriate column in an excel file. One may also export the data into its own excel file. This is done for both the time data and the distance along a path data. As the void grows, the distance along the path will decrease. To determine the data along a path as the void grows, the data is arranged along the path such that the edges align, subtracting the true distance from the original distance, 0.230 mm.

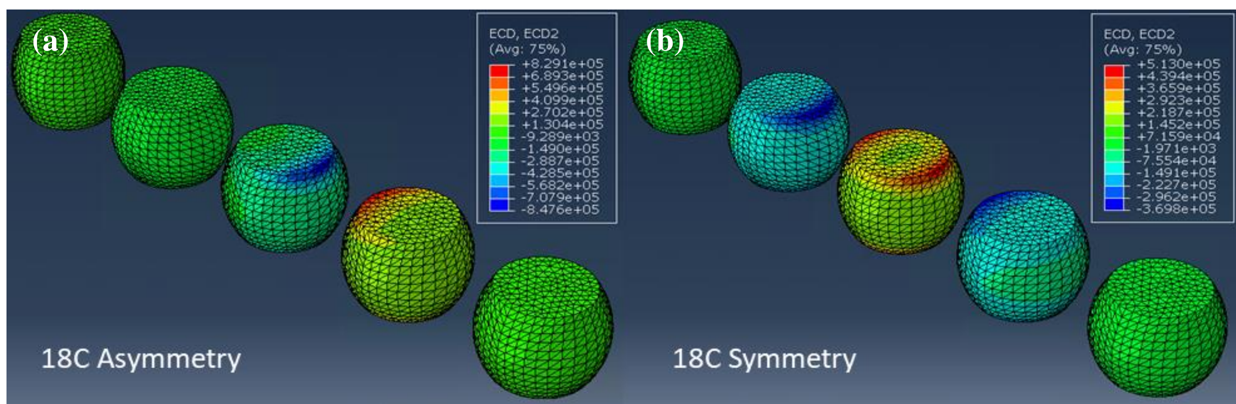

Figure 33 18C **(a)** Asymmetry and **(b)** Symmetry Current Flow Configuration Current Density Voltage Input.

Figure 33 is a snapshot of the solved 18μm UBM WCSP model (18C) studies, illustrating the current density in the DUT under **(a)** asymmetrical and **(b)** symmetrical current flow configurations in accordance with the voltage inputs calculated in **Table 4**. The asymmetrical current flow configuration forces the current to enter through the bottom of the solder bump second

from the right, or the DUT. It exits the top left corner of the DUT, the highest amount of current density being 0.08 kA/cm^2. The symmetrical current flow configuration forces the current to one corner of the DUT.

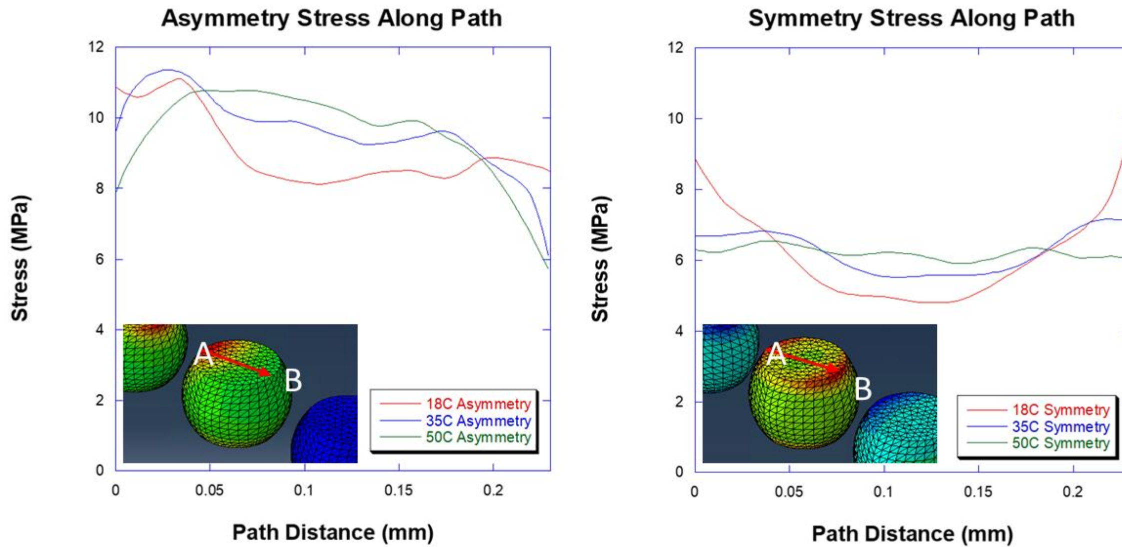

Figure 34 Comparative compressive stress across DUT interface for **(a)** asymmetrical and **(b)** symmetrical current flow configurations with voltage input conditions.

Figure 34 illustrates the trend of the current and stress distribution along the interface between the solder bump and the UBM, with a voltage input. Where the current density is the highest is where current crowding and JH are most likely to be most prominent. It is also in these sites where the DUT is most susceptible to EM voiding. The JH accelerates the EM progression while the stress would theoretically block the void growth. The magnitude of the stress and current density is notably higher in asymmetrical current flow configurations than in the symmetrical current flow configuration. This may support the prediction that early-failed WCSPs in either current flow configuration had comparable MTTFs and therefore reliability. This can largely be credited to the c-axis alignment in the DUT's microstructure at the site of current crowding. Meanwhile, later-failed samples had notably longer MTTFs for the symmetrical current flow configuration, likely owing to the difference in stress and current crowding on the DUT. The

current crowding is lower in the DUT for WCSPs studied under symmetrical current flow configurations, and therefore these samples tested under these conditions are not as susceptible to EM failure. The phenomena behind these findings will be further discussed in future sections. This model can be supportive of the general experimental trend observed; however, the current density is lower than what was predicted.

Figure 35 showcases two plots generated along a path across the DUT at the interface between the solder bump and the UBM in the x-direction. One may observe in both plots that the stress is notably dampened with thicker UBMs. Likewise, the current density is also dampened, supporting the secondary role that the UBM plays in the WCSP model. The voltage applied is in accordance with those calculated and presented in **Table 4**.

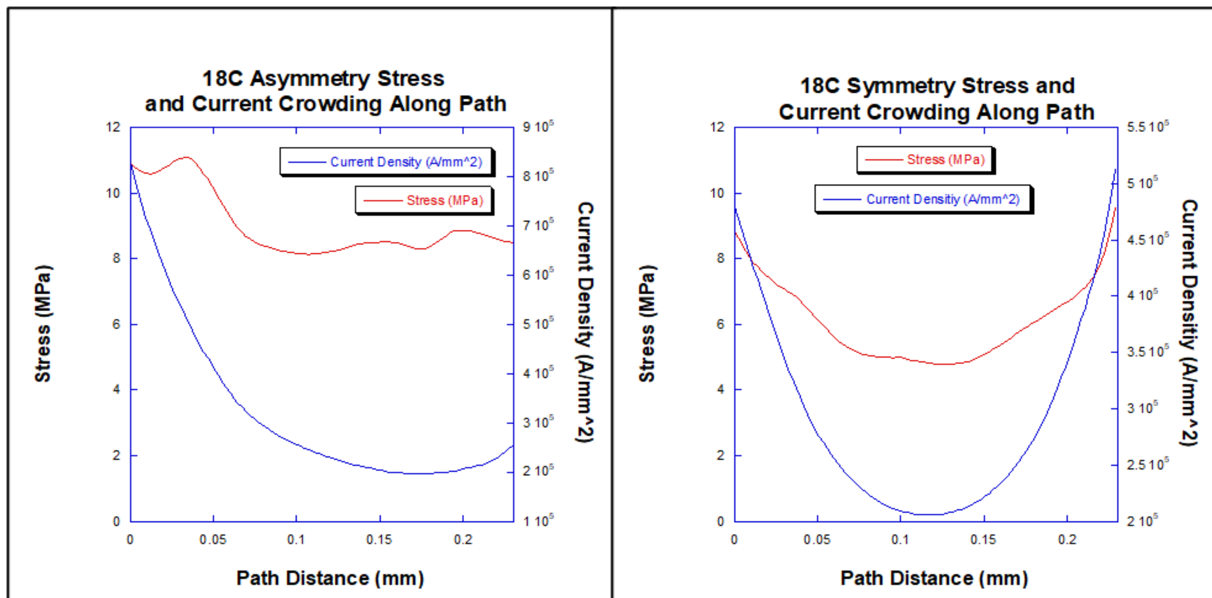

Figure 35 Plots of von Mises stress along a path with respect to current density for 18C WCSP **(a)** asymmetry and **(b)** symmetry models with voltage input.

Pulsed-DC studies were done using the voltage inputs to gain further validation of the feasibility of ABAQUS CAE for transient studies. For the first 10,000 seconds, the voltage was

applied and then the pulsed-voltage was applied. An amplitude function was applied to the voltage in order to dictate the "on" vs. "off" time or DF. While we observe a lower level of stress in the 33% DF condition, it takes a considerably longer amount of time to plateau to the point where the stress is simply fluctuating rather than fluctuating and declining in such a shark tooth fashion as the 50% DF and the 75% DF. In fact, the time for which the model takes to settle with the pulsed DC depends on the DF, suggesting that other factors are changing within the model as it is solving – likely the resistance and current density, which is causing the JH to change as well, thus impacting the stress trend. **Figure 36** is a plot of the stress fluctuation with pulsing voltage, illustrating exactly this observation. This is another concern to be addressed next.

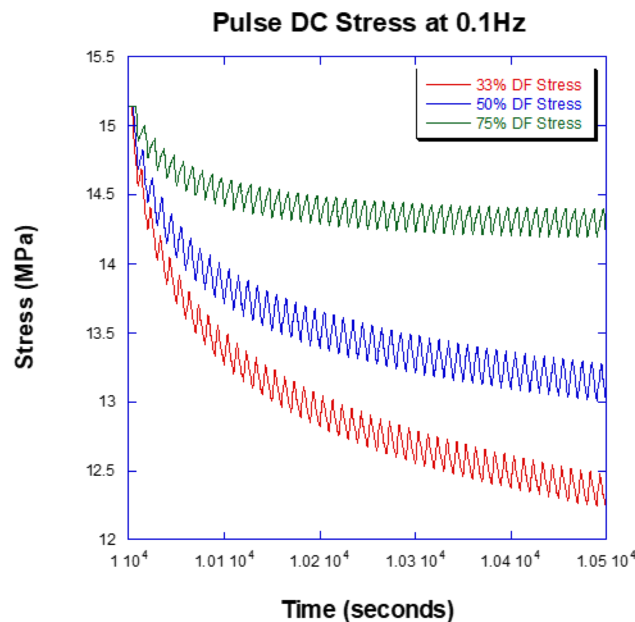

Figure 36 Pulsed-DC von Mises stress for 33%, 50%, and 75% DFs under voltage input conditions.

The results from WCSP models utilizing a voltage input boundary condition yielded trends which explain the comprehensive reliability performance of the WCSPs and their variable UBM thicknesses under different current flow configuration. However, utilizing a voltage boundary condition instead of a surface current density load resulted in unrealistic and inaccurate results. The resistance increases with JH. Following Ohm's law, with a constant voltage but an increasing

resistance, the current density applied was actually much smaller than was required. To maintain the JH in this sort of setup, the air coefficient was set to 1, which is typical of air without forced convection. In EM testing, forced convection is necessary to maintain the ambient temperature, and that can range between 5 and 500 W/(m^2K). So, not only is the current density too low, but so is the air coefficient. This, in turn, affected the stress development within the model, as well. Additionally, the time for which the model takes to settle down using a voltage input takes considerably longer, likely owing to the change in the current and resistance with the JH over time. This is especially clear in transient pulsed-DC studies, where the stress fluctuations are smaller than expected. Further, the time for which the pulsed-DC stress and JH to plateau and the model to settle takes well over 500 seconds for higher DFs and even longer for low DFs. This is a highly indicative clue that the voltage may be constant because that is what was dictated, but that does not mean that the current and the resistance remain constant. That said, using the voltage input boundary condition does not properly simulate experimental methods, in which WCSPs are subjected to constant current conditions. A solution to these issues is by opting to use a constant surface current density load rather than a voltage boundary conditions (while maintaining the voltage grounds). The next section delves into the steps to determine the boundary conditions which best capture the physics with a constant current density.

3.5 Modifying FEM Boundary Conditions to Reflect Current Density, Joule Heat, and Convection Parameters

The solution to the shortcomings of voltage boundary conditions in ABAQUS CAE is to apply a current density load, in this case, 9.63 kA/cm^2. It is also predicted that while the submodels are excellent at cutting the computational costs of the simulation, they result in higher JH and stress than what may be predicted in a full-sized model.

Following the CAD parameters laid out in **Table 2**, the submodel is created as a single part in SolidWorks. It is comprised of 18 sections, including a PCB, five Cu vias, five SAC solder bumps, three UBMs, one RDL, two Cu posts, and one Si die. The SolidWorks model is exported as a STEP file, and then imported into ABAQUS/CAE. Upon the importation of the STEP file, the material properties are defined according to **Table 3**, the material sections are generated, and each of the sections is assigned a material section.

Just as was done in the voltage studies, the instances were established, and a mesh was generated using the assembly tab of the model tree. The entire submodel seed size was set as 2E-5. A linear thermal-electrical-structural element type was assigned to the mesh and the mesh control was set to a Q3D4 free mesh. After generating all of these, the mesh was then generated on the model. This will result in a number of elements and nodes, which will depend on the size of the model and the mesh size. For instance, for the 18C model with the 18µm UBM under these mesh settings, the meshed model's number of nodes and elements are 124,660 and 679,926, respectively. Models with thicker UBMs would have a larger number of nodes and elements.

Surfaces and sets were then defined. A current density input surface was defined, to which a surface current density load was applied later. Convection surfaces, CONVEC1 through

CONVEC7-2 were also defined. The total number of surfaces defined are 9. Sets are also assigned, which are tagged when setting up the boundary conditions. Three sets for the X, Y, and Z constants were defined and assigned to the bottom surfaces of the model (Cu vias and PCB bottom). Next, the voltage ground set was defined and also defined and assigned to the bottom of the Cu vias connected to the circuit, in accordance with the current flow configuration.

Next, two steps were defined. The first step, labeled "Initial" is steady-state, which is useful for establishing the X, Y, and Z constant boundary conditions, which limit the model from rotating or sliding in any direction. These were assigned to the bottom faces of the PCB, and Cu vias of the model. The predefined ambient temperature is also defined in the first step, which was set to 150°C for this step. The second step, labeled "Step 1" is transient, which means it is time-dependent and is useful for solving problems which lack linearity solutions. "Step 1" was set to calculate for 500 seconds. The initial step was set to 0.01, the minimum step size was set to 0.001, and the maximum step size was set to 10. The maximum temperature change allowed per increment was set to 2 degrees.

In "Step 1", the boundary conditions were set. The predefined boundary conditions and the constraints which were defined in the "Initial" step were automatically propagated in "Step 1". Next, the voltage grounds were assigned to the voltage ground set previously assigned and the voltage value was set to zero and instantaneous. The current surface load was then applied to the surface previously assigned for the current input. Because this model was set to simulate the findings under 4 A current, the current density defined as uniformly 9.63 kA/cm^2 with an instantaneous amplitude, meaning it is constant, which is consistent with direct current conditions. Next, the convection air boundary conditions were set first by assigning the interaction properties, which will be referenced when assigning interactions. This interaction property is the air

coefficient, which is set to 250 W/(m^2K) based on the level required to achieve respectable JH in a full model, where the JH is maintained at around 10°C and the model is under forced convection. Next, the interactions are assigned as surface film conditions. The sink temperature was set to 150°C and the air coefficient was referenced.

Output requests were selected. In ABAQUS, two types of outputs are involved: History Output Requests and Field Output Requests. History Output Request selected was energy, and outputs every 1 increment, n, was selected. The Field Output Requests selected include energy, contacts and forces, elastic stress, elastic strain, temperature (nodal and integrational), and current density. The data for the Field Output Requests was collected every 2 increments, n.

Once all boundary conditions, material properties, and mesh are all generated and assigned, a job is created. The job was set to save the data in a documents folder. The number of processors was set to 10. The job was then submitted and allowed to run, which took approximately 3 hours for the 5x1 submodel simulation.

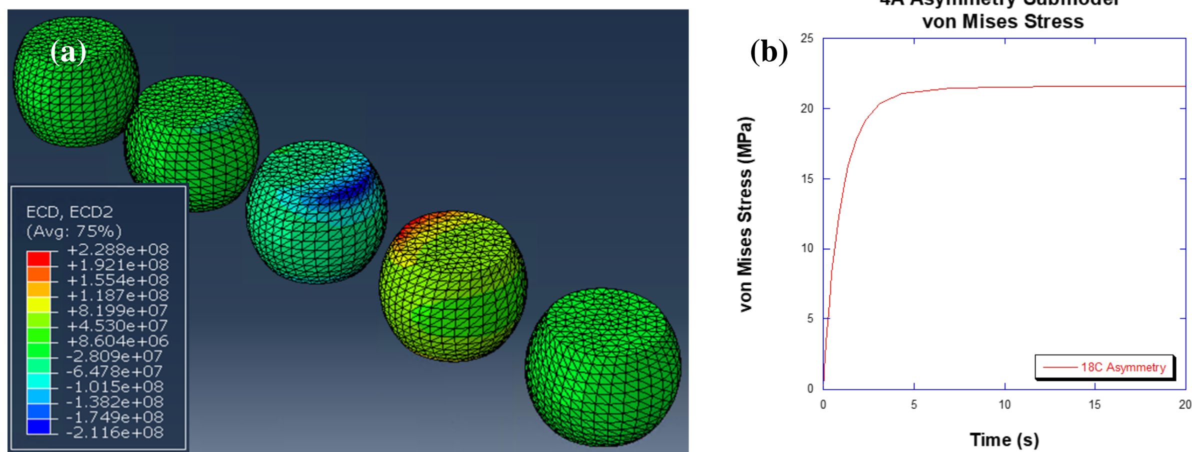

Figure 37 **(a)** Current density and **(b)** von Mises Stress in submodel subjected to 4 A asymmetrical current flow configuration

Preliminary constant surface current density load studies revealed that the model to settle surprisingly quickly in a submodel – within 15-20 seconds, as shown in the plot in **Figure 37 (b)**, where the stress vs. time is presented. A full model is necessary for verification, to determine if there is a thermal mass effect in the model, and to estimate the proper forced air convection coefficient for the model.

The full model follows the design outlined in **Table 2**. It consists of the PCB with a 5x5 BGA mounted onto pads covering Cu vias with a pitch of 0.4 mm. There are 25 each of solder joints and Cu vias. 18µm-thick UBMs are situated on top of the circuit solder bumps (identifiable by the solder bumps with finer mesh structures). Above the UBMs are 0.0007 mm RDL layers, which are connected to the Si die. All the surrounding support bumps which are not part of the WCSP sample circuitry are bonded to the Si die by 0.0187 mm-thick Cu UBMs. Only the 18µm-thick UBM WCSP sample was examined in this model due to computational expense.

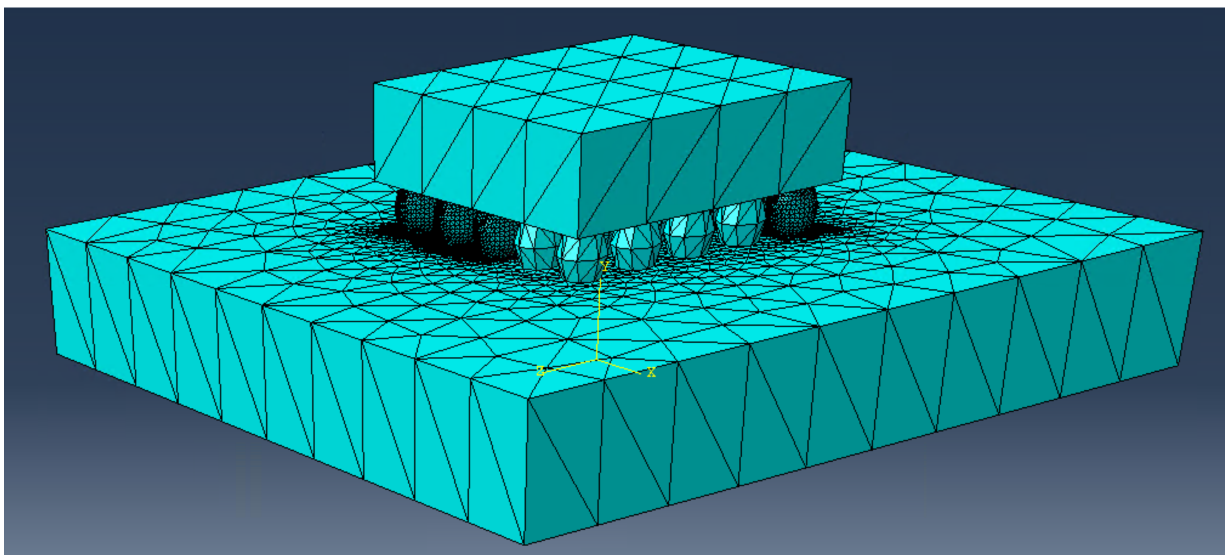

Figure 38 Full model mesh structure.

First, the full model must be meshed. Seeing as it has considerably more sections, amounting to 79, and therefore elements and nodes a balance between the solve time, the mesh size, and the convergence of the model is necessary. The mesh must be refined in critical areas (circuit Cu vias, UBM, RDL, and solder bumps, including the DUT) and can be coarser in less critical areas (Si, PCB, non-circuit solder bumps and vias). The finer mesh was set to 2E-5 (just like the submodel). Meanwhile, the coarser solder bumps and vias were set to 2E-4. Finally, the Si and the PCB were set to 0.0005. The PCB and the Si chip were easier to set for a coarser mesh due to their simplicity in design. The Cu vias and the solder bumps that are not critical for the study were set at a finer mesh than the Si and PCB for two reasons: 1) they are smaller sections with a smaller number of nodes so the mesh, if successfully likely would not have succeeded on these alone; and 2) in order to meet with the critical DUT and circuit mesh, a medium was necessary to minimize the number of bad elements. The mesh of the full model may be observed in **Figure 38**.

An initial full model with 5 A current (12.03 kA/cm^2) was used to estimate these values. The target Joule Heat was approximately 13-15°C. Because the model was likely to settle about 5x longer than the submodel, 10,000 seconds would have been a ridiculously long solve time. Thus, the step time was set to 150 seconds for good measure. To obtain the respectable JH, the air coefficient was set to 250 W/(m^{2}K). The simulation time for the full model was just over 3 days. **Figure 39** illustrates the full model's current density for the **(a)** asymmetrical current flow configuration and **(b)** the symmetrical current flow configuration. **Figure 40 (a)** is a plot of the von Mises vs time for the asymmetrical model. It takes approximately 75 seconds for the model's JH and stress to settle for both symmetrical and asymmetrical current flow configurations. Additionally, the same observation was made for the full model which was subjected to 4 A

current, as is observed in **Figure 41** and **Figure 42**. Thus, it is proven that there is, indeed a thermal mass effect in the model.

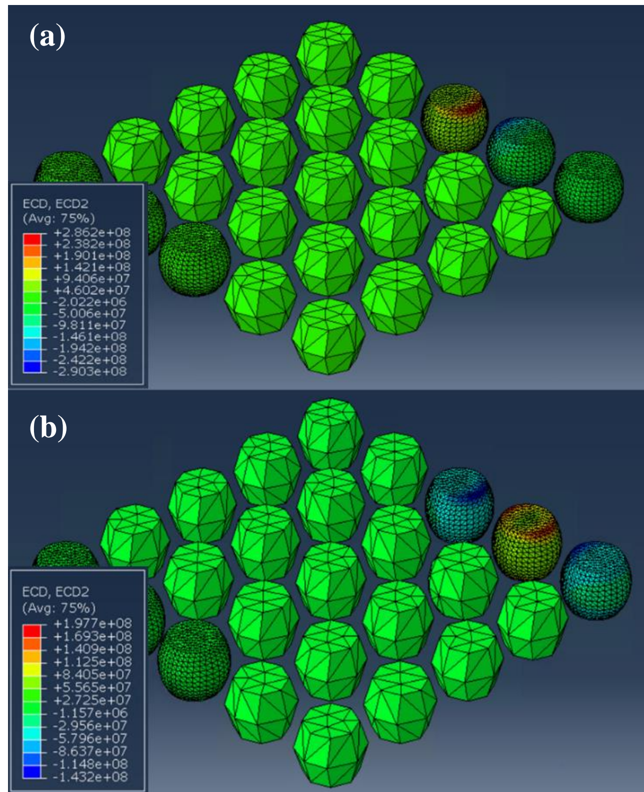

Figure 39 View of current density in full model subjected to 5 A in **(a)** asymmetrical and **(b)** symmetrical current flow configuration.

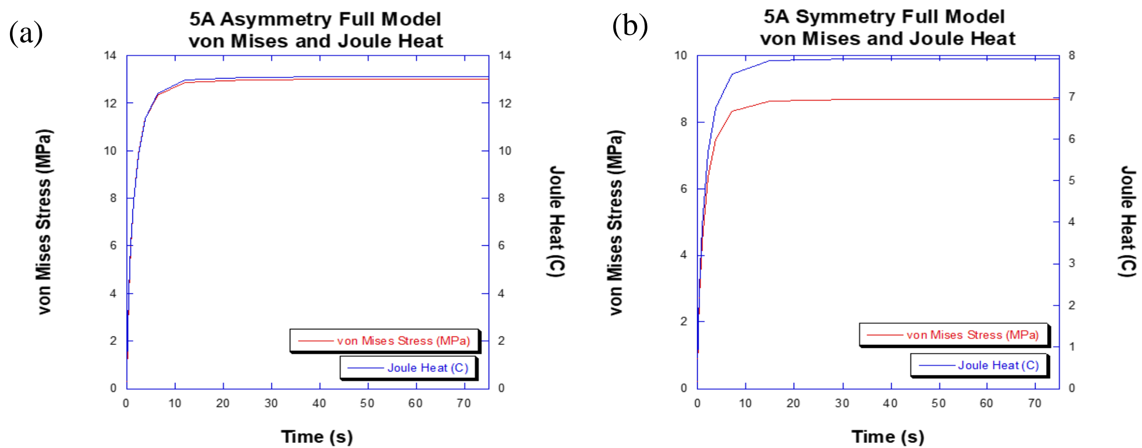

Figure 40 Full Model von Mises and JH vs. Time under 5 A current in **(a)** asymmetrical and **(b)** symmetrical current flow.

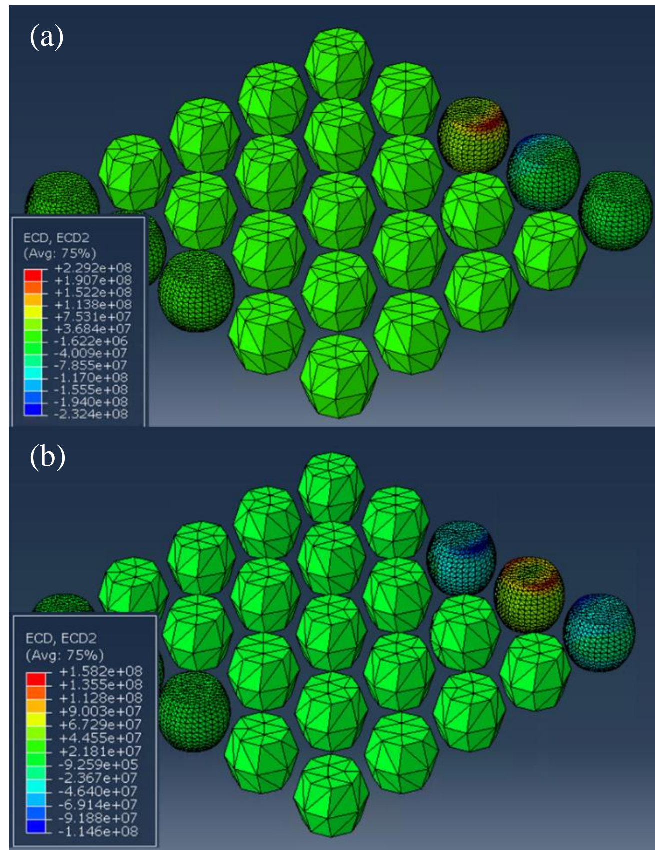

Figure 42 View of current density in full model subjected to 4 A in **(a)** asymmetrical and **(b)** symmetrical current flow configuration.

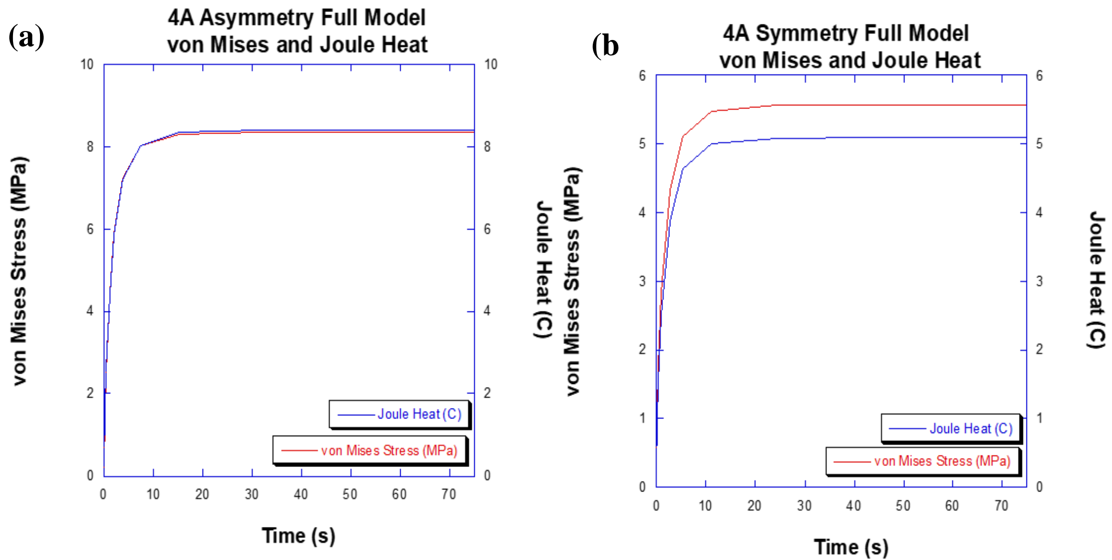

Figure 41 Full Model von Mises and JH vs. Time under 4 A JH and von Mises in **(a)** asymmetrical and **(b)** symmetrical current flow.

The model settled within 75 seconds, indicating that the full model takes about 5x longer to settle than the submodel does. The JH is lower in the full model than in the submodels, as well. This proves that we do indeed see a thermal mass effect. The key takeaway from this study is that the trends observed in the submodel may still not report perfect values; however, the trends should still be relevant to theoretically explaining EM simulation results. With this information, we can carry on with the simulations on submodels, which is necessary for identifying the stress trends with respect to EM reliability with varying package parameters.

CHAPTER 4: CURRENT FEEDING CONFIGURATIONS AND THEIR FUNDAMENTAL EFFECTS ON ELECTROMIGRATION RELIABILITY OF WAFER-LEVEL CHIP SCALE PACKAGE SOLDER JOINTS

In this chapter, the effects of the current flow configuration on the current crowding, JH, and stress development and their relationships to the EM failure kinetics observed in comprehensive EM testing of WCSPs will be examined. The two current feeding configurations studied are symmetrical and asymmetrical, whereby the DUT experiences the current crowding on both corners and on one corner at the top of the DUT, for each respective current feeding configuration.

4.1 Background

In this study, the fundamental effects of current feeding configurations on the JH, current crowding, and stress by using FEM. The results of this simulation are expected to explain underlying stress effects which impact WCSP interconnects which fail later in accelerated EM tests. The current feeding structures which were examined are symmetry and asymmetry. Accelerated EM test data indicates that there is a significant amount of stress induced by JH and current crowding at the cathode end of the SAC solder interconnect. The work done in this study is meant to confirm this prediction and to identify a key link between the stress generation and the MTTF with respect to current flow configuration.

Experimental results suggest a likelihood that an asymmetrical current feeding configuration leads to a higher amount of current crowding at the cathode end of the DUT, which is where the highest amount of JH occurs. The typical amount of JH generation observed in tested WCSP samples is around 10°C of JH. This high amount of JH from current crowding results in a

level of stress high enough to influence EM failure kinetics as it plays a role in either accelerating or postponing EM failure. The prediction for FEM results is that they will reveal a high amount of current crowding in the asymmetry current flow configuration as the current exits through one corner of the DUT, while the current density will be almost halved for the symmetry current flow configuration as the current path splits and the current exits out of the two top corners of the DUT. The results of this effect will vary depending on the UBM layer thickness, another study for which the objectives will be discussed in Chapter 5.

Experimental results further indicate that there is no difference in MTTF between symmetry and asymmetry current flow configurations in early failures, which may be attributed to EM failure along the [001] c-axis alignment of Sn grain orientation. Later failures, however, appear to show that WCSPs with thinner UBMs show a larger number of later failures in samples tested under symmetrical current flow configurations than asymmetrical flow configurations. This may be attributed to the difference in the level of current crowding and JH, resulting in a different level of stress on either corner at the top of the DUT, where the voids are most likely to occur. Further, this difference in later-failed samples is more prominent in those with thinner UBMs than those with thicker UBMs, possibly owing to the decrease in current crowding with UBM thickness. FEM results are expected to confirm a difference in current crowding and stress among the two current flow configurations. FEM results should lead to a better understanding of how current crowding and stress contribute to experimental EM reliability results.

4.2 Comparative EM Performance of WCSPs under Symmetrical and Asymmetrical Current Flow Configurations

Comprehensive EM tests comparing the WCSP samples under two different current flow configurations were conducted previously by Yi Ram Kim, a PhD student in Dr. Choong-Un Kim's research lab at the University of Texas at Arlington. Samples were provided by Texas Instruments. 20 samples of each sample type, WCSPs with 18 µm, 35 µm, and 50 µm-thick UBMs were tested under the same conditions with the same level of current and ambient temperature accounting for JH in the DUT under each current flow configuration.

Figure 43 is an BSE image obtained using an SEM of a typical cross-section of an untested WCSP solder joint. The interface between the UBM and the SAC solder joint, the location at the cathode end of the solder joint where voiding is most likely to occur, is still intact. The solder joint is clearly bonded to the Cu Via/Lead Frame, with no signs of tension or IMC formation. This is the starting point before the EM testing commences. During the EM test, a void would form at one

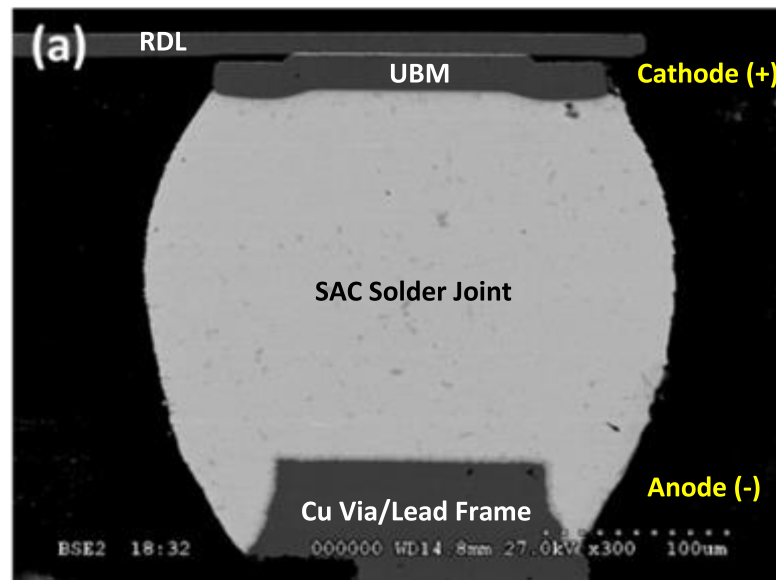

Figure 43 Cross-sectional BSE image of an untested WCSP solder joint [**27**].

of the corners at the cathode end of the DUT as the conductive material is transported via EM. As EM transpires, the IMC will grow so that as one investigates closer to the Cu via, a higher concentration of Cu is observed as the Cu material displaced from the cathode end of the solder joint accumulates at the anode end of the solder joint. It was originally predicted that the key difference between the symmetrical and asymmetrical current flow configurations is the level of current crowding. It was assumed that the level of current crowding combined with the JH and opposing effects of compressive stress would be the deciding factor. From a logical standpoint, asymmetrical current flow configuration samples should fail at a faster rate than samples tested under a symmetrical current flow configuration. This original prediction can be credited to the added current crowding at one corner of the cathode end of the solder joint. This corner would be highly susceptible to EM with a considerably higher current density, and thus electrons colliding with conductive atoms. However, this theory was thwarted by a separate complication: microstructural effects at the typical failure site on EM failure kinetics.

Interestingly, when comparing the EM performance between the samples tested under symmetrical and asymmetrical current flow configurations, the reliability among early-failed samples did not particularly differ. Thus, the general consensus among the EM testing results was that there was no obvious difference in the MTTF for samples which failed early on in the test. In fact, early failures appeared to be random. It was determined that while there is no notable difference in the reliability of packages which failed earlier in the test, those which failed later in the test appeared to have higher reliability under the symmetrical current flow configuration. This key difference was most notable in the WCSPs with 18µm-thick UBMs than in those with 50 µm-thick UBMs. This can be observed in the two cumulative probability plots comparing the

symmetrical and asymmetrical reliabilities for both WCSPs with 18μm-thick UBMs and 50 μm-thick UBMs featured in **Figure 44**.

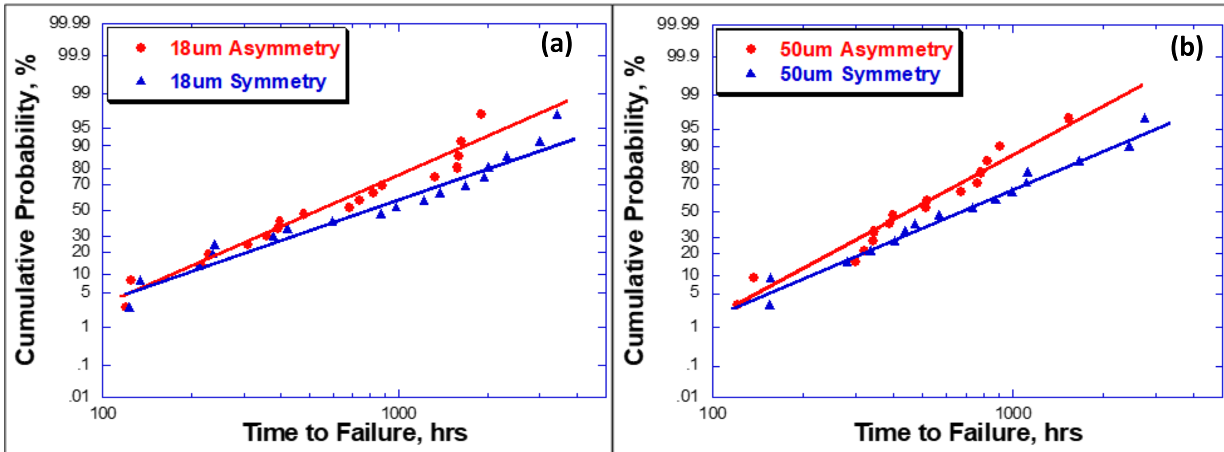

Figure 44 Cumulative probability vs TTF plots comparing reliability between symmetrical and asymmetrical current flow configurations for **(a)** 18C and **(b)** 50C WCSP samples.

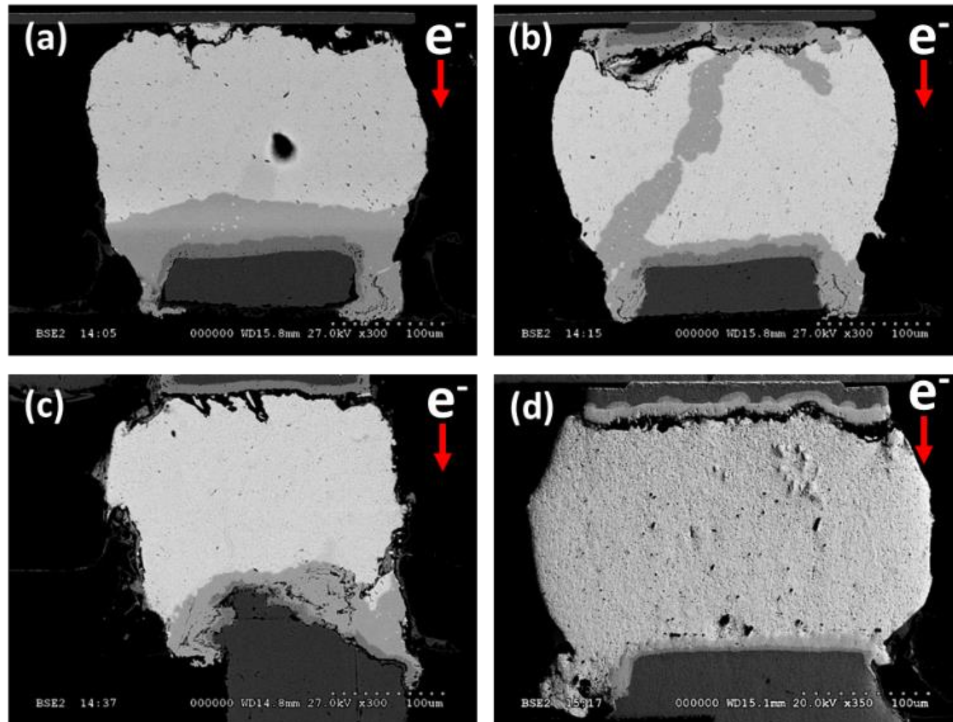

Figure 45 SEM images obtained by Yi Ram Kim et. al. of early-failed samples tested in different batches. **(a)** is the 1st failed sample among WCSP samples with 18μm-thick UBMs, **(b)** is the 2nd failed sample among WCSP samples with 18μm-thick UBMs, **(c)** is the 3rd failed sample among WCSP samples with 18μm-thick UBMs, and **(d)** is the 4th failed sample among WCSP samples with 15 μm-thick UBMs [27].

Figure 44 contains plots of the cumulative probability as a function of time to failure (TTF) for **(a)** 18μm UBM symmetry vs asymmetry and **(b)** 50 μm UBM symmetry vs asymmetry. Judging by the plots, there appears to be no major difference in MTTF between symmetry and asymmetry current flow configurations early failures. This may be attributed to EM failure along the c-axis alignment of Sn grain orientations, and further investigation done by Yi Ram Kim et. al. [27] support this theory. Meanwhile, **Figure 45** includes four cross-sectional SEM images of the first, second, and third samples which failed among a batch of WCSP samples with 18μm-thick UBMs and the fourth sample which failed among a batch of WCSP samples with 15 μm-thick UBMs. Comparing these SEM images with the cross-sectional SEM images of samples which

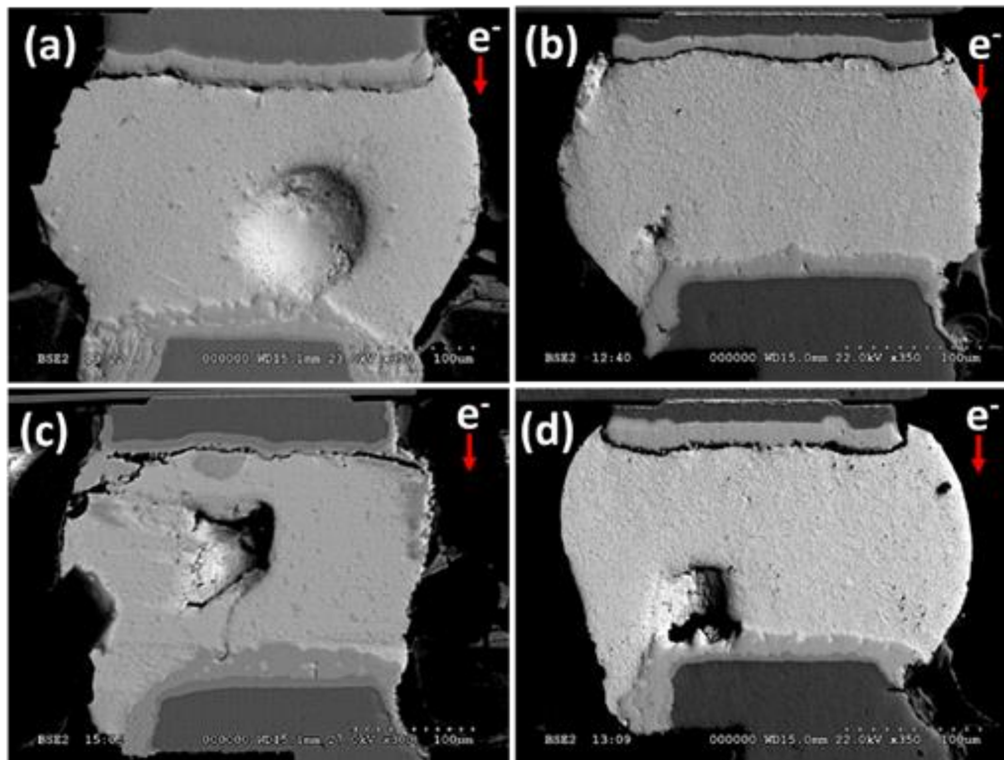

Figure 46 SEM images obtained by Yi Ram Kim et. al. of early-failed samples tested in different batches. **(a)** is the 17th sample which failed among WCSP samples with a 32 μm-thick UBM, **(b)** is the 18th sample which failed among WCSP samples with 15 μm-thick UBMs, **(c)** is the 18th sample which failed among WCSP samples with 18μm-thick UBMs, and **(d)** is the 19th sample which failed among WCSP samples with 15 μm-thick UBMs [27].

failed later in the test, it is difficult to identify any key microstructural differences that would give any indication of why the WCSP samples which failed early on in the test appears to have a random failure trend. The SEM images of WCSP samples which failed later in their respective tests are feature in **Figure 46**.

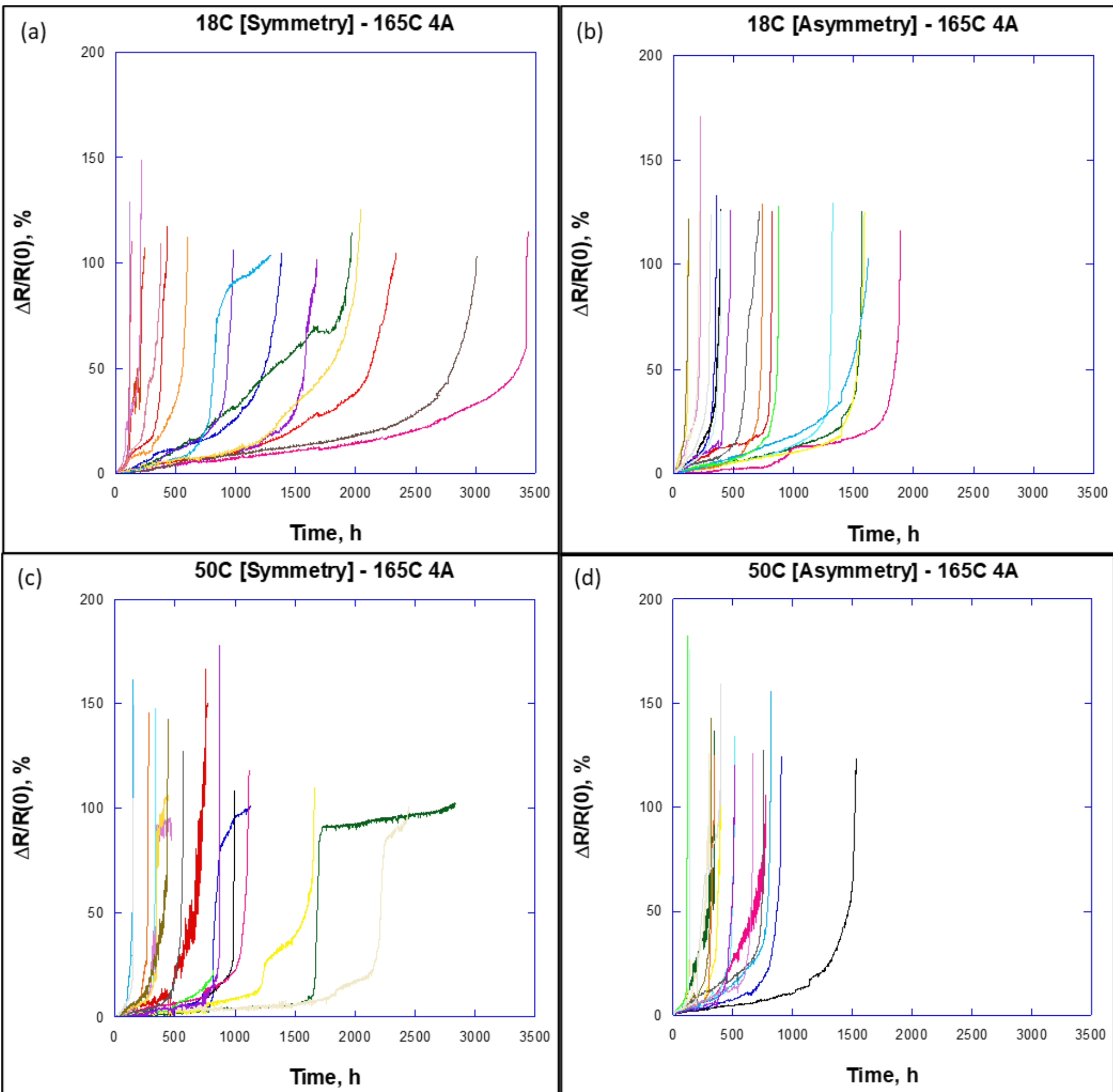

Figure 47 EM plots of **(a)** 18μm WCSP tested under symmetry, **(b)** 18μm WCSP tested under asymmetry, **(c)** 50 μm WCSP tested under symmetry, and **(d)** 50 μm WCSP tested under asymmetry 165°C and 4 A test conditions.

To further investigate the WCSP failure kinetics among samples which failed early on in the EM test, the raw data was compared. **Figure 47** shows four plots with raw data from 18µm symmetry and asymmetry tests under 165°C and 4 A conditions, and 50 µm symmetry and asymmetry tests under 165°C and 4 A conditions. When examining the %R change in either 18µm or 50 µm samples appears to be random; however, runaway failure appears to happen at later times in symmetry than asymmetry, which can be attributed to the current flow configuration and resultant difference in current crowding.

EBSD data obtained by Yi Ram Kim et. al. demonstrates the likelihood that early failure rates are heavily influenced by the microstructure at the failure site, in addition to the current

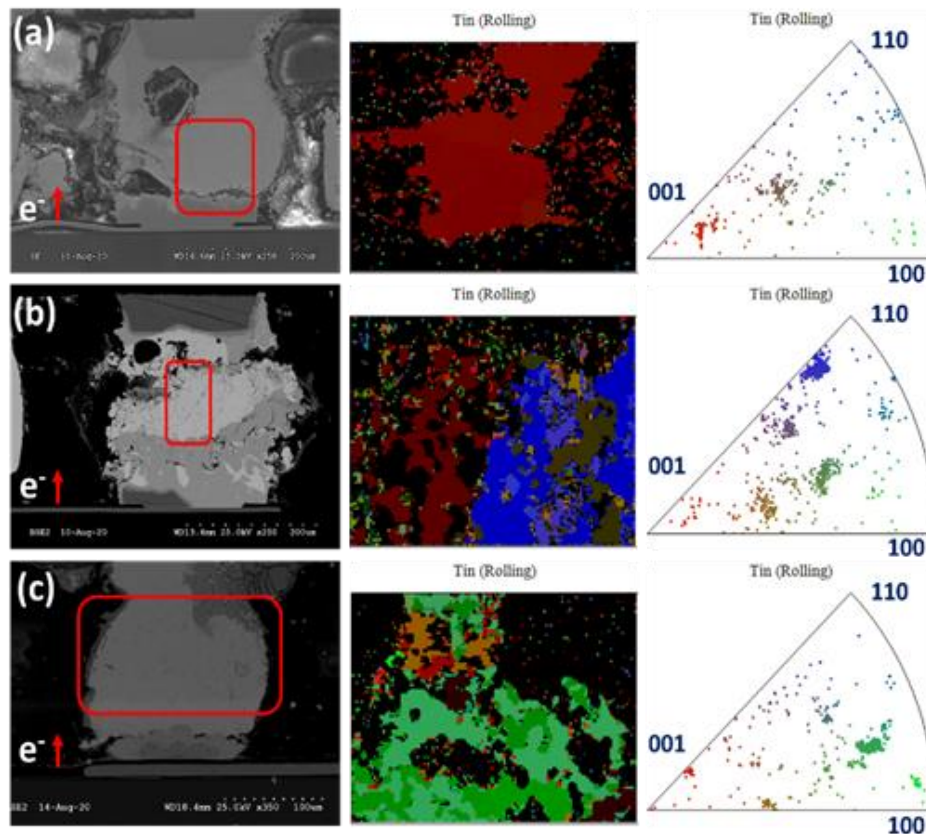

Figure 48 EBSD results obtained by Yi Ram Kim et. al. The EBSD images depict the Sn crystal orientation map, as well as the inverse pole figure in the sample rolling direction. **(a)** is an early-failed sample with a 5% failure rank. **(b)** is a moderately early-failed sample with a 21% failure rank, and **(c)** is a late-failed sample with an 81% failure rank [27].

crowding and compressive stress. Ultimately, EBSD images led to the conclusion that early failures are caused by the c-axis alignment of the Sn grain orientations at the failure site. Since Sn has a BCT structure, its lattice has the constants a=b= 5.83 Å and c=3.18 Å. If the c-axis is aligned with the EM direction, the lattice structure will allow for a larger diffusion path, requiring a lower activation energy compared to the a and b axes. This reduction in activation energy for EM to occur may result in up to a 500X faster diffusion rate. This concludes that the alignment of the c-axis, or [001] grain orientation, with the EM directionality significantly accelerates the EM failure kinetics. The presence of the c-axis alignment at the typical failure site complicates the ability to identify the difference in EM kinetics in different current flow configurations, that is, for early failures. EBSD images obtained to prove this theory were presented by Yi Ram Kim et. al. and can be seen in **Figure 48**.

The EBSD results obtained and presented by Yi Ram Kim et. al. can be used to interpret and identify the location of c-axis alignment, or [001] grain orientation, in the DUT with the EM direction. The red on the tin rolling map indicates the c-axis alignment, and judging by the failure ranking, this confirms the theory that the c-axis alignment is at play in early-failed samples, as presented in **Figure 48 (a)**. **Figure 48 (c)**, however, shows EBSD results of a sample which failed later in the test with an 81% failure rank, which shows very little red in the solder joint. What c-axis grain orientation is present is not enough to drastically accelerate EM failure kinetics. Meanwhile, since the SAC solder bump material has a BCT structure, the c-axis alignment provides a larger diffusion path for EM-diffusion species to pass through. With this ease in atomic diffusion, the Cu is able to diffuse considerably faster in this orientation than in alignments which are perpendicular to the EM direction. Thus, this alignment requires a smaller activation energy, contributing to low-rank failures. Recalling Black's equation, a smaller activation energy leads to

a lower MTTF for samples which have a c-axis alignment. Consequently, the EM failure kinetics are considerably faster, and the reliability of the solder joint is compromised. In fact, the c-axis alignment with the EM path renders EM reliability predictions useless for early failures, as the kinetics are accelerated and wildly unpredictable as failures occur randomly.

Traditional EM testing and failure analysis has not shown to demonstrate a clear difference in the effects of current flow configuration among early-failed samples, or low-rank failure samples. Samples which failed later in the EM tests, however, appear to demonstrate that the symmetrical current flow configuration extends the lifetime of the WCSP DUTs. This extension is much more pronounced in 18μm UBM WCSPs than 50 μm UBM WCSPs. This is clear by the number of failures which occur in the symmetrical current flow configuration data presented in **Figure 44**, after the last data point for the asymmetrical current flow configuration. The fact that the 18μm WCSP's results are more pronounced than 50 μm WCSP's is likely due to the current density distribution along the DUT/UBM interface, where failure is most likely to occur. It may also be due to the dampening of the CTE effect by a thicker UBM. The effect of the UBM thickness will be discussed in the next section; however, to explain the different effects of the current flow configuration, it is worth noting that the extension of MTTF in 50 μm UBM WCSPs is not as obvious as it is in 18 μm UBM WCSPs, and there is an explanation for that.

It is predicted that while it has its limitations, compressive stress benefits the EM reliability of solder joints, and FEM results of stress development with current flow configuration are expected to support this theory.

4.3 Current Flow Configuration Study Model Parameters, Material Properties, and Modeling Procedures

The design of the WCSP sample is purposefully laid out to control the failure mode during EM testing. The packages are constructed and connected to a current source such that one solder joint bears the brunt of the burden from the current flowing through the solder joint. The two support bumps sharing the circuit also have current flowing through them, but considering the current density is lower when it flows through these, they are very unlikely to fail.

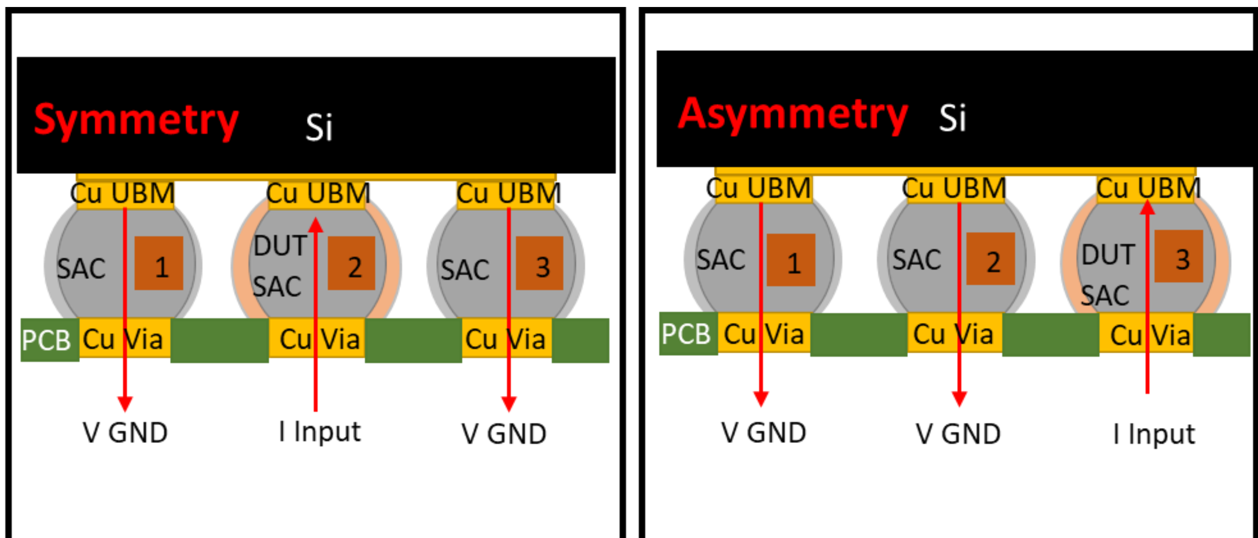

Figure 49 Symmetrical and asymmetrical current flow configurations.

The two current flow configurations studied in this research aim are symmetrical and asymmetrical. The circuit through which the current flows through consists of three solder joints. In the case of the symmetrical current flow configuration, the current would flow through the bottom of the middle solder joint and exit through the top corners of the solder joint so that it may exit through the two neighboring solder joints. In the case of an asymmetrical current flow configuration, the current enters the bottom of the farthest right solder joint in the circuit and exits through one of the top corners leading to the two support bumps. **Figure 49** depicts the two

different current flow configurations under investigation. In the case of the symmetry current flow configuration, solder joint 2 is the DUT, through which the current enters the circuit. Solder joint 1 and 3 are the two support bumps through which the current exits the circuit. In the case of the asymmetrical current flow configuration, solder joint 3 is the DUT solder joint, through which the current enters the circuit. Solder joints 1 and 2 are the two support bumps through which the current exits the circuit. The electrons flow in the opposite direction and are most heavily concentrated in the DUT for each current flow configuration to induce failure solely in the DUT.

Following the CAD parameters laid out in **Table 2**, which was presented in Chapter 3, the submodel is created as a single part in SolidWorks. It is comprised of 18 sections, including a PCB, five Cu vias, five SAC solder bumps, three UBMs, one RDL, two Cu posts, and one Si die. The SolidWorks model is exported as a STEP file, and then imported into ABAQUS/CAE. Upon the importation of the STEP file, the material properties are defined following **Table 3**, which was presented in Chapter 3. The material sections are then generated, and each of the sections is assigned a material section.

Next, in the assembly tab of the model tree, instances were generated, and the mesh was directed to be independent so that the mesh can be done on the instance. Seeds along the edges of the model were defined. Since this submodel is $1/5^{th}$ of the full model, the seeding was defined consistently as 2E-5. A linear thermal-electrical-structural element type was assigned to the mesh and the mesh control was set to a Q3D4 free mesh. After generating all of these, the mesh was then generated on the model. This will result in a number of elements and nodes, which will depend on the size of the model and the mesh size. For instance, for the 18C model with the 18μm UBM under these mesh settings, the meshed model's number of nodes and elements are 124,660 and

679,926, respectively. Models with thicker UBMs would have a larger number of nodes and elements.

To save time in setting the boundary conditions, surfaces and sets were defined. A current density input surface was defined, to which a surface current density load was applied later. Convection surfaces, CONVEC1 through CONVEC7-2 were also defined. The total number of surfaces defined are 9. Sets are also assigned, which are tagged when setting up the boundary conditions. Three sets for the X, Y, and Z constants were defined and assigned to the bottom surfaces of the model (Cu vias and PCB bottom). Next, the voltage ground set was defined and also defined and assigned to the bottom of the Cu vias connected to the circuit, in accordance with the current flow configuration.

Next, two steps were defined. The first step, labeled "Initial" is steady-state, which is useful for establishing the X, Y, and Z constant boundary conditions, which limit the model from rotating or sliding in any direction. These were assigned to the bottom faces of the PCB, and Cu vias of the model. The predefined ambient temperature, 150°C, is also defined in the first step. The second step, labeled "Step 1" is transient, which means it is time-dependent and is useful for solving problems which lack linearity solutions. "Step 1" was set to calculate for 500 seconds. The initial step was set to 0.01, the minimum step size was set to 0.001, and the maximum step size was set to 10. The maximum temperature change allowed per increment was set to 2 degrees.

In "Step 1", the boundary conditions were set. The predefined boundary conditions and the constraints which were defined in the "Initial" step were automatically propagated in "Step 1". Next, the voltage grounds were assigned to the voltage ground set previously assigned and the voltage value was set to zero and instantaneous. The current surface load was then applied to the

surface previously assigned for the current input. Because this model was set to simulate the findings under 4 A current, the current density defined as uniformly 9.63 kA/cm^2 with an instantaneous amplitude, meaning it is constant, which is consistent with direct current conditions. Next, the convection air boundary conditions were set first by assigning the interaction properties, which will be referenced when assigning interactions. This interaction property is the air coefficient, which is set to 250 W/(m^{2}K) based on previously determined information in the previous chapter with the full model, where the JH was maintained at around 10°C and the model is under forced convection. Next, the interactions are assigned as surface film conditions and the sink temperature was set to 150°C.

Output requests were selected. In ABAQUS, two types of outputs are involved: History Output Requests and Field Output Requests. History Output Request selected was energy, and outputs every 1 increment, n, was selected. The Field Output Requests selected include energy, contacts and forces, elastic stress, elastic strain, temperature (nodal and integrational), and current density. The data for the Field Output Requests was collected every 2 increments, n.

Once all boundary conditions, material properties, and mesh are all generated and assigned, a job is created. The job was set to save the data in a documents folder. The number of processors was set to 10. The job was then submitted and allowed to run, which took approximately three hours per simulation.

Post-processing involved obtaining images of each simulation run after isolating the critical regions, the solder bumps. Next, the maximum values of each output of interest were identified: current density in the y-direction (traditionally, the z-direction for most materials science and engineering texts), temperature to obtain the JH in the DUT, compressive stress, von Mises stress,

shear stress, and strain. The integral point for the maximum of each of these outputs were selected, and a plot of each output over time was obtained, then exported to an excel file, which was then arranged, and plotted via KaleidaGraph. The highlights of these findings are discussed next.

4.4 Result and Discussion

As previously discussed, typical EM failure analysis and testing did not reveal a clear difference in solder interconnect reliabilities when subjected to two different current flow configurations for samples which failed earlier in the tests. This is largely owed to the presence of the c-axis alignment of the SAC grain orientations so that it is parallel to the EM direction, thus vastly accelerating EM failure kinetics. That said, FEM will also not likely be applicable for WCSPs which failed early on in EM experiments. However, the FEM results presented in this study can be related to the trends observed in WCSPs which failed later in the test, with failure ranks higher than 25%.

FEM reveals that the DUT undergoes a much more significant amount of current crowding and resultant JH under an asymmetrical current flow configuration that it does under a symmetrical current flow configuration. It is seen that where the current density is the highest, JH is also the highest. The accumulation of current density is current crowding, and this plays a significant role in EM failure kinetics. Where a greater concentration of current density is present, a larger concentration of electrons bombards the diffusing conductive material. This higher concentration of electrons colliding with the EM-diffusing species accelerates the EM failure kinetics. That said, judging by the FEM results, the void nucleates where the current crowding is the highest. In this

case, the void will typically nucleate on the edge of the DUT/UBM interface, where the current crowding is the highest.

Figure 50 features two plots which illustrate the current crowding trend along the interface between the UBM and the DUT SAC solder joint. Under a symmetrical current flow configuration, the current density is highest on either edge of the DUT. Meanwhile, under an asymmetrical current flow configuration, the current density is highest on just one edge of the DUT. That location of current crowding is where the void is most likely to nucleate before it propagates across the SAC/UBM interface.

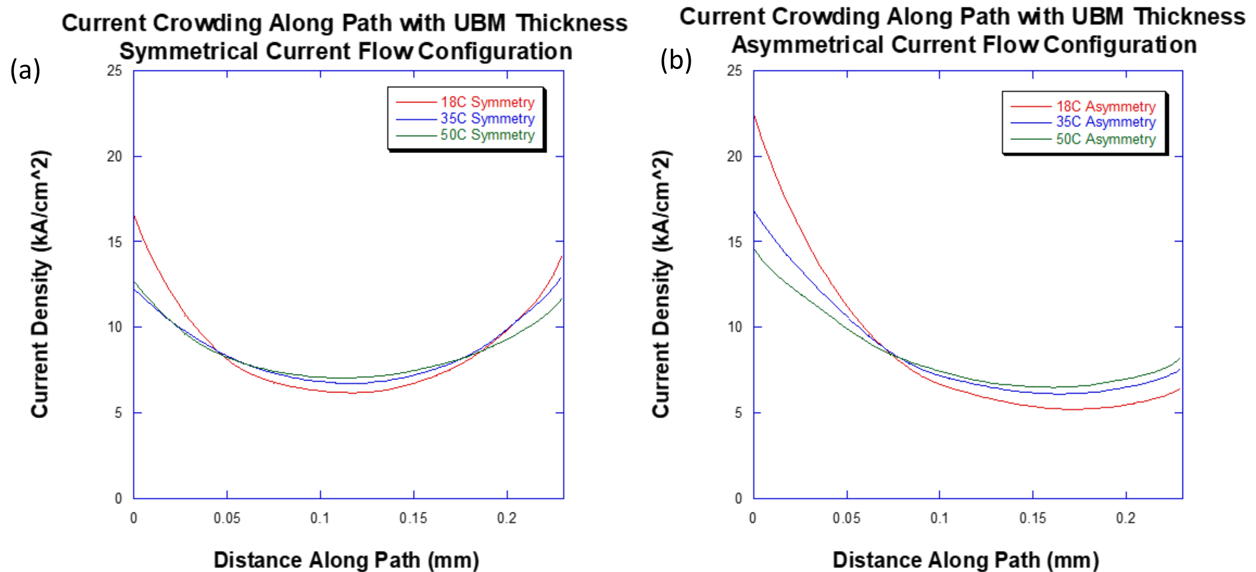

Figure 50 Current density plots across interface with UBM thickness for (a) symmetry and (b) asymmetry current flow configurations.

In asymmetrical current flow configurations, the void will nucleate on one side of the DUT's cathode end, where the current crowding and stress is the highest. It is certain that at this location, the void will initiate. The current density and the JH will be concentrated at the void front once one should nucleate.

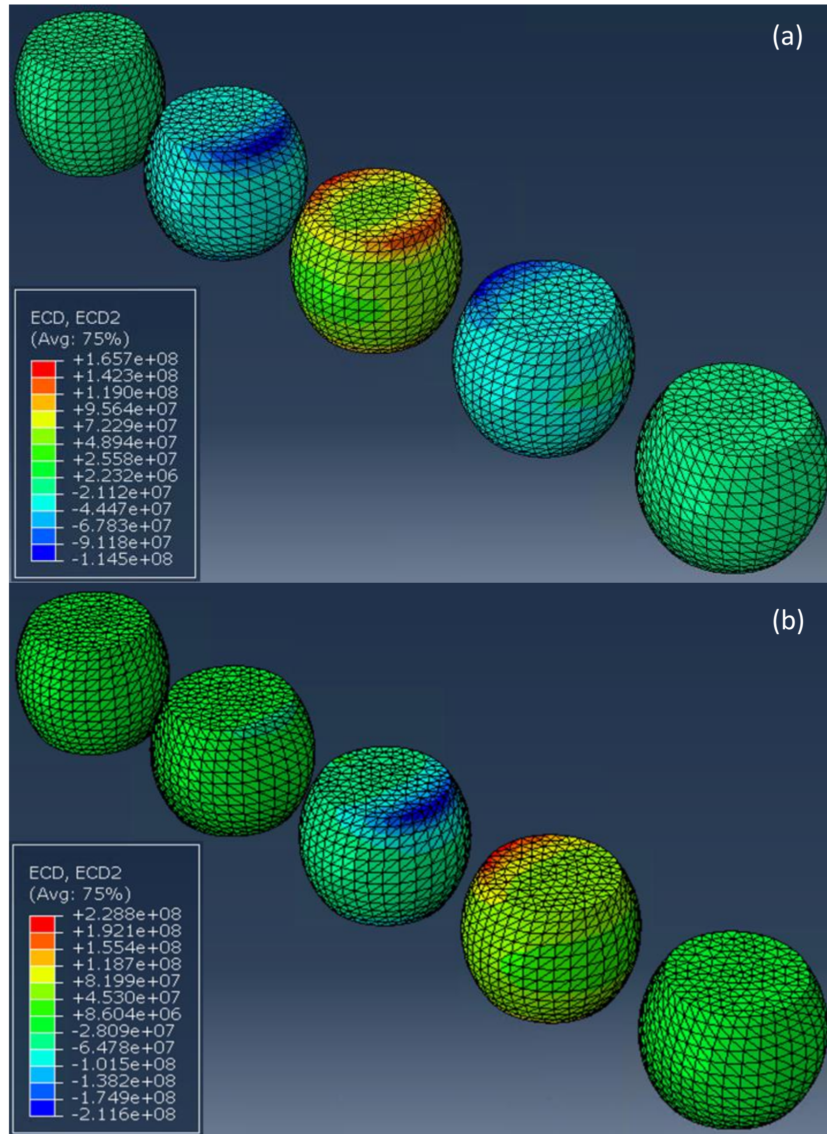

Figure 51 Result portal viewing window in ABAQUS revealing the resultant current density in WCSPs with 18μm-thick UBMs under **(a)** symmetrical and **(b)** asymmetrical current flow configurations.

Figure 51 depicts screenshots obtained from the ABAQUS results viewport of the current density within the solder bumps in WCSP models with 18μm-thick UBMs for **(a)** symmetrical and

(b) asymmetrical current flow configurations. Note that in the symmetrical current flow configuration, the center solder bump is the DUT, and experiences the greatest amount of current density, particularly at the two top edges at the cathode end. The two bumps neighboring the DUT are the support bumps included in the testing circuit. Theoretically, they experience about half of the total current density each than the DUT in the middle does. The two outermost solder bumps on either end of the submodel are not subjected to any current flow. Meanwhile, in the asymmetrical WCSP submodel, the solder bump second from the right experiences the highest among of current density, and therefore expands the most. Second most is the middle solder bump and the third most is the solder bump second from the left. This leaves the two outermost solder bumps which do not experience any current flow.

As EM progresses, vacancy flux overwhelms the atomic flux and vacancies begin to nucleate as conductive material migrates through the SAC solder interconnect by way of vacancy exchange. This vacancy exchange leads to material loss and void nucleation at the SAC solder/UBM interface. As the vacancies accumulate at the cathode end, tensile stress is expected to result, thus leading to an acceleration of void nucleation and propagation. However, compressive stress is present where vacancies are depleted. Compressive stress is resultant of a volume change in the solder material as it expands with the increased temperature while the surrounding materials expand at a lower rate. Particularly, the neighboring solder joints which undergo a lower current density and therefore lower JH act as a constraint against the expanding DUT. Consequently, the JH caused by the current crowding in the DUT may lead to a beneficial side-effect: compressive stress. Compressive stress will be concentrated at the void front, causing a stiff region in the Sn matrix, through which EM is inhibited. The compressive stress can thus be

effective at blocking the void growth as vacancies become depleted, so long as its benefit is not overwhelmed by the current crowding effect.

Based upon the current crowding along the interface between the UBM and the DUT SAC solder bump, the JH follows a similar trend, where it is highest where the current escapes the SAC solder joint in the circuit, however, a thermal gradient caused by the current crowding effect would be much more pronounced in the asymmetrical current flow configuration than in the symmetrical

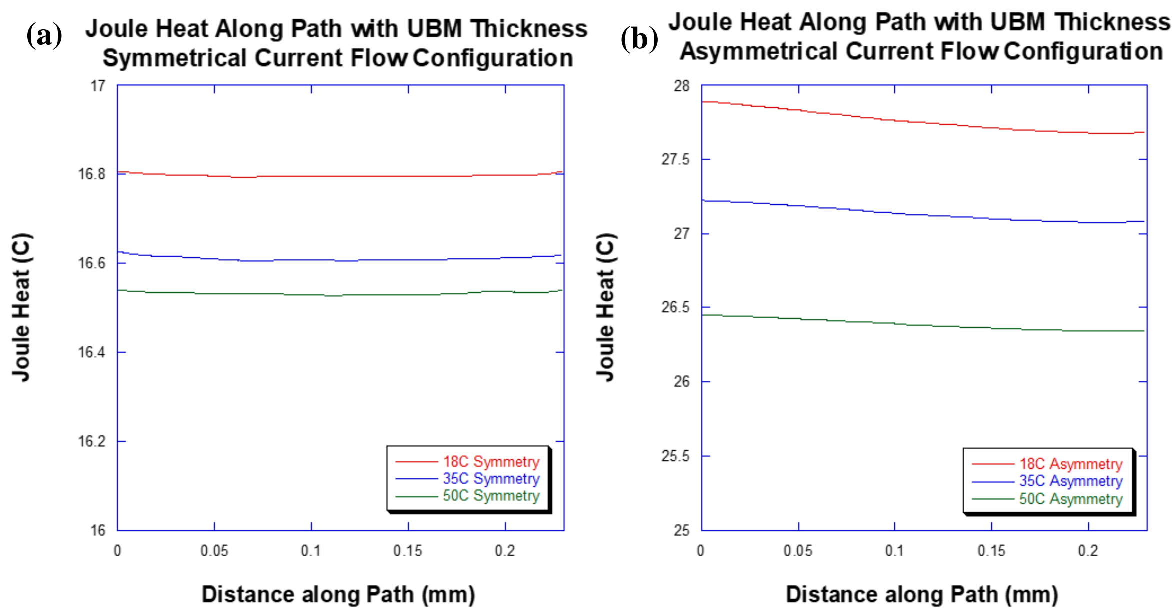

Figure 52 Joule heat plots across interface with UBM thickness for **(a)** symmetry and **(b)** asymmetry current flow configurations.

current flow configuration. The FEM results of the JH distribution along the interface is highlighted in **Figure 52**. The thermal gradient is visible, but minute enough to not make a large difference in the stress distribution. The stress distribution will be most influenced by other constraints. Most notable between the two current flow configurations is the stark difference in the levels of JH between the symmetrical and asymmetrical current flow configurations. As a reminder, the JH may present benefits such as compressive stress, but it may also serve as an adversary to the EM reliability as it accelerates the EM kinetics. **Figure 53** is a screenshot of the

WCSP submodel with 18μm-thick UBMs subjected to **(a)** symmetrical and **(b)** asymmetrical current flow configurations. The JH within the model pretty clearly follows the trend set by the current density.

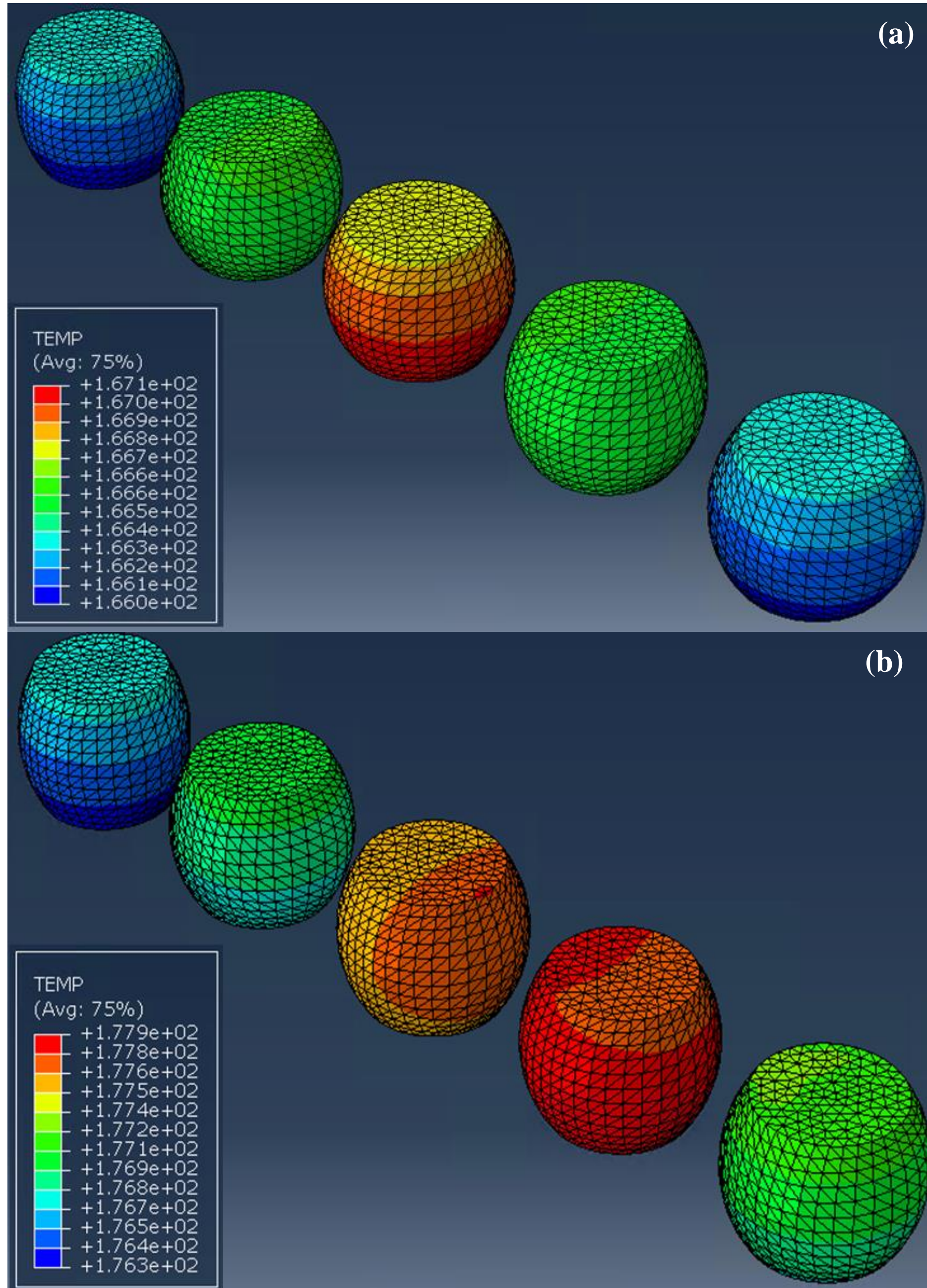

Figure 53 Result portal viewing window in ABAQUS revealing the resultant temperature increase in WCSPs with 18μm-thick UBMs under **(a)** symmetrical and **(b)** asymmetrical current flow configurations. The starting temperature was 150℃, and a much more significant level of JH is observed in the asymmetrical current flow configuration then the symmetrical current flow configuration.

Figure 54 illustrates the compressive stress distribution along the interface between the SAC solder bump interconnect and the UBM. It is much more distributed in the case of the symmetrical current flow configuration but has a higher maximum level of compressive stress is observed in the asymmetrical current flow configuration. The length across the interface is 0.230 mm.

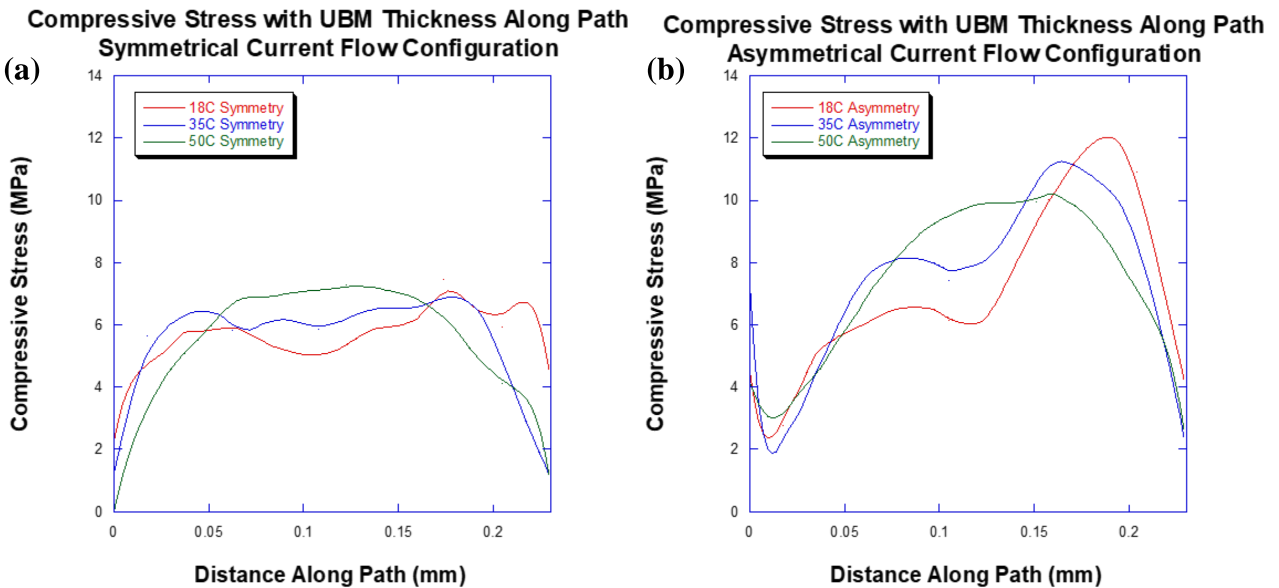

Figure 54 Compressive stress plots across interface with UBM thickness for **(a)** symmetry and **(b)** asymmetry current flow configurations.

Note that the compressive stress is most concentrated within 0.05 mm from the edges where the current density is highest in the WCSP models subjected to a symmetrical current flow configuration. This suggests that the void is probably allowed to nucleate, but once the void would form and propagate to that point within the solder joint, the compressive stress near the current crowding region will block its further growth until current crowding and JH becomes overwhelming enough to overcome. The relatively equal stress on either end of the DUT can be owed to concurrent phenomena: 1) the current crowding leading to JH and expansion in the DUT, 2) the two support bumps included in the testing circuit located on either side of the DUT, and 3)

the two outermost support bumps excluded from the testing circuit. There is one neighboring bump on either side of the DUT, through which the current exits the circuit to the ground. These two neighboring bumps, which are included in the test circuit, each experience about half of the current crowding and JH than the middle DUT bump does, and therefore, they experience less JH, and less expansion. The support bumps consequently act as constraints. Most constraining within the model, however, are the two outmost solder bumps on either end of the submodel, as they do not have any current flowing through them, and thus they have a substantially lower amount of JH, the only level of JH coming from the neighboring bumps which do carry current.

Examining the results obtained in WCSP models subjected to asymmetrical current flow configurations, the stress is not highest near the current crowding region in the DUT, at the interface between the UBM and the SAC solder joint. It is actually higher on the side where the current density is lowest. This can absolutely be owed to the constraint from the neighboring solder bump, which does not have any current flowing through it, and thus acts as the most constraining bump near the DUT in the submodel. In this submodel, the two support bumps included in the testing circuit also act as constraints against the expansion of the DUT, although with less effect than the two bumps which are not subjected to current flow. In fact, the support bump nearest to the DUT, which is subjected to current, expands greater than the solder bump in the circuit which is situated farthest from the DUT. Taking all of this into consideration, between the location of the highest current density and the compressive stress, it can be deduced that the asymmetrical current flow configuration is less effective at blocking void propagation across the interface between the SAC solder bump and the UBM.

Taking the current density, JH, and compressive stress trends into account, the WCSP submodels subjected to the symmetrical current flow configuration follow the trend previously predicted. The void will nucleate on either side of the DUT's cathode end, where the current crowding and stress will be comparably similar. There is almost an equal chance of the void forming on either side of the DUT's cathode end when subjected to the symmetrical current flow configuration due to the split in the current path. In the case of symmetrical current flow configuration, there is a considerably smaller amount of current crowding, JH, and stress in the symmetrical current flow configuration than in the asymmetrical current flow configuration; however, it appears that the compressive stress observed in the symmetrical current flow configuration is more beneficial than that in the asymmetrical current flow configuration. **Figure 55** is a schematic showing the likely location for a void to nucleate in **(a)** symmetrical and **(b)** asymmetrical current flow configurations.

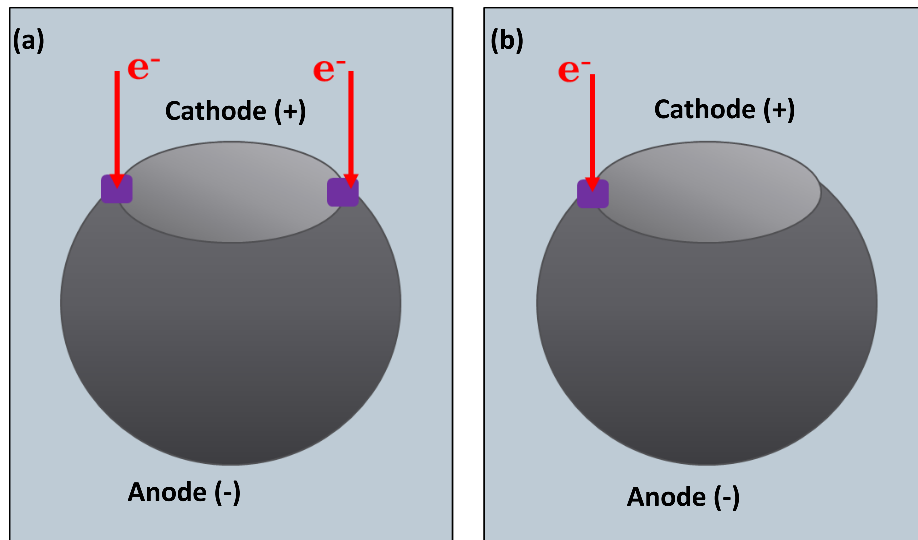

Figure 55 Schematic showing the likely location for a void to nucleate at the cathode end of the DUT, highlighted in purple, where the arrows and red e^- indicate the location of current crowding for **(a)** symmetrical and **(b)** asymmetrical current flow configurations.

The benefits of stress are a welcome relief by reliability engineers and industry; however, if the current crowding is high enough or the stress is insufficient, the benefit from the compressive stress will not be observed. Excessive JH will certainly advance the void growth rate. With high enough current densities, the number of electrons transferring momentum forces to atoms within the BCT lattice of the SAC solder joint will overwhelm the forces from compressive stress, allowing vacancies to form and the void front to advance. The void will propagate along the DUT/UBM interface until a critical void length is reached and runaway failure commences. EM failure is likely to eventually occur, the kinetics of which depending on the level of benefit from the compressive stress on the DUT.

4.6 Conclusion

In conclusion, FEM simulations reveal what was theoretically predicted based on EM test results. When comparing the two current flow configurations, the asymmetrical current flow configuration had significantly higher current crowding, higher JH, and stress than what was observed in symmetrical current flow configurations; however, the locality of the compressive stress combined with the locality of the current crowding shows that the benefit of the compressive stress blocking the void growth is most enjoyed in samples which are subjected to a symmetrical current flow configuration.

It can be predicted that the abovementioned parameters have an effect on the samples which failed later in the test; however, they do not seem to have had an effect on early-failed samples. In fact, early-failed samples, based upon EM results and based upon these findings, appear to fail randomly, owing to the c-axis alignment of the SAC grain orientations at and near the interface between the SAC solder joint and the UBM with the direction of the EM. This can be particularly

detrimental at the point where the current density is the greatest, and thus where the void nucleates and from where the void propagates. It is this grain alignment that has been known to accelerate the EM failure kinetics. Unfortunately, in these cases, no amount of stress can delay the EM failure, as the alignment of the BCT lattice allows the migrating material to travel between atoms quite easily.

While the c-axis alignment phenomenon has been realized in early-failed samples, the stress does, however, appear to affect the samples during later fail times. A clear difference in reliability and stress locality among the two current flow configurations reveals that the symmetrical current flow configuration enjoys the benefits of the compressive stress the most and therefore extends the reliability of the WCSP solder joints well beyond the asymmetrical current flow configuration reliability - by nearly 1500 hours among the last samples to fail in the EM tests. This is valuable from a fundamental standpoint, but not so beneficial from a reliability standpoint, as industry is most interested in when the earliest failures occur. The challenge to thwart premature failure among solder joints remains to prevent the alignment of the grain orientations with the c-axis by inducing anisotropic grain orientations, which is not an easy task to accomplish during the reflow process.

The next challenge is harnessing the benefit of compressive stress through WCSP parameters, which is where Chapters 5 and 7 become relevant.

CHAPTER 5: FUNDAMENTAL EFFECTS OF UNDER BUMP METALLIZATION THICKNESS ON ELECTROMIGRATION RELIABILITY OF WAFER-LEVEL CHIP SCALE PACKAGE SOLDER JOINTS

In this chapter, the effects of the UBM thickness on the current crowding, JH, and stress development and their relationships to the EM failure kinetics observed in comprehensive EM testing of WCSPs will be examined. This research was done in tandem with that which is presented in Chapter 4. We have already identified a benefit of compressive stress, which appears to be thwarted by excessive current crowding, as we have seen in asymmetrical current flow configuration conditions. Now, the research is aimed at understanding how UBM thickness can enhance the benefit of compressive stress and where that benefit becomes limited. The three UBM thicknesses studied include 18 µm, 35 µm, and 50 µm. These were studied under the two current feeding configurations, symmetrical and asymmetrical.

5.1 Background

In this study, the fundamental effects of Cu UBM on EM reliability of WCSPs. Recall that UBMs are commonly deployed in industry as a means to extend the reliability of solder joints by providing a Cu reservoir to be consumed as EM progresses through the interconnects. The UBM is typically deposited so that it lies between the SAC solder joints and the RDL. It thus lies just above the cathode end of the solder joint, where EM effectively forces conductive materials to migrate, leaving vacancies and prompting void nucleation and growth across the DUT. Three UBM thicknesses were examined in the EM testing and so they are also incorporated in FEM WCSP models. The shortest UBM is 18µm-thick. The tallest UBM is 50 µm-thick. As middle ground, a 35 µm-thick UBM is also studied. Prior to EM testing, a general hypothesis was that

there lies a linear relationship between the UBM-thickness and the EM reliability or MTTF. This prediction was based upon the likely dampening effect on the CTE and improved current distribution, therefore lower JH, along the interface between the UBM and the SAC solder joint.

Contrary to early predictions, EM reliability tests of WCSPs with varying UBM thicknesses revealed that no such linear relationship exists among these samples. The results go one to suggest that in addition to EM failure mechanisms, mechanical mechanisms also appear to play a significant role in EM failure.

It is thereby suggested that a competition between two factors impacting the EM kinetics: 1) the Cu supply to satisfy EM mechanisms and 2) the compressive stress on the DUT which may block the propagation of an EM void across the DUT/UBM interface. These two competing factors reveal that there is an optimal UBM thickness among those subjected to EM testing. A balance between the Cu supply and the compressive stress must be met if reliability engineers seek to optimize the benefit of UBM thicknesses in electronic packages.

The level of stress, JH, and current crowding are compared among the UBM thicknesses and with EM experimental results. FEM will allow the identification of a link between the stress generation and the MTTF with respect to the UBM thickness. The significance of this research is not only interesting fundamentally, but it also has potential expansion and applicability to industry. Identifying the relationship between the EM reliability and the mechanical and physical trends observed in FEM may lead to improved methodology for enhancing devices. Some of the improved methodology includes saving time and cost on sample preparation by narrowing down testing matrixes or making intuitive decisions on design and materials selection based on FEM findings.

5.2 EM Performance of WCSPs with Varying UBM Thicknesses

The general hypothesis before EM testing was that an increase in the UBM thickness would extend the lifetime of the solder joint in a linear fashion, followed by a saturation of this benefit at a critical UBM thickness. However, experimental data suggests that there is an inflection point where an optimal thickness of a UBM can be determined for the extension of EM reliability.

There appears to be an optimal thickness of UBM, as reported by Kim et. al. in **Figure 56**, where the 35 µm UBM samples outlive both 50 µm and 18µm UBM samples [1]. The plot featured in **Figure 56** shows that WCSPs with 18µm-thick UBMs have MTTFs of just over 600 hours. The WCSP samples with 50 µm-thick UBMs, which are considerably thicker, have MTTFs of around 450 hours. Finally, the WCSP samples which incorporated 35 µm-thick UBMs have a MTTF of around 850 hours – a significant improvement from the 18µm-thick UBMs and more than the 50 µm-thick UBMs. The trend observed in this MTTF plot supports the conclusion that of the three UBMs, the 35 µm-thick UBM is the most optimal for extending the reliability of WCSPs against EM failure. This begs the question: why? The answer to that is that there are likely other mechanical mechanisms playing a role in addition to classical EM voiding.

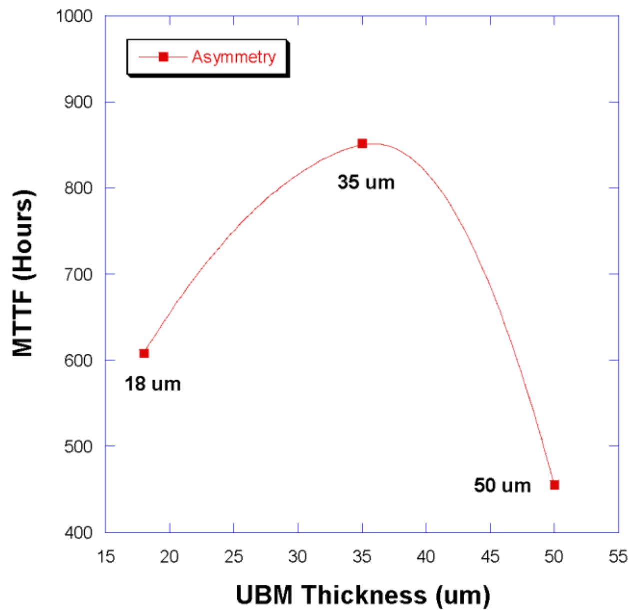

Figure 56 Graph of different UBM thicknesses' mean-time-to-failure (MTTF) [1].

To further understand the EM failure mechanisms occurring in the solder joint as a result of an added Cu reservoir, cross-sectional BSE images were obtained and presented in literature by Yi Ram Kim et. al. **Figure 57** depicts four images obtained using an SEM in BSE mode. **Figure 57 (a)** presents cross-sectional images of WCSP DUTs with 18μm-thick UBM reservoirs. It

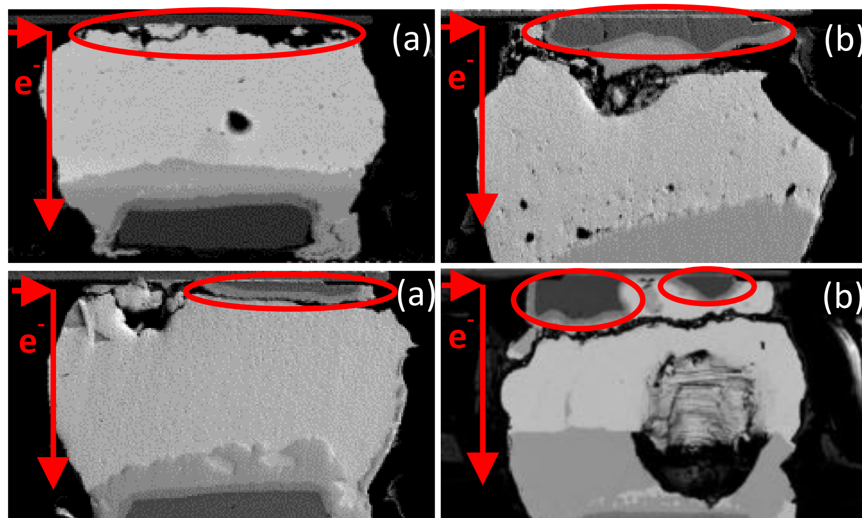

Figure 57 Cross-sectional BSE images obtained via SEM of WCSPs with **(a)** 18 um and **(b)** 50 um-thick UBMs presented by Yi Ram Kim et. al. [1].

appears that the solder joint failed by classical EM mechanisms as a void is present along the interface between the SAC solder joint and the UBM. Most notable, is that the 18µm-thick UBM is almost completely consumed. **Figure 57 (b)** presents cross-sectional images of WCSP DUTs with 50 µm-thick UBM reservoirs. Similar to the 18µm UBM samples, the solder joints appear to have failed by classical EM failure kinetics as the void has completely propagated across the interface between the UBM. The notable difference, though, is that a significant amount of the Cu material remains in the 50 µm Cu reservoir. Comparing these images to the MTTF plot in **Figure 56**, there is an unknown mechanism occurring in the background, which is impacting the EM reliability. This makes 18C and 50C samples particularly interesting.

As discussed earlier, the WCSP test circuit is comprised of three solder bumps. One solder bump, the DUT, is subjected to a higher amount of current density than the two support bumps in the circuit, through which the current escapes the circuit to the ground. While all three are experiencing current flow and thus JH, one solder bump is going to expand farther than the others with the increase in temperature. The two support solder bumps in the circuit act as constraints, as they are not expanding as far as the DUT. Theoretically, the DUT should thus be under compression and the two support bumps should be under tension, and BSE images obtained by Yi Ram et. al. prove this theory to be true.

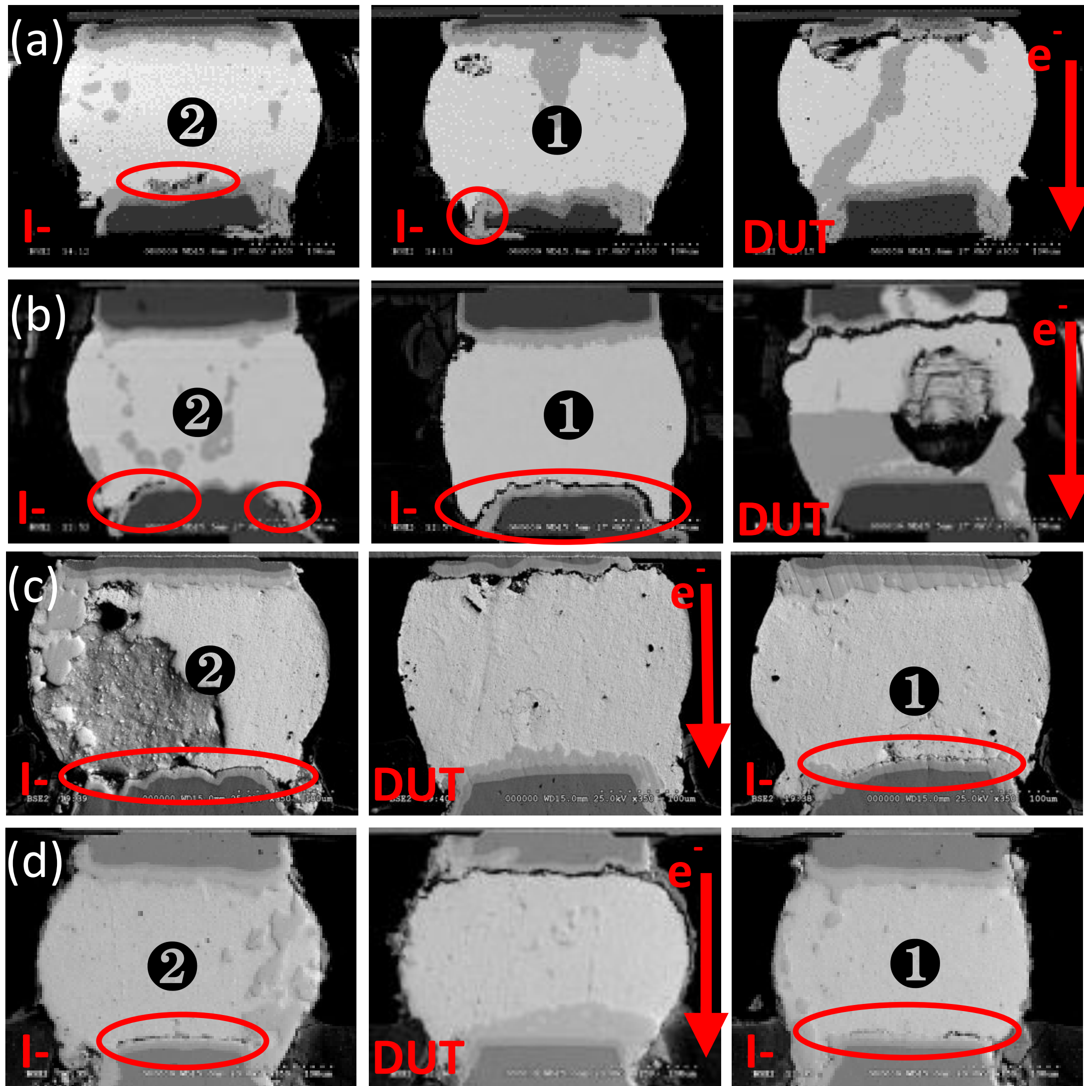

Figure 58 Cross-sectional BSE images obtained via SEM of WCSPs **with (a)** 18 µm-thick UBMs tested under an asymmetrical current flow configuration **(b)** 50 µm-thick UBMs tested under an asymmetrical current flow configuration, **(c)** 18 µm-thick UBMs tested under a symmetrical current flow configuration, and **(d)** 50 µm-thick UBMs tested under a symmetrical current flow configuration. [1].

Figure 58 contains a series of SEM images obtained in BSE mode. **Figure 58 (a)** and **(c)** are representative cross-sectional images of solder bumps incorporated in WCSP samples with 18µm-thick UBMs which failed under asymmetrical and symmetrical current flow configurations, respectively. **Figure 58 (b)** and **(d)** are representative cross-sectional images of solder bumps incorporated in WCSP samples with 50 µm-thick UBMs which failed under asymmetrical and

symmetrical current flow configurations, respectively. In every case, the DUT has a void which has propagated across the DUT, along the interface between the DUT SAC solder joint and Cu UBM interface. Meanwhile, a tell-tale sign of tensile stress can be seen at the bottom cathodic ends of the support bumps denoted as 1 and 2 – a crack from the delamination of the support bumps from the Cu pad or lead frame. The cracks are pointed out by the red circles.

We now have proof that mechanical stress plays a role throughout the EM process. In thin films, it has been identified in regions where vacancies are depleted during EM. In larger interconnects, like those used in flip-chip packages, compressive stress is known to occur due to the high level of JH and thus temperature change in the DUT caused by a high current density. It is known that stress-related degradation of solder joints under high current densities occurs, and thus compressive stress is known to have consequences. For example, should the presence of compressive stress be relieved, the tensile stress leads to void propagation across the solder joint. Additionally, morphological evolutions in the formation of hillocks and whiskers at the anode follow the release of compressive stress [**28**]. However, the solder joint may enjoy the presence of active compressive stress at the cathode, particularly near the location where vacancies and eventual voids are formed by EM. The compressive stress may prove to benefit the EM reliability as the mechanical stiffness concentrated at or near the void front assists in blocking void growth, working against the classical EM mechanism. We can hypothesize that compressive stress can benefit the EM failure reliability.

5.3 Under Bump Metallization Study Model Parameters, Material Properties, and Modeling Procedures

This study was actually done in concurrence with Chapter 4, so all three UBMs were studied under both symmetrical and asymmetrical current flow configurations. Thus, the same procedures were followed.

The submodel is created as a single part in SolidWorks according to the CAD parameters laid out in **Table 2** presented in Chapter 3. It is comprised of 18 sections, including a PCB, five Cu vias, five SAC solder bumps, three UBMs, one RDL, two Cu posts, and one Si die. The SolidWorks model is exported as a STEP file, and then imported into ABAQUS/CAE. After the STEP file is imported, the material properties are defined according to **Table 3**, also presented in Chapter 3. The material sections are generated, and each of the sections is assigned a material section.

In the assembly tab of the model tree, instances were generated, and the mesh was directed to be independent so that the mesh can be done on the instance. The seed sizes for the mesh were defined along the edges of the model as 2E-5, a linear thermal-electrical-structural element type was assigned to the mesh, and the mesh control was set to a Q3D4 free mesh. With the completed mesh, each model had over 100,000 nodes and over 600,000 elements.

A current density input surface for the current density load was defined. Then convection surfaces, CONVEC1 through CONVEC7-2 were also defined. Three sets are defined for the X, Y, and Z constants and assigned to the bottom surfaces of the model (Cu vias and PCB bottom). The voltage ground set was then defined and assigned to the bottom of the Cu vias connected to the circuit, in accordance with the current flow configuration.

Two steps were defined next. The first step, labeled "Initial" is steady-state, which is useful for establishing the X, Y, and Z constant boundary conditions, which limit the model from rotating or sliding in any direction. These were assigned to the bottom faces of the PCB, and Cu vias of the model. The predefined ambient temperature is also defined in the first step, which was set to 150°C for this step. The second step, labeled "Step 1" is transient, which means it is time-dependent and is useful for solving problems which lack linearity solutions. "Step 1" was set to calculate for 500 seconds. The initial step was set to 0.01, the minimum step size was set to 0.001, and the maximum step size was set to 10. The maximum temperature change allowed per increment was set to 2 degrees.

In the "Step 1", the boundary conditions were set. The predefined boundary conditions and the constraints which were defined in the "Initial" step were automatically propagated in "Step 1". Next, the voltage grounds were assigned to the voltage ground set previously assigned and the voltage value was set to zero and instantaneous. The current surface load was then applied to the surface previously assigned for the current input. Because this model was set to simulate the findings under 4 A current, the current density defined as uniformly 9.63 kA/cm^2 with an instantaneous amplitude, meaning it is constant, which is consistent with direct current conditions. Next, the convection air boundary conditions were set first by assigning the interaction properties, which will be referenced when assigning interactions. This interaction property is the air coefficient, which is set to 250 W/(m^{2}K) based on previously determined information in the previous chapter with the full model, where the JH was maintained at around 10°C and the model is under forced convection. Next, the interactions are assigned as surface film conditions and the sink temperature was set to 150°C.

History Output Request selected was energy, and outputs every 1 increment, n, was selected. The Field Output Requests selected include energy, contacts and forces, elastic stress, elastic strain, temperature (nodal and integrational), and current density. The data for the Field Output Requests was collected every 2 increments, n.

Once all boundary conditions, material properties, and mesh are all generated and assigned, a job is created. The job was set to save the data in a documents folder, 10 processors were selected, and then the job was submitted and allowed to run, which took approximately three hours per simulation.

Post-processing involved obtaining images of each simulation run. Next, the maximum values of each output of interest were identified: current density in the y-direction (traditionally, the z-direction for most materials science and engineering texts), temperature to obtain the JH in the DUT, compressive stress, von Mises stress, shear stress, and strain. The integral point for the maximum of each of these outputs were selected, and a plot of each output over time was obtained, then exported to an excel file, which was then arranged, and plotted via KaleidaGraph. The highlights of these findings are discussed next.

5.4 Result and Discussion

The hypothesis deduced from the EM performance of WCSPs with varying UBM thicknesses was that compressive stress is playing a role in the EM failure kinetics in addition to the Cu UBM reserve material. It is believed that a sufficient level of compressive stress may block the propagation of an EM void across the DUT, thereby prolonging runaway EM failure. Meanwhile, the current crowding in the solder joint interconnect accelerates EM failure kinetics. These two counteracting phenomena occur in tandem, and two mechanisms dictating the EM

failure kinetics are competing with one another: 1) Cu UBM supply providing more Cu and prolonging EM void nucleation and 2) compressive stress blocking void growth once it nucleates.

Thicker UBMs were expected to yield a wider distribution of current density across the cathode end of the DUT solder joint, resulting in a decrease in current crowding, which is true. This can be credited to the fact that the current does not adjust to exit the solder bump, as the 50 μm UBM provides more current path before the current path turns and exits the circuit. Furthermore, the thicker UBM also provides a dampening effect, as the Cu UBM:SAC ratio is increased, offsetting the CTE mismatch effect. However, thicker UBMs would result in higher amounts of JH due to an increase in resistance with an increase in conductive material. Theoretically, the decrease in current crowding along with the added dampening effect of the thicker UBM are expected to result in a smaller amount of compressive stress at the cathode end of the solder joint.

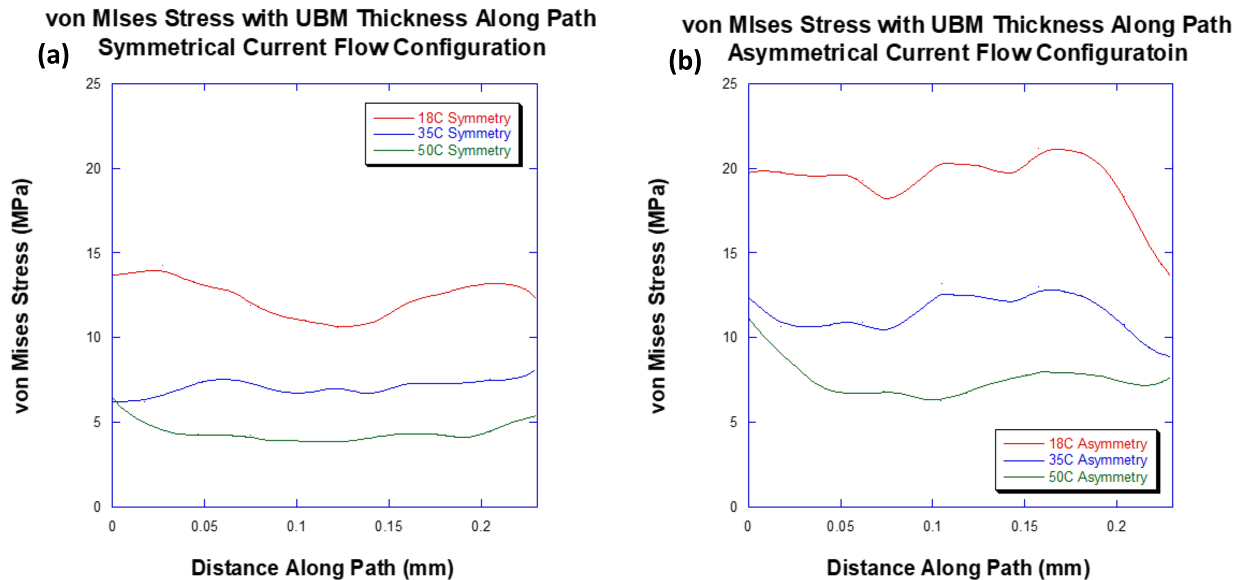

Figure 59 von Mises stress plots across interface with UBM thickness for **(a)** symmetry and **(b)** asymmetry current flow configurations.

Recalling **Figures 50, 52,** and **54** from Chapter 4 shown below, the current density, JH, and compressive stress along the path is impacted by the UBM thickness. We see in all cases that as the UBM thickness increases, the current crowding, JH, and von Mises stress are all dampened. The von Mises stress, shown in **Figure 59**, a component of stress which accounts for the principal stress and shear stress is very clearly dampened, and it appears that the 35 µm UBM provides a good balance between the two other UBM thickness samples. Most intriguing, though, is that the DUT in the 35 µm UBM WCSP samples actually experiences a greater amount of compressive stress than the 18µm UBM in different areas along the SAC solder bump/Cu UBM interface. Overall, though, the UBM thickness also dampened the maximum compressive stress.

Taking a closer look at **Figure 50**, we see that the current is highly concentrated on both corners at the top of the DUT under a symmetrical current flow configuration and only in the top left corner of the DUT under an asymmetrical current flow configuration. In the case of the symmetrical current flow configuration, we observe that the maximum current density along the

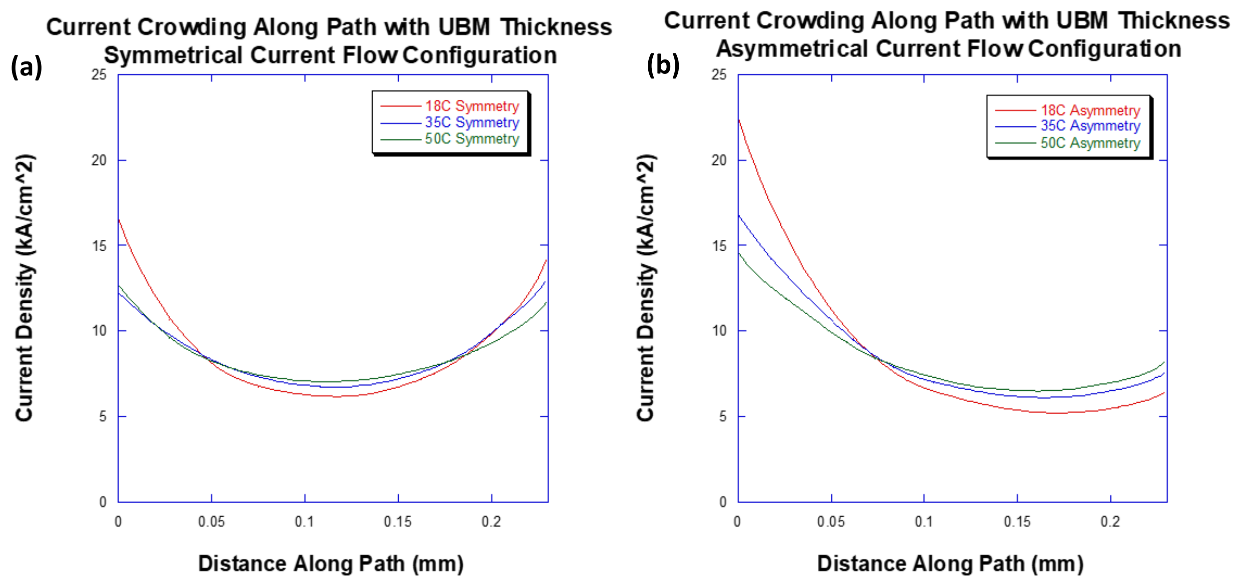

Figure 50 Current density plots across interface with UBM thickness for **(a)** symmetry and **(b)** asymmetry current flow configurations.

interface between the SAC solder joint and the Cu UBM in the 18 μm, 35 μm, and 50 μm UBM WCSP samples is 16.6, 12.9, and 12.7 kA/cm^2, respectively. Under an asymmetrical current flow configuration, we observe that the maximum current density along the interface between the SAC solder joint and the Cu UBM in the 18 μm, 35 μm, and 50 μm UBM WCSP samples is 22.4, 16.8, and 14.6 kA/cm^2, respectively.

Examining **Figure 52**, we see that the locations of the highest levels of JH follow a similar trend to the current density among the two different current flow configurations. Under a symmetrical current flow configuration, we observe that the maximum JH along the interface between the SAC solder joint and the Cu UBM in the 18 μm, 35 μm, and 50 μm UBM WCSP samples is 16.8, 16.6, and 16.5°C, respectively. Under an asymmetrical current flow configuration, we observe that the maximum JH along the interface between the SAC solder joint and the Cu UBM in the 18μm, 35 μm, and 50 μm UBM WCSP samples is 27.9, 27.2, and 26.5 °C, respectively.

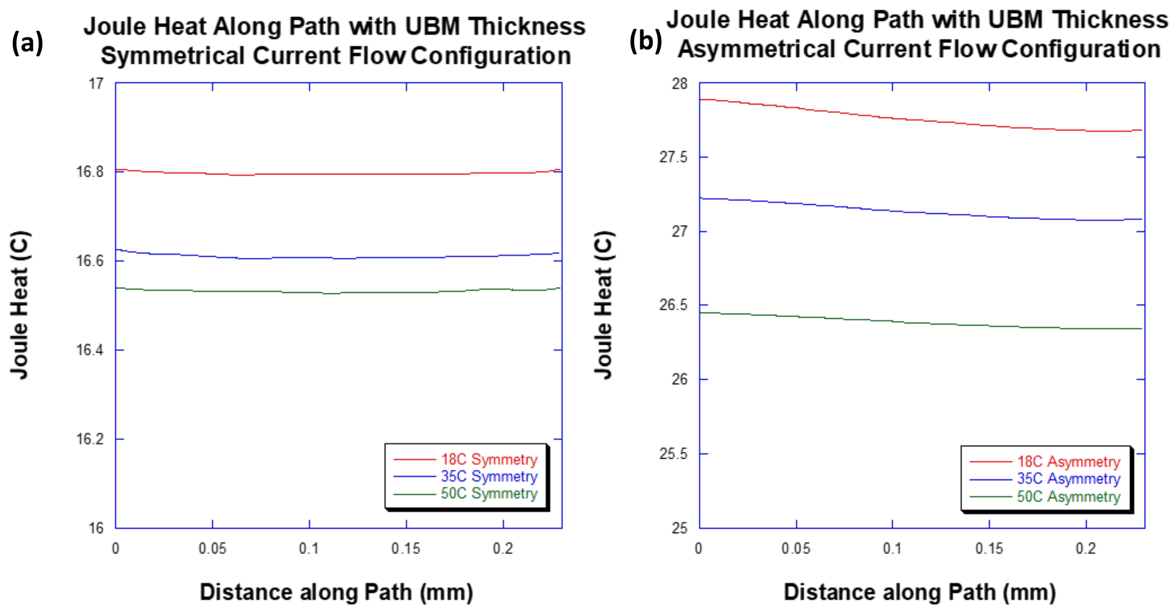

Figure 52 Joule heat plots across interface with UBM thickness for **(a)** symmetry and **(b)** asymmetry current flow configurations.

Of course, this level of JH is exaggerated compared to how it would be in a full model; however, the key takeaway is the general trend in how the UBM impacts the JH.

Further confirming the findings along the interface between the SAC solder joint/UBM interface for each WCSP model type, a maximum value of the current density and JH reached was also recorded and compared among the three UBM thickness variables. **Figure 52** includes plots comparing **(a)** current crowding and **(b)** JH among the WCSP models with the variable UBM thicknesses. It is clear, at least in the case of the current crowding, that the UBM dampens the current density at the interface. Under symmetrical current flow configurations, the difference between the current crowding in the WCSP model with a 35 µm-thick UBMs and the 50 µm-thick UBMs is very minimal compared to the former with 18µm-thick UBMs. In the case of asymmetrical current flow, the UBMs the difference is significant between the three UBM thicknesses. The current crowding trend does not share a linear relationship with the UBM thickness, which may relate to the nonlinear relationship observed in MTTF.

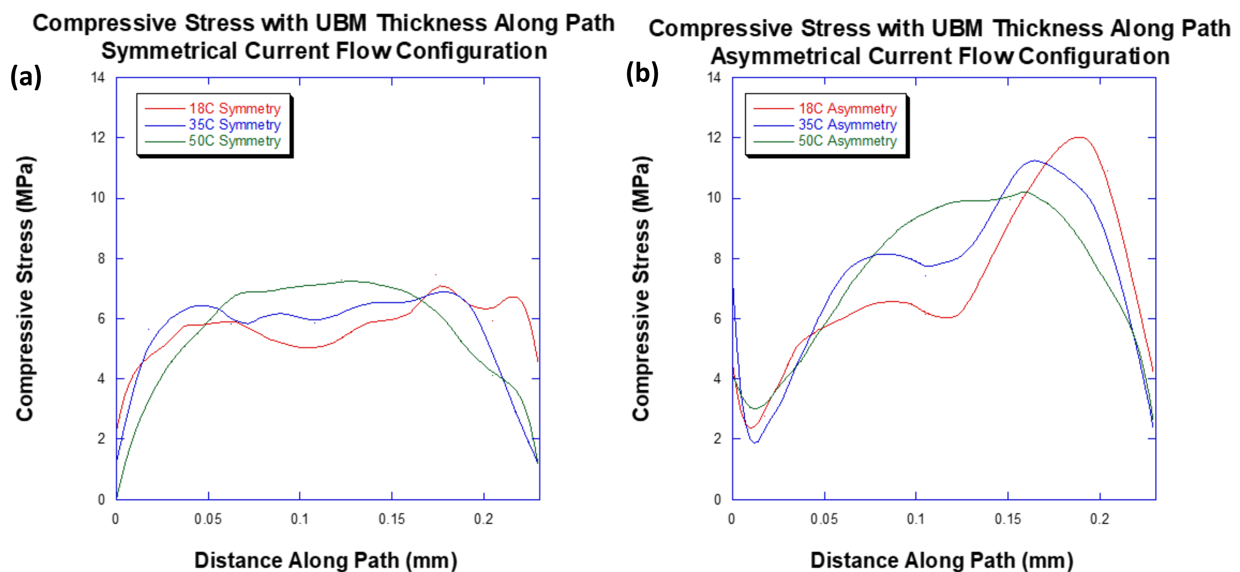

Figure 54 Compressive stress plots across interface with UBM thickness for **(a)** symmetry and **(b)** asymmetry current flow configurations.

Finally, examining the plots in **Figure 54**, we observe that the maximum compressive stress values and their locations varies. Under both current flow configurations, we see a strikingly dampened level of compressive stress at the edges where the current density is the highest in WCSP models with 50 µm-thick UBMs compared to the WCSP models with 35 µm and 18 µm. Imagine the DUT solder bump as it is subjected to current flow. Where the current is most concentrated, the electrons are bombarding the conductive atoms, driving their migration, and leaving behind vacancies. This would be occurring at either top corner in DUTs subjected to a symmetrical current flow configuration and the top left corner in DUTs subjected to an asymmetrical current flow configuration.

Let us consider the condition of the DUTs under symmetrical current flow configuration. At one of the very edges of the DUT/UBM interface, a void may form eventually. It may form sooner in the 18 µm WCSP samples simply due to the limited Cu supplied by the UBM, but later in the 50 µm WCSP samples because there is an ample Cu supply provided by the UBM. The void in the 18µm WCSP sample will not likely form until a considerable amount of the Cu UBM is consumed. The void may form sooner in the 18µm WCSP sample but based upon the location of the maximum stress under symmetrical current flow configurations, that void will be stalled by the compressive stress which develops within 50 µm of the solder bump edge. The compressive stress which becomes concentrated at the void front blocks its continued propagation, that is, until it is eventually relieved possibly due to deformation or diffusion at the interface as the conductive atoms eventually falter to the high current density and JH. Meanwhile, the void may form later in the 50 µm WCSP sample because of the excessive Cu reservoir supplied by the UBM. But because of the low level of compressive stress in the DUT with a 50 µm UBM compared to other UBM thicknesses, as shown by FEM, the Cu does not need to be fully consumed or mostly consumed

before a void eventually forms. Based upon the location of the maximum compressive stress, which is considerably far away from the edge where the current crowding is the highest, that void is allowed to grow almost unhindered until it reaches a critical length and runaway failure commences.

Now, let us consider the condition of the DUTs under an asymmetrical current flow configuration. At the top left edge of the DUT/UBM interface, a void may form eventually. Similar to the symmetrical current flow configuration, a void may form sooner in the 18μm WCSP samples because of the limited Cu supply. Also like the symmetrical current flow configuration, the void may form later in the 50 μm WCSP samples because it has a greater Cu supply. Similar to the behavior under symmetrical current flow configurations, the void in the 18 μm WCSP sample will not likely form until a considerable amount of the Cu UBM is consumed. Although the graph clearly shows that the highest level of compressive stress is closer to the far edge of the DUT, away from the current crowding region. Despite this, the asymmetrical current flow configuration will have a higher amount of stress at the void front in the 18μm than in the 50 μm WCSP samples. So even if a void may form sooner in the 18μm WCSP sample, the stress will still work to block the void growth, though not as effectively as it would in the case of symmetrical current flow configurations as the current density is still considerably high. This further supports the findings observed in the symmetry vs. asymmetry study, where late-failed samples tested under the symmetrical current flow configuration had longer MTTFs than those tested under the asymmetrical current flow configuration. sample but based upon the location of the maximum. Similar to what may be occurring under symmetrical current flow configurations, the WCSPs with 50 μm UBM will have a void nucleate later due to the Cu supply. However, because of the high

current crowding compared to the symmetrical current flow configuration and mostly because of the considerably lower compressive stress, the stress is not sufficient to delay the void propagation across the interface.

Figure 60 **(a)** and **(b)** are plots of the maximum current crowding and JH with UBM thickness also comparing for symmetrical and asymmetrical current flow configurations, respectively. In all cases, the current density decreases in a nonlinear fashion, but in the case of symmetrical current flow configurations, the 35C UBM's current crowding is very similar to that observed in 50C UBMs. Both have a considerable improvement in the current density from that observed in 18C UBMs. In all cases, JH decreases, as well, but not by much. This could possibly be credited to the increase in resistance along the circuit a longer path as the UBM increases in thickness.

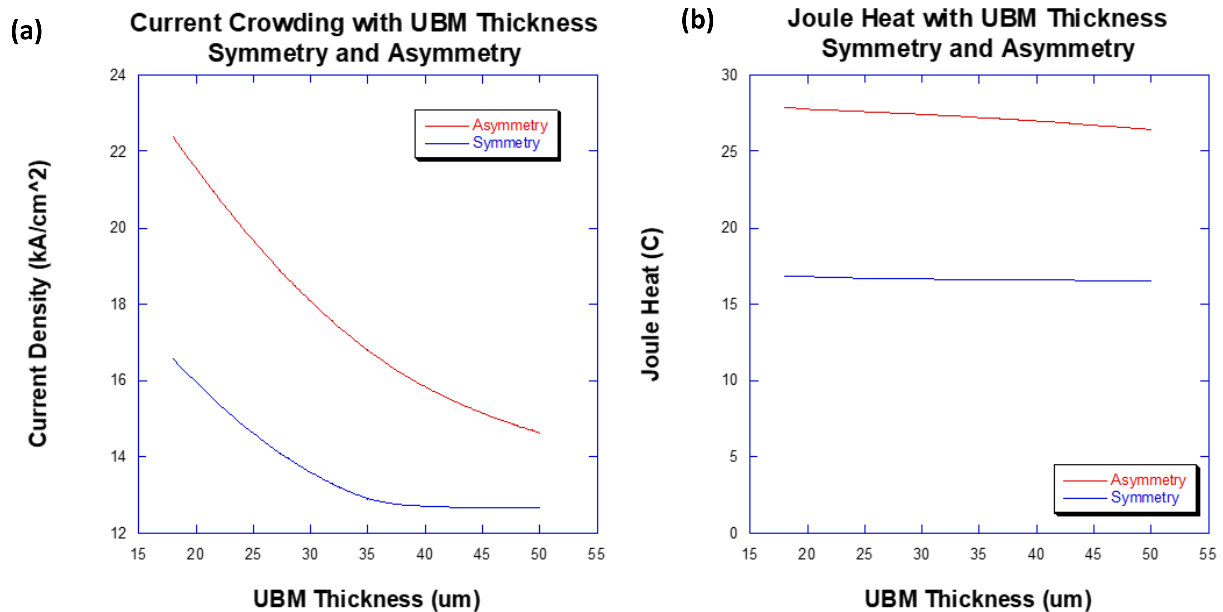

Figure 60 Plots of **(a)** current crowding with UBM thickness and **(b)** Joule Heat with UBM thickness for symmetry and asymmetry current flow configurations.

In both current flow configurations, the compressive stress in the DUTs of WCSPs with 35 μm-thick UBMs follows a similar trend as those with 18 μm-thick UBMs, but it actually exceeds the level of compressive stress achieved in the 18μm-thick UBM samples in critical areas along the interface. Judging by the drastic improvement in MTTF and the higher compressive stress than 18 μm-thick UBM samples observed in DUTSs in WCSPs with 35 μm-thick UBMs, it seems that a "balance" might not be what was achieved; rather, a stark improvement. It seems that the 35 μm UBM not only seems to provide a good balance between the Cu supply and stress – it exceeds in both areas.

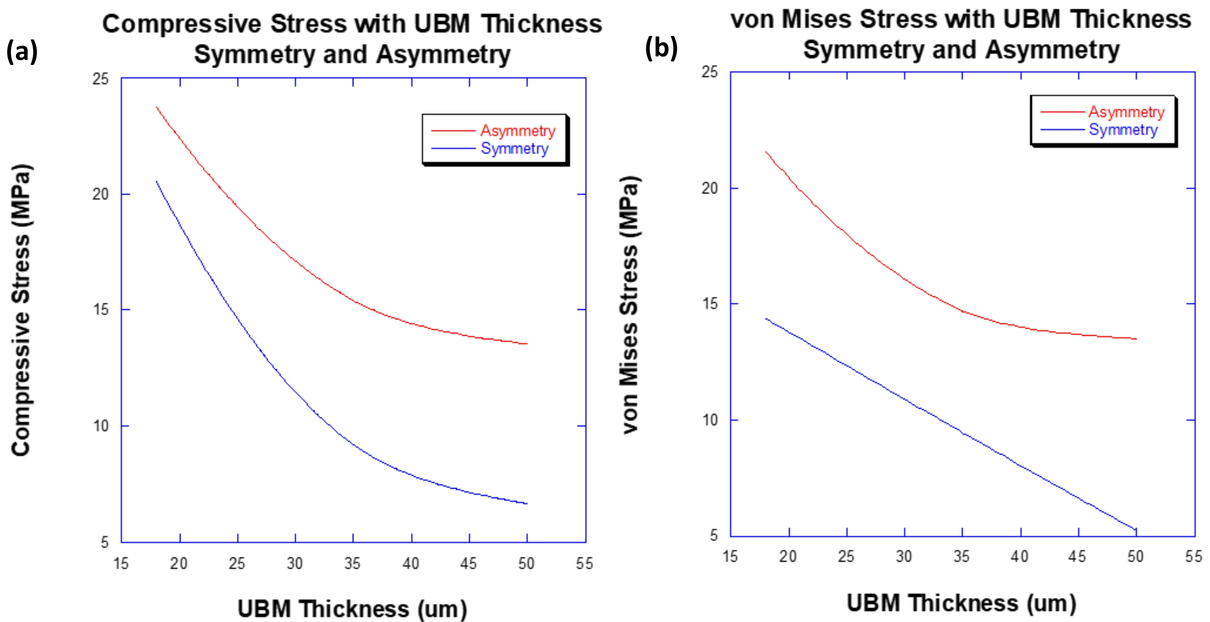

Figure 61 Plots of **(a)** compressive stress with UBM thickness and **(b)** von Mises stress with UBM thickness for symmetry and asymmetry current flow configurations.

Figure 61 includes plots of **(a)** the maximum compressive stress with UBM thickness and **(b)** the maximum von Mises stress with UBM thickness for symmetrical and asymmetrical current flow configurations. The two plots further confirm the findings supporting that thicker UBMs dampen the compressive stress and von Mises stress. The trend observed in compressive stress

with UBM thickness is nonlinear for both symmetrical and asymmetrical current flow configurations. However, the trend observed in von Mises stress with UBM thickness is nonlinear for asymmetrical current flow configurations, likely owing to the considerably higher level of JH and thus CTE mismatch effects. Meanwhile, the trend resembles a linear relationship between the UBM thickness and the maximum von Mises stress in symmetrical current flow configurations. This likely owes to the two support bumps on either side of the DUT acting as constraints affecting the level and distribution of von Mises stress along the DUT interface.

In summary, the UBM thickness does appear to have a dampening effect on the stress, as predicted, due in part to the aspect ratio of the SAC/UBM material and to the current density distribution in the DUT and along the SAC/UBM interface. Larger UBMs appear to dampen the effects of the CTE mismatch, and therefore stress, as indicated on the edges of the solder bump along the SAC/UBM interface, where current crowding regions are most prevalent. There is also a lower amount of stress overall as well as JH in the current crowding regions with thicker UBMs. This trend in the dampening effect is especially obvious in the symmetrical current flow configuration, as we can see by the distribution of the stress along the interface. This improved distribution likely contribute to the improved EM reliability in later-failed samples tested under symmetrical current flow configurations as we saw in Chapter 3. As mentioned before, however, there is a limit to the benefits of the stress or current crowding limitation as there has to be a balance between current crowding, Cu supply, and compressive stress in the package's ICs. EM and FEM results suggest that of the three UBM parameters tested, the optimal UBM thickness is 35 μm, because it supplies more Cu while the dampening effect is not as high as that observed in the DUT with a UBM that is 50 μm thick.

5.6 Void Growth Effects on Stress

In this section, the effects of the void growth across the interface between the UBM and the SAC solder joint are presented. The WCSP models of each UBM thickness were modified so to track the current density, JH, and stress are tracked as a void grows. Four void sizes are investigated for each UBM thickness and under both symmetrical and asymmetrical current flow configurations. The artificial voids are 10 µm-thick, with lengths of 0.04 mm, 0.05 mm, 0.06 mm, and 0.08 mm. This constitutes areas of 0.0062 mm^2, 0.0082 mm^2, 0.0103 mm^2, and 0.0148 mm^2, which accounts for a void growth across 17.4%, 21.7%, 26.1%, and 34.8% of the interface, respectively. Total, twenty-four models implementing artificial voids are studied and compared to the six models without voids which have already been presented.

As the void propagates, the current crowding and stress become more concentrated at the void front. Higher current accelerates void propagation through EM. Higher stress, as has been shown, can slow EM kinetics by blocking the void growth as it becomes concentrated at the void front. The benefit of compressive stress is limited, however, by the current crowding effect. The UBM thickness and the current flow configuration impact the effects of stress and current

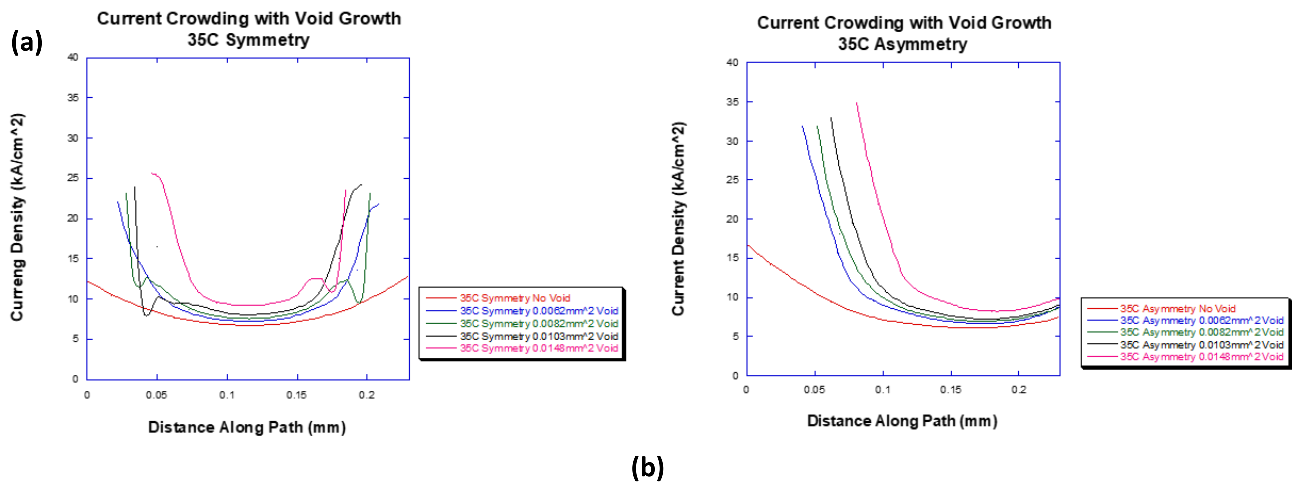

Figure 62 Current crowding plots with void growth across interface between SAC and UBM for **(a)** symmetry and **(b)** asymmetry current flow configurations.

crowding. After a certain void length, 35C has slightly higher stress than 18C, which suggests that after that critical void length, the 35 µm-thick UBM has a better current distribution and Cu supply than 18µm while also allowing a higher stress level, which could explain the longer MTTF, as well. The void growth effect is most impactful at the early stage of void growth, as the timing for

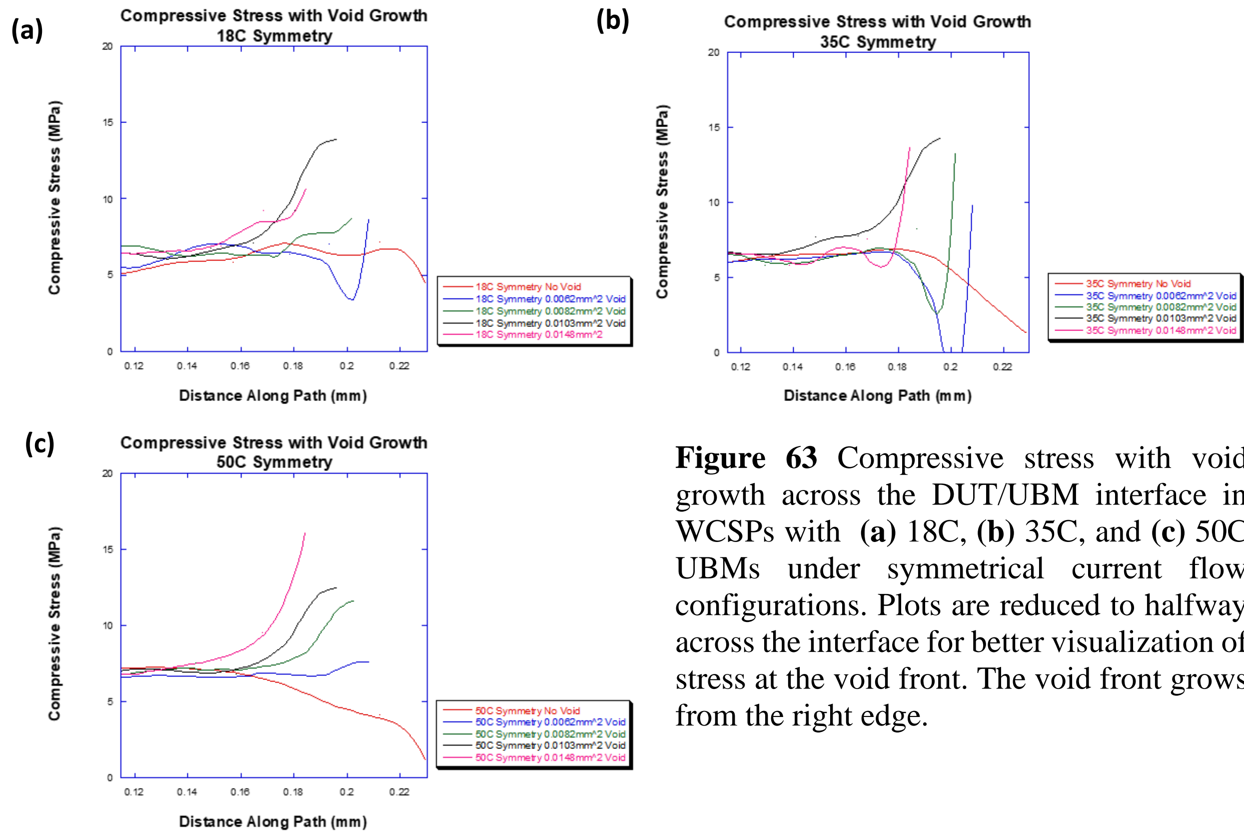

Figure 63 Compressive stress with void growth across the DUT/UBM interface in WCSPs with **(a)** 18C, **(b)** 35C, and **(c)** 50C UBMs under symmetrical current flow configurations. Plots are reduced to halfway across the interface for better visualization of stress at the void front. The void front grows from the right edge.

when the void nucleates and the rate at which it propagates decides the EM reliability and kinetics.

Figure 62 **(a)** and **(b)** includes exemplary plots of the current crowding with the void growth along the interface between the interface between the SAC solder joint and the UBM for symmetry and asymmetry current flow configurations, respectively, among WCSP samples with 35 µm UBMs. The general trend is applicable to all three UBM thicknesses, but the magnitudes differ due to the UBM thickness effect. The current crowds at the two corners or one corner on the cathodic end of the DUT under a symmetrical and asymmetrical current flow configuration,

respectively. In both cases, as the void grows, the current density also increases at the void front. In the void front region, JH also increases. Depending upon the UBM thickness, the magnitudes of each of these will vary.

Figure 63 (**a**), (**b**), and (**c**) presents three plots of compressive stress plotted along a line across the interface between the DUT and the UBM in WCSP models with 18µm, 35 µm, and 50 µm respectively, as a void propagates across the interface under a symmetrical current flow configuration. **Figure 64** (**a**), (**b**), (**c**) present three plots of compressive stress plotted along a line across the interface between the DUT and the UBM in WCSP models with 18µm, 35 µm, and 50 µm respectively, as a void propagates across the interface under an asymmetrical current flow configuration. Generally, the magnitudes of the compressive stress increase as the void length increases.

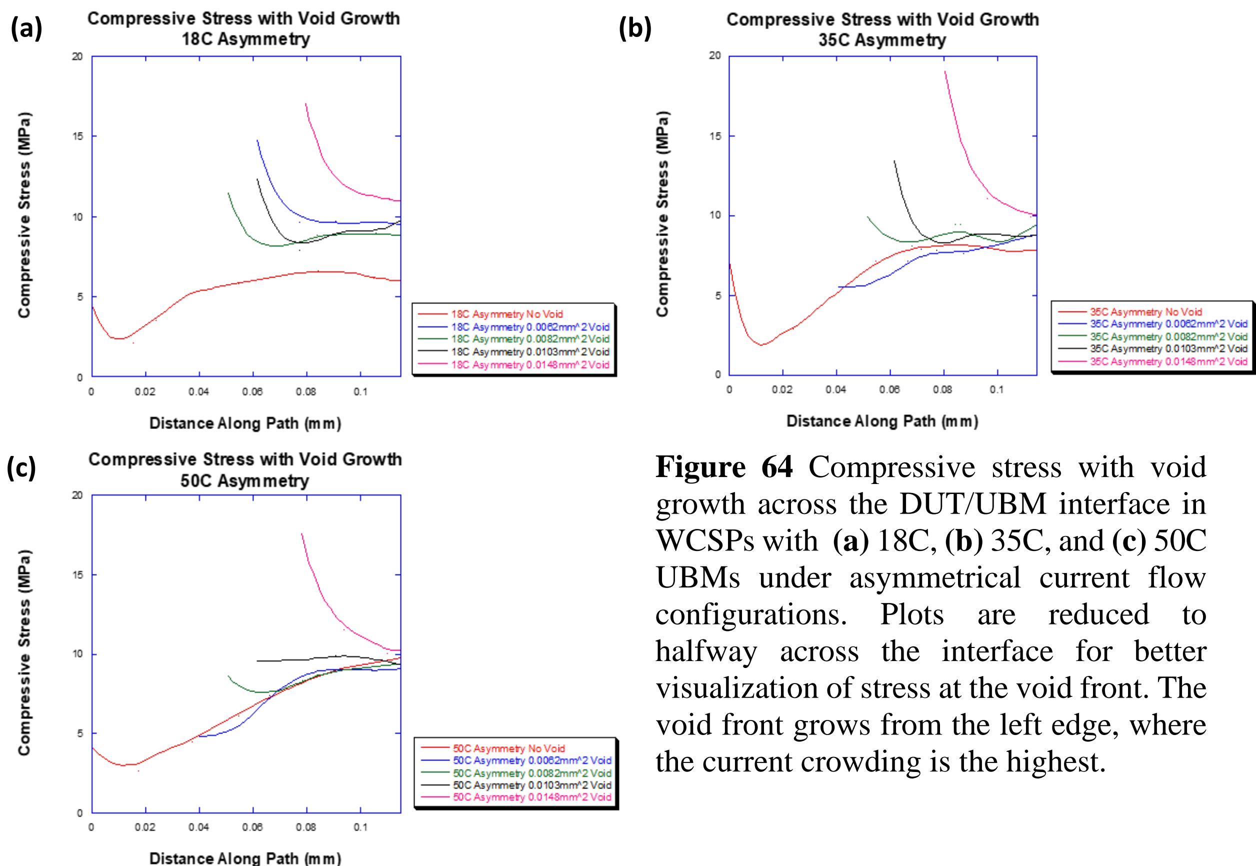

Figure 64 Compressive stress with void growth across the DUT/UBM interface in WCSPs with **(a)** 18C, **(b)** 35C, and **(c)** 50C UBMs under asymmetrical current flow configurations. Plots are reduced to halfway across the interface for better visualization of stress at the void front. The void front grows from the left edge, where the current crowding is the highest.

Plots of the maximum compressive stress at the interface and the compressive stress at the void front under symmetrical and asymmetrical current flow configurations are presented in **Figure 65**. The maximum level of stress at the interface between the DUT and the Cu UBM as well as the compressive stress at the void both overall increase as the artificial void increases in size. We see after a critical void length that the maximum compressive stress and the compressive stress at the void front in the WCSP models with 35 μm-thick UBMs will exceed that in the WCSP models with 18μm-thick UBMs, indicated by the brackets in the plots. Under symmetrical current

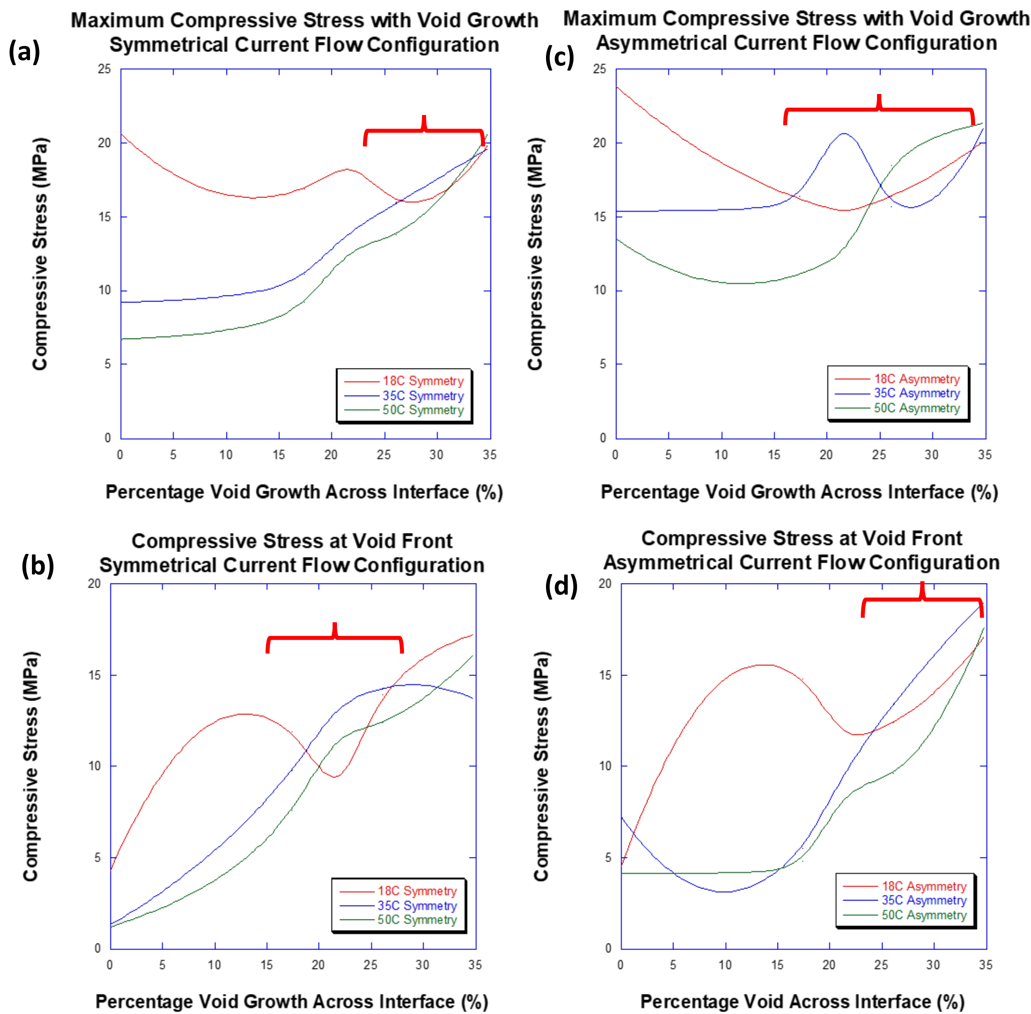

Figure 65 Plots of **(a)** maximum compressive stress and **(b)** compressive stress at the void front under a symmetrical current flow configuration. Plots of **(c)** maximum compressive stress and **(d)** compressive stress at the void front under an asymmetrical current flow configuration.

flow configurations, the maximum compressive stress in the 35C WCSP DUTs exceeds the maximum compressive stress in 18C WCSP DUTs after 17.4% of the interface is consumed by EM. At the void front, in the critical compressive stress zone, where the compressive stress is most active in blocking void growth and current density is most concentrated, the compressive stress in 35C WCSP DUTs exceeds that in 18C WCSPs after 21.7% of the interface is consumed. In symmetrical current flow configurations, the maximum compressive stress in 35C WCSP DUTs exceeds that in 18C WCSP DUTs after 26.1% of the interface is consumed. However, at the void front the compressive stress in 35C WCSPs exceeds that in 18C WCSPs when between 17.4% and 26.1% of the interface is consumed. Suffice to say, based upon the compressive stress at the void front, the compressive stress in 35C WCSPs out-benefits that in 18C WCSPs after 17.4% of the void is consumed under symmetrical current flow configurations and after 21.7% of the interface is consumed under asymmetrical current flow configurations.

This trend could potentially explain the difference in the MTTF, as the 35C WCSP samples have both sufficient Cu supply and sufficient compressive stress to slow the void propagation across the interface, surpassing the performance of 18C WCSP samples. Both 18C and 35C WCSPs generally have higher stress as the void grows than 50C WCSP models do, models of which show an increase in compressive stress, but with a slower increase than the models with thinner UBMs. This information combined with what we know about the Cu supply supports the theory derived from EM testing and previously presented FEM results in this report that the 50C WCSP samples supply ample Cu to offset the effects of EM. However, the thick UBM and thus higher ratio of Cu present compared to the SAC solder material dampens the stress by dampening the current crowding. So, while a sufficient amount of Cu us provided by the thicker UBM, the stress is dampened, and despite the dampened current crowding, the stress is insufficient to block

void growth once it forms. And thus, WCSPs with 18μm-thick UBMs do not supply enough Cu, so a void nucleates relatively earlier than it would if more Cu were supplied; however, the high level of stress caused by the lower Cu UBM:SAC ratio slows the EM void propagation and leads to higher MTTFs observed in WCSPs with 18μm-thick UBMs. Meanwhile, 35C UBM samples enjoy the best of both worlds and provides a good balance: sufficient Cu supply to delay void nucleation and sufficient stress to slow void propagation.

5.7 Conclusion

FEM and EM results lead to the conclusion that there is indeed an inflection point in the benefit resulted by the UBM thickness. Too thin of a UBM, and the limiting variable is the Cu supply. The lower Cu supply provided by thinner UBMs is believed to lead to void nucleation relatively early in the test compared to WCSPs with thicker UBMs. However, the high compressive stress generated thanks to the lower Cu UBM:SAC ratio is sufficient to prolong the void growth. Too thick of a UBM and the limiting variable is the compressive stress. The greater Cu supply provided by the thicker UBMs is believed to delay the void nucleation to later in the test compared to thinner UBMs, however, the high Cu UBM:SAC ratio dampens the compressive stress generated which is insufficient to slow the void nucleation across the interface as EM commences. Finally, an optimal UBM thickness is identified by EM tests and by FEM studies. 35 μm-thick UBMs in WCSPs appear to provide sufficient Cu to prolong void nucleation. With lower Cu UBM:SAC ratios compared to 50C WCSPs, 35C WCSPs allow a sufficient amount of compressive stress to slow the void growth. Supportive evidence of this was presented where at some points across the interface, the 35C WCSP DUTs showed to generate a greater magnitude of compressive stress, including as the void grows across the interface, than that achieved in 18C WCSPs.

CHAPTER 6: PULSED-DC DUTY FACTOR CONDITIONS AND THEIR FUNDAMENTAL EFFECTS ON ELECTROMIGRATION RELIABILITY OF WAFER-LEVEL CHIP SCALE PACKAGE JOINTS

We now understand that there is a benefit to stress during constant DC provided it is sufficient to slow EM void growth and isn't surpassed by the negative effects of current crowding. In this chapter, FEM is utilized to gain further understanding of potential limitations under non-DC conditions. In this chapter, FEM is utilized to simulate the on-off time for pulsed DC in a WCSP to gain insight on the stress development and current crowding with fluctuating DC conditions to better understand failure mechanisms in samples tested under varying pulsed-DC DFs.

6.1 Background

It has been well-established that the demand for thinner, more efficient devices continues to persist. Therefore, smaller interconnects, including solder bumps, are incorporated in microelectronic packaging. Due to the drive for higher efficiency, these interconnects are subjected to a significant level of current density. The combination between the smaller cross-sectional area through which the current flows through and the higher-power devices makes the solder interconnects more susceptible to EM failure, leading to vast efforts to mitigate such risks for failure.

Thus far, we understand that EM may occur in in-use conditions and the most commonly studied use-condition is DC. We also have a better understanding of the benefits to compressive stress under DC conditions. Many EM experiments, however, neglect non-DC conditions such as pulsed-DC due to difficulty and expense in obtaining pulsed-DC power units. Instead, previous

studies have assumed a cumulative damage model, where EM damage occurs during the "on-time" and pauses during the "off-time."

This FEM study is motivated by intriguing pulsed-DC EM test results obtained by Yi Ram Kim et. al. whose study not only debunked the cumulative failure model assumption that was applied to pulsed-DC conditions, but also indicated that three failure mechanisms are at play during low-frequency pulsed-DC tests: 1) classical EM failure by EM voiding; 2) fatigue-assisted EM failure; and 3) creep ratcheting failure. This chapter will present FEM simulations of WCSPs subjected to pulsed-DC conditions in high-frequency and low-frequency conditions. These FEM findings will be correlated to EM findings published by Yi Ram Kim et. al.

6.2 EM Performance of WCSPs Subjected to Pulsed-DC conditions.

Prior to starting the EM experiment, the pulsed DC effect was expected to follow a linear cumulative failure model; however, experimental studies have revealed that that is not the case. In fact, the longer on-off times, or greater DF, results in a shorter MTTF, and thus lower EM reliability rates. Cross-sectional analyses of failed samples tested under high DFs demonstrated that the DUT fails in a fatigue-like failure mechanism, as a thin crack is formed along the IMC layer at the DUT/UBM interface on the cathode end of the DUT. Also surprising is shorter on-off times, or lower DF, result in longer MTTF, increasing the WCSP DUT's reliability against EM failure. FEM analysis is expected to reveal a mechanism where the DUT heats up with JH associated with the current "on-time," and then cools down with a drop in JH during the current "off-time." The stress is expected to be higher than the yield stress of the SAC material; however, in order for fatigue to occur, there must be some plastic deformation. Therefore, it is expected that the level of compressive stress will be arrested by the yield stress, and work will occur, leading to dislocation gliding and other forms of plastic deformation during the "on-time." Relaxation, and

therefore tensile stress, will occur during the "off-time." It is expected that cyclic stress will occur as a result in fluctuations of JH in the DUT, with higher DFs leading to a fatigue-like failure mechanism.

Historically, EM studies have focused on DC and how it impacts EM failure kinetics. While this may be useful for understanding EM failure mechanisms and kinetics in various devices, there is a limitation in the applications because experimentation has not explored non-DC conditions. Therefore, until recent studies conducted by Kim et. al. [2, 3], there was little understanding of how non-DC conditions impact EM failure kinetics [29-45]. This hinders a comprehensive understanding of EM failure kinetics because many devices operate under non-DC conditions. So, to gain a better understanding of EM failure kinetics under non-DC conditions, Kim et. al. [2, 3] developed a method to test solder interconnects incorporated in WCSP samples under pulsed-DC EM conditions. Their comparative study operated the test under four different conditions, including DC and a low-frequency pulsed current with DF dictating the on-time.

The DFs tested were 33%, 50%, and 75% at 0.1 Hz, which translated to an on-time of 3.3 seconds and off-time 6.7 seconds, on-time of 5.0 seconds and off-time of 5.0 seconds, and on-time of 7.5 seconds and off-time of 2.5 seconds, respectively, in ten second cycle-increments. These DF at a frequency of 0.1 Hz were also briefly compared with a 50% DF at 10,000 Hz, where the time-cycle-increment is 0.001 seconds, and it was determined that a pulse DC at such a high frequency will behave similar to 100% DF or just DC conditions. Prior to completing this experimental study, Kim et. al. expected the failure kinetics to follow a cumulative damage mode, which accounted for the damage which occurred during the on-times. The assumption was that it would follow a MTTF adaptation of Black's Equation, which would suggest that the MTTF would share an inverse relationship with the DF [2, 3]. Early hypotheses predicted that samples tested

under a pulsed-DC condition of 33% DF would have a lifetime 3X that of those tested under 100% DF (or DC) conditions. This relationship described in **Eq. 25** below, which follows the cumulative damage model.

$$MTTF\ (DF) = \frac{100}{DF} * MTTF\ (DC) \qquad \textbf{[Eq. 25]}$$

To initiate EM studies, a circuit was created to induce the DC pulse on and off times. A MOSFET driver with a programmed Arduino was configured to control the DF at a low frequency of 0.1 Hz, where during off time, the current was bypassed to the ground. The findings came as a surprise and are presented in **Figure 66** below. **Figure 66** is a graph comparing the cumulative probability of WCSP samples which were tested under the four DF conditions, with a current density of 9.63 kA/cm2 and a temperature of 165°C and at a frequency of 0.1 Hz.

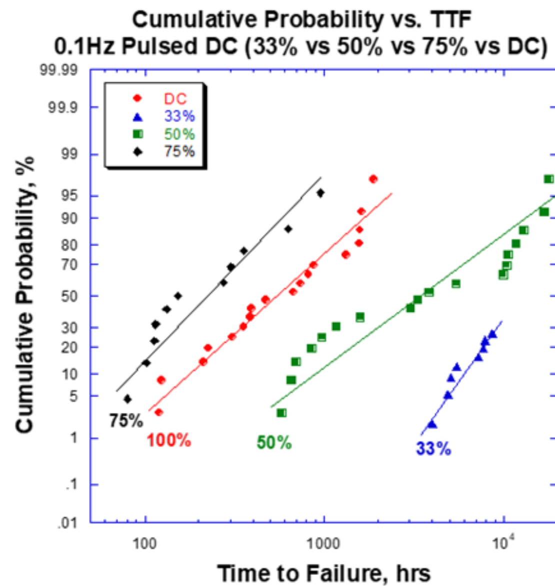

Figure 66 Graph of time to failure as a function of cumulative probability of pulse-DC conditions at a frequency of 0.1 Hz. The DF 33%, 50%, 75%, and 100% (DC) are all compared [3]

The cumulative probability vs. TTF graph shows that the samples which were tested under 75% DF conditions actually have a worse reliability against EM failure than those tested under

100% DF conditions. Samples which are tested under 50% DF conditions show an improvement in reliability compared to 100% DF, and samples tested 33% DF conditions show such a drastic increase in reliability that not all samples have yet failed after over a year of experimentation.

Upon microstructural inspection of sample which failed under 75% DF, SEM images in **Figure 67** were obtained. Interestingly, a crack is visible along the IMC at the interface between the solder joint and the Cu UBM in the 75% DF-failed sample. The sample which failed under 50% DF conditions showed a thin EM void and the sample which failed under 100% DF shows traditional voiding consistent with DC EM failure.

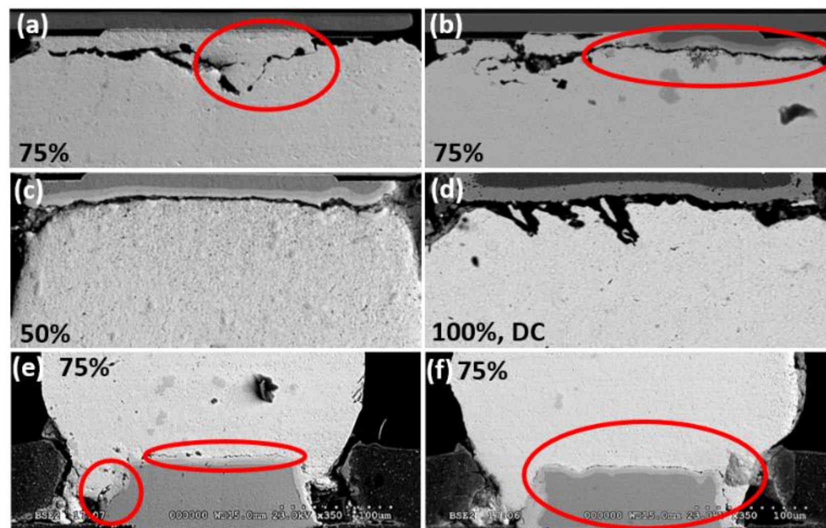

Figure 67 Cross-sectional SEM images obtained using the backscattered electron (BSE) mode. Each DUT was tested at a frequency of 0.1 Hz. **(a)** and **(b)** are images of the DUT tested under 75% DF conditions, **(c)** is an image of the DUT tested under 50% DF conditions, and **(d)** is an image of the DUT tested under 100% DF (DC). The supporting bumps, indicated by **(e)** and **(f)** show signs of tension at the bottom of the bump, as the solder joint delaminates from the Cu pad/LF at the interface between the solder bump and the Cu via. [**3**]

The crack and void suggest that significant plastic deformation, dislocation gliding and thus dislocation densification, and strain hardening occur with fluctuating temperature and stress during the pulse "on" and "off" cycles. The SEM images confirm that there is likely a fatigue-like failure which occurs in samples which failed under 75% DF conditions, as the morphology differs from samples which failed under 50% DF and 33% DF. What is predicted is that there is cyclic

compression with JH at the top of the solder bump, at the interface between the solder bump and the Cu UBM, and there is tension at the bottom of the supporting bumps with JH. During the "on-time" intervals, it is predicted that the solder joint would expand with the JH from current crowding. During the "off-time," the solder joint would contract back from cooling. Longer "off-times," allow for self-reparation within the solder joint, prolonging EM failure, explaining the longer failure time for samples which were subjected to 33% DF testing conditions. It is clear based on this morphological evidence that fatigue failure plays a significant role with the cyclic compressive stress, suggesting that there is likely a second, competing failure mechanism, where mechanical fatigue is involved. FEM simulations are expected to reveal significant stress fluctuations with temperature fluctuations as the current switches between "on" and "off" times.

Also compelling was the overwhelming evidence of creep ratcheting failure in WCSPs subjected to 33% DF low-frequency pulsed-DC conditions. The SEM images presented in **Figure 68** demonstrate the push-out effect, a classical sign of creep ratcheting failure in solder bumps. It is believed that with the longer relaxation times at a constant temperature, creep ratcheting eventually becomes the mode of failure of WCSP solder joints subjected to such conditions.

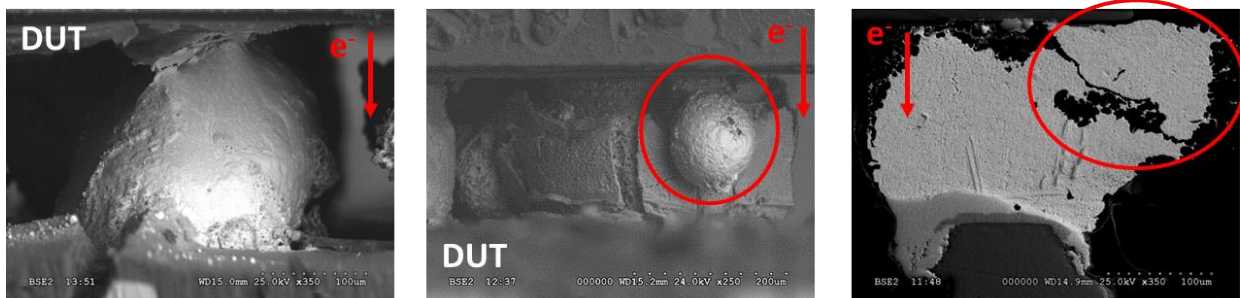

Figure 68 Evidence of creep ratcheting failure in SEM cross-sectional failure analysis of WCSPs tested under 33% DF low-frequency pulsed-DC conditions.

6.3 Predicted Stress Effect Under Pulsed-DC Conditions

One of the most concerning aspects impacting the reliability of microelectronic packaging is the stress interaction between the package components due to a CTE mismatch between materials which are bonded to one another. A CTE mismatch is problematic when the package undergoes a temperature change. The DUT will experience a greater amount of stress than the surrounding umps as it is subjected to a higher degree of current density and therefore JH. Meanwhile, the support bumps act as a constraint. The expansion that the DUT experiences will depend on the CTE. Since the solder bump's CTE does not match with that of Cu, and other package components, and we see stress generation in the presence of temperature change.

While stress has been learned to benefit EM reliability, as presented in earlier chapters, the pulsing current from the pulsed-DC testing condition is expected to cause fluctuating stress, a schematic of which presented in **Figure 69**, which would be a culprit of fatigue-enhanced EM failure.

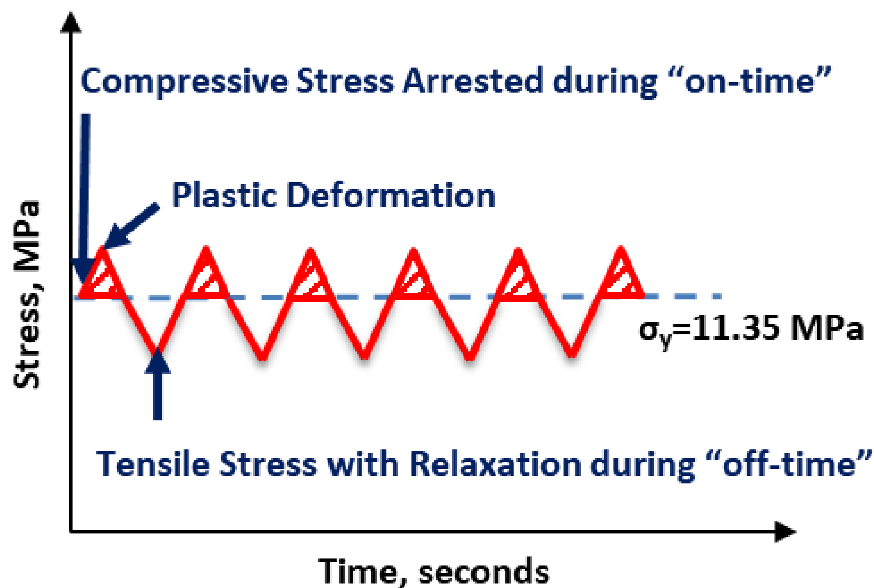

Figure 69 Predicted stress response to pulsed-DC test conditions.

Based upon EM testing results, it is hypothesized that when the current flows through the circuit, the DUT expands farther than the support bumps, so it is under compression while the support bumps are under tension. During the “on-time,” it is predicted that the compressive stress on the DUT will be arrested by the yield stress, which is approximately 11.35 MPa at 160°C, and it is during that time when plastic deformation is most likely to occur. During the “off-time,” the stress is removed and the DUT is believed to be under tension as it cools from the loss of JH and it is predicted that during this “off-time,” relaxation and eventual recrystallization may occur.

6.4 WCSP FEM Model and Elastic Computational Approach - Elastic

Following the CAD parameters listed in **Table 2,** which was presented in Chapter 3, the WCSP model consists of a 5x5 BGA on a PCB with 5x5 Cu-filled vias and pads. The solder bumps are bonded to the Cu pads with which they share a 230 µm diameter interface. Above the solder bumps are 18 µm-thick UBMs with 230 µm diameters. Situated between the UBM and the Si die is the RDL, which would be responsible for routing current into the Si chip in a functioning package. The entire model was created as a single part with many separate bodies in the model, which are the different sections assigned later in ABAQUS. A full-scale model is created in SolidWorks and reduced to a submodel for simplicity. The SolidWorks submodel is exported as a

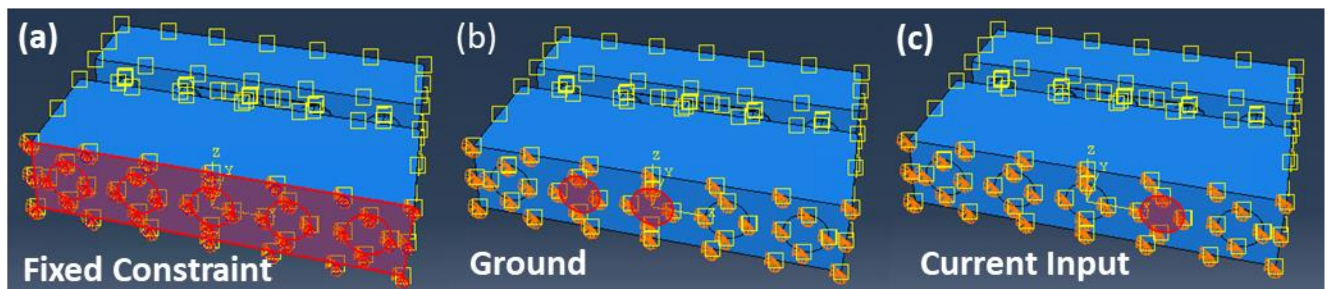

Figure 70 Boundary conditions of WCSP model indicating **(a)** fixed constant for X, Y, and Z, **(b)** current ground or output, and **(c)** current density input.

STEP file and imported to ABAQUS/CAE, where material properties outlined in **Table 3** from Chapter 3 and other boundary conditions are assigned.

Three parameters are measured in this FEM study: current crowding, JH, and stress. Elastic strain, elastic stress (von Mises stress is of particular interest as it can give an inclination of plastic response of the material although we are working with elasticity as von Mises accounts for shear stress in addition to principal stress), temperature, and current crowding in the y-direction are selected outputs for elastic studies. Using the model tree, sections are created, instances are generated, material properties are defined and assigned to the 18 subsections of the submodel. Assigned boundary conditions include a fixed constraint on the bottom faces of the PCB and the Cu vias. An asymmetrical current flow configuration with a ground and surface density input of 9.63 kA/cm^2 as highlighted in **Figure 70**. The current crowding will be concentrated on one side of the DUT, equaling 18.8 kA/cm^2. Four duty factors are studied at 0.1 HZ, including 33%, 50%, 75%, and 100% DF. Based upon **Eq. 26**, where f and t are frequency and time, respectively, we can calculate the cycle for each frequency presented in **Table 5**

$$f = 1/t \qquad \textbf{[Eq. 26]}$$

Frequency (Hz)	Cycle Time (seconds)
0.1 Hz (low-frequency)	10 s
100 Hz	1/100 s
1000 Hz (high-frequency)	1/1000 s

Table 5 Pulsed-DC cycle time per frequency.

Thus, in accordance with the four DFs simulated, the cycle on/off times are dictated by the DFs. The current is on for 3.3 seconds and off for 6.7 seconds for the 33% DF pulsed-DC condition.

The current is on for 5.5 seconds and off for 5.0 seconds for the 50% DF pulsed-DC condition. The current is on for 7.5 seconds and off for 2.5 seconds for the 75% DF pulsed-DC condition. Finally, the current is constantly on for the 100% DF condition, which is essentially DC. The DFs are controlled in the program using an amplitude tool, which, during the computation is multiplied

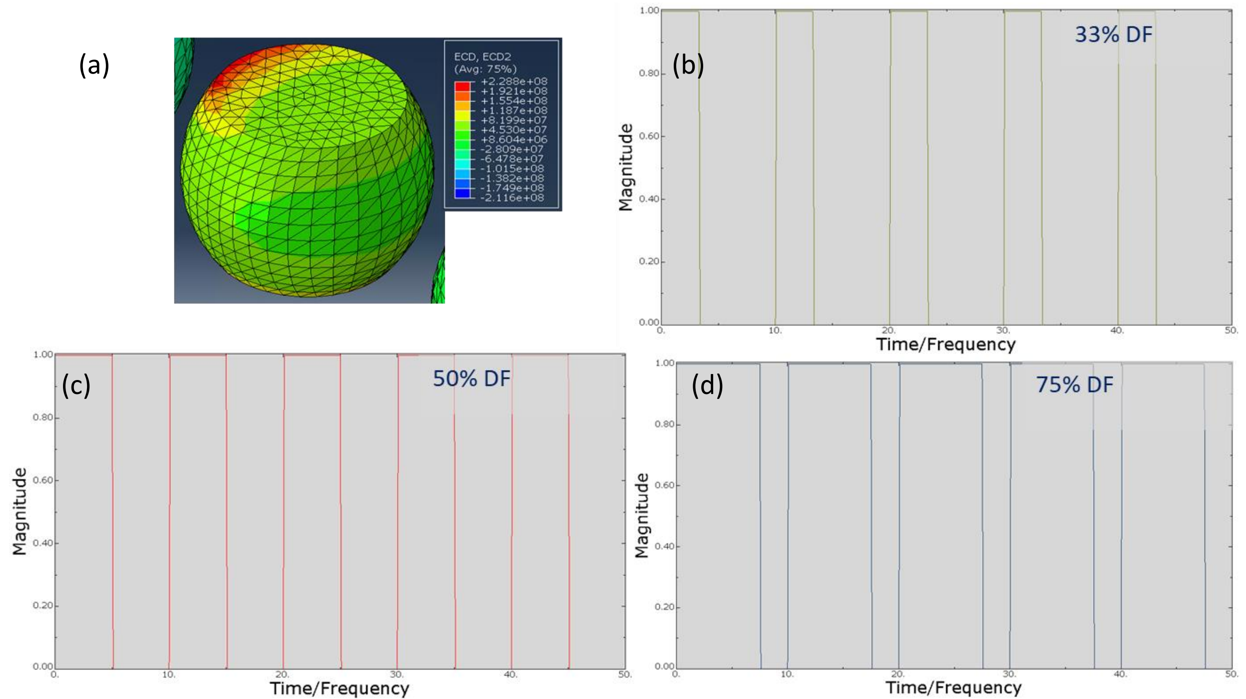

Figure 71 Applied current density and current crowding. (a) is the current crowding on the DUT; (b) is the 33% DF amplitude graph multiplied by the current density load for the 33% DF pulsed-DC condition at 0.1 Hz; (c) is the 50% DF amplitude graph multiplied by the current density load for the 50% DF pulsed-DC condition at 0.1 Hz; and (d) is the 75% DF amplitude graph multiplied by the current density load for the 75% DF pulsed-DC condition at 0.1 Hz.

by the current input, thus generating the pulsed-DC effect in the model. The amplitude plots are presented in **Figure 71**, where the magnitude during the "on-time" is 1 and the magnitude during the "off-time" is 0. These magnitudes are assigned to the current load and multiplied by the current load magnitude, 9.63 kA/cm^2 so that during the "on-time", the applied current density is 9.63 kA/cm^2 and during the "off-time", the applied current density is 0 kA/cm^2.

The seeding was defined consistently on all model edges as 2E-5 meters, which gave a reasonable mesh refinement size with decent result accuracy, but satisfactory computational time. A linear thermal-electrical-structural element type was assigned to the mesh and the mesh control was set to a Q3D4 free mesh. After generating all of these, the mesh was then generated on the model. Meshing the model results in a number of elements and nodes, depending on the size of the model and the seed size, and translated element size. For instance, this study examines the 18C model. The 18C model incorporates an 18 μm-thick UBM. Under these mesh settings, the meshed model's number of nodes and elements are 124,660 and 679,926, respectively.

Surfaces and sets were then defined. A current density input surface was defined, to which a surface current density load was applied later. Convection surfaces, CONVEC1 through CONVEC7-2 were also defined. The total number of surfaces defined are 9. Sets are also assigned, which are tagged when setting up the boundary conditions. Three sets for the X, Y, and Z constants were defined and assigned to the bottom surfaces of the model (Cu vias and PCB bottom). Next, the voltage ground set was defined and also defined and assigned to the bottom of the Cu vias connected to the circuit, in accordance with the current flow configuration.

Next, three steps were defined. The first step, labeled "Initial" is steady-state, which is useful for establishing the X, Y, and Z constant boundary conditions, which limit the model from rotating or sliding in any direction. These were assigned to the bottom faces of the PCB, and Cu vias of the model. The predefined ambient temperature is also defined in the first step, which was set to 150°C for this step. The second step, labeled "Step 1" is transient, was set to calculate for 500 seconds. The initial increment was set to 0.01, the minimum increment size was set to 0.001, and the maximum increment size was set to 10. The maximum temperature change allowed per

increment was set to 2 degrees. “Step 2” was set to account for the pulsed-DC effect for each DF and the calculation time was set to 150 seconds with the initial increment size set to 0.001, the minimum increment size set to 0.0001, and the maximum step size was set to 0.1.

In “Step 1”, the boundary conditions were set. The predefined boundary conditions and the constraints which were defined in the “Initial” step were automatically propagated in “Step 1”. Next, the voltage grounds were assigned to the voltage ground set previously assigned and the voltage value was set to zero and instantaneous. The current surface load was then applied to the surface previously assigned for the current input. The current density defined as uniformly 9.63 kA/cm2 with an instantaneous amplitude, meaning it is constant, which is consistent with direct current conditions. Next, the convection air boundary conditions were set first by assigning the interaction properties, which will be referenced when assigning interactions. This interaction property is the air coefficient, which is set to 250 W/(m^2K). Next, the interactions are assigned as surface film conditions and the sink temperature was set to 150°C. All were kept the same for “Step 2”, except the amplitude was set to match with the respective duty factors for each study, as outlined in **Figure 71**.

Output requests were selected. In ABAQUS, two types of outputs are involved: History Output Requests and Field Output Requests. History Output Request selected was energy, and outputs every 1 increment, n, was selected. The Field Output Requests selected include energy, contacts and forces, elastic stress, elastic strain, temperature (nodal and integrational), and current density. The data for the Field Output Requests was collected every 2 increments, n.

Once all boundary conditions, material properties, and mesh are all generated and assigned, a job is created. The job was set to save the data in a documents folder. The number of processors

was set to 10. The job was then submitted and allowed to run, which took approximately three days per simulation.

Post-processing involved obtaining images of each simulation run. Next, the maximum values of each output of interest were identified: current density in the y-direction (traditionally, the z-direction for most materials science and engineering texts), temperature to obtain the JH in the DUT, compressive stress, von Mises stress, shear stress, and strain. The integral point for the maximum of each of these outputs were selected, and a plot of each output over time was obtained, then exported to an excel file, which was then arranged, and plotted via KaleidaGraph. The highlights of these findings are discussed next.

6.6 Result and Discussion

In a realistic situation, accounting for plasticity, the stress applied during the “on-time” would be arrested by the yield stress, and the solder material would spontaneously deform to the

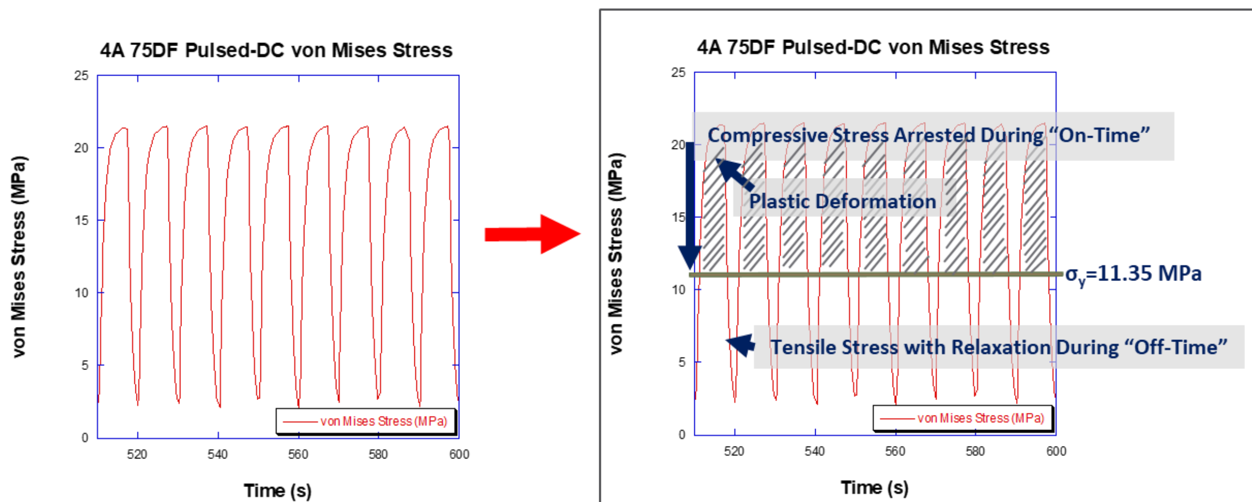

Figure 72 Theoretical schematic plot of the von Mises stress predicted to occur during the “on-time” and the “off-time” cycles. The yield stress, plastic deformation, arrested compressive stress during the “on-time,” and the tensile stress with relaxation during the “on-time,” and the tensile stress with relaxation during the “off-time.”

stress. During the "off-time," the stress would decrease to below the yield stress, allowing the solder joint to relax, and the stress is then in tension. Thus, a tension-compression thermal fatigue mechanism will combine with the EM failure mechanism, leading to an accelerated failure time and therefore a lower EM reliability. Such is the case for samples subjected to 75% DF pulsed-DC conditions.

Looking at the 75% DF von Mises stress curve in the plot in **Figure 72**, we observe that during the "on-time," compressive stress is applied. The von Mises stress is measured to be 21.5 MPa, which exceeds the yield stress of approximately 11.35 MPa. Thus, the excess stress results in plastic deformation with dislocation gliding and work-hardening. Dislocation gliding is a natural phenomenon which takes place to reduce the internal stress in the solder joint. It multiplies dislocations, which leads to high dislocation density, which then leads to work hardening. Work-

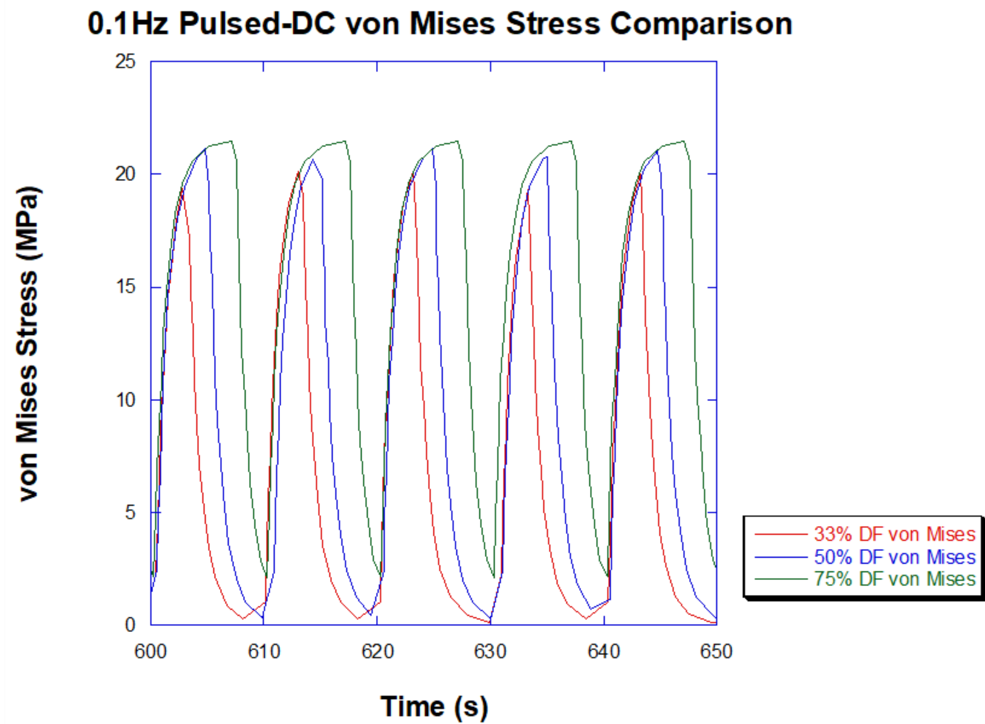

Figure 73 Von Mises stress of three DFs below 100% under 0.1 Hz frequency pulsed-DC.

hardened solder bumps are more susceptible to mechanical fatigue failure in the presence of cyclic stress.

Figure 73 is a plot of the von Mises stress of the three DFs below 100% under 0.1 Hz low-frequency pulsed-DC conditions. During the "off-time," the removal or reversal of stress occurs and thus the von mises stress drops from 21.5 MPa to 4.5 MPa, which is well below the yield stress. The stress transforms from compressive stress to tensile stress of 17.0 MPa. During this time, relaxation and material softening can occur, and recrystallization may only occur if enough time is allowed. However, crack growth from thermal fatigue cycling may progress faster than the recrystallization would. It can be concluded then, that if too short of a relaxation time is allowed, we see the acceleration of EM failure by fatigue. This supports the proposed failure mechanism of samples tested under 75% DF, where a crack is observed along the UBM/SAC interface in EM failed samples.

Meanwhile, in 33% DF conditions, the stress gets as high as 20 MPa due to a shorter "on-time" than 75% DF and the stress drops to as low as 0.1 MPa. The 33% DF conditions allow a sufficient for the relaxation period to achieve dynamic recrystallization and grain refinement during the "off" period. The time required for recrystallization is greater than the time required for fatigue crack propagation. Both microstructural features, recrystallization and fatigue cracking, are essentially competing with one another, and whichever prevails depends on the pulsed-DC DF. In the case of 33% DF pulsed-DC conditions, the recrystallization microstructural mechanism is dominant. With ample time for relaxation, the process of dynamic recrystallization essentially enables the self-repair or reset of the SAC joint's microstructure. This explains the lifetime of the samples tested under 33% DF conditions.

However, during the “off-time,” the load is kept constant at a high temperature. The stress will gradually reduce, allowing time-dependent deformation to occur, such as diffusion, dislocation climb, and creep. Creep ratcheting is evidenced by the squeezing out of the solder material from where the solder joint should be, as seen in the earlier SEM photos. That gives the indication that the WCSP solder joints are likely to fail from creep ratcheting due to the conditions induced by low DF pulsed-DC conditions.

6.7 Effects of High-Frequency Pulsed-DC Conditions

In experimental results, Kim et. al. observed that the MTTF in samples tested under 1000 Hz pulsed-DC conditions is comparable to that for those tested under 100% DF or DC. Judging by the pulsed-DC FEM results obtained with 1000 Hz high-frequency conditions, a very minimal drop in von Mises stress is observed during the “off-time” and it does not drop below the yield

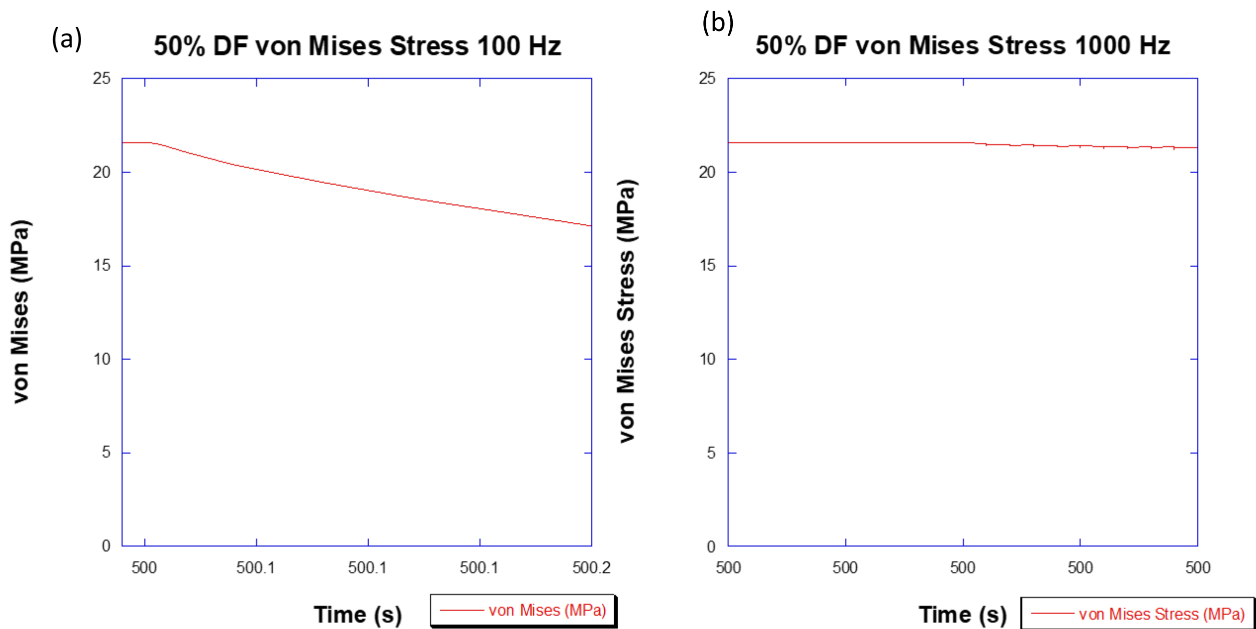

Figure 74 Plots of von Mises stress as a function of time for **(a)** 100 Hz. and **(b)** 1000 Hz. high-frequency pulsed-DC conditions.

stress, nor does it fluctuate above and below the yield stress. This suggests that tension-compression fatigue-enhanced EM is not likely to occur under high-frequency pulsed-DC conditions, unlike what was observed under low-frequency pulsed-DC conditions.

FEM was conducted for 100 Hz for good measure, and while the von Mises stress dropped more considerably than it did for 1000 Hz conditions, the stress is still not expected to drop below the yield stress or fluctuate above and below the yield stress, as can be observed in **Figure 74**.

Based upon these findings, it is relatively safe to assume that thermal fatigue is highly unlikely to occur in WCSPs subjected to high-frequency pulsed-DC conditions. Likewise, creep ratcheting is not expected to occur since the relaxation period is almost negligible compared to those allowed during 0.1 Hz low-frequency pulsed-DC tests.

6.8 Conclusion

In conclusion, with the pulsed-DC conditions, we observe three EM failure mechanisms which influence EM failure kinetics: 1) classical EM with voiding and failure by open circuit; 2) fatigue failure, which may accelerate classical EM failure; and 3) creep ratcheting, which is time-dependent and relies on a mechanism that decelerates EM failure kinetics. The two competing microstructural mechanisms include fatigue and creep ratcheting. Fatigue is caused by spontaneous deformation, while creep is time and stress-dependent. Fatigue occurs with cyclic stress and creep occurs with a constant load and temperature. The repetition of plastic deformation at the crack tip leads to crack propagation, as described in **Figure 75**. Additionally, we have current crowding at the void front, thus leading to thermal fatigue assisted EM failure. Longer “off-times” allow for sufficient time for self-repair of the microstructure.

With this ample relaxation time, we may observe dynamic recrystallization, where the microstructure may reset during the "off-time." This recrystallization takes longer than crack growth does, which is why we observe a stark difference in failure mechanisms and kinetics between 33% and 75% DFs.

These findings are critical because an improved understanding of the stress development and microstructural consequences may allow for modified in-use current applications to reduce effects of fatigue on EM failure kinetics. They may also allow for improved materials selection and package design to prolong thermal fatigue-enhanced EM failure kinetic. Understanding these mechanisms can lead to breakthroughs in design improvements.

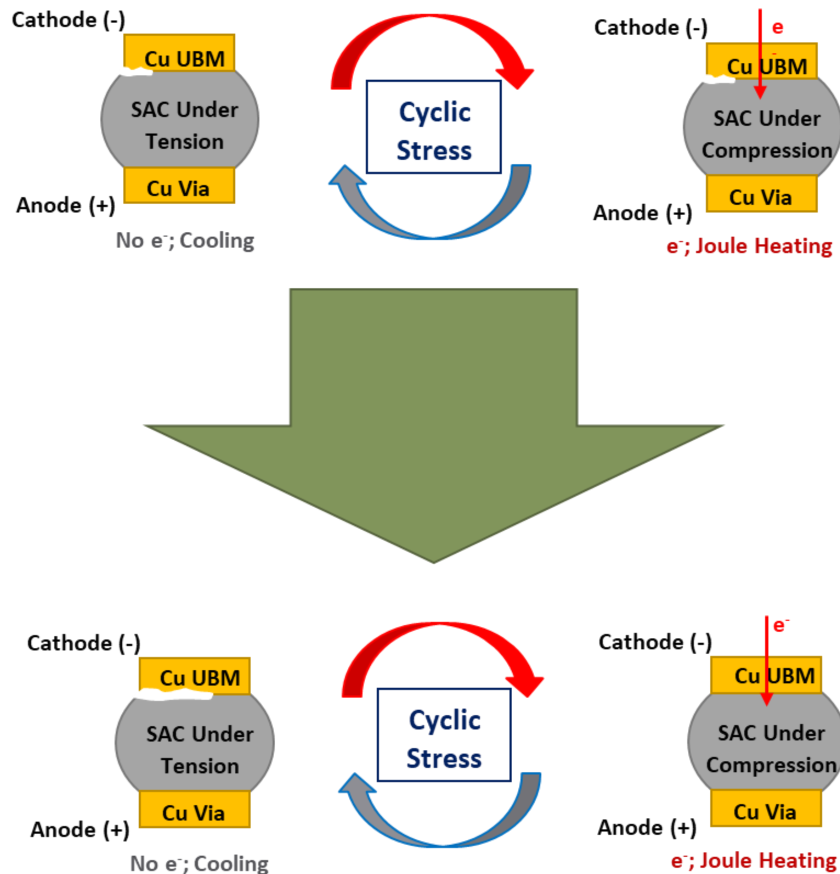

Figure 75 Schematic of cyclic stress contributing to crack and void propagation, thus accelerating EM failure kinetics.

The path forward involves more in-depth plasticity studies modeling the crack propagation at the void tip, which would require damage modeling and would likely necessitate the use of a supercomputer. Currently, AC studies are underway with the intent to gain an understanding of non-DC conditions without added effects like fatigue and creep ratcheting. FEM studies expanding on AC conditions are merited, as well.

CHAPTER 7: POLYIMIDE OPENING SIZES IN WAFER-LEVEL CHIP SCALE PACKAGES AND THEIR FUNDAMENTAL EFFECTS ON ELECTROMIGRATION RELIABILITY

We now understand that compressive stress is beneficial under certain current conditions and among WCSPs with certain design parameters. Taking a step further, the focus of this chapter is to exploit the benefits of compressive stress and controlling current crowding to gain optimal conditions and design parameters which could extend to industrial efforts in improving WCSP interconnects' reliability against EM failure. A layer of polyimide (PI) is deposited between the Si, RDL, UBM, and SAC solder joint. PI layers included in this fashion are meant to provide structural support. In this particular study, however, the PI layer is included with controlled opening sizes to determine which PI opening size is most beneficial in terms of current crowding, JH, and ultimately EM reliability.

7.1 Background

FEM has been implemented to simulate the effects of the PI opening size on the current crowding, JH, and stress to gain insight on their impacts on EM reliability in WCSPs. Between the RDL and the UBM, a 7 μm PI layer is situated, with Cu-filled openings which route current between the RDL and the UBM. The PI opening sizes vary from small, medium, and large with diameters 124 μm, 144 μm, and 160 μm, respectively. All models would have an 18μm UBM layer situated between the RDL and the solder joint.

The experimental aspect of this research this aim is intended to supplement is ongoing, so there are no EM test results to compare this FEM study with, which makes it all the more exciting. Theoretically, WCSP models that have PI layers with limited PI opening sizes are expected to

impact the current density, JH, and compressive stress. A hypothesis is that smaller PI openings are expected to be more beneficial than larger PI openings.

WCSPs with smaller PI openings are predicted to have a greater amount of current crowding than WCSPs with larger PI openings. At the same time, WCSPs with smaller PI openings between the UBM and the RDL would likely experience a greater amount of JH and compressive stress towards the center of the solder joint on the cathode end but a smaller amount of compressive stress along the perimeter of the solder joint, where the UBM it shares a contact with does not have contact with the pad that leads to the conductive RDL. WCSP samples which have a larger PI opening have a larger contact area between the UBM and the RDL will likely have a larger amount of compressive stress along the contact area in relation to the area which does share a contact between the UBM and the RDL but a greater current density distribution, particularly allowing current to access the edges where voids typically nucleate. The trend which is expected to be observed in this aim will supplement whatever the EM reliability results are to be yielded, in time. Judging by the relation between the earlier aims and their impact on EM reliability, a general prediction may be that samples with a smaller PI opening would have proven to enhance the reliability of these packages against EM failure.

7.2 Methodology: Model Parameters, Material Properties, and FEM Boundary Conditions

Following the CAD parameters laid out in **Table 2**, which was presented in Chapter 3. The submodel is created as a single part in SolidWorks. The PI opening models use a similar design as the WCSP models do. The main difference is the inclusion of a 7 μm-thick PI layer between the

Cu UBM and the Cu RDL, which is located on the Si die. **Figure 76** below illustrates the SolidWorks CAD model. It is comprised of 23 sections, including a PCB, five Cu vias, five SAC solder bumps, three UBMs, three Cu connections between the UBM and the RDL, one RDL, two Cu posts, and one Si die. The SolidWorks model is exported as a STEP file, and then imported

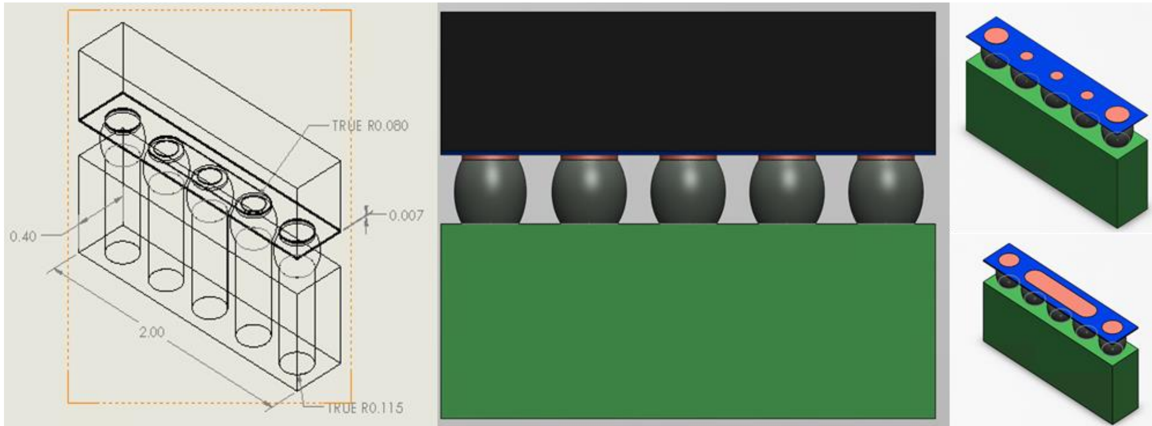

Figure 76 SolidWorks model of various PI opening diameters in WCSP. Three models have been created for each PI opening, small, medium, and large. The PI opening will be defined for each of the three models: small, medium, and large circular opening with diameters 124 µm, 144 µm, and 160 µm, respectively. The blue in the model represents the PI, where the openings allow contact between the RDL and Si, and only allow a small opening to the UBM from the RDL. The PI thickness is 7 µm. Everything else in the model is the same as that in the WCSP model without the PI layer.

into ABAQUS/CAE. Upon the importation of the STEP file, the material properties are defined according to **Table 3** from Chapter 3, the material sections are generated, and each of the sections is assigned a material section.

Next, in the assembly tab of the model tree, instances are generated, and the mesh was directed to be independent so that the mesh can be done on the instance. Seeds along the edges of the model were defined. Since this submodel is $1/5^{th}$ of the full model, the seeding was defined consistently as 2E-5. A linear thermal-electrical-structural element type was assigned to the mesh and the mesh control was set to a Q3D4 free mesh. The number of elements and nodes increase

with the increasing UBM thickness, but in general, all models had over 100,000 nodes and over 600,000 elements After generating all of these, the mesh was then generated on the model.

To save time in setting the boundary conditions, surfaces and sets were defined. A current density input surface was defined, to which a surface current density load was applied later. Convection surfaces, CONVEC1 through CONVEC7-2 were also defined. The total number of surfaces defined are 9. Sets are also assigned, which are tagged when setting up the boundary conditions. Three sets for the X, Y, and Z constants were defined and assigned to the bottom surfaces of the model (Cu vias and PCB bottom). Next, the voltage ground set was defined and also defined and assigned to the bottom of the Cu vias connected to the circuit, in accordance with the current flow configuration.

Two steps were then defined. The first step, labeled “Initial” is steady-state, which is useful for establishing the X, Y, and Z constant and ambient temperature (150°C) boundary conditions, which limit the model from rotating or sliding in any direction. The X, Y, and Z constraints were assigned to the bottom faces of the PCB, and Cu vias of the model. The second step, labeled “Step 1” is transient, which means it is time-dependent and is useful for solving problems which lack linearity solutions. “Step 1” was set to calculate for 500 seconds. The initial step was set to 0.01, the minimum step size was set to 0.001, and the maximum step size was set to 10. The maximum temperature change allowed per increment was set to 2 degrees.

In the “Step 1”, the boundary conditions were set. The predefined boundary conditions and the constraints which were defined in the “Initial” step were automatically propagated in “Step 1”. Next, the voltage grounds were assigned to the voltage ground set previously assigned and the voltage value was set to zero and instantaneous. The current surface load was then applied to the surface previously assigned for the current input.

The FEM testing matrix, as shown in **Table 6** includes Symmetry and Asymmetry current flow configurations with 18 μm-thick UBM layers between the solder bump and the PI layer. Within the PI is a Cu filling, through which current flows from the UBM to the RDL.

Structure	**PI Opening Diameter (μm)**	**Temperature (°C)**	**Current (A) Symmetry & Asymmetry**	**Current Density (kA/cm^2)**
18C	124 (small)	165	4	9.63
18C	144 (medium)	165	4	9.63
18C	160 (large)	165	4	9.63

Table 6 PI Opening WCSP FEM Testing Matrix

All boundary conditions are kept the same as tested in WCSPs without a PI layer. Testing temperature was set to 165°C, and the current applied was 4 A, or 9.63 kA/cm^2 at the Cu via pad/Solder bump and at the Cu UBM/Solder bump interfaces. The current crowding at the PI opening was considerably smaller, reducing to 33.12 kA/cm^2, 24.56 kA/cm^2, and 19.89 kA/cm^2, for small, medium, and large PI openings, respectively.

Next, the convection air boundary conditions were set first by assigning the interaction properties, which will be referenced when assigning interactions. This interaction property is the air coefficient, which is set to 250 $W/(m^2K)$ based on previously determined information in the previous chapter with the full model, where the JH was maintained at around 10°C and the model is under forced convection. Next, the interactions are assigned as surface film conditions and the sink temperature was set to 150°C.

History Output Request selected was energy, and outputs every 1 increment, n, was selected. The Field Output Requests selected include energy, contacts and forces, elastic stress, elastic strain, temperature (nodal and integrational), and current density. The data for the Field Output Requests was collected every 2 increments, n.

Once all boundary conditions, material properties, and mesh are all generated and assigned, a job is created. The job was set to save the data in a documents folder. The number of processors was set to 10. The job was then submitted and allowed to run, which took approximately three hours per simulation.

7.4 Result and Discussion

Results from the FEM simulations of WCSP models with varying PI opening sizes indicate that there is a considerable difference in the outputs of interest among the three PI opening diameter variables. While not much is known physically, applying the knowledge obtained from earlier models gives an intuitive clue that the WCSP model with the smaller PI opening is most beneficial in advancing the EM reliability of WCSPs.

Figure 77 **(a)**, **(b)**, **(c)**, and **(d)** include screenshots of the current density and compressive stress under asymmetrical and symmetrical current flow configurations. It is worth noting that the compressive stress appears to be highest in the center bump in the model. This may be owed to a combination between the current density, particularly for the symmetrical current flow configuration, and also to the support bumps which are under tension, thus constricting the model

as it expands freely with the change in temperature. The current density images, presented in **(a)** and (c), clearly demonstrate, however, the current flow throughout the model.

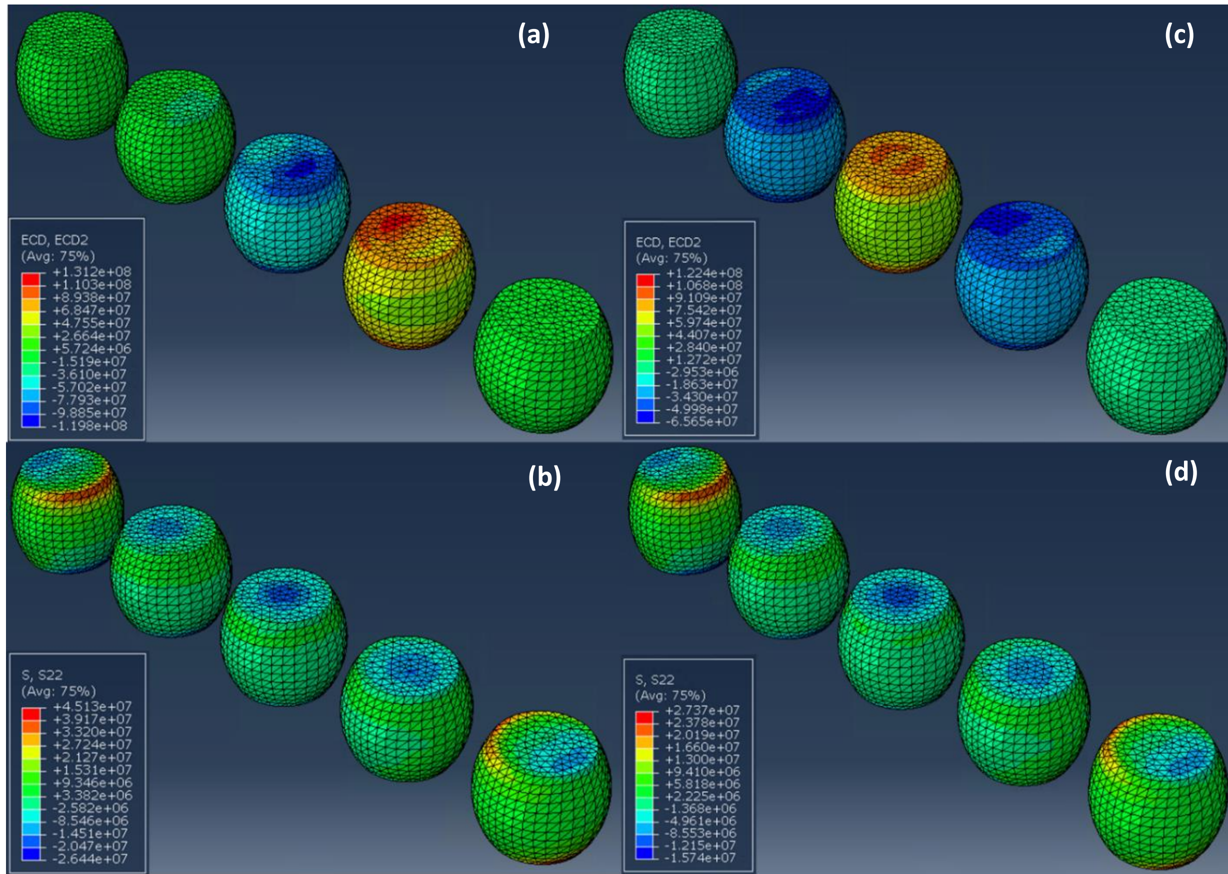

Figure 77 Screenshots of **(a)** current density and **(b)** compressive stress in WCSP PI model with a small PI opening diameter subjected to an asymmetrical current flow configuration; **(c)** and **(d)** current density and compressive stress in WCSP PI model with a small PI opening diameter subjected to a symmetrical current flow configuration.

The level of JH under a symmetrical current flow configuration was 21.3°C, 19.9°C, and 19.2°C, for the WCSP model with small, medium, and large PI openings, respectively. The level of JH under an asymmetrical current flow configuration was 36.0°C, 33.6°C, and 32.9°C, for the WCSP model with small, medium, and large PI openings, respectively.

While the current crowding through the largest PI opening is lower than that observed in the WCSP model with the smallest PI opening diameter, more interestingly, the large PI opening actually demonstrates a higher level of current crowding at the DUT cathodic edge at the interface between the UBM/PI/SAC solder joint. Meanwhile, the smallest PI opening demonstrates a lower level of current crowding at the DUT cathodic edge at the interface between the UBM/PI/SAC. It seems that the current path becomes more concentrated in the center of the DUT/UBM interface than at the edges. This particular finding can be observed in **Figure 78**, where the current density is plotted along a line across the interface between the Cu UBM and the SAC solder joint.

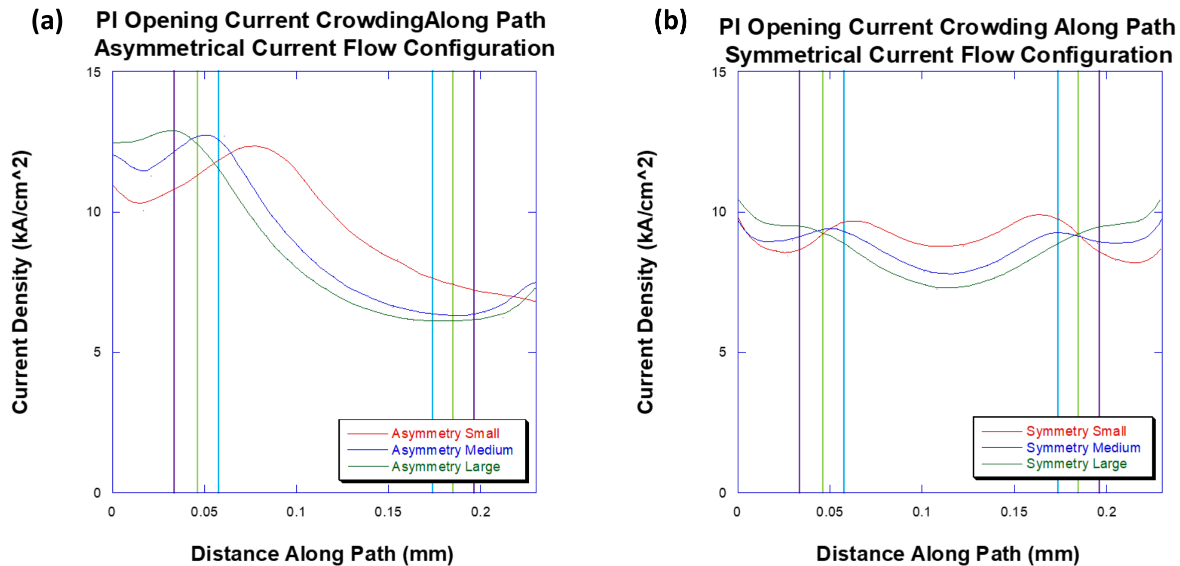

Figure 78 Current density plots along a path at the UBM/SAC solder bump interface with PI opening diameter for **(a)** asymmetrical and **(b)** symmetrical current flow configurations. Blue, green, and purple vertical lines resemble the location of the small, medium, and large PI opening edges, respectively.

Additionally, the compressive stress appears to be higher in magnitude at the DUT/UBM interface in WCSP models with smaller PI openings. Oppositely, the compressive stress is lower in the WCSP models with larger PI openings. The plots featured in **Figure 79** illustrate the compressive stress along the interface between the UBM/SAC solder bump interface. The

increased compressive stress alone can be predicted to be beneficial for EM failure reliability, especially for smaller PI openings. As has already been established, compressive stress appears to benefit the reliability of solder interconnects because it acts to block the void growth under EM conditions. However, the stress does not paint the whole picture for the reliability of a package interconnect. Also important, as we well know, is how the current crowding may inhibit any benefit compressive stress may provide.

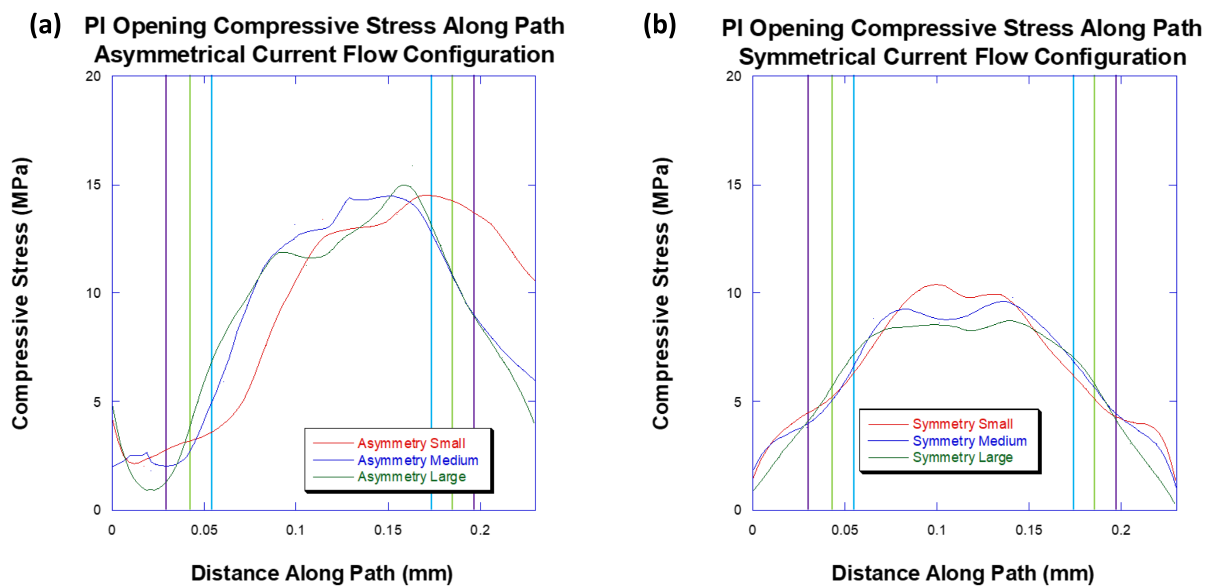

Figure 79 Plots of compressive stress along path with PI opening diameter for **(a)** asymmetrical and **(b)** symmetrical current flow configurations. Blue, green, and purple vertical lines resemble the location of the small, medium, and large PI opening edges, respectively.

By the current density and compressive stress plots, it can be predicted that the small PI openings serve to benefit the WCSP more so than the small PI openings. The biggest clue actually lies with the combination between the location of the current density and the compressive stress. In all PI opening models, the compressive stress appears to be concentrated in the center of the DUT/UBM interface, reflecting the location of the PI opening. The asymmetrical current flow configuration resembles that which was observed in earlier studies comparing the compressive stress among UBM thicknesses. While the stress favors the opposite side of the current density

and JH, it is high and works against EM failure. However, because of the location of the current relative to the stress, the WCSPs subjected to asymmetrical current flow configurations are not likely to perform as well as those subjected to symmetrical current flow configurations. Under the symmetrical current flow configuration, the stress appears to be more consolidated near the center of the UBM/SAC solder joint interface than it was under asymmetrical current flow configurations.

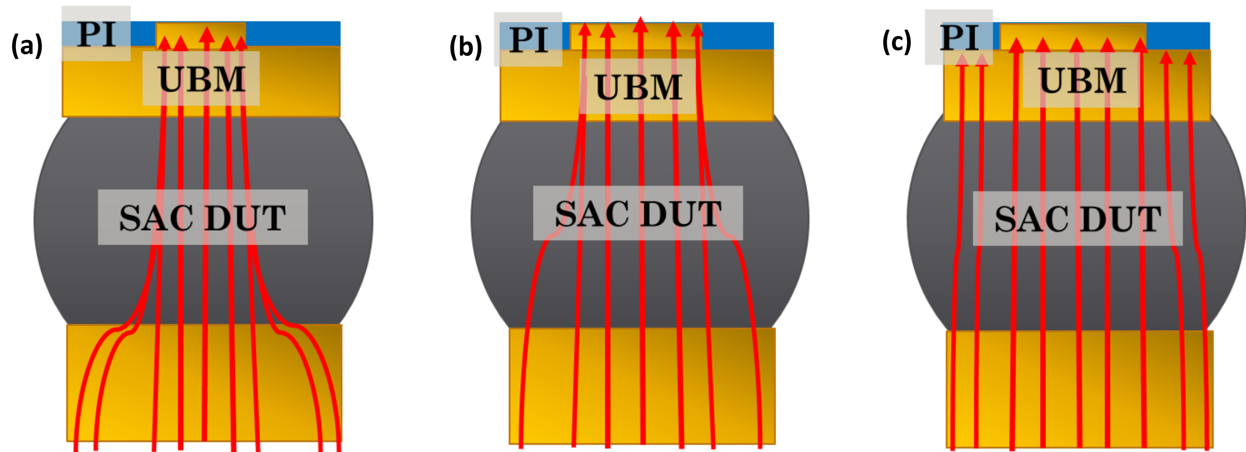

Figure 80 Current path behavior with respect to PI opening. (a) is the depiction of the current path as it flows through the interconnect with a small PI opening in the model; (b) is the depiction of the current path as it flows through the interconnect with a medium PI opening in the model; (c) is the depiction of the current path as it flows through the interconnect with a large PI opening in the model.

Figure 80 is a schematic of the current path behavior as it passes through the solder interconnect depending on the PI opening diameter. It is believed that a smaller PI opening forces the current density to correct itself earlier in the current path than the larger PI opening does. Because the current density is mostly consolidated to the center of the interface for small PI opening models, a limited amount of the UBM/SAC interface is subjected to high current crowding ideal for EM conditions. This allows perhaps for the control of where a void will form. Should it form in the center of the DUT first, perhaps the current crowding will apply on both fronts of the void, but a lower level of current density than if it were conglomerated at a void which may form asymmetrically from the outer edge of the DUT. Also, should a void nucleate along the interface,

the UBM/SAC interface will remain in contact toward the edges where little to no current density is present. Most helpful, though, is by controlling where the void will form so that it would be located where the compressive stress is the highest, a void may be further delayed thus prolonging the EM failure kinetics. The current density trend observed in smaller PI openings is not observed in models with larger PI openings. In fact, the current rushes toward the outer edges of the DUT/UBM interface in models with larger PI openings, subjecting the edges to current crowding and adding potential for a void to form on the outer edges in addition to the middle of the DUT/UBM interface.

This leads to the conclusion that the WCSP model with a large PI opening will not be immune to the effects of EM, and so the samples with smaller PI openings are expected to have better EM reliability than those with larger PI openings. The large level of current crowding at the DUT edge is predicted to contribute to accelerated EM kinetics of large PI opening samples in comparison with smaller PI opening samples.

6.6 Conclusion

Overall, simulative results indicate that samples with smaller PI openings will be most reliable against EM failure. Smaller PI openings not only influence the current density so that the current path is altered, and current density is contained to the middle of the DUT/UBM interface, sparing the outer edges of the DUT, but the compressive stress is also mostly concentrated at the center of the DUT. The compressive stress in the center of the DUT/UBM interface among WCSP models with small PI openings is considerably higher than that observed with larger PI openings, and it is predicted to be sufficient enough to delay the growth of the void across the interface.

Most importantly, however, is that the current density and the compressive stress are contained in the center of the DUT/UBM interface, allowing a contact to remain between the DUT and the UBM in non-current crowding regions. The regions where current crowding is not present are actually typical void nucleation sites in WCSPs which do not have a PI layer with controlled openings. Because these do not undergo current crowding, at least not until a void occupies the center of the DUT where the current path is routed through, there is a predicted delay in EM failure. This is predicted to happen since a large area of the DUT/UBM interface will remain intact, thus maintaining a circuit for a longer duration.

CHAPTER 8 : CONCLUSIONS AND FUTURE WORK

A baseline has been established of the capabilities of identifying a relationship between EM kinetics and solder material behaviors through FEM. FEM was used to study the stress, JH, and current density trends among WCSPs with varying design parameters to gain greater understanding of EM reliability results previously obtained and published by Yi Ram Kim et. al.

Our investigation has shown that compressive stress benefits the WCSP interconnect reliability against EM mechanisms as it blocks the void growth across the interface between a SAC solder joint and a UBM. The benefits of the compressive stress are limited by the current crowding and JH. FEM studies have been taken a step further to identify interconnect designs and parameters which best benefit WCSPs against EM failure, such as UBM thickness and controlled PI openings. FEM studies also provided supporting evidence for ideal current conditions such as symmetry DC, asymmetry DC, and pulsed-DC under low and high-frequencies.

Overall, this work has proven the effectiveness of obtaining a relationship between the material behavior and EM kinetics. A considerable number of variables are compared in this study to gain some insight and intuition on EM performance of WCSPs and other package types. However, valuable future work would involve mesh convergence studies, unique to each model and condition, to obtain concrete and reliable values of stress generated in each thermal-electrical-structural model. The average size of the mesh used in the models presented in this research had element sizes of 2E-5, generating over 100,000 elements, which is suitable for identifying reliable trends but perhaps not beneficial for ideal accuracy in obtaining concrete numbers for applicability to real life situations. Models with this mesh size required about three hours to solve. Too course of a mesh, (any mesh with elements larger than 5E-5) generated bad elements and the jobs failed. Refining to elements with 1E-5 or smaller in size in all sections of the model generated such a

fine mesh that it required an outrageous amount of time to solve – several days for a simple submodel in which the current was constant and only elasticity is accounted for. Considering the fact that at least 33 models were necessary to run in this research alone – and several iterations of these were used to identify ideal boundary conditions – a timeline where the simplest model requires several days to solve is not sustainable.

An ideal convergence study would begin with a starting point in the number of nodes in the model and the amount of time required to solve such a problem would be recorded. The time required to solve as the number of nodes are doubled would follow an exponential curve. Eventually, a certain number of nodes would prove to be acceptable in terms of obtaining reliable results (the value of stress will not change much with an increase in nodes in the mesh) in an acceptable amount of time. These types of studies, especially for a large number of models, at least 33 models alone from the research presented in this report, would require a significant amount of time. This would thus require the use of a supercomputer to not only save time and computation costs, but to allow a significant increase in nodes, as normal desktops are unable to solve a mesh with a large number of nodes in a respectable amount of time. A barrier to accomplishing this, however, is licensing restrictions. ABAQUS has allotted 14 seats between our research group and another. The seats are only allowed to be used on UTA computers and accessed through a UTA IP address. It is possible to run simulations using ABAQUS on the Texas Advanced Computing Center (TACC) supercomputer; however, a significant amount of bureaucracy is projected to contribute to delays. Additionally, the TACC does not operate programs using a graphical user interface (GUI) like ABAQUS on a desktop, and instead operates off of command prompts, so there will be a learning curve for new users. Now that this work is complete, however, it may allow

ease of budgeting free computation time allotted to UTA students by the TACC and may save computational costs overall.

8.1 CURRENT FEEDING CONFIGURATIONS AND UBM THICKNESSES AND THEIR FUNDAMENTAL EFFECTS ON ELECTROMIGRATION RELIABILITY OF WAFER-LEVEL CHIP SCALE PACKAGE SOLDER JOINTS

In tandem, FEM and EM tests are conducted to compare the effects of current flow configurations and UBM thickness. The two current flow configurations subjected the WCSP samples and WCSP models to different levels of current density to identify the most beneficial current flow configuration while also gaining a fundamental understanding of such effects. The three UBM thicknesses considered were 18 μm, 35 μm, and 50 μm, all of which were selected to gain an understanding of the UBM thickness effect on EM failure kinetics and mechanisms.

Under the two current flow configurations, symmetrical and asymmetrical, EM results did not indicate a difference in behavior between the two current flow configurations. In fact, the failure kinetics appeared to be random among samples which failed earlier in the test, regardless of current flow configuration. FEM results did not show any calculated differences between the two current flow configurations which would translate to early-failed samples. Thus, we can conclude based upon FA conducted on EM-tested WCSPs that samples which failed earlier in the test were likely owing to the c-axis alignment of the Sn grain orientations so that they were parallel to the EM path. The alignment of the grain orientations to the c-axis creates a larger path through which conductive atoms may easily migrate. This phenomenon accelerates EM kinetics, sometimes by 500X, according to literature. This relationship is not something that could be simulated through the style of FEM approach presented in this dissertation. While FEM may not

have been able to provide clues as to the behavior of SAC solder joints which failed earlier in the EM tests, FEM results did identify a relationship between the current flow configuration and EM kinetics among late-failed samples. Because asymmetrical current flow configurations have higher current densities than symmetrical current flow configurations do, they have lower MTTFs than WCSPs tested under symmetrical current flow configurations. This is something that was predicted intuitively, and the current density behavior observed FEM confirm the results obtained in FEM.

UBMs are commonly employed by industry to offset the effects of EM kinetics by supplying more Cu to the circuit, which is forced from the cathode end to the anode end of the DUT. The added Cu allows EM to commence but delays the formation of EM voids. What was discovered during EM testing and confirmed by FEM is that the failure kinetics are impacted by two factors: 1) Cu supply and 2) compressive stress. The thickest UBMs (50 μm), which have a higher Cu:SAC ratio, have shown to not only distribute the current density along the interface more evenly, but also to dampen the effects of the CTE mismatch between the two bonded materials. Voids in WCSP solder interconnects will likely be delayed thanks to the greater Cu supply, but the low compressive stress is not effective at blocking the void growth. Thus, the limiting variable for WCSP solder joints with thicker UBMs is the compressive stress. The thinnest UBMs (18 μm), which have a lower Cu:SAC ratio allows higher current density and lower Cu reservoir, so a void may nucleate early in the EM tests, but the high stress effectively slows the void propagation. Thus, the limiting variable for WCSP solder joints with thinner UBMs is the Cu supply. Of the three UBMs tested, the most optimal UBM thickness was 35 μm-thick. This provided a sufficient Cu supply and compressive stress to the DUT during EM testing compared the two more extreme UBM thicknesses. The compressive stress observed during the void nucleation and propagation indicated that after a critical void length, after between 21-26% of the

interface has been consumed, the compressive stress concentrated at the void front and the maximum amount of compressive stress along the interface exceeds the magnitudes achieved with WCSP models with 18 µm-thick UBMs. This could explain the nonlinear relationship where the MTTFs of WCSPs with 35 µm-thick UBM far exceed the WCSPs with the thicker and thinner UBMs.

Future works to expand on the benefits provided by WCSPs by identifying a more ideal UBM thickness than 35 µm-thick UBMs. The three UBM thicknesses were originally selected as arbitrary thin, medium, and thick UBMs. Perhaps a slightly thinner or slightly thicker UBM may prove to increase the WCSP solder joint's reliability far better than 35 µm-thick UBMs can.

8.2 PULSED-DC DUTY FACTOR CONDITIONS AND THEIR FUNDAMENTAL EFFECTS ON ELECTROMIGRATION RELIABILITY OF WAFER-LEVEL CHIP SCALE PACKAGE JOINTS

Much has been understood about the EM kinetics under DC conditions, and the research thus presented support findings which identify compressive stress as a reliability benefit under DC conditions. However, pulsed-DC conditions introduce entirely new reliability challenges. Under pulsed-DC conditions, three EM failure mechanisms which influence EM failure kinetics can be identified: 1) classical EM with voiding and failure by open circuit; 2) fatigue failure, which may accelerate classical EM failure; and 3) creep ratcheting, which is time-dependent and relies on a mechanism that decelerates EM failure kinetics. Fatigue and creep ratcheting failure are both competing microstructural mechanisms which occur in the DUT depending upon the DF conditions. Fatigue is caused by spontaneous deformation and occurs with cyclic stress. Meanwhile, creep is time and stress-dependent and occurs with a constant load and temperature. The repetition of plastic deformation at the crack tip leads to crack propagation. With the

compounding current crowding at the crack tip and void front, thermal fatigue assisted EM failure occurs. Lengthier “off-times” allow a sufficient amount of time for self-repair of the microstructure to occur. The abundant relaxation time allowed in pulsed-DC conditions at lower DFs may lead to dynamic recrystallization, where the microstructure may reset and undergo self-repair during the “off-time.” Dynamic recrystallization requires more time than crack growth does, which is why we observe a difference in failure mechanisms and kinetics between the 33% and 75% DFs. 33% DFs allow sufficient time for dynamic recrystallization . 75% DFs restrict the relaxation time, therefore preventing dynamic recrystallization to occur and instead allowing crack propagation to commence. 75% DFs thus lead to fatigue-assisted EM failure. 35% DFs eventually lead to EM failure while those which almost appear to be immortal eventually experience creep-ratcheting failure.

We also observed that fatigue and creep ratcheting are two mechanisms unique to low-frequency pulsed-DC conditions. EM tests conducted under high-frequency DC, at 1000 Hz with 50% DF, conditions proved this to be true as the MTTF obtained from samples tested under this condition were very similar to those tested under DC. FEM revealed that under high-frequency pulsed-DC conditions, the fluctuation in current, temperature, and therefore stress is miniscule because of how quickly the current shifts on and off, thus not allowing sufficient time for a cooling or heating effect that would lead to such failure mechanisms.

Valuable future work pertaining to this study would be to successfully obtain an improved model accounting for plasticity in the model. Exploration in this realm has begun, though with some hurdles.

Finally, plasticity and current crowding trends in FEM studies of WCSP under AC conditions may also be useful in understanding those types of EM tests, as well.

8.2.1 Considerations on Creep Behavior in Pulsed-DC Conditions

The Anand visco-plasticity Model was developed in the 1980's and has commonly been deployed in plastic FEM studies of microelectronic packaging, specifically solder joints, subjected to creep and fatigue to estimate their lifetimes [46]. It does not employ any explicit yield conditions for loading-unloading criterion. The plastic strain in the model is determined by the current stress, internal state variables, and temperature. Anand's model assumes that plastic flow is expected to occur at all non-zero stress levels. The creep in an Anand model is described by a flow equation, where *Q, k, T, s, A, m, x, s* is the activation energy, Boltzmann's constant, absolute temperature, flow stress, pre-exponential factor, strain rate sensitivity, multiplier of stress, deformation resistance stress built-in as a state variable, respectively.

$$\frac{d\mathcal{E}_p}{dt} = A[\sinh\left(\frac{\xi\sigma}{s}\right)]^{\frac{1}{m}}\exp\left(\frac{-Q}{kT}\right) \qquad \textbf{[Eq. 27]}$$

The deformation resistance stress is evolved in the following three equations, which utilize Anand parameters, A, q, x, m, h0, Ŝ, n, a, and s0, provided in **Table 7**.

$$\frac{ds}{dt} = [h_0\left(|B|\right)^a\frac{B}{|B|})]\frac{d\mathcal{E}_p}{dt} \qquad \textbf{[Eq. 28]}$$

$$B = 1 - \frac{s}{s^*} \qquad \textbf{[Eq. 29]}$$

$$s^* = \hat{S}[\frac{1}{A}\frac{d\mathcal{E}_p}{dt}\exp\left(\frac{Q}{kT}\right)]^n \qquad \textbf{[Eq. 30]}$$

Table 7. Anand Model Material Constants for Sn3.8Ag0.7Cu									
	s_0 *(MPa)*	*Q/R* *(K)*	*A* (sec^{-1})	ξ	*m*	h_0 (MPa)	Ŝ (MPa)	*n*	*a*
Sn3.8Ag 0.7Cu	3.2992	9883	15.773	1.063	0.3686	1076.9	3.1505	0.0352	1.6832

Table 8. Anand Model variables for Sn3.8Ag0.7Cu [46].

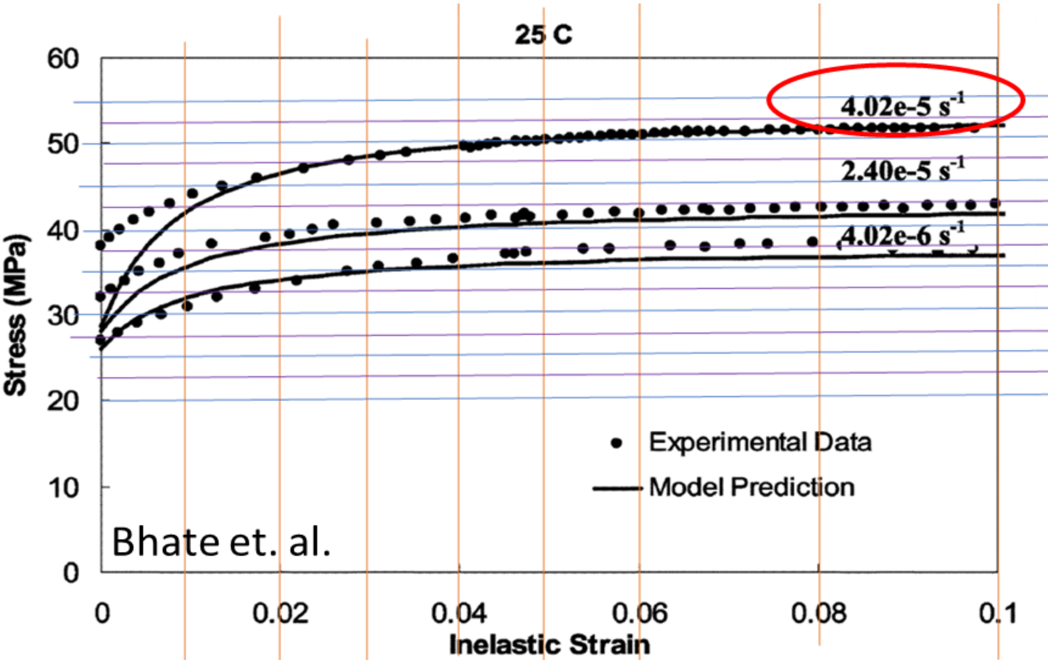

Figure 81 SAC387 yield stress vs. inelastic strain plot from which data is extracted [46].

Yield Stress (MPa)	Plastic Strain
37.5	0
43.75	0.01
46.25	0.02
47.5	0.03
49	0.04
50	0.05

Table 7 SAC387 yield stress vs plastic strain data extracted from literature [46].

However, ABAQUS/CAE does not support specifying this model. The proposed solution to this issue is by exporting inelastic strain-yield stress data from literature, taken at 25°C, and manually inputting the data into the ABAQUS/CAE material properties list. **Table 8** summarizes the plastic strain vs. yield stress data extracted from the plot presented by Bhate et. al. in **Figure 81** [46]. This is necessary for the plasticity model, in any case. One thing to note, however, is that the data collected in this study was done at a relatively low strain rate, but it is among the most descriptive data available to the SAC387 solder material. This is something to bear in mind, although the resulting plastic stress and strain outputs should still reveal a reliable trend. A simple plasticity model can be paired with this isothermal plasticity data with the Power Law, which is a creep model which considers the diffusion creep mechanism, most commonly used to predict the steady-state creep response of solder alloys. The Power Law is defined by **Eq. 31** where A and *n* are the power law multiplier and the exponent constants, respectively. Q is the activation energy; R is the universal gas constant; and T is the absolute temperature in K.

$$\dot{\varepsilon}_{cr} = A\sigma^{n} \exp\left(\frac{-Q}{RT}\right) \qquad \textbf{[Eq. 31]}$$

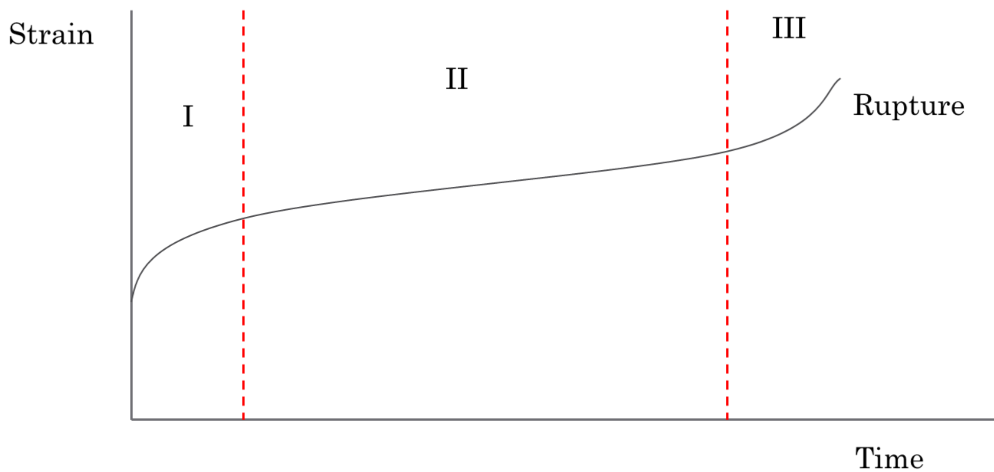

Figure 82 Strain vs. Time plot illustrating creep deformation, which is divided into three regions: I) primary creep with an initial rapid rate, which slows with time, II) secondary creep, which is steady state, and III) tertiary creep, which has an accelerated creep rate until it ruptures.

According to Wiese et. al., the power law multiplier, exponent, and activation energy for SAC387 as cast is 6E-23, 19, and 84.2, respectively. The power law multiplier, exponent, and activation for SAC387 after storing at 125°C for 24-1176 hours is 1E-12, 13, and 75.2, respectively [47].To obtain the desired outputs, the outputs in the step must be modified to include PEEQ in addition to plastic strain and plastic stress. Additionally, when setting up the step in the model, it must be directed to collect viscoelastic, swelling, and creep data throughout the simulation.

Because the Anand Model is not supported by ABAQUS/CAE, and we want to collect fatigue along with creep-related data, the Darveaux Model was also considered. In 2000, Darveaux adapted the Anand visco-plasticity model to illustrate the behavior in solder joints under high temperature and the degradation of solder joints as cracks initiate and propagate, which are both estimated using the Power Law. The Darveaux Model is thus also commonly used for FEM studies of microelectronic packages under thermal-electrical-structural cyclic stress conditions to simulate the creep and fatigue that may occur in the solder bumps [48-50]. It has been accepted by the scientific community and is estimated to achieve an estimated 25% of accuracy in its lifetime prediction capabilities. The Darveaux model involves both primary and secondary creep, as illustrated in **Figure 82**. Unfortunately, it, too, is not supported by ABAQUS/CAE.

This leaves the Double Power Law, which also is not supported by ABAQUS/CAE; however, we can define the Garafalo Sine-Hyperbolic Double Power Law with constants and variables defined by Schubert's Constitutive Model [51-53]. The Sine-Hyperbolic Double Power Law is presented by **Eq. 32**, where A is the power law multiplier, α is the hyperbolic sine multiplier, n is the equivalent stress order, and Q is the activation energy. The constants derived by Schubert et. al. is presented in **Table 9**. This is also well-suited for modeling the behavior of

solder alloys in electronic packaging which are subjected to creep and fatigue; however, it is not as common or well-known as the Anand Model.

$$\dot{\mathcal{E}} = A_1(sinh\alpha\sigma)^n exp(-\frac{Q}{RT}) \qquad \textbf{[Eq. 32]}$$

Solder	SAC 387 (Schubert et. al.)
Power Law Multiplier (A)	3.2E+4
Hyperbolic Sine Multiplier (α)	0.037
Equivalent Stress Order (n)	5.1E-6
Activation Energy (Q)	6.53E+4
Universal Gas Constant	8.314

Table 9 Schubert's Constitutive Model constants assigned to SAC387's material properties in ABAQUS/CAE [51].

More consideration and research is necessary to determine the best method to accounting for plasticity in thermal-electrical-structural FEM studies, particularly for this work where both fatigue and creep play a prominent role in EM failure kinetics.

8.2.2 Considerations on Fatigue Behavior in Pulsed-DC Conditions

One of the drawbacks for all the models suggested to account for creep is that they are suitable for just that: creep. Although some studies do use models like Darveaux and Anand for fatigue, they have limitations for cyclic loading, which is why the Oak Ridge National Laboratory Constitutive Model has also been taken into consideration. Generally, creep models for cyclic loading are complicated and must be added to a model, but ORNL's model simplifies this process because it can give approximate results without having to perform the cyclic loading numerically [54, 55]. The yield stress vs plastic strain parameter inputs for ORNL must be kinematic and cyclic

yield stress vs plastic strain must also be entered. One of the limitations with this model, however, is that it is commonly implemented for steel materials subjected to cyclic loading and cyclic thermal conditions. Therefore, while this model may be useful combined with the Sine-Hyperbolic Double Power Law and the plastic strain and yield stress material data inputs, it is important to be aware that the results may be a bit off from what would be expected.

Also considered, which is actually more traditional for thermal cycling, but not typically used for current stress is the Manson-Coffin relationship, given by **Eq. 33**, where the fatigue model parameters σ'_F, E, ε'_F, b, and c are material constants which are obtained from low cycle fatigue test data [5].

$$\frac{\Delta\varepsilon}{2} = \frac{\sigma'_F}{E}(2N)^b + \varepsilon'_F(2N)^c \qquad \textbf{[Eq. 33]}$$

The coefficient, c, and exponent m are both determined experimentally in the Coffin-Manson Equation, given by **Eq. 34**, which is used to estimate the fatigue life model for bulk solder joints.

$$N_f = c(\Delta\gamma_{in})^m \qquad \textbf{[Eq. 34]}$$

While the Manson-Coffin model it excellent for estimating fatigue life for thermal cycling, it is not relevant to this type of study for two reasons: 1) we are not interested in obtaining the number of cycles to failure, rather obtaining the plastic stress and strain information with cyclic stress caused by pulsed current and 2) the added complications from EM failure mechanisms make this type of model unreliable for properly estimating the behavior and lifespan of samples which fail by fatigue-assisted EM.

After this consideration, the methods discussed in section 8.2.1 appear to be the best options among those proposed so far to simulate the plastic stress and plastic strain in thermal-electrical-structural studies.

8.2.3 Current Challenges and Potential Future Setbacks

Thus far, obstacles in obtaining valuable results may be credited to two things: 1) Mesh and increment size limitations, and 2) shear stress outputs are possibly lower than necessary to obtain valuable plastic stress and plastic strain outputs under current boundary conditions. There is a limitation in the mesh size, increment size, and the large amount of time needed to calculate a much more complicated problem now that plasticity is involved. The outputs needed for a thorough analysis of material response to two failure mechanisms simultaneously adds to that complexity. The shear stress obtained in the model with the current constraints and boundary conditions potentially yields too low of a shear stress, possibly owing to the fact that the temperature diffusion from the core of the solder to the solder surface is not as efficient as is necessary to properly capture the physics, thus plastic stress and plastic strain is either too low or zero in recently attempted studies. This parameter is subject to change depending on how the heat conduction is modeled, and it is possible that defining the convection does not resolve this alone.

Future work may necessitate efforts in improving the models already developed to properly account for plasticity by improving the thermal conductivity definition in the model. Likely, this will require a supercomputer because of the size of the mesh and the increment sizes that appear to be required. The aforementioned barriers in setting up computational capabilities using ABAQUS will also pose as a potential barrier. Additionally, because a considerably refined mesh appears to be needed, completing a convergence study on this particular model would be beneficial.

8.3 POLYIMIDE OPENING SIZES IN WAFER-LEVEL CHIP SCALE PACKAGES AND THEIR FUNDAMENTAL EFFECTS ON ELECTROMIGRATION

The effects of PI layer opening diameters on WCSP reliability were studied to gain a prediction on which PI opening diameter is most beneficial to the EM reliability of solder interconnects in WCSPs. The particular aim is to predict which PI opening diameter provides the most benefit from compressive stress and controlled current crowding. WCSP samples with the PI layer and varying opening diameters are currently under investigation in EM experiments, so there is nothing published to compare these results with. However, based upon what we know from current flow configuration and UBM studies with WCSP models, we can estimate that the PI opening that has the best compressive stress and current density trends will likely be most beneficial to EM reliability.

Three PI opening diameters were studied: small, medium, and large, equating to 124 μm, 144 μm, and 160 μm, respectively. The WCSP PI opening models were designed with the same UBM thickness of 18 μm and the FEM boundary conditions matched those which WCSPs without PI layers were subjected to for comparability. Based upon the current crowding trends, and the level of compressive stress, both in the center of the DUT, the smallest PI opening is predicted to be most beneficial to EM reliability. With the smaller PI diameters, the current path is corrected early, allowing the current to mostly crowd toward the center of the DUT, where the void most likely would initiate after all the Cu from the UBM is consumed; however, the outer edges of the DUT are spared from current crowding, allowing a contact to be maintained in the outer realm of the DUT/UBM interface. Meanwhile, the WCSP models with the largest PI opening diameters are predicted to be least beneficial to EM reliability because the current is allowed to reach the outer

edges of the DUT, which may result in void formation at the outer edges in addition to the middle of the DUT/UBM interface. This could prove to be problematic and may accelerate EM failure kinetics.

Future work is warranted in exploring the PI opening behavior among WCSPs with thicker UBMs, especially those which are 35 μm-thick, as those proved to be most beneficial in the UBM thickness study.

8.3 SOLDER JOINT GEOMETRIES IN POWER-WAFER-LEVEL CHIP SCALE PACKAGES AND THEIR FUNDAMENTAL EFFECTS ON ELECTROMIGRATION

CAD models of power-level chip scale packages (PWCSP) have been created; however, due to the limited time, this has been excluded from this dissertation research. FEM of this model will be valuable supplemental evidence of the EM performance observed in samples tested under EM conditions, which is currently ongoing. PWCSPs are modified WCSPs in which solder interconnects will theoretically be capable of carrying a greater magnitude of current density. The two DUTs in the PWCSP which are compared each have a square solder joint with a 1:2 and a 1:3 rectangular ratio, respectively. Compared to the WCSP solder joint's height of 230 μm, the PWCSP solder joint's height is 75 μm, as depicted in **Fig. 83. (a).** As for the small rectangular

PWCSP solder joints, they are depicted in **Fig. 83 (c)**, and are 230 μm wide, 460 μm long, and 75 μm tall. The large rectangular PWCSP solder joints are 230 μm wide, 690 μm long, and 75 μm

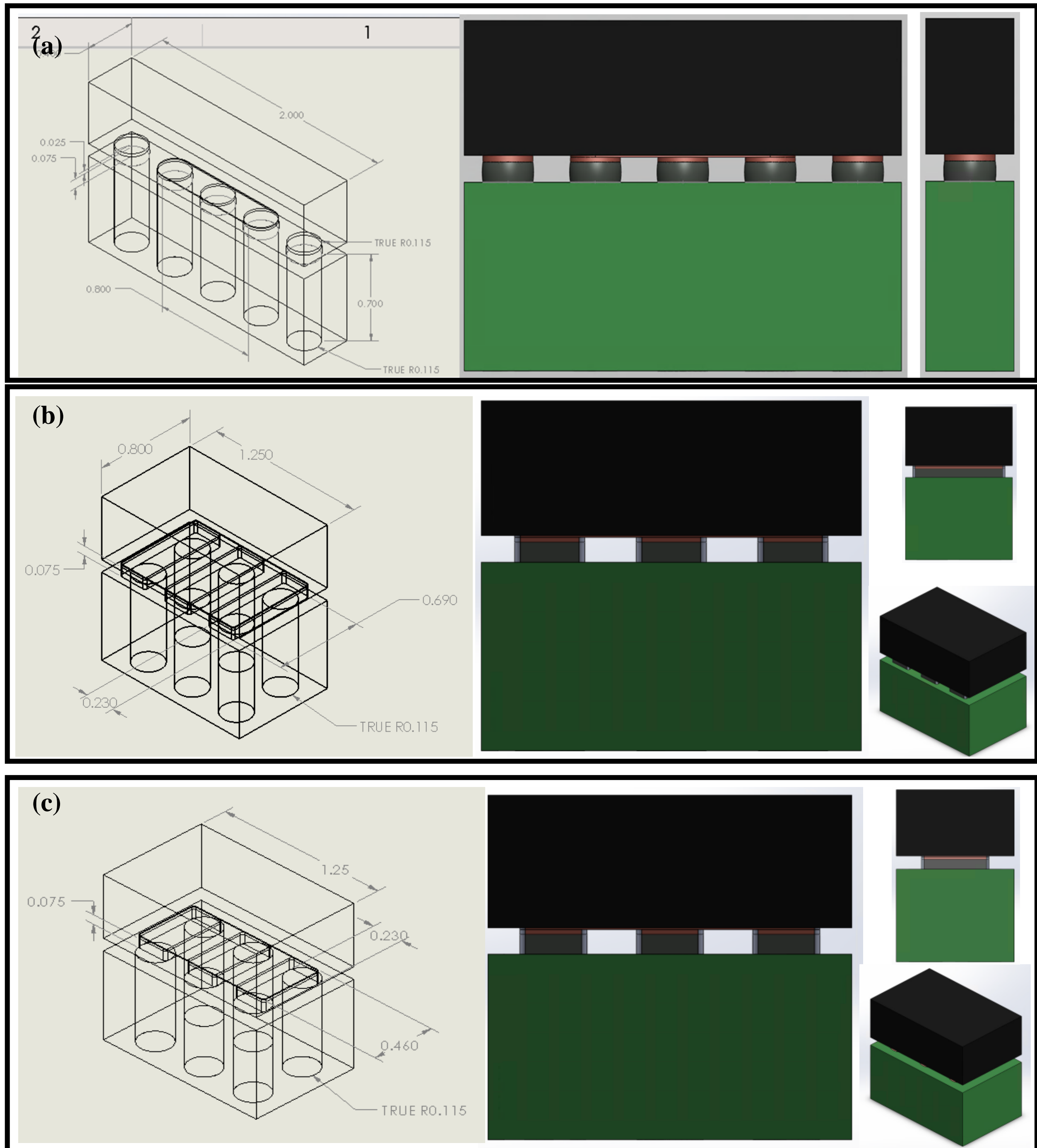

Figure 83 SolidWorks models for **(a)** PWCSP round solder joint, **(b)** PWCSP for large rectangular solder joint, and **(c)** PWCSP for small rectangular solder joint. of various PI opening diameters in WCSP. Three models have been created for each PI

tall, as illustrated in **Fig. 83 (b)**. For all of the PWCSP solder joints presented in **Figure 83**, the UBM thickness is 18μm, but 35 μm and 50 μm should also be investigated.

Table 10. PWCSP FEM Testing Matrix				
Structure	**DUT (75 μm tall)**	**Temperature (°C)**	**Current (A)**	**Current Density (kA/cm^2)**
18C	Round	165	4	9.63
35C	Round	165	4	9.63
50C	Round	165	4	9.63
18C	Small Rectangular	165	7.5	7.09
18C	Small Rectangular	165	8	7.56
35C	Small Rectangular	165	7.5	7.09
35C	Small Rectangular	165	8	7.56
50C	Small Rectangular	165	7.5	7.09
50C	Small Rectangular	165	8	7.56
18C	Large Rectangular	165	9.6	6.05
18C	Large Rectangular	165	7.6	4.79
35C	Large Rectangular	165	9.6	6.05
35C	Large Rectangular	165	7.6	4.79
50C	Large Rectangular	165	9.6	6.05
50C	Large Rectangular	165	7.6	4.79

Table 10 Proposed future FEM study matrix of PWCSP models.

The experimental research which is applicable to this FEM study is ongoing; however, it is predicted that the rectangular PWCSP solder joints should result in a greater distribution of

current crowding at the SAC/UBM interface due to a greater contact area between the Cu vias and the SAC solder joints in rectangular PWCSP solder joints compared to the WCSP solder joints. All round and rectangular solder joints have a greater UBM:SAC aspect ratio in PWCSP solder joints than the round solder joints used in WCSP, which is predicted to improve the current crowding distribution. Further, a shorter solder height is predicted to increase the degree of compressive stress. This is predicted because a shorter amount of material limits the dislocation gliding path, inhibiting the capability for the material to relieve the stress accumulated due to the CTE mismatch and JH. However, due to the increased UBM:SAC aspect ratio, the effects of this CTE mismatch may be mitigated depending on the UBM thickness, as confirmed in Chapter 5.

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Biographical Information

Allison Theresa Osmanson earned her B.S. in Materials Science and Engineering from Washington State University in Pullman, WA in 2016. She later earned her M.S. under the direction of Dr. Witold Brostow in Materials Science and Engineering from the University of North Texas in Denton, TX in 2018. There, she also taught introductory engineering physics laboratories and mentored TAMs and undergraduate students. Subsequently, Allison joined Dr. Choong-Un Kim's Electronic Materials Laboratory at the University of Texas at Arlington in Arlington, TX in Fall 2018 to pursue her PhD in Materials Science and Engineering. There, she became a recipient of the Texas Instruments/SRC Company-Named Fellowship, with which she was awarded in 2019.

Throughout her studies, Allison has gained research experience in multiple areas including polymers, energy storage, shape memory alloys, metallurgy, tribology, affordable point-of-care biosensor technology, and electronic materials. Consequently, Allison's research emphasis, under the direction of Dr. Choong-Un Kim, has shifted to electronic materials and interconnect reliability of semiconductor packaging. Under Dr. Kim's supervision, Allison has worked with a team on multiple projects related to electromigration (EM) reliability in metal interconnects. In addition to usual experimental investigation techniques, Allison uses finite element method (FEM) for complimentary understanding of mechanical effects caused by semiconductor package designs on EM failure kinetics. The last 1.5 years of Allison's PhD research have been devoted to FEM.

Allison has held internship positions at Texas Instruments (Packaging Engineering Intern, 2020) and the US Army Research Laboratory (UCEP Materials Science/Tribology Intern, 2018). Beginning December 2021, she will be a Packaging Engineer at Texas Instruments in Dallas, Texas.