The Effects of SnAgCu Solder Interconnect Package's Parameters on Electromigration Failure Mechanisms

By

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Abstract

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The primary concern of this dissertation is the electromigration (EM) failure mechanism found in Sn-Ag-Cu (SAC) solder alloys integrated in WCSP (wafer-level chip scale package) packaging structure and factors affecting the failure mechanisms. To the end, accelerated electromigration (EM) tests are conducted on SnAgCu (SAC) solder interconnects in wafer-level chip scale packages (WCSPs or WLCSPs) with different package structures and use-condition parameters. The package structure parameters include different under bump metallization (UBM) thicknesses, Sn grain orientation, while the various in use conditions includes pulsed direct current (DC), and alternating current (AC). The major findings made in the studies are presented in separate chapters outlined as below.

In Chapter 2, the effects of the UBM thickness on the EM reliability of SAC solder joints are studied and presented. One of the highlighting findings of this study is a discovery of a hidden mechanism controlling the EM failure mechanism occurs with the classical EM failure mechanism. The hidden EM failure mechanism is suggested based on the observation that the EM resistance does not show a linear increase with UBM

thickness. Nor does the EM reliability become saturated after a critical UBM thickness. Instead, the EM reliability decreases above a certain critical limit in the UBM thickness. Since a thicker UBM has a greater amount of Cu supply, the observation contradicts the conventional view on the role of UBM that prolongs EM failure. The initial hypothesized explanation to this finding is that the increased exposure of fast EM diffusion Sn grain orientation or weak-links at the Cu UBM and SAC interface as UBM gets thicker. This is based on a more evenly distributed EM flux across the interface by reducing current crowding effect at the corners of the interconnect. However, a comparative EM study by switching the current flow configuration to reduce the current crowding effect yielded results that disagree with this proposition. It is found that the impact of the level of current crowding on EM reliability does not differ much with different the UBM thickness. This defies the initial speculation that there would be a smaller improvement in EM reliability in thicker UBM samples when the current configuration is switched. These results suggest that the UBM thickness affects the EM failure mechanism in a more complicated manner. Considering hidden factors such as the compressive stress that acts against the growth of the EM void is necessary in order to better understand the mechanism.

Chapter 3 presents the effects of Sn's grain orientation on EM failure kinetics. Comprehensive studies of EM reliability of solder interconnects have suggested that early EM failure may have different failure kinetics depending on the grain orientation of Sn within the solder bump. The Sn has anisotropic properties because of its body centered tetragonal (BCT) crystal structure. Sn has a fast EM diffusion at a grain orientation of [001] or along c-axis due to its relatively larger diffusion path compared to other orientations. Both early failures and late failures from the same accelerated EM tests are characterized

with scanning electron microscopy (SEM) and electron backscattered diffraction (EBSD) to study a relationship between early EM failure and Sn grain orientation. SEM analysis does not show distinctive microstructure differences between early and late failure features. EBSD analysis shows a distinctive feature of Sn grain orientation. The early failures have a high concentration of Sn's c-axis alignment with the EM current direction, while the late failures have less or no c-axis alignment of the Sn grain orientations. The failure analysis suggests that the c-axis alignment with the EM current direction near the Cu and SAC interface accelerates the EM failure kinetics, causing early EM failures. The early failures are detrimental to reliability assessments as they skew test data.

Chapter 4 reports a simple way to mitigate the early EM failures using a substrate effect that induces a biased nucleation of Sn grain orientations. Since the Sn's c-axis alignment accelerates the EM kinetics and causes early EM failures, the utilization of the substrate effect is chosen to give preferred reflowed Sn grain orientations. The various sizes of SAC solder balls ranging from 200μm to 760μm are reflowed on polycrystalline Cu substrates and (111), (110), and (100) textured single crystal Cu substrates. The EBSD analysis of reflowed SAC solder balls reveals that a substrate effect is a simple and effective way to mitigate Sn grain orientation effects on EM reliability. The EBSD analysis and key findings are presented and discussed in this chapter.

Chapter 5 discusses the effects of non-DC load on EM failure mechanism, kinetics, and microstructure are studied using low frequency pulsed-DC. This study is conducted because the understanding of non-DC effects is significantly lacking because of difficulty of setting up tests. The failure kinetics of non-DC conditions were expected to follow a cumulative model, which only accounts EM damage during the "on" time. The accelerated

EM tests of WCSP samples are conducted under 4 different low frequency pulsed-DC conditions: 0.1Hz pulsed-DC with duty factors (DFs) of 33%, 50%, 75%, and 100% (DC). The EM failure kinetics shows a highly nonlinear relationship with the DF. The result of EM test suggests that there are at least two competing factors affecting the EM failure kinetics in an opposite manner under low frequency pulsed-DC EM conditions. Specifically, the failure kinetics are accelerated at high DF and decelerated at low DF. The resistance change data with a 2-stage EM failure further supports two EM acceleration and deceleration failure mechanisms. Failure analysis finds a new observation of unique failure mode involving three mechanisms in SAC solder interconnects subjected to low frequency pulsed-DC conditions: 1) EM, 2) temperature fluctuation-induced mechanical fatigue, and 3) dynamic recrystallization. The two mechanisms, the classical EM mechanism and a secondary EM acceleration mechanism, contribute to failure in tandem, a phenomenon which has not been observed in the past. A unique observation of these two mechanisms is that thermal fatigue accelerates EM failure kinetics. Evidence of fatigue crack formation and growth across the solder joint along with fluctuating temperature and stress with pulsing “on” and “off” current obtained through cross-sectional failure analysis of failed samples and a finite element method (FEM) model, respectively. The low DF samples have exponentially increased EM lifetime, suggesting EM failure deceleration mechanism unlike high DF pulsed-DC samples. The squeeze-out SAC solder deformation indicates an involvement of dynamic recrystallization that causes superplasticity. The dynamic recrystallization decelerates EM failure kinetics by removing fast EM diffusing grain orientation and reducing work

hardening of SAC. The fine grain sizes of SAC under EBSD further support the dynamic recrystallization of SAC solder.

Chapter 6 presents the effect of alternating current load condition on EM mechanism because low-frequency pulsed-DC has effects on EM mechanisms which are far too complicated, such as thermal-mechanical fatigue and dynamic recrystallization. Comparative AC EM tests with varying frequencies and DFs are conducted to remove the complicated thermal fluctuation. The common assumptions of AC effects on EM are that samples fails with the classical EM failure mechanism with its failure microstructures with an effect of material healing or recovery. Based on the damage recovery model, the higher-frequency AC would fail slower than lower-frequency AC would do because higher-frequency AC has more effective EM healing effects. However, the accelerated AC EM tests reveal that the samples under high-frequency AC fail faster than those under low-frequency AC. Furthermore, the IMCs of failed samples tested under AC completely differ from classical EM-induced IMC formation, which is Cu_6Sn_5 and Cu_3Sn near the anode side of interconnects. The IMCs are formed in the middle of the solder interconnects. The faster failure rate of high-frequency AC and the abnormal IMC microstructure suggest two things. First, the assumed healing effects are not as extensive as assumed. Second, the IMC formation and dissolution are not spontaneous, as assumed, but have different rates.

Acknowledgement

I want to thank my supervising professor, Dr. Choong-Un Kim, for guiding me through the doctoral program with various constructive criticisms. I was able to learn various knowledge and wisdom in engineering, work ethics, and dedication. I want to thank my fellow doctoral colleagues, Hossein Madanipour, Geng Ni, Allison Teresa Osmanson, and Mohsen Tajedini, and many masters and undergraduate students for their collaborations in this research. I want to thank Characterization Center for Materials & Biology (CCMB) staffs for training me to use various equipment for characterizations of samples. Lastly, I want to thank Semiconductor Research Corporation (SRC) and Texas Instruments Inc. for their supports and collaborations. The projects are funded by SRC under GRC Task ID: 2789.001 and 2949.001.

Dedication

First, I thank God for guiding and encouraging me throughout the doctoral path. He led me by introducing various people, and opportunities. I want to thank my girlfriend who became wife, HyonJi, for supporting me and being there for me. I want to thank and wish a long life for our rescued dog, Indy, for cheering me by bothering me to play with him.

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Chapter 1
Introduction

1.1. Research Overview

This research investigates the electromigration (EM) failure mechanisms and kinetics in lead-free SnAgCu (SAC) solder-based interconnects with various packaging parameters and current load conditions in an effort to establish a better EM reliability prediction model that can account for any overlooked or assumed EM failure mechanisms. In this research, a series of comparative EM tests is conducted to investigate the effects of various package parameter changes on EM failure mechanisms and kinetics. The first parameter is the under bump metallization (UBM) layer thickness with three different thicknesses, 18μm, 35μm, and 50μm. The second parameter is the direct current (DC) flow configuration by switching between symmetrical and asymmetrical current flow configurations, causing symmetrical or asymmetrical current crowding regions, respectively. The third parameter is different Cu substrates and their effects on SAC solder microstructure, especially grain orientation. The fourth parameter is the non-DC EM current load condition, such as pulsed-DC and alternating current (AC). The main goals to achieve are: 1) to have a better understanding of the EM failure mechanisms and kinetics under various parameters, 2) to identify any overlooked and new EM failure mechanisms resulted from various parameter changes, and 3) to help develop a direction in developing package design rules to enhance the EM reliability of electronic packages.

1.2. Research Motivation and Objectives

This research is primarily motivated by the increasing vulnerability of aggressively shrinking microelectronic packages to EM. This threat continues as the microelectronic packages and their interconnects are designed to be smaller to meet the demands of smaller devices with smaller form factors and higher performance and current-carrying capabilities. The smaller interconnects are inherently exposed to higher current densities due to their reduced cross-sectional areas and are thus more vulnerable to EM-induced failures. To understand the failure mechanism and thus to increase EM reliability of packages, numerous accelerated EM studies have been conducted over the past several decades on various packages under various testing conditions. However, many EM contributing factors complicate the full and accurate understanding of the EM failure mechanisms and kinetics that enable an accurate EM reliability prediction. Better understandings on the mechanism from these studies would enable engineers to have a robust reliability prediction model that is backed by well understood EM mechanisms and kinetics. The model gives an accurate assessment of a package's reliability, reducing cost and time for developing a specific package design.

The main objective of this project is to study the EM failure mechanisms and kinetics of SAC solder interconnects inside a flip-chip wafer-level chip scale package (WCSP or WLCSP). The accelerated EM experiments are designed and conducted to study the effects on EM failure mechanisms, kinetics, and microstructural changes. The EM experiments have various test temperatures and current densities of the same samples to construct an EM reliability prediction model. The same tested temperatures and current densities are applied to samples with differently configured parameters to

study the effects of each parameter on EM mechanisms and kinetics. An extensive amount of failure analysis is performed on the EM tested samples to study macrostructural changes, microstructural changes, and EM failure modes as an effort to explain test data and failure phenomena observed during the accelerated EM tests.

1.3. Research Flow

The research effort is roughly divided to give a general overview of the research flow. Literature reviews are done throughout the entire research duration. In the first year, two existing EM test systems are maintained and modified to have an additional ability to conduct EM tests with an oil-medium cooling system instead of an air-medium cooling system. While conducting accelerated EM tests, three new EM test systems are built over the first two years to increase the EM test capacity from testing 400 samples to testing 1000 samples concurrently. The first part of the first phase of EM tests began by conducting a comparative test to investigate the effects of the UBM layer thickness and an Ni diffusion barrier layer on the UBM. In the second year, the study of current flow configuration begins to further investigate the test data of UBM layer thickness to suggest an EM failure mechanism. In the same year, the constant current pulsed DC generating module is designed and produced to start the study of the pulsed DC effect. In the third year, the study of the current flow configuration effect is done. The UBM thickness effect, Ni barrier layer on UBM effect, and pulsed DC effect are continued with remaining test matrix. In the fourth year, the second phase of EM test began with new additional samples with different sets of parameters. The comparative study of AC effect started to study the pulsed DC effect without a complicated thermal fluctuation. WCSPs with different PI opening sizes are also studied for their comparative understanding of the effects of

varying current densities flowing through the PI opening. The new WCSP configuration for a power specific application is studied. The power WCSP (PWCSP) has two rectangular shaped solder interconnects with different ratios. It also has wider, yet shorter SAC solder interconnects compared to those of WCSP. In the fifth year, the early EM failures are investigated with an effort to prevent early EM failures caused by Sn's c-axis alignments. The various sized SAC solder balls are reflowed on different Cu substrates, ranging from polycrystalline to textured single crystal.

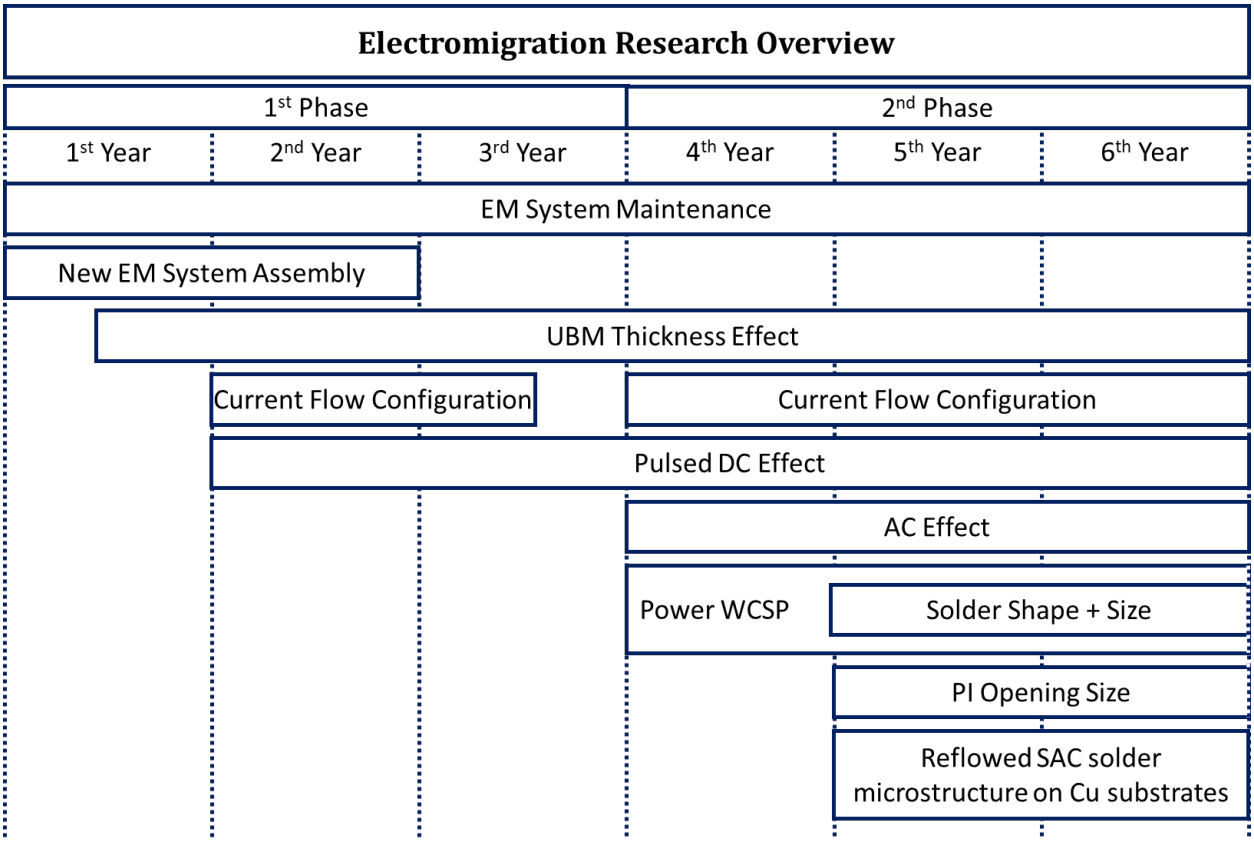


Figure 1-1. The timeline of the electromigration research. The box with dotted edge indicates a continuity of research, such as Power WCSP and PI Opening Size.

1.4. Literature Review

There are four major material migrations that can happen with various factors within a solid body. The first is a thermomigration by temperature gradient within a solid

body. The second is a chemical migration by chemical concentration gradient within a solid body. The third is a stress migration that is caused from a stress gradient. The fourth is an EM from an electric field. All these material migration mechanisms have the potential to cause failure. However, the EM becomes a major reliability concern as devices get aggressively smaller and the current density of solder interconnects approaches and exceed 10kA/cm^2 [1]–[6].

EM happens when current flows within a conductor, generating two forces that affect metal ions within a solid body. The first is an electrostatic force, F_{field}, which is also known as a Coulomb force or Coulomb interaction. It is an interactive force that repulses or attracts two electrically charged objects. The electrostatic force from a current flow is in the same direction as the electric field. However, since the negative charged electrons shield the positive metal ions, the electrostatic force can be safely ignored. The second is an electron wind force, F_{wind}, which is also known as an ion wind. It is caused by the momentum exchange between electrons and metal ions. The electron wind force pushes metal ions with the flow of electrons, causing the electron wind force to act in the opposite

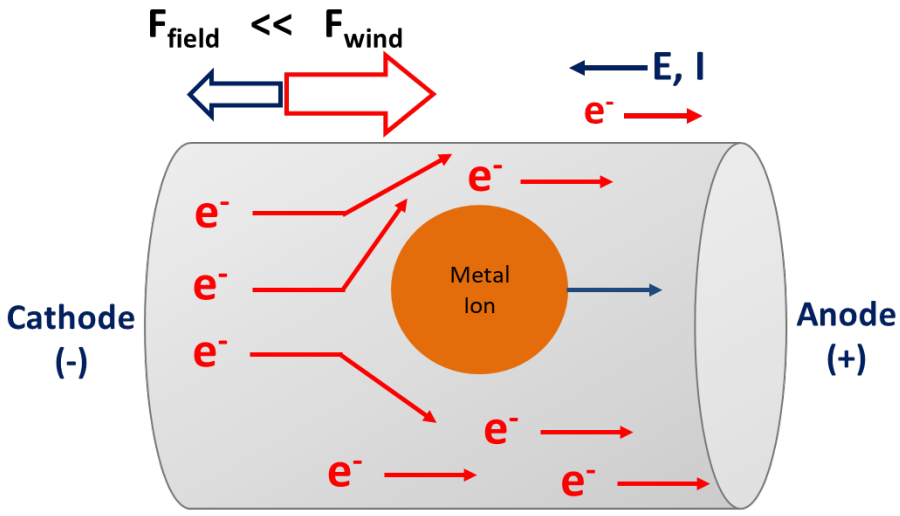


Figure 1-2. Illustration of electron wind force and electrostatic force within a conductor.

direction of the electric field. The amount of electron wind force can be massive. Once the electron wind force exceeds the activation energy, E_a, then an EM-induced atomic diffusion process begins, causing metal ion migration in the direction of electron movement, which is from the cathode (-) to the anode (+) [7]. Fig. 1-2 illustrates the electrostatic force and electron wind force within a conductor.

1.4.1. EM Failure by Current Crowding

The solder interconnect's design causes a current crowding region at the interface between the Cu UBM and the SAC solder bump. Since the cross-section of the Cu path is about two orders of magnitude smaller than that of the SAC solder bump, the changes in the current direction and the current density lead to current crowding [3]–[6], [8]–[12]. The current crowding region has an excessively higher local current density than the average current density throughout the interconnect. The combination of higher current density and local temperature further accelerates the local atomic diffusion, causing the interface of the UBM and SAC solder bump to become a weak point in the package when subjected to EM. Therefore, the accelerated EM kinetics lead to the nucleation of a void first at the current crowding region, after which the EM kinetics propagate the void across the entire interface.

1.4.2. Classical EM Failure Mechanism in Solder Interconnects

If solder interconnects have homogeneous diffusion at every location, then there would be no vacancy formation that causes void nucleation because the speed of material removal and replenishment is the same. However, microelectronic package's interconnects consist of various materials, causing an inhomogeneous diffusion. The EM flux divergency creates vacancies at inhomogeneous regions [3], [5], [6], [8], [13]–[15].

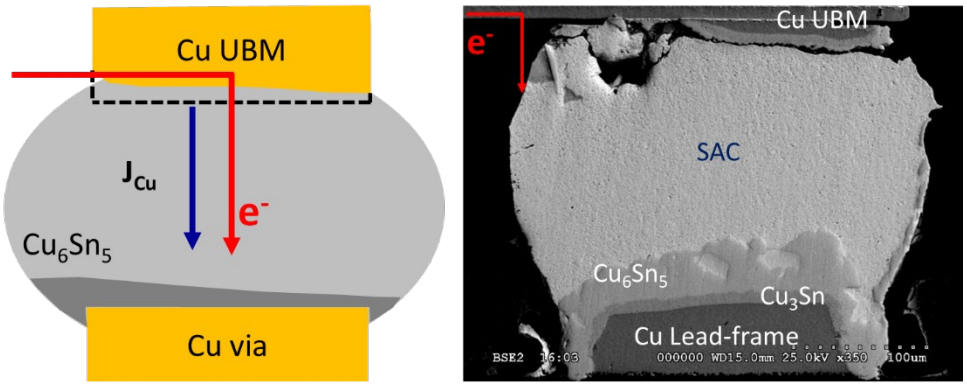


Figure 1-3. (a) Schematics of the conventional EM failure mechanism. (b) SEM image of a sample with EM-induced failure.

When vacancies are saturated in the EM flux divergence region, the void nucleates. With a constant current load, the reduced current path area increases current density, which increases Joule heating (JH) and temperature. The increased JH and current density further accelerate the speed of diffusion, increasing the rate of void propagation. Once the void reaches a critical length, the void propagates rapidly, exponentially increasing the resistance until catastrophic failure finally occurs. This resistance change behavior is called a conventional EM runaway failure. This void nucleation and void propagation are part of the classical EM failure mechanism of solder joints subjected to DC conditions. Here, the interface of the UBM and the SAC solder ball is a plane of atomic flux divergence; Cu diffusion in Sn is faster than Cu diffusion in Cu [4]. As shown in Fig. 1-3 (a), the Cu diffuses first at the current crowding region due to a higher local EM flux divergence, leaving Sn intact because Cu has a lower activation energy.

Cu diffusion in Sn has an activation energy of around 0.79eV, while Sn self-diffusion has an activation energy around 0.96eV [7], [16], [17]. The diffused Cu from the cathode end of the solder joint forms an intermetallic compound (IMC) at the anode end of the solder joint in the form of Cu_6Sn_5. As more Cu diffuses, the concentration of Cu at

the anode near the Cu via increases and forms the Cu_3Sn IMC. The SEM image of a sample with EM-induced failure show both Cu_6Sn_5 and Cu_3Sn IMCs in Fig. 1-3 (b).

Some inhomogeneities that cause inhomogeneous diffusion are the JH, the coefficient of thermal expansion (CTE) mismatch driven stress gradient, the geometry of the package, multiple diffusing species from changes in layers, the presence of a chemical gradient, the interfacial microstructure, the rate of interfacial reaction that leads to the development of an intermetallic compound (IMC), and many other factors [1]–[3], [5], [7], [18], [19]. These inhomogeneities cause EM-induced diffusion flow divergence which is also known as EM flux divergence. The imbalanced accumulations or depletions of materials within an interconnect cause voids, hillocks, or whiskers.

Due to the many EM-affecting factors, the development of an EM reliability prediction model is very complicated and often uses aggressive assumptions to reduce a number of contributing factors. The famous Black's equation illustrates the key parameters that determined the EM failure rate back in the 1960s [20]. The equation shows that the EM flux is proportional to the current density. Black's equation is widely accepted and used throughout the microelectronics industry to predict EM reliability. Black first introduced the empirical EM mean time to failure (MTTF) equation based on a thin film under DC conditions [20]. The Black's equation is as follows:

$$\mathrm{MTTF} = \frac{A}{j^n} e^{\frac{Q}{k_b T}} \tag{1-1}$$

where A is a constant, j is the current density, n is the current exponent, Q is the activation energy, k_b is the Boltzmann's constant, and T is the temperature in Kelvins. Since Black's equation is based on a thin film study, its predictive model cannot be generally applied to all the packages with different parameters, such as UBM thickness, UBM layer

components, polyimide (PI) opening size, current load conditions, Sn grain orientations, different surface finishing, LF thickness, solder ball height, pitch size, and more.

Another important factor for EM is JH. JH is a physical effect when the current passes through a conductor and generates thermal energy, resulting in an increase in the conductor's temperature. In other words, the electric energy is converted to thermal energy due to the resistance of a conductor. The JH follows the Joule-Lenz law which can be written as the following:

$$P \propto I^2 R \tag{1-2}$$

where P represents the power of thermal energy, I is the current, and R is the resistance of the conductor. As illustrated in equation (1-1), the increased temperature from JH would accelerate failure by EM; therefore, it is important to consider JH as one of the major contributing factors determining the EM failure kinetics and mechanisms.

1.4.3. EM Failure by Hillocks and Whiskers Growth

The growth of hillocks and whiskers is a failure mode of EM. As shown in the SEM images presented in Fig. 1-4, the hillocks can cause a delamination or a crack within the dielectric layer, and whiskers can cause an electric arc and a short-circuit failure [3], [5], [21], [22]. Whiskering is a crystalline metallurgical phenomenon that causes a spontaneous growth of tiny metallic hairs from a surface as high as 0.64 mm with a single crystal structure [3], [21], [22]. The internal compressive stress and external stress cause whisker growth. Whiskering does not cause deterioration of solderability or Sn coating, but the longer whiskers can cause a short-circuit failure. Therefore, a careful selection of the passivation layer on interconnect surfaces would increase the EM resistance

regarding a formation of hillocks and whiskers [13]. Fig. 1-5 illustrates different grain boundaries that form hillocks and whiskers.

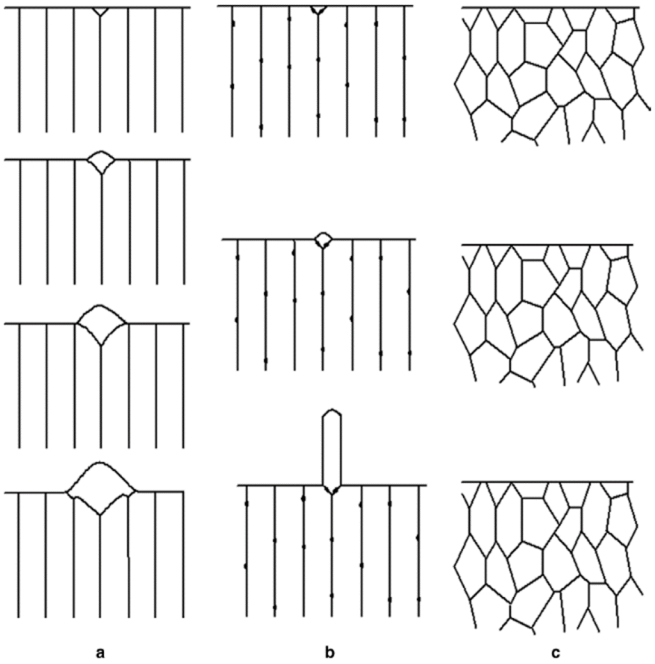


Figure 1-4. Illustrations of (a) hillocks formation where grain boundaries are mobile, (b) whiskers formation where grain boundaries are pinned, and (c) no extrusions with noncolumnar grain boundaries [22].

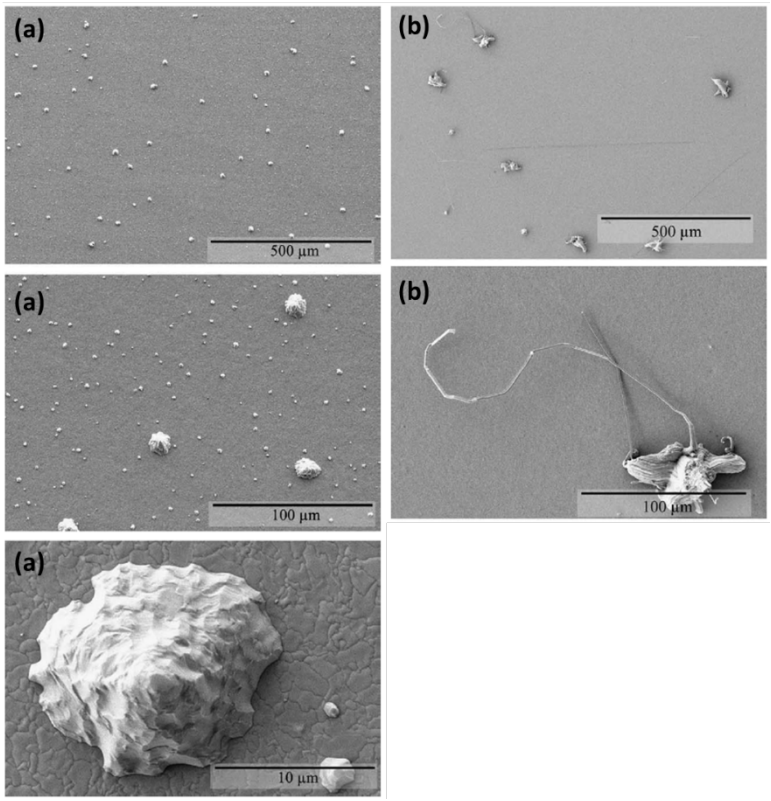


Figure 1-5. SEM images of (a) hillocks and (b) whiskers [22].

1.5. Samples Selection

Wafer-level chip scale packages (WCSPs or WLCSPs) are selected for accelerated EM testing. A WCSP consists of a 400μm pitch 5x5 SAC solder ball grid array (BGA) without underfill. A Cu under bump metallization (UBM) with various thicknesses typically lies between the Cu redistribution layer (RDL) on the Si substrate and the 230μm tall SnAgCu (SAC) solder alloy bumps. These solder bumps are bonded to Cu pads which cap the Cu vias in a printed circuit board (PCB), through which current is routed for EM testing. The advantage of the WCSP is the relatively larger SAC solder bumps which make studying EM failure mechanisms and metallurgical factors affecting EM failure mechanisms easier [23]–[25]. Si die itself from WCSP has a well-defined and isotropic coefficient of thermal expansion (CTE). But when the Si die is attached to a PCB substrate in a flip-chip assembly, then other stresses are needed to be considered. The linear shear stress is caused by the CTE mismatch between the Si and the PCB. The tension and compression are caused from component warpage. The combination of smaller pitch, relatively larger body size, and multiple stresses cause the WCSP to be the one of the worst EM resistant structures and instead cause them to be more prone to stress-assisted failures [5]. Fig. 1-6 shows the schematic of a WCSP, showing the Si wafer, the 5x5 SAC

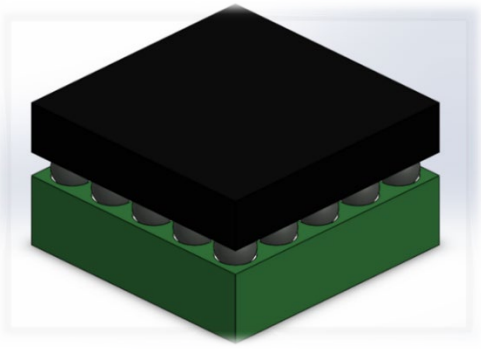


Figure 1-6. Schematics of wafer-level chip scale package (WCSP).

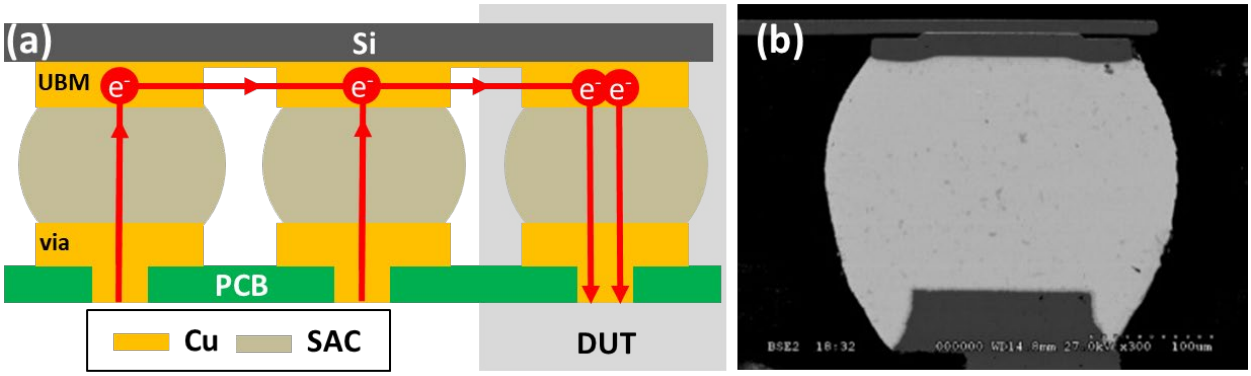


Figure 1-7. (a) Schematics of test current flow configurations. (b) Cross-sectional scanning electron microscopy (SEM) image of device under test (DUT) with backscattered electron (BSE) image mode.

solder BGA, band the PCB. The asymmetrical current flow configuration is shown in Fig. 1-7 (a). The right-most bump is the device under test (DUT) that is studied. The current flow configuration exposes the DUT to the highest current density, ensuring the first failure within the DUT rather than the other solder bumps in the circuit. As shown in Fig. 1-7 (a), the current starts to flow from the DUT and exits through the two supporting bumps. In other words, the electron wind causes atomic mass transportation from the top of the DUT, near the UBM, to the bottom of the DUT, near the Cu via. Fig. 1-7 (b) shows the cross-sectional scanning electron microscopy (SEM) image of an as-received sample in backscattered electron (BSE) mode. The SEM image shows SAC alloy and Cu components, namely the UBM and via. The cross-sectional area of the UBM is significantly thicker than that of Cu trace, developing a current crowding region at the corner of the UBM [3], [12]. Due to a higher local current density from current crowding, the void nucleates at a corner of the UBM/SAC interface first, then propagates to the other end of the interface. The current crowding region induces the classical EM voiding and void propagation

The various samples with different packaging parameters are prepared to study their effects on EM failure mechanisms, kinetics, and microstructures. The first set of

samples has different UBM thicknesses of 18μm, 35μm, and 50μm. The second set of samples has different thickness of Ni and Pd layers as UBM barrier layer. The third set of samples has different PI opening sizes: small, medium, and large. The different WCSP for power application is added with a name of power WCSP (PWCSP). PWCSP has two different rectangular solder bump geometries, one with 2:1 ratio and another with 3:1 ratio. Furthermore, PWCSP has about 75μm tall SAC solder bumps compared to the 230μm tall SAC solder bumps in the WCSP. The combination of high solder geometry ratio and the shorter height of solder bumps of PWCSPs would cause a greater degree of compressive stress development because the smaller surface has difficulty in dislocation gliding to relieve stress.

1.6. Accelerated Electromigration Test Setup and Test Procedure

Fig. 1-8 shows the EM systems which were designed and built in-house to allow the conduction of accelerated EM tests. The five racks of the accelerated EM test system,

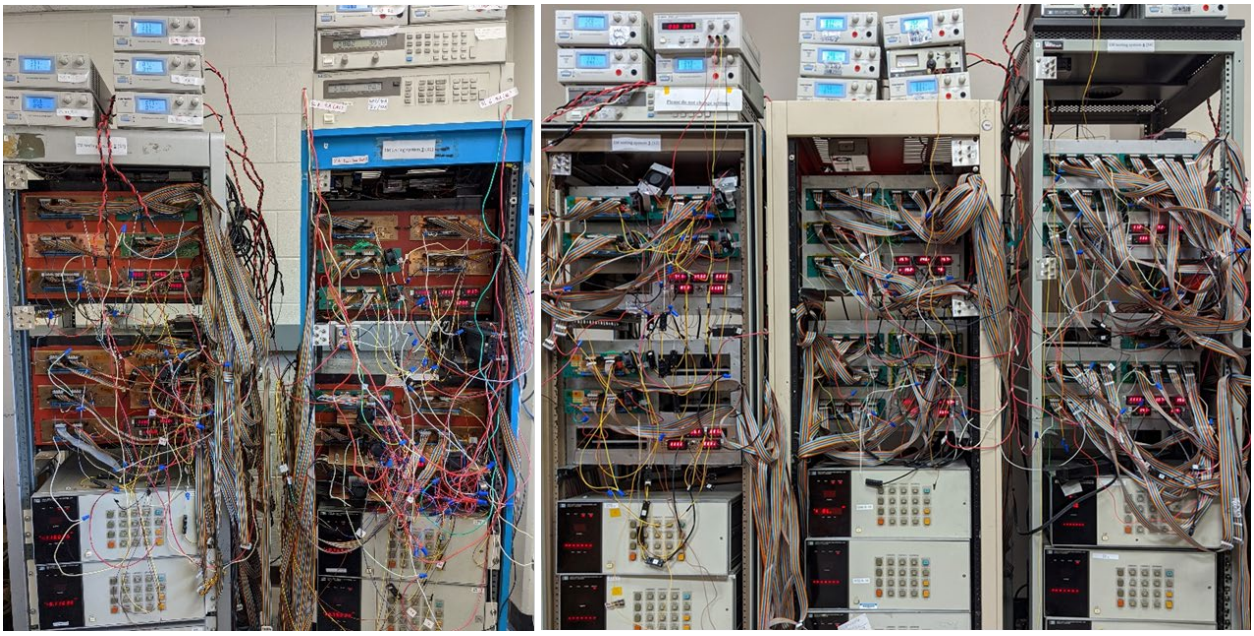


Figure 1-8. The five racks of the accelerated EM test system that can test 1,000 samples simultaneously.

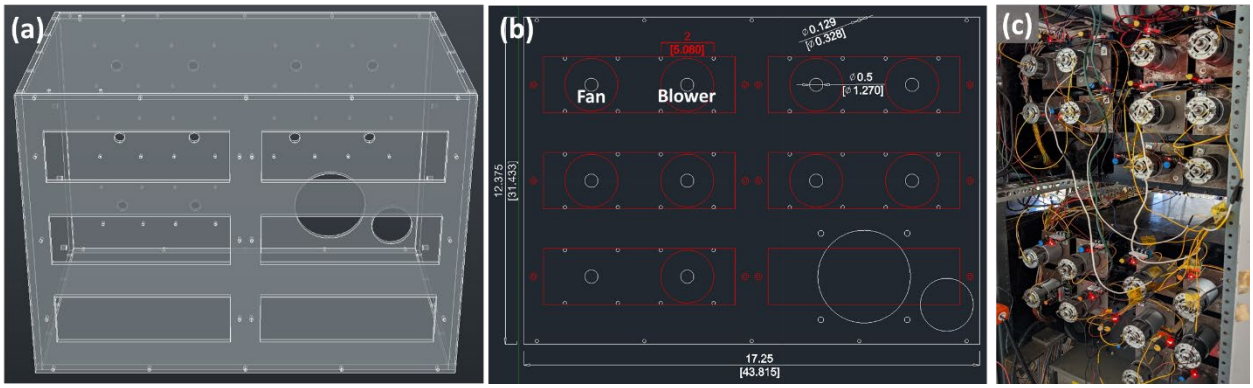


Figure 1-9. (a) Front CAD view of the modified EM oven in 3-D. (b) Back CAD view of the modified oven in 2-D. (c) The actual view of the back of the accelerated EM test oven.

which have a total of ten testing ovens, are used simultaneously to test up to 1,000 samples concurrently. Each oven has five individual slots that have individual cooling systems and heating elements for setting a test temperature. The old system only had one fan for a forced convection cooling, but the level of cooling was not enough. As shown in Fig. 1-9 (b) and (c), the additional fan is added to the oven slot to enhance the cooling to have an effective JH dissipation and a uniformity of temperature within an oven slot. The standard accelerated EM test consists of 20 serially connected samples mounted on a test structure per one test leg. The test structure from Fig. 1-10 was designed in house

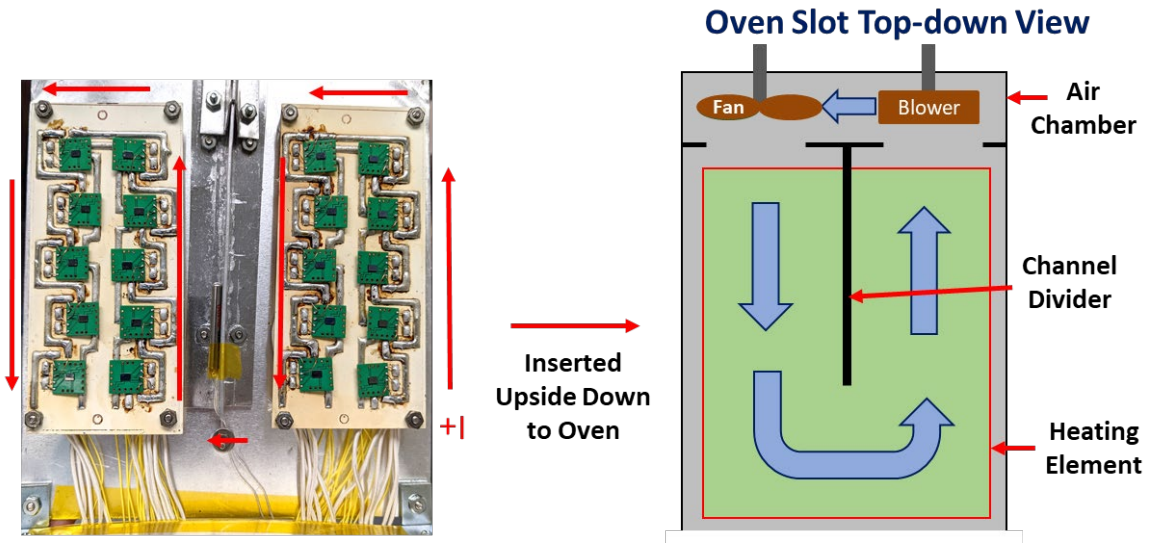


Figure 1-10. The picture of EM test structure with 20 samples mounted on. The schematic of the accelerated EM test structure with an air-medium cooling system.

Figure 1-11. CAD and real-life pictures of EM test structure with an oil-medium cooling.

and built specifically for air-medium accelerated EM tests. Each sample has two voltage taps, one at the DUT's via and another at the top of the DUT's UBM, measuring the voltage change to assess EM damage and failure. Furthermore, the oil-medium cooling test structure from Fig. 1-11 is designed and produced to accommodate to test packages that require high current density and JH. All the test structures have a pt100 Resistance Temperature Detector (RTD) to accurately measure an ambient oven temperature throughout the pre-test JH calibration and EM test process.

As a pre-test procedure, JH calibration is conducted to measure and compensate the JH generated from samples. The DUT resistances are measured at five different ovens ambient temperatures, ranging from 60°C to 110°C. A small current of 0.4A is used to measure the DUT voltage without JH. Since the solder interconnect has a linear relationship between resistance and temperature, the extrapolated linear fit of measurements give a target DUT resistance for a target test temperature. With the test current applied, which generates JH, the ambient oven temperature is adjusted to match the DUTs' resistance to the target resistance to compensate for the JH.

1.7. Sample Preparation for Failure Analysis

The samples which endured EM-induced failure are molded with epoxy to be cross-sectioned and analyzed under a scanning electron microscope (SEM) and Energy-dispersive X-ray spectroscopy (EDS). The first step of this process is making a sample mount. The samples are held with two wooden pieces and superglue perpendicular to the ground. A cut PVC pipe is used as a casing with Vaseline on both the PVC pipe and the ground to easily detach the epoxy. A solution of “QUICKMOUNT 2 Resin” and “QUICK-MOUNT 2 Hardener” is mixed in a 5 to 1 ratio. The mixed epoxy is poured into the casing and then cured overnight. The second step is grinding the samples to the cross-section of interest. The molded sample is removed from the casing and then grinded down to a point where Si wafer is exposed with 220-grit wet sandpaper on “Buehlar Ecomet 3,” a variable speed grinder polisher. 800-grit wet sandpaper is used to further approach the DUT. Once the DUT’s solder bump becomes visible and a miniscule amount of material has been ground, the 1500-grit wet sandpaper is used to slowly grind down to reach desired position of the sample, which is the center of the solder bump. Once the desired cross-section position is reached, the 3000-grit wet sandpaper is used to remove any other rough scratches left from lower grit sandpaper. The third step is polishing the samples’ cross-sectional surface. The three different polishing pads and three different polishing solutions are used to polish the surface of the samples to an appropriate condition for each analysis. The “MicroPolish™ II Alumina” 1.0 μm powder that is mixed with water is used on a “TEXPAN” polishing pad to remove finer scratches from the 3000-grit wet sandpaper, then 0.05 μm “MicroPolish™ Alumina” solution is used on “MICROPAD 2” polishing pad to make the surface as flat as possible with almost no

scratch marks. Step 4 is taping samples to reduce electric charging. The polished samples are then wrapped with Cu tape to reduce the exposure of the nonconductive epoxy, which would otherwise contribute to charging in the SEM. The fifth step is sputter-coating sample surface. The Cu-taped samples are sputter-coated with carbon using “CrC-100 Sputtering System” to further increase the conductivity of surface to reduce the electron charging buildup, which would otherwise make it difficult to obtain a valuable image.

For EBSD analysis, sample preparation steps need to be slightly modified. Since EBSD analysis uses Kikuchi patterns from a very thin top-layer of sample surface, it is necessary to acquire flat and stress-free surface for a clear Kikuchi pattern. The samples are molded with crystal bonds instead of epoxy to remove the mold at the end of sample preparation to minimize charging effects on samples. To prepare an EBSD appropriate sample surface, Cu taping and carbon sputter-coating are omitted, and then two additional steps are implemented to prepare a stress-free sample surface. Samples are prepared up to the aforementioned third step, polishing with 0.05 μm Alumina polishing solution. Step 4 of EBSD sample preparation is chemical and mechanical polishing. The 0.06 μm “SIAMAT Blue Colloidal Silica” polishing suspension is used on a “BLACK CHEM 2” polishing pad to chemically etch and polish the sample surface. Step 5 of EBSD sample preparation is ion milling. As a final step, samples are ion milled for 15 to 20 minutes using “IM4000 Plus” to remove a thin layer of stressed surface.

Chapter 2
Effects of UBM Thickness on Electromigration Failure Mechanism in SAC Solder Interconnects

2.1. Introduction

Since the EM failure kinetics are not solely affected by the EM flux level, but also by the flux divergence, the EM failure kinetics are known to be affected by multiple factors of the SAC solder interconnect. These factors include the presence or absence of alloying elements, the degree of JH, the interfacial microstructure, the intermetallic compound (IMC) formation, and much more [2], [19], [26]–[28]. The demand and need for improved EM reliability of the microelectronic packages have motivated extensive studies on the impact of such factors to gain a better understanding the EM failure mechanism [1], [3], [4], [10], [12], [14], [19], [26], [27], [29]–[33].

Among various factors, the UBM has become a particular interest because it can be a simple solution among other methods to improve EM reliability of packages. Interest in the implementation of thicker UBM layers is rooted to the observation that the classical EM failure mechanism is typically associated with the depletion of UBM. Since the diffusion of materials from the UBM by the EM flux divergence cause void nucleation and propagation, UBMs with increased thickness are considered to delay the void nucleation by providing an added conductive material supply which would theoretically need to migrate before void nucleation and propagation can occur [1], [10], [13]. This approach seems reasonable especially when Cu UBM is considered. For a Cu UBM, the classical

EM failure mechanism diffuses Cu first from the cathode to the anode side of the solder bump and nucleates void by depleting Cu since Cu diffusion in Sn has lower activation energy than Sn self-diffusion has [7]. Providing a substantial amount of Cu supply in the form of an UBM layer may impede or suppress the void nucleation. However, it is unknown if the Cu supply mechanism maintains effective after a limit of UBM thickness is reached. Xu et al. reports that the degree of current crowding is reduced as UBM gets thicker [34]. In addition to Xu et al., Lin et al. reported that the peak current density, current crowding, decreases from 630kA/cm^2 to 440kA/cm^2 by increasing UBM thickness from 0.3 μm to 0.8 μm, which is significantly higher than average current density of 5.0kA/cm^2 [29]. The result shows that the local peak current density is about 100 times higher than average current density. Furthermore, Tu reports the 100kA/cm^2 at current crowding region while average current density is 10kA/cm^2, 10 times lower than the current crowding region [3] .

In addition to using UBM as an effective diffusion barrier layer between the chip pad and solder bump to enhance EM resistivity of packages, UBM is used to connect die to substrate with solder bumps as shown in Fig. 2-1. Therefore, the proper UBM selection is crucial for its role in package's reliability. The UBM is used as solder adhesion layer,

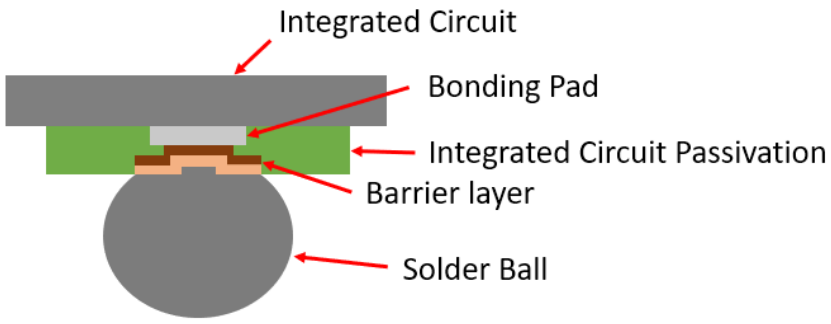


Figure 2-1. Schematics of solder interconnects, illustrating bonding pad, integrated circuit (IC), IC passivation, UBM, barrier layer, and solder ball.

diffusion barrier, adhesion promoter, and plating base for solder bumps [35]. In order to fulfill its roles, the UBM needs to address several issues [35]. The UBM needs to avoid film delamination, UBM failure, or Si cratering. It is imperative to understand the UBM and solder IMC growth to predict IMC's impact on reliability. The minimal electrical contact resistance between UBM and solder is necessary, too.

As an effort to increase the EM resistance of solder bumps in electronic packages, the combinations of elements are used as diffusion barrier layers. The Cu, Ti, Pd, Ni, W, and more are commonly used for barrier layers [1], [3], [29], [30], [33]–[42]. The barrier layers are known to hinder the EM induced diffusion of Cu from UBM due to Cu's slower diffusion through barrier layers, whose elements slow diffusions through solder alloys. For example, Lin et al. tests Cu UBM with the Ni barrier layer at the bottom, but none at the sides of UBM [29]. The study reports that the IMC growth occurs more rapidly at the side of Cu UBM. In addition, Lin et al. reports that as the Ni barrier gets thicker from 0.3μm to 0.8μm, the MTTF increases without changing any other aspects of the interconnects [29]. The new combinations may have unexpected EM failure mechanisms or kinetics. Therefore, different combinations of elements require extensive studies to understand different IMC formations and microstructures of solder ball, which have effects on the overall reliability of electronic packages. Furthermore, the UBM is known to change the IMC formation rate and its composition. The IMC formation rate change affects undercooling as well as other aspects, such as microstructures and hardness [38], [39]. The EM and thermal fatigue lifespan were affected by the UBM thickness [30]. Therefore, careful selection of UBM would benefit EM resistivity of packages.

2.2. Background

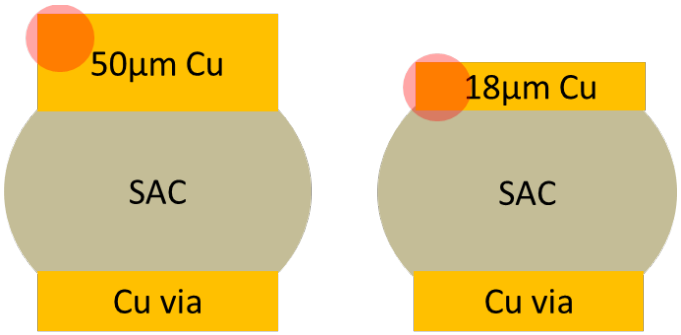


Figure 2-2. Schematics of thinner and thicker UBM interconnects with red circles indicating different current crowding regions.

2.2.1. Current Crowding of Different UBM Thicknesses

As mentioned in Chapter 1, current crowding happens when there is a significant change in the current density or the current direction. Therefore, when the current flows into the solder interconnect from the Cu redistribution layer on the Si chip, the cross-sectional area differences can be as high as 100 times, causing a current crowding region in the interconnect. Current crowding results in a much higher local current density, non-uniform JH, and faster EM kinetics [3], [9], [12], [29], [34]. Therefore, the UBM is consumed faster and ultimately has an increased EM-induced failure rate. The thinner UBM interconnect would have a current crowding region closer to the interface between the UBM and the SAC solder bump, which is a weak point. On the other hand, the thicker UBM interconnect has the current crowding region closer to the Si wafer, slowing down the EM at the weak point. Fig. 2-2 shows the illustrations that marks two different current crowding regions. Since a thin UBM interconnect has less amount of Cu, the EM-induced void nucleates faster than that in a package with a thicker UBM interconnect.

2.2.2. Anisotropic Properties of Tin

The Sn is known to have highly anisotropic EM properties because of its BCT crystal structures as illustrated on Fig. 2-3 [5], [43]–[52]. The c-axis or [001] grain

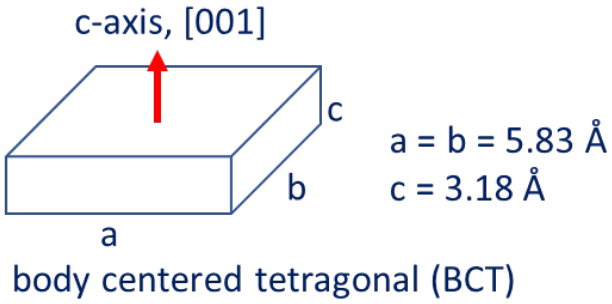


Figure 2-3. Schematics of Sn's body-centered tetragonal (BCT) crystal structure, indicating c-axis with a red arrow.

orientation of Sn is referred to as a weak-link because of its faster diffusion rate compared to the two other axes. Sn has lattice constants of a = b = 5.83Å and c = 3.18Å. The c-axis provides the largest diffusion pathway for atoms to easily migrate through the SAC solder alloy. Once the c-axis is aligned with the EM flux direction, the Cu diffusion rate is reported be higher than that of other two axes [44]–[46], [49]–[53]. As shown in Fig. 2-4, Yeh and Huntington reported that Ni has diffusivities of $1.19 \times 10^{-9} cm^2/sec$ along the a-axis and $7.88 \times 10^{-5} cm^2/sec$ along the c-axis [50]. Dyson et al. reported that Cu has diffusivities of

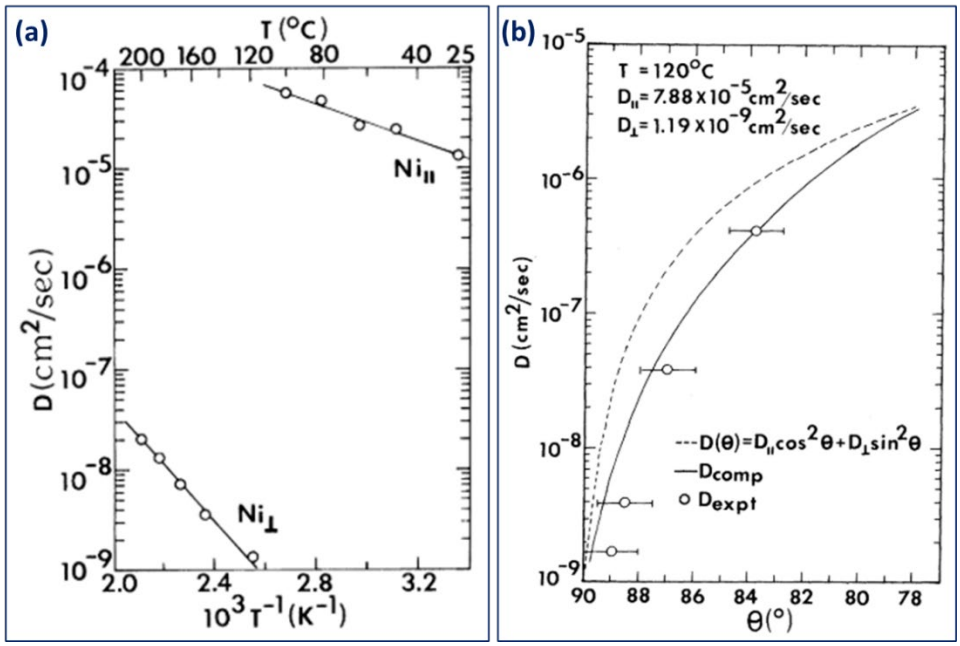


Figure 2-4. (a) Temperature dependence of diffusivity for Ni along a and c axes of Sn. (b) Comparison of numerically computed values and experimental results for diffusion of Ni close to the basal planes of Sn [50].

$2.00x10^{-6}cm^2/sec$ along the c-axis, which is 500 times faster than that along the a-axis [53]. In some cases, the alignment of the c-axis or weak-links with the EM direction would become a controlling EM failure mechanism.

2.3. Motivation and Expectations

This part of the study investigates the role and the effectiveness of different Cu UBM thicknesses on EM failure mechanisms and kinetics. It is motivated by the need for a more accurate EM reliability prediction. Particularly, the focus is on whether the impedance of void nucleation by increasing UBM thickness may not have the same effectiveness after reaching a certain UBM thickness. The comparative accelerated EM study on SAC interconnects is first conducted with three different UBM thicknesses. The initial expectation is a linear scaling of EM lifetime with the increase in Cu UBM thickness, and then a plateau after a certain UBM thickness due to a saturation of Cu UBM thickness benefits, which is similar to what Zheng et al. (study on 10μm, 6μm, and 1.5μm of various UBMs), Lin et al. (study on 0.3μm, 0.5μm, and 0.8μm Ni UBM), and Yiping et al. (study on 5μm and 10μm Ni UBM) reported [1], [29], [30]. However, the experimental data obtained in this study defy these expectations. The EM reliability decreases after a certain critical UBM thickness. An initial postulation is formed to explain the result. The postulation is that the EM failure rate is determined by a competition between a limited Cu supply and the c-axis alignment with the EM direction or weak-links exposure. The thicker UBM sample has a more evenly distributed EM flux across the interface of Cu and SAC because current crowding region is at the corner of the solder interconnect. The resulting evenly distributed EM flux activates weak-links across the Cu and SAC interface, accelerating EM failure. To test the initial postulation, the second comparative study of

SAC interconnects is conducted under two different current flow configurations, symmetrical and asymmetrical, to dictate two different current crowding regions. The expectation of different current crowding regions is that there will be an overall improvement in EM failure rate due to the current density and JH reduction. The thinnest UBM sample would have the greatest amount of improvement because of the highest amount of reduction. The test disapproves that weak-links exposure is another primary EM failure mechanism competing with the classical EM failure mechanism. Therefore, a hidden factor causes other primary EM failure mechanism that competes with the classical EM failure mechanism.

2.4. Samples and Experimental Setup

This comparative study is set to investigate the UBM thickness effect and the current crowding effect. The wafer-level chip scale package (WCSP or WLCSP) samples with three different bare Cu UBM thicknesses are used, which are 18μm, 35μm, and 50μm Cu UBM thicknesses. The 18μm thick Cu UBM sample would yield the highest amount of current crowding and have a limited Cu supply. On the other hand, the 50 μm thick Cu UBM sample would yield a significantly reduced current crowding and have an almost infinite Cu supply to delay the EM-induced failure. The two different current crowding regions, asymmetry and symmetry, are tested with all three groups of different UBM thickness samples. The asymmetrical current crowding region contributes to faster EM kinetics as it causes the highest amount of JH. The symmetrical current crowding region contributes to slower EM kinetics by theoretically reducing the JH by half in two different regions.

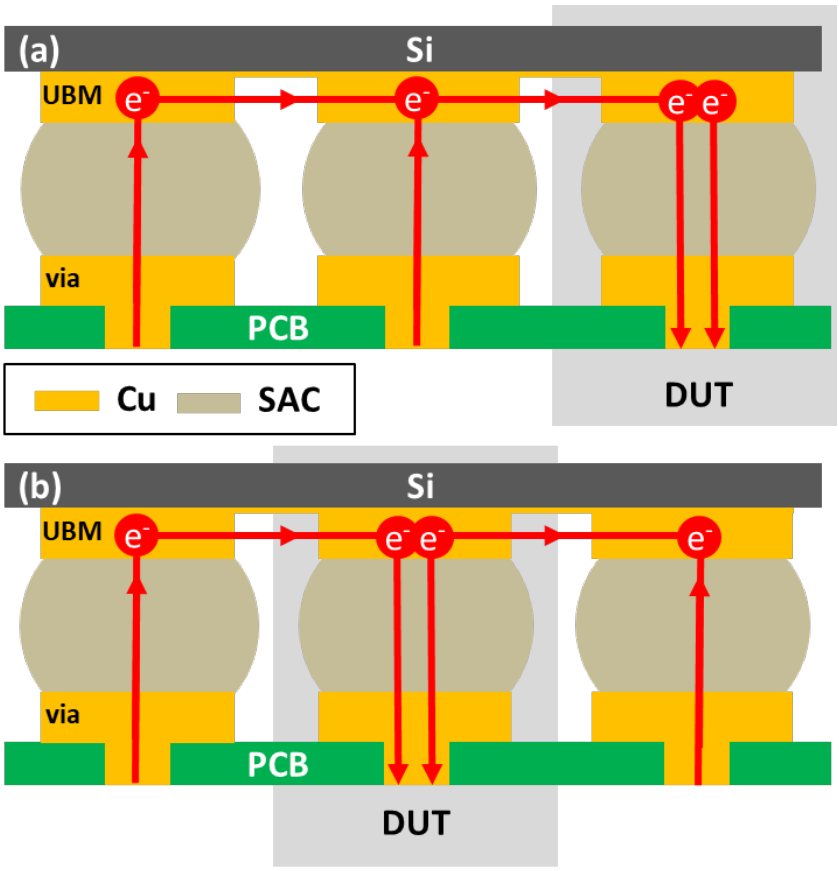


Figure 2-5. Current connection schematics of tested sample for the (a) asymmetrical and the (b) symmetrical current crowding configuration.

Fig. 2-5 shows the schematics of current flow configurations on the samples to induce both asymmetrical and symmetrical current crowding regions for comparison. The symmetrical current crowding region is investigated for a comparative study on the interplay between Cu UBM thickness and current crowding. For asymmetrical current crowding configuration, the right most bump is the DUT as shown in Fig. 2-5 (a). Fig. 2-5 (b) uses the center solder bump as a DUT, so the current flows from both right and left, causing symmetrical current crowding. This symmetrical current crowding configuration is used to study the interplay between UBM thickness and current crowding regions. The DUT is connected by itself with two neighboring supporting bumps for EM tests. This circuitry ensures that the DUT fails first by EM before the other two supporting bumps do.

Table 2-1 shows the accelerated EM test matrix for UBM thickness effect comparative study. Table 2-2 shows the testing matrix for asymmetrical and symmetrical current crowding region orientations in the comparative study. Each test condition consists of 20 WCSP samples, which are serially connected in an in-house designed and built testing structure. The overall results and conclusion are shown in next section.

Table 2-1. Shows the accelerated EM test matrix for each sample.

Sample Structure	Test Conditions	
UBM Cu, µm	Temperature, °C	Current Density, kA/cm^2
18	135	9.63
	165	
	150	12.04
	135	13.24
	165	
	150	
35	165	9.63
	150	12.04
	135	13.24
50	165	9.63
	150	12.04
	135	13.24

Table 2-2. Shows the accelerated EM test matrix for each sample

Sample Structure	Test Conditions	
Asymmetry Current Crowding Regions		
UBM Cu, µm	Temperature, °C	Current Density, kA/cm^2
18	165	9.63
35	165	9.63
50	165	9.63
Symmetry Current Crowding Regions		
UBM Cu, µm	Temperature, °C	Current Density, kA/cm^2
18	165	9.63
35	165	9.63
50	165	9.63

2.5. Results and Discussions

2.5.1. Effect of UBM Thickness on Mean Time to Failure

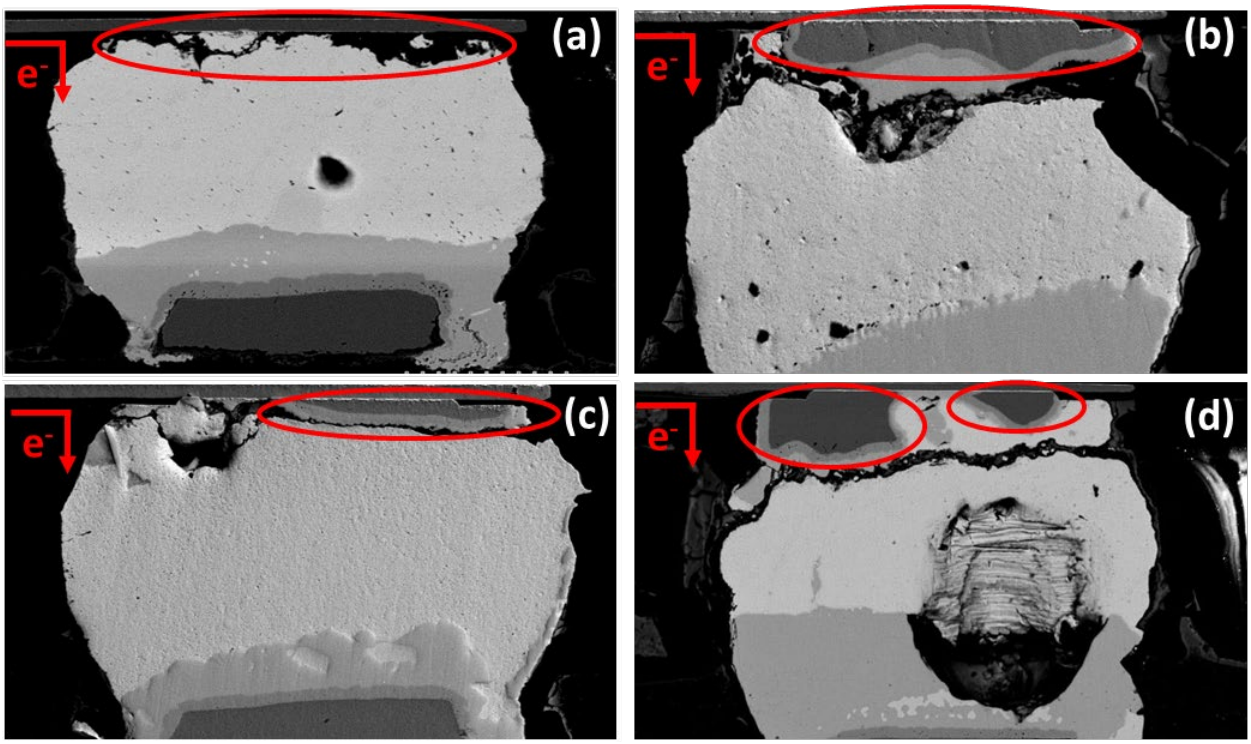


Figure 2-6. Cross-sectional SEM pictures in BSE-mode for 18 μm (a) and (c) and 50 μm (b) and (d) UBM samples under asymmetrical current crowding orientation.

The samples tested under the asymmetrical current flow configuration are cross-sectioned and analyzed under SEM. Fig. 2-6 (a) and (c) shows the DUT in a WCSP with an 18μm-thick UBM. A void nucleation is located in the region where the current crowding is the highest. The SEM image shows that the UBM Cu is nearly completely consumed. Fig. 2-6 (d) and (d) show the DUTs in WCSPs with 50μm-thick UBMs. These SEM images show a random distribution of Cu UBM consumption along the interface, rather than in the corner where the electrons enter the DUT solder bump. Fig. 2-6 confirms that current crowding becomes alleviated and the EM flux becomes evenly distributed across the interface between the Cu UBM and the SAC solder bump with increased UBM thicknesses. The microstructure matches with the classical EM failure mechanism that current crowding and Cu depletion lead to a critical open circuit failure.

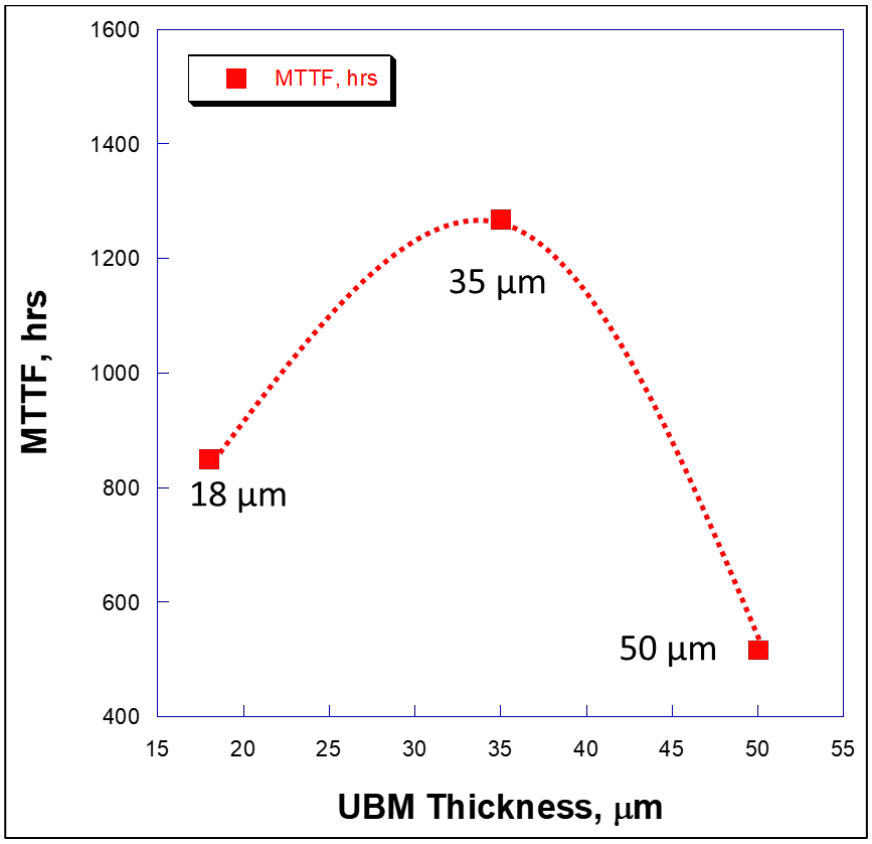


Figure 2-7. Graph of different UBM thickness samples' mean-time-to-failure (MTTF).

The experimental MTTF data obtained from tested samples under an asymmetrical current flow configuration show the complex effects of UBM thickness on the EM failure kinetics. The results differ from the initial prediction and interpretations from previous studies [4], [10], [29]–[31]. Fig. 2-7 shows that the EM kinetics is not linear relationship with UBM thickness. The 35µm UBM sample has the longest MTTF among 18µm and 50µm UBM samples. The MTTF of 50µm UBM sample suggest that EM reliability becomes worse after a critical UBM thickness. Thus, this result suggests that there is the critical UBM thickness that maximize the EM reliability benefit of UBM. While this result is critical for the implementation of a UBM in industry, it also introduces a complication which makes it difficult to fully understand the responsible failure mechanism. The current crowding or limited Cu supply is not the sole EM failure mechanism affecting

the EM failure rate; rather, it seems to compete with another primary EM failure mechanism.

2.5.2. Effect of Current Crowding Regions

It is postulated that the effect of UBM thickness on EM failure kinetics involves a competition between two primary EM failure mechanism based on the Fig. 2-6 and 2-7. The first competing failure mechanism is the classical EM failure mechanism that failure kinetics is determined by the amount of Cu supply and thus the current crowding. The second failure mechanism is speculated to be an increased exposure of weak-links as the UBM gets thicker. The limited Cu supply allows SAC interconnect to develop a void faster at the Cu and SAC interface, thus the EM failure can be delayed by increasing the UBM thickness. The effect of an increasing Cu supply becomes saturated and no longer improves the EM failure kinetics at a critical UBM thickness. The wider current distribution and weak-links distribution then may become a controlling failure mechanism determining EM failure kinetics. As mentioned in section 2.2.2, Sn is known to have highly anisotropic properties from its BCT crystal structure [5], [19], [43], [45]–[51], [54]–[56]. Cu diffuses 37 to 500 times faster along the c-axis of Sn compared to a or b axes [45], [49], [54], [56], [57]. Therefore, the EM failure kinetics is the fastest when the c-axis is aligned with EM current direction. When the UBM is thin, then the c-axis Sn grain orientation alignment at the solder interconnect where the current density is the highest, the solder interconnect is extremely vulnerable to the EM failure mechanism. The EM failure kinetics along the c-axis or weak-links becomes a determining failure mechanism for early EM failures in thinner UBM samples. The other Sn grain orientations are less prone to EM mechanism, so the Cu supply effect becomes a controlling mechanism. When the UBM thickness is

thicker than the critical thickness, the current crowding effect no longer plays a role, however, multiple c-axis aligned grains along the Cu and SAC interface are exposed to the current. This is why Cu consumption areas are random at multiple locations along the interface of Cu and SAC in Fig. 2-6 and thus induces faster EM failures.

To validate the postulate, a comparative study with a symmetrical current flow configuration is conducted. If the postulate is correct, then the 18μm and 50μm-thick UBM samples would have slower EM failure rates due to of the decreased current crowding effects. The effects of reduced current crowding level would be greater on 18μm UBM samples than 50μm UBM. Therefore, changing the current flow configuration would affect EM failure kinetics more in thinner UBM samples than it would in thicker UBM samples.

The EM test data graph in Fig. 2-8, presenting the cumulative probability with the time to failure (TTF), suggest that the changing current flow configuration shows similar extent of EM kinetics improvement in both 18μm and 50μm UBM samples. Furthermore, the lack of improvement on early failures by switching current flow configuration suggests that the current crowding and weak-links distribution is not a primary mechanism competing with the classical EM failure mechanism in determining the EM failure kinetics,

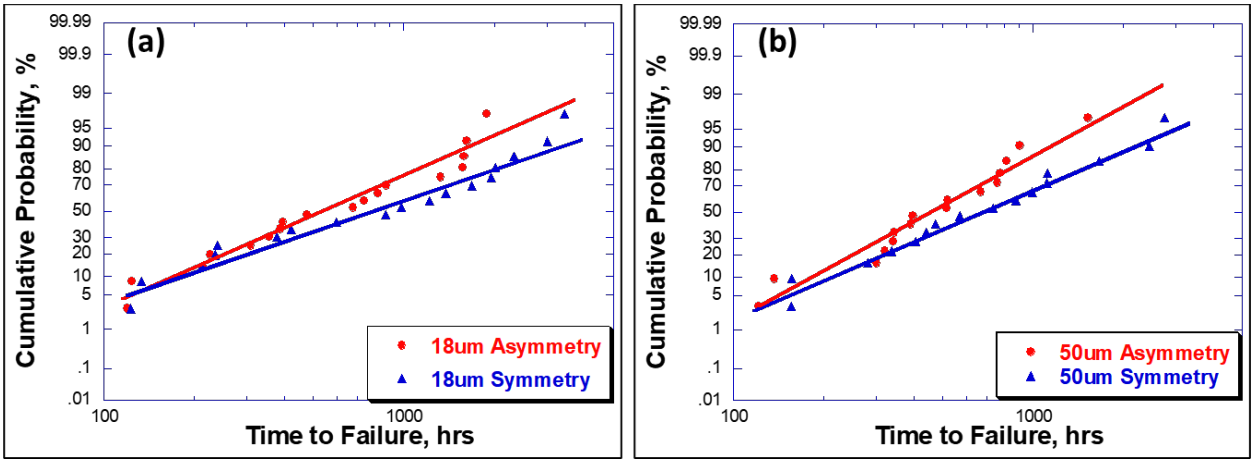


Figure 2-8. Graph of normalized time to failure as a function of cumulative probability for (a) 18 μm and (b) 50 μm UBM thickness samples in asymmetrical and symmetrical current crowding orientations

disapproving the postulate. The data show that there is some level of effect from current crowding reduction, but that is not the second primary EM failure mechanism. As a result, the compressive stress may be considered as a possible hidden factor.

2.5.3. Stress as a Hidden Parameter

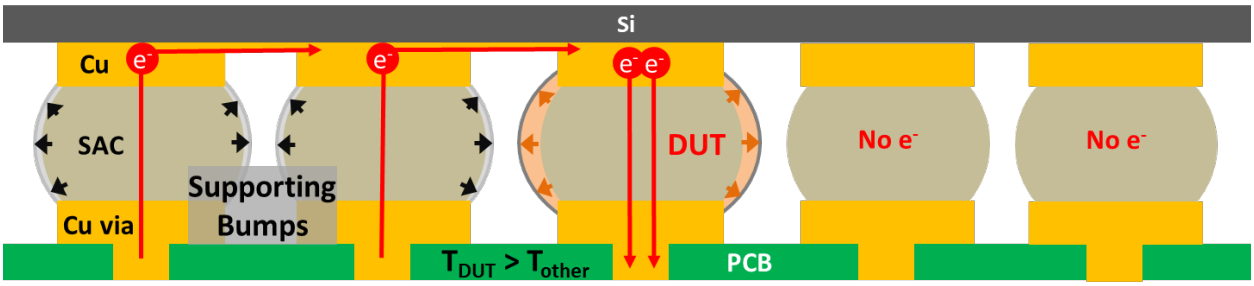
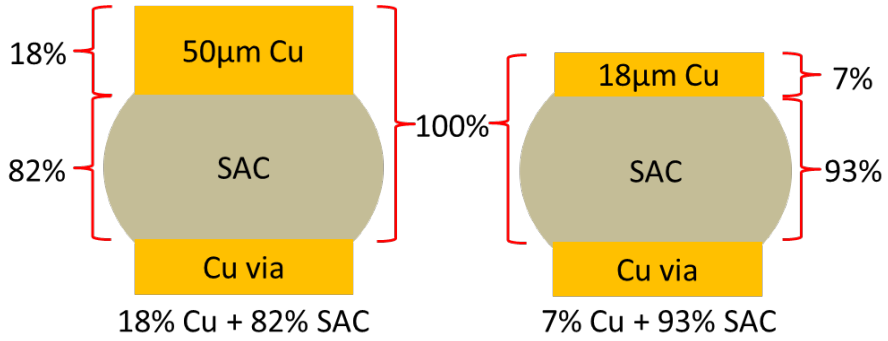


Figure 2-9. Schematics of current connection, illustrating the highest amount of current density through the DUT.

Since the c-axis alignment cannot explain the complicated relationship between the EM failure rate and the UBM thickness, another hidden parameter, stress, is considered to explain the experimental data. Compressive stress is reported to slow down EM by slowing down the diffusion rate and the void propagation rate [3], [30], [31]. The current connection of solder interconnects in Fig. 2-9 shows that the DUT is under the highest amount of current density among the solder bumps, thus having the highest amount of JH. The temperature gradient from the different amounts of JH in the solder bumps in the test circuit causes the DUT to expand the most among the three connected solder bumps. Since 22 other SAC solder interconnects do not have current, the rigid Si substrate and PCB confine the DUT and supporting bumps' expansion. The highest amount of expansion of DUT induces compressive stress, and the surrounding bumps are under tensile stress. The CTE mismatch between the Cu and the SAC solder alloy changes the amount of compressive stress on the DUT as UBM thickness changes. Cu has about 17ppm/°C, and SAC alloy has about 24ppm/°C. Fig. 2-10 illustrates the



Coefficient of Thermal Expansion (CTE)	
Cu	~17 ppm/°C
SAC	~24 ppm/°C

Figure 2-10. Schematics of solder interconnects of 18 µm and 50 µm UBM thickness samples, showing different percentage of Cu and SAC within UBM and SAC solder ball.

different ratio of Cu in the UBM and the SAC solder height combined for the 18µm and the 50µm UBM samples with a 230µm tall SAC solder ball. Considering the amount of Cu in UBM and SAC in solder ball as 100%, the 18µm UBM sample has 7% Cu and 93% SAC alloy. The 50µm UBM sample has 18% Cu and 82% SAC alloy, having a higher percent of Cu than the 18µm UBM sample does. Since Cu has a lower CTE, the higher percent of Cu in the 50µm UBM sample causes smaller expansion than the 18µm UBM sample does. The higher compressive stress in 18µm UBM samples causes slower void propagation than that of 50µm UBM samples. The difference in compressive stress and its effects between different UBM thickness amplifies as the void propagates, causing higher JH with increased current density.

Further evidence of stress involvement can be found through microscopic failure analysis. The SEM images in Fig. 2-11 show cracks near Cu via by tension on supporting bumps for both 18µm and 50µm UBM samples under both asymmetry and symmetry current configurations. The cracks at the Cu via of the supporting bumps but not in the DUT suggests that the DUT expands sufficiently to cause a tensile stress on its neighboring supporting bumps and receive compressive stress on itself.

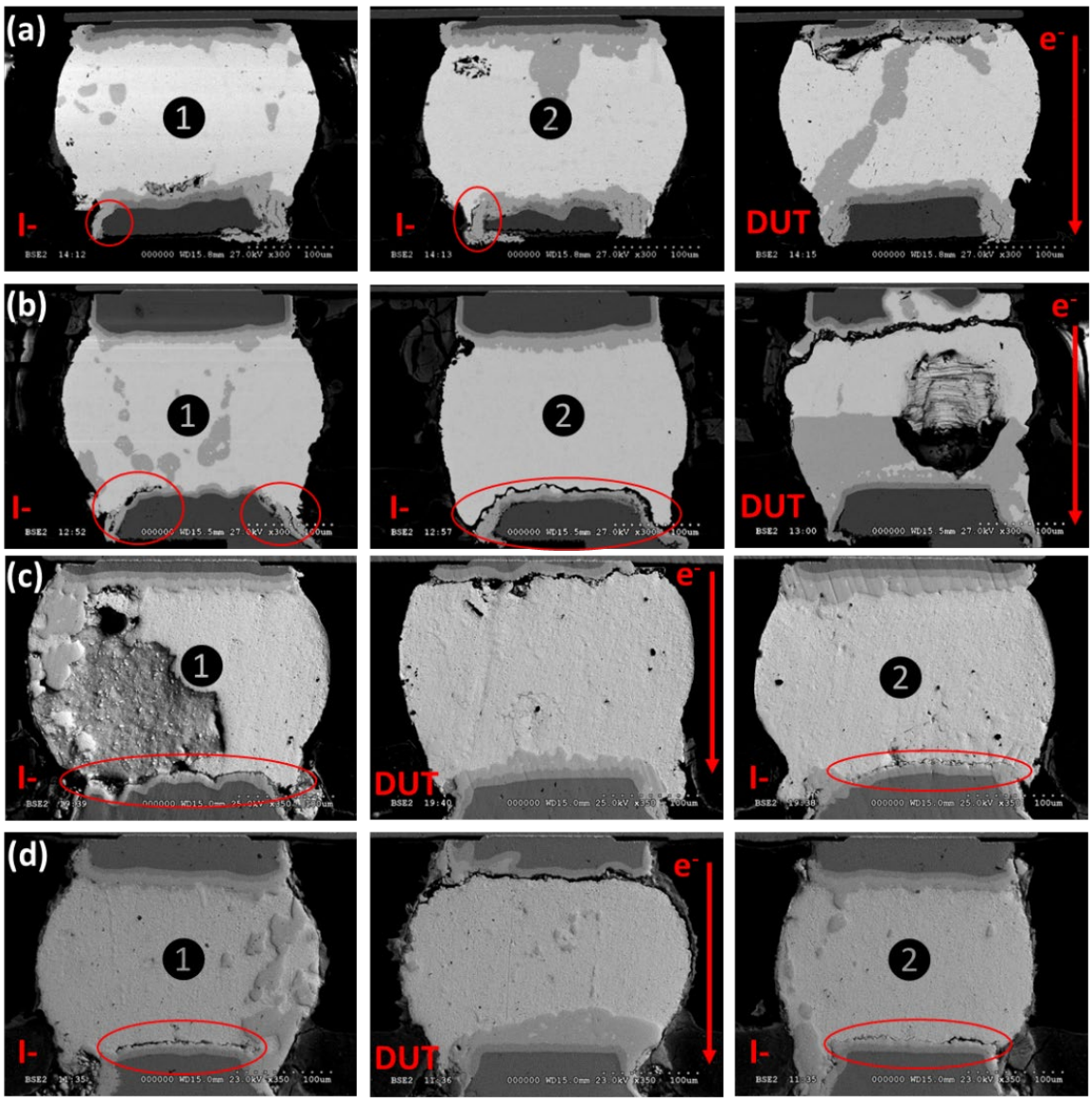


Figure 2-11. Cross-sectional SEM pictures in BSE-mode, showing 18μm UBM sample tested under (a) asymmetrical and (c) symmetrical current crowding orientations and 50μm UBM sample tested under (b) asymmetrical and (d) symmetrical current crowding orientations. The red circles indicate the evidence of tensile stress involvement.

2.5.4. EM Failure Mechanism on Different UBM Thickness

The microstructures indicate that the classical EM failure mechanism is still a major factor responsible for inducing failures within SAC solder interconnects. However, the experimental data and failure analysis suggest that there are two primary EM failure mechanisms competing with one another, and those determine the EM failure rate for

different UBM thickness. The two primary competing EM failure mechanisms are limited Cu supply and compressive stress in the DUT. The thinner UBM samples' failure rate is determined by the UBM depletion from a limited Cu supply. The thicker UBM samples' failure rate is determined by a faster void propagation rate due to a smaller compressive stress than in thinner UBM samples. The competition between the two EM failure mechanisms explains the finding that both 18 μm and 50 μm UBM samples fail faster than 35μm UBM samples.

Fig. 2-12 illustrates the two proposed competing EM failure mechanisms. The 18μm UBM samples have faster void nucleation because of limited Cu supply, while the 50μm UBM samples have slower void nucleation due to almost infinite Cu supply. However, once the void nucleates, the 50μm UBM samples have faster void propagation due to an insufficient amount of compressive stress, but the 18μm UBM samples have slower void propagation due to a sufficient amount of compressive stress.

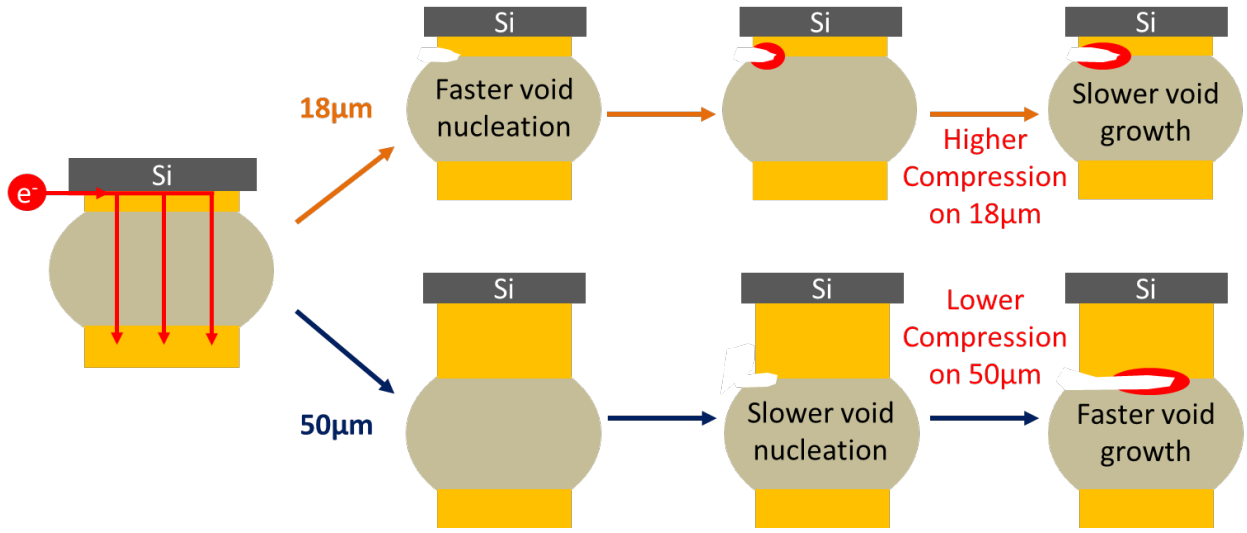


Figure 2-12. Illustration of EM failure mechanism for 18μm (thinner) UBM sample and 50μm (thicker) UBM sample.

2.6. Conclusion

The UBM thickness effects on EM failure mechanism and kinetics are studied by conducting a comprehensive EM test and characterization of SAC solder interconnects in WCSP. The results reveal that there are at least two competing EM failure mechanisms affecting the EM failure kinetics. The UBM acts as a Cu reservoir to reduce the EM flux divergence by resupplying diffused Cu. The Cu supply effect controls the EM failure kinetics below a critical UBM thickness. After the UBM thickness reaches the critical thickness, the EM failure mechanism is no longer controlled by the Cu supply but by a second mechanism. The initial postulation of the second mechanism is the weak-link exposure that accelerates EM failure kinetics. The EM test with two different current crowding regions shows that the weak-link exposure is not the controlling mechanism. The stress is the second hidden mechanism that controls EM failure kinetics after a critical UBM thickness. With the highest amount of current density and JH, the DUT is under compressive stress. Due to the CTE mismatch between Cu and Sn, the solder interconnects are under different amounts of compressive stress depending on the UBM thickness. The thinner UBM sample has a higher ratio of Sn, which has a higher CTE than Cu, so it has a higher compressive stress than the thicker UBM sample does. The stress explains the complicated relationship between the MTTF and the UBM thickness observed from the comparative EM tests. It is important to consider stress as one of the major factors affecting the EM failure mechanisms and kinetics. Therefore, using the critical UBM thickness to balance the role of the UBM as a Cu reservoir and the compressive stress is key to maximizing the benefit of the UBM on the EM resistance of the microelectronic packages.

Chapter 3
The Relationship Between the Sn Grain Orientation and the Electromigration Reliability of SAC Solder Interconnects

3.1. Early Failures by Fast EM Diffusion Along C-Axis

The most of comprehensive EM tests on WCSP samples show the first few failure samples experiencing failure much lot faster than the rest of samples does within a same test group despite different test conditions and package configurations [14], [26], [32]. The early failures give biased and inaccurate statistical calculations of the test results, hindering the accuracy of EM studies. The early failures are often assumed to be correlated with the c-axis of the Sn grain orientation. The Sn has BCT crystal structure that has a shorter c crystal lattice than the a and b crystal lattice. The c lattice constant is 3.18Å, and a and b lattice constants are 5.83Å. Due to the BCT crystal structure and its atoms' locations, Sn has anisotropic properties, including mechanical and electrical [5], [26], [43]–[52]. As mentioned in Section 2.2.2, the EM diffusion along the c-axis, [001], is easier than that along the a and b axes due to a larger diffusional path. The larger diffusion path requires a lower activation energy to diffuse Cu through the c-axis than any other two axes. Therefore, when the c-axis is aligned with the EM direction, Cu diffuses faster, nucleating a void at the Cu and SAC interface [26], [44]–[46], [49]–[53]. There has been a study that reports that the EM diffusion along c-axis can be up to 500 times faster than other two axes [53]. This highly anisotropic diffusion property of Sn causes the c-axis alignment to be the EM failure mechanism controlling early EM failures, which differs from

the classical EM failure mechanism that occurs in the rest of the test group. The EM failure mechanism of early failures is studied by microstructural failure analysis with an SEM and an EBSD. The SEM failure analysis does not yield any significant difference in microstructure between early failures and late failures. The EBSD analysis of Sn grain orientation and its comparison to the TTF data indicate an involvement of the Sn's anisotropic properties.

In some instances, a package can fail earlier than the calculated reliability limit, causing a detrimental result. These early failures are especially detrimental for industries where the first 5% or lower failures are used to calculate the reliability of a package. There have been many efforts to mitigate failure by simply adding an additional UBM and diffusion barrier layers. However, the simpler and more reliable way to improve EM reliability of a package is to manipulate Sn grain orientation as they are reflowed. The study to confirm the early EM failure mechanism, which is an alignment of c-axis with EM direction, is studied, and the result is discussed in this chapter. The following chapter talks about a simple yet effective way to mitigate early EM failure by preventing the c-axis alignments.

3.2. Results and Discussions

3.2.1. Early EM Failures Within a Test Group

When an accelerated EM test is done, a log-normal distribution and cumulative probability are graphed and used to calculate the MTTF, the shape factor (σ), and the failure distribution of the test samples. The cumulative probability graph in Fig. 3-1 (a) has four early failures that are highlighted with red circles. The early failures have a different slope than rest of the group, indicating that the early EM failures have different EM failure

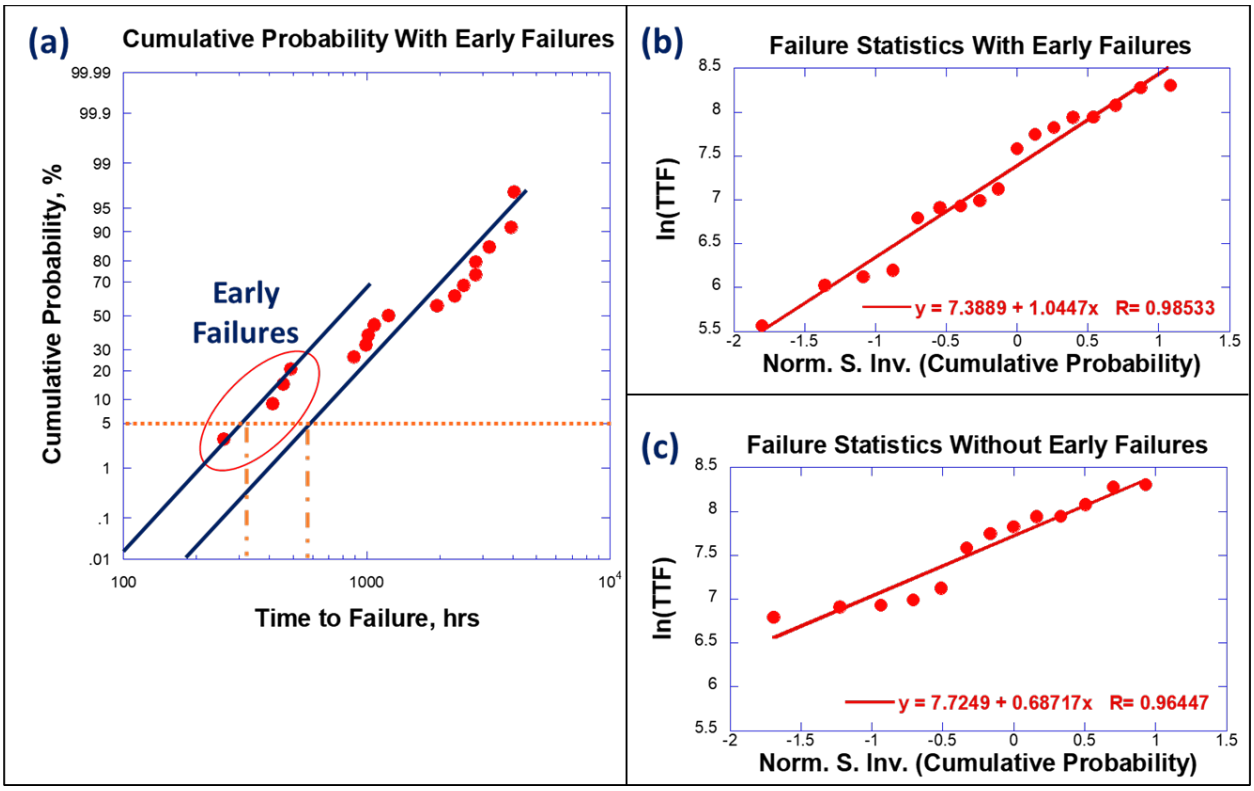


Figure 3-1. Graph of failure statistics. (a) Shows graph of time to failure as a function of cumulative probability. (b) and (c) show an inverse of the standard normal cumulative distribution with the cumulative probability as a function of natural logarithm of time to failure with and without early failures, respectively, to calculate shape factor and mean time to failure [32].

mechanism than rest of the group. The different EM failure mechanism of early failures plays an important role in inducing faster EM failure kinetics. For a log-normal distribution graph, the inverse of standard normal cumulative distribution with cumulative probability is x-axis. The natural logarithm of TTF, ln(TTF), is set as the y-axis. The cumulative probability is calculated with the following equation,

$$\text{Cumulative Probability} = \frac{R-0.3}{TR+0.4} \tag{3-1}$$

where R is the rank or order of a failed sample within a group, TR is the total rank or test group size. Fig 3-1 (b) and (c) show the log-normal distribution graphs with linear-fit calculations of test groups with and without early EM failures, respectively. The MTTF is calculated with the linear-fit equation of the log-normal distribution graph with the following equation,

$$\mathrm{MTTF} = e^{\text{y-intercept}} \quad (3\text{-}2)$$

where the y-intercept represents the y-intercept of the linear-fit equation of the log-normal distribution. The slope of the linear-fit equation is the shape factor (σ), which represents the distribution of failed sample in a group. The shape factor is normally less than 1.0 and stays around 0.6. The shape factor of the group, including early failures, is 1.0, but the group without early failures is 0.69, which is closer to an accurate and acceptable value. Using the equation (3-2), MTTF of sample group with and without early failures is calculated. The group with early failures has a shorter MTTF of 1618 hours compared to 2264 hours of the group without early failures. The difference further supports the argument that early failures yield biased EM test results.

3.2.2. Sn Grain Orientation in Early and Late Failures

The SEM and EBSD failure analysis are done to study the early EM failure mechanism in solder interconnects. Unlike the regular SEM, EBSD analysis is highly sensitive to sample surfaces and gives crystallographic data on samples microstructure surfaces within an order of tens of nanometers. The diffracted electrons from corresponding diffracting planes are detected and captured through a charge-coupled device (CCD) camera as Kikuchi lines that form a pattern. The Kikuchi lines are digitally processed and produce index data. The index data are compared to a digital data base and identify crystalline structure and crystallographic grain orientation.

SEM images of early failed samples from different test groups are shown in Fig. 3-2. They are first four failures. Fig. 3-3 shows the SEM images of late failures from microstructures observed through SEM show no distinctive difference between early and different test groups, ranging from seventeenth failures to nineteenth failures. The failure

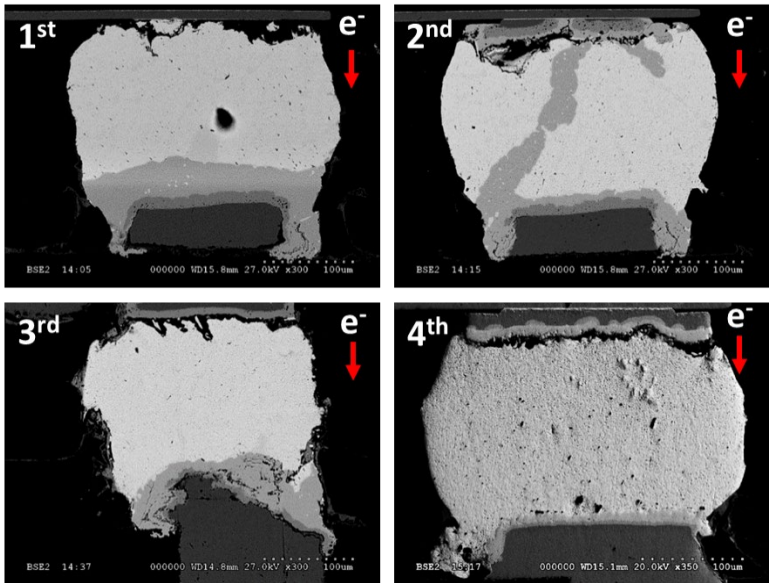


Figure 3-2. SEM images of early failed samples from different test groups. 1st failed sample has 18μm Cu UBM, 2nd failed sample has 18μm Cu UBM, 3rd failed sample has 18μm Cu UBM, and 4th failed sample has 15μm Cu UBM [32].

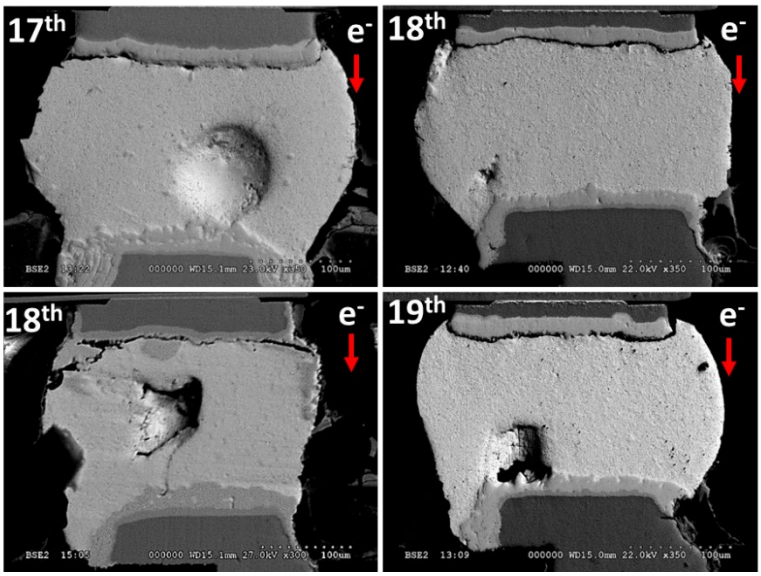


Figure 3-3. SEM images of failed samples from different test groups. 17th failed sample has 32μm Cu UBM, 18th failed sample has 15μm Cu UBM, 18th failed sample has 18μm Cu UBM, and (d) 19th failed sample has 15μm Cu UBM [32].

late failures. They all have failure features consistent with the classical EM failure features of void nucleation and propagation at the cathode side of the solder joint with an IMC formation at the anode side of the solder joint. With a careful investigation, the small difference in void size can be seen. The void size is slightly smaller in late failures. This

is most likely due to the fast EM diffusion caused by the c-axis alignment. When the Cu at the UBM and SAC interface diffuses quickly through Sn's c-axis, it leaves vacancies that can be filled by the Cu UBM. Since the diffusion rate of Cu through the c-axis is a lot faster than it is through Cu in the UBM, the higher discrepancy of the Cu diffusion rate between Cu through Cu and Cu through Sn's c-axis increases the void size in samples which failed earlier than in samples that failed later in the tests.

EBSD analysis is conducted to study Sn's grain orientation within the SAC solder to see its relationship with the early EM failure mechanism and a clear difference in failure features. EBSD analysis gives a better insight of mechanism responsible for early EM failures. The BCT crystal structure of Sn gives anisotropic properties. The relatively larger diffusion path along the c-axis or the [001] direction induces faster Cu diffusion due to a lower required activation energy. An inverse pole figure illustrates a stereographic projection like a regular pole figure. The main difference between regular and inverse pole figure is that an inverse pole figure is plotted relative to a specific sample direction, such as normal, rolling, and transverse directions. A regular pole figure is drawn relative to a sample's axis. The inverse pole figure is more convenient and precise for analyzing the Sn grain orientation and may be used as a heatmap for a crystal orientation map, which only shows colors of grain orientations. Since the samples are cross-sectioned vertically and prepared for EBSD analysis, the crystal orientation along the rolling direction of the sample is parallel to the EM load direction. Therefore, the c-axis or [001] grain orientation observed in the rolling direction EBSD results shows the c-axis alignment with EM current.

EBSD analysis results of samples failed in different orders are shown in Fig. 3-4. c-axis alignment is colored with red on crystal orientation map and the inverse pole figure.

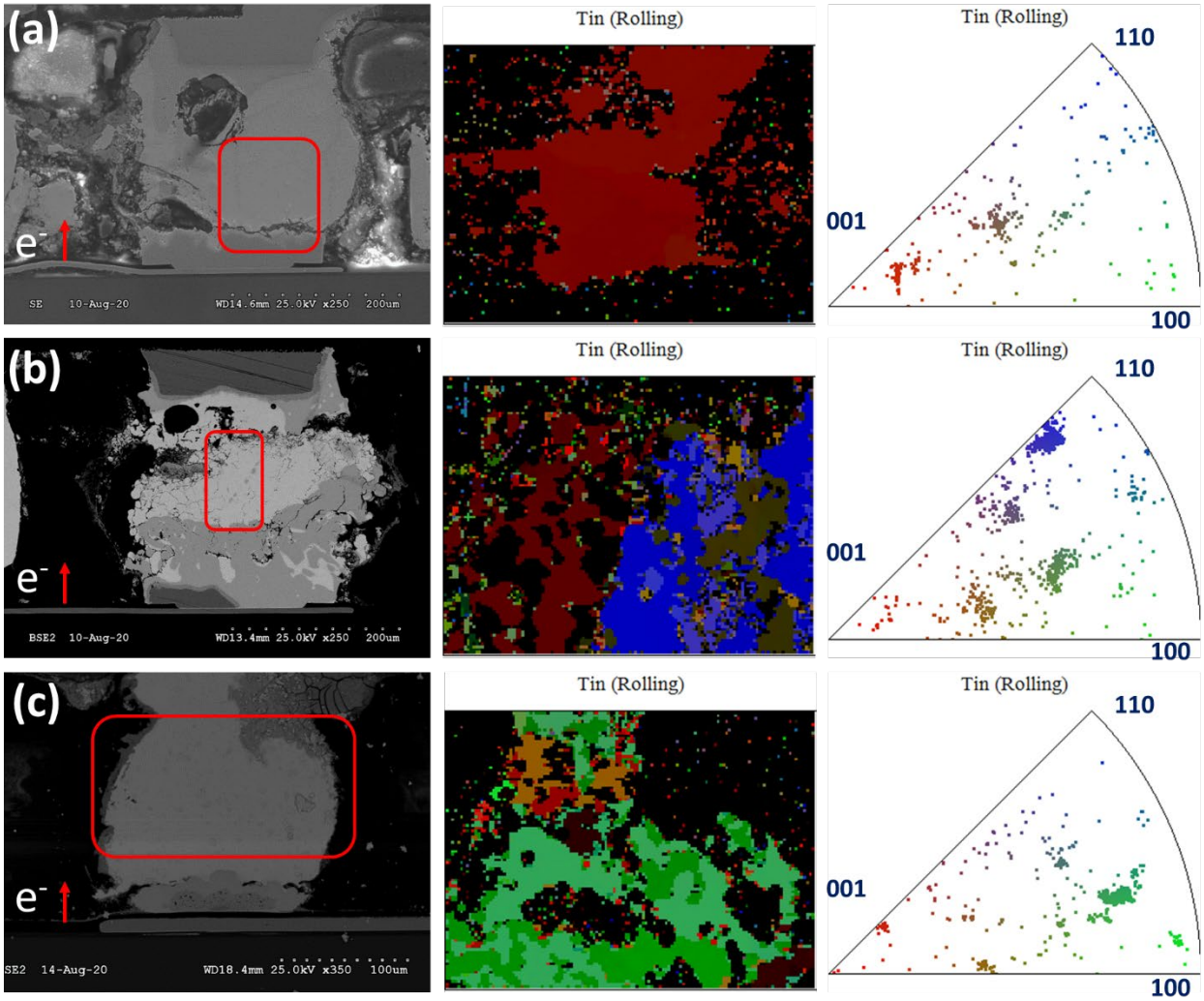


Figure 3-4. EBSD results showing Sn's crystal orientation map and inverse pole figure in rolling direction. (a) Sample with 5% failure rank, (b) sample with 21% failure rank, and (c) sample with 81% failure rank [32].

Fig. 3-4 (a), (b), and (c) show the EBSD results of samples with different failure ranks. The failure rank is calculated by dividing the order of the sample failed by the total number of samples within the test group. Therefore, the 5% failed first, 21% failed fourth, and 81% failed sixteenth. The 5% and 21% failure ranks are less than 25% failure rank. First through fifth failures have a danger of being early EM failures depending on the failure kinetics compared to the rest of the group. The 5% failure rank sample shows a high concentration of red color, highlighting the regions of the grain orientations that align closely with the [001] direction compared to those of 21% and 81% failure rank samples.

In addition, the shade of red color for 21% failure rank sample is darker than that in the 5% failure rank sample. The cluster of Sn grain orientation of the red color is farther away from the [001] orientation on the inverse pole figure. The darker red color and the cluster farther away from the [001] corner mean that 21% failure rank sample has a Sn grain orientation that is more off-angled from the c-axis than that with the 5% failure rank sample is. In addition to the Sn grain orientation that is more off-angled to [001], the blue color grain orientation is not aligned with the c-axis, causing a slower diffusion rate. The crystal orientation map of the 81% failure rank sample in Fig. 3-4 (c) does not show any red color, not having any c-axis alignment. The concentration of c-axis alignment decreases as failure rank increases from 5% to 81%. This phenomenon clearly indicates that the alignment of the c-axis with the direction of the current is the controlling EM failure mechanism that determines the EM failure kinetics of early EM failures.

The EM failure mechanism of c-axis alignment can be explained by Black's equation that is mentioned in early Section 1.4.2. Since Cu diffusion through the c-axis requires a lower activation energy, the Cu starts to diffuse faster through the c-axis than it does through the other two axes. The lower required activation energy and resulting accelerated EM failure kinetics lead to early failures that reduce the MTTF of the test group. The SAC solder interconnects with a c-axis alignment are responsible for early EM failure and discrepancies in the EM reliability prediction calculations and models.

3.3. Conclusion

The early EM failures of WCSP samples are studied with SEM and EBSD analysis to better understand the early EM failure mechanism. The cumulative probability data and the log-normal distribution data show that early failures have a different EM failure

mechanism and kinetics. Early failures give biased MTTF and shape factor data. EBSD analysis suggests that samples have faster EM kinetics with a higher concentration of c-axis alignment with EM direction. EBSD results of first failed sample show a high degree of c-axis alignment of the Sn grain orientations with the EM direction. The sixteenth failed sample does not have any c-axis alignment of Sn grain orientations. This difference clearly shows the important role that the c-axis alignment with the EM direction plays in controlling the EM failure kinetics responsible for early failures. The relatively larger diffusion path along the c-axis and its lower required activation energy explain the fast EM diffusion rate along the c-axis compared to the a and b axes. It is important to identify and exclude early EM failures from statistical calculations to get an accurate understanding of the experimental package structure parameter and its effects on the EM reliability and the EM failure mechanism. To improve the EM reliability of an electronic package, it is important to find a simple and effective method to remove Sn's c-axis alignment with the EM direction to prevent early failures which otherwise skew EM reliability calculations.

Chapter 4

Mitigating Early EM Failures of WCSP: Effects of Cu Substrate on Reflowed SAC Solder Balls

4.1. Simple and Effective Way to Prevent Early EM Failures

The previous chapter and the paper titled “Relationship Between the Grain Orientation and the Electromigration Reliability of Electronic Packaging Interconnects” confirm that the c-axis alignment near the Cu UBM and SAC solder interface causes early EM failures, defying an accurate EM reliability prediction [32]. Therefore, it is very important to determine how to prevent those early detrimental failures. A simple approach to removing the c-axis alignment near the Cu and SAC interface is to manipulate the Sn grain orientations so that they would have preferred orientation away from c-axis. The method chosen uses a substrate that SAC solder will be reflowed on because if its effect is proven to be successful, then it would be a simple yet effective way to eliminate Sn’s fast EM diffusion grain orientation effects. If using a textured Cu substrate can cause reflowed Sn to have a preferred orientation, then it would be a simple and effective method to increase reliability of a package by eliminating the possibility of early failures.

There have been several studies to achieve a specific the grain orientation of various metals using different textured substrates and deposition methods [58]–[69]. Lu, Shen, Wu, and Chen report a method to fabricate unstable (111) oriented nanotwinned Cu film using DC electroplating for lower thermal stability to prepare (100) oriented Cu thin film [58]. Viloan, Helmersson, and Lundin report different ion acceleration methods

to achieve (111) and a mixed (111) and (200) textured Cu thin film depositions using high-power impulse magnetron sputtering (HiPIMS) [59]. Wei, Huang, Woo, Zheng, Wen, and Zhang report to deposit a mixed (111) and (110) textured Cu thin film with a direct current magnetron sputtering [70]. Du and Li report to achieve a dominant (111) textured deposited Cu thin film to decrease the (111) and increase the (110) Cu grain by annealing [62]. Lee et. al. showed that it is possible to grow (111) textured single crystal Cu thin films on a sapphire substrate using RF sputtering techniques with a single crystal Cu target [64]. Vanstreels et. al. reports a super secondary grain growth that increases the (111) texture in a thick sputtered Cu thin film using high-sputter-bias conditions [68]. Ito, Umezawa, and Nakanishi report that the time of flight impact-collision ion scattering spectroscopy (TOF-ICISS) can be used to achieve heteroepitaxial growth of Ag on (111) textured Ni substrate [63]. They report finding a heteroepitaxial growth of [11$\bar{2}$] and [$\bar{1}\bar{1}$2] Ag on Ni substrate by using different substrate temperature during deposition. Mróz, Jankowski, and Nowicki report a physical vapor deposition of (111) oriented Ag on (111) textured Ni substrate [65]. Most of them are focused on thin films with different deposition methods.

While some deposited metals show a promising preferred grain orientation, the lack of studies on reflowed SAC solder on various substrates gives void in the understanding [71]–[74]. The following four studies show a promising substrate effect that can be used for manipulating reflowed Sn grain orientation. Hu, Yang, Kang, Hu, and Li investigate the effects of (100) and (110) textured Cu substrates on the Cu/Sn IMC growth [71]. Cu_6Sn_5 IMC are all rounded yet more protruded with (100) Cu substrate, which indicate a lower interfacial energy for Cu/SAC interface with (100) Cu substrate. Qiao, Liu,

Ma, and Zhao study and report that temperature gradient and multi-reflow process are keys to control Sn grain orientation in micro solder joints during reflowing process [72]. Zhong et al. report a strong preferred growth of Cu_6Sn_5 IMC by reflowing with a (111) textured Cu substrate under a temperature gradient [73]. As a result of the reflow process with temperature gradient, Cu_6Sn_5 IMC has a strong preferred orientation of $[11\bar{2}0]$ parallel to the direction of temperature gradient. Hsu, Zeng, Xian, Belyakov, and Gourlay investigate the effects of Cu or Ni substrates on the Cu_6Sn_5 IMC orientation [74]. Cu_6Sn_5 IMC shows strong preference toward [0001] on Cu substrate and has strong preference toward $[10\bar{1}0]$ on Ni substrate. Based on these articles, the textured Cu substrate effect is investigated as a strong candidate to manipulate Sn grain orientation during reflow process. The results are discussed in following sections.

4.2. Samples and Experimental Setup

Sn grain orientations of SAC solder balls reflowed on Cu substrates are analyzed through EBSD analysis to study a substrate effect. The SAC solder balls are reflowed on different types of Cu substrates to mimic the interface of Cu and SAC in the SAC solder interconnects. The four different types of Cu substrates are used to study. The first is a polycrystalline Cu substrate, using a regular PCB, for a regular SAC solder interconnect condition without any substrate effect. The second is differently textured single crystal Cu substrates to see the effects of substrates on SAC grain orientation. The single crystal Cu substrates have three different textures, (111), (110), and (100), to further study the effectiveness among different textured Cu substrates. Furthermore, the different sizes of SAC solder balls are reflowed, ranging from 200μm to 760μm, to compare the effectiveness of substrate effect on various SAC solder ball sizes.

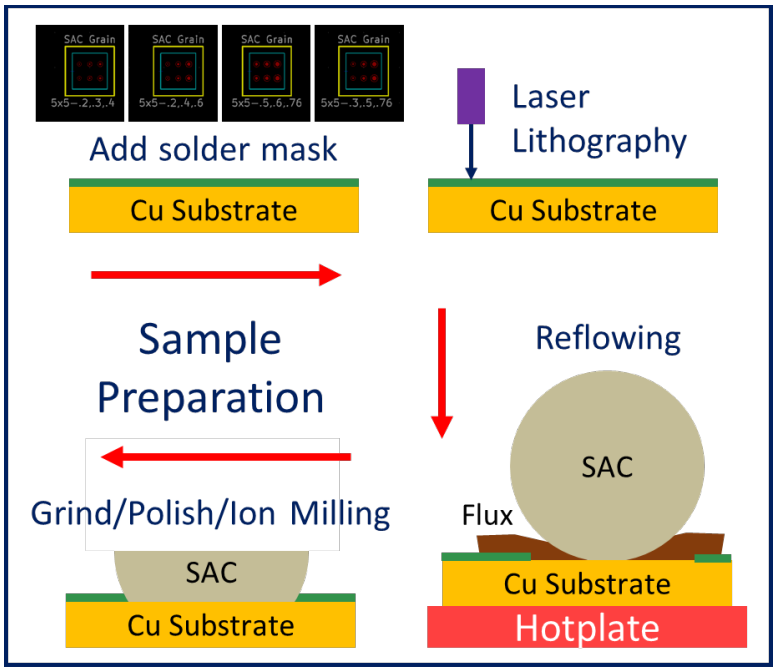


Figure 4-1. An illustration of sample preparation steps for the Cu substrate effect study.

At first, the Cu substrates are polished using 0.05μm alumina to achieve a smooth surface. As shown in Fig. 4-1, the solder masks are lithographed on the Cu substrates with a solder mask pattern with different opening diameters for different SAC solder ball sizes. Once the lithography is done, the flux is applied, and the appropriated SAC solder balls are placed on the openings. The samples with SAC solder balls go through a reflow process on a hotplate with a peak temperature of 300°C for 10 minutes. Once the reflow process is finished, the crystal bond is used on the sample surface as a mold to provide supports on the SAC solder balls against shear forces during grinding and polishing. The SAC solder balls are ground and polished in the top-down view with a modified CNC (computer numerical control) machine with grinding and polishing pads. This sample preparation method allows the EBSD analyzation of multiple SAC solder balls. As a final sample surface preparation method, the crystal bond is melted in acetone, then the sample is ion milled for EBSD analysis.

4.3. Results and Discussions

The EBSD analysis is performed to investigate the Cu substrate effects on the reflowed SAC solder balls, mimicking SAC solder interconnects' Cu and SAC interfaces. Fig. 4-2 shows the EBSD results of the Sn grain orientation of SAC solder balls reflowed on a polycrystalline Cu substrate. The SAC solder ball typically consists of three to four SAC solder grains. The Sn grain orientation is widely distributed despite the different SAC solder ball sizes. As expected, the polycrystalline Cu substrate does not cause any Sn grain orientation preference in reflowed SAC solder balls. Sn grain orientations of SAC solder ball reflowed on polycrystalline Cu substrate for 400μm SAC solder ball are [102], [213], [331], [552], [612], [314], [312], and [531]. The 760μm SAC solder ball has grain orientations of [311], [411], [431], [100], [103], [210], [311], [411], [302], [101], [105], [331], and [313]. The EBSD analysis clearly shows that the SAC solder reflowed on polycrystalline Cu substrate has random grain orientations regardless of SAC solder ball sizes. On the other hands, the textured single crystal Cu substrate show a tightly distributed Sn grain orientation for smaller reflowed SAC solder balls.

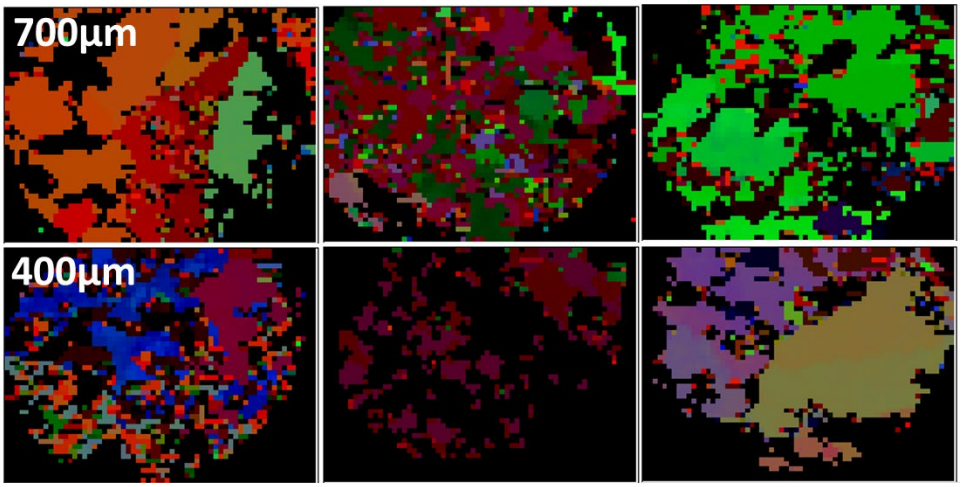


Figure 4-2. EBSD results of Sn grain orientation of SAC solder reflowed on polycrystalline Cu substrate.

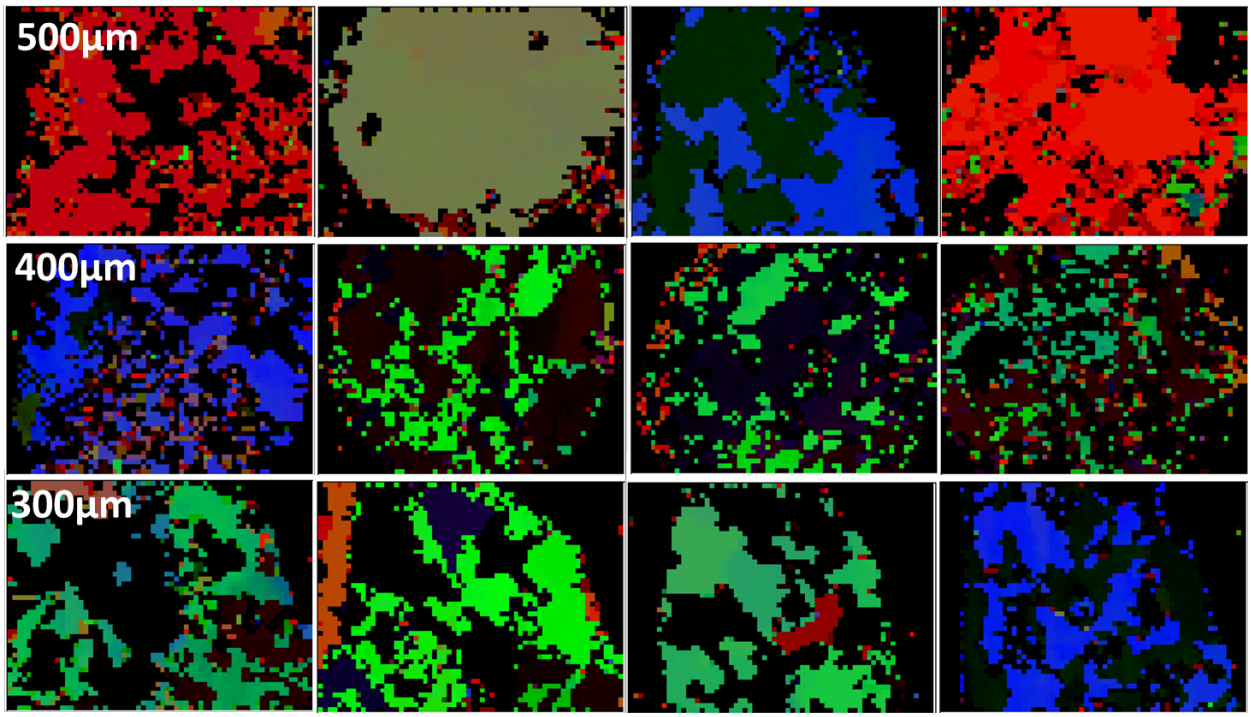


Figure 4-3. EBSD results of Sn grain orientation of SAC solder reflowed on (111) textured single crystal Cu substrate.

Fig. 4-3, Fig. 4-4, and Fig. 4-5 show the EBSD results of the (111), (110), and (100) textured single crystal Cu substrates, respectively. While none of textured Cu substrates causes a preferred Sn grain orientation in bigger SAC solder balls, 400µm and smaller SAC solder balls appear to give a biased grain orientation. The (111) textured Cu substrate with 400µm and smaller SAC solder balls gives two major grain orientations, indicated with green and blue colors in Fig. 4-3. The (111) textured Cu substrate has Sn grain orientation of [771], [701], [101], and [410] for 400µm SAC solder ball and [310], [100], [721], and [110] for 300µm SAC solder ball. Compared to (111) textured Cu substrate, (110) and (100) textured Cu substrates have a weaker Sn grain orientation preference. The (110) textured Cu substrate have a roughly four preferred Sn grain orientation, including a dangerous [001] grain orientation starting from 300µm SAC solder substrates. They are blue, red, dark red, and green colors. The bright red from Fig. 4-4

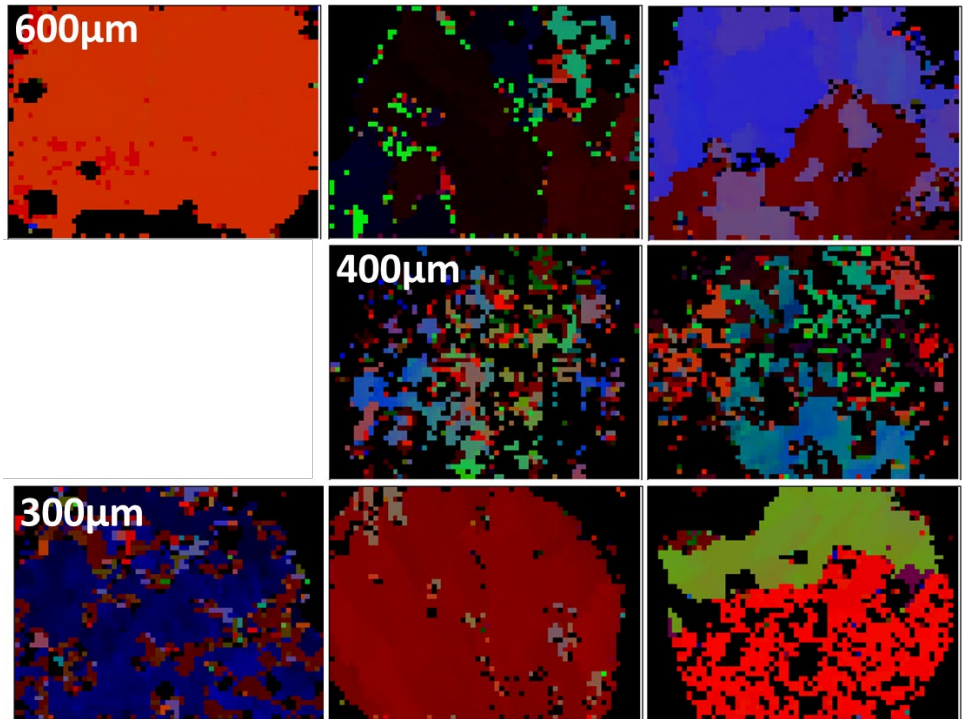


Figure 4-5. EBSD results of Sn grain orientation of SAC solder reflowed on (110) textured single crystal Cu substrate.

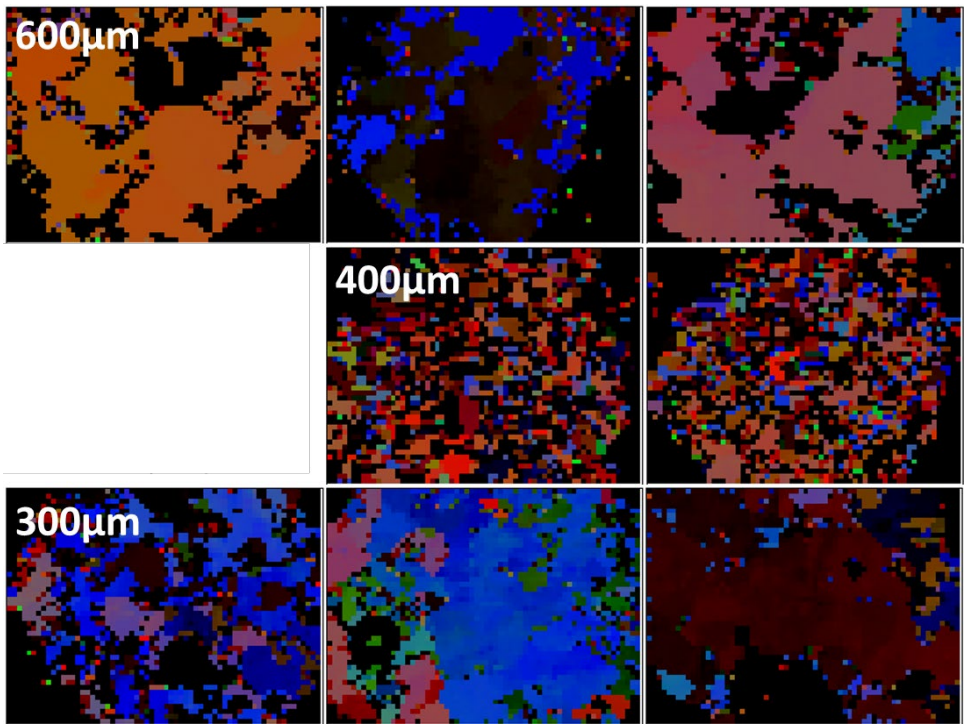


Figure 4-4. EBSD results of Sn grain orientation of SAC solder reflowed on (100) textured single crystal Cu substrate.

indicates the dangerous Sn's c-axis. The (110) textured Cu substrate has Sn grain orientation of [741], [621], [210], and [112] for 400μm SAC solder ball and [431], [542], [211], [001], and [301] for 300μm SAC solder ball. The 300μm SAC solder balls reflowed on (100) textured Cu substrate seem to have two grain orientations, dark red and blue colors in Fig. 4-5. However, the blue color is not one solid blue color, but a shade of blue color. The shade of blue color indicates the Sn grain orientation is widely distributed. As a result, the (100) textured Cu substrate has biased Sn grain orientations of [312] and [553] for the 400μm SAC solder ball and [761], [321], [320], and [543] for the 300μm SAC solder ball.

The 300μm SAC solder balls' inverse pole figure (IPF) heatmaps are overlapped in Fig. 4-6. The overlapped IPF heatmaps further support that the (111) textured Cu substrate is the best candidate, giving the most biased Sn grain orientations. It has only two preferred Sn grain orientations near [110] and [100] with very tight distribution. The IPF heatmaps of a (110) textured Cu substrate shows roughly four preferred Sn grain orientations including a dangerous [001] grain orientation with a tight distribution. The (100) textured Cu substrate's IPF heatmaps reveal that it has a wide distribution of Sn

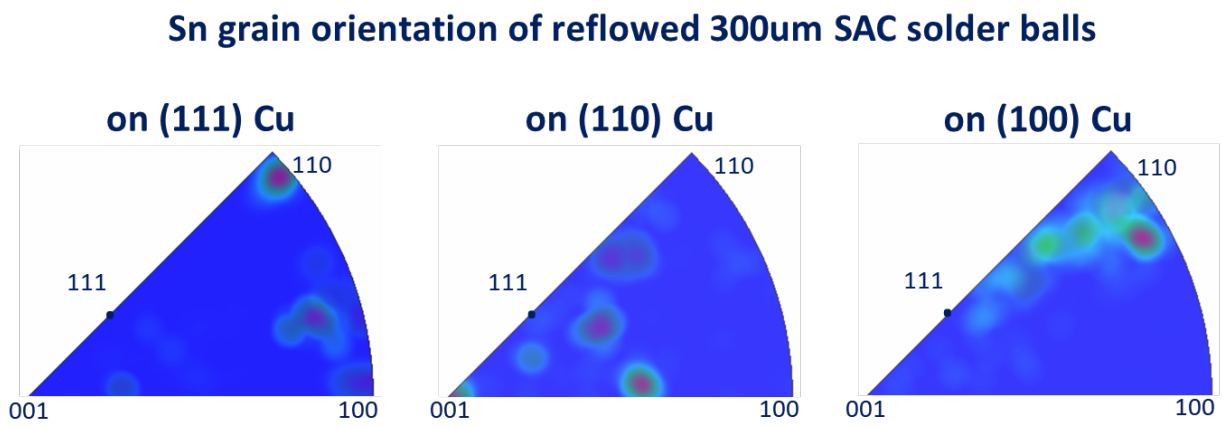


Figure 4-6. The overlapped inverse pole figure (IPF) heatmap of 300μm SAC grain orientation that is reflowed on single crystal Cu substrate.

grain orientations with scattered preferred grain orientations between [111] and [110]. The IPF heatmaps of 300μm SAC solder on three Cu substrates reinforce that (111) is the best textured Cu substrate to prevent early EM failures to remove c-axis in Sn grain orientation. (110) textured Cu substrate seems to be the second best, yet the c-axis orientation preference causes the (110) Cu substrate to be an unsuitable candidate to prevent the c-axis alignment. Therefore, the (100) textured Cu substrate is the second-best candidate to prevent the c-axis alignment of Sn. A continuation of this study is necessary to better understand the underlying mechanism causing the Sn grain orientation preference on textured single crystal Cu substrate for smaller SAC solder balls.

4.4. Conclusion

The fast EM diffusion through Sn's c-axis causes the early EM failures within SAC solder interconnects. The early EM failures have different EM failure mechanisms from the remaining samples in the test group which fail later in the accelerated EM tests. Early failed samples are known to yield biased test data of MTTF and shape factor. The early EM failure mitigation effort of substrate effect is studied to remove the c-axis alignment using the Cu substrate effect to manipulate reflowed SAC's Sn grain orientation. The EBSD analysis reveals that the polycrystalline Cu substrate yields a random Sn grain orientation for all different SAC solder ball sizes. The EBSD analyses of textured single crystal Cu substrates clearly show that there is a substrate effect that affects Sn's grain orientation as the SAC solder reflows onto the Cu substrate. The textured Cu substrates is a simple and effective method to remove early EM failures by giving biased Sn grain orientation. It can be used in SAC solder interconnect assembly to prevent early EM failures without changing packaging structure parameters. The tight distribution of four

preferred grain orientations of (110) textured single crystal Cu seems to be a good candidate. However, one of the preferred grain orientations is the c-axis, which is a major factor causing early EM failures. Therefore, it is actually not a good candidate. The (100) textured single crystal Cu substrate does not have a c-axis grain orientation preference, yet the preferred grain orientation spreads widely between [111] and [110] orientations. The best candidate to incorporate in SAC solder interconnects assembly to prevent early EM failures is the (111) textured single crystal Cu substrate. It has two preferred Sn grain orientation near [110] and [100] with a very tight distribution.

Chapter 5
SAC Solder Interconnect EM Failure Mechanism and Microstructure Changes under Low-Frequency Pulsed DC

5.1. Background

There are many prior studies about EM in efforts to understand contributing factors and their effects on EM failure mechanisms and kinetics. As mentioned in earlier chapters, those factors include stress, interface microstructure, grain orientation of Sn, types of alloying elements, the degree of JH, the rate of IMC formation, among others [1]–[3], [7], [14], [18], [19], [26], [32], [75]–[80]. Most EM studies are conducted under DC load conditions like those presented in Chapters 2 through 4. Because of this, there is a lack in understanding the effects of EM under non-DC load conditions [26]. Therefore, the EM reliability of packages under non-DC load conditions has often been assumed by extending the understanding of DC load condition studies and applying them to non-DC conditions.

Since there is a select few EM studies under non-DC load conditions, the exact EM failure mechanism is not fully understood [81]–[84]. For EM failure kinetics and mechanisms under pulsed DC, the microelectronic package industry often accepts and modifies a common assumption called the cumulative damage model that is developed from DC EM studies. The cumulative damage model only accounts for EM damage during the “on” time and assumes that zero damage accrues during the “off” time. The cumulative

damage model assumes that there is an inverse linear relationship between the EM lifespan and the pulsed-DC duty factor (DF), a ratio of the “on” time per cycle.

The assumption of using the cumulative damage model is a logical yet a detrimental one. The assumption is made and accepted because of the lack of commercially available constant current pulsed-DC power supplies and the difficulty of setting up the accelerated EM tests. The various factors of package structure parameters affecting the EM mechanisms further complicate making accurate EM failure models and EM reliability assessments. As a results, various studies of pulsed-DC show results contradicting each other while also contradicting previously made assumptions [85]–[93]. Most of the studies either have limited data, not having statistical importance, or use excessively aggressive assumptions [9], [84], [90], [92], [94]–[97]. Tao, Cheung, and Hu show a defect relaxation model for pulsed DC of Al-2%Si, Al-4%Cu/TiW, and Cu system [84]. Tao, Cheung, and Hu say that the defect relaxation time, τ, is exponentially dependent on temperature and is determined by material characteristics and microstructures. He reports that samples tested under pulsed-DC conditions have longer MTTFs than those under DC load conditions. Thus, the cumulative damage model assumption may prove to be incorrect for the reliability assessment. The non-DC effects on EM study are necessary to obtain an applicable reliability model under pulsed-DC. The lack of understanding of EM under non-DC load conditions may lead package design toward the wrong direction. The importance of understanding non-DC effects on EM failure mechanisms motivated this research.

The metallurgical and structural parameters that affect the EM failure mechanism, such as CTE mismatch driven stress, temperature, and chemical potential gradient, can

be relaxed during the “off” time of pulsed-DC. This means that EM damage progress can be either repaired or exacerbated by the combination of these parameters with EM. This combination may affect the EM failure mechanism and kinetics in unexpected ways even though the common expectation is an overall improvement in EM reliability under pulsed-DC conditions compared to that under DC conditions.

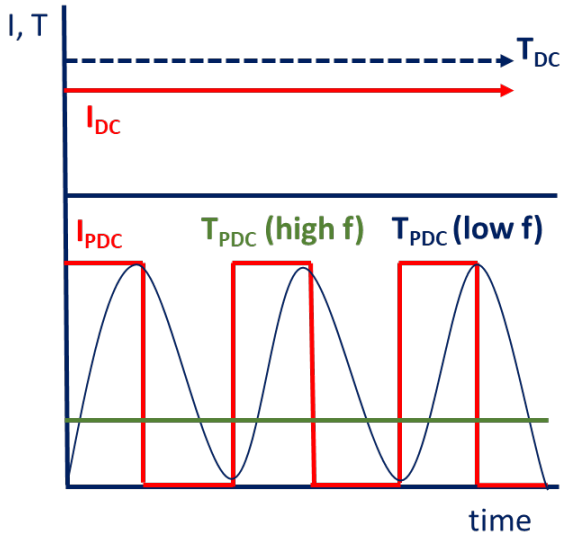


Figure 5-1. The graph illustrates current types and temperature changes for DC, pulsed DC at high frequency, and pulsed DC at low frequency.

Among the multiple factors, the one key factor that is important to consider for pulsed-DC effects on EM is the temperature change. As shown in Fig. 5-1, DUT under DC load is in isothermal condition and can be described well with the Black’s empirical equation with some modifications for specific situations. However, the DUTs tested under low-frequency pulsed-DC conditions are thereby tested under non-isothermal conditions. The temperature fluctuation can complicate the EM failure kinetics because of the thermal stress involvement. On the other hand, the DUTs tested under high-frequency pulsed-DC conditions are under isothermal conditions like that of DC because the thermal constant

is not high enough to have a temperature change with the very short current “on” and “off” times.

5.2. Expectations

Even with the studies supporting the cumulative damage model, it is predicted that there are more complicated effects of the pulsed DC load condition on EM mechanism and reliability because of thermal stress fluctuation from the temperature fluctuation. Furthermore, the metallurgical, thermal, chemical, and structural parameters, such as the CTE mismatch-driven stress, temperature, and chemical potential gradient, can be dormant during the “off” period of a cycle. These mechanisms can have complicated effects on EM by either repairing or exacerbating EM damage, affecting EM failure kinetics and mechanisms. Even though a common expectation of pulsed-DC’s effects on EM failure rate is an overall decrease in failure rate compared to that of DC, metallurgical and structural parameters may affect the EM failure kinetics and mechanisms in unexpected ways. A comparative study is conducted to investigate the effects of pulsed-DC on EM failure kinetics and to study EM failure mechanism changes under pulsed-DC. The comparative study tests the validity of the assumption of the cumulative damage model of EM under pulsed DC and provide better understanding of EM failure mechanisms and kinetics under pulsed DC to enhance package design rules.

5.3. Experimental Setup

A comparative accelerated EM study with various frequencies and DFs is conducted to investigate the uncertainty of the pulsed-DC effects on EM behavior and to validate the assumption of the cumulative damage model. WCSP samples with 230μm

SAC solder ball and 18μm bare Cu UBM are tested. The samples are tested at 165°C with a current density of 9.63kA/cm^2. The pulsed-DC EM tests are completed under 10,000Hz with 50% DF and 0.1Hz with 33%, 50%, 75%, and 100% (DC condition) DFs. DF is a ratio of “on” period to “off” period in a cycle of pulsed DC. For example, 75% DF of 0.1Hz, which has a 10 second period per cycle, means that there are 7.5 seconds of “on” period and 2.5 seconds of “off” period. 0.1Hz 50% DF and 33% DF respectively have 5 seconds of “on” period and 5 seconds of “off” period, and 3.3 seconds of “on” period and 6.7 seconds of “off” period. The 10,000Hz pulsed DC EM test ran over 10,000 hours and stopped because no significant EM damage is observed in samples.

One of the most challenging parts of conducting accelerated pulsed-DC EM tests is to create and apply constant current pulsed-DC with the square waveform to samples because a power supply that can generate such a current is not commercially available or what is available is very expensive and has limited functionalities. Therefore, a pulsed-DC generating PCB module shown in Fig. 5-2 (a) is designed and produced to generate the square waveform pulsed DC with desired frequency and DF. The PCB module is connected in between the DC power supply and test samples. The simple and detailed schematics of the PCB module are shown in Fig. 5-2 (b) and (c). The crowbar circuit that is incorporated inside the PCB module generates the behavior of a square waveform pulsed-DC. The PCB consists of a MOSFET (SCT3080ALGC11), a MOSFET driver (IXDN614PI), an Arduino Uno, a step-up adjustable DC-DC converter (MT3608), a heatsink (E2A-T247-38E), a 40x20x20 mm computer fan, capacitors, and resistors. 12V DC is supplied to power the Arduino Uno, the computer fan, and the MT3608. The Arduino Uno is a function generator that can act as a PWM with an appropriate program.

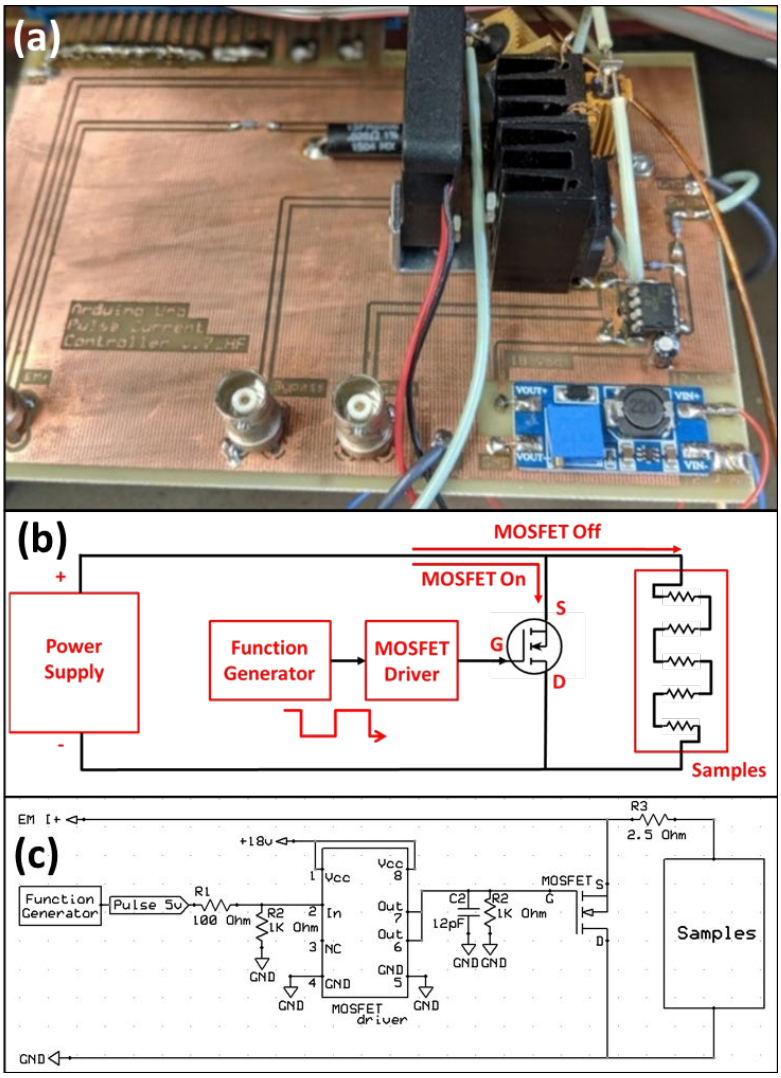


Figure 5-2. (a) shows the pulsed direct current generating PCB module. (b) shows general circuit connection of pulsed direct current PCB module. (c) shows the detailed circuit schematic of pulsed direct cur-rent module. The 18V is supplied to MOSFET driver. Function generator acts as a pulse width modulation (PWM) and sends 5V or 0V to the MOSFET driver. According to PWM inputs, the MOSFET driver sends outputs (18V or 0V) to open or close the MOSFET. When the MOSFET is opened, the accelerated EM test current flows through the samples, acting as “on” condition. When the MOSFET is closed, the accelerated EM test current bypasses the samples to the ground, acting as the "off” condition.

STC3080ALGC11 N-MOSFET is chosen because it has high drain-source voltage (600V), wide range of gate-source voltage (DC) (-4V to +26V) with a recommended drive voltage (V_{gs_op}) of 0V and +18V. The static drain-source on-state resistance is low (80mΩ at 25°C) when V_{gs_op} is +18 V. The IXDN614PI MOSFET driver has very short rise time (25ns) and fall time (18ns). As shown in Fig. 5-3, it also has one input to control two outputs with

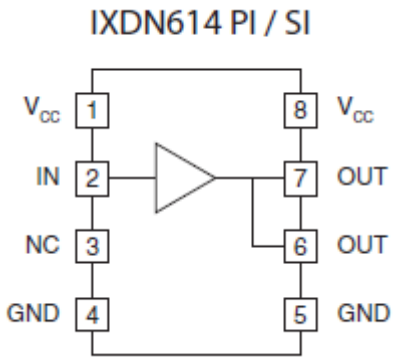


Figure 5-3. Illustration of the MOSFET driver's (IXDN614PI) pin configuration.

same polarities with wide range of supply voltage (-0.3V to +40V) and output current (±14A).

With an Arduino program that I wrote, which is mentioned earlier in Chapter 1, the Arduino Uno can output a pulsed square waveform of desired frequency and DF appropriate for a test condition with 0V and 5V. Fig. 5-3 shows the MOSFET driver's pin configurations. The 0V or 5V output is applied to MOSFET driver's (IXDN614PI's) logic input pin, pin number 2. The MT3808 boosts 12V DC to 18V DC. The boosted 18V is applied to the MOSFET driver's power input pins, pin number 1 and 8. Since the MOSFET driver has a regular input and output logic, 5V from the Arduino Uno to logic input pin turns on the output of the MOSFET driver, supplying 18V to the MOSFET's gate. The 18V of gate-source voltage of the MOSFET closes the source and drain channel, allowing current to flow from the source to drain of the MOSFET. The EM test current, DC from a power supply, passes through the source and drain of the MOSFET to ground, bypassing the samples and mimicking the "off" stage of pulsed-DC. On the other hand, when 0V is applied to the MOSFET driver's logic input pin, the driver has 0V output, causing the gate-source voltage of the MOSFET to be 0V. The MOSFET's source and drain is opened, shutting off any current flow, and the test current bypasses the MOSFET and passes

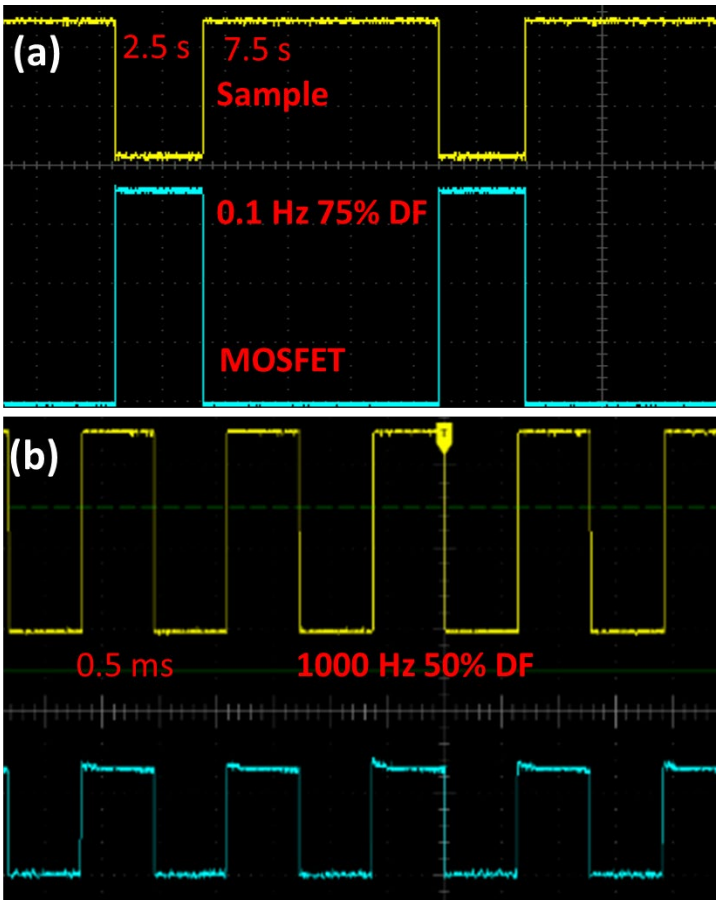


Figure 5-4. Oscilloscope images of the square waveform pulsed direct current test current of (a) 0.1Hz 50% DF and (b) 1000Hz with 50% DF.

through the samples, mimicking the “on” stage of pulsed-DC. The MOSFET and resistors are attached to the heatsink. The 40x20x20 mm computer fan is positioned next to the heatsink to cool down both the MOSFET and resistors. With this configuration of the crowbar circuit in the pulsed-DC generating PCB module, a pulsed-DC EM test current with square waveform without distortion is produced. The oscilloscope of produced pulsed-DC are shown in Fig. 5-4. The Table 5-1 shows the accelerated EM test matrix for the comparative study of pulsed-DC effect. Each test condition consists of 20 WCSP samples which are serially connected.

Table 5-1. shows the accelerated EM test matrix for investigating pulsed DC effects on EM failure mechanisms.

Sample Structure		Test Conditions			
UBM Cu, µm	UBM Ni, µm	Temperature, °C	Current Density, kA/cm^2	Frequency, Hz	DF, %
18	0	165	9.63	0 (DC)	N/A
				10,000	50
				0.1	33
				0.1	50
				0.1	75
				0.1	100

5.4. Results and Discussions

5.4.1. Temperature Change Measurement

Since the temperature of the DUT changes as the current switches between “on” and “off”, the amplitude of the temperature change within the DUT is calculated at different frequencies at 50% DF to find a trend of DUT temperature change as frequency changes. Resistance temperature detector (RTD) within the samples’ DUT is used to measure the resistance at a specific temperature with 2 mA current. The five different resistances are measured with corresponding five temperatures. The measured resistance is converted to voltage using Ohm’s law,

$$V = IR \tag{5-1}$$

where V is voltage, I is current, and R is resistance. Since the resistance of the DUT scales monotonically as temperature increases, the voltage also changes linearly. The five different voltages are measured at five different temperatures to calculate a linear fit equation. The linear fit equation is then used to calculate the temperature of the DUT under pulsed-DC at a certain frequency. The DUT temperature change is measured at various frequencies ranging from 0.0033Hz (300 seconds period) to 1000Hz (0.001 second period). Fig. 5-5 (a) shows a graph of RTD’s voltage change with gate’s voltage

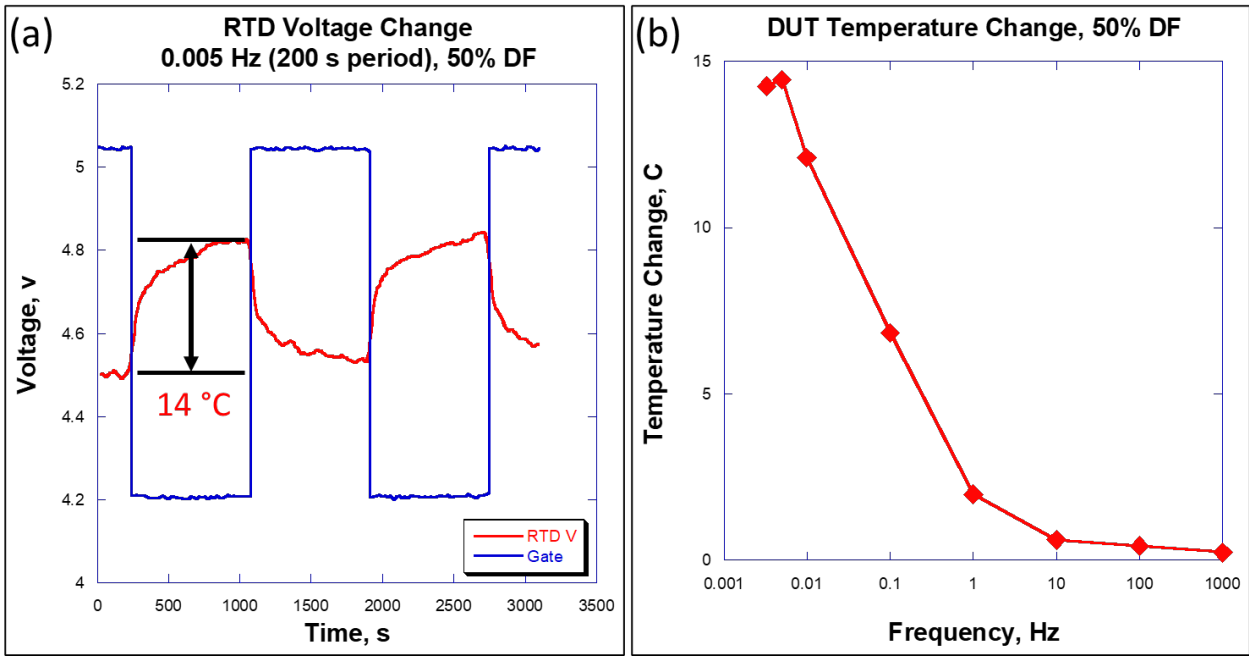


Figure 5-5. (a) Graph of RTD's voltage change at 0.005Hz 50% DF for calculating DUT temperature change. (b) Graph of calculated DUT temperature change with various frequencies, ranging from 0.0033Hz to 1000Hz, at 50% DF.

change at 0.005Hz 50% DF. The 0.005Hz 50% DF pulsed DC induces 14°C of temperature change within DUT as the current turns on and off by using a calculated linear-fit equation. Fig. 5-5 (b) shows calculated DUT temperature changes at various frequencies. There are two plateaus; one is when frequency is higher than 10Hz, and another is when frequency is lower than 0.005Hz. DUT temperature change plateaus at 0.005Hz and lower with 14°C and at 10Hz and higher with 1°C of temperature change. It shows that DUT temperature change depends on frequency. Based on these measurements, the DUT which is tested under high-frequency pulsed-DC conditions, higher than 10Hz, would have a constant temperature and a lower effective temperature. Meanwhile, the DUT which is tested under low-frequency pulsed-DC conditions, lower than 0.005Hz, would have a temperature fluctuation with a target effective temperature. The test conditions, which are 10,000Hz and 0.1Hz, would have 1°C and 7°C of DUT temperature changes, respectively.

The high frequency pulsed DC EM test, which is tested at 10,000Hz 50% DF, has an extremely slow failure rate to a point that there were not any failures even after 10,000 hours. Therefore, the high-frequency pulsed-DC EM test is suspended in order to conduct other tests. The 14°C low effective DUT temperature seems to partially explain the extremely slow failure rate along with a constant DUT temperature and a halved current density compared to the DC EM test condition.

5.4.2. EM Failure Kinetics Dependence on Duty Factors

The cumulative damage model assumes that samples tested under pulsed-DC with a 33% DF would have 3 times longer EM lifespan than those under DC load conditions, or 100% DF. It also says that samples tested under pulsed-DC with a 75% DF would have 1.3 times longer EM failure time than those under DC load conditions, or 100% DF. However, the comparative EM study results contradict this assumption of a

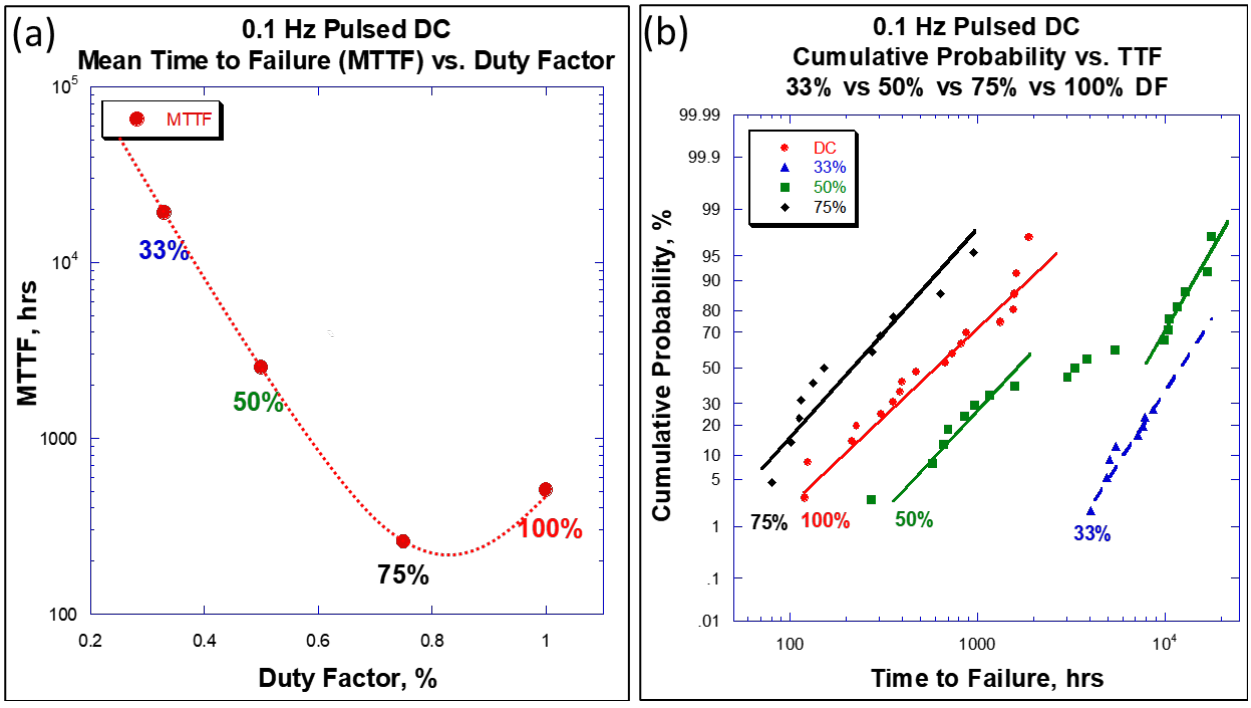


Figure 5-6. Graph of (a) mean time to failure vs. duty factor (DF) and (b) cumulative probability vs. time to failure.

cumulative damage model. Fig. 5-6 (a) and (b) shows graph of DF as a function of MTTF and graph of TTF as a function of cumulative probability, respectively. Fig 5-6 clearly exhibits the highly nonlinear relationship between DF and EM under pulsed-DC load conditions. The most notable thing is that 75% DF samples fail even faster than samples under DC conditions. This suggests that there is an EM failure acceleration mechanism that dominates and controls EM failure kinetics at high DF under low-frequency pulsed-DC. The difference of MTTF and TTF between 75% DF and 100% DF data is significant to dismiss experimental errors. On the other hand, 33% DF fails extremely slowly compared to other DFs. The MTTF of samples tested under 33% is exponentially increased compared to those tested under the other two pulsed-DC DFs and 100% DF or DC. This shows a change in EM failure mechanism from EM acceleration to EM deceleration mechanism as the DF decreases. Furthermore, the slope changes the in the cumulative probability of samples tested under the pulsed-DC 50% DF condition in Fig 5-

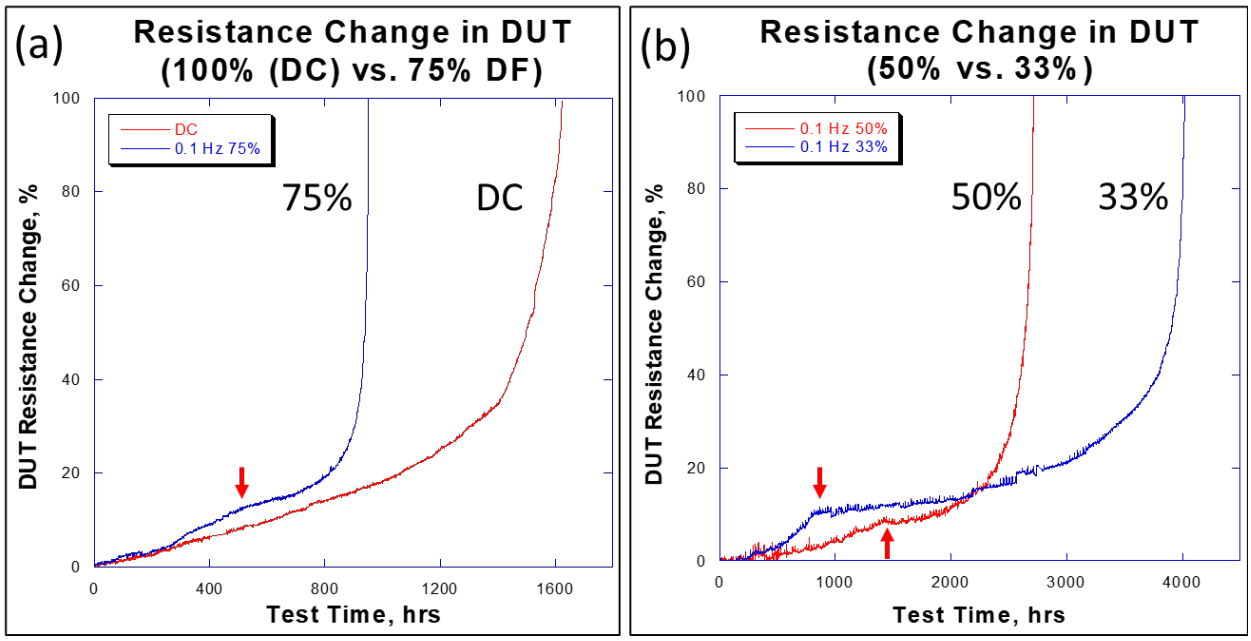


Figure 5-7. Graphs of the resistance change in DUT as a function of test time for (c) 75% and 100% DF and (d) 33% and 50% DF.

6 (b) between early half failures and late half failures further supports that there are two EM failure acceleration and deceleration mechanisms. The slope of early half failures of 50% DF samples matches that of 75% DF samples, indicating that they share a similar EM failure mechanism. The similar slope of late half failures of 50% DF and 33% DF supports that they share the same EM failure mechanism. The two EM failure mechanisms are competing with each other in determining EM failure kinetics; one is accelerating the EM failure kinetics, and the other is decelerating the EM failure kinetics.

Further evidence of the EM failure acceleration and deceleration mechanisms is observed in the resistance changes within the DUT over time. Fig 5-7 shows the percentage change in the resistance within DUT as a function of the test time. The 100% DF, which is DC condition, shows a classical 1-stage EM failure curve. However, all the pulsed-DC DF conditions show 2-stage EM failure curves, further supporting the competition between two EM failure mechanisms. The red arrows in the Fig 5-7 marks positions where resistance change rate changes.

5.4.3. EM Failure Acceleration Mechanism by Mechanical Fatigue

The cross-sectional failure analysis of microstructural morphology introduces additional evidence of an EM failure acceleration mechanism. The cross-sectional SEM images of samples tested under 50% and 100% DF low-frequency pulsed-DC show the classical EM failure features of void nucleation at the current crowding region and void propagation across the interface of Cu UBM and SAC solder in Fig 5-8 (c) and (d). Unlike microstructure of 50% DF and 100% DF, 75% DF samples in Fig 5-8 (a) and (b) shows the conventional EM void nucleation and propagation to a certain critical void length before crack-induced failure. The crack through SAC solder consists with failure feature

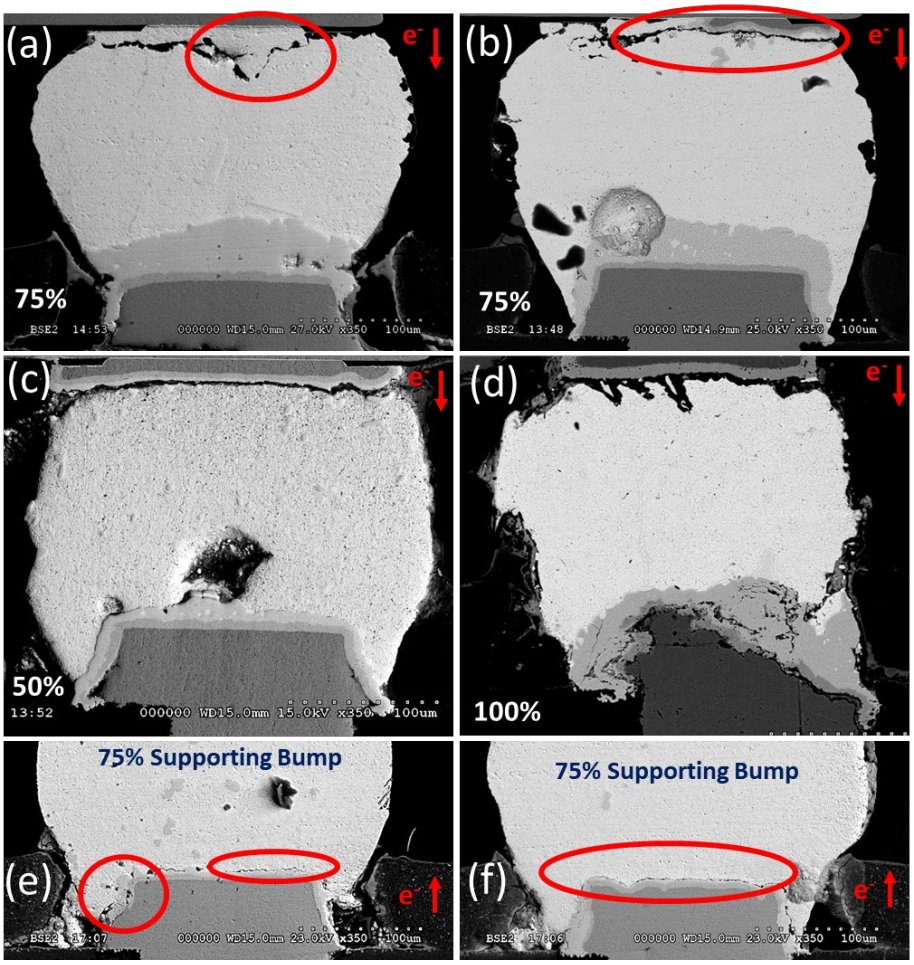


Figure 5-8. Cross-sectional SEM pictures in BSE mode. DUT tested under 0.1Hz at (a) and (b) 75% DF, at (c) 50% DF, and at (d) 100% DF (DC). Supporting bumps tested under 0.1Hz at (e) and (f) 75% DF.

of mechanical fatigue, indicating an involvement. Similar to the UBM thickness effect study in Chapter 2, the DUT is under compression, while the surrounding bumps are under tension. The evidence of tension involvement is observed by cracks near the Cu vias in the supporting bumps shown in Fig. 5-8 (e) and (f). Therefore, the cross-sectional SEM images of the 75% DF samples suggest that mechanical fatigue is involved and most likely accelerates EM failure kinetics under a high DF low-frequency pulsed-DC load condition.

Based on the DUT temperature change measurement, SEM failure analysis, and MTTF data, the following EM failure acceleration mechanism is proposed for solder

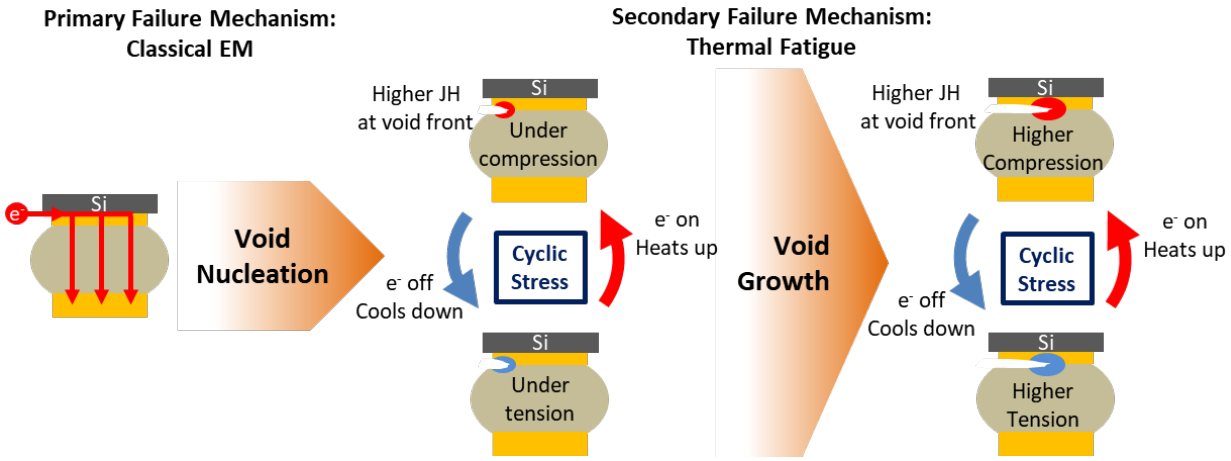


Figure 5-9. The illustration of EM failure acceleration mechanisms under pulsed DC at high DF, which is the combination of void nucleation, void propagation, and mechanical fatigue.

interconnects under pulsed-DC at high DF in Fig. 5-9. As the void propagates, the interfacial current path decreases. The reduced path increases local current density and local JH. The increased local current density and local JH amplify the amplitude of stress fluctuation within the DUT. In addition, dislocation gliding within the solder reduces the internal stress from thermal stress fluctuation, but it also multiplies numbers of dislocations, rapidly increasing the dislocation density, thus inducing work-hardening. The work-hardened SAC limits dislocation gliding and decreases ductility but has higher yield strength, increasing the strength limit that causes fatigue failure. Since the yield strength does not continuously increase from work-hardening, thermal stress fluctuation eventually exceeds the yield strength, thus activating fatigue. At the critical void length where the thermal stress fluctuation amplitude exceeds the critical stress intensity factor, a catastrophic failure by crack occurs as seen in fatigue failures. Therefore, the combination of classical EM failure mechanism and the thermal stress fatigue is the EM failure acceleration mechanism that plays an important role in determining the EM failure kinetics at high DF.

5.4.4. Recrystallization, Superplasticity, and New Ratcheting Failure Mode

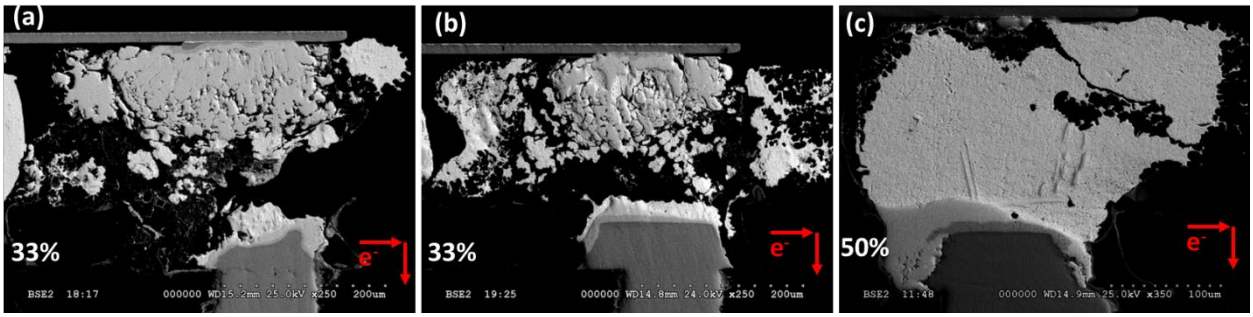


Figure 5-10. SEM images of failed samples with extreme solder deformations and extrusions.

In addition to a microstructural failure feature resembling mechanical fatigue failure features, the SEM failure analysis discovers unexpected macrostructural changes. As shown in Fig. 5-10, solder bumps show a huge extrusion out of the SAC solder bump. These extreme extrusions are mostly reported in thin film studies, not in SAC solder interconnects [98]–[101]. SAC solder interconnects do not show the extreme deformation because of Sn's BCT structure which has relatively rigid properties, limiting deformation and elongation. The limited slipping system in BCT limits dislocation gliding, thus limiting the level of plastic deformation. However, superplasticity is one mechanism that can cause a huge plastic deformation in a BCT structure. The superplasticity causes materials to deform beyond its normal strain limit. Recrystallization induces grain refinement to remove work-hardening of solder from thermal stress fluctuation during pulsed-DC EM test, leaving fine grains. Recrystallization often reduces strength and hardness but increases ductility. However, the dynamic recrystallization, which nucleates and grows new defect-free grains during recrystallization rather than afterwards, has relatively higher ductility compared to static recrystallization. The combination of dynamic recrystallization, plastic deformation, and thermal stress cycling causes superplasticity of SAC solder, resulting a huge extrusion. To confirm the superplasticity of the SAC solder ball which

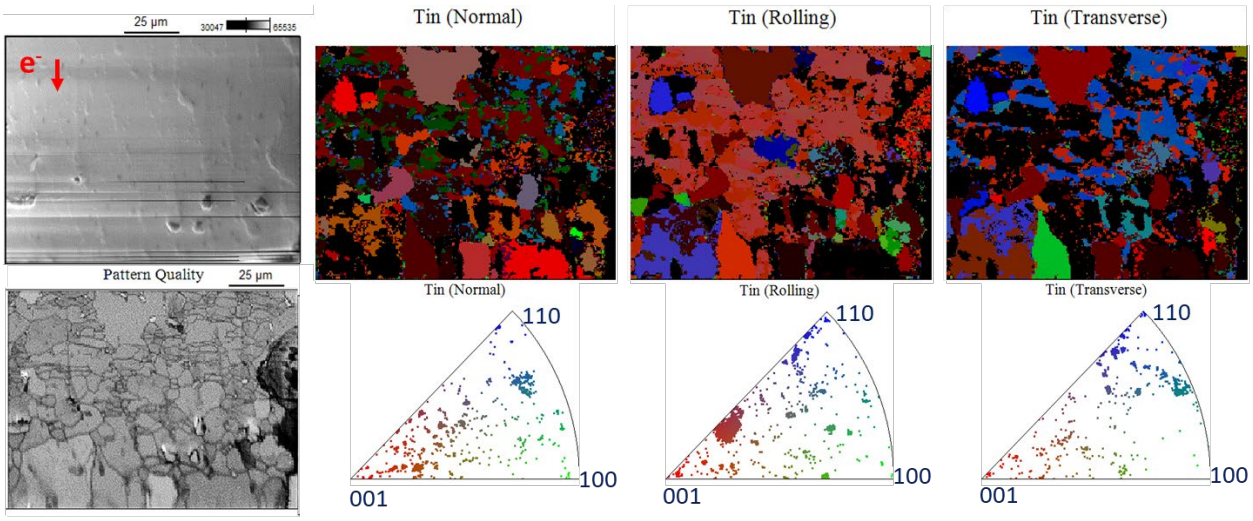


Figure 5-11. EBSD result of DUT with superplasticity, showing features of recrystallization.

can be characterized by fine grain sizes, EBSD analysis of cross-sectioned samples with extrusions is conducted.

The EBSD results shown in Fig. 5-11 has a fine grain size in the SAC solder, unlike typical SAC solder, which has a few large grains that are often referred to as a “beach ball” pattern. The fine grain boundaries clearly suggest that initial large grains of SAC solder recrystallize during the pulsed DC EM test and become finer grains, which are the common feature of recrystallization. EBSD analysis confirms the dynamic recrystallization of SAC solder and supports that the macrostructural failure feature, a SAC solder extrusion, is indeed caused by superplasticity. The superplasticity of SAC solder causes a new failure mode within solder interconnects, a creep ratcheting failure mode. Ratcheting is caused by an asymmetric thermal stress cycling and continuously deforms materials [102]–[106]. With the asymmetric thermal stress fluctuation from asymmetric current feed configuration and the location of DUT, SAC solder is prone to ratcheting phenomenon. With the combination of dynamic recrystallization of SAC and ratcheting

mechanism, SAC solder has superplastic deformation in one direction, posing a danger of short circuit failure that results in a catastrophic failure of a device.

5.4.5. EM Failure Acceleration and Deceleration Mechanisms

The evidence of recrystallization of the SAC solder gives further insight into the difference between the EM failure acceleration mechanism at high DF and EM failure deceleration mechanism under low DF pulsed-DC conditions. The dynamic recrystallization reduces the work-hardening effect from thermal stress. Since the samples under high DF pulsed-DC conditions have relatively shorter current off time or relaxation time, samples have a shorter period of low effective temperature that has reduced EM flux. Furthermore, the dislocations multiply faster than recrystallization removes them, which work-hardens the SAC and makes interconnects prone to fatigue. Therefore, the interconnects are eventually failed by fatigue cracking once the thermal stress fluctuation increases and reaches critical stress intensity factor by the classical EM failure mechanism. On the contrary, the samples under low DF pulsed-DC conditions have relatively a longer relaxation time and a lower effective temperature which reduces EM flux. The longer relaxation time maximizes the benefit of dynamic recrystallization that nucleates and grows defect-free grains, reducing work-hardening. In addition, recrystallization removes fast EM diffusing grain orientation, which is the alignment of the c-axis of Sn with the EM current direction. The combination of dynamic recrystallization, the removal of the fast EM diffusing grain orientation, and longer low-effective temperature explain the nonlinearly scaled EM failure deceleration that is observed in samples tested under low DF pulsed-DC conditions.

5.5. Conclusion

The effects of pulsed-DC on the EM failure mechanism and kinetics are studied with a comparative study with two different frequencies, 10,000Hz and 0.1Hz, and various DFs, 33%, 50%, 75%, and 100%. The DUT temperature change is measured and compared among various frequencies. The measurement shows that the DUT temperature is isothermal, like that in DC conditions, and the fluctuation is low when the frequency is higher than 10Hz. For frequencies lower than 10Hz, the DUT temperature fluctuation increases and plateaus at 14°C as the frequency decreases. This measurement shows the important role of temperature change within the DUT, affecting EM reliability of the solder interconnects because it induces thermal stress fluctuation at low frequency. The tested frequency, 0.1Hz, has DUT temperature fluctuation of 7°C, generating a thermal stress fluctuation. The high-frequency pulsed-DC EM test, which is tested under 10,000Hz at 50% DF, has an extremely slow failure rate, outlasting 10,000 hours. The combined 14°C lower effective DUT temperature, constant DUT temperature, and a halved current density of DC explain the extremely slow EM failure rate in low-frequency, low DF pulsed-DC conditions. The low-frequency pulsed-DC test data, SEM images, and EBSD analysis show two competing EM failure mechanisms, resulting the highly nonlinear relationship between the DF and the EM failure kinetics. The result contradicts the common assumption of a cumulative damage model in pulsed-DC conditions. The first contradiction is the EM failure acceleration mechanism in samples tested under low-frequency, high DF pulsed-DC conditions, resulting in accelerated EM failure kinetics compared to samples tested under DC conditions. The EM failure acceleration mechanism is the combination of the conventional EM failure mechanism that increases the amplitude of the thermal stress fluctuation and the thermal fatigue from

the temperature fluctuation. The second contradiction is the EM failure deceleration mechanism in samples tested under low-frequency, low DF pulsed-DC conditions. The EM failure deceleration mechanism is the combination of a relatively longer period with a low EM flux from the low effective temperature and recrystallization of the DUT. Another notable microstructural behavior is the extreme extrusion of SAC solder, introducing a new ratcheting failure mode. The dynamic recrystallization and the asymmetric thermal stress fluctuation cause a superplastic deformation of the SAC solder in one direction, posing a danger of a short circuit failure. Therefore, it is important to include stress as an important parameter to improve the EM reliability prediction, especially when developing design rules of a package for an application with low-frequency, high DF pulsed-DC use-conditions.

Chapter 6

EM Failure and Microstructural Evolution in SAC Solder Interconnects Under AC Load Condition

6.1. Motivation and Expectations

The previous chapter and the pulsed-DC EM papers titled “Study of Electromigration Failure in Solder Interconnects under Low Frequency Pulsed Direct Current Condition” confirm complicated effects of pulsed-DC on EM mechanism and kinetics [14]. Due to the complicated effects of thermal stress fluctuation, the discovered EM acceleration and deceleration mechanisms are not directly connected to the non-DC effect. Therefore, the actual non-DC effects on the EM mechanism have not yet been fully discovered. The constant current with a switching polarity of alternating current (AC) gives an isothermal condition for samples under AC load condition. The AC is the ideal non-DC load condition to study non-DC effects on the EM mechanism and kinetics because of its isothermal condition, like those in DC conditions. The isothermal condition of AC means that any discovered mechanism and effect are directly connected to non-DC effects. This gives a better understanding of non-DC EM mechanisms and failure features, such as the IMC formation and dissolution processes, void growth, and more. The understanding of non-DC effects on the EM mechanism and kinetics would guide a reliability assessment baseline for solder interconnects under AC signals by providing critical data. The following sections present AC effects on the EM kinetics, the EM failure mechanism, and the microstructure in the SAC solder joint.

6.2. Experimental Setup

A comparative study with various frequencies and DFs is conducted to capture the effects of non-DC load conditions on EM failure mechanisms without the complication of cyclic thermal stress caused by pulsed-DC load condition. Similar to pulsed-DC EM tests, WCSP samples are tested at 165°C with a current density of 9.63kA/cm^2. The AC EM test conditions are 10,000Hz with 50% and 75% DF and 0.1Hz with 50% and 75% DF. Controlling the AC EM test is done under DC. The DF is a ratio of forward polarity (classical EM damage) to backward polarity (damage recovery or reversal). For example, 75% DF of 0.1Hz means that there are 7.5 seconds of classical EM damage or forward flux and 2.5 seconds of damage recovery or reverse flux.

Similar difficulties in setting up pulsed-DC EM tests are faced while setting up the AC EM tests. Constant current AC power supplies with variable frequencies and DFs are not commercially available, and those which are available have limited capabilities and are extremely expensive. Therefore, a constant current AC generating module shown in Fig. 6-1 (a) is designed and produced to generate ideal square waveform AC with desired frequency and DF from DC. The AC generating module is connected between DC power supply and samples. The detailed schematics of the AC PCB module is shown in Fig. 6-1 (b). The circuit is based on an H-bridge that is often used for controlling a DC motor to go forward and backward. The circuit consists of four N-MOSFETs (STC3080ALGC11) which are divided into two groups, four heat sinks (WV-T247-101E) for each N-MOSFET, one MOSFET driver (IXDF604PI) with two opposite outputs, one Arduino Uno as a PWM, two DC power sources, two 40x20x20mm computer fans, resistors, capacitors, and

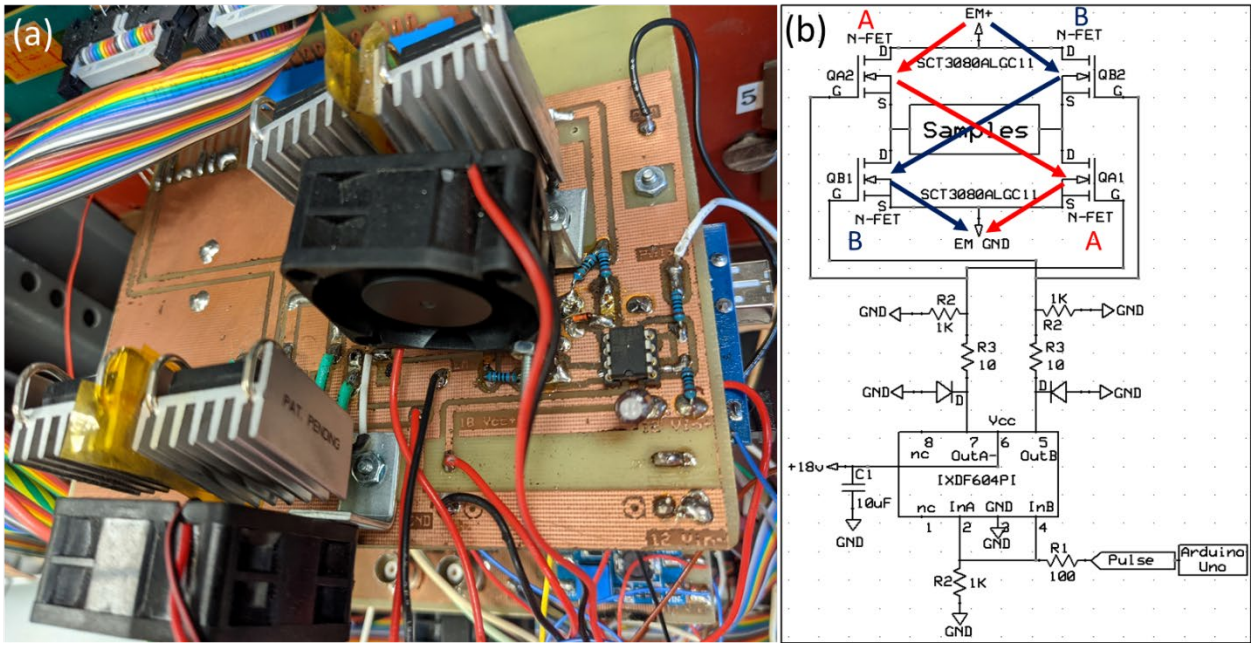


Figure 6-1. (a) shows the constant current alternating current (AC) generating PCB module. (b) shows the detailed circuit schematic of pulsed DC module. The 18V is supplied to MOSFET driver with two opposite polarity outputs. Function generator, Arduino Uno, acts as a pulse width modulation (PWM) and sends 5V or 0V to the MOSFET driver. According to PWM inputs, the MOSFET driver sends outputs (18V or 0V) to open or close a group of MOSFET. When a "A" group of MOSFET is closed, the accelerated EM test current flow with a forward polarity. When a "B" group of MOSFETs is closed, the accelerated EM test current flow with a backward polarity.

diodes. As shown in Fig. 6-1 (a), one computer fan is positioned behind the two MOSFET's heatsinks to cool down the MOSFETs. Instead of using a one step-up adjustable DC-DC converter (MT3608) per one pulsed DC generating module, a 150W DC-DC Boost Converter Module to power multiple AC generating PCB Modules was used. The 150W DC-DC converter has an input range of 10-32V and a maximum current of 16A and an output range of 12-35V and a maximum current of 10A. It is suitable to supply appropriate voltage, +18V, to the MOSFET drivers on multiple AC generating PCB modules and pulsed DC generating PCB modules at the same time. STC3080ALGC11 N-MOSFET is chosen because it has high drain-source voltage (600V), wide range of gate-source voltage (DC) (-4V to +26V) with a recommended drive voltage (V_{gs_op}) of 0V and +18V. The static drain-source on-state resistance is low (80mΩ at 25°C) when V_{gs_op}

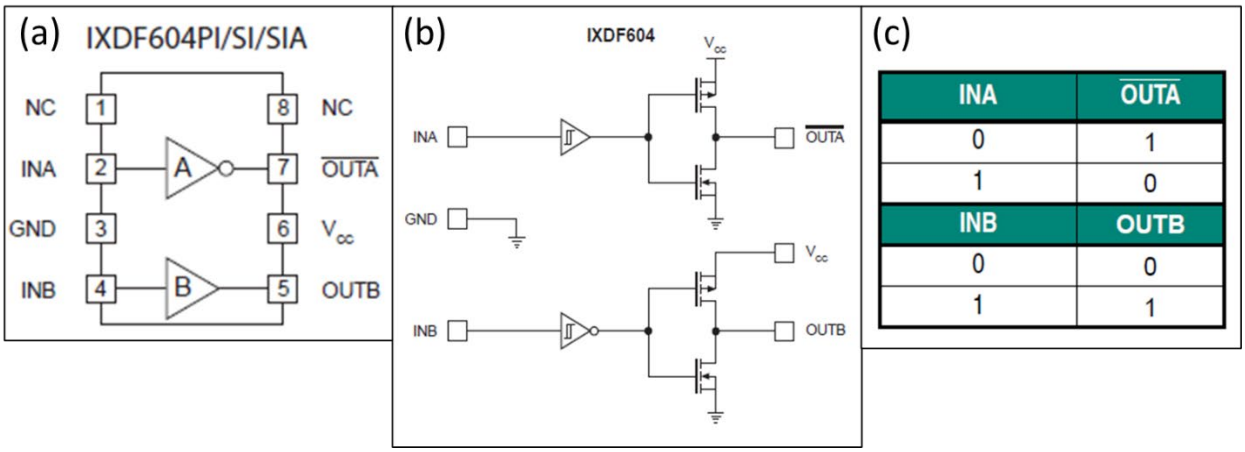


Figure 6-2. IXDF604PI MOSFET driver's (a) pin configuration, (b) block diagram, and (c) logic table.

is +18 V. The IXDF604PI MOSFET driver has very short rise time (9ns) and fall time (8ns), which are shorter than the IXDN614PI MOSFET driver used in the pulsed-DC generating module. As shown in Fig. 6-2, it also has two individual inputs to control two individual outputs with opposite polarities and a wide range of supply voltage (-0.3V to +40V) and output current (±4A).

12V DC is supplied to power the Arduino Uno, the computer fans, and 150W DC-DC converter. Arduino Uno is running a program that is written by me to act as a function generator, creating a pulsed square waveform of a desired frequency and DF with a magnitude of 0V and 5V. The generated 0V and 5V are supplied to MOSFET driver's

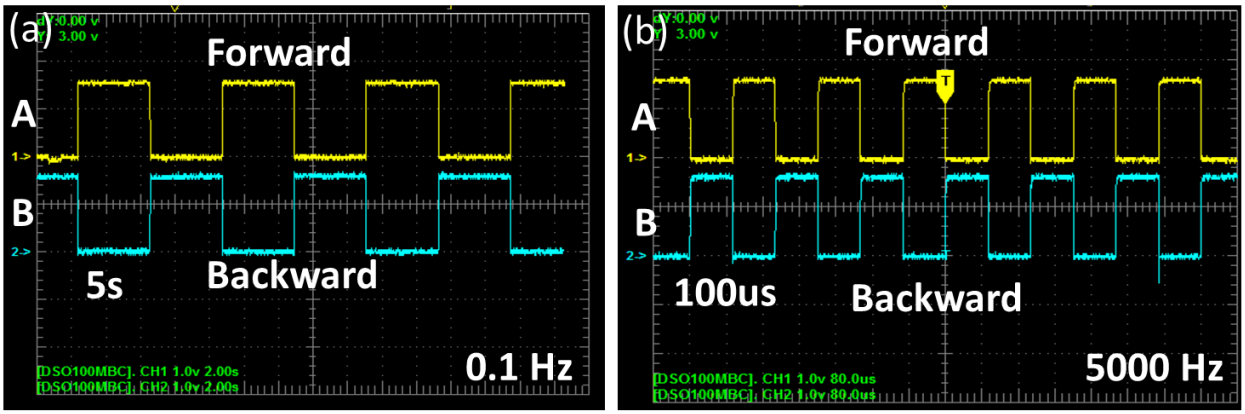


Figure 6-3. Oscilloscope images of the constant current AC at (a) 0.1Hz 50% DF and (b) 5000Hz 50% DF, showing a square waveform.

logic input pins, pin 2 and 4, to control outputs. Since the outputs, pin number 5 and 7, of MOSFET drivers have an opposite polarity, driver output supplied voltage of 18V through pin 5 while no voltage comes out of pin 7 when 5V is applied to pin number 2 and 4. When 0V is applied to pin 2 and 4, then 18V going out through pin 7 while pin 5 is off. The achieved square waveform AC is shown in Fig. 6-3. The Table 6-1 shows the accelerated EM test matrix for the comparative study of AC effect. Each test condition consists of 20 WCSP samples serially connected.

Table 6-1. Shows the accelerated EM test matrix for investigating AC effects.

Sample Structure		Test conditions			
UBM Cu, µm	UBM Ni, µm	Temperature, °C	Current Density, kA/cm2	Frequency, Hz	DF, %
18	0	165	9.63	0 (DC)	N/A
				0.1	50
				0.1	75
				10,000	50
				10,000	75

6.3. Results and Discussions

The material healing effect assumes that the samples tested under low-frequency AC conditions fail faster than those tested under high-frequency AC do. The comparative AC EM test results shown in Fig. 6-4 denies this assumption, in which the cumulative probability graph and the MTTF graph are plotted. The sample under DC load condition clearly fail the fastest. The most notable aspect of MTTF graph in Fig. 6-4 (b) is that samples tested under the 10kHz AC fail faster than those tested under the 0.1Hz AC condition for both 50% DF and 75% DF. The samples tested under the DC EM condition have a MTTF of 2700 hours, while samples tested under the 0.1Hz 50% DF AC EM condition have a MTTF of 10000 hours, which is 3.7 times longer than DC condition. The samples tested under the 10kHz 50% DF AC EM condition have a MTTF of 7650 hours,

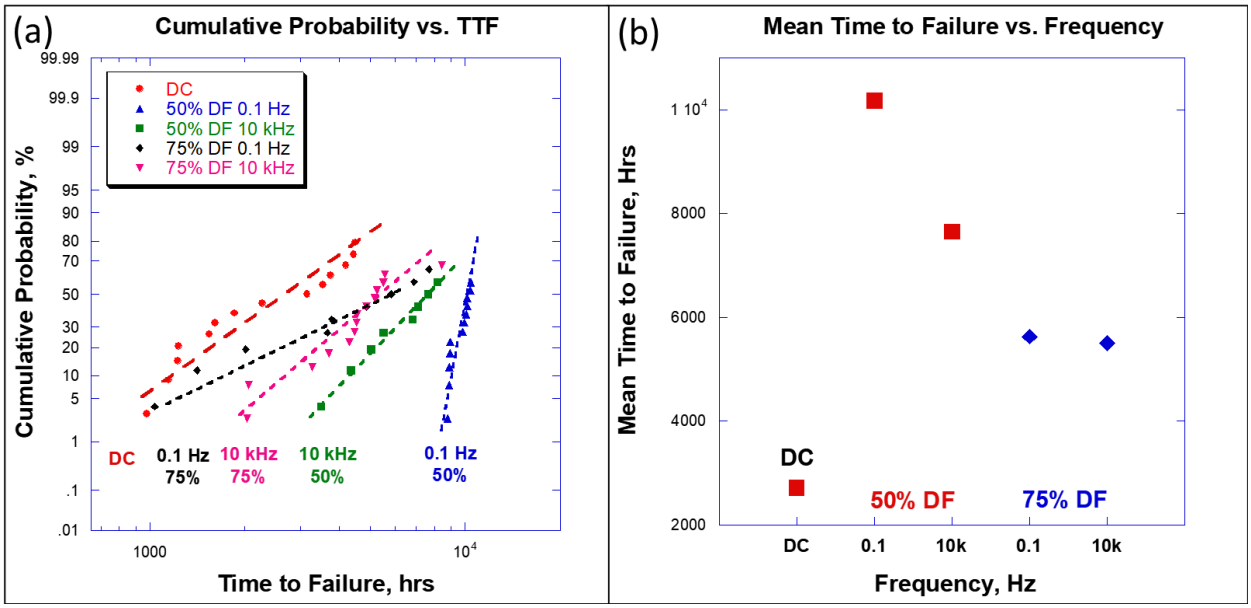


Figure 6-4. The graphs of AC EM test data. (a) The graph of the time to failure as a function of cumulative probability. (b) The graph of the mean time to failure.

which is 2.8 times longer than those tested under the DC condition. The MTTF of samples tested under 0.1Hz and 10kHz with 50% DF differ significantly, so experimental error can be ruled out. However, the MTTF of samples tested under 75% DF low- and high-frequency AC do not greatly differ, indicating that the high-frequency asymmetrical AC does not improve the EM reliability as much as high-frequency symmetrical AC conditions do, as expected. The 3 to 4 times increase in the EM lifespan indicates that the AC EM healing effect is not as effective as other articles have reported, where almost no EM damage is observed. The healing effect is not as effective because the IMC formation and dissolution process is not spontaneous as assumed. The nonspontaneous IMC formation and dissolution process accumulate EM damage, leading to a classical EM failure of an open circuit by voiding.

One notable feature in Fig. 6-4 (a) is the steep cumulative probability slope representing samples tested under 0.1Hz frequency and 50% DF AC conditions. The steep slope in the cumulative probability graph with TTF means that the failure time of

samples are distributed very tightly. This indicates that the EM failure kinetics for samples tested under 0.1Hz frequency and 50% DF AC conditions is not affected by the Sn grain orientation as other AC EM conditions are. The anisotropic properties of Sn's BCT crystal structure causes accelerated EM diffusion along the c-axis, causing a wide distribution of failure time. The recrystallization of the SAC solder removes the c-axis in 0.1Hz 50% DF AC as seen in Chapter 5 [14]. When the fundamental factor behind the 0.1Hz 50% DF AC's narrow failure time distribution is understood, then those can be incorporated into SAC solder interconnect assembly design rules to prevent early EM failures in addition to Cu substrate effects. The prevention of early EM failures improves the EM reliability [32].

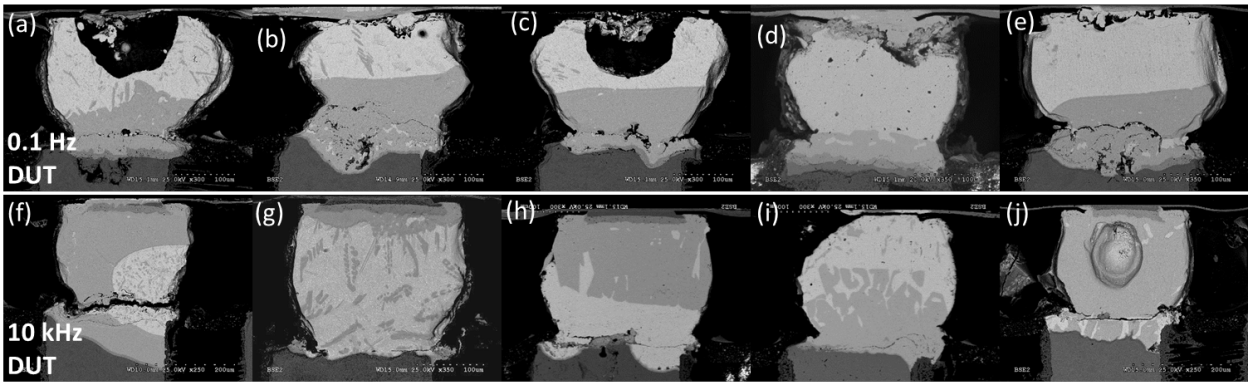


Figure 6-5. Cross-sectional SEM pictures of (a)-(e) 0.1Hz 50% DF AC and (f)-(j) 10kHz 50% DF AC.

Under cross-sectional failure analysis using an SEM, observations of recrystallization, a precipitation effect, IMC instability, anisotropic IMC growth, and nonspontaneous IMC formation and dissolution process are seen. Fig. 6-5 shows SEM cross-sectional pictures of failed samples under both 0.1Hz and 10kHz AC load conditions. The major difference between these failures and the failure features of the classical EM failure mechanism is that the location of EM damage is randomized in samples tested under AC conditions. Some of samples failed at the Cu UBM and SAC interface, and others failed at the Cu via and SAC interface. The randomness indicates

that the high EM flux divergence area at the interface between the Cu UBM and the SAC interface is not the major factor determining the EM void nucleation location. In Fig. 6-5 (a), (b), (f), (g), and (i), the IMC forms in the middle of the SAC solder interconnect. The IMC formation location indicates that the IMC formation and dissolution are not a spontaneous process, as has been widely assumed. If the IMC formation and dissolution are a spontaneous process, then the EM damage should be fully recovered, which is not observed in samples tested under AC conditions. The IMC will not be formed by the EM process, but only by thermomigration and a chemical concentration gradient. The thermomigration and chemical concentration gradient form an IMC at the interface between the Cu and SAC.

The needle-shaped IMCs are observed mostly in samples tested under 10kHz AC conditions. Fig. 6-6 shows SEM pictures of samples tested under both 10kHz and 0.1Hz AC conditions. The Cu_6Sn_5 IMC forms as a needle shape IMC with Cu_3Sn IMC core. The

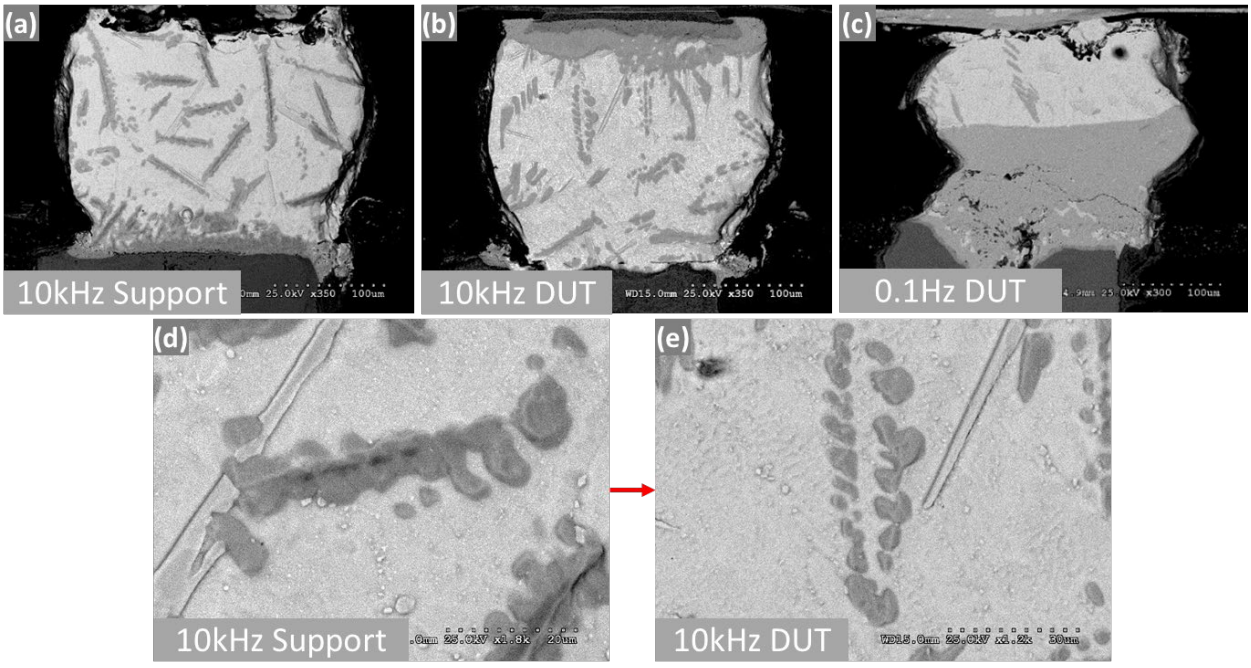


Figure 6-6. SEM images of (a) 10kHz supporting bump, (b) 10kHz DUT, and (c) 0.1Hz DUT. IMC microstructure SEM images of (d) 10kHz supporting bump and (e) 10kHz DUT.

IMC has round edges all along the interface of IMC. The round edges indicate an instability at IMC interface. Since supporting bump has half amount of current density of DUT, IMC observed in supporting bump evolves into IMC observed in DUT. Comparing Fig. 6-6 (d) and (e), IMC evolution is concluded that the needle shaped Cu_6Sn_5 IMC with Cu_3Sn IMC core breaks into small clusters of Cu_6Sn_5 IMC without Cu_3Sn IMC core. The breakdown of IMC supports the IMC instability. The larger numbers of needle shaped IMCs in 10kHz AC indicate that 0.1Hz AC has more stable IMC formation than 10kHz AC.

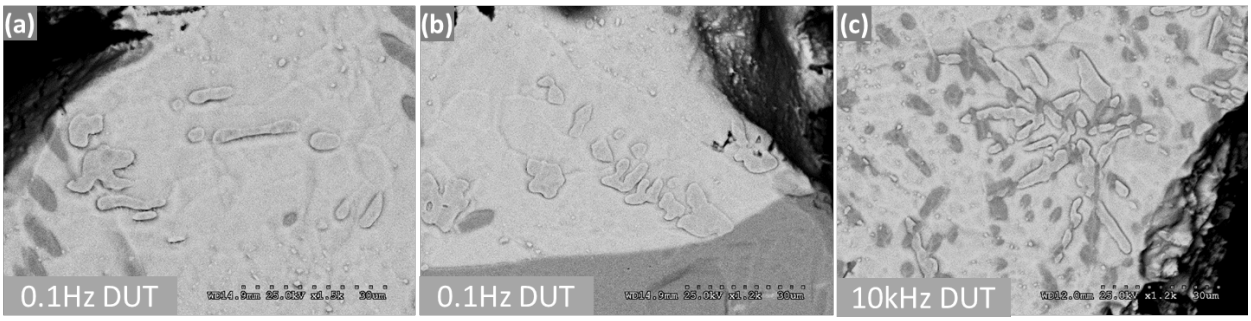


Figure 6-7. SEM images of Ag_3Sn IMC dendrites in (a) and (b) 0.1Hz AC DUT and (c) 10kHz AC DUT.

The dendritic growth of IMCs is observed in Fig. 6-5 (b), (f), and (g). Zoomed-in SEM images of the Ag_3Sn IMC dendrites are shown in Fig. 6-7. The size of Ag_3Sn IMC dendrites is larger in 10kHz samples than those in 0.1Hz samples. The dendritic IMC indicates an anisotropic growth which is caused by bi-directional nonconstant EM flux divergence. Since dendritic growth of IMCs indicate an instability, this evidence further supports that the 0.1Hz frequency AC condition has better IMC stability than the 10kHz frequency AC condition does.

The Ag_3Sn IMCs form a platelet structure in the SAC solder [2], [75], [78], [107]–[112]. However, SAC solder bumps under AC load conditions form a lot of fine circular Ag_3Sn IMC in Fig. 6-8. These circular IMC formations are positioned in grain boundaries and hinder Cu's grain boundary diffusion. Therefore, the fine Ag_3Sn IMCs slow down the

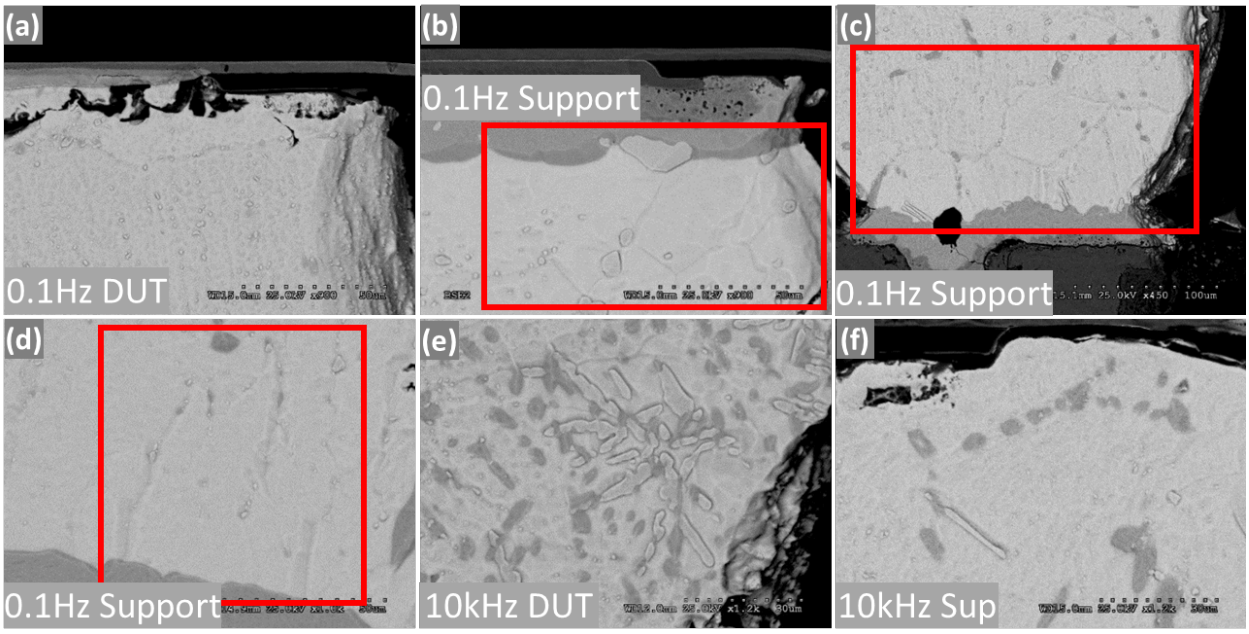


Figure 6-8. Cross-sectional SEM images of (a) 0.1Hz AC DUT, (b), (c), and (d) 0.1Hz AC supporting bump, (e) 10kHz AC DUT, and (f) 10kHz AC supporting bump. Small circles are Ag_3Sn IMC. Rectangles marks fine Sn grains.

EM failure kinetics. The amount of fine circular Ag_3Sn IMC in samples tested under 0.1Hz AC conditions exceeds the amount in samples tested under 10kHz AC conditions, indicating a higher degree of precipitation effects under 0.1Hz AC conditions. The small SAC grain sizes in samples tested under 0.1Hz AC conditions, presented in Fig. 6-8 (b), (c), and (d), indicate that SAC undergoes recrystallization and removes fast EM diffusion Sn grain orientation of c-axis. This partially explains why samples tested under 0.1Hz AC conditions are not affected by the Sn grain orientation effect. The fine Ag_3Sn IMCs are positioned in recrystallized SAC grain boundaries, supporting a higher degree of precipitation effects of 0.1Hz AC. Recrystallization and IMC's precipitation effect explain why samples tested under 0.1Hz AC conditions fail slower than those tested under 10kHz AC conditions do.

EM under AC conditions is still caused by the classical EM failure mechanism of void nucleation and propagation. The SAC solder interconnect under AC has two EM flux

divergence points. One is at the Cu UBM and SAC solder interface, and another is at the Cu via and SAC solder interface. The constant current AC's polarity change gives a bi-directional nonconstant EM flux divergence at the divergence interfaces. Therefore, the classical EM failure mechanism can happen at either of the Cu and SAC interfaces on either end of the solder joint, meaning that the IMC formation location is random. The IMC formation in the middle of the SAC solder indicates that the IMC formation and dissolution process is not spontaneous as assumed before. The recrystallized SAC under a 0.1Hz AC condition removes Sn's fast EM c-axis grain orientation, thus the failure kinetics are not affected by the Sn grain orientation effects. The fine circular Ag_3Sn IMCs at the grain boundaries give precipitation effects and hinder Cu grain boundary diffusion. The recrystallization and larger numbers of fine Ag_3Sn IMCs yield slower EM failure kinetics under 0.1Hz AC compared to 10kHz AC. The combination of recrystallization, IMC instability, and the precipitation effect plays an important role in determining the EM failure kinetics under AC load conditions.

6.4. Conclusion

AC EM tests are conducted to understand the non-DC effects on the EM mechanism, kinetics, and microstructures without the complicated effects of thermal stress fluctuation caused by pulsed-DC conditions. The comparative accelerated AC EM tests show that the commonly assumed material healing model is incorrect. Samples tested under low-frequency AC conditions fail faster than those tested under high-frequency AC conditions. The failed microstructural features indicate an IMC instability, anisotropic growth of IMCs, and a nonspontaneous process of IMC formation and dissolution. The IMC formation at the middle of the SAC solder interconnect indicates a

nonspontaneous IMC formation and dissolution process because the IMC formation requires incubation time, while IMC dissolution is almost instant. The bi-directional nonconstant EM flux divergence of AC causes the classical EM failure mechanism to happen at either the interface between the Cu UBM and the SAC solder joint or the interface between the Cu via and the SAC solder joint. The bi-directional nonconstant EM flux divergence resulted by AC causes IMC instability and forms needle-shaped IMCs that break into small clusters of IMCs. The observed dendritic IMCs is further evidence of IMC instability with anisotropic IMC growth. The larger Ag_3Sn IMC dendrite arm spacing in 0.1Hz further supports that the 0.1Hz AC condition yields less IMC instability than 10kHz AC condition does. The Ag_3Sn IMC forms fine circles instead of normal platelet IMCs under AC conditions. These IMCs are located between SAC grain boundaries and give precipitation effect by hindering Cu's grain boundary diffusion. The finer grains in samples tested under 0.1Hz AC conditions indicate a recrystallization that removes fast EM diffusion Sn grain orientation and gives a narrow failure distribution. The very tight distribution of failure time of samples tested under 0.1Hz 50%DF AC conditions can be partially explained by precipitation effects and recrystallization.

Chapter 7
Overall Conclusion and Future Work

7.1. Overall Conclusion and Implication

Comprehensive studies comparing various package parameters and testing conditions have proven that package parameters and use-conditions have complicated effects on EM failure mechanisms and kinetics of solder interconnects. The UBM thickness study shows that there are at least two competing mechanisms affecting EM failure kinetics. When the UBM thickness is below the critical thickness, the UBM's intended role as a Cu supplier controls the EM failure kinetics. The UBM supplies Cu to reduce flux divergence as the Cu diffuses away. Once the UBM thickness increases to the critical thickness, the first well-known EM failure mechanism of the UBM no longer controls the EM failure kinetics, and the secondary failure mechanism starts determines the EM failure kinetics. The secondary EM failure mechanism is the compressive stress which is known to prolong void nucleation. The different amounts of current densities on solder interconnects within the package develops compressive stress on the DUT, which has the highest amount of current density, and tensile stress on the surrounding interconnects. The different CTEs of Cu and Sn cause different levels of stress development on different UBM thicknesses. Since Sn has a higher CTE than Cu, thinner UBM interconnects, which have a higher ratio of Sn to Cu than thicker UBM interconnects, have a higher amount of compressive stress than thicker UBM interconnects. The package with thinner UBMs than the critical UBM thickness would have a faster void

nucleation than that of the package with a UBM that is thicker than the critical UBM thickness. However, once the void nucleates, the package with the UBM which is thicker than the critical UBM thickness has a faster void propagation than that of the package with a thinner than the critical UBM thickness because of slower compressive stress development. These complicated effects of the UBM thickness show that the EM reliability of a package can be increased by considering an optimal UBM thickness that maximizes the benefits of both the abundant Cu supply of the thick UBM and the high compressive stress of the thin UBM.

Early EM failures have been observed within a test group despite tested samples having different packaging parameters. Sn's BCT crystal structure gives anisotropic properties. Sn has the fastest EM diffusion along its c-axis grain orientation, which is in the [001] direction, due to its anisotropic properties. The EBSD analysis of early and late failures within a same test group confirms that the c-axis alignment is causing the early EM failures. In an effort to identify a method to mitigate early EM failure, the substrate effect is studied. Different sizes of SAC solder balls, ranging from 200μm to 760μm, are reflowed on different Cu substrates. The prepared Cu substrates are polycrystalline from PCB and textured single crystal. The single crystal Cu substrates have three different textures, (111), (110), and (100). The EBSD analysis of reflowed SAC solder balls show that there is substrate effect, causing Sn grain orientation preference. (111) has the tightest distribution of Sn grain orientation with two preferred Sn grain orientations near [110] and [100]. While (110) has the second-best Sn grain orientation distribution, one of its preferred Sn grain orientations is [001], a c-axis. (100) textured Cu substrate does not have c-axis grain orientation preference, but the Sn's preferred grain orientation spreads

between [111] and [110] orientations. Therefore, (111) textured single crystal Cu substrate is the best candidate to implement into SAC solder interconnect to prevent early EM failures by the c-axis alignment of Sn grain orientations.

Non-DC effects on EM failure mechanism, kinetics, and failure features are first studied by using pulsed-DC load condition. The pulsed-DC EM study also shows the importance of the DUT temperature change that causes a thermal stress fluctuation, having a complicated effect on the EM failure mechanisms and kinetics. The measured DUT temperature fluctuation increases to as high as 14°C in low-frequency pulsed-DC conditions, inducing the thermal stress fluctuation. The DUT temperature under high-frequency pulsed-DC conditions is isothermal, not inducing a thermal stress fluctuation. Therefore, the high-frequency pulsed DC EM test shows extremely slow failure kinetics from the low effective temperature and the halved current density of DC, showing no failure after 10,000 hours. The low-frequency pulsed-DC EM test data suggests two competing EM failure mechanisms in determining the EM failure kinetics: one is an acceleration mechanism at high DF, and another is a deceleration mechanism at low DF. The EM failure acceleration at high DF is caused by the combination of classical EM failure mechanism, which is void nucleation and propagation, and the thermal stress fluctuation induced fatigue. As the SAC solder is exposed to thermal fluctuation, dislocation gliding happens to reduce internal stress while increasing the dislocation density, causing work-hardening. The increased strength and hardness from work-hardening cause solder interconnects to be stiffer, thus they become more vulnerable to a fatigue-cracking failure mechanism. Therefore, when EM damage within a solder interconnect progresses through void nucleation and void propagation to a certain extent,

the amplitude of the thermal stress fluctuation exceeds the solder material's yield strength, activating fatigue. When the EM void propagation continues to the critical length, then failure by fatigue cracking occurs. Under low DF, low-frequency conditions, the EM failure deceleration mechanism is the combination of recrystallization of SAC solder that removes the fast EM diffusing grain orientation, low effective temperature, and relatively longer relaxation period with a reduced EM flux. The longer relaxation period maximizes the EM failure deceleration mechanism of recrystallization. The recrystallization reduces dislocation density, alleviating work-hardening, and removes fast EM diffusing grain orientation, c-axis or [001] grain orientation, which aligns with the EM flux direction. Another notable phenomenon observed during SEM failure analysis of samples failed under pulsed-DC EM testing conditions is the extreme extrusion of SAC solder, suggesting a new ratcheting failure mode. The EBSD analysis of highly deformed DUT supports the superplasticity of SAC solder by dynamic recrystallization and asymmetric thermal stress cycling, causing ratcheting. This level of extrusion poses the danger of a short circuit failure.

AC EM tests are conducted to understand the non-DC effects on the EM failure mechanism, kinetics, and microstructures without the complicated effects of thermal stress fluctuation caused by pulsed-DC conditions. The AC EM reliability model is based on a damage or material recovery model. Therefore, samples tested under higher frequency conditions are presumed to fail slower than those tested under lower frequency conditions because lower frequency AC has a longer period of one EM direction to cause more permanent EM damage. However, the comparative accelerated AC EM tests show that the material healing model is incorrect. The AC EM test shows that the

recrystallization and precipitation effects determine the EM failure kinetics. The samples under higher frequency (10kHz) AC fail faster than the samples under lower frequency (0.1Hz) AC do. The failed microstructures from cross-sectional failure analysis indicate an IMC instability, anisotropic growth of IMCs, and a nonspontaneous process of IMC formation and dissolution. The IMC formation in the middle of the DUT SAC solder interconnect indicates that the IMC formation and dissolution process is not spontaneous. IMC formation needs some incubation time, while IMC dissolution is instant. If the IMC formation and dissolution are spontaneous processes, then the IMCs would not form in the middle of the SAC solder joint because the SAC solder interconnects would only be damaged by thermomigration and chemical concentration gradient. The random IMC formation area between the Cu UBM/SAC interface and the Cu via/SAC interface supports that the bi-directional nonconstant EM flux divergence is a key factor in the AC EM failure mechanism. The needle-shaped with round edges of Cu_6Sn_5 IMCs with Cu_3Sn core are observed in the supporting bumps, and smaller clusters of Cu_6Sn_5 IMCs without Cu_3Sn are observed in the DUT. Since the supporting bump has half the amount of the DUT's current density, this is a sign of an IMC instability under AC EM, forming a needle-shaped IMC first, which then evolves into smaller circles of IMCs. The observed dendrite IMCs are further evidence of IMC instability with anisotropic IMC growth. The dendritic growth of Ag_3Sn IMC is observed in samples tested under both 0.1Hz and 10kHz AC conditions. However, the microstructures of samples tested under 0.1Hz AC conditions have a smaller number of dendritic IMCs and shorter dendrite arm spacing than those under 10kHz AC conditions. This supports the conclusion that samples tested under 0.1Hz AC conditions have less IMC instability than those under 10kHz AC conditions.

Furthermore, the Ag_3Sn forms fine circular IMCs instead of normal platelet IMCs. They are positioned between the grain boundaries and give a precipitation effect, hindering Cu's grain boundary diffusion. The finer grains of the microstructures in samples tested under 0.1Hz AC conditions indicates an involvement of recrystallization, which removes the fast EM diffusion Sn grain orientation. The finer grains and fine Ag_3Sn IMC at the grain boundaries hinder the Cu diffusion through the grain boundary, slowing the EM failure kinetics, in samples tested under 0.1Hz AC load conditions. The very tight distribution of failure time for samples tested under 0.1Hz AC conditions can be partially explained by precipitation effects and recrystallization.

For the different UBM thickness study, the compressive stress and the different UBM thicknesses give two competing mechanisms in determining EM failure kinetics. Finding critical UBM thickness is important to maximize the benefit of higher Cu supply effect and compression effect for improving EM reliability. The thermal stress fluctuation and the recrystallization observed during the pulsed DC EM test also give EM failure acceleration and deceleration mechanisms, complicating the EM reliability prediction. Therefore, it is crucial to include stress as an influential parameter affecting EM failure mechanisms and kinetics to improve EM reliability prediction. Furthermore, the faster failure kinetics of pulsed DC at 0.1Hz 75% DF shows that the EM reliability prediction based on the DC load condition may be incorrect for a certain application. It is important to consider that the DC is not the worst EM test condition when developing design rules for a package for an application with low frequency pulsed DC at high DF. The early EM failures can be prevented by utilizing a substrate effect. The (111) textured single crystal Cu substrate gives a tightly distributed and highly preferred Sn grain orientation when

SAC solder is reflowed. The AC EM test reveals that the commonly assumed material healing mechanism is not a major factor determining the EM failure kinetics under AC load conditions. The recrystallization and precipitation effects determine the EM failure kinetics for AC EM; rather, the AC EM's bi-directional nonconstant EM flux divergence causes IMC instability. The IMC instability is observed by the IMC evolution of a needle-shaped Cu_6Sn_5 IMC with a Cu_3Sn core into small clusters of Cu_6Sn_5 IMCs. The nonspontaneous IMC formation and dissolution process causes the IMC to form at the middle of SAC solder interconnects. It is important to conduct simulation studies to gain more insight on the AC EM mechanisms.

7.2. Future Work

The UBM thickness effect, pulsed DC current load effect, and AC current load effect yield very interesting results and new EM failure mechanisms and kinetics so far. However, the exact effects of other various package parameters on EM reliability are still

Figure 7-1. Schematics of DUT of second set of WCSP samples, showing different solder shapes.

unknown and can only be speculated. Therefore, more WCSP samples are designed with different package parameters to study their effects on EM failure mechanisms, kinetics, and failure microstructures. A second set of WCSPs would have different polyimide (PI) opening sizes, Ni barrier layers, UBM thicknesses with Ni barrier layer, no UBM, smaller solder ball height, rectangular UBM and solder shape, and more as some are shown in Fig. 7-1. Some groups of the second set of WCSP are set as control groups, having redundant package parameters consistent with the first set of WCSP samples. The control groups establish a base line and confirm the compatibility between the first and second set of samples, so that first and second set of test results can be compared.

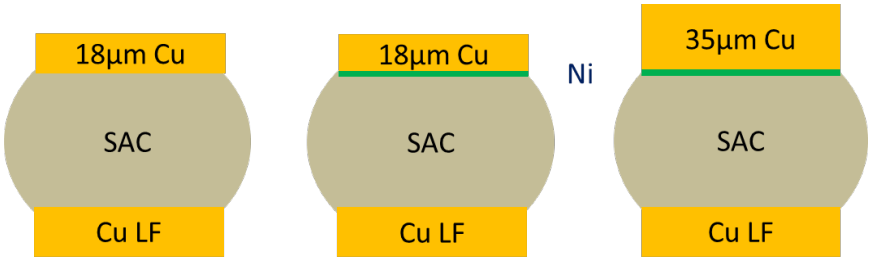


Figure 7-2. Schematics of WCSP samples with Ni barrier layer

After the surprising findings from the UBM thickness effect study, the effects of Ni barrier layer will be investigated to identify any overlooked effects on the EM failure kinetics and mechanisms. Samples with an additional Ni barrier layer toward the SAC solder on top of the Cu UBM are tested with different Cu UBM thicknesses as shown in Fig. 7-2. The samples have three different Ni barrier layer thicknesses, 0.2µm, 0.5µm,

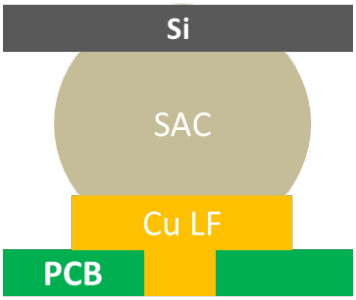


Figure 7-3. Schematics of solder interconnect without any UBM

and 3μm. The Cu UBM thicknesses range from 18μm to 35μm. Furthermore, the samples without any UBM, shown in Fig. 7-3, are going to be tested to compare the effects of the UBM thickness. Since the samples without the incorporation of a Cu UBM do not have any Cu supply and reservoir, they would fail a lot faster than any other samples with UBMs.

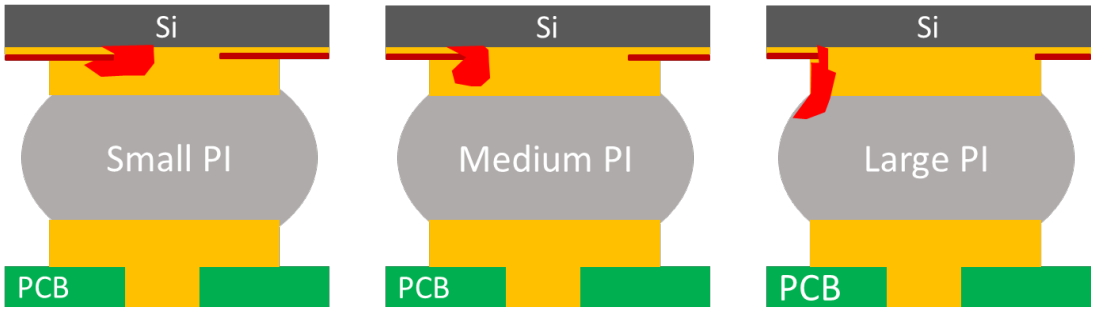


Figure 7-4. Schematics of WCSP samples with small, medium, and large polyimide opening sizes, showing three different current crowding regions and local JH areas.

The samples with different sizes of polyimide (PI) opening are going to be tested to find the effects of the PI opening parameter on EM reliability. The Fig. 7-4 also illustrates regions where current crowding occurs for each PI opening size and the corresponding local high JH regions. The smallest PI opening size samples would cause the current crowding and JH region be closer to the Si wafer, while the largest PI opening size samples would cause the current crowding and JH region to be closer to the Cu UBM and SAC solder interface. Since the interface of the Cu UBM and SAC solder is a weak-point where EM flux divergence is the highest, the largest PI opening sample would fail the fastest among the three different PI opening size samples.

Another WCSP sample group is called power WCSP (PWCSP), which is designed for a power-specific application. PWCSP has a 75μm solder bump height, which lies in between the heights of BGA and microbumps. PWCSP samples are designed to investigate the effects of SAC solder interconnect shape and height. PWCSP samples have a rectangular shape solder interconnects with two different ratios, 2:1 and 3:1 ratio

marked as DUT 3 and DUT 4 from Fig. 7-1. The combination of shorter solder bumps and rectangular shapes would generate a greater degree of compressive stress which would influence EM failure mechanisms and kinetics more than that of WCSP samples does because they have a smaller surface area to relieve the internal stress by dislocation gliding. The PWCSP will be tested in an oil-medium cooling system because the samples require higher current to flow, generating higher JH.

Lastly, a study of the effects of a high-frequency (10kHz) 50% DF pulsed DC EM testing condition test is planned. It will be ran with a compensation for the 14°C lower effective DUT temperature to ensure its failures. Table 7-1 shows the second set of WCSP sample configuration. Table 7-2 shows the WCSP samples configurations for different PI opening sizes. Table 7-3 shows the PWCSP sample configurations.

Table 7-1. Shows the second set of WCSP sample configuration.

Sample Structure	
UBM Cu, µm	UBM Ni, µm
18	0
18	0.2
35	0.5
18	0.5
0	0
18	0

Table 7-2. Shows the WCSP samples configurations for different polyimide (PI) opening sizes.

Sample Structure		
UBM Cu, µm	UBM Ni, µm	PI Size (Polyimide)
18	0.2	L
		M
		S

Table 7-3. shows the PWCSP sample configurations.

Sample Structure		
UBM Cu, µm	UBM Ni, µm	Solder Ratio
50	3	2:1
35	3	2:1
50	3	3:1
50	0.2	2:1

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Biographical Information

Yi Ram Kim received his Bachelor of Science (B.S.) in Chemistry from the College of William & Mary in May 2015. He joined the University of Texas at Arlington and pursued his Doctor of Philosophy (Ph.D.) through B.S. to Ph.D. program in Materials Science and Engineering in August 2016. He researched on the microelectronic package reliability areas focused on electromigration (EM). He developed more in-depth knowledge on EM, effects of different current loads, stress, under bump metallization (UBM) thickness, SAC alloy solder intermetallic compound (IMC) development over time, circuits, and overall electronic packages through literature, discussions with his advisor and colleagues, and different hands-on tasks. He combined the knowledge with various hands-on tasks, including expanding EM testing capacity, design/process printed circuit board (PCB) modules, data analysis, and post-mortem failure analysis of the samples. Through research, he found and proposed multiple novel EM failure mechanisms, failure features, and failure kinetics.

Appendix A

Arduino Uno Program Code

Due to its small form factor and versatility, Arduino Uno is used as a pulse width modulation (PWM) device to generate desired frequency and duty factor (DF). There are two ways that I programmed to generate desired frequency and DF. First is based on digitalWrite, analogRead, TriggerRead, delay, and delayMicroseconds commands. The example of the first generated Arduino Uno code is shown in Fig. A-1. This code is written to generate 0.1Hz 50% DF with a square waveform for pulsed-DC and AC EM tests. The loop function part, code-line 31-58, is where it reads input from data acquisition unit and generate appropriate PWM signals. The code set Pin 12 as PWM output and Pin A1 as input from HP data acquisition unit. As shown in code-line 16 to 25, every desired frequency's periods are in the code, so a few words can simple be swapped or substituted in delay commands in code-lines 48 and 55 to create different frequencies and DFs. As can be seen in code-lines 31- 58, the loop function part of the program needs an input read function during the "Off" condition of pulsed-DC, or reverse direction of AC, in order to read a consistent value. The code is relatively long and has an extra delay in code-lines 44-50. The delay is caused by a code-line reading input from HP data acquisition unit during "off" condition of pulsed DC or reverse polarity of AC. So, it can set the Arduino signal to be "on" condition of pulsed DC or forward polarity of AC as soon as HP data acquisition unit starts to read data from test samples. This gives a constant polarity of data reading, not giving an in accurate values. As a result, the code needed to adjust its delay time to account for input read delays. Therefore, a few trials and errors with oscilloscope are needed to achieve an accurate frequency and DF.

At first, only 5V and ground pins from the HP data acquisition relay board are connected directly into the Arduino. When more than one pulsed-DC or AC EM test slots

are installed, the Arduino starts to distort frequency and sometimes completely stops generating pulses. The investigation shows that the isolation between slots created ground looping, causing an irregular operation of the PWM. The ground looping is resolved by adding a relay between the HP data acquisition unit's relay board and

```
// This section defines the pins on the Arduino. S
// pecify the intigers (int) TTL1.
int TTL1 = 12;
int Trigger = A1;
int TriggerRead = 0;

//This tells the Arduino to treat the pins as output.
void setup() {
  analogReference(DEFAULT);
  pinMode(TTL1, OUTPUT);
  pinMode(Trigger, INPUT);
}

// Define the number of conditions.
// Define the length of time (in ms or us) for each condition.
int con1 = 5000; // 1/2 of 10 seconds for 0.1 Hz
int con2 = 1000;   // 1/2 of 2 seconds for .5 Hz
int con3 = 500;  // 1/2 of 1 second for 1 Hz
int con4 = 50;   // 1/2 of .1 seconds for 10 Hz
int con5 = 5;    // 1/2 of .01 seconds for 100 Hz
int con6 = 1;    //  1/2 of .002 seconds for 500 Hz
int con7 = 500;  // 1/2 of .001 seconds for 1,000 Hz [USE delayMicroseconds()] (1000 Microseconds)
int con8 = 100;    // 1/2 of 200 microseconds for 5,000 Hz (200 Microseconds)
int con9 = 50;  // 1/2 of .0001 seconds for 10,000 Hz  (100 Microseconds)
int con10 = 10;  //  1/2 of .00005 seconds for 50,000 Hz (20 Microseconds)

int i;

// Arduino loops generating desired frequency and duty factor
// Set pin as High/ON or Low/Off for each condition, and the waits for the duration of condition.
void loop() {
  TriggerRead = analogRead(Trigger);
  if (TriggerRead < 130) // input <1V
  {
    digitalWrite(TTL1, LOW); // Forward direction [AC] | Off Condition [Pulsed DC] = MOSFET Off (I through Samples)
    TriggerRead = analogRead(Trigger);
  }

  if (TriggerRead > 512) // input >2.5V
  {
    //Condition 1
    digitalWrite(TTL1, HIGH); // Reverse direction [AC] | On Condition [Pulsed DC] = MOSFET On (I bypass Samples)
    for (i = 0; i < con1; i++) // Repeat with i increment with 1 till delay reach
    {
      TriggerRead = analogRead(Trigger);
      if (TriggerRead < 103) // check Relay state and exit loop if it is on, enabling one directional current during data reading
        break;
      //delay(con1);
      delayMicroseconds(991); //for >1,000 Hz
    }

    //Condition 2
    TriggerRead = analogRead(Trigger);
    digitalWrite(TTL1, LOW); // Forward direction
    delay(con1);
    //delayMicroseconds(con7); //for >1,000 Hz
  }
}
```

Figure A-1. Arduino code for 0.1Hz constant current square waveform pulsed DC and AC generation code without a relay connection to a HP data acquisition unit.

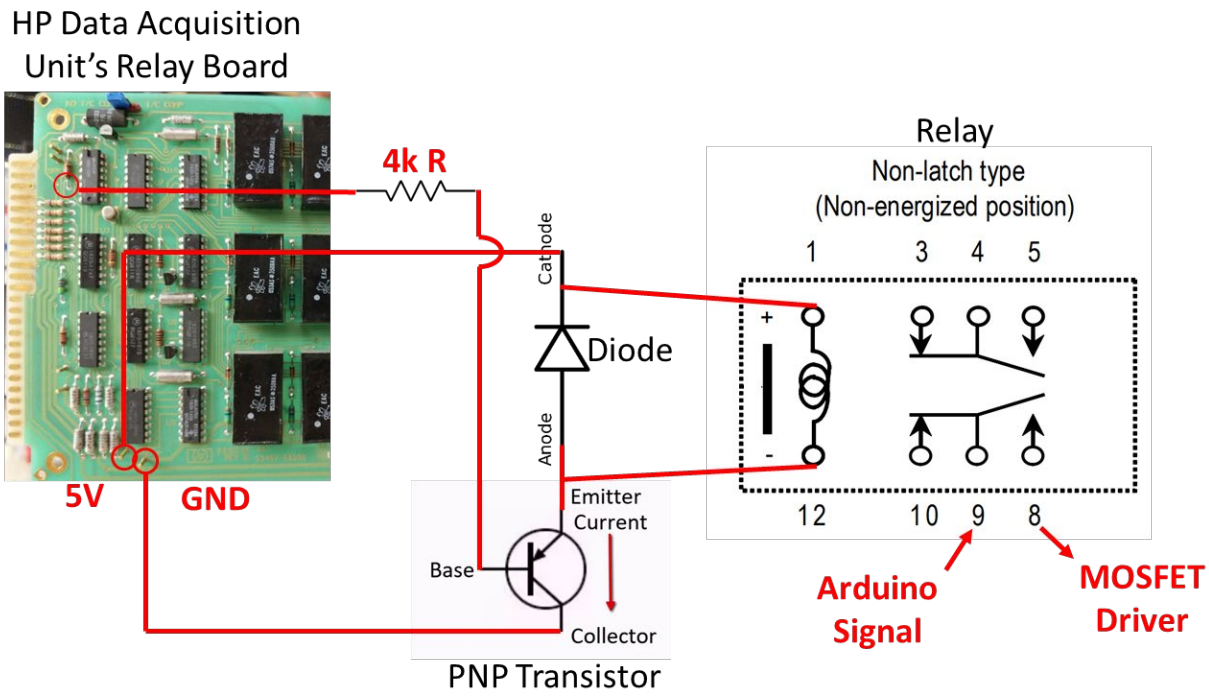

Figure A-2. Illustration of connecting a relay to HP data acquisition unit's relay board to produce one directional current while HP data acquisition unit is reading test data.

Arduino's input pin as shown in Fig. A-2. This isolate ground of each HP unit's ground and Arduinos from each EM test slots. The addition of relay enables me to simplify the Arduino's code by removing input reading commands completely. Fig. A-3 shows the simplified code that removes 8 lines of code, which were causing delays. This code was called "bit-banging pulsed width modulation" and great to use up to 4kHz. The advantage of it was that I have a full control of frequency and DF. It is simple to change frequency and DF. However, there were few disadvantages. First disadvantage and the most important for me is the limitation of frequency. The second disadvantage is that any interruptions affects the timing, which was shown in Fig A-1. The code needed to be tested few times with oscilloscope to achieve a desired frequency and DF.

With the limitation of bit-banging PWM preventing me from achieving 5kHz or higher frequency, an investigation was done using the PWM registers of Arduino's

microcontroller, ATmega328P, directly. As shown in Fig. A-4, several timer registers are used, such as TCCRnA and TCCRnB, WGM, CS, COMnA and COMnB, and OCRnA and OCRnB. TCCRnA and TCCCRnB are main control bits for timers. These each have Waveform Generation Mode bits (WGM), Clock Select bits (CS), and Compare Match

```
// Arduino loops generating desired frequency and duty factor
// Set pin as High/ON or Low/Off for each condition, and the waits for the duration of condition.
void loop()
{
  TriggerRead = analogRead(Trigger);
  if (TriggerRead < 512) // input <2.5V
   {
    digitalWrite(TTL1, LOW); //MOSFET Off (I through Samples) | Off Condition
    TriggerRead = analogRead(Trigger);
  }
  if (TriggerRead > 615) // Input >3V
  {
    //Condition 1
    digitalWrite(TTL1, HIGH); //MOSFET On (I bypass Sampes) | On Condition
    delayMicroseconds(con9); //for >1,000 Hz
   //Condition 2
    TriggerRead = analogRead(Trigger);
    digitalWrite(TTL1, LOW); //MOSFET Off (I through Samples) | Off Condition
    delayMicroseconds(con9); //for >1,000 Hz
  }
}
```

Figure A-3. A loop function part of Arduino code for 10kHz constant current square waveform pulsed DC and AC generation code without a relay connection to a HP data acquisition unit.

```
void setup() {
//This tells the Arduino to treat the pins as output.
  pinMode(3, OUTPUT); // B
  pinMode(11, OUTPUT); // A

// Resetting Timer/Counter Control Registers
  TCCR1A = 0;
  TCCR1B = 0;
  TCCR2A = 0;
  TCCR2B = 0;

// Internal clock settings -> Setting Timer/Counter Control Registers (TCCRnA and TCCRnB)
  TCCR2A = _BV(COM2A0) | _BV(COM2B1) | _BV(WGM21) | _BV(WGM20);
      // _BV(COM2A1) = non-trigger mode /// _BV(COM2A0) = trigger mode with _BV(WGM22)from TCCR#B
      // WGM21 + WGM20 = Fast PWM without trigger | Add WGM22 from B = Fast PWM with OCRA trigger
  TCCR2B = _BV(WGM22) | _BV(CS20);
      // CS20 = 001 = no prescaler | 010 = 8 | 011 = 32 | 100 = 64 | 101 = 128 | 110 = 256 | 111 = 1024 = CS20 CS21 CS22
      // _BV(WGM22) -> Trigger mode with OCR#A
  OCR2A = 159; // Pin 11 50 kHz | Changing-> change DF and frequency
  OCR2B = 79; // Pin 3 100 kHz | Changing-> change DF and frequency
}

void loop() {
}
```

Figure A-4. Arduino code for 10kHz constant current square waveform pulsed DC and AC generation with a relay connection between HP data acquisition unit and Arduino Uno.

Output A or B Mode bits (COMnA or COMnB). WGM controls modes of timer for TCCRnA and TCCRnB. CS control the clock's prescaler. COMnA and COMnB can enable, disable, or invert output A and B. OCRnA and OCRnB set a level for output A and B. Datasheet of ATmega328P is used to determine which values and which modes are needed to generate desired frequency and DF. Timer 2 is used with a trigger mode with few adjustments. The timer's top limit is set to 159 and use prescaler of 1 to achieve high frequency. As a result, 50kHz and 100kHz outputs with 50% DF are obtained. The frequency and DF calculations are shown in Fig. A-5.

```
Timer 2 (Adjusted, Trigger mode). 0-159 (160)
Output A frequency: 16 MHz / 1 / 160 /2 = 50,000 Hz
Output A duty cycle: = 50%
Output B frequency: 16 MHz / 1 / 160 = 100,000 Hz
Output B duty cycle: (79+1) / 160 = 50 %
```

Figure A-5. Calculation of frequency and duty factor resulted by using PWM timer registers.