IMPACT OF MATERIAL MODELS ON IMMERSION COOLED ELECTRONICS PACKAGES AND RELIABILITY ASSESSMENT FOR CHIP-PACKAGE INTERACTION

By

TUSHAR CHAUHAN

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Tushar Chauhan, 7th May 2021

DEDICATION

I would like to dedicate my PhD Dissertation

To

My parents

Alkaben, Jashvantbhai

For their love and support.

And, to

The best friend and life partner,

Vrushaly

For her encouragement and love.

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ABSTRACT

IMPACT OF MATERIAL MODELS ON IMMERSION COOLED ELECTRONICS PACKAGES AND RELIABILITY ASSESSMENT FOR CHIP-PACKAGE INTERACTION

Tushar Chauhan, Supervising Professor: Dereje Agonafer, The University of Texas at Arlington

The immersion cooling for IT equipment has been around for decades. From thermal energy management perspective, immersion cooling is better than traditional cooling technology. However, there is need for more work in open literature when it comes to impact of immersion cooling on the reliability of IT equipment to make it commercially implemented. Detailed study of material compatibility of the various electronics packaging materials for immersion cooling is essential to understand their failure modes and reliability. The stiffness and thermal expansion are critical material properties for electronics mechanical design. This part of the study mainly focuses on two things. The first part studies the impact of thermal aging in dielectric fluid for single-phase immersion cooling on the low loss material printed circuit boards (PCB) thermo-mechanical properties. The weight of the PCB samples was measured intermittently to quantify absorption of the dielectric fluid into PCBs or leaching of the plasticizers from PCBs into the fluid. Second part studies the impact of thermal aging on thermo-mechanical properties of low-loss PCBs in the air. The low-loss PCBs, Megtron6 are aged in the mineral oil, and in the air at four different temperatures, 22°C, 50°C, 75°C, and 105°C for 720

hours. The complex modulus and coefficient of thermal expansion are characterized before and after aging for both part and compared.

Thermal interface materials (TIMs) are critical for the thermal management of electronic packages. Different kinds of TIMs are currently used in the industry to reduce the contact thermal resistance and improve performance of electronic systems. While designing electronic systems, attention is given to characterizing the performance of TIMs and understanding the reliability of the TIM materials under different environmental loading conditions. As the reliability study of TIMs is not a matured subject, there is a growing interest to understand the mechanical behavior of TIM materials and how they change under various environmental loading conditions. In this study, four commercially available TIMs are studied under high temperature storage and thermal cycling loading conditions. In the first part of the work, the change in the thermal expansion coefficient of a representative of the group due to high temperature storage test is studied using Thermomechanical Analyzer (TMA). For the second part of the work, an assembly was made to the test the performance of the TIM materials under thermal cycling conditions. Samples with different TIM thickness were prepared and tested in an environmental chamber. An inspection was performed visually and with the aid of microscope. The results and lessons learnt are presented.

Chip package interaction (CPI) in combination with the ELK material presents novel challenges to reliability of electronics devices. As the geometric features gets smaller with advancing silicone technology nodes, the first level reliability presents more challenges.

Multi-level sub-modeling approach is utilized to study the CPI reliability. Various approaches to evaluate fracture mechanics parameters numerically have been investigated and compare for chip-package interaction application. This study investigates effect of the metal densities, crack locations on the chip package interaction reliability for BEOL stack.

CHAPTER 1. INTRODUCTION

1.1. Motivation

As Gordon Moore predicted the number of transistors will double on device every two year back in 1965, knows as Moore's law. The integrated complexity was traded by manufacturing yield to reduce the cost per component [1] [2]. The Dennard's scaling in 1975 provided more technical insight into scaling of the MOFET transistors. The gate oxide thickness, channel width, and channel length were scaled by a scaling factor to fulfill Moore's law predictions [3]. The voltage and the current also scaled by same scaling factor, and as a result the power density of the device remain constant moving from one silicone technology node to next by scaling down [3]. The Dennard scaling was leveraged by industry until ~2004 when it hit limit due short channel for 1 nm gate oxide thickness [4]. Increasing transistor density with no power scaling was big challenge to overcome for electronics industry. The clock speed for the processor has been almost stagnant as shown in Figure 1. The way forward industry adopted is multi-core processors.

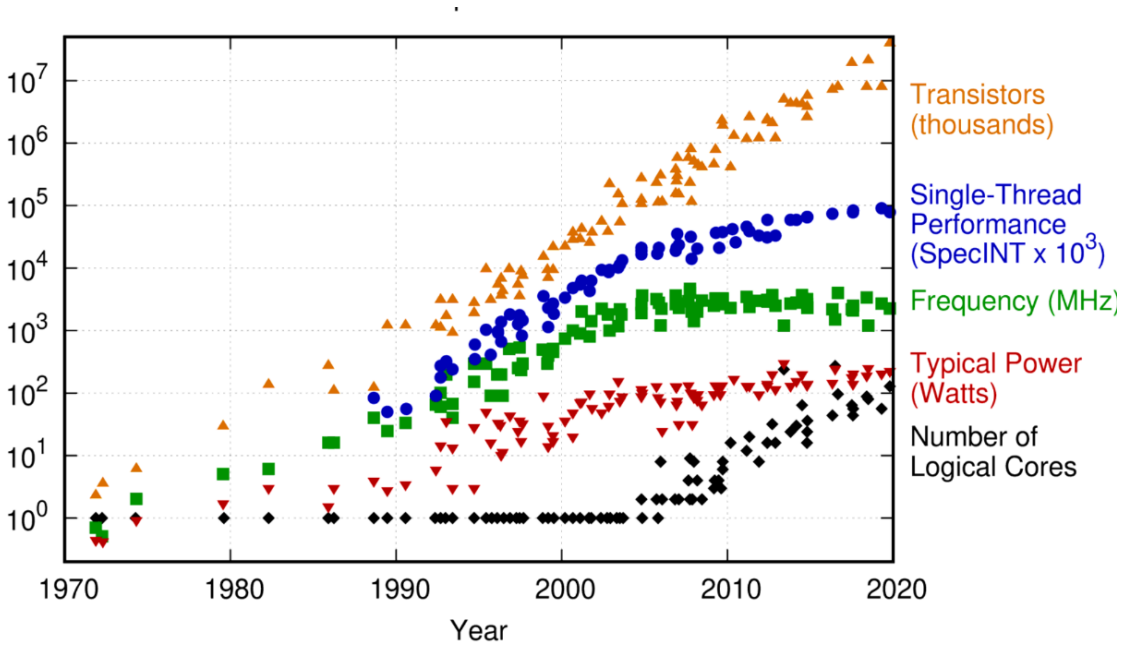

Figure 1: Microprocessor trend for last 48 years [5]

The Moore's law was driving force for evolution of electronics industry. While the Moore's law is not completely out of game, it has slowed down. Electronics industry is following the International Technology Roadmap for Semiconductors (ITRS) defined by Institute of Electrical and Electronics Engineers (IEEE)[6]. Once the two-dimensional(2D) densities reached the limit, third dimension was utilized to stack similar chips in three-dimension(3D) known as homogenous integration, also known as More Moore (MM). Industry were able to leverage MM to increase the density at chip level. Then came, More than Moore road map (MtM), introduced by IEEE in 2015, also known as ITRS 2.0, which presented scope to increase functional density at chip level as well as package level [6]. The MtM shifted focus of innovation from chip to system level. The Heterogenous Integration (HI) is critical for implementing MtM. IEEE defined HI as "the integration of

separately manufactured components into a higher-level assembly that, in the aggregate, provides enhanced functionality and improved operating characteristics"[6].

While HI provides the way forward to cater increasing functional density for electronic circuits, it also presents novel challenges. Some of the major challenges are thermal management and reliability. Thermal management comprises issues like hot spots, thermal density, how to improve the heat dissipation capabilities of packages. Reliability comprises, models for reliability prediction, improved fracture toughness of dielectrics, CTE mismatch compensation for large die and warpages to name some [6].

There are several ways to address these challenges such as experimental analysis, numerical(simulation) analysis, and analytical analysis. Most of the problems are too complex to be addressed by analytical approach. The experimental analysis is excellent approach and been followed widely, at the same time it requires enormous economic resources and time consuming. Numerical approach can address complex problems with advancements in computational resources recently. One of the most widely used numerical approach is finite element analysis. Lots of commercial codes out there makes it easy to implement and time efficient.

Finite element analysis has three main aspects, model (geometry), material models, boundary and loading conditions. The electronics devices is made of various materials like silicon, Accuracy of material properties and material models of various material in electronics package stack are crucial for the numerical analysis. The material models are

very important for finite element analysis studied, the accuracy of the results dependents highly on the accuracy of the material properties of the materials in the electronics packages namely, silicone die, die attach, solder ball, thermal interface materials, substrate, printed circuit boards [7] [8] [9] [10] [11].

Most common failure modes observed in the electronics devices for front end of the line are time dependent dielectric break down, hot carrier injection, negative bias temperature instability, surface inversion [12]. Common failure mechanisms for the back end of the line are time dependent dielectric break down, aluminum or copper electromigration/corrosion, copper/aluminum stress migration [12]. Fatigue failure due to temperature cycling and thermal shock, interfacial failure due to temperature cycling and thermal shock, intermetallic and oxidation failure due to high temperature, failure due to tin whiskers, are commonly observed failure mechanisms in the electronics packaging [12]. For the electronics packaging, especially for the failure due to thermo-mechanical stresses due to coefficient of thermal expansion (CTE) mismatch, material properties such as Youngs modulus and CTE are crucial [13] [14].

1.2. Research objective

The research conducted in this work will help to understand different techniques for thermo-mechanical material characterization for essential components of electronic packages. Mechanical characterization of the low loss printed circuits boards after thermal aging in mineral oil and in air will help understand how thermal aging affects the

modulus and CTE after the aging and how it will impact the reliability and could be leveraged for numerical study.

The second project will help understand the impact of thermal aging on the thermal expansion or CTE of thermally conductive gap fillers and impact of thermal cycling on the thermal degradation of the thermally conductive gap fillers. The final project will help choose best fracture analysis numerical technique for the fracture/delamination assessment within back end of the line structure. Parametric study done for the flip chip ball grid array package under the chip package interaction loading to study the impact of wiring density and crack location within BEoL structure on the reliability will provide the guideline for the similar future studies.

1.3. Organization of dissertation

Dissertation thesis contains four chapters, first chapter contains the motivation for this research work and objective. Three chapters focuses on the three different research projects. Each project contains, abstract, introduction, materials and methods, results, discussion, conclusion, and summary sections. Introduction contains literature search, contemporary work, motivation, other technical concepts and information necessary to understand the research work. Materials and methodology describe sample preparation methods, experimental instruments and know-how of their working principles, and experimental procedures. For numerical studies, this section contains the model dimensions, material properties used, modeling techniques, mesh sensitivity analysis and

other necessary concepts and information necessary to understand the research work presented. The result sections contain the contour plots, bar plots, other type of result plots, tabulated results, presented in best format to comprehend the obtained results with the error bars and technical assumptions if any. The discussion sections focus on comprehending and explaining the obtained results in the contacts of the study and research objectives. The conclusions and summary section focus on the main conclusions and summarizes the work and important take away from this study.

CHAPTER 2. IMPACT OF IMMERSION COOLING ON THERMO-MECHANICAL PROPERTIES OF LOW-LOSS MATERIAL PRINTED CIRCUIT BOARDS

2.1. Abstract

With the boom in consumer electronics, the need for information transfer has increased multifold. The internet has become everyday necessity. The requirement for real-time data transmission is all time high increasing the need for more data centers. On the other hand, for traditional datacenters one third of the total energy consumed is directed towards cooling information technology (IT) equipment. High demand for new datacenters, vast amount of energy consumption, and their impact on the climate requires datacenter industry to make them energy efficient and opt for immersion cooling technologies. The immersion cooling for IT equipment has been around for decades. From thermal energy management perspective, immersion cooling is better than traditional cooling technology. However, there is need for more work in open literature when it comes to impact of immersion cooling on the reliability of IT equipment to make it commercially implemented. Detailed study of material compatibility of the various electronics packaging materials for immersion cooling is essential to understand their failure modes and reliability. The stiffness and thermal expansion are critical material properties for electronics mechanical design. Printed circuit board/substrate is a critical component of electronic package and heavily influences failure mechanism and reliability of electronics system/package. This study mainly focuses on two things. The first part studies the impact of thermal aging in dielectric fluid for single-phase immersion cooling

on the low loss material printed circuit board's (PCB) thermo-mechanical properties. The weight of the PCB samples were measured intermittently to quantify absorption of the dielectric fluid into PCBs or leaching of the plasticizers from PCBs into the fluid. Second part of the study is the impact of thermal aging on thermo-mechanical properties of low-loss PCBs in the air. The low-loss PCBs, Megtron6 are aged in the mineral oil, and in the air at four different temperatures, 22°C, 50°C, 75°C, and 105°C for 720 hours. The complex modulus and coefficient of thermal expansion are characterized before and after aging for both part and compared.

2.2. Introduction

The heat generated by electronics equipment in datacenter has been consistently increasing due to developments in the semiconductor industry and miniaturization. It is further fueled by the advances in technologies and online services [15]. Out of total energy consumed by data center, approximately 52% is consumed by demand-side systems within IT equipment like processors, server power supply, storage, communication, and other services while 48% is consumed by supply side system including UPS, switch gears, lighting, PDU and cooling. The traditional cooling alone consumes approximately 38% for total datacenter energy consumption[16]. The electricity consumption of the datacenters is increasing all over the world with annual increase rate of 10% since 2005. As per Japanese ministry of economy, the electricity consumption will be five times greater by 2025. [17] In 2014, US datacenters consumed approximately 70 billion kWh, which is 1.8% of total U.S. electricity consumption. The

electricity consumption of datacenters in U.S. has increased by 4% from 2010 to 2014. [18] The energy consumption of china's data center industry was 160.89 TWh in 2018 and is expected to reach 266.79 TWh by 2023. [19] The carbon footprint of the datacenters from 2002 was 76 MtCO2e, and is expected to increase to 259 MtCO2e with annual increase rate of 7%. [20] Because of the strong electricity usage of datacenters, especially cooling, the reduction of the energy consumption is increasingly becoming top priority for IT businesses and policy makers.[21]

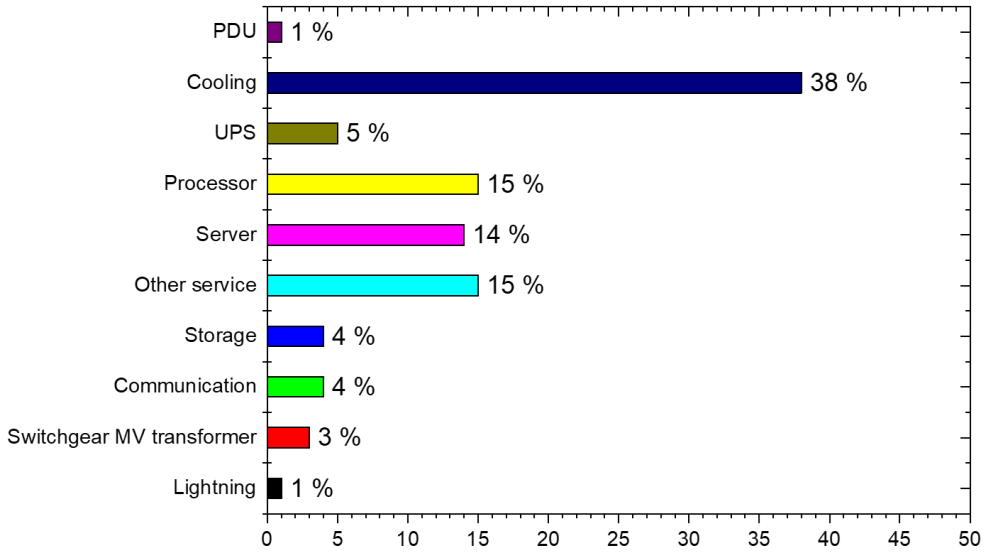

Figure 2: Analysis of typical datacenter energy consumption

Despite impressive progress being made during the past decades, there are still serious technical challenges in thermal management of electronics devices or microprocessors. Two main cooling challenges are adequate removal of increased heat flux and highly non-

uniform power dissipation.[22] The maximum power dissipation and heat flux for the high performance microprocessors are increasing and have reached to more than 300 W and 190 W/cm^2. The heat dissipation of the chip is increasing approximately 7% annually.[3] The air cooling is not able to cope with this increasing heat flux density. There is a need for data center industry to explore and implement different energy efficient cooling technologies. Figure 3, shows the approximate maximum power density per rack supported by respective cooling technology and power usage efficiency. An air cooling and indirect liquid cooling can handle up to 30 kW/rack and 60 kW/rack respectively. Beyond this power density, the direct liquid cooling/immersion cooling is required. [23] The power usage efficiency (PUE) is highest for the immersion cooling with respect to air cooling and indirect cooling technology.

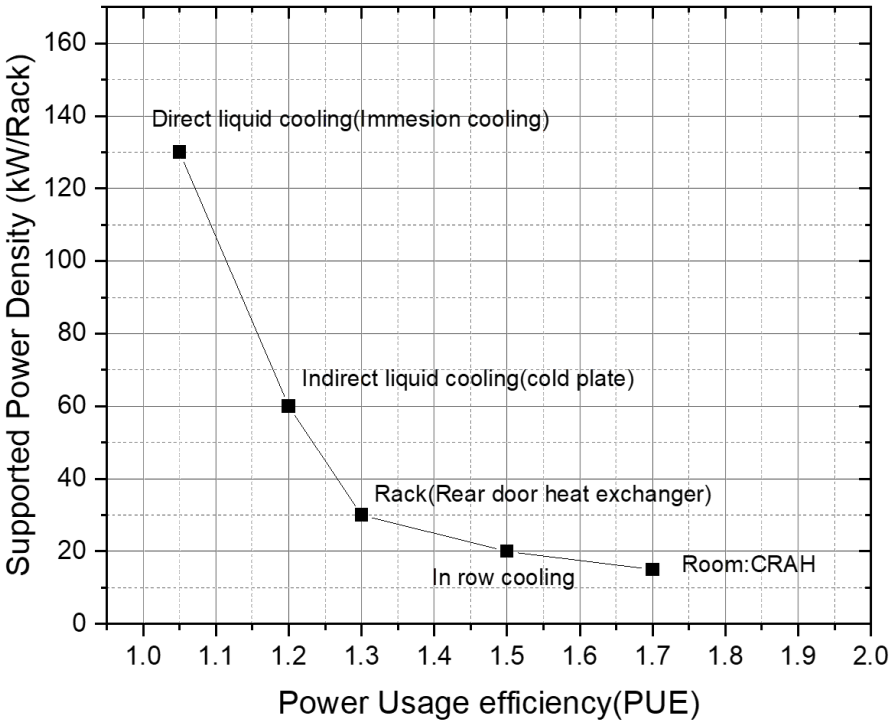

Figure 3: Cooling techniques for data center and supported power densities and PUEs [23]

The immersion cooling is classified based on the phase of the dielectric fluid, single-phase immersion cooling and two-phase immersion cooling. Further it has been classified based on the enclosure into enclosed chassis, open bath and hybrid. [24] For the single-phase immersion cooling the dielectric fluid is circulated in close loop to absorb heat from IT equipment and in secondary loop the heat is rejected to atmosphere from dielectric fluid. The dielectric fluid remains in the liquid phase, provides 1200 times higher volumetric thermal mass than the air-cooling [25]. In two-phase immersion cooling, dielectric fluid

changes phase from liquid to vapor upon absorbing heat from IT equipment beyond its boiling temperature. It again condenses back to liquid phase from vapor by rejecting heat to condenser, the heat will be rejected to ambience ultimately.

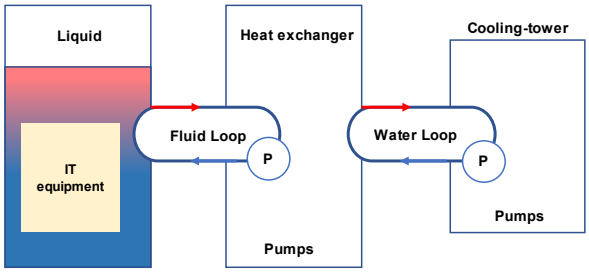

Figure 4: Single phase Immersion cooing conceptual diagram.

Controlled impedance and specific transmission line performance are necessary for design and high-performance materials for circuit board lead electronics industry to invent FR-4 grade dielectric materials to meet the need. High-speed designs requiring low-loss tangent and lower dielectric constant have steered material research and development to invent advanced FR-4 laminates like Panasonic Megtron6, Isola FR408, Nelco N4000-13, and even e-glass engineered to lower dielectric constant such as Nelco's SI(for signal integrity) cloth[26]. The main advantage of Megtron6, the low-loss materials printed circuit board (PCB) compared to traditional FR-4 PCBs are low transmission loss, low dielectric constant, low dielectric dissipation factor, and high heat resistance. The dielectric constant and dissipation factor for Megtron6 is 3.5, and 0.003 compare to 4.2, and 0.018 for traditional FR4 PCBs respectively.[27] MEGTRON6 PCBs are used for crucial

applications such as ICT infrastructure equipment, supercomputers, measuring instrument, antenna. [28]

Reliability study for the air cooled ITE is mature. The dominant failure modes and the mechanisms are established and defined for the air-cooled IT equipment and electronics packaging in form of JEDEC standard [12]. The operating conditions for the immersion cooling is different than air cooling as the ITE is immersed in fluorocarbon or hydrocarbon based dielectric fluids[29] . The various failure prone parts namely silicon die package, back end of line structure, underfill, die attach, solder balls, substrate and printed circuit board remain in the contact with the dielectric fluid constantly replacing the air. Immersion cooled systems also undergoes the temperature change due to load fluctuation. Change in the cooling fluid from air to dielectric fluid entails the detail investigation study of reliability and material compatibility for immersion cooling. Different types of mechanical failure modes have been observed in the electronics packaging. Most dominant mechanical failure mechanisms for electronic packages are fatigue failure due to temperature cycling, instantaneous fracture due to thermal shock, and tin whiskers.[12] Electronic package contains various materials stacked together having different coefficient of thermal expansion (CTE). This CTE mismatch together with changing temperature within system induces mechanical stresses. The impact of mechanical stresses must be studied to gain better understanding of the reliability of electronics packaging for immersion cooling systems.

There are three major ways to study the mechanical reliability of immersion cooling, i.e. experimental, analytical, and numerical. The experimental analysis is pricier among all three and the problem at hand is too complex to study analytically. Numerical method proves itself as the cost and time effective approach; a finite element method is popular and widely adopted numerical method. One of the key factors for failure analysis using finite element is accuracy of material properties of electronic packages to formulate the problem. The change in the material properties with aging in the dielectric fluids at high temperatures is crucial information for such numerical study of failure analysis under various loading conditions namely temperature cycling and creep.

Kennedy et al. demonstrated, for epoxy/E-glass after aging in sea water, the fatigue strength decreased by 20% and tensile stress was decreased by 25% [30]. Kumarasamy et al. concluded, the tensile strength and modulus of glass-fiber-reinforced polymer deceased after aging in aviation fuels namely kerosene, biodiesel, and blend fuel[31]. It is important to study the impact of aging electronic materials in the various dielectric fluid on their material properties.

Ramdas et al. showed, modulus decreased for 370HR and 185HR printed circuit boards after aging them in EC-100 dielectric fluid for 700 hours[10]. Shah et al concluded that the Young's modulus decreased significantly, increase in CTE for printed circuit boards of server immersed in mineral oil for 8 months compared to air cooled server. [8] Shah aged printed circuit board in mineral oil and EC 100 dielectric fluid for 288 hours at 45°C to find the increase in Young's modulus and CTE. [32] This study focuses on impact of thermal

aging of Megtron6 printed circuit board in dielectric fluid, mineral oil. Megtron6 PCB was aged for 700 hours in the mineral oil and in air at four different temperatures namely 25°C, 50°C, 76°C and 106°C. Modulus and CTE was measured for the samples aged in mineral oil and for samples aged in air using Dynamic mechanical analyzer and Thermomechanical analyzer respectively and compared.

2.3. Materials and Methods

2.3.1. Method

2.3.1.1. Dynamic Mechanical Analyzer (DMA)

Dynamic Mechanical Analysis is the technique to measure sample's kinetic properties such as elasticity and viscosity. The sinusoidal load is applied to sample via probe in form of stress/strain and sinusoidal stress/strain caused is measured and plotted as a function of time or temperature. [33] Different module of DMA including tension, bend, shear, and compression deformation attachment are used to measure different material properties depending on sample shape, modulus, and measurement purpose. The viscoelastic properties like storage modulus and loss modulus can be measured by DMA.[33] The Complex Modulus, whose magnitude is comparable to Young's modulus can be obtained using equation (1) using storage and loss modulus.[7]

$$E^* = E' + iE'' \qquad (1)$$

$$|E^*| = \sqrt{E'^2 + E''^2} \qquad (2)$$

$$Tan\ \delta = \frac{E''}{E'} \qquad (3)$$

In equations (1), (2) and (3), E* is complex modulus, E' is Storage modulus and E" denotes loss modulus. The DMA used for this study has a temperature range of approximately -150°C ~ 600°C. Auto LN_2 gas cooling unit dispenses liquid nitrogen to reduce temperature of the furnace below the room temperature.[34] Figure 5 shows major components of DMA.

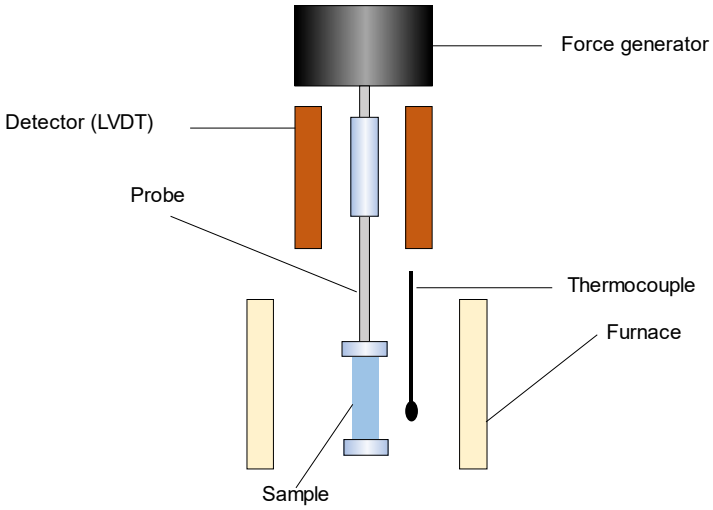

Figure 5: Dynamic Mechanical Analyzer.[33]

2.3.1.2. Thermomechanical Analyzer (TMA)

Thermomechanical analysis is technique in which the deformation of the sample is measured as a function of time or temperature while non-oscillating stress is applied. [35] The Thermo-mechanical Analyzer module is used to measure thermal mechanical characteristics such as thermal expansion, thermal contraction, and softening. The Thermal Stress-Strain Analyzer is used to measure the stress-strain as function of time or temperature. The TMA has a temperature range of approximately -150°C ~ 600°C. One of the three probes, expansion/contraction probe, penetration probe, tension probe can be selected based on the analysis and sample type. Liquid nitrogen is used as the cooling agent to bring the temperature in furnace below room temperature. The sensor is a linear variable differential transformer.[36] Figure 6 shows major components of TMA.

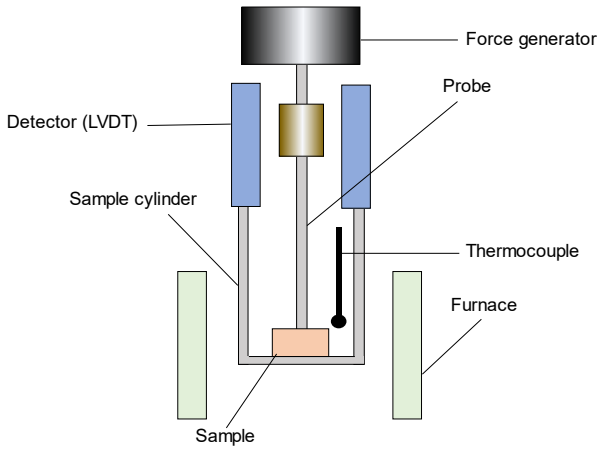

Figure 6: Thermomechanical Analyzer.[35]

2.3.1.3. Weighing scale

To study the dielectric fluid absorbance into the PCB sample with respect to thermal aging in dielectric fluid a digital weighing scale was used. The weighing scale has a stage inside a glass enclosure to avoid the errors caused by the air pressure around the stage. It has the readability of 0.01 mg and repeatability (standard deviation) of ≤± 0.02 mg to measure the slightest change in weight of the PCB sample. [27]

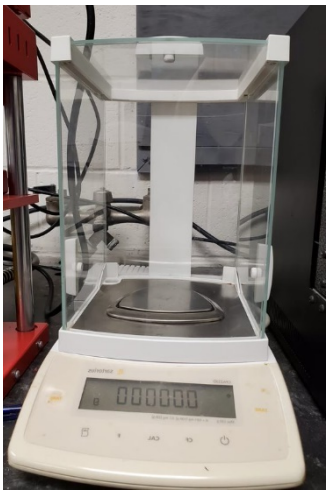

Figure 7: Weighing scale.

2.3.2. Sample Preparation

2.3.2.1. Cutting of the samples

The ~2 mm thick Megatron6 PCB was cut into at least four samples each for each case studied for TMA and DMA to ensure statistical accuracy. For DMA bending attachment the PCB was cut into samples of 50 mm X 4 mm samples approx. Total 32 samples were prepared for DMA measurements. For CTE measurement using TMA, the PCB was cut into samples of 8mm X 4mm approx. Total of 32 samples for TMA measurement were prepared. Figure 8 shows the typical sample for DMA and TMA. In addition to 32 PCB samples, 2 dummy samples were prepared to study the dielectric fluid absorbance into PCB.

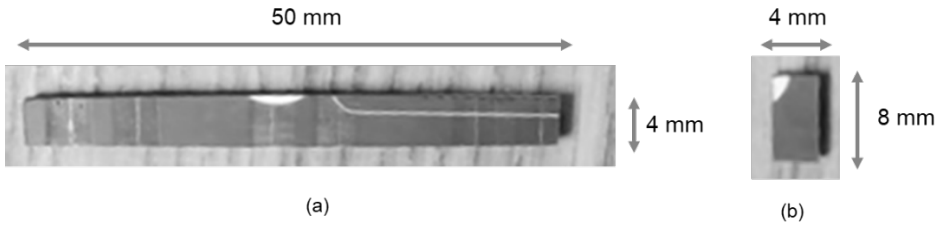

Figure 8: (a) DMA Sample; and (b) TMA Sample

2.3.2.2. Thermal Aging

There are 8 different cases of aging performed based on aging environment parameters namely, aging temperature and aging fluid. 4 PCB samples each for DMA and TMA were aged at four different temperatures (25°C, 50°C,75°C, and 105°C) and in two different

fluids (air and mineral oil). Details of the number of samples aged for ~ 720 hours for each case is given in Table 1. Figure 9 shows the typical aging set up of PCB samples immersed in mineral oil and placed into furnace.

Table 1: Aging of the Metron6 PCB samples in air and dielectric fluid (mineral oil)

Aging temperature	**Aging time**	**Number of samples aged Mineral oil**	**Number of samples aged in Air**
25°C	~ 720 hours	4 DMA samples + 4 TMA samples	4 DMA samples + 4 TMA samples
50°C		4 DMA samples + 4 TMA samples	4 DMA samples + 4 TMA samples
75°C		4 DMA samples + 4 TMA samples	4 DMA samples + 4 TMA samples
105°C		4 DMA samples + 4 TMA samples	4 DMA samples + 4 TMA samples

Figure 9: Aging PCB sample immersed in Mineral oil inside a furnace.

2.3.3. Experimental Procedure

2.3.3.1. DMA

Samples used for DMA tests had a length of ~50 mm, width of 4 mm, and ~2 mm thickness. The sample was measured using the digital calipers having 0.02 mm accuracy. Based on the expected modulus of the material and the sample geometry factor calculated from sample dimensions, bending attachment was chosen for the current study. The post-aging oil immersed samples were gently cleaned with paper towel before mounting to DMA for test. The settings used for testing samples in the bending mode are for hard sample shown in Table 2. The experiment was performed for 0.5, 1, 2, 5 and 10 Hz frequencies and temperature range from -40°C to 220°C. Most used frequencies in the industry are selected to account for the frequency and temperature dependent behavior of material. Measurements for 1 Hz were used to compare the properties of pre-aging and post-aging samples. The isothermal hold of was performed at the beginning temperature of -40°C to stabilize the temperature fluctuations within +/- 3°C. To account for the thermal mass of the sample and reduce the lag in sample temperature to furnace temperature, slower heating rate of 2°C/minute was used during experiment compare to 10°C/minute. Figure 10 shows the sample mounted for the testing using bending attachment.

Table 2:Settings use for DMA testing in tensile mode.

Parameters	Value
Minimum tension/ compression force	200 mN
Tension/ compression force gain	1.5
Force amplitude	2000 mN
L Amplitude	10 um

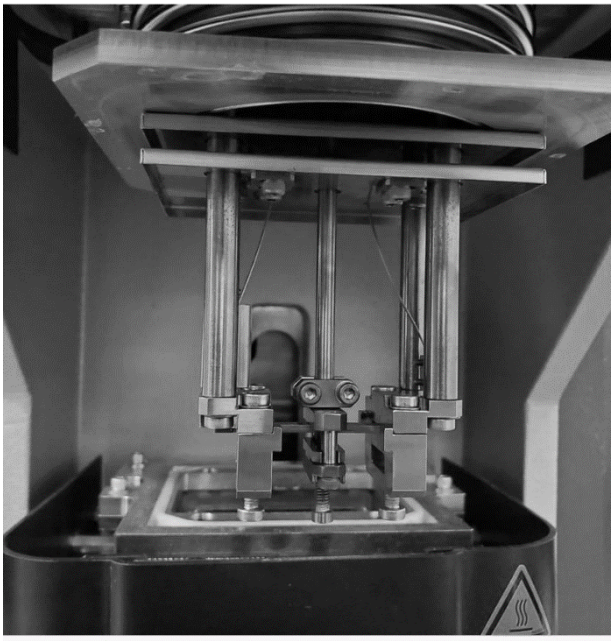

Figure 10: Megtron6 sample mounted on DMA for testing.

2.3.3.2. TMA

Typical rectangular sample of ~8 mm length, ~4 mm width and ~2 mm thickness was used for TMA measurements. The in-plane CTE of the Megtron6 PCB was measured, and sample were mounted such that the length (8mm) was parallel to the measurement probe of TMA as shown in Figure 10. TMA probe was cleaned before starting the series of measurement with ethanol to remove any residuals on the probe. The post-aging oil immersed samples were cleaned gently with paper towel to remove access mineral oil on the sample before mounting. Aluminum CTE was measured to perform and compared with literature value for sanity check. For the current study, Thermal-mechanical Analyzer mode of the TMA and expansion/compression quarts probe of 3 mm diameter is used.

Figure 11: Megton6 PCB sample mounted on the TMA for testing.

Optimum 100 mN force were constantly applied on the sample through probe during experiment to maintain proper contact between sample and probe and to not constrain the thermal expansion of the sample during experiment. The experiment was performed for temperature range -40°C to 220°C. Isothermal hold was performed with stability criteria of having initial temperature fluctuation within +/- 2°C to attain desired temperature of the sample at beginning of test. The length and thickness of the sample were measured with digital calipers having the accuracy of 0.02 mm. The length of the sample were measured using TMA with accuracy of 0.05 mm [36]. Measurement was performed with ramp rate of 2°C/minute, lower than the found in literature to mitigate a little lag between TMA furnace temperature and sample temperature.

2.3.3.3. Weighing the post-aging oil immersed dummy PCB sample

Two dummy Megtron6 PCB samples of size ~30 mm length, ~4 mm and ~2 mm thickness were used to study dielectric fluid absorbance into Megtron6 PCB material. One of the dummy samples was immersed in mineral oil at 25°C and other at 50°C. The samples were taken out at interval of ~24 hours to measure the weight. The process was repeated for ~650 hours. The total time from weight measuring process was approximately ~5 minutes, including taking out sample, weighing, and putting it back. Megtron6 PCB dummy sample was gently cleaned to remove access mineral oil on the surface of sample for precise measurement.

2.4. Results

2.4.1. DMA results

2.4.1.1. Complex modulus for each temperature for immersed and Air case

Figure 12 to Figure 15 show the comparison of DMA measurement of the complex modulus for the immersed and non-immersed sample at 25°C, 50°C, 75°C and 105°C, respectively. The measurements were run for at least 4 times for the immersed sample and at least 3 times for the non-immersed sample. The average of the complex modulus along with the standard deviation is shown in the figure below for the temperature range of the -40°C to ~210°C.

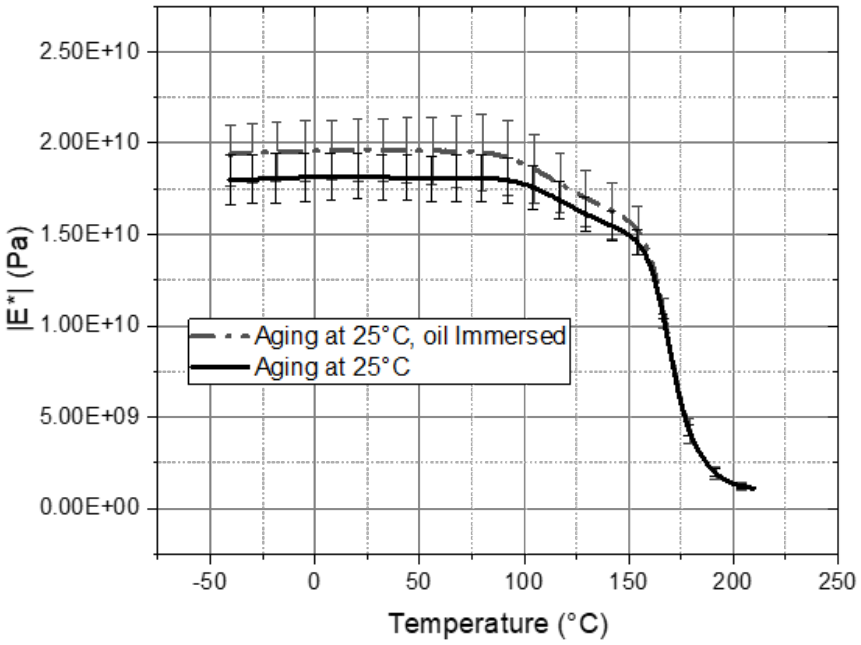

Figure 12: Comparison of complex modulus aged at 25°

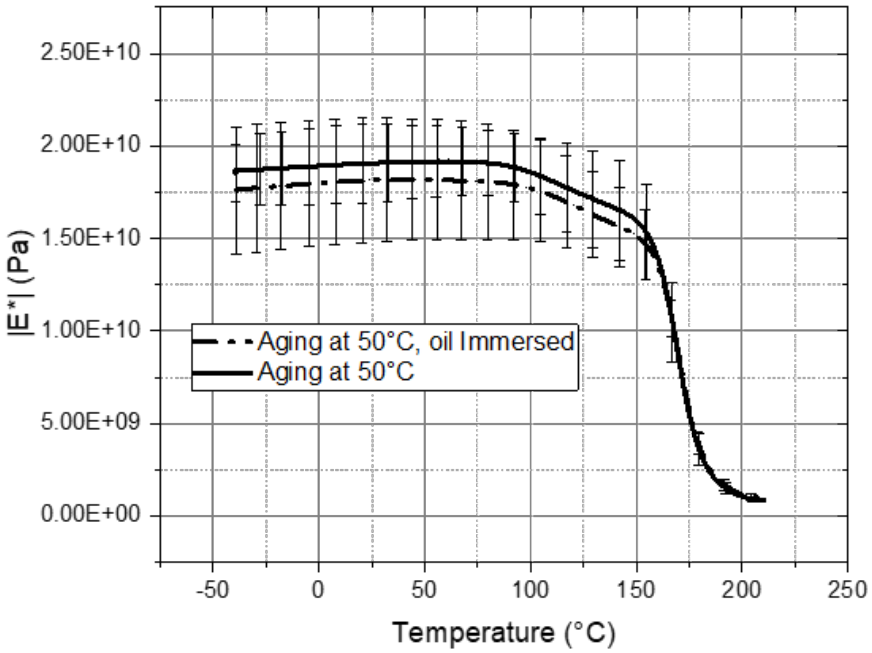

Figure 13: Comparison of complex modulus aged at 50°C.

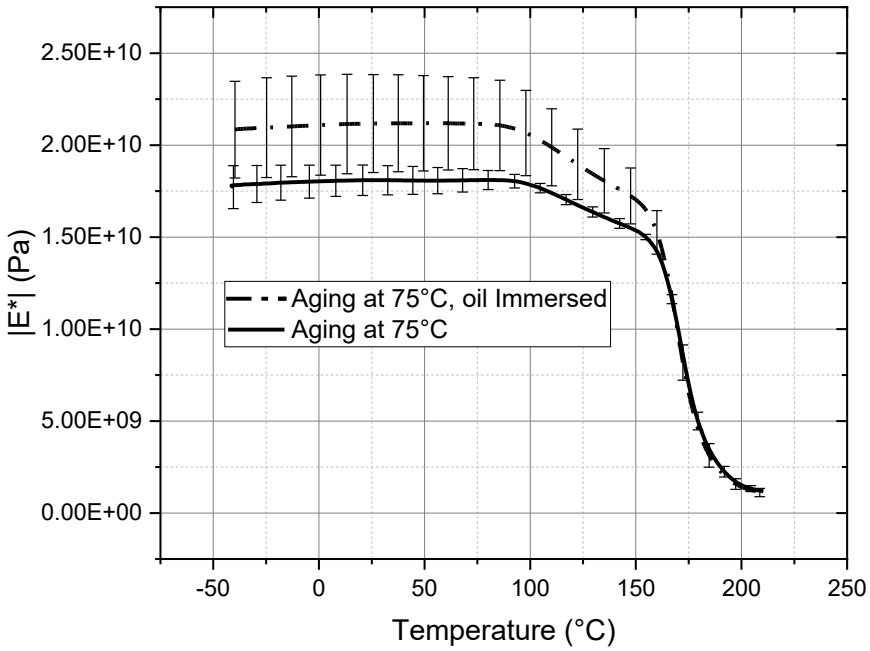

Figure 14: Comparison of complex modulus aged at 75°C

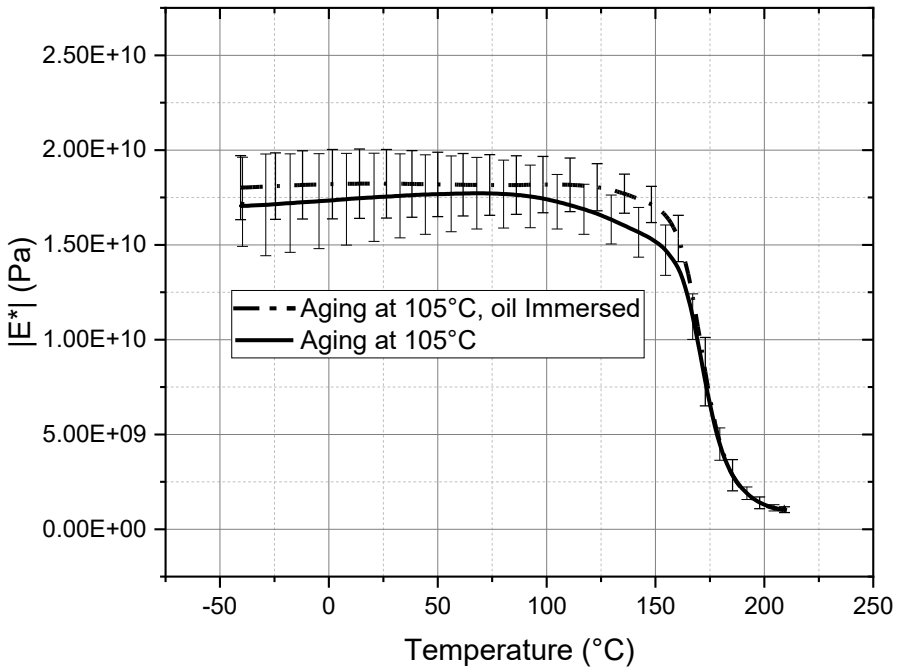

Figure 15: Comparison of complex modulus aged at 105°C.

2.4.1.2. Combine plot for all the temperatures for the immersed samples

Figure 16 shows the combined plot for all the temperatures for the immersed samples along with the standard deviation of the complex modulus.

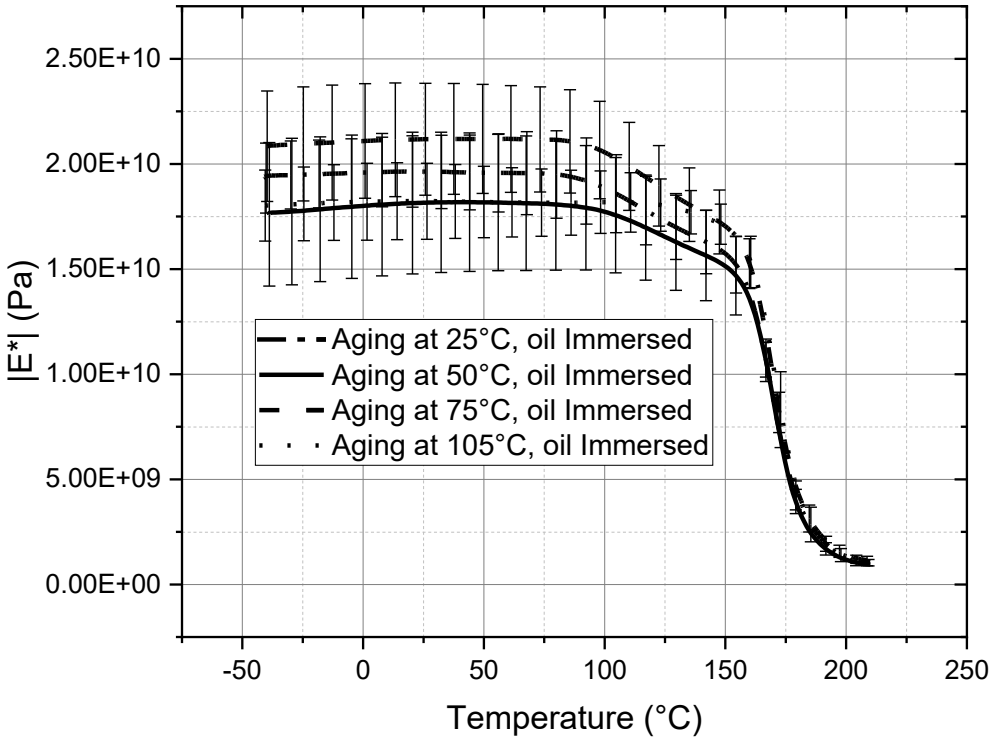

Figure 16: Complex modulus of the immersed sample at different temperature.

Figure 17 shows the combine plot for all the temperatures for the non-immersed samples along with the standard deviation of the complex modulus.

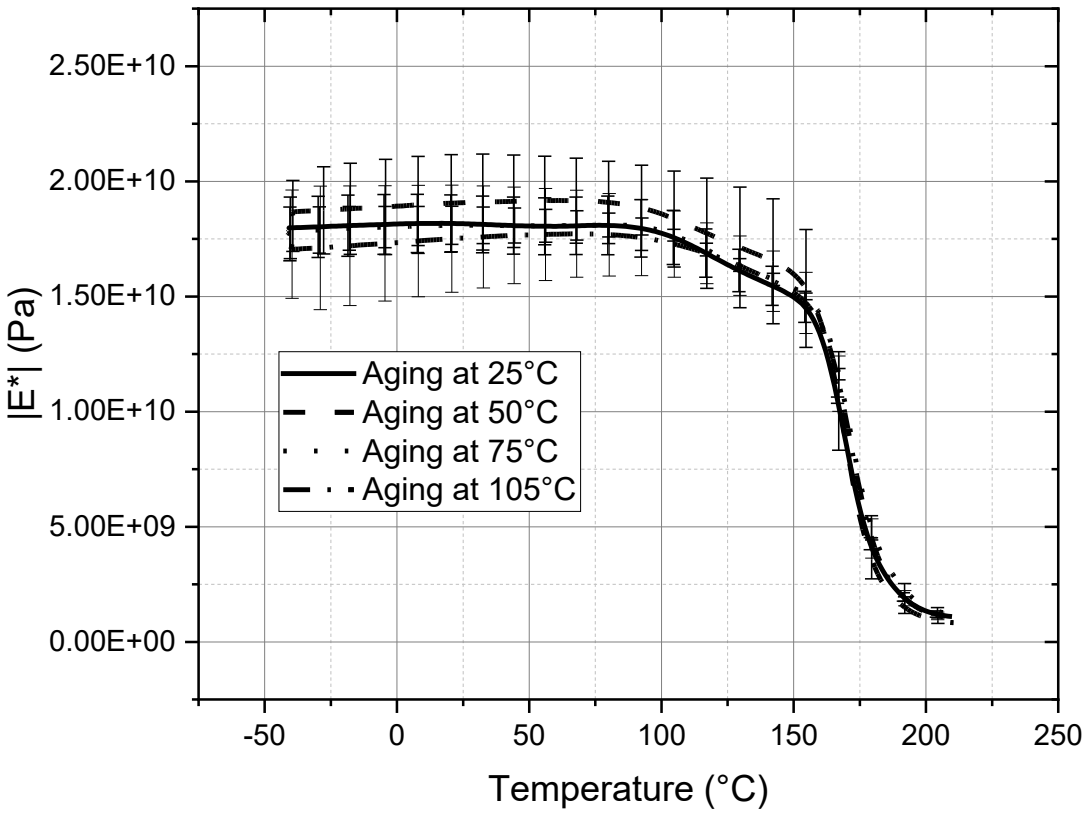

Figure 17: Complex modulus of the non-immersed sample at different temperature.

2.4.2. TMA results

Figure 18 and Figure 19 shows the TMA measurement of the coefficient of thermal expansion for non-immersed and immersed sample thermally aged at different temperature, respectively. Figure 20 shows the comparison of CTE for non-immersed aged and immersed aged samples at four different temperatures. At each temperature,

at least 4 measurement was completed, and the average and the standard deviation is shown in the figure below.

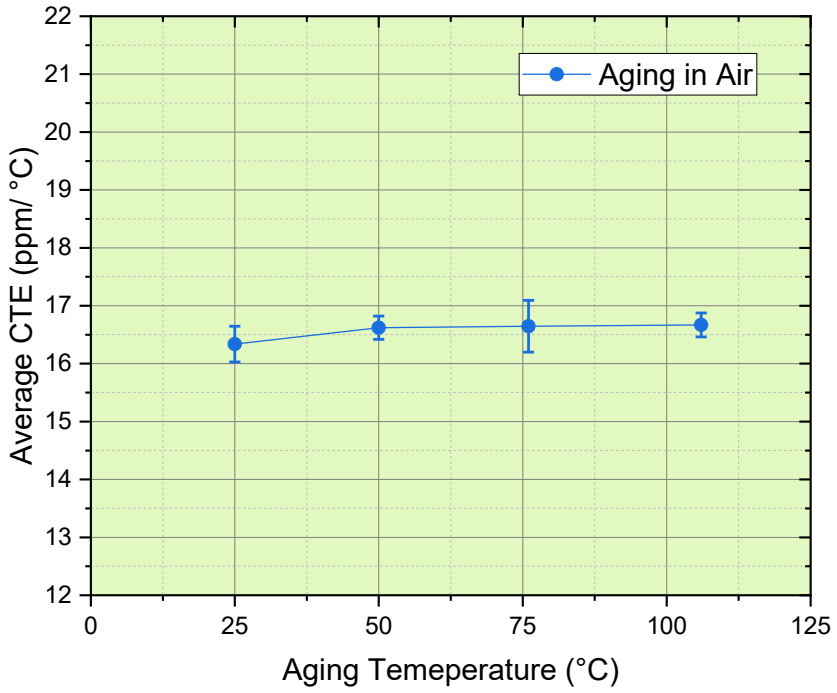

Figure 18: Coefficient of thermal expansion of the non-immersed sample at different temperature.

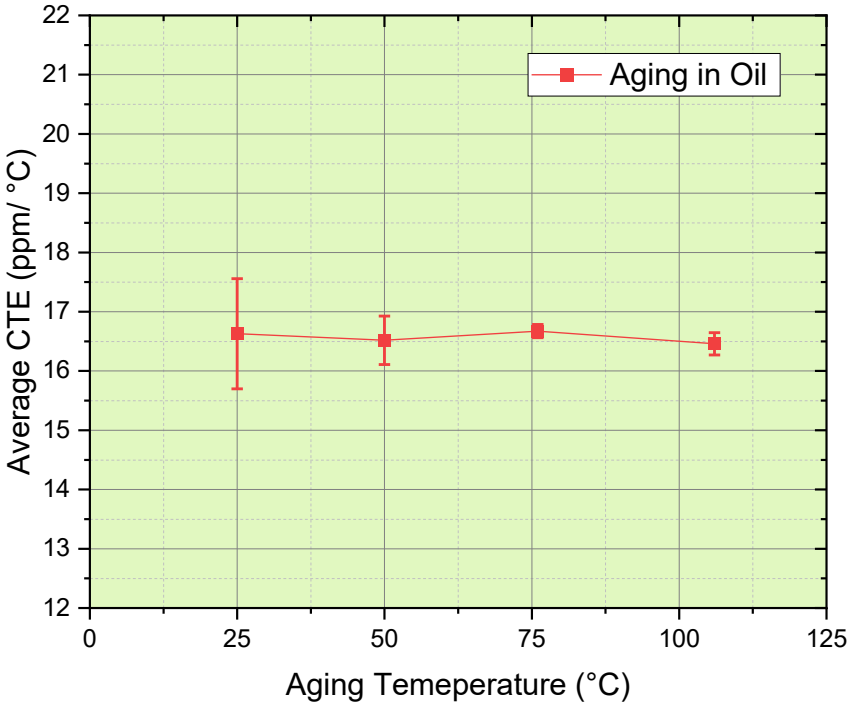

Figure 19: Coefficient of thermal expansion of the immersed sample at different temperature.

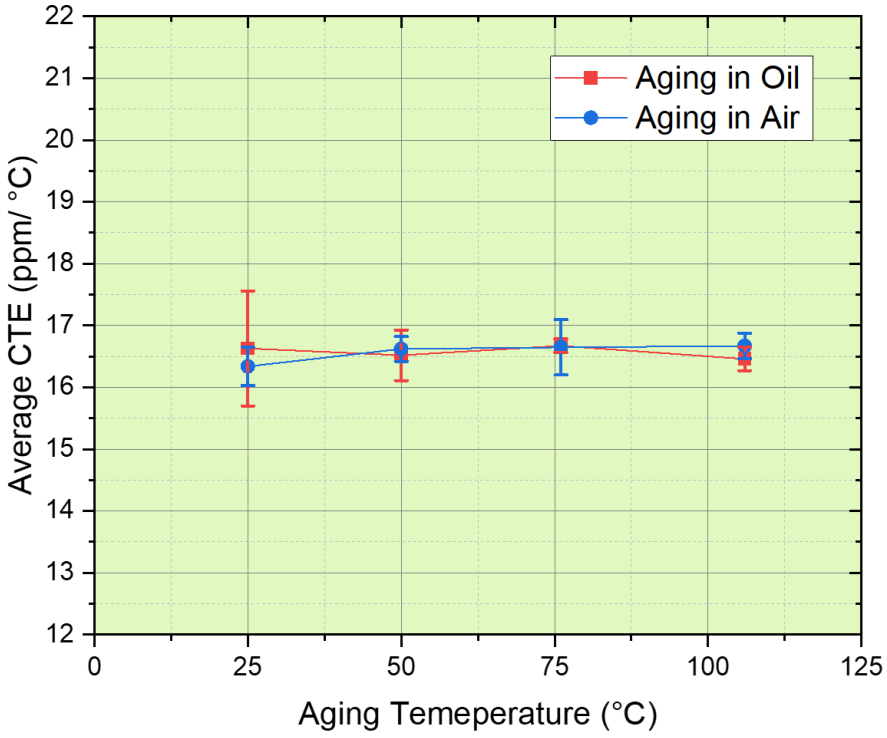

Figure 20: Coefficient of thermal expansion of the immersed and non-immersed sample at different temperature.

2.4.3. Weight absorbance results

Figure 21 and Figure 22 shows the weight measurements for the dummy Megtron PCB samples immersed into mineral oil at two different temperatures 25°C and 50°C respectively to study dielectric fluid absorbance into PCB sample. One sample was used for each temperature.

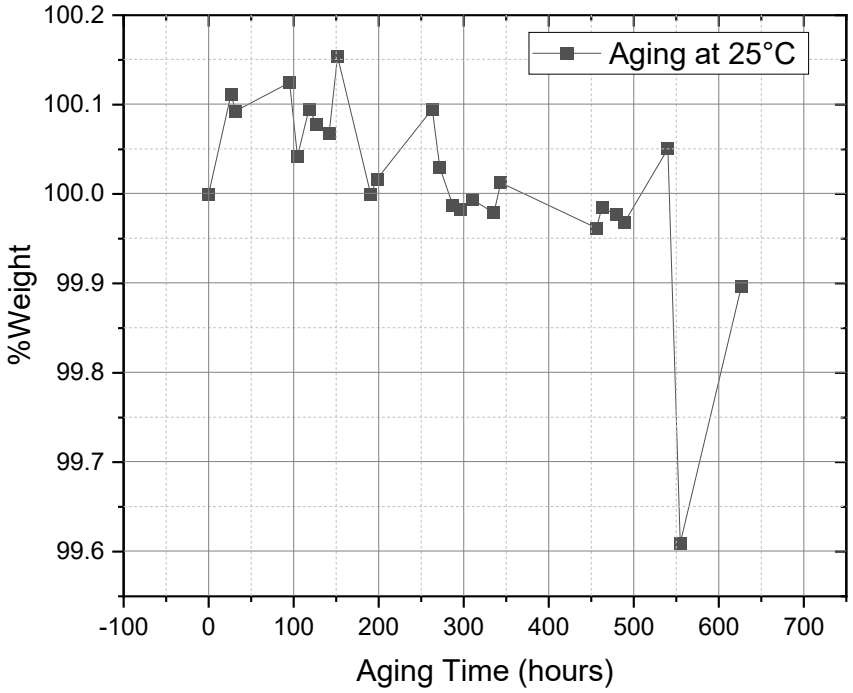

Figure 21: Change in the weight of Megtron6 sample immersed in mineral oil over time at 25°C

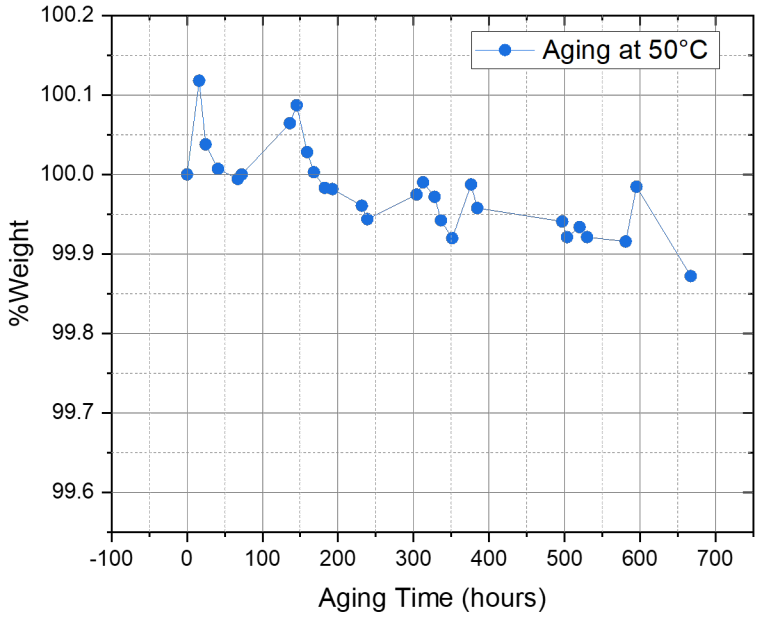

Figure 22: Change in weight of Megtron6 PCB sample immersed in mineral oil at 50°C

2.5. Discussion

In section 2.4.1, Figure 12 to Figure 15 shows the comparison of results for DMA measurements for Megtron6 PCB samples aged in mineral oil and aged in air at four different temperatures. For each plot minimum four samples were tested and averaged. The standard deviation for the results at 25°C, 50°C, 75°C and 105°C temperatures are respectively 7%, 15%, 11% and 9% for oil immersed samples, while 7%, 11%, 5%, and 14% for samples aged in air. Sample to sample variation in terms of copper connections density, slight variation in sample width are potential causes for large error bars.

Predefined torque was applied to minimize the variation in clamping force to attach sample. At the start temperature, isothermal hold was applied to attain thermal equilibrium. This increased the measurement time of DMA to approximately 2.5 hours. The presented data shows the glass transition temperature (T_g) of pre-aging Megtron6 PCB is 155°C, 171°C and 179°C derived respectively from storage modulus, loss modulus and loss tangent. Ehrler studied thermomechanical properties of high frequency PCB base materials and the glass transition temperature (T_g) of pre-aging Megtron 6 found in this study can be corelated to results found from this literature [37]. There is negligible change in the T_g of Megtron6 samples aged in the air and mineral oil compare to pre-aging sample. From literature the glass transition temperature for the Megtron6 is expected to be 185°C using DSC and 210°C using DMA [27].

The complex modulus of the pre-aging sample as shown in Figure 12 is 18 GPa for temperature range -40°C to 90°C. From temperature 90°C to 155°C, complex modulus decreases from 18 GPa to 14.4 GPa linearly. After T_g, the modulus decreases rapidly from 14.4 GPa to ~1 GPa. There is a slight change in the complex modulus for Megron6 PCB samples aged in air at 50°C, 75°C and 105°C compared to pre-aging sample as shown in Figure 17. The data presented in Figure 16 shows negligible change in the complex modulus values of the Megtron6 PCB samples aged in mineral oil. This change is within the error margin and could be attributed to sample to sample variation. The expected flexure modulus for Megtron6 PCB pre-aging sample is 18-19 GPa [28]. Similar studies in

the literature demonstrated decrease of modulus in the FR-4 PCBs after aging in dielectric fluids [10], [32].

Data presented in the Figure 18 to Figure 20, shows the comparison of the CTE for the pre-aging and post-aging samples in air and oil of Megtron6 PCB for temperature range -40°C to 160°C. For each measurement at least four samples were tested to take average value of CTE. The CTE values for the pre-aging sample is 16.3 ppm/°C, which is significantly higher than the silicon chip in electronic packaging stack up. The post-aging samples in air at temperatures 50°C, 75°C and 105°C the CTE value is ~16.7 ppm/°C, the change is negligible compare to pre-aging samples. CTE values for the post-aging samples in mineral oil at temperatures 25°C, 50°C, 75°C and 105°C are in range of 16.5-16.7 ppm/°C as shown in Figure 19. The change in the CTE value is within margin of error bars, can be attributed to sample-to-sample variation in terms of copper density. The expected CTE for Megtron6 from open literature is 14-16 ppm/°C, which agrees to result presented.

Figure 21 and Figure 22 show dielectric fluid absorption into dummy Megtron6 sample at two temperatures, 25°C and 50°C respectively during ~630 hours of aging in the mineral oil. There are three possibilities, weight of the sample will increase, decrease, or remains same. Increase in weight of sample implies absorbing of dielectric fluid into PCB sample while decrease in weight of the PCB sample implies leaching of plasticizers from sample into dielectric fluid. No change in weight of the sample implies either both absorbing and leaching took place at same rate to nullify each other or no absorbing and leaching took place at all. Metrgon6 sample immersed in mineral oil at 25°C, demonstrated that total

weight increased by ~0.1% points from beginning to ~150 hours and then weigh started decreased by 0.2% points from 150 hours to ~650 hours. Sample immersed into mineral oil at 50°C, shows weight of the sample increased by ~0.05 % point from beginning to 150 hours and then weight decreased by 0.15% points from 150 hours to ~650 hours. Data presented indicates initially the absorbance of the dielectric fluid into PCB sample was dominant and after ~150 hours mark, leaching of plasticizers from PCB sample into dielectric fluid was dominant for aging temperatures 25°C and 50°C. This was preliminary experiment with one sample for each temperature which not statistically robust. The focus of this segment of the study is more on defining methodology for similar future investigations to provide better understating of impact of immersion cooling thermo-mechanical properties.

2.6. Conclusion

In summary, the thermo-mechanical properties of low-loss modulus PCB were studied using DMA and TMA. One set of low-loss PCB samples were tested for post aging in air and other set of samples were tested for post aging in mineral oil for 720 hours at four different temperatures, 25°C, 50°C, 75°C and 105°C. Multiple samples were tested to obtain average values and standard deviations. The CTE values for the post aging samples in air practically remain same. The in-plane CTE values for post aging samples in mineral oils at four temperatures change negligibly and remain ~16.5 ppm/°C before glass transition temperature. The complex modulus and glass transition temperature for the post aging samples in the air and mineral oil at four different temperature did not change.

Thus, it is concluded that mineral oil as a dielectric fluid does not have any adverse effects on the thermo-mechanical properties of low-loss Megtron6 PCB. This work can be used to understand the impact of immersion cooling on the thermo-mechanical properties of low-loss PCBs. The dielectric fluid absorbance measurement technique demonstrated in this study may be adopted to gain more understating and insight about impact of immersion cooling dielectric fluid on thermo-mechanical properties of various electronics packaging materials. Furthermore, modulus, CTE and glass transition temperature values measured may be used to perform numerical studies such as Finite Element Analysis (FEA) to assess reliability of immersion cooling under different loading conditions.

CHAPTER 3. IMPACT OF THERMAL AGING AND CYCLING ON RELIABILITY OF THERMAL INTERFACE MATERIALS

3.1. Abstract

Thermal interface materials (TIMs) are critical for the thermal management of electronic packages. Different kinds of TIMs are currently used in the industry to reduce the contact thermal resistance and improve performance of electronic systems. Greases, elastomeric pads, epoxies, and thermally conductive gap fillers are some of the most common types of TIMs. While designing electronic systems, attention is given to characterizing the performance of TIMs and understanding the reliability of the TIM materials under different environmental loading conditions. The most common approach is to measure the thermal performance at the start and end of accelerated testing conditions. As the reliability study of TIMs is not a matured subject, there is a growing interest to understand the mechanical behavior of TIM materials and how they change under various environmental loading conditions. In this paper, four commercially available TIMs are studied under high temperature storage and thermal cycling loading conditions. In the first part of the work, the change in the thermal expansion coefficient of a representative of the group due to high temperature storage test is studied using Thermomechanical Analyzer (TMA). For the second part of the work, an assembly was made to the test the performance of the TIM materials under thermal cycling conditions. Samples with different TIM thickness were prepared and tested in an environmental chamber. An

inspection was performed visually and with the aid of microscope. The results and lessons learnt are presented in this paper.

3.2. Introduction

Thermal Interface Materials (TIMs) are an important component in electronic packages used to minimize the contact resistance between adjacent surfaces. The thermal contact resistance at the interface of various components in Thermoelectric packaging is one of the major issues in thermal design. Without TIMs, the gaps in the mating surface are filled with air resulting in high contact resistance due to the low thermal conductivity of air. [38]Design of an efficient heat dissipation path is paramount to sustaining the life cycle of the electronic system. According to Gwinn et. al., an ideal TIM would have to be deformable to conform to rough surfaces, be safe and durable, has very high conductivity and has low thicknesses. [39] Even though the ideal TIM is yet to be developed, there is a wide range of research to tackle various drawbacks of currently available TIMs and develop TIMs that are close to ideal. For example, Chow et. al. has investigated copper nanowires as high-performance TIMs with high mechanical compliance. [40] Sun et. al. has proposed a novel nanocomposite thermal interface material for high reliability and heat dissipation[41] ; Tong et. al. has proposed Carbon nanotube (CNT) arrays with high conductance [42]; while Li et. al. proposed boron arsenide crystals and isotopically enriched cubic boron phosphide for high conductivity and for use in harsh environment [43], [44]. Though more work needs to be done before they are widely used in the industry, these researches have exciting prospect.

Different types of TIMs are currently used in the industry. The main categories of TIMs include: greases, phase change materials (PCMs), elastomeric pads, thermal conductive gap fillers, and epoxies [38], [45]. Most of the TIMs are made of organic matrix such as silicone and high thermal conductivity fillers such as metals or ceramics [46]. In most applications, thermal greases are most extensively used [46]. However, for applications where the dry out and pump out of greases pose a challenge, thermally conductive gap fillers are used. These materials have the advantage that they are liquid during application, enabling them to fill the interstitial voids. Curing in place, the thermally conductive gap fillers do not pump out and can be used in situations where greases cannot be used. Moreover, the thermally conductive gap fillers do not require high pressure to conform to mating surfaces. Because they are solid at Beginning of Life (BOLife) and End of Life (EOLife), thermally conductive gap fillers are focus of the reliability study presented in this paper.

The performance and characteristics of TIMs at EOLife is compared to BOLife in order to assess reliability. Most common practice is to characterize the thermal performance such as thermal conductivity. Recently, there is a growing focus to understand the mechanical behavior of TIMs and understand how changes in mechanical properties contribute to degradation of thermal performance through time. For example, Subramanian has recently studied mechanical properties of TIMs and the major challenges faces by researchers [47]. However, the reliability testing of TIMs is not matured when compared

to other components such as solders joints, and there is a need for more work in this area [46].

High temperature storage test and temperature cycling are some of the most common test conditions used to perform accelerated stress testing [48]. Previous researchers have studied the performance thermal interface materials under these test conditions [46]. In this paper, the mechanical properties and behavior of four commercially available thermally gap fillers is presented. The paper has two components. First the thermal expansion coefficient of one of the representatives of the group is studied, and the change in property before and after high temperature aging is presented. Second, an assembly is made from aluminum and glass, and thermal interface materials of different thickness were applied. The assembly was placed in an environmental chamber and tested for 1000 cycles. At the end of the test, inspection was performed for crack and delamination on the samples, and the results are presented in this paper.

3.3. Materials and Methods

3.3.1. Sample Preparation

For this study, commercially available thermally conductive gap fillers with an average performance (thermal conductivity between 4 - 6 W/mK) were used. Two different kinds of samples were prepared. Samples prepared for the thermal aging test are described in the next section. Another set of samples were prepared for thermal cycling tests, and their preparation is described in the thermal cycling section below.

3.3.1.1. Thermal Aging

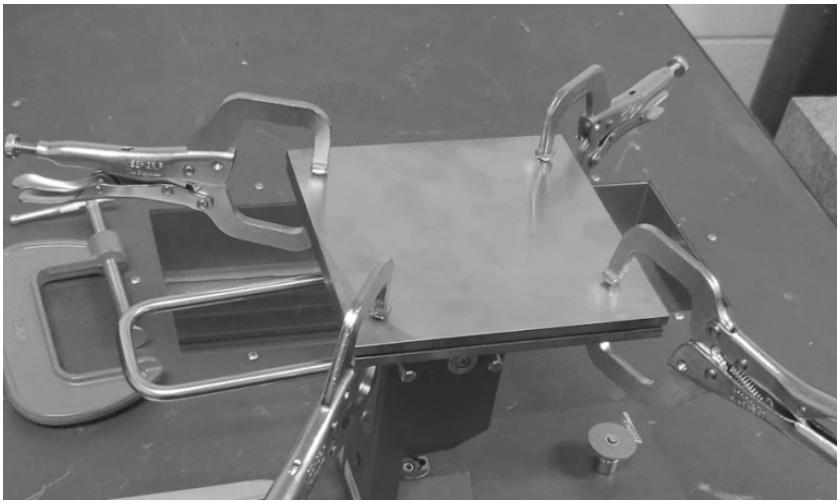

Figure 23: Assembly used to prepare samples. Pressure was applied to obtain uniform thickness.

The assembly shown in Figure 23 above was used to prepare samples for the thermal aging test and TMA analysis. One mm spacers were placed between the plates to ensure uniform thickness of the samples. Clamps were used to apply pressure during curing. The assembly was kept at room temperature (~25 °C) for 24 hours to cure. After curing, the top plate was removed, and samples were cut for TMA measurements. The cured sample and sample used for TMA analysis are shown in Figure 24 and Figure 25 below.

Figure 24: Cured sample obtained after removing the top plate.

Figure 25: Sample on TMA stage before CTE measurement.

3.3.1.2. Thermal Cycling

For the thermal cycling tests, assemblies as those shown in Figure 4 below were made. The TIM material was sandwiched between glass and aluminum plates. The two materials were selected for having very different thermal expansion coefficients. After curing, the assemblies were placed in an environmental chamber, and the thermal cycling test was run to experimentally study the reliability of the TIM materials under thermal cycling. Four types of thermally conductive gap filler materials (TIMs) are used in this study. In this paper, they are referred as TIM A, TIM B, TIM C and TIM D. For each TIM, 8 assemblies were made with thicknesses of 0.3 mm and 1 mm. In total, 32 test assemblies were prepared and placed in environmental chamber for thermal cycling. TIM A has the highest thermal conductivity among the four studied TIMs. The high thermal conductivity was attained with higher amount of thermally conductive gap fillers. As a result, TIM A was the most viscous.

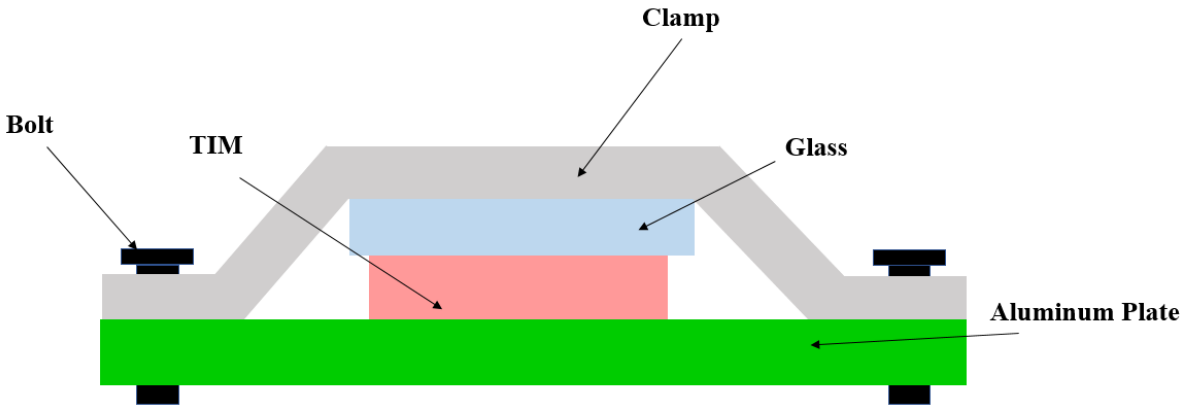

Figure 26: Cross section of the assembly used for thermal cycling experiment.

3.3.2. Experimental Tests

The working principle and description about thermomechanical analysis is given in the section 2.2.1.1. Before experimental measurement, the dimension of samples was measured using a digital caliper that has an uncertainty of 0.02 mm. Typical dimension of samples used for TMA measurement was ~ 7 cm x 7 cm. The TMA probe was used to measure the thickness of samples with precision of 0.05 mm. Temperature range of 25 °C to 150 °C was used for TMA measurements with a ramp rate of 2 °C/min.

For thermal cycling, after curing, samples were placed in an environmental chamber shown in Figure 27. Two different tests were conducted. One set of samples were thermally aged for 720 hrs. JESD22-A103, condition A was used for the tests. The second set were tested under thermal cycling. JESD22-A104D, condition G was used to set the test profile. The chamber was operated for 1000 cycles using the profile given in Figure 28 below. After 1000 cycles were completed, samples were inspected visually for cracks

and delamination. Further analysis was performed using an optical microscope. Results of the inspections are shown in the following section.

Figure 27: Chamber used for thermal cycling test (top). Samples inside the environmental chamber (bottom).

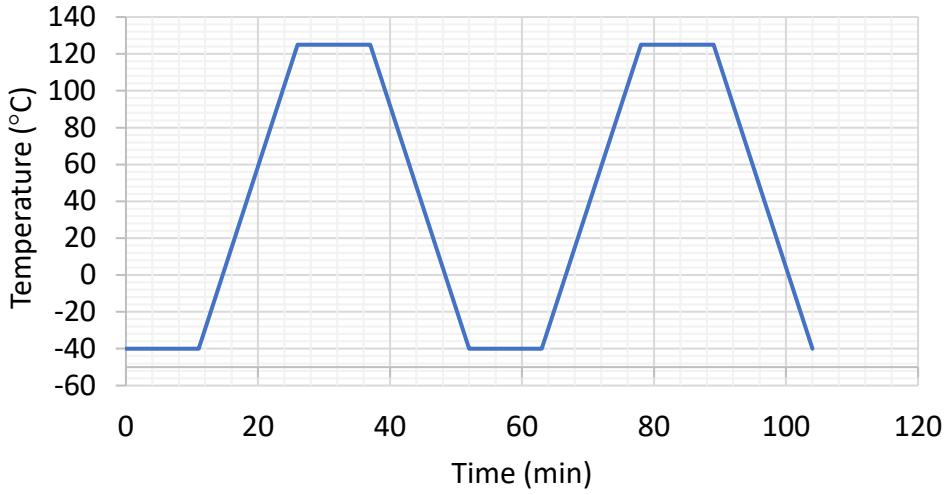

Figure 28: Thermal cycling profile used for this study.

3.4. Results

For TIM D, five samples were tested on TMA for thermal expansion coefficient measurement and the relative length comparison for pre aged and post aged samples are shown in Figure 29.

Figure 30 shows comparison of assembly with TIM A before and after thermal cycling. On left side TIM has defects introduced at time of dispensing, on right side crack is shown to have formed from these defects after thermal cycling. Figure 31 shows that no cracks or delamination was observed for assembly with TIM D.

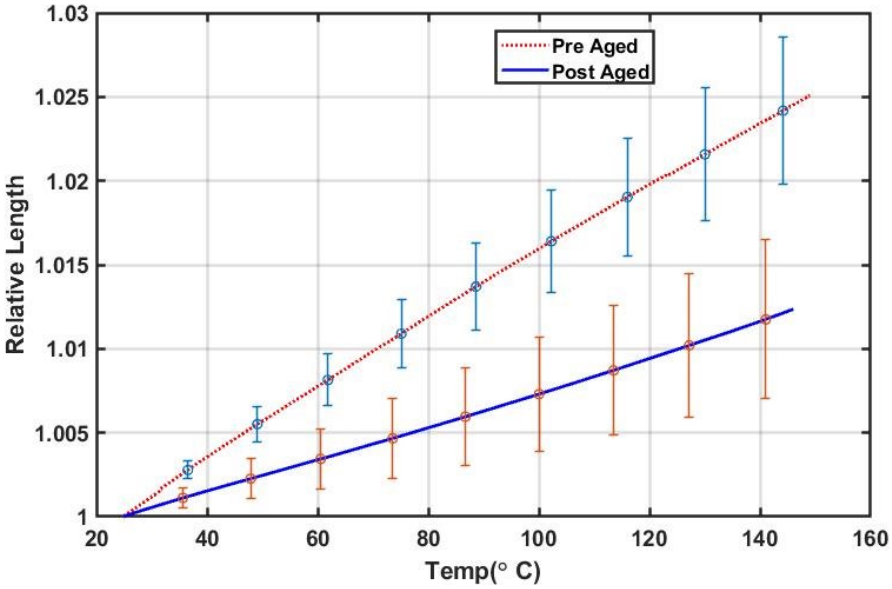

Figure 29: Thermal expansion comparison for before and after thermal aging for TIM D.

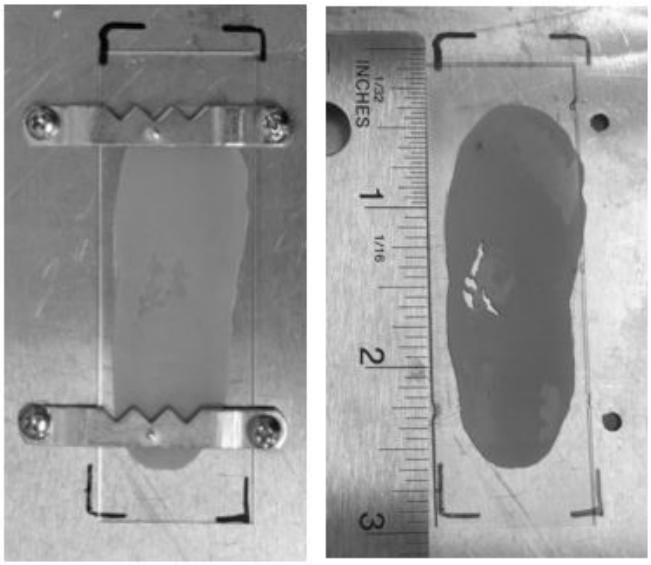

Figure 30: Cracks in TIM A: sample with defect before thermal cycling (left), after thermal cycling (right).

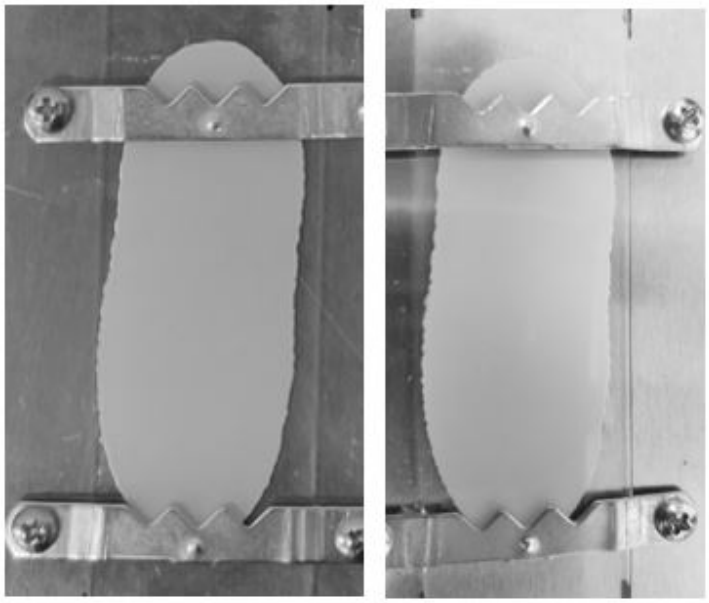

Figure 31: TIM D, before thermal cycling (left) and after thermal cycling (right).

Figure 32 shows comparison before and after thermal cycling for TIM A. The image taken after thermal cycling shows delamination and cracks on the edges of assemblies. Figure 33 and Figure 34 shows delamination and cracks on TIMs after thermal cycling. In Figure 33 and Figure 34, darker portions in the right-side microscopic image are area of TIM with no defects, grey regions show delamination, and brighter regions pointed out with arrows are cracks.

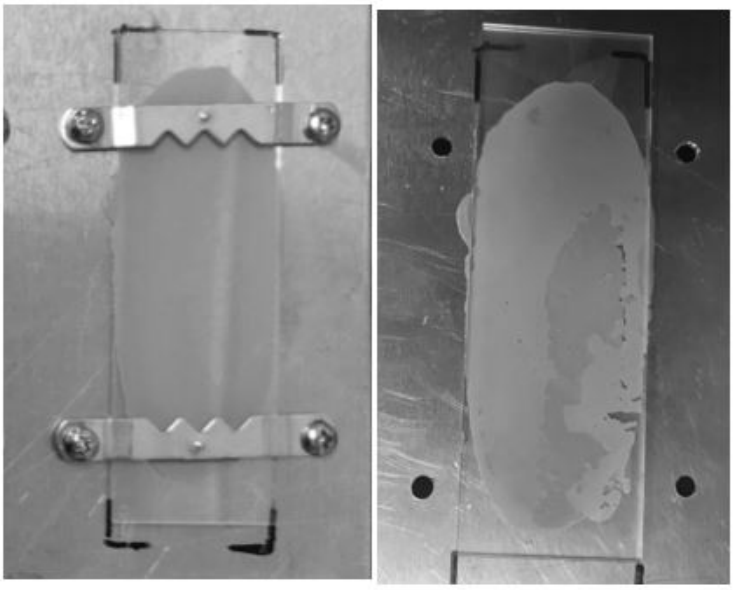

Figure 32: TIM A, before thermal cycling (left) and after thermal cycling (right).

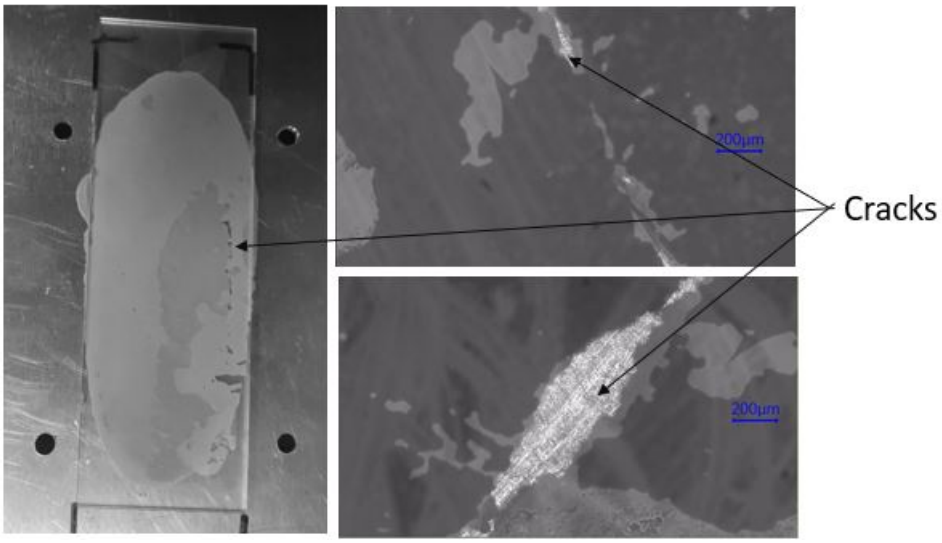

Figure 33: Cracks on TIM after thermal cycling, and microscope images shown in the right.

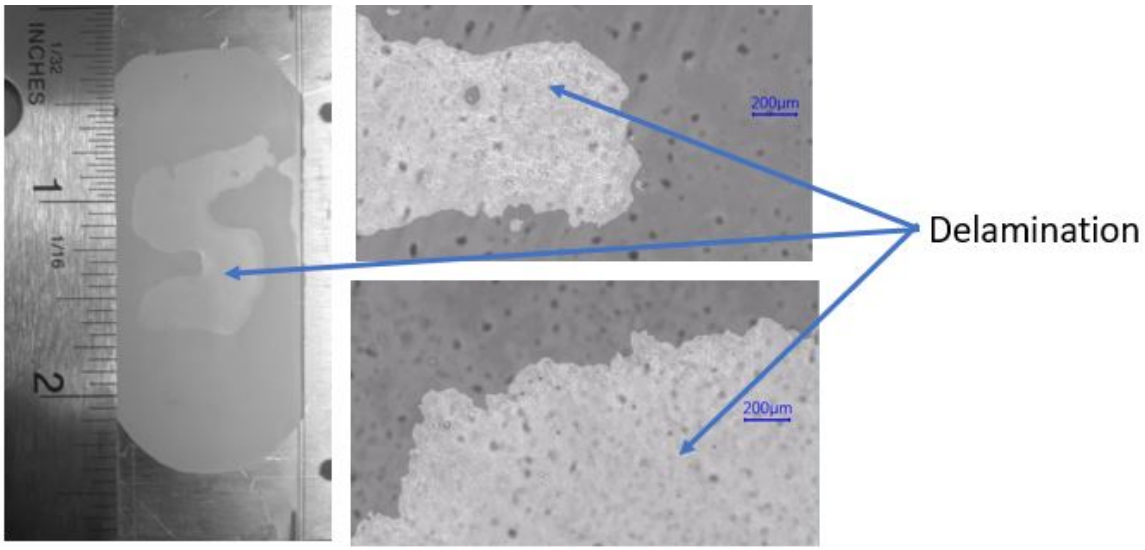

Figure 34: Delamination on TIM after thermal cycling, and microscope images shown in the right.

Table 3: Number of cracks and delamination in TIMs after thermal cycling

	TIM A	TIM B	TIM C	TIM D
	Assembly with 0.3 mm thick TIM			
Delamination	3	3	4	4
Cracks	2	0	0	0
	Assembly with 1 mm thick TIM			
Delamination	0	0	0	1
Cracks	0	0	0	0

3.5. Summary and conclusion

Reliability of thermal interface materials was studied under various environmental loading conditions using four commercially available thermally conductive gap fillers. Samples were prepared and tested in an environmental chamber. One mm thick samples were cured and placed in at oven at 125 °C for 720 hours for high temperature baking test. A second set of samples were prepared into an assembly and placed in an environmental chamber and tested for 1000 thermal cycles.

Figure 29 shows the change in the thermal expansion coefficient of TIM D before and after high temperature aging. Before the high temperature aging, the total expansion for the temperature ranges of 25°C to 145 °C was measured to be approximately 2.5%. This is considerably higher when compared to other components of electronic packaging. After aging, the thermal expansion decreased from approximately 2.5% to 1.2%. This is due to the fact that the base material for the TIM under study is silicone, and mass density increases after thermal aging and reduces the molecular motion resulting in lower CTE in polymers[49]. Relatively high standard deviations observed in Figure 29 are due to ambient noise, sample to sample variation, accuracy and precision during sample measurements.

In the second part of the study, four different kinds of TIMs were studied under thermal cycling. After 1000 thermal cycles, delamination was observed in 15 samples, and major

cracks were observed in 2 samples. Table 3 lists number of cracks and delamination observed for the different TIMs studied. For assemblies with 0.3 mm thick TIMs, 14 out of the 16 assemblies showed delamination while 2 of the 16 assemblies showed cracks. For assemblies with 1 mm thick TIMs only one delamination was observed. These observations show that lower thickness samples are more susceptible to have delamination and/or cracks after thermal cycling. In thermal design, it is desirable to have low bond line thickness for TIMs. The above observations call for caution as the increase in thermal performance might be negated with a decrease in reliability for low thickness TIMs. A rigorous reliability assessment is needed to understand the risk and benefits before finalizing designs.

Another observation made during this study was that TIM A had the most cracks when compared to the other TIMs. As discussed above, the high thermal conductivity of TIM A is achieved by having large amount of filler materials. These materials increased the viscosity and decrease the flowability of the material during application. As shown in Figure 9, defects were introduced to the sample before thermal cycling test was performed. These initial defects served as points for crack initiation and the after-testing image shows that large cracks have formed around these initial defects. These cracks will decrease the performance of the TIM as they will lead to increase in thermal resistance and potential development of hot spots. As such, it is critical to pay special attention when applying the TIM materials to ensure there are no voids or defected introduced to the samples. For this study, glass was used to make the assembly for its low CTE and

transparence that allowed for visual and optical investigation. The wettability of glass might have been a factor and contributed to the relatively larger amount of delamination observed. For future work, this work can be expanded by using materials that are not necessarily transparent and have closer wettability to materials used in electronic packaging. Nondestructive analysis methods such as computerized tomography (CT) scans or confocal scanning acoustic microscopy (CSAM) can be used for future investigations.

CHAPTER 4. IMPACT OF METAL DENSITIES AND CRITICAL CRACK/FLAW LOCATIONS ON CHIP PACKAGE INTERACTION RELIABILITY

4.1. Abstract

Following silicone node technology and geometric shrinkage of transistors, the least geometric feature sizes in back end of line (BEOL) structure is getting smaller. First level interconnect pitch is decreasing and with that copper pillar technology is increasingly replacing solder bump technology. As the geometric features gets smaller with advancing silicone technology nodes, chip package interaction (CPI) in combination with the ultra-low-K (dielectric constant) material, and copper pillar first-level interconnects presents novel challenges to reliability of electronics devices. In this study, various approaches to evaluate fracture mechanics parameters computationally have been investigated and compared for fracture or delamination failure in BEOL due to CPI. This study also investigates effect of the metal densities, crack/flaw orientation, crack locations within BEOL structure stack on the first level reliability due to CPI.

4.2. Introduction

As the number of transistor density increases due to scaling of the integrated circuits to improve the performance of the microelectronic devices, the complexity of BEOL stacks has presented many reliability challenges [6]. To improve the functionality and performance of microelectronic device as the BEOL become more complex, semiconductor industries have replaced Al/SiO2 with copper and ELK/ULK material to

avoid signal interference [50]. The need to adapt many new materials to accommodate modern ultra-large-scale integration (ULSI) as the dimensions of the device shrink and the number of metal length and interconnection level increases, poses unique reliability challenges in Chip to Package interface[50]. In the lifetime of the device it endures thermal stress during processing, packing and operation which can induce local stress resulting in crack initiation and propagation.

Chip Package interaction (CPI) is the stresses in the semiconductor device due to the package. The cause of stresses are due to the CTE mismatch between the silicon and different materials in the package. The induced thermo-mechanical stresses during thermal excursion compromise the structural integrity in the BEOL stacks[51] [52] [53] [54] [55]. The evolution of the mechanical stresses during flip-chip assembly in global and local regions are due to the fabrication processes that consists of many steps with different temperatures. For instance, during the deposition process in the BEOL, low-K/ULK dielectric layer is deposited at stress free temperature of 400°C [56]. Similarly, the stress-free temperature for copper, oxide and nitride are 200°C, 400°C and 400°C respectively. Moreover, temperature associated with bump formation, substrate attachment, bump reflow and underfilling are 220°C, 25°C, 220°C and 170°C respectively. Hence the intrinsic stresses are developed during these heating and cooling operations due to the CTEs mismatch [56].

For the modern semiconductor devices with BEOL consisting of many layers of interconnects, vias and dielectric layers from local to global interconnects, BEOL layers

near the silicon has dense wiring and contacts. The density and complexity of wiring gradually decreases as the BEOL layers connects to the package [57]. At the local layers, the need of the ULK-dielectric material is essential to improve signal propagation and prevent leakage. Any ULK-dielectric candidate must address key material issues such as permittivity, process compatibility and reliability [58]. At the intermediate layer low-K dielectric material is used as the density of the wiring is reduced and at the global layer the SiO_2 is used as the dielectric. The various material used as the dielectric in different layers of BEOL with different material properties effects the reliability as the ULK material has significantly lower modulus than the SiO_2. The need to use the porous material as instralevel dielectric to reduce the dielectric constant is the main cause of reduced modulus of the structure [59].

Due to the complexity and the fine features in the BEOL stacks, multilevel sub-modeling is normally implemented for mechanical reliability study of BEoL structure under CPI loadings. Sub-modeling is finite element technique to obtain more accurate results in the region of interest in the model. The model discretization in the region of interest might be too coarse to obtain desired results with accuracy while having smaller mesh discretization for entire model might be time consuming and requires higher computational resources [60]. In such situations, the sub-modeling approach could be leveraged to generate finely meshed model for region of interest. Similar approach could be used multiple times for analysis, based on the amount of detail present in the model known as multi-level sub-modeling. BEOL in the package contains enormous geometrical

details. Additionally, considering the geometry feature size vary approximately by six orders of magnitude for major package dimensions, multilevel sub-modeling approach has been adopted for optimal use of computational resources.

Fracture or interfacial delamination is one of the most dominant failure mechanisms within BEOL structure under CPI loading entails the need to evaluate fracture parameters. Most common method used to computationally calculate the fracture mechanics parameters such as energy release rate is modified virtual crack closure technique(MVCCT) also known as virtual crack closure technique(VCCT) and J-integral for electronics reliability under CPI [61] [62] [63] [64]. The MVCCT was implemented with specialized codes in conjunction with general purpose finite element codes as it was not implemented in the popular commercial finite element codes such as MSC Nastran, ABAQUS, ANSYS, ASKA until 2004 [1]. To implement MVCCT in conjunction with the general-purpose finite element code, the reaction force, and relative displacement obtained for the nodes on the crack front and on crack surface respectively together with the crack opening area to evaluate ERR [65]. The formulations to evaluate ERR depends on the type of the element used for finite element analysis [65]. As of today, there are many commercial finite element codes such as ANSYS and ABAQUS (most frequently used) with native techniques to evaluate fracture/delamination parameters[66] [67].

In open literature, impact of various package parameters has been studied on the BEOL structure reliability under CPI loading. V. Cherman et. al studied if CTE of the substrate influences the chip package interaction in a flip chip-chip scale package (FCCSP) due to

mass reflow and thermomechanical compression bonding which involves extreme temperature conditions. It was shown that by lowering CTE of substrates by an insignificant amount, low in-plane stresses are induced on the chip [68]. Kashi Vishwanath Machani et. al worked on the complexity involved in thermomechanical problems of CPI risks and developing a new finite element approach called cohesive zone material (CZM) to predict BEOL failure in a FCCSP package during chip attachment or mass reflow processes. This work implements CZM effectively without introducing crack and it is quantitatively validated by the experimental data [69]. Wang Wei et. al studied a polyimide which is used to give structural support to package and its impact on the chip package interaction for flip chip copper pillar packages. It is known that BEOL failure occurs mainly due to passivation crack and low-K, extremely low-K (ELK) delamination and the effect of polyimide in these failure modes from fracture mechanics perspective [70]. Zhuo-Jie Wu et. al worked on the CPI reliability challenges in large die applications with respect to the kerf size. The BEOL reliability is evaluated by hammer test of 15 cycles of reflow and it was shown that narrow kerfs of 100um width were more susceptible for dicing induced damage while wide kerfs of 300um width are prone to delamination in thermal cycle stress due to increased energy release rate in the cracks [71]. Hak Baick et. al worked on the thermomechanical reliability issues by CPI on low K/ ULK when epoxy molding compounds (EMC) are used in the package. Numerical simulations and reliability tests were done to show that EMC with a higher storage modulus provides better reliability and induces less stresses at the bump and under bump and concluded that BEOL interconnect reliability depends on parameters like tensile and compressive interfacial

stresses [72]. Zhuo-Jie Wu et. al worked on the kerf size and substrate effect on the CPI reliability in large dies with five different configurations. Finite element method was used with different stress configurations to analyze the failure mechanisms and solutions were proposed to resolve the failures. The narrow kerfs passed the test without failures while wide kerfs failed due to the increased ERR because of crack length extension [73]. Number of copper connections in the given metal layer and number of vias vary locally if the focus is on the small region of BEOL structure with multilevel sub-modeling. While there have been various studies to show the impact of different aspects of the package on CPI reliability, it is critical to understand impact of variations in BEOL structures on interfacial delamination.

In this study, for the first part, three different techniques to computationally evaluate fracture parameters namely specialized VCCT, ANSYS native VCCT and ANSYS native J-integral have been studied and compared for first level reliability under CPI within BEOL structure. Second part of this study focuses on the impact of varying metal density within the BEOL structure, crack orientation, and crack location on the ERR which is driving force for the delamination.

4.3. Methods

4.3.1. Numerical fracture analysis methods

4.3.1.1. Virtual crack closure technique

a. The specialized virtual crack closure techniques

The specialized VCCT technique is used in conjunction with general purpose finite element analysis. For the existing crack/flaw in the geometry and the reaction forces, and relative displacement are obtained after finite element analysis. For eight node brick element, the reaction force directional components, X, Y and Z is obtained in three directions, i.e. x, y and z for the node on the crack front shown in Figure 35 [65]. The relative displacement, i.e. w, u and v are obtained for the pair of the nodes just before the crack front as shown in Figure 35. The energy release rate for mode I, II and III is calculated using equations (1), (2) and (3) respectively [65]. The reaction forces and the relative displacement is obtained manually by user written specialized codes to evaluate energy release rate.

$$G_I = -\frac{1}{2\Delta A} Z_{Li}(w_{Ll} - w_{Ll*}) \quad (1)$$

$$G_I = -\frac{1}{2\Delta A} X_{Li}(u_{Ll} - u_{Ll*}) \quad (2)$$

$$G_I = -\frac{1}{2\Delta A} Y_{Li}(v_{Ll} - v_{Ll*}) \quad (3)$$

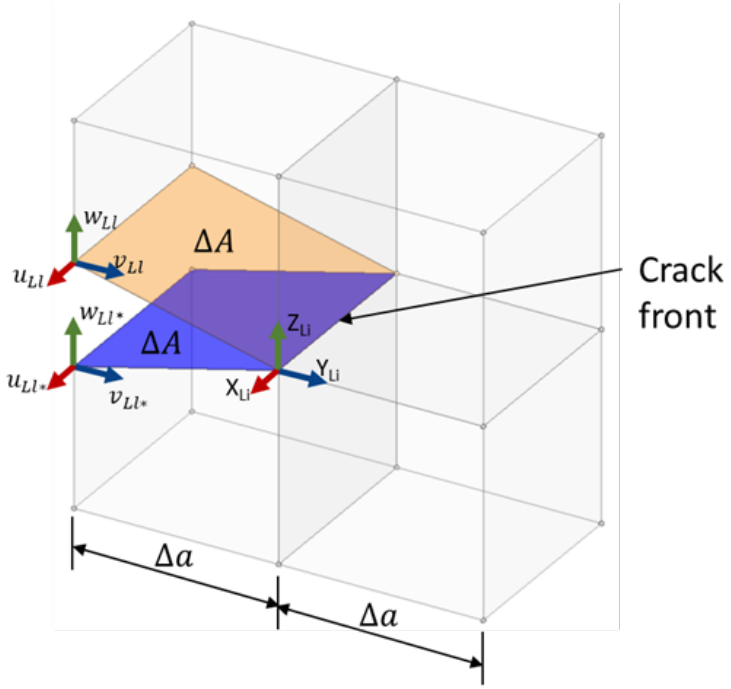

Figure 35: Virtual crack closure technique for four node brick elements

b. ANSYS native virtual crack closure techniques

ANSYS has the in-built feature using VCCT to evaluate energy release rate. The approach is similar where they obtain the reaction forces Rx, Ry and Rz [66]. The relative displacement between the top and bottom nodes of the crack face is calculated as shown in Figure 36. Finally, equation (4), (5) and (6) are utilized to calculate mode I, II and III energy release rates [66]. There is no requirement for user written specialized codes.

$$G_I = -\frac{1}{2\Delta A} R_Y \Delta v \tag{4}$$

$$G_I = -\frac{1}{2\Delta A} R_X \Delta u \tag{5}$$

$$G_I = -\frac{1}{2\Delta A} R_Z \Delta w \tag{6}$$

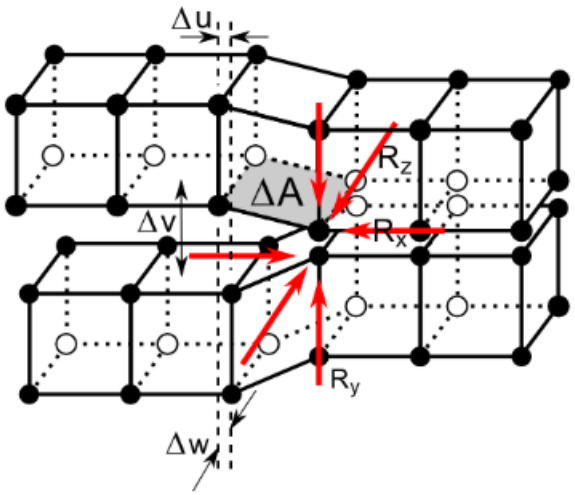

Figure 36: ANSYS native VCCT schematic for 3D geometry [66]

4.3.1.2. ANSYS native J-Integral technique

ANSYS has the in-built native feature to evaluate ERR using J-integral. J-integral evaluation is based on the domain integral for two-dimensional and three-dimensional analysis [66]. To use this approach there is no requirement of user written specialized codes.

4.3.2. Model dimensions

4.3.2.1. Double cantilever beam compact specimen

The notched compact tensile specimen described in Section A4 of the E 3999 ASTM standard is shown in Figure 37. For the ideal test specimen all the other dimensions are dictated once the horizontal length (W) of the specimen from the center of the hole to the end is set. The crack length is measured from the center of the hole to the tip of the crack. All the other dimensions of the test specimen are set as shown in Figure 37. The value for dimension W is 40 mm and crack length, a is 18 mm for the purpose of this study.

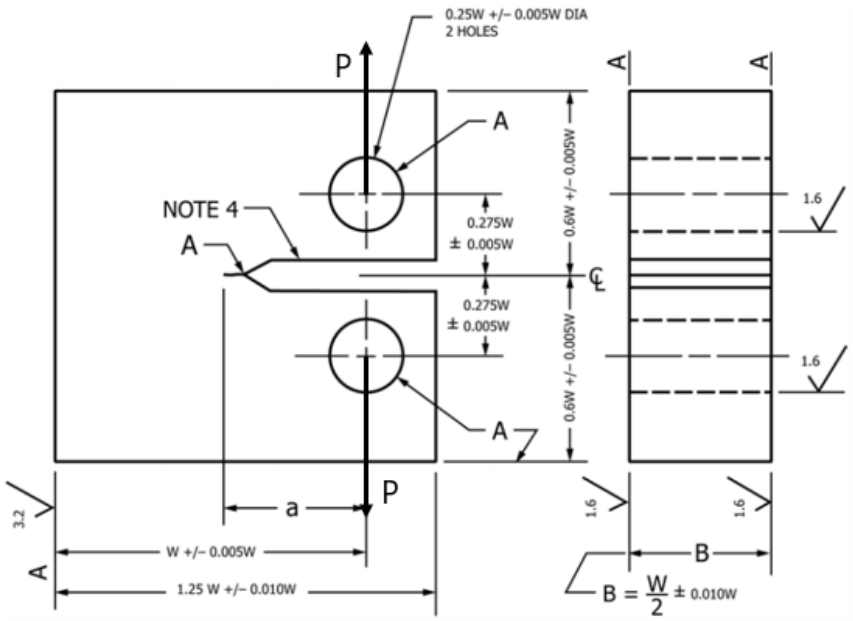

Figure 37: Compact tensile C(T) Specimen- Standard Proportion

4.3.2.2. Flip-chip ball grid array package

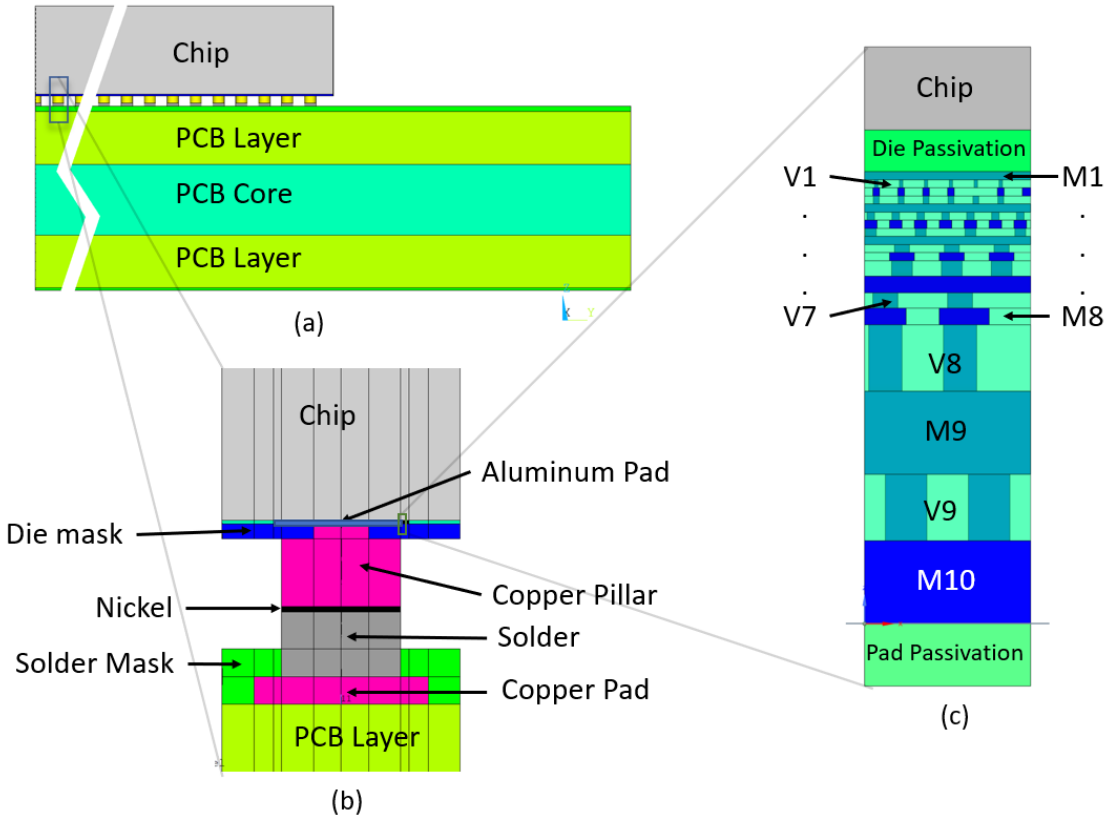

Figure 38: Material component in (a) Package level, (b) Bump level, (c) Wafer Level

The size of the chip and PCB is 6.5 mm x 6.5 mm and 13 mm x 13 mm respectively. The dimensions are listed in Table 4 is for 25 x 25 BGA package shown in Figure 38. Table 5 lists the dimensions of metal and via layer in the BEOL of the Wafer level.

Table 4: Dimensions of the component shown in Figure 38, (a) and (b)[74].

Component	Dimension (um)
Chip thickness	500
Pitch	130
PCB Layer thickness	300
PCB Core thickness	400
Aluminum Pad Diameter	74
Die mask thickness	10
Aluminum Pad thickness	3
Pillar diameter	65
Copper thickness	37
Nickel thickness	3
Solder thickness	35
Solder Mask thickness	30
Copper Pad diameter	95
Copper pad thickness	15

Table 5: Layer thickness at wafer level as shown in Figure 38, (c).

Metal Layer	Normalized Metal layer thickness	Via Layer	Normalized Via thickness
M1	x	V1	0.95x
M2	x	V2	0.95x
M3	x	V3	0.95x
M4	x	V4	0.95x
M5	x	V5	0.95x
M6	x	V6	1.85x
M7	2x	V7	1.85x
M8	2x	V8	8x
M9	10x	V9	8x
M10	10x		

4.3.3. Boundary and loading conditions

Quarter symmetric model is used for optimum use of computational resources, and boundary conditions are shown in Figure 39 for package level model. For the subsequent levels of models in the multi-level sub-modeling approach, the displacements calculated at cut boundary of the coarse model will be used as boundary conditions for sub-model. Body force in terms of temperature change from ~230°C to ~25°C is applied as loading based on reflow process for first level interconnect.

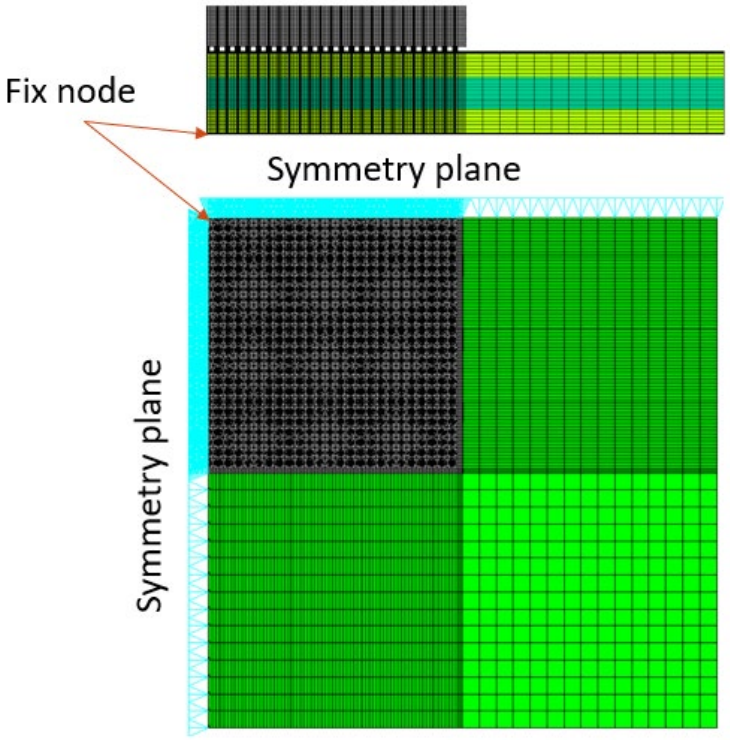

Figure 39: Boundary conditions at package level

4.3.4. Multilevel Sub-modeling

The minimum geometry feature size in the BEOL structure is approximately ~10^{-9} m and at the package level the typical geometry feature size is ~10^{-3} m. There is difference of six orders of magnitude in the geometry feature size, which presents enormous amount of geometry and model details. To overcome such challenges and utilize optimum computational resources, multi-level sub-modeling approach is implemented for this study. The model has four levels namely, package level, bump level, BEOL level and finally the local BEOL level shown in Figure 40. Package level model contains details about overall package, size of the die, total number of pillars and substrate. The bump level model then focused on the one pillar with more details compare to package level model; corner pillar is chosen based on the maximum first principal stress. The BEOL level model focuses on the region of the bump/pillar, comprising BEOL stack structure, partial die, and pillar pad. BEOL structure, is model with combining via and metal layers as single block with effective material property based on the volumetric average of copper connections and respective dielectric material in given layer. There are ten such layers and one such layer is horizontally divided into three regions based on the copper connection density, region A, region B and region C as shown in Figure 40, (c). The region A has the highest copper connection density, region B is with lower copper connections density and region C has no copper connections present. The wafer level model is detailed model with the copper connections structure in the BEOL structure.

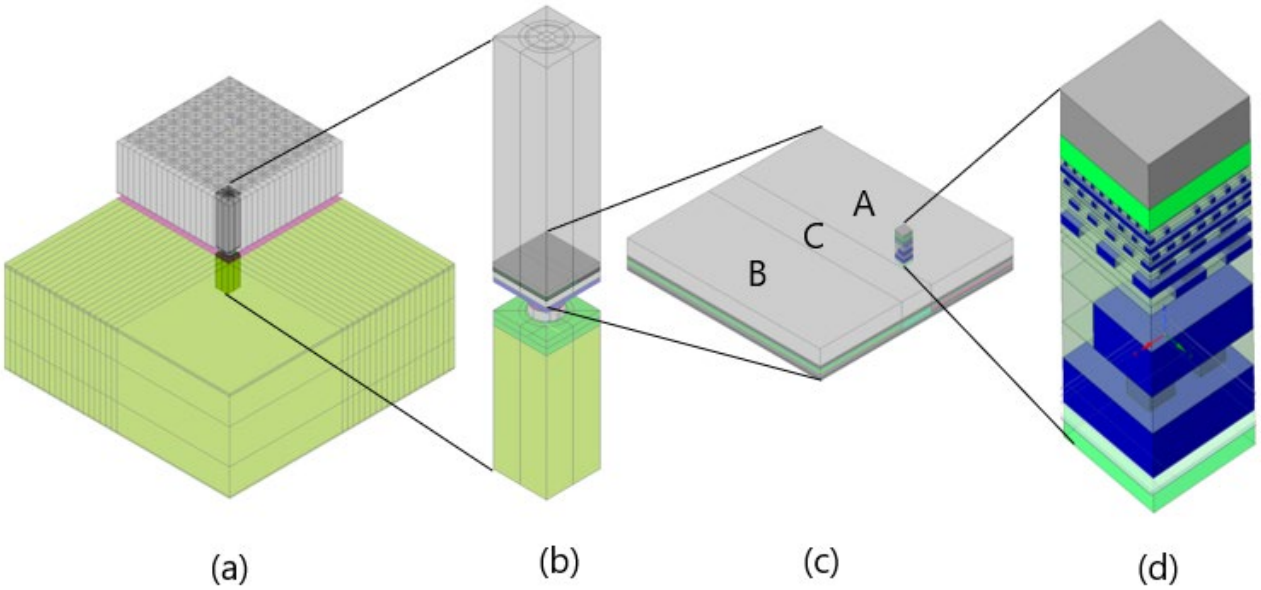

Figure 40: Model with multi-level sub-modeling approach, (a) Package level model, (b) Bump level model, (c) BEOL level model, (d) Wafer level model

4.3.5. Thermo-mechanical material properties

Table 6: Material properties for model [74] [55] [75]

Materials	CTE (ppm/°C)	Youngs Modulus (Gpa)	Poisson's ratio
Copper	17	122	0.34
Aluminum	25	70	0.33
Silicon Die/ Chip	2.6	130	0.278
Die mask	70	1.8	0.3
Pad Passivation	0.5	70000	0.34
Solder mask	50/60(Tg=110°C)	3.2/0.11	0.32
PCB layer	16/160(Tg=170°C)	7.5/0.75	0.32
PCB core	7	26.9	0.3
Low- dielectric (LK)	8	17000	0.3
Ultra-low-k dielectric (ULK)	18	4000	0.3
Nickle	13.1	207	0.31
Die passivation (Teos)	1.4	72	0.2
Solder ball	19	88.53-0.142*T	0.36

Table 7: ANAND's constants for SAC305 [75]

Anand Constants	SAC305
S_o (MPa)	18.07
Q/R (1/K)	9096
A (1/s)	3484
E	4.0
M	0.20
h_o (MPa)	144,000
S (MPa)	26.4
n	0.01
a	1.90

4.3.6. Mesh sensitivity analysis

Mesh sensitivity analysis is presented below in Figure 41. The Maximum ERR values for horizontal 2D crack of size 0.2 um length and 0.2 um width is plotted for different meshes. The crack size, location and other parameters are constant except mesh. ANSYS native J-integral method is implemented to evaluate ERR. Eight node brick element and four node

tetra-hederal elements are used for FEA analysis. The mesh with 3.55 million elements is used for analysis as the change in the maximum ERR is 1.5 % going from mesh with elements 3.55 million to number 3.9 million.

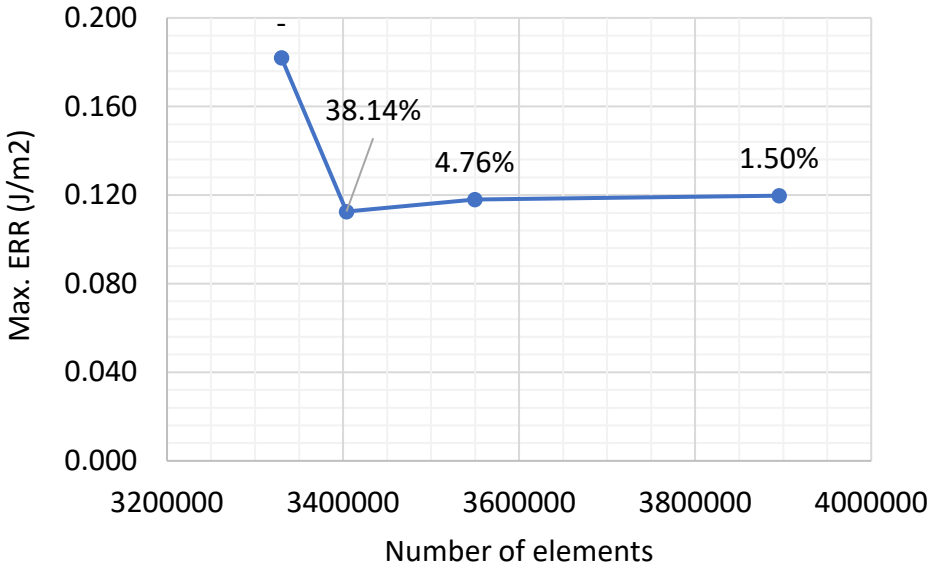

Figure 41: Mesh sensitivity analysis.

4.4. Results

4.4.1. Comparison of the various fracture/delamination parameter evaluation

Three numerical fracture parameters evaluation techniques namely, specialized VCCT, ANSYS native VCCT, and ANSYS native J-integral have been studied and compared for BEOL stack structure delamination under CPI loading with analytical solution. The double cantilever beam compact specimen as per section A4 of the E 3999 ASTM standard have been used for the study with dimension details shown in section 4.3.2.1. The load of 500

N is applied for all the cases to cause mode I fracture. The material of the specimen is structural steel. The analytical solution for this standard specimen is given by equation (7) and (8).

$$K_I = f\left(\frac{a}{W}\right)\frac{P}{B\sqrt{W}} \ , f\left(\frac{a}{W}\right) = \frac{2+\frac{a}{W}}{\left(1-\frac{a}{W}\right)^{\frac{3}{2}}}\,[0.866 + 4.64\,(\frac{a}{W}) - 13.32\,(\frac{a}{W})^2 + 14.72\,(\frac{a}{W})^3 - 5.60\,(\frac{a}{W})^4] \tag{7}$$

$$G_I = -\frac{{K_I}^{2'}}{E'} \ , E' = E \ for \ plane \ stress, \qquad E' = \frac{E}{1-v^2} \ \ for \ plane \ strain \tag{8}$$

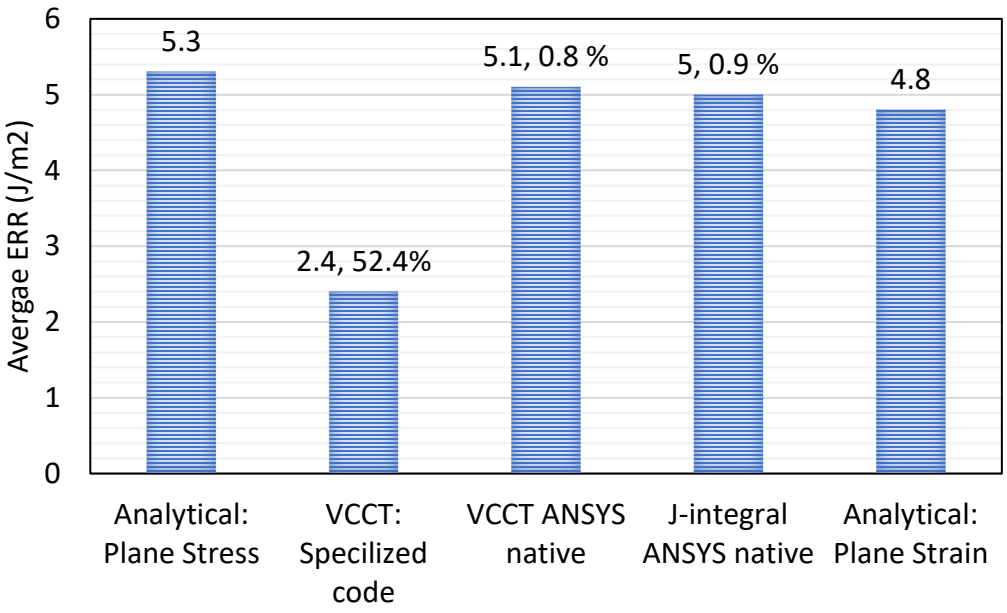

Figure 42: Double cantilever beam compact specimen ERR comparison

Figure 42 shows the comparison of the ERR evaluated using three different numerical methods with analytical solution for double cantilever beam compact specimen.

4.4.2. Impact of crack location on the flip-chip BGA package CPI reliability

For the package level model, the corner bump was chosen based on the maximum von-mises stress for the bump level model. The bump level model results are not presented as they are used as cut-boundary conditions for the subsequent level of model. The Horizontal 2D crack of size, ~0.2 um length and ~0.2 um width is introduced in BEOL stack structure. Figure 43 shows the 2D crack on top of metal layer M7. Vertical position of the crack is at the interface of metal layer and via layers. The crack locations are at interfaces M10-V9, M9-V8, M8-V9…M2-V1 and on the top of M1 layer. The horizontal location of

the crack was determined such that metal, and dielectric will form bottom and top crack surface respectively. ANSYS native J-integral is used to evaluate ERR under the micro bump reflow temperature cycle loading conditions. Figure 44 shows maximum ERR values obtained for introducing crack on the top of different metal layers in BEOL structure.

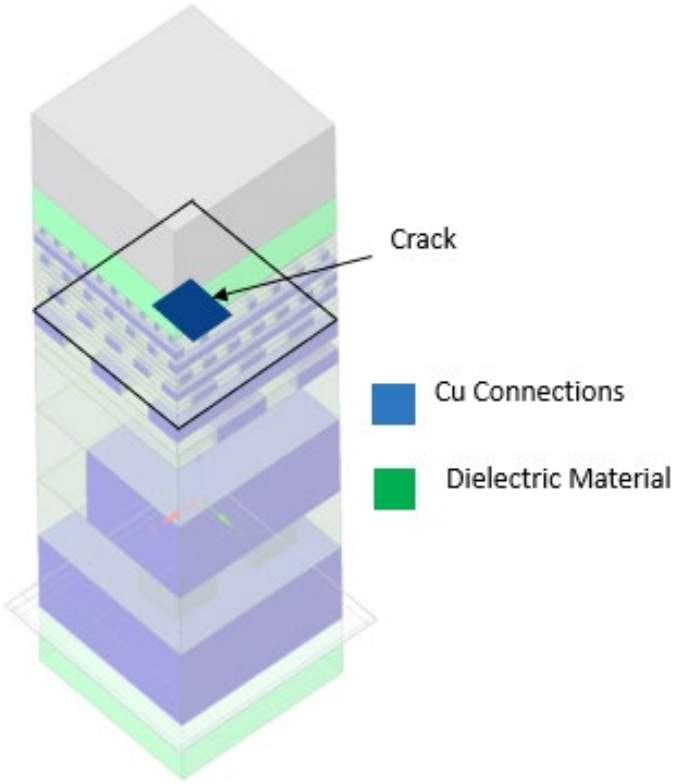

Figure 43: Wafer level structure with 2D crack on t top of M7 metal layer.

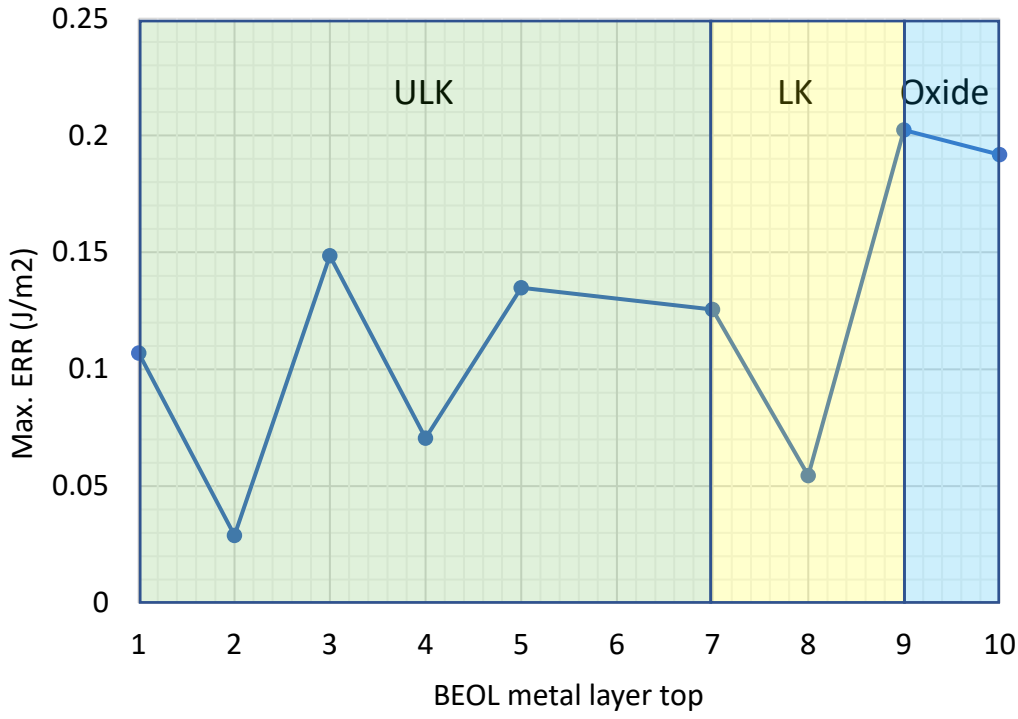

Figure 44: Maximum ERR values crack on different metal layers within BEOL structure

4.4.3. Impact of wiring density on the flip-chip BGA package CPI reliability

The impact of wiring density has been studied both at BEOL level model and at wafer level model. First the impact of wiring density is studied by varying the structure within the BEOL stack by changing variables like the copper connections in metal layers, presence of via between two metal layers, and presence of copper connections in the global BEOL metal layers M9 and M10. Five different variations of the structures have been studied based on the above parameters as shown in Figure 45. The structure 1 has the copper connections present in all the metal layers and via present in all the via layers. Structure

2 has no copper connections in the metal layers but has the via presence in the via layers. Structure 3 has the copper connections in all the metal layer but no vias in the via layers. Structure 4 has no copper connections as well as no vias in the via layers. Structure 5 has the no copper connections for the global metal layers, M9-M10 and no vias for via layers V8-V9. 2D square crack of ~0.2 um was introduced on top of metal layer M7 for all the cases. The maximum ERR values for each structure are tabulated in the Table 8.

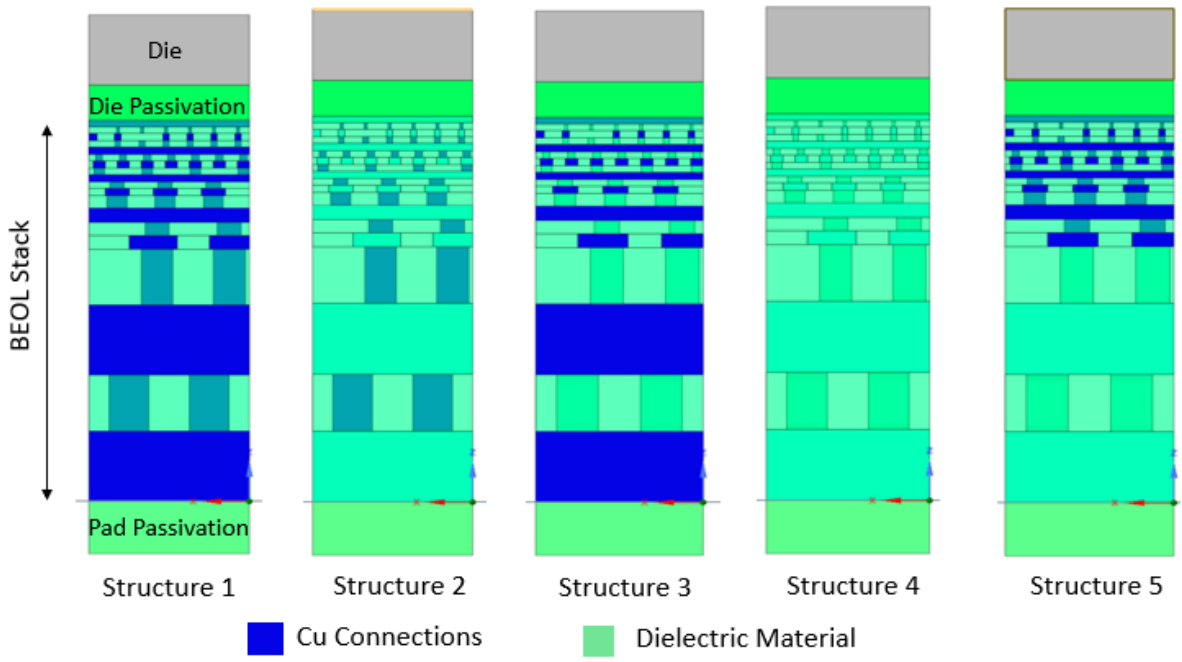

Figure 45: Wafer level structures based on presence of Cu connections and via in BEOL structure

Table 8: Maximum ERR values for the different wafer level structures

	Structure 1	Structure 2	Structure 3	Structure 4	Structure 5
ERR. Max (J/m^2) * 10^{-2}	12.6	4.3	8.5	3.4	9.6

The impact of wiring density is also studied by changing the gap size at wafer level model and changing the average metal density in all the metal layers in region A. Before that maximum ERR was calculated for the different location, denoted by 1 to 9, of the wafer level model with respect to BEOL level model as shown in the Figure 46. For each location, 1 to 9, 2D crack was inserted on the top of metal layer M3. The maximum ERR values are for all nine locations are shown in Figure 47.

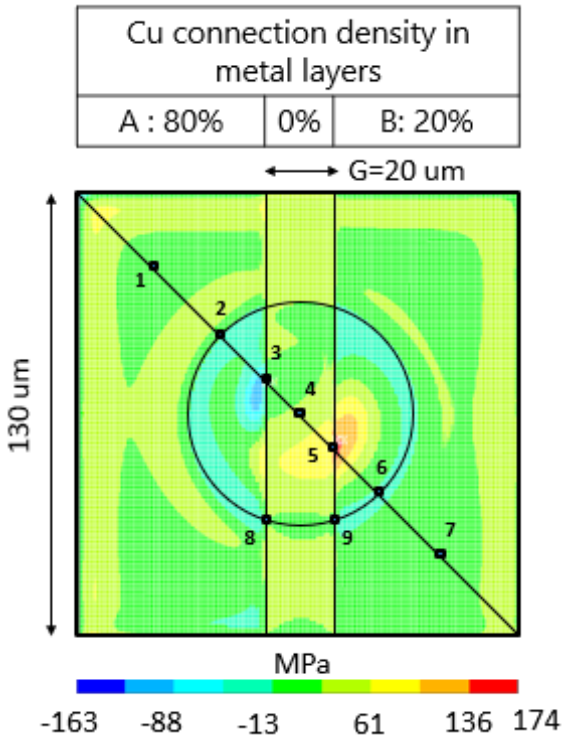

Figure 46: BEOL level model first principal stress on M3 top and wafer level model locations

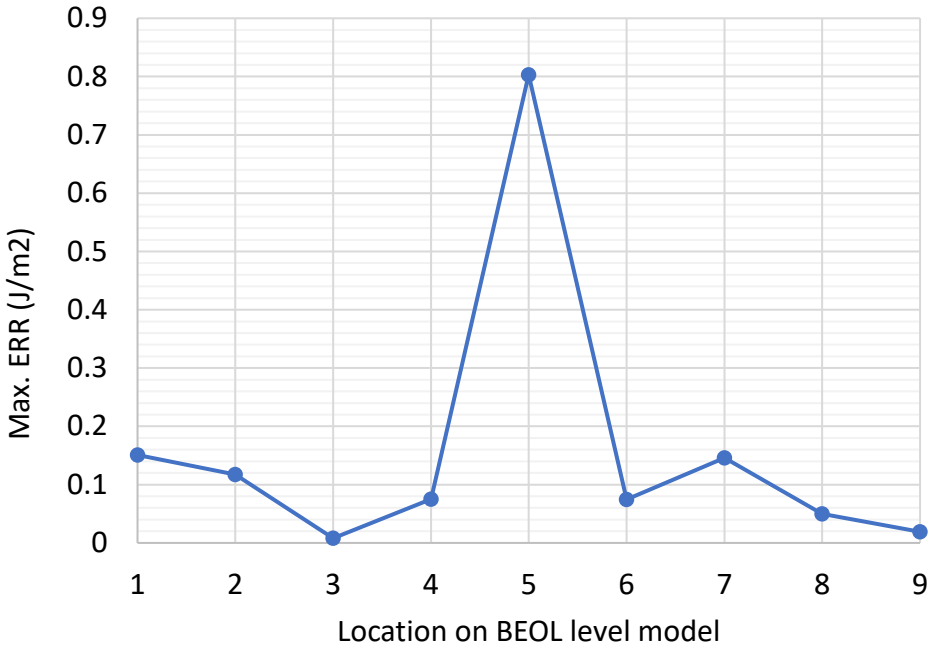

Figure 47: Maximum ERR values for locations 1 to 9 on BEOL level model

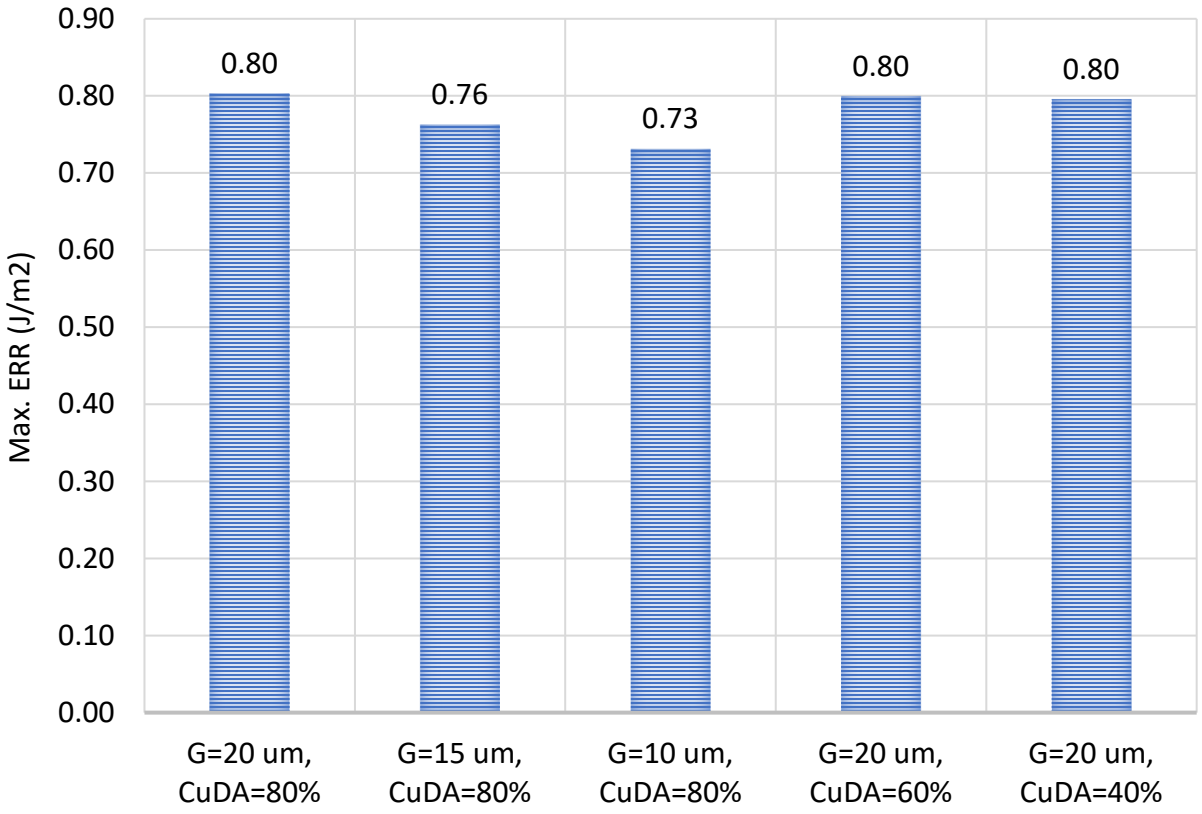

Figure 48: Impact of gap width and region A metal density at BEOL level model on ERR

At BEOL level model, the impact of gap width, a region with no metal density in metal layers and average metal density, region A was studies and results are presented in the Figure 48.

4.5. Discussion

4.5.1. Comparison of the various fracture/delamination parameter evaluation

Three numerical techniques been compared for the fracture/delamination study namely VCCT specialized code, VCCT ANSYS native, J-integral ANSYS native. The results for the DCB specimen are shown using each of numerical technique and compared with analytical solution. The ERR value using VCCT specialized code are off by more than 50 % from analytical solution as shown in Figure 42. The major difficulties with VCCT approach are to obtain correct reaction force for the nodes on the crack front and relative displacement of the nodes on the crack surfaces. Moreover, user need to use specialized code in addition to general purpose finite element analysis. There is always potential risk of human error with this approach. The ERR values using other two approaches, VCCT ANSYS native and J-integral ANSYS native, is in close agreement with analytical solution. These approaches do not involve any manual specialized codes for post processing to evaluate ERR for fracture/delamination. Further to compare the VCCT ANSYS native to J-integral ANSYS native, the J-integral requires finer mesh near the crack front compare to VCCT native. However, J-integral allows user to use hexahedral (brick element) mesh as well as tetrahedral element mesh compare to VCCT where user need to mesh model with hexahedral elements only [66]. The unstructured mesh method feature within ANSYS which could be used with tetrahedral mesh entails accurate ERR values using J-integral approach.

4.5.2. Impact of crack location and orientation on the flip-chip BGA package CPI

Horizontal 2D crack geometry is introduced on top of each metal layers within BEOL structure to study the impact of crack location on the ERR. Results are presented in Figure 44. The maximum value for the ERR was observed for the crack on top of metal layer M9, at the interface of the oxide and low-k dielectric materials. The critical ERR values, which is material property, for these materials are more than ~4 J/m^2 [76]. Critical ERR value for ultra-low-k(ULK) dielectric material is ~2 J/m^2 [59]. Considering the low critical ERR values for ULK materials, crack in the metal layers M1-M6 was studied and the crack location on the top of metal layer M3 was considered critical despite lower ERR than crack on the top of metal layer M9.

4.5.3. Impact of wiring density on the flip-chip BGA package CPI reliability

Impact of the wiring density was studied at wafer level for different BEOL structures based on presence of copper connection and number of via in the structure under study. Five different variations of wafer level model structures have been studied and results are presented in the Table 8. The maximum ERR value was observer for the structure 1 compare to all the structures. The structure 1 has the maximum copper connections in all metal layers as well as maximum number of vias present compare to other structure. With multi-level sub-modeling approach, based on these results, wafer level model should be selected with maximum number of copper connections present in all metal layers with

maximum vias to design for worst case scenario in terms of BEOL structure and account for all the variations within BEOL structure.

Wafer level model location was changed with respect to BEOL level model to study the impact of gap region and average metal density. Various locations, 1 to 9 were selected as shown in Figure 46 to study the impact, wafer level model where the location was chosen from different region. The locations were chosen to represent different regions like, region A, region B, region C and their intersections with each other and with pillar/bump boundary. The maximum ERR values for all the locations are presented in Figure 47. The maximum ERR value was at locations 5 which is on the intersection of region B with 20% metal density and region C with 0% metal density. The value for the maximum ERR was at the same location as the maximum first principal stress.

The impact of the gap width, G for region C and average metal density in region A were studied and results are presented in Figure 48. The maximum ERR value is proportional to the gap width G and there is negligible impact in ERR values with respect to average metal density of region A. The reason for negligible impact of average metal density in region A is because of the location for the maximum ERR value is on the boundary of the region B and region C, which is not affected by change in metal density for region A.

4.6. Summary and Conclusion

Three numerical fracture/delamination evaluations techniques such as, VCCT specialized, VCCT ANSYS native, and J-integral ANSYS native have been studied and compared for BEOL reliability under CPI loading. J-integral ANSYS native proved flexible approach allowing use of tetrahedral mesh for complex BEOL structure and was in close agreement with analytical solution for DCB specimen. Parametric analysis under the CPI loading have been performed for flip chip ball grid array package to study the impact of wiring density and crack location within BEOL structure. The wafer level BEOL structure with maximum via and copper connections in all metal layers in BEOL structure induced maximum ERR. The crack location, on top of metal layer M3, was highest among the metal layers M1-M6 having ULK dielectric material. The maximum ERR was propositional to gap size of the region with no copper connections and was proportional to first principal stress. Parametric study presented in this work could be leveraged as a guideline for the similar future studies for reliability assessment of the packages under CPI loading.

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BIBLIOGRAPHY STATEMENT

Tushar Chauhan received Bachelor of Engineering degree in mechanical engineering from the Maharaja Sayajirao University of Baroda. He worked as mechanical design engineer for General Electrics (Alstom India Ltd) in renewable energy division on hydro power plants for five years. He received the master's degree (MS) in mechanical engineering from SUNY Binghamton, NY where he was awarded Dr. Bhagwan Gajwani fellowship.

Tushar is a Graduate Research Assistant (GRA) in the Electronic, MEMS and Nano-electronics Packaging Center (EMNSPC) at the University of Texas at Arlington. His current research focuses material characterization and compatibility of electronics devices for immersion cooling and reliability assessment under CPI loading. During his PhD, Tushar interned at Marvell Technology Group Ltd. (Inphi Corporation), LA in 2020-2021 where he worked on reliability assessment of electronics packages under CPI loading and developed numerical fracture analysis toolkit.