CHARGE TRANSFER AND BUILT-IN FIELDS AT A SEMICONDUCTOR-CRYSTALLINE OXIDE INTERFACE: EFFECTS OF THE INTERFACE DIPOLE AND SURFACE TERMINATION

By

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Abstract

Charge transfer and built-in fields across semiconductor heterojunctions underpin the functionality of virtually all device technologies. In this regard, interfaces between insulating oxides and semiconductors have been extensively studied due to the success of metal-oxide-semiconductor (MOS) technology. Perovskite oxides were originally proposed as potential replacements as a gate dielectric for MOS field-effect transistors because device scaling effects make SiO_2 gate leakage too high. However, perovskite oxides containing transition metals display many other properties not found in semiconductors such as ferroelectricity, high-T superconductivity and metal-insulator transitions. Recent advancements in growth technology allow for the creation of structurally coherent interfaces between crystalline complex oxides and semiconductors, enabling the study of band alignment and charge transfer across them. Inherent to semiconductor-crystalline oxide interfaces is an interfacial dipole that modifies the structure near the interface. Key to realizing functional behavior at semiconductor-crystalline oxide interfaces is the ability to electrically couple their properties at the interface including band offsets and band bending. In this work we show that the interfacial dipole of a $SrTiO_3$/Si heterojunction can be modified through space charge and surface termination to realize tunable band alignment across semiconductor-crystalline oxide interfaces. Additionally, a new method of deposition-last device patterning is discussed in which the substrate is patterned before film growth to circumvent the need for specific dry- and wet-etching processes typical of transition-metal oxides. The ability to tune band alignment and built-in fields across semiconductor-crystalline oxide heterojunctions opens a pathway to realize functional behavior in hybrid heterojunctions.

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Chapter 1: Introduction

1-1 Motivation

Semiconductor heterojunctions are the basis for electronic and optoelectronic device technologies that have revolutionized energy harvesting and computing technologies. Central to the development of electronic technologies is the understanding of charge transfer and built-in electric fields across heterojunctions. One of the most widely used heterojunction devices is the p-n junction in which a heterojunction is made between a p-type and n-type semiconductor. The charge transfer and resulting electric fields across the heterojunction determine device behavior. Herbert Kroemer recognized in his Nobel lecture that the *"interface is the device"* [1.1]. Examples of semiconductor heterojunction devices are shown in Figure 1.1.

Figure 1.1: Various electronic devices created from semiconductor heterojunctions. Some examples include transistors, integrated circuits, solar cells, lasers and light-emitting diodes.

Another important heterojunction responsible for the rapid advancement in computational technology is the one between insulating SiO_2 and Si which is used in metal-oxide-semiconductor (MOS) capacitors comprising the gate stack of MOS field-effect transistors (FETs). To match increasing computational demands, MOSFET device scaling is required such that more transistors can fit onto one chip. Device scaling requires that the gate oxide thickness decreases, and ultimate scaling limits are reached for poly-Si/SiO_2/Si gate stacks when the insulating SiO_2 layer reaches ~1 nm. The scaling limit occurs because the oxide thickness becomes too thin to act as a good insulator since tunneling effects will increase gate leakage, which in turn effects device performance. To circumvent this problem, a thicker layer of a higher dielectric constant material can be used such that the required capacitance per unit area remains the same as for a SiO_2 gate insulator. In this regard, heterojunctions between crystalline oxides and semiconductors have been extensively studied in search of a replacement for the SiO_2 gate insulator due to their higher dielectric constants and inherently low density of interface trap states [1.2].

Advances in epitaxial growth techniques were first utilized to created MOS devices out of crystalline $SrTiO_3$ and Si in 1998 [1.3]. The authors established that by paying careful attention to the energetics of each deposited layer, commensurate, thermodynamically stable heterojunctions could be created from $SrTiO_3$ and Si. MOS devices created from these heterojunctions were found to have an equivalent-oxide-thickness (EOT) of < 1 nm, and working MOSFET devices were created using STO/Si heterojunctions by the Motorola group in 2000 [1.4]. However, the type-II band alignment at STO/Si interfaces led to high leakage currents in the devices. To reduce leakage currents, researchers at IBM created MOSFETs out of a larger bandgap oxide, $SrHfO_3$ and Si [1.5]. However, HfO_2 gate insulators have emerged as the top oxide of choice for MOSFET devices [1.6].

While many commercially successful devices have been created from semiconductor heterojunctions [1.7], most remain within the metal-oxide-semiconductor (MOS) paradigm in which the oxide strictly acts as a gate dielectric. Beyond being high-k dielectrics, complex oxides, which typically contain transition metals, also exhibit rich electronic phase diagrams because of their strongly correlated electrons in d orbitals. Transition metal oxides have been

found to exhibit a variety of material properties including dielectric, semiconducting, ferroelectric, high-T superconductivity, ferromagnetism and other correlated electron phenomena [1.8], [1.9]. Complex oxides with the perovskite crystal structure are intriguing because advances in film growth techniques now allow these structures to be epitaxially grown on diamond cubic and zincblende (100) surfaces such as Si, Ge, GaAs and GaN. [1.3], [1.10], [1.11].

Epitaxial growth of complex oxides on semiconductors allows for integration of their material properties to be incorporated into currently viable commercial infrastructure. While epitaxial growth allows for incorporating multifunctional material properties on semiconductor platforms, it is necessary to also couple the electrical properties of complex oxides with those of semiconductors. Interfaces between semiconductors and complex oxides exhibits abrupt discontinuities in elemental composition, crystal structure and type of bonding at the interface, which transitions from being covalent to ionic. The differences in material properties between semiconductors (high carrier mobilities and direct band gaps) and complex oxides (ferroelectric, ferromagnetic and metal-insulator transitions) means epitaxially combining them in heterojunctions may allow electrical coupling between them to produce properties that are not found in either material [1.12], [1.13].

To electrically couple oxides with semiconductors it is necessary for dielectric displacement to be continuous at the interface [1.14], which requires that the interface have a very low defect density and be free of any unwanted interfacial oxide. Since MBE allows for the creation of near perfect interfaces free of interfacial oxides, it is now possible to study electrical coupling across crystalline oxide-semiconductor heterojunctions.

Conventional methods of altering band alignments at semiconductor heterojunctions can also be applied to oxide-semiconductor heterojunctions such as band-gap engineering in which band gaps are altered by compositional changes. This has been demonstrated for crystalline oxide-semiconductor heterojunctions where a solid solution of $SrTiO_3$ and $SrZrO_3$ was grown epitaxially on Ge [1.15]. More recently, Lim *et al.* demonstrated charge transfer at a semiconductor-crystalline oxide interface resulting in a hole gas in the Si [1.16]. It was found

that the hole gas carrier density at $SrNb_xTi_{1-x}O_3$/Si(100) interface could be tuned through modification of Nb content in the oxide which acts as an n-type dopant in STO. It was suggested that the hole gas formation was due to the interplay between the type-III band alignment, surface depletion and the presence of oxygen impurity donors near the Si surface.

The overall goal of this work is to extend the understanding of the band alignment at $SrTiO_3$/Si heterojunctions by systematically studying the phase space of parameters implicated in hole gas formation at $SrTiO_3$/Si heterojunctions. The ability to tune heterojunction band offsets opens an additional pathway to create designer heterojunctions where the distinct but complementary properties of oxides and semiconductors can be electrically coupled in heterojunction devices.

1-1.1 Tuning band alignment at a semiconductor-crystalline oxide heterojunction via electrostatic modulation of the interfacial dipole

To better understand the cause of the type-III band alignment at STO/Si heterojunctions and the effects of oxygen impurity donors on charge transfer and band offsets, a series of films with different oxygen impurity content are grown and characterized. A combination of electrical transport, hard x-ray photoelectron spectroscopy (HAXPES), secondary ion mass spectroscopy (SIMS), STEM imaging and first principles DFT calculations are used to explore the physical and electronic structure of STO/Si heterojunctions. Inherent to semiconductor-crystalline oxide heterojunction interfaces is an electronic dipole that forms due to bonding at the interface. It was found that the dipole can be exploited to tune the band offsets through space charge across the heterojunction interface. The tunability of the interface dipole is explored by variation in oxygen impurity concentration as well as other n-type dopants in Si. The band alignment was tuned from a type-II band alignment with minimal charge transfer and small valence band offset to a type-III band alignment with significant charge transfer and large valence band offset. In principle, a combination of band gap engineering and space charge modification of the interface dipole could allow for a wide variety of band offsets and built-in potential profiles to be realized in semiconductor-crystalline oxide heterojunctions [1.17].

1-1.2 Sub-monolayer surface termination control of charge transfer across a semiconductor-crystalline oxide heterojunction

Surface depletion at STO/Si heterojunctions is thought to be correlated to the band alignment at the interface. In this regard, STO/Si heterojunction band offsets and charge transfer are explored through deposition of various oxide capping layers such as SrO, BaO, TiO_2, $BaTiO_3$, La-STO and amorphous STO. A combination of electrical transport and photoelectron spectroscopies are used to study the effects of various surface terminations. While the underlying mechanism is still under debate, the capping layers have significant impacts on band alignment and charge transfer across the heterojunction interface [1.18].

1-1.3 Deposition-last lithographically defined epitaxial complex oxide devices on Si(100)

The patterning and etching of heterojunction materials to create devices must be established if the heterojunctions will ever reach commercial availability. However, because transition metal oxides often require specific recipes to be created to selectively etch away layers to create devices, it is necessary to develop device creation methods in which the transition metal oxide can be grown after device patterning. A new method of device fabrication is presented in which a pseudo-mask is created on the semiconductor substrate by texturing the surface through a combination of wet- and dry-etch techniques. The pseudo-mask enables direct oxide epitaxy on the substrate in which epitaxy is inhibited outside of the device regions. This method has been successfully demonstrated to create STO/Si(100) Hall bar devices. A combination of electrical transport, XRD, AFM and SEM imaging are utilized to study the electrical and structural properties of the Hall bar devices created on Si(100) surfaces [1.19].

1-2 Statement of Originality

The work presented in Chapters 5, 6 and 7 is collaborative in nature, so I will summarize the contributions of myself and others.

In Chapter 5: Tuning Band Alignment at a Semiconductor-Crystalline Oxide Heterojunction, MBE film growth and electrical transport measurements were carried out by me. Analysis of electrical transport data was done by and me and J. H. Ngai. Film growth and electrical transport measurements and analysis of the 12 nm STO/Si-CZ sample were done by Z. H. Lim. HAXPES measurements were done by J. Gabel and T.-L. Lee at Diamond Light Source. Analysis and fitting of HAXPES spectra was done by S. A. Chambers and P. V. Sushko at Pacific Northwest National Lab (PNNL). First-principles DFT calculations were also done by P. V. Sushko. ADF and iDPC STEM imaging and analysis was carried out by A. N. Penn and J. M. LeBeau at North Carolina State University and MIT, respectively. STEM-EELS was done by D. M. Kepaptsoglou and Q. M. Ramasse at SuperSTEM. SIMS data was taken by Z. Zhu at PNNL. Lab based HAXPES data was acquired at Temple University by A. X. Gray and his students J. R. Paudel, R. K. Sah and J. D. Grassi. Some STEM imaging and analysis was done by B. E. Matthews and S. R. Spurgeon and PNNL.

In Chapter 6: Sub-monolayer surface termination control of charge transfer across a semiconductor-crystalline oxide heterojunction, MBE film growth and electrical transport measurements and analysis were done by me. HAXPES data was acquired at Diamond Light Source by J. Gabel and T.-L. Lee, and analysis and fitting of the HAXPES spectra was done by S. A. Chambers and P. V. Sushko at PNNL. SIMS data was taken by Z. Zhu at PNNL.

In Chapter 7: Deposition-last lithographically defined epitaxial complex oxide devices on Si(100), the photolithography mask design was done by J. H. Ngai and G. Lorkowski at UTA. Conceptualization of the deposition-last mask design and process design was done by J. H. Ngai. The creation of patterned wafers, MBE film growth and electrical transport measurements were done by me. XRD, AFM and SEM sample characterization was carried out by J. C. Jiang at UTA.

Chapter 2: Background

2-1 Semiconductors

Semiconductors can come in several different types including elemental (i.e. Si, Ge), binary (i.e. GaAs, GaN) and oxide semiconductors. The focus here will be on elemental semiconductors since Si is the most widely in industry.

The crystal structure of Si is diamond cubic which is a face-centered cubic structure with a two-atom basis of (0,0,0) and (¼, ¼, ¼). Atoms in the diamond cubic structure are tetrahedrally bonded to its four nearest neighbors as shown in Figure 2.1. Si has a lattice constant of 0.543 nm.

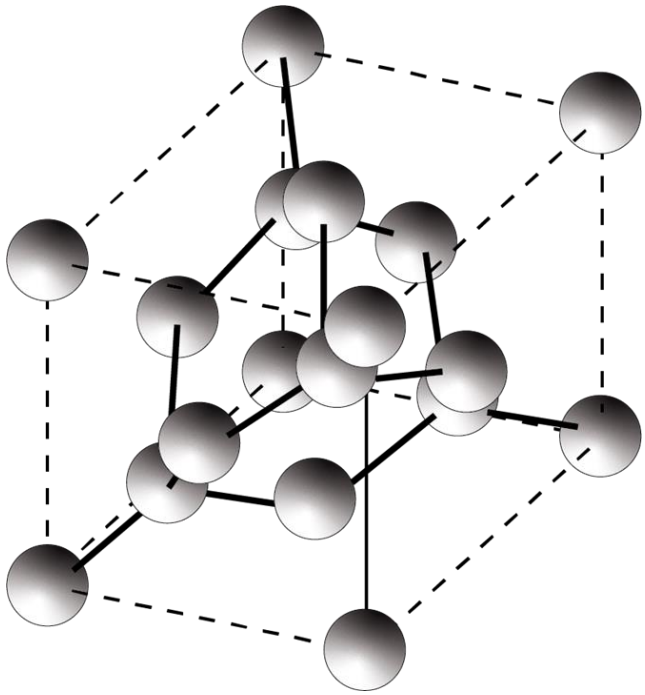

Figure 2.1: Diamond cubic crystal structure. Each Si atom has tetrahedral coordination with the 4 nearest neighboring Si atoms.

A key feature of intrinsic, group IV semiconductors is that they have a band gap in which the valence(conduction) band is filled (empty) at 0 K. At finite temperatures, however, there will be some occupation of states in the conduction band and unoccupied states in the valence band following the Boltzmann distribution.

A parabolic energy dispersion relation can be used near the band edges:

$$E(k) = \frac{\hbar^2 k^2}{2m^*}$$

where m^* is the effective mass of the charge carriers and is determined by the curvature of the E-k relationship. The difference in energy from the top of the valence band to the bottom of the conduction band is called the *band gap* of the material. Some semiconductors, such as Si, have *indirect band gaps* where the top of the valence band and bottom of the conduction band are at different k values. Others, such as GaAs, have *direct band gaps* where the top of the valence band and bottom of the conduction band are at the same k values. For processes that involve transitions between the valence and conduction bands, momentum is conserved for direct gaps and not conserved for indirect gaps. This makes GaAs a particularly useful semiconductor for photonics applications since electrons falling from the conduction band to valence band, a process called *recombination*, can produce photons since there is no need for additional momentum to be supplied through phonon interactions.

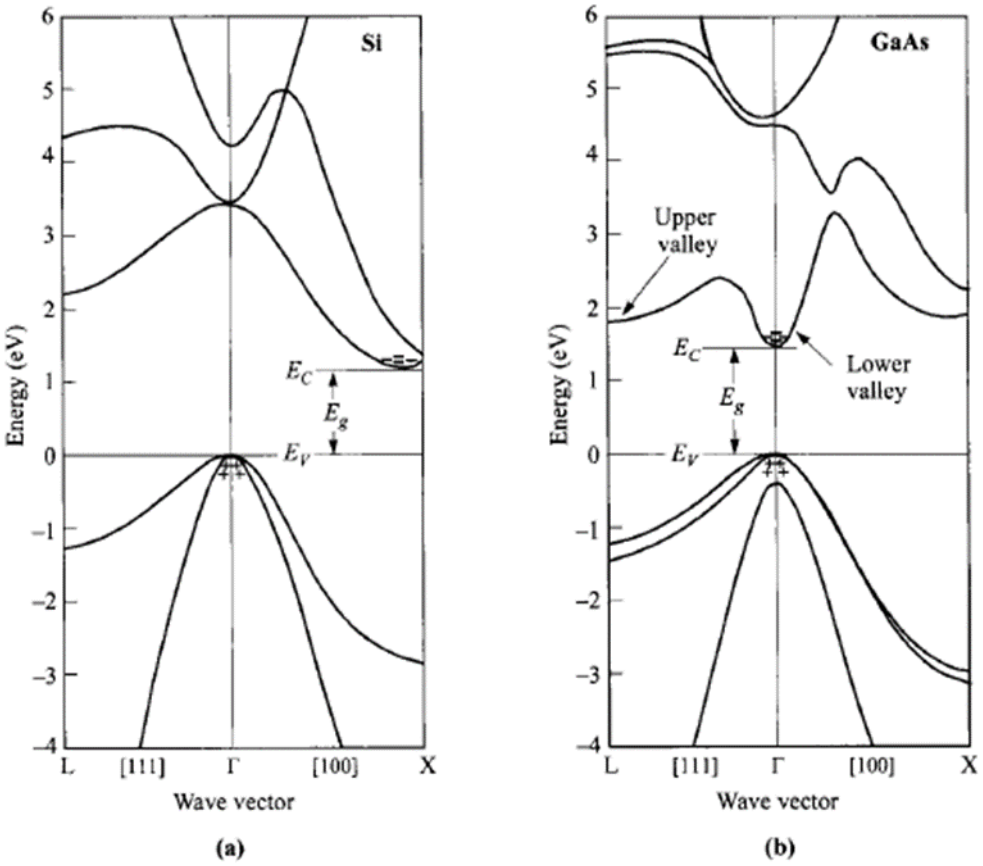

Figure 2.2: Energy band dispersion for (a) Si and (b) GaAs [2.1].

Semiconductors can be made to be conductive by *doping* either n-type or p-type using elements with either one extra (group V) or one less (group III) valence electron which act as electron donors or acceptors, respectively. Typical dopants used in Si are B and Ga for p-type doping and P and As for n-type doping. The dopant levels typically lie close to the band edges and occupation of conduction or valence band levels is a function of temperature and the proximity of the dopant level to the band edge. Detailed calculations of carrier concentrations in semiconductors as a function of dopant density, temperature and distance to the band edges can be found in Simon Sze and Kwok Ng's textbook *Physics of Semiconductor Devices* [2.1].

A key property for designing heterojunction devices is the electron and hole carrier mobility in the material. Mobilities are a function of both carrier concentration and temperature as seen in Figure 2.3. Since carrier mobilities are often significantly higher in

semiconductors than in transition metal oxides, integration of oxides and semiconductors may allow for the exploitation of higher carrier mobilities of semiconductors with the functional properties of complex oxides.

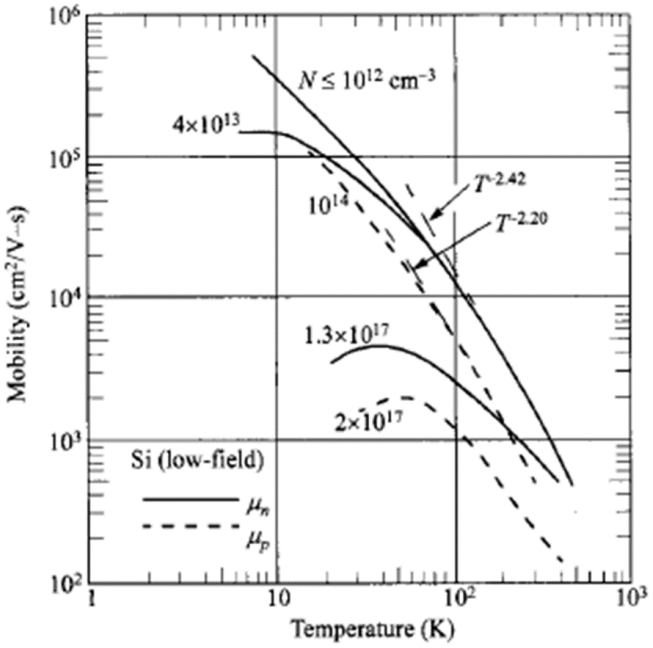

Figure 2.3: Si mobility as a function of temperature and carrier density [2.1].

2-2 Complex Oxides

Complex oxides are materials containing oxygen and two or more other elements. When one of the other elements is a transition metal, the material is called a transition metal oxide. Oxides are of great interest for both fundamental research and technological applications because they exhibit a wide range of material properties such as dielectric, semiconducting, ferroelectric, ferromagnetic, superconducting and other strongly correlated phenomena [2.2], [2.3], [2.4].

Of particular interest here are transition metal oxides with the *perovskite* crystal structure with the formula ABO_3, as they can be epitaxially integrated onto other cubic lattices such as diamond cubic and zincblende semiconductors like Si, Ge and GaAs. The structure is a

combination of face-centered cubic and body-centered cubic with A- and B-site cations occupying the corners and center of the cubic structure, respectively. O atoms occupy the face centers and form octahedral coordination with the B site transition metal as shown in Figure 2.4. One of the reasons perovskites exhibit a wide range of material properties is due to the perovskite structure allowing almost every element in the periodic table to be incorporated into it.

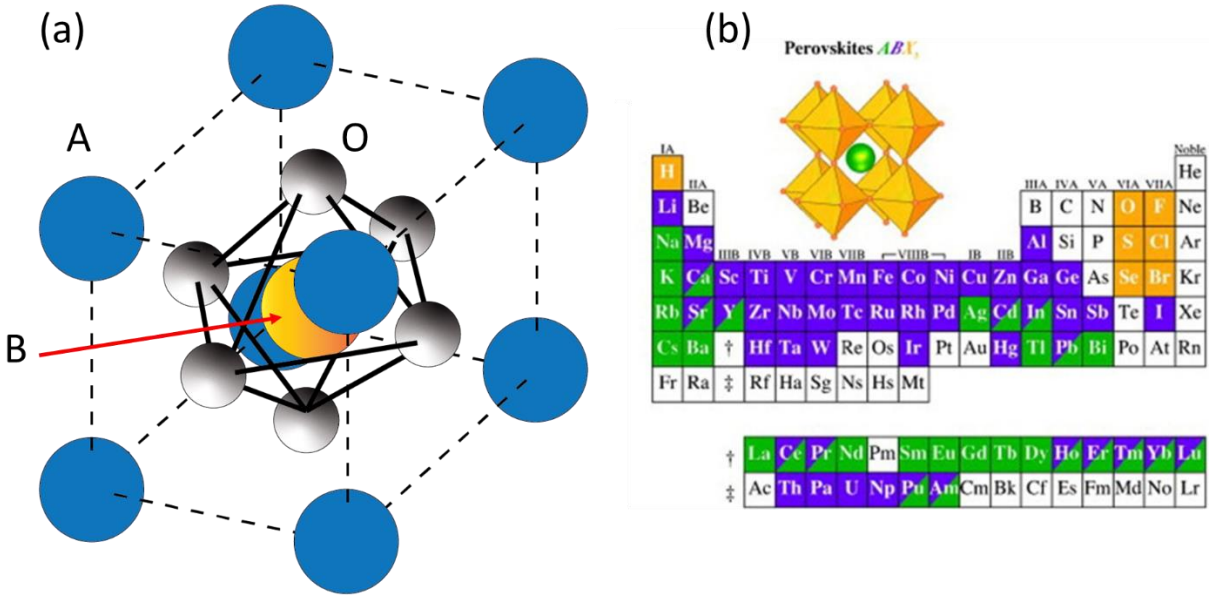

Figure 2.4: (a) Perovskite crystal structure, ABO_3. (b) Periodic table indicating which elements can be incorporated into the perovskite structure [2.5].

For insulating, semiconducting and metallic oxides, the bands are analogous to conventional band theory as shown in Figure 2.5, except the valence bands are made up of O 2p orbitals and the conduction bands are the transition metal d orbitals. The valence electrons are d electrons. A key feature of complex oxides is the spatial confinement of d orbitals compared to s orbitals such that the overlap of orbitals plays a much larger role in electronic properties. Band widths are determined by the overlap of d orbitals in adjacent unit cells.

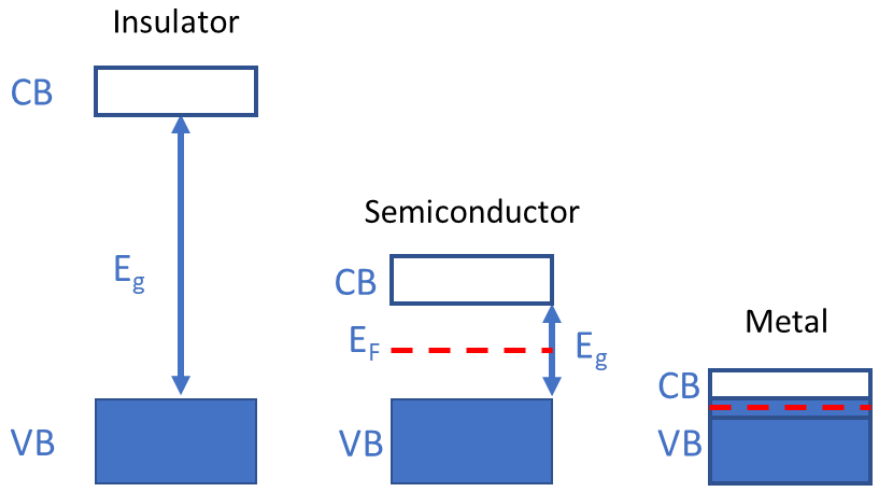

Figure 2.5: Band theory description of insulators, semiconductors and metals. Insulators have wide band gaps and filled (empty) valence (conduction) bands. Intrinsic semiconductors are similar to insulators but with smaller band gaps such that at elevated temperatures there are some valence band electrons excited to the conduction band. In metals, the conduction and valence bands overlap.

Electrons in the B site transition metal atom can occupy d orbitals d_{xy}, d_{yz}, d_{zx}, $d_{x^2-y^2}$ and d_{z^2}, which are degenerate as free atoms. However, within the perovskite structure, these orbitals are perturbed by the octahedral coordination with oxygen atoms and the energy levels are split into 3-fold degenerate t_{2g} and 2-fold degenerate e_g energy levels. The two higher energy levels, e_g, being the orbitals that have lobes in the direction of oxygen anions and the lower energy levels, t_{2g}, having lobes pointing away from oxygen anions.

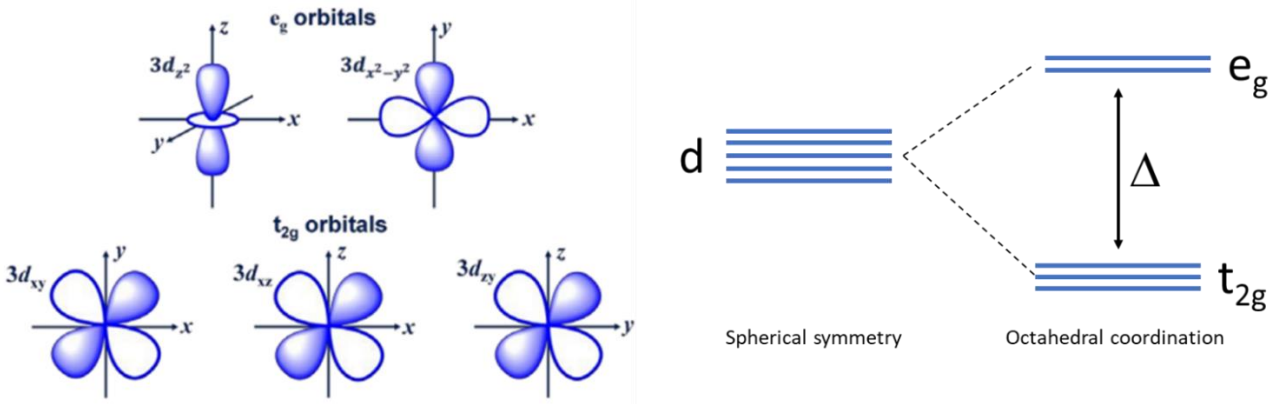

Figure 2.6: (Left) The five 3d orbitals [2.6] (Right) 3d energy level splitting in an octahedrally coordinated crystal field.

In adjacent unit cells, hybridization between B site transition metal d orbitals and O p orbitals occurs which allows electrons to hop between B site atoms by way of O atoms. The bonding angle between B-O-B bonds can be either 180° or less, depending on the relative size of the A- and B- site atoms. Different size atoms will produce distortions in the structure and can be calculated using the Goldshmidt tolerance factor:

$$t = \frac{r_A + r_O}{\sqrt{2}(r_B - r_O)}$$

r_A, r_B and r_O are the ionic radii of the A-site atoms, B-site atoms and O atoms, respectively. The tolerance factor determines the degree of distortion in the structure and for a stable perovskite structure, $0.89 < t < 1$. For $SrTiO_3$, the tolerance factor is close to 1 and the Ti atoms sits in the center of the O octahedra.

Distortions in the structure are rotations of the O octahedra. Octahedral rotations have the effect of changing the B-O-B bonding angles and effect the electronic properties of the material in different ways [2.7]. Octahedral compression or elongation, called Jahn-Teller distortions, produce a change in symmetry which results in further energy level splitting. One method of intentionally producing distortions in a perovskite structure is by growing a thin film on a substrate that has a different lattice parameter to produce strain in the film [2.8].

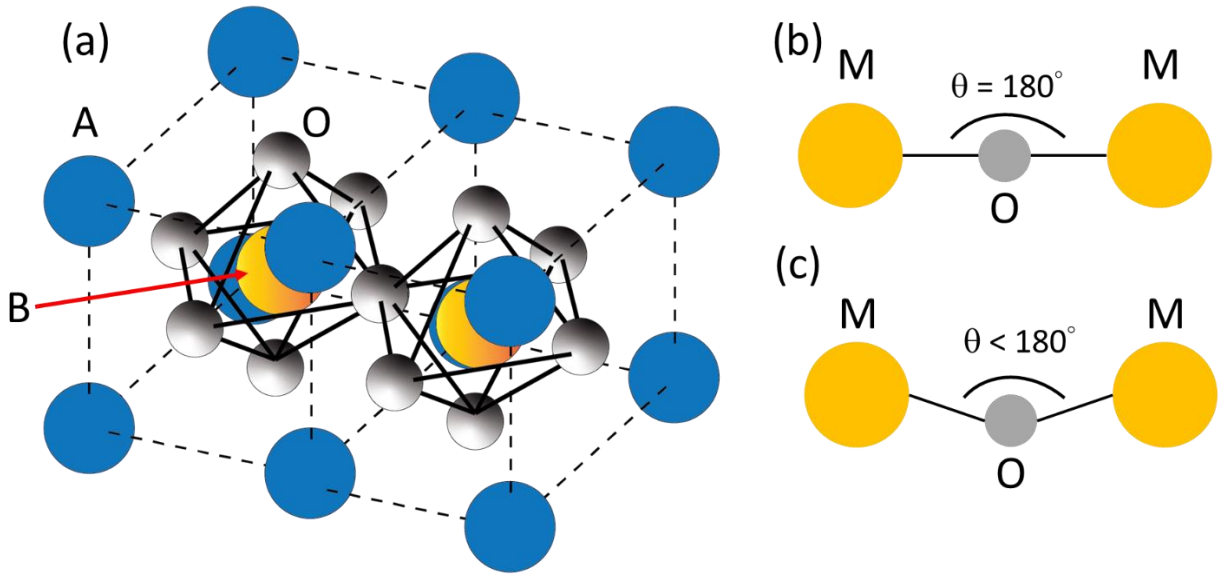

Figure 2.7: (a) Adjacent perovskite unit cells showing how B-site metal cations are connected through oxygen anions. (b) and (c) show schematics of the metal-oxygen-metal bonding angle in ideal perovskite structures and octahedrally rotated perovskite structures, respectively.

2-3 Band Alignment at Heterojunction Interfaces

There are three different ways energy bands can align at interfaces: type-I (straddling), type-II (staggered) and type-III (broken). As shown in Figure 2.8, for type-I band alignments, the CB and VB of Material 2 straddle the CB and VB of Material 1, creating a barrier for electrons and holes in the Material 1 to be transferred to Material 2. This type of band alignment requires that the band gap of Material 2 be larger than the band gap of Material 1. For type-II (staggered) band alignments, the CB of Material 2 lies in the band gap of Material 1, while the VB of Material 2 lies below the VB of Material 1. In type-III band alignments, both the CB and VB of Material 2 lie below the VB of Material 1.

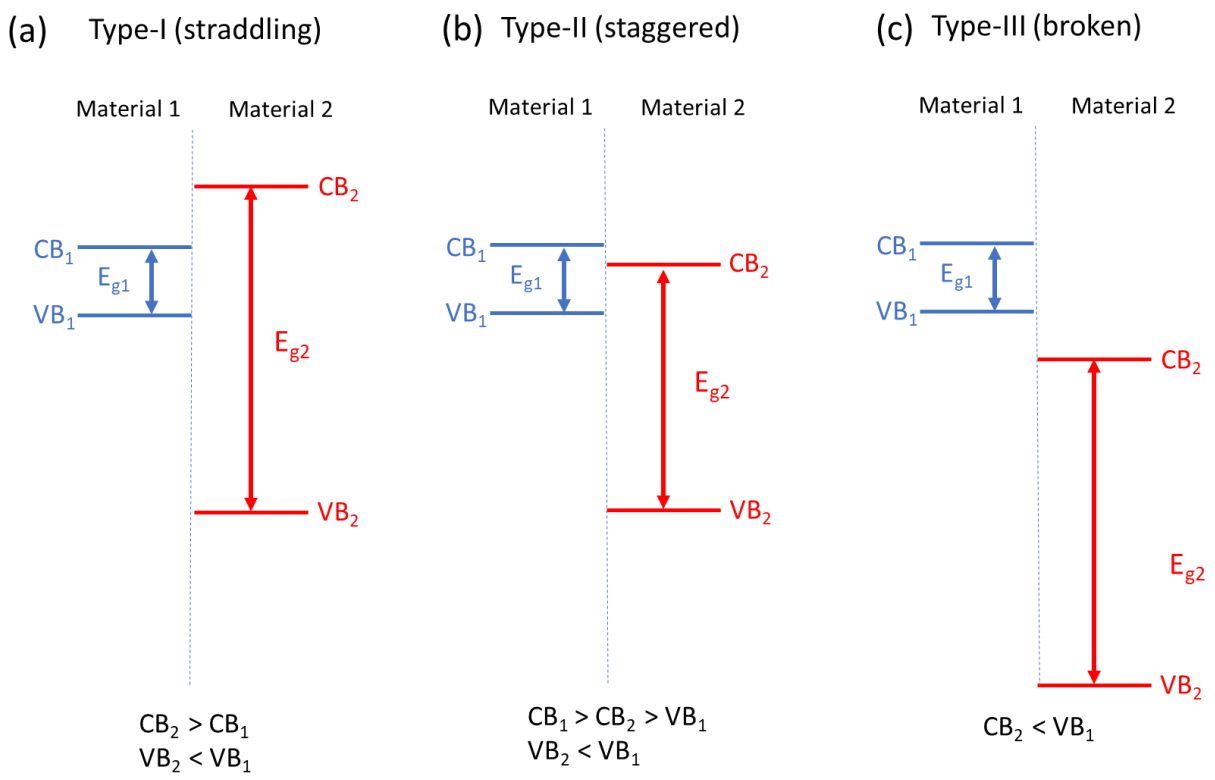

Figure 2.8: (a) Type-I (straddling) band alignment. (b) Type-II (staggered) band alignment. (c) Type-III (broken) band alignment.

A central problem in designing electronic devices is the determination and manipulation of band alignment and band offsets at heterojunctions as they are key parameters in determining device functionality. In this regard, it is important to understand how band alignment is determined at interfaces.

Starting from one of the simplest interfaces, when two metals are brought into electrical contact, electron transfer from one to the other will occur until the Fermi levels equalize. This will result in a contact potential difference of:

$$V_C = \frac{(\Phi_1 - \Phi_2)}{e}$$

Φ_1 and Φ_2 are the work functions of the two metals and e is the elementary charge. For metals, the work function is defined as the amount of energy needed to remove an electron from the highest occupied state (from a partially filled band) to just outside the material (vacuum level).

Band alignment at a semiconductor-semiconductor interface is complicated by the fact that there can be bonding across the interface, forming interface dipoles. There are two types of dipoles that can be formed: dipoles created by charge exchange between interface states [2.9], and dipoles formed by epitaxial bonding at crystalline interfaces [2.10]. Dipoles that arise from epitaxial bonding between crystalline materials are central to this work and discussed further in Chapter 5. Charge exchange between interface states is discussed here.

In the Schottky limit, where the effects of bonding can be neglected, the conduction band offset is equal to the difference in electron affinities, χ.

$$\Delta E_{CB} = \chi_a - \chi_b$$

While the electron affinity model works for systems in which the effects of bonding can be neglected, it is often the case that some degree of charge exchange exists between interface gap states. In this regard, it is necessary to define a new quantity, the charge neutrality level (CNL), which can be calculated as a weighted average of the density of states of bulk conduction and valence bands [2.11]. Additionally, the Schottky pinning parameter, S, gives an indication of the degree of charge exchange between interface states. The pinning parameter can be calculated from the equation:

$$S = \frac{1}{1 + 0.1(\varepsilon_\infty - 1)^2}$$

Here, ε_∞ is the optical dielectric constant of the material. With the CNL and pinning parameter defined, the conduction band offset for a heterojunction between semiconductors “a” and “b” can be calculated from

$$\phi_n = \left(\chi_a - \Phi_{CNL,a}\right) + \left(\chi_b - \Phi_{CNL,b}\right) + S(\Phi_{CNL,a} - \Phi_{CNL,b})$$

In the Schottky limit (no pinning), S = 1, the conduction band offset is the difference in electron affinities. The Bardeen limit (strong pinning), S = 0, the conduction band offset will also depend on the charge neutrality levels:

$$\text{Bardeen limit: } \phi_n = \left(\chi_a - \Phi_{CNL,a}\right) + \left(\chi_b - \Phi_{CNL,b}\right)$$

In general, though, S will be between 0 and 1 and the conduction band offset can be found by aligning the charge neutrality levels, modified by the S parameter. Expanding this model to wide band gap oxides is possible if the conduction bands can be accurately described by the tight-binding model as in transition metal oxides with d electron conduction bands [2.12]. Wide gap oxides like SiO_2 (S = 0.86) tend to have larger S values than smaller gap oxides like $SrTiO_3$ (S = 0.28) and so conduction band offsets depend more on electron affinities (CNLs) for materials with larger (smaller) band gaps.

Since the CNLs for transition metal oxides are calculated from bulk DOS, there are few ways that the band offsets may be tuned. Firstly, since transition metal valence bands are made up of O p states and conduction bands are transition metal d states, the CNL can be lowered by changing the ratio of CB and VB DOS, which can be achieved by changing the transition metal valence [2.13]. Additionally, CB offsets can be altered is by changing the band gap of the oxide through substitution of a transition metal with 4 or 5 d electrons in place of one with 3 d electrons. One example of this is the substitution of Zr on the B site of perovskite $SrTiO_3$ to form a solid solution of $SrZr_xTi_{1-x}O_3$ (SZTO) which was found to increase the CBO between SZTO and Si relative to that of STO and Si [2.14].

While this model works quite well for wide band gap oxides, it depends entirely on properties of bulk materials such as the electron affinities and CNLs (calculated from bulk DOS). More detailed calculations are required when attempting to include details interfacial bonding. Density functional theory calculations by A. M. Kolpak and S. Ismail-Beigi [2.10] reveal the band offsets are sensitive to interface chemistry and structural arrangement of atoms at the interface. They show that an interfacial dipole is formed at the interface between a crystalline oxide and semiconductor due to the strong electronegativity of oxygen. The interface dipole and its effect on band alignment is explored in Chapter 5 of this thesis.

Chapter 3: Molecular Beam Epitaxy (MBE)

3.1 MBE Overview and General Technique

Molecular Beam Epitaxy is a thin film deposition technique developed by at AT&T Bell labs in the 1960's [3.1], although earlier experiments on the interaction of molecular beams with surfaces was carried out by Gunther [3.2]. The development of MBE, like many other deposition methods, followed from technological advances in other areas. Stoichiometric control of epitaxial films followed from the three-temperature method developed by Gunther in which individual source elements were kept at different temperatures and the substrate at a third temperature. Film quality was further increased when methods to clean substrate surfaces became available. One of the earliest used methods used was ion bombardment to remove native oxides and subsequent thermal annealing to recover from surface damage, which was used to successfully grow single crystal InSb [3.3] and GaAs [3.4] films. The development of UHV systems allowed for the use of RHEED for real-time monitoring of the effect of growth conditions on the properties of the film which is one of the main reasons why MBE is so successful today.

Precise control over film composition and the ability to create smooth, uniform films epitaxially integrated onto a variety of substrates has allowed for wide variety of electronic and opto-electronic devices to be created [3.5] and has led to six Nobel prizes [3.6], [3.7], [3.8], [3.9], [3.10], [3.11]. An excellent history of early MBE technology and devices created can be found in Muhammed Henini's book [3.12]. MBE is widely used in both research and industry today for both fundamental studies and mass production of devices, respectively.

The term *molecular beam* describes the directional flow of atoms or molecules that make up the film. Note that to have a molecular beam, the system must be in ultra-high vacuum (UHV) so there is no collision of beam atoms with gases in the chamber. In UHV pressure ranges (10^{-7}-10^{-12} mbar or 7.5^{-8}-7.5^{-13} Torr), the mean free path of atoms is very high. *Epitaxy* refers to the layer-by-layer crystalline growth of a material in which the film has a structural relationship to the substrate it is growing on, as well as a small lattice mismatch

(<10%). The idea is to direct molecular beams of each source element at a heated substrate where the atoms are given enough kinetic energy to move around on the surface and find their lowest energy state, part of a crystal.

Thin film deposition techniques can be classified as either *physical* or *chemical*. Chemical vapor deposition (CVD) techniques rely on a chemical reaction at the substrate surface whereas physical vapor deposition (PVD) techniques only require the energy needed for the film to condense from the vapor phase (molecular beam) into a crystalline film. There are several different PVD techniques including sputtering deposition, thermal evaporation, electron-beam (e-beam) evaporation and MBE.

While sputtering and e-beam evaporation techniques give large amounts of kinetic energy to the elements being deposited, MBE allows for low energy atoms since the sources are often thermally evaporated using a heating element instead of sputtered from the source material using a high-energy electron beam or plasma.

The MBE system in Dr. Ngai's lab was custom built by Dr. Ngai and several students including myself. The system is specifically designed for deposition of complex oxide films but is also capable of growing group IV semiconducting films. The system consists of a main chamber (MC) in which the MBE process is carried out, and a smaller load-lock (LL) chamber which can be isolated from the main chamber to load and unload samples from the chamber while maintaining UHV in the main chamber. Wafers are inserted into the LL transfer arm and once base pressure is reached the wafer can be transferred into the MC manipulator using the transfer arm. The main chamber has a manipulator capable of holding 2" diameter wafers which can move in any direction and rotate to ensure sample uniformity.

Getting the chamber down to UHV pressures (10^{-10} Torr) requires the use of a two-stage pumping system. In the first stage, an oil-free scroll pump is used as a roughing pump to pump the system down from atmospheric pressure to ~2^{-4} Torr. The second stage is a pair of cryogenic pumps (cryopump) which are attached to the main chamber and load-lock chamber. The LL cryopump gives a base pressure of ~2^{-7} Torr while the MC cryopump allows for a base pressure of ~2^{-10} Torr. Cryopumps work by condensing gases from the chamber on a cold

manifold which is cooled to ~10 K using a He compressor, which capture gases such as N_2, O_2 and Ar, while an activated charcoal stage captures lighter elements such as He. The cryopumps and He compressor make a closed-cycle refrigeration system where the cooling occurs due to repeated refrigeration cycles (reference for Handbook of Vacuum Technology). The MC is equipped with an ion gauge to measure the pressure and a Residual Gas Analyzer (RGA), which is a quadrupole mass spectrometer, to measure the partial pressures of various gases in the system. After venting the system and baking out the chamber the RGA is a valuable tool to help determine if there any leaks in the system as well as determining if the chamber walls and source materials are properly outgassed. A mass spectrometer (Hidden Analytical) is also installed in the system which can measure the partial pressures of metal vapors for *in-situ* determination of source fluxes during film growth.

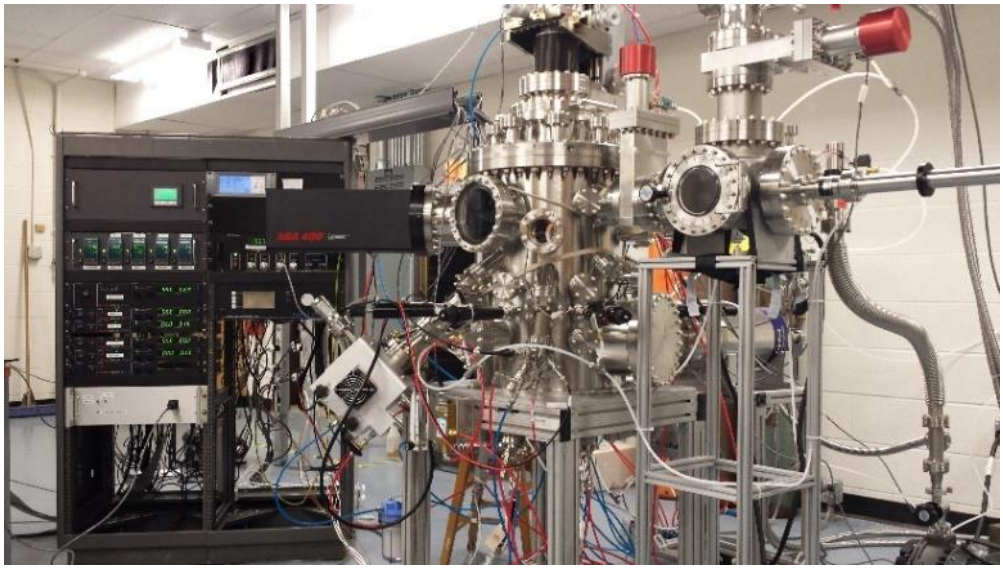

Figure 3.1: Custom-build oxide MBE system at UTA Arlington.

High-purity solid source elemental materials are thermally evaporated from effusion cells (SVTA and Veeco) which consist of a crucible, heating element, heat shield, a thermocouple for measuring the cell temperature and water lines for cooling the cell. The system has five effusion cells installed and are located at the bottom of the main chamber

pointed upward at the substrate. Each cell has a mechanical shutter which can be opened or closed from a LabView program to control which elemental species the substrate is exposed to. This allows for precise control of stoichiometry in the deposited film and atomically abrupt heterojunctions to be formed. The fluxes are measured using a quartz crystal microbalance (QCM) which measures the rate of mass deposition per unit area by measuring changes in the oscillation frequency of a quartz crystal resonator. Calibration curves are measured to determine the deposition rate as a function of effusion cell temperature which can be fit to Arrhenius curves as shown in Figure 3.2. Unfortunately, calibration curves will change as a source is being used up so that measurement with a QCM is still required.

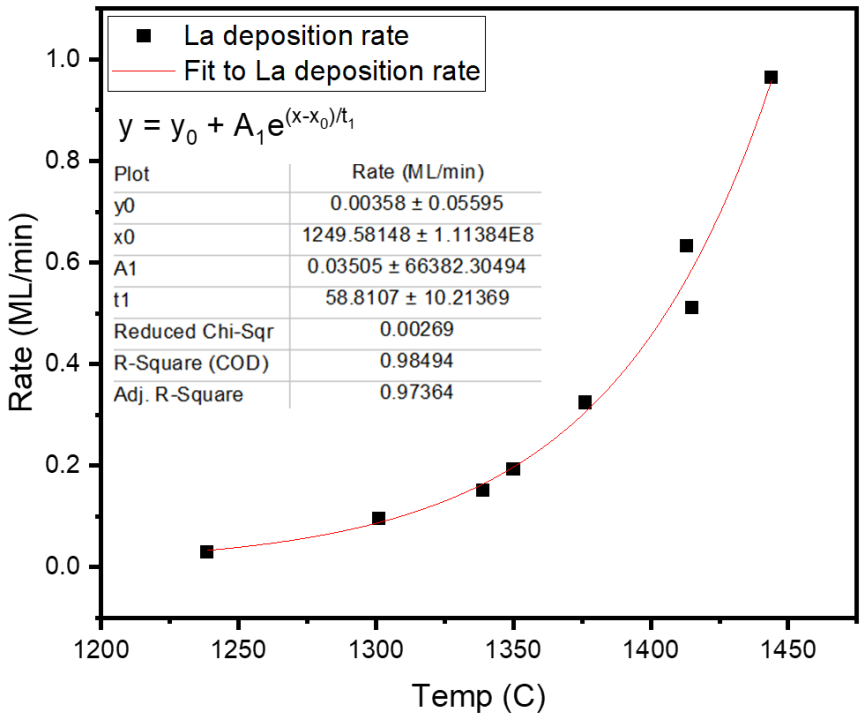

Figure 3.2: Calibration curve for Lanthanum evaporation rate versus effusion cell temperature.

In addition to the five effusion cells, the system is equipped with an e-beam evaporator to allow growth of films using metals that have low vapor pressures. Figure 3.3 shows the

approximate effusion cell temperature that is needed to get a high enough vapor pressure to achieve reasonable film growth rates for various elements [3.12].

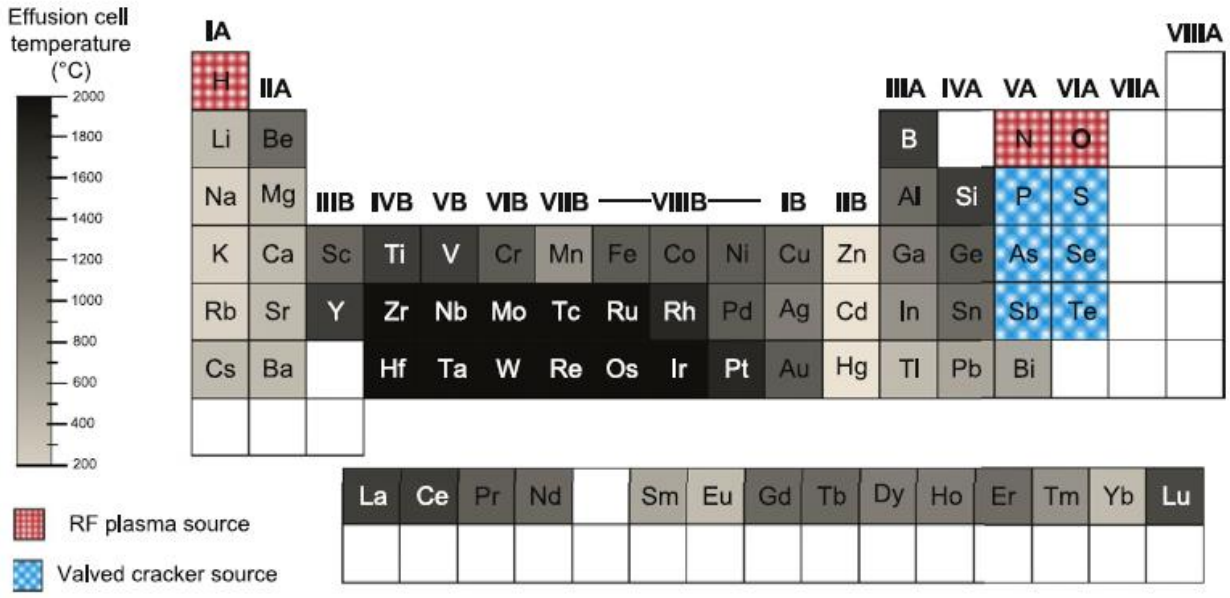

Figure 3.3: Effusion cell temperatures needed to achieve reasonable growth rates for MBE growth [3.12].

Oxygen is introduced into the system via a leak valve connected to a radio-frequency (RF) plasma system (Veeco). A calibration of oxygen pressure at the oxygen leak valve versus chamber background pressure is shown in Figure 3.4. The difference in pressure is due to impedance in the O_2 plasma source.

The growth of epitaxial STO/Si(100) using this system is discussed in section 3.3.

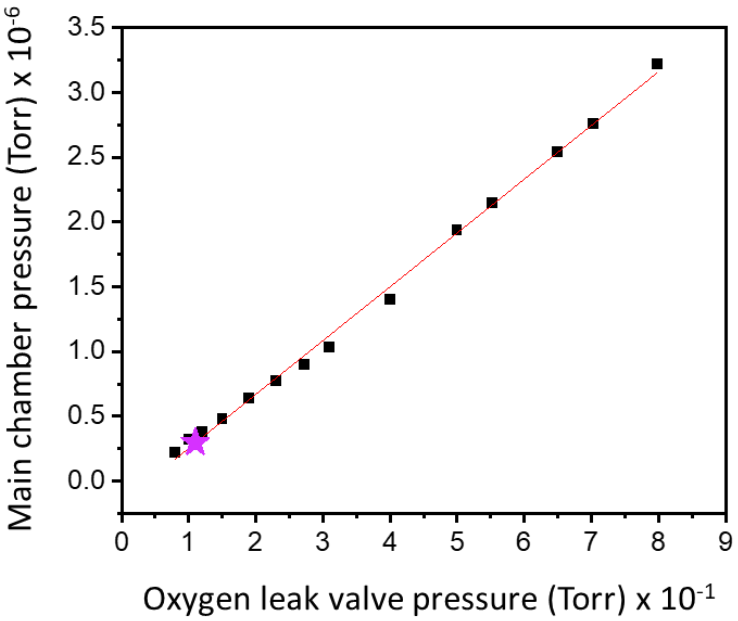

Figure 3.4: Oxygen partial pressure calibration showing what pressure is needed at the leak valve to obtain a desired oxygen partial pressure in the main chamber. The purple star indicates typical oxygen background pressure ($3x10^{-7}$ Torr) used for film growth in this work.

3.2 Reflection High Energy Electron Diffraction (RHEED)

Reflection High Energy Electron Diffraction (RHEED) is a low-angle diffraction technique capable of giving *in-situ* information of a crystal surface during film growth. The setup consists of an electron gun which can create a high energy electron beam (~keV) and both collimate and deflect the beam to allow scanning across the sample surface. The beam is diffracted off a wafer surface at a very low angle of incidence (< 5°) and onto a phosphor window which produces photons when hit with high energy electrons. Collimation of the electron beam is done by deflecting the beam directly onto the phosphor screen and adjusting the beam and objective voltages. Once the beam is well collimated, the X and Y deflection controls allow for positioning the beam on the sample surface. A schematic of the RHEED setup is shown in Figure 3.5.

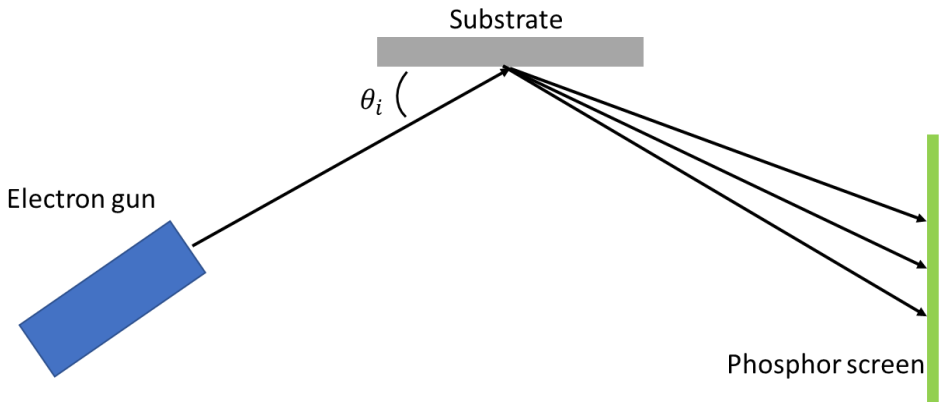

Figure 3.5: Schematic of RHEED system setup. An electron gun emits a high-energy electron beam which is aimed at the substrate surface. Diffraction patterns are viewed on a phosphor screen.

The low angle of incidence gives makes RHEED a highly surface sensitive technique which can determine surface structure and observe surface reconstructions. Observation of surface reconstructions is particularly important when growing epitaxial films as small amounts of material (< 1 ML) can change the structure of the surface layer relative to the substrate as discussed in section 3.3.

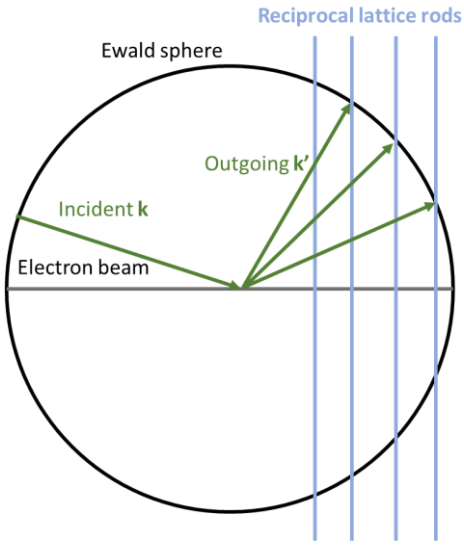

Figure 3.6: Ewald sphere construction for RHEED. Constructive interference patterns are produced when the reciprocal lattice rods intersect the Ewald sphere.

Electrons with an incident wave vector, **k**, impinging on a crystalline surface will diffract according to the Laue diffraction condition for elastic scattering, $\Delta\mathbf{k} = \mathbf{k'} - \mathbf{k} = \mathbf{G}$, where **k** is the incident wave vector, **k'** is the outgoing wave vector and **G** is the reciprocal lattice vector. The incident wave vector has a wavelength of $\lambda = 2\pi/|\mathbf{k}|$. Since elastic scattering requires that $|\mathbf{k}|^2 = |\mathbf{k'}|^2$, the outgoing wave vector will end on a sphere of radius $|\mathbf{k}|$, the Ewald spere. The Ewald sphere construction is shown in Figure 3.6 projected onto 2 dimensions for simplicity. Since the low angle electron diffraction is very surface sensitive, electron diffraction of the surface is essentially from a 2-dimensional plane in which the real-space lattice vector approaches zero. When converted to reciprocal space, the real-space lattice vector perpendicular to the surface will become a lattice rod. The intersection of the reciprocal lattice rods with the Ewald sphere gives constructive interference patterns on the phosphor screen in the form of dots. Along with the surface reconstructions that can be observed with RHEED, qualitative information about the crystal quality can be extracted from the RHEED patterns such as surface roughness as shown in Figure 3.7.

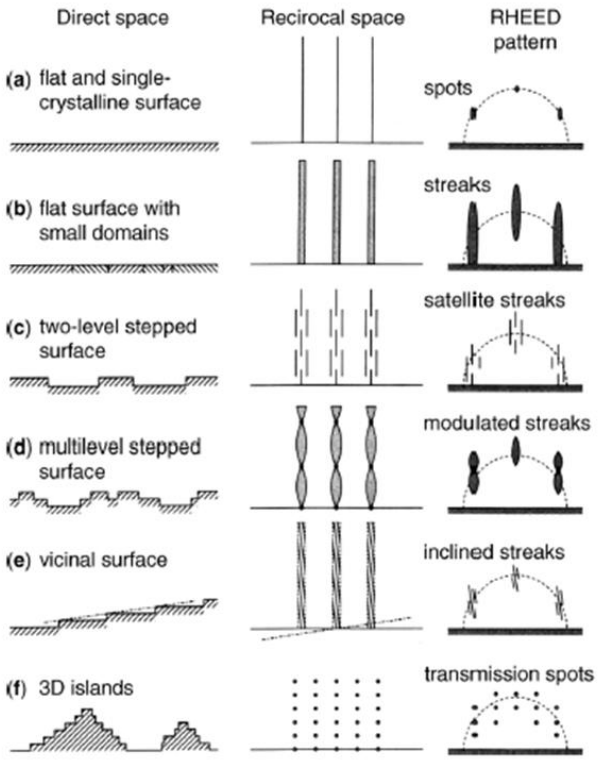

Figure 3.7: Various RHEED patterns produced from different surface morphologies [3.13].

During epitaxial growth, it is common to rotate the substrate to increase film uniformity. Substrate rotation also facilitates RHEED observations in different crystallographic directions. As the substrate rotates, RHEED patterns will rotate correspondingly, and different crystallographic directions can be surmised from the streak separation. Real space lattice plane spacing will be inversely proportional to the reciprocal space lattice plane spacing. Lattice planes for a cubic structure are shown in Figure 3.8 in which the lattice is shown in real space and projected to 2 dimensions to account for the surface sensitivity of RHEED.

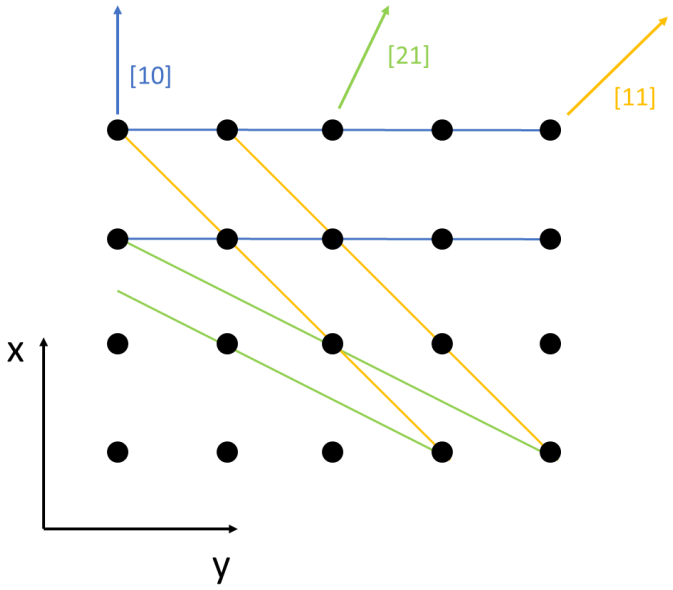

Figure 3.8: Schematic of a cubic crystal structure surface showing the [10], [11] and [21] crystallographic directions.

Lattice plane separation is largest for [10] then decreases in size for [11] and [21] planes which results in RHEED streaks being closest together for [10] planes and increasing in separation for [11] and [21] directions.

Since RHEED is capable of operating during epitaxial growth, it allows for the study of surface structure and film quality during epitaxial growth. This has no doubt been one of the driving factors in the success of MBE as it allows real-time feedback of film structure and quality as a function of growth parameters. In fact, oscillations in the RHEED intensity can be

correlated to surface smoothness within one unit cell, giving intensity oscillations as the film grows for films growing in the layer-by-layer growth mode.

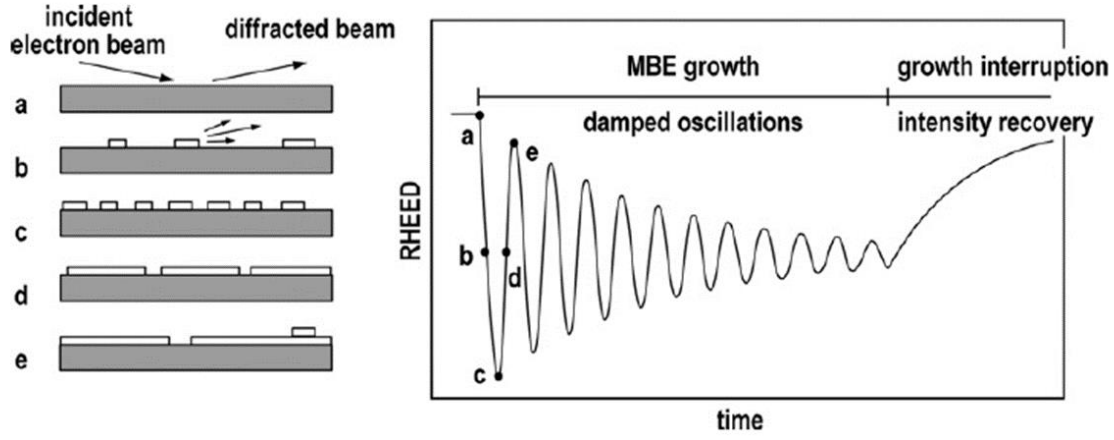

Figure 3.9: Schematic of RHEED oscillations which can be monitored to verify layer-by-layer film growth [3.12].

3.3 Growth of $SrTiO_3$ on Si(100)

The growth of $SrTiO_3$ on Si (100) was first achieved in 1998 by McKee et al. [3.14] in which they used a 0.5 ML Sr template to inhibit the formation of amorphous SiO_2 at the heterojunction interface. The 0.5 ML Sr template can be directly deposited on clean, dimerized Si(100) surfaces or created using a Sr desorption method developed at Motorola [3.15]. The growth of STO on Si(100) surfaces using the Motorola method for SiO_2 removal is described in this section, and is the growth process employed throughout this work.

Wafers are inserted into the MBE system either directly from the manufacturer packaging or after a 3-step cleaning process in acetone, methanol and isopropanol if other processing is required. Wafers are exposed to an activated oxygen produced from high purity O_2 gas in a radio-frequency (RF) source for 10 min at 226 W) to clean off any residual organics from the surface to prevent the formation of SiC at high temperatures. 2 ML of Sr metal is

deposited at 550 °C and heated to 870 °C to form and desorb the native oxide as SiO which is facilitated by the Sr metal [3.15]. As the SiO_2 is desorbed, excess Sr occupies the space where Si dimers would typically form for a clean Si (001) surface. The surface is monitored using RHEED to determine when the surface is clean as evidenced by a (2x1) reconstruction as shown in Figure 3.10.

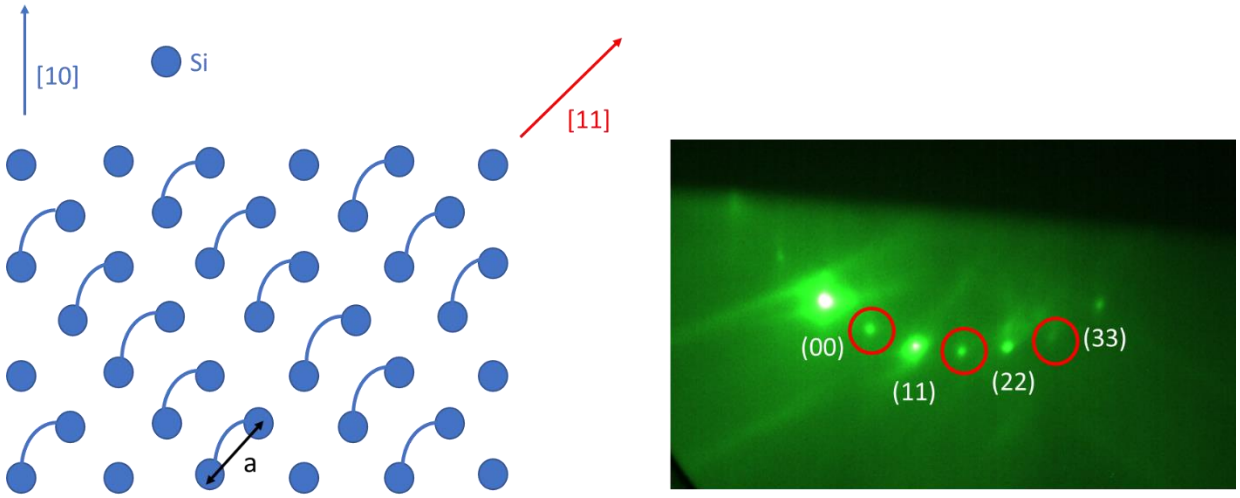

Figure 3.10: Clean Si surfaces dimerizes perpendicular to step edges. The red circles show the 2x1 reconstruction associated with dimerization.

The wafer is then cooled to 660 °C in which a transition from a (2x1) structure to a (3x2) structure can be seen which forms for ~1/6 ML Sr coverage as shown in Figure 3.11. Additional Sr is deposited at 660 °C until the surface structure changes back to a (2x1) structure indicating 0.5 ML Sr coverage as shown in Figure 3.12. The 0.5 ML Sr serves a protective layer against the formation of SiO_2 as well as a template for STO to crystallize on.

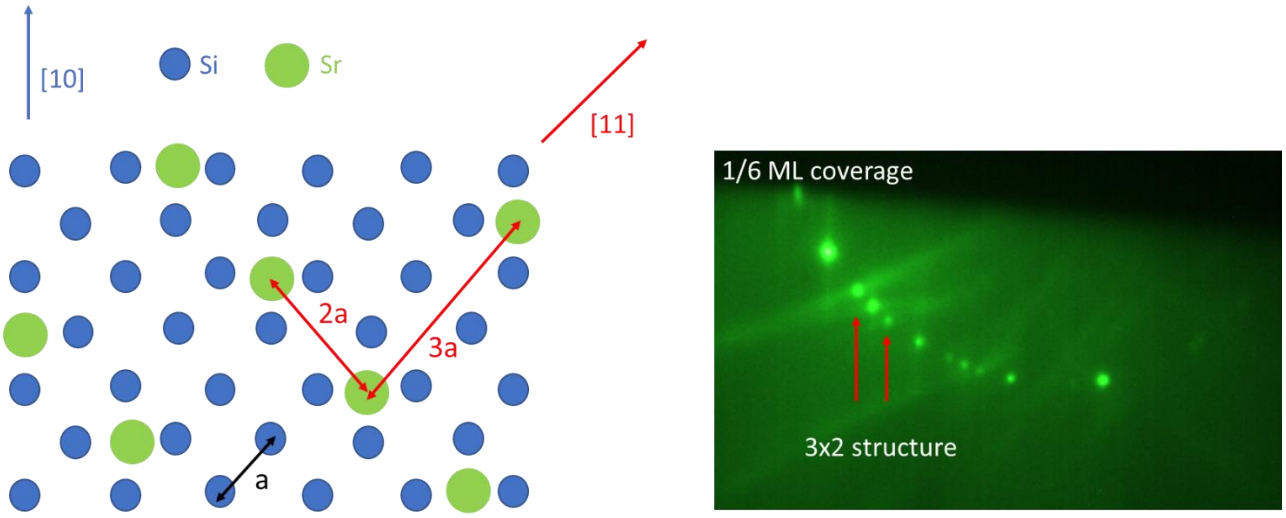

Figure 3.11: 1/6 ML Sr coverage gives a 3x2 surface structure at ~660 °C.

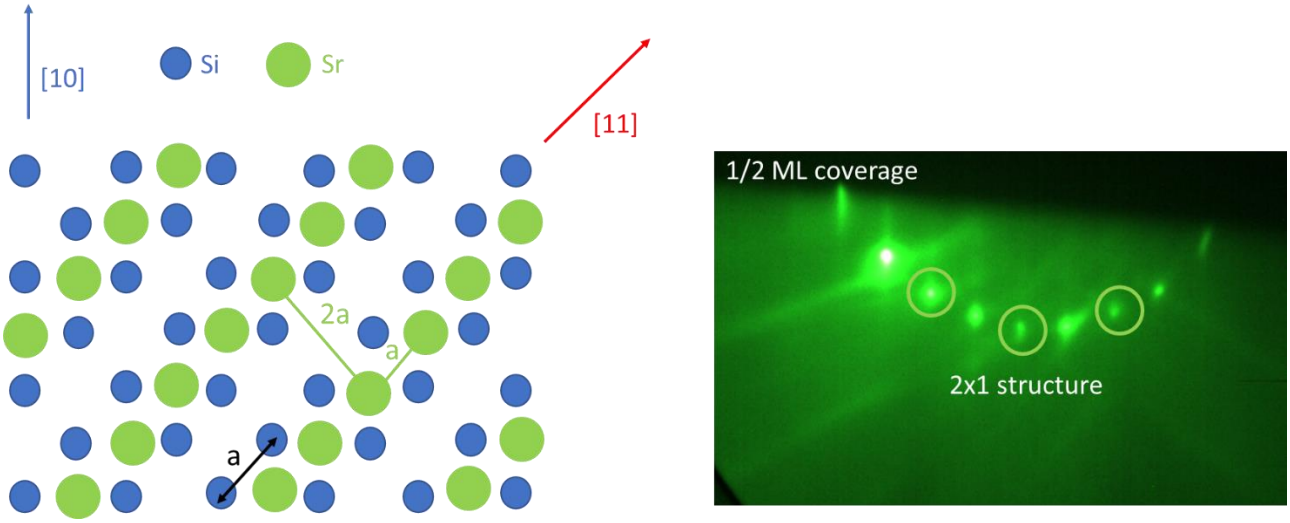

Figure 3.12: At ½ ML Sr coverage a 2x1 structure forms.

The wafer is cooled to room temperature and an additional 0.5 ML of Sr is deposited, resulting in a (2x1) to (3x1) reconstruction. This result is unexpected since it would seem reasonable for the additional 0.5 ML of Sr atoms to fill in the available empty rows creating a (1x1) surface structure as shown in Figure 3.13. However, what is observed is that for 1 ML Sr coverage there is a (3x1) reconstruction [3.16], [3.17]. It has been suggested that the (3x1)

structure forms due to the way 1 ML of Sr atoms interact with the underlying substrate which can allow rows of dimers to form underneath the Sr layer. DFT calculations by A. A. Demkov and X. Zhang show that the most stable structure for 1 ML Sr coverage has a row of Si dimers every third row, giving the observed (3x1) surface structure [3.18]. The (3x1) structure seen for 1 ML Sr coverage becomes a (1x1) structure when oxidized [3.17].

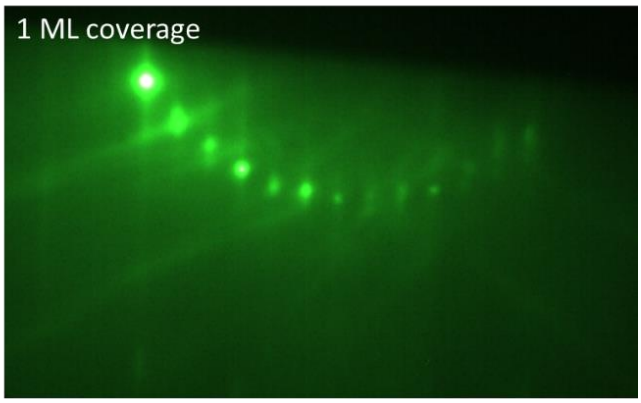

Figure 3.13: 1 ML Sr coverage results in a (3x1) structure.

The wafer is then exposed to oxygen for ~15 s at ~2.5×10^{-7} Torr O_2 partial pressure to oxidize the Sr metal followed by the deposition of another 0.5 ML SrO at room temperature. 1.5 ML of Ti and Sr are then co-deposited in an oxygen background, followed by an additional 0.5 ML of TiO_2. There is now a total of 3 ML of SrO and 2 ML of TiO_2 on the wafer as shown in Figure 3.14.

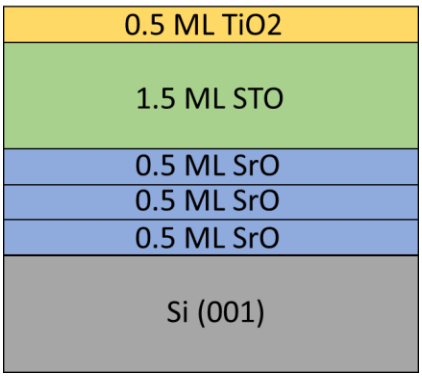

Figure 3.14: Deposited layers for a 2.5 UC thick STO film before crystallization.

To crystallize the film as 2.5 u.c. $SrTiO_3$, the wafer is heated to 580 °C and left for 2 min. Typical film crystallization temperatures are ~430 °C - ~500 °C with lower crystallization temperatures indicating better film crystallinity and typically leads to better quality films when subsequent layers are deposited. The crystallization of 2.5 u.c. STO/Si(100) is summarized in Figure 3.15.

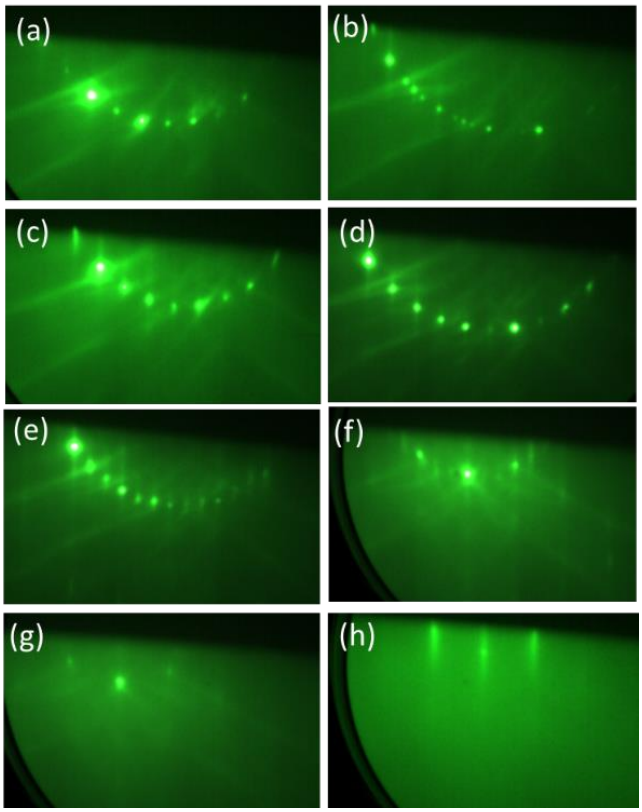

Figure 3.15: (a) Clean Si at 580 °C. (b) 1/6 ML Sr coverage at 660 °C. (c) ½ ML Sr coverage at 660 °C. (d) ½ ML Sr coverage at room temperature. (e) 1 ML Sr coverage at room temperature. (f) 1 ML SrO coverage at room temperature. (g) 1 ½ ML SrO coverage at room temperature. (h) 2.5 u.c STO at 580 °C.

For a 12 nm thick $SrTiO_3$ film, the wafer is cooled from 580 °C to 300 °C and 4 u.c. of STO are deposited at 300 °C. The lower growth temperature helps to prevent the formation of SiO_2

at the STO/Si interface which happens much faster at higher temperatures [3.19]. We find that 6.5 u.c. STO is sufficiently thick to stop SiO_2 formation when additional layers are deposited at higher temperature as observed in STEM images of the heterojunctions as shown in Figure 3.16. Additional layers are co-deposited at 580 °C until a thickness of 12 nm is reached.

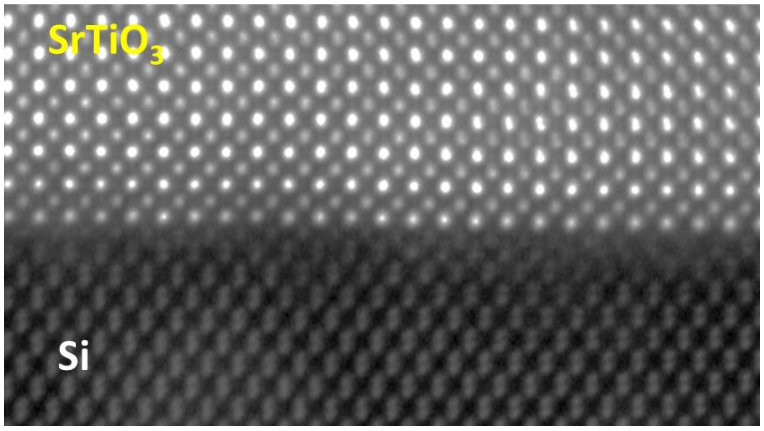

Figure 3.16: STEM of 12 nm STO/Si(100) reveals an atomically abrupt interface with no interfacial SiO_x formation.

Chapter 4: Characterization techniques

4-1 Electrical transport

4-1.1 Van der Pauw

The simplest way to measure the resistance of a sample is to pass a current (I) through it and measure the voltage drop (V) parallel to the direction of current flow. The resistance, R, is then calculated from Ohm's Law.

$$V = IR$$

While this can be helpful for measuring samples that are very resistive, it can be troublesome for low resistance samples because it will include contributions from both the contact resistance and the potential drop across the wires. To eliminate these contributions a 4-wire technique is typically used where one set of wires provides the current density through the sample while the other set of wires measures the potential drop across it as shown in Figure 4.1.

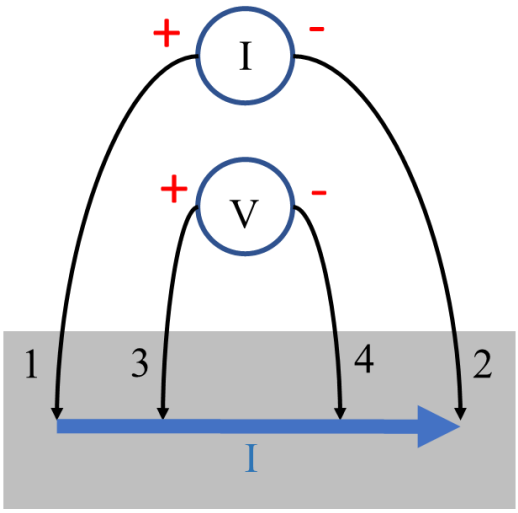

Figure 4.1: 4-point resistance measurement wiring diagram. An electrical current is supplied through the two outer wires labeled 1 and 2. Another set of wires labeled 3 and 4 are used to measure the potential drop across a portion of the sample.

While the 4-point measurement technique is very useful, it does require that the 4 electrical contacts be made in a straight line and that the distance between contacts is much larger than the film thickness. A generalization of the four-point technique was published by L. J. van der Pauw in 1958 [4.1].

The Van der Pauw technique is a widely used measurement technique that allows for electrical transport properties to be measured for arbitrarily shaped samples if the electrical contacts are small and located on the edge of the sample, there are no holes in the sample and the sample does not vary in thickness. Typical contact arrangements for the van der Pauw method are shown in Figure 4.2.

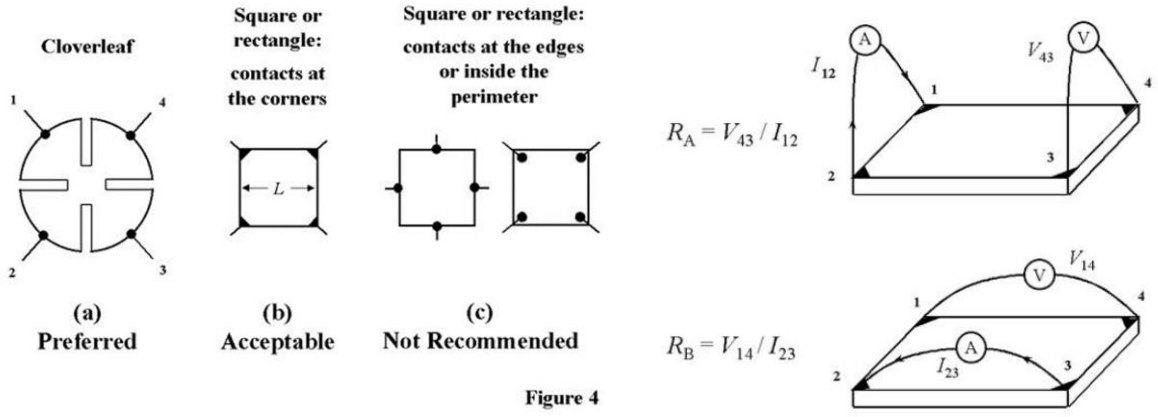

Figure 4.2: Correct and incorrect wiring arrangements for use in the van der Pauw method are shown on the left. Wiring arrangement for the measurement of R_A and R_B used to calculate the sample sheet resistance, R_s [4.2].

While the van der Pauw method works for arbitrarily shaped samples, we typically use 5x5 mm^2 samples that are either cleaved from the wafer or diced depending on the wafer thickness (thick wafers must be diced). Samples are mounted to a *puck* using Kapton tape (which is compatible with both high and low temperatures) and Al wires are wedge-bonded using a Westbond 7476E-79 wire bonder as shown in Figure 4.3.

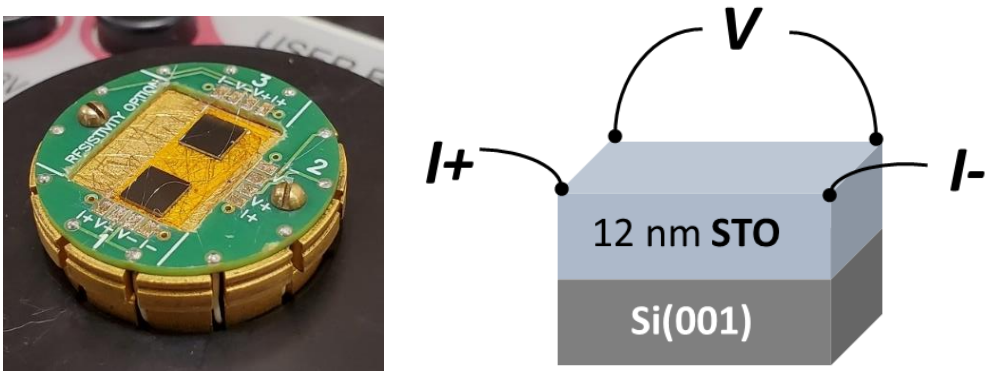

Figure 4.3: (Left) PPMS puck with two samples mounted and wired using the arrangement shown on the right.

Resistance measurements are carried out using two Keithley systems, a Keithley 2400 Sourcemeter to provide source and sense functions, and a Keithley 2700 Multimeter with a Keithley 7709 Matrix Module to multiplex the source and sense functions of the Keithley 2400 to the appropriate sample leads for measurements using the van der Pauw geometry. For a typical sheet resistance measurement this requires a total of eight measurements. Using the wiring convention of Figure 4.3, four sets of measurements are made.

$$R_{21,34} = V_{34}/I_{21} \qquad R_{12,43} = V_{43}/I_{12}$$

$$R_{32,41} = V_{41}/I_{32} \qquad R_{23,14} = V_{14}/I_{23}$$

$$R_{43,12} = V_{12}/I_{43} \qquad R_{34,21} = V_{21}/I_{34}$$

$$R_{14,23} = V_{23}/I_{14} \qquad R_{41,32} = V_{32}/I_{41}$$

Measurement consistency requires that each measurement must give the same result with the polarity of the wires reversed.

$$R_{21,34} = R_{12,43}$$

$$R_{32,41} = R_{23,14}$$
$$R_{43,12} = R_{34,21}$$
$$R_{14,23} = R_{41,32}$$

These eight measurements are used to calculate the two *characteristic resistances*, R_A and R_B.

$$R_A = (R_{21,34} + R_{12,43} + R_{43,12} + R_{34,21})/4$$
$$R_B = (R_{32,41} + R_{23,14} + R_{14,23} + R_{41,32})/4$$

The van der Pauw equation is then solved to determine the sheet resistance, R_s.

$$\exp(-\pi R_A/R_S) + \exp(-\pi R_B/R_S) = 1$$

This measurement is repeated over the temperature range of 400 K – 4 K every 3 K with a temperature ramp rate of 3 K/min. Higher temperature ramp rates often cause samples to peel up from the Kapton tape causing the samples to lose thermal contact with the puck or electrical contacts to break loose from the sample or puck.

4-1.2 Hall Measurements

When an electric current passes through a material in the presence of a perpendicular magnetic field the charges will experience a force from both the electric field and magnetic field, the Lorentz force.

$$\boldsymbol{F} = -q(\mathbf{E} + \mathbf{v} \times \mathbf{B})$$

The resulting voltage drop that builds up perpendicular to the direction of electric current is known as the *Hall voltage*, V_H. Measurements of this voltage allow for the

determination of both the sign of charge carriers and the free charge density present in the material which are related by the equation below, where n_s is the sheet carrier density, I is the current, B is the magnetic field, q is the elementary charge and V_H is the Hall voltage.

$$n_s = \frac{IB}{q|V_H|}$$

The carrier mobility, μ, is given by:

$$\mu = \frac{1}{qn_sR_s}$$

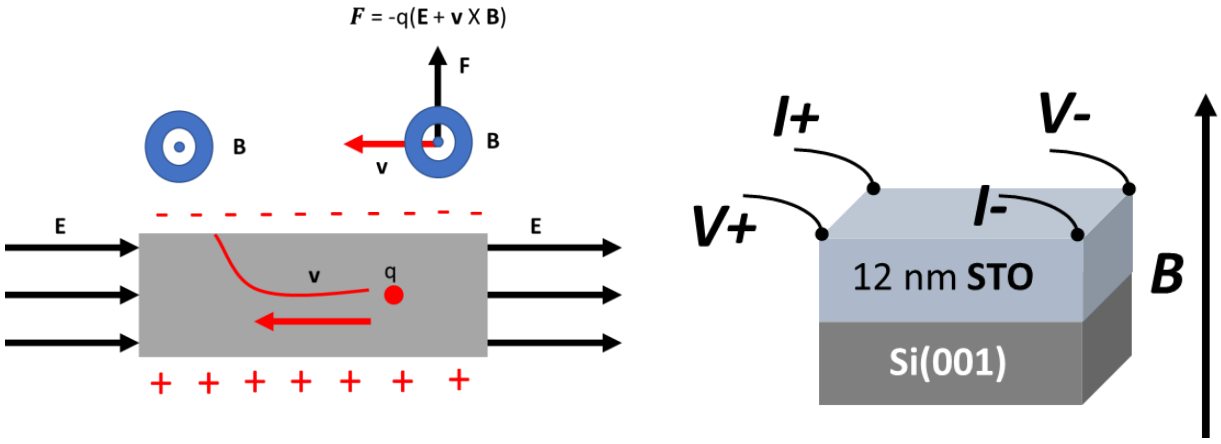

Figure 4.4: (a) Schematic of the Hall effect. (b) Wiring configuration for Hall measurements.

Measurements of the Hall voltage are done in a similar way as for the sheet resistance except a current is supplied diagonally across the sample and the voltage measured perpendicular to it. As Hall voltages can be very small, excitation currents must be chosen to be large enough to produce voltages that are large enough to measure accurately, typically a few hundred mV is sufficient and excitation currents are typically chosen to match that used for sheet resistance measurements. Since small variations in wiring placements can result in large offset voltages during Hall voltage measurements, it is necessary to take two measurements, one with a positively directed magnetic field and one with a negatively directed magnetic field.

Using the same corner labels as in Figure 4.4, Hall measurements require the following voltages to be measured for each magnetic field strength:

$$V_{13P}, V_{31P}, V_{24P}, V_{42P}$$

V_{13P} represents the voltage measured between terminals 2 and 4 with current being supplied from terminals 1 and 3 with the magnetic field directed in the positive direction. The magnetic field is varied between +8 T to – 8 T every 0.25 T allowing for removal of the offset voltage by subtracting voltages from equivalent magnitude magnetic fields on either side of zero field. The voltages measured for negatively directed magnetic field are denoted as:

$$V_{13N}, V_{31N}, V_{24N}, V_{42N}$$

The difference in positive and negative field voltages is then calculated as:

$$V_C = V_{24P} - V_{24N}$$

$$V_D = V_{42P} - V_{42N}$$

$$V_E = V_{13P} - V_{13N}$$

$$V_D = V_{31P} - V_{31N}$$

The subscripts C, D, E and F are don't have any special significance as the Hall voltage is calculated from all four of these measurements as a sum. The Hall voltage is calculated as:

$$V_H = \frac{(V_C + V_D + V_E + V_F)}{8}$$

The factor of 8 accounts for the 8 separate measurements taken, with the Hall voltage being the average of them.

The polarity of V_H gives information on the type of carriers that dominates the conduction. If $V_H > 0$, the sample is p-type and if $V_H < 0$, the sample is n-type. The Hall resistance, R_{xy} is then calculated from Ohm's law as the ratio of the Hall voltage, V_H and the excitation current, I.

$$R_{xy} = \frac{V_H}{I}$$

The sheet carrier density is then calculated from a linear fit of R_{xy} vs. B:

$$\frac{V_H}{I} = R_{xy} = \frac{1}{qn_s} * B$$

The slope of the linear fit is then used to calculate n_s:

$$n_s = \frac{1}{q * slope}$$

The mobility is then calculated using the zero-field sheet resistance, R_s, measured at that temperature using the van der Pauw method. While this holds true for bulk samples, it is necessary to consider multiple channels of conduction for heterojunctions as discussed below, particularly if R_{xy} is non-linear.

4-1.3 Fitting R_{xy} to 2- and 3-carrier models

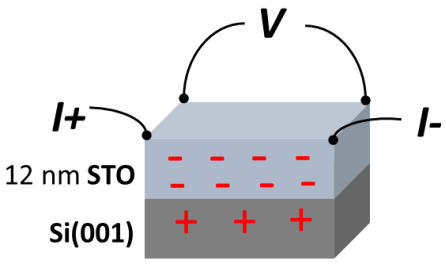

Figure 4.5: 2-channel conduction with different carrier types and densities. Fitting non-linear R_{xy} curves requires the use of a 2- or 3-carrier model.

When the Hall resistance, R_{xy} is nonlinear, it must be assumed that there are multiple channels of conduction which contribute to the total Hall resistance [4.3]. For two channels of conduction, the Hall resistance R_{xy} is given by:

$$R_{xy} = \frac{B}{q}\frac{(\mu_1{}^2 n_1 + \mu_2{}^2 n_2) + (\mu_1\mu_2 B)^2(n_1 + n_2)}{(\mu_1 n_1 + \mu_2 n_2)^2 + (\mu_1\mu_2 B)^2(n_1 + n_2)^2}$$

Where B is the magnetic field, q is the elementary charge (make appendix with defined values), n_1, n_2, μ_1 and μ_2 are the carrier densities and carrier mobilities of the two conducting channels. The conducting channels are typically chosen to be the mobile electrons in the SrTiO3 (oxygen vacancies act as electron donors in STO) and the holes in the inversion layer that forms very close to the Si interface (discussed later). In this case, $n_1 = n_{e,STO}$ (STO electron density), $\mu_1 = \mu_{STO}$ (STO electron mobility), $n_2 = n_{h,Si}$ (Si hole density) and $\mu_2 = \mu_{h,Si}$ (Si hole mobility). However, in some heterojunctions we find that there is no hole gas formation in the near-interfacial region and that the two-carrier model describes the mobile electrons in the STO and mobile electrons in the Si (oxygen impurities act as electron donors in Si). Additionally, we find that depending on the substrate used, there may be thermally excited electrons in the Si, typically near 400 K. When these intrinsic carriers start to increase enough to have an effect on the R_{xy} data, a 3-carrier model must be used with $n_3 = n_{e,Si}$ and $\mu_3 = \mu_{e,Si}$.

$$R_{xy} = \frac{B}{q}\left[\frac{(n_1\mu_1{}^2 + n_2\mu_2{}^2 + n_3\mu_3{}^2) + (\mu_1\mu_2 B)^2(n_1 + n_2) + (\mu_1\mu_3 B)^2(n_1 + n_3) + (\mu_2\mu_3 B)^2(n_2 + n_3) + (\mu_1\mu_2\mu_3 B^2)^2(n_1 + n_2 + n_3)}{(n_1\mu_1 + n_2\mu_2 + n_3\mu_3)^2 + (\mu_1\mu_2\mu_3 B^2)^2(n_1 + n_2 + n_3)^2 + (\mu_1\mu_2 B)^2(n_1 + n_2)^2 + (\mu_1\mu_3 B)^2(n_1 + n_3)^2 + (\mu_2\mu_3 B)^2(n_2 + n_3)^2 + (\mu_1\mu_2\mu_3 B^2)(2n_1n_2\mu_3 + 2n_2n_3\mu_1 + 2n_3n_1\mu_2)}\right]$$

Fits to this model can be obtained by fitting R_{xy} vs. B using a non-linear curve fitting algorithm. In this work, Origin was used for non-linear fitting using the Levenberg-Marquardt algorithm (LMA).

Since there are four parameters the fits are non-unique unless further constrained. We constrain the zero field Hall resistance to be equal to the sheet resistance (longitudinal resistance) of the sample taken using the Van der Pauw technique (as discussed in section 4-1.1) at the same temperature the Hall resistance was measured.

$$R_s = R_{xx}(0) = \frac{1}{e(n_1\mu_1 + n_2\mu_2)}$$

Since Origin's non-linear curve fitting does not support non-linear constraints to be used, a separate constraint calculator is set up in an Excel spreadsheet to compare R_s and $R_{xx}(0)$. The fits are then done iteratively by first fitting the R_{xy} curve in Origin to obtain the parameters n_1, n_2, μ_1 and μ_2. These parameters are fed into the constrain calculator in Excel to calculate $R_{xx}(0)$. Depending on if $R_{xx}(0)$ is less than or greater than R_s, the parameters can then be adjusted in Origin to force $R_{xx}(0)$ to more closely match R_s. There is often a great deal of going back and forth between the two to adjust parameters and calculate the constraint until a good match (typically within 10 Ω/sq.) is reached along with a good fit to R_{xy} since it is possible to get a poor fit to the data but match the constraint. Unfortunately, it seems that a fully automated algorithm including non-linear constraints would be difficult to achieve since the shape (curvature) of R_{xy} is very strongly dependent on small changes in the parameters, even with the number of LMA iterations increased to the maximum and the best tolerance available in Origin.

We find that even though we have constrained $R_{xx}(0) = R_s$ at the temperature R_{xy} is measured at, fits to R_{xy} are not unique. To rule out non-physical values of the mobilities and sheet densities, we additionally constrain the mobilities to be close to those reported for bulk Si and STO films. We note that mobilities of uniformly doped bulk crystals can differ significantly from non-uniformly doped heterojunctions, due to the spatial confinement of dopants and carriers in the heterojunction, and the ability to spatially separate itinerant charge carriers from their ionized donor or acceptor atoms [4.4].

Carrier mobilities in both semiconductors and oxides are limited by scattering which is a function of both the carrier density (ionized impurity scattering) and temperature (phonon scattering). Since ionized dopants in Si act as scattering sites, higher doped carrier densities give lower carrier mobilities. Additionally, at higher temperatures, there is increased phonon scattering which acts to decrease carrier mobility. A combination of ionized impurity and phonon scattering contributes to the total mobility of carriers; therefore, we additionally

constrain the carrier mobility in Si to match that of values extracted from Figure 2.3 [4.5]. We also constrain the carrier mobilities in STO to be lower than what has been reported for STO films grown using hybrid MBE, which allows for films with lower defect densities due to near perfect cation stoichiometry [4.6].

The fitting procedure described here is used throughout this work to extract carrier densities and mobilities of MBE grown STO/Si heterojunctions.

4.2 Hard x-ray photoelectron spectroscopy (HAXPES)

X-ray photoelectron spectroscopy (XPS) is a powerful technique that probes the chemical composition as well as details about the chemical environment of samples such as how elements are bonded together by measuring the binding energy, E_B, of core-level electrons from a sample. X-rays impinging on a sample surface will knock out electrons from the sample by way of the *photoelectric effect*. The kinetic energy, E_k, of the emitted electrons, or *photoelectrons*, is measured using an energy analyzer. If the x-ray source is monochromatic, then the photon energy, $E_{photon} = h\nu$, is a known quantity and can be regarded as a constant. Typical XPS sources are Al k_α x-rays with energy 1486.7 eV.

Conservation of energy requires that the binding energy of an electron emitted from a sample to be equal to the photon energy minus the work function of the sample and kinetic energy of the emitted electron as shown in Figure 4.6.

$$E_B = E_{photon} - (E_{kinetic} + \phi)$$

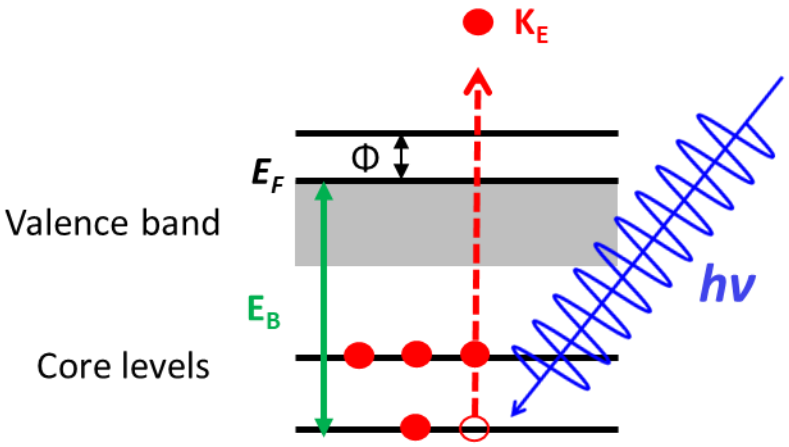

Figure 4.6: Schematic of the photoemission process. An incoming photon can knock out a core-level electron which is ejected from the sample with a kinetic energy which is measured using an energy analyzer.

X-rays with energy 1.487 keV, which are in the *soft x-ray* range, can penetrate up to a few microns into a sample, however, photoelectrons leaving the sample can only escape from ~1-2 nm from the sample surface due to scattering. This distance, λ, is known as the *attenuation length* and is material dependent since scattering event probabilities are different. This means that conventional XPS using Al k_α x-rays is highly surface sensitive, and is therefore used to measure properties of materials very near sample surfaces.

However, electrons from deeper into a sample can have their binding energies shifted and line shapes changed due to the electrostatic potential profile in the sample. Since our work focuses on thin film heterojunctions, it is desirable to have an XPS technique that can probe further into a sample so that information about electric fields can be probed. To do this, we make use of *hard x-rays* which have photon energies from ~5-10 keV using a technique called *hard x-ray photoelectron spectroscopy* (HAXPES). This is done as part of a collaborative effort between groups at PNNL and Diamond Light Source. HAXPES measurements are carried out by

Judith Gabel and Tien-Lin Lee at Beamline I09 at Diamond Light Source, and analysis and fitting of the spectra by Scott Chambers and Peter Sushko at Pacific Northwest National Lab.

An illustration of how electric fields inside of a crystal can be probed using the HAXPES technique is shown in Figure 4.7.

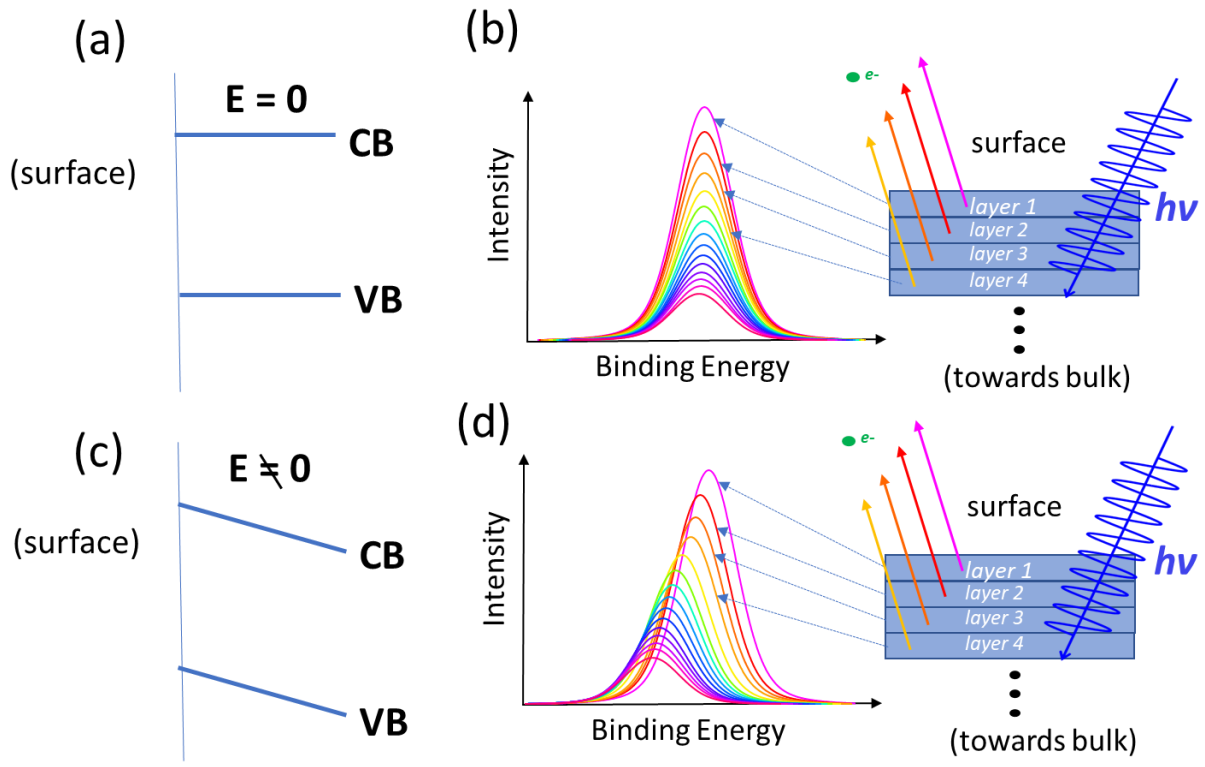

Figure 4.7: (a) Energy bands with no electric field. (b) Core-level photoelectron spectra are sums of all photoelectrons from each layer within the probe depth. With no built-in fields, core-level spectra are symmetric. (c) Energy bands will bend in the presence of an electric field. (d) Core-level spectra from samples with built-in fields will show asymmetric broadening due to binding energy shifts associated with the field.

With no electric field in the material, the bands will be flat because no field means there is no gradient in potential as shown in Figure 4.7 (a).

$$E = -\nabla \mathrm{V} = 0$$

Figure 4.7 (b) shows what a core-level line shape would like if it was built up of photoelectrons emitted from a sample with flat bands. Since electrons deeper into the sample will have a higher probability of scattering, the intensity of emitted electrons from deeper in the sample will be smaller than the intensity of electrons emitted from close to the surface. The core level line shape is made up of the sum of all electrons measured such that each "layer" will contribute some amount of the total intensity, with decreasing intensity from layers deeper in the sample.

Figure 4.7 (c) shows what the presence of an electric field does to the energy bands. Since there will be a gradient in the potential profile, the energy bands will no longer be flat which is called *band-bending*. Photoemitted electrons deeper in the sample now need to overcome the additional potential to leave the sample which modifies their kinetic energy.

$$E_k = E_{photon} - (E_B - \phi - q\Delta \mathrm{V})$$

This can be thought of as a shift in the binding energy and such that each layers deeper in the sample will have their binding energies shifted the most. When all layer intensities are summed up the result is that the core-level line shape is broadened as shown in Figure 4.7 (d). Thus, the core-level line shapes carry information about the presence of electric fields in a sample. Fits to the spectra allow for determination the band-edge profiles across a heterojunction.

Before spectra can be fit, the binding energy scale must be calibrated to a standard. In this case, the scale was calibrated using Au 4f core levels and the Au Fermi edge. This calibration shifts sample spectra by some constant value in binding energy such that the binding energy at the Fermi level is zero. The result is that binding energy spectra are measured relative to the Fermi level.

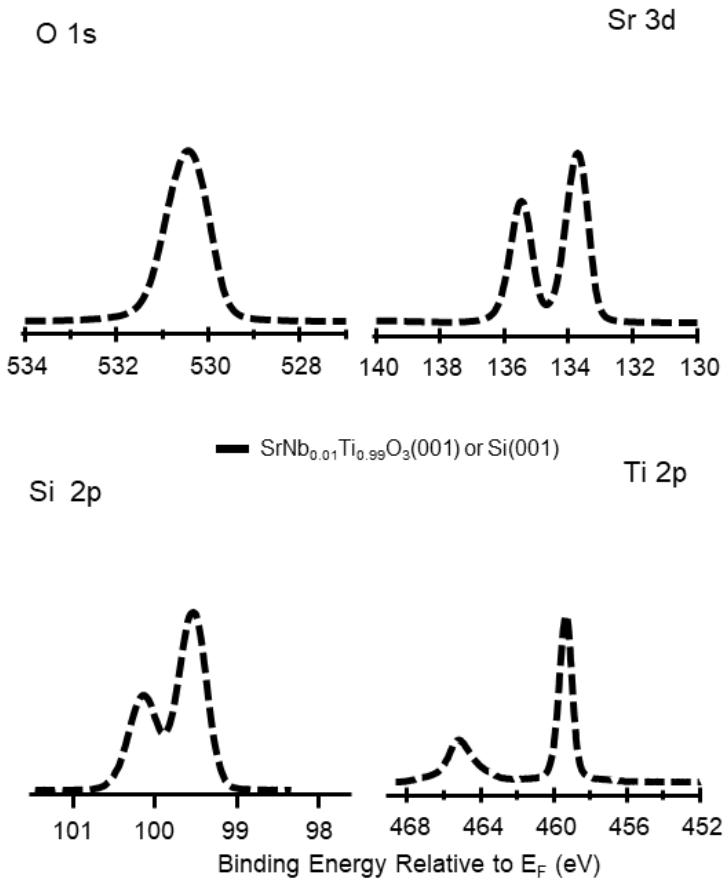

Figure 4.8: O 1s, Sr 3d, Ti 2p and Si 2p core-level spectra obtained from bulk $SrNb_{0.01}Ti_{0.99}O_3$ and Si reference samples. Heterojunction spectra are fit using reference spectra [4.7].

Fitting the spectra requires reference spectra from bulk materials or thick films that are free of any built-in potentials due to charge transfer. Figure X shows reference spectra of O 1s, Sr 3d, Si 2p and Ti 2p photoelectron spectra taken from a clean Si(100) and single crystal $SrNb_{0.01}Ti_{0.99}O_3$(100) (SNTO). Nb doped STO is used to prevent charging during HAXPES measurements which can result in binding energy shifts that are not representative of the sample itself. The choice of spectra used is material dependent. Good spectra to use are ones with sharp peaks and high intensities with no complex shapes so that binding energies can be determined accurately.

The fits themselves are done by assigning each layer withing the probe depth (determined by the x-ray energy used) of the material a reference spectrum (Si 2p or Ti 2p) attenuated by a damping factor, exp(-z/λ), where z is the depth of the layer and λ is the attenuation length. The binding energy for each layer is then allowed to vary over all possible binding energies. A trial spectrum is then created from the sum of all layers and compared to the experimental spectra. Optimization of the binding energies is done by minimizing a cost function

$$\chi = \sqrt{\frac{1}{n}\sum_{i=1}^{n}[I_{exp}(\varepsilon_i) - I_{sim}(\varepsilon_i)]^2 + p\sum_{j=1}^{m}[\varepsilon_{max}^{k}(j) - \varepsilon_{max}^{k}(j+1)]^2}$$

The first term is the RMS deviation which shows how good the fit is, while the second term is used to minimize potential gradients with depth so that a monotonic fit is achieved. The fitting process is then iterated until χ is minimized. Fits for a 12 nm STO/Si-CZ heterojunction are shown in Figure 4.9.

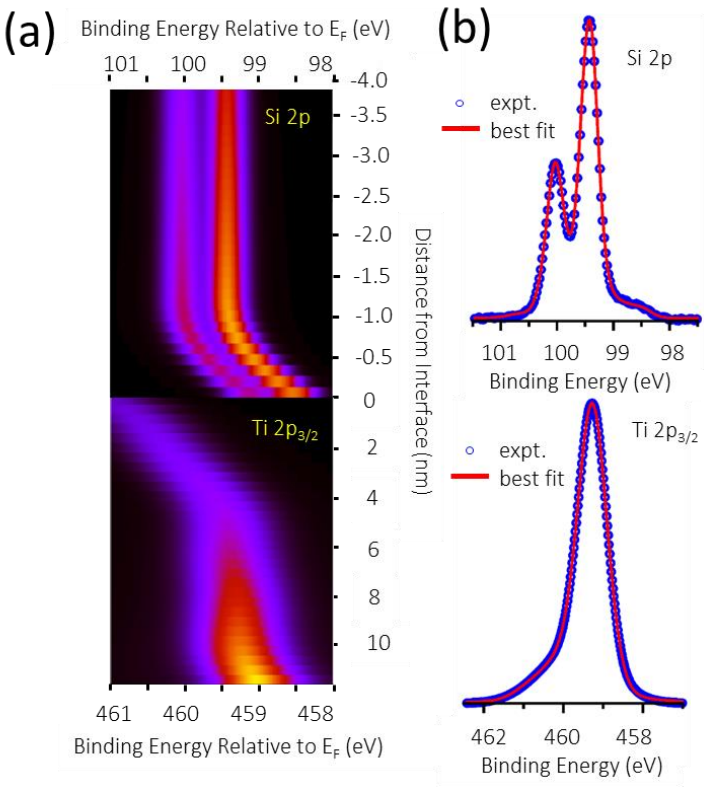

Figure 4.9: (a) Extracted band edge profiles for a 12 nm STO/Si-CZ heterojunction. (b) Si 2p and Ti $2p_{3/2}$ core-level spectra for a 12 nm STO/Si-CZ heterojunction. Also shown are fits to the core-level spectra [4.8].

The binding energies for each layer are then converted to valence band edge profiles using the measured difference in core levels and VBM's of the reference materials using the equation:

$$E_V(z) = E_{CL}(z) - (E_{CL} - E_V)_{ref}$$

$E_{CL}(z)$ is the depth dependent core-level binding energy relative to the Fermi level extracted from fits to the core-level spectra and $(E_{CL} - E_V)_{ref}$ is the difference in core-level and VBM of the reference spectra. The conduction band edge profile is found by taking the difference in $E_v(z)$ and the bulk band gap, E_g:

$$E_C(z) = E_V(z) - E_g$$

The spectra in Figure 4.9 are taken from our previous work [4.8] and are used again in our study discussed in Chapter 5.

Band offsets can also be determined from the XPS spectra by a method developed by Kraut et al. [4.9], [4.10]. A schematic of a general band diagram is shown in Figure 4.10. By inspection, the valence band offset can be determined at the heterojunction.

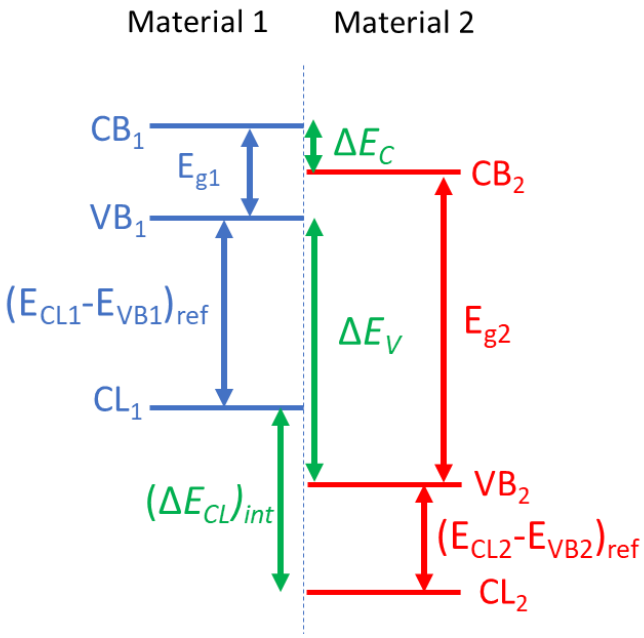

Figure 4.10: Band offset determination from XPS spectra.

The valence band offsets are calculated as:

$$\Delta E_{VB} = (E_{CL1} - E_{VB1})_{ref} - (E_{CL2} - E_{VB2})_{ref} + (\Delta E_{CL})_{int}$$

Note that the signs must be considered and depend on the relative energies of core levels and valence band edges. The CB offsets are then calculated using the band gaps.

$$\Delta E_{CB} = \Delta E_{VB} + (E_{g1} - E_{g2})$$

HAXPES is used in both Chapter 5 and 6 of this work to study STO/Si heterojunction charge transfer and band bending.

Chapter 5: Tuning Band Alignment at a Semiconductor-Crystalline Oxide Heterojunction via Electrostatic Modulation of the Interfacial Dipole

5-1 Introduction

Charge transfer across semiconductor heterojunctions and the electric fields that arise therefrom underpin the functionality of virtually all device technologies. One example of this is the p-n junction, where a p-type doped semiconductor is brought into contact with an n-type doped semiconductor. Electrons (holes) from the n-type (p-type) region will diffuse across the interface, recombining with the holes (electrons) on the other side of the interface. This process will leave behind the ionized dopant atom cores on either side of the junction and this region will be free of mobile charge carriers and is known as the *depletion region*. The leftover donor and acceptor cores in the depletion region are known as *space charge* and there is an electric field present through this region. We know from electrostatics that the field, **E**, will give a gradient in the potential profile through the depletion region and is manifested in the energy-band diagram as *band bending*. An illustration of the p-n junction space charge and band bending is shown in Figure 5.1. The p-n junction is a basic building block of many device technologies including diodes, transistors, solar cells and light-emitting diodes (LEDs) [5.1]. Functionality of devices like the p-n junction diode are determined by the band alignment at the junction interface which determines the direction of charge transfer across the interface.

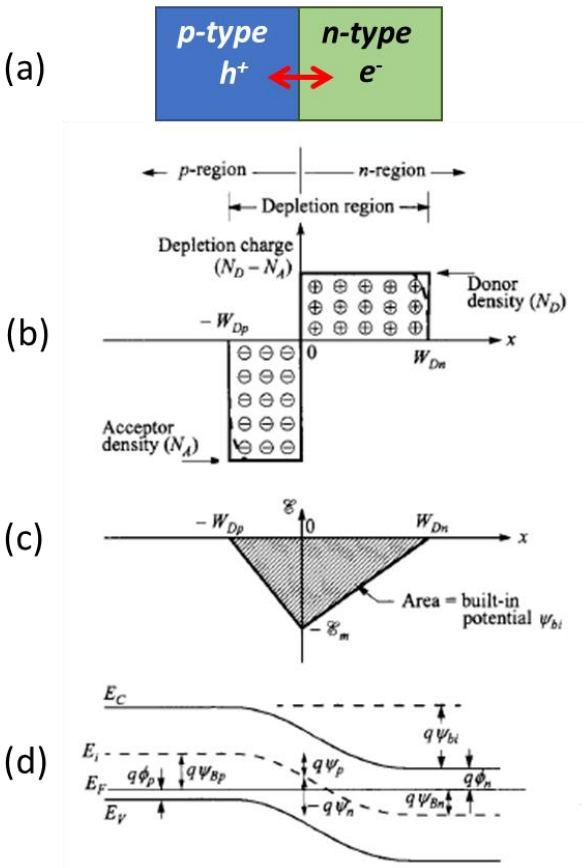

Figure 5.1: (a) Schematic of a p-n junction device. (b) p-n junction space-charge distribution at equilibrium. (c) Electric field distribution resulting from space charge formation in a p-n junction. (d) Energy band diagram of a p-n junction. (b), (c) and (d) taken from [5.1].

Hybrid heterojunctions formed between semiconductors and crystalline complex oxides offer novel functionality due to their mixed covalent and ionic characteristics. Heterojunctions formed between covalent semiconductors and ionic complex oxides provide an interesting setting to study charge transfer and built-in fields because they exhibit discontinuities in composition and the bonding transitions from being covalent to ionic across the heterojunction interface. Band alignment is determined by both bulk properties (electron affinities, χ) and the distribution of charge across the interface due to bonding.

The perovskite oxide $SrTiO_3$ is very well lattice matched to Si(100) if rotated 45° from the Si(100) surface, with a lattice mismatch of 1.68 %. The STO lattice constant is larger than that of the rotated Si lattice such that STO films grown epitaxially on Si are compressively

strained. Advances in growth techniques [5.2] allow for the growth of high quality epitaxial STO films free of interfacial SiO_x that would inhibit charge transfer across the interface. Inherent to epitaxial $SrTiO_3$/Si interfaces is a built-in dipole that modifies the structure near the interface. The strong electronegativity of oxygen anions in near interface region of the $SrTiO_3$ pulls electrons away from the Si surface which distorts the structure by pulling oxygen anions toward the interface and pushes the metal cations (Sr/Ti) away from the interface as shown in Figure 5.2.

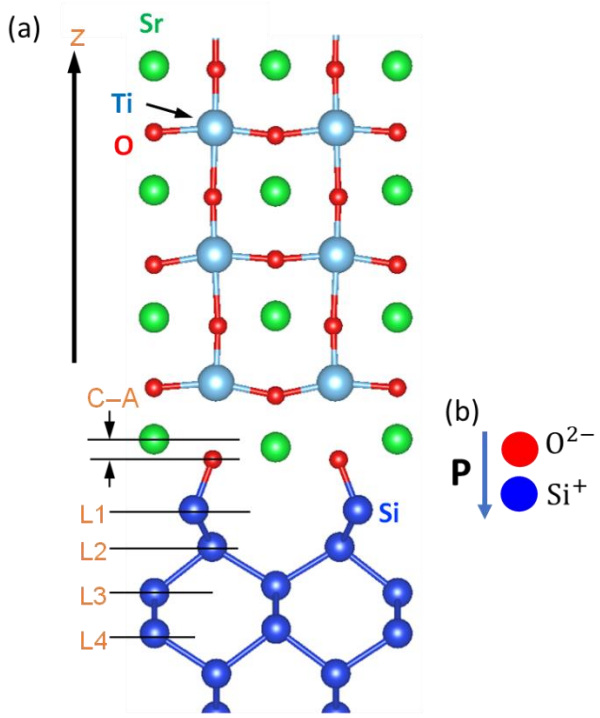

Figure 5.2: (a) DFT structural model of a $SrTiO_3$/Si interface [5.3] C-A displacement produces a polarization at the interface which can be tuned through space charge. DFT modeling of the interface is discussed in section 5-3. (b) Schematic of the $O^{2-}Si^{+}$ interface dipole.

We demonstrate that the interfacial dipole associated with bonding across the $SrTiO_3$/Si heterojunction can be tuned through space charge, thereby enabling the band alignment to be altered via doping. The ability to alter band-alignments at hybrid heterojunctions sets it apart from conventional semiconductor heterojunctions in which band alignment changes via space charge are relatively small. Oxygen impurities in Si act as donors that create space charge by

transferring electrons across the interface into $SrTiO_3$. The space charge induces an electric field that modifies the interfacial dipole, thereby tuning the band alignment from type II to III. The transferred charge, accompanying built-in electric fields, and change in band alignment are manifested in electrical transport and hard x-ray photoelectron spectroscopy measurements. *Ab initio* models reveal the interplay between polarization and band offsets. We find that band offsets can be tuned by modulating the density of space charge across the interface. Modulating the interface dipole to enable electrostatic altering of band alignment opens additional pathways to realize functional behavior in semiconducting hybrid heterojunctions.

5-2 Experiment

We present a comparative study of 12 nm $SrTiO_3$ films grown on Czochralski (CZ) and float-zone (FZ) grown Si(100) wafers grown by oxide molecular beam epitaxy (MBE). Film growth conditions are identical so the only effects that should be seen are due to the difference in wafer properties. Manufacturing CZ Si ingots involves using a seed crystal to pull molten Si contained in a silica crucible. Part of the silica crucible walls are incorporated into the molten Si so wafers grown using this method contain oxygen impurities from the crucible. This process was invented in 1918 by Jan Czochralski. FZ wafers on the other hand are grown using a vertically oriented silicon rod in an inert gas atmosphere or vacuum that is passed through radio-frequency coil which locally melts the Si as it passes through the coil. This process is known as *zone melting* and was developed in 1966 by William Pfann [5.4]. Impurities present in the original silicon rod are incorporated into the molted region and pushed to the end of the rod as it passes through the coil. Since there is no crucible involved in this process there will not be any oxygen impurities present in the finished product.

Additionally, 4 and 8 nm STO films were grown on the same CZ Si(100) wafers as the 12 nm STO/Si-CZ sample to study the film thickness effect on modulating the interface dipole. It is postulated that surface depletion plays a key role in modulating the interfacial dipole and these samples study this effect by bringing the surface-interface distance closer together. Oxygen impurity concentration in the Si is also studied as a function of film thickness. Additional 12 nm

films on grown on doped CZ wafers to study the effect of wafer dopant concentration since oxygen impurities in the CZ Si are another key to modulating the interface dipole through space charge.

STO films are grown in a custom-built MBE chamber operating at a base pressure of ~$3x10^{-10}$ Torr. 2" diagonal, (100) oriented, 300 µm thick wafers are inserted into the chamber and cleaned using an activated oxygen source produced from a radio-frequency source operating at 226 W. 2 ML of Sr metal are deposited on the wafer at 550 °C and heated to 870 °C to form and desorb the native SiO_x layer. A 2x1 reconstruction is observed using RHEED indicating a clean, dimerized Si surface. The wafers are cooled to 660 °C and 0.5 ML of Sr metal is deposited which creates an interfacial layer that prevents Si oxidation and serves as a template for STO growth. An additional 2.5 ML SrO and 2 ML TiO_2 are co-deposited at room temperature and heated to 580 °C to crystallize the film as 2.5 UC STO. An additional 4 UC STO is deposited at 300 °C to prevent Si oxidation which occurs when exposing the wafer to oxygen at high temperature. The wafer is then heated back to 580 °C to deposit additional layers until the desired film thickness is reached. Additional details about the growth of STO/Si(100) can be found in section 3-3. RHEED of both 12 nm STO/Si-CZ and 12 nm STO/Si-FZ heterojunctions along the [10] crystallographic direction is shown in Figure 5.3.

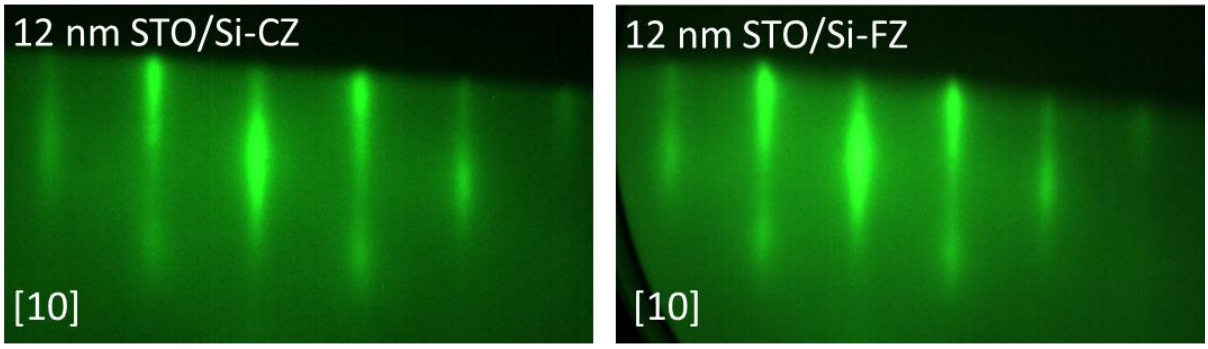

Figure 5.3: RHEED of 12 nm STO/Si-CZ and 12 nm STO/Si-FZ films along the [10] direction showing comparable film quality.

After film growth, wafers are diced (Disco Dad3220) into 5x5 mm^2 pieces and mounted to a Physical Properties Measurement System (PPMS, Quantum Design) puck using Kapton tape. Electrical contacts are created using Al wedge bonding (Westbond) at each corner of the sample. Electrical transport measurements were done using the van der Pauw geometry as described in section 4-1.1 in a Quantum Design DynaCool system. Transport properties were measured as a function of temperature (4-400 K) and applied magnetic field ($\pm$ 7-8 T). Hall resistance data is fitted to a two-carrier model since the Hall resistance, R_{xy}, is non-linear for most temperatures, indicating that there are multiple channels of conduction present in the heterojunction. Fitting details can be found in section 4.1-2.

HAXPES measurements were carried out by Judith Gabel and Tien-Lin Lee at Beamline I09 at Diamond Light Source and analysis and fitting of the spectra by Scott Chambers and Peter Sushko at Pacific Northwest National Lab.

STEM ADF and iDPC imaging was done by Aubrey Penn and James LeBeau. STEM-EELS measurements were done by Demie Kepaptsoglou and Quentin Ramasse at the SuperSTEM facility. Additional STEM imaging and sample preparation for STEM-EELS was done by Steven Spurgeon and Bethany Matthews at PNNL. SIMS data was taken by Zihua Zhu at PNNL. First-principles DFT calculations were done by Peter Sushko at PNNL. Additional details about the equipment used can be found in our publication [5.3].

5-3 Results

Scanning transmission electron microscopy (STEM) images of 12 nm STO/CZ-Si and 12 nm STO/Si-FZ heterojunctions show atomically abrupt interfaces free of SiO_x. Polarization near the interface can be seen in both samples as oxygen atom off centering relative to SrO and TiO_2 lattice planes. Figure 5.4 shows annular dark field (ADF) and integrated differential phase contrast (iDPC) images of both heterojunctions. iDPC imaging allows for imaging of both heavy and light elements simultaneously, revealing the positions of oxygen atoms [5.5]. Enhanced iDPC images shown in Figure X (c) and (d) reveal that the oxygen atoms that are displaced

downward relative to Sr and Ti atoms. Larger scale images show the films are smooth and uniform but with occasional anti-phase boundaries that appear at substrate steps defects and steps as shown in Figure 5.5.

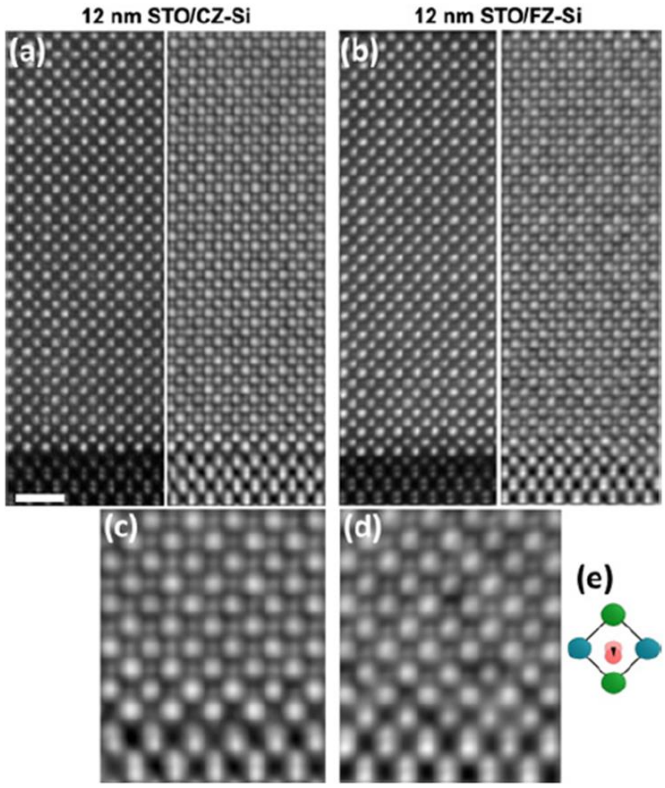

Figure 5.4: ADF and iDPC images of (a) 12 nm STO/Si-CZ and (b) 12 nm STO/Si-FZ heterojunctions. (c) and (d) are magnified iDPC images showing oxygen displacement (e) toward the Si in the near-interface region.

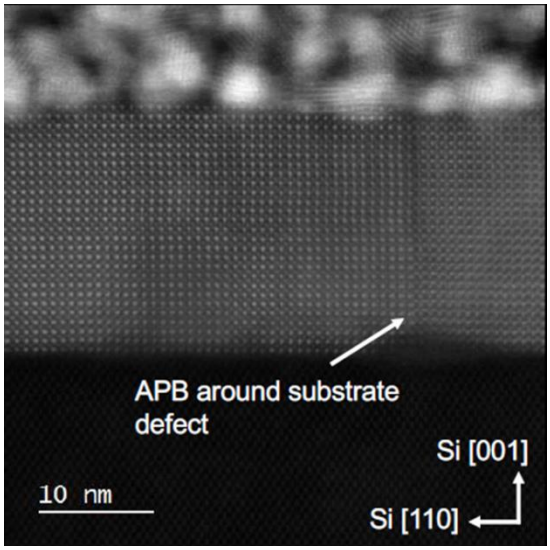

Figure 5.5: HAADF image taken around a substrate defect showing the presence of anti-phase boundaries in the film that can appear at substrate defects and step edges.

In addition to ADF and iDPC STEM imaging (Aubrey Penn and James LeBeau), we sent samples to Demie Kepaptsoglou and Quentin Ramasse at the SuperSTEM facility for atomically resolved EELS measurements. Figure 5.6 (a) and (b) show maps of the Sr $L_{2,3}$ and Si K edges. EELS mapping indicates sharp interfaces with minimal intermixing. Additionally, the first oxide layer is seen to be SrO as expected from the growth method and what has been previously reported [5.2], [5.6]. As discussed later, this also rules out the HAXPES Si 2p low binding energy feature as being due to $TiSi_2$ interfacial bonding. Figure 5.6 (c) and (d) show fine structure mapping of the Ti $L_{2,3}$ edge across the interface for 12 nm STO/Si-CZ and 12 nm STO/Si-FZ samples. In the perovskite structure, ABO_3, the B-site cation gives up its valence electrons to the surrounding oxygen anions such that the B-site atom has charge +4 and the oxygen atoms have charge -2. The B-site cation, in this case Ti, will be bonded to 6 oxygen atoms which form an octahedron. Crystal field theory (CFT) takes into account the effect of the TiO_6 octahedra on the Ti electronic states and splits the five-fold degenerate Ti 3d states into three-fold degenerate t_{2g} and two-fold degenerate e_g energy levels. The splitting of t_{2g} and e_g features in the EELS spectra merge when Ti is in a Ti^{3+} configuration [5.7]. Away from the interface, 12 nm STO/Si-CZ heterojunction exhibits Ti^{4+} character. Splitting of both L_2 and L_3 features is seen from

the 7th layer from the interface all the way to the 4th layer of the interface, with the L_2 intensity and splitting decreasing faster than L_3. On the Si side of the interface, layer 1, a trend toward Ti^{0+} is seen which can be attributed to a high density of electrons transferred from the Si.

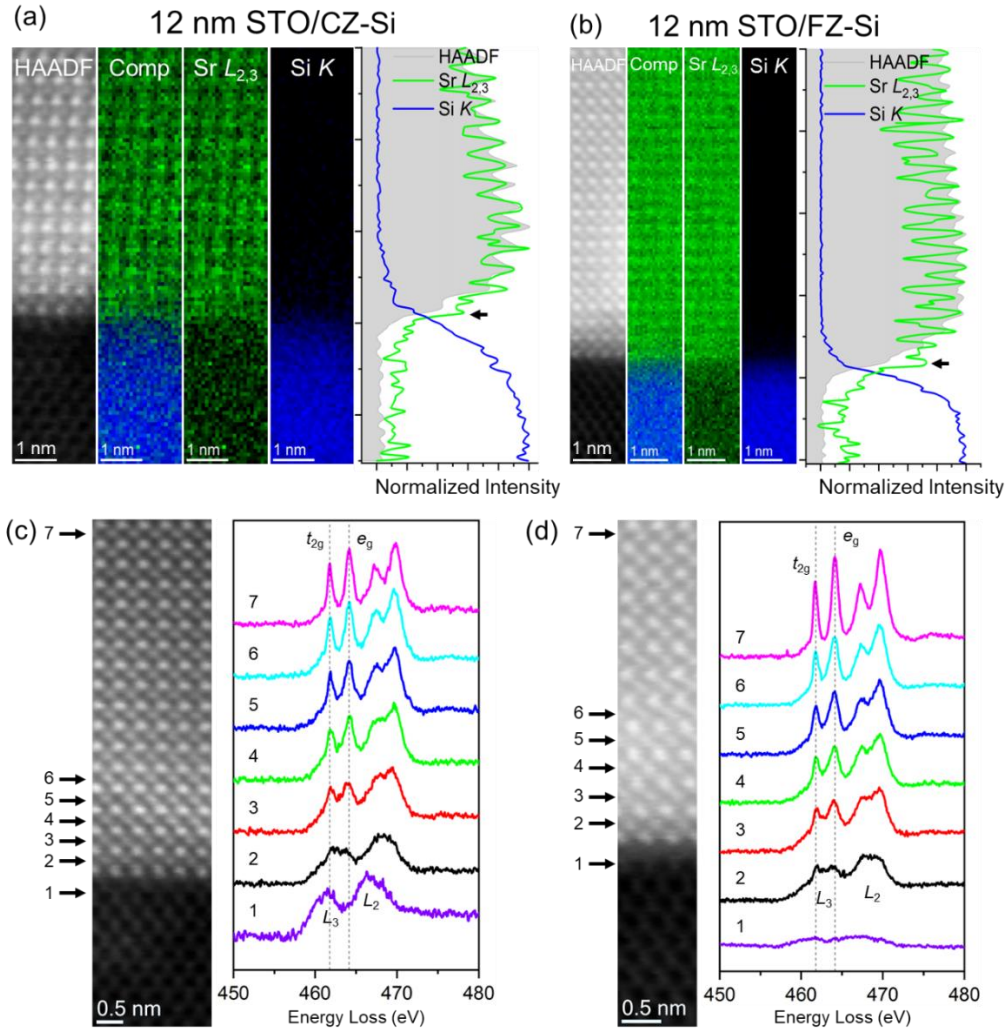

Figure 5.6: (a) and (b) show maps of Sr $L_{2,3}$ and Si K edges for 12 nm STO/Si-CZ and 12 nm STO/Si-FZ heterojunctions. (c) and (d) show fine structure mapping of the Ti $L_{2,3}$ edge across the interface for the 12 nm STO/Si-CZ and 12 nm STO/Si-FZ heterojunctions.

For the 12 nm STO/Si-FZ heterojunction, t_{2g} and e_g splitting is still seen all the way up to layer 2, the closest layer to the interface while the Si side on the interface, layer 1, has almost no Ti signal at all. Further differences in the Ti valence are probed using HAXPES.

Electrical transport measurements using the van der Pauw configuration of a 12 nm STO/Si-CZ heterojunction shows a lower sheet resistance, R_s, throughout the entire temperature range measured (10 K - 400 K) than for 12 nm STO/Si-FZ. The 12 nm STO/Si-FZ heterojunction exhibits non-monotonic behavior in sheet resistance when cooling. From 400 K – 300 K, R_s increases, then decreases from 300 K – 179 K, then increases again below 179 K. For 12 nm STO/Si-CZ samples, R_s decreases from 400 K – 325 K, increases rapidly from 325 K - ~275 K, then increases at a slower rate below 275 K.

As shown in Figure 5.7, for the 12 nm STO/Si-FZ sample, R_{xy} is non-linear and negative throughout the entire temperature range while the 12 nm STO/Si-CZ is positive and non-linear at high temperatures and transitions to being negative and non-linear as the temperature is lowered through the non-monotonic anomaly in R_s.

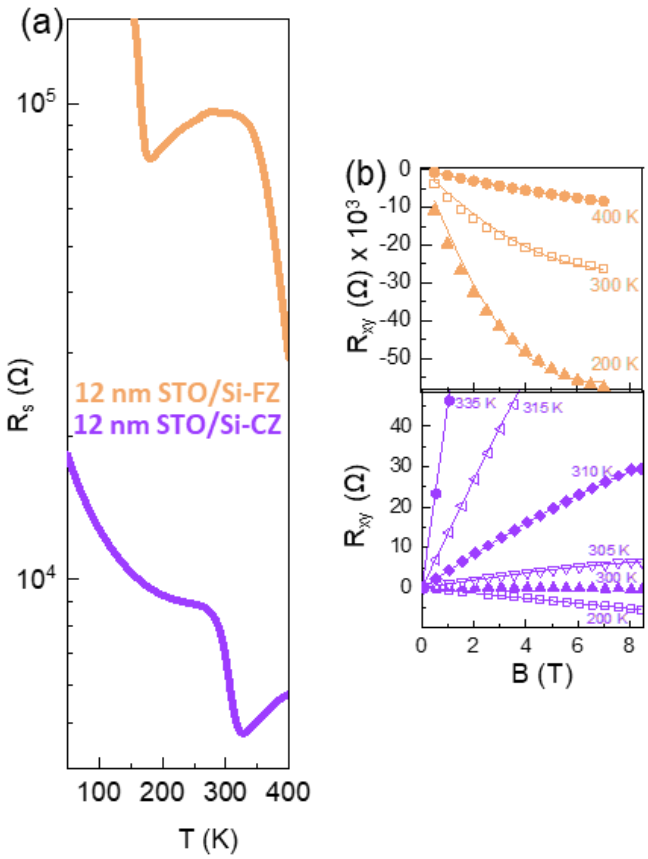

Figure 5.7: (a) R_s for the 12 nm STO/Si-CZ and 12 nm STO/Si-FZ heterojunctions. (b) R_{xy} for the 12 nm STO/Si-CZ and 12 nm STO/Si-FZ heterojunctions. Note that R_{xy} is negative throughout the entire temperature range for the 12 nm STO/Si-FZ heterojunction but R_{xy} for the 12 nm STO/Si-CZ heterojunction shows a crossover in sign from positive to negative near the non-monotonic anomaly in R_s.

Fits to the Hall resistance data indicates that the non-linearity in R_{xy} for the 12 nm STO/Si-FZ arises from 2-channel conduction of electrons in the STO with very low mobilities (~1-2 $cm^2V^{-1}s^{-1}$) and electrons in the Si with much higher mobilities (~1000-3000 $cm^2V^{-1}s^{-1}$). Fits to the Hall resistance data for 12 nm STO/Si-CZ heterojunctions indicate that there is 2-channel conduction consisting of electrons in the STO and holes in the Si. Note that mobilities for electrons and holes at room temperature are typically quoted as 1400 and 450 $cm^2V^{-1}s^{-1}$,

respectively, although changes in carrier density will affect those values [5.1] as shown in Figure 2.3.

Carrier densities and mobilities of electrons in the STO and holes in the Si extracted from fits to the 2-carrier model are shown in Figure 5.8 below.

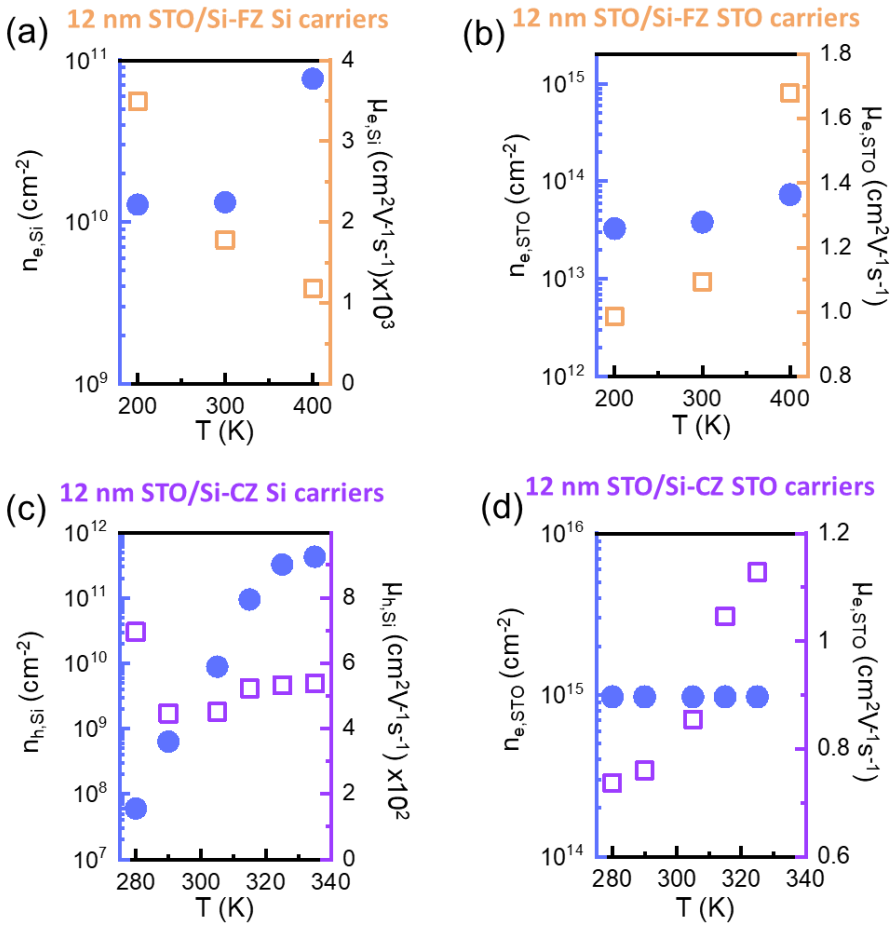

Figure 5.8: Electron carrier densities and mobilities for (a) electrons in the FZ Si and (b) electrons in the STO for the 12 nm STO/Si-FZ heterojunction. Carrier densities and mobilities of (c) holes in the CZ Si and (d) electrons in the STO for the 12 nm STO/Si-CZ heterojunction. Carrier densities and mobility values are extracted from fits to R_{xy} data using the 2-carrier model as described in section 4-1.3.

The decreased sheet resistance in the 12 nm STO/Si-CZ sample as compared to the 12 nm STO/Si-FZ sample is attributed to the increased electron carrier density in the 12 nm STO/Si-CZ sample. Hall measurements at 200 K, well below the temperature at which a hole gas appears in the 12 nm STO/Si-CZ sample indicate sheet densities of $n_{e,STO}$ = 9.7x10^{14} cm^{-2} and 3.3x10^{13} cm^{-2} in the 12 nm STO/Si-CZ and 12 nm STO/Si-FZ samples, respectively. Since films are grown under low oxygen pressures to prevent SiO_x formation at the interface, oxygen vacancies, denoted as V_O, are present in the STO for both films and the upper bound for V_O in either heterojunction must be 3.3x10^{13} cm^{-2} since both films are grown under identical conditions. The extra carrier density present in the STO film grown on a CZ wafer must have something to do with the substrate.

The question naturally arises: why is there such a difference in electrical transport given that the films are grown under identical conditions, and why are there mobile holes in the Si for the 12 nm STO/Si-CZ sample? For holes to be present in the Si the valence band maximum would have to cross the Fermi level since there are only n-type dopants present in the CZ Si (oxygen impurities).

To further understand what the energy bands in these heterojunctions looks like, we employ the use Hard X-ray Photoelectron Spectroscopy measurements which can determine band edge profiles across heterojunctions by fitting core-level photoelectron spectra. For the 12 nm STO/Si-CZ and 12 nm STO/Si-FZ samples, an x-ray energy of 5.9 keV at an incidence angle of 10° from the surface.

Details about the equipment used for the HAXPES measurements and fitting can be found in section 4-2.1. Additional lab-based HAXPES measurements were carried out by Alex Gray's group at Temple University which corroborate the main features seen in the spectra but with poorer resolution and count rate.

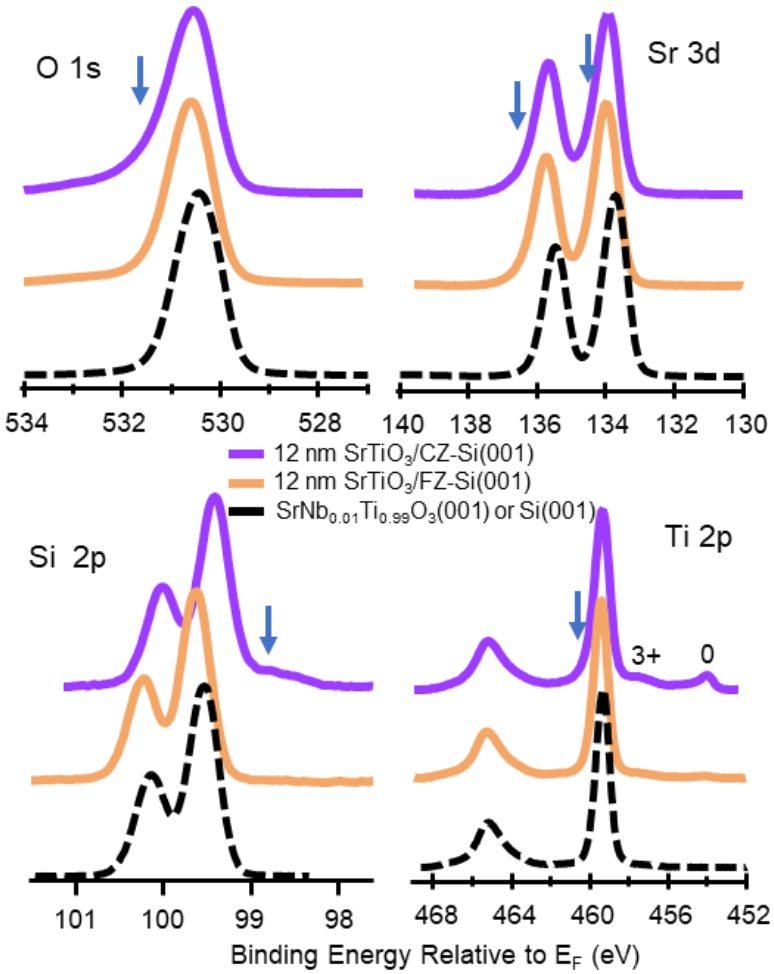

Figure 5.9: Si 2p, O 1s, Sr 3d and Ti 2p core level photoelectron spectra for 12 nm STO/Si-CZ, 12 nm STO/Si-FZ heterojunctions and reference spectra from bulk Si(100) and $SrNb_{0.01}Ti_{0.99}O_3$(100). Blue arrows indicate core level broadening associated with band bending. Note the lower valence features present in the Ti 2p spectra which are much larger in intensity for the 12 nm STO/Si-CZ heterojunction than for the 12 nm STO/Si-FZ heterojunction.

O 1s, Sr 3d, Si 2p and Ti 2p spectra are shown for the 12 nm STO/Si-CZ, 12 nm STO/Si-FZ and reference spectra from single crystal $SrNb_{0.01}Ti_{0.99}O_3$ and Si(100) samples in Figure 5.9. The spectra for the 12 nm STO/Si-CZ heterojunction show asymmetric broadening to higher binding energy for O 1s, Sr 3d and Ti 2p core levels, as indicated by arrows in Figure 5.9 (a). The shift to higher binding energy suggests that the STO bands bend downward near the interface such that

electrons closer to the interface will need to pass through a larger potential to leave the sample surface than if the bands were flat. The additional lower energy features seen in the Ti 2p spectra for the 12 nm STO/Si-CZ sample are lower valence states of Ti. Fits to the spectra show multiple Ti valences states are present which is due to charge transfer from the Si to STO. Since Ti valences range from 0+ to 4+ [5.8], it is possible for a combination of these to be present depending on where the transferred charges sit in the STO. For example, it is expected that charges transferred from the Si to STO lie much closer to the interface than to the Si surface since there will be positively charged donor cores on the Si side of the interface. Note that multiple oxidation states present could also be due to disorder or inadequate supply of oxygen during film growth, however, this is ruled out since films grown under the same conditions on an LSAT substrates do not show lower valence features as shown in Figure 5.10, indicating that they are due to the STO/Si heterojunction.

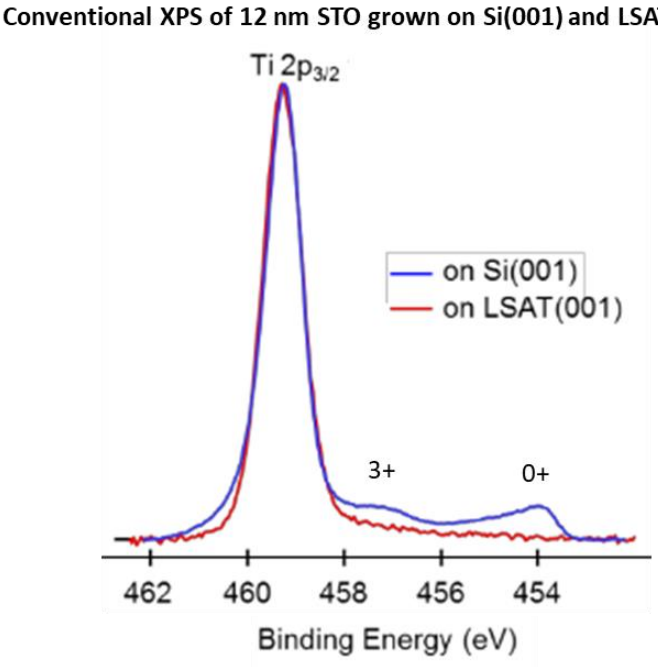

Figure 5.10: Conventional XPS Ti $2p_{3/2}$ spectra for 12 nm STO films grown on CZ Si(100) and LSAT(100). The lower valence features seen in the 12 nm STO/Si-CZ spectra are absent for the 12 nm STO/LSAT spectra indicating the features are due to the STO/Si interface instead of disorder or inadequate oxygen flux during epitaxial growth.

While broadening to higher binding energies is due to non-localized fields, the lower valence features having lower binding energies is due to localized field distributions within the perovskite unit cell. The nominal valence of Ti in the perovskite structure is 4+ but if electrons are added to it to decrease the valence to 3+, 2+, 1+ or 0+, they will act to screen the nuclear charge and decrease the amount of energy needed to leave the sample, the binding energy. Since the lower valences do not appear in STO/LSAT heterojunctions, we conclude that they are due to charge transfer from the Si.

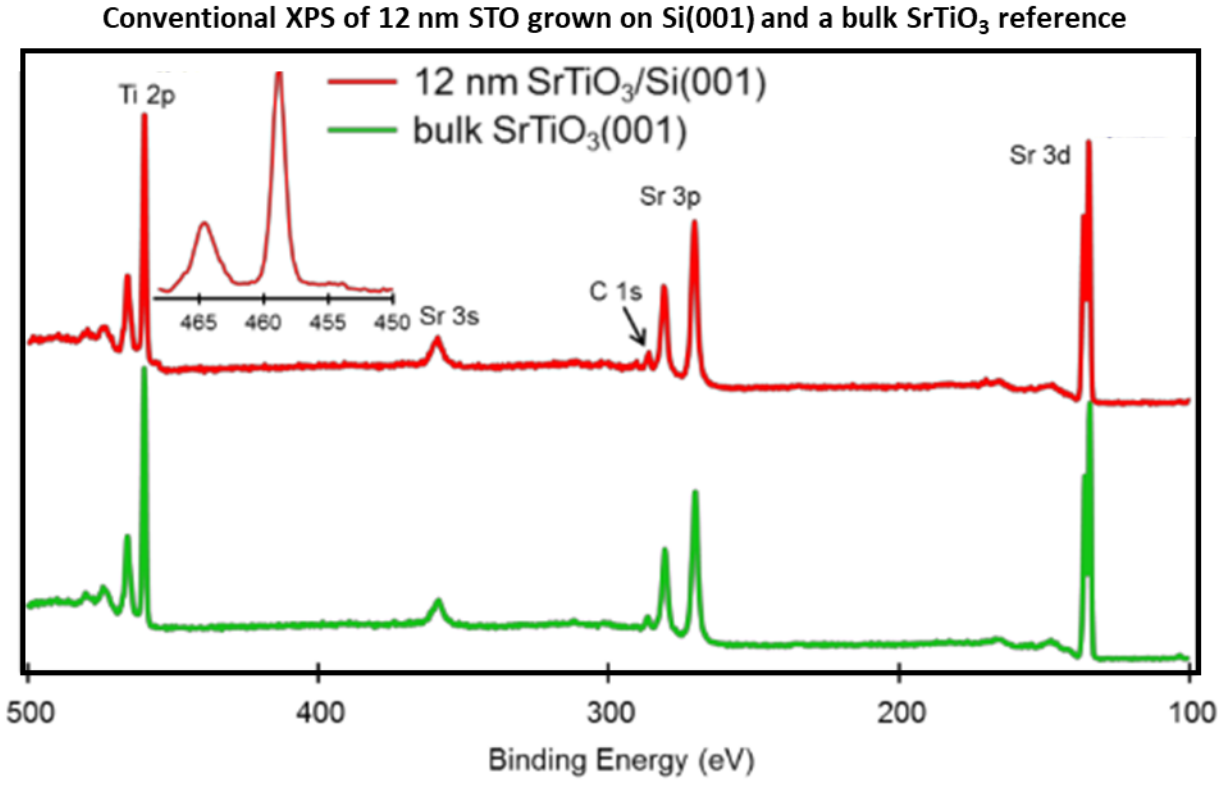

Figure 5.11: Conventional XPS spectra for the 12 nm STO/Si-CZ heterojunction compared to spectra obtained for bulk STO. Note the lack of Ti low valence features in the bulk STO.

A comparison of conventional XPS spectra for 12 nm STO/Si-CZ heterojunction and bulk $SrTiO_3$ are shown in Figure 5.11. Since conventional XPS uses lower excitation energies, the

probe depth is only 1-2 nm from the sample surface, meaning any feature changes seen in the spectra must be due to near-surface effects. The only discernable difference in the spectra is the additional lower valence feature of the Ti 2p which has a reduced intensity when compared to HAXPES Ti 2p spectra of the same heterojunction. It can be concluded from this that the lower valence features lie closer to the heterojunction interface than the STO surface. The absence of core-level broadening to higher energies also indicates that the potential near the surface is weak (bands are flatter and closer to the Fermi level) compared to the potential near the interface.

To provide further evidence of the spatial distribution of the potential throughout the heterojunction, angle resolved HAXPES for the 12 nm STO/Si-CZ heterojunction is shown in Figure 5.12 which probes the depth dependance of the features seen in Ti $2p_{3/2}$ and Si 2p core level line shapes. Note that angle-resolved HAXPES data was taken as part of a different study [5.9] but is the same 12 nm STO/Si-CZ sample used in this work.

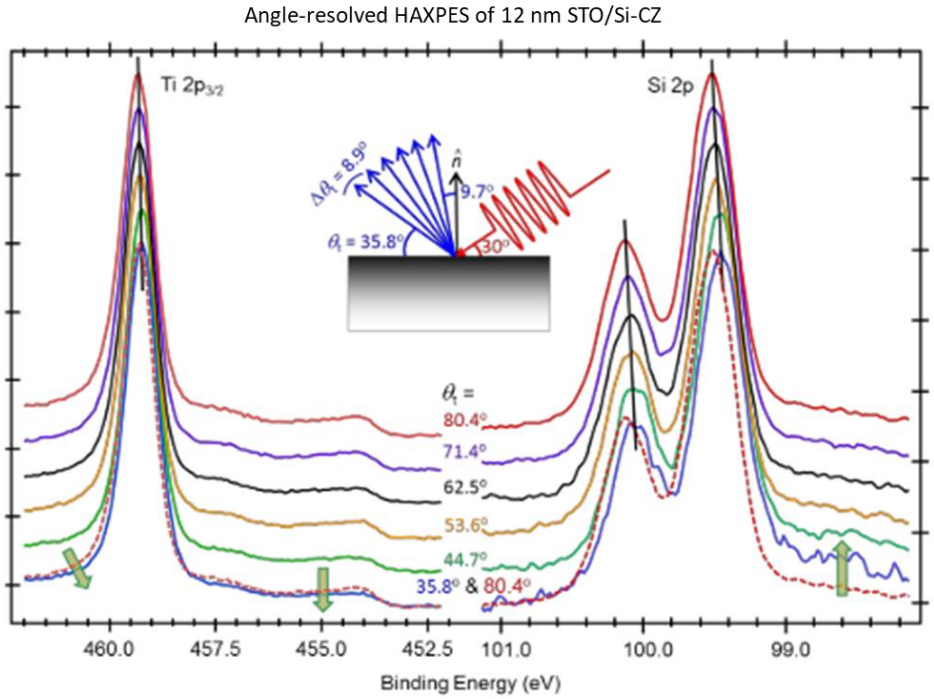

Figure 5.12: Angle resolved HAXPES for 12 nm STO/Si-CZ heterojunction measured as a function of take-off angle, θ_t. Note the decrease in broadening and lower valence features for the Ti 2p spectra as θ_t decreases and the increase in Si 2p lower binding energy shoulder.

An x-ray incidence of 30° from the sample surface was used and outgoing photoelectrons were binned into groups of $\Delta\theta_t$ = 8.9 ° to collect all photoelectrons in that range as a function of binding energy. Since what is measured is the photoelectron kinetic energy, it is helpful to think to the angular distribution dependance as a function of the velocity vector. Each energy measured will have an angular distribution in which photoelectrons leaving the sample at higher angle have a larger velocity component perpendicular to the surface than photoelectrons leaving the sample at lower angles which have a higher velocity component parallel to the sample surface. As the take-off angle, θ_t, is lowered, the effective probe depth decreases because the velocity component perpendicular to the surface is lower which relates to the escape depth of photoelectrons in the sample. The probe depth variation can be seen in the Si 2p line shape as a function of take-off angle. As the take-off angle decreases from 80.4° to 35.8°, the low energy shoulder of the Si 2p line shape increases because the measurement is more sensitive to the near interface Si region where the bands are expected to bend sharply upwards as expected from electrical transport measurements which indicate the presence of a hole gas in the Si. An opposite trend is seen in the Ti $2p_{3/2}$ lower valence features which decrease in intensity while the sharpest part of the Ti $2p_{3/2}$ peak shifts to lower binding energy because the measurement is more sensitive to the top part of the film because the lower take-off angle is more sensitive to STO layers closer to the surface where the potential is thought to be weaker from conventional XPS measurements.

Fits to the Si 2p and Ti $2p_{3/2}$ core level spectra are made by first assigning reference spectra that are minimally affected by band bending and surface core-level shifts to each layer within the heterojunction, attenuated by a damping factor. Each layer is assigned a random binding energy and a model spectrum is made from the sum of each layer's reference spectrum shifted by a random binding energy. The goodness of the fit is calculated from a cost-function as described in section 4.2-1 and the process is repeated until a good fit is reached. The binding energies for each layer are then converted to binding energy relative to the Fermi level by

$$E_V(z) = E_{CL}(z) - (E_{CL} - E_V)_{ref}$$

where $E_{CL}(z)$ is the core level binding energy obtained from the fits, with z being the depth, and $(E_{CL} - E_V)_{ref}$ is the difference in core level and valence band maximum of the reference sample. This shifts the depth distribution of the core-levels found from fitting by the difference in reference spectra core level and valence band maximum to obtain the valence band profile relative to the Fermi level.

Fits to the 12 nm STO/Si-CZ Si 2p and Ti $2p_{3/2}$ spectra are shown in Figure 5.13 (a) and (b). Band edge profiles for 12 nm STO/Si-CZ and 12 nm STO/SI-FZ heterojunctions are shown in Figure 5.13 (c). For the 12 nm STO/Si-CZ heterojunction, a type-III band alignment is seen with the Si VB above the STO CB. On the Si side of the heterojunction, the bands bend sharply upward near the interface and then flatten out within 2 nm moving toward the bulk. On the STO side of the heterojunction, the bands bend strongly downward close to the interface, flatten out ~4 nm from the interface, then bend slightly upward at the surface. Band offsets are calculated using the equation:

$$\Delta E_{VB} = (E_{Si\ 2p_{\frac{3}{2}}} - E_{VB,Si})_{Si} + \left(E_{Ti\ 2p_{\frac{3}{2}}} - E_{VB,STO}\right)_{STO} - (E_{Ti\ 2p_{\frac{3}{2}}} - E_{Si\ 2p_{\frac{3}{2}}})_{int}$$

The valence band offset was found to 5.46 eV, with the STO VB being 5.46 eV below the Si VB. The conduction band offset is then calculated from the bulk band gaps and valence band offset using the equation:

$$\Delta \mathrm{E}_{CB} = \Delta E_{VB} + (E_{g,Si} - E_{g,STO})$$

The conduction band offset was found to be 3.26 eV, with the CB of STO being 3.26 eV below the CB of Si. Note that the Si VB crosses the Fermi level which gives rise to hole gas formation in the Si.

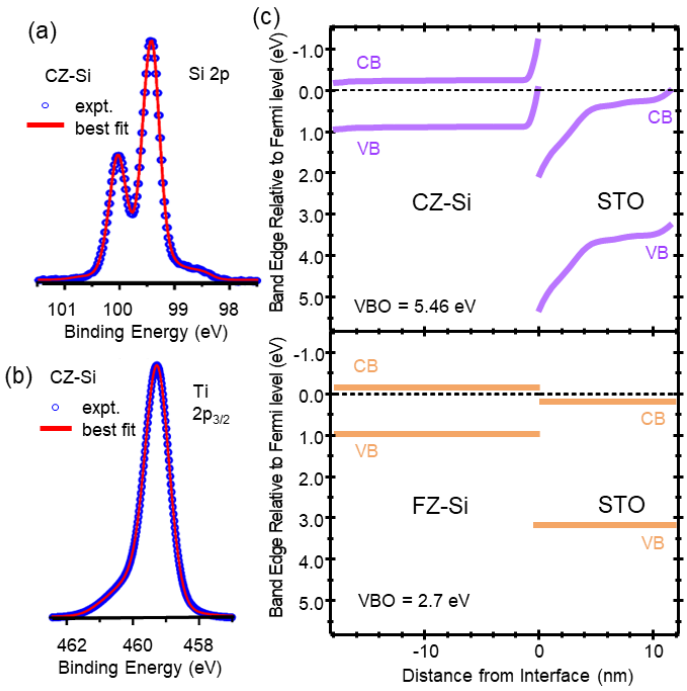

Figure 5.13: Fits to 12 nm STO/Si-CZ core level line shapes (a) Si 2p and (b) Ti $2p_{3/2}$. (c) Band edge profiles for 12 nm STO/Si-CZ and 12 nm STO/Si-FZ heterojunctions. Valence band offsets (VBOs) were found to be 5.46 and 2.7 eV for the 12 nm STO/Si-CZ and 12 nm STO/Si-FZ heterojunctions, respectively.

In contrast to the strong asymmetries in the 12 nm STO/Si-CZ heterojunction core levels, there is very little asymmetry seen in the core level line shapes of the 12 nm STO/Si-FZ heterojunction and the bands were found to be flat despite the small low valence features seen in the Ti $2p_{3/2}$ line shape. The band alignment is type-II, with the STO VB below the Si VB and the STO CB between the Si CB and VB. A valence band offset of 2.7 eV and a conduction band offset of ~0.5 eV was found for the 12 nm STO/Si-FZ heterojunction.

To briefly summarize the HAXPES results for the 12 nm STO/Si-CZ and 12 nm STO/Si-FZ heterojunctions: The 12 nm STO/Si-CZ heterojunction shows a type-III band alignment where the Si bands are bend sharply upwards at the interface while the 12 nm STO/Si-FZ heterojunction shows a type-II band alignment with flat bands (no built-in fields) throughout the heterojunction. The central question then becomes: why do we see a change in band

alignment for two identically grown films? As postulated in a previous study, the formation of a hole gas in the 12 nm STO/Si-CZ sample results from the interplay of three things: surface depletion, type-III band alignment and oxygen impurities in the CZ Si. While the type-III band alignment is necessary for formation of a hole gas, surface depletion and oxygen impurity concentration were not extensively studied before. Surface depletion is studied in Chapter 6 while oxygen impurity concentration is discussed here.

Even though the 12 nm STO/Si-CZ heterojunction has a type-III band alignment, the main source of electrons transferred to the STO are not from the VB of Si. This is evident from the 2-carrier model fits to R_{xy} which reveal the hole gas density in the Si to be ~$5x10^{-9}$ cm^{-2} while the electron carrier density in the STO to be ~$1x10^{15}$ cm^{-2} at 300 K, a difference of almost 4 orders of magnitude. In addition, since the maximum number of electron carriers (oxygen vacancies) in the STO was found to be $3.3x10^{13}$ cm^{-2} from fits to the 12 nm STO/Si-FZ heterojunction, there are ~$9.7x10^{14}$ unaccounted for itinerant electrons in the STO grown on CZ Si than in STO grown on FZ Si.

Secondary ion mass spectroscopy (SIMS) of the two 12 nm STO/Si heterojunctions reveals that there is a significant accumulation of oxygen impurities near the Si interface for the 12 nm STO/SI-CZ heterojunction as compared to the 12 nm STO/Si-FZ heterojunction. SIMS data was obtained at Pacific Northwest National Lab by Zihua Zhu using Cs^+ ions.

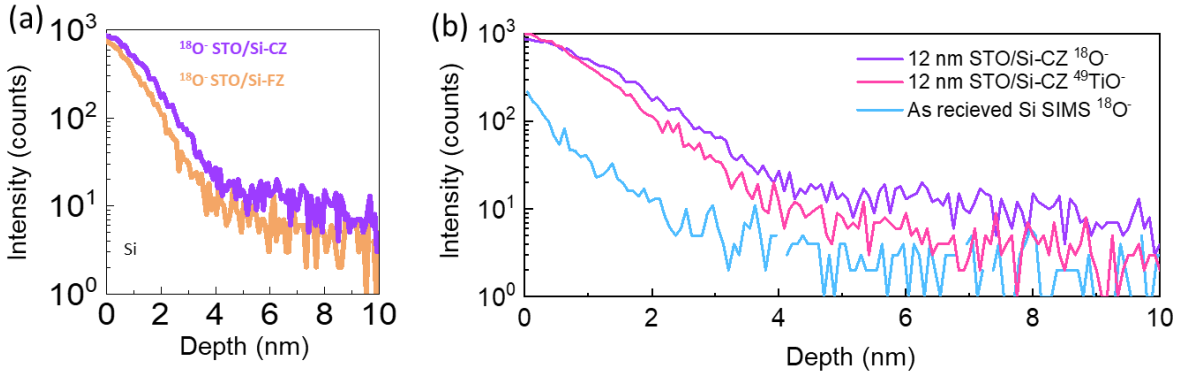

Figure 5.14: (a) SIMS $^{18}O^-$ profiles relative to the Si surface for 12 nm STO/Si-CZ and 12 nm STO/Si-FZ heterojunctions. (b) SIMS $^{18}O^-$ and $^{49}TiO^-$ profiles for the 12 nm STO/Si-CZ heterojunction compared to the $^{18}O^-$ profile of an as-received Si(100) wafer.

Figure 5.14 (a) shows a comparison of SIMS $^{18}O^-$ signal for the 12 nm STO/Si-CZ and 12 nm STO/Si-FZ heterojunctions, where the zero is the interface between STO/Si determined by the crossover between $^{30}Si^-$ and $^{18}O^-$ signals. The isotope $^{18}O^-$ was chosen because the $^{16}O^-$ signal saturates the detector giving an inaccurate representation of the oxygen impurity profile. The $^{18}O^-$ signal is larger in intensity for the 12 nm STO/Si-CZ heterojunction as compared to the 12 nm STO/Si-FZ heterojunction. The presence of $^{18}O^-$ impurities in the FZ Si indicate oxygen diffusion from the STO into the Si during epitaxial growth. While oxygen impurities inherent to the CZ Si manufacturing process are initially electrically inactive since they sit at interstitial sites, they will precipitate and diffuse toward the surface when heated and become electrically active n-type dopants in Si [5.10], [5.11]. To rule out knock-on effects, the $^{18}O^-$ signal is compared to the $^{49}TiO^-$ signal, which is more closely matched in mass to the of Cs^+ ions used in the measurement (Figure 5.14 (b)). Since the $^{18}O^-$ signal is larger than the $^{49}TiO^-$ signal, the $^{49}TiO^-$ signal represents the maximum effect that knock-on would create. Both signals from the 12 nm STO/Si-CZ sample are compared to the $^{18}O^-$ signal of an as received CZ Si wafer which shows a smaller oxygen impurity concentration near the surface and the measured concentration is likely a combination of the native oxide layer and knock-on effects. Additionally, ToF-SIMS reveals the oxygen impurity profile to be primarily within ~4 nm of the interface which helps to create a sharp potential profile near the interface when depleted of carriers, which will be discussed later in this chapter in the context of doped Si wafer effects on band alignment.

In the presence of a type-III band alignment, oxygen impurity donor electrons from the Si will be transferred to the STO creating a space-charge region between the depleted oxygen impurities in the Si and the transferred electrons in the STO. Depending on the proximity of the Si VB to the Fermi level, oxygen impurities in the Si may either be only partially depleted or fully depleted. When no oxygen impurity donors are transferred to the Si or are partially depleted, remaining electrons in the Si will conduct in parallel with electrons in the STO which results in a negative, non-linear R_{xy} as observed for the 12 nm STO/Si-FZ heterojunction. Fits to the R_{xy} data at 300 K indicate that the electron sheet density in the Si is $n_{e,Si} = 1.2\text{x}10^{10}$ cm^{-2}. When fully depleted and the Si VB is very near or above the Fermi level, the heterojunction is in the *inversion* regime and holes in the Si conduct in parallel with electrons in the STO which

manifests in electrical transport as a crossover in sign of R_{xy} as measured for the 12 nm STO/Si-CZ heterojunction.

Since the only difference in the two heterojunction is the type of Si wafer, and thus oxygen impurity content, the question becomes: how does the presence of a higher concentration of extra oxygen impurity donors in the 12 nm STO/Si-CZ heterojunction give rise to a change in band alignment from type-II to type-III that leads to inversion in the Si? The proposed model is that the space charge created by the transfer of oxygen donors from Si to STO modifies the interfacial dipole so that the VBO increases, thereby promoting further charge transfer to occur.

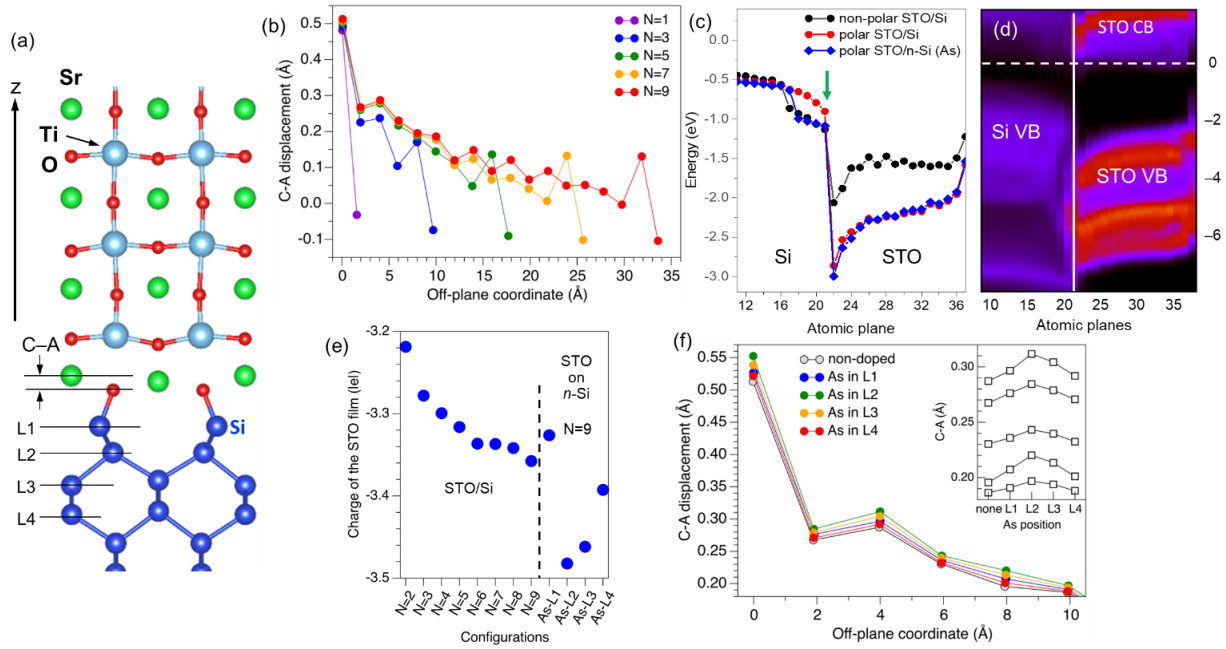

Figure 5.15: (a) DFT model of a polar STO/Si heterojunction allowed to fully relax. The interfacial dipole distorts the structure near the interface, resulting in increased C-A displacement. (b) Calculated C-A displacements for various film thicknesses, N. (c) VBO for polar, non-polar and doped polar heterojunction models. (d) DOS projected onto each atomic plane for the polar, undoped heterojunction. (e) Charge transfer from Si to STO as a function of film thickness and As_{Si} dopant position. (f) Calculated C-A displacement profiles as a function of As_{Si} dopant position.

First-principles density functional theory (DFT) calculations by Peter Sushko help to elucidate the relationship between VBO and space charge for STO/Si heterojunctions. First, structural polarization in the STO is studied by comparing polar and non-polar STO/Si heterojunctions that are nominally undoped. A model heterojunction is shown in Figure 5.15 (a) in which cation (C) - anion (A) displacements are defined as the offset between Sr^{2+} and O^{2-} atoms in the SrO planes in the out-of-plane direction. For the non-polar scenario, SrO and TiO_2 planes are held in place at their average positions in the fully relaxed bulk STO structure. In the interfacial layer there are competing forces between Si^{+}-O^{2-} interface bonding and Sr^{2+}-O^{2-} attraction. The interface dipole is present in both polar and non-polar structures and is created by the strong electronegativity of O pulling electrons away from the Si surface. The Si^{+}-O^{2-} bond is the interface dipole and when the structure is allowed to relax, O^{2-} anions are displaced toward the Si^{+} and Sr^{2+} and Ti^{4+} are pushed away from the Si^{+} creating a polarization in the +z direction (away from the interface). Polarization in the +z direction is opposed by surface rumpling which displaces O^{2-} ions outward and Ti^{4+} ions inward, creating a polarization in the -z direction. Competition between these two structural polarizations creates a film polarization that varies throughout the film. C-A displacements were calculated as a function of film thickness N in unit cells as shown in Figure 5.15 (b). For each film thickness, C-A displacement is a maximum (~0.5 Å) at the interface then decreases toward the bulk of the film close to 0 Å, then shifts to a negative C-A displacement in the outermost layer due to surface rumpling. Note that 0 Å C-A displacement (fully relaxed) only occurs for films thicker than ~7 u.c. since thinner films are still strained to the Si.

Comparison of VBOs for the polar and non-polar heterojunctions modeled with 9 u.c. thickness is shown in Figure 5.15 (c) and it was found that a larger VBO occurs for the polar structure than for the non-polar structure. The DOS projected onto each atomic plane for the polar undoped STO/Si heterojunction is shown in Figure 5.15 (d). For the polar heterojunction, the Si^{+}-O^{2-} separation is shorter than for the non-polar heterojunction. The VBO change can be understood heuristically by thinking of the Si^{+}-O^{2-} bond distance as a parallel plate capacitor in which decreasing the plate separation increases the potential across the plates. While this heuristic picture helps to understand what is happening at the interface, DFT studies have

recognized that the interfacial polarization includes all bonding in the interfacial region including Sr bonding [5.12] and that the VBO can be correlated to the density of bonds across the interface and increases the amount of charge gained by STO from Si due to bonding. Our DFT calculations are consistent with these results as the polarized structure is found to decrease the Si-O^{2-} bond distance and increase the charge gained per supercell from Si from -1.7 |e| for a non-polar 9 u.c. thick structure and -3.35 |e| for a polar 9 u.c. thick structure.

So far, we have discussed the difference in VBO for polar and non-polar structures for undoped heterojunctions. If we then add in electron donors to the DFT model, what happens to the polarization? Since it is unknown exactly how O impurities act as donors in Si [5.10], we use substitutional arsenic (As_{Si}) dopants in the model since As atoms have one more valence electron than Si atoms. We find that for undoped Si, the amount of charge transferred to STO increases with film thickness up to ~9 u.c. at which point the charge transfer saturates as shown in Figure 5.15 (e). Substitutional As_{Si} dopants (1 As atom/supercell) are then added into the 9 u.c. thick film, taken as the bulk limit of charge transferred for undoped heterojunctions, and vary the position of As_{Si} atoms with depth, labeled as L1– L4 in Figure 5.15 (a). As_{Si} dopants in the first Si interfacial layer do not enhance the charge transfer, however, for As dopants in layers L2-L4, charge transfer increases with proximity to the interface. The minimal charge transfer seen for L1 dopants is somewhat expected as the As atom will bond with O^{2-} instead of acting as an n-type dopant in Si. While we expected the transferred charge from Si to STO to increase the VBO at the interface, there is very little effect on VBO seen for As atoms in the L2 layer as compared to the undoped polarized heterojunction as shown in Figure 5.15 (c). Instead, what is observed is an increase in C-A displacement which is a maximum for As in the L2 layer (~0.55 Å in the interfacial layer) and decreases with As distance to the interface with the minimum C-A displacement being for the undoped polar structure (~0.51 Å in the interfacial layer).

While this is not the expected result, there are differences in the DFT model and experimentally created heterojunctions. The 12 nm (32.5 u.c.) film thickness used in this study are relaxed in the bulk whereas the DFT model used 9 u.c. thick films which remain strained to the substrate. Since experimental heterojunctions are relaxed, they cannot respond to

transferred charge by further polarizing the lattice and structural compensation cannot occur with increasing space charge. Thus, we expect increasing the space charge can indeed change the VBO.

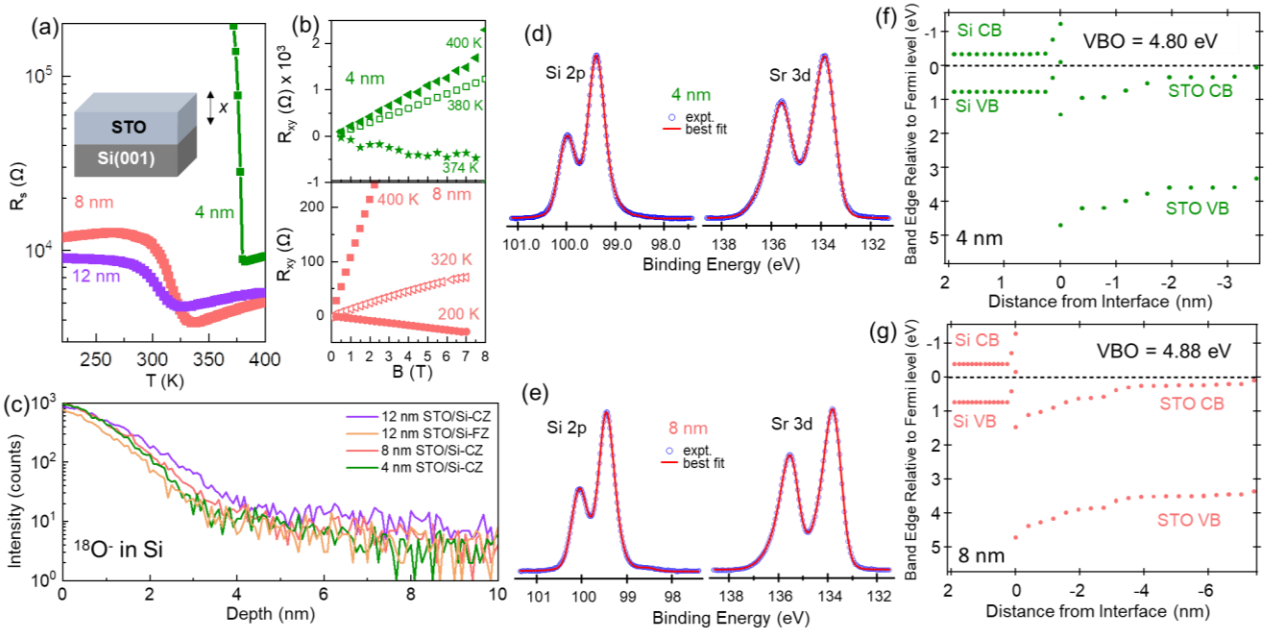

Figure 5.16: (a) Sheet resistance, R_s, of 4, 8 and 12 nm STO/Si-CZ heterojunctions. Note the decrease in R_s and hole gas onset temperature as a function of film thickness. (b) Hall resistance, R_{xy}, as a function of temperature for 4 and 8 nm STO/Si-CZ heterojunctions. (c) SIMS $^{18}O^-$ signals for 4, 8 and 12 nm STO/Si-CZ and 12 nm STO/Si-FZ heterojunctions in the Si as a function of depth from the interface. (d) and (e) show Si 2p and Sr 3d core-level line shapes and fits for the 4 and 8 nm STO/Si-CZ heterojunctions, respectively. (f) and (g) show band edge profiles extracted from the fits in (d) and (e) for 4 and 8 nm STO/Si-CZ heterojunctions, respectively. VBOs were found to be 4.80 and 4.88 eV for 4 and 8 nm STO/Si-CZ heterojunctions, respectively.

To show that the VBO can be tuned through space charge, additional 4 nm and 8 nm thickness STO/CZ films were grown under identical conditions. Electrical transport for 4 nm STO/Si-CZ and 8 nm STO/Si-CZ samples is shown in Figure 5.16 (a) and (b). Sheet resistance for

the 12 nm STO/Si-CZ sample is included for comparison. As the film thickness decreases, the sheet resistance increases, and the temperature at which the hole gas appears increases. The crossover in R_s between 8 and 12 nm thick films may be due to slight differences in the CZ wafers used which were taken from different batches of wafers with the same nominal properties. R_{xy} indicates the presence of a hole gas for both 4 and 8 nm thick films. Fits to the 4 and 8 nm STO Si 2p and Sr 3d core levels are shown in Figure 5.16 (d) and (e), along with their respective band edge profiles in (f) and (g). Both the 4 and 8 nm STO/Si-CZ heterojunctions are found to have a type-III band alignment. VBOs are found to increase from 4.80 eV for 4 nm STO to 4.88 eV for 8 nm STO to 5.46 eV for 12 nm STO films. SIMS $^{18}O^-$ signals are shown for 4, 8 and 12 nm STO/Si-CZ heterojunctions and for the 12 nm STO/Si-FZ heterojunction in Figure 5.16 (c). As the film thickness increases, we find that the oxygen impurity concentration increases. Since film growth rate is constant for all films (~1 ML/min), the increased oxygen content is attributed to oxygen diffusing from STO to Si during epitaxial growth for longer durations. Of note here is that oxygen concentration in the 12 nm STO/Si-FZ sample is less than for the 4 nm STO/Si-CZ sample, indicating that the oxygen impurity concentration found in the 12 nm STO/Si-FZ sample is below the threshold needed for a type-II to type-III band alignment change to be induced. One point to note is that all HAXPES measurements were carried out at 300 K and despite the 4 nm STO/Si-CZ sample showing a type-III alignment with the Si VBM above the Fermi level, electrical transport shows the onset of hole gas formation ~375 K. This may seem inconsistent at first glance, but we note that the sharp upturn seen in R_s for the 4 nm STO/Si-CZ sample is due to non-linear current-voltage characteristics measured at lower temperatures giving inaccurate R_s values below ~375 K. Above 375 K, the electrical contacts were found to have a linear current-voltage relationship. Thus, the sharp upturn in R_s does not mean the hole gas disappears at that temperature but that we are not able to measure it. This is a common problem we find when trying to measure very thin films (< 6 nm).

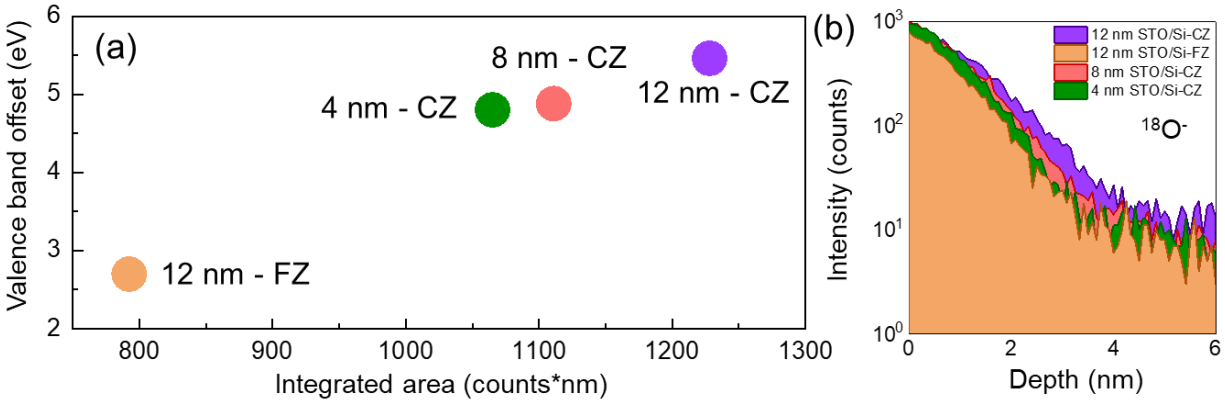

Figure 5.17: (a) Variation in the valence band offset at STO/Si heterojunctions with oxygen impurity content. (b) SIMS $^{18}O^-$ signals for 4, 8 and 12 nm STO/Si-CZ and 12 nm STO/Si-FZ heterojunctions. Integrated counts were taken within the first 6 nm of Si surface as defined by the crossover in $^{30}Si^-$ and $^{18}O^-$ SIMS signals.

The tunability of VBO as a function of film oxygen concentration near the interface is summarized in Figure 5.17. To quantify the oxygen content effect on VBO, SIMS $^{18}O^-$ signals are integrated within the first 6 nm of the Si, with the zero being the Si surface. The total number of counts is plotted against the measured VBOs for 4, 8 and 12 nm STO/Si-CZ and 12 nm STO/Si-FZ samples in Figure 5.17 (a), and we find that larger oxygen impurity content gives larger VBOs.

Since VBOs can be increased by increasing the number of dopants in the Si, we further explore this by growing 12 nm thick STO films on n-type doped Si substrates with different phosphorous dopant concentrations. Figure 5.18 (c) and (d) show core level spectra for 12 nm STO films grown on uniformly doped Si wafers with phosphorous concentrations of $10^{15} – 10^{16}$ cm^{-3} and $10^{17} – 10^{18}$ cm^{-3} throughout the bulk. There is a decrease in lower valence states seen in the Ti $2p_{3/2}$ core level with increasing phosphorous dopant concentration indicating reduced charge transfer from the Si to STO. This is consistent with electrical transport measurements at 100 K shown in Figure 5.18 (b) which give electron carrier densities in the STO to be $n_{e,STO/n\text{-}Si\text{-}CZ(10^{15}\text{-}10^{16}cm^{-2})}$ = 3.15 x 10^{14} cm^{-2} which is almost an order of magnitude less than for the undoped CZ wafer, which has an electron carrier density in the STO at 100 K of $n_{e,STO/Si\text{-}CZ}$ = ~1 x

10^{15} cm^{-2}. Note that the n-type substrates are too conductive to reliably measure until the carriers freeze out at low temperature, thus, R_s and R_{xy} are only shown below freeze out and transport below freeze out was not obtainable for the 12 nm STO/n-Si(10^{17}-10^{18} cm^{-2}). Fits to the core-level spectra are shown in Figure 5.18 (e) and (f) and it was found that there is a decrease in VBO with increasing phosphorous dopant density from 5.46 eV for the undoped 12 nm STO/Si-CZ sample to 4.17 and 3.79 eV for the 12 nm STO/n-Si(10^{15}-10^{16} cm^{-2}) and 12 nm STO/n-Si(10^{17}-10^{18} cm^{-2}) samples, respectively. The addition of n-type dopants in the Si bulk act to screen the positive space charge near the Si interface, weakening the electric field across the interface and reducing the VBO. This leads to an important point: the doping profile in the Si must be considered to decrease screening effects.

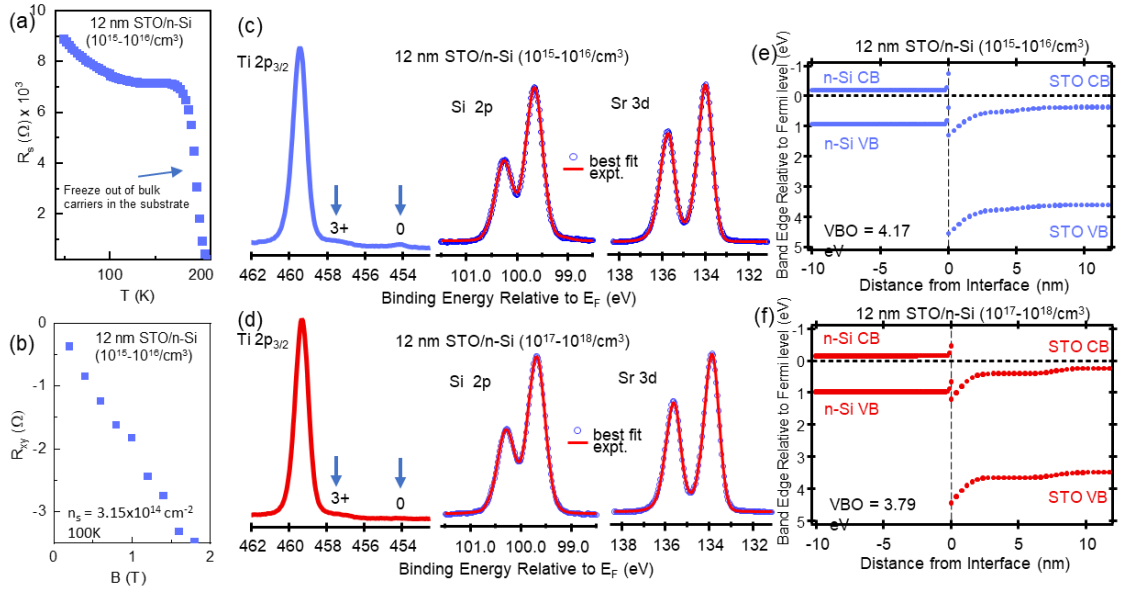

Figure 5.18: (a) and (b) show R_s and R_{xy} for the 12 nm STO/n-Si (10^{15}-10^{16} cm^{-3}), respectively. (c) Ti 2p, Si 2p and Sr 3d core-level spectra for the 12 nm STO/n-Si (10^{15}-10^{16} cm^{-3}). Fits to the Si 2p and Sr 3d line shapes are shown along with the experimentally measured spectra. (d) Ti 2p, Si 2p and Sr 3d core-level spectra for the 12 nm STO/n-Si (10^{17}-10^{18} cm^{-3}). Fits to the Si 2p and Sr 3d line shapes are shown along with the experimentally measured spectra. (e) and (f) show the band-edge profiles across the 12 nm STO/n-Si (10^{15}-10^{16} cm^{-3}) and 12 nm STO/n-Si (10^{17}-10^{18} cm^{-3}) heterojunctions, respectively. VBOs were found to be 4.17 and 3.79 eV for 12 nm STO/n-Si (10^{15}-10^{16} cm^{-3}) and 12 nm STO/n-Si (10^{17}-10^{18} cm^{-3}) heterojunctions, respectively.

5.4 Conclusions

In summary, we demonstrate that the band alignment at a semiconductor-crystalline oxide interface can be tuned through modification of the interfacial dipole by introducing space charge across it. The ability to the tune band alignment at hybrid heterojunctions sets them apart from conventional semiconductor heterojunctions which have relatively weak interfacial dipoles and longer screening lengths. Electrostatic altering of band alignment opens additional pathways to realize functional behavior in semiconducting hybrid heterojunctions.

Chapter 6: Sub-monolayer surface termination control of charge transfer across a semiconductor-crystalline oxide heterojunction

6.1 Introduction

In this chapter, we continue to explore the phase space of $SrTiO_3$/Si heterojunctions to understand and control the band offsets at the interface by studying the effect of surface termination on band offsets at the buried STO/Si interface. As discussed in Chapter 5, surface depletion is attributed as one of the drivers for hole gas formation in STO/Si-CZ heterojunctions, along with a type-III band offset and oxygen impurities in the Si. In Chapter 5, effects of oxygen impurity concentration on the band offsets were discussed, and it was found that increasing the oxygen impurity concentration near the STO/Si interface increased the VBO through electrostatic modification of the interfacial dipole. This resulted from the transfer of itinerant charge carrier in the Si to the STO, leaving behind a space charge region that in turn modified the interfacial dipole. This chapter discusses the role of surface depletion on the band offsets at STO/Si interfaces.

Older studies of STO surface states, both theoretical and experimental, indicate that there are no intrinsic surface states within the bandgap for pristine, stoichiometric STO surfaces. However, it was found that by Ar^+ irradiating the surface to intentionally produce O vacancies, researchers were able to produce defect states within the band gap associated with the transfer of electrons from O to Ti atoms, partially filling the Ti 3d band [6.1], [6.2]. Additionally, the deposition of 1 ML of Ti metal on TiO_2 surfaces was found to produce oxygen vacancies similar to what had previously been reported for Ar^+ irradiated surfaces. Both studies indicate the presence of Ti^{3+} on the surface due to oxygen vacancies.

More recently, thin, donor doped STO films were found to have a surface depletion layer [6.3], which spatially separated charge carriers from their donors due to the built-in

potential. The large temperature dependent dielectric response in STO increases the surface depletion layer depth with decreasing temperature.

Other groups have found that surface space charge regions on STO surfaces can be modified by exposing the surface to oxygen at elevated temperatures in UHV. Michael Andrä and co-workers found that increasing the oxygen exposure pressure, the Fermi level near the surface shifts deeper into the band gap, in which they found the maximum shift to be ~0.6 eV below the conduction band edge. The shift in Fermi level was correlated to a negatively charged surface layer which is attributed to the formation of Sr cation vacancies or charged oxygen adsorbates on the surface [6.4]. A more extensive study by Michael Andrä and co-workers indicates that the surface band bending increase with increasing oxygen pressure at elevated temperatures is the result of SrO formation near the surface which leaves behind Sr vacancies [6.5].

Scott Chambers and co-workers were able to measure surface core-level shifts on STO/p-Ge heterojunctions using XPS. They found that there was core-level broadening in the Sr 3d spectra due to the formation of $Sr(OH)_x$ at the STO surface from the interaction with atmospheric water vapor [6.6].

The surface termination of STO (SrO or TiO_2) has been found to be important for adsorption processes such as CO_2 adsorption for photocatalytic CO_2 reduction. Cha Luo and co-workers showed that while SrO terminated STO surfaces promote CO_2 surface adsorption, TiO_2 terminated STO surfaces exhibited higher photocatalytic activity [6.7]. DFT studies by other groups, indicate that SrO and TiO_2 terminated STO surfaces will have work function differences of several eV, and that surface defects such as O adsorbates, oxygen vacancies and Sr vacancies or adatoms can further change the work function [6.8], [6.9] which can alter band alignment at heterojunction interfaces.

Lim et al. studied the effects of surface depletion on charge transfer across a Nb doped STO/Si-CZ heterojunction as a function of Nb doping and STO film thickness [6.10]. The depletion region is inversely proportional to the square root of the carrier density:

$$d_{dep} \propto \frac{1}{\sqrt{n_{3d}}}$$

Increasing the carrier density decreases the depletion region depth such that more heavily doped STO should have smaller depletion regions as shown in Figure 6.1 (a). This can be seen in Figure 6.1 (b) in which the non-monotonic anomaly in R_s associated with hole-gas formation decreases in magnitude with increasing Nb dopant concentration in STO films, and it was found that the hole-gas carrier density decreased with increasing Nb dopant concentration. Additionally, increasing the film thickness to decouple the surface depletion band bending from the heterojunction interface resulted in decreased charge transfer from Si to STO as shown in Figure 6.1 (c).

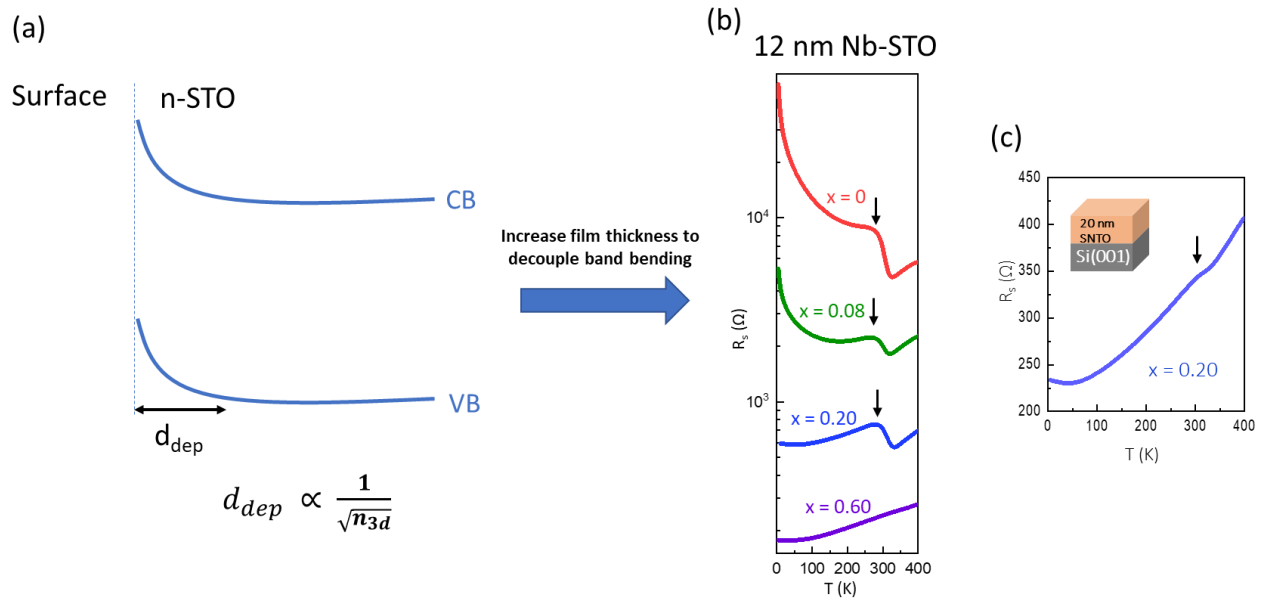

Figure 6.1: (a) Surface depletion at n-STO surfaces. (b) Sheet resistance of 12 nm $SrNb_xTi_{1-x}O_3$/Si heterojunctions as a function of Nb content, x. (c) Sheet resistance of a 20 nm $SrNb_{0.2}Ti_{0.8}O_3$/Si heterojunction.

The decrease in hole-gas carrier density with increasing Nb content (which decreases the depletion width) and increased film thickness suggests that surface depletion plays a key role in allowing charge to transfer from the oxygen impurity donors in Si to the STO, driving the transition from type-II to type-III band alignment and hole-gas formation in the Si.

In this chapter, we seek to understand the relationship between surface termination layers and surface adsorbates on STO/Si heterojunction band alignment and charge transfer across the interface.

6.2 Experiment

12 nm STO films were grown on 2" diagonal, 500 µm thick CZ Si wafers under identical growth conditions with varying surface terminations. A comparative study of differently terminated STO/Si surfaces is presented using electrical transport measurements and x-ray photoelectron measurements. For the photoelectron measurements, two sets of data are presented: hard x-ray (6 keV) and soft x-ray (600-1000 eV). This allows for the study of band bending throughout the heterojunction (hard x-ray) to be compared to details about the surface chemistry (soft x-ray). The XPS data is compared to electrical transport measurements taken in the van der Pauw configuration as a function of temperature and applied magnetic field. The surface terminations studied in this work are listed in Table 6.1.

Sample name	Sample description
STO/Si – no cap	Baseline 12 nm STO/Si-CZ sample – no cap
1 nm BaO/STO/Si	12 nm STO capped with 1 nm BaO
1 u.c. BTO/STO/Si	12 nm STO capped with 1 unit cell of $BaTiO_3$
1.5 nm LaSTO/STO/Si	1.5 nm STO capped with 1.5 nm La-STO (3%)
1.1 ML TiO_2/STO/Si	12 nm STO capped with 1.1 ML TiO_2
0.7 ML TiO_2/STO/Si	12 nm STO capped with 0.7 ML TiO_2
0.3 ML TiO_2/STO/Si	12 nm STO capped with 0.3 ML TiO_2
1.0 ML SrO/STO/Si	12 nm STO capped with 1.0 ML SrO

0.7 ML SrO/STO/Si	12 nm STO capped with 0.7 ML SrO
0.3 ML SrO/STO/Si	12 nm STO capped with 0.3ML SrO
1 u.c. aSTO/STO/Si	12 nm STO capped with 1 unit cell of amorphous STO

Table 6.1: Sample names and descriptions for the capping layers used in this study.

The sample set consists of a baseline 12 nm STO/Si-CZ heterojunction analogous to what has been studied previously [6.10], [6.11], and 10 samples capped with different layers. There are two series of sub-monolayer caps consisting of 0.3, 0.7 and ~1 ML of SrO and TiO_2 layers deposited at 450 °C in an oxygen background pressure of ~$3x10^{-7}$ Torr.

Electrical transport measurements are done using the van der Pauw geometry as described in Chapter 4.1. Wafers are diced into 5x5 mm^2 samples and mounted to a puck with Kapton tape. Electrical contacts are made to the sample corners using Al wedge wire bonding. Electrical transport measurements were carried out using a DynaCool PPMS (Quantum Design) as function of temperature and applied magnetic field. Two Keithley source meters are used in conjunction to multiplex the measurement signals to the appropriate electrical contacts. Fits to the Hall resistance, R_{xy}, data is done using either a 2- or 3-carrier model from which the carrier densities and mobilities of each conducting layer are extracted. At high temperatures, most sample which required the use of a 3-carrier model to account for thermally excited electrons in the Si substrate. While this was not seen in previous studies [6.10], [6.11], it is noted that the wafer thickness used for this set of samples is 500 µm thick instead of the 300 µm thick wafers used in previous studies so that there are more thermally generated electrons in the substrate.

Fits to the hard x-ray core-level photoelectron spectra are done as described in detail in Chapter 4.2. Each layer within the probe depth is assigned a bulk reference core-level spectrum, attenuated by a damping factor. Each reference spectrum is assigned a random binding energy. A trial spectrum is made to check the goodness of the fit, and the process is repeated until the

cost function is minimized. The resulting fit is used to create depth resolved band edge profiles relative to the Fermi energy.

6.3 Results

The baseline 12 nm STO/Si-CZ sample (no capping layer) electrical transport data shown in Figure 6.2 gives similar results to other uncapped 12 nm STO/Si-CZ samples studied previously [6.10], [6.11]. R_s shows a non-monotonic anomaly near room temperature in which a hole gas is present in the Si above it and not present below it, as evidenced by the crossover in sign of R_{xy} from positive to negative as the temperature is decreased across the non-monotonic anomaly in R_s. Below the hole gas transition temperature, R_{xy} is negative and linear indicating the transport is dominated by mobile electrons in the STO with low carrier mobilities. Since the films are grown in a low oxygen background to prevent SiO_x formation at the interface, the charge carriers in the STO are due to oxygen vacancies which are known to act as n-type dopants in STO [6.12]. Above the hole gas transition temperature, R_{xy} is positive and non-linear indicating the presence of two channel conduction with holes in the Si conducting in parallel with electrons in the STO. As discussed in Chapter 5, charge transfer from oxygen impurities in the Si to the STO gives rise to a space charge layer that modifies the interface dipole such that the band alignment changes from type-II to type-III. The Si VB edge sits just above the Fermi level, creating an inversion layer in the near interface region in the Si. The surface of the STO also exhibits upward band bending such that the STO CB crosses E_F and the surface is depleted of mobile charge carriers. Also shown in Figure 6.2 are the carrier densities and mobilities extracted from fits to the R_{xy} data for the uncapped 12 nm STO/Si-CZ heterojunction. The temperature dependence of the STO carrier density indicates increased itinerant electron carrier density in the STO with temperature, consistent with electron transfer from the oxygen impurity donors in the Si. It is noted that the slight downturn in R_s ~400 K was found to be due to thermally generated carriers in the bulk Si substrate with carrier density ~$5x10^{10}$ cm^{-2}, which is comparable to theoretically predicted values [6.13]. Fits at 400 K are obtained using a 3-

carrier model in which electrons in the STO conduct in parallel with holes in the Si inversion layer and thermally generated electrons in the bulk of the Si substrate.

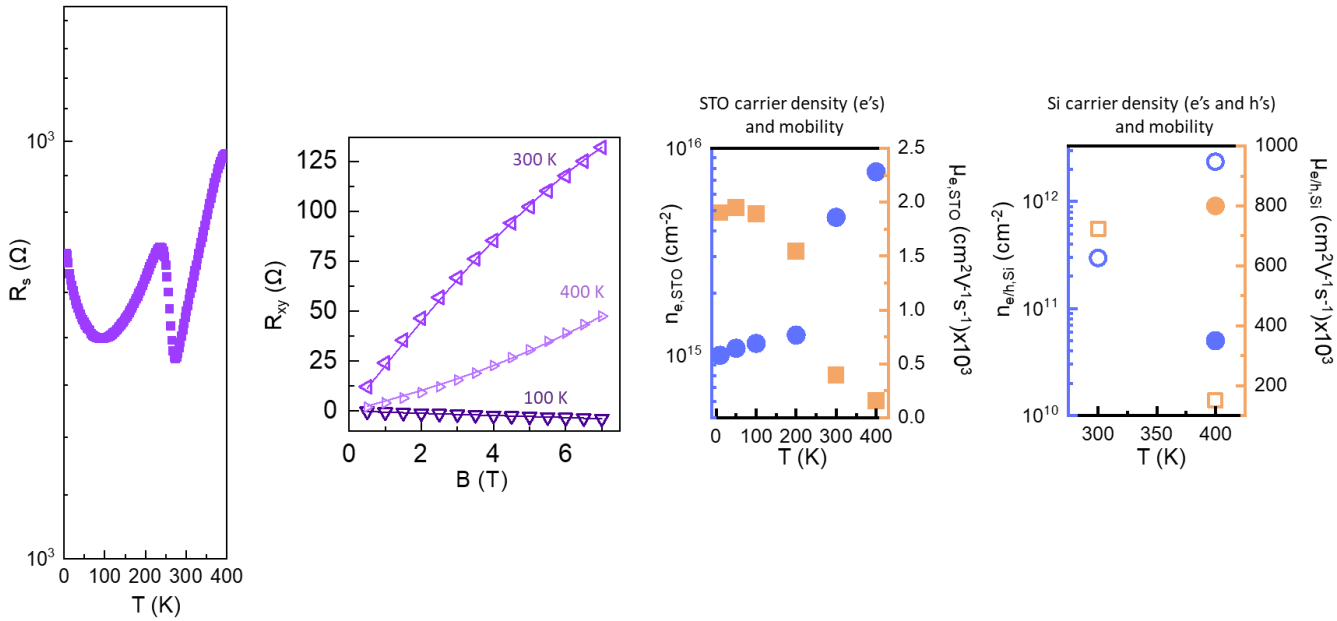

Figure 6.2: (Left) Sheet resistance and R_{xy} for the uncapped 12 nm STO/Si-CZ sample. (Right) Carrier densities and mobilities extracted from fits to R_{xy} are represented by closed and open shapes for electrons and holes, respectively.

A comparison of the electrical transport behavior for uncapped 12 nm STO/Si-CZ and the 1 nm (2 u.c.) BaO capped STO/Si heterojunction is shown in Figure 6.3. R_s for the 1 nm BaO capped sample is higher throughout the entire temperature range than the uncapped sample. For the 1 nm BaO capped sample, the sheet resistance increases monotonically when cooling from 400 K, although there is an anomaly in R_s that occurs from ~350 K - ~300 K. R_{xy} is negative throughout the entire temperature range and is non-linear from 400 K to 250 K. Below 250 K, R_{xy} is negative and linear. In the linear regime, electrical transport is dominated by oxygen vacancies in the STO. Fits to R_{xy} indicate that the non-linearity in R_{xy} from 250 – 400 K arises from electrons in the STO with low mobilities (~0.35 – 10 $cm^2V^{-1}s^{-1}$) conducting in parallel with

electrons in the Si with higher mobilities (~1000 – 3200 $cm^2V^{-1}s^{-1}$). The absence of a hole-gas for the 1 nm BaO capped sample is in stark contrast to the uncapped 12 nm STO/Si-CZ sample which shows the presence of a hole gas from 300 K – 400 K. Since both films were grown on identical substrates with identical growth conditions, we can conclude that the presence of a 1 nm BaO surface capping layer is responsible for the inhibited charge transfer across the STO/Si interface.

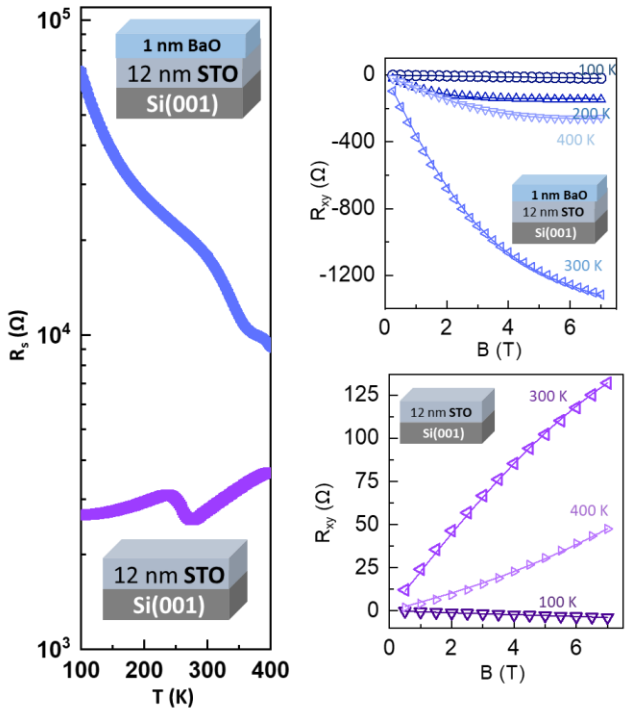

Figure 6.3: (Left) Sheet resistances, R_s, for the 1 nm BaO capped and uncapped STO/Si heterojunctions as a function of temperature. (Right) R_{xy} for the 1 nm BaO capped and uncapped STO/Si heterojunctions as a function of temperature and applied magnetic field.

Carrier densities and mobilities extracted from fits to R_{xy} for the 1 nm BaO capped sample data are shown in Figure 6.4. Unlike the uncapped sample which showed monotonic increase in $n_{e,STO}$ with increasing temperature, we find non-monotonic changes in $n_{e,STO}$ for the 1 nm BaO capped sample. At low temperatures (100 K), $n_{e,STO}$ ~$2x10^{14}$ cm^{-2} for the 1 nm BaO capped sample which is an order of magnitude less than for the uncapped STO sample in which

$n_{e,STO}$ ~ 1x10^{15} cm^{-2} at 100 K. For the 1 nm BaO capped sample, as the temperature increases, instead of $n_{e,STO}$ increasing as we observed for the uncapped STO/Si sample, we see a decrease in $n_{e,STO}$ down to ~2.2x10^{13}/cm^2 at 225 K which we note is comparable to $n_{e,STO}$ = 3.3x10^{13} cm^{-2} that was found for the 12 nm STO/Si-FZ sample at 200 K in Chapter 5 [6.11], which was taken as a maximum for the oxygen vacancy concentration in the STO. $n_{e,STO}$ for the 1 nm BaO capped sample then increases with increasing temperature up to ~1.4x10^{15} cm^{-2} at 400 K, which is lower than $n_{e,STO}$ = 7.7x10^{15} cm^{-2} measured at 400 K for the uncapped STO/Si sample. An inverse trend in $\mu_{e,STO}$ for the 1 nm BaO capped sample is observed, in which the mobility increases from ~0.34 $cm^2V^{-1}s^{-1}$ at 100 K to ~9.8 $cm^2V^{-1}s^{-1}$ at 225 K, then decreases to ~0.45 $cm^2V^{-1}s^{-1}$ at 400 K. We note that fits to the carrier mobilities were constrained to have mobilities close to those reported for bulk Si and STO films, however, some deviation occurs due to the non-uniform doping profiles in the heterostructures. We find that we can obtain better fits to the data by allowing all parameters to vary freely, but that we obtain non-physical values for the carrier mobilities. In the Si, we find that $n_{e,Si}$ for the 1 nm BaO capped heterojunction generally increases with temperature while $\mu_{e,Si}$ decreases with temperature as expected from the literature [6.13].

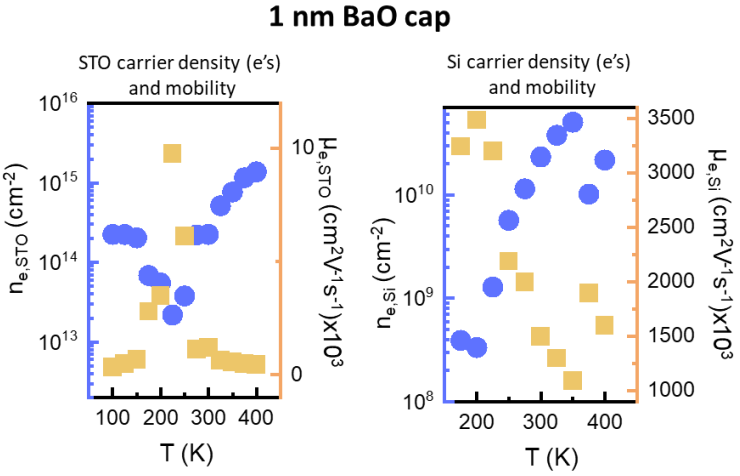

Figure 6.4: Sheet resistances and mobilities in both the STO and Si for the 1 nm BaO capped STO/Si heterojunction extracted from fits to the R_{xy} data.

The electrical transport behavior shown by the 1 nm BaO capped and the uncapped STO/Si-CZ samples is similar to what was observed in Chapter 5 for the 12 nm STO/Si-FZ and 12 nm STO/Si-CZ samples, respectively. Thus, we infer that the band alignment for the 1 nm BaO capped (uncapped 12 nm STO/Si-CZ) sample should be type-II (type-III). As discussed in Chapter 5, differences in oxygen impurity content in the Si near the interface can account for differences in charge transfer across the heterojunction. Here, we rule this out since we do not see significant differences in oxygen impurity content between the 1 nm BaO capped and uncapped STO/Si-CZ samples as measured by SIMS. A comparison of $^{18}O^-$ SIMS signals for the 1 nm BaO capped and uncapped STO/Si-CZ heterojunctions is shown in Figure 6.5.

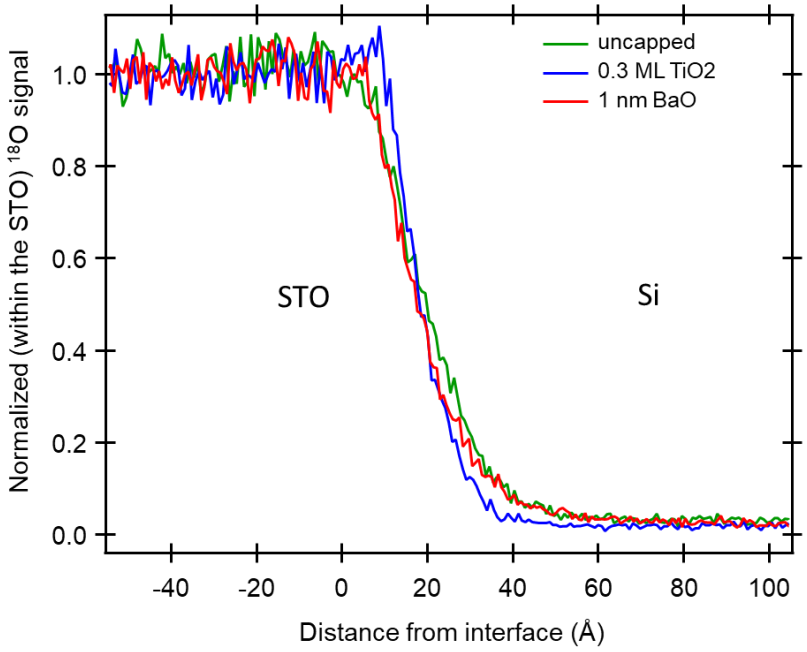

Figure 6.5: Normalized SIMS $^{18}O^-$ signals showing similar oxygen impurity concentrations in the 1 nm BaO capped and uncapped STO/Si heterojunctions. Also shown is the SIMS $^{18}O^-$ signal for the 0.3 ML TiO_2 capped STO/Si heterojunction.

Since we do not see any significant differences in Si oxygen impurity content between the two samples, we attribute the difference in electrical transport behavior between the 1 nm BaO and uncapped STO/Si-CZ heterojunctions to the 1 nm BaO surface capping layer. The

question arises as to what is happening at the STO surface that inhibits charge transfer across the heterojunction interface for the 1 nm BaO capped sample. As discussed in the introduction, surface depletion can be affected by surface oxygen adsorbates or cation vacancies.

To study the effects of surface capping layers on surface adsorbate chemistry and surface depletion, we employ the use of hard and soft x-ray photoelectron spectroscopy (HAXPES, XPS) techniques which can be used to map band-edge profiles and study surface adsorbate chemistry, respectively. HAXPES Si 2p, Ti 2p and Sr 3d core-level spectra are shown in Figure 6.6 for the 1 nm BaO capped and uncapped 12 nm STO/Si-CZ heterojunctions. For the uncapped 12 nm STO/Si-CZ heterojunction, core-level broadening is seen for Si 2p, Ti 2p and Sr 3d spectra, indicating the presence of strong built-in fields associated with charge transfer of electrons from the Si to STO and strong band bending. For the 1 nm BaO capped sample, however, there is essentially no difference between heterojunction and reference spectra (dashed black lines), except for the increased intensity near 103 eV in the Si 2p spectra which is attributed to interfacial bonding.

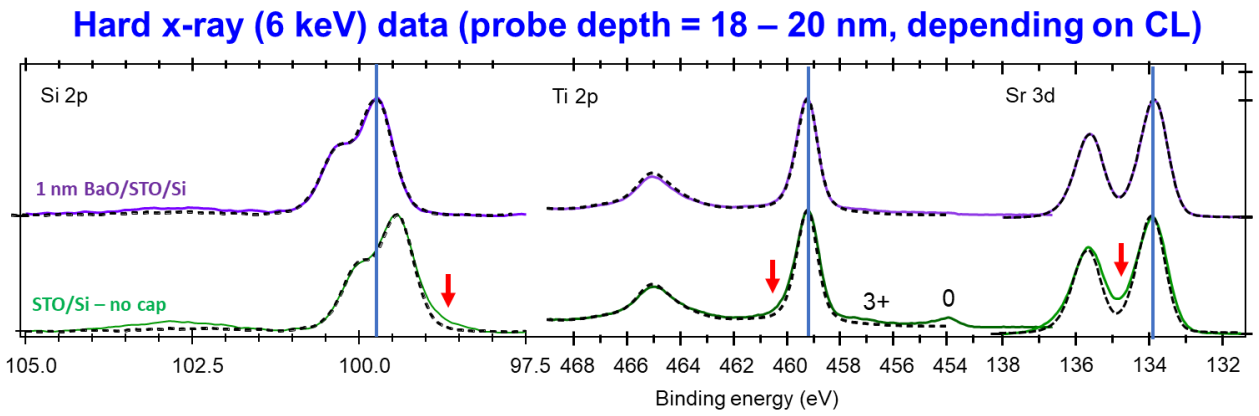

Figure 6.6: Si 2p, Ti 2p and Sr 3d core-level HAXPES spectra for the 1 nm BaO capped and uncapped STO/Si heterojunctions. While there is significant broadening present in all core-levels for the uncapped STO/Si heterojunction, the 1 nm BaO capped STO/Si heterojunction core levels are almost identical to the reference spectra.

Band-edge profiles extracted from fits to the core-level spectra as described in section 4-2 are shown in Figure 6.7. For the uncapped 12 nm STO/Si-CZ heterojunction, a type-III band alignment is observed with strong upward band bending in the Si and downward band bending in the STO as the bands approach the interface. The Si VBM crosses the Fermi level, creating an inversion layer in the Si near the interface, consistent with the electrical transport measurements which indicated the presence of a hole gas in the Si. Additionally, the STO CBM crosses the Fermi level indicating the STO surface is depleted of itinerant charge carriers.

In contrast to the uncapped 12 nm STO/Si-CZ heterojunction, the 1 nm BaO capped STO/Si-CZ heterojunction shows a type-II band alignment, with flat bands throughout the heterojunction. The Si CBM lies below the Fermi level indicating the presence of itinerant charge carriers in the Si. This corroborates the electrical transport measurements shown in Figure 6.3 which showed the presence of electrons in the STO conducting in parallel with electrons in the Si. The itinerant carriers in the Si are oxygen impurity donors in the Si. Both electrical transport and HAXPES indicate that no significant charge transfer from Si to STO occurs for the 1 nm BaO capped sample.

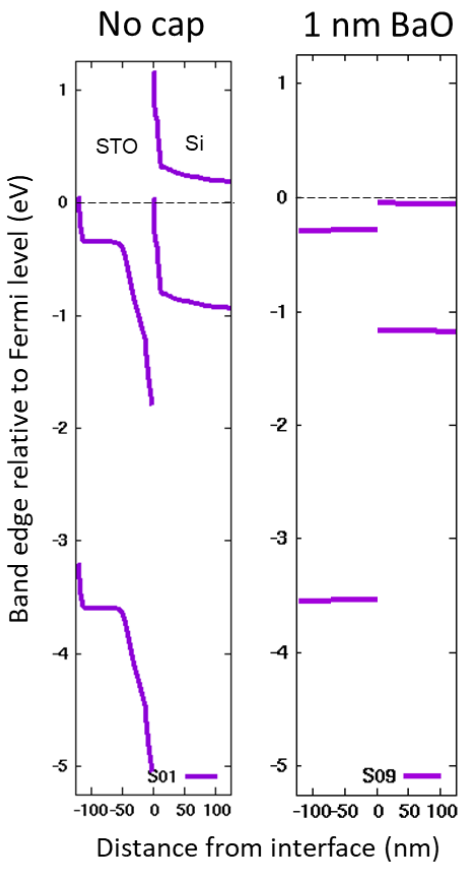

Figure 6.7: Band edge profiles extracted from fits to the core-level spectra in Figure 6.6 for the uncapped and 1 nm BaO capped STO/Si heterojunctions.

Why do we see such a difference in electrical transport and a transition from type-III to type-II band alignment with the addition of a 1 nm BaO capping layer? A comparison of the effects of surface termination on surface adsorbates is shown in Figure 6.8. If the addition of the 1 nm BaO surface capping layer were to affect the type and concentration of surface adsorbates, we would expect differences in core-level spectra measured with XPS [6.6]. We refer to the surface adsorbates here as surface "junk" which are present on all samples exposed to atmosphere. There are no significant differences in C 1s and O 1s core levels measured for the 1 nm BaO and uncapped STO/Si heterojunctions, indicating that there is no significant difference in surface adsorbates for the two samples. While the origin of the observed change

in band alignment is still under investigation, we can rule out differences in surface "junk" (at 300 K) as the driving factor.

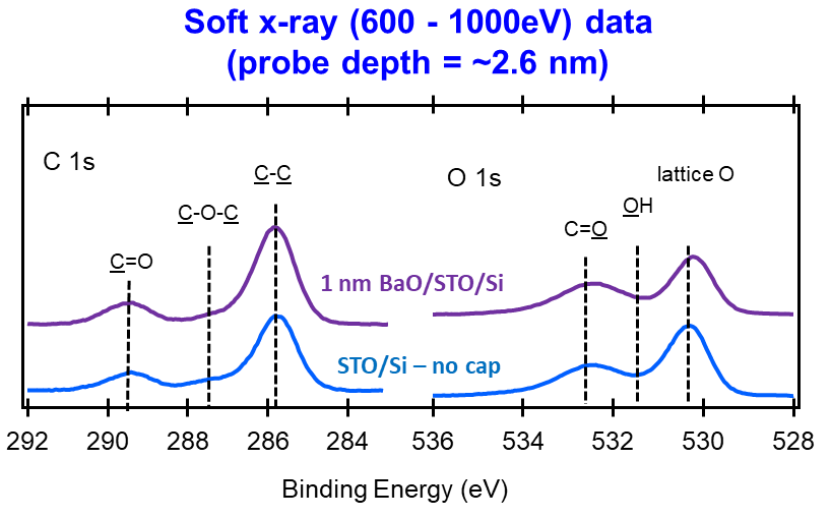

Figure 6.8: C 1s and O 1s soft x-ray core-level spectra for the uncapped and 1 nm BaO capped STO/Si heterojunctions indicate that there is no significant difference in surface junk between the two samples.

While we observe large changes in electrical transport for the 1 nm BaO capped sample compared to the uncapped sample, we also observe changes for all other capping layers. Electrical transport data for 0.3 ML, 0.7 ML and 1.1 ML TiO_2 capped samples are shown in Figure 6.9. As the TiO_2 capping layer thickness increases, a systematic increase in R_s is observed below the non-monotonic anomaly, indicating lower STO carrier density with increasing TiO_2 thickness. Fits to R_{xy} reveal that below the non-monotonic anomaly, the STO carrier density increases with increasing TiO_2 thickness. For the 0.3 ML TiO_2 capped sample, R_{xy} is non-linear and negative for temperatures above 200 K, indicating electrons in the Si also conduct in parallel with electrons in the STO indicating very little charge transfer from Si to STO. For all temperatures above 200 K, R_{xy} remains negative and nonlinear for the 0.3 ML TiO_2 capped sample, indicating that there is no hole gas formation or at least below the threshold to make a

significant impact on R_{xy}. The smaller $n_{e,STO}$ measured in the 0.3 ML TiO_2 capped sample is consistent with little charge transfer from the Si oxygen impurities. For the 0.7 and 1.1 ML TiO_2 capped samples, R_{xy} remains negative and linear below the non-monotonic anomaly in R_s, indicating that transport is dominated by electrons in the STO, which is corroborated by the larger $n_{e,STO}$ measured for them. Both the 0.7 and 1.1 ML TiO_2 capped samples show a hole gas with onset temperatures of 350 and 300 K for 0.7 and 1.1 ML TiO_2 capped samples, respectively. This indicates that the thinner the TiO_2 cap, the higher the transition temperature for hole-gas formation. Based on the electrical transport properties, we expect a type-II (type-III) band alignment for the 0.3 ML (0.7 and 1.1 ML) TiO_2 capped heterojunctions.

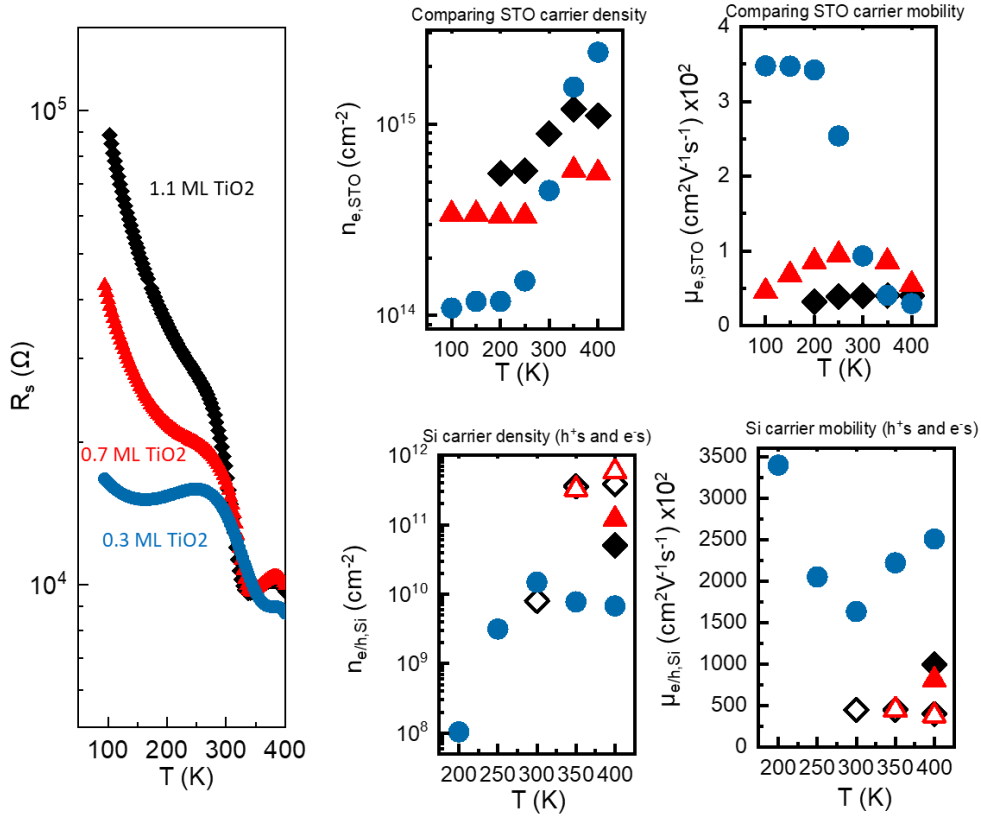

Figure 6.9: (Left) Sheet resistance as a function of temperature for the 0.3, 0.7 and 1.1 ML TiO_2 capped STO/Si heterojunctions. (Right) Carrier densities and mobilities of electrons (closed shapes) and holes (open shapes) in the STO and Si extracted from fits to the R_{xy} data.

Band edge profiles derived from fits to the hard x-ray core-level photoelectron spectra are shown in Figure 6.10. As the TiO_2 capping layer thickness is increased, the bulk Si CB shifts upward from below E_F for the 0.3 ML TiO_2 capped sample to above E_F for the 0.7 and 1.1 ML TiO_2 capped samples. In the interface region, the Si CB increasingly bends upwards with increasing TiO_2 coverage from no band bending for 0.3 ML TiO_2 coverage to ~1 eV band bending for the 1.1 ML TiO_2 capped heterojunction, indicating increased charge transfer with increasing TiO_2 coverage. The STO CB edge at the interface shifts downward with increasing TiO_2 thickness and the band alignment shifts from type-II to type-III. Both the absence of hole gas formation seen in electrical transport for the 0.3 ML TiO_2 capped sample and the presence of a hole gas for 0.7 and 1.1 ML TiO_2 capped samples is supported by the band edge profiles derived from hard x-ray spectra, with the VBO increasing with increasing TiO_2 thickness as shown in Figure 6.10. It is noted that the flat band region of the 0.7 ML and 1.1 ML TiO_2 capped samples is slightly further from E_F than for the 0.3 ML TiO_2 capped sample. Additionally, for the 0.3 ML TiO_2 capped sample, E_F lies above the Si CBM like the 1 nm BaO capped sample, which is consistent with electrical transport measurements that showed the presence of itinerant electrons in the Si for both samples. The position of the Si CBM relative to E_F indicates less charge transfer from the Si oxygen impurity donors to the STO for both the 0.3 ML TiO_2 and 1 nm BaO capped STO/Si heterojunctions.

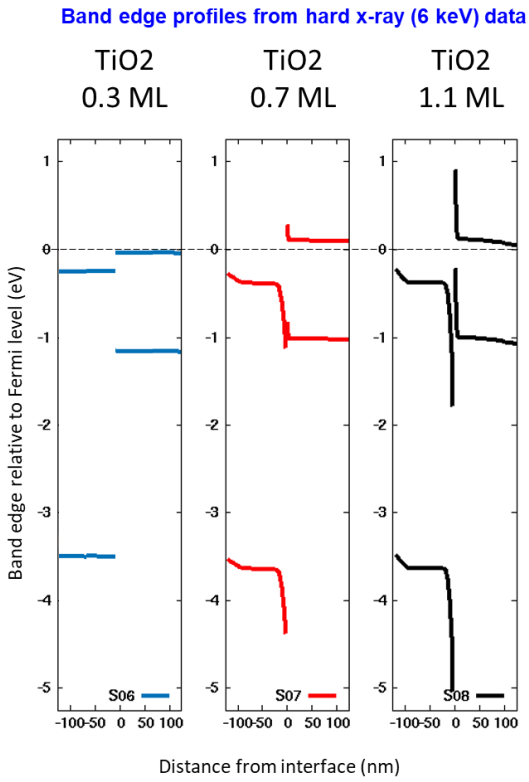

Figure 6.10: Band edge profiles extracted from fits to the HAXPES core-level spectra for the 0.3, 0.7 and 1.1 ML TiO_2 capped STO/Si heterojunctions. Si 2p, Ti 2p and Sr 3d core-level spectra for the TiO_2 capped STO/Si heterojunctions are shown in Figure 6.16.

Soft x-ray core-level spectra for the TiO_2 capped samples rules out differences in surface junk as driving the differences in electrical transport and band-edge profiles for the 0.3, 0.7 and 1.1 ML TiO_2 capped samples as shown in Figure 6.11.

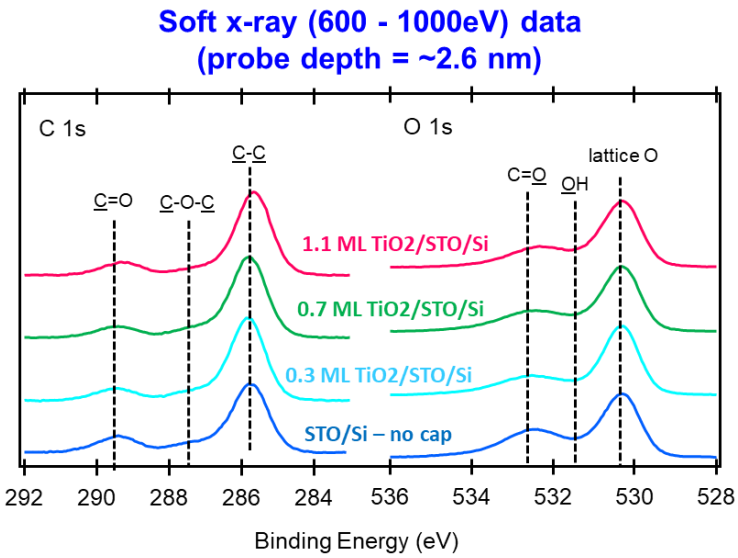

Figure 6.11: C 1s and O 1s soft x-ray core-level spectra for the uncapped and 0.3, 0.7 and 1.1 ML TiO_2 capped STO/Si heterojunctions indicate that there is no significant difference in surface junk between the samples.

Electrical transport data for 1.5 nm LaSTO/STO/Si, 1 u.c. aSTO/STO/Si, 1 u.c. BTO/STO/Si and uncapped STO/Si heterojunctions are shown in Figure 6.12. A systematic increase in R_s is seen for each capping layer with the lowest R_s being for the uncapped STO sample. The increase in R_s for each capping layer is consistent with the decreased electron carrier density measured in the STO for each layer. The non-monotonic anomaly in R_s and a crossover in sign of R_{xy} indicate that a hole gas is present for all four samples at elevated temperatures.

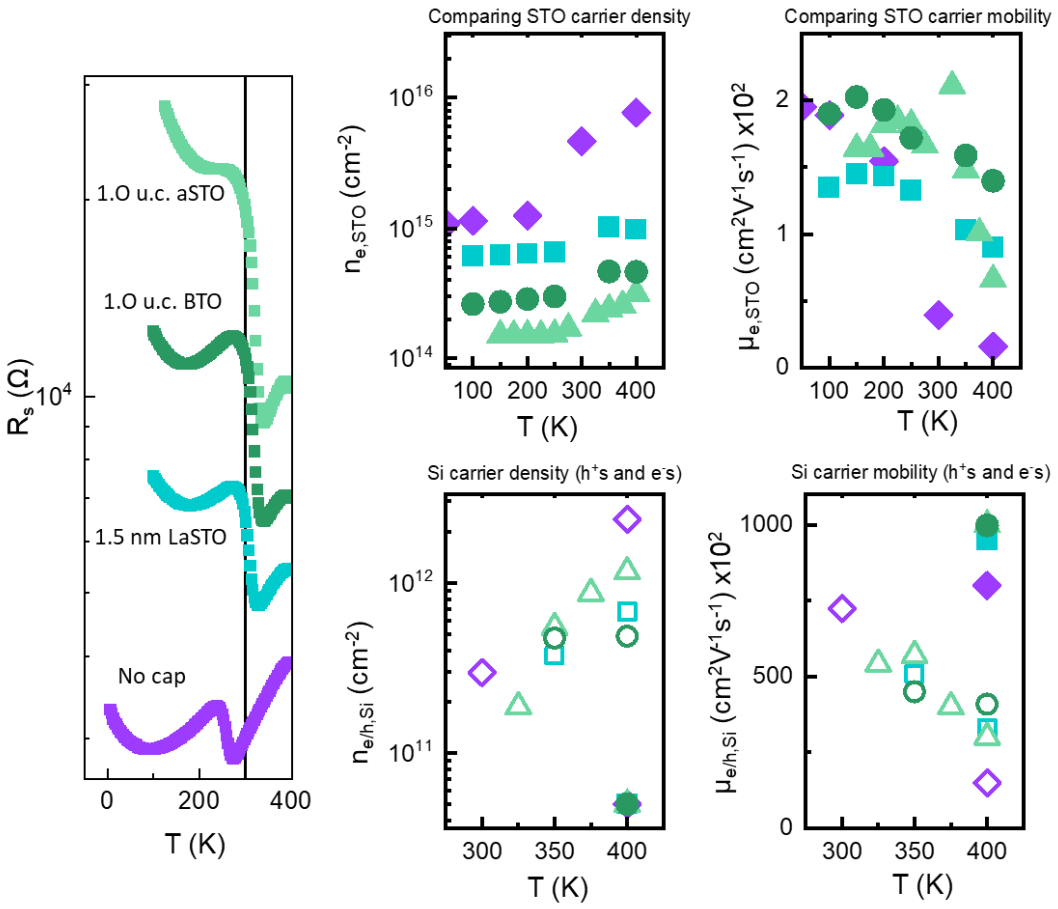

Figure 6.12: (Left) Sheet resistance as a function of temperature for the uncapped and 1.5 nm LaSTO, 1 u.c. BTO and 1 u.c. aSTO capped STO/Si heterojunctions. (Right) Carrier densities and mobilities of electrons (closed shapes) and holes (open shapes) in the STO and Si extracted from fits to the R_{xy} data.

Band edge profiles extracted from HAXPES core-level spectra measured at 300 K are shown in Figure 6.13. From left to right, the Si VB edge moves further away from E_F and the strong upward band bending seen in the Si for the uncapped sample decreases to a flat band in the 1.0 u.c. BTO capped sample. Since HAXPES spectra were taken at 300 K and the hole gas transition temperature for LaSTO, aSTO and BTO capped samples is ~325-350 K, it is expected that the Si VB edge would not cross E_F, which is corroborated by the band edge profiles derived

from core-level spectra. The STO CBM crosses E_F only in the uncapped STO/Si heterojunction, indicating that surface depletion increases charge transfer from Si to STO.

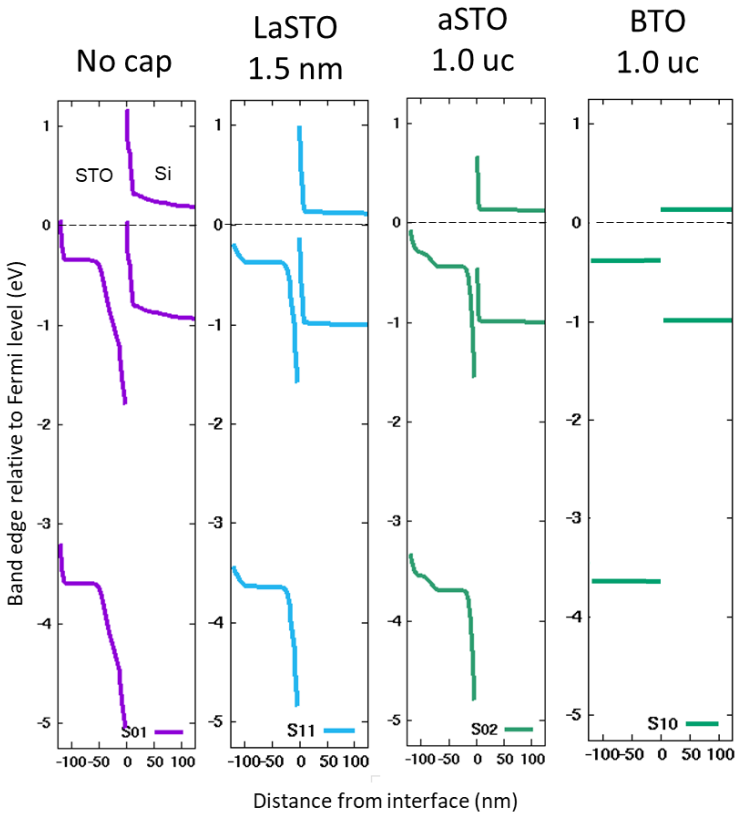

Figure 6.13: Band edge profiles extracted from fits to the HAXPES core-level spectra for the uncapped and 1.5 nm LaSTO, 1 u.c. aSTO and 1 u.c. BTO capped STO/Si heterojunctions. Si 2p, Ti 2p and Sr 3d core-level spectra for the heterojunctions are shown in Figure 6.16.

The interpretation of SrO capped samples is complicated by the fact that the SrO capping layer likely reacts with atmospheric water vapor. Sheet resistance and carrier densities and mobilities extracted from R_{xy} data for 0.3, 0.7 and 1.0 ML SrO capped samples are shown in Figure 6.14. Electrical transport indicates the presence of a hole gas for 0.3, 0.7 and 1.0 ML SrO capped samples from 350 – 400 K. However, HAXPES core-level spectra for SrO capped samples taken at 300 K are almost identical to the reference spectra, thus, all three show flat bands

throughout the heterojunction with a type-II band alignment, similar to what was observed for the 1 nm BaO capped sample.

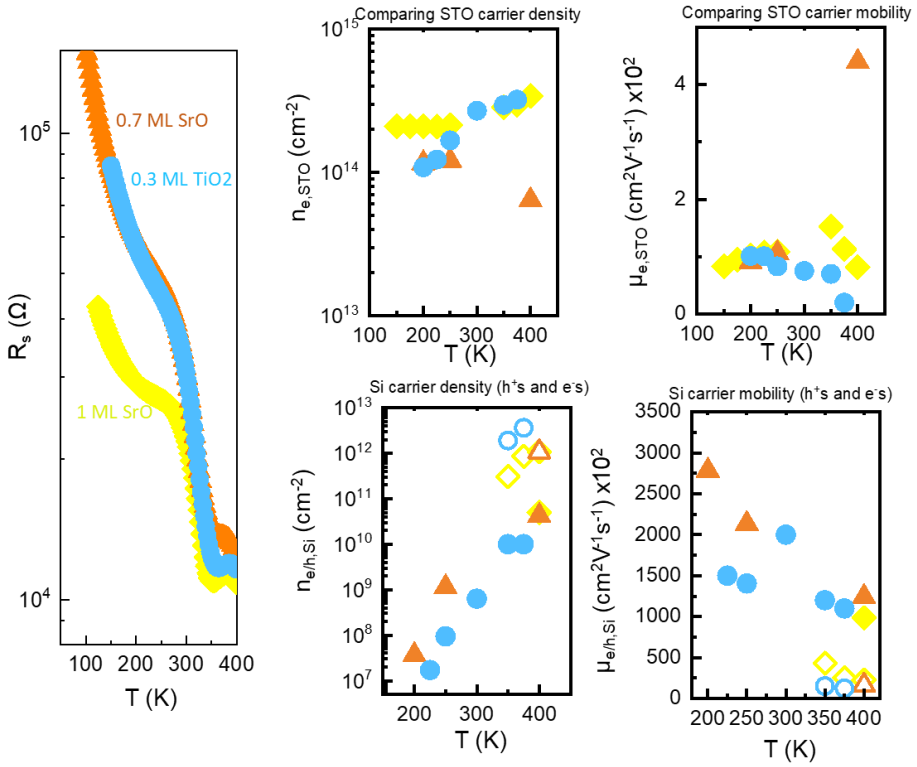

Figure 6.14: (Left) Sheet resistance as a function of temperature for the 0.3, 0.7 and 1 ML SrO capped STO/Si heterojunctions. (Right) Carrier densities and mobilities of electrons (closed shapes) and holes (open shapes) in the STO and Si extracted from fits to the R_{xy} data.

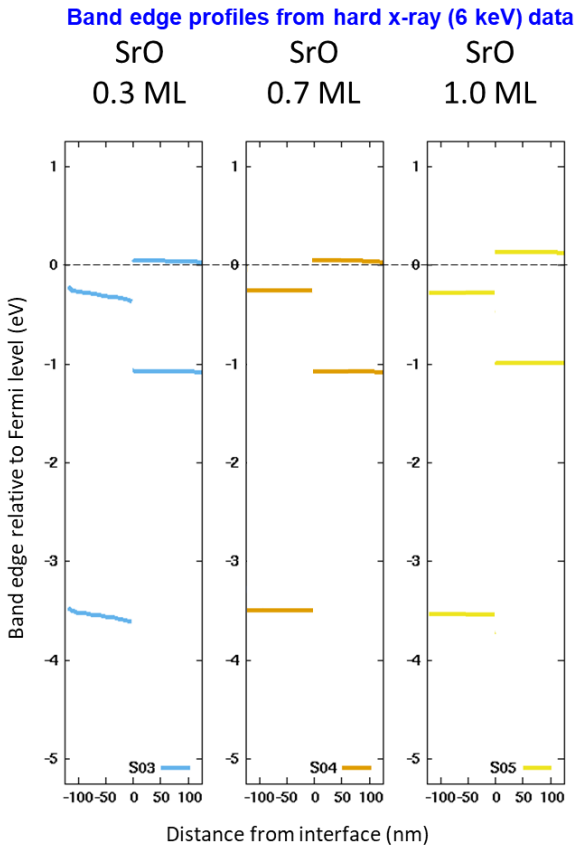

Figure 6.15: Band edge profiles extracted from fits to the HAXPES core-level spectra for the 0.3, 0.7 and 1 ML SrO capped STO/Si heterojunctions. Si 2p, Ti 2p and Sr 3d core-level spectra for the SrO capped heterojunctions are shown in Figure 6.16.

Si 2p, Ti 2p and Sr 3d HAXPES core-level spectra for all 11 samples are shown in Figure 6.16, along with phase pure reference spectra. Most of the samples show little to no core-level broadening or lower valence features in the Ti 2p core-levels. Samples that do show significant core-level broadening and lower valence Ti 2p features associated with charge transfer from Si oxygen impurities to STO are the 1.5 nm La-STO/STO/Si, 1.1 ML TiO_2/STO/Si, 0.7 ML TiO_2/STO/Si, 1 u.c. aSTO/STO/Si and the uncapped STO/Si heterojunctions, which is consistent with the measured electrical transport properties of the heterojunctions.

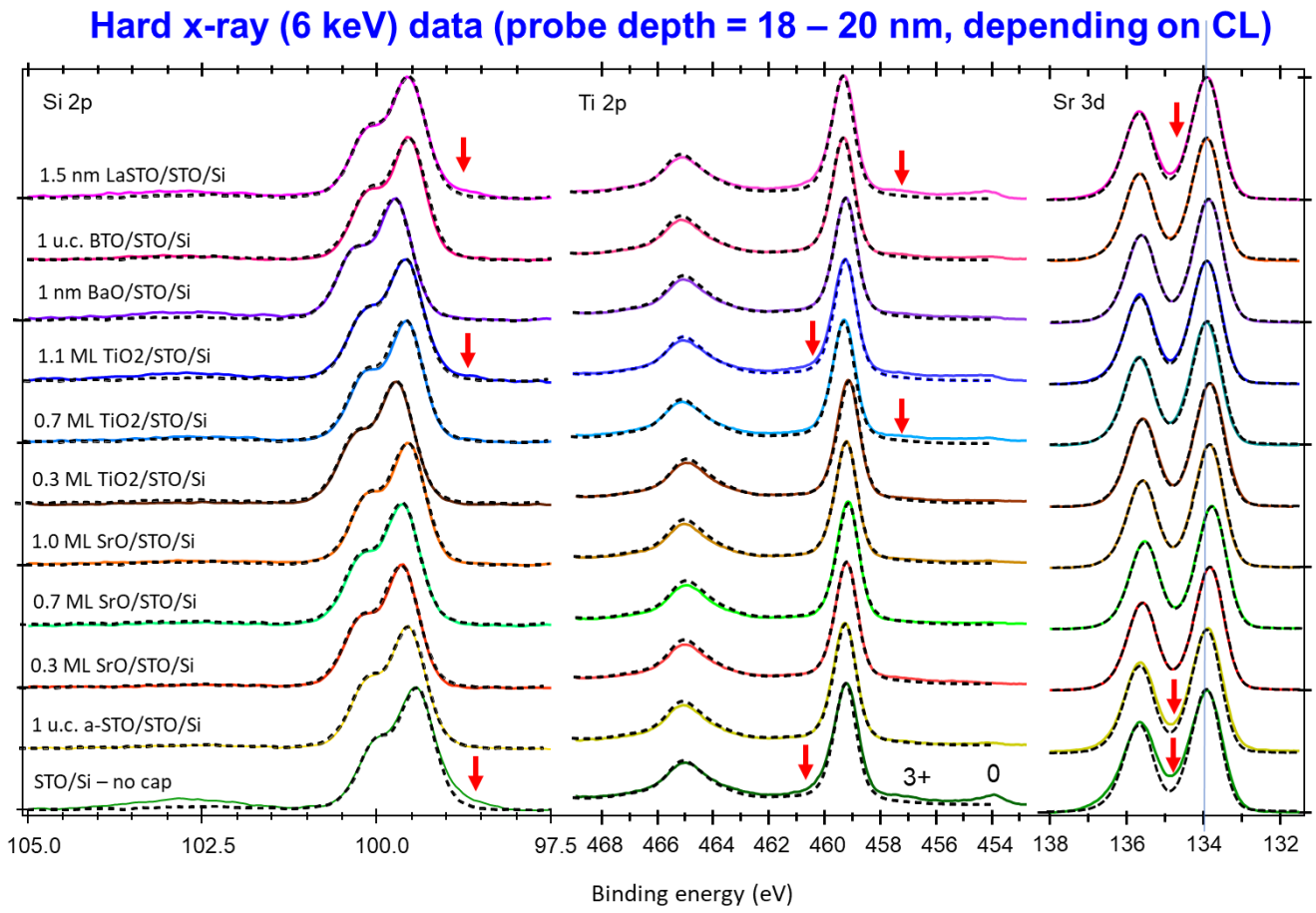

Figure 6.16: HAXPES Si 2p, Ti 2p and Sr 3d core-level spectra for all capped and uncapped STO/Si heterojunctions. Red arrows are used to indicate some of the core-level broadening associated with built-in electric fields in the heterojunctions.

Soft x-ray photoelectron Sr 3d and Ti 2p spectra for all 11 samples is shown in Figure 6.17. Since the lower binding energy of soft x-rays gives a lower probe depth, any core-level broadening or asymmetry must be due to built-in fields near the STO surface. Again, we see little difference in many of the spectra taken at room temperature compared to the bulk reference spectra. Samples that show broadening are the 1.5 nm La-STO/STO/Si, 1.1 ML TiO_2/STO/Si, 0.7 ML TiO_2/STO/Si and the uncapped STO/Si heterojunctions. Note that the magnitude of the near surface core-level broadening is less than the broadening seen in hard x-

ray spectra, indicating that any band bending near the surface is weaker than it is further into the sample.

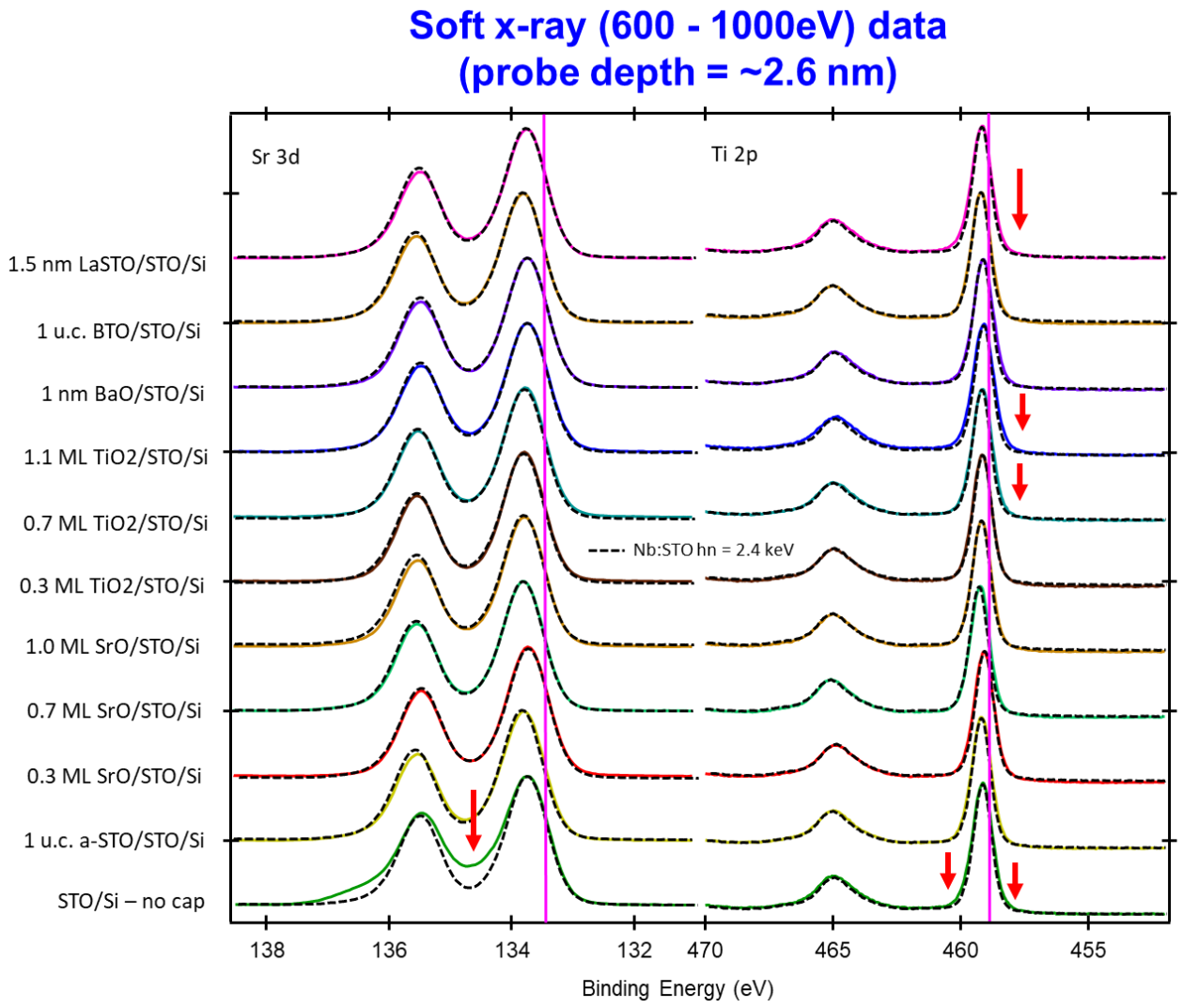

Figure 6.17: Sr 3d and Ti 2p core-level XPS spectra for all capped and uncapped STO/Si heterojunctions. Red arrows indicate core-level broadening associated with built-in electric fields in the heterojunctions.

Additionally, soft x-ray C 1s and O 1s core-level spectra for all 11 samples are shown in Figure 6.18, indicating that there are similar species and amounts of surface junk on all samples.

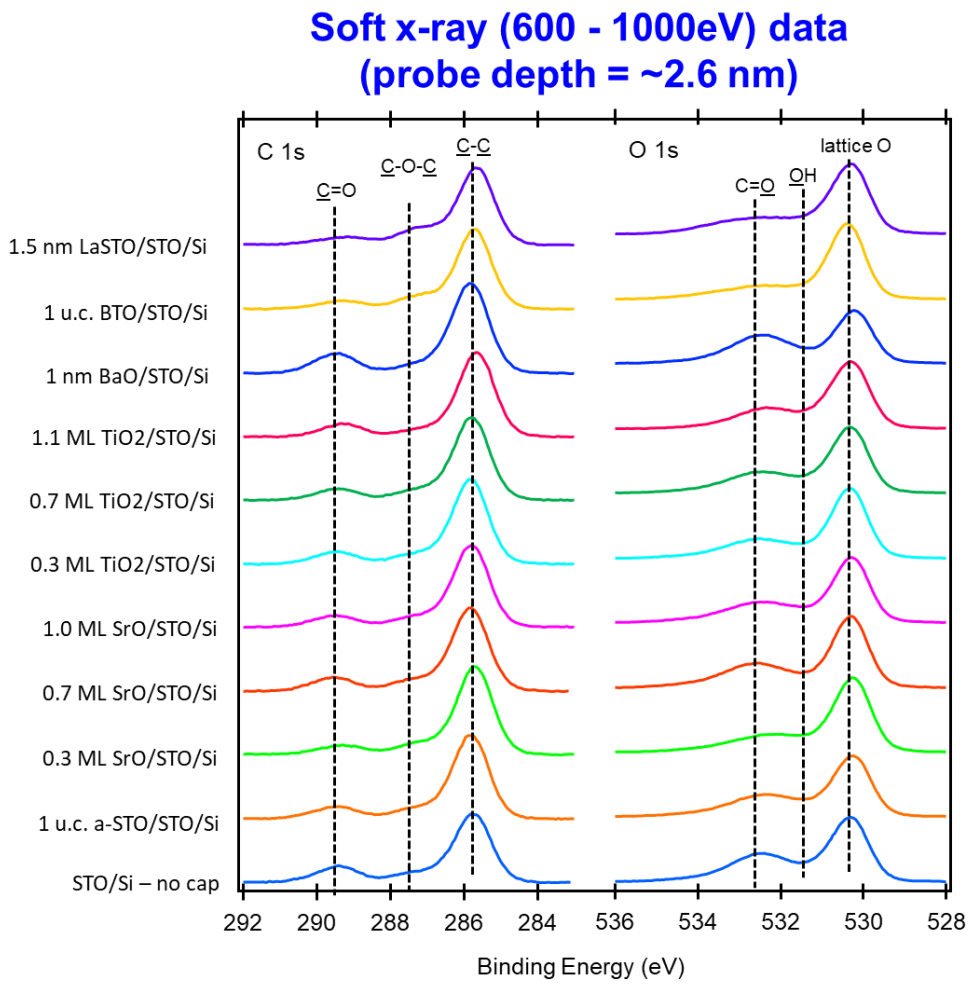

Figure 6.18: C 1s and O 1s core-level XPS spectra for all capped and uncapped STO/Si heterojunctions.

6.4 Conclusions

While the addition of theoretical modeling of surface capping layers is needed to fully understand the effects on charge transfer across the STO/Si interface, there are some general things that can be drawn from the results. The addition of any of the capping layers used here acts to inhibit charge transfer across the buried STO/Si interface. Capping layers that do not contain Ti inhibit charge transfer more than capping layers that contain Ti. Additionally, there is no significant difference in surface junk present on samples with different capping layers. Both

electrical transport and photoelectron spectroscopy measurements indicate that sub-monolayer surface coverage is sufficient to inhibit hole gas formation at room temperature as the onset of hole gas formation all samples with a cap is pushed to higher temperatures.

Chapter 7: Deposition-last lithographically defined device structures on Si

7-1: Introduction

Complex oxides exhibit a wide array of interesting electrical properties that could potentially be used to create new devices that exhibit properties not found in semiconducting heterojunctions. Perovskite oxides with the ABO_3 structure are particularly interesting because many different properties can be realized by substitution of A- and B- site cations in the structure [7.1, 7.2]. For example, heterojunctions formed between $LaAlO_3$ and $SrTiO_3$ have been shown to form a high mobility electron gas despite both oxides being insulators in the bulk [7.3]. While there are many interesting phenomena that appear at oxide-oxide heterojunctions, large scale manufacturing of single crystal oxide substrates is not yet achievable. In this regard, the epitaxial growth of perovskite oxides on semiconductors provides a pathway in which the interesting properties of perovskite oxides can be integrated with technologically relevant substrates such as Si.

To create devices out of thin film heterojunctions requires the use of some type of patterning technique which can involve both wet and dry etching. Top-down approaches such as lithography are typically used to create devices in which the film is first grown and then devices are formed by etching away the unwanted material layers. This involves the use of an etch mask (photoresist or other material) to define a device area in which different layers must be selectively etched away using wet and dry-etch techniques. This requires a method that can selectively etch away the film layer without etching the mask or other layers of material, and specific recipes must be developed to do so [7.4]. Wet etching techniques are isotropic in nature and undercutting of the film layer means that there is a scaling limit that must be considered when creating devices with wet etching. Dry etching can be anisotropic but requires specific recipes to be developed for different oxides.

Alternative approaches have been developed to create devices using a hard mask layer that is deposited on the substrate before epitaxial growth [7.5, 7.6, 7.7]. The use of a hard mask

layer requires that the masking layer be compatible with the epitaxial growth process including oxidizing conditions and high temperatures required for epitaxial growth. In this regard, oxides themselves are typically used as masking layers since they can withstand the oxidizing conditions and high temperatures. Another challenge with using a hard mask layer during film growth is shadowing effects of the masking layer which limits device scaling.

Here we discuss the development and use of a deposition-last process in which we created devices out of epitaxial STO on Si(100) substrates by use of a pseudo-mask created by texturing the Si outside of the desired device region. The process involves texturing the Si with a combination of wet and dry-etching where the device region is first defined with a photoresist pattern and the Si outside of that region is textured by CF_4 dry etching and subsequent wet etching in a tetramethylammonium hydroxide (TMAH) solution. The idea is to roughen the Si surface such that film crystallization will be inhibited.

7-2 Experiment and Results

The mask design used in this project is shown in Figure 7.1. The central square region allows the use of RHEED during epitaxial growth. This region will be covered with photoresist during the etching process so that the final wafer will have epi-polished Si in the central square. Surrounding the central square is a series of 5x5 mm^2 lots containing Hall bar devices with varying widths and the outermost patters are variable sized pads for capacitance-voltage measurements (not used in this project). To facilitate XRD and electrical transport of films grown on textured areas, two 5x5 mm^2 regions are left open such that they will undergo texturing during the etching process. XRD and electrical transport measurements of films grown on epi-polished Si can be measured from samples taken from the central square. Mask alignment is done using the fiducial marks at each corner of the mask. The large “C” in the bottom left corner is to facilitate alignment and wafer dicing.

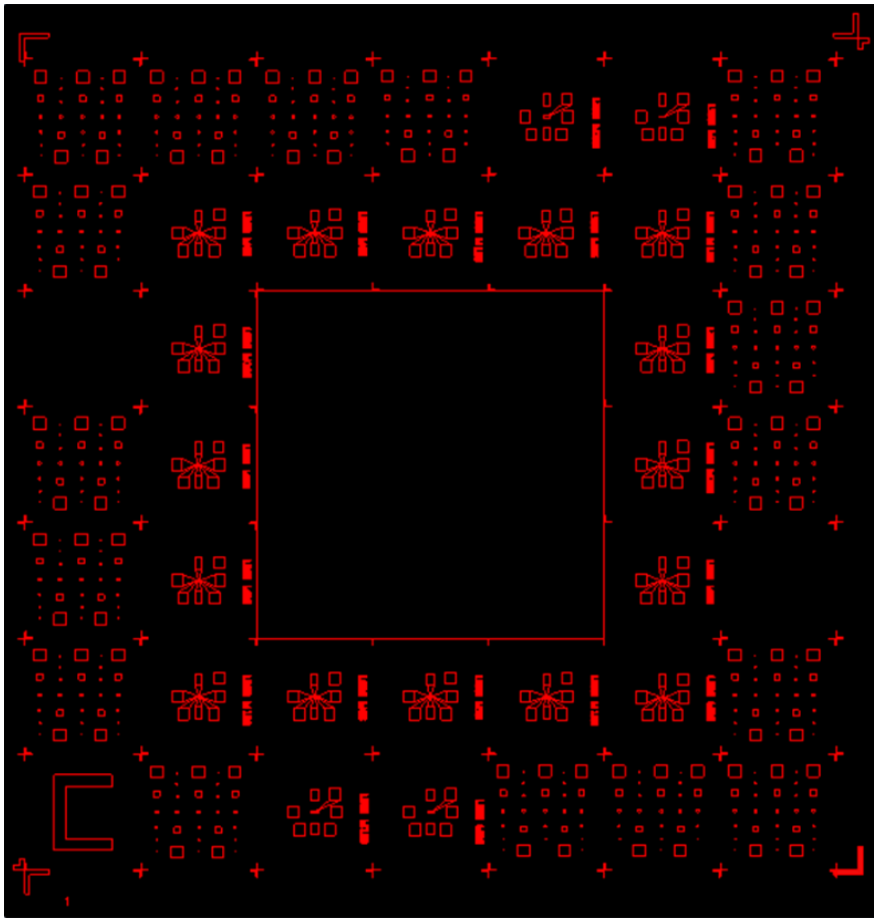

Figure 7.1: Mask design for deposition-last devices. The central square is used to facilitate RHEED during epitaxial growth. The wafer is portioned into 5x5 mm^2 lots in which each lot contains one device. Lots are separated after film growth by dicing along the fiducial lines.

Initial attempts at defining device regions involved etching in a heated potassium hydroxide (KOH) solution which readily etches the Si [7.8], however, KOH etching will leave excess K + ions on the silicon surface and we find that while this does allow for clean Si surfaces to be seen in RHEED, STO films did not crystallize despite seeing all reconstructions up to 1.5 ML SrO coverage. TMAH is a good alternative to KOH etching as it does not leave any residual ions on the Si surface after etching and has been successfully used to texture Si surfaces for

solar cell applications [7.9]. In particular, the surface roughness is a key factor for improving light trapping in solar cells which increases their efficiency.

Previous studies have shown that TMAH etching of Si surfaces is highly dependent on etching parameters such as TMAH concentration and etching temperature. In general, high (> 25 %) TMAH solutions result in smooth Si surfaces and low concentrations (~5 %) result in rough surfaces [7.10]. The difference stems from the fact that TMAH etching is anisotropic and etch rates vary with crystallographic planes and etching parameters. J. S. You et al. measured the etch rate variations as a function of etching temperature and TMAH concentration for (111) and (100) planes for low TMAH concentrations [7.11].

P. Papet et al. showed that the addition of a surfactant, in this case isopropanol, will result in a more uniform Si surface roughness [7.9]. While we found this to increase the size of the pyramidal hillocks created during etching, they are still separated by smooth Si regions as shown in Figure 7.2.

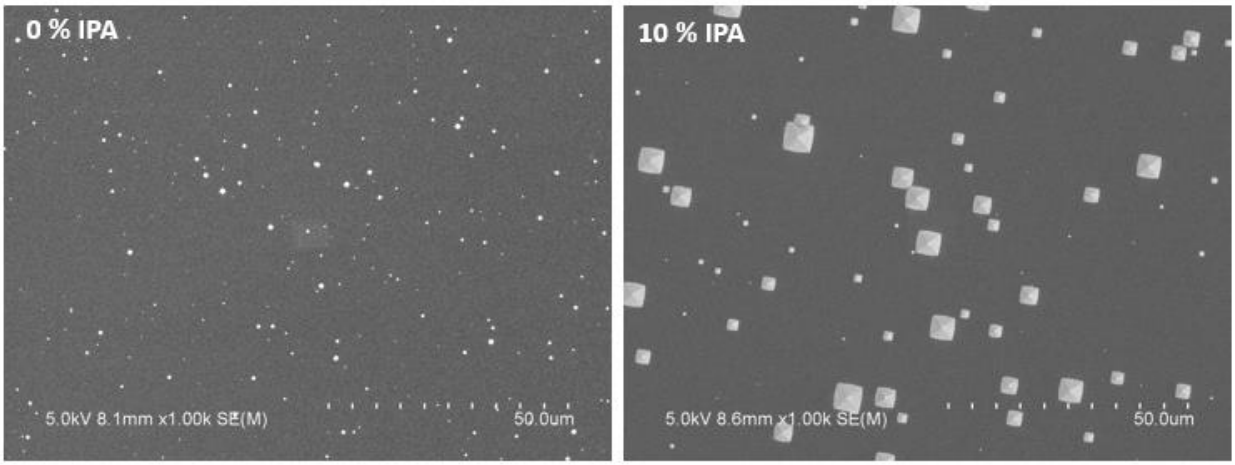

Figure 7.2: (a) and (b) are SEM images of a Si surface etched 20 min in a 5 % TMAH solution at 75 °C without IPA and with 10 % IPA, respectively.

We find that to achieve uniformly rough surfaces the Si surface must be roughened before TMAH etching. As shown in Figure 7.4 below, the surface can be roughened during dry-etching with CF_4, and the roughness increases with increasing etch time up to ~15 min. Average

roughness values were measured using AFM for 0 min, 5 min, 10 min and 15 min RIE etching and found to be 0.28 nm, 4.7 nm, 8.9 nm and 8.6 nm, respectively.

Longer dry-etch times are not achievable with our current process since a thicker photoresist layer is necessary to hold up under longer CF_4 etch times. At 20 min RIE etching the photoresist layer was etched through, damaging the epi-polished Si underneath. If the RIE etching step is followed with a TMAH etching step, a uniformly rough Si surface can be achieved as seen in Figure 7.3 below.

The process flow to create lithographically defined device structures on a 2" diagonal square piece of Si is shown in Figure 7.3.

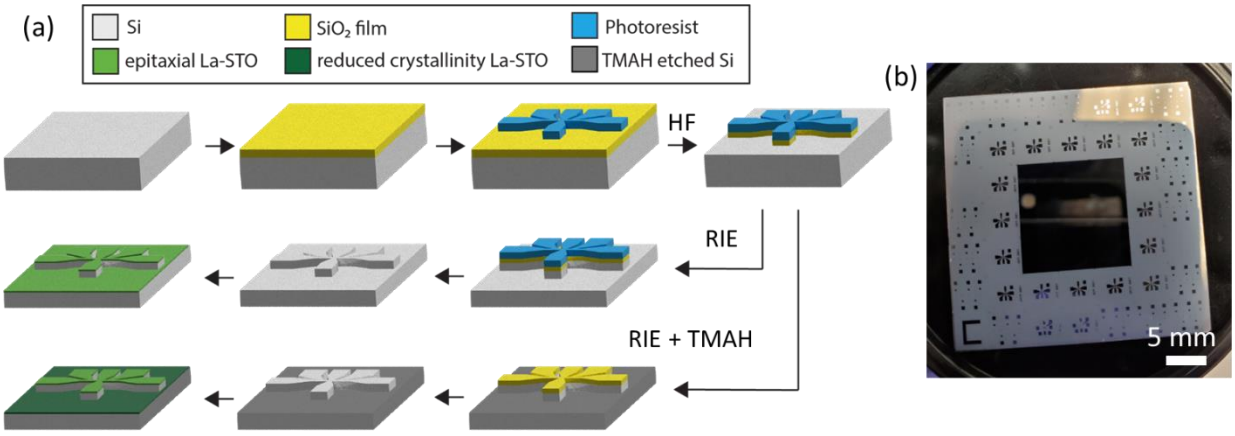

Figure 7.3: (a) Schematic of the process flow to create a deposition-last device. (b) Optical image of an RIE and TMAH etched substrate [7.12].

The Si wafers used in this project are 4" in diameter, nominally undoped, (100) oriented, CZ grown wafers from Virginia Semiconductor. 4" wafers were diced all the way through into 2" diagonal square pieces using a Disco Dad3220 dicing saw. The wafers must be cleaned immediately following dicing to prevent adhesive from the dicing tape or excess Si from the dicing process from sticking to the surface which is very difficult to remove later. The wafers were washed in an ultrasonic bath of acetone, methanol, and isopropanol for 10 min each, then blow dried with dry N_2 gas. The wafers were examined under an optical microscope to ensure

all residue from the dicing process was removed. If there is still some residue, an additional 3-step cleaning process must be done. After the wafers are cleaned, a 120 nm SiO_2 hard mask was deposited on the surface using a Trion Orion II LPCVD system at 360 °C. Photoresist (Shipley 1813, positive photoresist) is then spun onto the SiO_2 surface using the following recipe which results in a ~1.2 μm thick photoresist layer as measured using a profilometer (profilometer name):

1. Spread – ramp from 0 - 500 rpm at 100 rpm/s
2. Spin – ramp from 500 rpm - 4000 rpm at 1000 rpm/s and spin for 60 s
3. Stop – ramp from 4000 rpm - 0 rpm at 1000 rpm/s

The wafer is then soft-baked on a hotplate at 115 °C for 1 min. Following the soft-bake step, the wafer is loaded into an OAI Backside Aligner to expose the masked wafer to ultraviolet (UV) light for 11 s at a power density of (insert here). After exposing to UV light, the wafer is baked again on a hotplate for 1 min at 110 °C to harden the photoresist which was not exposed to UV. The photoresist pattern is then developed in MF-319 developer for a total of 45 s, with the developer shaken around between 15-20 s, 30-35 s, and 40-45 s, then rinsed in de-ionized water 3-4 times and blow dried with dry N_2. Photoresist patterns are inspected under an optical microscope to ensure they are fully developed and that the photoresist adheres well to the SiO_2 surface. For thick SiO_2 layers photoresist will sometimes have trouble adhering to the oxide and will peel up and come off the surface. There are a few things that can be done to increase adhesion: bake the wafer at ~150 °C on a hotplate for 30 min (removes moisture) or spin on an additional layer of (forgot name) which is designed to increase adhesion of photoresist to the oxide layer. After inspection of the photoresist pattern, wafers are etched in 10:1 $HF:H_2O$ solution for ~30 s to etch away the exposed SiO_2 layer. This step ensures that there is very little to no oxide left in the exposed region since the following dry etch step will etch Si and SiO_2 at different rates (insert etch rates here). Wafers are then dry etched in a Technics Macro Series 8800 RIE in 150 mT mixture of 96 % CF_4, 4 % O_2 background at 400 W, 30 kHz RF power for three 5 min intervals. This step etches the exposed Si at a rate of ~120 nm/min. It was found that the Si surface roughness increases with increasing etch times up to a ~10 min. Figure 7.4 shows AFM topography scans for as-diced and 5, 10 and 15 min CF_4 etching times.

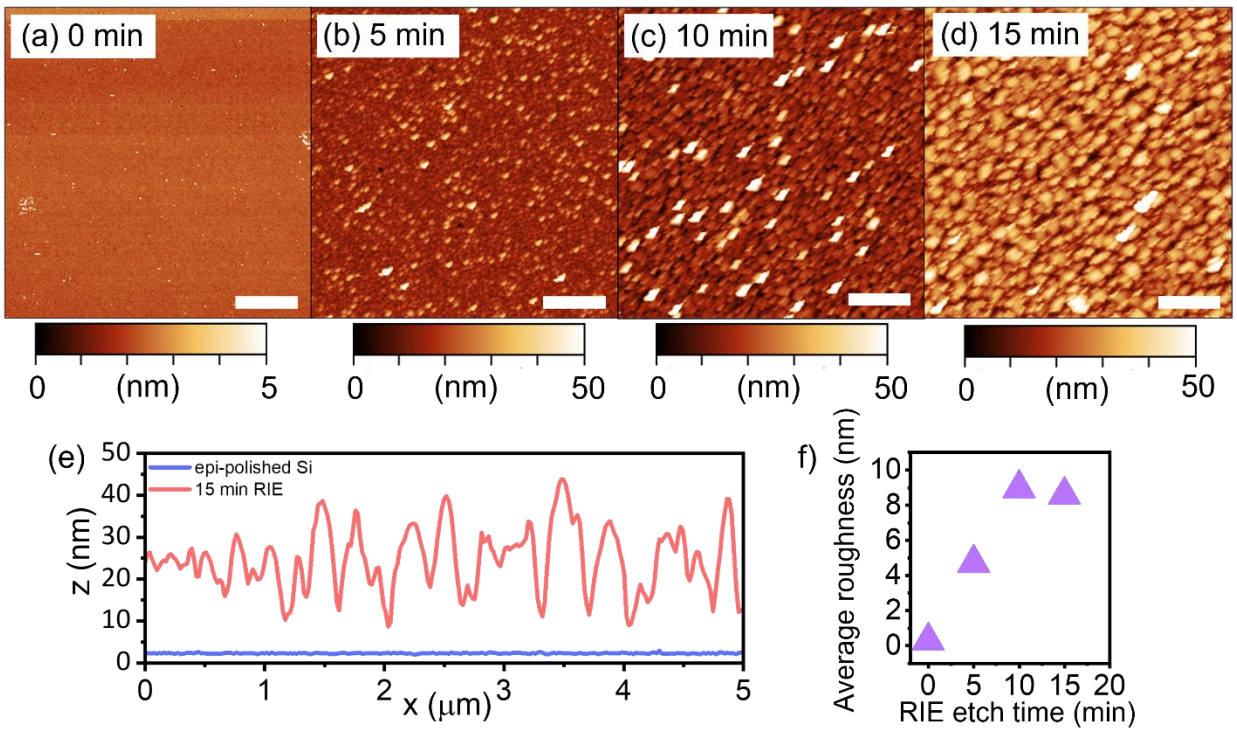

Figure 7.4: (a) AFM topography scan of a pristine, epi-polished Si surface. (b), (c) and (d) AFM topography scans of 5 min, 10 min and 15 min RIE etched Si surfaces. The white scale bars are 1 μm. (e) Topography line scans for epi-polished Si and 15 min RIE etched Si. (f) Average roughness, R_a, as a function of RIE etch time [7.12].

If this is the desired device structure and background surface roughness, then the TMAH etching step can be skipped. An additional TMAH etching step must be done to inhibit the crystallization of MBE grown oxide layers. To do this, wafers were first etched briefly (10 s) in 10:1 HF dip to remove any native oxide, then etched in 5% TMAH, 10% IPA, 85% DI water solution heated to 80 °C for 6.5 min. This time was chosen based on several factors including the TMAH etch rate of LPCVD grown SiO_2 (etches faster than thermal SiO_2), desired surface roughness (to inhibit MBE grown layer crystallinity) and undercutting factors (discussed in). After removing the wafer from the TMAH solution, it is thoroughly rinsed with DI water to remove any excess etching solution. During TMAH etching we find that the photoresist is completely etched away and (look up) some amount of the SiO_2 is etched away with pinholes

etched through it. This may be due to the poorer quality of LPCVD SiO_2 as compared to thermal SiO_2. Pinholes can still be seen after removing the SiO_2 layer Figure 7.5.

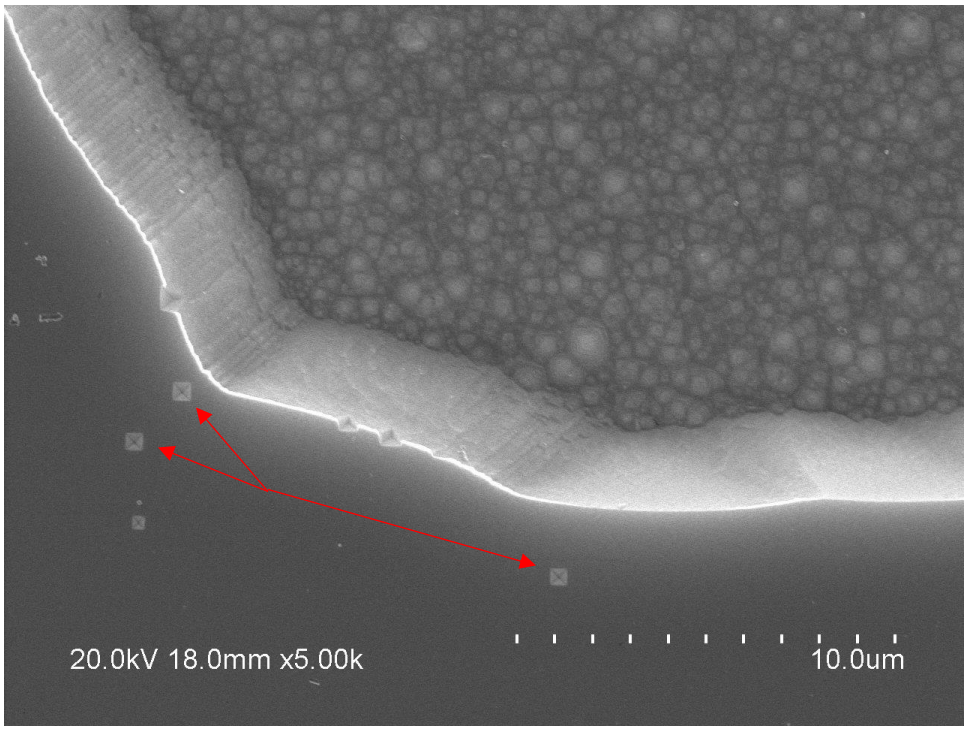

Figure 7.5: SEM image of a finished device revealing pinholes in the SiO_2 layer formed during TMAH etching can be seen on the final device surface as etch pits.

After TMAH etching and rinsing, the wafers are again cleaned using the 3-step cleaning process to make sure all residual photoresist is removed from the wafer. The SiO_2 mask is then removed by dipping into a 10:1 HF solution for ~5 min, which should result in the surface being hydrophobic (no SiO_2 remaining). Wafers are then loaded into the MBE chamber for La-STO growth.

The MBE growth of STO on Si(001) is described in detail in section 3.3 but additional information specific to growth on patterned Si substrates is provided here. To facilitate growth, the center of the pseudo-mask contains no device areas as can be seen in Figure 7.1 and 7.3 (b) so that the RHEED electron beam can still be utilized in the epitaxy to observe surface

reconstructions during the process. The high temperature required to desorb the native SiO_x layer is not compatible with hard masks that would breakdown or react with the Si at those temperatures, however, since the pseudo-mask used here is made entirely of Si this presents no problem here. A 6.5 u.c. thick STO film is grown which acts as a buffer layer for the 32 UC $La_{0.1}Sr_{0.9}TiO_3$ (12 nm) to be deposited at 580 °C. RHEED of clean, dimerized Si(100) and the final 15 nm La-STO film can be seen in Figure 7.6 (d), (e), (f) and (g). The wafer is then diced into 5x5 mm lots in which SEM images of one of the devices can be seen in Figure 7.6.

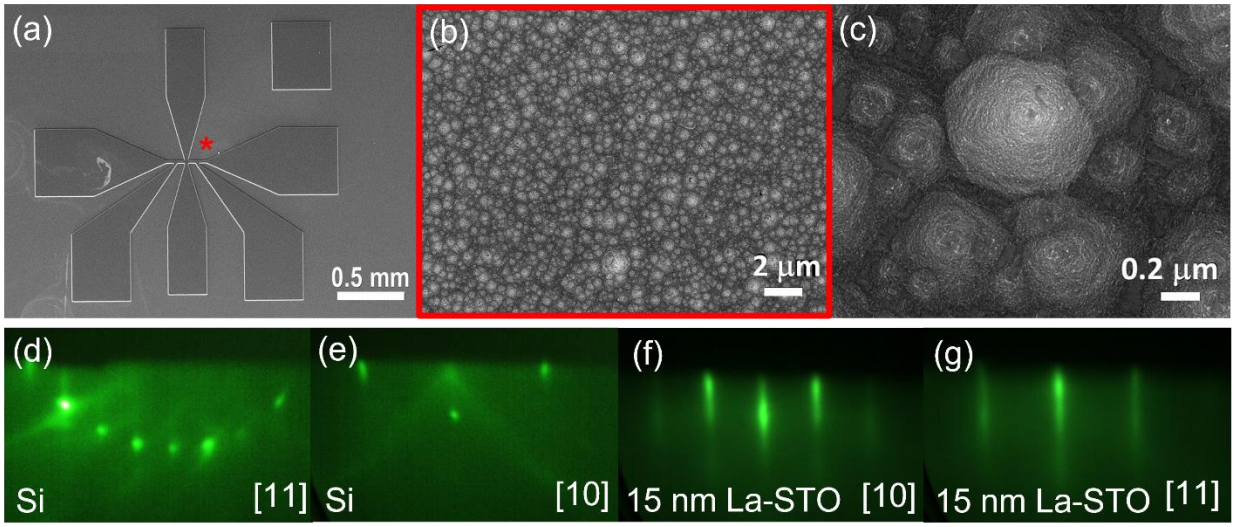

Figure 7.6: (a) SEM image showing a finished device. (b) and (c) show enhanced areas marked with the red * in (a). (d) and (e) show RHEED images along the [11] and [10] azimuths after desorption of the native oxide. The 2x1 structure seen in the [11] direction indicates a clean, reconstructed Si surface. (f) and (g) RHEED images of a 15 nm La-STO film along the [10] and [11] azimuth, respectively [7.12].

Devices were also made from a wafer RIE etched 15 min in a RF generated CF_4 plasma and samples from etched regions and center regions of both were analyzed using x-ray diffraction (XRD).

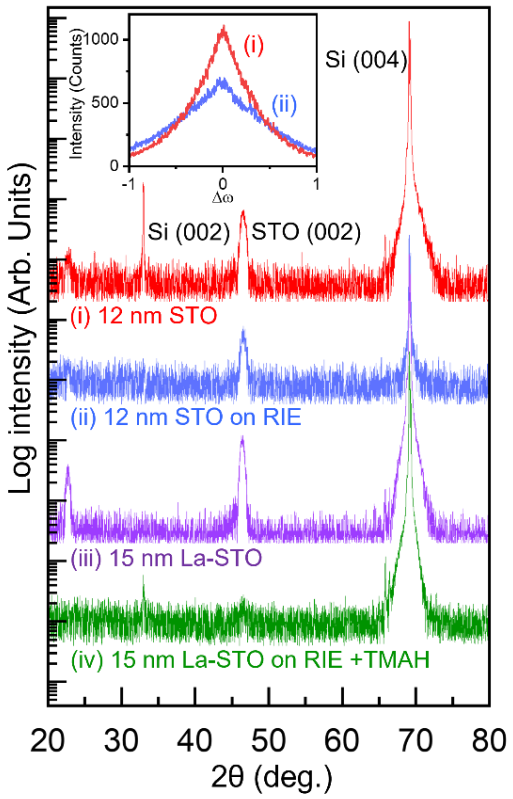

Figure 7.7: Survey scans of a 12 nm STO/Si heterojunction grown on pristine and RIE etched Si surfaces and 15 nm La-STO/Si heterojunction grown on pristine and RIE + TMAH etched surfaces. The inset shows rocking curves for the 12 nm STO/Si heterojunction on pristine and RIE etched Si [7.12].

As can be seen in Figure 7.7, films grown on wafers with pseudo-masks created using only RIE still show single crystal STO can be grown despite the rougher surface present in the pseudo-mask region. The inset of Figure 7.7 shows a rocking curve comparison of 12 nm STO grown on pristine Si and the RIE etched region, indicating reduced crystallinity for STO grown on the RIE etched surface. However, for the 15 nm La-STO grown on RIE + TMAH etched Si, the STO (002) peak is barely visible above the background indicating very poor film crystallinity in the rough region.

Electrical transport measurements of a 15 nm La-STO/Si heterojunction Hall bar device are shown in Figure 7.8. As shown in a previous study [7.13], doped $SrTiO_3$ grown epitaxially on

Si(100) shows 2-channel conduction with electrons in the STO and holes in the Si. This is manifested in the electrical transport as a non-monotonic anomaly in R_s and a crossover in sign in R_{xy} from positive to negative is the temperature is lowered. Above the crossover point, holes in the Si conduct in parallel with electrons in the STO, while below the crossover electrons in the Si conduct in parallel with electrons in the Si. This can be explained if the band alignment shifts from type-II (staggered gap) to type-III (broken gap) where the Si valence band crosses the Fermi level. As shown in previous studies (Chapter 5), the change in band alignment from type-II to type-III results from modulation of the interface dipole due to electron transfer from oxygen donors in the Si to STO. The resulting space-charge modifies the interface dipole to change the band alignment from type-II to type-III.

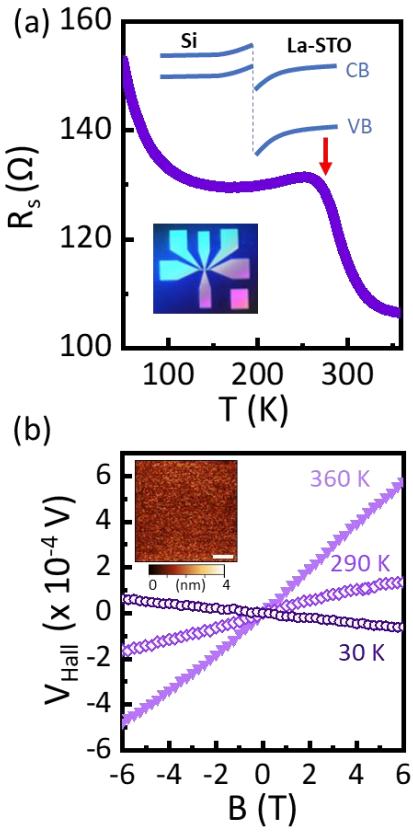

Figure 7.8: (a) Sheet resistance as a function of temperature for a 15 nm La-STO/Si Hall bar device. Insets are a diagram of the band-alignment expected from the electrical transport and an optical image of a 15 nm La-STO/Si Hall bar device. (b) Hall voltage as a function of applied magnetic field and temperature. An AFM topography scan of a 15 nm La-STO surface [7.12].

The presence of a hole gas at high temperatures is consistent with having an interface free of any SiO_x that would inhibit charge transfer across the heterojunction, demonstrating that high quality interfaces can be retained despite aggressive RIE and TMAH etching of the wafer. The inset of Figure 7.9 (b) shows a smooth, featureless La-STO surface.

A drawback of using wet etch techniques is that they often produce undercutting. TMAH etching Si is anisotropic and etch rates in different crystallographic directions changes with TMAH concentration and the temperature of the etching solution. The etch rate ratio of (111) to (100) planes can be up to an order of magnitude higher than other anisotropic alkaline-based etchants such as KOH.

Landsberger et al. [7.14] explain the formation of hillocks on TMAH etched Si surfaces as being due to the sensitivity of the etch rate of (101) planes with Si concentration dissolved into the TMAH. As the dissolved Si content increases, the etch rate of (101) planes decrease compared to (100) planes, which occurs for low TMAH concentrations. The undercutting etch rate was measured by J. You et al. [7.11], and it was found that the undercutting etch rate decreases with higher TMAH concentration and increases with higher temperature. An undercutting etch rate of 50 nm/min was measured for a photoresist pattern aligned to the <110> direction with a 5% TMAH solution at 80 ^{o}C. Our experimentally determined (100) etch rate of 250 nm/min means that ~20% of the device may be undercut during the etching. Decreasing the undercutting ratio can be achieved by increasing the TMAH concentration although there is a trade off with surface roughness. It has been found that above ~22% TMAH concentration there are no pyramidal hillocks formed during the etching process [7.10]. In addition, it has been shown that adding a surfactant (IPA) to the etching solution decreases the undercutting ratio [7.15].

7-3 Conclusions

In conclusion, we developed a method to texture a Si substrate to inhibit the epitaxial growth of perovskite oxides outside of the defined device regions. We showed that we can still

obtain clean, reconstructed Si surfaces and that high quality interfaces between epitaxial oxides and Si can be created despite aggressive processing of the wafer. This method allows for semiconductor-crystalline oxide device structures to be created without the need to develop specific etching recipes for various oxides because the film is grown after the device regions are defined.

Chapter 8: Conclusions

In Chapter 5, we demonstrate that the band alignment at a semiconductor-crystalline oxide interface can be tuned through modification of the interfacial dipole by introducing space charge across it. Since the interfacial dipole is modified through electric fields that arise from the transfer of itinerant electrons from Si to STO, we establish that band alignment can be modified through doping. We show that the band alignment can be tuned from type-II to type-III by increasing the oxygen impurity content in the Si be either growing on wafers with higher oxygen impurity content or by growing thicker STO films. Additionally, modification of substrate bulk doping levels was found to decrease charge transfer from Si to STO. In Chapter 6, we explored the effects of the surface termination of STO/Si heterojunctions. It was found that the addition of any capping layer acted to inhibit charge transfer from the Si to STO which varied with capping layer elemental composition and thickness. Capping layers as thin as 0.3 ML were found to give significantly different electrical transport properties than uncapped STO/Si heterojunctions grown on identical substrates with identical growth conditions. Theoretical analysis is needed to fully understand the effects of capping layers on the band alignment at the buried STO/Si interface.

In Chapter 7, we present a new process for creating devices from semiconductor-crystalline oxide heterojunctions in which the epitaxial layer is deposited after substrate patterning to prevent the need for specific etching recipes to be developed. The wafer is textured through a combination of wet- and dry-etching techniques such that the epitaxial oxide device layer sits above the textured substrate to prevent shadowing effects during deposition. This method could potentially be used to create devices from a wide variety of epitaxial oxides on semiconductors.

The ability to the tune band alignment at hybrid heterojunctions sets them apart from conventional semiconductor heterojunctions which have relatively weak interfacial dipoles and longer screening lengths. In principle, a combination of band gap engineering and space charge modification of the interface dipole could allow for a wide variety of band offsets and built-in potential profiles to be realized in semiconductor-crystalline oxide heterojunctions.

Electrostatic altering of band alignment opens additional pathways to realize functional behavior in semiconducting hybrid heterojunctions.

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