ASSESSMENT OF JOULE HEATING PROPERTIES OF VARIOUS SOLDER ALLOYS IN BGA ASSEMBLY

by

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Thesis

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DEDICATION

To my parents and sister, for unconditionally showing love and support throughout this time of my life.

To the rest of my family and friends for staying with me and encouraging me, hopefully I have made them proud.

ACKNOWLEDGEMENT

I would like to take this time to extend a great thank you to my advising professor, Dr. Choong-Un Kim, for guiding and training with constructive criticism. Without him I would not be half the engineer I am today without his teaching of various disciplines, work ethic, and dedication. I would also like to thank the plethora of doctoral, masters, and undergraduate colleagues I had the pleasure of collaborating with, Mohsen Tajedini, Yi-Ram Kim, Hariram Mohanram, Geng Ni, Allison Teresa Osmanson, Jorge Mendoza, Dharani Sholapur, and Ross Everett. I want to also thank Dr. Nancy Michael for starting me on the path of research and Materials Science and Engineering. I want to thank the staff of the Center for Cellular and Molecular Biology (CCMB) for training me in various equipment. Finally, I would like to thank the Semiconductor Research Corporation (SRC), Texas Instruments Inc., and Cisco Systems Inc. for their support and collaboration throughout my research tenure.

ABSTRACT

Assessment of Joule Heating Properties of Various Solder Alloys in BGA Assembly

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The continuing demands for smaller, yet higher performance devices have resulted in many revolutionary changes in device packaging in recent years, including the change in package form factors, structure, and the type of solder alloys used for the assembly. Because solder joints are exposed to various electrical and thermo-mechanical stresses, not only at use condition but also during their process into the assembly, they are prone to failure. Especially concerned in this respect is the current density that the solder joint is subjected to as it determines the level of Joule Heating (JH), thus the solder temperature, significantly affecting the joint reliability of solder. The JH in solder joints in the existing assembly may be at the manageable level with material redundancy, and more predictable with cumulated knowledge on the electrical and thermal properties of the solder alloys. The structural redundancy is increasingly limited, and even more troublesome is the fact that less familiar solder alloys (as well as joint structure) are employed to the assembly. Better understanding the thermal behavior of new solder alloys/structures in new packaging structures is therefore of utmost importance to enable advanced packaging.

The findings of this research present a greater understanding of different solder alloy's JH behavior and outside parameters affecting such through the resistivity to temperature calibration method (TCR) with the main objectives: 1) Identify the fundamental mechanism(s) driving the different JH behavior seen if any in the various solder alloys from a microstructural defect view; 2) Determine the impact of variance of PCB structure has on the overall JH level of a package. This thesis presents key evidence in our study regarding a better understanding of metallurgical and structural mechanisms effect on JH behavior. This research explores the benefits and shortcomings of TCR in that it gains information of JH at the interconnect level but determines the average of all interconnects tested. Although, traditional temperature measurements lack the ability or accuracy of determining the temperature change at the interconnect level that TCR offers. Previous work has suggested that resistivity and resistance as the main contributors to JH. Comparison of SAC305 and SnBi-based solder alloys' JH behavior revealed that microstructural defects such as macrovoids and cavities have been found to have a more significant impact than resistivity on the heat that individual solder joints produce. Although the true mechanism as to why this phenomenon is observed is still being investigated as on a macro-scale this behavior is not observed, our work has pointed to the effects of current crowding around such defects to be the cause of this unanticipated behavior. The presence of these macrovoids was also averse to traditional mechanisms of entrapped gases as the voids present in our research exist at both top and bottom of solder joints instead of only the top. Our research indicates that these macrovoids are caused by differential heating and cooling of adjacent solder joints resulting in internal stresses that displace large amounts of solder. Future work including further study into solder joints with known defects to determine the statistical correlation to this behavior, is also suggested in this thesis.

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CHAPTER 1: INTRODUCTION

1.1 Background and Significance

Reliability has become the most significant concern and challenge in the microelectronics industry as the demand for smaller, higher density devices increases [1]. There are several different structural package design choices such as component size and shape, material composition/ratios, interconnect methods printed circuit board (PCB) layout/design, surface finishes, etc. to help meet this growing demand for efficiency and size. With these constraints comes complex engineering challenges such as thermomigration, electromigration, and more pertaining to this study, joule heating. Thermomigration refers to the transport of a material driven by a temperature gradient, whereas electromigration is the transport of metal ions from a cathode to an anode through an electrically conductive medium [2, 3]. Joule heating (JH), also referred to as resistive or ohmic heating, on the other hand is the process of electrical current/energy being converted into heat as it flows through a given resistance [4]. Joule heating becomes more of a reliability issue the more complex ICs become with different materials being introduced due to coefficient of thermal expansion (CTE) mismatch. These mechanisms and phenomenon have led the microelectronics industry to push for package reliability to increase as it is directly tied to their resistance [5]. This research has been done in partnership with industry liaisons to gain a better understanding of the effects of how different solder materials, PCB layouts, and varying current densities contribute to joule heating.

This research aims to identify the temperature increase in solder joints induced by JH in a ball grid array package (BGA) using different PCB structures and four common solder alloys. To achieve this, the resistivity to temperature calibration method (TCR) was employed, which accurately captures the temperature behavior in solder joints. Traditional temperature

measurement methods may not provide a comprehensive understanding of the JH-induced temperature behavior in solder joints.

The results of this study will provide valuable insights into the behavior of solder joints in BGA packages under various current density conditions, helping to optimize the design and performance of electronic components. The TCR method employed in this study can be applied to future research to accurately measure the temperature behavior in other electronic components, enabling the development of more efficient and reliable electronic devices.

CHAPTER 2: LITERATURE REVIEW

2.1 Solder Alloys and Mechanical Properties

Historically, the electronics industry utilized Sn-Pb solders, specifically the eutectic 63Sn-37Pb, due to their low melting temperature, excellent wettability, high ductility, reliability, and low cost [6]. However, the health hazards associated with lead prompted the passing of the Safe Drinking Water Act in 1986, which prohibited the use of lead, including in electronics [6]. This led to the development of Pb-free solders, which are now widely used in the industry. Currently, the electronics industry primarily uses solders with varying concentrations of Sn, Ag, and Cu in "SAC" composition solder joints, as well as some other Sn-based alloys that include Bi and In in rare cases. However, complete replacement of Pb-based solders has not yet been achieved. The development of Pb-free solders has been a significant area of research in the electronics industry. The focus has been on finding a suitable replacement for Pb that meets the performance and reliability requirements of the industry while being environmentally safe. The current research efforts in this area include improving the mechanical and thermal properties of Pb-free solder alloys, as well as developing new techniques to process and fabricate Pb-free solder interconnects with high precision and repeatability. These different alloy compositions are utilized for more specific use cases in the industry. For instance, SAC alloys are more suitable for high-temperature applications due to their higher melting point compared to other Pb-free alloys and offer a balance between thermal fatigue, cost, and ease of manufacturing, making them ideal for various electronic applications.

In this research, the focus is on studying two specific SAC alloys: SAC305 and SACQ. SAC305, which is also known as Sn3.0Ag0.5Cu, has become the standard for Pb-free solders in the electronics industry due to its desirable melting temperature of 217˚C, which allows for

compatibility with existing infrastructure and manufacturing processes. Additionally, SAC305 has been shown to perform similar to higher Ag content SAC eutectic solders at a lower cost, making it an attractive choice for many applications [7]. As a result of its quick adoption, a large reliability database has been developed, allowing for better understanding and prediction of its performance in various applications.

However, the increasing cost of silver, which makes up a significant portion of SAC305, has driven the cost of this solder to around $40 per kg, three times the cost of ten years prior [7]. To mitigate this cost increase, alternatives have been extensively explored. One approach has been to modify the SAC alloy composition, leading to the development of SACQ, which contains less silver than SAC305. The selection of different SAC alloys is based on the ternary Sn-Ag-Cu phase diagram, as shown in Fig. 1. By studying the properties and behavior of different SAC alloys, researchers aim to identify alternatives to SAC305 that offer similar or improved performance at a lower cost.

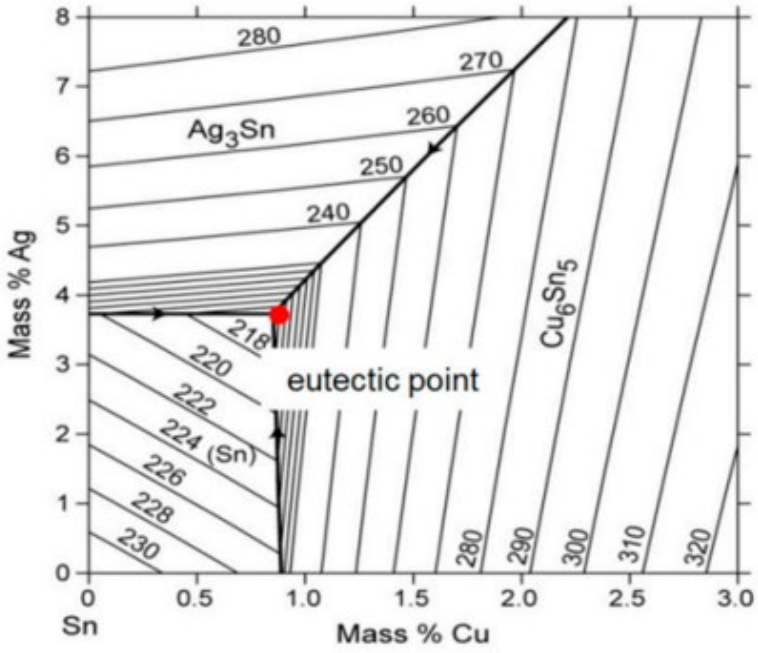


Figure 1. SAC305 Ternary Phase Diagram [8]

The SACQ alloy is composed of 92.45% Sn, 4.0% Ag, 0.5% Cu, 3.4% Bi, and 0.5% Ni which is quite similar to the composition of SAC305, except for the addition of Bi and Ni. The composition of which is presented in Table I. The addition of Bi to the SACQ solder alloy has been shown to improve the wettability and solder spread, while also reducing the melting/solidus temperature, which makes it a potentially attractive alternative to SAC305 [7]. The reduction in solidus temperature is due to the formation of a eutectic structure between Sn and Bi, which results in the formation of Bi-rich particles that increase the strength of the solder through precipitation hardening. However, some studies have reported that the addition of Bi to the solder can lead to embrittlement within the solder joints, resulting in solidification cracks due to the increased range of melting points. These characteristics make SACQ more desirable in applications where the operating temperature does not vary to an excessive extent. Therefore, it requires careful consideration of the application's temperature requirements and the solder's properties to ensure its reliability and suitability.

%Contents	
Element	SACQ
Sn	92.45
Ag	4.0
Cu	0.5
Bi	3.4
Ni	0.5

Table I. SACQ Compositional Breakdown

The other solder alloys used in this study are SnBiAg and SnBiIn, with their ternary phase diagrams shown in Fig. 2 and 3 respectively. The use of these alloys is relatively fresh, creating new reliability complications that have yet to be extensively researched, namely the effects of JH.

Most research on Pb-free solder has been on alternatives with melting temperatures in the 180-230˚C range. SnBi based solders can have melting points well below 180˚C, as low as 138˚C [8]. These lower melting temperatures become important as vertical stacking of chips is implemented more commonly, requiring a hierarchy of solder joints. A hierarchy, meaning that multiple reflow cycles will be required to properly connect chips. This requires that the first solder has the highest melting temperature so that as the subsequent levels are reflowed it does not melt the first. Another main reason for the demand of sub-180˚C melting temperature solders is that as packages become more integrated and chips size increases, warpage during the reflow process becomes a more serious issue [10]. The addition of a ternary element to eutectic SnBi solders has the advantage of improving the solderability/mechanical properties laid out in Table II as they suffer from being much more brittle in comparison to other solder alloys [8].

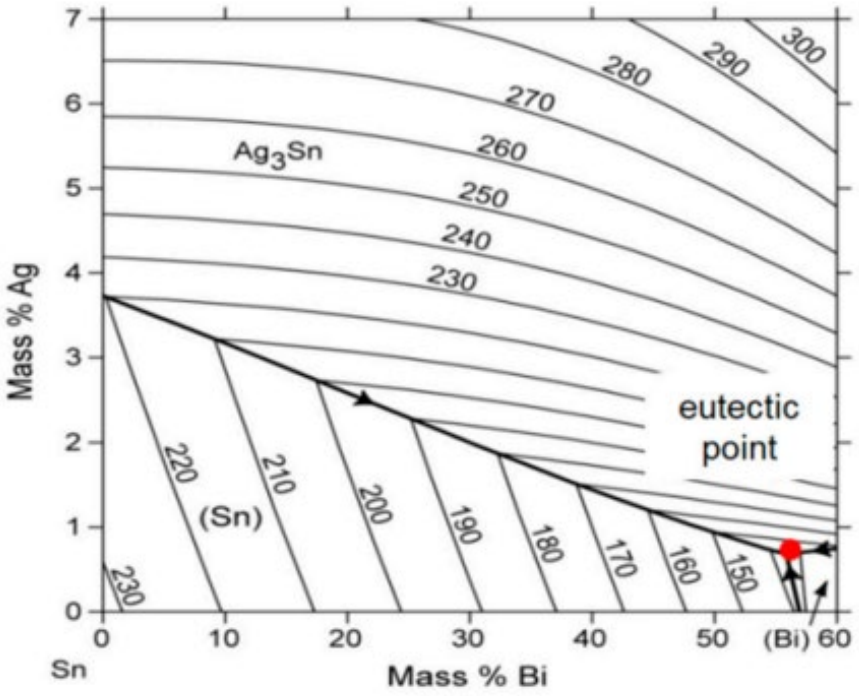


Figure 2. SnBiAg Ternary Phase Diagram [9]

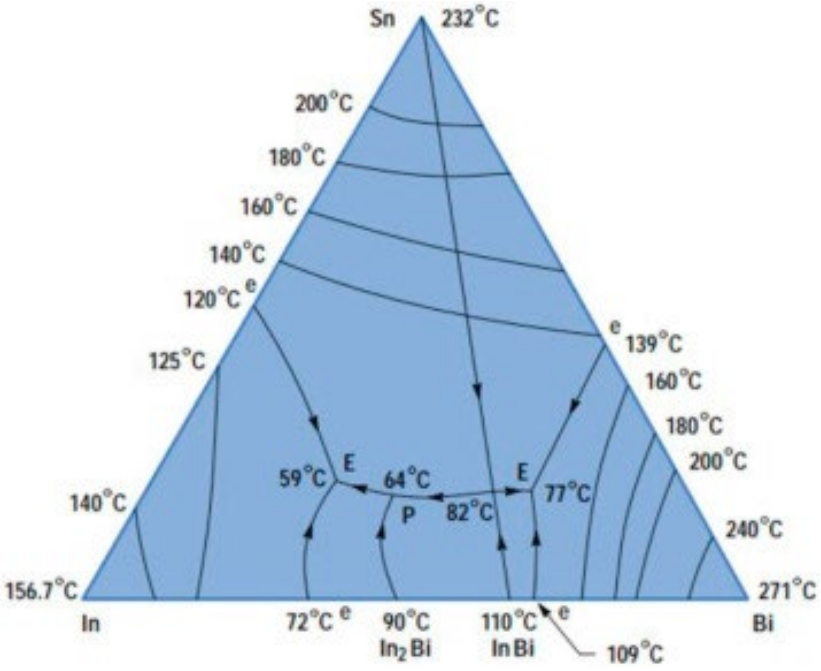


Figure 3. SnBiIn Ternary Phase Diagram [8]

Element	Alloy Composition	Melting Point (˚C)	Wettability	IMC Growth Gate	Tensile Strength (%)	Elongation (%)	Shear Strength (MPa)
In	Sn-58Bi-2In	129.7		Slightly	+6.5		+8.0
	Sn-58Bi-2.5In				Slightly	+104.5	
Ag	Sn-58Bi-1Ag	Little effect	Better	Decrease			
	Sn-58Bi-0.5Ag	Little effect	Better	Increase	+13.2	+80	+7 after aging
	Sn-58Bi-2Ag	139.0			+12.1		+6.7
	Sn-58Bi-2In-2Ag	133.6			+8.1		+12.9

Table II. Eutectic Sn-Bi Solder Property Changes with Ternary Element Addition [8]

2.2 PCB Surface Finishes in Relation to Solder Joint Reliability

One of the final processes in PCB fabrication is applying a surface finish to protect the exposed Cu regions from oxidation. The characteristics of a good surface finish are good solderability and bondability while also being smooth enough to allow for proper contact in connectors [11]. Due to the heat used in soldering, the elements and materials in the surface finish will diffuse into the solder, altering its properties, both electrically and mechanically. The alteration of such properties from a long-term reliability standpoint is still under extensive investigation. There are several surface finishes used in the industry, two common ones being Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG) and Organic Solderability Preservative (OSP).

ENEPIG has been regarded in recent years as the "universal" PCB surface finish after reliability comparisons to other common surface finishes revealed that ENEPIG provided higher solder joint reliability. Composed of three layers, electroless nickel (EN), electroless palladium (EP), and immersion gold (IG), the thicknesses of all three influence the interfacial reaction and therefore the reliability and possibly thermal properties of a solder joint. OSP surface finishes are a form of nonmetallic finish that unlike the metallic finishes, like ENEPIG, can be applied at much lower temperatures, reducing cost and environmental risks [11]. The main downfalls on OSP surface finishes are that it is not able to withstand multiple heat cycles or be used in applications where wire bonding is required. In comparing the two surface finishes in both electrical, thermal, and mechanical reliability testing of solder joint reliability the results are somewhat mixed as one behaves more favorable in some tests and less desirable in others and vice versa [11].

2.3 Resistivity and Joule Heating

Joule heating, or Ohmic heating, is a fairly simple concept. As current is passed through a conductor the total heat generated is proportional to the square of the passing current, conductor's resistance, and time, known as Joule's Law, shown in Eq. 1 [12]. The heat is a result of the electrical energy being converted into thermal energy.

$$Q = i^2Rt \qquad Eq.1$$

The classical mechanism of JH under DC conditions are resistivity/conductivity and current density. When the voltage is applied to a conductor, in this case solder joint, an electric field (E) is created, imposing a force on the charges in said conductor. Current density (J) is a function of DC current applied (i), and the area of the path the current is taking (A), defined in Eq. 2. Resistivity, denoted as ρ, is an intrinsic material property that describes how much a material can resist the flow of charges. Resistivity can be described in terms of electric field (E) and J, shown in Eq. 3. From Eq. 3 it can be seen that for a fixed current density a conductor with a higher resistivity compared to another will create a higher E, creating more heat energy to be dissipated. In the case of this research, samples exhibiting higher resistivity or resistance would then be expected to create a higher level of JH in comparison to other samples. Table III shows the ρ of the solder alloys used in this study and shows that SnBi alloys tend to high a higher ρ than SAC alloys.

$$J = \frac{i}{A} \qquad Eq.2$$

$$\rho = \frac{E}{J} \qquad Eq.3$$

Solder Alloy	Resistivity [μΩ·cm]
SAC305	13.2
SACQ	~13.2
SnBiIn	~14.5
SnBiAg	~14.5

Table III. Electrical Resistivities of the Four Solder Alloys Used in this Study

2.4 Coefficient of Thermal Expansion (CTE) Mismatch

One aspect of modern packaging that has become a main industry concern is the stresses induced by CTE mismatch between the different materials bonded to each other. Every material has its own CTE, and each package has several different materials, creating a wide range of CTE's in one package. As one material expands at a faster rate than another material it is bonded to it will result in a tensile stress in one and a compressive stress in another [13]. A smaller CTE material will restrict the expansion of the material with a higher CTE.

Table IV lists the CTE values of common packaging materials, and the main ones used in the samples tested in this research. The difference in CTE values of Si, Cu, and PCB in comparison to SAC solder alloys is expected to create a significant amount of shear stress during any heating processes (i.e., reflow, testing, etc.). In the case of SnBi solder alloys the CTE mismatch present between Si, Cu, and PCB is to a much lesser extent than SAC305. Stress generation of any kind can lead to mechanical failures within a semiconductor package as it can cause delamination of the solder joint to the substrate, warpage in the Si die or PCB, cratering in the Si die, etc.

Material	Coefficient of Thermal Expansion [ppm/°C]
Silicon (Si)	~3.0
Copper (Cu)	~17.0
Printed Circuit Board (PCB)	~17.0
SnAgCu (SAC) Solder Alloy	~24.0
SnBi Solder Alloy	~15.0

Table IV. Coefficient of Thermal Expansion Values of Common Package Materials

2.5 Joule Heating Characterization Methods

In the industry to measure the temperature of semiconductors under testing conditions methods of thermocouples, thermistors, RTD, and infrared (IR) thermal microscopy are commonly used. These methods have their own advantages and disadvantages. Thermocouples consist of two wires of dissimilar metals joined together where heat creates a thermoelectric potential that corresponds to a temperature change [14]. These offer the advantages of being simple and inexpensive while also withstanding high temperature ranges. Thermistors are typically a resistive wire or semiconductor material that has large resistance changes in response to small changes in temperature [15]. These come with the advantage of inexpensiveness, high accuracy, operate within a wide temperature range, but are quite more fragile than the alternatives and lack stability in long-term use. RTDs, or resistance temperature detectors, are similar to thermistors in that they are devices that have a resistance that changes in response to temperature but are highly accurate and stable over long periods of time and a wide temperature range [15]. These devices are made of pure metal where the resistance changes linearly proportional to temperature, unlike thermocouples and thermistors that are non-linear devices. IR thermal microscopy is a non-

contact/optical method of temperature measurement that detects the electromagnetic radiation emitted from a heat source [16]. There are several benefits to this method such as being non-contact making it easier to implement, measures across a large area, and can create 2D temperature maps of devices over time. Although IR thermal microscopy does have significant issues with semiconductor materials that are transparent or reflective as the emissivity does not allow for the sensor to accurately record temperature and is one of the most expensive. All these methods are limited in the fact that they only measure the surface temperature of a device or package or only the component(s) they are directly connected to, whether that be physically or electrically. They also do not offer the determination as to which component(s) are contributing to specific JH behaviors. This is where the TCR method fills that void.

The TCR method is the determination of the thermal coefficient of resistance of a conductor by measuring resistance values over a temperature range. The TCR is then taken as the slope over this temperature range [17]. The value of TCR is constant at every temperature for a given conductor, giving a linear relationship between resistance and temperature. This method is much more accurate in comparison to the others explained in this section as it directly measures the internal temperature of the conductor based off intrinsic properties of the materials instead of just surface level measurements. The implementation of this method is further explained in section 3.3.

2.6 Foster & Cauer Model Thermal Equivalent Circuit

The thermal behavior of the various components found within semiconductor packages can be described with several different thermal equivalent circuit models such as the Cauer Model and Foster Model. Both the Cauer and Foster Model are based on the theory of thermal impedance (Z_{th}) represented by a network of thermal resistances (R_{th}) and thermal capacitances (C_{th}) [18]. The

two models are equivalent representations with the main difference in how the R_{th} and C_{th} values of the circuit are assigned to components of the physical device.

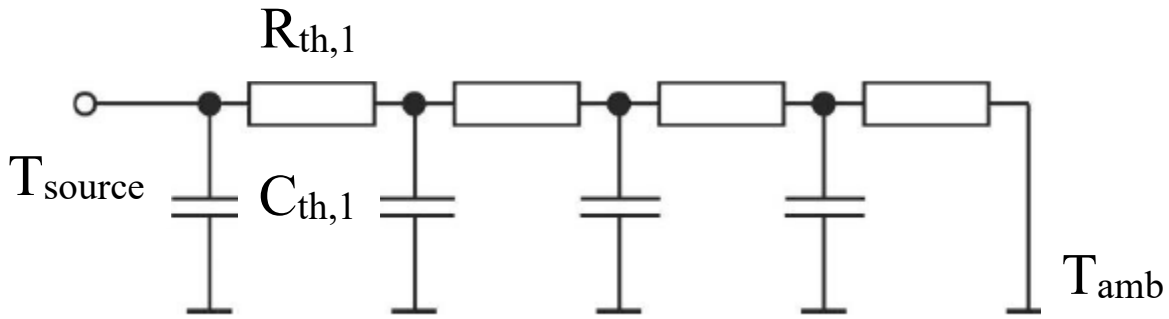


Figure 4. Cauer Model Thermal Equivalent Circuit [19]

The Cauer Model, shown in Fig. 4, reflects the physical setup of the device based on the R_{th} and C_{th} of the material properties of the individual layers. In this model and the Foster Model T_{source} and T_{amb} represent the temperature of the heat source and ambient temperature respectively. In the Cauer Model each C_{th} is connected to the thermal ground, or T_{amb}. This means that each node has a physical meaning corresponding to the chip, solder, substrate, PCB, etc., and the internal temperatures of each layer can be extracted [18]. This, however, is only available when the material properties of each layer are known and does not allow for ease of determining Z_{th} coefficient values.

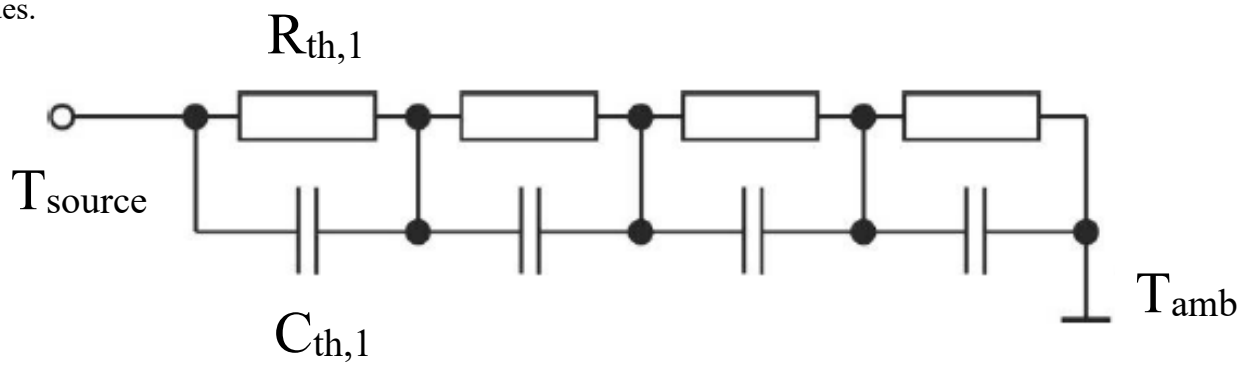


Figure 5. Foster Model Thermal Equivalent Circuit [19]

In the Foster Model, shown in Fig. 5, the R_{th} and C_{th} values do not correspond to specific layers or locations, so the values cannot be calculated from the material properties. Each pair of R_{th} and C_{th} in this model corresponds to a thermal element but do not have a physical meaning [18]. Meaning that only the overall thermal behavior from the measured points is certain. As such, the coefficients must be extracted by fitting the heating and cooling curves of the device to the expression for Z_{th}, shown in Eq. 4. Where τ_i is the thermal time constant comprised of both the R_{th} and C_{th} for a given component, shown in Eq. 5. Having the values τ_i allows for the thermal behavior of the component to be determined in respect to whether the thermal capacitance or resistance is the main contributor to the JH behavior [18]. For this, the Foster Model will be used in this study.

$$Z_{th(t)} = \sum_{i=1}^{n} R_{th,i}\left[1 - exp\left(-\frac{t}{\tau_i}\right)\right] \qquad Eq.4$$

$$\tau_i = R_{th,i}C_{th,i} \qquad Eq.5$$

CHAPTER 3. EXPERIMENTAL METHOD AND APPROACH

3.1 Sample Structure and Configuration

All sample packages used for this research were provided by Cisco Systems, Inc. The samples are assembled in a BGA package with four 5x10 quadrants for a total of 200 solder joints per chip with no underfill and 28-layer PCB structure. Each solder joint has a diameter of 300μm bonded between a via-in-pad plated over (VIPPO) (on the PCB side) and a Cu trace (on the Si chip substrate side). Fig. 6 shows a diagram of the cross-section view of the BGA assembly, and Fig. 7 shows a layout for how the solder joints are spaced out on the assembly. Fig. 8 shows an image of the physical boards with voltage and current tabs placed adjacent to the actual package connected through surface layer Cu traces.

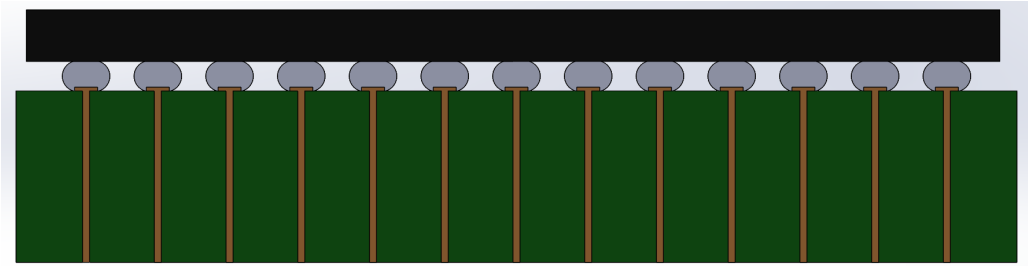


Figure 6. Cross-Sectional Layout Diagram of BGA Assembly

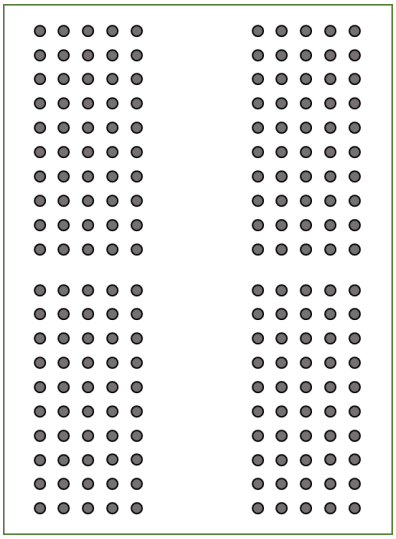


Figure 7. Solder Joint Layout Diagram

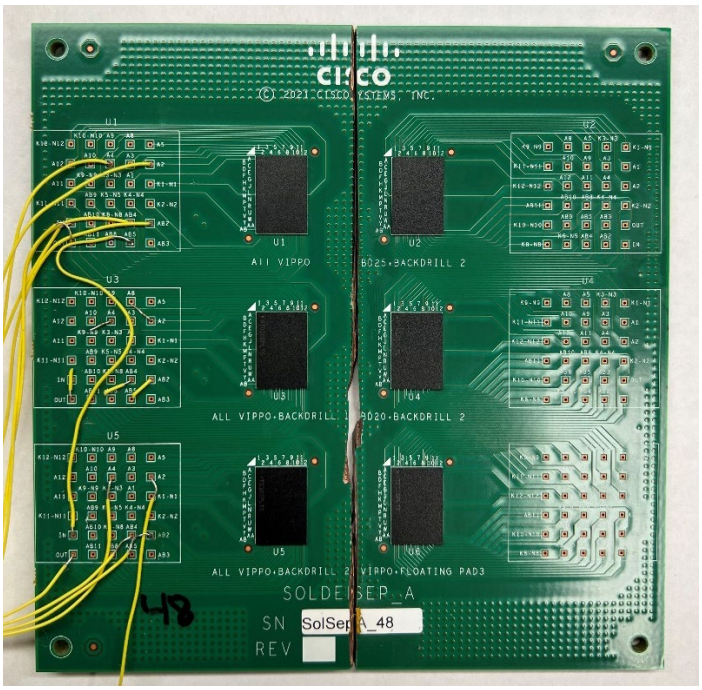
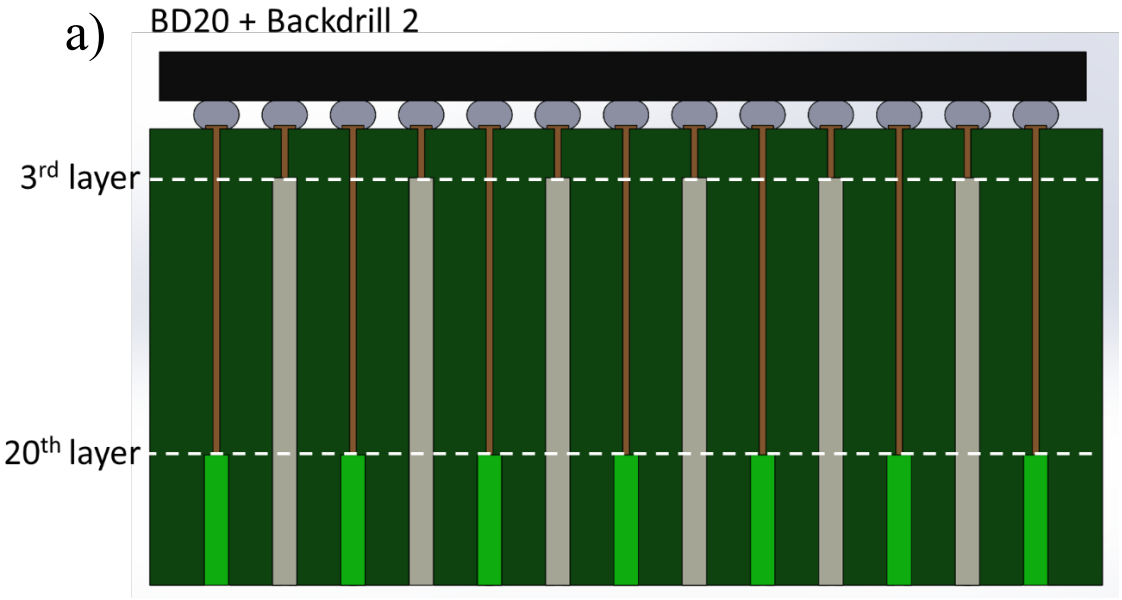


Figure. 8. Test Sample Board Provided by Cisco Systems, Inc.

This research involves the comparison of different samples based on three parameters: solder alloy, PCB structure, and surface finish. The variations in these parameters affect the amount of JH generated in the samples. The four solder alloys used in this study are SAC305, SACQ, SnBiIn, and SnBiAg. Each sample comprises one or a combination of two solder alloys in each ball, and the purpose is to analyze the effect of having a hierarchical structure of a lower melting temperature solder on the PCB side and a higher melting temperature on the chip side. The study also examines the influence of two types of surface finishes, ENEPIG and OSP on the performance of the samples. The focus of the study is to determine the significance of each of these parameters in relation to JH, which is a crucial factor affecting the reliability of the solder joints in electronic devices.

For the PCB structure there were six different combinations of VIPPO and backdrill (BD). Backdrill meaning that the VIPPO and some surrounding PCB is physically drilled out from the bottom to reduce the amount of heat that can be dissipated. The first PCB structure contains

VIPPO's for each solder joint. In theory this structure will have the best heat dissipation and lowest solder joint temperature as it has the most thermal mass to draw away heat from each joint. Each following structure will have varying levels of heat dissipation through different combinations of VIPPO and BD. Not only on a chip-to-chip level but on a joint-to-joint level where adjacent joints will have quite different heating/cooling profiles. The second and third structures have BD up to the fifth and third PCB layer for around a third of the solder joints, respectively. The fourth and fifth structures both have BD up to the third layer for two-thirds of the solder joints and BD to the 25th and 23rd layer for the remaining third, respectively. The sixth and final structure only has VIPPO's for a quarter of the solder joints with a floating pad at the third layer for the remaining solder joints. Each of these PCB structures allows for a comparison of how significant the board side is in dissipating heat and the effects this will have on the JH behavior. The cross-section and distribution of BD and VIPPO solder joints of the two main PCB structure types used in this research are shown below in Fig. 9 and 10 respectively where it can be seen how even solder joints directly next to one another will have completely different thermal profiles. The effect of these different structures will be explored to some extent in future sections.



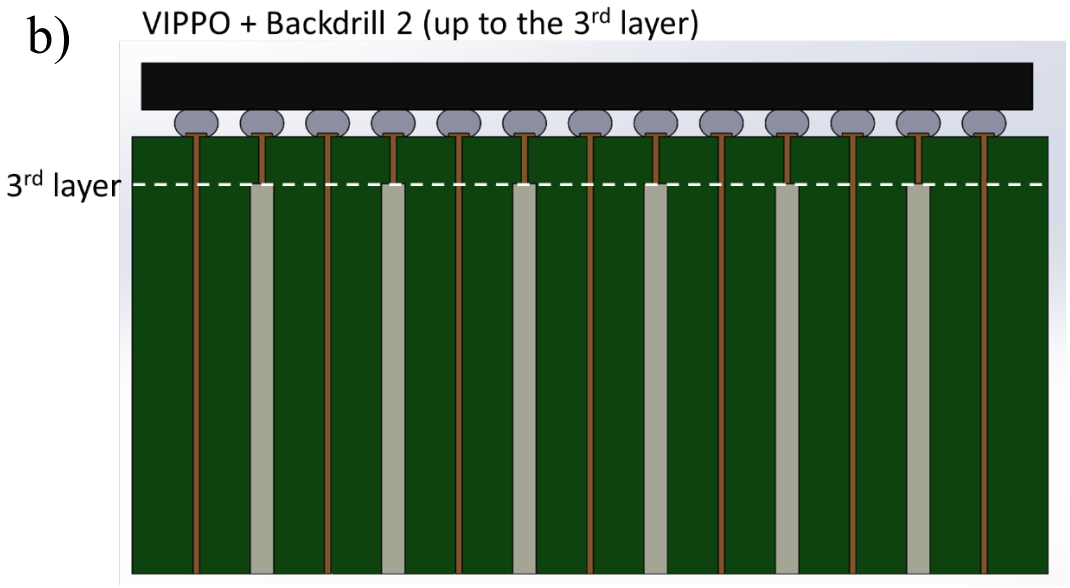


Figure 9. a) Cross-section diagram for BD20 + Backdrill 2 b) for VIPPO + Backdrill 2 PCB structures

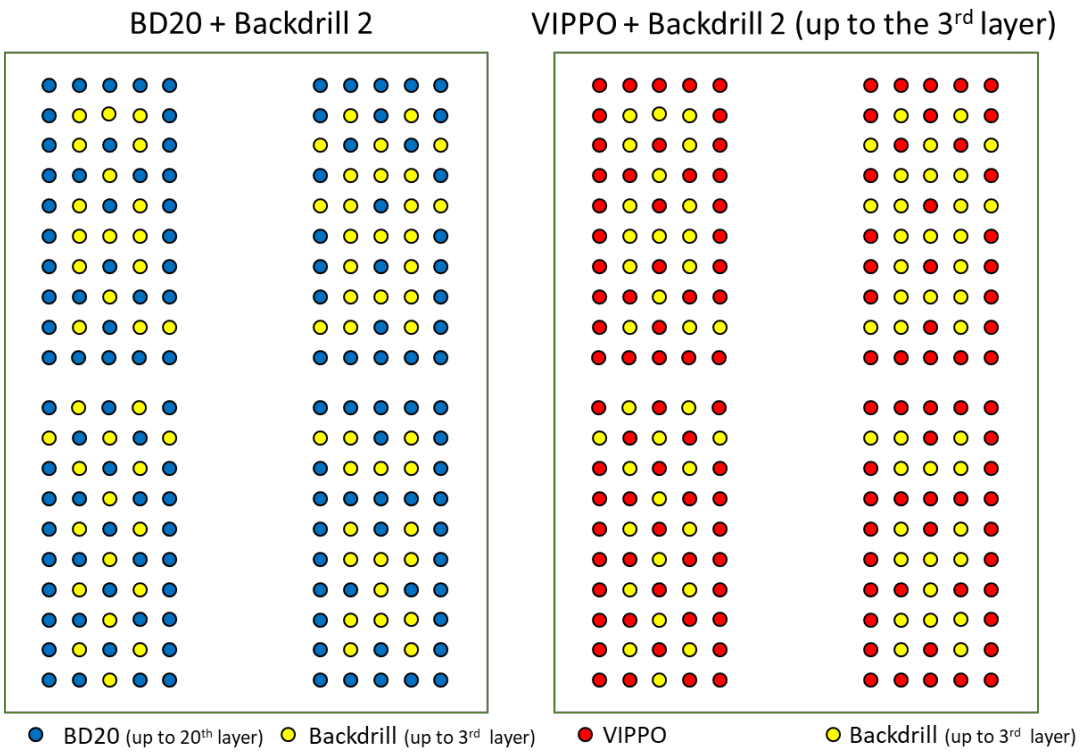


Figure 10. Distribution of each solder joint's PCB connection for the BD20+Backdrill 2 and VIPPO + Backdrill 2 PCB structures

3.2 Joule Heating Experimental Test Setup

To conduct the JH experiments several pieces of test equipment were required/constructed. Those being: a DC current supply (HP6621A) to apply high current to induce JH in the samples, a high-resolution voltage meter (HP3497A ±10μV), an oven to perform TCR calibration, a wind tunnel to capture the heating and cooling behavior of the samples, and a control computer to execute the LabView program measuring the voltage signals from the samples. Fig. 11 below shows each instrument in the testing environment.

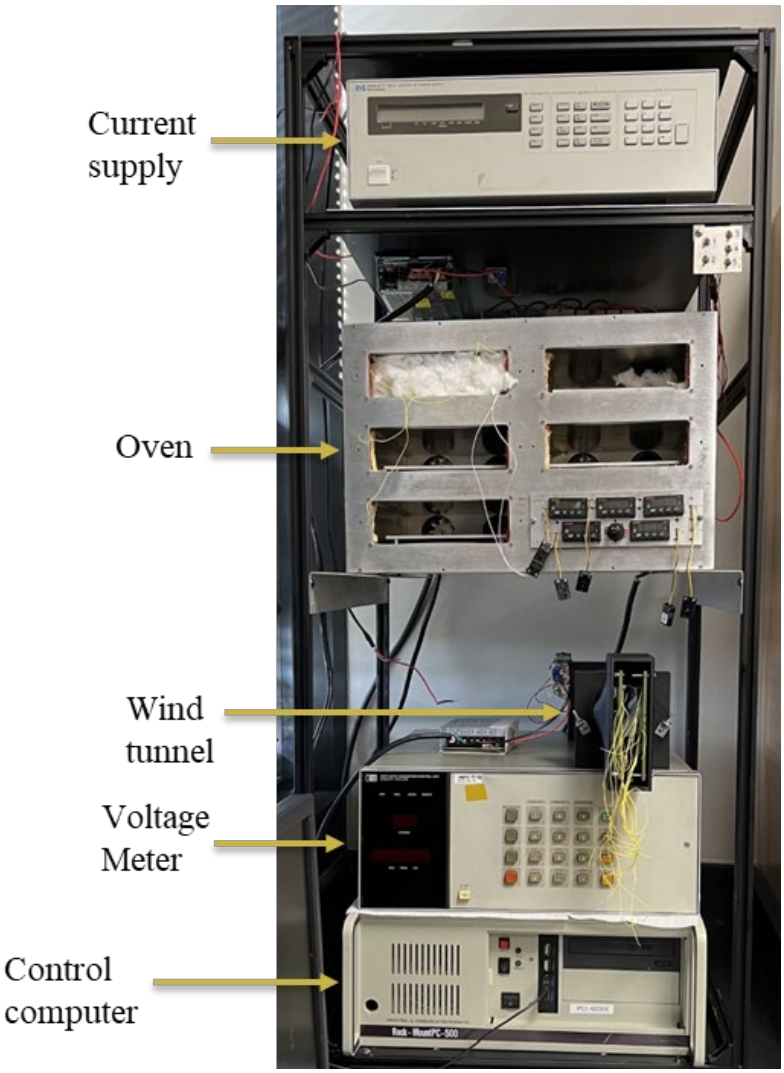


Figure 11. All test equipment used in the testing environment.

For the cooling behavior of the samples, a wind tunnel was constructed through the use of 3D printing to create a structure that allowed uniform heating and cooling. A fixed cooling rate was used with a uniform 8 m/s wind speed flowing over the top and bottom sides of the sample to provide even cooling. In the wind tunnel, shown in Fig. 12, samples were fixed on standoffs to ensure proper repeatability and that the space the sample is allowed to heat and cool in is identical for each test.

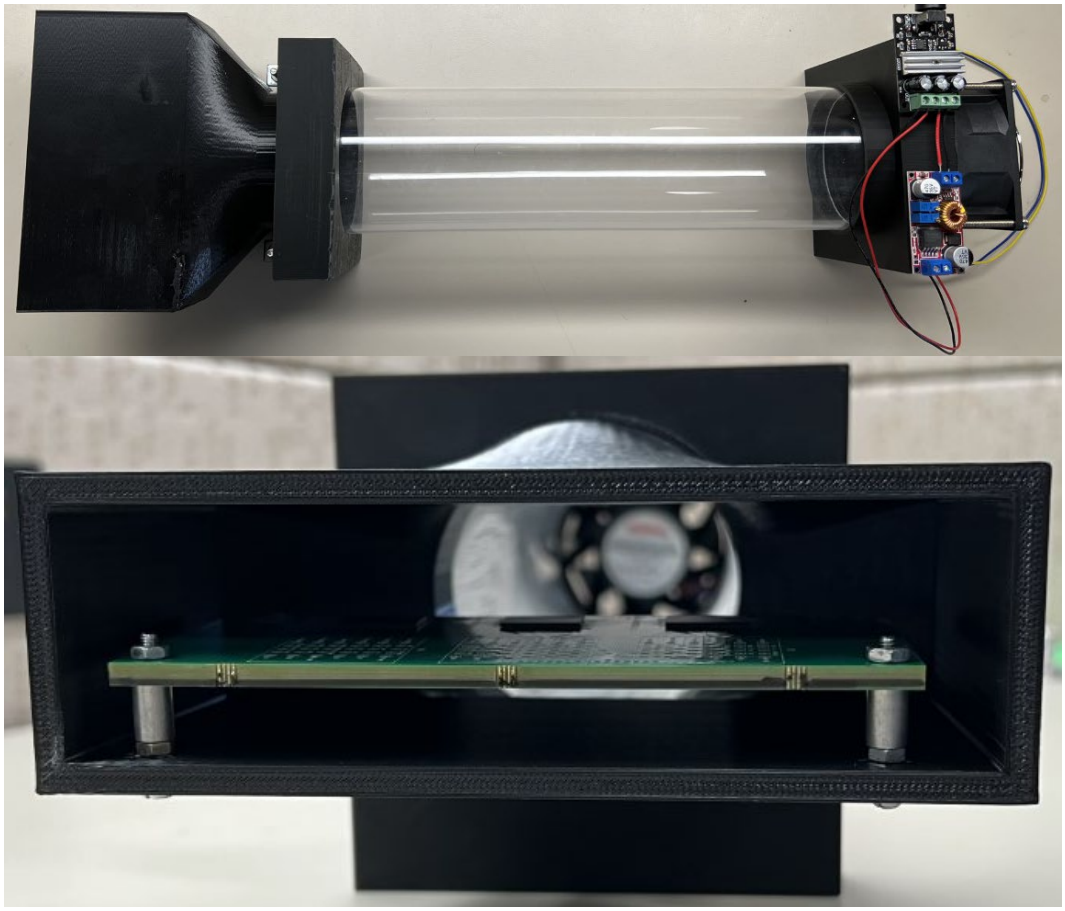


Figure 12. (Top) Top-down image of wind tunnel, (Bottom) Image of sample in fixed position on standoffs.

3.3 TCR Calibration Method

To determine the behavior of each chip the TCR calibration method was used. This method allows for the extraction of the relationship between resistivity to temperature. For each sample a constant current of 30mA was applied to create a measurable voltage but not high enough to induce heating. Once the current was applied voltage/resistance was measured at four different temperatures (60, 70, 80, 90˚C) set in the oven. The measured resistance at each temperature interval was then put to a linear fit as resistance and temperature have a linear relationship. A comparison of the four solder alloys calibration to one another is shown in Fig. 13. With the relationship known we were then able to convert the measured resistance into temperature accurately in the JH tests with the use of Eq. 6. Eq. 6 shows the linear relationship between resistance and temperature and how to extract temperature per given resistance. Where R_T is the conductor resistance at a certain temperature, α is the temperature coefficient of resistance for the conductor, R_0 is the projected resistance at 0˚C, and T_R is the temperature per given resistance. As explained in section 2.5 the value of α is constant over temperature ranges where the material properties are constant, allowing for a linear conversion to temperature for a given measured resistance. Calibration was conducted for each sample prior to any testing to ensure that the base JH behavior was captured in the event that testing at high current would damage the sample or cause any microstructural changes.

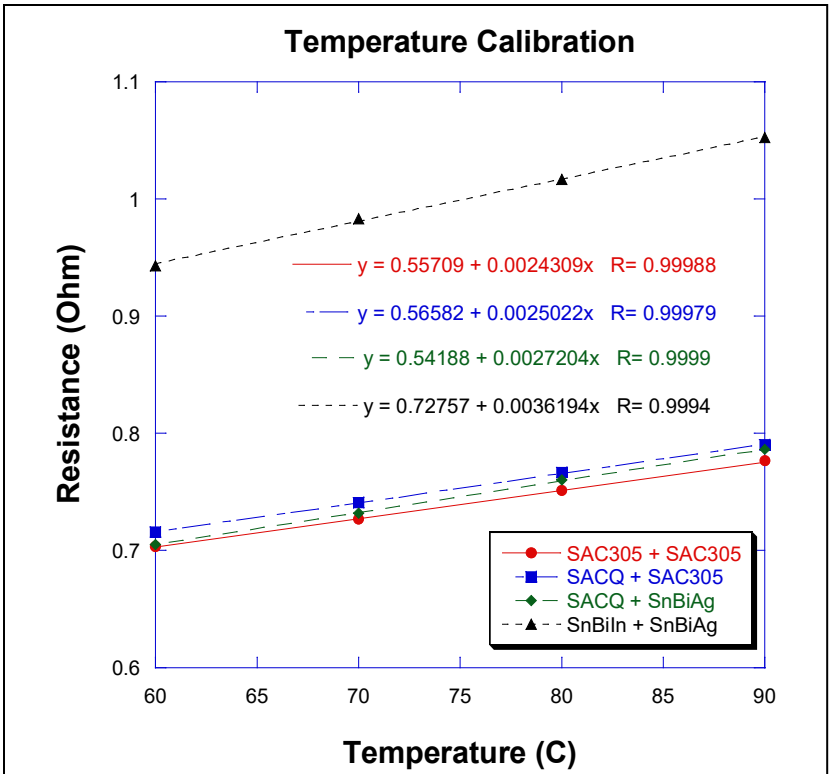


Figure 13. Temperature calibration plot of all four solder

$$R_T = \alpha T_R + R_0 \qquad Eq.6$$

3.4 Experimental Test Conduction and Method

The test methodology employed for this study was designed with the aim of minimizing the number of variables that may influence the behavior of JH in solder alloys. To this end, three current densities were utilized, namely 1389, 1944, and 2500 A/cm^2, with the intention of generating a comprehensive database that accounts for the behavior of each solder alloy and printed circuit board (PCB) structure at each current density. Moreover, three separate tests were conducted on three different configurations: full chip, half chip, and half row, to determine how the number of heat sources or solder joints affects the JH behavior, if at all. The full chip, half chip, and half row configurations were comprised of 180, 80, and 10 solder joints, respectively. For the

half chip and row tests current was only supplied to those specific areas to isolate their JH behavior. This resulted in a total of nine tests per chip, where three current densities were examined for each sample configuration.

To conduct each test a constant current was applied until a saturation temperature (T_{sat}) was reached. Each test began with the sample fully cooled and equalized to room temperature (≈25˚C). The heating process to reach $T_{sat,H}$ typically took around 30 to 50 minutes depending on current density and number of solder joints tested. Once $T_{sat,H}$ was reached the cooling fan was turned on until $T_{sat,C}$ was reached. The cooling process typically took around 10 minutes for each sample to maximally cool with the given cooling rate. Through the entire test the voltage/resistance is being measured, and once the test is completed the values are converted into temperature. An example of the results of this measurement is shown in Fig. 14. Once the values were converted the heating and cooling region were separated to extract data regarding JH behavior, further explained in section 3.5.

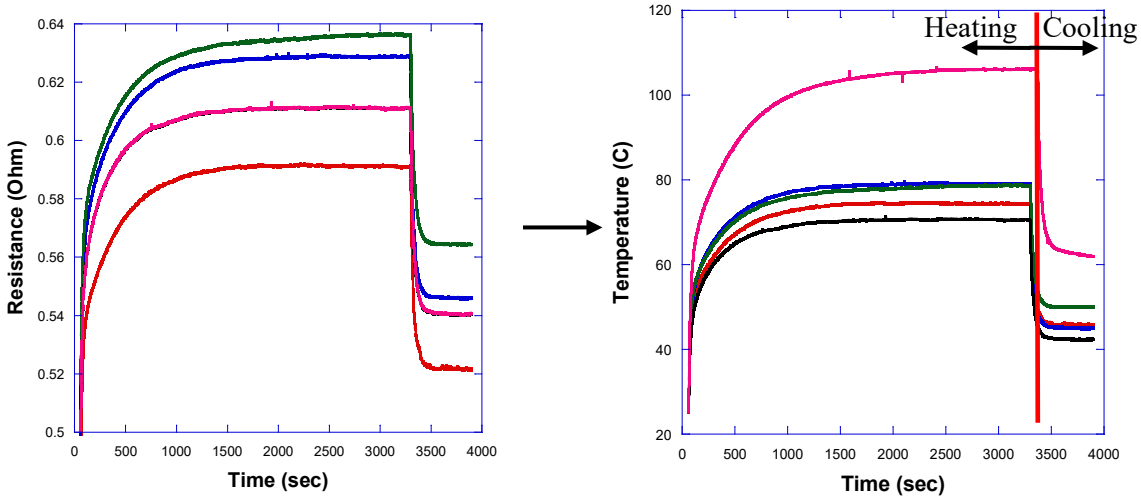


Figure 14. (Left) Resistance measurement over time with fixed current density. (Right) Conversion to temperature showing heating and cooling region of curve.

3.5 Joule Heating Behavior Data Extraction

For each test data was separated into a heating and cooling region to produce two separate curves. To extract the JH behavior from each region an exponential curve fit was applied to each region, shown in Eq. 7 and 8 for the heating and cooling regions respectively. Following the Foster Model to determine the JH behavior coefficients. Where T is the relative temperature of the sample at a given time, ΔT_H or ΔT_C is the change in beginning temperature to the saturation temperature, t is time, τ_H or τ_C is the thermal constant for heating or cooling, and $T_{sat,H}$ or $T_{sat,C}$ is the saturation temperature. From curve fitting these exponential equations the values of ΔT, τ, and T_{sat} are extracted for each current density used for each sample configuration. Comparing values of ΔT, T_{sat}, and τ from sample to sample tells the story of the overall JH behavior and a more in depth understanding as to how the intrinsic properties of the solder alloys, chip, and PCB structure affect JH. An example of the curve fit for the heating region is shown below in Fig. 15.

$$T = \Delta T_H \exp\left(-\frac{t}{\tau_H}\right) + T_{sat,H} \qquad \text{Eq. 7}$$

$$T = \Delta T_C \exp\left(-\frac{t}{\tau_C}\right) + T_{sat,C} \qquad \text{Eq. 8}$$

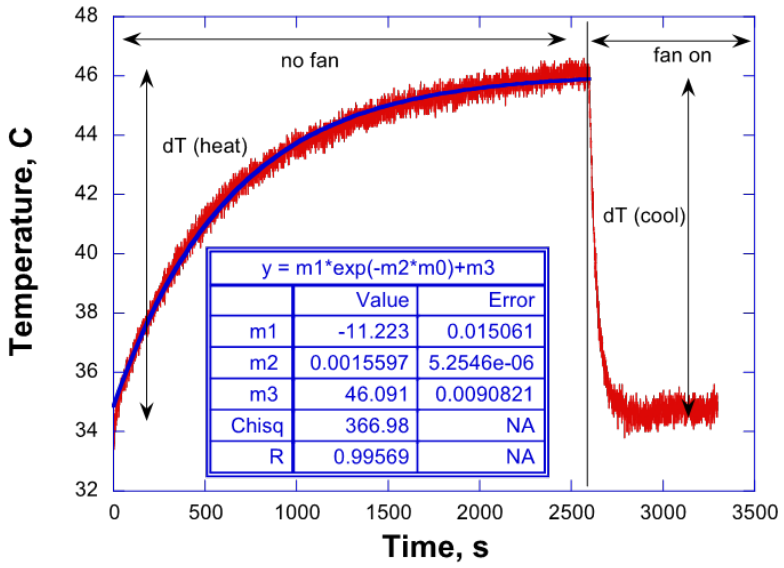


Figure 15. Example of curve fit JH behavior data extraction.

3.6 Sample Preparation and Microstructural Analysis

For microstructural analysis samples were physically cut from the main board to be cross-sectioned and analyzed by a scanning electron microscope (SEM). The first step in the process is to disconnect the chip from the main board by cutting it with a Dremel rotary tool. Once the sample is separated it is grinded until the cross-section of interest is reached, in this case the center of the solder ball. Various grit wet sandpaper was used for this process, ranging from 220-grit for bulk material removal to 3000-grit for scratch removal. The final step to prepare the samples for SEM imaging was polishing to an appropriate smoothness to remove any markings made from sanding for proper microstructural analysis without any confusion of the origin of any defects.

CHAPTER 4. CHARACTERIZATION OF JOULE HEATING PROPERTIES

4.1 Joule Heating Behavior Comparison between Solder Alloys

To compare the two extremes of the expected JH behavior the SAC305+SAC305 (SAC305) and SnBiAg+SnBiIn (SnBi) samples were used for being the lowest and highest resistive samples of the four respectively, shown in Fig. 10. From the TCR measurements of all samples these consistently showed the lowest and highest resistance, leading to the assumption that the SAC305 and SnBi would have the corresponding lowest and highest JH of all the samples. This also correlates with the resistivity values presented in Table III.

The aforementioned assumption is shown to be true in the sample configurations of full chip and half chip, but results of the half row measurements pose quite interesting results. Comparison of full chip and half chip measurements between the SAC305 and SnBi samples show that SnBi has the highest amount of JH in both cases. Fig. 16(a) shows this illustrates this behavior by juxtaposing both data sets of ΔT_H for both samples as a function of current density. These results show that per configuration SnBi has about a 15˚C increase in comparison to SAC305. This is expected with the SnBi samples near 30% increase in resistance by comparison.

The results of interest come from the half row measurements. In these tests the behavior is contrary to previous belief that resistance is the main contributor to JH behavior. In this instance SAC305 shows much higher relative JH than SnBi, shown in Fig. 16(b) comparing ΔT_H as a function of current density. These results show an over two times larger ΔT_H in the SAC305 samples. This would seem to contradict the commonly known phenomenon of higher resistive conductors creating higher levels of heat. That is until closer inspection of the microstructure of these samples is completed.

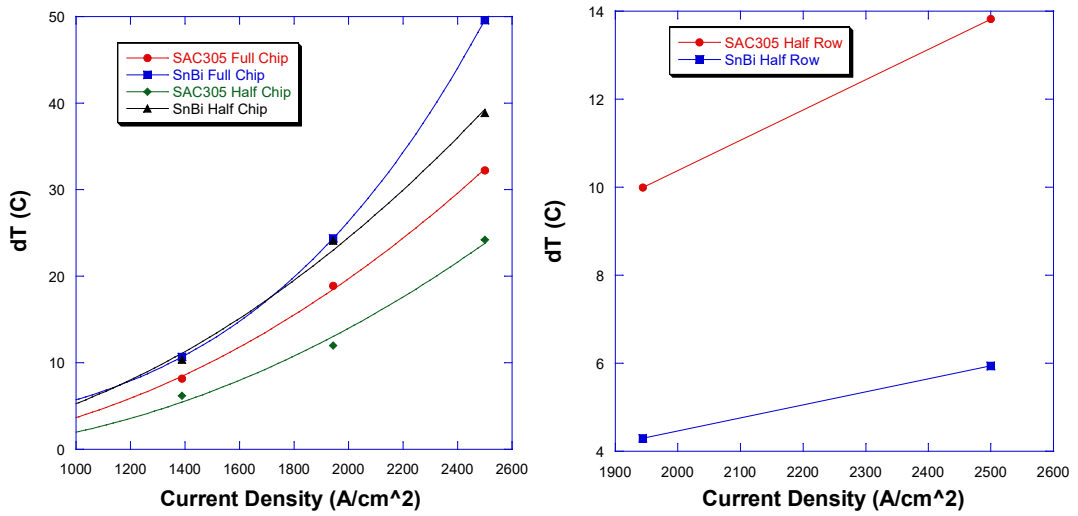


Figure 16. Comparison of SAC305 and SnBi ΔT_H Full Chip and Half Chip measurements (left) and Half Row measurements (right) as a function of current density.

This behavior is further evidenced when comparing values of τ_H between both SAC305 and SnBi samples at the full chip and half row levels. The value of τ gives the story of how long a given sample is taking to reach its saturation temperature, meaning that intuitively samples that are expected to reach a higher temperature (i.e., higher resistance samples) should have higher values of τ with the same current density. From Fig. 17 the full chip measurements show that the SnBi sample has higher values of τ_H per current density than the SAC305 sample. This is expected as the higher resistive sample should take longer to heat per given current density as it must heat to a higher temperature, given that all other parameters including PCB structure are kept constant and the only difference between samples is solder alloy. Contrast this with the plot in Fig. 17 of the τ_H of the half row and the behavior is completely opposite in that the SAC305 sample exhibits a noticeably greater value than that of the SnBi sample. This again would contrast the notion that simply higher resistive samples will create more heat than lower resistive ones.

Looking at these results through the scope of the Foster Model, the SAC305 sample should have a lower value of τ_H if all other parameters are kept equivalent to the SnBi sample. As τ_H is a function of R_{th} and C_{th} it can then be assumed that in the half row tested some parameter is causing both values to increase in the SAC305 sample. An exploration and proposed explanation as to why is discussed further in section 4.2.

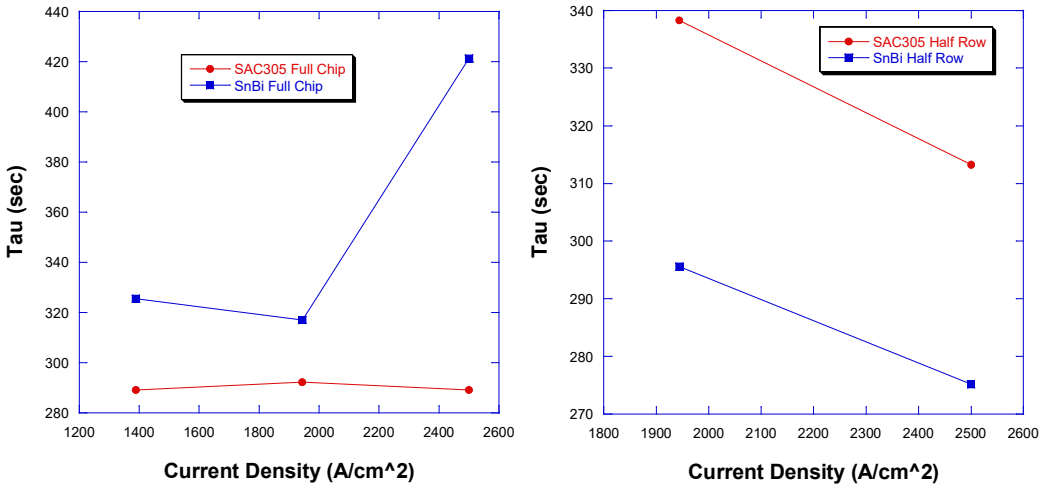


Figure 17. Comparison of SAC305 and SnBi τ_H Full Chip measurements (left) and Half Row measurements (right) as a function of current density.

4.2 Microstructural Analysis

Comparing solder cross-sections of SAC305 and SnBi samples shows interesting results in that SAC305 samples showed several interfacial defects in the form of large cavities/voids as opposed to SnBi samples that exhibited very few if any at all. Fig. 18 shows cross-sectional images of a SAC305 and SnBi sample in BSE mode, respectively.

Under testing conditions these large cavities will experience higher levels of heating due to current crowding around the edges of such defects. Current crowding can be thought of as consolidated current density, meaning at these areas where the current's path is blocked it will have

to force its way around creating a localized higher current density than the bulk of the solder joint. This will consequently result in higher temperatures in solder joints with defects as there are more points of current crowding. This phenomenon gives a partial explanation to how the full and half chip measurements show expected behavior, and the half row measurements show SAC305 having increased levels of joule heating than SnBi. If the tests were conducted on ten SAC305 solder joints that contained many more of these large cavities than the ten solder joints tested for the SnBi the JH of the SAC305 would theoretically be higher due to vastly increased levels of current crowding. Tests at the full chip and half chip level in contrast would then give measurements based on the entire package resistance averaging any of the microstructural defects seen in only certain solder joints. This would then explain why tests of higher levels of solder joints show expected results of SnBi having the higher level of JH as it has the higher resistance.

From the SEM images it is apparent that the large cavities are along the interface of the solder at both the chip side and PCB side. These defects though are not typical of damage from thermal or electrical testing but that of unoptimized manufacturing processes. Typical thermal fatigue and electromigration damage presents itself in the form of Kirkendall voids and cracks accompanied with an increase in intermetallic compound (IMC) formation. These SEM images suggest that the defects are during the initial reflow process as there are no signs of other failure mechanisms.

Our suspicion for these differences seen between the microstructures of SAC305 and SnBi samples is CTE mismatch and warpage. SAC305 has a much higher processing/reflow temperature in comparison to SnBi. SAC305 typically has around a 230-245˚C reflow temperature, whereas SnBi can be reflowed in a wide range of around 160-190˚C depending on added elements. At a minimum SnBi can be reflowed 40 ˚C lower than SAC305. This higher thermal gradient between

different materials exacerbates the effects of CTE mismatch in packages using SAC305 than SnBi based solders. With higher temperatures comes greater amounts of warpage and therefore stresses on both the Si chip side and PCB side. These compressive or tensile stresses could be the explanation for the large cavities in the SAC305 solder joints as it would cause some amounts of solder to displace as the package is undergoing cooling.

Also, the variance in PCB structure for each solder joint may be playing a key role in the cavity formation. It is our assumption that with the different combinations of VIPPO and BD seen in all but the first PCB structure the different thermal resistances and capacities seen in adjacent joints could lead to nonuniform cooling during the manufacturing process. As such, it would then be assumed that the PCB structure with VIPPOs under each solder joint will have the least number of defects due to the uniformity of heat dissipation. Future work is planned to determine if such is the case.

Another process we speculate that may be affecting the JH behavior of samples is discontinuous and localized warping of the Si chip causing internal stresses due to the different PCB structure under neighboring solder joints. Fig. 9 and 10 show the breakdown of this layout for two of the PCB structures. For five out of the six PCB structure configurations a solder particular solder joint with a VIPPO may be surrounded by solder joints with BD and vice versa. This could create areas of different cooling rates in the Si chip causing stresses to form. These stresses would then cause deformation of the Si in a tensile or compressive manner across the entire chip. This would result in the chip having deformations in its structure after heating and cooling resulting in defects and cracks forming in the Si. These types of damage and defects in the Si would then also act as points of excessive heating due to current crowding. A schematic showing how these internal stresses could form in a package is shown in Fig. 19. This effect still needs to

be further studied to find a direct correlation between the types of damage seen in the Si and the heat dissipation method attached on the PCB side of the solder.

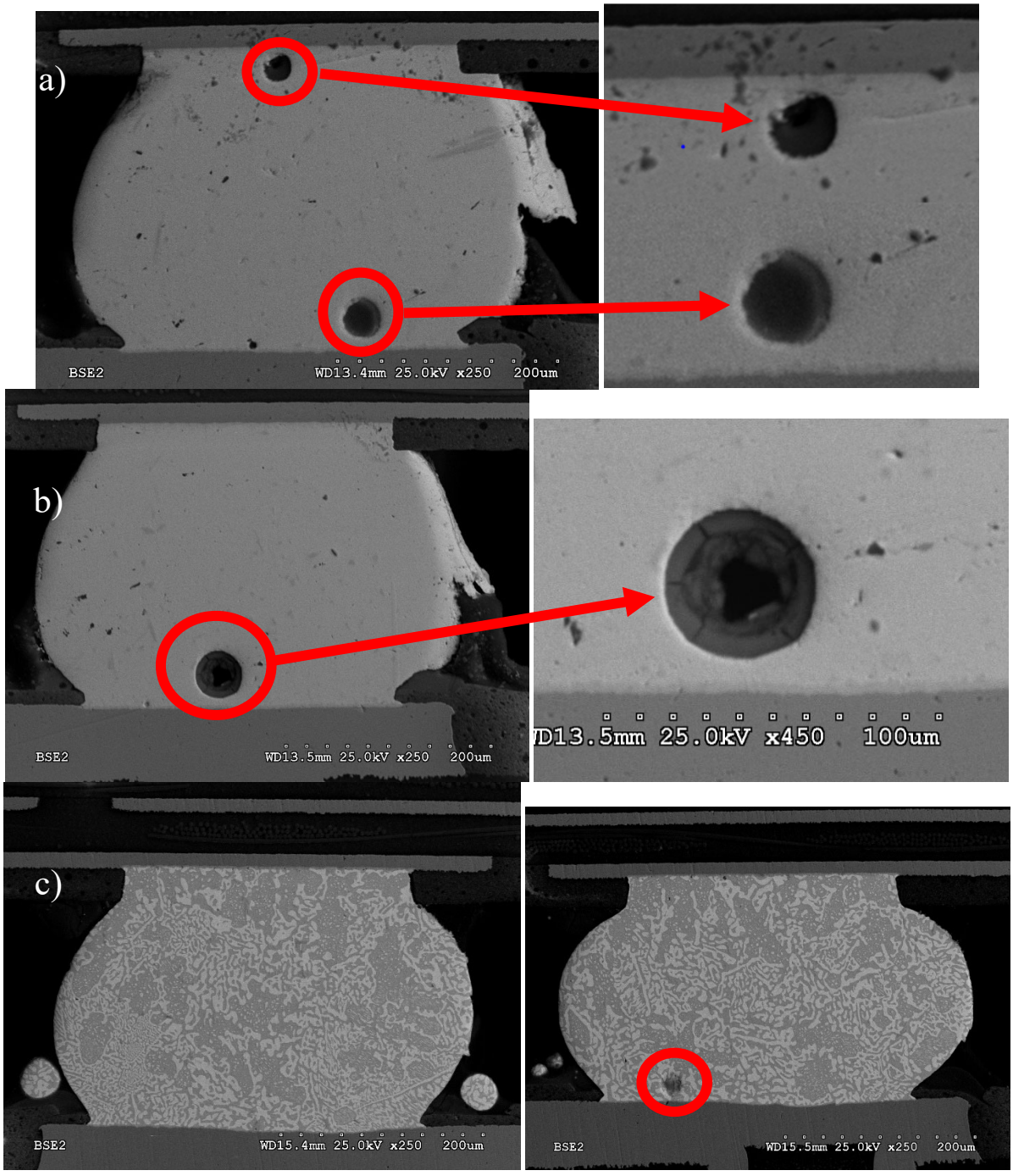


Figure 18. BSE mode SEM images of (a-b) SAC305 sample solder joints and (c) SnBi sample showing cavities formed during manufacturing process.

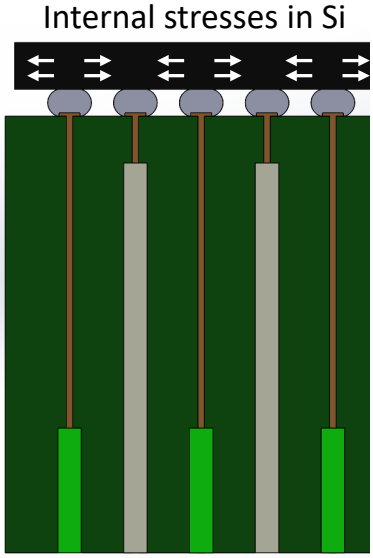


Figure 19. Schematic of Si internal stresses due to offset cooling caused by different solder joints having different heat dissipation methods.

CHAPTER 5. INDUSTRIAL IMPLICATIONS OF FINDINGS

5.1 Solder Defects During Manufacturing Processes

Macrovoids or process voids refer to large spherical or elliptical cavities that develop within solder joints during the manufacturing process. The formation of macrovoids is primarily attributed to the entrapment of gas bubbles that arise during the reflow process. These gases originate from various sources, including chemicals present in the flux, moisture present in the PCB, or water vapor generated through solder oxidation that reacts with flux when their boiling points are surpassed, resulting in gas entrapment [20]. Several factors associated with suboptimal manufacturing processes contribute to the occurrence of these macrovoids, such as inadequate substrate surface finish, excessive flux usage, heightened solder paste oxidation, and suboptimal reflow time and atmosphere conditions [20]. These manufacturing defects are well-documented within the industry, and certain mitigation strategies have been implemented to minimize their occurrence. However, the present research aims to explore factors that have received limited attention thus far. Specifically, it investigates the potential impact and significant role of thermal resistances and capacities of connected components on the formation of manufacturing defects in solder joints.

When comparing the typical microstructures of solder joints containing macrovoids resulting from entrapped gas with the solder joints investigated in this research, a distinct difference becomes apparent. In the former case, the cavities caused by trapped gases are typically located near or at the top interface of the solder, as the bubbles rise during the reflow process. However, in our samples, voids were unexpectedly observed in both the top and bottom interfaces of the solder. This observation suggests the involvement of additional mechanisms that require investigation to enhance the reliability of solder joints from their initial stages. The implications

of this investigation extend to various industrial aspects, including optimizing packaging designs and refining manufacturing processes. By addressing these issues, not only can the behavior of Joule heating be improved, but also other reliability concerns such as electromigration and thermal fatigue can be addressed.

One particular aspect of packaging design that warrants further study is the heat dissipation capacity of adjacent interconnects, even when all other parameters are held constant. This necessitates design engineers to consider not only the direct elements connected to each solder joint, such as substrates, surface finishes, vias, and traces, but also the secondary components linked to each joint. These secondary components may include the PCB, die/chip, additional layers of vias and traces, and other elements introduced for intricate and complex applications. In the case of the samples used in this study, the only differing parameters between SAC305 and SnBi samples were the solder alloy and reflow temperatures, while all other components and structures remained constant across the chips. This prompts a deeper investigation into the root causes of macrovoid formation at both the top and bottom surfaces.

The observation of macrovoids in our research, occurring at different locations within the solder joints, points to another potential mechanism, namely the stresses induced by differential cooling, as the primary culprit for these defects. A closer examination of the specific half-row utilized in our smaller-scale tests revealed an alternating PCB structure for each solder joint, as depicted in Fig. 20 (highlighted by the red box). The varying heat dissipation of individual solder joints may hold the key to understanding the unexpected microstructure and JH behavior observed. Throughout the manufacturing process, including preheating, reflow, and other heating/cooling cycles, each solder joint within the row experiences different temperatures compared to adjacent joints at any given time. This introduces unknown effects that currently rely on speculation,

emphasizing the need for further research to gain a comprehensive understanding of these underlying mechanisms.

Our main hypothesis revolves around the notion that the thermal gradient generated by the contrasting heat dissipation of the surrounding joints during heating or cooling induces nonuniform tensile and compressive stresses in the solder joint. To illustrate this, let's consider a closer examination of the third solder joint from the top of the half-row under investigation. Surrounding this joint, we find three joints with a different PCB structure (referred to as BD20), followed by another joint with the same PCB structure. Consequently, the solder joint in question would experience significantly higher heating or slower cooling compared to the three dissimilar adjacent joints. These thermal differentials could induce stresses within the solder, causing certain regions to separate from the bulk material, thereby leading to the macrovoids observed in our research. These stresses primarily manifest from the PCB side rather than the chip side, as that is where the main differentiating factor lies, explaining the presence of macrovoids on the bottom side of the solder joints as well.

In our future endeavors, we have devised a plan to conduct testing on the specific half-row indicated by the green box in Fig. 20, utilizing both the same SAC305 and SnBi samples. This particular row exhibits minimal variation in the PCB structure, not only within the joints of the row itself but also in relation to the adjacent joints, as the entire left side of this row lacks any joints. If our hypothesis holds true, it is expected that this half-row will display significantly fewer macrovoids, or potentially none at all, owing to the more uniform heat dissipation among all the solder joints. Consequently, the results obtained from this half-row will provide evidence supporting the notion that SAC305 exhibits a lower degree of JH, aligning with expectations due to its lower resistivity compared to the SnBi sample. To further validate and reinforce the results,

subsequent cross-sectional analysis will be performed following the completion of the aforementioned testing. This analytical approach will offer additional insights into the internal structure and characteristics of the solder joints, corroborating the findings obtained from the macroscopic observations.

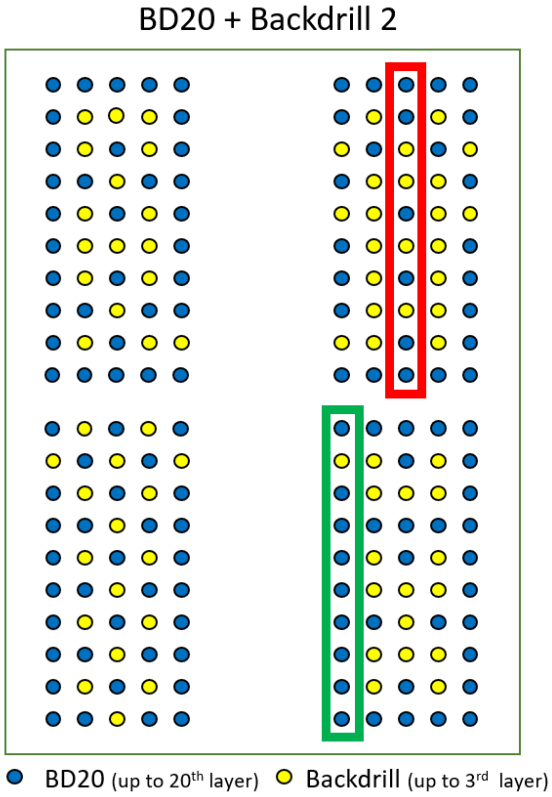


Figure 20. Diagram outlining specific half-row used for testing and half-row to be used in future testing.

CHAPTER 6. CONCLUSION AND FUTURE WORK

6.1 Overall Conclusions

A thorough investigation of various package parameters and testing conditions has revealed that both factors significantly and intricately impact the JH behavior of a package at certain levels. Specifically, a study was conducted to compare the JH behavior of SAC305 and SnBi solder alloys under identical testing conditions of current density, PCB structure, and number of solder joints tested. The study demonstrated that JH is not solely dependent on resistance and resistivity. In fact, the testing of 180, 80, and 10 solder joints indicated that at the smallest scale, the lower resistive material, SnBi, released more heat than the higher resistive material, SAC305. Conversely, testing at larger scales showed the expected behavior where SnBi samples had the highest level of JH. The contrasting behavior of the materials was not well understood until a thorough microstructural analysis was performed. These findings suggest that factors other than resistance and resistivity, such as the microstructural characteristics of the materials, play a significant role in determining JH behavior on the micro-scale.

SEM imaging of the cross-section of SAC305 and SnBi solder joints revealed the presence of large cavities near the interfaces of the solder joint mainly in SAC305 samples. These defects create points of potential current crowding and therefore higher heat than typically expected. Testing at the higher scale would then average out these singular cavities and behave in accordance with the total resistance of the package as opposed to a select few solder joints with these cavities. Further investigation into the microstructure revealed the effect of the different heat dissipation methods under each solder joint affecting local heating and cooling rates of the solder joint, Si chip, and PCB creating stresses and therefore defects. The defects seen in these samples are attributed to the manufacturing process and SAC305 having a much higher processing temperature

than SnBi, creating more internal stresses in the overall package. From this it was concluded that not only is resistance a main factor in determining JH behavior but also the microstructure and some unknown factors play a significant role in heat production in packages.

6.2 Future Work

Investigation into the effect of microstructural defects on JH behavior has generated intriguing results that have led to the discovery of new JH mechanisms. However, despite these findings, the precise relationship between microstructural defects and JH behavior remains largely unknown as the behavior is not observed on the macro-scale. To gain a better understanding of this relationship, future studies must focus on analyzing samples that possess known defects, similar to those that were investigated in the present research and compare them to samples that are known to have no defects. Additionally, small scale testing of these samples in different areas of the chip is necessary to determine whether there exists a statistical correlation between microstructural defects and JH behavior. Such tests would serve to narrow the correlation between microstructural defects and JH, helping to provide more accurate and precise results. Furthermore, to isolate the JH of the solder joints, it is important to determine the heat dissipation factor for each side of the Si chip and PCB, as well as the magnitude of their contribution to the overall JH. By understanding these factors, researchers will be better equipped to investigate the relationship between microstructural defects and JH behavior.

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