Study of Electron Energy Filtering for Cold Electron Transport at Room Temperature

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ABSTRACT

The Fermi-Dirac thermal excitation of electrons at room temperature has been a significant limitation to many technologically important phenomena such as single electron transport. The electron thermal excitation also degrades the performance of modern electronic devices as well as spintronic devices. The scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs) is hindered due to the thermal excitation of electrons at room temperature. Suppression of the thermally excited electrons at room temperature would therefore enable further scaling of the transistors, and in turn, improve the performance of the electronic devices.

This study demonstrates the suppression of electron thermal excitation at room temperature without using cryogenic cooling. This is done using a quantum well discrete energy level as an electron energy filter. The energy filter is placed between a source electrode and silicon, where the thermally excited electrons in the source are filtered out by a quantum well state and the energy-filtered cold electrons are injected to silicon. The energy filtering stack consists of a thin quantum well layer (~3nm/4nm/5nm SnO_2) bounded by tunneling barrier 1 (~0.5nm Al_2O_3 or 1nm Si_3N_4) and tunneling barrier 2 (~1.5nm Native SiO_2). This energy filtering structure has enabled cold-electron injection to silicon, with an effective electron temperature of ~0.08 Kelvin at room temperature. The current-voltage measurements show abrupt current jumps at specific voltages, which correspond to the alignment of a quantum well discrete energy level with the silicon conduction band edge. The differential conductance plot for the observed abrupt current jumps shows an extremely narrow peak, with a full width at half maximum (FWHM) of ~0.025 mV, corresponding to an effective electron temperature of ~0.08 Kelvin at room temperature. The cold-electron injection to silicon opens possibilities for extremely energy-efficient transistors with subthreshold slope values significantly below the room-temperature

subthreshold slope limit of 60mV/decade, e.g., 2mV/decade (corresponding to an effective electron temperature of ~10 Kelvin).

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Chapter 1: Introduction

One of the core components of modern electronic devices is the transistor[1-5]. As such, several research efforts have been focused on improving device performance of these transistors to allow for further scaling of these devices[6-13]. However, in recent times, any further scaling of metal-oxide-semiconductor field-effect transistors (MOSFET) has reached a bottleneck in terms of power consumption efficiency with the reduction in transistor size. At room temperature, due to thermal excitation of electrons, following the Fermi-Dirac distribution[14-18], the electrons are able to overcome the energy barrier and generate a current flow in the MOSFET devices. This results in an unwanted leakage current leading to a gradual subthreshold slope[19-22], which in turn forces the supply voltage to a high value (>0.5V), and thus limiting the scaling of these transistors. The electron thermal excitation is also the root cause of the suppression of many technologically important phenomena like single electron transport[23-37], coulomb staircase[38-49], coulomb blockade[50-62], etc. The suppression of electron thermal excitation will be a significant contribution towards being able to observe and implement these phenomena in our day-to-day life. Thus, electron thermal suppression and lowering transistor subthreshold slopes[63-82] has been the focus of many recent research efforts. High-k gate dielectrics[83-92] for steep subthreshold slopes, impact-ionization transistors[93-96], device architectures utilizing nano or micro electro-mechanical forces[97-104] and band-to-band tunneling in Tunnel Field Effect transistors have been investigated towards lowering the subthreshold slope values below the subthreshold slope limit. While these efforts were successful in suppressing the electron thermal excitation, they were required to be carried out at extremely low cryogenic temperatures[105-108].

This research presents a novel energy filtering architecture, by using a quantum well discrete energy level to filter out thermally excited electrons, which successfully demonstrates cold-electron injection to silicon at room temperature with an effective electron temperature of 0.08 Kelvin. The architecture effectively suppresses thermal excitation of electrons through the utilization of discrete quantum well energy levels to filter out the thermally energetic electrons and allow only the thermally suppressed cold electrons to tunnel through to the silicon conduction band upon application of a bias when the silicon conduction band is aligned with the quantum well discrete energy level.

Chapter 2: Energy Filtering Principle

2.1 Introduction

The energy filtering architecture utilized here to filter out thermally excited electrons consists of a thin quantum well layer sandwiched between two thin tunneling barrier layers, which in turn are bounded by source metal contact and silicon conduction band connected to a silicon metal contact. The discrete energy levels[109-111] of the quantum well layer is responsible for the filtering of thermally excited electrons from the source metal before they are able to enter the silicon conduction band channel.

2.1.1 Quantum Well Confinement

When one or more of the dimensions of a solid are reduced to nanoscale, the confinement of particles in the resulting nanostructure, usually electrons or holes, leads to a dramatic change in their behaviour. Quantum well is such a nanostructure wherein the particles are confined in one dimension[112, 113] whereas they are free to move in the other two directions. Typical nanoscale dimension of the confinement is 1-1000 nm. At such a scale, the dimension can be comparable to the de Broglie wavelength of the matter wave associated with the moving electron.

The energy of a matter wave associated with a moving electron which is experiencing no net force can have any reasonable value. It is just like a wave travelling along a stretched string of infinite length can have any reasonable frequency. But the confinement of a wave leads to quantization – that leads to the existence of discrete energies. This can be conceptually shown using an example of infinitely deep potential well as below.

In an ideal situation where the potential energy of the electron outside the well is assumed to be infinitely greater than that of an electron inside the well. If an electron in the well approaches either of the ends of the infinitely deep well, a force of essentially infinite magnitude reverses the motion of the electron, thus trapping it. Just like the standing wave in a length of a stretched string, the matter wave describing the confined electron in the well must have nodes at the either ends of the well. Then the quantum well of length L, can allow only those matter waves of de Broglie wavelength λ, for which:

$$L = n\frac{\lambda}{2}, \quad n = 1, 2, 3, ...$$

(1)

Assuming the total mechanical energy of the electron E is equal to its kinetic energy, the de Broglie wavelength can be expressed in terms of the momentum p and then energy E and mass m of the electron as:

$$\lambda = \frac{h}{p} = \frac{h}{\sqrt{2mE}}$$

(2)

It follows from Eq. 1 and Eq. 2 that the energy of the moving electron in the infinitely deep quantum well is quantised according to:

$$E_{\mathrm{n}} = (\frac{h^2}{8mL^2})n^2 \quad , \quad \text{for } n = 1,2,3, ...$$

(3)

The probability of detecting the trapped electron in the quantum well can be worked out by solving the Schrodinger's equation for the associated wave function. The modulus squared of this wave function gives the probability density- that is the probability of detecting an electron in a specified volume at a specified distance along the length of the well. It can be shown that these probability densities are also quantised and assume the sinusoidal forms with nodes at the boundaries of the wall. The frequency of these waves assumes discrete values and so does the energy.

In a practical case, the quantum well will not be infinitely deep. Such finitely deep quantum wells may be realized in semiconductors for example, by having a material of low bandgap sandwiched between two layers of a material with a wider bandgap. Though the discrete nature of the allowed energies of a moving electron in such a well is preserved, there is no simple formula for the energy levels as it is for infinitely deep quantum well. The wave function (and corresponding probability density function) is sinusoidal inside the well and exponential outside. Matching the sinusoid and exponential functions at the boundaries so that they join smoothly is possible only for certain specific values of the total energy of the electron. Finding the values of the discrete energies of a moving electron in such a well is a fairly complex mathematical problem that requires solving a transcendental equation by numerical approximation.

2.1.2 Quantum Well Energy Level Separation and Control

Upon entering the discrete energy level of the quantum well layer, the thermally excited electrons are trapped in the discrete energy level[114, 115] as they do not have any path available for excitation to a higher energy level if the energy level separation between adjacent discrete energy levels several fold larger than the room temperature thermal energy (>>0.025eV). The probability of electron excitation to a higher energy level is given by $e^{-(\Delta E/kT)}$;

where ΔE is the energy level separation.

T is the device operation temperature.

κ is the Boltzmann constant.

Thus, with the increase of discrete energy level spacing, the lower the probability of electron excitation to a higher level. The quantum well discrete energy levels' energy is given by the following equations:

$$\varepsilon_{Qw}(n) = (-a_n)\left[e^2 E^2 \hbar^2 / 2\, m_{eff}\right]^{1/3}$$

(4)

or $$\varepsilon_{Qw}(n) = (-a_n)\left[\left(E_{bending} \,/\, d\right)^2 \hbar^2 \,/\, 2m_{eff}\right]^{1/3}$$

(5)

where ε_{Qw}(n) is the energy of discrete energy levels, m_{eff} is the effective electron mass in the quantum well conduction band, e is the charge of an electron, E is the electric field across the quantum well, a_n is the sequence of airy function zeroes (a_0=-2.34, a_1=-4.01, a_2=-5.52, etc), $E_{bending}$ is the amount of band bending in the QW conduction band, d is the thickness of the QW film and $\hbar$ is Plank's Constant. From the above equations (4) and (5), the separation of energy levels in the quantum well is a function of Electric field and quantum well width given by ($E_{bending}$/d) and also the effective electron mass in the quantum well, m_{eff}. Now, Electric field across the quantum well is proportional to the charge density at the quantum well/ silicon dioxide (tunneling barrier 2) interface or the silicon dioxide (tunneling barrier 2) / silicon substrate interface.

The effective electron mass in the conduction band of the quantum well layer can be utilized to control the energy level spacing in the quantum well. The equation 3 and 4

shows that the energy values of the energy levels is proportional to 1 / $m_{eff}^{1/3}$. This would mean that a smaller effective mass would create a larger energy level separation in the quantum well discrete energy levels leading to a near zero probability of electron excitation to a higher energy level in the quantum well, which in turn resulting in that there will be no path available for electron excitation in the quantum well and the electrons will be suppressed to an effective electron temperature of Zero Kelvin. In this research, we investigate semiconducting metal oxides with low effective electron mass like Cr_2O_3 (m_{eff} = 1.84 m_e) and SnO_2 (m_{eff} = 0.28 m_e).

2.1.3 Cold-Electron Transport: Energy Filtering

Previous research in our group was able to successfully achieve cold-electron transport[116-119] using a Double barrier tunneling junction[120-125] and quantum well[126, 127] as the energy filtering architecture. The device architecture consisted of Source metal, a 2nm Cr_2O_3 layer which forms a quantum well layer, tunneling barrier 1, quantum dot discrete energy level as channel, tunneling barrier 1 and drain metal.

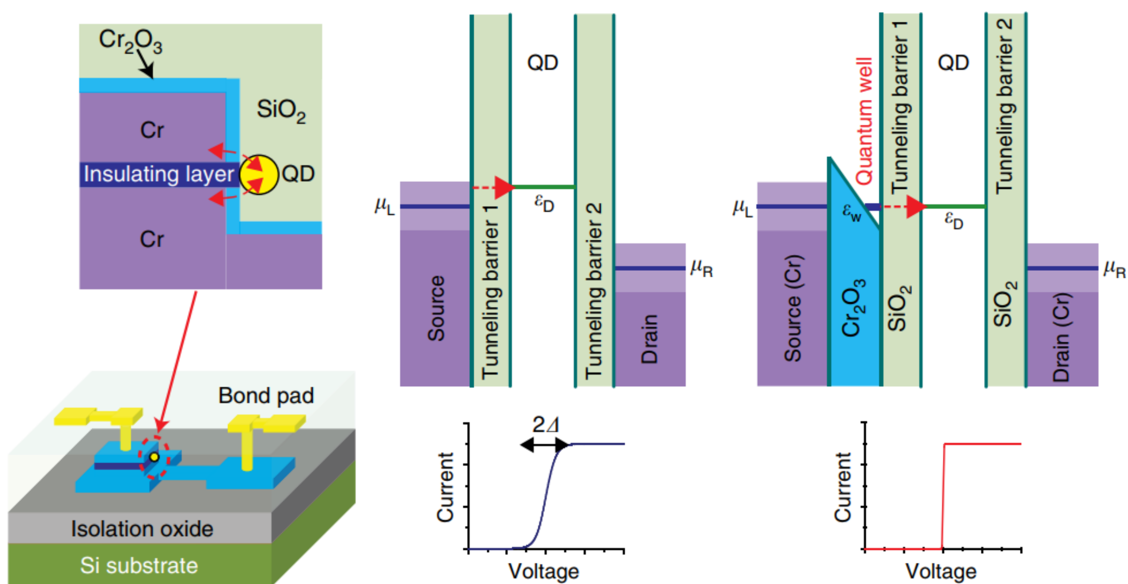


Figure 1: DBTJ device structure and energy band structure[23]

For a conventional MOSFET device, at room temperature, the thermally excited electrons from the source electrode are able to tunnel through the tunneling barrier into the quantum dot discrete energy level and reach the drain electrode. The fermi-dirac thermal smearing at the source electrode at room temperature, results in electrons occupying energy higher than the source metal fermi level. This leads to a gradual subthreshold slope with applied bias. However, with the introduction of a quantum well layer between the source and quantum dot channel, the thermally excited electrons from the source metal enter the discrete energy level of the quantum well layer and are trapped. This is due to the energy separation between the adjacent discrete energy levels in the quantum well layer being much larger than the room temperature thermal energy (>>0.025eV). As there is no path of excitation available to the trapped electrons, they are effectively cooled to extremely low temperatures (ideally 0 Kelvin). The electron transport only occurs when the quantum dot discrete energy level is aligned with the quantum well discrete energy level when a bias is applied to lower the quantum dot discrete energy level. This results in an abrupt current increase with applied bias which in turn leads to a steep subthreshold slope.

Chapter 3: Fabrication Procedures

3.1 Fabrication Procedure for Cold Electron Transistors.

This chapter describes in detail the fabrication procedure for quantum-well mediated electron transport transistor to achieve cold electron transport at room temperature. In this chapter we also discuss the problems encountered during fabrication and the solutions used to solve these issues like gate oxide leakage issues, passivation layer deposition spill over, wet etching and reactive etching thickness control. Our devices are fabricated on 4-inch p-type, p++ type and n-type, n++ type Silicon wafers. The Sample preparation utilizes fabrication processes like Thermal oxidation, Doping, Photolithography, Reactive Ion

Etching, Wet Etching, Electron Beam Deposition, and Sputter Deposition, etc. to complete the device and get it ready for IV characterization. The complete fabrication process is carried out in a class-10/100 cleanroom facility at the Nanofab Research Centre at The University of Texas at Arlington. The following chapters discuss stepwise in detail the fabrication procedure.

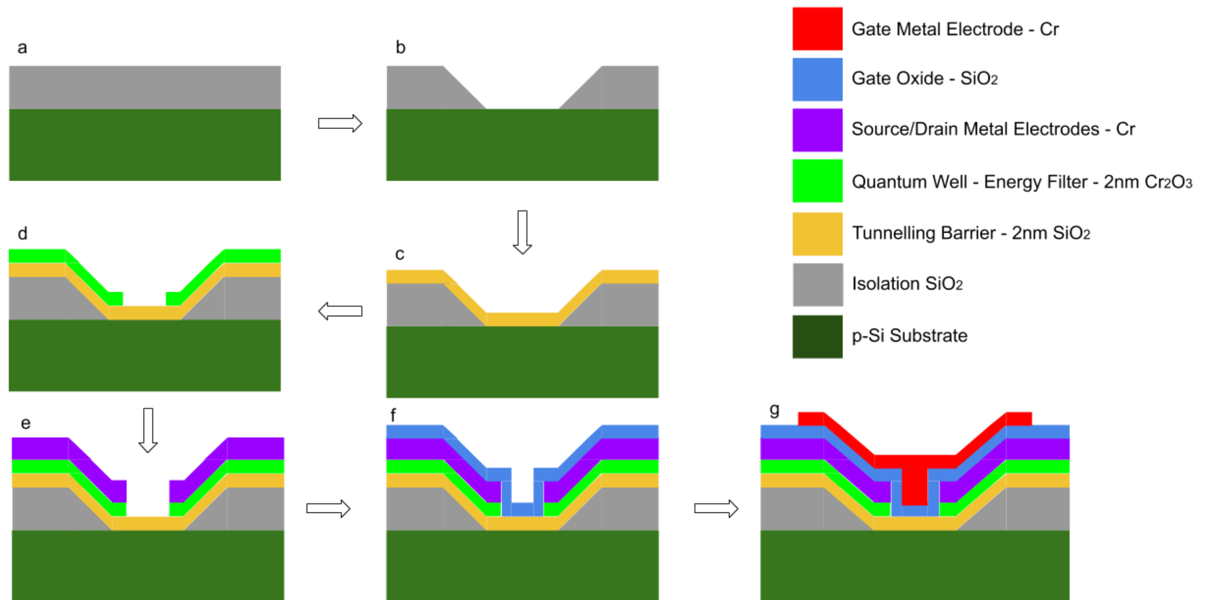


Figure 2: Process flow for the fabrication of a cold-electron transistor

3.1.1 Sample Preparation

For the fabrication of cold-electron transistors, we start with 4-inch p-type and n-type Silicon wafers. The wafers need to be thoroughly cleaned prior to beginning the fabrication procedure. The wafers are immersed in a freshly prepared piranha solution, which is a mixture of sulfuric acid and hydrogen peroxide in a 3:1 ratio. We take 60 mL of Sulfuric acid in a glass beaker and add 20 mL of hydrogen peroxide to it slowly along the sides of the beaker. Precaution needs to be taken when utilizing acids by wearing full PPE equipment when handling acids. The wafers are immersed in the Piranha solution for 30 min to remove any organic impurities. The wafer is then taken out and immersed in a DI

container for 5 minutes, followed by rinsing under running DI water and followed by immersion in a second DI water container for 5 minutes and then blow drying it with Nitrogen. This thorough DI water rinsing ensures that all piranha solution and residue is removed from the Silicon wafer. The Piranha cleaning step is followed by immersing the wafer in 49% Hydrofluoric acid for 10 minutes followed by 5-minute immersion in the first DI water container, 1 minute rinsing under running DI water and then immersing it in second DI water container for 5 minutes and then blow drying it with Nitrogen.

3.1.2 Thermal Oxidation (Passivation Layer)

After the thorough cleaning of the substrate wafers, the wafers were loaded into a thermal oxidation chamber (Tystar Oxidation Furnace) to grow a nominal thickness of 250nm of Silicon dioxide. The Silicon dioxide was grown using dry oxidation. The oxidation parameters were as follows:

Tystar Thermal Oxidation Furnace: KOHD250.001

Idle Temp: 450 C

Boat Out: 15 min

Boat In: 15 min

Ramp 700 C: 30 min ; N2: 5000 sccm

Stabilize: 30 min ; N2: 5000 sccm

Ramp 1100 C: 2 hrs ; N2: 5000 sccm

Hold: 3hrs 30mins ; O2: 3000 sccm

Anneal: 20 min ; N2: 5000sccm

Ramp down 700 C: 2 hrs ; N2: 5000sccm

Hold 700 C: Till alarm Acknowledged

The grown silicon dioxide thickness is measured using Nanospec at the centre and 4 quadrant regions to confirm the film thickness and uniformity. The 250nm thermal silicon dioxide is required as a passivation layer and a mask in order to leave a good margin for printing the silicon window pattern during the First Mask step which is explained in the next subsection.

Figure 3: Tystar Oxidation Furnace for Thermal Oxidation of Silicon

3.1.3 First Mask Lithography

The 250nm Silicon dioxide grown Si wafer is cut into four quadrants in preparation to print the First mask pattern to expose silicon surface and create a silicon window. The entire first mask lithography procedure is detailed in the subsections below.

3.1.3.1 Photolithography for Silicon Window Pattern Exposure

Each of the quadrants is spin-coated with a negative photoresist – NR9-1000PY. The Negative photoresist is coated on the sample quadrant by using a dropper to cover the entire surface and then spin-coated. The spin-coating parameters are as follows:

Step 1:

500 rpm; 100 rpm/s; 5 seconds

Step 2:

3000 rpm; 1000rpm/s; 60 seconds

Step 3:

0 rpm; 1000rpm/s; 0.1 seconds

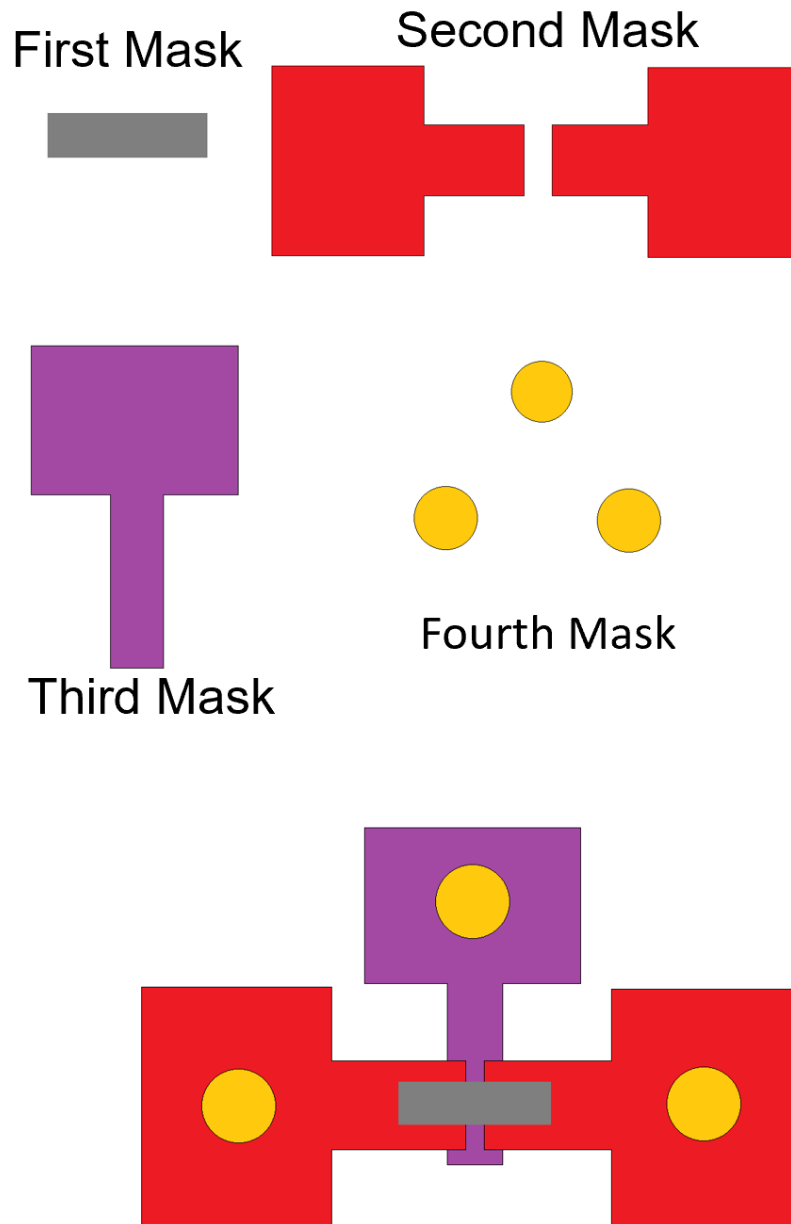


Figure 4: Mask design for the Cold-electron transport device fabrication

The spin-coated sample is then pre-baked at 150 °C for 1 minute on a hot plate. The samples are now ready for photolithography pattern exposure.

The photolithography mask is designed in such a way that it is divided into four quadrants, with each quadrant containing a pattern for the first, second, third and fourth mask patterns respectively. The photolithography mask is loaded onto the OAI Aligner with the First Mask pattern in the top right section. The substrate carrier wafer is loaded beneath the photolithography mask. The sample quadrant is fixed on the substrate carrier wafer beneath the first mask pattern. The quadrant and mask are aligned such that the entire first mask pattern is aligned within the sample quadrant. The first mask is pressed on to the sample quadrant and contact vacuum is turned on and the pattern exposure is carried out.

The photolithography patterning parameters are as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 19.6 mW/cm^2

Exposure Time: 6.1 seconds

Dose: 120 mJ/cm^2

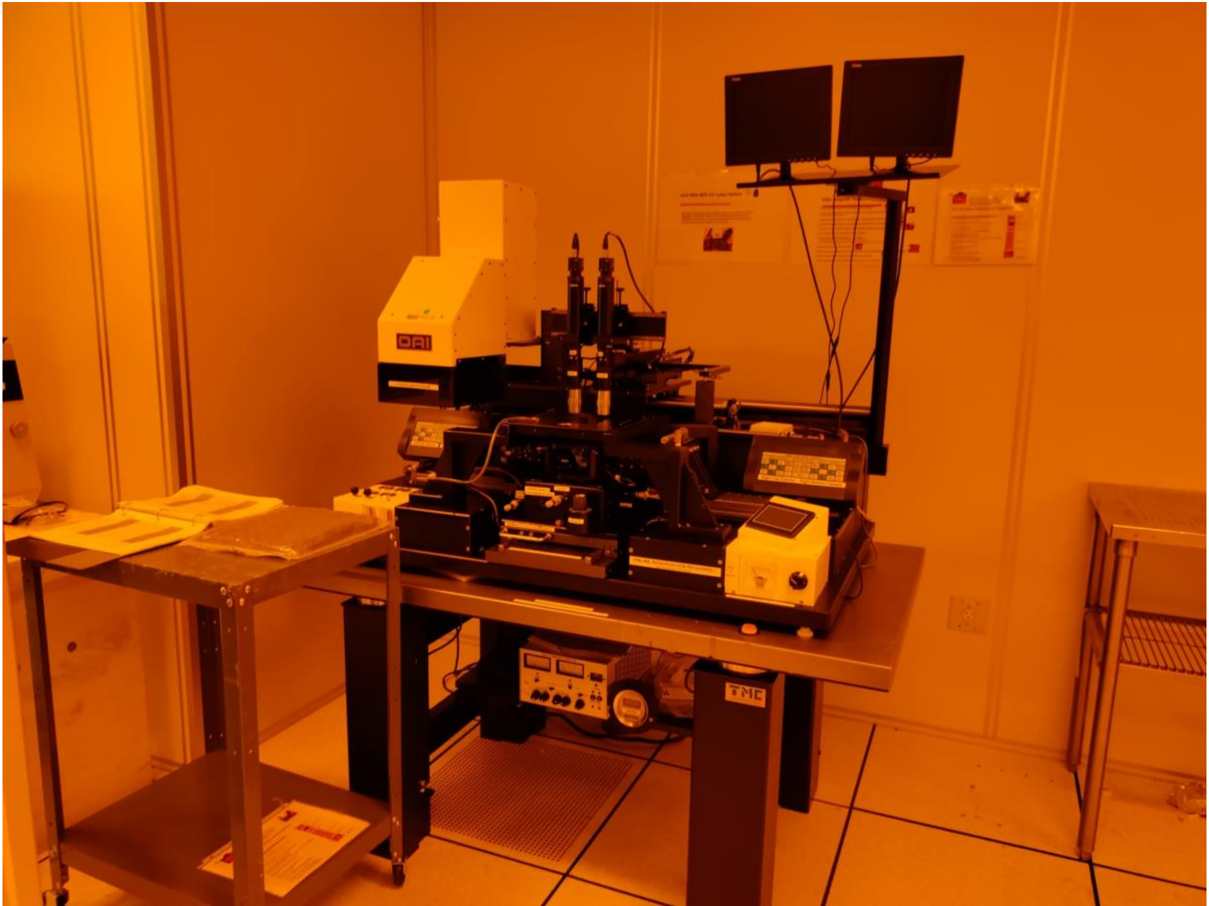


Figure 5: OAI Aligner Equipment for UV Photolithography

The Exposure time is adjusted based on measured Intensity so that the final dose is 120mJ/m^2. After exposure, the sample quadrant is then post baked at 100 °C on a hot plate for 1minute. The sample is allowed to cool down to room temperature. The sample is then developed in a photoresist developer – RD6. The sample is immersed in the developer - RD6 for 25 seconds with regular shaking (development time increased from 10s to 25 seconds due to observed resist residue in SEM after lift-off process) followed by DI water immersion in beaker 1 for 5 minutes with regular agitation and then in DI water beaker 2 for 5 minutes. The sample is then gently blow dried with nitrogen.

3.1.3.2 Silicon Dioxide etching using Reactive Ion Etching

The next step is to expose the Silicon surface inside the pattern area. This region will be used to deposit the energy filtering layer stack. Thus, the silicon in the pattern area will need to be exposed. The silicon dioxide present in the window pattern is etched using reactive ion etching in the Technics Macro RIE – 8800 equipment.

Figure 6: Technics Macro RIE – 8800 equipment for Reactive Ion Etching

A margin of 40nm silicon dioxide is left behind after the RIE to protect the silicon surface from the RIE plasma. The RIE etch step with a 40nm margin creates an uneven circular region at the centre of the wafer quadrant resulting in a difference in SiO_2 thickness of ~10nm at the centre region and the side region of the quadrant. We found that increasing

the SiO2 etch margin to 80 nm reduces this variation to ~1-3 nanometres. Thus, the SiO2 RIE etch recipe was adjusted to leave 80 nm SiO2 margin. The Silicon dioxide etching is separated into 2 stages with an oxygen clean step after each Silicon dioxide etch step. The silicon dioxide etch time is established by optimizing the etch rate by etching for different times using the CF4/O2 etch recipe. The different etch times and etch thicknesses are plotted and the etch rate for Silicon dioxide is calculated to be 0.7 nm/s.

The Reactive Ion Etching Parameters are as follows:

Step 1: 600W, 170mT, CF4: 30 sccm, O2: 7.2 sccm

Step 2: 350W, 200mT, O2: 11.0 sccm, 300s

Step 3: 600W, 170mT, CF4: 30 sccm, O2: 7.2 sccm

Step 4: 350W, 200mT, O2: 11.0 sccm, 300s

Once the RIE etching is done, the photoresist from the sample needs to be removed and measure the actual etched thickness.

3.1.3.3 Lift-off for Photoresist removal

The sample is immersed in Acetone and sonicated for 15 minutes, followed by rinsing in IPA (IPA rinse is done after acetone to avoid acetone residue left behind if the acetone dries on the sample surface). The sample is then immersed in IPA and sonicated for 15 minutes, then rinsed in IPA and gently blow dried with nitrogen. It was observed under SEM imaging that the RIE Etching leaves behind the redeposited resist residue in the window area. This residue should be able to be removed by additional oxygen plasma cleaning step in the Reactive Ion Etching. The samples were subjected to an additional 10 minutes, 20 minutes and 30 minutes of oxygen plasma RIE step. It was observed that the samples with the 10minutes and 20 minutes still had some residue left. The 30-minute

oxygen clean recipe was able to remove all the residue present in and near the window area.

The sample Silicon dioxide thickness profile is then measured using a profilometer (KLA Tencor-P6 Profilometer). The profile height and initial silicon dioxide thickness measurement difference should be close to 80nm. Then we can proceed to the next step in the fabrication process.

3.1.4 Wet Etching and Tunneling Barrier 2

Now that there is a 80 nm margin of silicon dioxide left in the window area, the silicon window needs to be exposed. As Reactive ion etching may damage the silicon surface if the plasma hits the silicon, wet etching of silicon dioxide is done to remove the final 80nm of silicon dioxide remaining in the window region. The nominal etch remaining thickness after wet etching needs to be 60 nm. This allows for a decent contrast for the next photolithography step for alignment. The sample is immersed in freshly prepared hydrofluoric Acid and etching is done in multiple steps to avoid over-etching. After immersion in hydrofluoric acid, the sample is then taken out and immersed in DI water beaker 1 for 5 minutes with vigorous shaking followed by regular shaking. It is then transferred to a second DI water for 5 minutes with regular shaking. The sample is then rinsed under running DI water for 1 minute. This thorough DI water rinsing is done to remove all the hydrofluoric residue present on the sample surface. Once the silicon dioxide in the window region is removed and the silicon is exposed, the sample is left in the air overnight to allow for the formation of a native silicon dioxide layer (Tunneling Barrier 2).

3.1.6 Energy Filtering Stack Formation

The next step is now to deposit the energy filter stack on top of the first mask silicon window. The Energy filter stack consists of 3 layers:

Tunneling Barrier 2: Native Silicon Dioxide

Energy Filter: Quantum Well Layer

Tunneling Barrier 1: Silicon Nitride or Aluminium Oxide

The first mask window region already has the first layer of the energy filter stack: the native silicon dioxide film which was grown in section 3.2.4.

3.1.5.2 Quantum Well Layer Deposition

The middle layer in the Energy filter stack is the quantum well formation. Different materials were used for the formation of quantum well layer: Cr_2O_3 and SnO_2. We found that the tin oxide quantum well layers showed the best results. The thin tin Oxide deposition was done using AJA Sputter deposition equipment.

The tin oxide deposition rate was determined by depositing a nominal 600 seconds with the following conditions,

SnO_2 Spark step 1:

Ignition Pressure: 35 mTorr

Power: 40 W

Ar: 30 sccm

Temperature: Room Temperature

Coat Time: 2 seconds (Plasma ignition)

SnO_2 Spark step 2:

Ignition Pressure: 35 mTorr

Power: 40 W

Ar: 15 sccm; O2: 6sccm

Temperature: Room Temperature

Coat Time: 2 seconds (Plasma ignition)

2 nm SiO_2 Deposition

Power: 40 W

Deposition Pressure: 5 mTorr

Ar: 15 sccm; O_2: 6 sccm

Temperature: Room Temperature

Pre-sputter Time: 120 seconds (required for target cleaning) (Sample shutter is closed.)

Deposition Time: *** seconds

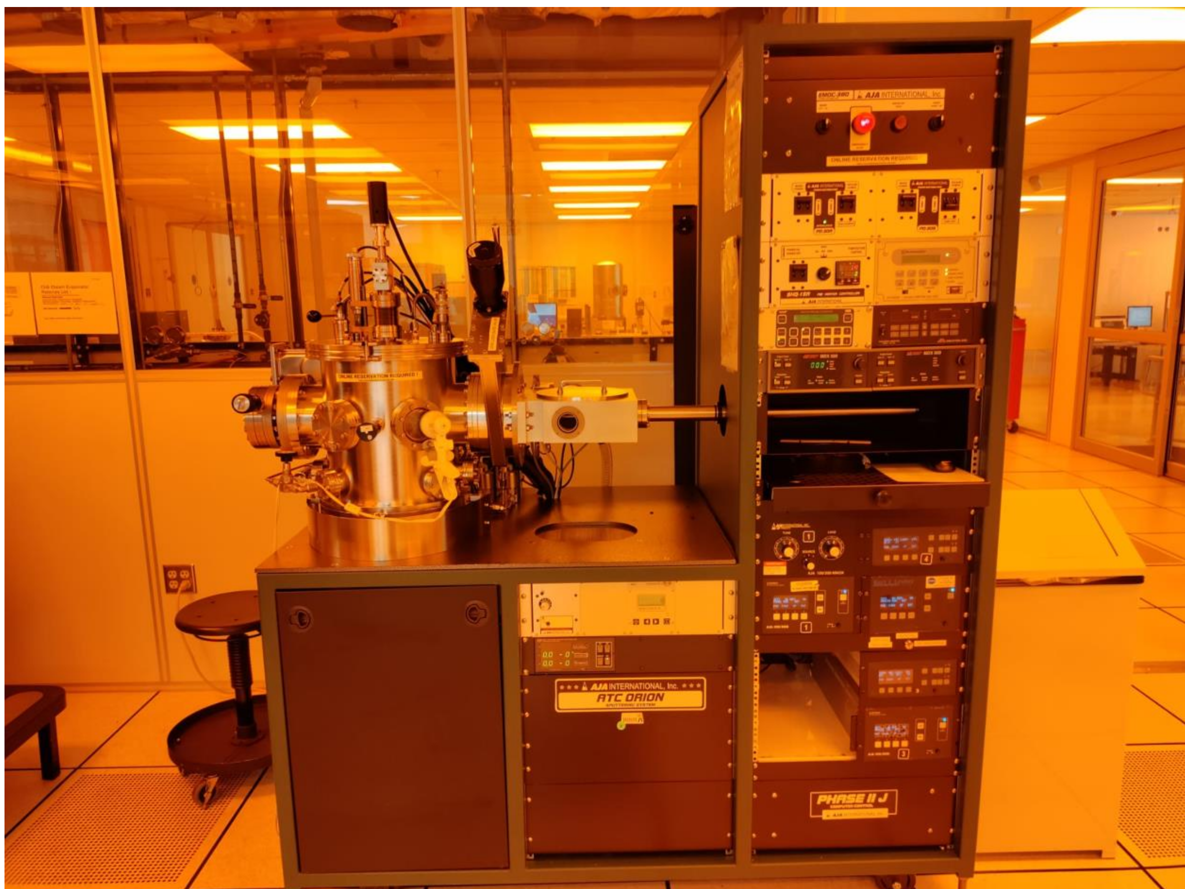


Figure 7: AJA Sputter Deposition equipment for DC and RF Sputtering

on a dummy sample and the deposited thickness was measured using Ocean Optics Reflectometer. The thickness was measured to be 8.28 nm with a 98 percent fit. Thus, the deposition rate was determined to be 0.0138 nm/s. This deposition rate was used to deposit the different tin oxide thicknesses from 1 nm, 2nm, 3nm, 4nm, 5nm, 7nm, 9nm for different samples to study the voltage variation of cold-electron transport with quantum well thickness.

3.1.5.3 Tunneling Barrier 1 deposition

After the quantum well layer deposition is done, the next step is to deposit the Tunneling Barrier layer 1. We are using silicon nitride as well as aluminium oxide as tunneling Barrier 2 material. The silicon nitride tunneling barrier was done in the AJA Sputter deposition equipment with the following parameters:

Power: 150W

Pressure: 5mT

Ar: 30sccm

The deposition time for 1 nm silicon nitride was calculated, from the deposition rate of 0.0159nm/s obtained for a dummy sample deposition, to be 62.6 seconds. For the samples with aluminium oxide tunneling barrier, the samples were shipped to Northwestern University to Tyler Gish from Dr. Hersam's group using Atomic Layer deposition equipment. The thickness deposited was 0.5 nm and 1.0 nm of aluminium oxide for different samples with similar thicknesses. The aluminium oxide thickness was varied to study the effect of tunneling barrier thickness on the shift in the cold-electron transport voltage. Once the energy filter stack is completed, we can then move to the next stage for the source and drain metal pads patterning.

3.1.5 Second Mask Lithography

Once the silicon window is covered by the Energy Filter stack we can now proceed to create a Source and Drain contact pads for the Cold electron transistors. The first step is to pattern the contact pad area using photolithography.

3.1.5.1 Photolithography for Source-Drain contact pads

The sample quadrant is spin-coated with a negative photoresist – NR9-1000PY. The photoresist is coated on the sample using a dropper to cover the entire surface and then spin-coated using the following parameters:

Step 1:

500 rpm; 100 rpm/s; 5 seconds

Step 2:

3000 rpm; 1000rpm/s; 60 seconds

Step 3:

0 rpm; 1000rpm/s; 0.1 seconds

After the spin-coating is done the sample quadrant is pre-baked on a hot plate at 150˚C for 1 minute and then allowed to cool down on a cooling plate.

The Second Mask Pattern from the Alignment mask is used for the Source-Drain contact pad patterning and is loaded on to the OAI Aligner. The substrate carrier wafer is loaded beneath the Mask inside the OAI Aligner, and the sample quadrant is fixed on the substrate carrier wafer using scotch tape at the base of the sample. The second mask pattern is aligned using the first mask alignment marks at the corners of the sample. After aligning we confirm the pattern slightly overlaps with the first mask silicon window pattern present on the sample. Once the mask is aligned with the alignment marks, the second mask is pressed

on to the sample and the pattern is exposed after contact vacuum is turned on. The photolithography pattern parameters are as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 19.6 mW/cm^2

Exposure Time: 10.2 seconds

Dose: 200 mJ/cm^2

After the exposure is done the sample quadrant is taken out and post-baked on a hot plate at 100°C for 1 minute. The sample quadrant is then placed on a cooling plate and allowed to cool

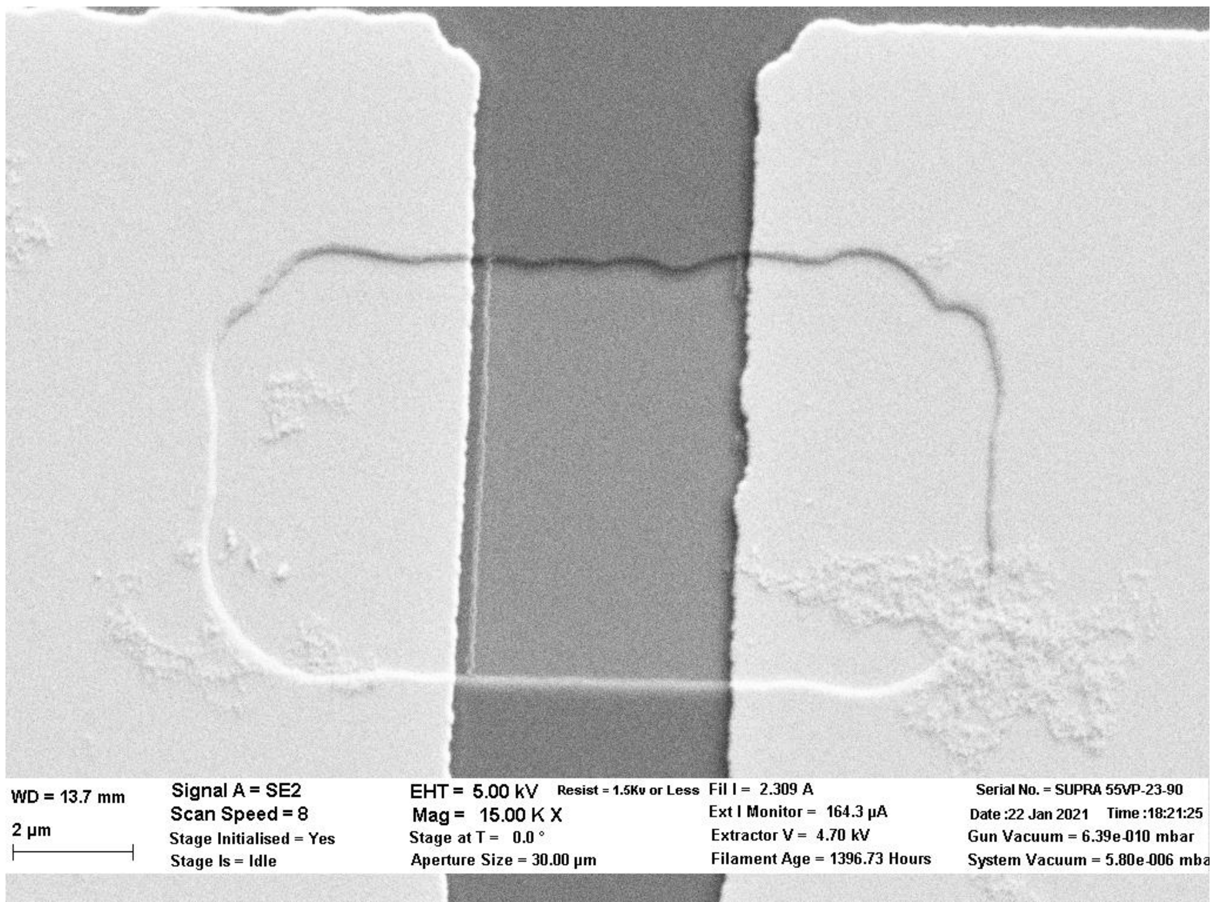
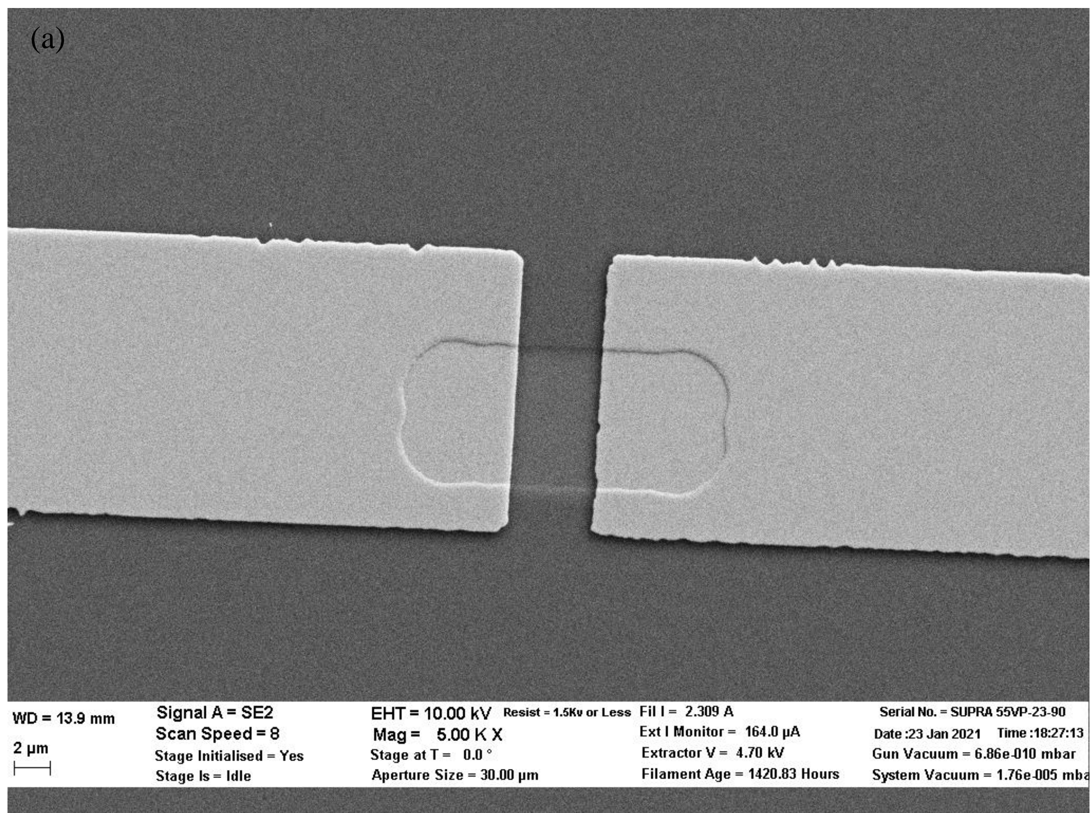


Figure 8: SEM Image showing photoresist residue after lift-off for 10 second RD6 development time

down to room temperature. After the sample quadrant cools down, the sample was developed for 10 seconds in a RD6 developer solution. However, this resulted in some resist residue remaining after metal deposition and lift-off process was done as shown in figure 6. The development process was then modified with an increased development time. The sample was instead immersed in a developer solution RD6 for 25 seconds with vigorous shaking to remove the unexposed regions of the photoresist. The sample is then immersed in DI water container for 5 minutes with regular stirring, then moved to a second DI water container for 5 minutes with regular stirring. The sample is then taken out and blow dried in nitrogen, leaving behind the second mask pattern on the photoresist coating on the sample.



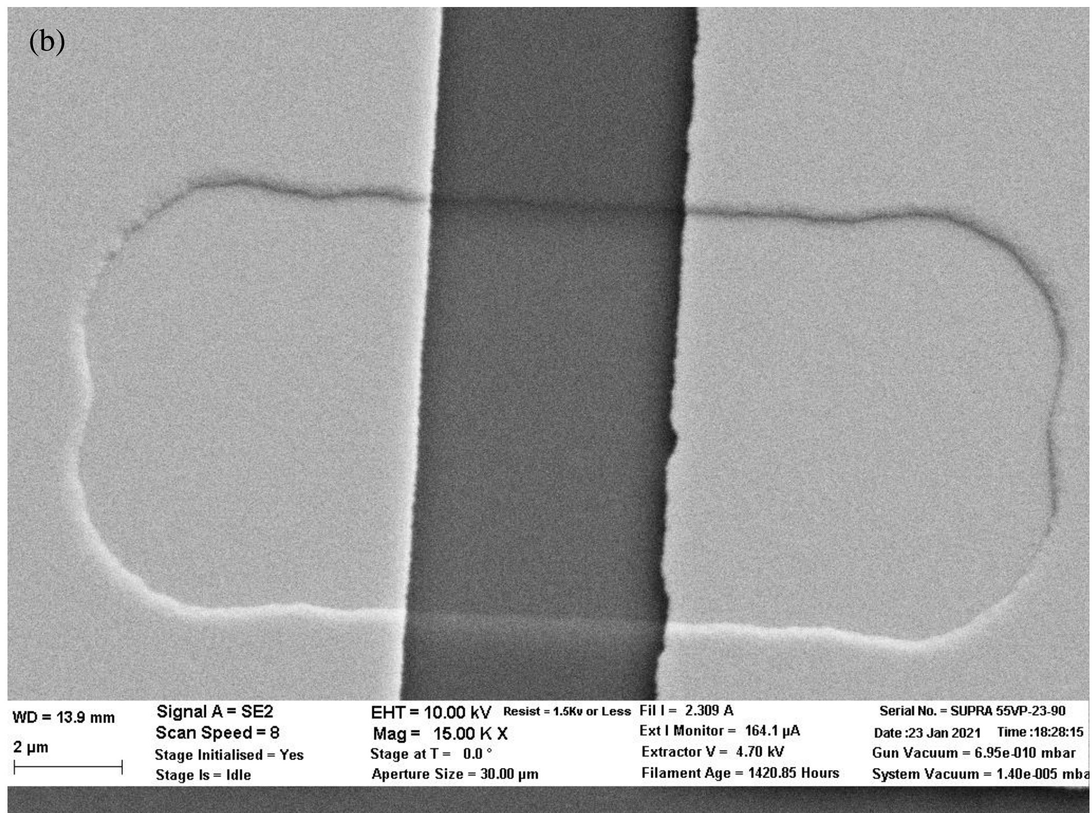


Figure 9: SEM Image showing no photoresist residue after lift-off for 25 second RD6 development time

3.1.5.6 Source-Drain Contact Metal Pad deposition

After the 2nd mask photolithography step the samples are loaded into CHA Solution or AJA E-Beam Evaporator to deposit Chromium with physical vapour deposition technique using Electron beam evaporator for Source and Drain electrode pads.

Procedure for CHA Solution:-

The Samples are loaded onto the substrate holder, and the Chamber is vented to load the samples and the crucibles. After the vent operation is completed and the chamber pressure is reached atmospheric pressure(7.5*E+2 Bar). The samples are loaded on a rotational substrate carrier in the tool. The Chromium Crucible are added to respective holders. After verifying the Thickness monitor crystal have a sufficient lifespan. The deposition chamber is closed and pump-down can be started. While the Chamber is pumping down to the

designed set point. The Deposition recipe can be added to the system which contains the deposition material, deposition rate, deposition thickness, and Substrate temperature. For Source and Drain pads we first deposit 50nm of Chromium with a 0.1nm/Sec deposition rate at room temperature. Once the deposition is completed for chromium.

Once the metals are deposited on the sample the chamber is again vented at atmospheric pressure in order to unload the Samples and the Crucible. After removing the samples from Chamber the chamber is again pumped down to the designed set point to avoid any contaminants inside the deposition chamber.

For AJA-E-Beam Evaporator:-

The Samples are loaded on the Sample Holder and the loading dock for the AJA-E Beam evaporator is vented with nitrogen. Once the loading dock has reached the atmospheric pressure we can load the samples on the Substrate delivery shaft with samples facing down. The Loading chamber is closed and is pumped down until the pressure inside the loading dock is not below 2.0E-5 torr. Once the pressure is below the set point the Deposition chamber gate can be opened and with the help of the Substrate delivery shaft the samples are loaded into the deposition chamber. The sample holder is attached to the rotational shaft which can control the distance from the source material and rotational speed. Once the sample holder is securely mounted the Substrate delivery shaft is retracted and the deposition chamber is closed. The rotations and the height of the sample holder are adjusted to the designed position and the rotational speed is adjusted according to the need. After Selecting the desired material crucible with the help of a material selector switch. We verify the Material Density and acoustic impedance is properly configured in the thickness monitoring system. Once the system is properly configured, we start the E-Beam gun and gradually increase the current to heat the material till we reach the desired deposition rate.

After reaching the stable deposition rate the substrate shutter can be opened and with the help of a thickness monitor the thickness of deposited material can be monitored. In our case, as the metal to deposit is Chromium it is deposited at 0.1nm/Sec rate with 60RPM Rotational speed at room temperature with a thickness of 50nm. Once we have deposited the desired thickness the Substrate shutter is engaged to prevent additional deposition on the sample.

Once the material deposition is completed the gun current is slowly reduced to minimal and the gun is powered off, and the sample rotations are turned off after verifying the loading dock pressure is still within the parameters, The loading docks door is opened and with the help of Substrate delivery shaft, the sample holder is moved back to the loading dock. And the Deposition chambers door is closed, and the Loading dock is vented to remove the samples from the equipment. The loading dock is kept in a Vacuum to avoid any contaminates going in the Loading dock.

3.1.5.6 Passivation layer deposition

After the Metals are deposited on the Samples to prevent any damage to the Source and Drain pads from the further process the passivation later of Silicon Dioxide was deposited on top of the metals using AJA Sputter deposition.

The samples were loaded into the AJA Sputter deposition tool using a load lock chamber. The samples are fixed onto a sample holder and inserted into the load lock chamber. The chamber is then pumped down to 2*E-5 torr pressure. Once the pressure is reached, the main chamber gate is opened, and the sample holder is slowly inserted into the main chamber for deposition. In the main chamber, the sample holder is lifted using hooks to loading height and the sample holder arm is retracted from the chamber. The main chamber door is then closed. The sample holder is then lowered to deposition height and sample rotation is turned on. The AJA sputter deposition is done using the following parameters:

SiO_2 Spark step:

Ignition Pressure: 35 mTorr

Power: 64 W

Ar: 30 sccm; O_2: 6 sccm

Temperature: Room Temperature

Coat Time: 3 seconds (Plasma ignition)

2 nm SiO_2 Deposition

Power: 148 W

Deposition Pressure: 5 mTorr

Ar: 30 sccm; O_2: 6 sccm

Temperature: Room Temperature

Pre-sputter Time: 120 seconds (required for target cleaning) (Sample shutter is closed.)

Deposition Time: 313.3 seconds

AJA Sputter deposition of SiO2 as a passivation layer resulted in a side layer deposition due the conformal nature of sputter deposition. This unwanted layer formation needed to be removed in order to lower complications during gate oxide deposition and sidewall formation. In order to prevent the side layer formation during the passivation step, the SiO2 deposition was switched to be done using CHA E-beam Evaporator.

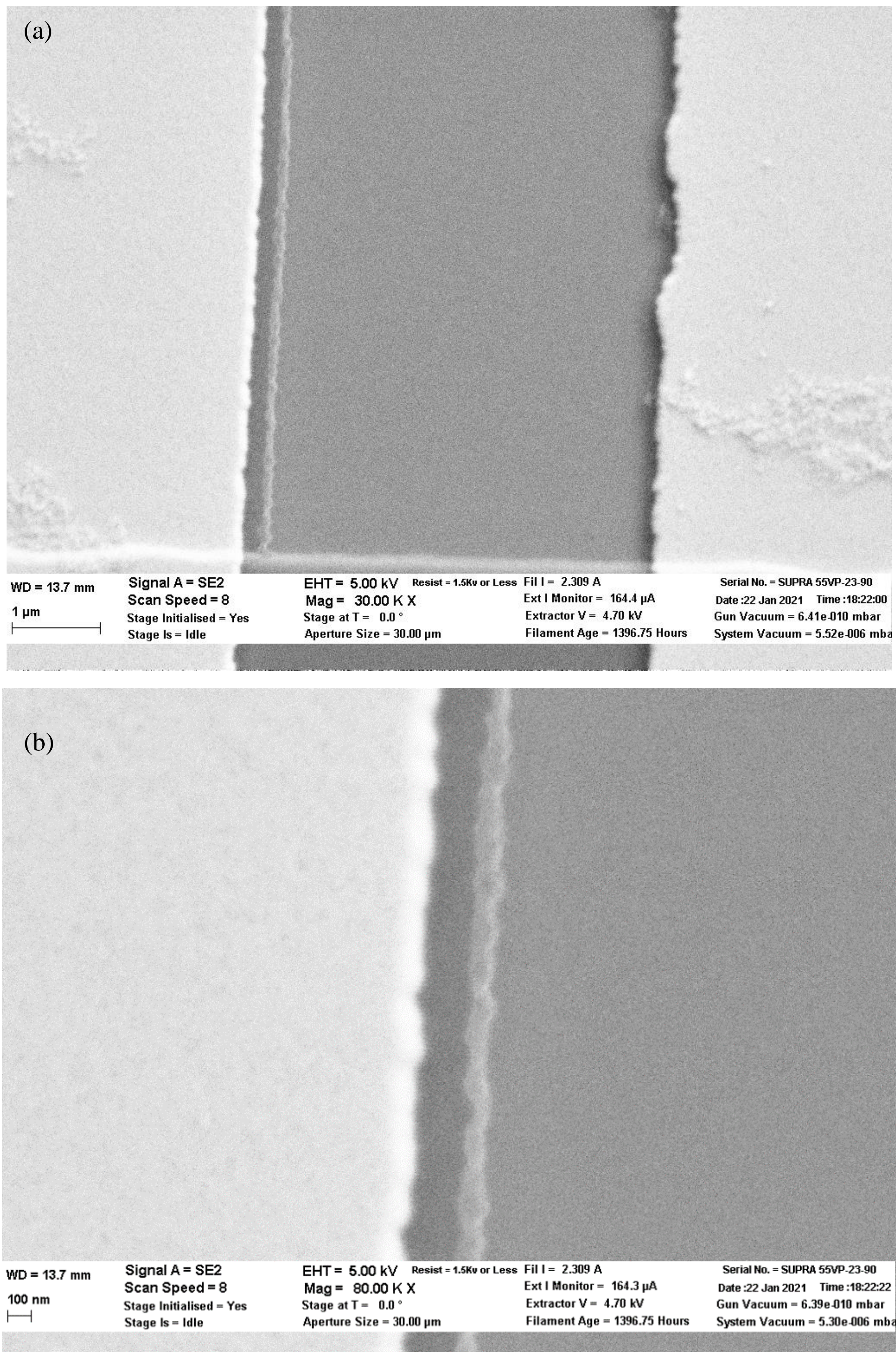
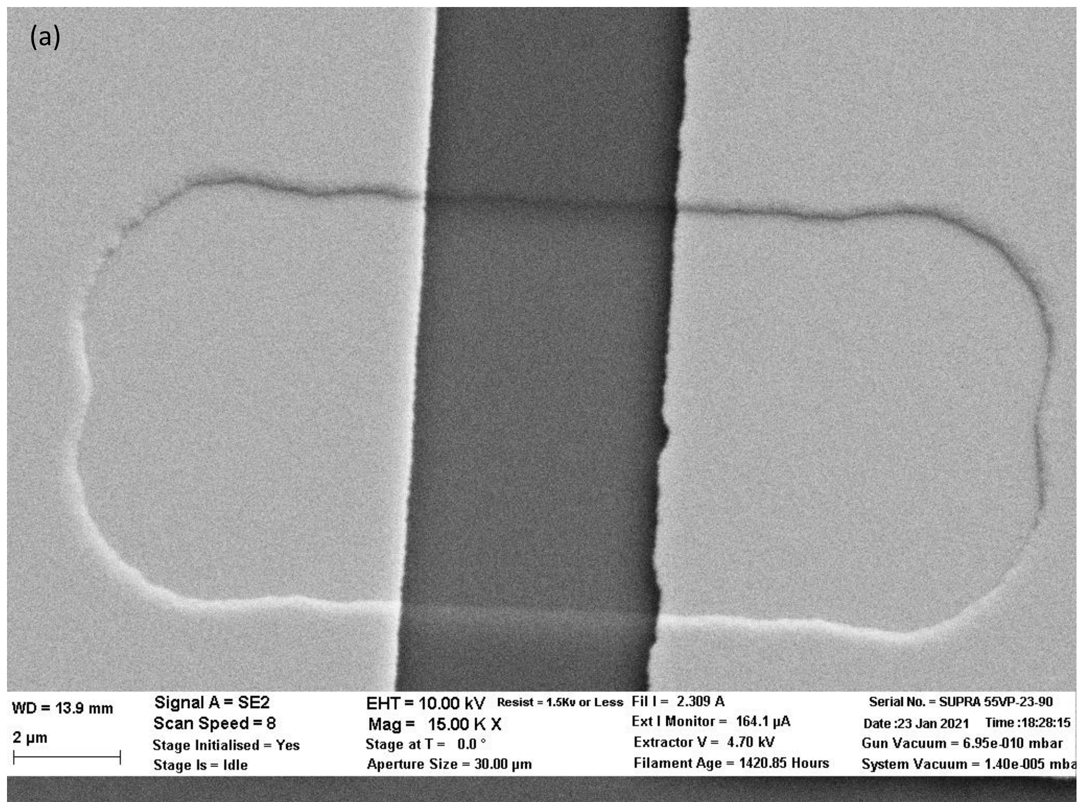


Figure 10: SEM Image showing passivation layer SiO2 deposited using AJA Sputter deposition. Side layer formation due to conformal deposition of SiO2 using sputter deposition

To deposit the silicon dioxide on the sample the samples are loaded on the CHA Solutions Sample Holder with the help of Clips and screws. After ensuring the cryo pump is below 10K temperature the CHA E-beam evaporator's deposition chamber is vented to the atmospheric pressure. Once the chamber has reached atmospheric pressure the chamber is lifted up in order to load the sample and source material. The sample Holder is now loaded in the equipment with samples facing down. And the Silicon Dioxide granules filled with crucible are loaded into the deposition chamber. After verifying the Thickness monitor piezoelectric crystal have a sufficient lifespan the chamber is lowered, and rough pumping is started. Once the Pressure is reached below 10mTorr the High vacuum cryo pump can be engaged. On the Thickness monitor system, the Z-ratio and density of the material can be set to get accurate measurements. Once the Pressure is reached below 5E-6 Torr is reached we can start the E beam gun and start Current in the e-Beam is gradually increased till we get a desired deposition rate for the material, Once the stable deposition rate is reached the Substrate shutter is moved to start the deposition and with the help of Thickness monitor system the thickness of deposited material is observed. After desired thickness is reached the Substrate shutter is engaged to prevent further deposition from happening on samples. In our case, we deposit the Silicon Dioxide at 0.15nm/Sec deposition rate at Room temperature for 100nm. After the deposition is completed the E-beam current is slowly reduced and after reaching minimal current the E-Beam gun is powered off. The High vacuum pumps vents are closed to prevent damages to the pump. Once the Vents are closed the Deposition chambered is vented to atmospheric pressure to remove the sample and Source material. The Deposition chamber is kept at the Vacuum to avoid contaminants going into the chamber. The SEM image showed no side layer formation after using e-beam evaporation for the 50nm SiO_2 passivation layer deposition.



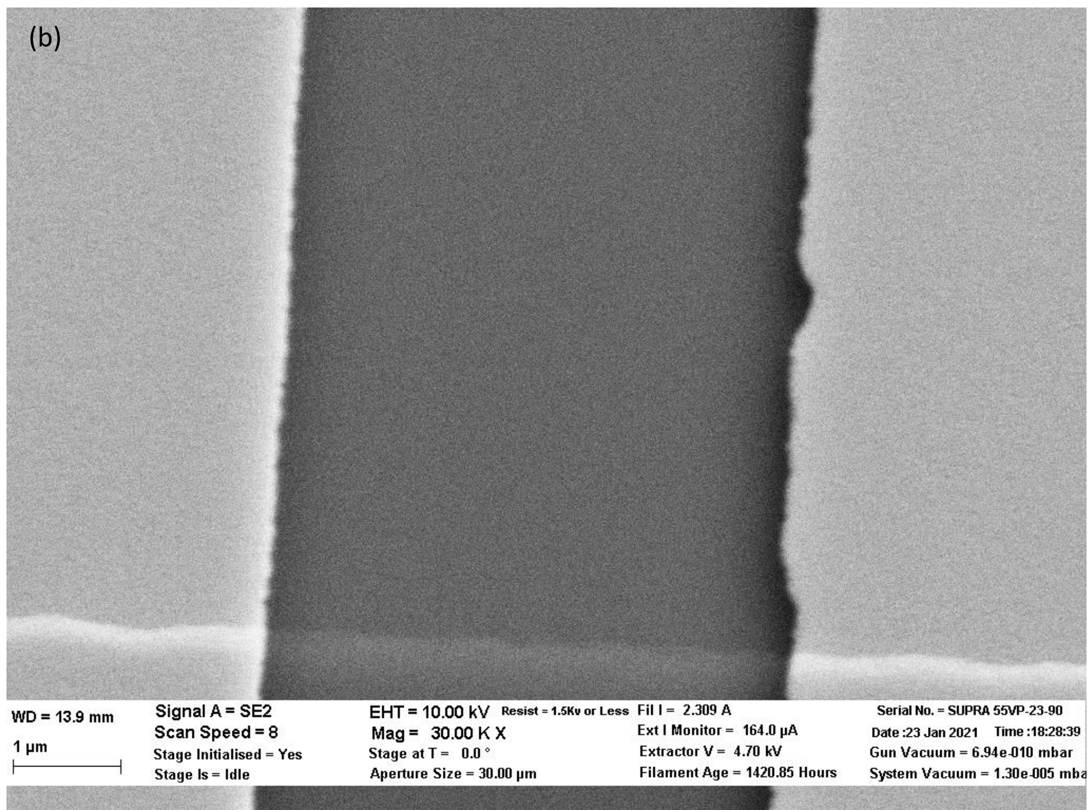


Figure 11: SEM Images showing no side layer formation after SiO2 passivation layer deposition using CHA ebeam evaporation

3.1.5.3 Lift-off

After the passivation layer is deposited the sample quadrant is unloaded from the CHA E-Beam Evaporator equipment. The photoresist needs to be removed using a lift-off process. The sample quadrant is immersed in Acetone and sonicated for 5 minutes followed by a 30 second IPA rinse. The sample is then immersed in IPA and sonicated for 5 minutes, again followed by an IPA rinse for 30 seconds. It is then blow dried in Nitrogen. The Sonication steps are listed below:

Step 1: Acetone Sonication (5 minutes) + IPA Rinse (30 seconds)

Step 2: IPA Sonication + IPA Rinse (30 seconds)

Step 3: Nitrogen Blow dry

3.1.5 Gate Dielectric Deposition

At this stage after the lift-off is done, the sample consists of a source and drain electrode in contact with the silicon channel through the energy filter stack (1nm Sputtered Si3N4 or 0.5nm Al2O3 as tunneling barrier 1 / QW: 3nm or 4nm or 5nm sputtered SnO_2 / Native SiO_2 (1.5nm) as tunneling barrier 2 / Si). The source-drain electrodes have varying separation between them to act as varying gate lengths in the second photomask pattern. The silicon channel in the window area between the source and drain electrodes is now exposed and needs to be covered with a gate dielectric material in order to pattern the gate electrode on top. Initially, we used a thin 10nm film of silicon dioxide as the gate dielectric, to separate the gate electrode and the silicon channel. The gate dielectric material needs to be of high quality. This is important because a good quality dielectric is needed to reduce gate leakage current as much as possible. The dielectric material deposited using a Plasma Enhanced Chemical Vapor deposition (PECVD) has better film quality compared to sputter deposited and e-beam evaporated silicon dioxide or silicon nitride material. Thus, for the

gate dielectric deposition we use the TRION ORION II PECVD/LPCVD System. As the equipment is processed by multiple groups in the cleanroom and used for a variety of different recipes, we need to run a PECVD cleaning recipe prior to utilization.

For loading the sample into the equipment, we first vent the load lock with nitrogen to avoid any corrosive and hazardous gasses that can enter the cleanroom. Then we load our wafer inside the load lock and start to pump down the chamber. While the system is pumping down we can load our recipe and change any required parameters. Once a set pressure is reached the reactor door is opened and with the help of a robotic arm, the wafer is moved into the deposition chamber and placed on the electrodes. And the arm is again moved back into the load lock. And the main deposition chamber is also pump-down to set pressure and the temperature is set according to the recipe needs. Once all the parameters are within the limit the recipe is started.

A standard PECVD cleaning recipe is used prior to use. The cleaning recipe process time is 10 minutes. This will ensure that all gases and residue remaining in the main PECVD chamber are cleaned and removed.

After the clean recipe is done, the deposition chamber is opened and with the help of a robotic arm the wafer is moved back to the load lock and the deposition chamber gate is closed. After the gate is closed the load lock is vented with nitrogen to remove any gasses and to increase the pressure inside the load lock to atmospheric pressure to remove the wafer. After removing the wafer that we used to clean the chamber we need to load a dummy wafer for the chamber conditioning recipe. Once the chamber is cleaned, we need to run a conditioning recipe on a dummy wafer for a long duration to stabilise the chamber conditions with the gases used during the main process. We use different dummy wafers for different materials to avoid any contamination in the chamber. The Conditioning recipe

for the SiO2 is a multi-step process. The PECVD chamber is maintained at 380°C. The process conditions for the conditioning recipe are as follows:

PECVD Conditioning Recipe

Recipe: KOH_SiO2 @380C @ 400W ICP power

Step 1

600 mT, N2: 250sccm,380C, 1200s

Step 2

600 mT, N2: 250sccm; N2O: 179sccm; SiH4/Ar: 5sccm, 380 C, 600s

Step 3

600 mT, N2: 250sccm; N2O: 179sccm; SiH4/Ar: 5sccm, 380 C, 400 W ICP RF, 660s

Step 4

250 mT, N2: 250sccm, 380 C, 180s

After the conditioning process is completed, the dummy wafer is unloaded from the chamber. The next step is to calculate the deposition rate for the PECVD silicon dioxide. As the required thickness of the deposited material is extremely thin ~10nm, the deposition rate needs to be calculated precisely. The deposition rate is established using dummy samples. These dummy samples were prepared by etching them with HF (10:1) for 5 minutes in order to remove any native silicon dioxide present on the dummy samples. These bare silicon dummy samples can now be used to determine the deposition rate for the plasma enhanced chemical vapor deposition silicon dioxide. All the dummy samples were approximately the same size to remove any parameter variation. Different thickness of silicon dioxide is deposited using on different dummy samples using different deposition times with the plasma enhanced chemical vapor deposition. The deposition parameters were as follows:

For SiO2 Deposition

Recipe: KOH_SiO2 @380C @ 400W ICP power

Step 1

600 mT, N2: 250sccm,380C, 1200s

Step 2

600 mT, N2: 250sccm; N2O: 179sccm; SiH4/Ar: 5sccm, 380 C, 600s

Step 3

600 mT, N2: 250sccm; N2O: 179sccm; SiH4/Ar: 5sccm, 380 C, 400 W ICP RF,

Deposition time = *** seconds

Step 4

250 mT, N2: 250sccm, 380 C, 180s

The samples were unloaded after deposition and the deposited thickness was measured using Ellipsometer and reflectometer. The refractive index used for the thickness measurements was 1.4571. The deposition thickness and deposition times were compiled in an excel sheet and the deposition rate was determined. Below is the deposition thickness data measured using ellipsometer, arranged in a table:

Ellipsometer PECVD Growth Rate										
Time (in seconds)	0	200	227	264	285	400	530	530	530	600
Thickness	0	25.992	42.3	47.6	63.832	64.975	90.826	88.558	91.612	113.291

Table: Deposition times and corresponding deposited SiO_2 thickness measured using Ellipsometer

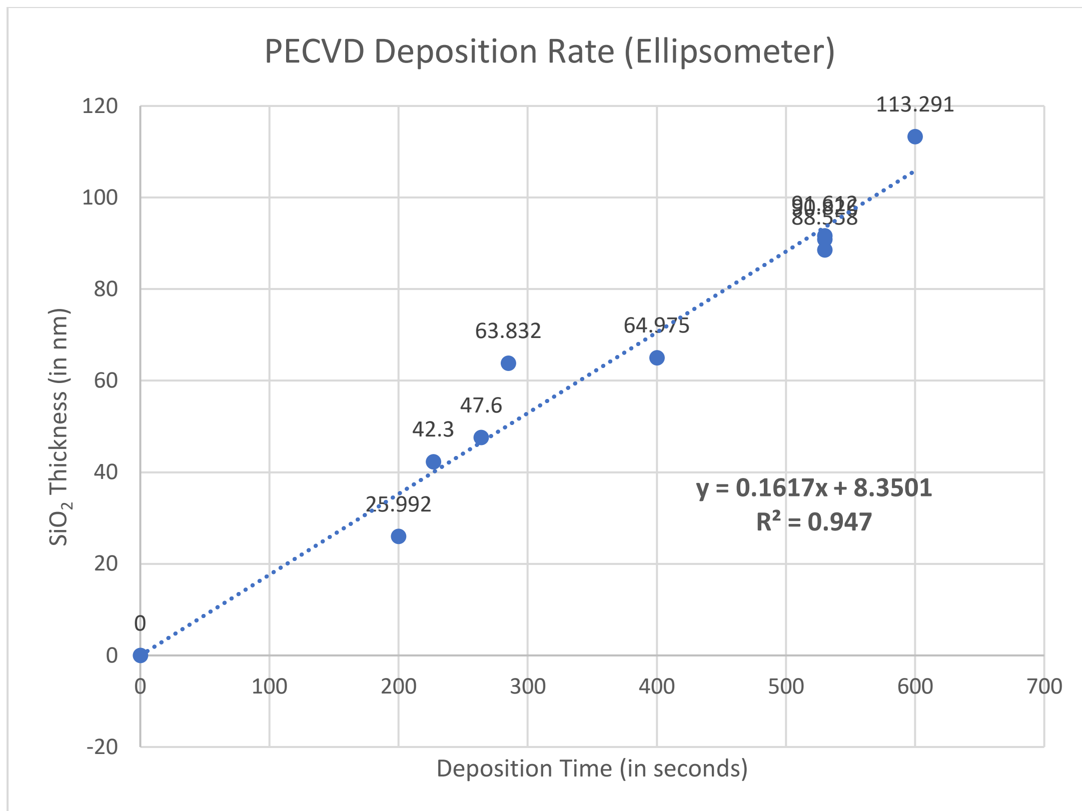


Figure 12: SiO2 Thickness deposited vs Deposition time (in seconds) measured using Ellipsometer showing deposition rate of 0.1617 nm/s

The deposition thickness data measured using reflectometer is given below:

	Reflectometer PECVD Growth Rate									
Time (in seconds)	0	200	227	264	285	400	530	530	530	600
Thickness	0	30.1	44.9	50.2	63.3	71.2	90.9	88.6	94.1	115

Table: Deposition times and corresponding deposited SiO_2 thickness measured using Reflectometer

The Ellipsometer and reflectometer measurements resulted in the same stable deposition rate of 0.16nm/s. We then use this deposition rate for our main samples to deposit a thin ~10nm Silicon dioxide using PECVD. However, prior to starting with the main sample, we run an additional deposition recipe for the ~10nm thickness using the calculated deposition rate. The thickness of the silicon dioxide on the dummy sample is measured and if the

actual deposited thickness is accurate, we then proceed with the actual deposition for the main samples.

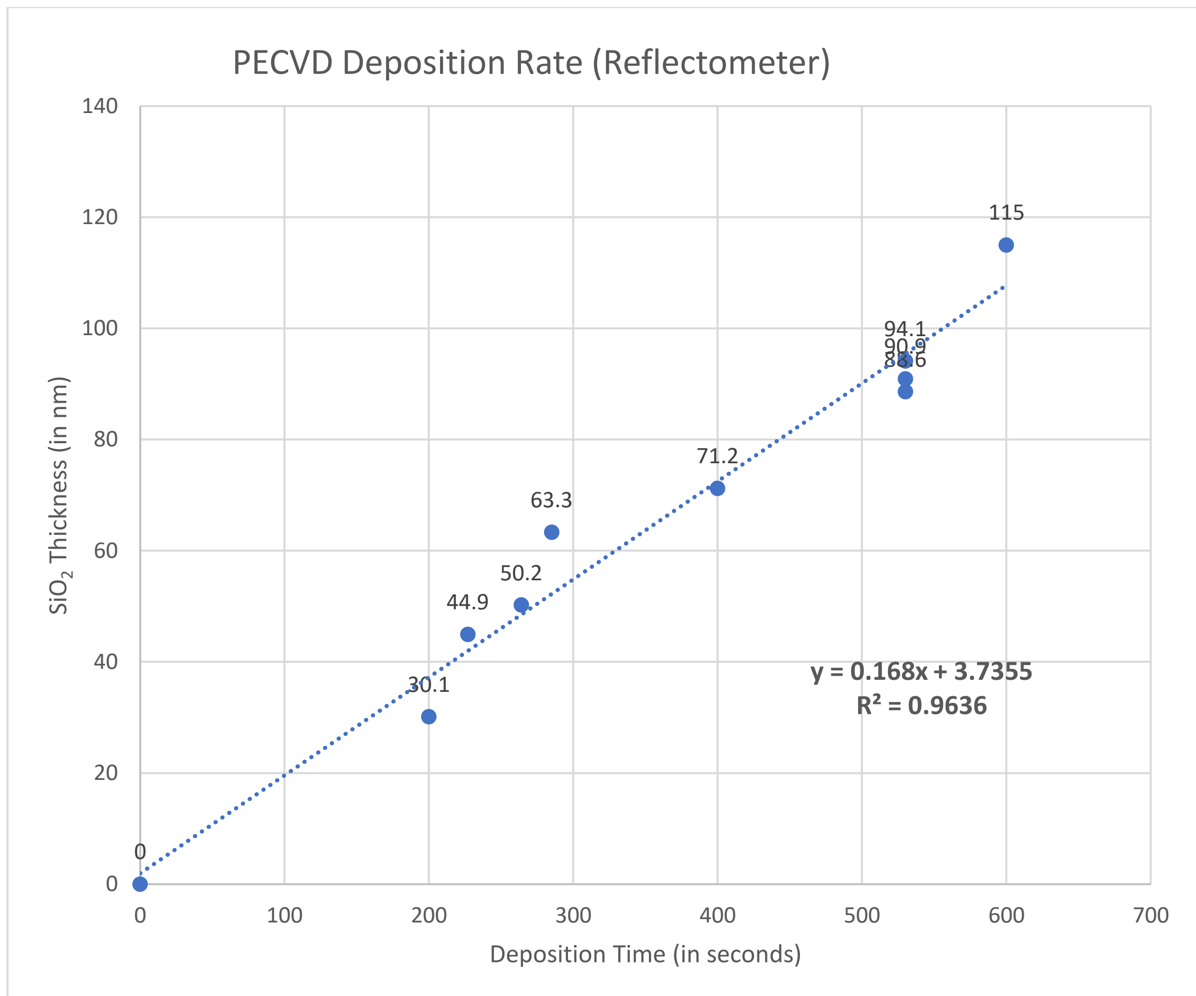


Figure 13: SiO2 Thickness deposited (in nm) vs Deposition time (in seconds) measured using Reflectometer showing deposition rate of 0.168 nm/s

The main samples are placed onto the 4-inch carrier wafer and loaded into the PECVD chamber which is maintained at 380°C. Th deposition parameters are as follows:

For SiO2 Deposition

Recipe: KOH_SiO2 @380C @ 400W ICP power

Step 1

600 mT, N2: 250sccm,380C, 1200s

Step 2

600 mT, N2: 250sccm; N2O: 179sccm; SiH4/Ar: 5sccm, 380 C, 600s

Step 3

600 mT, N2: 250sccm; N2O: 179sccm; SiH4/Ar: 5sccm, 380 C, 400 W ICP RF,

Deposition time = ~59.5 seconds

Step 4

250 mT, N2: 250sccm, 380 C, 180s

After the deposition is done the samples are unloaded from the PECVD chamber. However, we had an issue with gate leakage current with the ~10nm gate dielectric of silicon dioxide. A large percentage of devices showed gate leakage current which destroyed most of the fabricated devices. Therefore, we modified the gate dielectric deposition process to create a PECVD silicon dioxide sidewall[128, 129] formation. This formed thicker sidewalls along the source and drain metal contact that helped with the blocking of the gate leakage current through them.

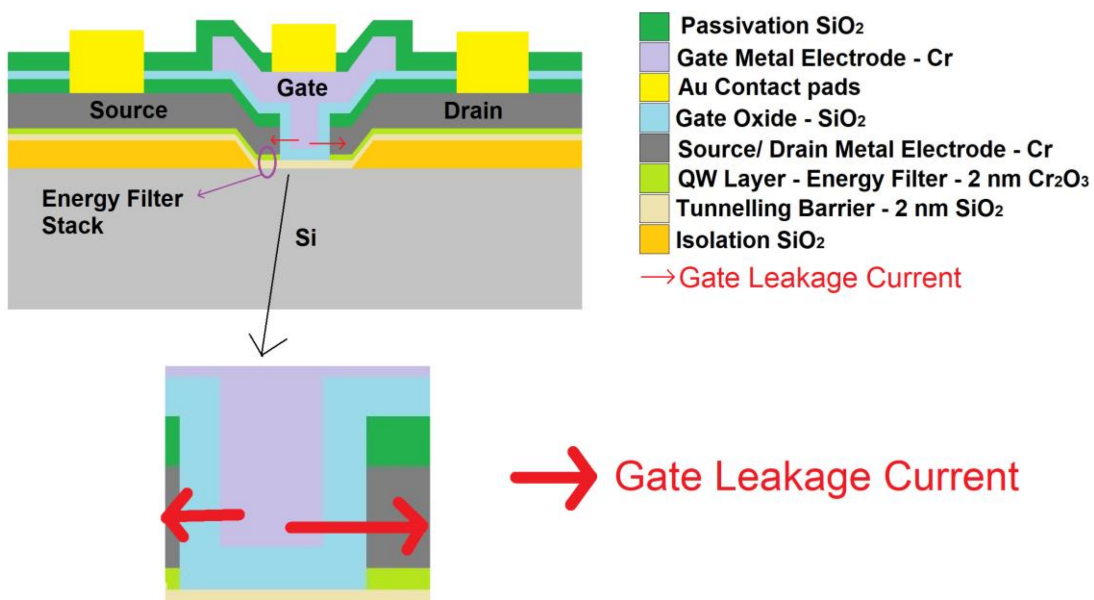


Figure 14: Schematic of device with gate leakage current path

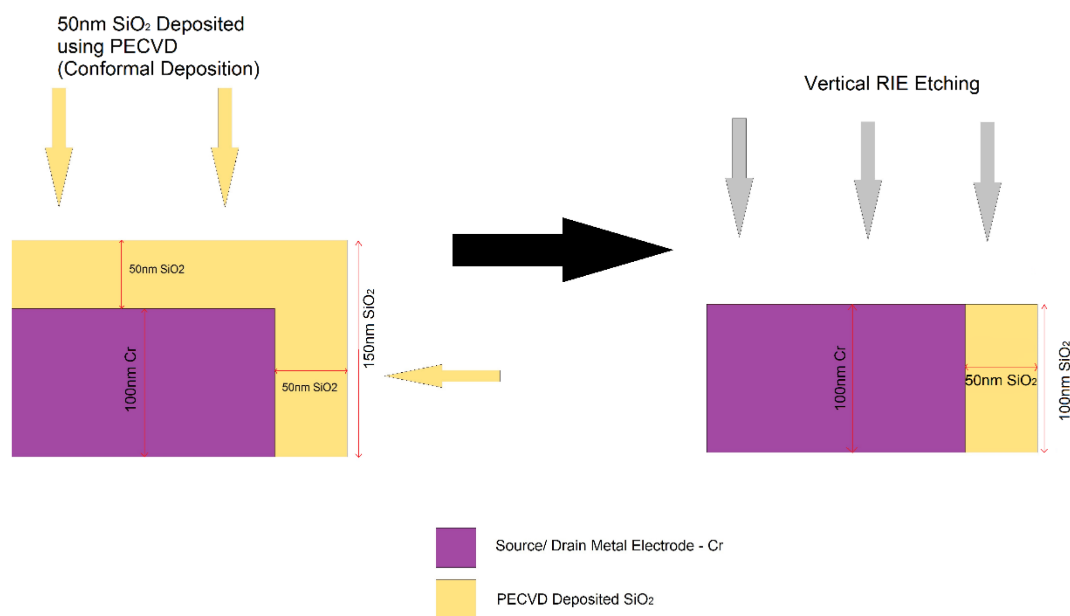


Figure 15: Schematic diagram showing sidewall formation process

For the sidewall formation process, a nominal sidewall thickness of 50nm of silicon dioxide was decided on to have a safe margin of thickness to prevent gate leakage current. The PECVD chamber needs to be cleaned prior to using it for deposition. The PECVD chamber is maintained at 380°C. The load lock chamber is first vented with nitrogen. After the load lock door is opened, the PECVD cleaning wafer is loaded into the chamber and the loading process is started. The loading process is automated. The loading arm inserts the cleaning wafer into the main PECVD chamber.

The PECVD Cleaning wafer is unloaded from the chamber once the cleaning recipe is completed. After the cleaning step is done, it is followed by the PECVD conditioning recipe. For the conditioning recipe a dummy wafer is used. The dummy wafer is loaded into the load lock chamber. It is then inserted into the main chamber by the automated process. The conditioning recipe is loaded, and the conditioning process is started. The process parameters for the PECVD conditioning step are as follows:

PECVD Conditioning Recipe

Recipe: KOH_SiO2 @380C @ 400W ICP power

Step 1

600 mT, N_2: 250sccm,380C, 1200s

Step 2

600 mT, N_2: 250sccm; N_2O: 179sccm; SiH_4/Ar: 5sccm, 380 C, 600s

Step 3

600 mT, N_2: 250sccm; N_2O: 179sccm; SiH_4/Ar: 5sccm, 380 C, 400 W ICP RF, 600s

Step 4

250 mT, N_2: 250sccm, 380 C, 180s

After the PECVD chamber conditioning is done, the deposition rate is calculated using the process mentioned earlier in this section. The deposition rate was calculated to be 0.0168nm/s. A dummy sample was used to test the deposition rate to deposit a nominal 50nm of silicon dioxide. The deposited thickness is measured using ellipsometer and reflectometer. If the deposited thickness is close to the deposition rate, we then proceed to deposition on the main samples. For the PECVD Sidewall formation process, we deposit a nominal 50nm of silicon dioxide, followed by reactive ion etching to etch back 45nm leaving behind 5nm of silicon dioxide as a gate dielectric material in the window area. The PECVD deposition is a conformal deposition which causes the 50nm silicon dioxide to be deposited on all surfaces. The reactive ion etching is anisotropic which is used to etch the silicon dioxide to be etched in a vertical direction which leaves behind 5nm silicon dioxide in the window area and on top of the source-drain electrodes. But the side surface of the source-drain electrodes will still have a lateral thickness of 50nm remaining behind which will provide sufficient insulation against gate leakage current.

The main samples are placed onto a 4-inch carrier wafer and loaded into the load lock chamber. The chamber is evacuated, and the loading process is started. The loading process is automatic and the samples along with the carrier wafer is inserted into the main PECVD deposition chamber. The chamber is maintained at 380°C for deposition. The deposition parameters are as follows:

For SiO2 Deposition

Recipe: KOH_SiO2 @380C @ 400W ICP power

Step 1

600 mT, N2: 250sccm,380C, 1200s

Step 2

600 mT, N2: 250sccm; N2O: 179sccm; SiH4/Ar: 5sccm, 380 C, 600s

Step 3

600 mT, N2: 250sccm; N2O: 179sccm; SiH4/Ar: 5sccm, 380 C, 400 W ICP RF,

Deposition time = ~297.6 seconds

Step 4

250 mT, N2: 250sccm, 380 C, 180s

After the deposition is done the samples are unloaded from the PECVD chamber and the deposited thickness is measured using ellipsometer and reflectometer. The refractive index used for silicon dioxide measurement is 1.4571. The next step is to etch back the silicon dioxide with a 5nm margin and the sidewall. The nominal RIE etch thickness is ~45nm. The reactive ion etch process need to be extremely precise because the 5nm margin is very small and there is a very little margin of error. If the samples are even slightly overetched, the silicon dioxide from the sidewalls will also be etched and expose the source-drain metal regions. This will defeat the entire purpose of the sidewall formation. For this reason, the silicon dioxide etch rate needs to be determined prior to etching the silicon dioxide. The

dummy samples deposited with the PECVD silicon dioxide prior to this step are used in the RIE etch rate determination. Several dummy samples with the same initial silicon dioxide thickness were etched with different etch times and the remaining silicon dioxide thickness is measured using the ellipsometer and reflectometer and is compiled into an excel file and the etch rate is determined. The etch rate determination data and plot for measurement using ellipsometer is shown below:

Ellipsometer				
Etch Time	20	30	40	50
Etched thickness	27.63	47.594	59.068	67.89

Table: Etch times and corresponding etched SiO_2 thickness measured using Ellipsometer

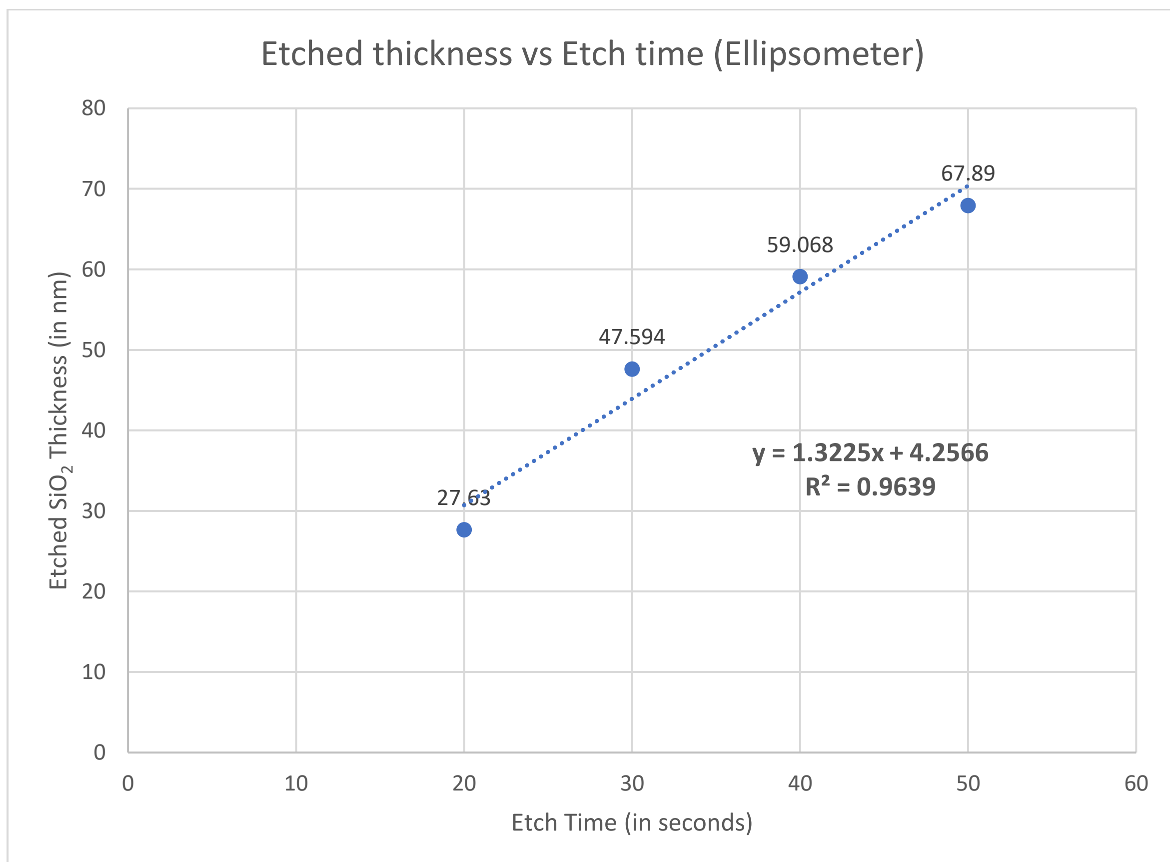


Figure 16: Etched SiO_2 thickness (in nm) vs Etch time (in seconds) measured using Ellipsometer

The etch rate determination data and plot measured using reflectometer is shown below:

Reflectometer				
Etch Time	20	30	40	50
Etched thickness	19.3	36.7	44.4	54.7

Table: Etch times and corresponding etched SiO_2 thickness measured using Reflectometer

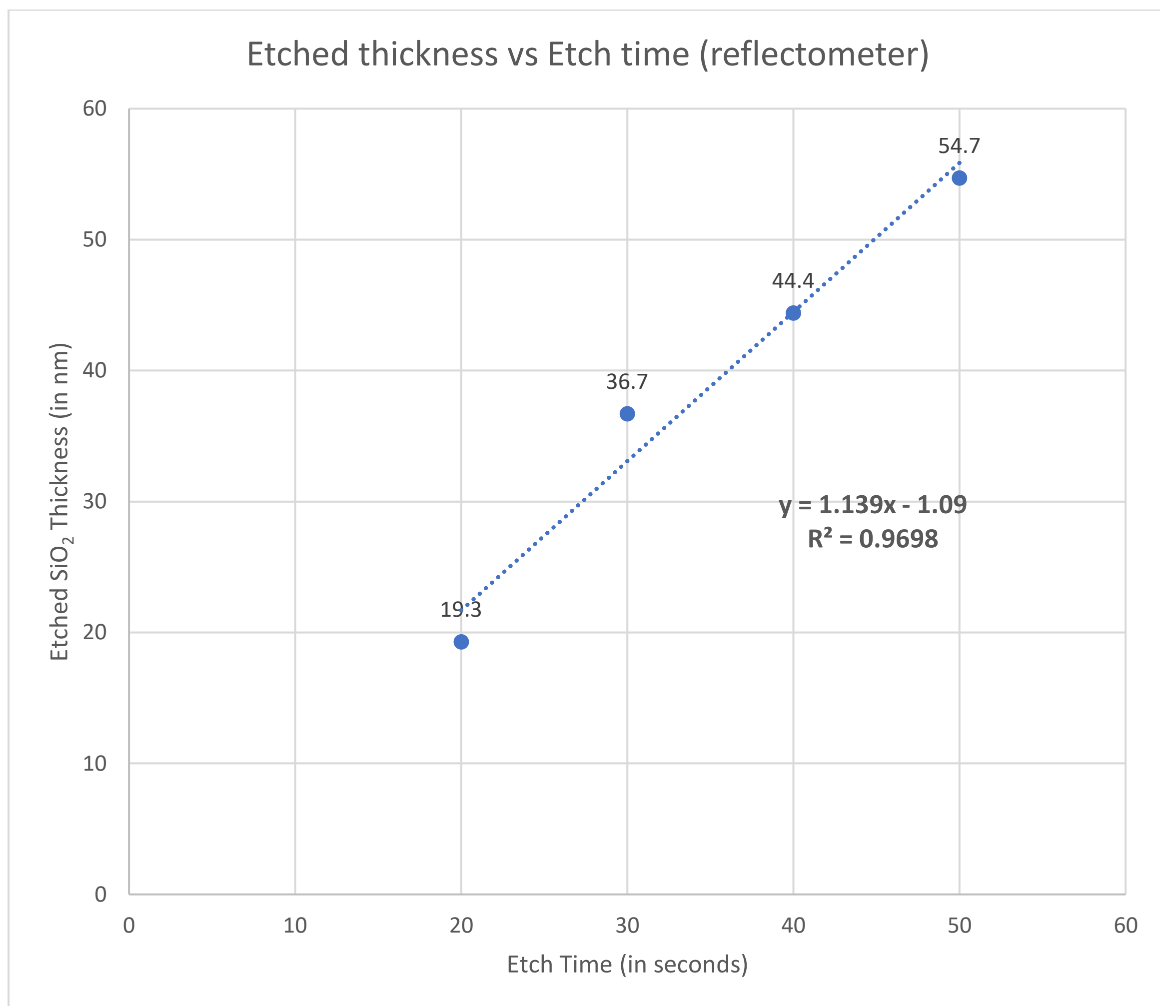
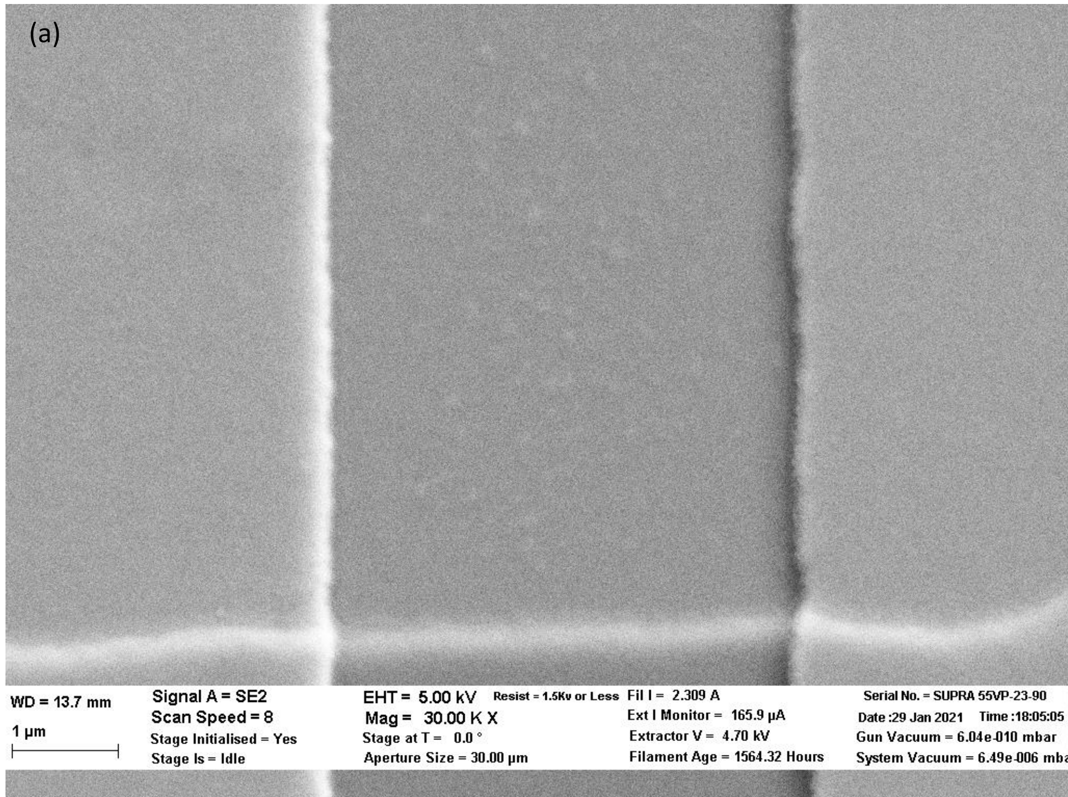
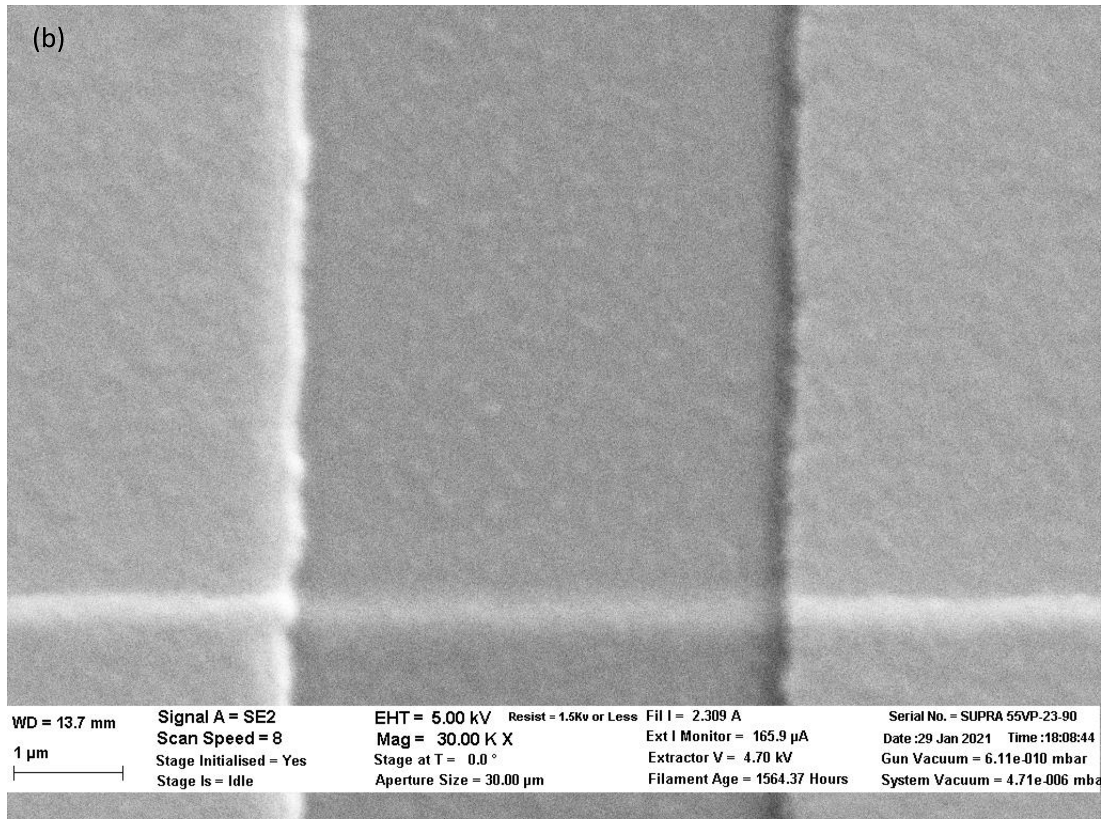


Figure 17: Etched SiO_2 thickness (in nm) vs Etch time (in seconds) measured using Reflectometer

The measured etched thicknesses from the ellipsometer and the reflectometer have slight variation from each other. The differing etched thickness gave rise to differing etch rate

determined from ellipsometer and reflectometer. The etch rate determined from the ellipsometer measurements was calculated to be 1.32 nm/s. Whereas the calculated etch rate from reflectometer measurements was 1.14 nm/s. This variation in etch rate due to different thickness readings may be due to a variety of different possible reasons. The measurement spot size for the ellipsometer and reflectometer are different, the location of measurement may vary for each sample and thus result in differing thickness readings. Additionally, the ellipsometer measurements are done after coupling to the nearest maxima or minima. If there are several maxima or minima lumped together, the final reading could just as easily couple to any of those measurements and thereby result in slightly different thickness measurements. Therefore, we use the higher etch rate between the ellipsometer and reflectometer to etch half of the remaining etch thickness. The remaining thickness is measured and the etch rate is calculated again. And the higher etch rate is used again to etch the remaining required etch thickness. This allows us a better margin and protects the sample from being over etched. The etch rate also varies slightly with the size of the sample due to different consumption of the reactive gases. Thus, it is important to etch only half of the required thickness first to avoid from over etching during the etching of the second half of the required etch thickness. Once the sidewall formation is done, the samples can then proceed to the next step for gate electrode patterning. The sidewall formation was able to resolve the gate leakage current issue.


(a)
WD = 13.7 mm
1 µm
Signal A = SE2
Scan Speed = 8
Stage Initialised = Yes
Stage Is = Idle
EHT = 5.00 kV
Resist = 1.5Kv or Less
Mag = 30.00 K X
Stage at T = 0.0 °
Aperture Size = 30.00 µm
Fil I = 2.309 A
Ext I Monitor = 165.9 µA
Extractor V = 4.70 kV
Filament Age = 1564.32 Hours
Serial No. = SUPRA 55VP-23-90
Date :29 Jan 2021 Time :18:05:05
Gun Vacuum = 6.04e-010 mbar
System Vacuum = 6.49e-006 mba


(b)
WD = 13.7 mm
1 µm
Signal A = SE2
Scan Speed = 8
Stage Initialised = Yes
Stage Is = Idle
EHT = 5.00 kV
Resist = 1.5Kv or Less
Mag = 30.00 K X
Stage at T = 0.0 °
Aperture Size = 30.00 µm
Fil I = 2.309 A
Ext I Monitor = 165.9 µA
Extractor V = 4.70 kV
Filament Age = 1564.37 Hours
Serial No. = SUPRA 55VP-23-90
Date :29 Jan 2021 Time :18:08:44
Gun Vacuum = 6.11e-010 mbar
System Vacuum = 4.71e-006 mba

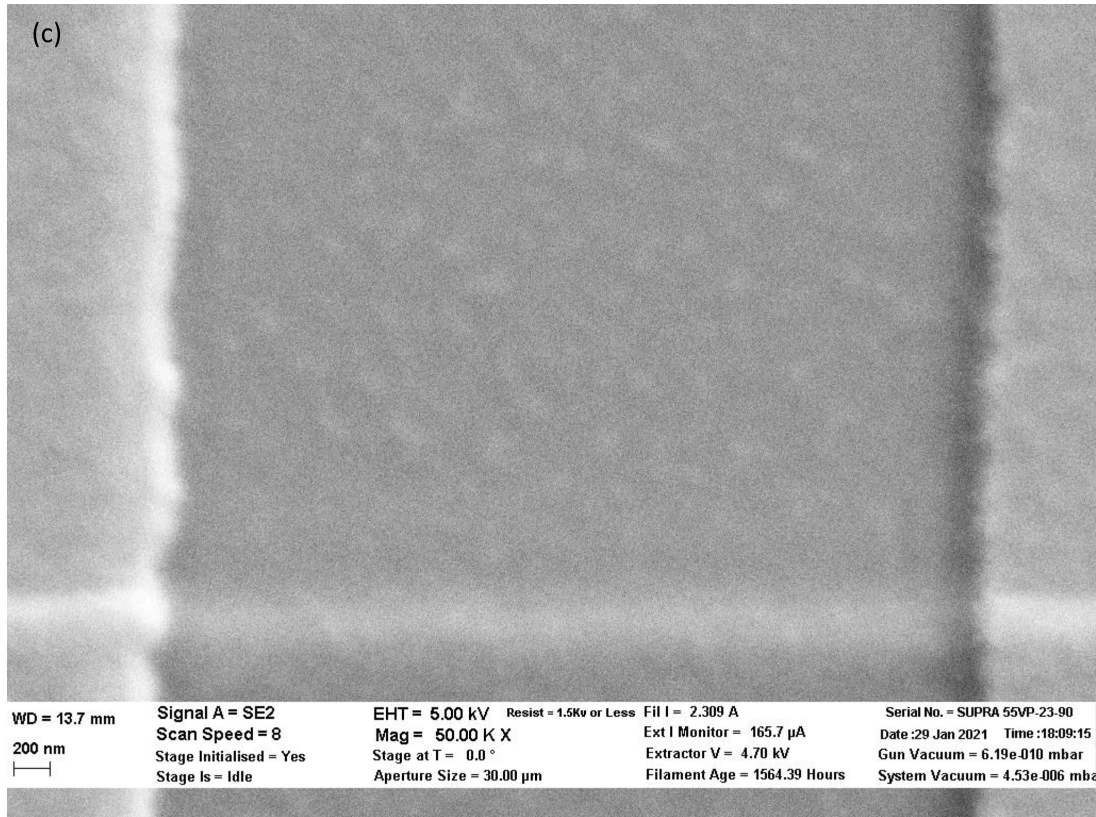


Figure 18: SEM Images showing residue formation after RIE etch step after PECVD deposition

However, after a few months of processing, the samples started to show gate leakage issues again. After a thorough investigation, we were able to pinpoint the gate leakage issue to the RIE etching step after the PECVD deposition. SEM images showed large (~µm) residue formation after the RIE etch step. We tried various thickness of PECVD and different etch thickness and sidewall thickness, different RIE etch times and additional Oxygen clean step after RIE (without over etching). The RIE residue was still visible, and the gate leakage current issue persisted. Therefore, we decided to remove the RIE step from the gate dielectric formation. Instead of PECVD sidewall formation, a thin silicon dioxide film with thickness of 30nm was deposited using PECVD. For a thinner gate dielectric alternative, we switched to using ~10nm of silicon nitride as the gate dielectric. For the 30 nm gate dielectric of silicon dioxide, the process was the same as before. After the passivation layer

deposition and lift-off, the next step was to deposit a 30 nm film of silicon dioxide using PECVD. As before, the standard PECVD clean recipe is run prior to proceeding with deposition. The PECVD chamber temperature is maintained at 380°C. The next step is to load a dummy wafer to start the PECVD conditioning recipe. The dummy wafer is inserted into the main PECVD deposition chamber from the load lock chamber. The process parameters are as follows for the conditioning recipe:

PECVD Conditioning Recipe

Recipe: KOH_SiO2 @380C @ 400W ICP power

Step 1

600 mT, N2: 250sccm,380C, 1200s

Step 2

600 mT, N2: 250sccm; N2O: 179sccm; SiH4/Ar: 5sccm, 380 C, 600s

Step 3

600 mT, N2: 250sccm; N2O: 179sccm; SiH4/Ar: 5sccm, 380 C, 400 W ICP RF, 600s

Step 4

250 mT, N2: 250sccm, 380 C, 180s

After the PECVD chamber conditioning process is finished, the conditioning wafer is unloaded from the PECVD chamber through an automatic unloading process. Now, dummy samples are prepared after HF (10:1) etching for 5 minutes and placed on the 4-inch PECVD carrier wafer and loaded into the load lock chamber. The load lock chamber is evacuated, and the loading process is started which inserts the carrier wafer along with the dummy samples into the main PECVD deposition chamber. Using the deposition rate calculated earlier the dummy samples were deposited with 30nm silicon dioxide. The deposited samples and the carrier wafer are unloaded from the PECVD deposition chamber. The thickness of the deposited silicon dioxide is measured using ellipsometer and

reflectometer. If the measured thickness is close to the nominal thickness, the main samples are placed on the 4-inch PECVD carrier wafer and loaded into the PECVD load lock chamber and inserted into the PECVD main deposition chamber. The deposition process is then started using the following parameters:

For SiO_2 Deposition

Recipe: KOH_SiO2 @380C @ 400W ICP power

Nominal PECVD oxide thickness = 30nm

Step 1

600 mT, N_2: 250sccm,380C, 1200s

Step 2

600 mT, N_2: 250sccm; N_2O: 179sccm; SiH_4/Ar: 5sccm, 380 C, 600s

Step 3

600 mT, N_2: 250sccm; N_2O: 179sccm; SiH_4/Ar: 5sccm, 380 C, 400 W ICP RF, 435s

Step 4

250 mT, N_2: 250sccm, 380 C, 180s

For deposition thickness of below 30nm for silicon dioxide, gate leakage current was observed for most of the devices. In order to deposit a thinner gate dielectric, a 10nm film of silicon nitride is deposited using PECVD. The standard PECVD clean process is done at 380°C. A PECVD conditioning process needs to be run before the main sample deposition process. The process parameters for the PECVD chamber conditioning for silicon nitride deposition are as follows:

For PECVD Conditioning for Si_3N_4

Recipe: Si3N4-Nanofab@300C @ 100W ICP power & 10W RIE power

Step 1

500 mT, N2: 250sccm, NH3: 50sccm SiH4/Ar: 20sccm 300C, 90s

Step 2

500 mT, N2: 250sccm; NH3: 50sccm; SiH4/Ar: 20sccm, 300 C, 100W ICP power &

10W RIE power 660s

Step 3

250 mT, N2: 250sccm, 300 C, 240s

After running the conditioning recipe, we run the same recipe on the freshly etched dummy wafer to determine the deposition rate, as there are always small variations we have observed because of various controlled factors. We run the recipe multiple times till we get a stable deposition rate. Once the stable deposition rate is determined, we load our Samples on top of the dummy wafer, as the equipment requires a full 4inch wafer to be placed inside the deposition chamber on top of the electrodes.

After loading the samples, for the actual deposition we keep all the parameters the same apart from the deposition time. The deposition rate is determined, and the deposition time is calculated for the main samples and the recipe for silicon nitride deposition of 10 nm is processed using the following parameters:

For Si3N4 Deposition

Recipe: Si3N4-Nanofab@300C @ 100W ICP power & 10W RIE power

Nominal PECVD oxide thickness = 10nm

Step 1

500 mT, N2: 250sccm, NH3: 50sccm SiH4/Ar: 20sccm 300C, 90s

Step 2

500 mT, N2: 250sccm; NH3: 50sccm; SiH4/Ar: 20sccm, 300 C, 100W ICP power &

10W RIE power 118s

Step 3

250 mT, N2: 250sccm, 300 C, 240s

After the PECVD deposition is completed for the gate dielectric, we can then proceed to the third mask step for the gate metal electrode patterning process.

3.1.5 Third Mask Lithography

Once the silicon window is protected by the Gate dielectric layer, we can now proceed to create a gate contact for the cold electron transistor. The first step is to pattern the gate contact pad area using photolithography.

3.1.5.1 Photolithography for Gate contact pads

The sample quadrant is spin-coated with a negative photoresist – NR9-1000PY. The photoresist is coated on the sample using a dropper to cover the entire surface and then spin-coated using the following parameters:

Step 1:

500 rpm; 100 rpm/s; 5 seconds

Step 2:

3000 rpm; 1000rpm/s; 60 seconds

Step 3:

0 rpm; 1000rpm/s; 0.1 seconds

After the spin-coating is done the sample quadrant is pre-baked on a hot plate at 150˚C for 1 minute and then allowed to cool down on a cooling plate.

The Third Mask Pattern from the Alignment mask is used for the Gate contact pad patterning and is loaded on to the OAI Aligner. The substrate carrier wafer is loaded

beneath the Mask inside the OAI Aligner and the sample quadrant is fixed on the substrate carrier wafer using scotch tape at the base of the sample. The Third mask pattern is aligned using the second masks alignment marks at the corners of the sample So that the third mask pattern is overlapping with the first mask silicon window pattern present on the sample. Once the third mask is aligned with the alignment marks, the third mask is pressed on to the sample and the pattern is exposed after contact vacuum is turned on. The photolithography pattern parameters are as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 19.6 mW/cm^2

Exposure Time: 6.1 seconds

Dose: 120 mJ/cm^2

After the exposure is done the sample quadrant is taken out and post-baked on a hot plate at 100˚C for 1 minute. The sample quadrant is then placed on a cooling plate and allowed to cool down to room temperature. After the sample quadrant cools down, the sample is immersed in a developer solution RD6 for 25 seconds with vigorous shaking to remove the unexposed regions of the photoresist. The sample is then immersed in DI water container for 5 minutes with regular stirring, then moved to a second DI water container for 5 minutes with regular stirring. The sample is then taken out and blow-dried in nitrogen, leaving behind the third mask pattern on the photoresist coating on the sample.

3.1.5.6 Gate Contact Metal Pad deposition

After the 3rd mask photolithography step the samples are loaded into CHA Solution or AJA E-Beam Evaporator to deposit Chromium and Gold with physical vapour deposition technique using Electron beam evaporator for Source and Drain electrode pads.

Procedure for CHA Solution:-

The Samples are loaded onto the substrate holder, and the Chamber is vented to load the samples and the crucibles. After the vent operation is completed and the chamber pressure is reached atmospheric pressure(7.5*E+2 Bar). The samples are loaded on a rotational substrate carrier in the tool. The Chromium Crucible are added to respective holders. After verifying the Thickness monitor crystal have a sufficient lifespan. The deposition chamber is closed and pump-down can be started. While the Chamber is pumping down to the designed set point. The Deposition recipe can be added to the system which contains the deposition material, deposition rate, deposition thickness, and Substrate temperature. For Source and Drain pads we first deposit 50nm of Chromium with a 0.1nm/Sec deposition rate at room temperature. Once the deposition is completed for chromium.

Once the metals are deposited on the sample the chamber is again vented at atmospheric pressure in order to unload the Samples and the Crucible. After removing the samples from Chamber, the chamber is again pumped down to the designed set point to avoid any contaminants inside the deposition chamber.

For AJA-E-Beam Evaporator:-

The Samples are loaded on the Sample Holder and the loading dock for the AJA-E Beam evaporator is vented with nitrogen. Once the loading dock has reached the atmospheric pressure we can load the samples on the Substrate delivery shaft with samples facing down. The Loading chamber is closed and is pumped down until the pressure inside the loading

dock is not below 2.0E-5 Torr. Once the pressure is below the set point the Deposition chamber gate can be opened and with the help of the Substrate delivery shaft the samples are loaded into the deposition chamber. The sample holder is attached to the rotational shaft which can control the distance from the source material and rotational speed. Once the sample holder is securely mounted the Substrate delivery shaft is retracted and the deposition chamber is closed. The rotations and the height of the sample holder are adjusted to the designed position and the rotational speed is adjusted according to the need. After Selecting the desired material crucible with the help of a material selector switch. We verify the Material Density and acoustic impedance is properly configured in the thickness monitoring system. Once the system is properly configured, we start the E-Beam gun and gradually increase the current to heat the material till we reach the desired deposition rate. After reaching the stable deposition rate the substrate shutter can be opened and with the help of a thickness monitor the thickness of deposited material can be monitored. In our case, as the metal to deposit is Chromium it is deposited at 0.1nm/Sec rate with 60RPM Rotational speed at room temperature with a thickness of 50nm. Once we have deposited the desired thickness the Substrate shutter is engaged to prevent additional deposition on the sample.

Once the material deposition is completed the gun current is slowly reduced to minimal and the gun is powered off, and the sample rotations are turned off after verifying the loading dock pressure is still within the parameters, The loading docks door is opened and with the help of Substrate delivery shaft, the sample holder is moved back to the loading dock. And the Deposition chambers door is closed and the Loading dock is vented to remove the samples from the equipment. The loading dock is kept in a Vacuum to avoid any contaminates going in the Loading dock.

3.1.5.6 Passivation layer deposition

After the metal deposition is done, the next step is to deposit the passivation layer to protect the electrodes in further process. We are using silicon dioxide as a passivation layer with thickness of 50nm it was done in the AJA Sputter deposition equipment with the following parameters:

Power: 148W

Pressure: 5mT

Ar: 30sccm, O2: 6sccm

The deposition time for 1 nm silicon dioxide was calculated, from the deposition rate of 0.00637 nm/s obtained for a dummy sample deposition, to be 7837 seconds.

3.1.5.3 Lift-off

After the Passivation layer is deposited, the sample quadrant is unloaded from the AJA Sputter equipment. The photoresist needs to be removed using a lift-off process. The samples are is immersed in Acetone and sonicated for 5 minutes followed by a 30 second IPA rinse. The sample is then immersed in IPA and sonicated for 5 minutes, again followed by an IPA rinse for 30 seconds. It is then blow dried in Nitrogen. The Sonication steps are listed below:

Step 1: Acetone Sonication (5 minutes) + IPA Rinse (30 seconds)

Step 2: IPA Sonication + IPA Rinse (30 seconds)

Step 3: Nitrogen Blow dry

3.1.5.1 Photolithography for Via holes

The sample quadrant is spin-coated with a negative photoresist – NR9-1000PY. The photoresist is coated on the sample using a dropper to cover the entire surface and then spin-coated using the following parameters:

Step 1:

500 rpm; 100 rpm/s; 5 seconds

Step 2:

3000 rpm; 1000rpm/s; 60 seconds

Step 3:

0 rpm; 1000rpm/s; 0.1 seconds

After the spin-coating is done the sample quadrant is pre-baked on a hot plate at 150˚C for 1 minute and then allowed to cool down on a cooling plate.

The Fourth Mask Pattern from the Alignment mask is used for the Gate contact pad patterning and is loaded on to the OAI Aligner. The substrate carrier wafer is loaded beneath the Mask inside the OAI Aligner and the sample quadrant is fixed on the substrate carrier wafer using scotch tape at the base of the sample. The Fourth mask pattern is aligned using the Third mask's alignment marks at the corners of the sample So that the third mask pattern is overlapping with the first mask silicon window pattern present on the sample. Once the third mask is aligned with the alignment marks, the Fourth mask is pressed on to the sample and the pattern is exposed after contact vacuum is turned on. The photolithography pattern parameters are as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 19.6 mW/cm^2

Exposure Time: 6.1 seconds

Dose: 120 mJ/cm^2

After the exposure is done the sample quadrant is taken out and post-baked on a hot plate at 100˚C for 1 minute. The sample quadrant is then placed on a cooling plate and allowed to cool down to room temperature. After the sample quadrant cools down, the sample is immersed in a developer solution RD6 for 25 seconds with vigorous shaking to remove the unexposed regions of the photoresist. The sample is then immersed in DI water container for 5 minutes with regular stirring, then moved to a second DI water container for 5 minutes with regular stirring. The sample is then taken out and blow-dried in nitrogen, leaving behind the third mask pattern on the photoresist coating on the sample.

3.1.3.2 Silicon Dioxide etching using Reactive Ion Etching

The next step is to expose the Metal Pads of electrodes in the pattern area. This region will be used to Probe the device for I-V Characteristic measurements and provide protection with the passivation layer on the rest of the device. Thus, the metal in the pattern area will need to be exposed. The silicon dioxide present in the pattern is etched using reactive ion etching in the Technics Macro RIE – 8800 equipment.

The silicon dioxide etch time is established by optimizing the etch rate by etching for different times using the CF4/O2 etch recipe. The different etch times and etch thicknesses are plotted and the etch rate for Silicon dioxide is calculated to be 0.7 nm/s. As the Selectivity for SiO2 v/s Metal is very high we don't need to keep any margin in this process

The Reactive Ion Etching Parameters are as follows:

Step 1: 600W, 170mT, CF4: 30 sccm, O2: 7.2 sccm, 300s

Step 2: 350W, 200mT, O2: 11.0 sccm, 180s

Once the RIE etching is done, The contact IV of the exposed are is measured using I-V Probe station. Once we confirm the I-V Characters are liner we can assume the Metal on the pads are exposed. Then we can proceed to the metal deposition for the contact Probs.

3.1.5.6 Gate Contact Metal Pad deposition

After the 4th mask photolithography step the samples are loaded into CHA Solution or AJA E-Beam Evaporator to deposit Chromium and Gold with physical vapour deposition technique using Electron beam evaporator for Source and Drain electrode pads.

Procedure for CHA Solution:-

The Samples are loaded onto the substrate holder, and the Chamber is vented to load the samples and the crucibles. After the vent operation is completed and the chamber pressure is reached atmospheric pressure(7.5*E+2 torr). The samples are loaded on a rotational substrate carrier in the tool. The Chromium and the Gold Crucibles are added to their respective holders. After verifying the Thickness monitor crystal have a sufficient lifespan. The deposition chamber is closed and pump-down can be started. While the Chamber is pumping down to the designed set point. The Deposition recipe can be added to the system which contains the deposition material, deposition rate, deposition thickness, and Substrate temperature. For Source and Drain pads we first deposit 50nm of Chromium with a 0.1nm/Sec deposition rate at room temperature. Once the deposition is completed for chromium. The chamber is again pumped down to the designed pressure set point. And after reaching the desired vacuum pressure the gold deposition is started for the thickness of 15nm with 0.1nm/Sec deposition rate at room temperature.

Once both the metals are deposited on the sample the chamber is again vented at atmospheric pressure in order to unload the Samples and the Crucible. After removing the samples from Chamber the chamber is again pumped down to the designed set point to avoid any contaminants inside the deposition chamber.

For AJA-E-Beam Evaporator:-

The Samples are loaded on the Sample Holder and the loading dock for the AJA-E Beam evaporator is vented with nitrogen. Once the loading dock has reached the atmospheric pressure we can load the samples on the Substrate delivery shaft with samples facing down. The Loading chamber is closed and is pumped down until the pressure inside the loading dock is not below 2.0E-5 torr. Once the pressure is below the set point the Deposition chamber gate can be opened and with the help of the Substrate delivery shaft the samples are loaded into the deposition chamber. The sample holder is attached to the rotational shaft which can control the distance from the source material and rotational speed. Once the sample holder is securely mounted the Substrate delivery shaft is retracted and the deposition chamber is closed. The rotations and the height of the sample holder are adjusted to the designed position and the rotational speed is adjusted according to the need. After Selecting the desired material crucible with the help of a material selector switch. We verify the Material Density and acoustic impedance is properly configured in the thickness monitoring system. Once the system is properly configured we start the E-Beam gun and gradually increase the current to heat the material till we reach the desired deposition rate. After reaching the stable deposition rate the substrate shutter can be opened and with the help of a thickness monitor the thickness of deposited material can be monitored. In our case, as the 1 metal to deposit is Chromium it is deposited at 0.1nm/Sec rate with 60RPM Rotational speed at room temperature with a thickness of 50nm. Once we have deposited the desired thickness the Substrate shutter is engaged to prevent additional deposition on

the sample. The Current for the E-Beam gun is slowly reduced to prevent damage to the gun and after reaching minimal current the gun is switched off. The different material crucible is then selected and again configured with the thickness monitor according to the material property. Once the deposition chamber pressure has dropped to the designed setpoint, The gun can be again powered on to deposit new material In our case the second material is Gold which is deposited at 0.1nm/Sec at Room temperature for 15nm of thickness.

Once all the material deposition is completed the gun current is slowly reduced to minimal and the gun is powered off, and the sample rotations are turned off after verifying the loading dock pressure is still within the parameters, The loading docks door is opened and with the help of Substrate delivery shaft, the sample holder is moved back to the loading dock. And the Deposition chambers door is closed and the Loading dock is vented to remove the samples from the equipment. The loading dock is kept in a Vacuum to avoid any contaminates going in the Loading dock.

3.1.5.7 Lift-off

After the deposition is done, the photoresist needs to be removed using a lift-off process. The samples are immersed in Acetone and sonicated for 5 minutes followed by a 30 second IPA rinse. The sample is then immersed in IPA and sonicated for 5 minutes, again followed by an IPA rinse for 30 seconds. It is then blow dried in Nitrogen. The Sonication steps are listed below:

Step 1: Acetone Sonication (5 minutes) + IPA Rinse (30 seconds)

Step 2: IPA Sonication + IPA Rinse (30 seconds)

Step 3: Nitrogen Blow dry

The device fabrication is now complete and can be utilized for current voltage characterization.

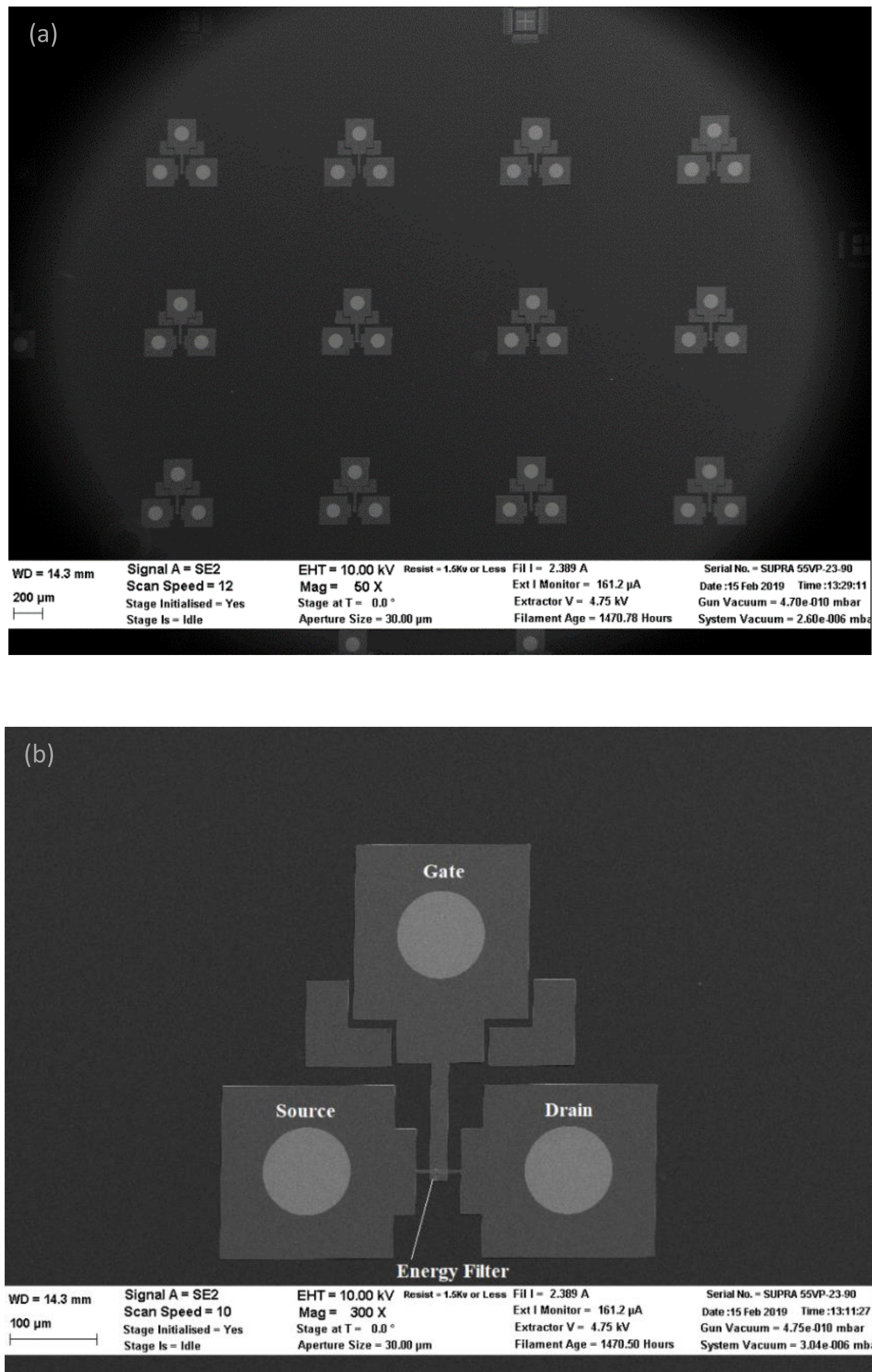


Figure 19: SEM images showing (a) CET devices array and (b) top view of a single transistor device

3.2 Fabrication Procedure for Single Particle Placement of Nanoparticles

3.2.1 Introduction

Controlled placement of nanoparticles[130, 131] at specific location is of significant importance towards fabrication of functional materials[132] where placement of individual nanoscale building blocks[133, 134] plays an important role towards improving future electronic[135], magnetic and optical[136] device applications. Single-particle placement of nanoparticles using electrostatic guidance[137-140] provides a promising method to allow for a large-scale controlled placement of these building blocks on a large area. Other methods have been attempted for assembling a particle assembly of colloidal particles[141, 142] via convective and capillary assembly[143-147] and using DNA molecules to direct placement of nanoparticles[148], however our group is working on placement of individual nanoparticles by electrostatically guiding them onto electrostatic templates to achieve single nanoparticle placement per template.

3.2.2 Wafer Cleaning

For the single particle placement experiment, we start with a standard 4-inch bare silicon wafer. The single particle placement process requires the formation of SAMs layers and as a result the samples used for the single particle placement experiment are required to be thoroughly cleaned prior to utilization.

The sample cleaning process consists of Piranha cleaning process and followed by a HF (10:1) clean step. For the piranha cleaning step, we need to use freshly prepared piranha solution. Piranha solution is a 3:1 solution of Sulfuric acid and hydrogen peroxide. Piranha solution is prepared in a glass beaker. 60ml of sulfuric is measured using a glass measuring cylinder and transferred to a large glass beaker. The measuring cylinder is thoroughly cleaned using running DI water. This is followed by measuring out a 10ml of hydrogen peroxide in the glass measuring cylinder which is added to the glass beaker containing

sulfuric acid very slowly. The hydrogen peroxide is added dropwise along the edges of the beaker to the sulfuric acid. This precaution needs to be taken in order to avoid the splashing of the piranha solution as the process is highly exothermic. Once the piranha solution is ready, the 4-inch bare silicon wafer is immersed into the solution for 30 minutes. After the 30 minutes are done, the wafer is taken out and immersed in the first DI water container for 5 minutes with regular stirring. The wafer is then taken out and transferred to a second DI water container for 5 minutes with regular stirring. After the second DI water immersion is done, the wafer is taken out and rinsed under running DI water for 1 minute. The wafer is then blow dried with nitrogen.

The next step in the cleaning process is the HF (10:1) etch step. HF (10:1) is taken in a HDPE beaker. The Piranha cleaned wafer is then transferred to the HF (10:1) and immersed in the beaker for 10 minutes. The wafer is then taken out and transferred to a second DI water container for 5 minutes with regular stirring. After the second DI water immersion is done, the wafer is taken out and rinsed under running DI water for 1 minute. The wafer is then blow dried with nitrogen.

3.2.3 Thermal Oxidation - Tystar – 100nm Silicon Dioxide Growth

The cleaned wafer needs to be coated with a thermal oxide layer before dicing the wafer to avoid contamination of the wafer surface. After the thorough cleaning of the 4-inch bare silicon wafer is done, the wafer is loaded into the Tystar oxidation furnace for oxidation. A nominal silicon dioxide thickness of 100nm is required to be grown on the wafer. The oxidation parameters are as follows:

Tystar Thermal Oxidation Furnace: SPP100NM

Idle Temp: 450 C

Boat Out: 15 min

Boat In: 15 min

Ramp 700 C: 30 min ; N2: 5000 sccm

Stabilize: 30 min ; N2: 5000 sccm

Ramp 1100 C: 2 hrs ; N2: 5000 sccm

Hold: 2hr 10mins ; O2: 3000 sccm

Anneal: 20 min ; N2: 5000sccm

Ramp down 700 C: 2 hrs ; N2: 5000sccm

Hold 700 C: Till alarm Acknowledged

After the oxidation is done the wafer is unloaded from the Tystar oxidation furnace.

3.2.4 Wafer Dicing

The wafers are then loaded into the Dicing equipment. The dicing parameters for the samples are 6mm by 9mm pieces. The dicing machine makes deep scratches on the wafer with sample grids of 8mm by 9mm sizes. After dicing is done the sample surface contains contamination due to the presence of city water during dicing process.

3.2.5 Wafer Cleaning

Thus, the wafer cleaning process needs to be done again. However, before starting the cleaning process, we need to strip the oxide layer present on the wafer. This is done by using HF(10:1) etch step. The wafer is immersed in a HDPE beaker containing HF (10:1) for 10 minutes. The wafer is taken out and immersed in a first DI water container for 5 minutes with regular stirring. The wafer is then taken out and transferred to a second DI water container for 5 minutes with regular stirring. After the second DI water immersion is done, the wafer is taken out and rinsed under running DI water for 1 minute. The wafer is then blow dried with nitrogen.

The piranha cleaning and the HF (10:1) etch process needs to be repeated to completely get rid of any contamination that may have occurred during the dicing process. Again, we need to use a freshly prepared piranha solution for the cleaning process. The piranha solution is prepared by taking 60mL of sulfuric acid in a large glass beaker. A 20mL of hydrogen peroxide is added dropwise along the walls of the beaker into the sulfuric acid. This step needs to be done very carefully and slowly as the process is very exothermic in nature. Proper precautions need to be taken when handling these acids. Full PPE equipment needs to be worn when handling acids. After the piranha solution is ready, the processed wafer is then immersed into the piranha solution for 30 minutes. After the completion of 30 minutes, the wafer is taken out and immersed in the first DI water container for 5 minutes with regular stirring. The wafer is then taken out and transferred to a second DI water container for 5 minutes with regular stirring. After the second DI water immersion is done, the wafer is taken out and rinsed under running DI water for 1 minute. The wafer is then blow dried with nitrogen.

The piranha cleaned wafer is then transferred to a HDPE beaker containing HF (10:1) and immersed in it for 10 minutes. The wafer is taken out and immersed in a first DI water container for 5 minutes with regular stirring. The wafer is then taken out and transferred to a second DI water container for 5 minutes with regular stirring. After the second DI water immersion is done, the wafer is taken out and rinsed under running DI water for 1 minute. The wafer is then blow dried with nitrogen.

3.2.6 Thermal Oxidation – Tystar – 10nm Silicon Dioxide Growth

Now that the wafers have been cleaned thoroughly, we need to grow a thin layer, ~10nm, of silicon dioxide using thermal oxidation. The cleaned wafer is loaded into the Tystar oxidation furnace for thermal oxidation. A nominal oxide thickness of 10nm is required to be grown using the thermal oxidation step. The oxidation parameters are as follows:

Tystar Thermal Oxidation Furnace: SPP10NM

Idle Temp: 450 C

Boat Out: 15 min

Boat In: 15 min

Ramp 700 C: 30 min ; N2: 5000 sccm

Stabilize: 30 min ; N2: 5000 sccm

Ramp 750 C: 1 hr ; N2: 5000 sccm

Hold: 170mins ; O2: 3000 sccm

Anneal: 20 min ; N2: 5000sccm

Ramp down 700 C: 2 hrs ; N2: 5000sccm

Hold 700 C: Till alarm Acknowledged

The wafer is unloaded from the Tystar oxidation furnace. The wafer is then subjected to another surface cleaning step.

3.2.7 Wafer Surface Cleaning

Another batch of Piranha solution is freshly prepared using 3:1 solution of sulfuric acid and hydrogen peroxide. 60mL of sulfuric acid is taken is a large glass beaker. To this sulfuric acid, 20mL of hydrogen peroxide is added along the walls of the beaker dropwise very slowly and taking extreme care. Full PPE gear needs to be worn when handling acids. Once the piranha solution is ready, the wafer is immersed in the piranha solution for 30 minutes. After the 30-minute immersion is done, the wafer is taken out and immersed in the first DI water container with regular stirring. The wafer is then taken out and rinsed under running DI water for 1 minute followed by immersion in the second DI water container for 5 minutes. The wafer is then taken out and rinsed under running DI water for 1 minute. The wafer is then transferred to a beaker containing IPA and is sonicated for 10 minutes. After the sonication is done the wafer is thoroughly blow dried with nitrogen for

at least 2 minutes. This is important as any IPA residue will cause contamination during the following bake out step. After the thorough drying of the wafer with nitrogen, the wafer is heated on a hot plate at 200°C for 30 minutes.

3.2.8 E-beam Lithography Procedure:

The diced and cleaned wafer is cut into a 4x5 sample with each part of 6mm by 9mm size. The sample is then spin-coated with e-beam photoresist – maN-2401. The spin-coating parameters are as follows:

Step 1:

500rpm; 100rpm/s; 5seconds

Step 2:

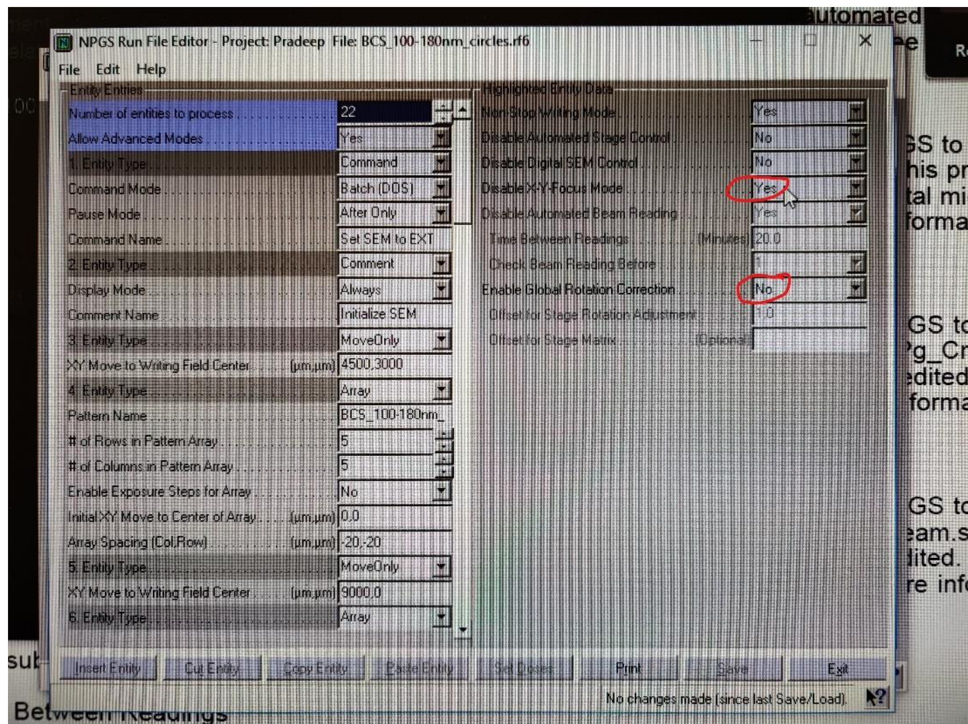
3000rpm; 1000rpm/s; 30seconds

Step 3:

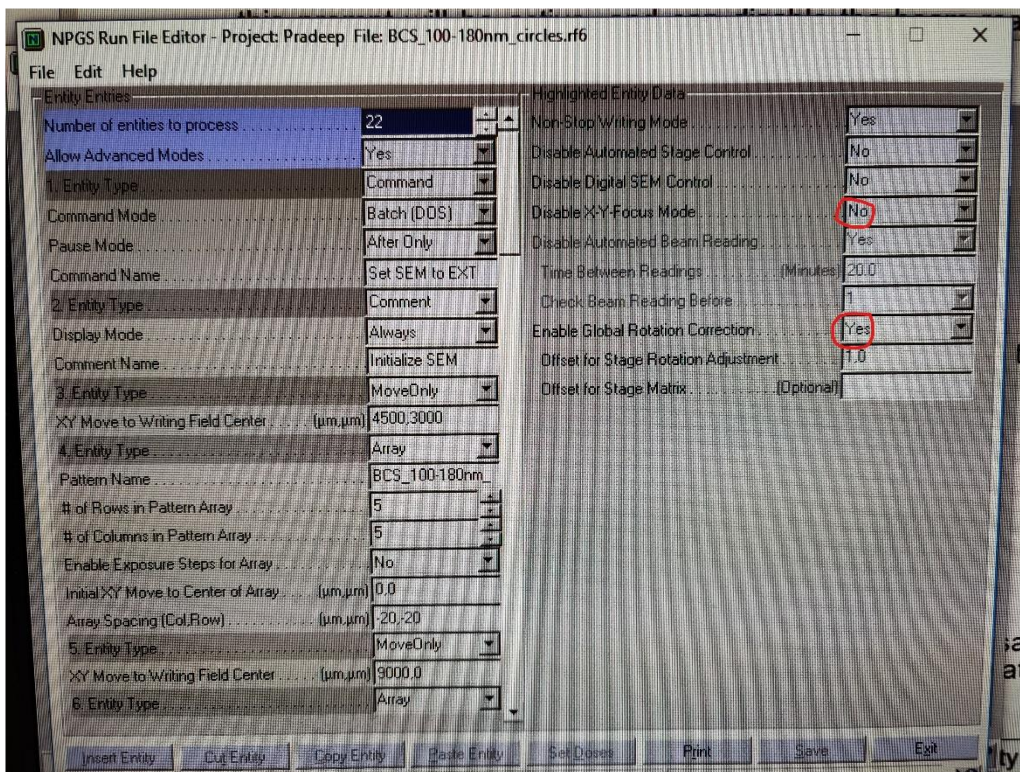
0rpm; 1000rpm/s; 0.1s

The sample is pre-baked on a hot plate at 90°C for 1 minute after the spin-coating step. The sample is now ready for e-beam lithography patterning process.

1. Before loading sample into e-beam writer chamber, Right click on the required pattern run file (*.rf6). Pattern File we are using is C_90-110nm_10x10um_400-500nm pitch.rf6.
2. This file contains 2 patterns: a) C-90-110nm holes array and b) BCS_100-180nm holes array.
3. In the right click menu, select Run File Editor.



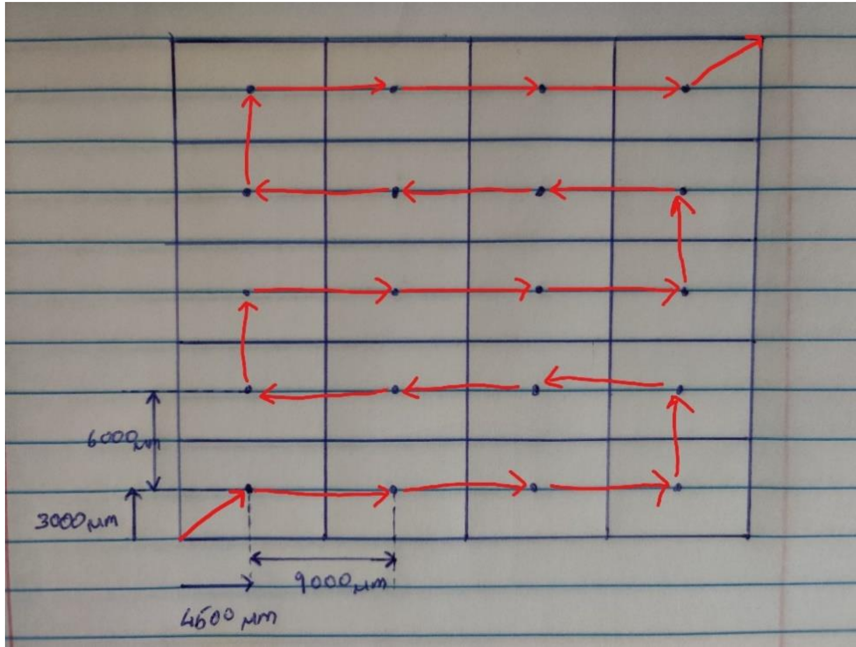
4. On the right-hand side there are settings for XY Focus Mode and Global Rotation Correction. Set each setting as shown below:



5. On the left-hand side we need to set up multiple entities as shown above.

6. Copy the command and comment entity as is.

7. The array entity is responsible for creating the pattern.
8. The Pattern name in the array entity we use is C_90-110nm_10x10um_400-500nm pitch_3x3 and BCS_100-180nm_3x3.
9. The array entity creates an array of the C_90-110nm and the BCS_100-180nm pattern in an array of 3 by 3 – as defined by the number of rows and columns specified in the array entity.
10. The array spacing defines the centre-to-centre distance between the adjacent patterns.
11. Our sample consists of 9mm by 6 mm samples in a 4 by 5 array. We need to make this 3 by 3 array of pattern on all 20 samples. The second BCS pattern is written at an offset of 500um from the C_90-110nm pattern.
12. We introduce the "Move Only Entity" which defines the coordinates to which the stage will be moved before the pattern is written.
13. We need to create an Array entity for each sample. Copy and paste the Array Entity. This will copy all the data on the right hand side as is. And Before each array entity, we insert a Move Only Entity. Thus, for a 4 by 5 sample, we need 40 Array entities and 41 Move Only Entities.
14. Each Move Only Entity is used to move stage to pattern on an adjacent sample. The "Move Only" coordinates are relative to current position of beam. The 4 by 5 sample architecture is as shown:



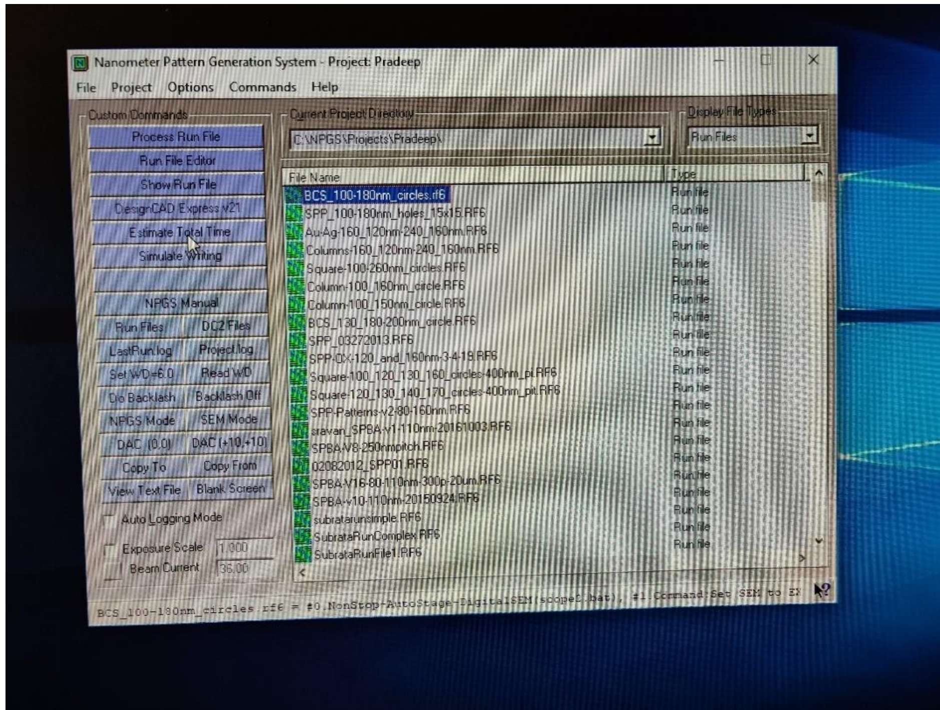
15. The initial position of the beam is at the corner of the entire 4 by 5 sample.
16. Therefore, the first “Move only” coordinates will be (4500, 3000). This moves the beam position to the centre of the first sample. The Array entity patterns the sample.
17. An additional Move only entity (500,0) is used to move to an adjacent location to write the second array pattern on the 1st sample. The subsequent “Move only” entity coordinates (8500, 0) moves the beam to the second sample.
18. X-direction Move only coordinates will be (500, 0) + (8500, 0), and (-500, 0) + (-8500, 0). Y-direction move only coordinates will be (500, 6000) and (-500, 6000).
19. After defining all entities to complete the pattern array, we define an additional Move Only entity to move the gun away from the final pattern. The “Move Only” coordinates for the final move is (4000, 3000). This moves the beam to the top right corner of the sample. (All the Move Only relative coordinates are shown in the figure below).

1. 4500,3000
2. 500,0
3. 8500,0
4. 500,0
5. 8500,0,
6. 500,0
7. 8500,0
8. 500,0
9. -500,6000
10. -500,0
11. -8500,0
12. -500,0
13. -8500,0
14. -500,0
15. -8500,0
16. -500,0
17. 500,6000
18. 500,0
19. 8500,0
20. 500,0
21. 8500,0,
22. 500,0
23. 8500,0
24. 500,0
25. -500,6000
26. -500,0
27. -8500,0
28. -500,0
29. -8500,0
30. -500,0
31. -8500,0
32. -500,0
33. 500,6000
34. 500,0
35. 8500,0
36. 500,0
37. 8500,0
38. 500,0
39. 8500,0,
40. 500,0
41. 4000,3000

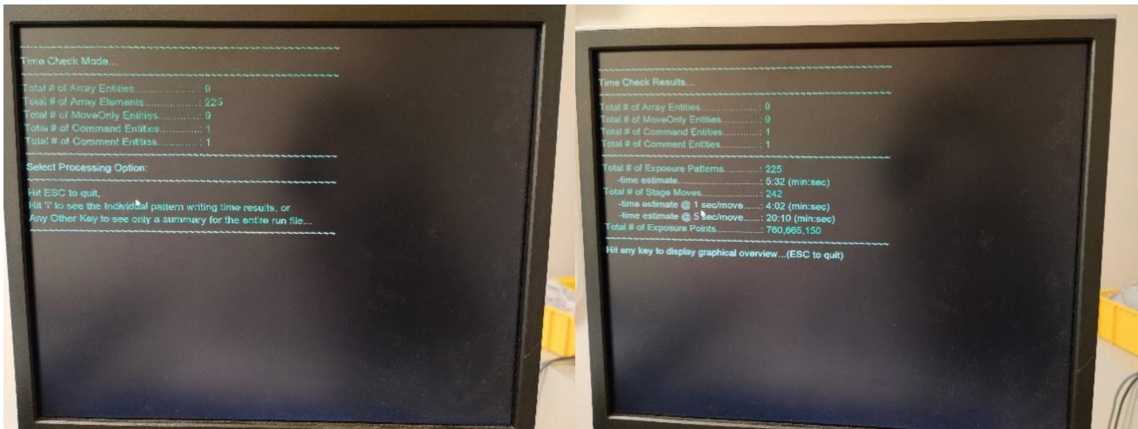
20. We also need to define a new Command Entity – EHT_off.bat to turn off the EHT.

21. Once all the entities are defined. Save the file and exit.

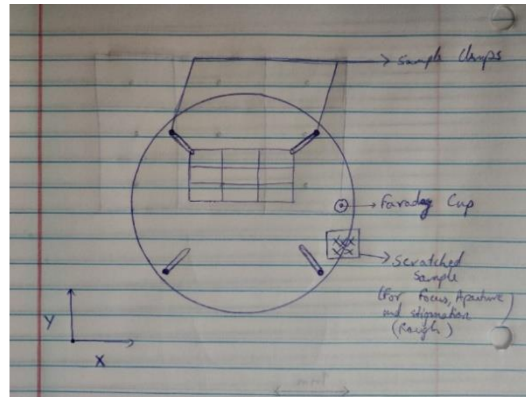
22. The defined pattern and pattern time can be verified using the Estimate total time option:

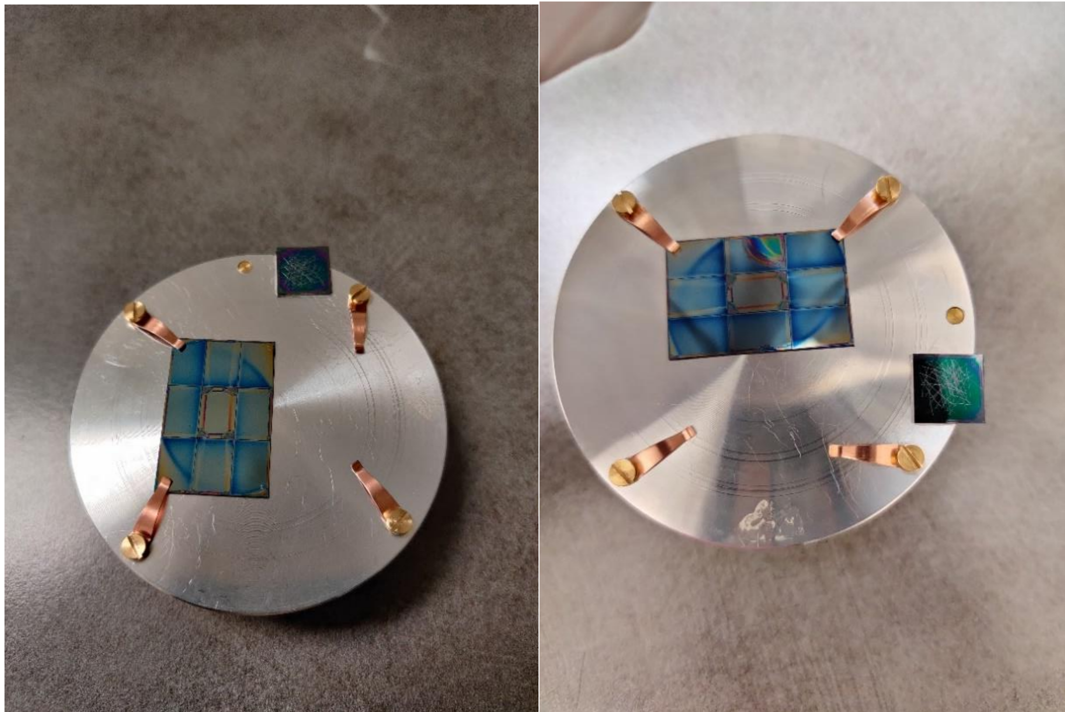


23. This opens a new window. We wait for a few seconds for the estimation to complete.



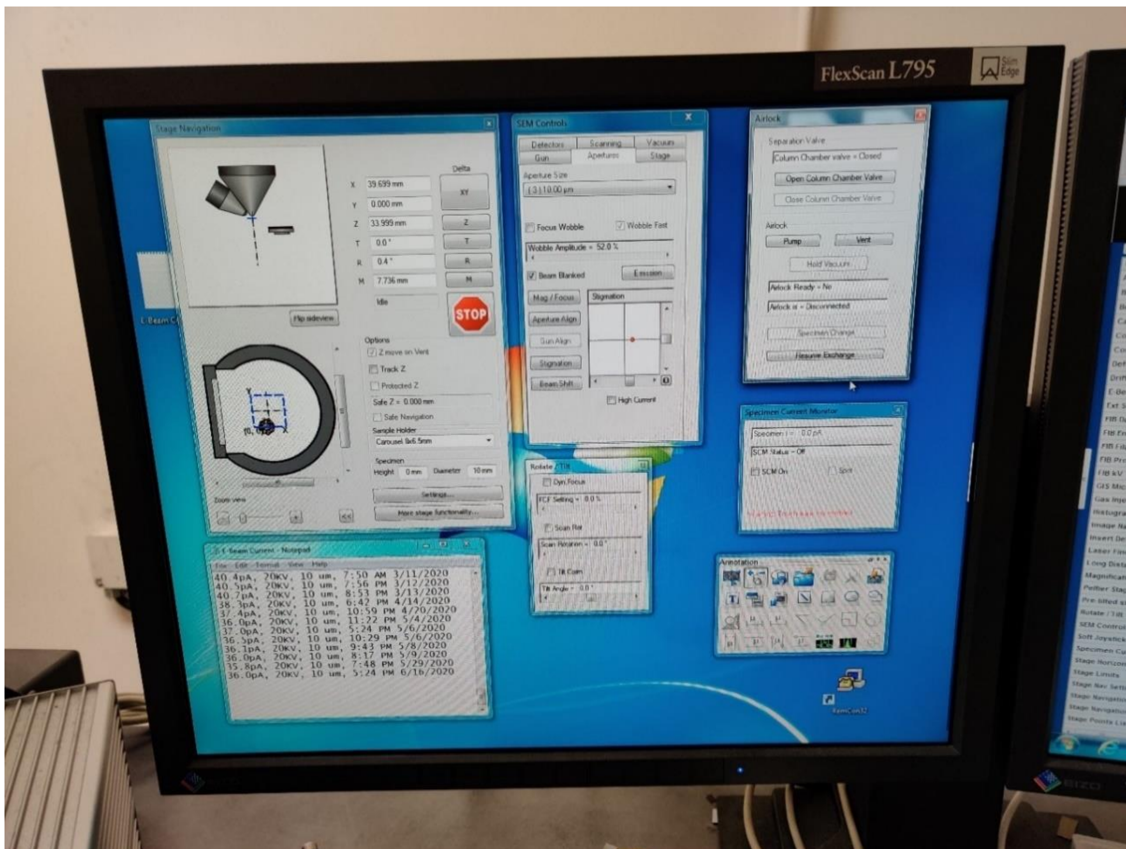
24. Follow the onscreen instructions to display the graphical overview of the pattern and verify the distance between each pattern location and the initial and final beam position.
25. Fix the sample onto the bigger ebeam stage (Stage belongs to Dr. Zhou's Group – Zhonghe Liu).

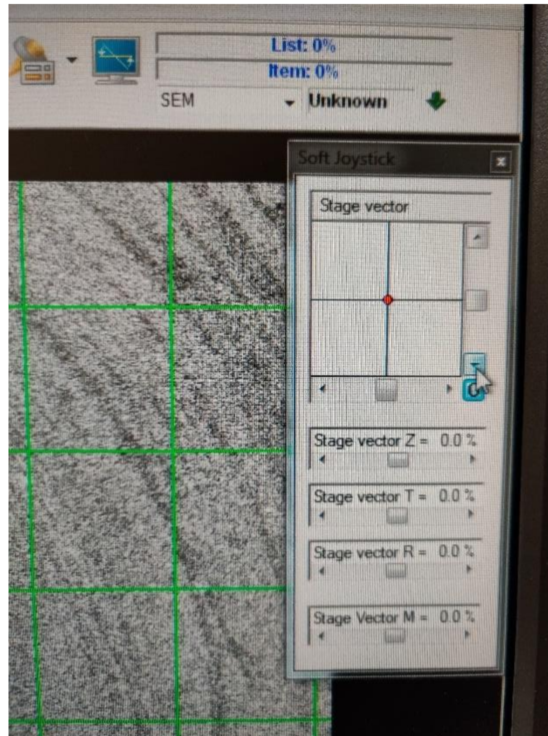




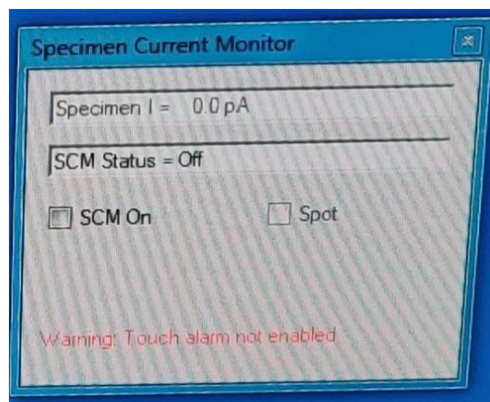
26. Do not remove the small sample fixed at the edge of the stage. This is used for rough Focus, aperture alignment and stigmation.
27. Do not rotate the stage with respect to the bottom attachment. The screws on the stage are aligned with the X and Y axis. The faraday cup is at a specific coordinate. Rotation will shift the coordinates for the faraday cup and misalign the X and Y axis of the stage.
28. The stage can accommodate a 4 by 5 SPP sample.
29. The sample should be attached with one edge parallel to the screw locations. This will roughly align the sample edge with the X axis making it easier to adjust the rotation alignment for automated patterning.

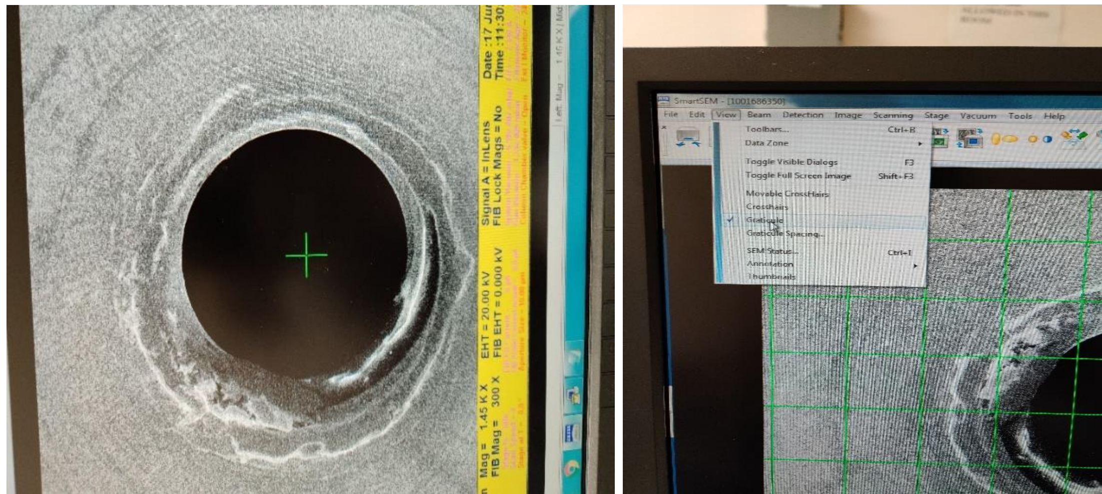
30. Load the stage into the ebeam loadlock and insert it into the ebeam chamber using the loading procedure according to training.
31. Do not turn ON the EHT yet.
32. Open all the panels shown below: Stage navigation, SEM Controls, Airlock, Rotate/Tilt, Specimen Current Monitor and Soft Joystick. Also open the Ebeam Current notepad file from the desktop.



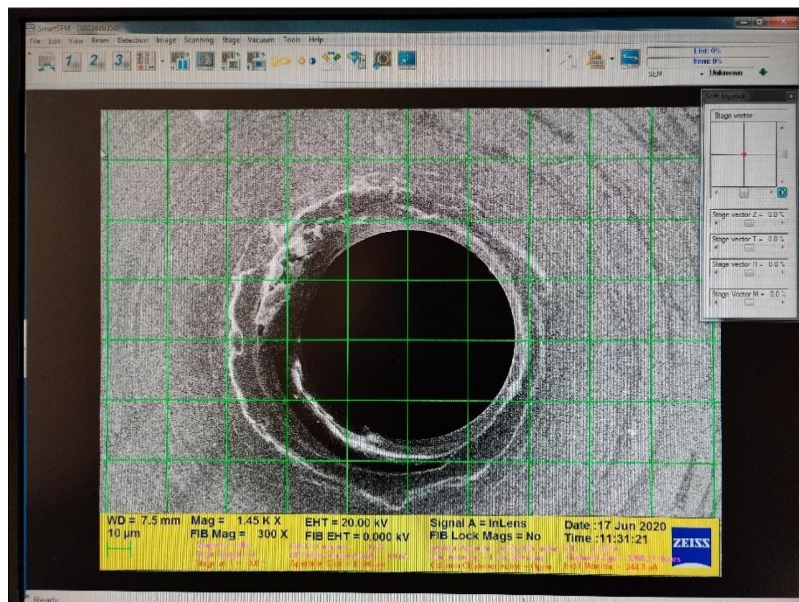


33. Move the stage by inputting the coordinates for the faraday cup in the stage navigation box.
34. Set Rotation to 350.7 degrees. Faraday Cup Coordinates: 20.728, 49.494
35. Set Stage Height to 41.821 mm. Move stage Z height using joystick.
36. Turn on the EHT. Focus on the edge of the faraday cup. The focus for the Faraday cup is very close to WD = 7.5mm. Input this value and do rough adjustment to bring the faraday cup into focus.
37. Select Spot mode from the Specimen Current Monitor Box. This creates a green crosshair where the beam is in spot mode.

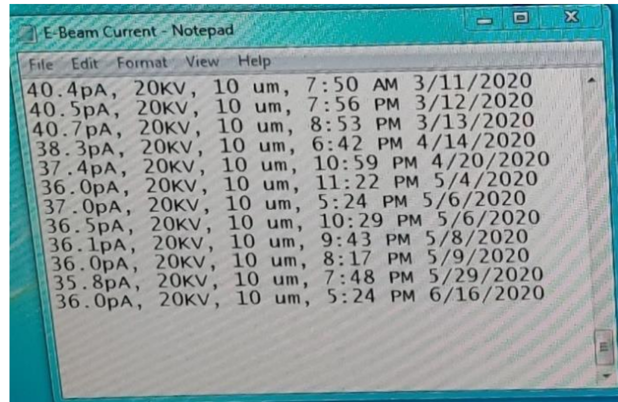




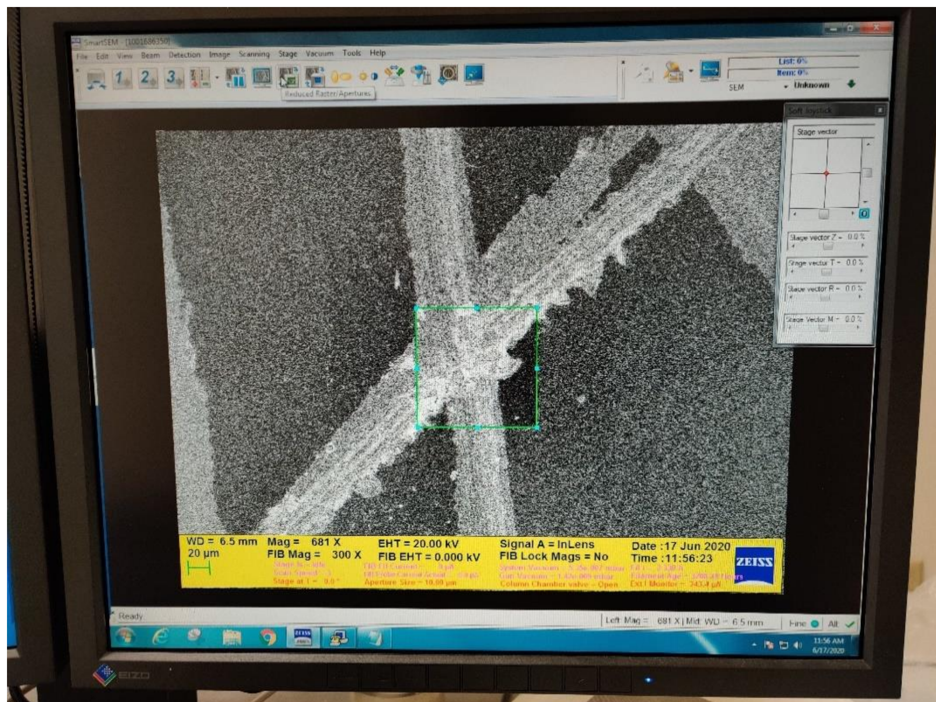
38. From the View dropdown menu select Graticule option to enable on-screen grid.
39. Use the grid to centre the spot crosshair.



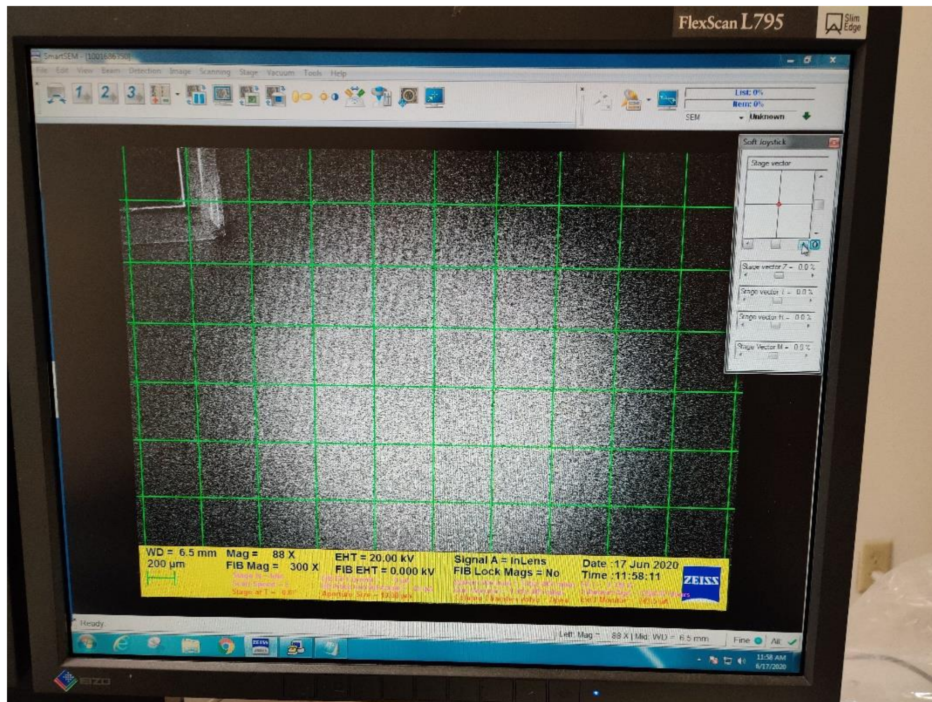
40. When the spot crosshair is perfectly centred it is no longer visible when graticule is turned on.
41. Check the SCM ON box. This will measure the beam current. Wait for 2 minutes for the beam current to stabilize.
42. Note down the reading in the Ebeam current notepad file. Enter the Current Value, EHT Voltage and Aperture Size. The Press F5 – this automatically inputs the current time for the reading:



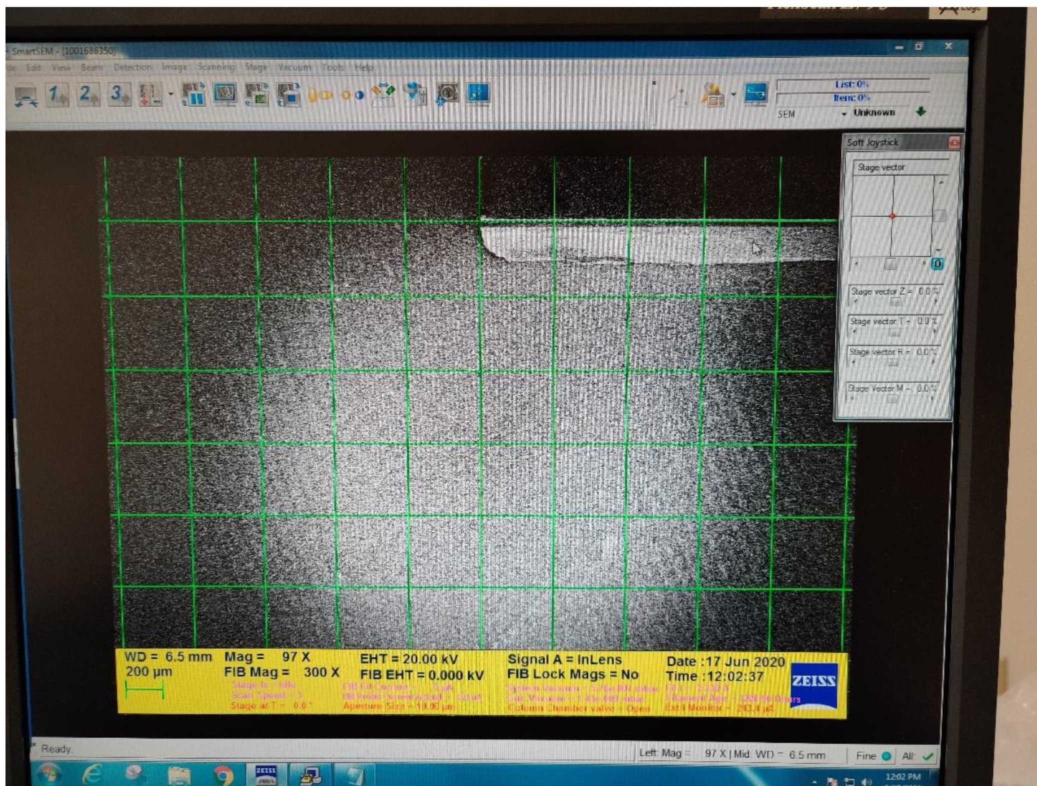
43. Save the file. Input this current value in the *.rf6 file for patterning we edited earlier in NPGS window and save and exit the file.
44. Now use the soft joystick box to move the stage to the small sample attached beside the faraday cup.
45. Pay attention to the direction of movement of the stage when using the soft joystick. This will be useful when moving along our sample edge to prevent accidental exposure.
46. Use the criss-cross marks on the attached small dummy sample and do rough focus, aperture alignment and stigmation.



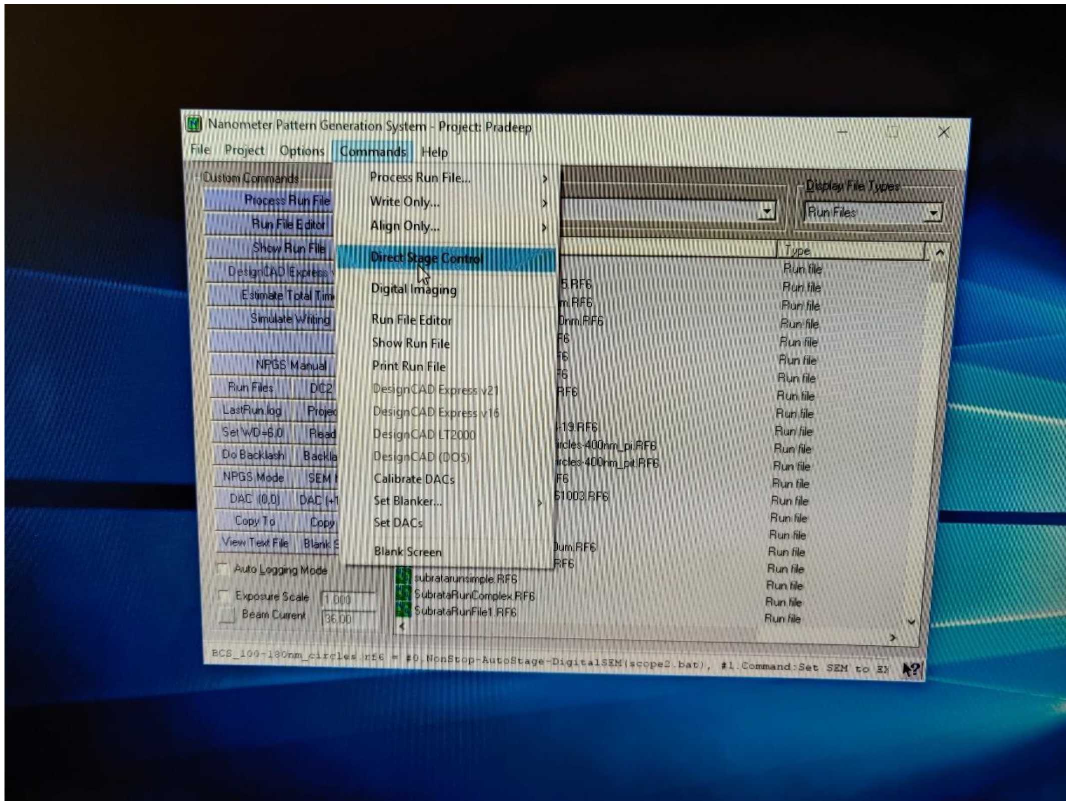
47. The dummy sample and main sample height are similar. The focus for the sample is roughly at WD = 6.0 mm. Aperture alignment is done at 30kX. We can use this value and do fine adjustments to get final focus and save time.
48. Now we use the soft joystick to move the stage slowly towards our sample edge.



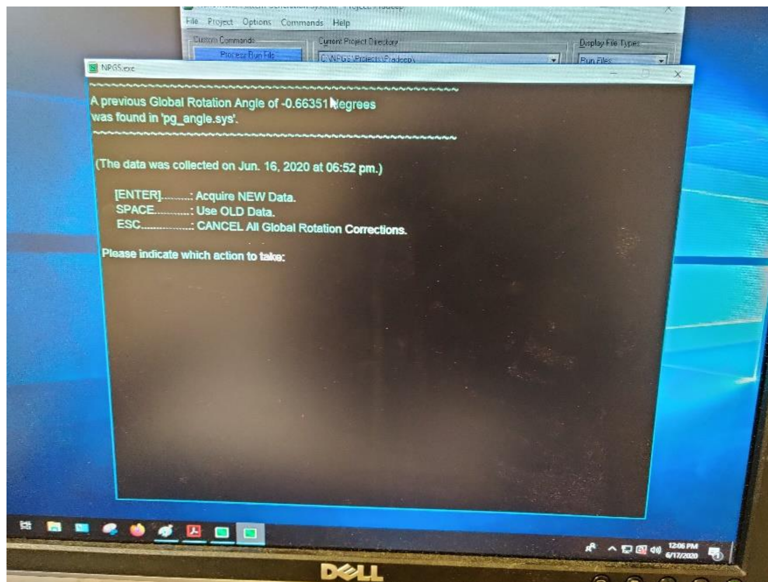
49. Once the sample edge is visible, do not move more than 1 grid inside the sample. 1 grid is roughly 300 um. This exposure should not affect our final pattern region.
50. Now using the soft joystick, slowly move along the bottom edge to the bottom left corner of the sample.



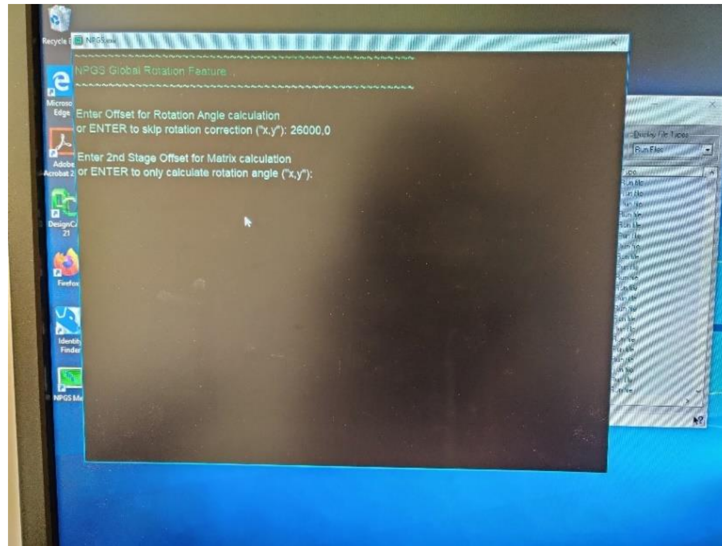
51. Align the corner and edges of the sample with the grids as shown above using the soft joystick.
52. Now, in the NPGS Window, from the Commands dropdown menu select Direct Stage Control.



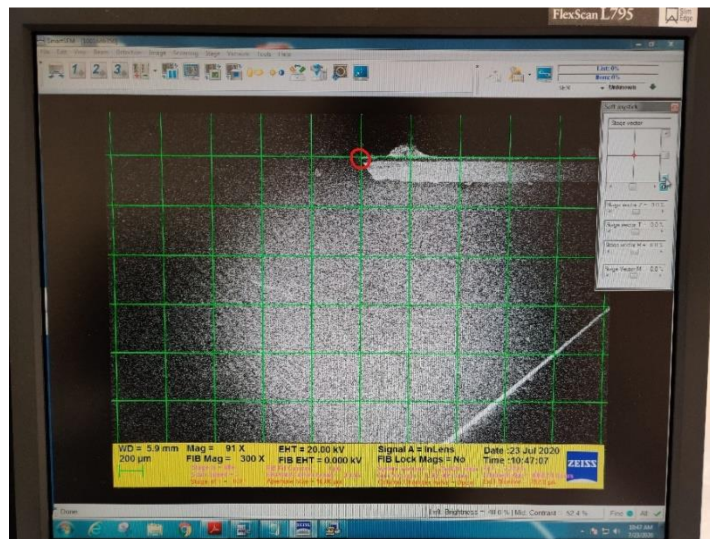
53. This opens a new window as shown below:

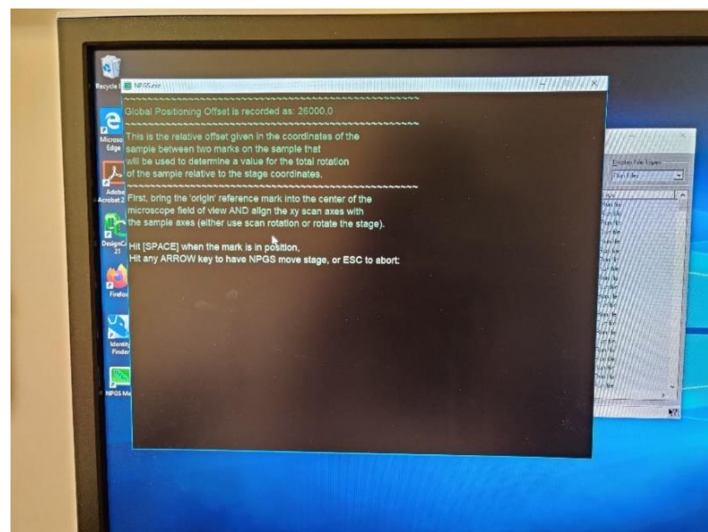


54. Press Enter to acquire new data. Then input a value slightly smaller than the sample dimension to calculate rotation angle offset. Here, 35000 um puts us within the sample boundary. Press Enter. This brings up Matrix Offset calculation (We don’t require this). Press Enter again to skip Matrix offset calculation.

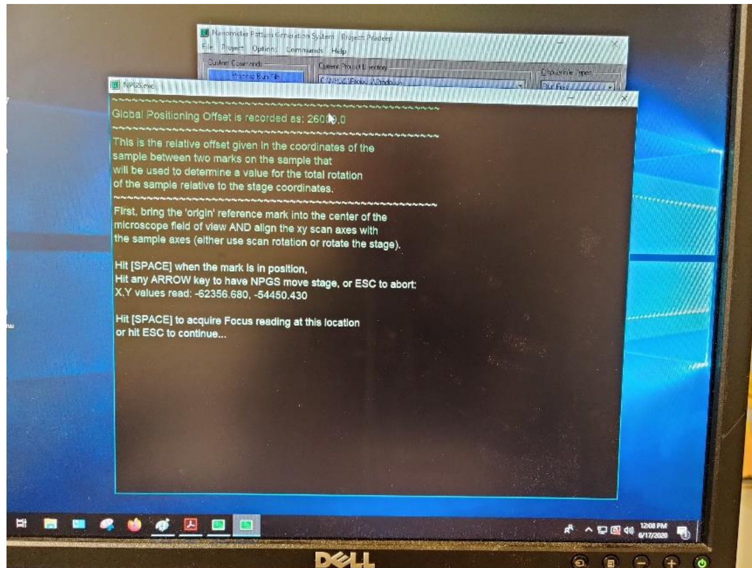


55. In the SmartSEM window, check that the grid is aligned with the sample edges.

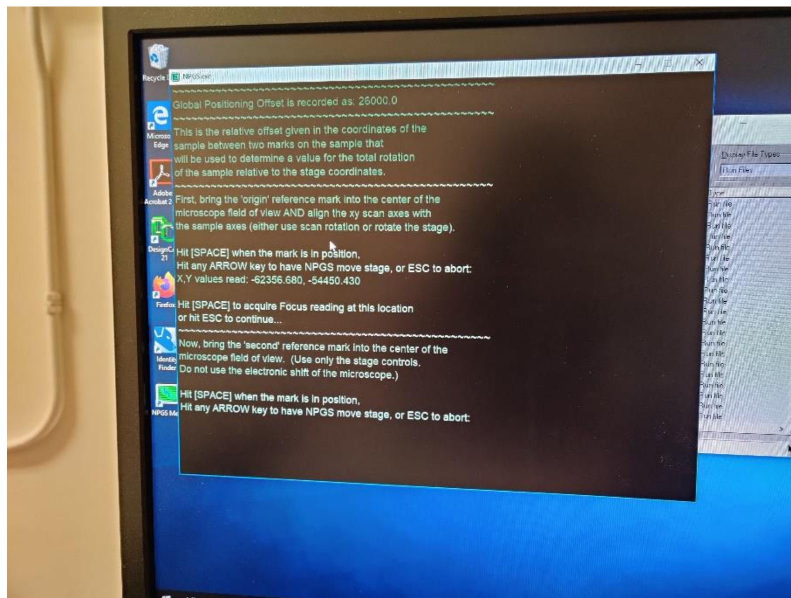




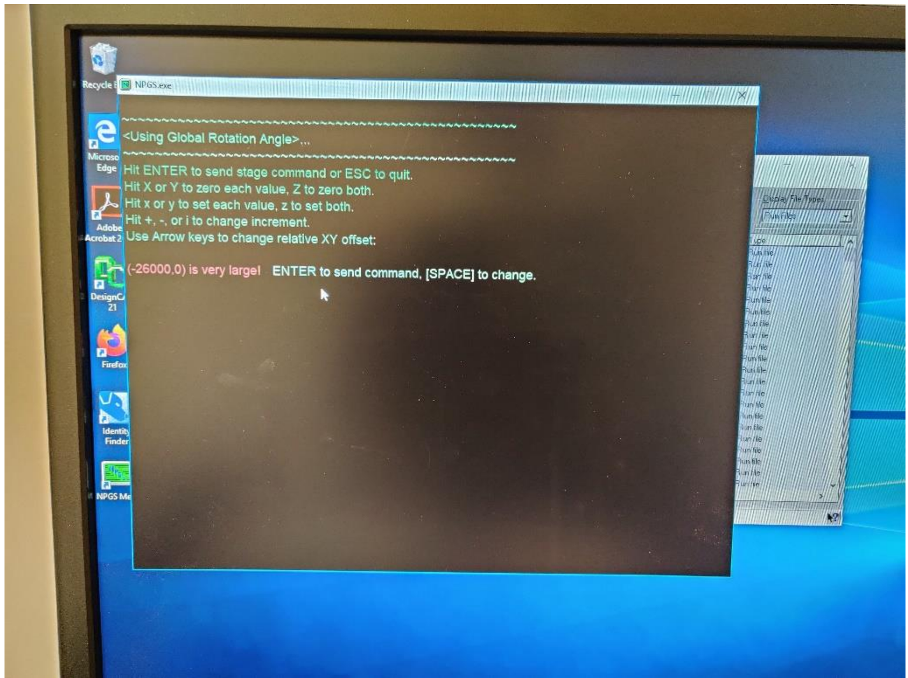
56. Hit [Space] to input this coordinate.



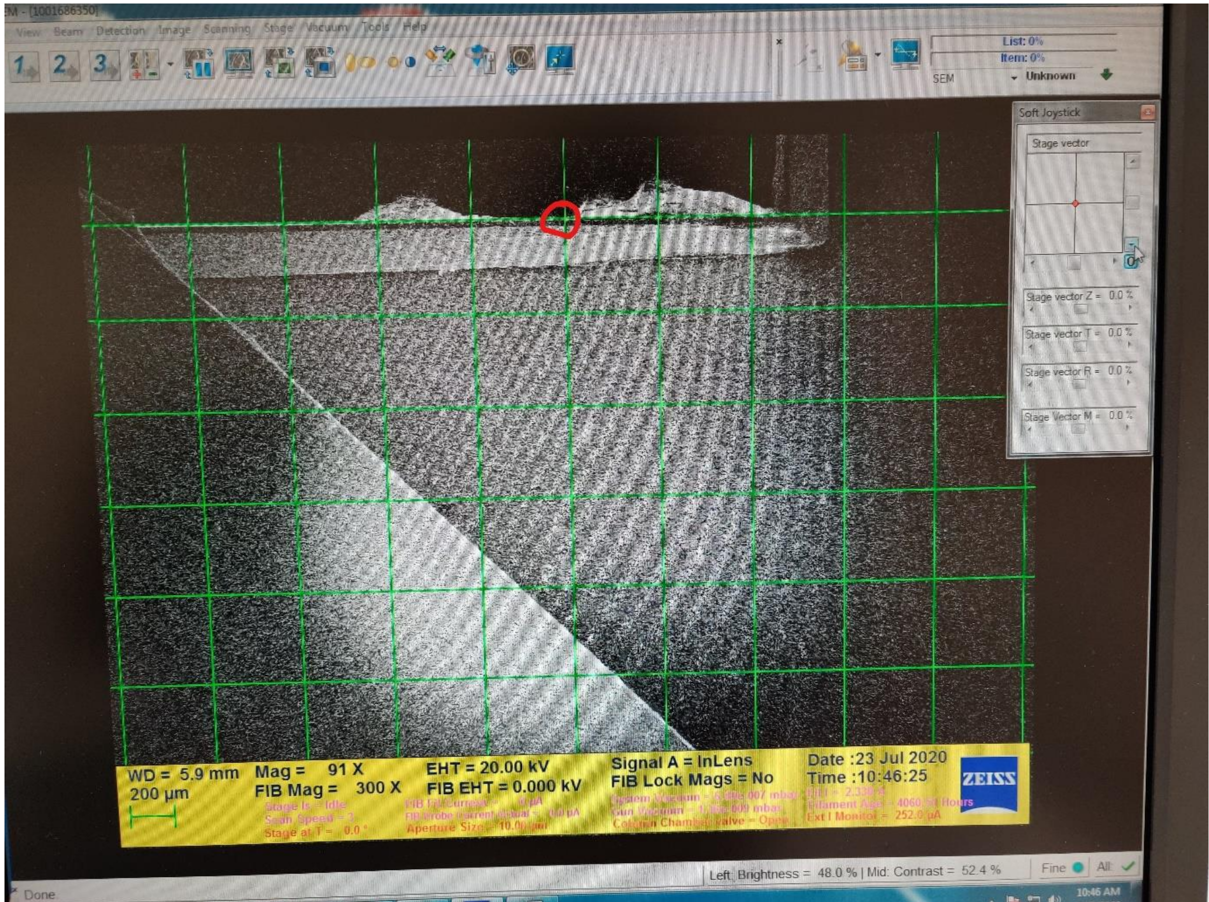
57. Press Esc to skip Focus adjustment for now (We will focus later).



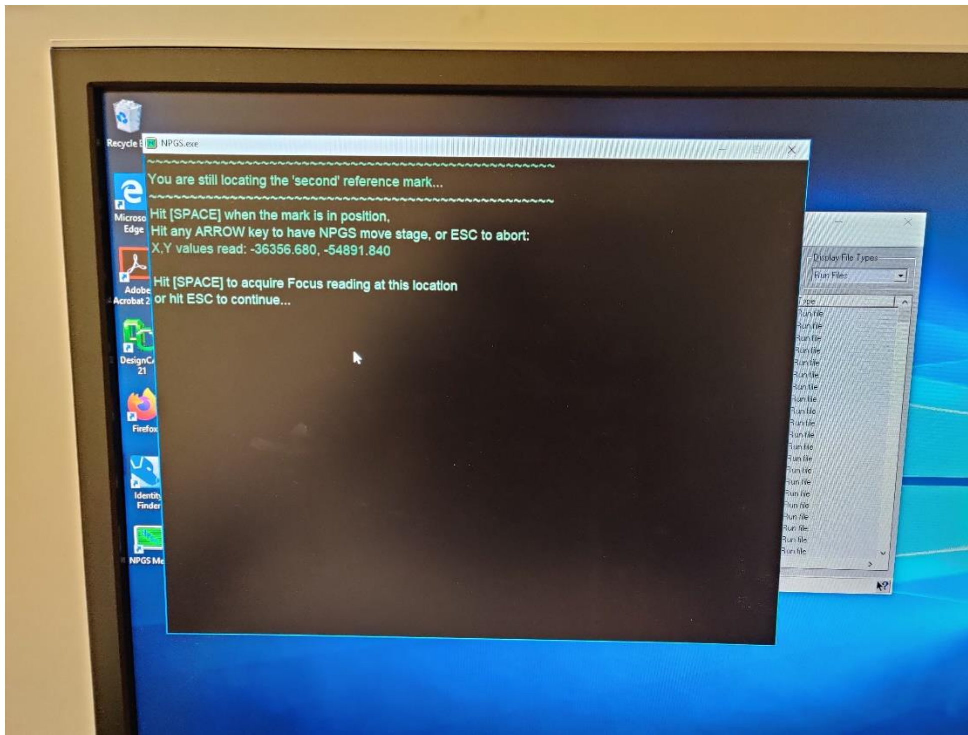
58. Press the arrow keys to input stage movement command. Input X: 35000.0 um, Y: 0.0 um and press enter. Press Enter again to move the stage.



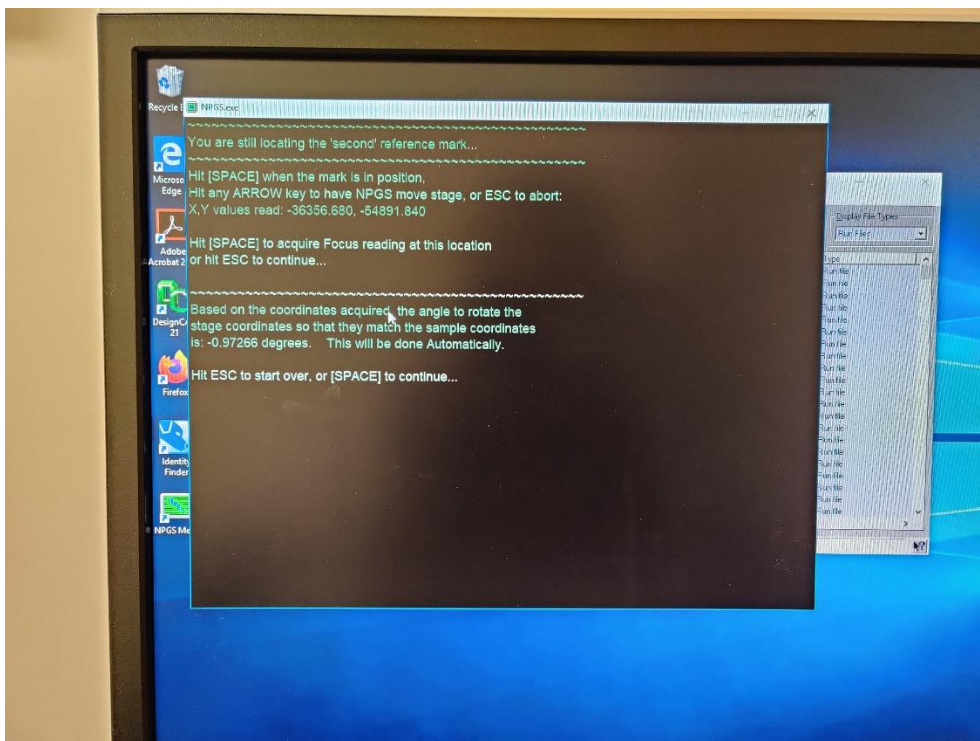
59. In the SmartSEM window, adjust the stage using the soft joystick. Align the sample edge with the 1st horizontal grid line. Use only the Y axis movement. Do not move in X direction.



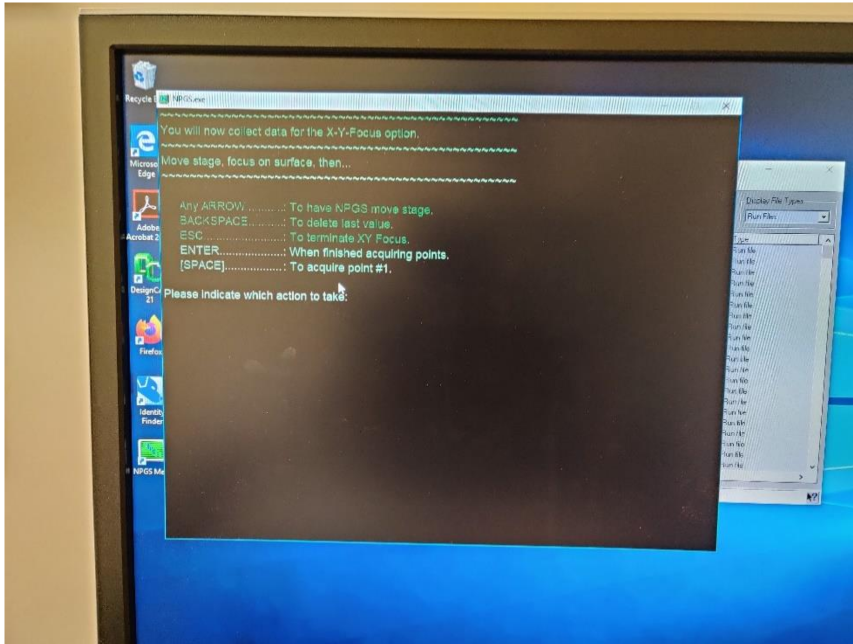
60. In the NPGS window, Hit Space when the sample edge is perfectly aligned with the 1st horizontal grid line.



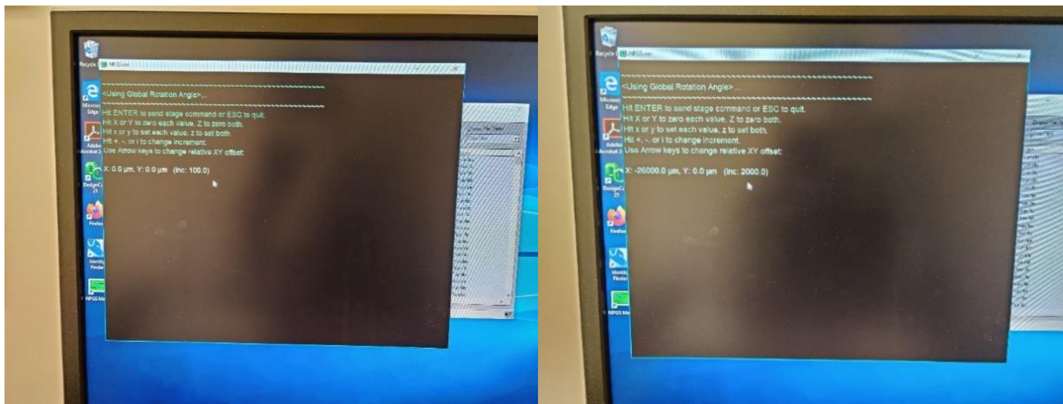
61. Press Esc to continue.

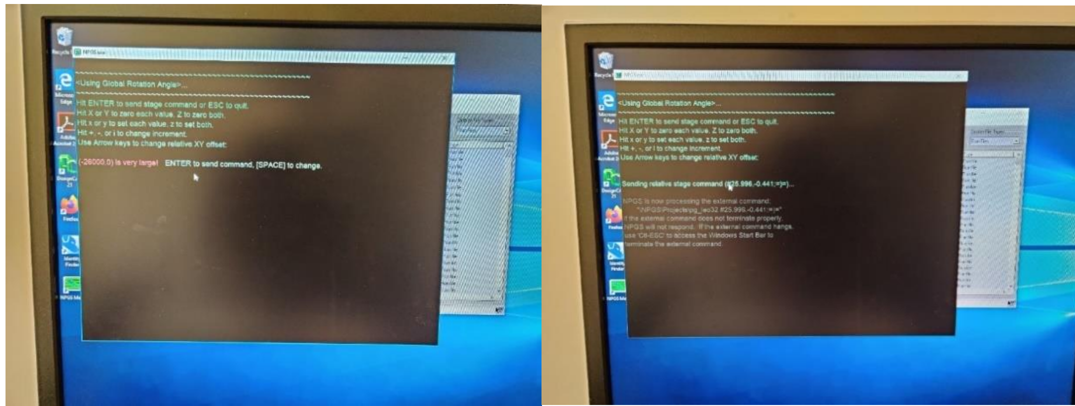


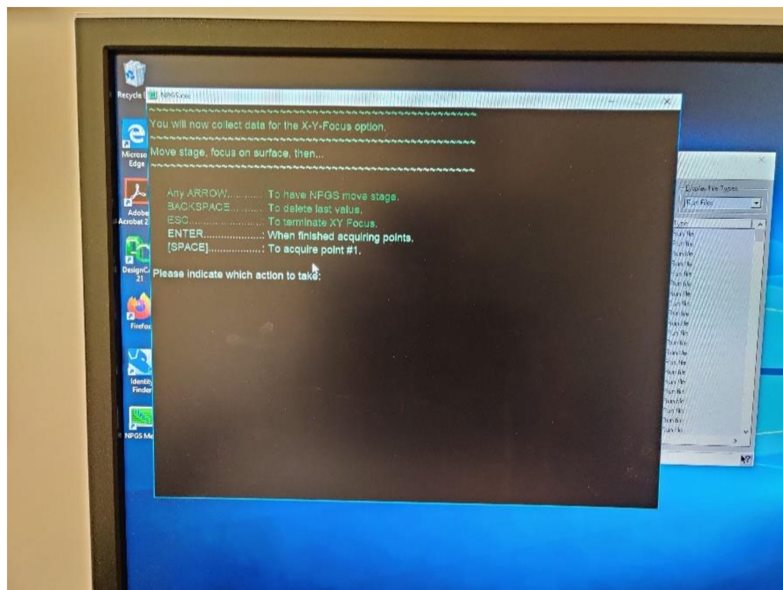
62. Angle rotation is calculated automatically. Hit [Space] to continue. This will then begin the next steps to set the focal plane. We need to acquire focus at 4 points on the sample to specify the focal plane on the sample.



63. Move the stage back to the bottom left corner using the arrow key to input stage movement command.

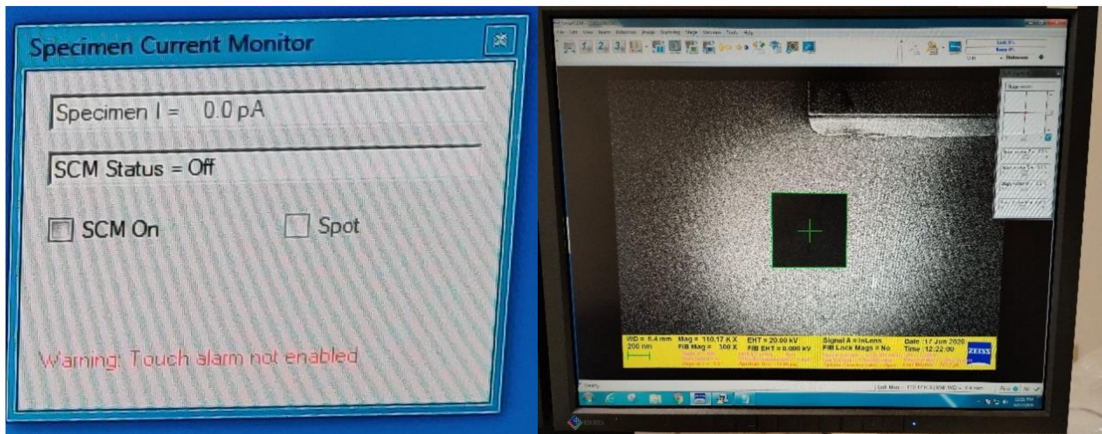






64. Follow the on-screen instructions to reach the bottom left corner of our sample. Centre on the bottom left corner of the sample. Use the reduced raster scan mode to avoid exposing large regions of sample.
65. Zoom in to 10 kX and locate the scratch mark. Zoom in to 30kX.
66. Find a debris near the scratch mark. Zoom in to 100 kX. Make sure the debris is slightly off centre.
67. Adjust Focus and Stigmation carefully. (WD=~6.0 mm for focus and stigmation adjustment), (Brightness: 48.0 %, Contrast: 52.6 %)
68. Good focus will give sharp edges for debris. Move slightly away from debris at magnification >100kX. Burn spot for >30s.
69. Turn on the Spot Mode to burn a spot.

70. Burn time will vary depending on chamber contamination.



71. Wait for ~30s and turn Off spot mode.

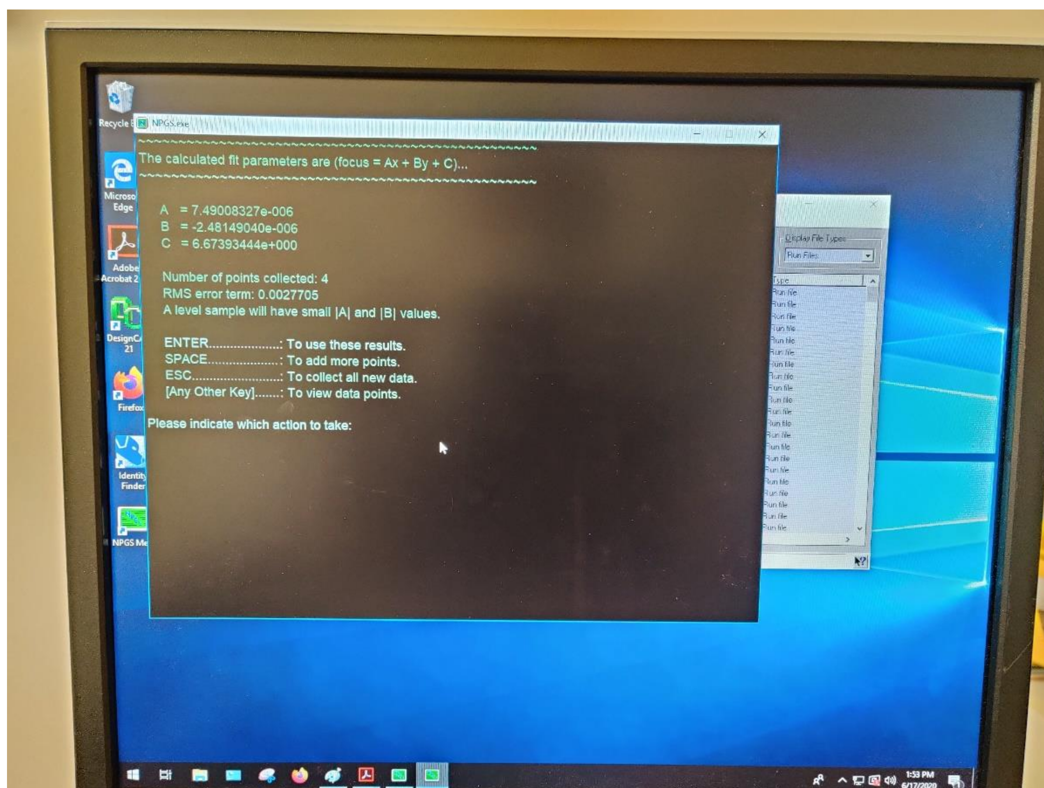
72. Spot visibility depends on chamber contamination. If contamination is high spot will be visible after 5s burn. Else longer burn time will be required.

73. Spot shape depends on Stigmation. If stigmation was good, spot will look circular in shape. If spot is elongated or any other shape, Re-adjust stigmation at debris and burn spot again to confirm.

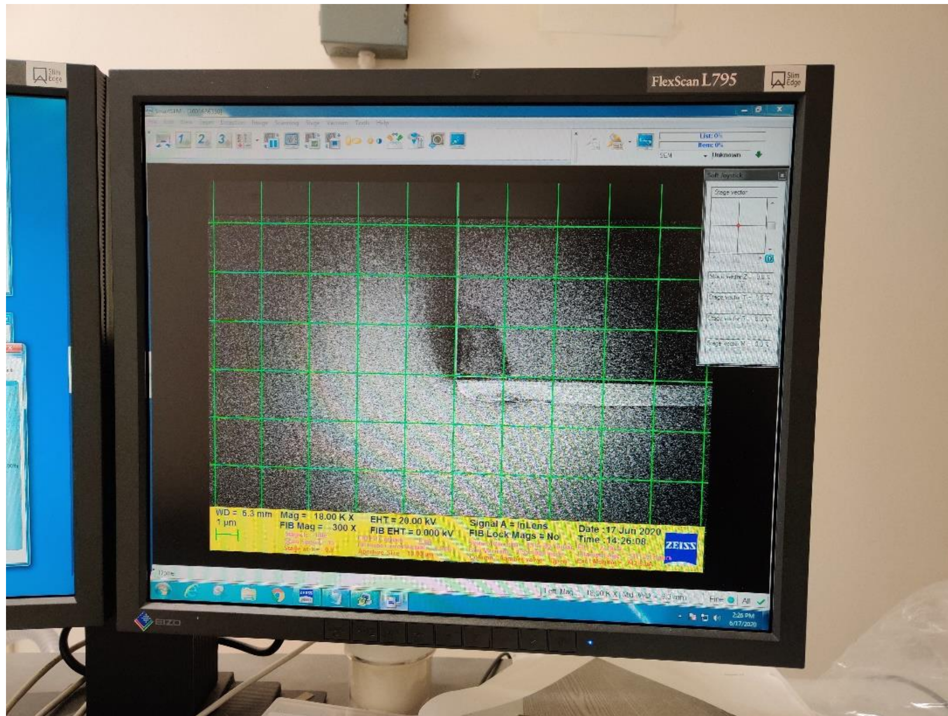
74. Also, spot diameter is dependent on magnification at which spot was burnt. Ex. 100kX will give 60nm diameter, 300kX will give 25nm diameter, etc.

75. After confirming stigmation is good, Press [Space] to accept point number 1 in the Direct Stage Control Window.

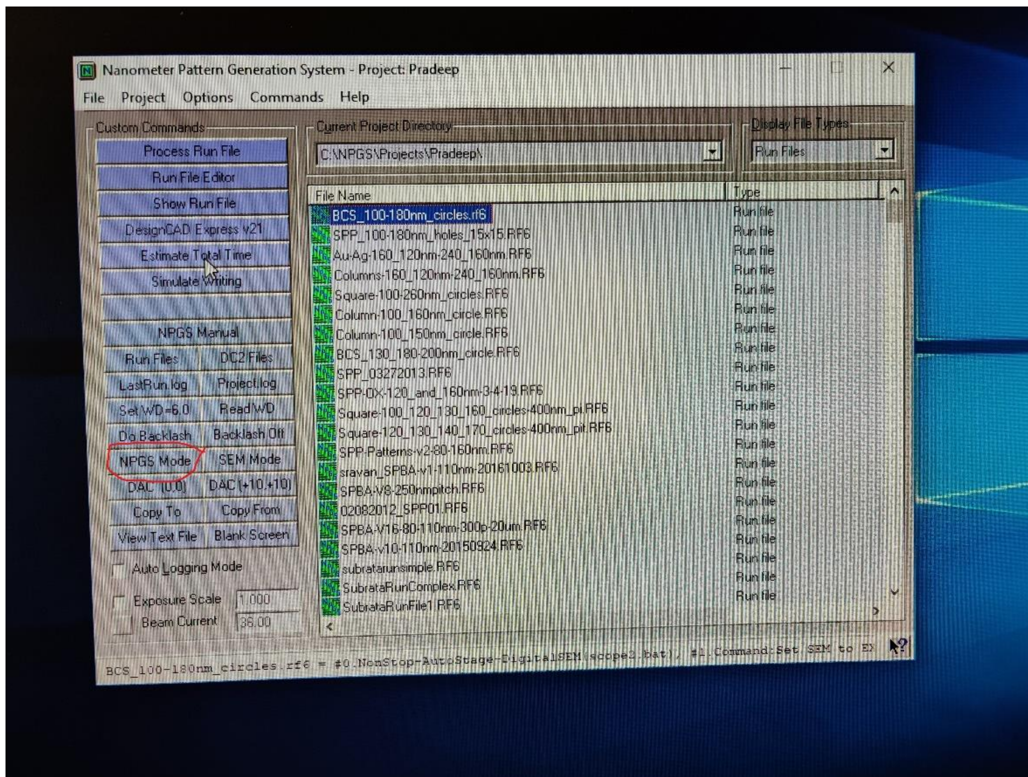
76. Now blank the beam and move the stage using arrow key by X: ****um, Y: ****um. This will bring the stage close to the bottom right corner of the sample. This will move the stage to accept the 2nd point.
77. Find debris near scratch and adjust Focus (>100kX) and accept point.
78. Move to the top right corner, find debris, adjust focus and accept point.
79. Move to the top left corner, find debris, adjust focus and accept point.
80. Once all focus points are accepted, press Enter to complete Focus plane calculation.



81. Blank the beam and move stage to the bottom left corner of the sample. Centre on the corner and zoom in to 18kX.



82. In the NPGS window, Click on NPGS Mode.



83. Right Click on the rf6 file we edited earlier and select Process Run File. Hit [Space] twice. This starts the Patterning. The e-beam pattern takes approximately 90 minutes to write on 20 samples

84. Once the writing is done the beam automatically moves to the top right corner of the sample as we specified earlier in the rf6 file and the EHT is shut down.
85. Now, we unload the sample and develop it.

Troubleshooting Issue with Pattern getting stuck:

Problem: After selecting process run file, the patterning gets stuck at pattern 1 and doesn’t proceed.

Solution:

1. Open task manager and end the 2nd and 3rd NPGS applications.
2. Open Projects folder in NPGS folder and go to Pradeep Folder.
3. Find 2 temporary run files starting with %.
4. Delete both files.
5. Restart the computer. Check to see if the files are deleted. If not, delete them again.
6. Go to command menu and select Calibrate DAC option.
7. Process Run file. Wait till the patterning starts. If the patterning is stuck, repeat the previous steps and load an older run file and modify with required pattern files.

Development

The sample is developed using a e-beam photoresist developer maD-525 solution. The sample is immersed in the maD-525 solution for 25 seconds with gentle shaking. The shaking needs to by very gently in order to avoid damaging the patterned photoresist pillars present on the sample.

3.2.9 AJA E-beam evaporation for Metal deposition to form hole pattern

The next step is to deposit thin layers of 3nm Cr and 5nm of Au using e-beam evaporation process to print the hole array pattern on the samples.

the sample is fixed on the sample holder using clamps and loaded into the load-lock chamber. The load-lock chamber is pumped down to $2.0*10^{-5}$ mbar. The main chamber gate is opened, and the sample holder is slowly inserted into the main chamber. The sample holder is then hooked to a stage inside the main deposition chamber, and the load-lock arm is taken out, and the main chamber gate is closed. After the pressure reaches below $5.0*10^{-6}$ mTorr the stage control and thickness monitor are turned on, and the source shutter is opened.

The material density of the material to be deposited is input into the thickness monitor to monitor the deposited thickness. The e-beam power is turned on and the current is slowly ramped up until the deposition starts. The current is ramped up to reach the optimal deposition rate on 1.0 Å/s and allowed to stabilize for 1 minute. The sample shutter is then opened, and the thickness monitor thickness is reset at the same time. The deposition rate is observed and maintained at 1.0 Å/s. The deposition parameters for the Cr deposition are as follows:

Deposition Material: Cr

Thickness: 3nm

Deposition Temperature: Room temperature

Deposition Rate: 1.0 Å/s

When the deposited thickness reaches 3nm, the source and sample shutter are closed at the same time and the e-beam current is slowly ramped down to 0. The e-beam power is then switched off. The source metal is then switched to Au. The material density and acoustic impedance are adjusted for Au film deposition. The source shutter is opened, the e-beam power is turned ON. The e-beam current is then ramped up slowly to reach deposition current. The deposition rate is stabilized at 1.0 Å/s. The substrate shutter is

opened, and the deposition process is started. The deposition parameters for Au deposition are as follows:

Deposition Material: Au

Thickness: 5nm

Deposition Temperature: Room temperature

Deposition Rate: 1.0 Å/s

The thickness monitor and the stage control are turned off. The main chamber to load-lock door is opened and the load-lock arm is inserted into the main chamber. The sample holder is lowered onto the load-lock arm and detached. The load-lock arm is withdrawn along with the sample holder. The main chamber door is closed, and the load-lock chamber is vented to atmosphere. The sample holder is taken out and the sample is removed from the sample holder.

3.2.10 Lift-off and Sample surface cleaning

After the deposition is done the sample are immersed in Acetone beaker and sonicated for 5 minutes. The sample is taken out and rinsed in IPA followed by IPA sonication for 5 minutes and IPA rinsing. The sample is then immersed in the developer solution of maD-525 for 5 minutes. The sample is then taken out and thoroughly rinsed using running DI water and blow dried with nitrogen.

The 4x5 samples are then cut into individual pieces for a total of 20 pieces of 6mm by 9mm samples. The samples are immersed in IPA and then sonicated in IPA for 10 minutes. The samples are taken out and blow dried with nitrogen. After the cleaning is done, the samples need to be stored in ethanol immediately after the IPA sonication.

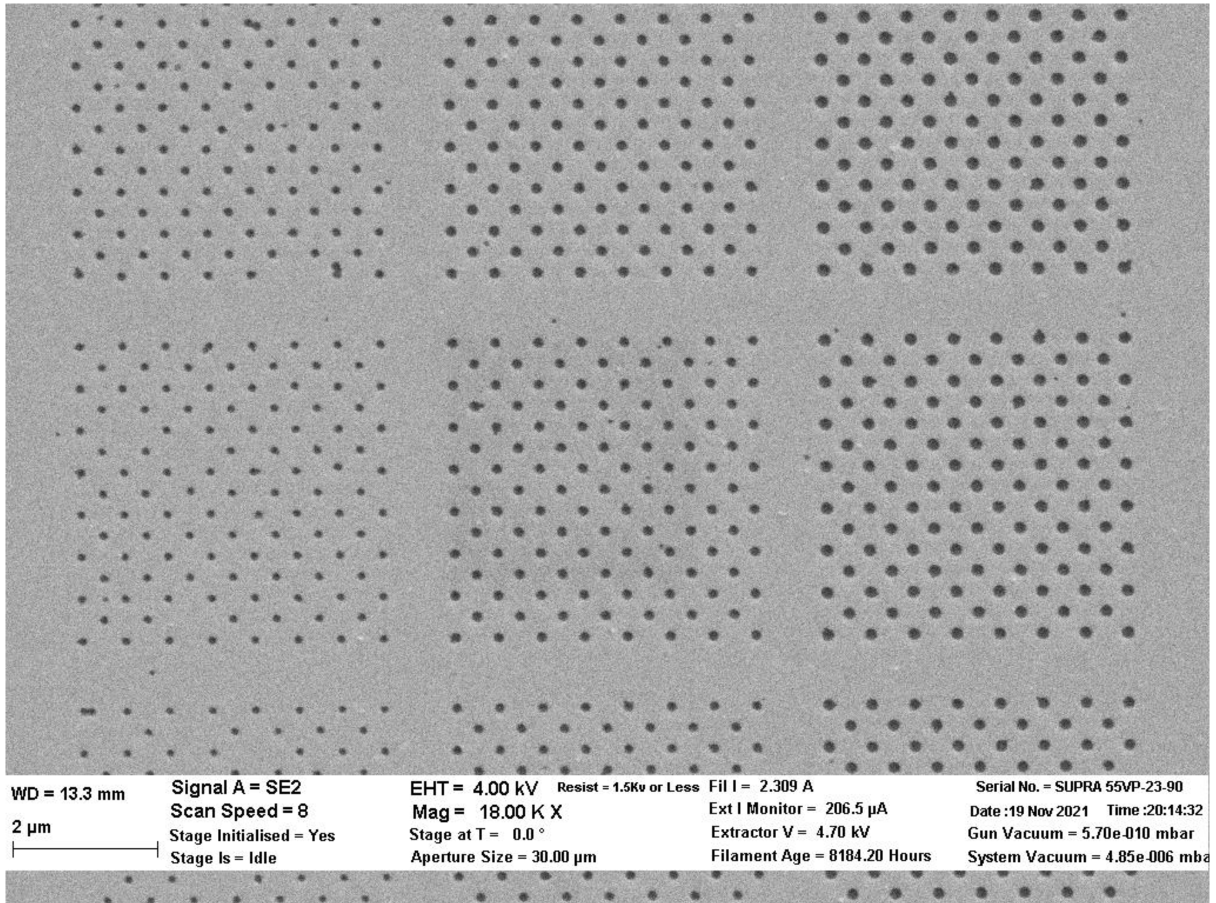


Figure 20: SEM Image showing the completed SPP pattern template containing hole arrays

3.3 Fabrication Procedure for Quantum Well-Si electron transport device

This chapter describes in detail the fabrication procedure for quantum-well mediated electron transport device to achieve cold electron transport at room temperature. In this chapter we also discuss the problems encountered during fabrication and the solutions used to solve these issues like moisture formation due to Peltier effect, wet etching and reactive etching thickness control. Our devices are fabricated on 4-inch p-type, p++ type and n-type, n++ type Silicon wafers. The Sample preparation utilizes fabrication processes like Thermal oxidation, Photolithography, Reactive Ion Etching, Wet Etching, Electron Beam Deposition and Sputter Deposition, etc. to complete the device and get it ready for IV characterization. The complete fabrication process is carried out in a class-100 cleanroom facility at the Nanofab Research Centre at The University of Texas at Arlington. The following chapters discuss stepwise in detail the fabrication procedure.

3.3.1 Sample Preparation

For the fabrication of cold-electron transistors, we start with 4-inch p-type and n-type Silicon wafers. The wafers need to be thoroughly cleaned prior to beginning the fabrication procedure. The wafers are immersed in a freshly prepared piranha solution, which is a mixture of sulfuric acid and hydrogen peroxide in a 3:1 ratio. We take 60 mL of Sulfuric acid in a glass beaker and add 20 mL of hydrogen peroxide to it slowly along the sides of the beaker. Precaution needs to be taken when utilizing acids by wearing full PPE equipment when handling acids. The wafers are immersed in the Piranha solution for 30 min to remove any organic impurities. The wafer is then taken out and immersed in a DI container for 5 minutes, followed by rinsing under running DI water and followed by immersion in a second DI water container for 5 minutes and then blow drying it with Nitrogen. This thorough DI water rinsing ensures that all piranha solution and residue is removed from the Silicon wafer. The Piranha cleaning step is followed by immersing the

wafer in 49% Hydrofluoric acid for 10 minutes followed by 5-minute immersion in the first DI water container, 1 minute rinsing under running DI water and then immersing it in second DI water container for 5 minutes and then blow drying it with Nitrogen.

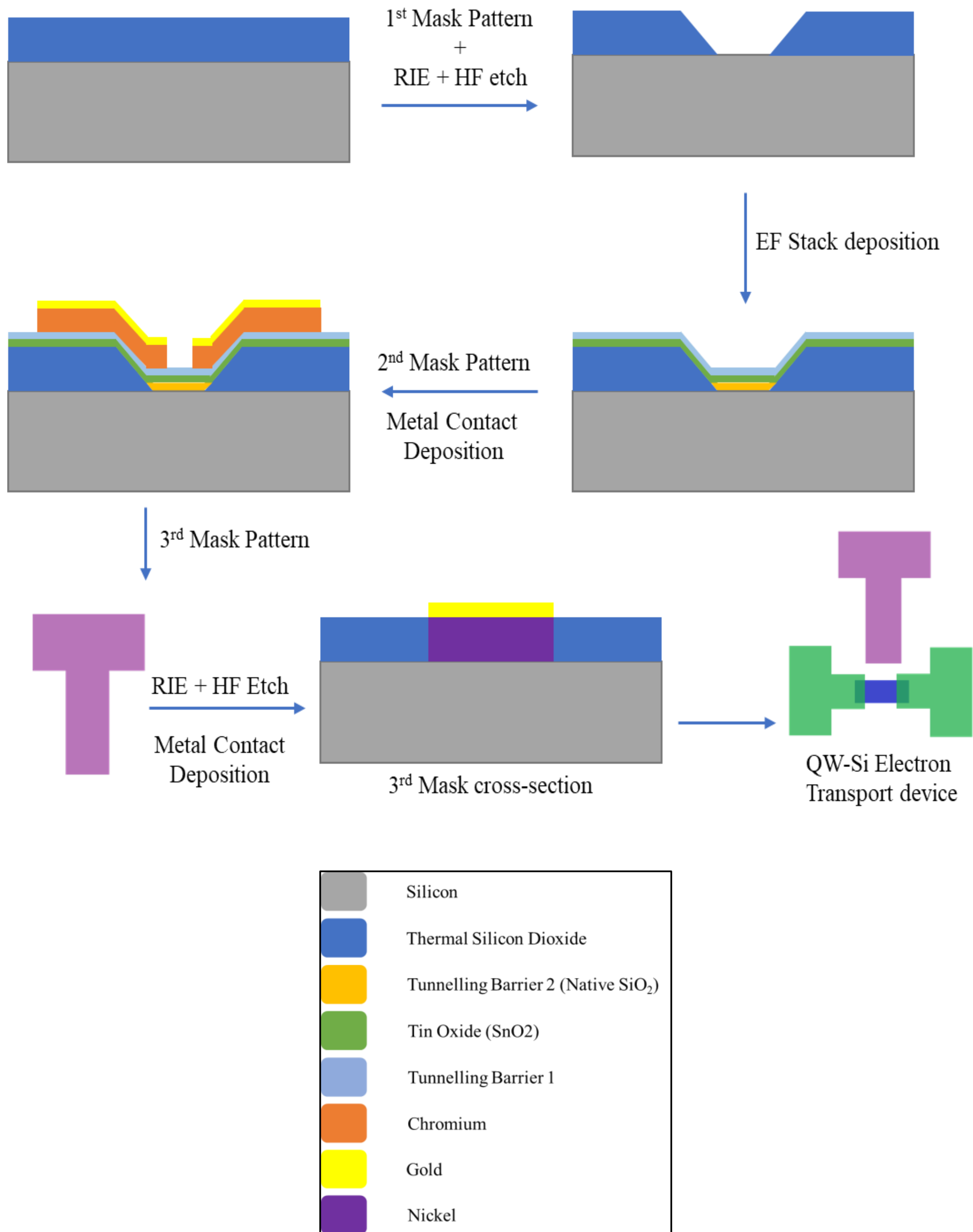


Figure 21: Process Flow Diagram showing fabrication of QW-Si Electron Transport Device (Top) and Legend (Bottom)

3.3.2 Thermal Oxidation (Passivation Layer)

After the thorough cleaning of the substrate wafers, the wafers were loaded into a thermal oxidation chamber (Tystar Oxidation Furnace) to grow a nominal thickness of 250nm of Silicon dioxide.

Figure 22: Tystar Oxidation Furnace for Thermal Oxidation of Silicon

The Silicon dioxide was grown using dry oxidation. The oxidation parameters were as follows:

Oxidation temperature: 1100 ℃

Oxidation Time: 3hrs 30 min

Oxygen flow: 3000sccm

The grown silicon dioxide thickness is measured using Nanospec at the centre and 4 quadrant regions to confirm the film thickness and uniformity. The 250nm thermal silicon dioxide is required as a passivation layer and a mask in order to leave a good margin for printing the silicon window pattern during the First Mask step which is explained in the next subsection.

3.3.3 First Mask Lithography

The 250nm Silicon dioxide grown Si wafer is cut into four quadrants in preparation to print the First mask pattern to expose silicon surface and create a silicon window. The entire first mask lithography procedure is detailed in the subsections below.

3.3.3.1 Photolithography for Silicon Window Pattern Exposure

Each of the quadrants is spin-coated with a negative photoresist – NR9-1000PY. The Negative photoresist is coated on the sample quadrant by using a dropper to cover the entire surface and then spin-coated. The spin-coating parameters are as follows:

Step 1:

500 rpm; 100 rpm/s; 5 seconds

Step 2:

3000 rpm; 1000rpm/s; 60 seconds

Step 3:

0 rpm; 1000rpm/s; 0.1 seconds

The spin-coated sample is then pre-baked at 150 °C for 1 minute on a hot plate. The samples are now ready for photolithography pattern exposure.

The photolithography mask is designed in such a way that it is divided into four quadrants, with each quadrant containing a pattern for the first, second, third and fourth mask patterns respectively. The photolithography mask is loaded onto the OAI Aligner with the First Mask pattern in the top right section. The substrate carrier wafer is loaded beneath the photolithography mask.

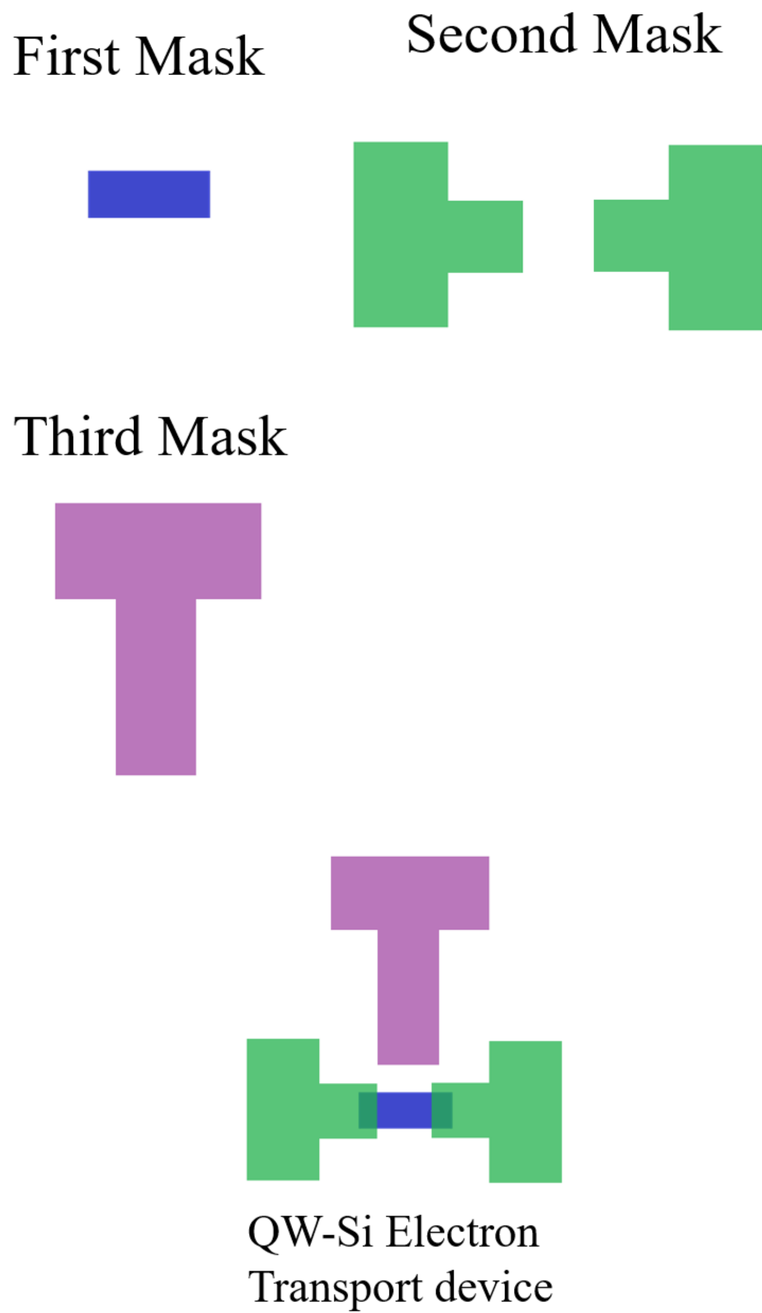


Figure 23: First mask to third Mask Patterns for the QW-Si Electron transport device

The sample quadrant is fixed on the substrate carrier wafer beneath the first mask pattern. The quadrant and mask are aligned such that the entire first mask pattern is aligned within the sample quadrant. The first mask is pressed on to the sample quadrant and contact vacuum is turned on and the pattern exposure is carried out.

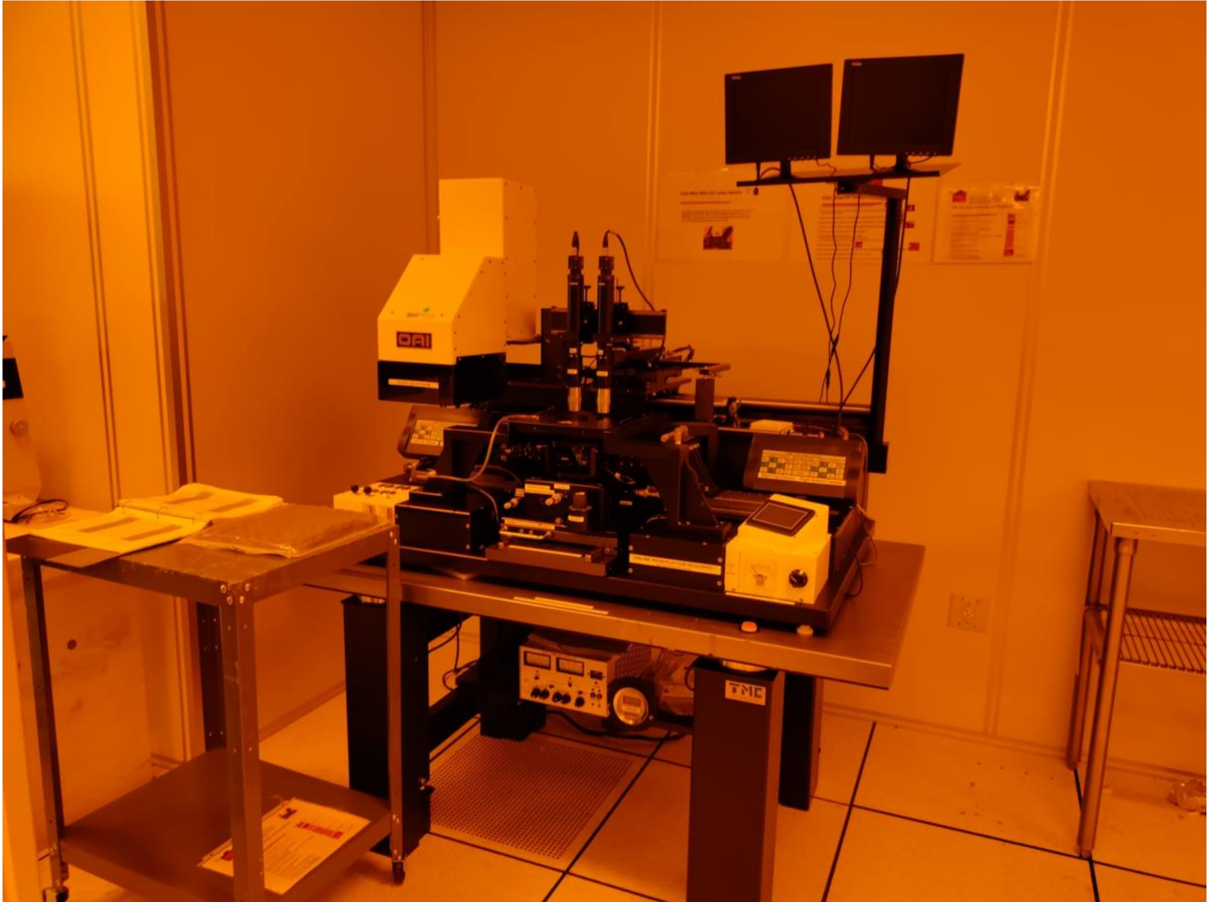


Figure 24: OAI Aligner Equipment for UV Photolithography

The photolithography patterning parameters are as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 19.6 mW/cm^2

Exposure Time: 6.1 seconds

Dose: 120 mJ/cm^2

The Exposure time is adjusted based on measured Intensity so that the final dose is 120mJ/m^2. After exposure, the sample quadrant is then post baked at 100 °C on a hot plate for 1minute. The sample is allowed to cool down to room temperature. The sample is then developed in a photoresist developer – RD6. The sample is immersed in the developer - RD6 for 25 seconds with regular shaking (development time increased from 10s to 25 seconds due to observed resist residue in SEM after lift-off process) followed by DI water immersion in beaker 1 for 5 minutes with regular agitation and then in DI water beaker 2 for 5 minutes. The sample is then gently blow dried with nitrogen.

3.3.3.2 Silicon Dioxide etching using Reactive Ion Etching

The next step is to expose the Silicon surface inside the pattern area. This region will be used to deposit the energy filtering layer stack. Thus, the silicon in the pattern area will need to be exposed. The silicon dioxide present in the window pattern is etched using reactive ion etching in the Technics Macro RIE – 8800 equipment. A margin of 40nm silicon dioxide is left behind after the RIE to protect the silicon surface from the RIE plasma. The RIE etch step with a 40nm margin creates an uneven circular region at the centre of the wafer quadrant resulting in a difference in SiO2 thickness of ~10nm at the centre region and the side region of the quadrant.

Figure 25: Technics Macro RIE – 8800 equipment for Reactive Ion Etching

We found that increasing the SiO2 etch margin to 80 nm reduces this variation to ~1-3 nanometres. Thus, the SiO2 RIE etch recipe was adjusted to leave 80 nm SiO2 margin. The Silicon dioxide etching is separated into 2 stages with an oxygen clean step after each Silicon dioxide etch step. The silicon dioxide etch time is established by optimizing the etch rate by etching for different times using the CF4/O2 etch recipe. The different etch times and etch thicknesses are plotted and the etch rate for Silicon dioxide is calculated to be 0.7 nm/s.

The Reactive Ion Etching Parameters are as follows:

Step 1: 600W, 170mT, CF_4: 30 sccm, O_2: 7.2 sccm

Step 2: 350W, 200mT, O_2: 11.0 sccm, 300s

Step 3: 600W, 170mT, CF_4: 30 sccm, O_2: 7.2 sccm

Step 4: 350W, 200mT, O_2: 11.0 sccm, 300s

Once the RIE etching is done, the photoresist from the sample needs to be removed and measure the actual etched thickness.

3.3.3.3 Lift-off for Photoresist removal

The sample is immersed in Acetone and sonicated for 15 minutes, followed by rinsing in IPA (IPA rinse is done after acetone to avoid acetone residue left behind if the acetone dries on the sample surface). The sample is then immersed in IPA and sonicated for 15 minutes, then rinsed in IPA and gently blow dried with nitrogen. It was observed under SEM imaging that the RIE Etching leaves behind the redeposited resist residue in the window area. This residue should be able to be removed by additional oxygen plasma cleaning step in the Reactive Ion Etching. The samples were subjected to an additional 10minutes, 20 minutes and 30 minutes of oxygen plasma RIE step. It was observed that the samples with the 10minutes and 20 minutes still had some residue left. The 30-minute oxygen clean recipe was able to remove all the residue present in and near the window area.

The sample Silicon dioxide thickness profile is then measured using a profilometer (KLA Tencor-P6 Profilometer). The profile height and initial silicon dioxide thickness measurement difference should be close to 80nm. Then we can proceed to the next step in the fabrication process.

3.3.4 Wet Etching and Tunneling Barrier 2

Now that there is a 80 nm margin of silicon dioxide left in the window area, the silicon window needs to be exposed. As Reactive ion etching may damage the silicon surface if the plasma hits the silicon, wet etching of silicon dioxide is done to remove the final 80nm of silicon dioxide remaining in the window region. The nominal etch remaining thickness after wet etching needs to be 60nm. This allows for a decent contrast for the next photolithography step for alignment. The sample is immersed in freshly prepared hydrofluoric Acid and etching is done in multiple steps to avoid over etching. After immersion in hydrofluoric acid, the sample sis then taken out and immersed in DI water beaker 1 for 5 minutes with vigorous shaking followed by regular shaking. It is then transferred to a second DI water for 5 minutes with regular shaking. The sample is then rinsed under running DI water for 1 minute. This thorough DI water rinsing is done to remove all the hydrofluoric residue present on the sample surface. Once the silicon dioxide in the window region is removed and the silicon is exposed, the sample is left in air overnight to allow for the formation of a native silicon dioxide layer (Tunneling Barrier 2).

3.3.5 Third Mask Lithography

Once the silicon window is protected by the native silicon dioxide layer, we can now proceed to create a silicon contact for the Quantum Well-silicon electron transport device. The first step is to pattern the Silicon contact pad area using photolithography.

3.3.5.1 Photolithography for Silicon contact pads (with slight shifting)

The sample quadrant is spin-coated with a negative photoresist – NR9-1000PY. The photoresist is coated on the sample using a dropper to cover the entire surface and then spin-coated using the following parameters:

Step 1:

500 rpm; 100 rpm/s; 5 seconds

Step 2:

3000 rpm; 1000rpm/s; 60 seconds

Step 3:

0 rpm; 1000rpm/s; 0.1 seconds

After the spin-coating is done the sample quadrant is pre-baked on a hot plate at 150˚C for 1 minute and then allowed to cool down on a cooling plate.

The Third Mask Pattern from the Alignment mask is used for the Silicon contact pad patterning and is loaded on to the OAI Aligner. The substrate carrier wafer is loaded beneath the Mask inside the OAI Aligner and the sample quadrant is fixed on the substrate carrier wafer using scotch tape at the base of the sample. The Third mask pattern is aligned using the first mask L shaped alignment marks at the corners of the sample and then the mask is shifted slightly upwards so that the third mask pattern does not overlap with the first mask silicon window pattern present on the sample. Once the third mask is aligned with the corner L shaped alignment marks, the third mask is pressed on to the sample and the pattern is exposed after contact vacuum is turned on. The photolithography pattern parameters are as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 19.6 mW/cm^2

Exposure Time: 6.1 seconds

Dose: 120 mJ/cm^2

After the exposure is done the sample quadrant is taken out and post-baked on a hot plate at 100˚C for 1 minute. The sample quadrant is then placed on a cooling plate and allowed to cool down to room temperature. After the sample quadrant cools down, the sample is immersed in a developer solution RD6 for 25 seconds with vigorous shaking to remove the unexposed regions of the photoresist. The sample is then immersed in DI water container for 5 minutes with regular stirring, then moved to a second DI water container for 5 minutes with regular stirring. The sample is then taken out and blow dried in nitrogen, leaving behind the third mask pattern on the photoresist coating on the sample.

3.3.5.2 Reactive Ion Etching to etch Silicon dioxide

Now we need to etch the silicon dioxide present in the third mask pattern region to expose the silicon surface for metal deposition. However, we need to leave a margin of 10 nm silicon dioxide to protect the silicon surface from the reactive ion etching in order to prevent contamination of the surface. Thus, leaving a margin of 10 nm silicon dioxide we etch the remaining silicon dioxide using the following parameters during the reactive ion etch process:

Step 1:

600W, 170mT, CF_4: 30 sccm, O_2: 7.2 sccm

Step 2:

350W, 200mT, O_2: 11.0 sccm, Etch time: 30 seconds

The etch time for the CF_4 / O_2 etch step is calculated based on the etch rate calculated previously. The etch time will be calculated as follows:

Etch time = (Initial thickness – 10nm) / 0.7nm/s

3.3.5.3 Lift-off

After the Reactive Ion Etching is done, the sample quadrant is unloaded from the Technics RIE-3300 equipment. The photoresist needs to be removed using a lift-off process. The sample quadrant is immersed in Acetone and sonicated for 5 minutes followed by a 30 second IPA rinse. The sample is then immersed in IPA and sonicated for 5 minutes, again followed by an IPA rinse for 30 seconds. It is then blow dried in Nitrogen. The Sonication steps are listed below:

Step 1: Acetone Sonication (5 minutes) + IPA Rinse (30 seconds)

Step 2: IPA Sonication + IPA Rinse (30 seconds)

Step 3: Nitrogen Blow dry

The sample quadrant is cut into 3 samples namely – A, B and C. Each sample remaining SiO_2 thickness is measured using P6 – Profilometer. Nominally, there should be 5nm -10 nm silicon dioxide remaining in the third mask pattern area. Next, we need to remove this remaining silicon dioxide and expose the silicon surface beneath in the third mask region.

3.3.5.4 Photolithography mask for wet etching (with slight shifting)

The samples are then spin-coated again with negative photoresist – NR9-1000PY. The spin coating parameters are as follows:

Step 1:

500 rpm; 100 rpm/s; 5 seconds

Step 2:

3000 rpm; 1000rpm/s; 60 seconds

Step 3:

0 rpm; 1000rpm/s; 0.1 seconds

After the spin coating is done, the samples are pre-baked at 150°C for 1 minute on a hot plate. The samples are loaded into the OAI Aligner for third mask alignment to pattern the third mask pattern over the previous third mask pattern on the sample. The sample is fixed on the carrier wafer beneath the Mask. The Mask is aligned with the sample such that the third mask pattern overlaps with the previous third mask pattern on the sample and the contact vacuum is turned on. The UV exposure is done with the following parameters:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 19.6 mW/cm^2

Exposure Time: 6.1 seconds

Dose: 120 mJ/cm^2

After the UV exposure, the sample is unloaded and post-baked at 100°C for 1 minute on a hot plate. The sample is then allowed to cool down to room temperature on a cooling plate. The sample is immersed in a developer solution of RD6 for 25 seconds with vigorous shaking and then immersed into the first DI water container for 5minutes with regular stirring followed by immersion into the second DI water container for 5 minutes with regular stirring. The sample is then taken out and blow dried with Nitrogen until the sample is completely dry. This step removes the photoresist from the third mask area and exposes the 5nm-10nm remaining silicon dioxide present after the reactive ion etch process.

3.3.5.5 Wet Etching of Silicon Dioxide

Now, we need to remove the remaining silicon dioxide present in the third mask pattern area. The photoresist patterned sample is then immersed into a Hydrofluoric acid solution

with 10:1 strength for 20 seconds. The immersion time should not exceed 25 seconds as the photoresists starts cracking close to 30 seconds. After the 20 second immersion in hydrofluoric acid (10:1), the remaining silicon dioxide should have been removed. This can be confirmed by measuring the contact current using the I-V probe station (Agilent 4155C). The silicon contact current should be linear and in the range of 0.1-0.7 μA. If the current is lower and not linear, then the photoresist needs to be removed by Acetone and IPA sonication for 5 minutes each and then nitrogen blow dry, and then followed by the third mask and hydrofluoric acid etch steps again. Once the contact current for the exposed surface is in the 0.1-0.7 μA range, we proceed to the next step of deposition of metal contact pad.

Figure 26: Homebuilt Sputter deposition equipment for DC and RF Sputter deposition

3.3.5.6 Silicon Contact Metal Pad deposition

Now we need to deposit Metal contact pad in the etched region where silicon surface is exposed. The samples are loaded into a homebuilt sputter deposition tool for Aluminium deposition.

We deposit Aluminium using RF sputtering. The deposition parameters for Al deposition are as follows:

Pressure: 4mT

Power: 200W

Ar: 35sccm

Deposition Thickness: 200nm

Deposition Time: 261 seconds

3.3.5.7 Lift-off

After deposition is done, the samples are taken out and immersed in acetone and sonicated for 5 minutes followed by IPA rinsing. It is then immersed in IPA and sonicated for 5 minutes followed by IPA rinsing and blow dried with nitrogen.

3.3.5.8 Ohmic Contact: RTA Heating

The samples are then loaded into the RTA chamber and heated at 550°C for 1 minute. The samples are taken out and the silicon to silicon IV is measured from one Aluminium metal contact pad to an adjacent Aluminium metal contact pad using the IV probe station (Agilent 4155C) equipment. If the current is linear and in the range of milli Amperes, we can proceed to the next step. If the current is lower and is not linear, the samples are loaded back into the RTA chamber and heated for at 400°C for 1 hr. The silicon-to-silicon current

is measured again. The current is measured again using IV probe-station and should be linear and in mA range. This indicates that the Al-Si has become ohmic contact.

3.3.6 Energy Filtering Stack Formation

The next step is now to deposit the energy filter stack on top of the first mask silicon window. The Energy filter stack consists of 3 layers:

Tunneling Barrier 2: Native Silicon Dioxide

Energy Filter: Quantum Well Layer

Tunneling Barrier 1: Silicon Nitride or Aluminium Oxide

The first mask window region already has the first layer of the energy filter stack: the native silicon dioxide film which was grown in section 3.2.4 before the third mask step.

3.3.5.2 Quantum Well Layer Deposition

The middle layer in the Energy filter stack is the quantum well formation. Different materials were used for the formation of quantum well layer: Cr_2O_3 and SnO_2. We found that the tin oxide quantum well layers showed the best results. The thin tin Oxide deposition was done using AJA Sputter deposition equipment. The tin oxide deposition rate was determined by depositing a nominal 600 seconds with the following conditions:

SnO_2 Spark step 1:

Ignition Pressure: 35 mTorr

Power: 40 W

Ar: 30 sccm

Temperature: Room Temperature

Coat Time: 2 seconds (Plasma ignition)

SnO_2 Spark step 2:

Ignition Pressure: 35 mTorr

Power: 40 W

Ar: 15 sccm; O2: 6sccm

Temperature: Room Temperature

Coat Time: 2 seconds (Plasma ignition)

2 nm SiO_2 Deposition

Power: 40 W

Deposition Pressure: 5 mTorr

Ar: 15 sccm; O_2: 6 sccm

Temperature: Room Temperature

Pre-sputter Time: 120 seconds (required for target cleaning) (Sample shutter is closed.)

Deposition Time: *** seconds

The deposition was done on a dummy sample and the deposited thickness was measured using Ocean Optics Reflectometer. The thickness was measured to be 8.28 nm with a 98 percent fit. Thus, the deposition rate was determined to be 0.0138 nm/s. This deposition rate was used to deposit the different tin oxide thicknesses from 1 nm, 2nm, 3nm, 4nm, 5nm, 7nm, 9nm for different samples to study the voltage variation of cold-electron transport with quantum well thickness.

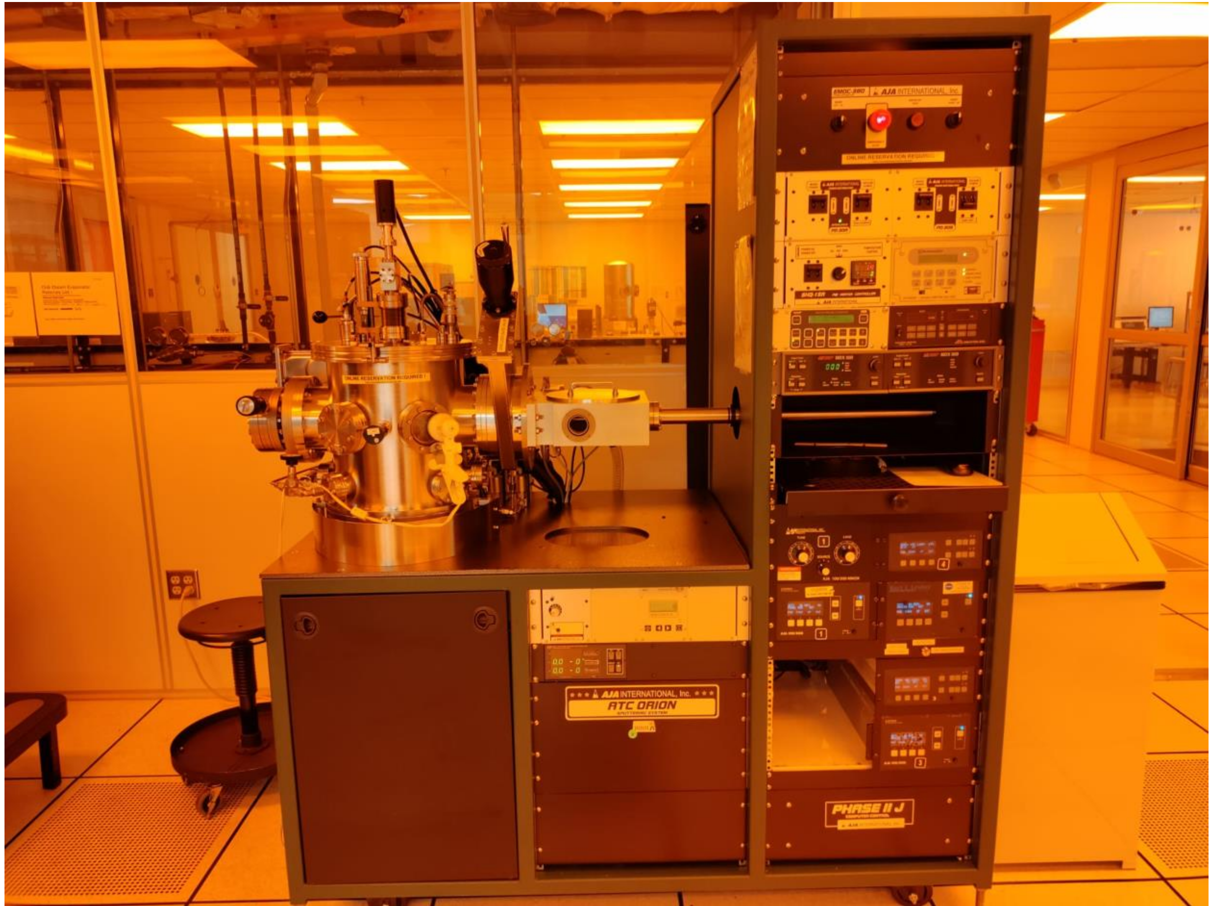


Figure 27: AJA Sputter Deposition equipment for DC and RF Sputtering

3.3.5.3 Tunneling Barrier 1 deposition

After the quantum well layer deposition is done, the next step is to deposit the Tunneling Barrier layer 1. We are using silicon nitride as well as aluminium oxide as tunneling Barrier 2 material. The silicon nitride tunneling barrier was done in the AJA Sputter deposition equipment with the following parameters:

Power: 150W

Pressure: 5mT

Ar: 30sccm

The deposition time for 1 nm silicon nitride was calculated, from the deposition rate of 0.0159nm/s obtained for a dummy sample deposition, to be 62.6 seconds. For the samples

with aluminium oxide tunneling barrier, the samples were shipped to Northwestern University to Tyler Gish from Dr. Hersam's group using Atomic Layer deposition equipment. The thickness deposited was 0.5 nm and 1.0 nm of aluminium oxide for different samples with similar thicknesses. The aluminium oxide thickness was varied to study the effect of tunneling barrier thickness on the shift in the cold-electron transport voltage. Once the energy filter stack is completed, we can then move to the next stage for the source and drain metal pads patterning.

3.3.7 Second Mask Lithograpy

The second mask consists of a source and drain electrode pad pattern. Now that the silicon contact pad and the energy filter tack have been completed, the next step is to pattern the source and drain electrode metal contact pads.

3.3.7.2 Photolithography for Source and Drain Electrode

The Samples are spin-coated with a negative photoresist: NR9-1000PY. The spin coating parameters are as follows:

Step 1:

500rpm; 100rpm/s; 5 seconds

Step 2:

3000rpm; 1000rpm/s; 60 seconds

Step 3:

0 rpm; 1000rpm/s; 0.1 seconds

The sample is then pre-baked at 150°C for 1 minute on a hot plate. The sample is then taken out and placed on a cooling plate and allowed to cool down to room temperature. The pattern mask with the second mask facing the top tight corner is then loaded into the OAI

Aligner photolithography equipment. The sample is fixed on the carrier wafer with scotch tape and loaded into the OAI aligner. The second mask pattern is aligned on the sample with the help of the first mask pattern present on the sample. The sample and mask need to be perfectly aligned in both the X and Y axis before contact is made. This is important because the first mask silicon window pattern is very small (in the range of 0.8 µm to 5 µm) and needs to be perfectly placed between the arms of the source and drain electrode pad patterns. Once the alignment is done and the sample is in contact with the mask, contact vacuum is activated and exposure is done. The photolithography exposure parameters are as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 19.6 mW/cm^2

Exposure Time: 10.2 seconds

Dose: 200 mJ/cm^2

After the exposure is done, the sample is unloaded from the OAI Aligner and post baked at 100°C for 1 minute on a hot plate. The sample is then taken out and placed on a cooling plate and allowed to cool down to room temperature. The sample is then immersed in a developer solution of RD6 for 25 seconds with vigorous shaking. The sample is then taken out and immersed in a DI water container with regular stirring for 5 minutes and then transferred to a second DI Water container for 5 minutes with regular stirring. The sample is then taken out and gently blow dried with nitrogen.

3.3.7.3 Source/Drain Electrode Deposition (50nm Cr Deposition)

After the second mask pattern is printed on the photoresist pattern on the sample, the source and drain metal electrodes need to be deposited on the sample. The source and drain metal used is chromium. The Chromium metal is deposited by e-beam evaporation using the AJA e-beam evaporator. For the AJA e-beam evaporator, the sample is fixed on the sample holder using clamps and loaded into the load-lock chamber. The load-lock chamber is pumped down to $2.0*10^{-5}$ mbar. The main chamber gate is opened, and the sample holder is slowly inserted into the main chamber. The sample holder is then hooked to a stage inside the main deposition chamber, and the load-lock arm is taken out, and the main chamber gate is closed. After the pressure reaches below $5.0*10^{-6}$ mTorr the stage control and thickness monitor is turned on, and the source shutter is opened.

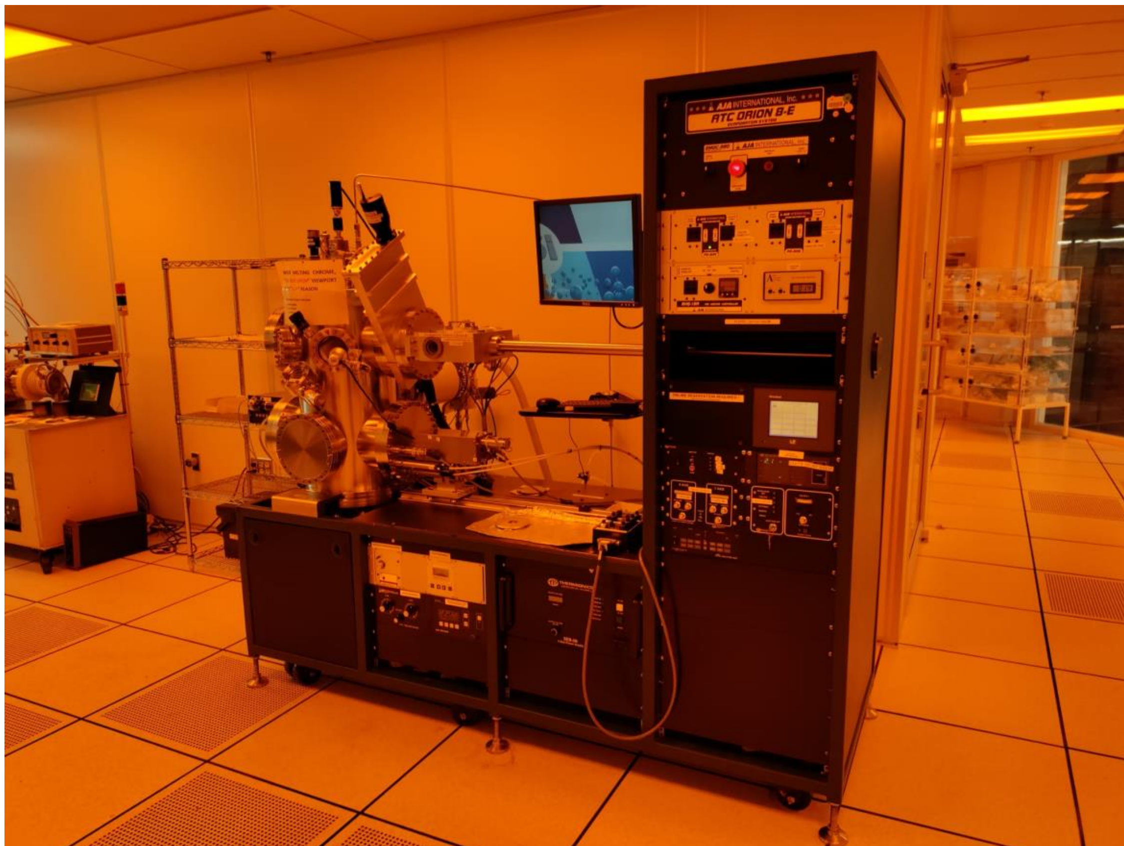


Figure 28: AJA e-beam evaporator equipment for metal deposition

The material density of the material to be deposited is input into the thickness monitor to monitor the deposited thickness. The e-beam power is turned on and the current is slowly ramped up until the deposition starts. The current is ramped up to reach the optimal deposition rate on 1.0 Å/s and allowed to stabilize for 1 minute. The sample shutter is then opened, and the thickness monitor thickness is reset at the same time. The deposition rate is observed and maintained at 1.0 Å/s. The deposition parameters for the chromium deposition are as follows:

Deposition Material: Chromium

Thickness: 50nm

Deposition Temperature: Room temperature

Deposition Rate: 1.0 Å/s

When the deposited thickness reaches 50nm, the source and sample shutter are closed at the same time and the e-beam current is slowly ramped down to 0. The e-beam power is then switched off. The thickness monitor and the stage control are turned off. The main chamber to load-lock door is opened and the load-lock arm is inserted into the main chamber. The sample holder is lowered onto the load-lock arm and delatched. The load-lock arm is withdrawn along with the sample holder. The main chamber door is closed, and the load-lock chamber is vented to atmosphere. The sample holder is taken out and the samples are removed from the sample holder.

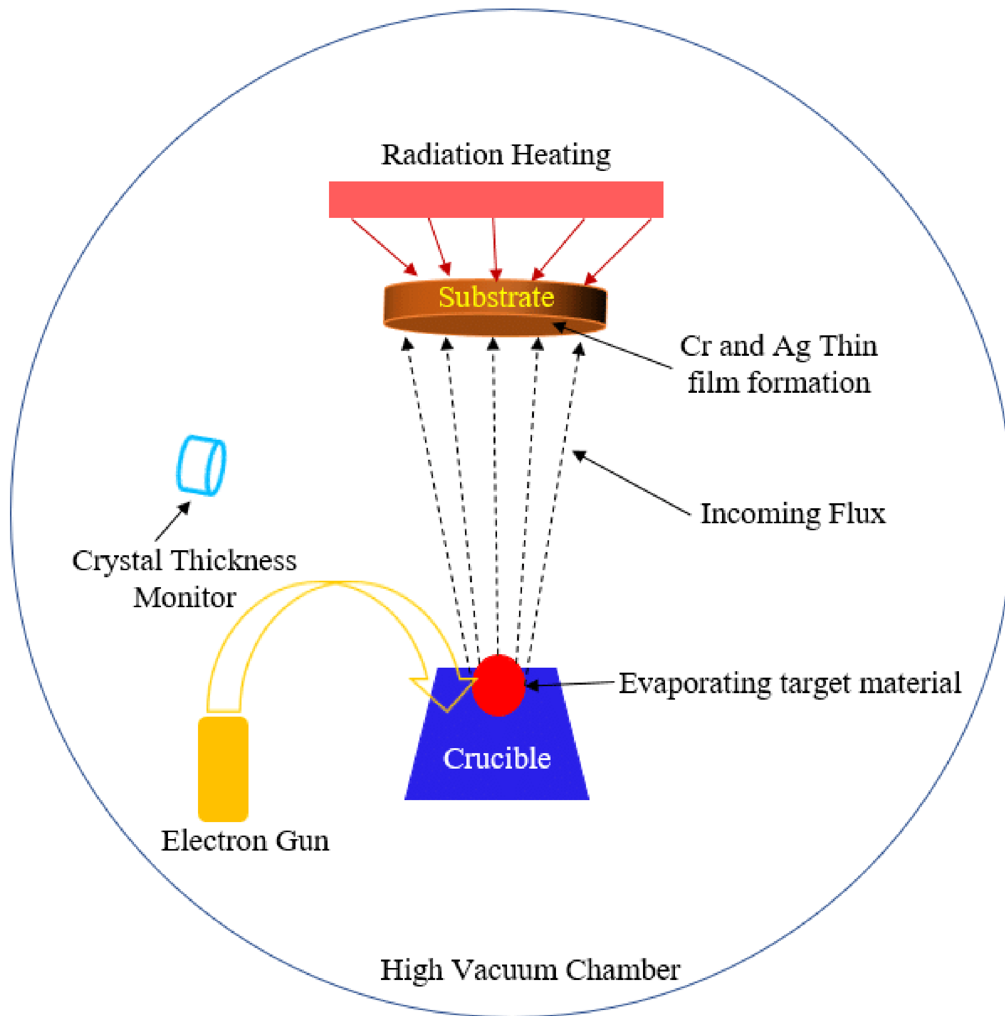


Figure 29: Schematic showing e-beam evaporation working principle[149]

3.3.7.4 Lift-off for photoresist removal

The sample is then immersed into acetone beaker and sonicated for 5 minutes followed by IPA rinsing for 1 minute. The sample is then immersed into IPA beaker and sonicated for 5 minutes followed by IPA rinsing for 1 minute, The sample is then blow dried with nitrogen.

3.3.8 Third Mask Lithography to remove EF stack from Si Contact Metal Pad

After the Energy filter stack deposition in section 3.2.6, the third mask metal contact pad is also covered with the energy filter stack. This layer on top of the third mask metal contact pad needs to be removed in order to carry out Current-Voltage measurements.

3.3.8.1 Third Mask Photolithography (Overlap)

Third mask lithography needs to be done again on the sample overlapping the previous third mask pattern. The sample is spin coated with negative photoresist, NR9-1000PY. The sample is fixed on a chuck and the sample surface is covered with the photoresist and spin coated using the following parameters:

Step 1:

500rpm; 100rpm/s; 5 seconds

Step 2:

3000rpm; 1000rpm/s; 60 seconds

Step 3:

0 rpm; 1000rpm/s; 0.1 seconds

The sample is removed from the chuck and pre-baked on a hot plate at 150°C for 1 minute. The sample is then placed on a cooling plate and allowed to cool down to room temperature. The sample is fixed on a carrier wafer using a scotch tape and is loaded into the UV photolithography equipment along with the Photolithography mask with the third mask pattern facing the top right corner. The third mask is aligned with the previous third mask pattern on the sample using the alignment marks such that the new third mask overlaps the existing third mask pattern. Once the alignment is done the mask is pressed on to the sample to make contact and contact vacuum is activated. The UV exposure is then started with the following parameters:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 19.6 mW/cm^2

Exposure Time: 6.1 seconds

Dose: 120 mJ/cm^2

After the exposure is done the sample is then taken out and post-baked on a hot plate at 100°C for 1 minute. The sample is then placed on a cooling plate and allowed to cool down to room temperature. It is then immersed in a developer solution of RD6 for 25 seconds with vigorous shaking to remove the unexposed photoresist. The sample is then taken out and immersed in DI water container for 5 minutes with regular stirring to remove any remaining developer. The sample is then transferred to the second DI water container for 5 minutes with regular stirring. The sample is then taken out and blow dried with nitrogen.

3.3.8.2 Reactive Ion Etching (Argon Etch to remove Energy Filter Stack)

The sample is loaded into the reactive ion Etch chamber in order to etch the energy filter stack from the third mask metal contact pad. The exposed third mask region of the sample is subjected to Argon plasma etching followed by oxygen plasma to remove any residue formed during the Argon etch. The etch parameters are as follows:

Step 1:

600W, 200mT, Ar: 25sccm, 240 seconds

Step 2:

350W, 200mT, O2: 11sccm, 60 seconds

After the reactive ion etching is done the samples are taken out of the RIE chamber and the contact IV for the silicon metal contact pad is measured using the Agilent 4155C IV-Probe station. If the contact IV is not linear and in the milli ampere range, the reactive ion etch

step is repeated and the contact IV is measured again. If the contact IV is linear and in the mA range, then we proceed to the lift-off process.

3.3.8.3 Lift-off

The sample is immersed in acetone and sonicated for 5 minutes. The sample is then rinsed in IPA for 1 minute and immersed in IPA and sonicated for 5 minutes. This is followed by IPA rinsing for 1 minute and blow dried with nitrogen.

3.3.9 RTA treatment for Annealing the Energy Filter

It was observed that annealing the samples at certain temperatures and times resulted in generating a sudden sharp current jump at specific voltages indicating cold-electron transport due to the discrete energy level alignment with silicon conduction band. Thus, the samples were heated in RTA chamber prior to IV measurements. The sample was loaded into the RTA Chamber and heated at different temperatures and times to study the variations of the sudden sharp jumps with different annealing conditions.

The samples are now ready and can be processed for electrical characterization.

The TEM image shows the SnO2 layer formed after e-beam deposition of Sn followed by 200°C - 1 hr annealing on a hot plate and post fabrication annealing in RTA at 500°C for 30 minutes. The quantum well formed using this process affords very little control over the actual thickness of the quantum well layer and also results in an uneven layer thickness of ~5nm SnO_2. The layered stack shown in the image is for the following materials: Au (15nm)/Cr (50nm)/ $SrTiO_3$ (1nm)/ SnO_2 (1.5nm Sn+200°C-1hr)/ Native SiO_2.

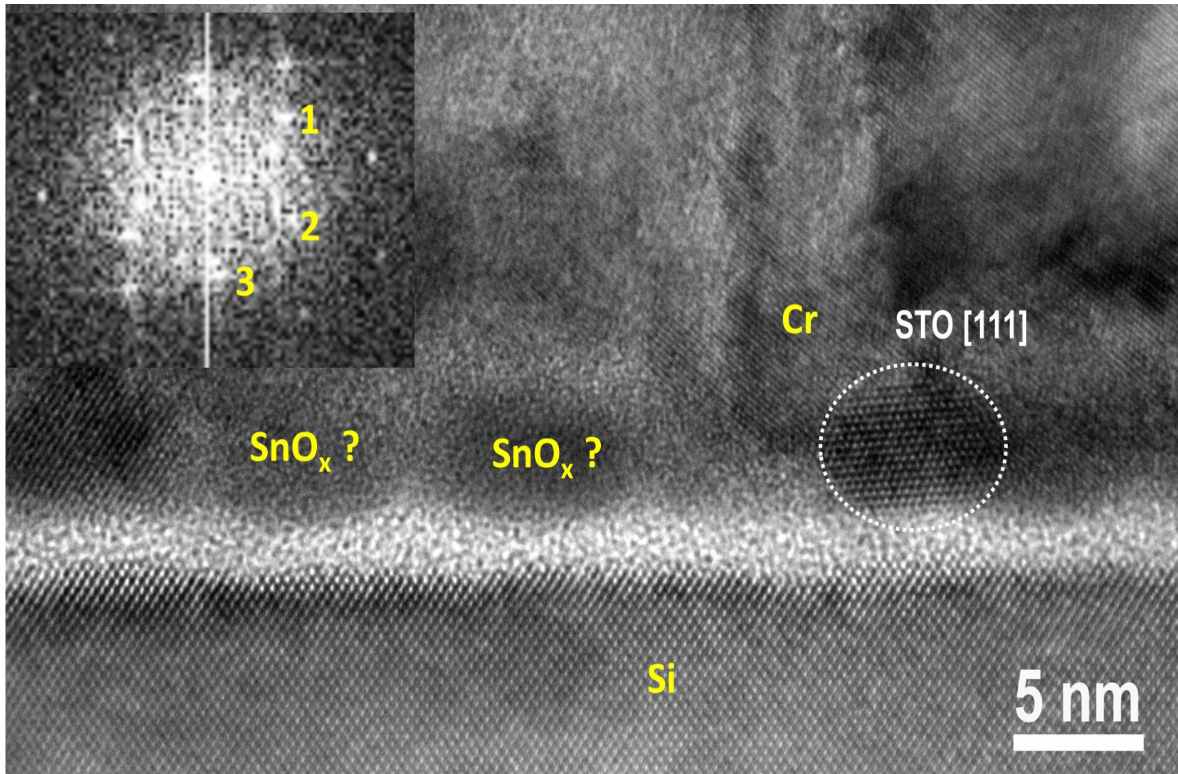
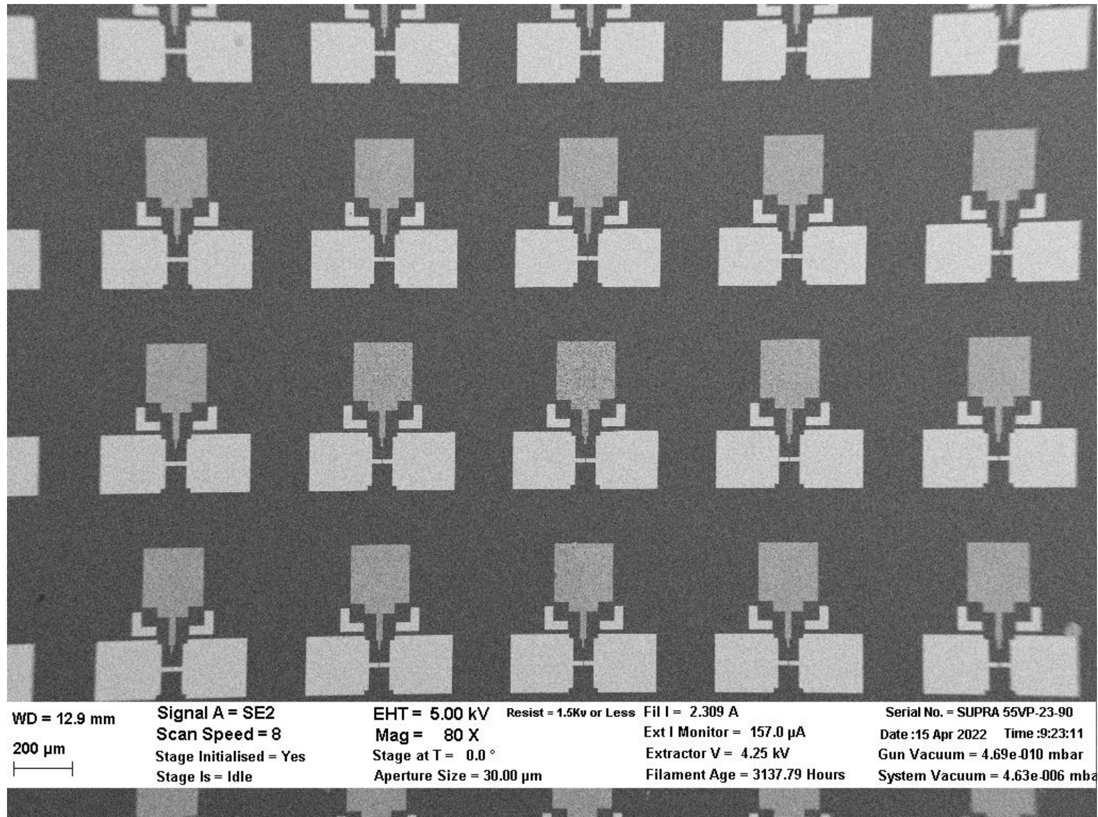


Figure 30: TEM Image showing the formation of the SnO2 layer after annealing at 200C-1hr on a hot plate followed by post-fabrication annealing in RTA at 500C for 30 min



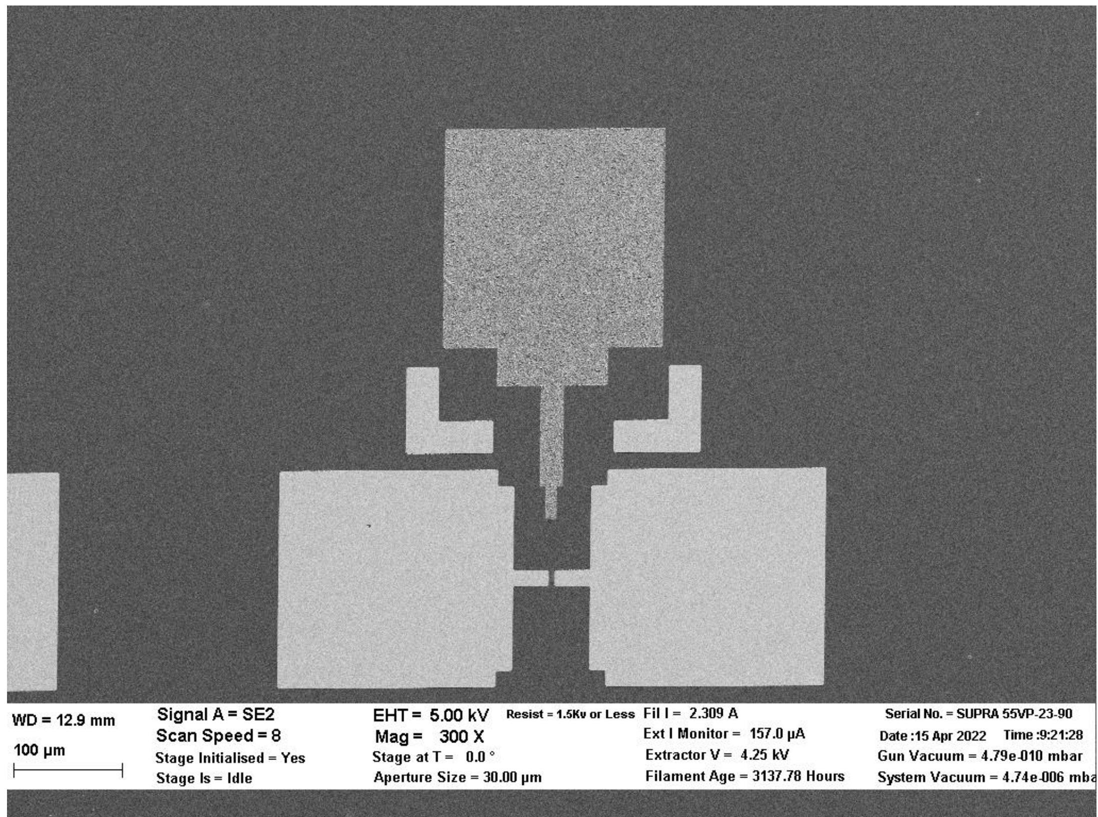


Figure 31: SEM images showing (Top) QW-Si electron transport devices array and (Bottom) top view of an individual device

Chapter 4: Results and Discussion

4.1 Electrical Characterization

IV characterization was done using IV Probe-station (Agilent 4155C) equipment in the cleanroom, IV Probe-station (Agilent ??), Lock-in Amplifier and Keithley-Agilent equipment in the Nanofab Lab. Current-voltage measurements were carried out from source metal through the energy filter stack to the silicon conduction band to the silicon metal contact. The source probe is connected to the SMU Unit 1 and the drain probe is connected to the SMU Unit 4 in the Agilent 4155C equipment.

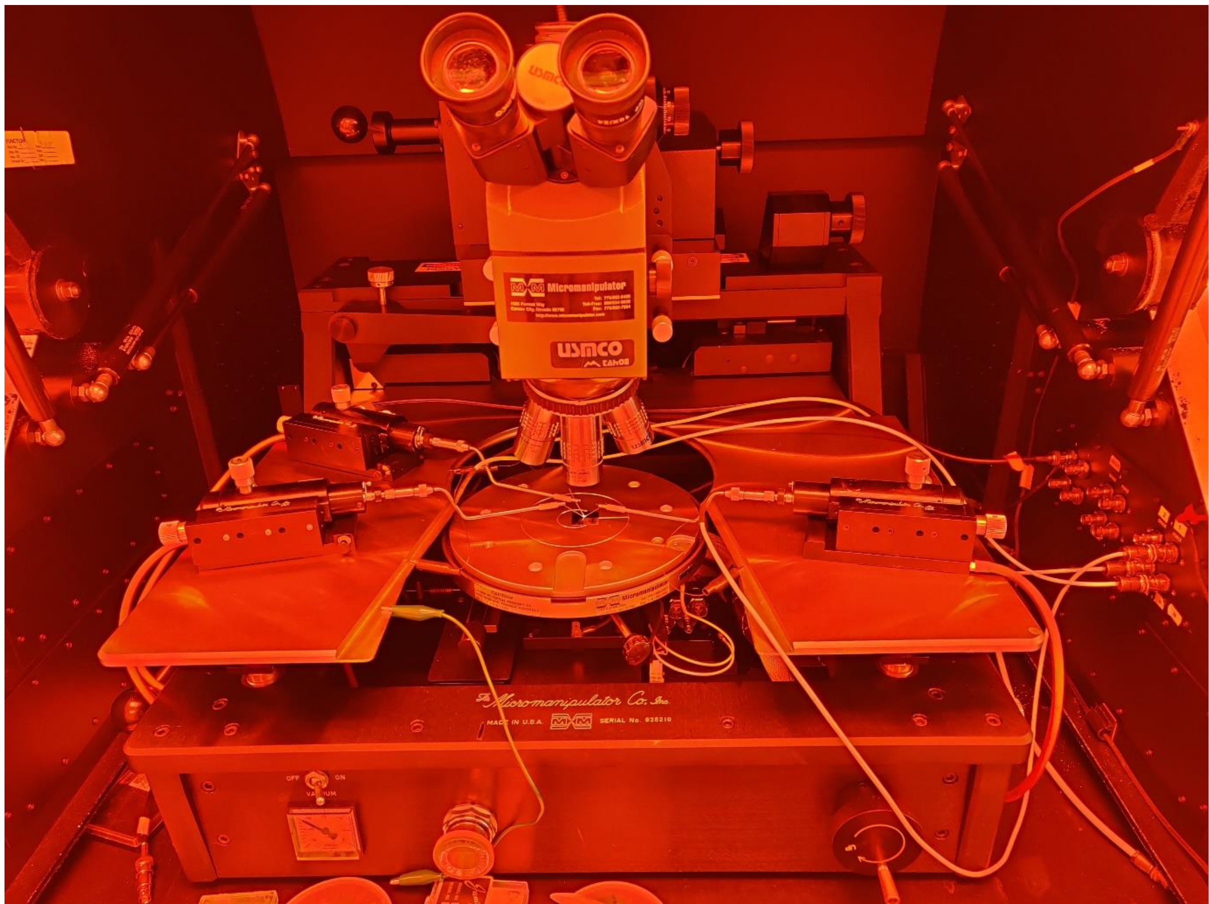


Figure 32: IV Probe station equipment for IV measurements

4.1.1 IV Measurements – Agilent 4155C – Cleanroom

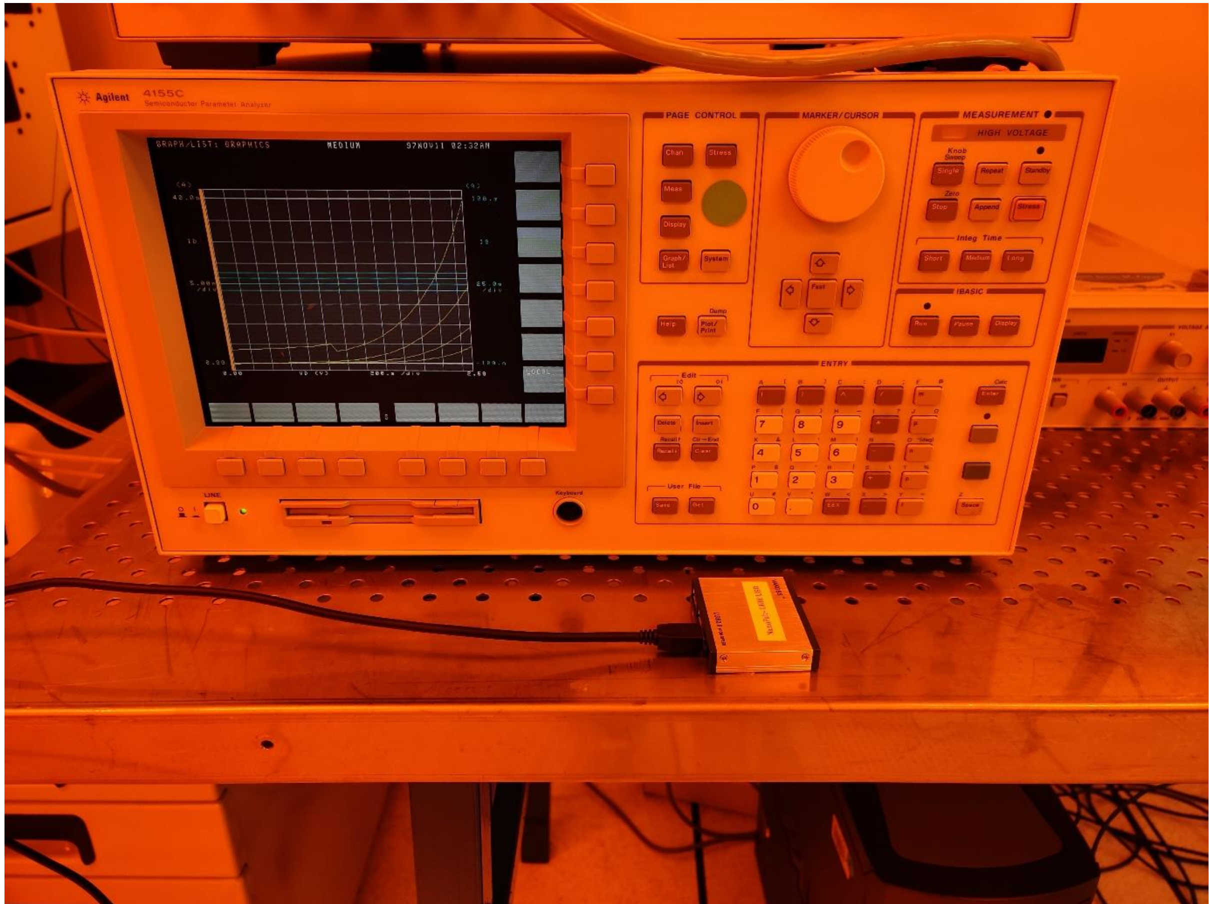


Figure 33: Agilent 4155C equipment for electrical characterization

The first devices with promising results fabricated with the following configurations of the Energy filter stack:

Native SiO_2 (~1.5 nm-2 nm) / 1.5 nm Sn deposited using E-beam evaporation + 200°C-1hr hotplate heating / 0.5 nm ALD deposited Al_2O_3. The sample was heated in RTA at 450°C for 15minutes post fabrication to make the silicon metal to silicon contact ohmic. This was done to minimize the potential drop occurring at the silicon metal and silicon interface. The devices measured (Fig. 10-11) gave consistent sharp jump at ~3.4 V source to silicon bias indicating alignment of the quantum well discrete energy level with the conduction band of silicon allowing an abrupt increase in the source-silicon current. The differential conductance for this device gave a full-width half maxima of 5 mV (Step size: 5mV)

corresponding to effective electron temperature of 16.45 Kelvin. However due to the limitation in the step size during measurement, measurement with higher resolution needed to be done using different equipment.

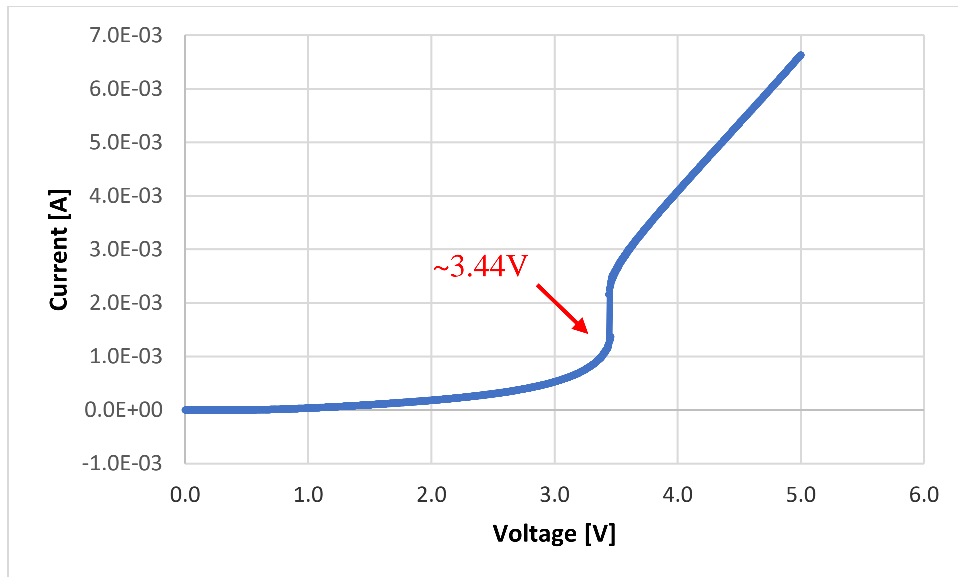


Figure 34: Source-Silicon IV through SnO2 Quantum Well Energy filter (EF Stack consists of Native SiO2/ QW: 1.5nm Sn heated at 200C-1 hr on a hot plate/ 0.5nm ALD deposited Al2O3)

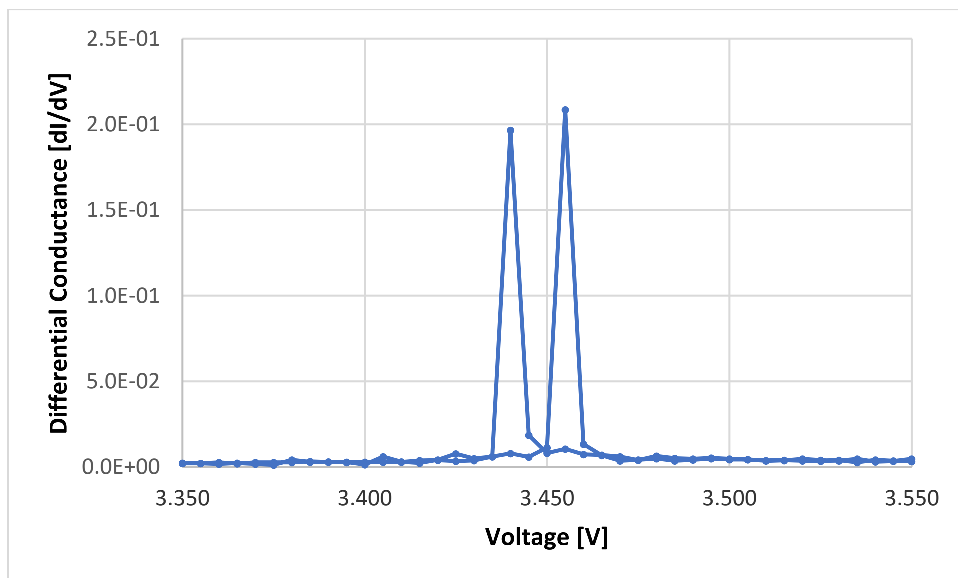
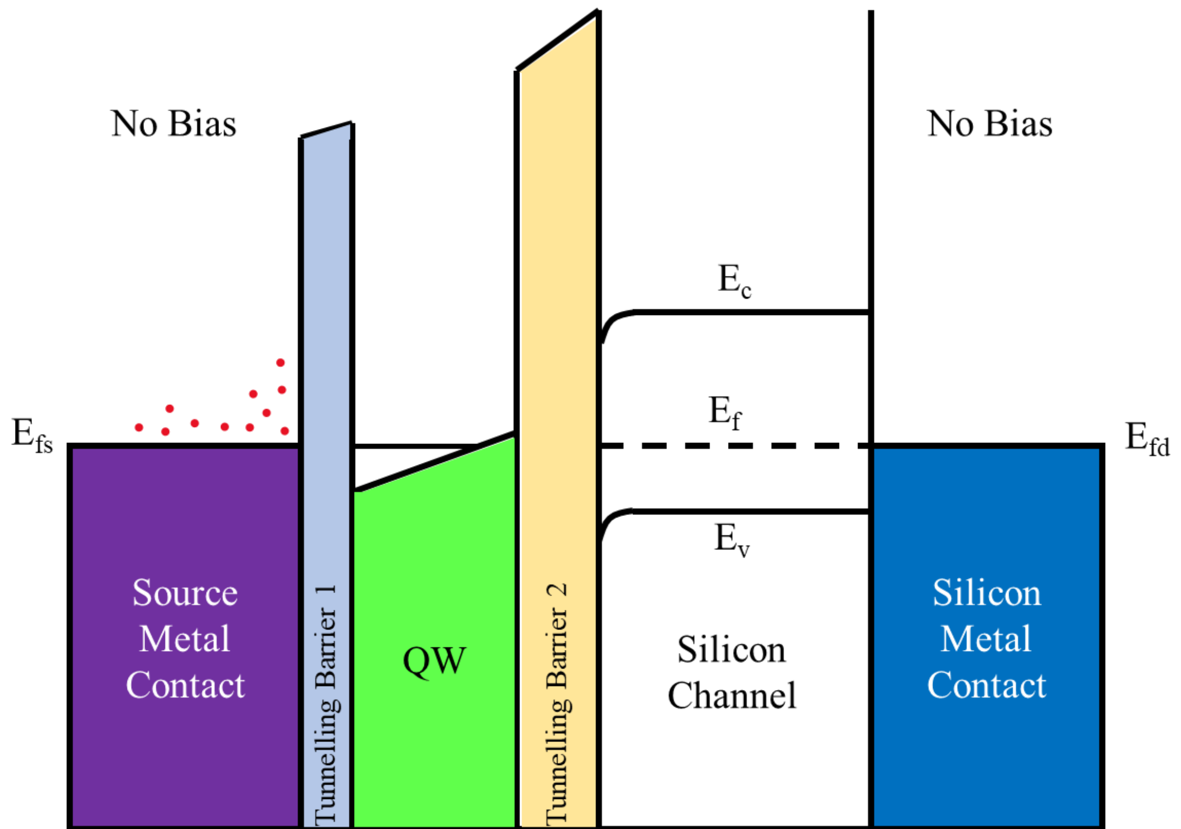


Figure 35: Differential conductance plot for Source-Silicon IV through SnO2 Quantum Well Energy filter (EF Stack consists of Native SiO2/ QW: 1.5nm Sn heated at 200C-1 hr on a hot plate/ 0.5nm ALD deposited Al2O3) (Forward and reverse measurements show a peak shift of 10mV)



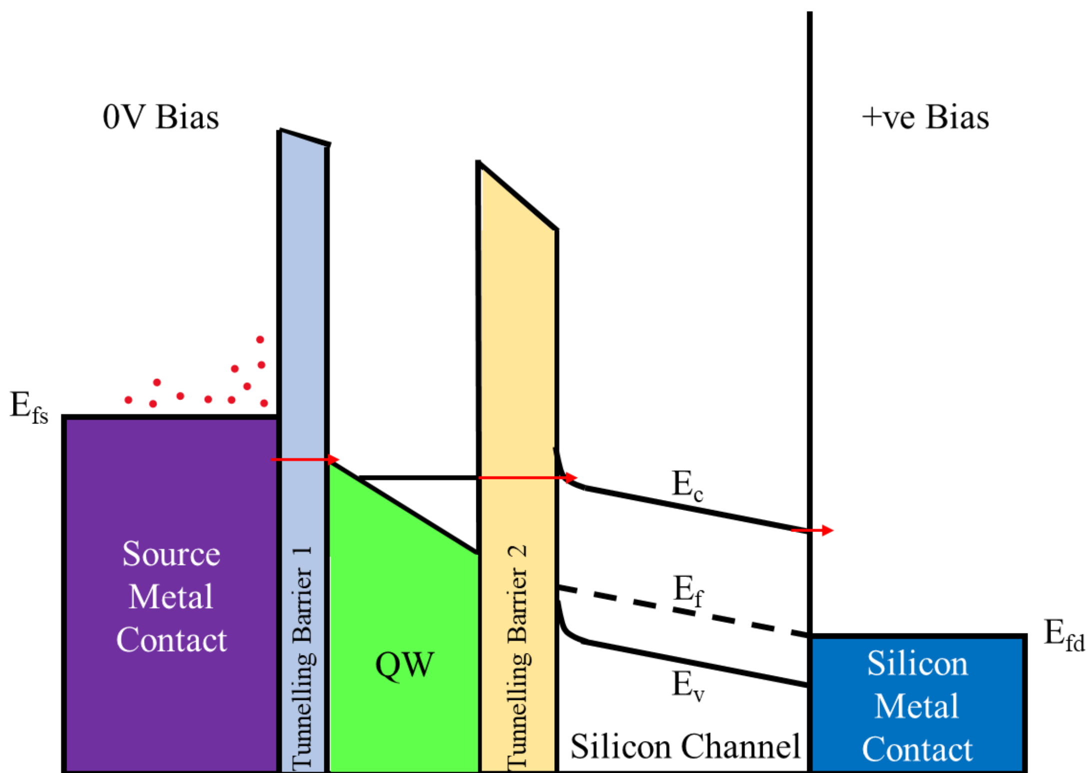


Figure 36: Energy Band diagram showing Electron transport through quantum well energy filter when a positive bias is applied

Here, the device architecture is made up of a silicon metal contact / pSi silicon and source metal which sandwich an energy filter stack consisting of ~1.5 nm-2 nm native silicon dioxide as tunneling barrier 2 / 1.5 nm e-beam evaporated Sn heated at 200°C-1hr on a hot plate to form a thin quantum well layer of SnO_2 / 0.5nm Al_2O_3 deposited by ALD as tunneling barrier 1.

The thermally excited electrons present in the source metal fermi level, upon entering the quantum well discrete energy level get trapped in the said discrete energy level as there is no path available for excitation to reach the silicon conduction band. When a positive bias is applied to the p-type silicon metal contact, the potential drop across the native silicon dioxide lowers the silicon conduction band energy level. Initially as the discrete energy level of the quantum well energy filter layer is below the silicon conduction band energy level, the source to silicon electron flow is suppressed resulting in low silicon-source current. As increasing positive bias is applied, the conduction band is further lowered so that upon reaching a specific voltage, the silicon conduction band is perfectly aligned with the discrete energy level in the quantum well layer. This alignment results in a sudden flow of electrons trapped in the quantum well discrete energy level to the silicon conduction band and to the silicon metal contact, thus, showing an abrupt increase in the silicon-source current. The abrupt current jump has a narrow differential conductance full width half maximum, which corresponds to extremely low effective electron temperatures.

The measured current jump observed (Fig. 34) has a rough current increase of 1.0 mA. The TEM image indicates that the individual single crystalline SnO2 grain size is about $(10nm)^2$. Calculating the current density through the single crystalline grain, the current density estimate will be $1.0*10^{13}$ A/m^2. This current density is several fold higher than the

maximum current density for the Cu wires, which is at 5 A/mm^2 = 5*10^6 A/m^2. Thus, the current density for the semiconducting material single crystalline grain of SnO2 of 1.0*10^{13} A/m^2 is not possible. Thus, the current path for the cold-electron transport through the quantum well layer must be occurring over a large area much larger than (10µm)^2.

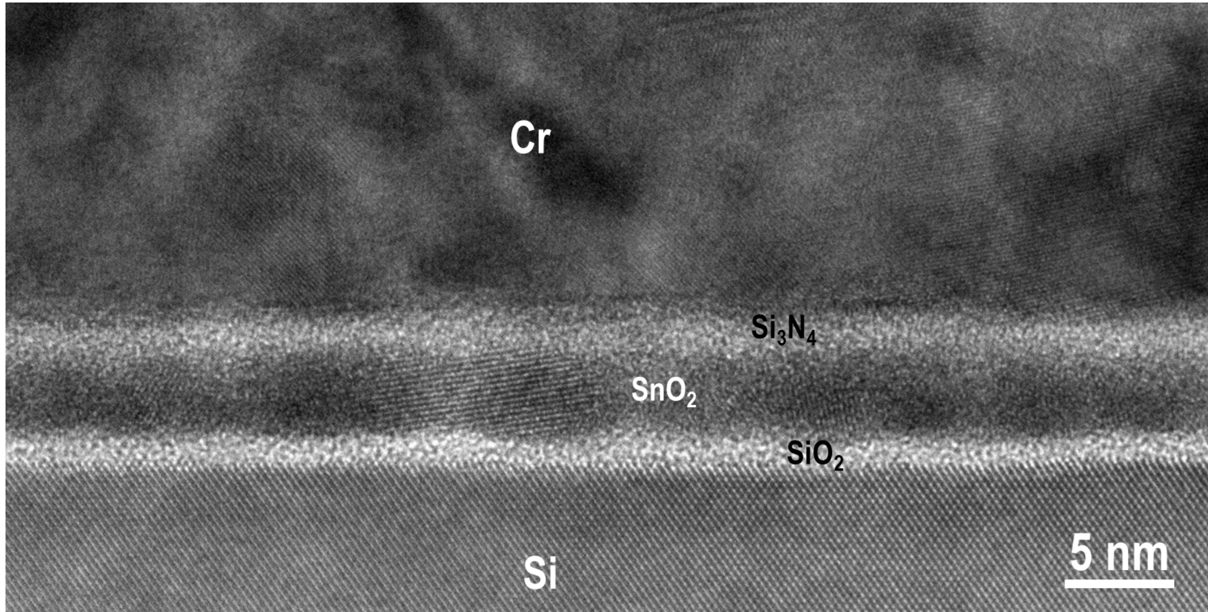


Figure 37: TEM image showing the grain sizes of SnO2 thin film. TEM image taken by Dr. Jiang in CCMB TEM equipment

That is, the large area of (>>10µm)^2 is acting as a single quantum well layer as there is a single abrupt current jump observed.

Another observation to be made here is that the current increase after the abrupt current jump for some devices is linear and for some devices it can be seen to be parabolic. This observation can be attributed to the density of states in the silicon conduction band. When the electron transport occurs in the linear region of the density of states for the silicon conduction band, the IV plot shows a linear current increase after the abrupt current jump. When the electron injection occurs in the parabolic region of the density of states[150-155] of the silicon conduction band, the current increase after the abrupt current jump will be parabolic.

4.1.2 Agilent ES2708 IV measurements

The current voltage measurements inside the cleanroom using Agilent 4155C showed majority of devices having issues with moisture formation during measurement. The moisture formation starts at the probe tips and spreads around the probe tip contact with the source metal surface. We suspect that this moisture formation is due to Peltier effect, resulting from the rapid heating and cooling of cold electrons moving from the QW layer to the silicon surface. This further indicated the cold-electron current jumps were real. Thus, in order to avoid the moisture formation on good devices during measurement, further measurements were carried out in vacuum using the Agilent ES2708 equipment and the Janis ST-500 Probe station in the Nanofab lab.

The sample was loaded into the ST-500 probe station measurement chamber after venting the chamber with dry nitrogen and carefully unscrewing the top lid and inner chamber cover. Special care needs to be taken to make sure that no screws should fall back inside the chamber as they would be impossible to remove without shipping the entire equipment to manufacturing. The sample loading and unloading process is done while wearing full face and hairnet cover, and nitrile gloves to prevent the measurement chamber contamination. Once the samples are loaded into the chamber the lids are screwed back on and the chamber is evacuated. The Agilent ES2708 Semiconductor parameter analyser is turned on for 30 minutes prior to measurements to warm up the system for optimal measurements.

Now the HRSMU probe tip is connected to the silicon metal contact pads on the sample. The other probe tip is connected to the drain pad. The probe tips are gently touched on the device electrodes and the connections are made. A voltage bias is applied to the silicon contact metal electrode. And the Current-voltage measurements are carried out.

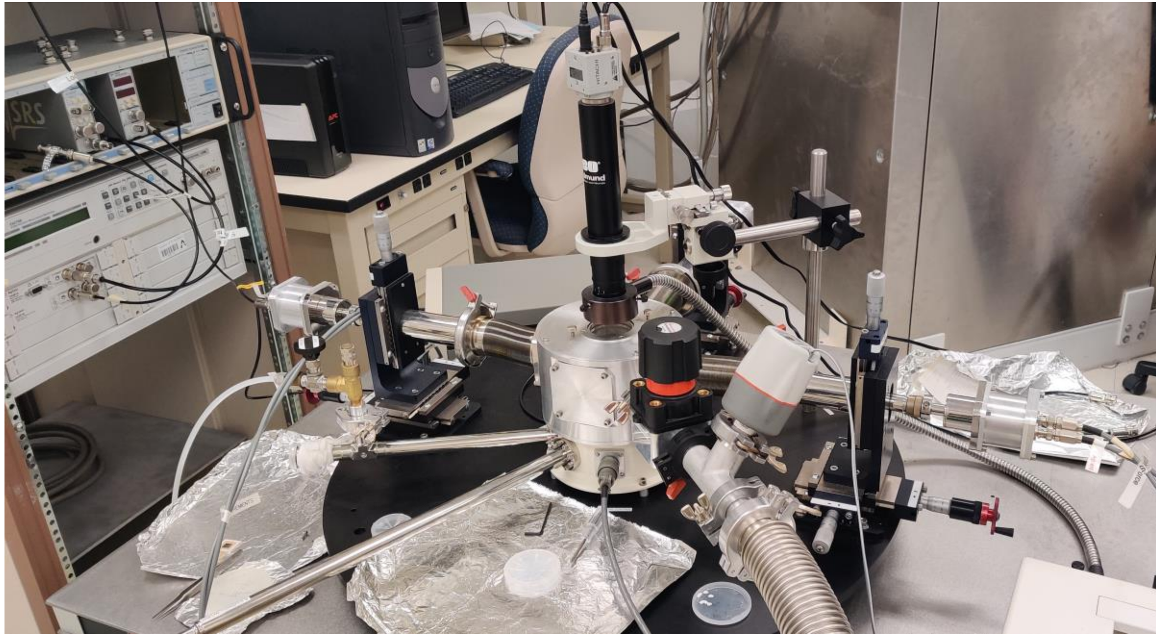


Figure 38: Current-voltage measurement setup for Vacuum measurement of devices

Devices were fabricated using sputtered tin oxide (SnO_2) as the QW layer. The sputter deposited QW layer gave us more control over the quantum well thickness. The deposition rate for the sputtered tin oxide material was as low as 0.0138 nm/second, which gave a good accuracy when depositing thin film of 3nm - 5nm layer of the quantum well layer. Figure 15-16 shows the current-voltage measurement of a device with EF stack: Native SiO_2 (1.5nm) / QW: 3 nm Sputtered SnO_2 / 1 nm Sputtered Silicon Nitride (Si_3N_4). Here, the thermally excited electrons from the source metal enter the quantum well layer discrete energy level and get trapped inside the said discrete energy level due to no other path available for excitation. However, when a positive bias is applied to the silicon metal contact, the potential drop across the tunneling barrier (Native SiO_2) lowers the silicon conduction band to a lower energy level. The silicon source current is still low as the discrete energy level is below the conduction band energy level and electrons are not able to tunnel through to the silicon conduction energy band. However, upon further increasing the positive bias, the silicon conduction energy Band gets aligned with the discrete energy level of the quantum well which has trapped electrons present. This alignment of the

quantum well discrete energy level and the silicon conduction band opens a path for the electrons trapped in the discrete energy level of the quantum well. These trapped electrons are now able to tunnel through to the silicon conduction energy band and result in an abrupt current jump as seen in figure 15 and 16. For this 3nm sputtered SnO_2 quantum well layer sample, the abrupt current jump is observed at close to ~3.37V positive bias. This specific voltage for the abrupt current jump is indicative of the discrete energy level placement and separation when the quantum well layer is formed and annealed. The differential conductance peak observed in figure 17 shows that the device has a Full-width half maximum of 2mV which corresponds to an effective electron temperature of 6.58 Kelvin showing proof of cold-electron transport at room temperature.

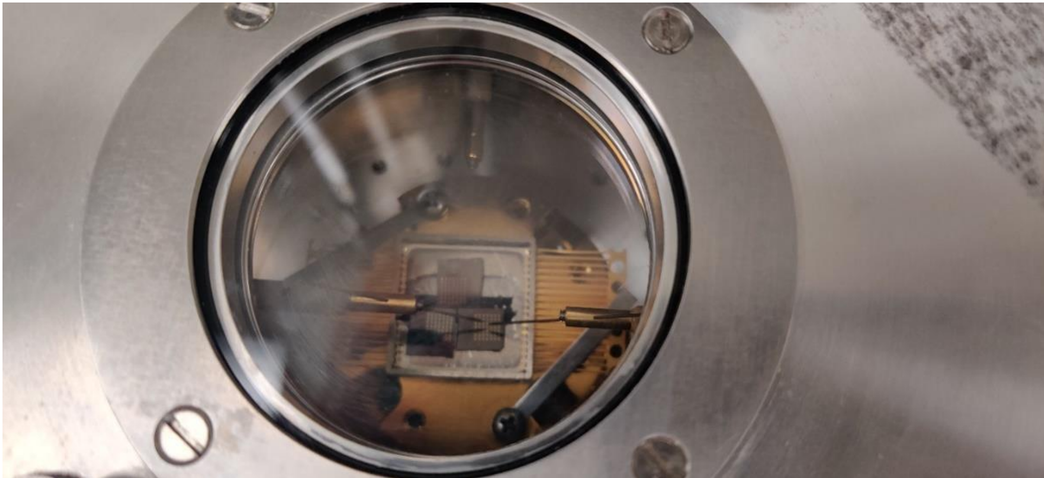


Figure 39: Image showing the sample placement with probe tips inside the vacuum measurement setup

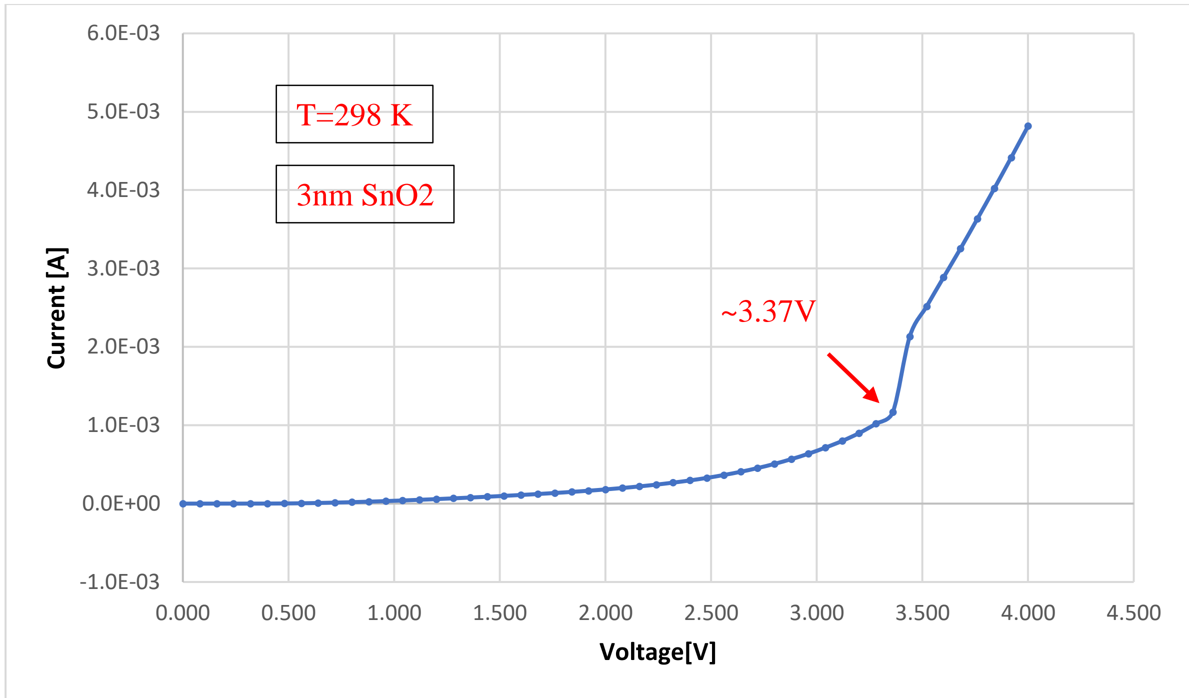


Figure 40: Source-Silicon IV through SnO2 Quantum Well Energy filter (EF Stack consists of Native SiO2/ QW: 3nm Sputtered SnO2 / 1 nm Sputtered Si3N4

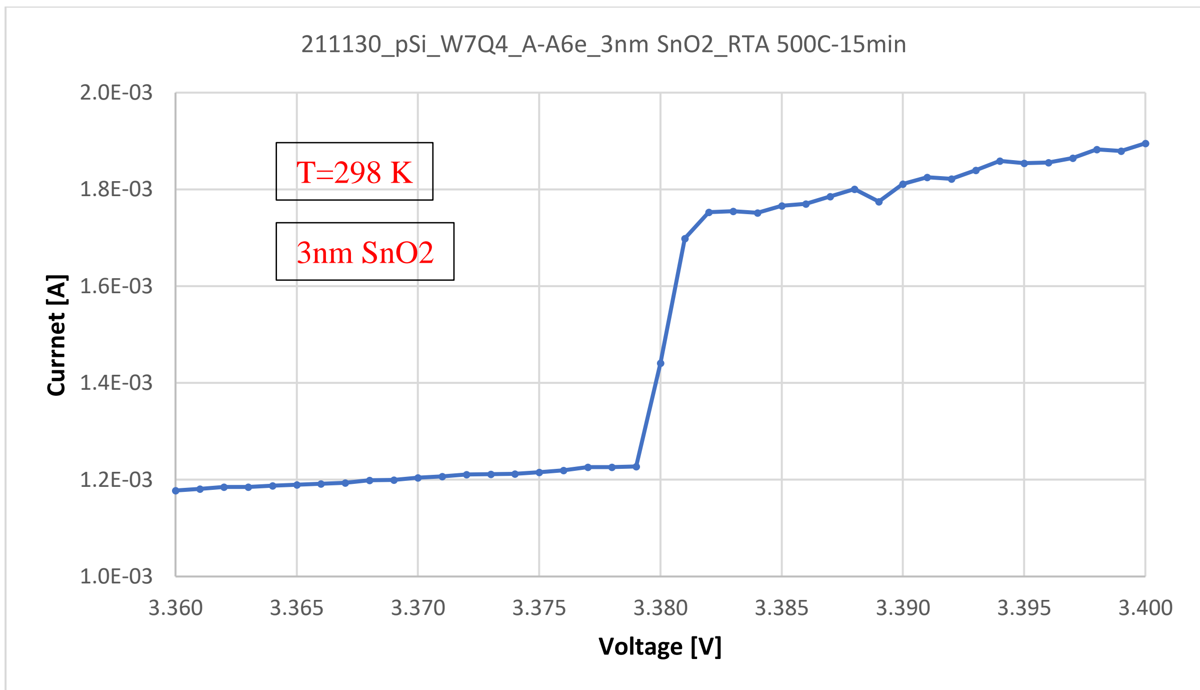


Figure 41: Source-Silicon IV through SnO2 Quantum Well Energy filter showing the abrupt current jump with higher resolution (1mV Voltage Steps) (EF Stack consists of Native SiO2/ QW: 3nm Sputtered SnO2 / 1 nm Sputtered Si3N4

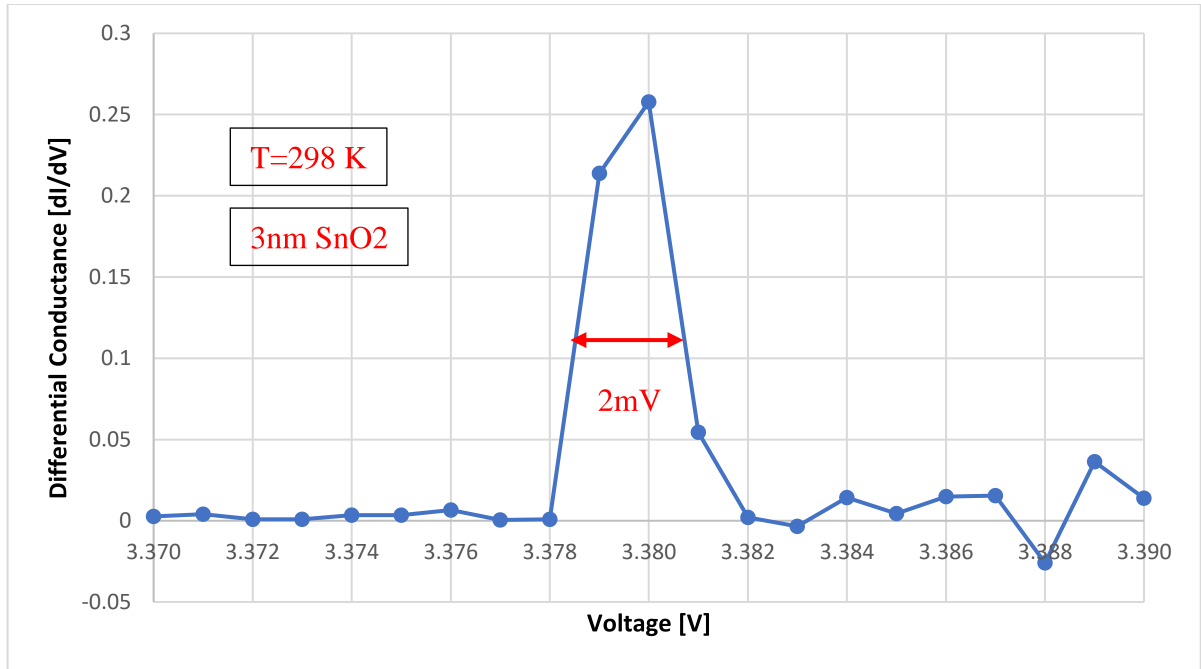


Figure 42: Differential Conductance vs voltage plot for device with (EF Stack consists of Native SiO2/ QW: 3nm Sputtered SnO2 / 1 nm Sputtered Si3N) shows FWHM of 2mV corresponding to 6.58 Kelvin effective electron temperature

Another good device measured on the sample showed an abrupt current jump (fig. 18-19) indicating cold-electron transport. As before, the thermally excited electrons from the source metal are trapped in the discrete energy level of the 3nm tin oxide quantum well. A positive bias was applied to the silicon metal contact. This lowers the silicon conduction energy band to a lower energy level. The silicon to source metal current is low when the discrete energy level is still below the conduction band energy. Upon further application of a positive bias at the silicon metal contact, this further lowers the silicon conduction band energy. When the silicon conduction band is perfectly aligned with the discrete energy level of the quantum well which is holding trapped electrons from the source metal, we see an abrupt current jump. This

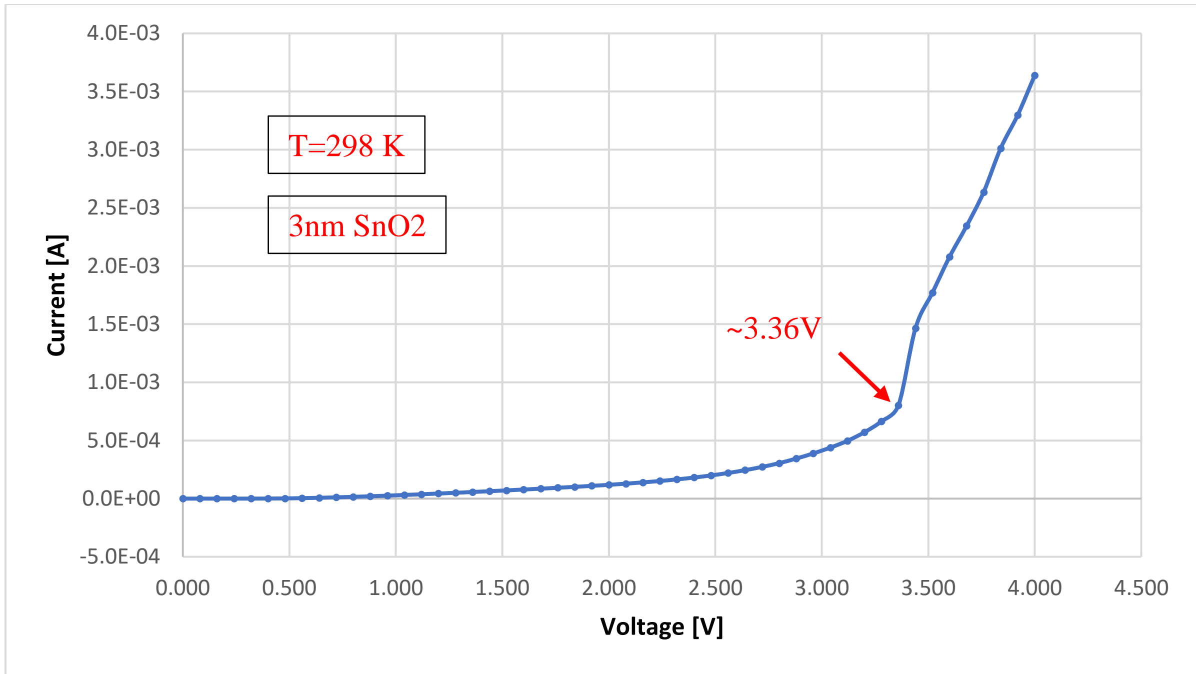


Figure 43: Source-Silicon IV through SnO2 Quantum Well Energy filter for another device (EF Stack consists of Native SiO2/ QW: 3nm Sputtered SnO2 / 1 nm Sputtered Si3N4

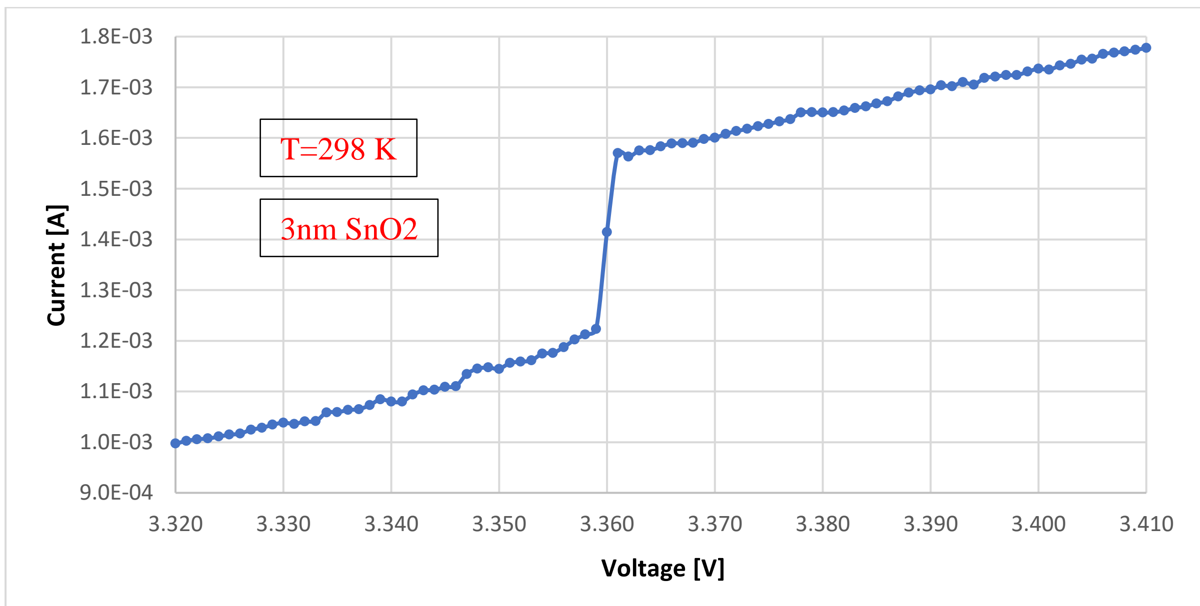


Figure 44: Source-Silicon IV through SnO2 Quantum Well Energy filter showing the abrupt current jump with higher resolution (1mV Voltage Steps) (EF Stack consists of Native SiO2/ QW: 3nm Sputtered SnO2 / 1 nm Sputtered Si3N4

sharp current jump due to the alignment of the discrete energy level shows cold-electron transport from source metal to silicon metal contact through an energy filter at room temperature. The abrupt current jump is seen at ~3.36 V. This specific voltage at which the sharp jump is observed is indicative of the discrete energy level placement and separation formed in the quantum well.

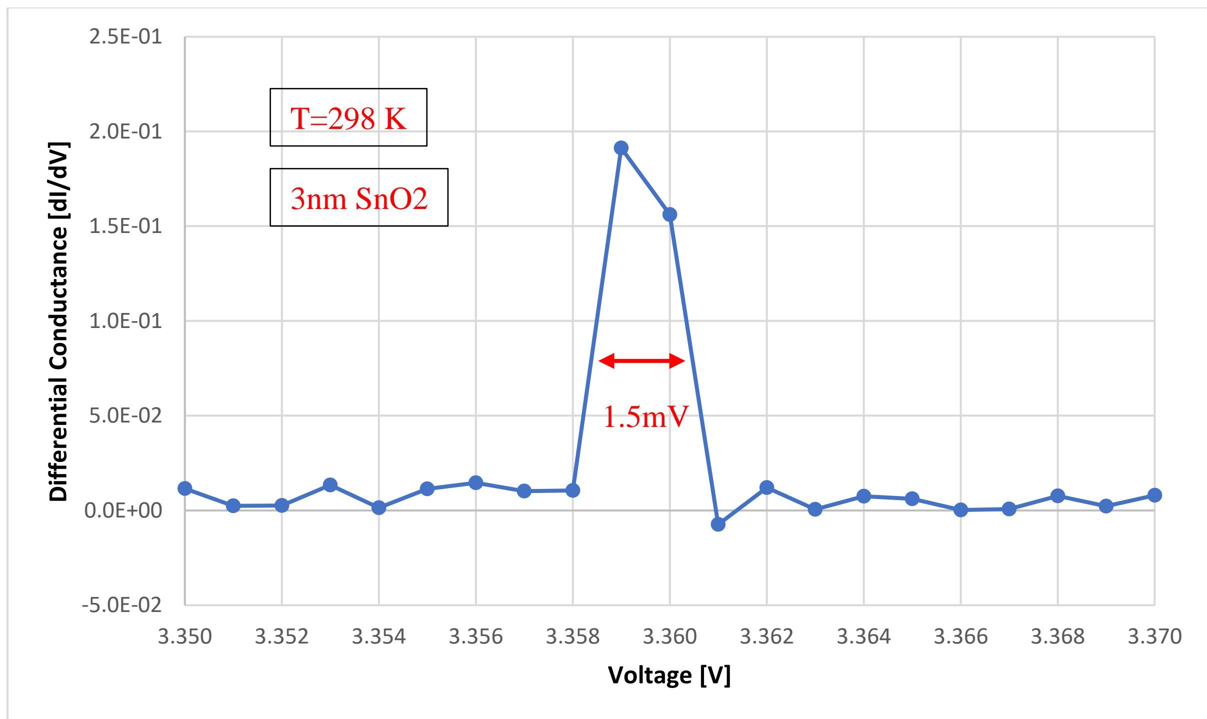
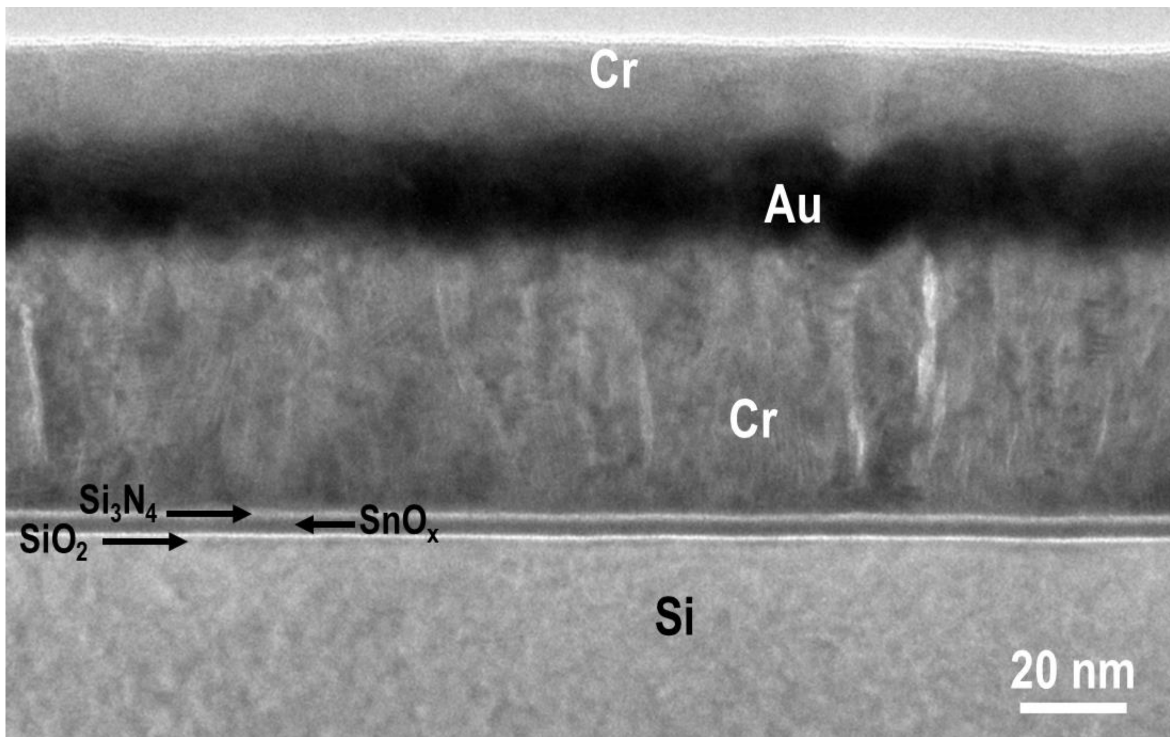


Figure 45: Differential Conductance vs voltage plot for device with (EF Stack consists of Native SiO2/ QW: 3nm Sputtered SnO2 / 1 nm Sputtered Si3N) shows FWHM of 1.5mV corresponding to 4.94 Kelvin effective electron temperature

The differential conductance vs voltage plot for the device measured in Fig. 18-19 shows a full-width half maximum of 1.5 mV. This FWHM corresponds to an effective electron temperature of 4.94 Kelvin measured at room temperature. These devices prove successful suppression of thermally excited electrons at room temperature and cold-electron injection to silicon at room temperature. The following TEM images (Fig. 21-22) shows the device structure layout and crystal structure of the different layers in the Energy filtering stack for the 3 nm SnO_2 device.



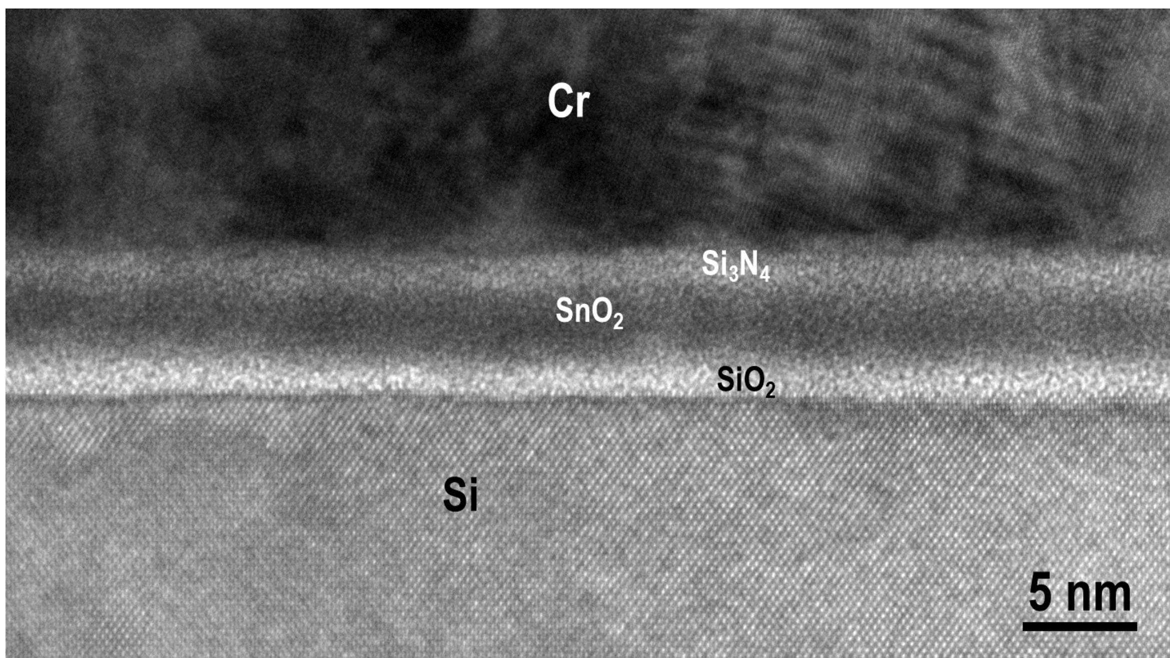
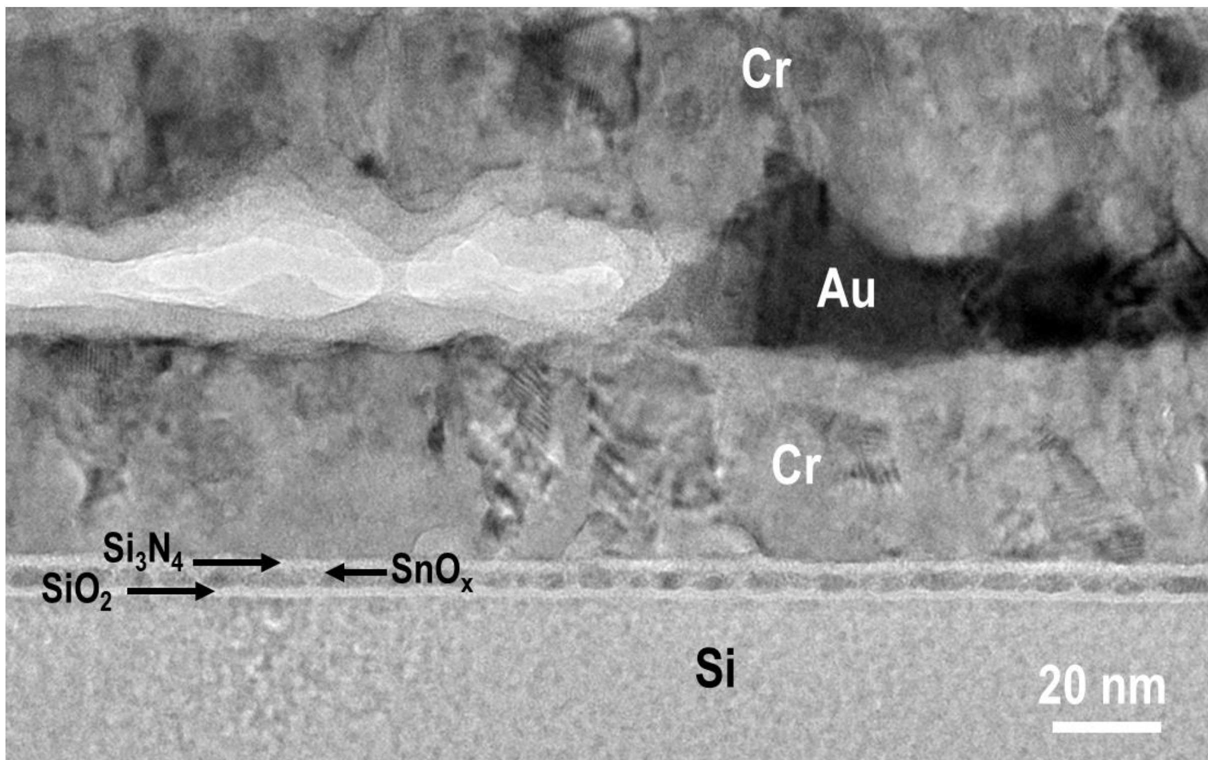


Figure 46: TEM image showing Energy filter layer stack for 50nm Cr/15nm Au/50nm Cr/1nm Si3N4/3nm SnOx/1nm SiO2/Si without additional RTA annealing



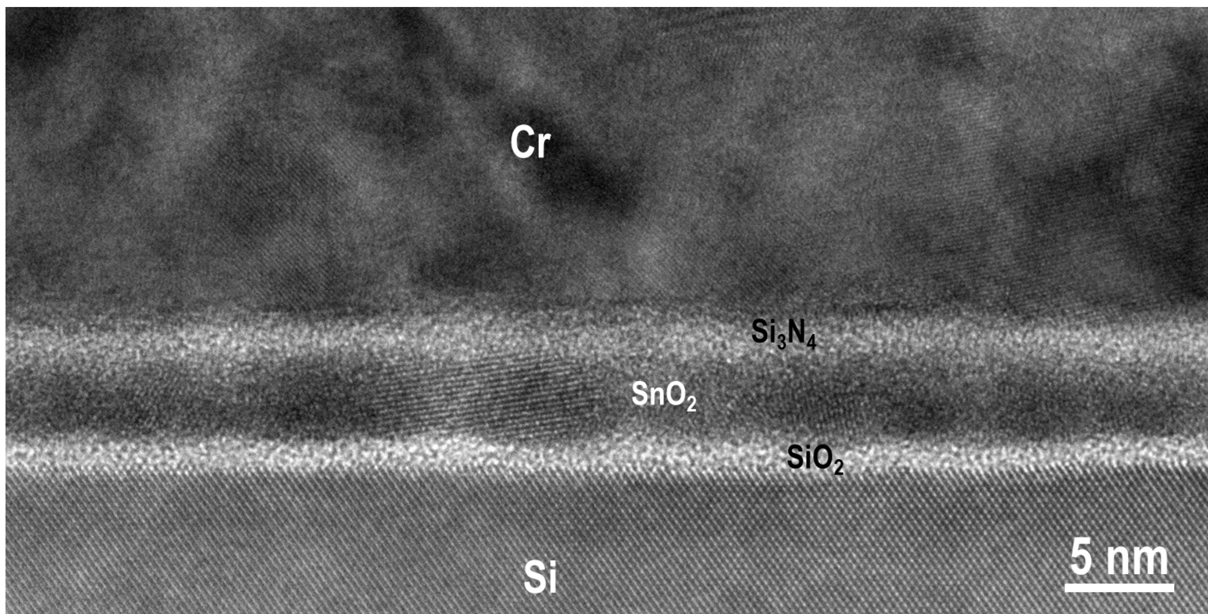


Figure 47: TEM image showing Energy filter layer stack for 50nm Cr/15nm Au/50nm Cr/1nm Si3N4/3nm SnOx/1nm SiO2/Si with RTA annealing at 500°C for 30 minutes

Further measurements were carried out for several more devices with varying parameters to study the effect of quantum well layer thickness and variation of annealing times on the specific voltage for the abrupt current jump location.

Three samples with the following conditions were prepared and source-silicon IV was measured: Native SiO2 (1.5nm) / QW: 4nm Sputtered SnO2 / 1nm Sputtered Si3N4. The samples were post-annealed after fabrication in RTA at 500℃ for 5 minutes / 10minutes and 20 minutes.

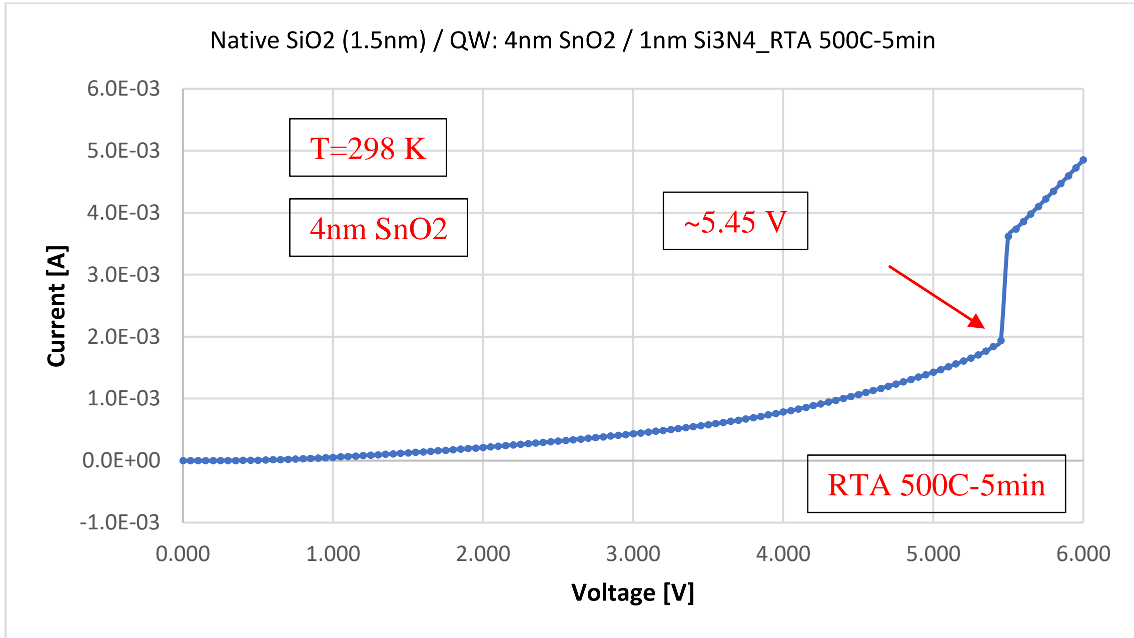


Figure 48: Source-Silicon IV for device with QW: 4nm SnO2, TB1: 1 nm Si3N4 and RTA 500C-5min

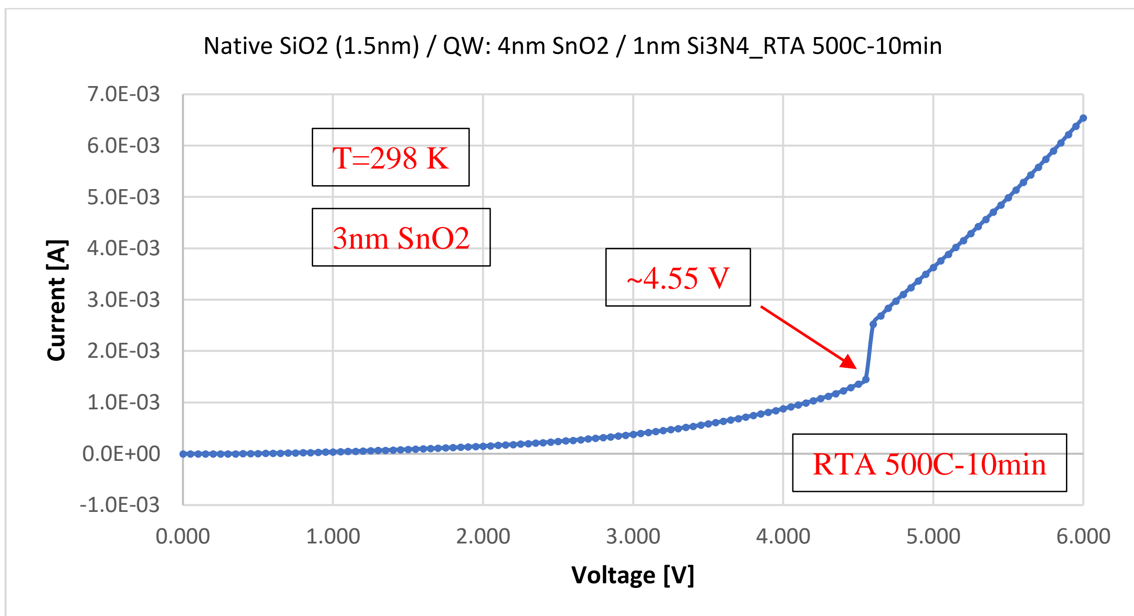


Figure 49: Source-Silicon IV for device with QW: 4nm SnO2, TB1: 1 nm Si3N4 and RTA 500C-10min

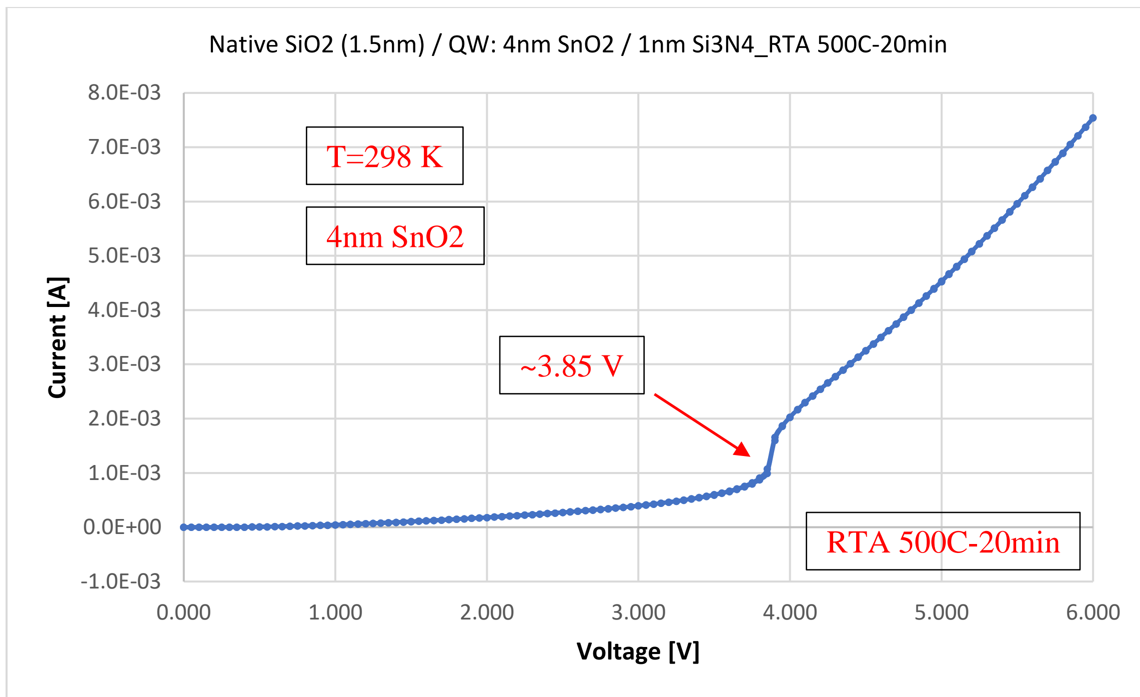


Figure 50: Source-Silicon IV for device with QW: 4nm SnO2 TB1: 1 nm Si3N4 and RTA 500C-20min

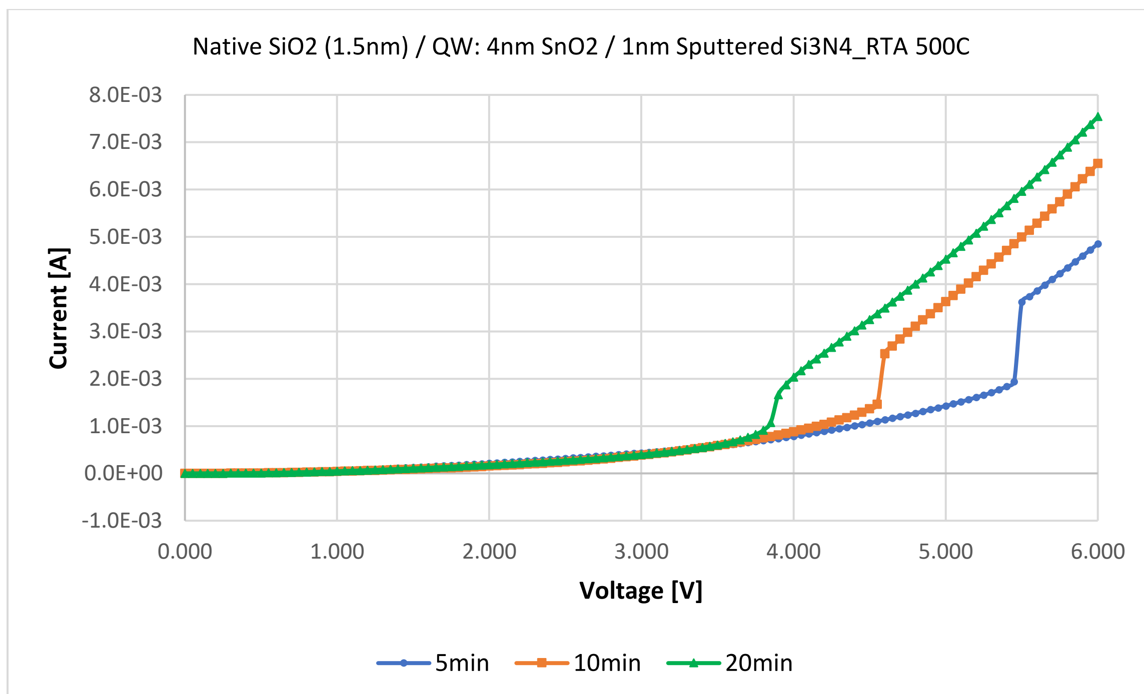


Figure 51: Source-Silicon IV showing variation of abrupt jump voltage with increased RTA annealing time

A clear shift was observed in the sharp current jump voltages with increase in annealing time. We suspect this may be due to a change in the crystal structure of the quantum well

layer resulting a change in the quantum well layer thickness. The change in quantum well layer thickness results in a shift in the discrete energy level of the quantum well. This shift causes a lower bias required to align the silicon conduction energy band with the discrete energy level which in turn results in the sharp jump being observed at a lower voltage bias.

4.1.3 Lock-in Amplifier SR830 Measurements

The Stanford Research 830 Lock-In Amplifier (Dual Phase) (SR-830) was used in conjunction with SR-570 (Current Pre-amplifier), Summing amplifier (SIM-980) and Scaling amplifier (SIM-983). The Agilent ES2708 Semiconductor parameter analyzer was used to generate a Direct Current (DC) Source and the SR-830 internal sine generator provided the sinusoidal Output (AC). The Agilent Semiconductor Parameter Analyzer was turned on for 30 minutes prior to use to warm up the system for optimal measurements. The probe tips were connected to the SMU on the parameter analyser using low noise triaxial cables. The shield is connected to the probe station to reduce noise. The chuck and the shield are all connected to the ground on the semiconductor parameter analyser. Measurements were done in the Janis ST-500 Probe station under vacuum. Sample loading and unloading was done with full face cover, hair net and using nitrile gloves to prevent any contamination of the measurement chamber inside the probe station. After the sample loading is complete and the chamber is evacuated, the Agilent ES 2708 parameter analyser is turned on.

The Native SiO_2 / QW: 1.5nm Sn + 200C-1hr / 0.5nm Al_2O_3 device was measured after annealing for 450°C for 15 minutes. The IV measurement was done with a step size of 0.25mV. The abrupt current jump was observed at ~3.31V as shown in the fig. 37. Lock-in Amplifier measurements were then done on the same device after locating the abrupt current jump voltage.

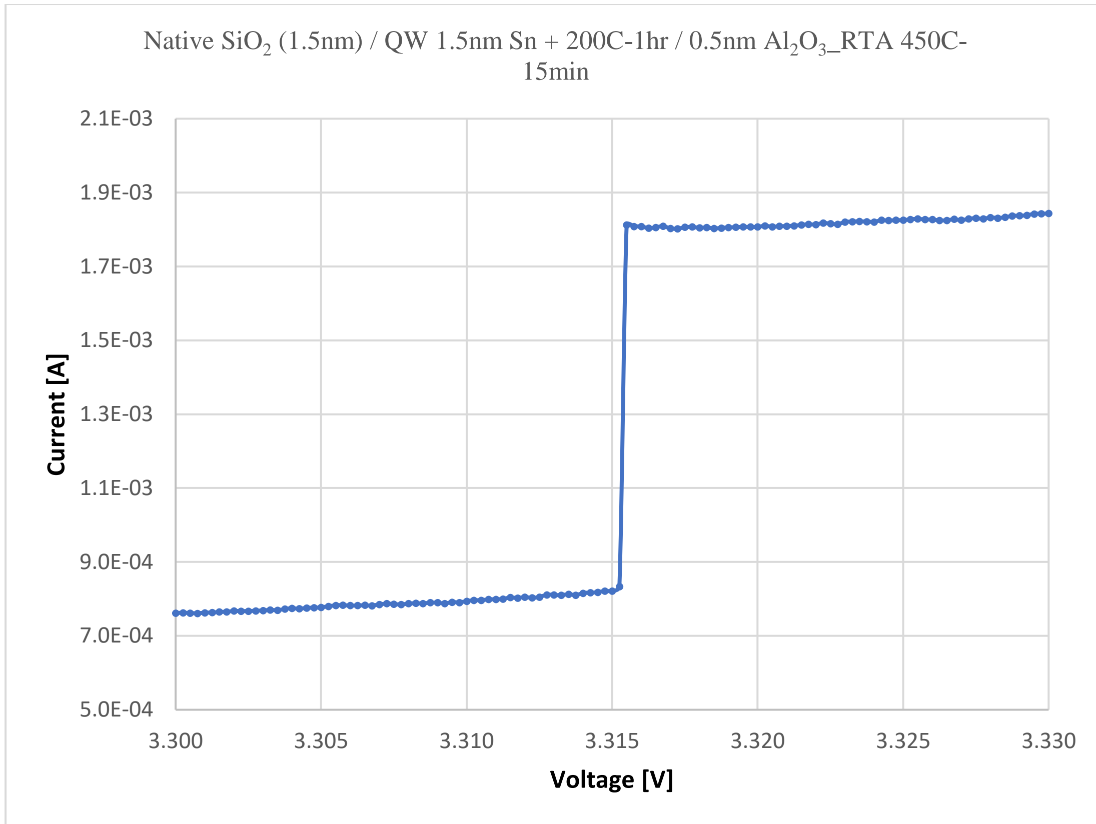


Figure 52: Source-silicon IV measurement showing abrupt current jump voltage location for device (Native SiO2 91.5nm) / QW: 1.5nm Sn + 200C-1hr / 0.5nm Al2O3)

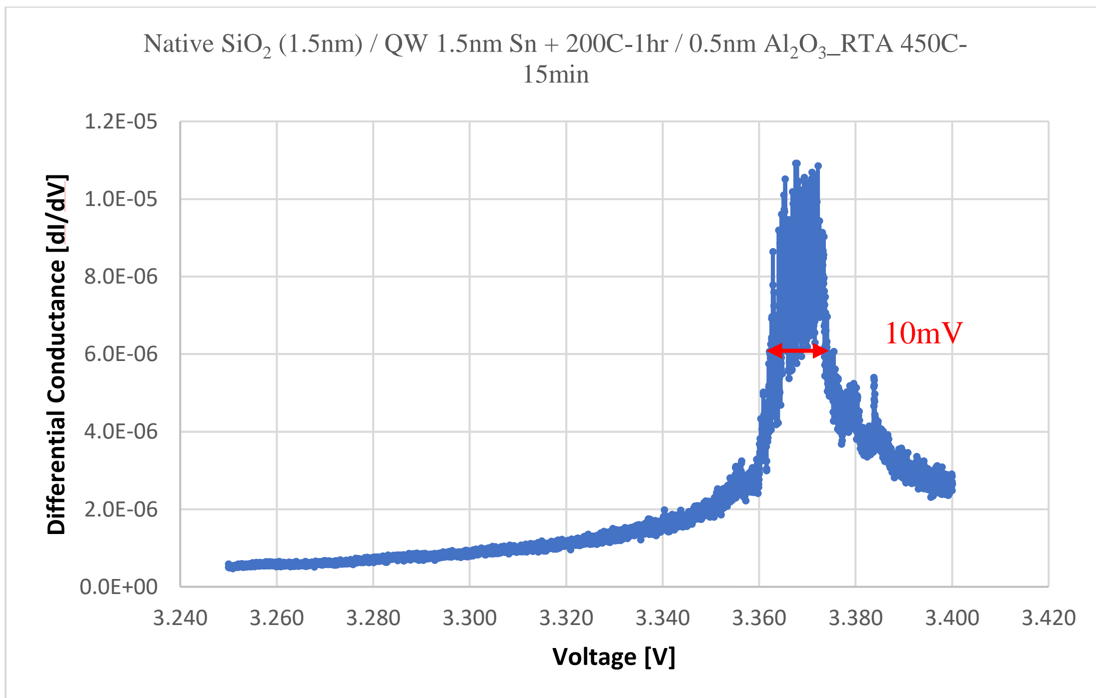


Figure 53: Lock-in Amplifier Differential Conductance vs Voltage measurements showing a FWHM of 10mV

The lock-in amplifier measurement was done with a step size of 0.025mV resolution. A differential conductance peak was observed with a full-width half maxima of 10mV which corresponds to an effective electron temperature of 32.91 Kelvin at room temperature. This show the successful suppression thermally excited electrons and cold-electron injection to silicon using a quantum well energy filter at room temperature.

4.1.4 Keithley-Agilent High Resolution IV Measurements

High resolution measurements were carried out to more precisely measure the differential conductance peaks and give accurate effective electron temperature readings. The silicon probe and the source metal probes were connected to the Agilent and Keithley equipment using a summing amplifier to give higher resolution measurements. New devices were fabricated using sputtered SnO_2 deposition to have more precise control over the quantum well layer thickness. These devices were measured using the Keithley-Agilent setup. Three different samples were prepared with varying quantum well thickness of 3nm SnO_2, 4nm SnO_2 and 5nm SnO_2. The samples were all annealed using the same RTA conditions of 500°C for 15 minutes.

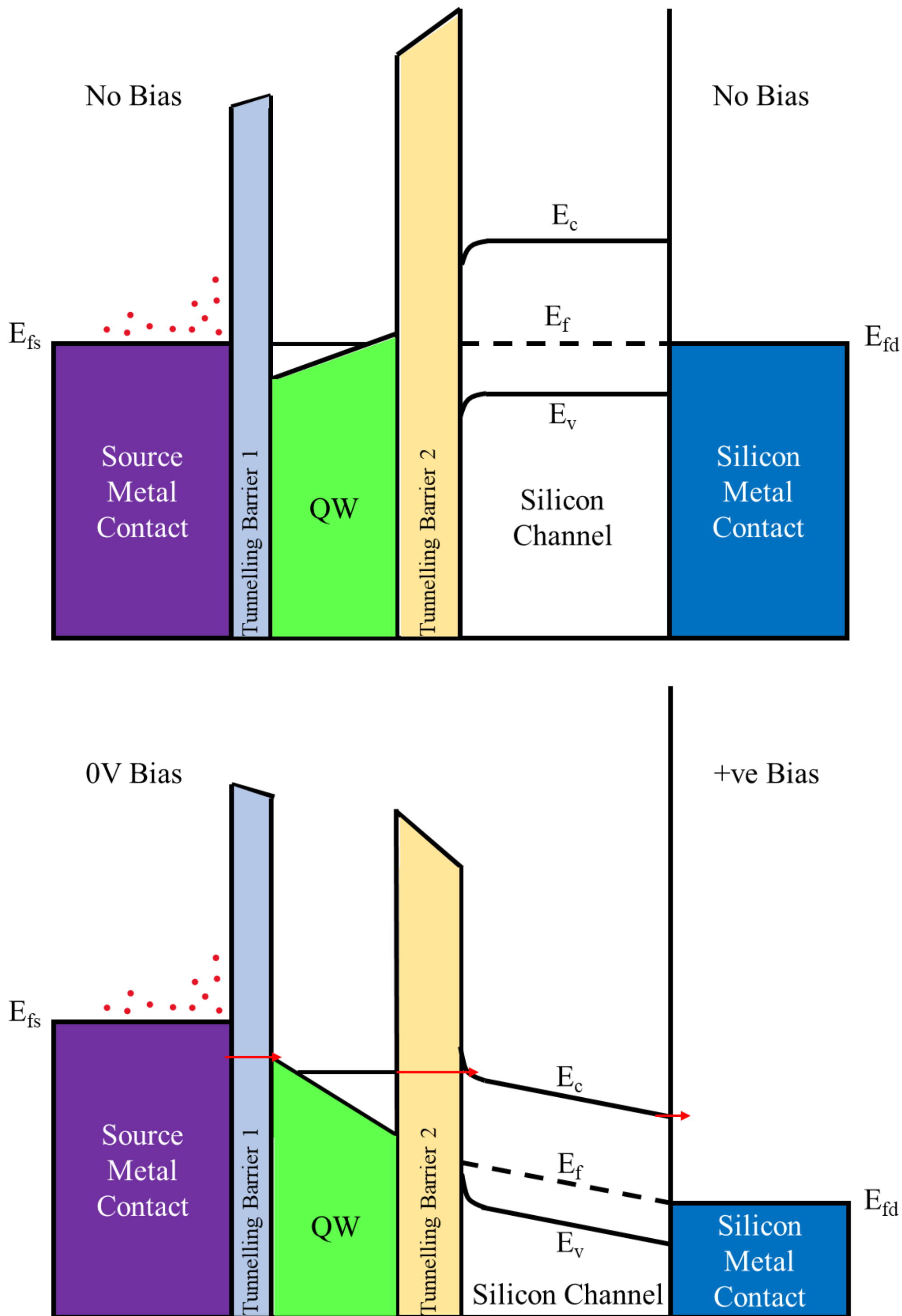


Figure 54: Energy Band diagram showing Electron transport through quantum well energy filter when a positive bias is applied

Here, the same principle is followed. The thermally excited electrons from the source metal enter the quantum well discrete energy level and get trapped due to no available path for

excitation due to the energy level separation of the quantum well energy levels being much larger than the room temperature thermal energy. When a positive bias is applied to the silicon metal contact, the silicon conduction energy band is lowered. As long as the quantum well discrete energy level is not aligned with the conduction energy band of silicon, there is no electron transfer taking place. Upon further increase of the positive bias, the silicon conduction energy band is lowered even more and is aligned with the discrete energy level of the 5 nm SnO_2 quantum well and we see an abrupt current jump at 2.8V applied bias. (Fig. 58). The

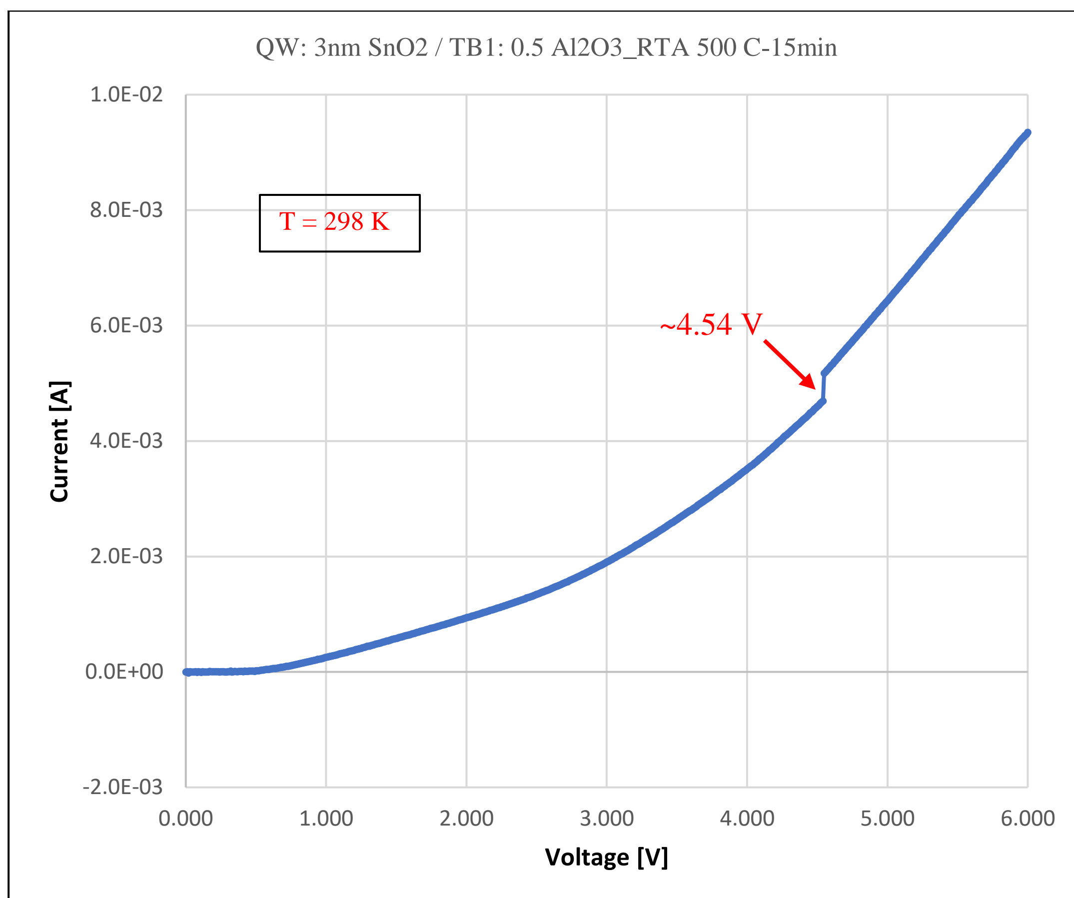


Figure 55: Source-Silicon IV for device with Native SiO2 / QW: 3nm SnO2 / 0.5nm Al2O3_RTA 500C-15min

zoomed-in plot for the abrupt current jump shows a very sharp jump at a resolution of 0.1mV voltage bias step size. The differential conductance vs voltage plot for the abrupt

current jump shows a very narrow differential conductance peak with a Full-width half-maxima (FWHM) of 0.1mV. Using the relation FWHM = 3.525*kT [116], The narrow dI/dV peak with FWHM of 0.1mV corresponds to an effective electron temperature of 0.33 Kelvin, thus, achieving cold electron injection to silicon at room temperature.

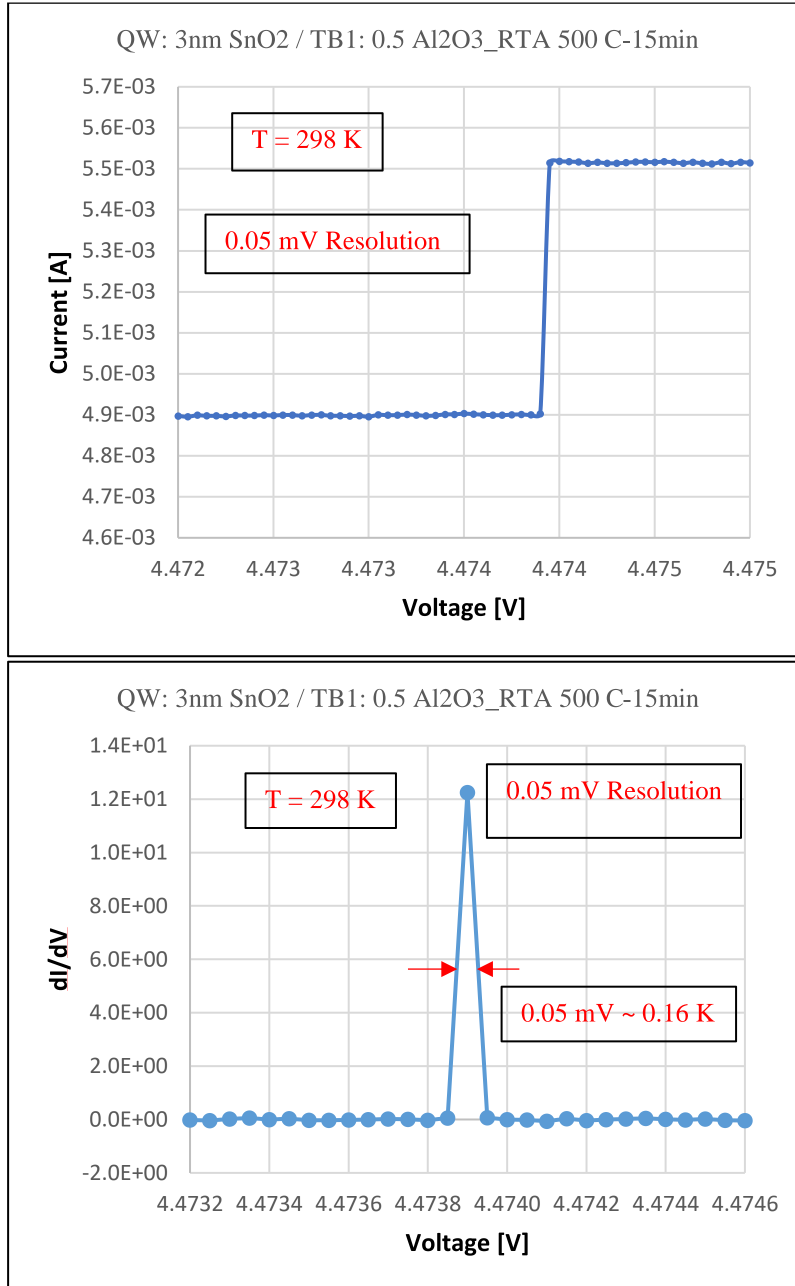


Figure 56: Differential Conductance vs Voltage for device with Native SiO2 / QW: 3nm SnO2 / 0.5nm Al2O3_RTA 500C-15min

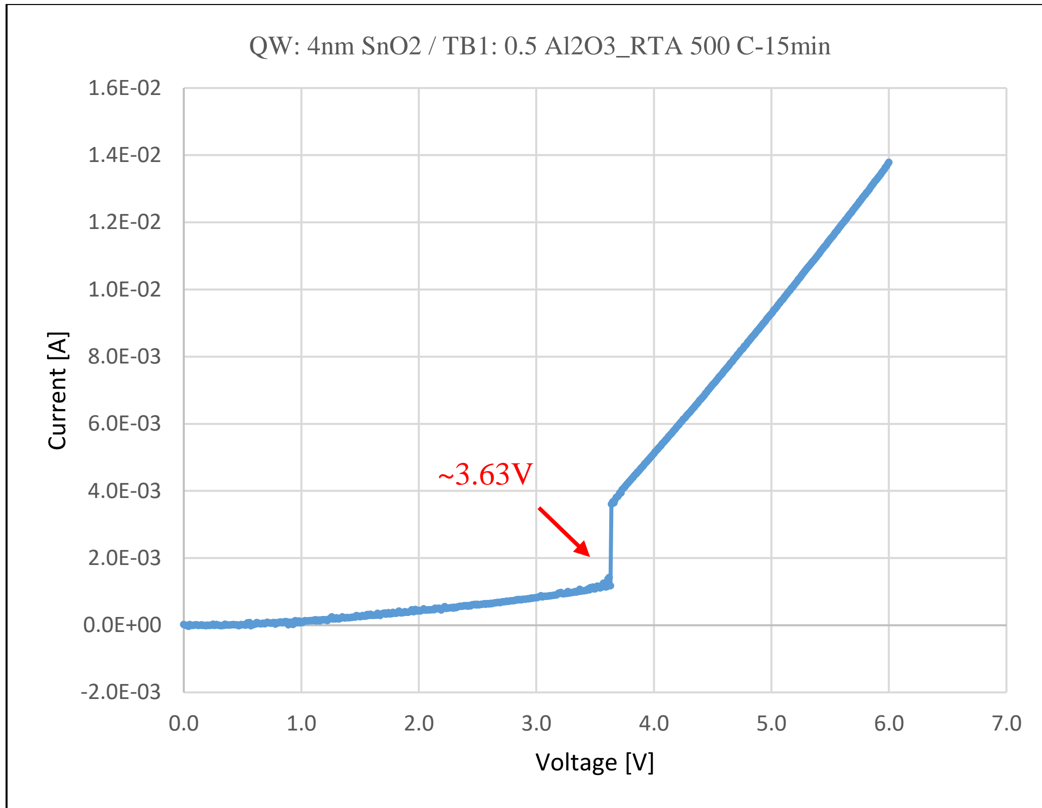


Figure 57: Source-Silicon IV for device with Native SiO2 / QW: 4nm SnO2 / 0.5nm Al2O3_RTA 500C-15min

The discrete energy levels for the 4nm and 3nm SnO_2 may be at a different energy level than the 5 nm SnO_2 quantum well layer and thus there is no abrupt jump visible at this positive voltage for the 3nm and 4nm. Increasing the positive bias further will align the silicon conduction band with the discrete energy level of the 4nm SnO_2 quantum well layer showing an abrupt current jump at 3.63V(Fig. 56) for 4nm sample. The zoomed-in plot for the 4nm samples shows a very sharp current jump at a resolution of 0.1mV voltage step size. This sharp current jump is observed as a narrow differential conductance peak in the differential conductance vs voltage plot. The differential conductance plot shows a narrow dI/dV peak of 0.1mV full-width half-maxima. The relation FWHM = 3.525*kT [116] is used to calculate the effective electron temperature for the 4nm sample current jump, which shows that the FWHM of 0.1mV corresponds to an effective electron temperature of 0.33

Kelvin, thus achieving cold-electron injection to silicon at room temperature for thew 4 nm SnO2 quantum well device. The 3 nm SnO_2 sample has its discrete energy level at an even lower energy than the 5 nm and 4 nm samples. Thus, an even higher bias is required to align the silicon conduction energy band with the discrete energy level of the 3nm SnO_2 quantum well layer.

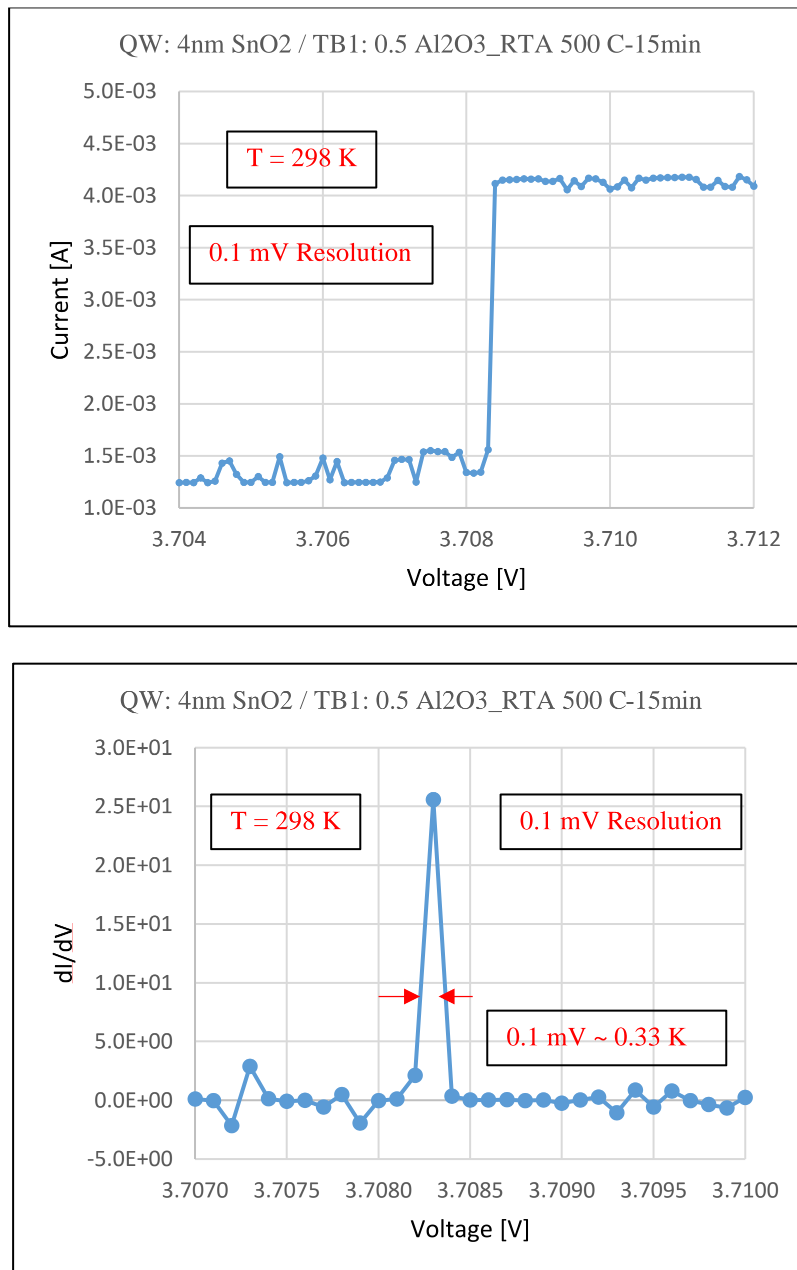


Figure 58: Differential Conductance vs Voltage for device with Native SiO2 / QW: 4nm SnO2 / 0.5nm Al2O3_RTA 500C-15min

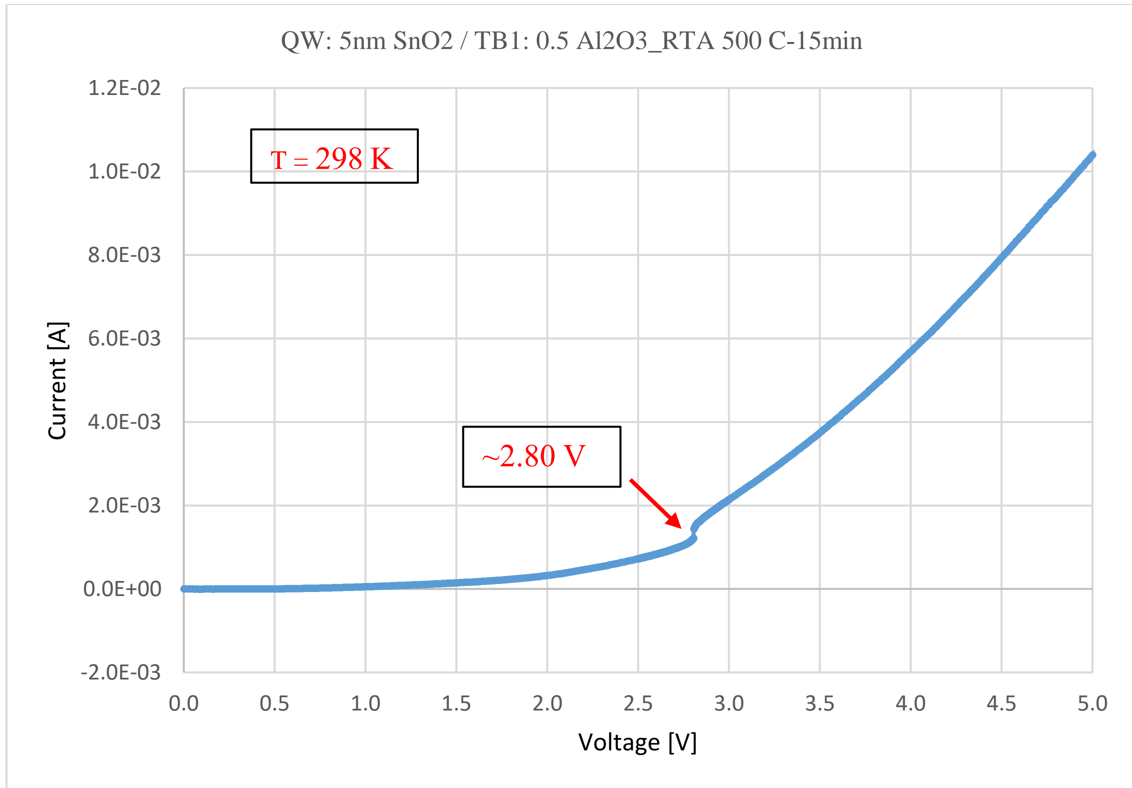


Figure 59: Source-Silicon IV for device with Native SiO2 / QW: 5nm SnO2 / 0.5nm Al2O3_RTA 500C-15min

When the discrete energy level of the quantum well is aligned with the silicon conduction energy band, there is an abrupt current jump at 4.54 V (Fig. 54) for the 3nm SnO_2 quantum well sample. The zoomed-in plot for the 3nm device shows a very sharp current jump with a resolution of 0.05 mV voltage step size. A very narrow differential conductance peak is observed at the location of the abrupt current jump in the differential conductance vs voltage graph. The Full-width half-maxima for the differential conductance peak for the 3nm samples was measured to be 0.05 mV. The relation FWHM=3.525*kT[116], is used to calculate the effective electron temperature of the 3nm sample. The FWHM of 0.05 mV corresponds to an effective electron temperature of 0.16 Kelvin, achieving cold-electron injection to silicon at room temperature.

It is observed that there is a shift in the abrupt current jump voltage with variation in the quantum well thickness. The required bias for cold-electron injection to silicon at room temperature increases with increase in the quantum well layer thickness.

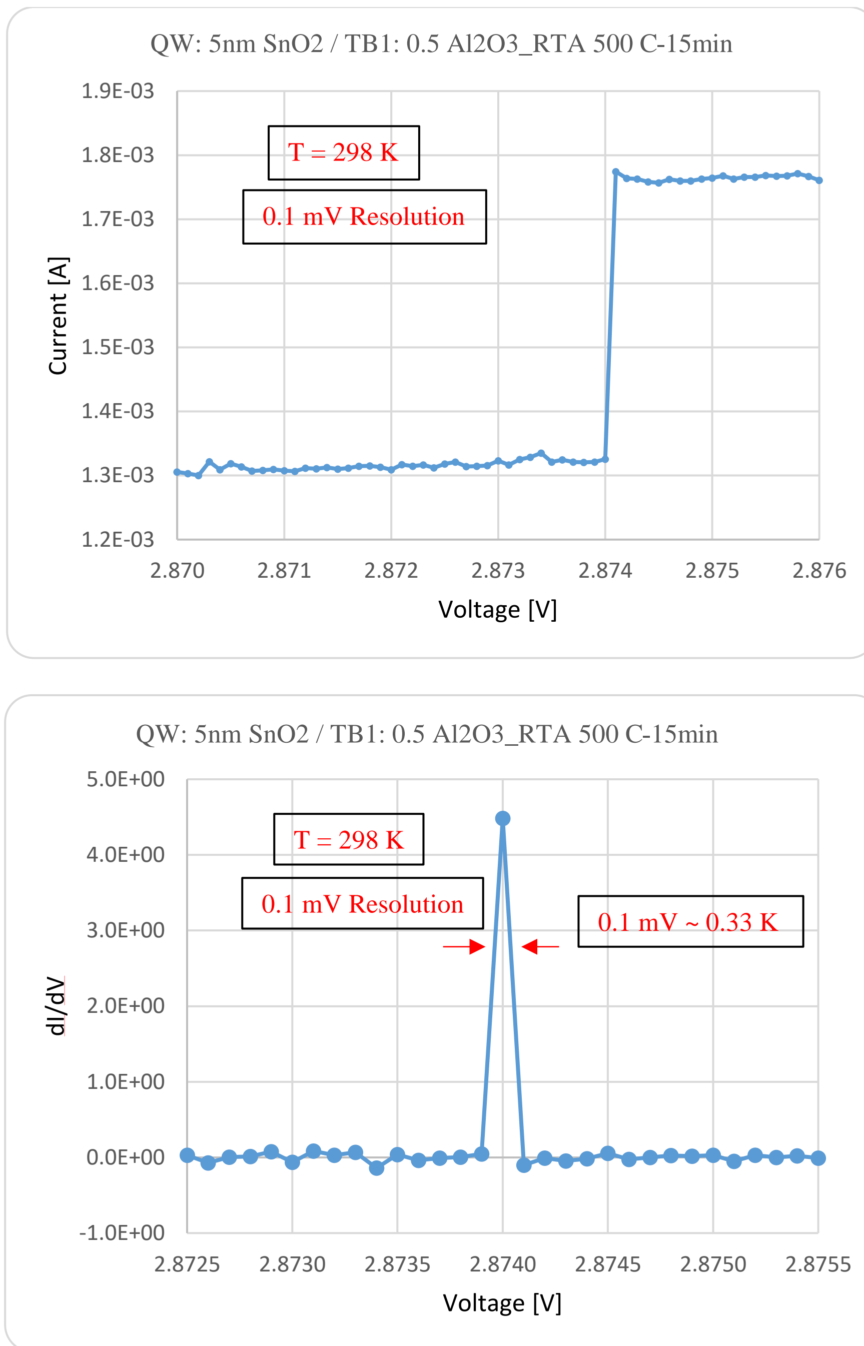
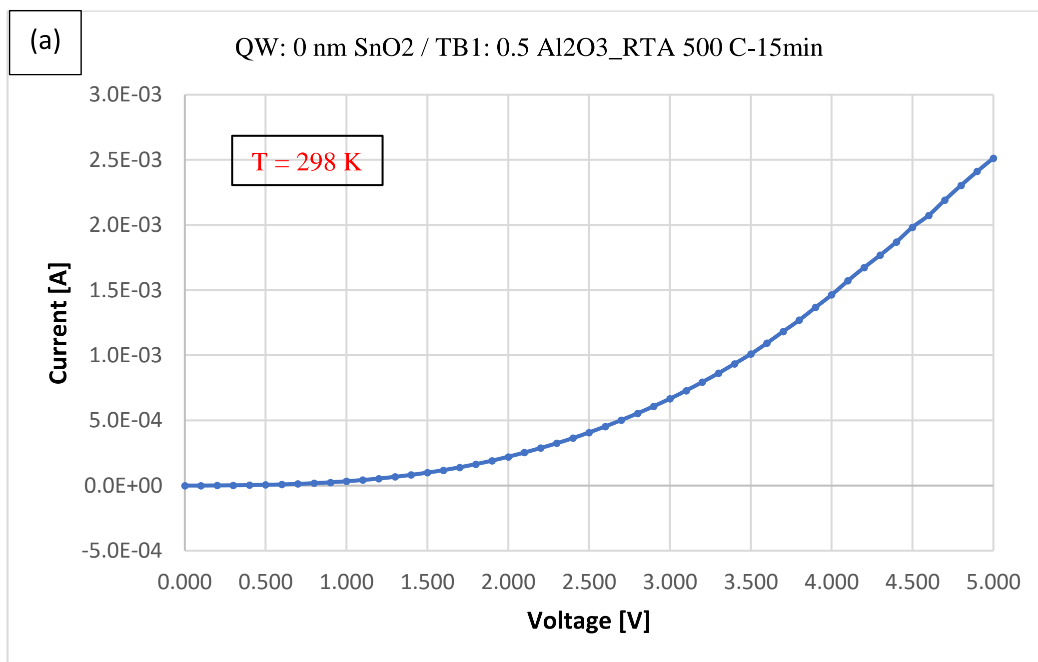
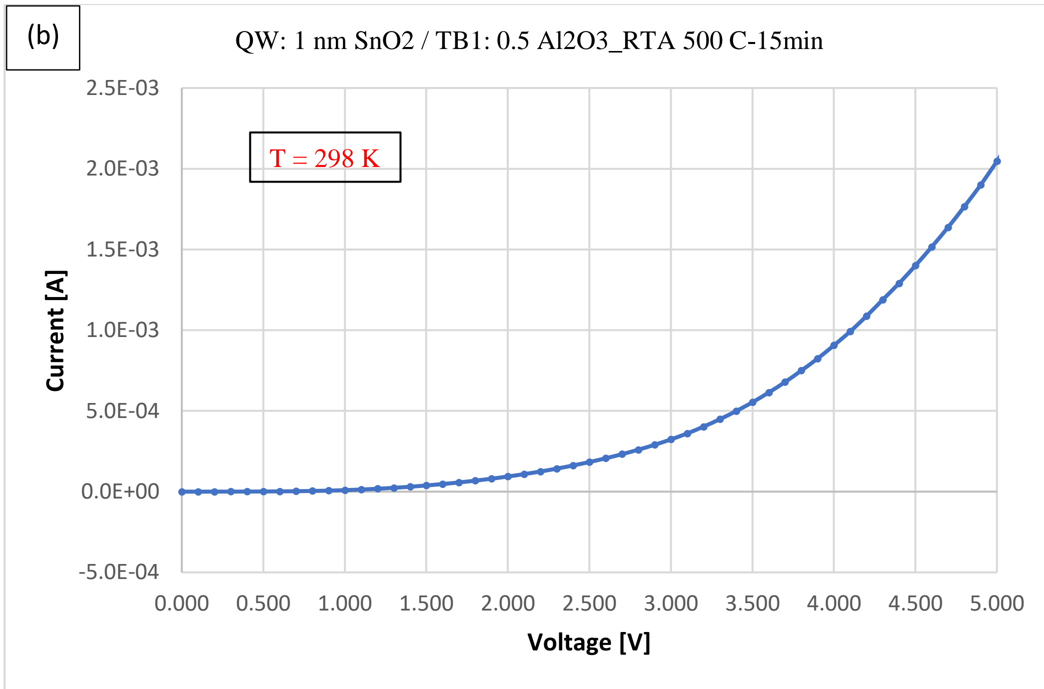


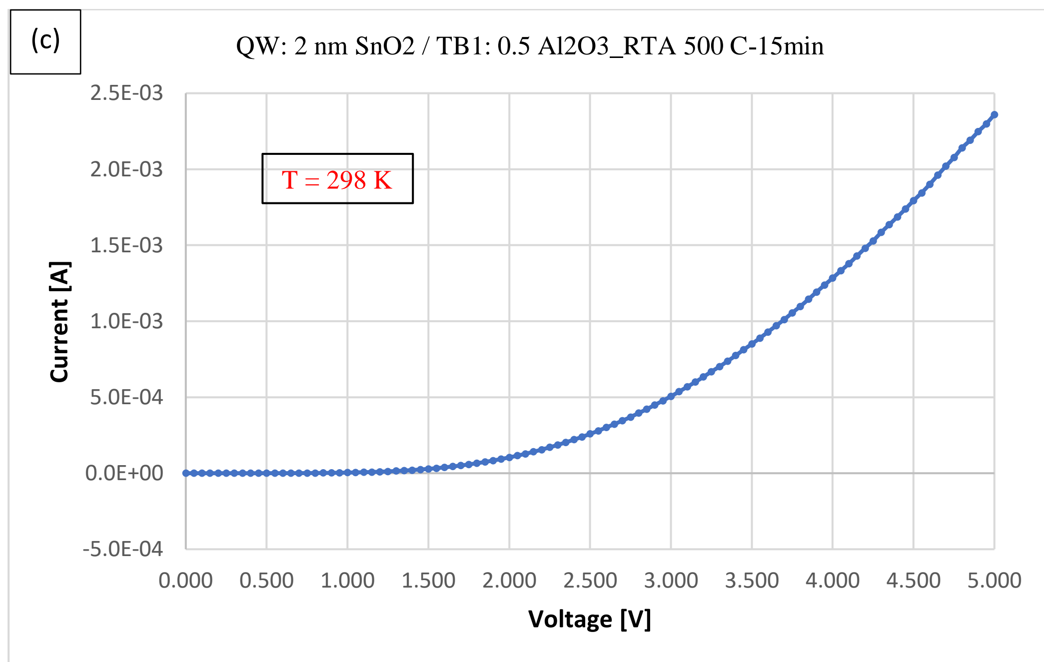
Figure 60: Differential Conductance vs Voltage for device with Native SiO2 / QW: 5nm SnO2 / 0.5nm Al2O3_RTA 500C-15min

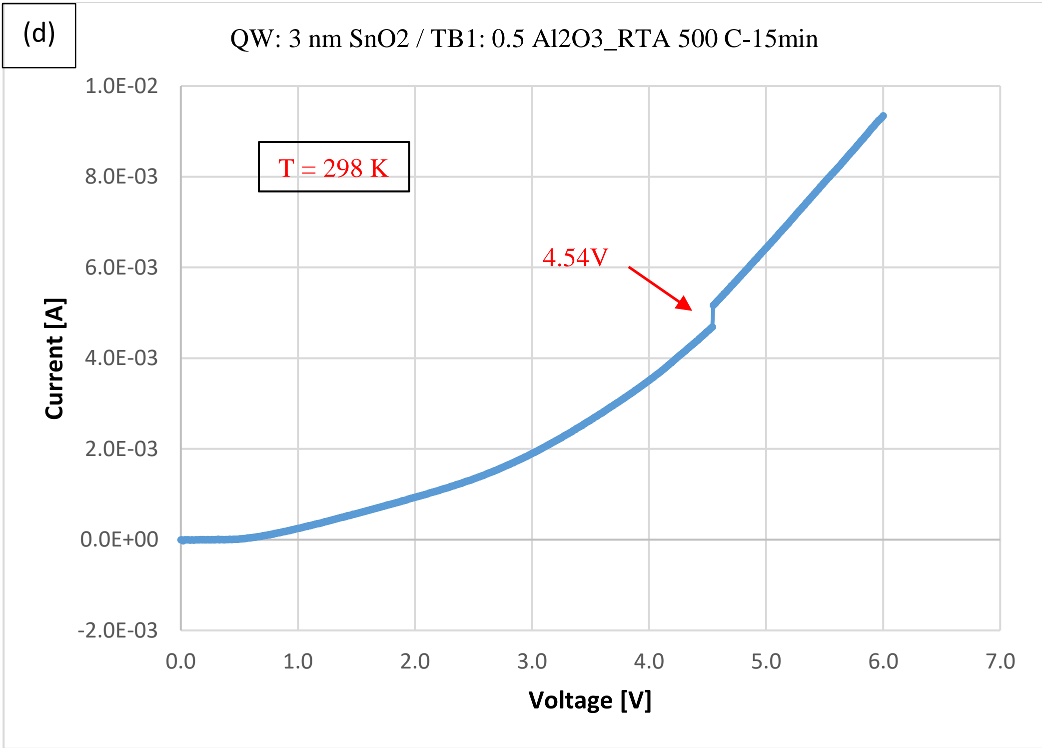
If the abrupt current jump observed was due to a breakdown through the thin films, we would see an increase in the abrupt current jump voltage with an increase in the quantum well thickness. A thinner film will require a lower bias to breakdown. However, the trend we see here, that is, the increase in the required bias for the abrupt current jump with a

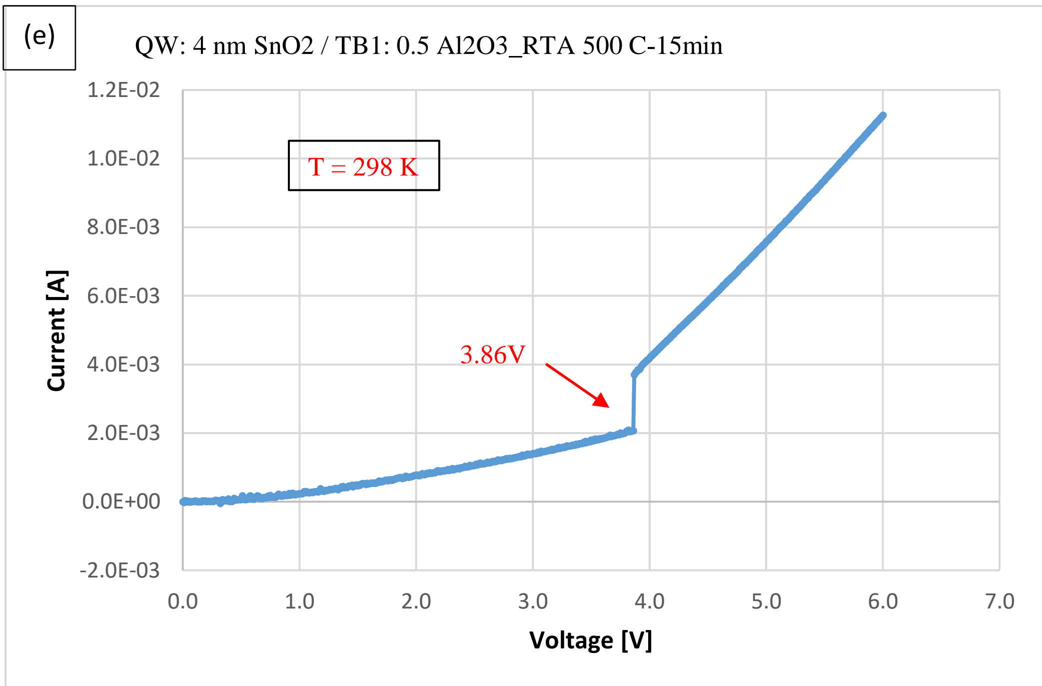
decrease in the quantum well thickness is the exact opposite of what would happen in the case of a breakdown. This is an indication that the abrupt current jumps observed are not a result of breakdown but are formed when the quantum well discrete energy level is aligned with the conduction energy band of silicon. Another batch of samples was fabricated to verify this trend. Different samples with varying quantum well thickness was fabricated with the following layers stack: 50nm Chromium / 0.5nm ALD deposited Aluminium oxide / Sputtered SnO2 film as quantum well layer (0nm, 1nm, 2nm, 3nm, 4nm, 5nm) / Native silicon dioxide (~1.5nm) / Silicon substrate / 200nm Aluminium Metal contact. The devices source-silicon IV was measured as shown in Fig. 60.




(b)
QW: 1 nm SnO2 / TB1: 0.5 Al2O3_RTA 500 C-15min
T = 298 K
Current [A]
2.5E-03
2.0E-03
1.5E-03
1.0E-03
5.0E-04
0.0E+00
-5.0E-04
0.000
0.500
1.000
1.500
2.000
2.500
3.000
3.500
4.000
4.500
5.000
Voltage [V]


(c)
QW: 2 nm SnO2 / TB1: 0.5 Al2O3_RTA 500 C-15min
T = 298 K
Current [A]
2.5E-03
2.0E-03
1.5E-03
1.0E-03
5.0E-04
0.0E+00
-5.0E-04
0.000
0.500
1.000
1.500
2.000
2.500
3.000
3.500
4.000
4.500
5.000
Voltage [V]


(d)
QW: 3 nm SnO2 / TB1: 0.5 Al2O3_RTA 500 C-15min
T = 298 K
4.54V
Current [A]
1.0E-02
8.0E-03
6.0E-03
4.0E-03
2.0E-03
0.0E+00
-2.0E-03
0.0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
Voltage [V]


(e)
QW: 4 nm SnO2 / TB1: 0.5 Al2O3_RTA 500 C-15min
T = 298 K
3.86V
Current [A]
1.2E-02
1.0E-02
8.0E-03
6.0E-03
4.0E-03
2.0E-03
0.0E+00
-2.0E-03
0.0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
Voltage [V]

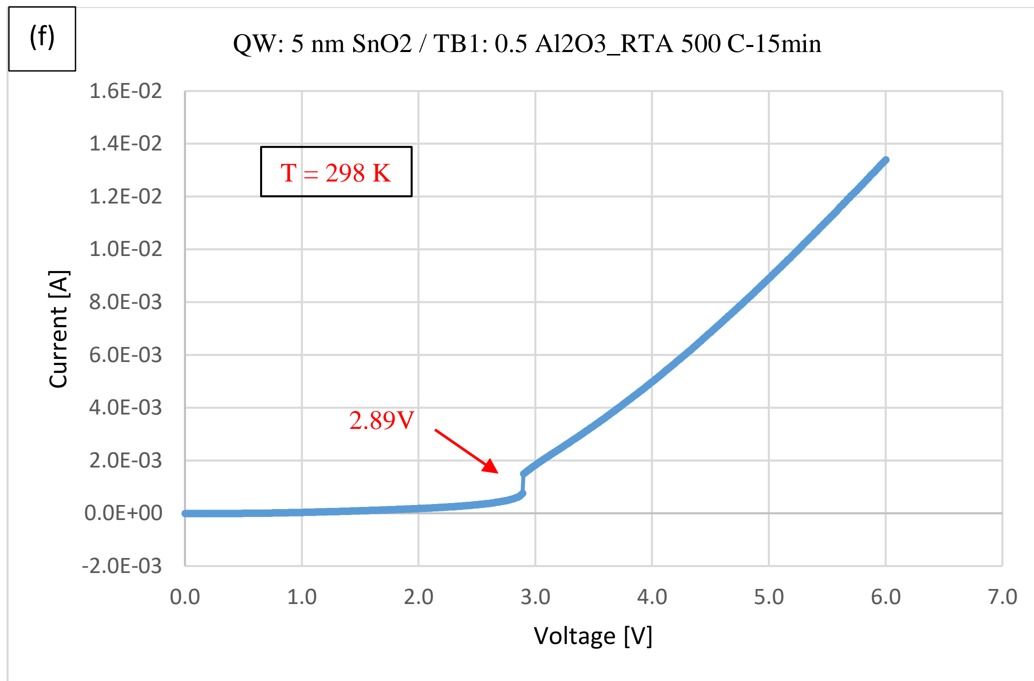


Figure 61: Source-Silicon IV for devices with QW thickness (a) 0nm, (b) 1nm, (c) 2nm, (d) 3nm, (e) 4nm, (f) 5nm

The devices with no quantum well layer, 1nm SnO2 quantum well layer and 2nm SnO2 quantum well layer is measured. There was no abrupt current jump observed. This may be due to the deposited film thickness being too thin. There are a few possible reasons for there to be no abrupt current jump indicating a cold-electron transport. First, the film is too thin, which could have allowed the electrons from the source to directly tunnel through to the silicon conduction band thus there was no current jump observed. Another reason could be that the sputtered SnO2 film is so thin that it may have caused defects to form like pin holes through which the source electrons are able to reach the silicon conduction band, leading to no cold-electron transport observed. The samples with 3nm, 4nm and 5nm SnO2 quantum well thicknesses showed abrupt current jumps at different voltages indicating cold-electron injection to silicon. It is observed that with the increase in quantum well layer thickness, the voltage required to observe the abrupt current jump becomes lowered. Another trend noticed here is the high current observed before the abrupt current jump. The

3nm SnO2 quantum well device shows an increasing current before the jump voltage. The increasing current slope before and after the jump voltage is almost identical. The 4nm SnO2 quantum well device also has an increasing current before the abrupt current jump voltage, but the magnitude of the current before the jump is lower than the 3nm SnO2 device.

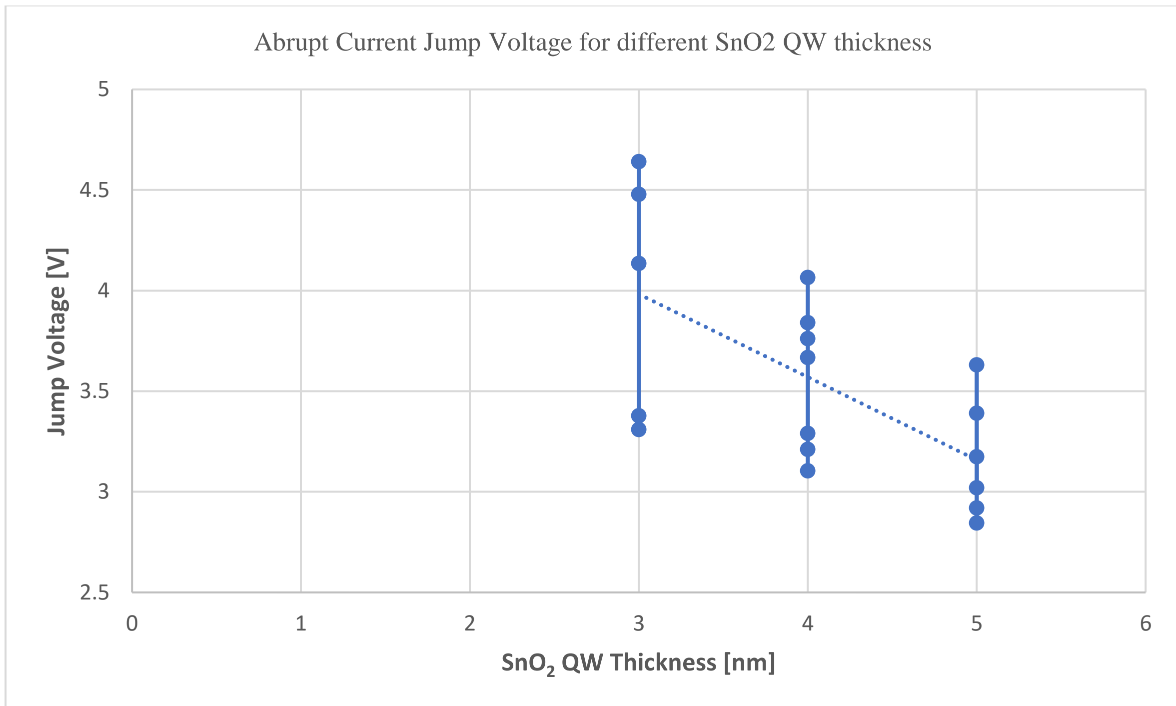


Figure 62: Abrupt Current Jumps Voltage variation with different SnO2 QW thickness

Also, the current slope before the jump voltage is low and after the jump the slope is increased. For the 5nm SnO2 device, the current before the jump voltage is very low and only after the abrupt current jump occurs, the current starts increasing. This trend observed may be because, with the increase in the SnO2 quantum well thickness deposited using Sputtering, any defects present in the film are covered up and the current through the defect energy levels no longer contribute to the source-silicon current. Figure 62 plots the voltages at which the abrupt current jumps were observed against the SnO_2 quantum well thickness. We see a trend here. The sharp current jump voltage seems to be decreasing with increase

in the quantum well layer thickness. This may be because, a higher quantum well layer thickness changes the quantum well discrete energy levels placements and their separation, which in turn would require a different bias to be applied to move the silicon conduction band to the appropriate discrete energy level and align perfectly. This decrease in current jump voltage with an increase in the quantum well layer thickness indicates the cold-electron injection is the reason for the abrupt current jump. The trend would have been the exact opposite if the current jump observed was due to breakdown (thinner films breakdown at a lower voltage bias).

Another observation can be made here from figure 61, (d) 3nm SnO2, (e) 4nm SnO2, (f) 5nm SnO2 IV plots. The graphs for the 3nm SnO2 device shows a high current before the abrupt current jump (cold-electron transport) occurs. The 4nm SnO2 device also shows a high current, but lower in magnitude than the 3nm SnO2 deivce. The 5 nm SnO2 device however, shows a much lower current before the abrupt current jump is observed. The source-silicon current observed before the abrupt current jump has a decreasing magnitude with an increase in the quantum well layer thickness. The high current observed in these devices may be attributed to current flow due to tunneling or due to defect states present in the thin film layers during deposition. The correct source of the high current can be identified by measuring the devices in a low temperature system. The low temperature measurement should lower the source-silicon current before the abrupt current jump if the high current was caused due to the defect states in the thin quantum well layer. Whereas the high current before the abrupt current jump will remain the same if the high current was due to tunneling through the thin films.

Chapter 5: Conclusion

Suppression of thermally excited electrons was demonstrated at room temperature without external cooling. This was done by using an energy filtering stack which consisted of a quantum well layer bounded by tunneling barriers on both ends. The energy filtering stack (tunneling barriers and quantum well layer) was sandwiched between the source electrode and the silicon substrate. The quantum well discrete energy level was used to filter out thermally excited electrons. Using this device architecture, we demonstrated cold-electron injection to silicon with an effective electron temperature of ~0.08 Kelvin. The I-V measurements showed abrupt current jumps and their differential conductance plots showed extremely narrow peaks, with FWHM of 0.025 mV. This Full-Width at Half-Maxima of the differential conductance peak corresponded to an effective electron temperature of 0.08 Kelvin. The abrupt current jumps were stable and showed that sub-1 Kelvin cold-electron injection to silicon is achieved at room temperature. The energy filtering approach has a potential to be utilized in realizing extremely energy efficient transistors with subthreshold slopes of much less than 60 mV/decade at room temperature.

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